Compal confidential

Schematics Document

Mobile Yonah uFCPGA with Intel

Calistoga_P/GM+ATI M52-T + ICH7-M core logic

2006-04-28

REV:1.0

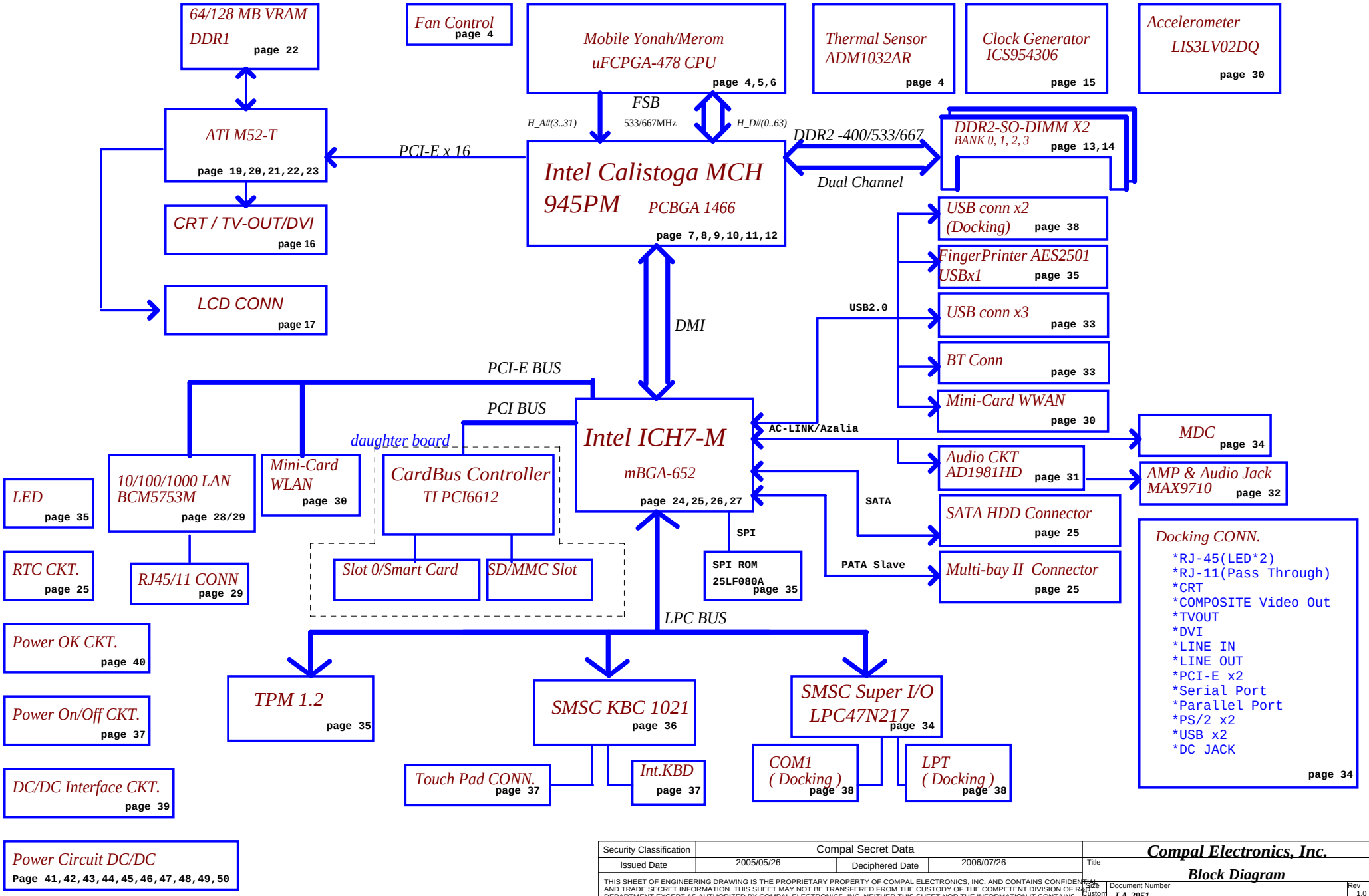
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.		
Title: *Cover Sheet*		
Size: Custom	Document Number: *LA-2951*	Rev: 1.0
Date: Friday, April 28, 2006	Sheet 1 of 54	

Compal confidential

File Name : LA-2951P

Caymus



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: Block Diagram			
Size: Custom	Document Number: LA-2951		Rev: 1.0
Date: Friday, April 28, 2006	Sheet 2 of 54		

Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (18.5V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH/ICH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_VCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Internal PCI Devices

DEVICE	Bus	PCI Device ID	IDSEL #
LAN	1	D8	AD24
Azalia	0	D27	AD11
PCI-E	0	D28	AD12
USB1.1/2.0	0	D29	AD13
PCI to PCI (DMI to PCI)	0	D30	AD14
AC97 MODEM	0	D30	AD14
AC97 Audio	0	D30	AD14
PATA/SATA	0	D31	AD15
LPC I/F	0	D31	AD15
SMBUS	0	D31	AD15
CPU I/F	0	D31	AD15
DMA	0	D31	AD15
PMU	0	D31	AD15

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
CARD BUS	D6	AD22	2	C D E G

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
M52@ : means build discrete sku with ATI VGA M52 .
UMA@ : means build UMA sku with Intel 945GM .

SPI@ : means just build when SPI I/F BIOS function reserve.
FWH@ : means just build when FWH I/F BIOS function reserve.
NOXDP@ : means just build when XDP function disable.
XDP@ : means just build when XDP function enable. When this time, docking PCI express will not work.

1021@ : means just build when SMsC KBC1021 chip selected.
LP@ : means just build when Low power clock gen. install
NOLP@ : means just build when Low power clock gen. NO install

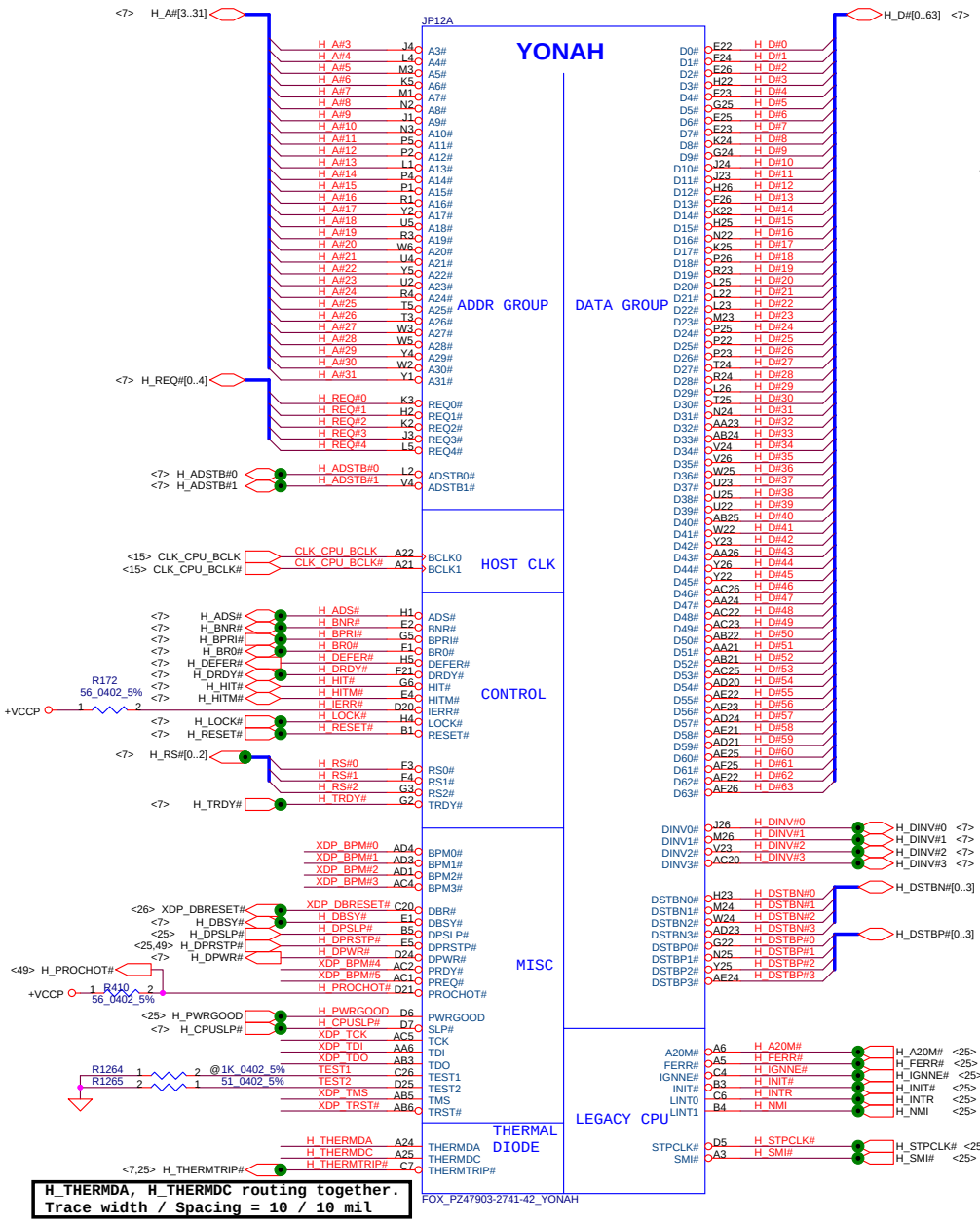
45@ : means need be mounted when 45 level assy or rework stage.

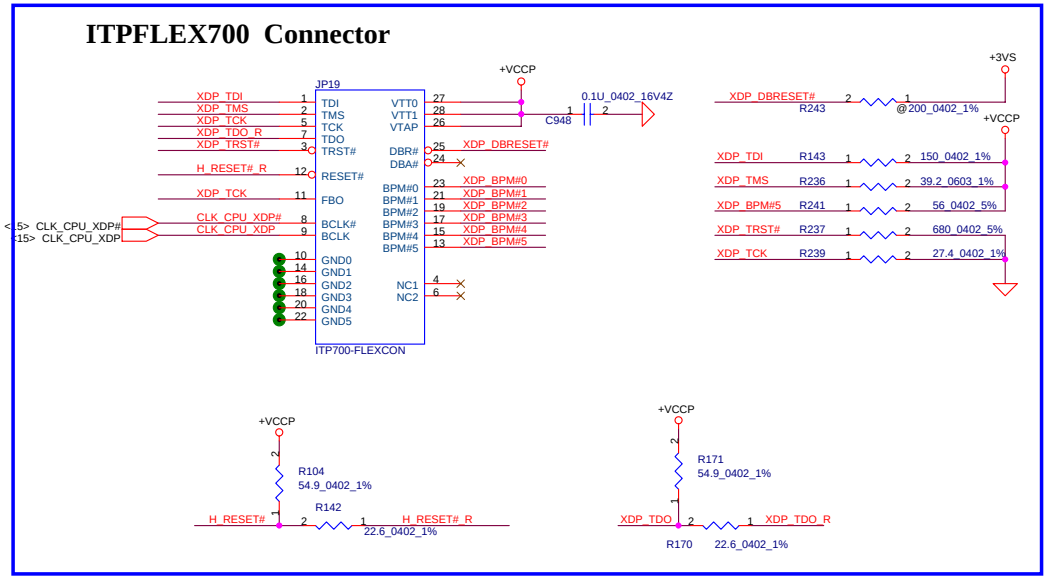
Compal Electronics, Inc.

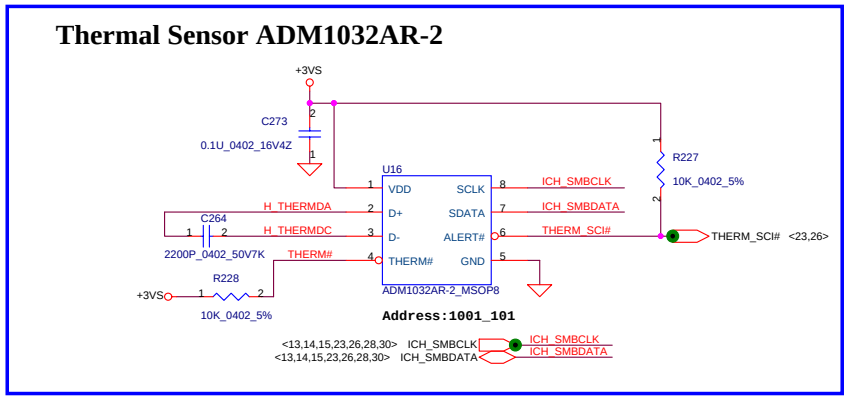
Title: Notes List

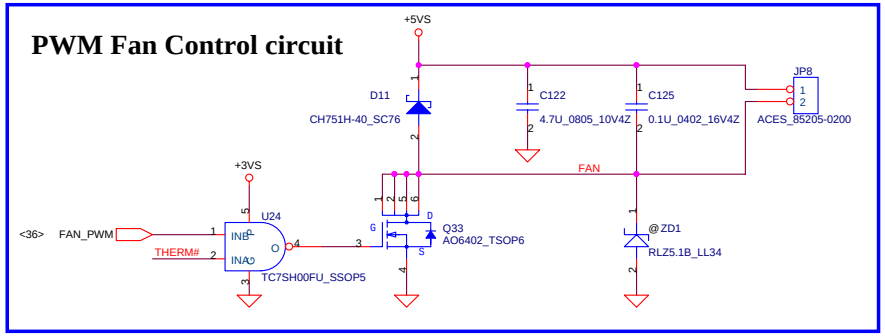
Size: C | Document Number: LA-2951 | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 3 of 54









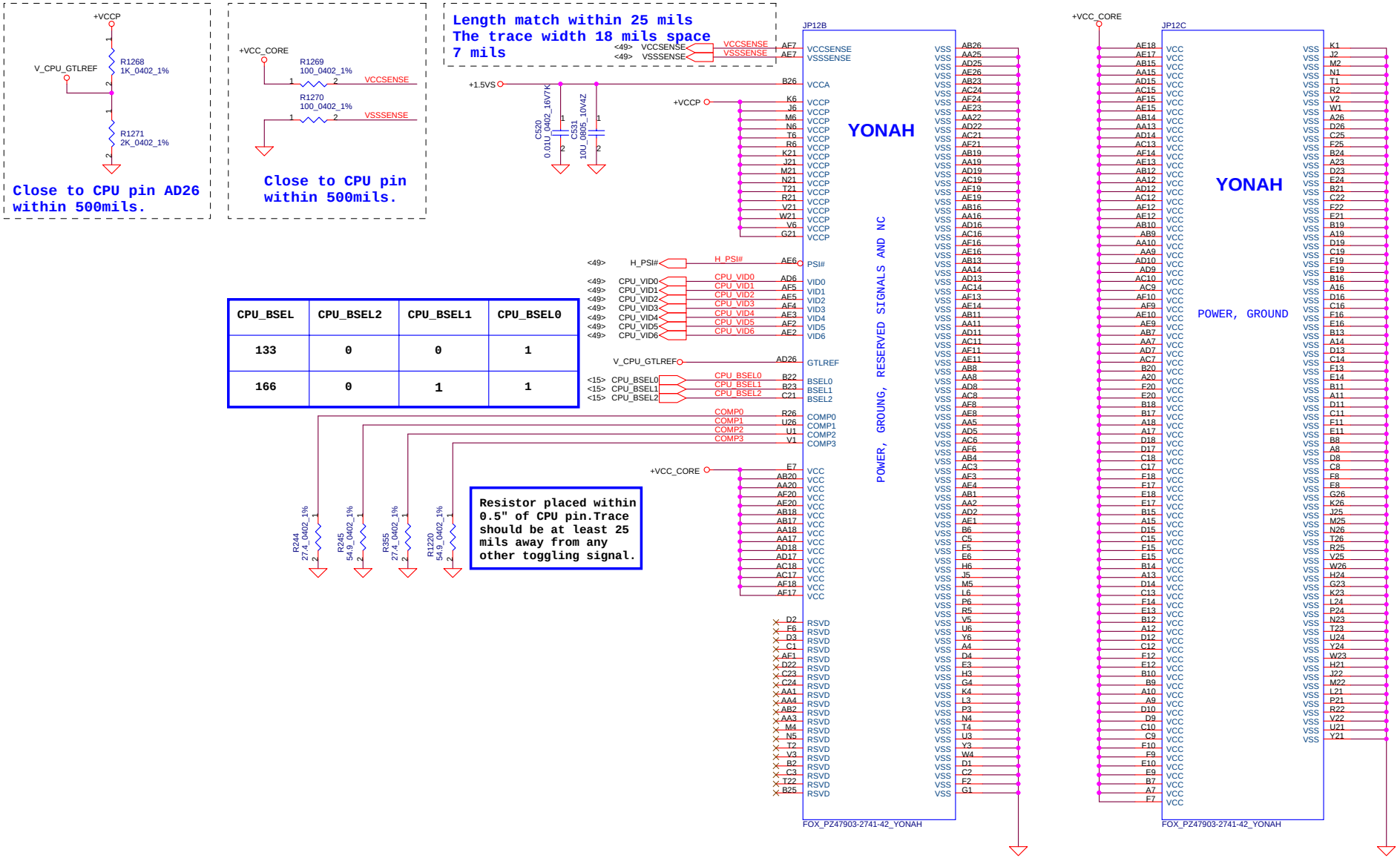
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: Yonah CPU in mFCPGA479

Size: Document Number: LA-2951 Rev: 1.0

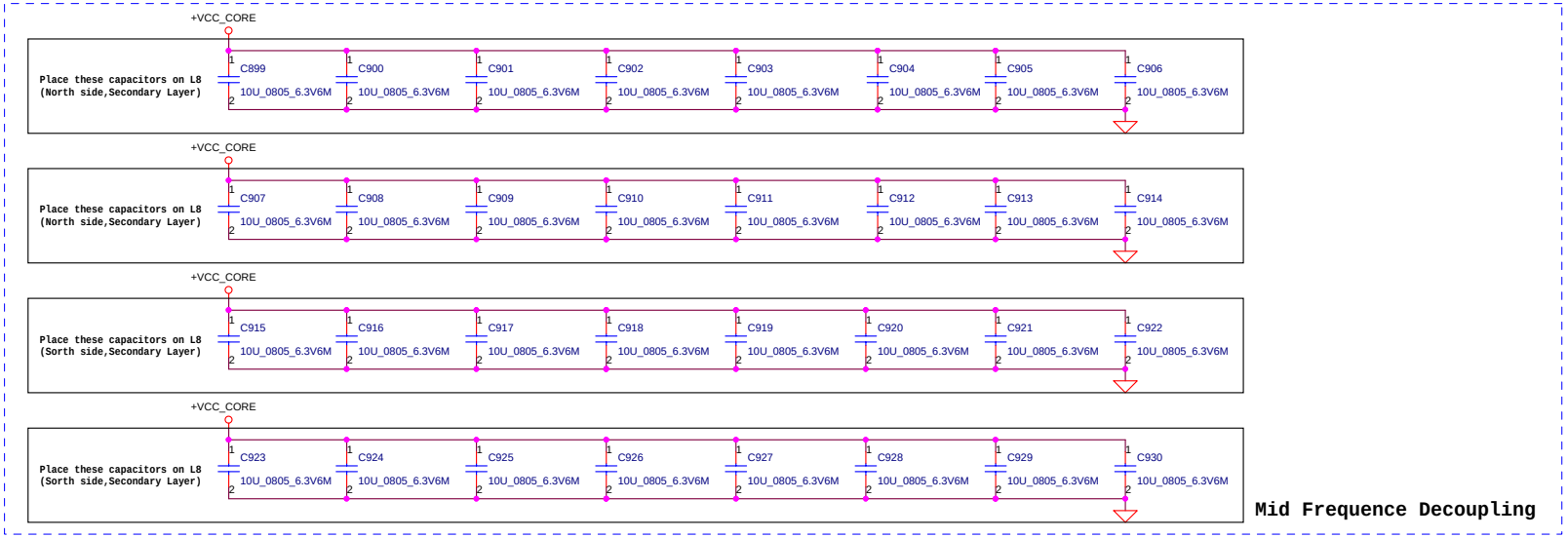
Date: Friday, April 28, 2006 Sheet 4 of 54

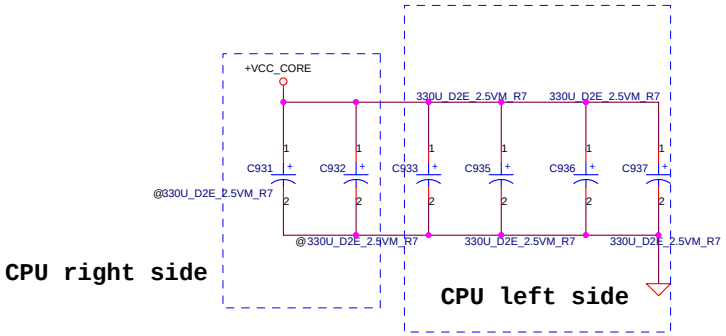


CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

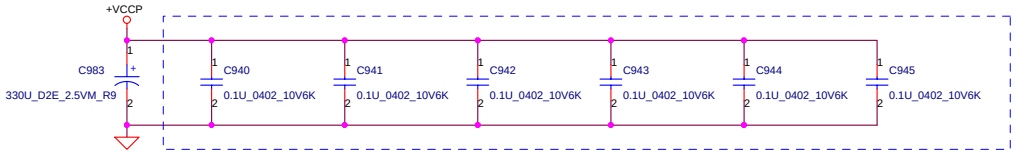
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: Yonah CPU in mFCPGA479			
Size:	Document Number: LA-2951		Rev: 1.0
Date: Friday, April 28, 2006	Sheet 5 of 54		





ESR <= 1.5m ohm
Capacitor > 1980uF



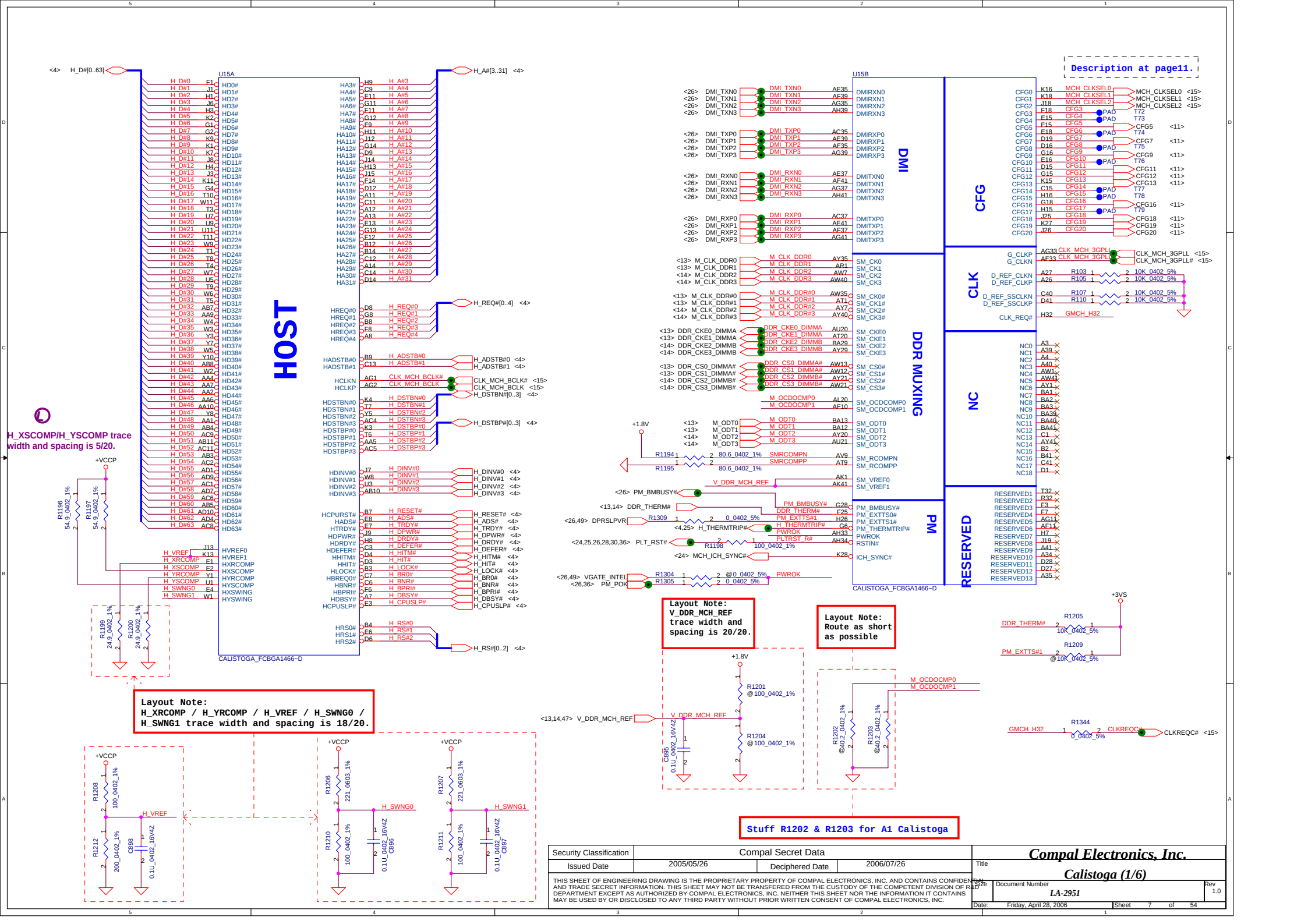
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

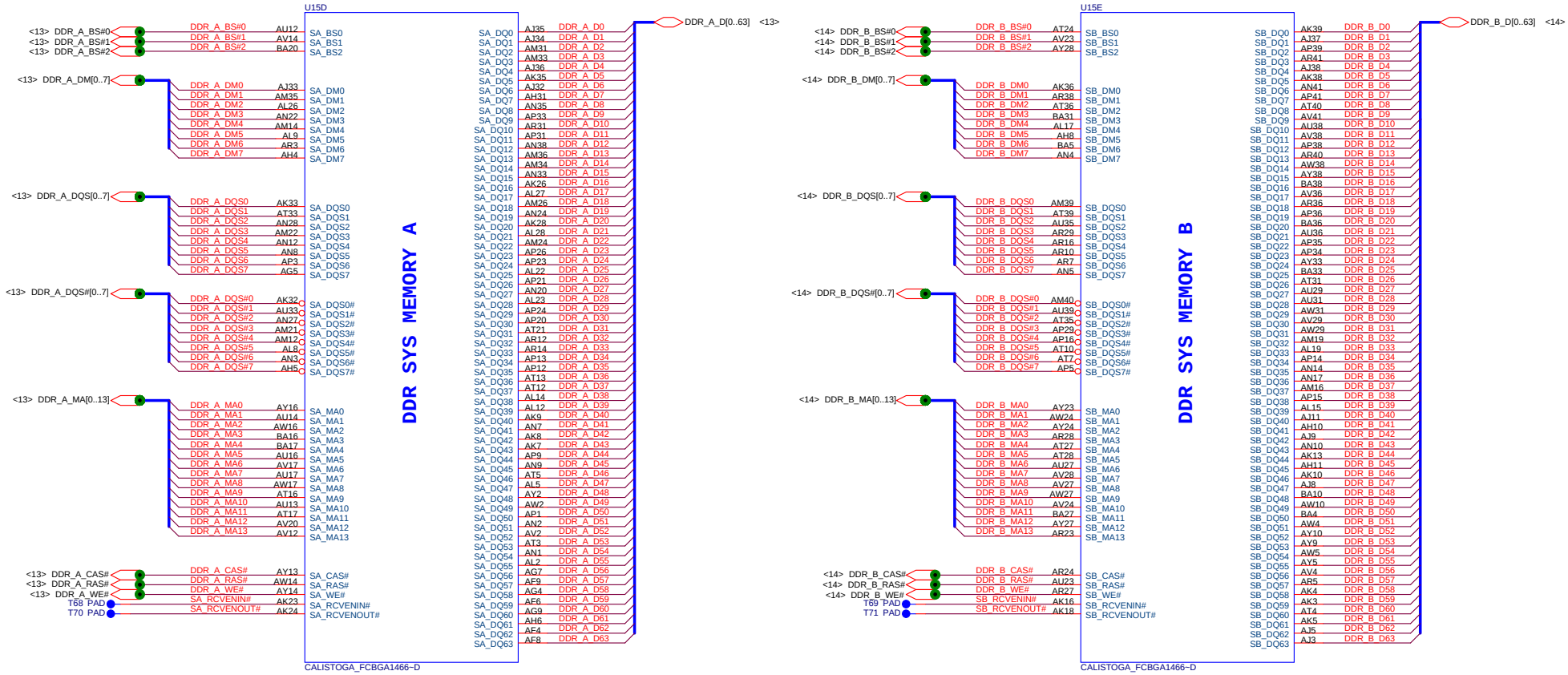
Compal Electronics, Inc.

Title: **CPU Bypass capacitors**

Size: | Document Number: **LA-2951** | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 6 of 54


Description at page11.
HOST
U15A
CALISTOGA_FCBGA1466-D
U15B
CALISTOGA_FCBGA1466-D
DMI
DDR MUXING
CFG
CLK
NC
RESERVED
PM
H_XSCOMP/H_YSCOMP trace width and spacing is 5/20.
Layout Note: H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 18/20.
Layout Note: V_DDR_MCH_REF trace width and spacing is 20/20.
Layout Note: Route as short as possible
Stuff R1202 & R1203 for A1 Calistoga
Security Classification
Compal Secret Data
Issued Date
2005/05/26
Deciphered Date
2006/07/26
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
Calistoga (1/6)
Size
Document Number
LA-2951
Rev
1.0
Date: Friday, April 28, 2006
Sheet 7 of 54



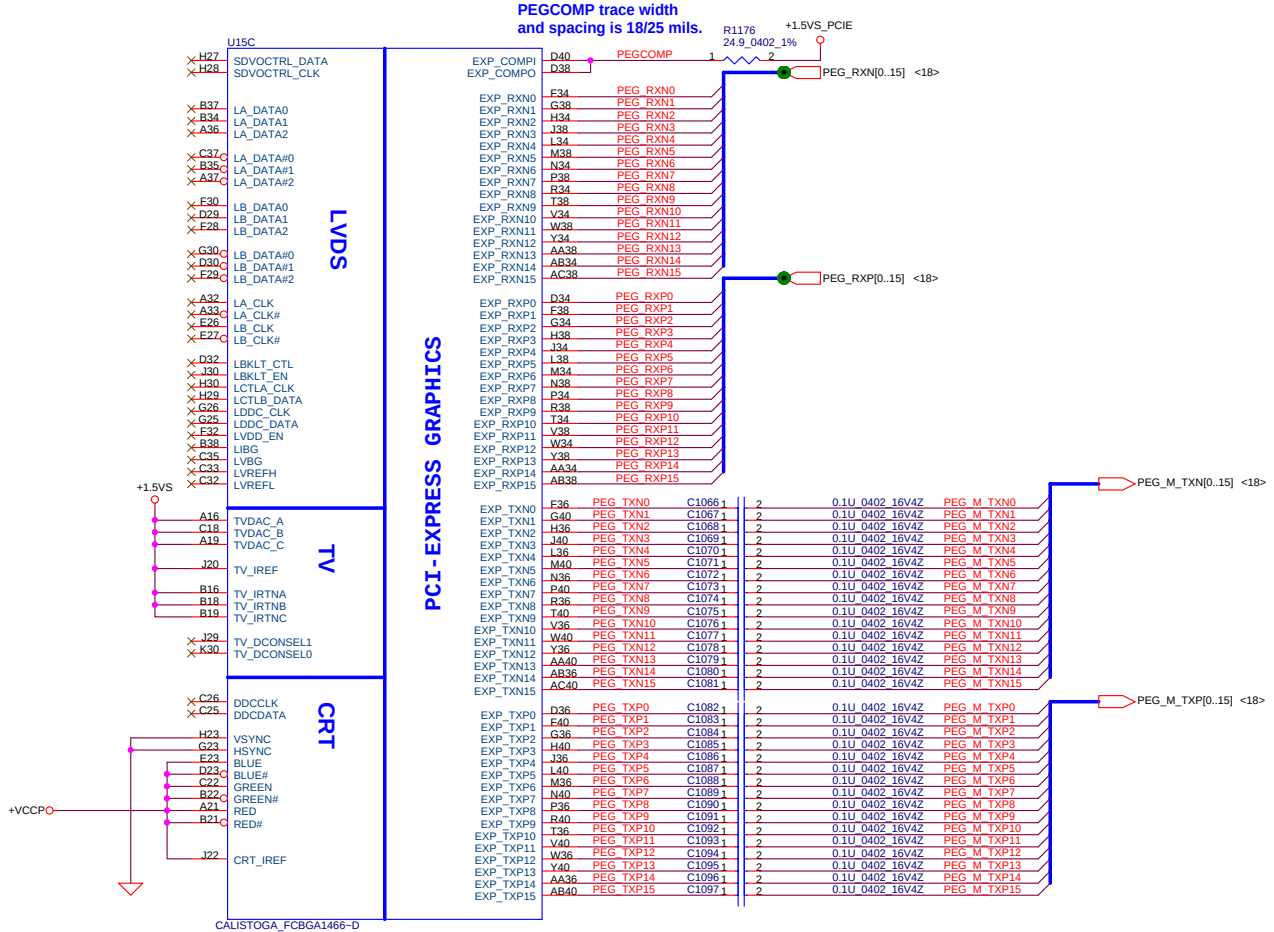
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **Calistoga (2/6)**

Size	Document Number	Rev
	LA-2951	1.0

Date: Friday, April 28, 2006 | Sheet 8 of 54



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: Calistoga (3/6)			
Size:	Document Number: LA-2951		Rev: 1.0
Date: Friday, April 28, 2006	Sheet 9 of 54		

Place close to Pin G41

W=40 mils

P O W E R

PCI-E/MEM/PSB PLL decoupling

45mA Max.

45mA Max.

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: **Calistoga (4/6)**

Size | Document Number: **LA-2951** | Rev: 1.0

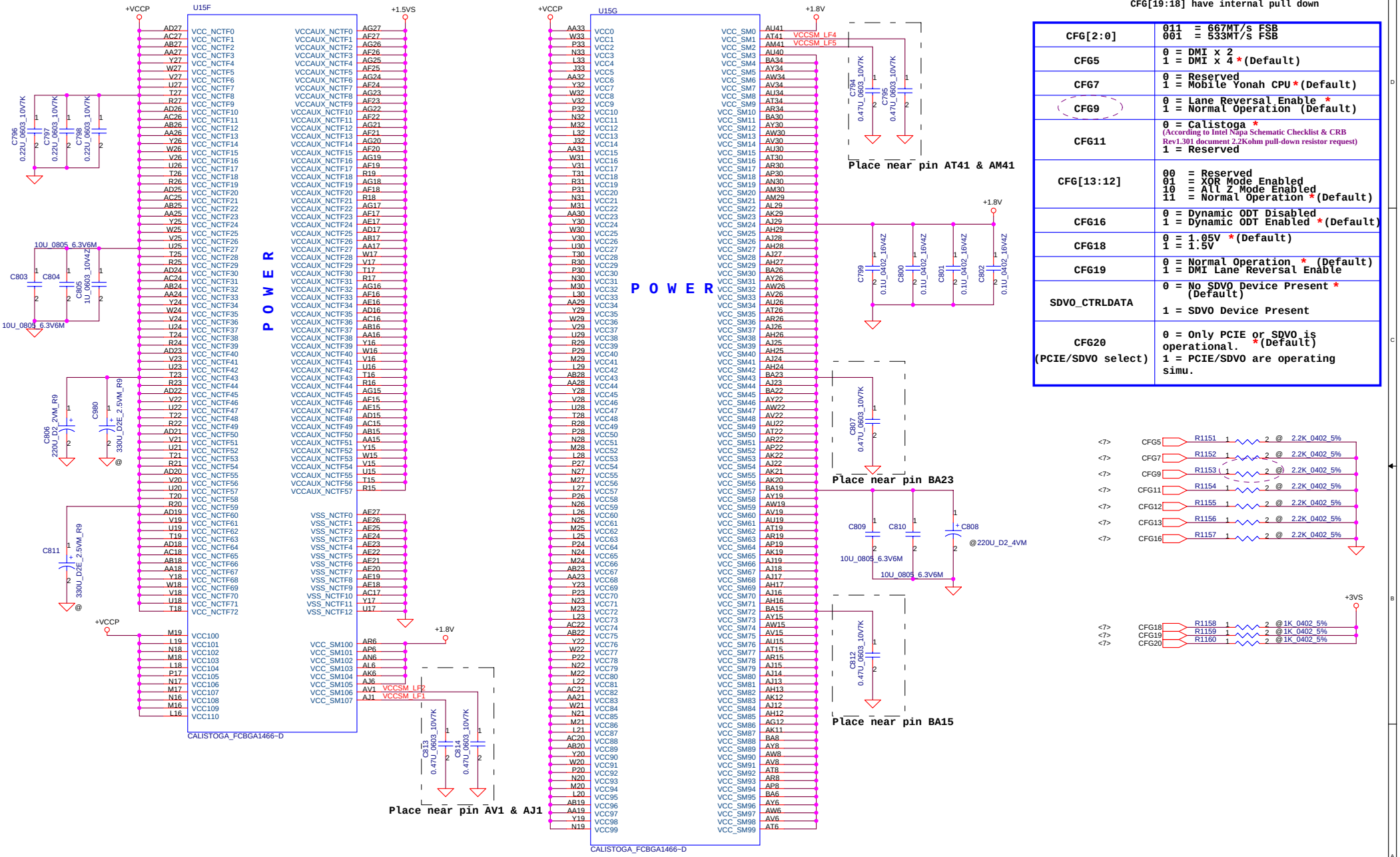
Date: Friday, April 28, 2006 | Sheet 10 of 54

Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable * 1 = Normal Operation (Default)
CFG11	0 = Calistoga * (According to Intel Napa Schematic Checklist & CRB Rev1.301 document 2.2Kohm pull-down resistor request) 1 = Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

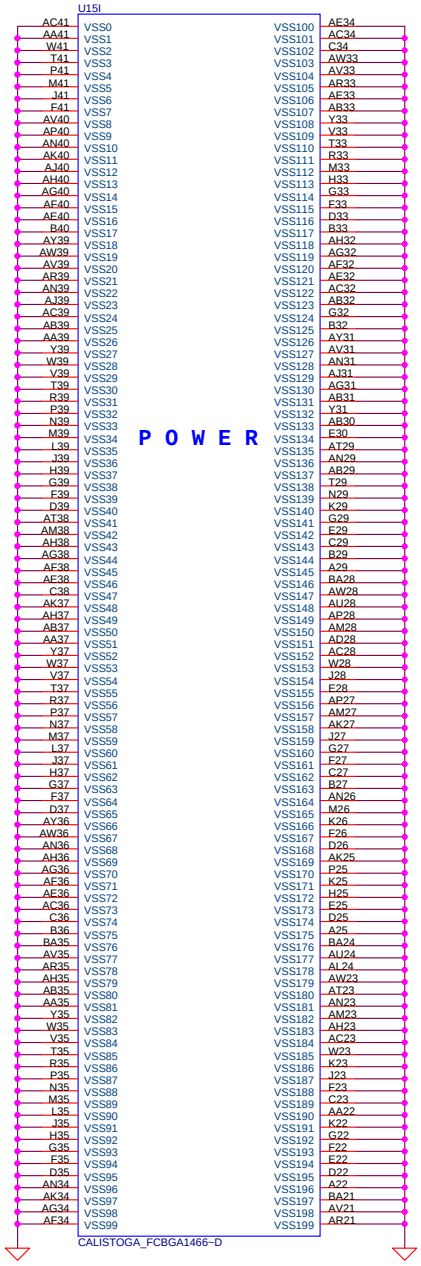
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: Calistoga (5/6)

Size: Document Number: LA-2951 Rev: 1.0

Date: Friday, April 28, 2006 Sheet 11 of 54



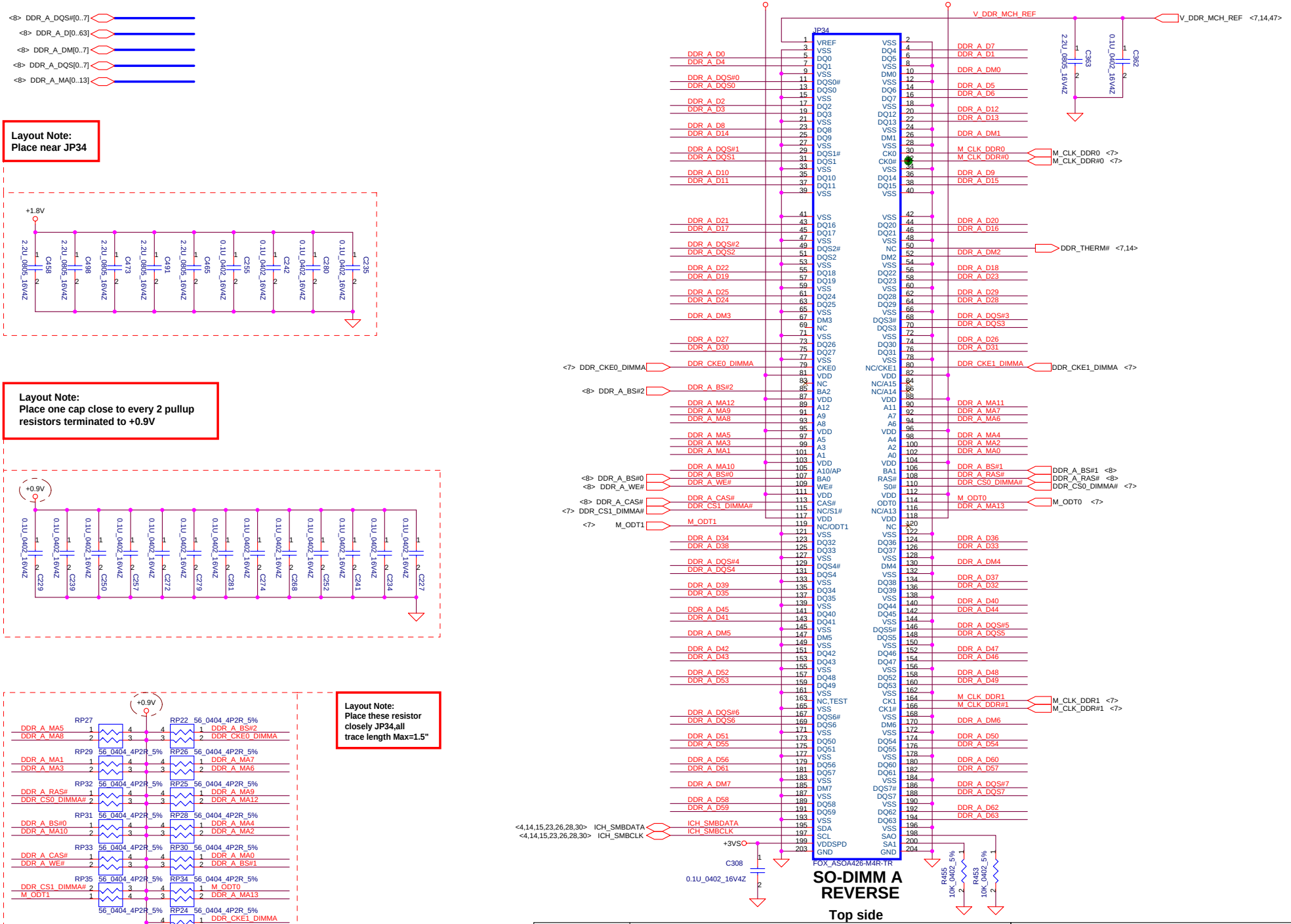
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **Calistoga (6/6)**

Size	Document Number	Rev
	LA-2951	1.0

Date: Friday, April 28, 2006 Sheet 12 of 54



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT1

Size: Document Number: LA-2951 Rev: 1.0

Date: Friday, April 28, 2006 Sheet 13 of 54

<8> DDR_B_DQS#[0..7]
<8> DDR_B_D[0..63]
<8> DDR_B_DM[0..7]
<8> DDR_B_DQS[0..7]
<8> DDR_B_MA[0..13]

Layout Note:
Place near JP34

+1.8V

2.2U_0805_16V4Z C236, C265, C247, C159, C164, C166
0.1U_0402_16V4Z C219, C188, C161

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

+0.9V

0.1U_0402_16V4Z C176, C179, C196, C197, C213, C220, C183, C210, C199, C173, C218, C163, C177

+0.9V

RP14 56_0404_4P2R_5%: DDR_B_MA1, DDR_B_MA3 / DDR_B_MA9, DDR_B_MA12
RP17 56_0404_4P2R_5%: DDR_B_BS#0, DDR_B_MA10 / DDR_CKE3_DIMMB, DDR_B_MA11
RP16 56_0404_4P2R_5%: DDR_B_MA0, DDR_B_BS#1 / DDR_B_MA5, DDR_B_MA8
RP18 56_0404_4P2R_5%: DDR_B_RAS#, DDR_CS2_DIMMB# / DDR_B_MA7, DDR_B_MA6
RP19 56_0404_4P2R_5%: DDR_B_CAS#, DDR_B_WE# / DDR_B_MA4, DDR_B_MA2
RP23 56_0404_4P2R_5%: DDR_CS3_DIMMB#, M_ODT3 / M_ODT2, DDR_B_MA13
RP10 56_0404_4P2R_5%
RP11 56_0404_4P2R_5%
RP12 56_0404_4P2R_5%
RP13 56_0404_4P2R_5%
RP15 56_0404_4P2R_5%
RP21 56_0404_4P2R_5%
RP9 56_0404_4P2R_5%: DDR_B_BS#2, DDR_CKE2_DIMMB

Layout Note:
Place these resistor closely JP10,all trace length Max=1.5"

+1.8V, +1.8V
V_DDR_MCH_REF → V_DDR_MCH_REF <7,13,47>
2.2U_0805_16V4Z C89, 0.1U_0402_16V4Z C90

JP10 — FOX_ASOA426-M2RN-7F

	VREF		VSS
DDR_B_D0	DQ0	DDR_B_D4	DQ4
DDR_B_D5	DQ1	DDR_B_D1	DQ5
	VSS		VSS
DDR_B_DQS#0	DQS0#	DDR_B_DM0	DM0
DDR_B_DQS0	DQS0		VSS
	VSS	DDR_B_D6	DQ6
DDR_B_D7	DQ2	DDR_B_D2	DQ7
DDR_B_D3	DQ3		VSS
	VSS	DDR_B_D12	DQ12
DDR_B_D8	DQ8	DDR_B_D13	DQ13
DDR_B_D9	DQ9		VSS
	VSS	DDR_B_DM1	DM1
DDR_B_DQS#1	DQS1#		VSS
DDR_B_DQS1	DQS1	M_CLK_DDR3	CK0
	VSS	M_CLK_DDR#3	CK0#
DDR_B_D10	DQ10		VSS
DDR_B_D11	DQ11	DDR_B_D14	DQ14
	VSS	DDR_B_D15	DQ15
			VSS
	VSS		VSS
DDR_B_D21	DQ16	DDR_B_D16	DQ20
DDR_B_D20	DQ17	DDR_B_D18	DQ21
	VSS		VSS
DDR_B_DQS#2	DQS2#	DDR_THERM# <7,13>	NC
DDR_B_DQS2	DQS2	DDR_B_DM2	DM2
	VSS		VSS
DDR_B_D22	DQ18	DDR_B_D17	DQ22
DDR_B_D23	DQ19	DDR_B_D19	DQ23
	VSS		VSS
DDR_B_D24	DQ24	DDR_B_D26	DQ28
DDR_B_D25	DQ25	DDR_B_D28	DQ29
	VSS		VSS
DDR_B_DM3	DM3	DDR_B_DQS#3	DQS3#
	NC	DDR_B_DQS3	DQS3
	VSS		VSS
DDR_B_D30	DQ26	DDR_B_D29	DQ30
DDR_B_D31	DQ27	DDR_B_D27	DQ31
	VSS		VSS
<7> DDR_CKE2_DIMMB	CKE0	DDR_CKE3_DIMMB	NC/CKE1
	VDD	DDR_CKE3_DIMMB <7>	VDD
	NC		NC/A15
<8> DDR_B_BS#2	BA2		NC/A14
	VDD	DDR_B_MA11	VDD
DDR_B_MA12	A12	DDR_B_MA7	A11
DDR_B_MA9	A9	DDR_B_MA6	A7
DDR_B_MA8	A8		A6
	VDD		VDD
DDR_B_MA5	A5	DDR_B_MA4	A4
DDR_B_MA3	A3	DDR_B_MA2	A2
DDR_B_MA1	A1	DDR_B_MA0	A0
	VDD		VDD
DDR_B_MA10	A10/AP	DDR_B_BS#1	BA1
<8> DDR_B_BS#0	BA0	DDR_B_RAS# <8>	RAS#
<8> DDR_B_WE#	WE#	DDR_CS2_DIMMB#	S0#
	VDD		VDD
<8> DDR_B_CAS#	CAS#	M_ODT2	ODT0
<7> DDR_CS3_DIMMB#	NC/S1#	DDR_B_MA13	NC/A13
	VDD		VDD
<7> M_ODT3	NC/ODT1		NC
	VSS		VSS
DDR_B_D37	DQ32	DDR_B_D33	DQ36
DDR_B_D36	DQ33	DDR_B_D32	DQ37
	VSS		VSS
DDR_B_DQS#4	DQS4#	DDR_B_DM4	DM4
DDR_B_DQS4	DQS4		VSS
	VSS	DDR_B_D38	DQ38
DDR_B_D35	DQ34	DDR_B_D39	DQ39
DDR_B_D34	DQ35		VSS
	VSS	DDR_B_D44	DQ44
DDR_B_D40	DQ40	DDR_B_D45	DQ45
DDR_B_D41	DQ41		VSS
	VSS	DDR_B_DQS#5	DQS5#
DDR_B_DM5	DM5	DDR_B_DQS5	DQS5
	VSS		VSS
DDR_B_D42	DQ42	DDR_B_D43	DQ46
DDR_B_D47	DQ43	DDR_B_D46	DQ47
	VSS		VSS
DDR_B_D48	DQ48	DDR_B_D49	DQ52
DDR_B_D53	DQ49	DDR_B_D52	DQ53
	VSS		VSS
	NC,TEST	M_CLK_DDR2	CK1
	VSS	M_CLK_DDR#2	CK1#
DDR_B_DQS#6	DQS6#		VSS
DDR_B_DQS6	DQS6	DDR_B_DM6	DM6
	VSS		VSS
DDR_B_D51	DQ50	DDR_B_D54	DQ54
DDR_B_D50	DQ51	DDR_B_D55	DQ55
	VSS		VSS
DDR_B_D60	DQ56	DDR_B_D56	DQ60
DDR_B_D61	DQ57	DDR_B_D57	DQ61
	VSS		VSS
DDR_B_DM7	DM7	DDR_B_DQS#7	DQS7#
	VSS	DDR_B_DQS7	DQS7
DDR_B_D58	DQ58		VSS
DDR_B_D59	DQ59	DDR_B_D62	DQ62
	VSS	DDR_B_D63	DQ63
<4,13,15,23,26,28,30> ICH_SMBDATA	SDA		VSS
<4,13,15,23,26,28,30> ICH_SMBCLK	SCL		SA0
+3VS	VDDSPD		SA1
	GND		GND

R257 10K_0402_5% +3VS
R254 10K_0402_5%
C301 0.1U_0402_16V4Z

SO-DIMM B
STANDARD
Bottom side

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.
Title: DDRII-SODIMM SLOT2
Size: Document Number: LA-2951 Rev: 1.0
Date: Friday, April 28, 2006 Sheet 14 of 54

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

FSB Frequency Selet:

CPU Driven *(Default)	Stuff	CLK_Ra CLK_Rb CLK_Rc
	No Stuff	CLK_Rd CLK_Re CLK_Rf
533MHz	Stuff	CLK_Rd CLK_Re CLK_Rf
	No Stuff	CLK_Ra CLK_Rb CLK_Rc
667MHz	Stuff	CLK_Rd CLK_Rf
	No Stuff	CLK_Ra CLK_Rb CLK_Rc CLK_Re

Place close to U25

Place crystal within 500 mils of CK410

Routing the trace at least 10mil

U25 ICS9LP306_TSSOP64

* Internal Pull-Up Resistor
** Internal Pull-Down Resistor

NOXDP@ : means just build when XDP function disable.

XDP@ : means just build when XDP function enable. When this time, docking PCI express will not work.

LCD(Low)/SRC(High) clock select

*High:Pin18/19 = 100MHz
Low:Pin18/19 = 96MHz

Pin44/45 function select

High:Pin44/45 = CLKREQ
*Low:Pin44/45 = CPUCLK2_ITP

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

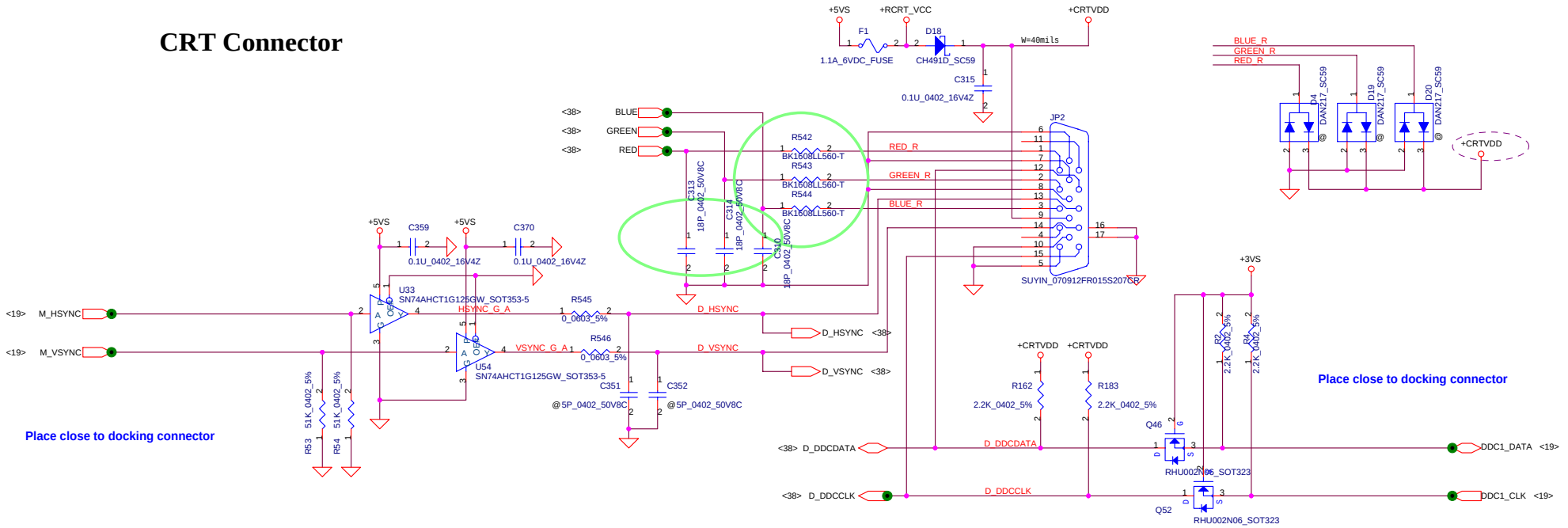
Compal Electronics, Inc.

Title: Clock generator

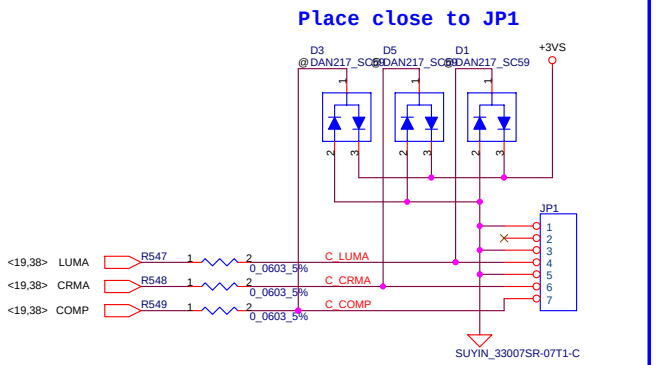
Size: Document Number: LA-2951 Rev: 1.0

Date: Friday, April 28, 2006 Sheet 15 of 54

CRT Connector



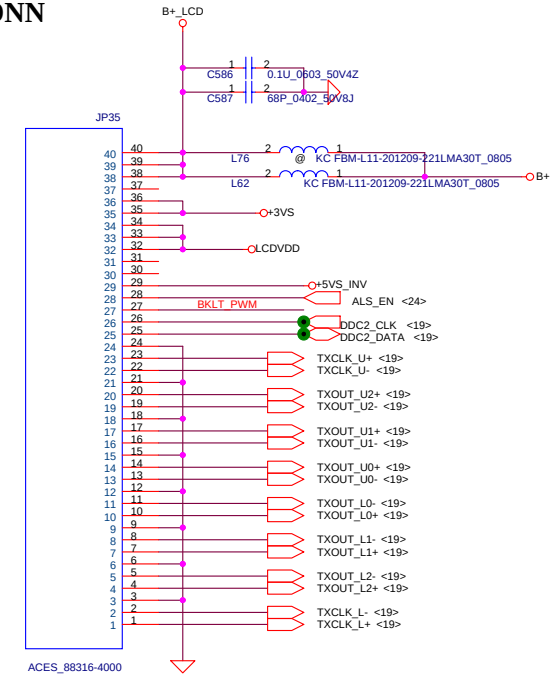
TV-Out Connector



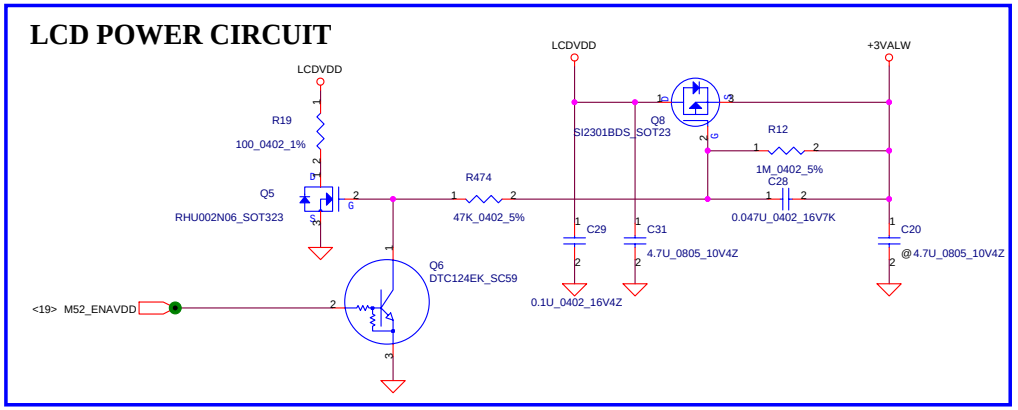
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

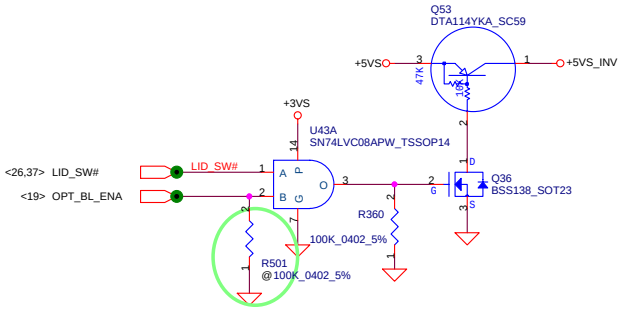
Compal Electronics, Inc.	
Title	CRT & TVout Connector
Size	Document Number: LA-2951
Rev	1.0
Date:	Friday, April 28, 2006
Sheet	16 of 54

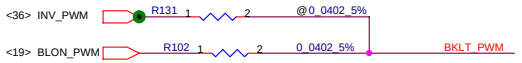
LVDS CONN



LCD POWER CIRCUIT



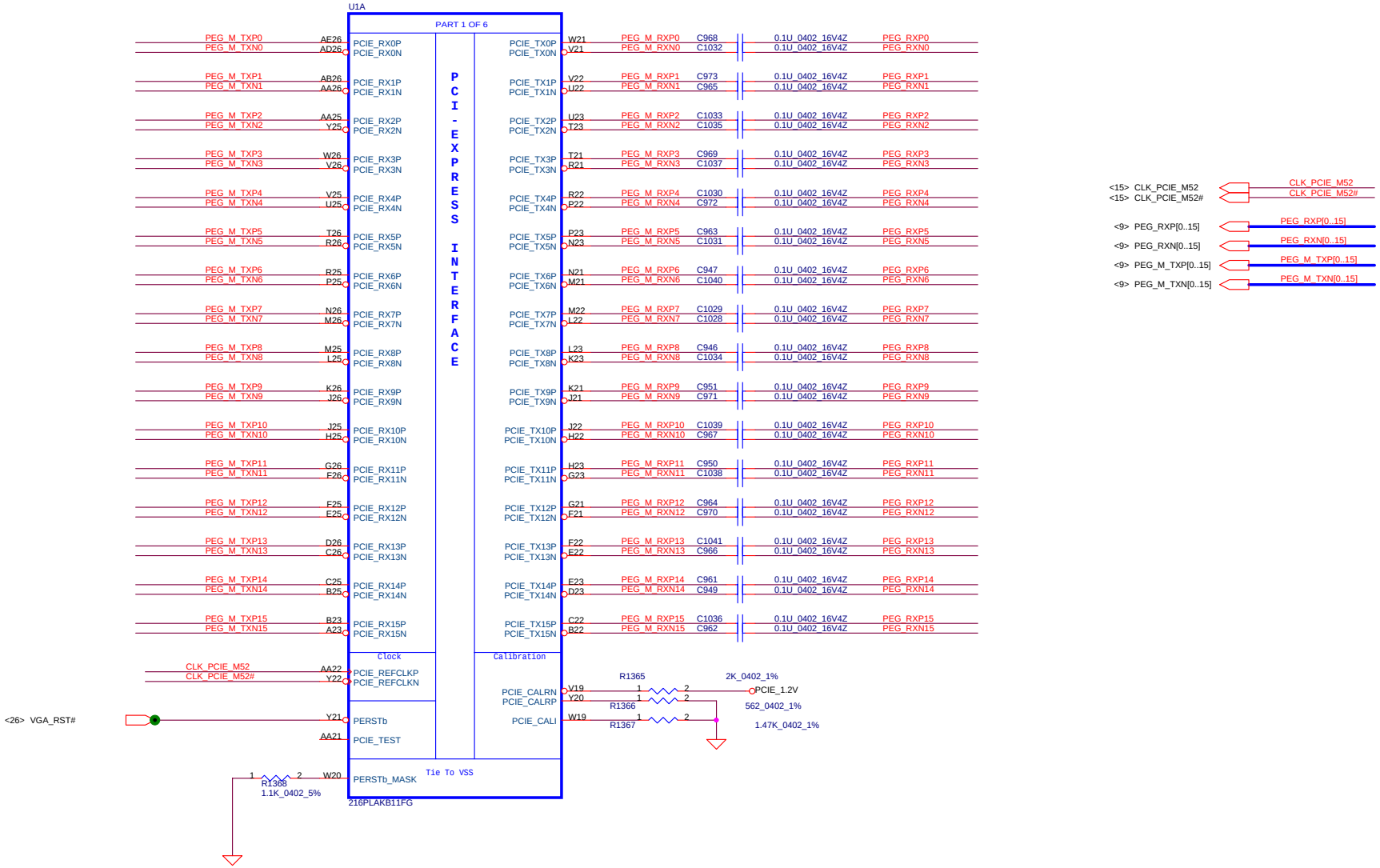




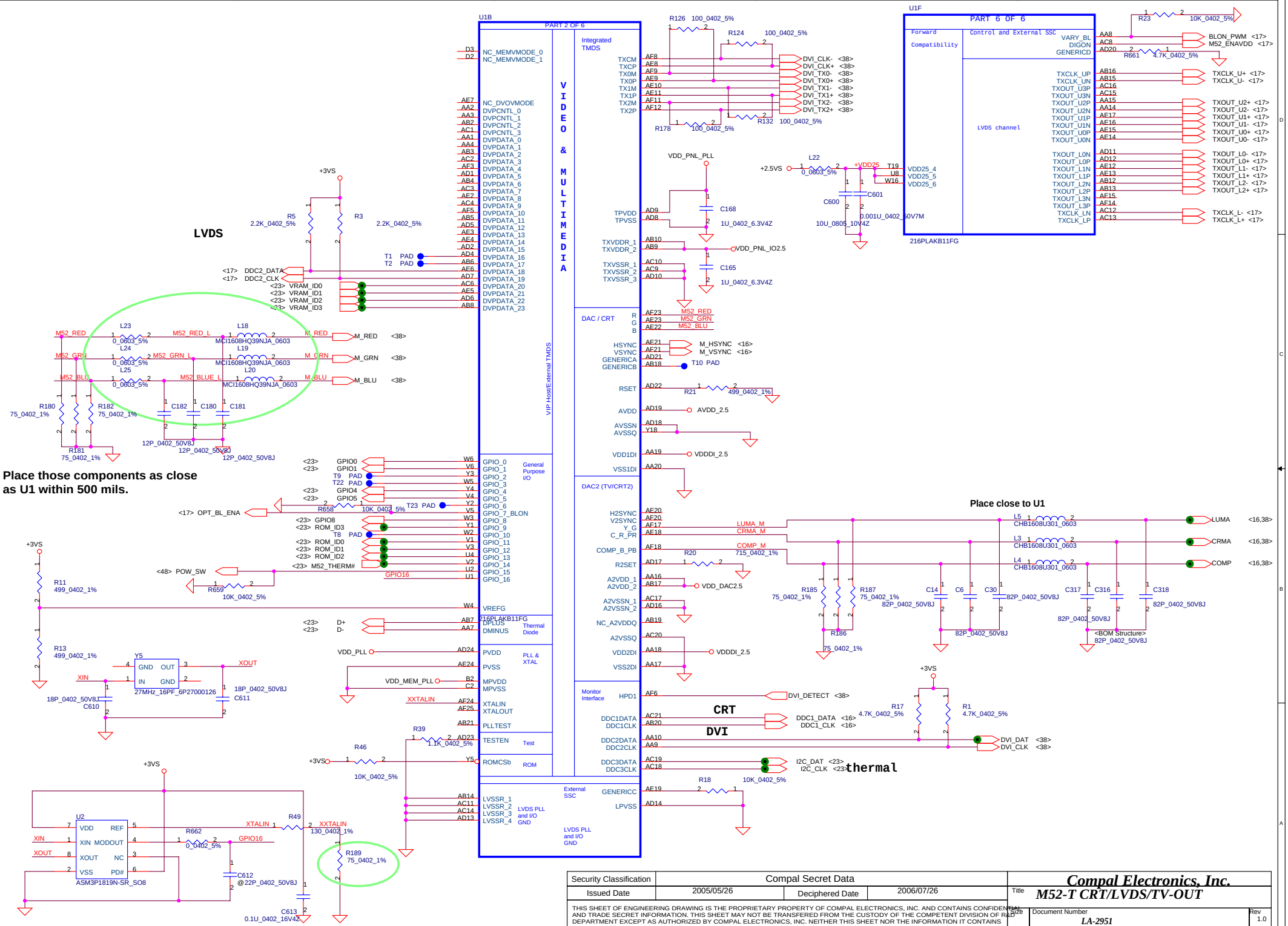
Support 3V inverter

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.	
Title	LCD CONN.
Size	Document Number: LA-2951 — Rev: 1.0
Date: Friday, April 28, 2006	Sheet 17 of 54



Compal Electronics, Inc.	
Title	M52-T PCIE interface
Size	Document Number: LA-2951 — Rev: 1.0
Date: Friday, April 28, 2006	Sheet 18 of 54



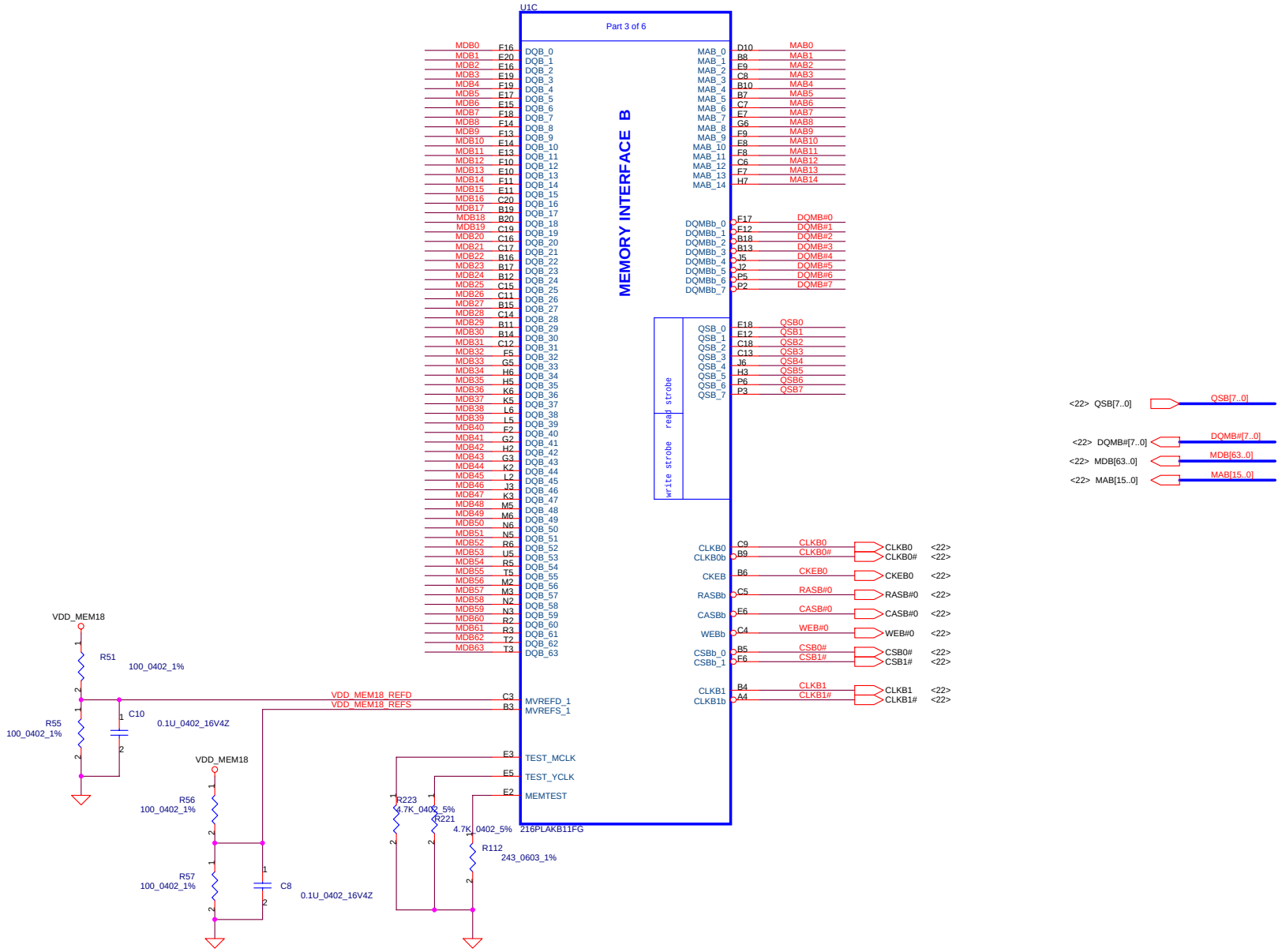
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **M52-T CRT/LVDS/TV-OUT**

Size	Document Number	Rev
	LA-2951	1.0

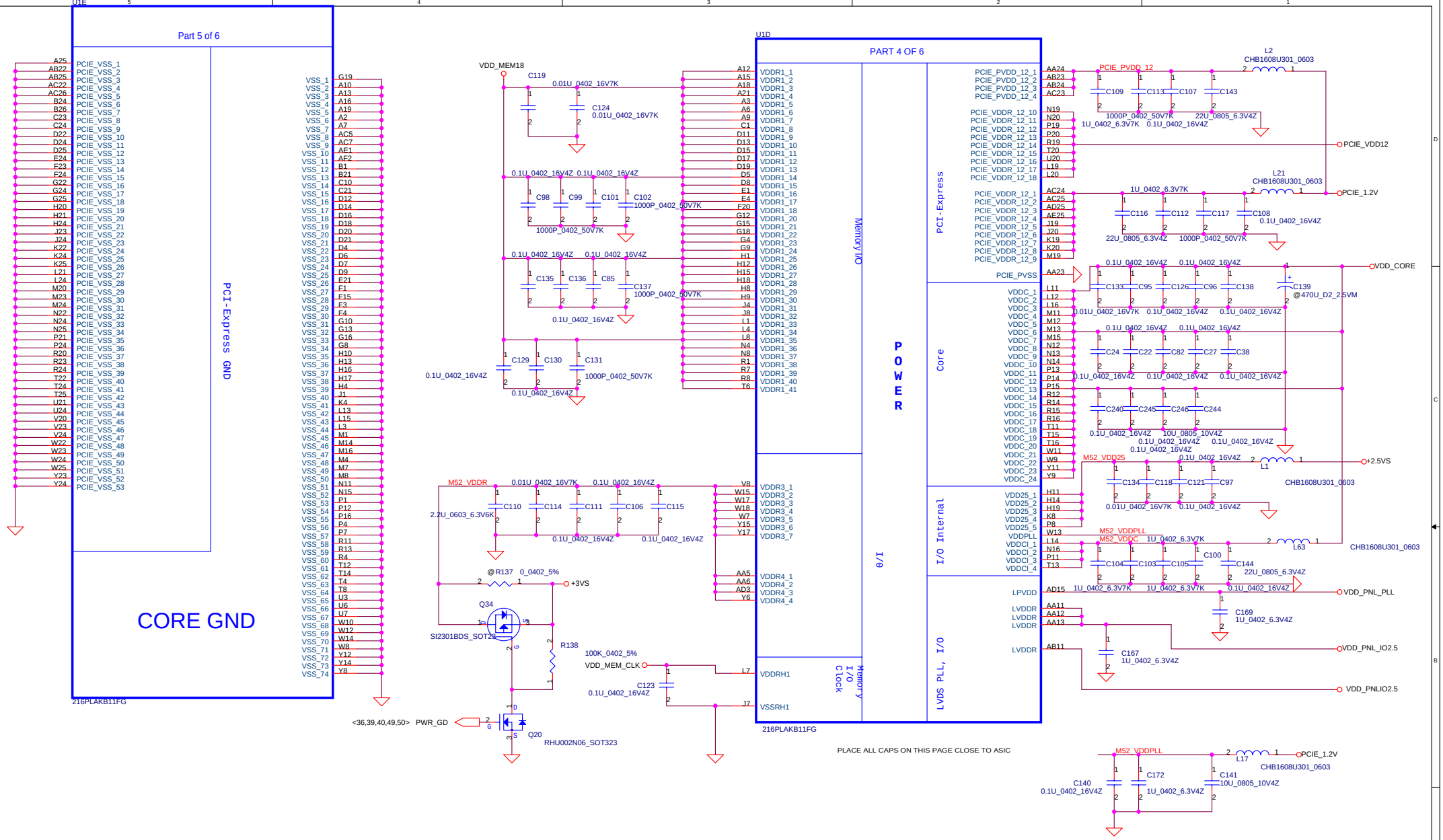
Date: Friday, April 28, 2006 | Sheet 19 of 54



M52@	R51,R55,C10,R56,R57,C8,R223,R221,R112

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.	
Title	M52-T MEM
Size	Document Number: LA-2951
Rev	1.0
Date: Friday, April 28, 2006	Sheet 20 of 54



PLACE ALL CAPS ON THIS PAGE CLOSE TO ASIC

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

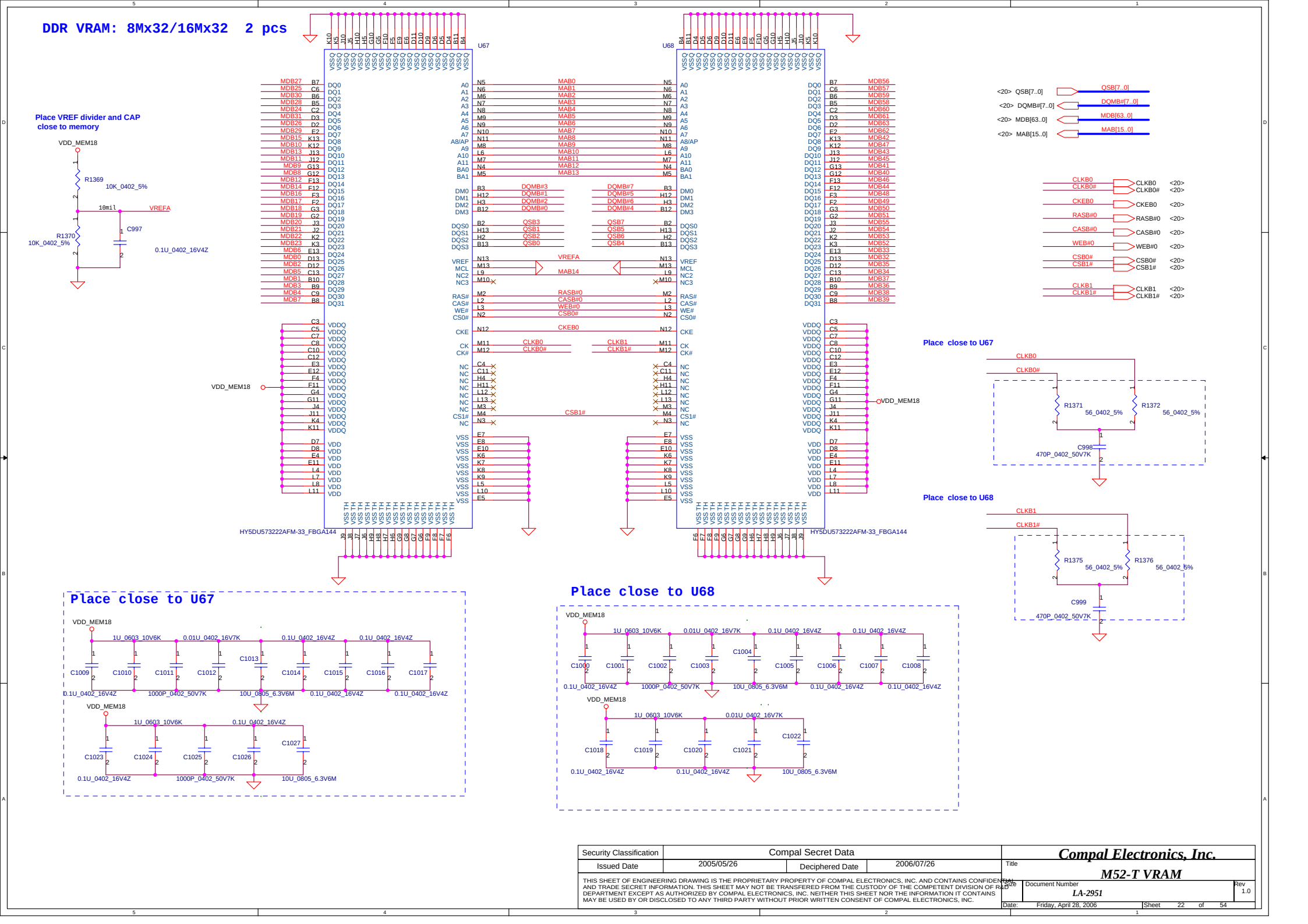
Compal Electronics, Inc.

Title: M52-T POWER

Size | Document Number: LA-2951 | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 21 of 54

DDR VRAM: 8Mx32/16Mx32 2 pcs



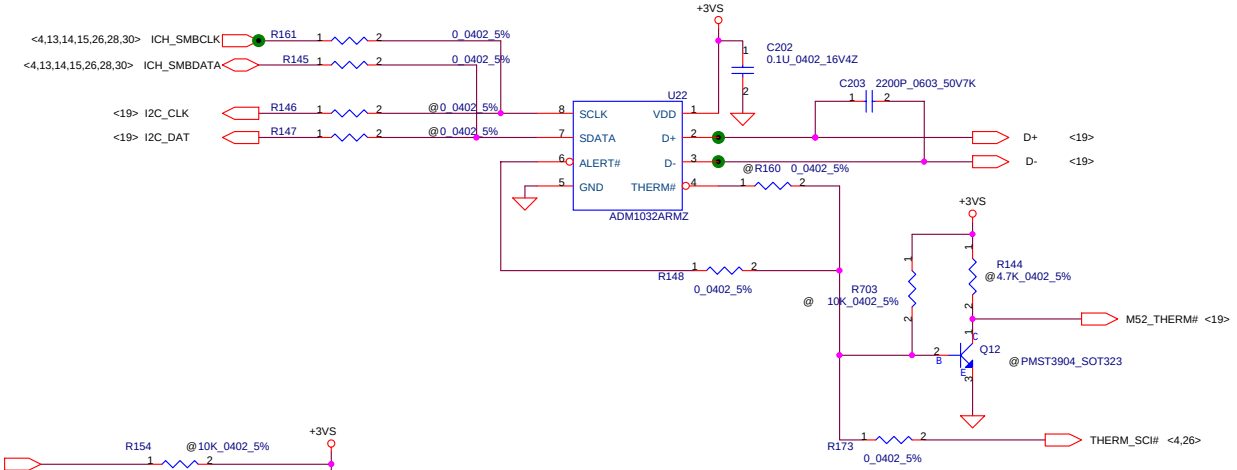
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

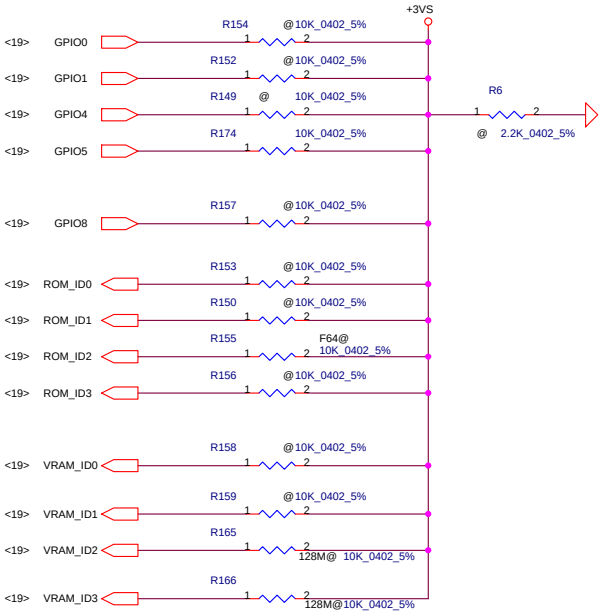
Compal Electronics, Inc.

Title: **M52-T VRAM**

Size | Document Number: **LA-2951** | Rev: 1.0

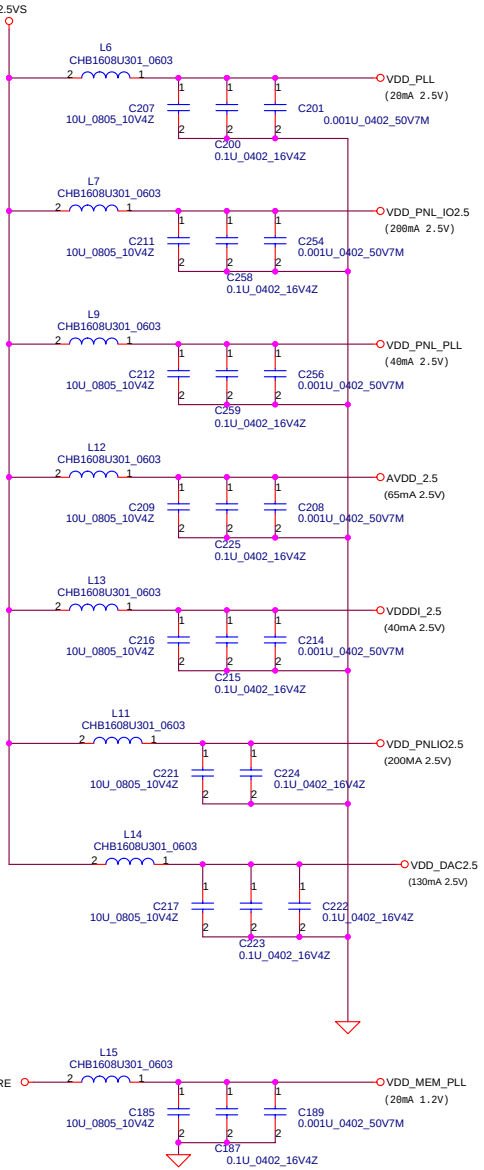
Date: Friday, April 28, 2006 | Sheet 22 of 54

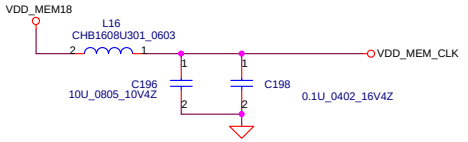


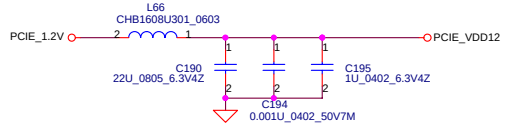


STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
TX_PWRS_ENB	GPIO0	FULL SWING	1
TX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE - TX DE-EMPHASIS DISABLED FOR MOBILE	0
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0
FORCE_COMPLIANCE	GPIO8	Force chip to get to compliance state quickly for tester pruposes	0
ROMIDCFG(3:0)	GPIO (9,13,12,11)	No ROM , with 128M frame buffer	0 0 0 X
		No ROM , with 64M frame buffer	0 1 0 X
VRAM_ID[0:3]	DVPDATA (20,21,22,23)	Samsung 8Mx32 1.8V F die K4D553235F-VC33	0 0 0 0
		Hynix 16Mx32 1.8V HY5DS113222FMP-28	0 0 0 1
		Hynix 8Mx32 1.8V HY5DS573222F-33	0 0 1 0
		Hynix 16Mx32 1.8V HY5DS113222FMP-33	0 0 1 1

	Samsung 64MB (300MHz)	Hynix 128MB (350MHz)	Hynix 64MB (300MHz)	Hynix 128MB (300MHz)
R165	0	0	1	1
R166	0	1	0	1







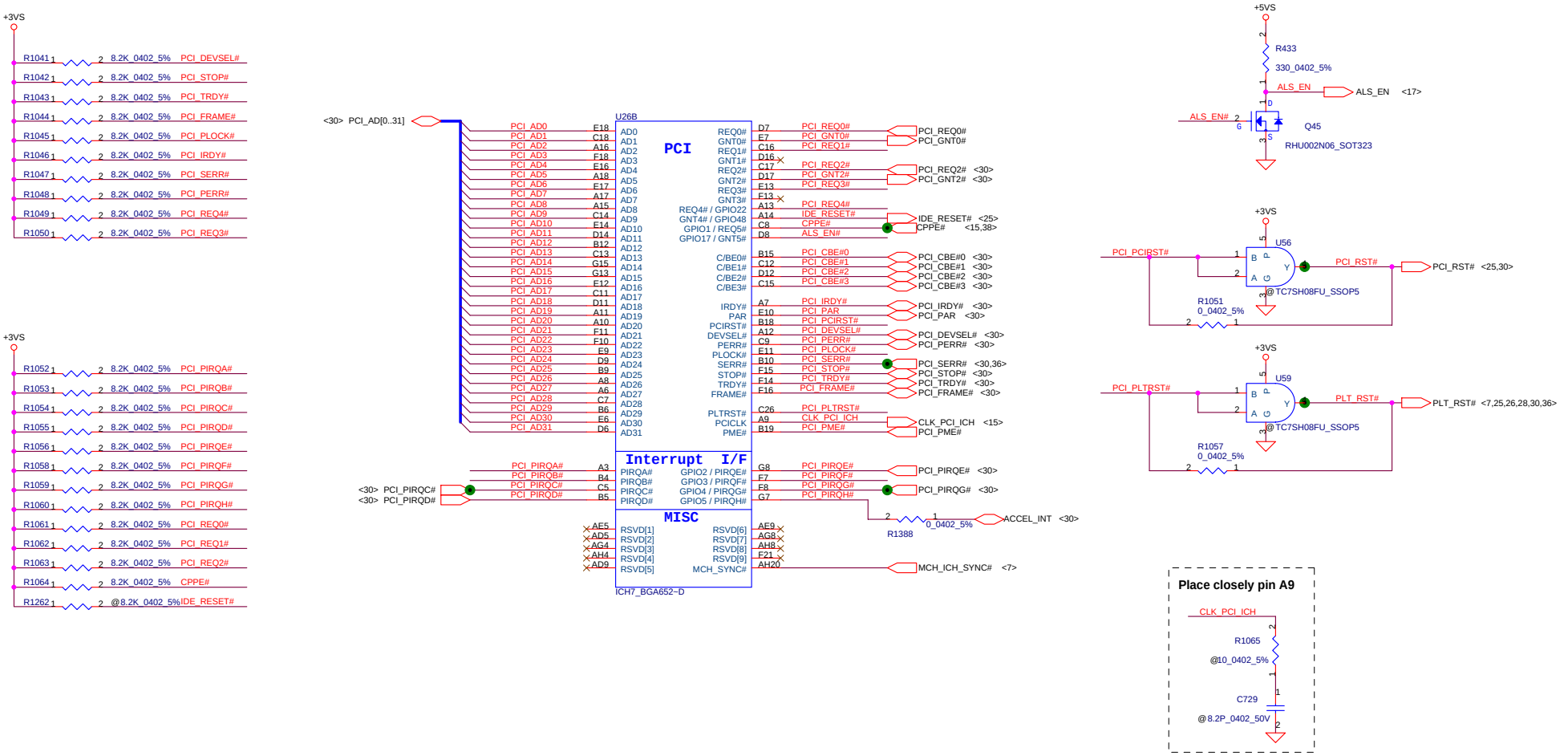
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **M52-T Filters / Strap**

Size	Document Number	Rev
	LA-2951	1.0

Date: Friday, April 28, 2006 Sheet 23 of 54



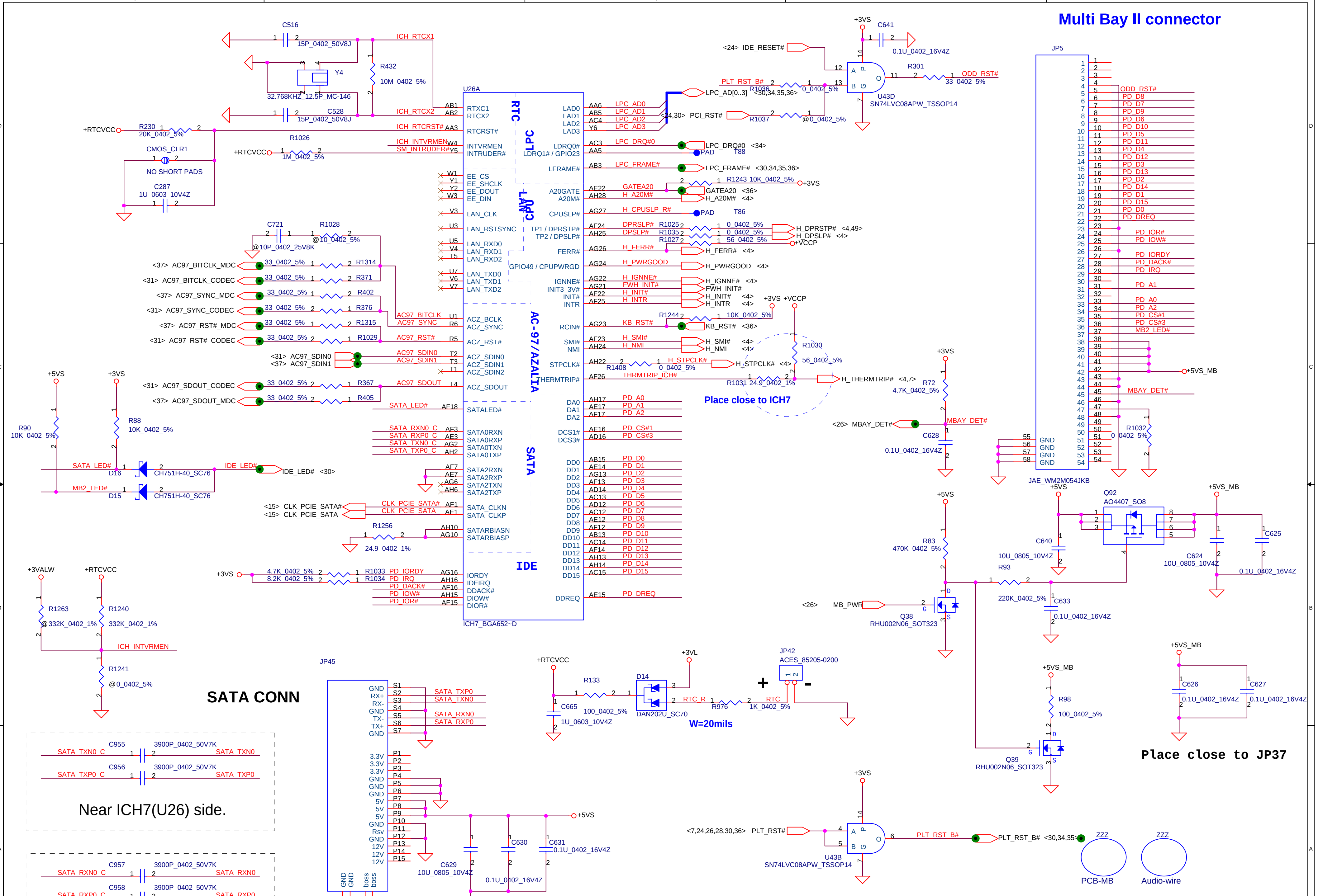
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: ICH7-M(1/4)

Size | Document Number: LA-2951 | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 24 of 54



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

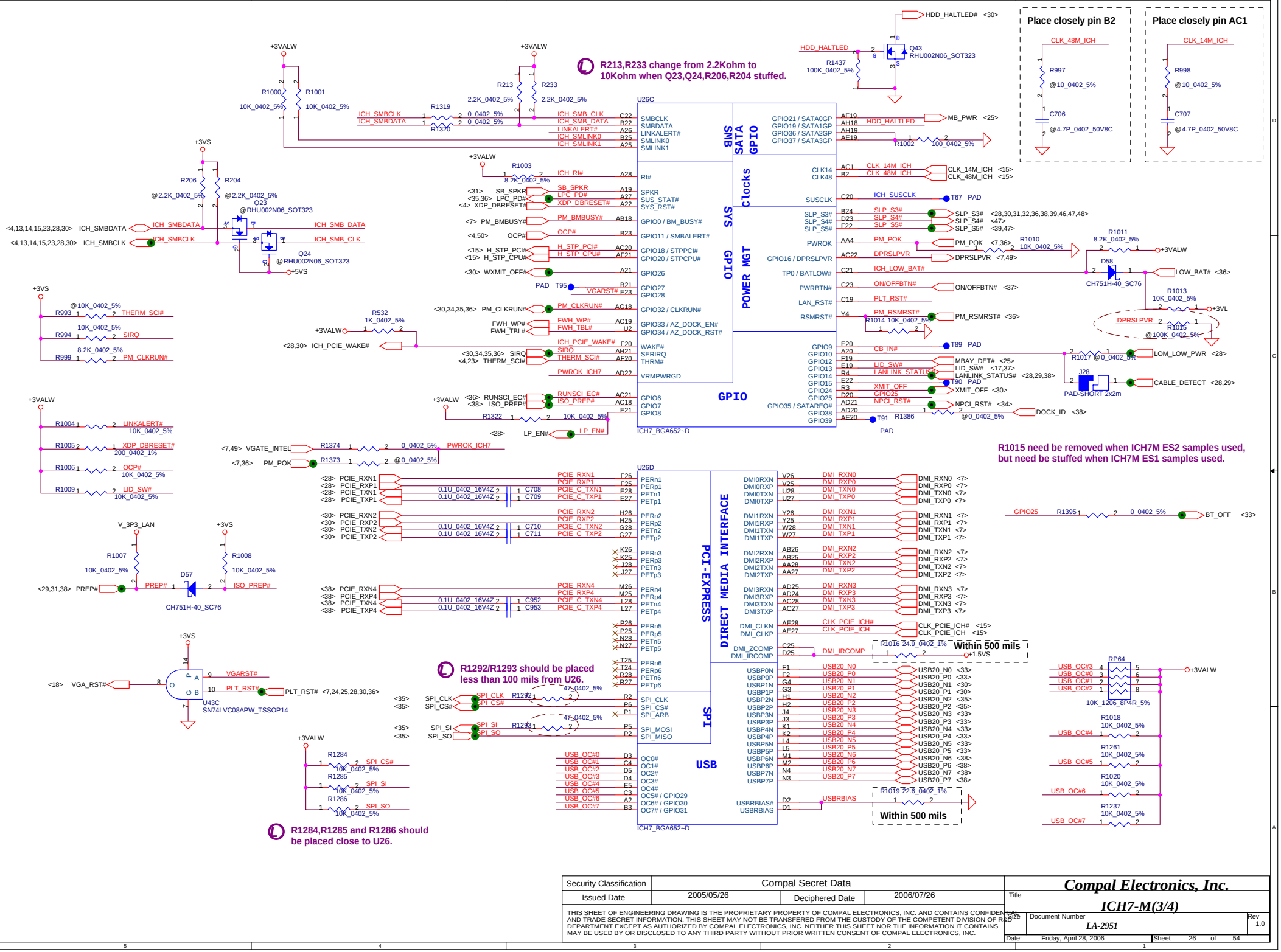
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

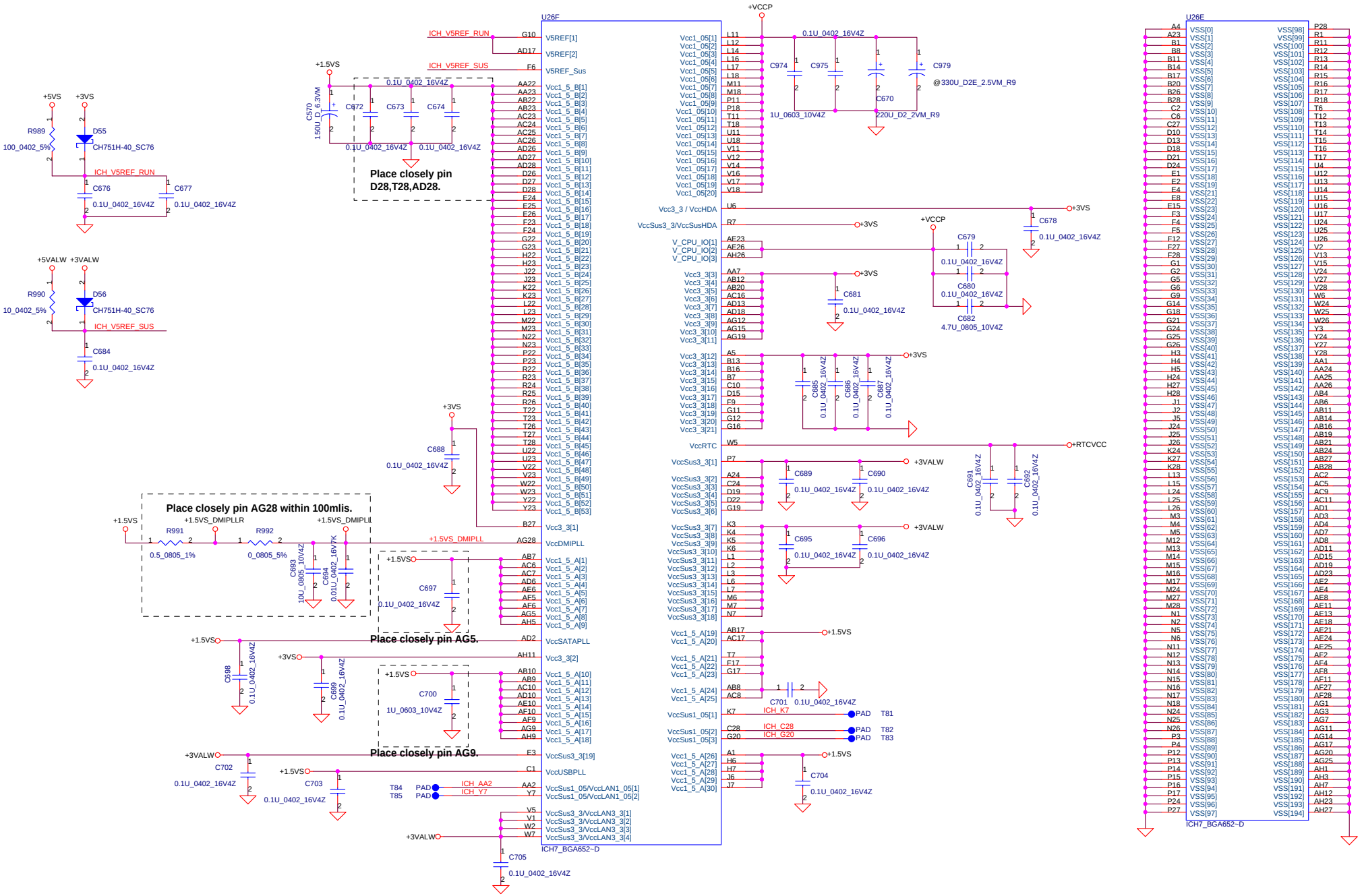
Compal Electronics, Inc.

Title: ICH7-M(2/4)

Size | Document Number: LA-2951 | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 25 of 54


R213,R233 change from 2.2Kohm to 10Kohm when Q23,Q24,R206,R204 stuffed.
Place closely pin B2
Place closely pin AC1
R1015 need be removed when ICH7M ES2 samples used, but need be stuffed when ICH7M ES1 samples used.
R1292/R1293 should be placed less than 100 mils from U26.
R1284,R1285 and R1286 should be placed close to U26.
Within 500 mils
Within 500 mils
U26C
U26D
ICH7_BGA652-D
SMB
SATA GPIO
Clocks
SYS
GPIO
POWER MGT
GPIO
PCI-EXPRESS
DIRECT MEDIA INTERFACE
SPI
USB
Security Classification
Compal Secret Data
Issued Date
2005/05/26
Deciphered Date
2006/07/26
Compal Electronics, Inc.
ICH7-M(3/4)
LA-2951
Rev 1.0
Friday, April 28, 2006
Sheet 26 of 54



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

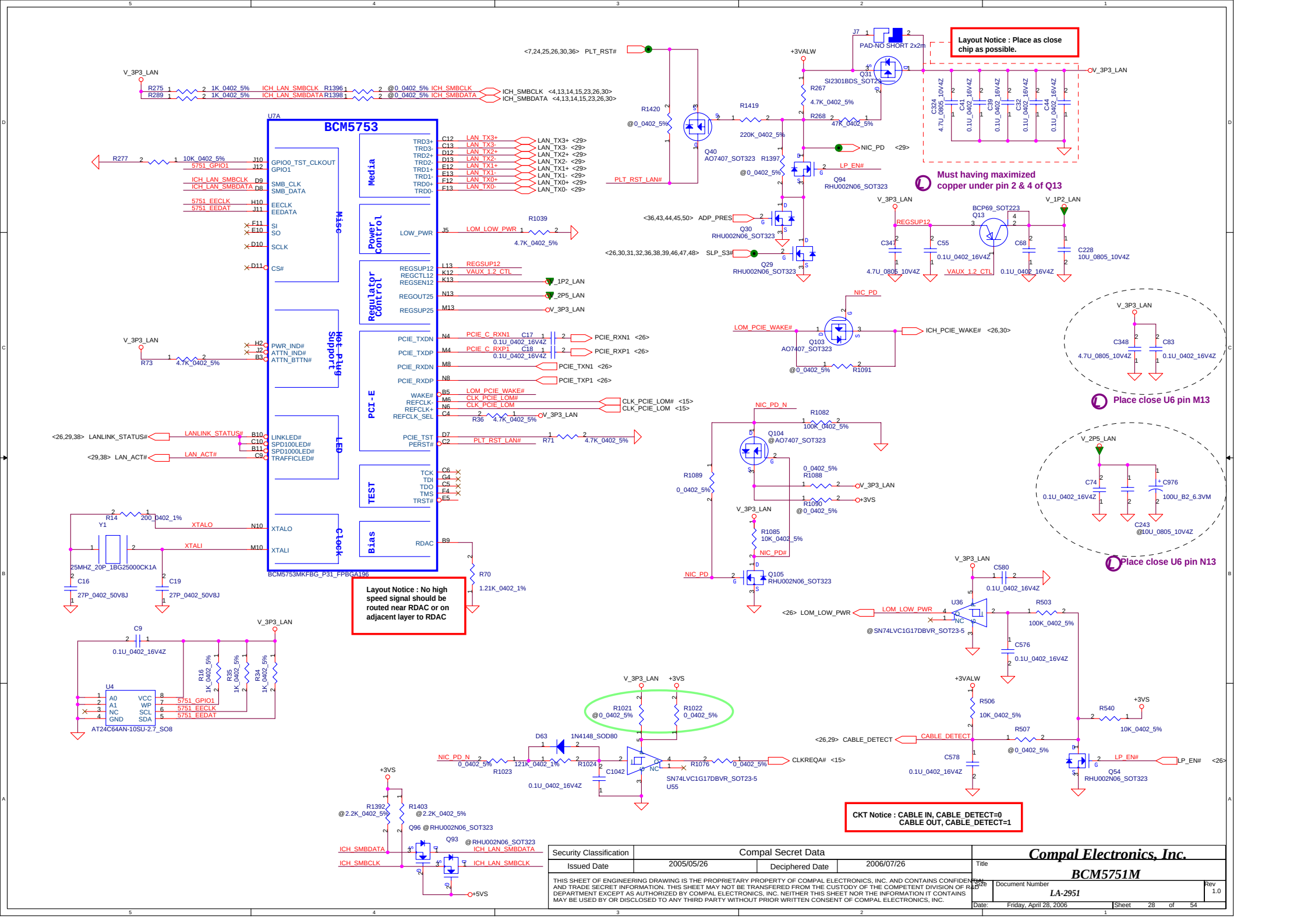
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

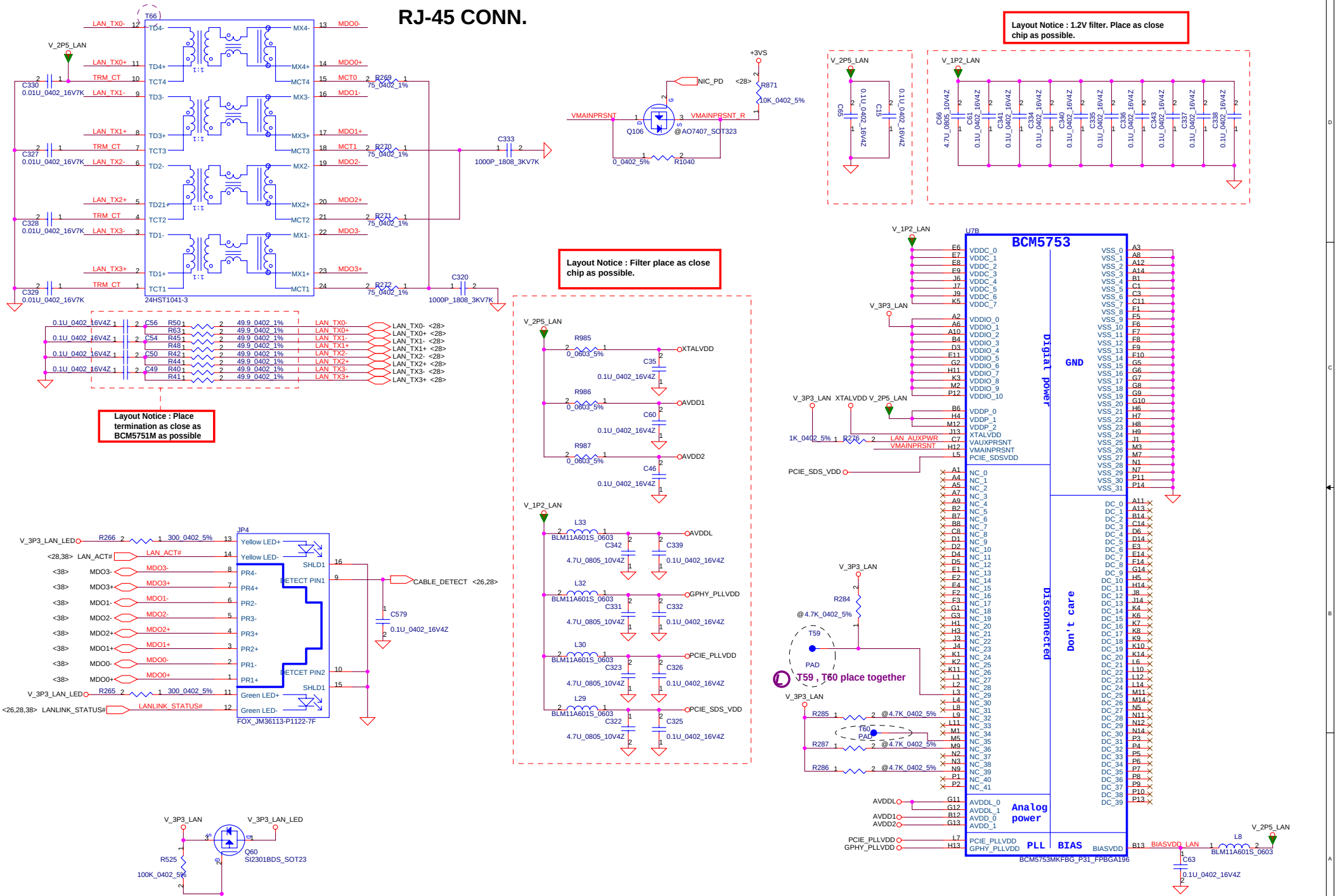
Title: **ICH7-M(4/4)**

Size: Document Number: **LA-2951** Rev: 1.0

Date: Friday, April 28, 2006 Sheet 27 of 54


BCM5753
U7A
Media
Power Control
Regulator Control
PCI-E
Hot Plug
LED
TEST
Bias
Clock
BCM5753MKFBG_P31_FPBGA196
Layout Notice : No high speed signal should be routed near RDAC or on adjacent layer to RDAC
Layout Notice : Place as close chip as possible.
Must having maximized copper under pin 2 & 4 of Q13
Place close U6 pin M13
Place close U6 pin N13
CKT Notice : CABLE IN, CABLE_DETECT=0
CABLE OUT, CABLE_DETECT=1
AT24C64AN-10SU-2.7_SO8
SN74LVC1G17DBVR_SOT23-5
SI2301BDS_SOT23
AO7407_SOT323
RHU002N06_SOT323
BCP69_SOT223
PAD-NO SHORT 2x2m
1N4148_SOD80
25MHZ_20P_1BG25000CK1A
Security Classification
Compal Secret Data
Issued Date
2005/05/26
Deciphered Date
2006/07/26
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
BCM5751M
Size
Document Number
LA-2951
Rev
1.0
Date:
Friday, April 28, 2006
Sheet
28
of
54

RJ-45 CONN.



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

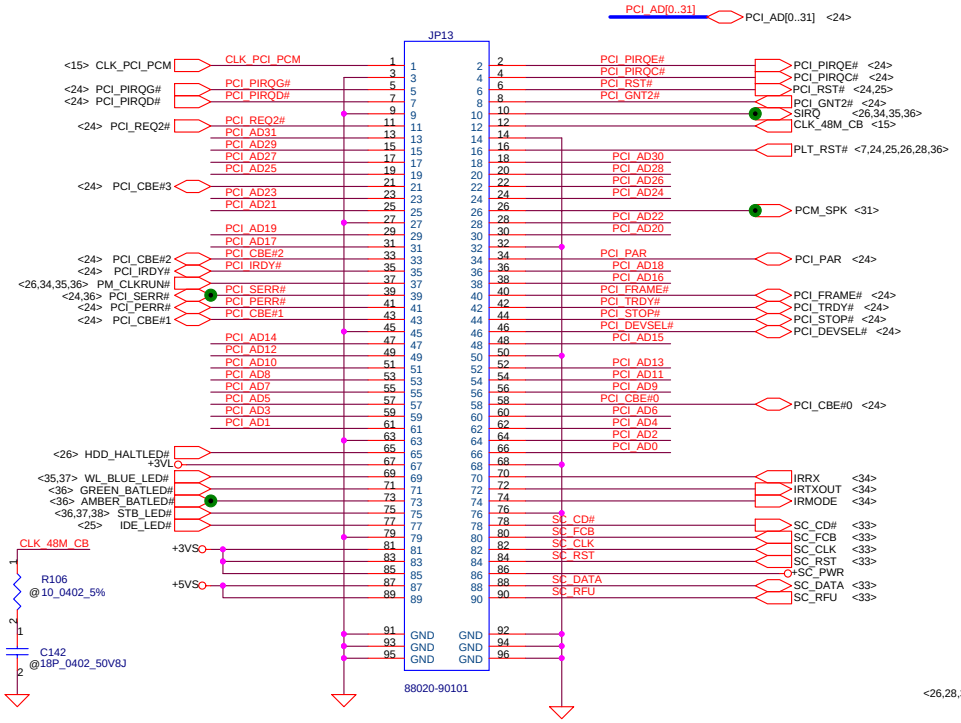
Compal Electronics, Inc.

Title: **Magnetic & RJ45/RJ11**

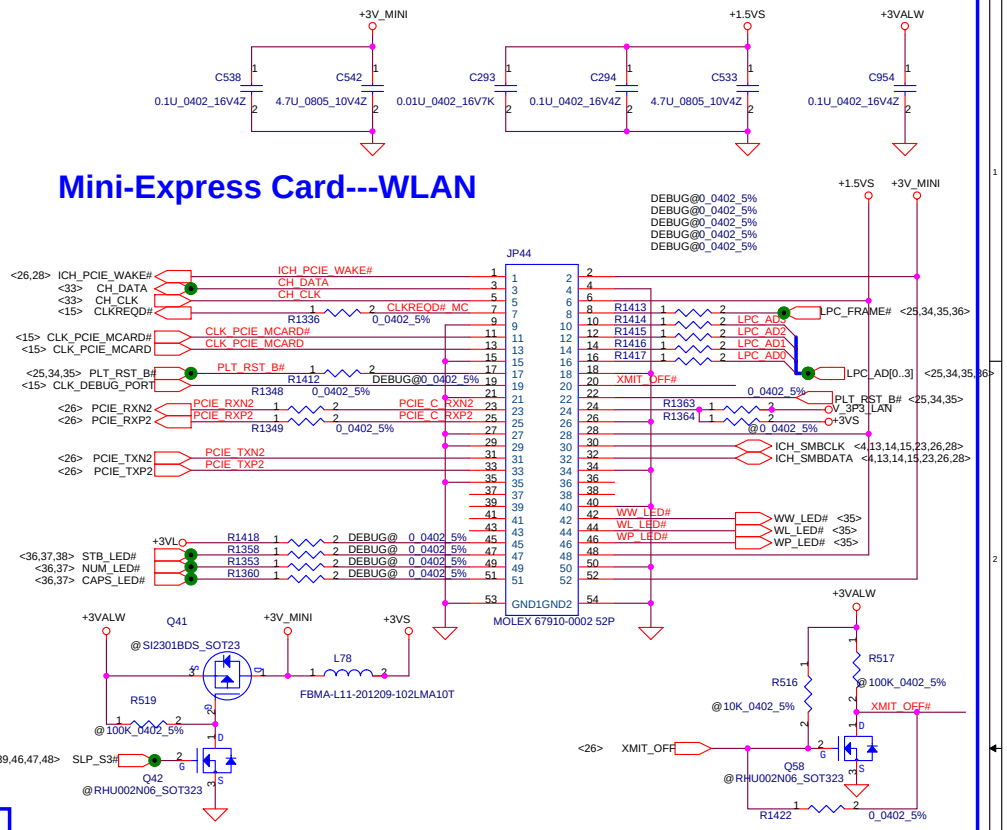
Size	Document Number	Rev
	LA-2951	1.0

Date: Friday, April 28, 2006 Sheet 29 of 54

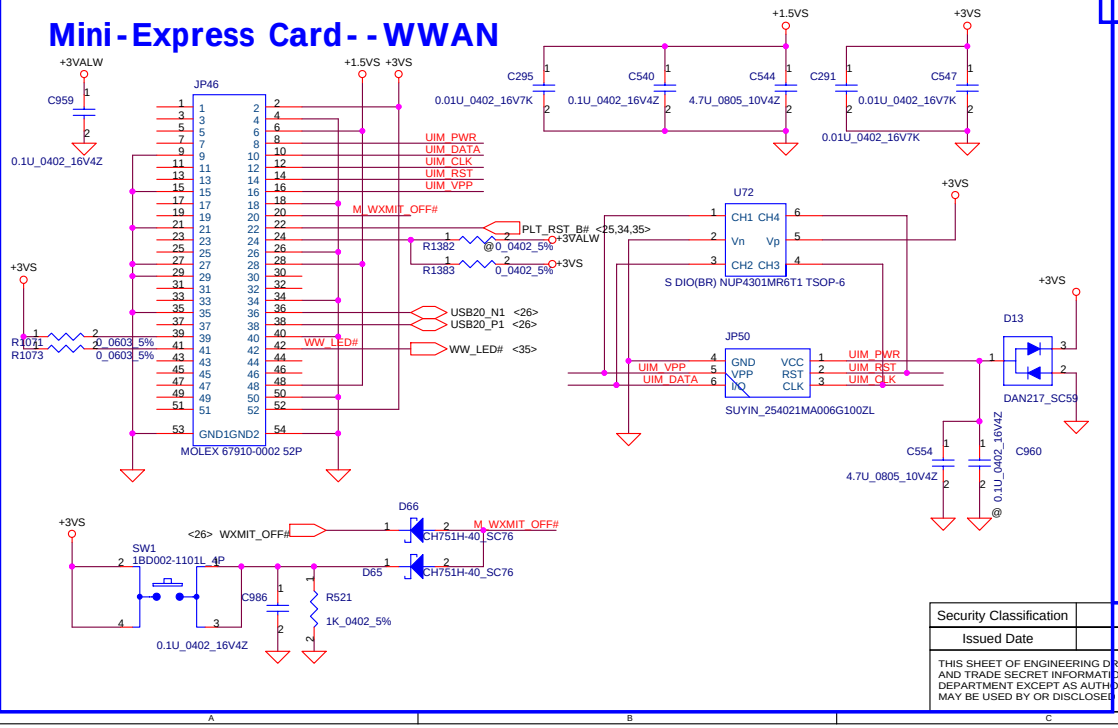
B/B connector with PCI / LED / FIR / SC interface



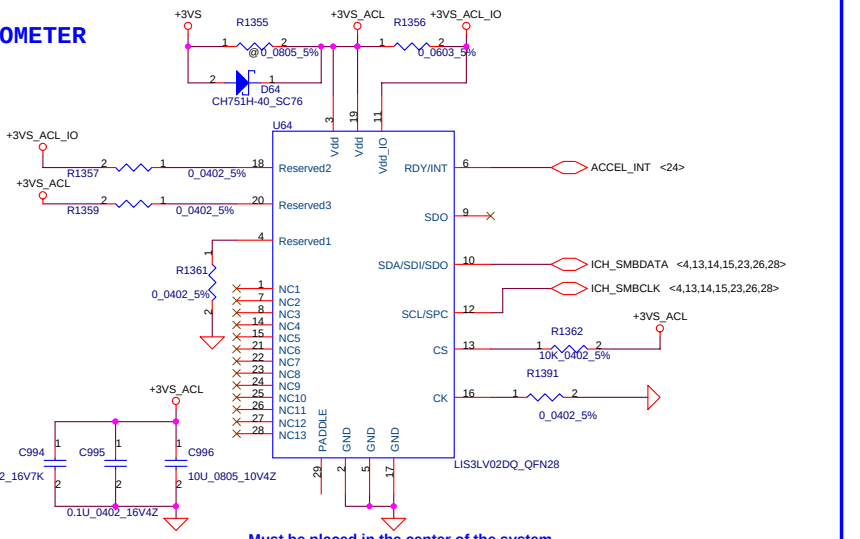
Mini-Express Card---WLAN



Mini-Express Card--WWAN



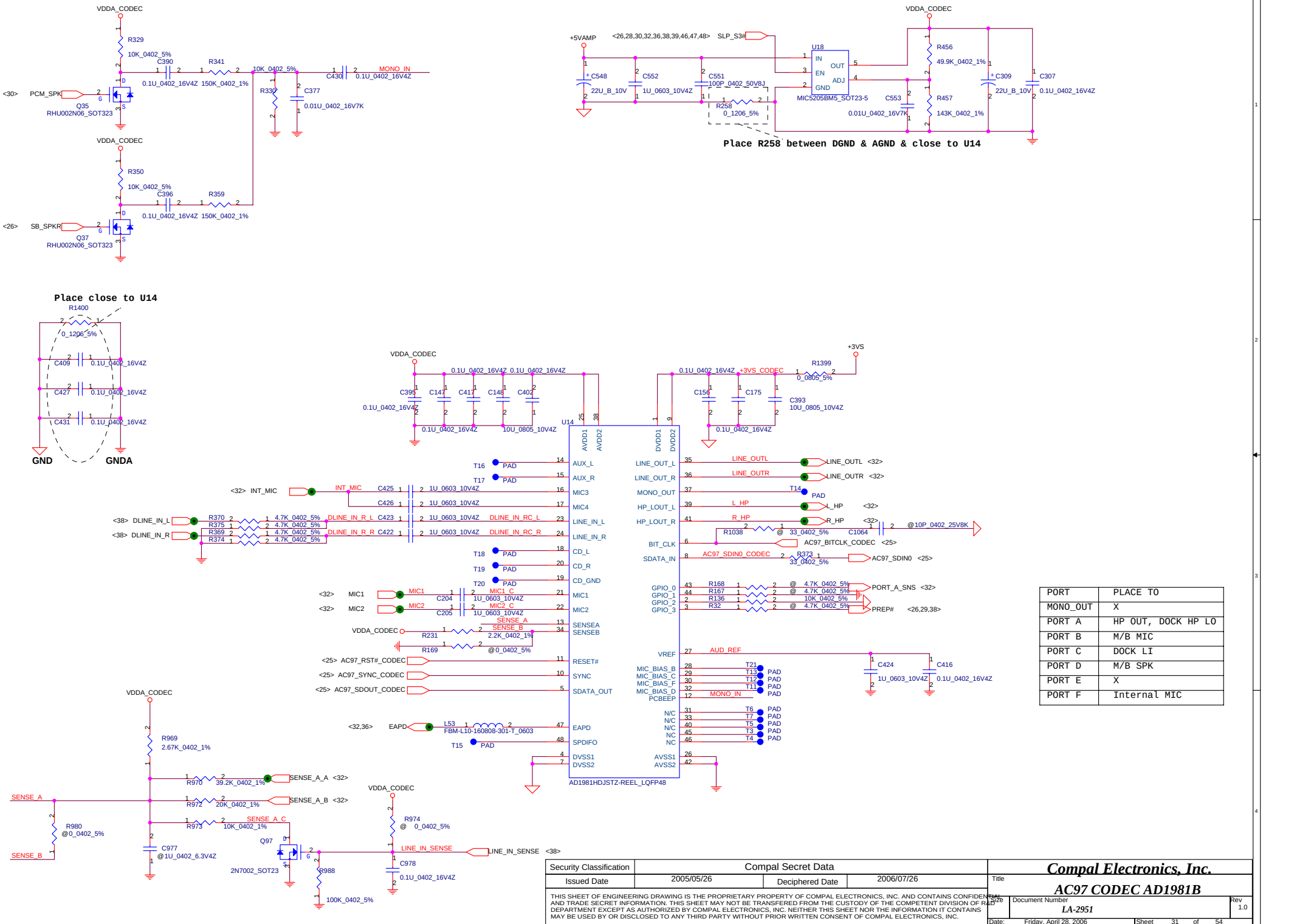
ACCELEROMETER



Must be placed in the center of the system.

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Title	*Compal Electronics, Inc.*		
	Mini-Card/Mini-PCI/Accelerometer		
Size	Document Number		Rev
	LA-2951		1.0
Date:	Friday, April 28, 2006	Sheet	30 of 54



PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT, DOCK HP LO
PORT B	M/B MIC
PORT C	DOCK LI
PORT D	M/B SPK
PORT E	X
PORT F	Internal MIC

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

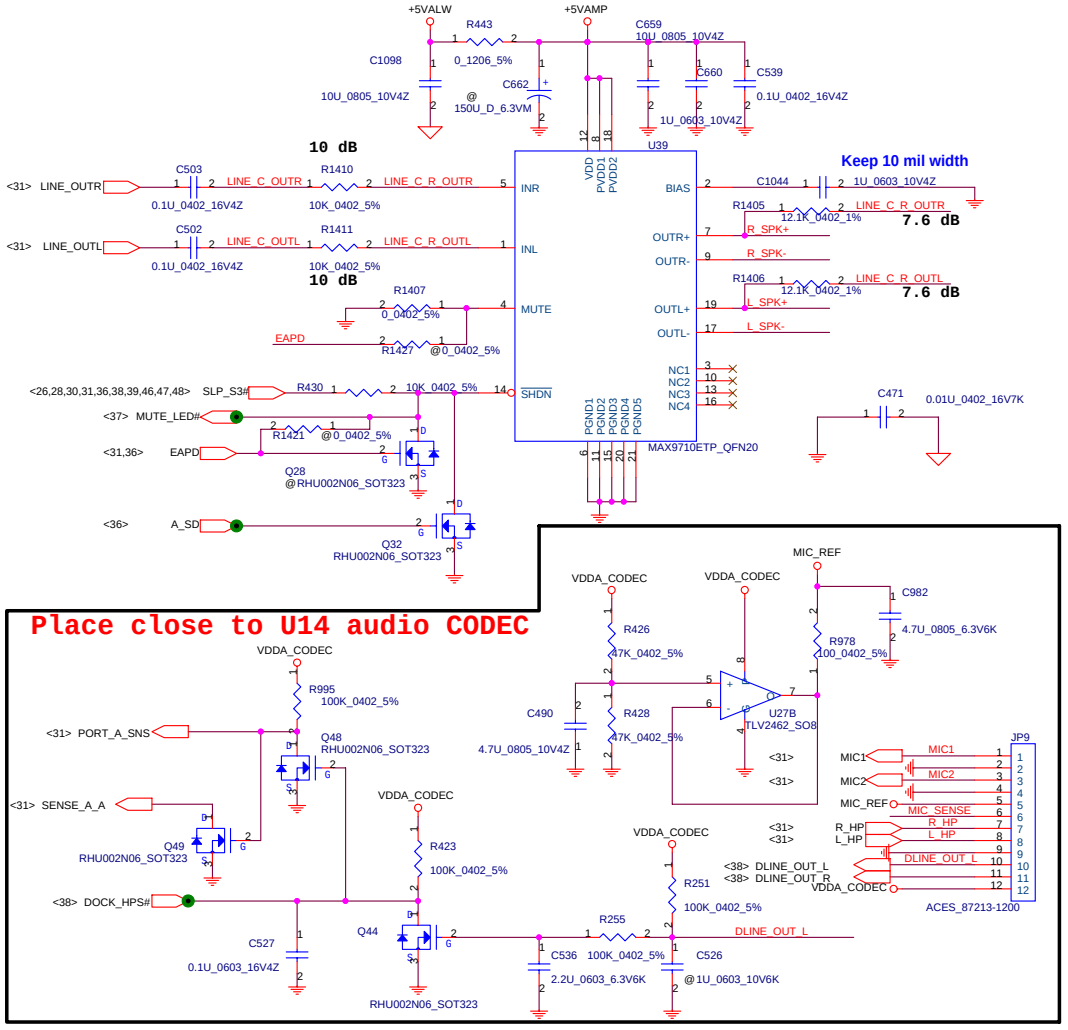
Compal Electronics, Inc.

Title: AC97 CODEC AD1981B

Size: Document Number: LA-2951 Rev: 1.0

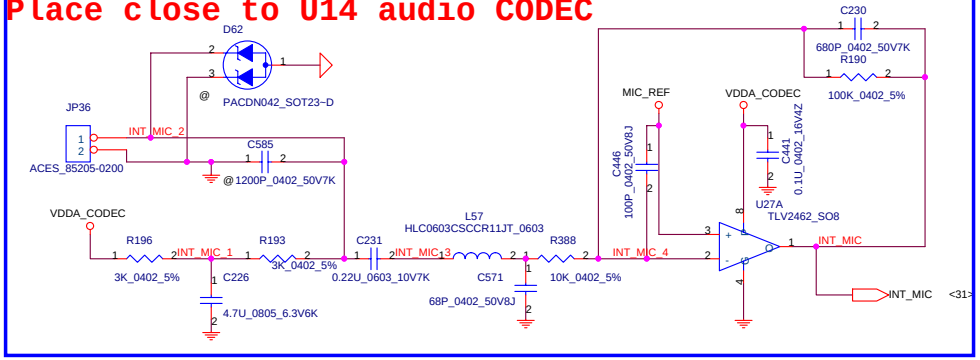
Date: Friday, April 28, 2006 Sheet 31 of 54

AMP. FOR INTERNAL SPEAKER



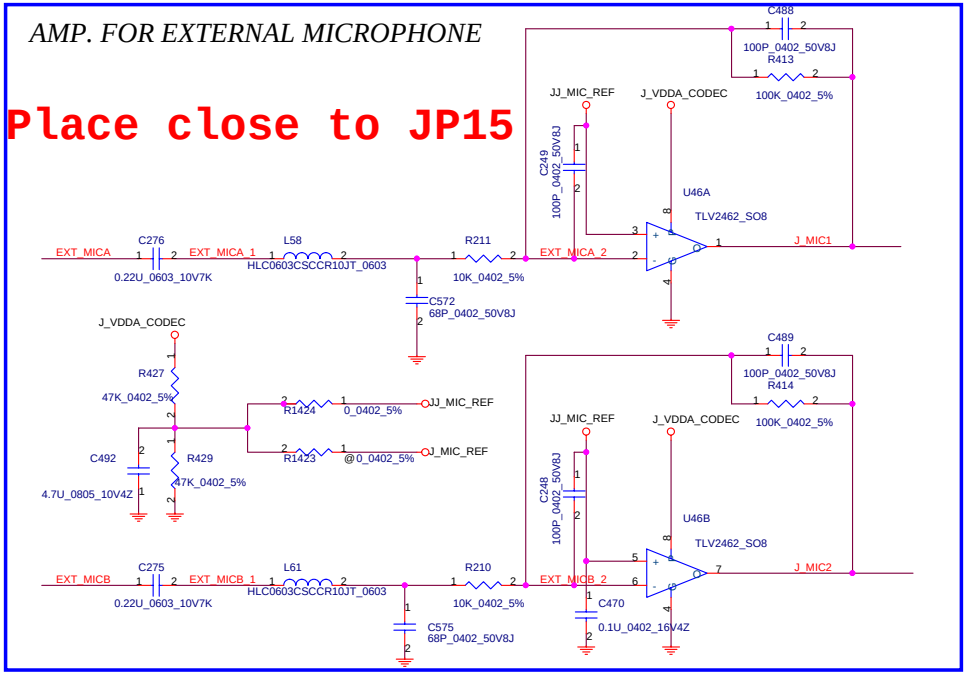
AMP. FOR INTERNAL MICROPHONE

Place close to U14 audio CODEC

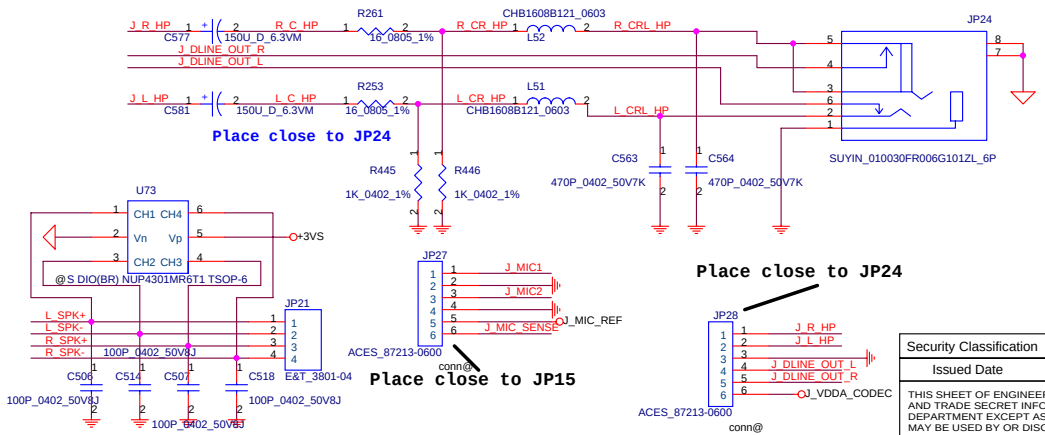


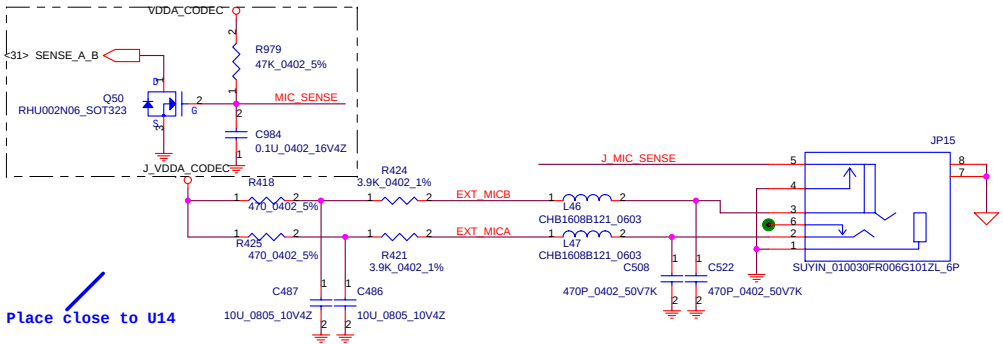
AMP. FOR EXTERNAL MICROPHONE

Place close to JP15



Place close to U14 audio CODEC





Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

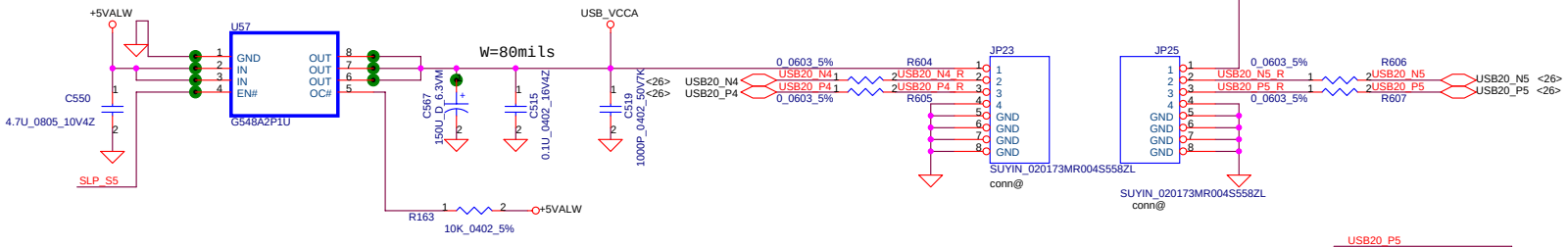
Compal Electronics, Inc.

Title: **AMP & Audio Jack**

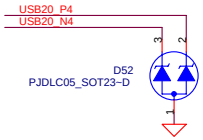
Size: | Document Number: **LA-2951** | Rev: 1.0

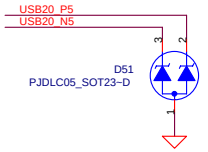
Date: Friday, April 28, 2006 | Sheet 32 of 54

Left side USB CONNECTOR 0

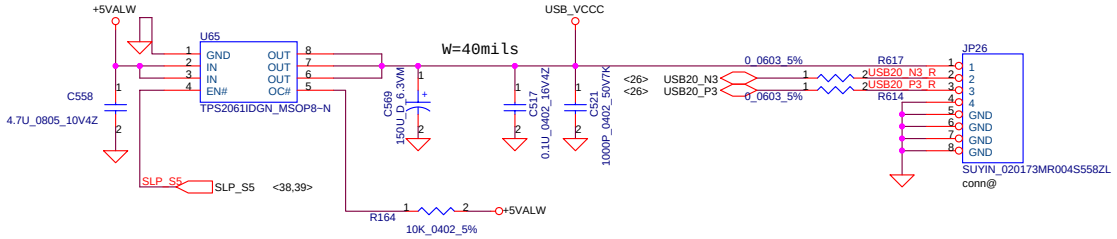


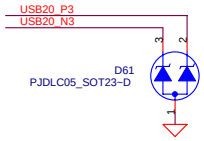
Left side USB CONNECTOR 1



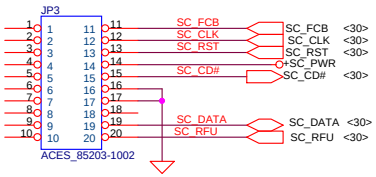


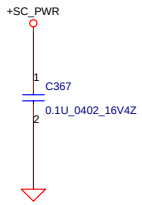
Right side USB CONNECTOR 0



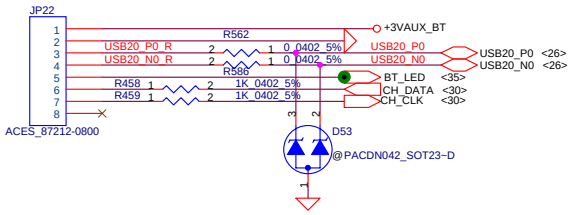


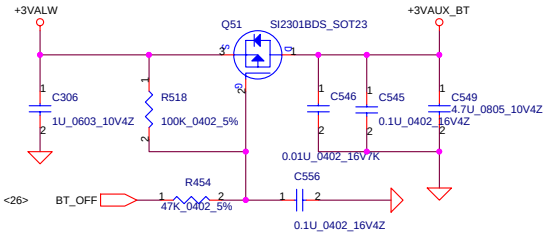
SMART Card connector





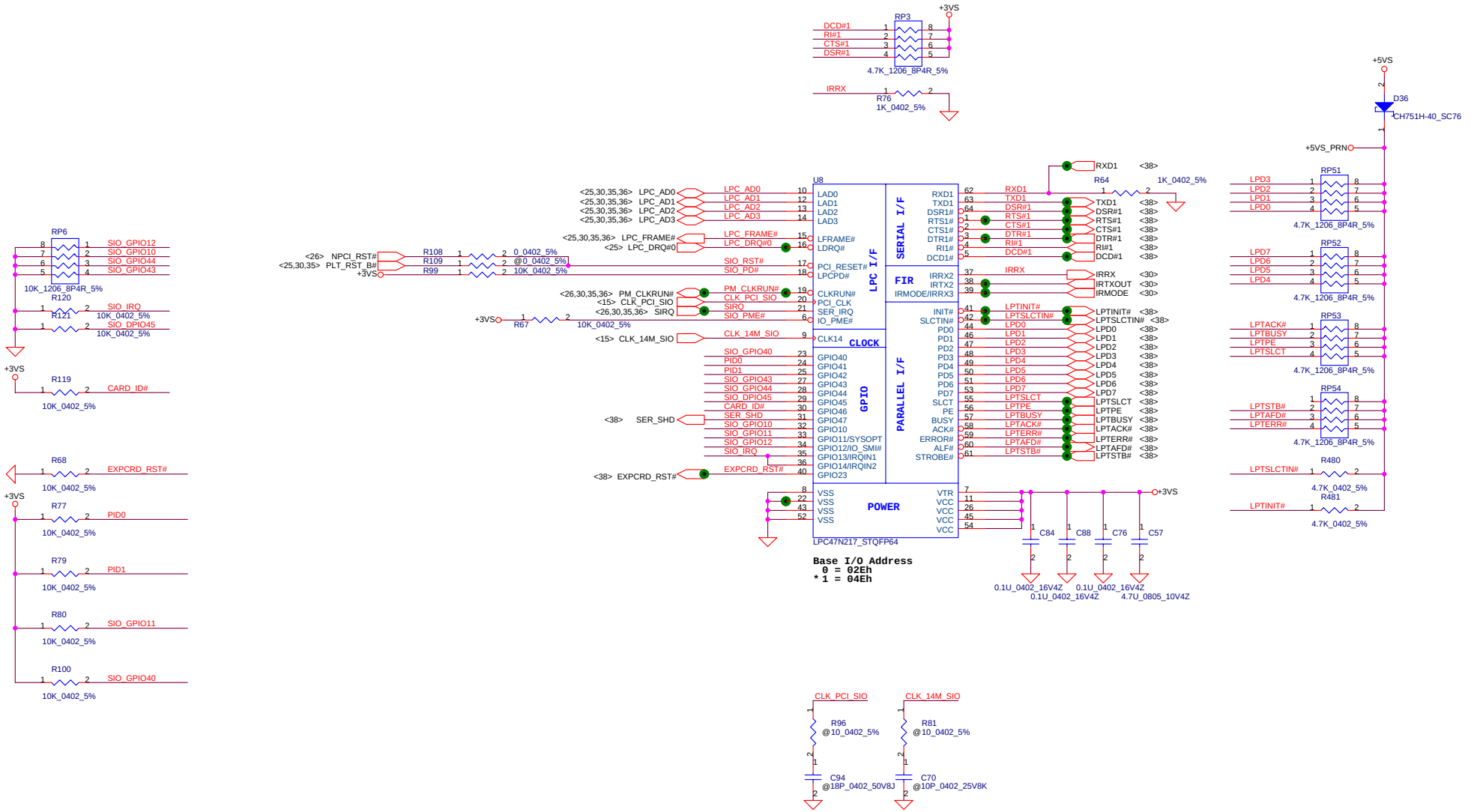
BT Connector





Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.	
Title	USB & BT Connector
Size	Document Number: LA-2951 — Rev: 1.0
Date: Friday, April 28, 2006	Sheet 33 of 54



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

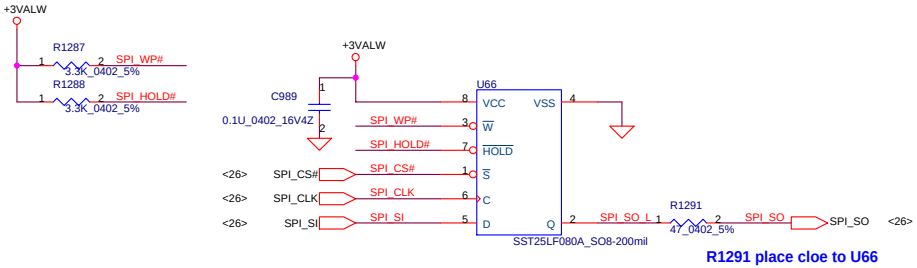
Compal Electronics, Inc.

Title: **SUPER I/O LPC47N217**

Size: | Document Number: **LA-2951** | Rev: 1.0

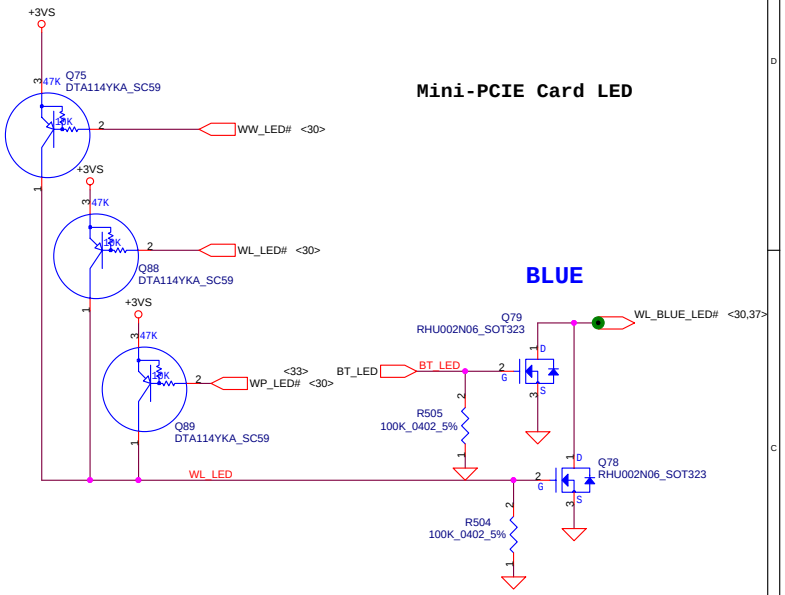
Date: Friday, April 28, 2006 | Sheet 34 of 54

BIOS ROM

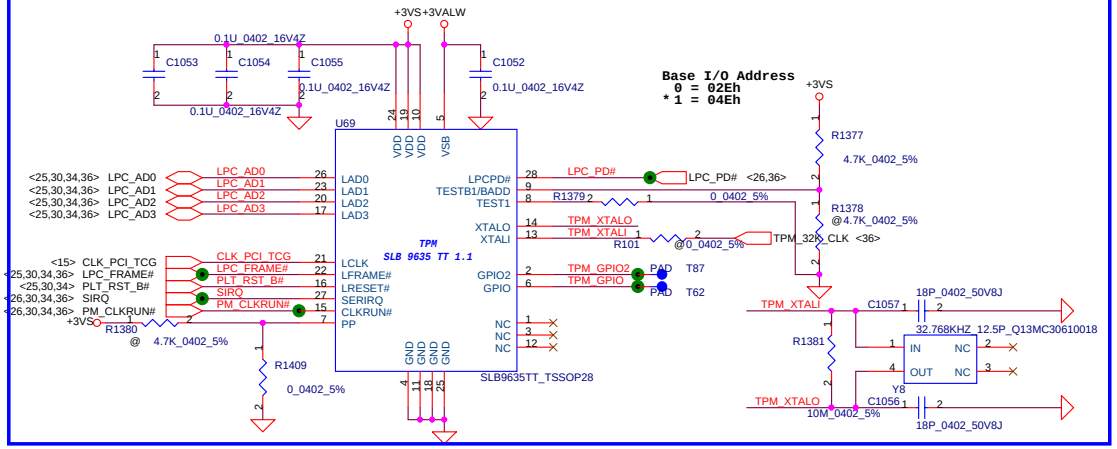


R1291 place cloe to U66

Mini-PCIE Card LED

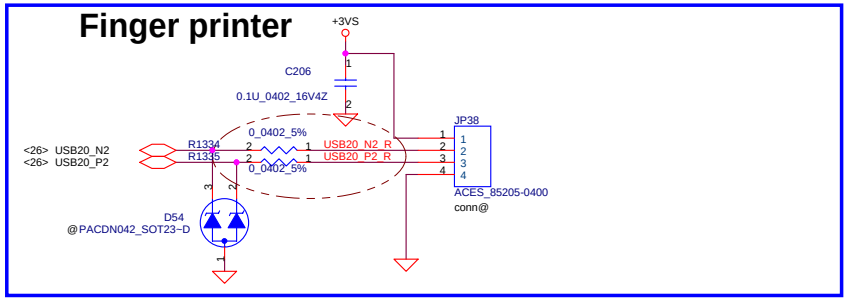


TPM1.2



Base I/O Address
0 = 02Eh
* 1 = 04Eh

Finger printer



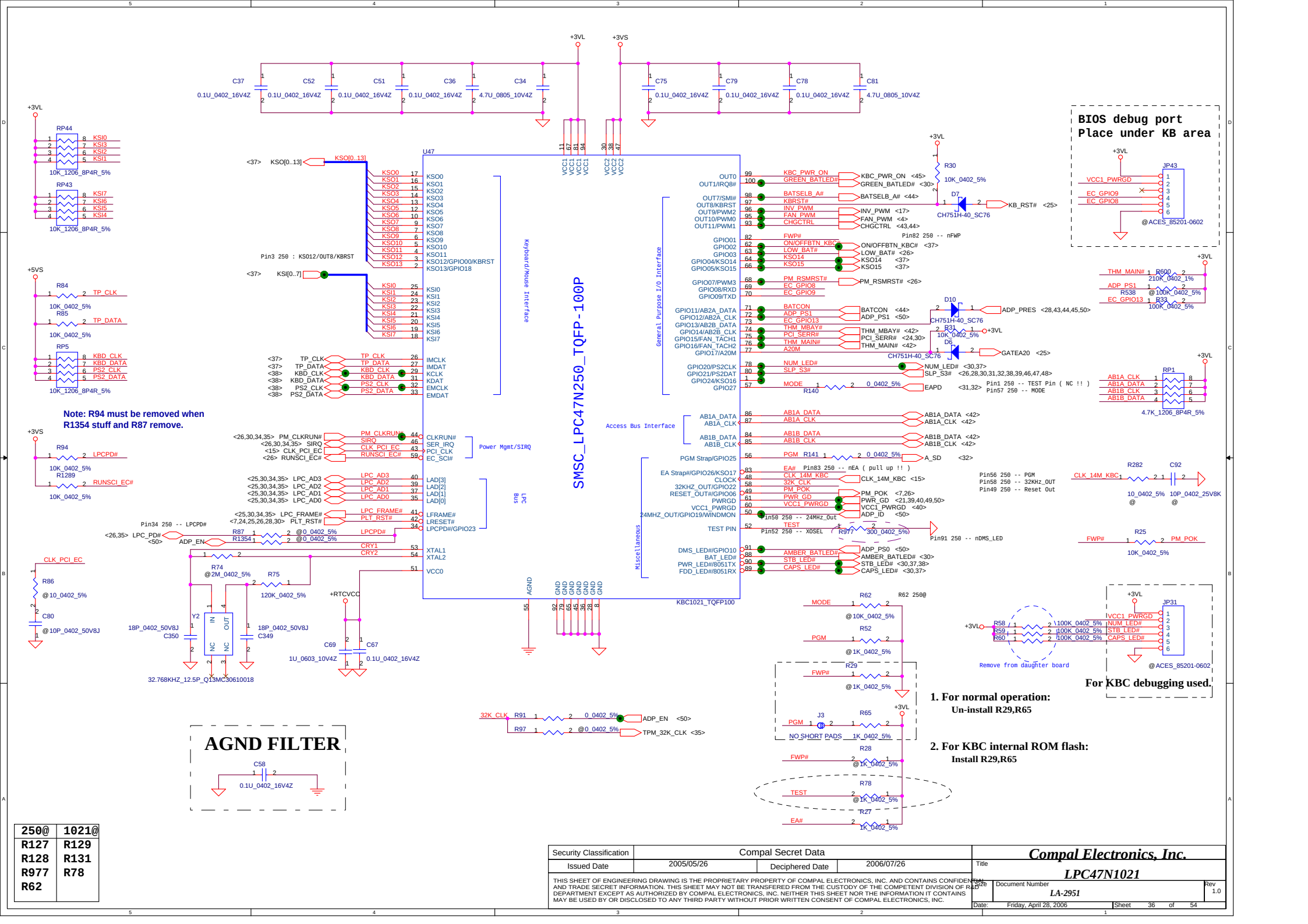
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

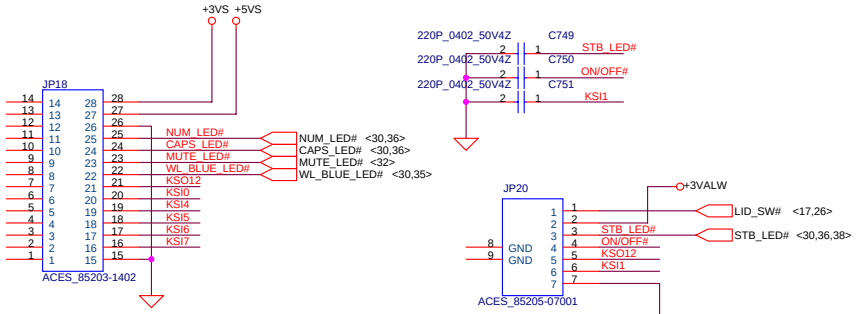
Title: TCG/BIOS ROM/PS2/LED/SW

Size | Document Number: LA-2951 | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 35 of 54


SMSC_LPC47N250_TQFP-100P
KBC1021_TQFP100
U47
Keyboard/Mouse Interface
General Purpose I/O Interface
Access Bus Interface
LPC Bus
Power Mgmt/SIRQ
Miscellaneous
BIOS debug port
Place under KB area
Note: R94 must be removed when
R1354 stuff and R87 remove.
AGND FILTER
For KBC debugging used.
1. For normal operation:
Un-install R29,R65
2. For KBC internal ROM flash:
Install R29,R65
Remove from daughter board
250@ 1021@
R127 R129
R128 R131
R977 R78
R62
Security Classification
Compal Secret Data
Issued Date
2005/05/26
Deciphered Date
2006/07/26
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
LPC47N1021
Size
Document Number
LA-2951
Rev
1.0
Date: Friday, April 28, 2006
Sheet 36 of 54

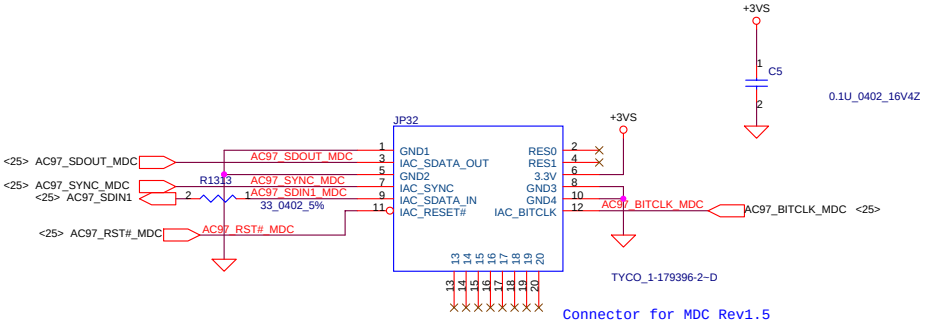
SWITCH BOARD.



WL,Vol up,Vol down,Mute,Present button

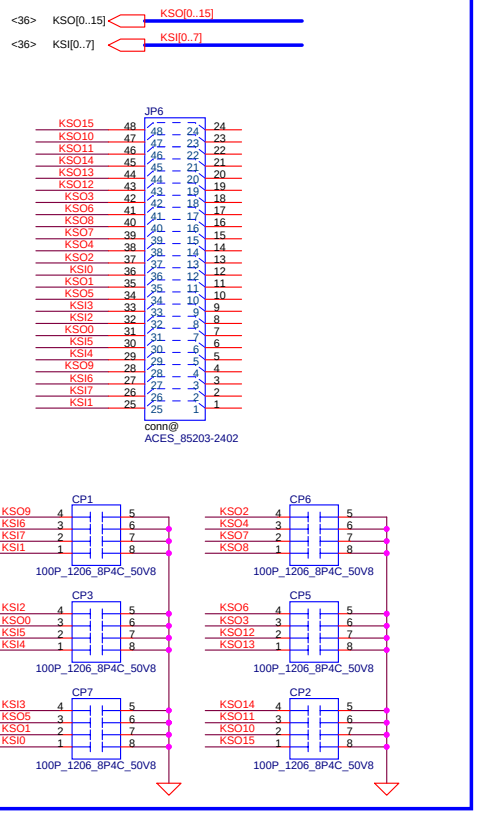
On/off ,information button

MDC 1.5 Conn.

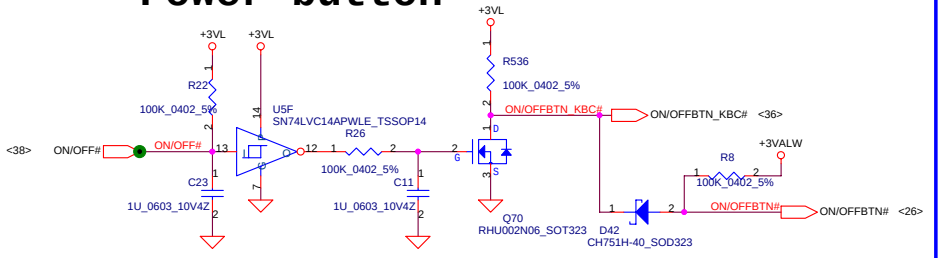


Connector for MDC Rev1.5

INT_KBD CONN.

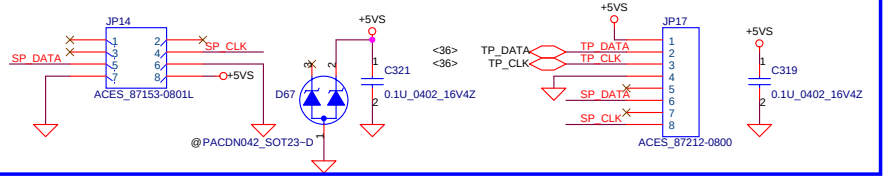


Power button



TrackPoint CONN.

T/P BOARD.



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

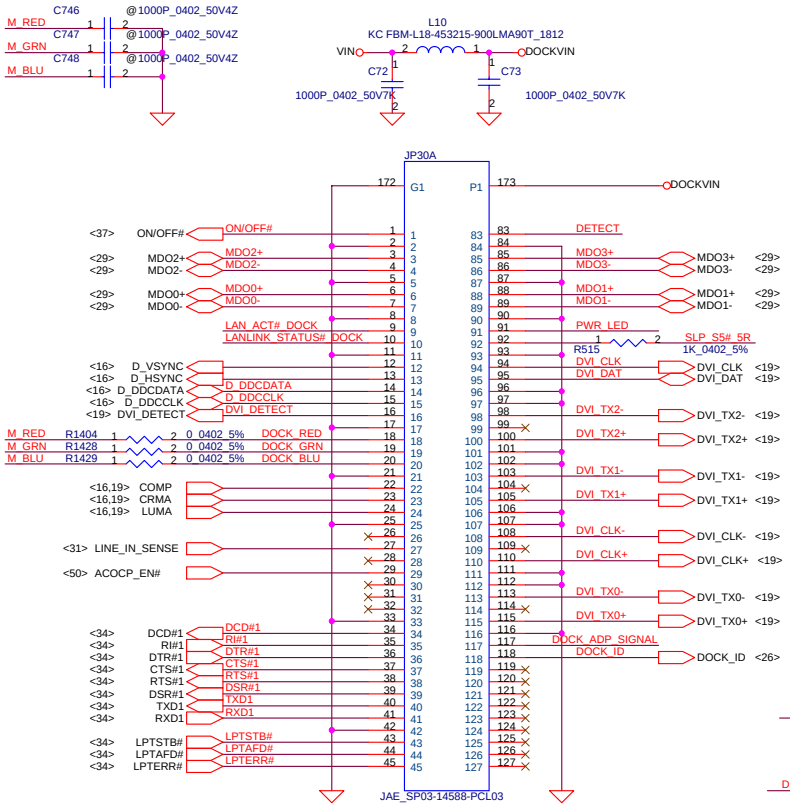
Compal Electronics, Inc.

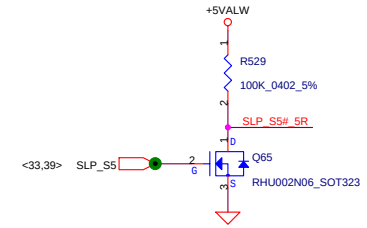
Title: MDC/KBD/ON_OFF/LID

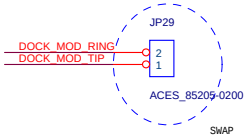
Size | Document Number: LA-2951 | Rev: 1.0

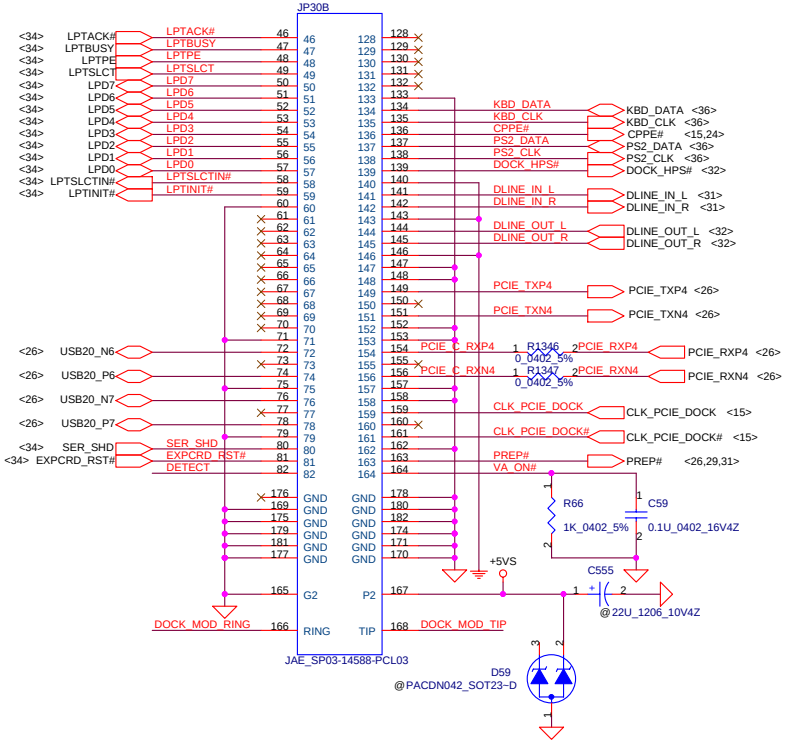
Date: Friday, April 28, 2006 | Sheet 37 of 54

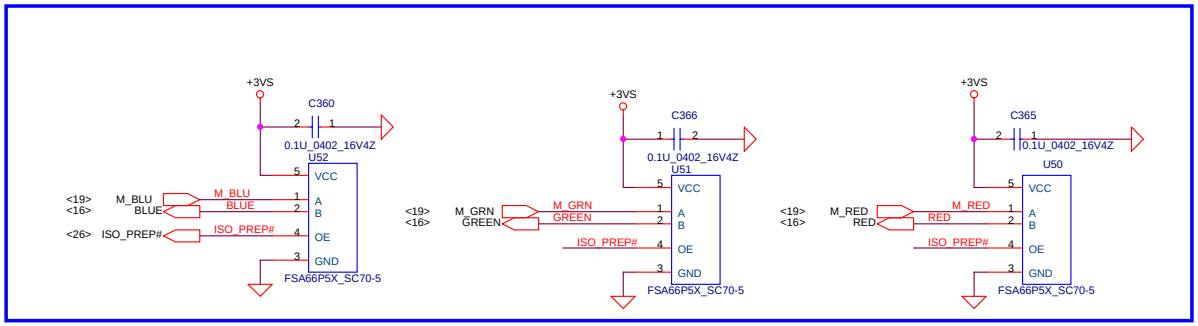
DOCK CONN. 184PIN

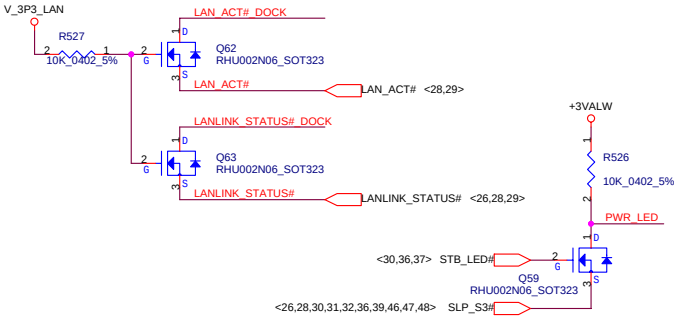












Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

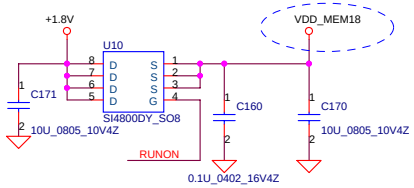
Title: **Docking CONN.**

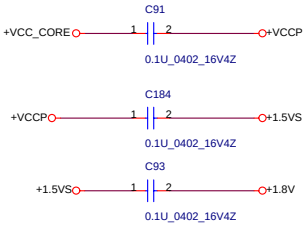
Size: Document Number: **LA-2951** Rev: 1.0

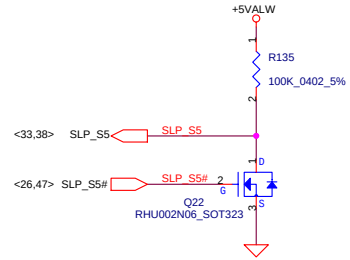
Date: Friday, April 28, 2006 Sheet 38 of 54

+1.8V to +1.8VS Transfer

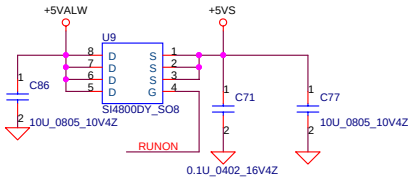
VRAM



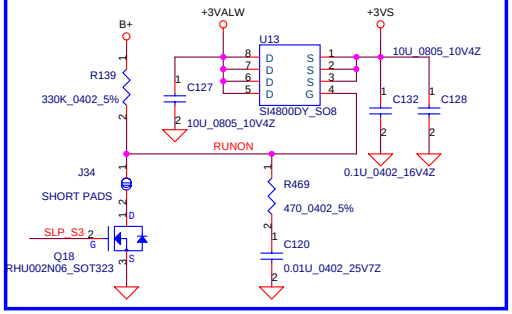


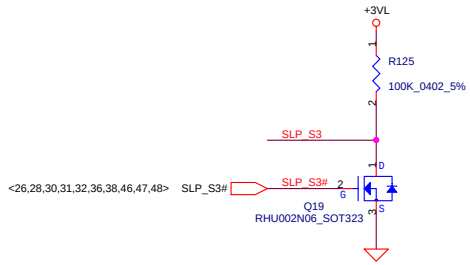


+5VALW to +5VS Transfer

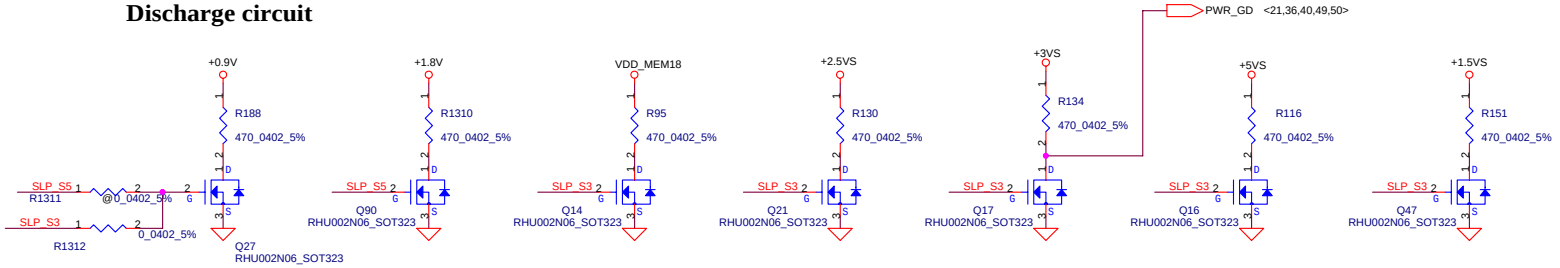


+3VALW to +3VS Transfer





Discharge circuit



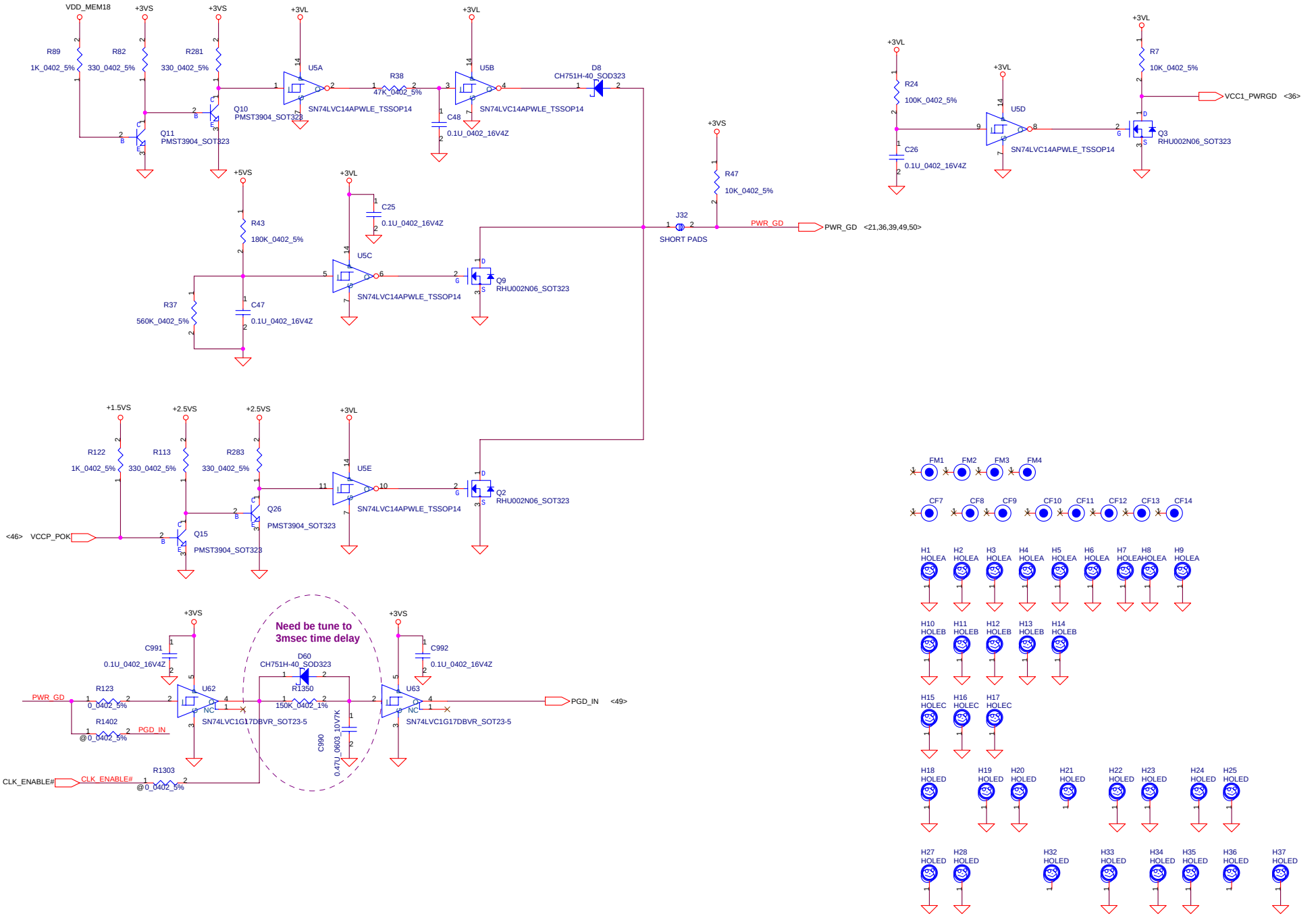
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **DC/DC Circuits**

Size | Document Number: *LA-2951* | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 39 of 54



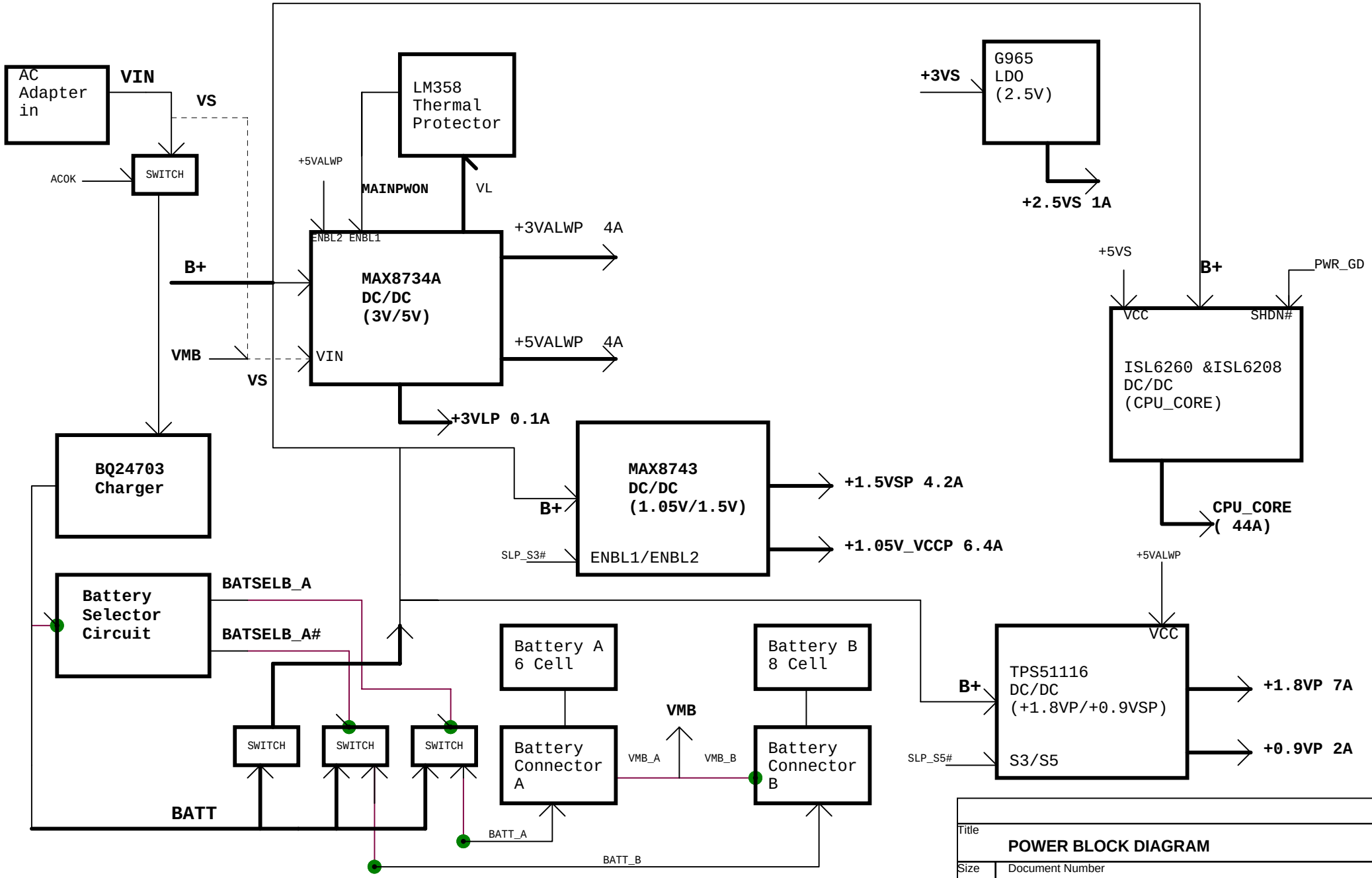
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

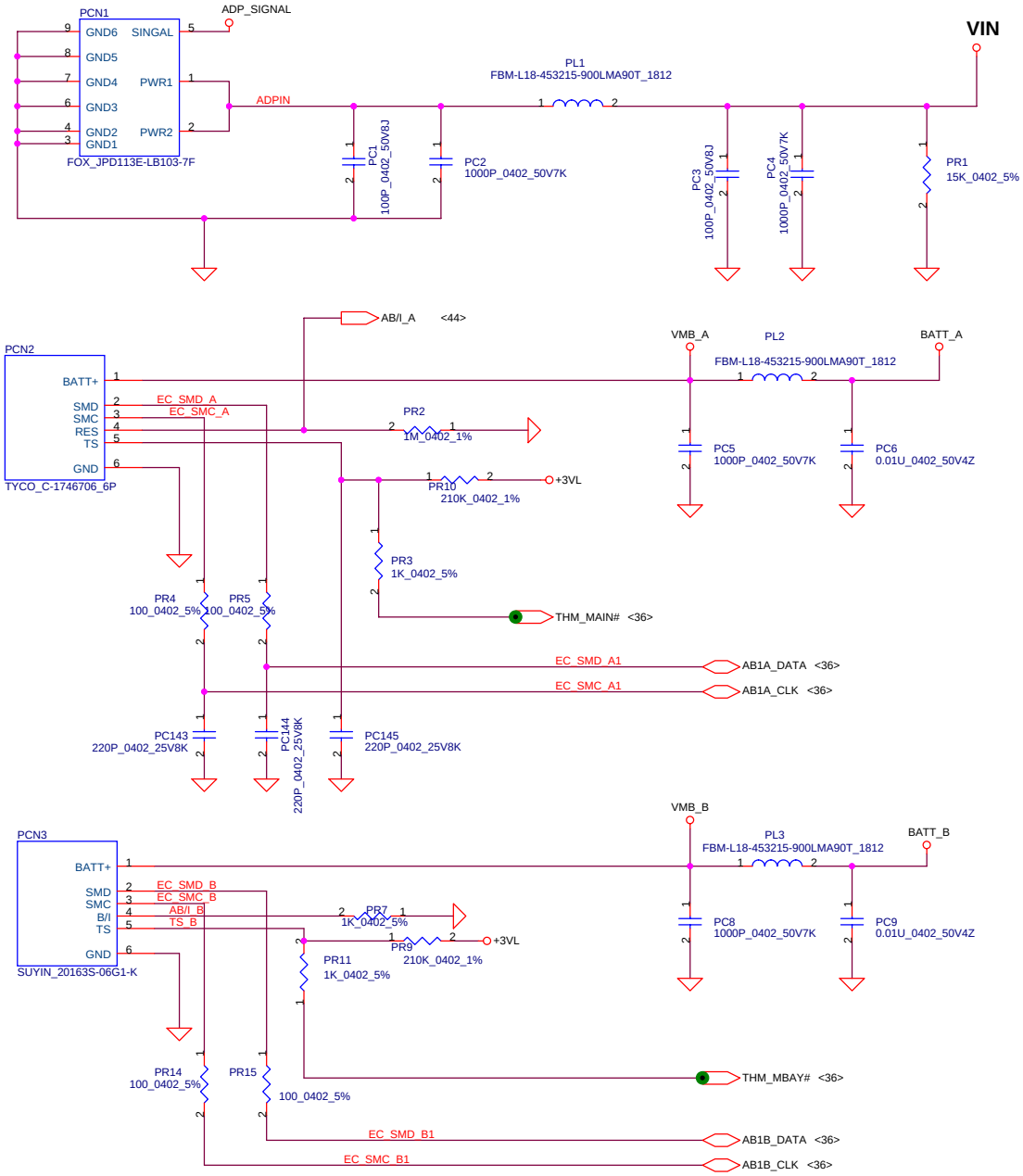
Title: **POK CKT**

Size: D | Document Number: **LA-2951** | Rev: 1.0

Date: Friday, April 28, 2006 | Sheet 40 of 54



Title	POWER BLOCK DIAGRAM	
Size	Document Number	Rev
Date: Friday, April 28, 2006	Sheet 41 of 54	



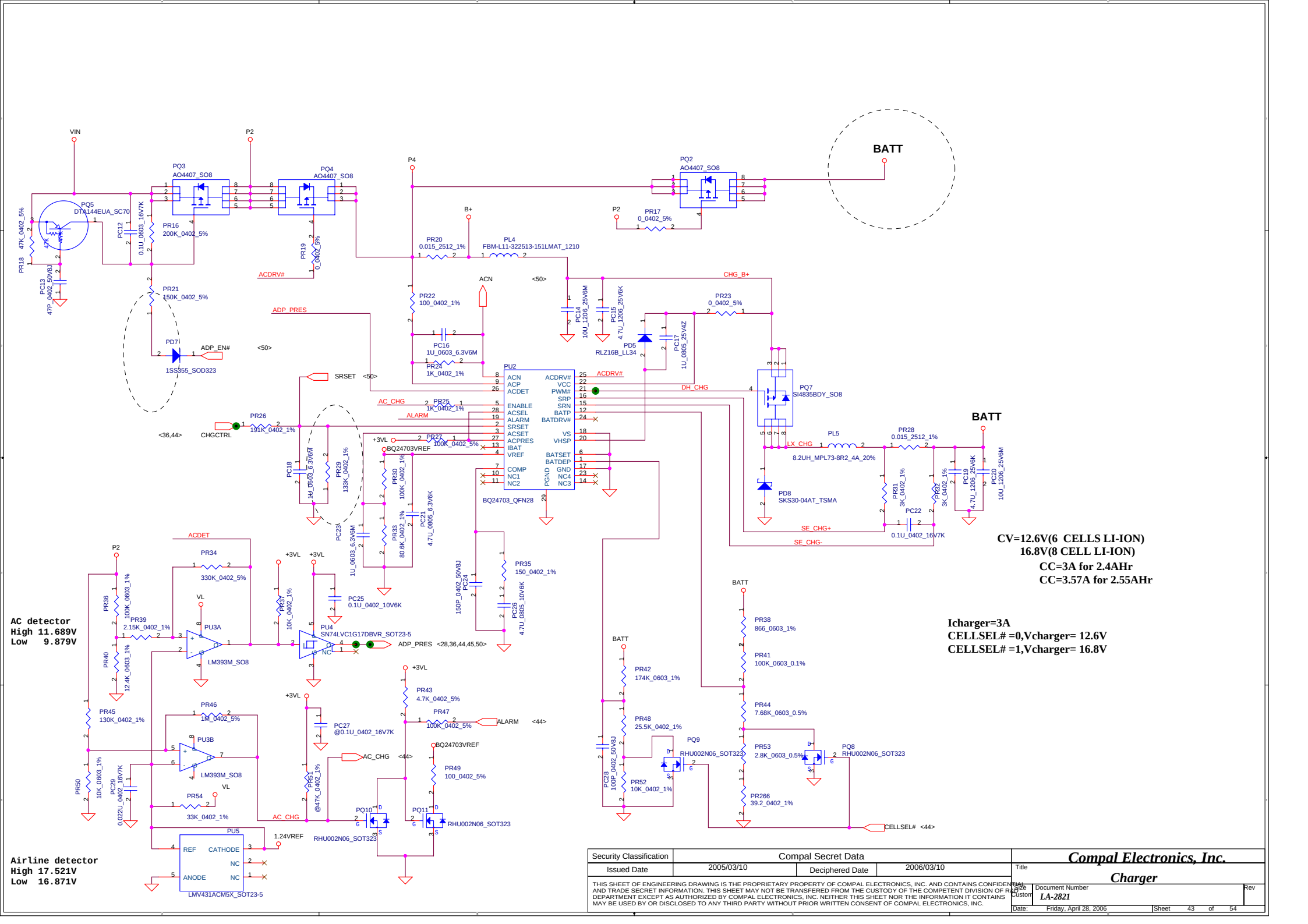
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **BATTERY CONN**

Size	Document Number	Rev
Custom	LA-2821	

Date: Friday, April 28, 2006 Sheet 42 of 54



CV=12.6V(6 CELLS LI-ION)
16.8V(8 CELL LI-ION)
CC=3A for 2.4AHr
CC=3.57A for 2.55AHr

Icharger=3A
CELLSEL# =0,Vcharger= 12.6V
CELLSEL# =1,Vcharger= 16.8V

AC detector
High 11.689V
Low 9.879V

Airline detector
High 17.521V
Low 16.871V

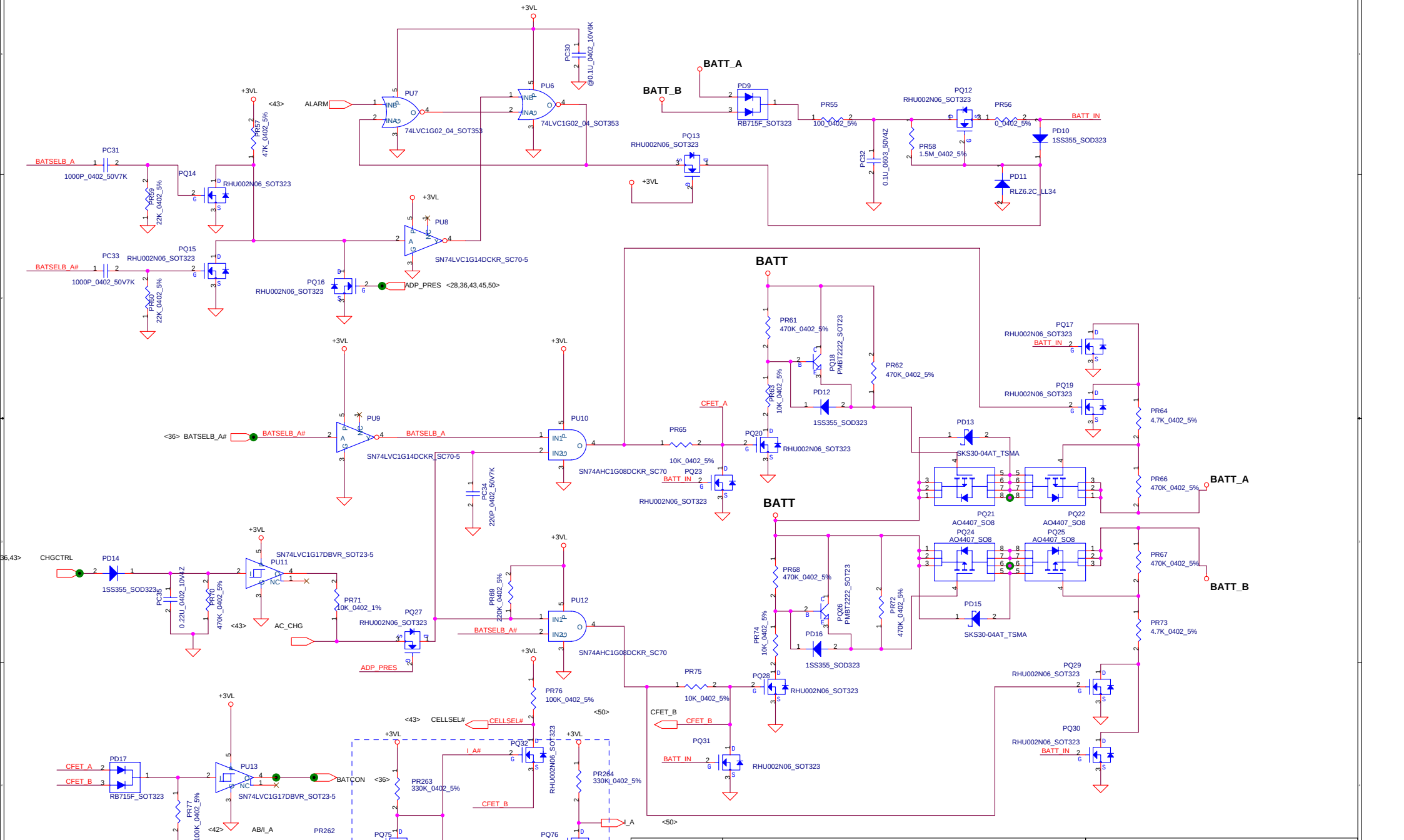
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Charger**

Size: Custom | Document Number: *LA-2821* | Rev:

Date: Friday, April 28, 2006 | Sheet 43 of 54



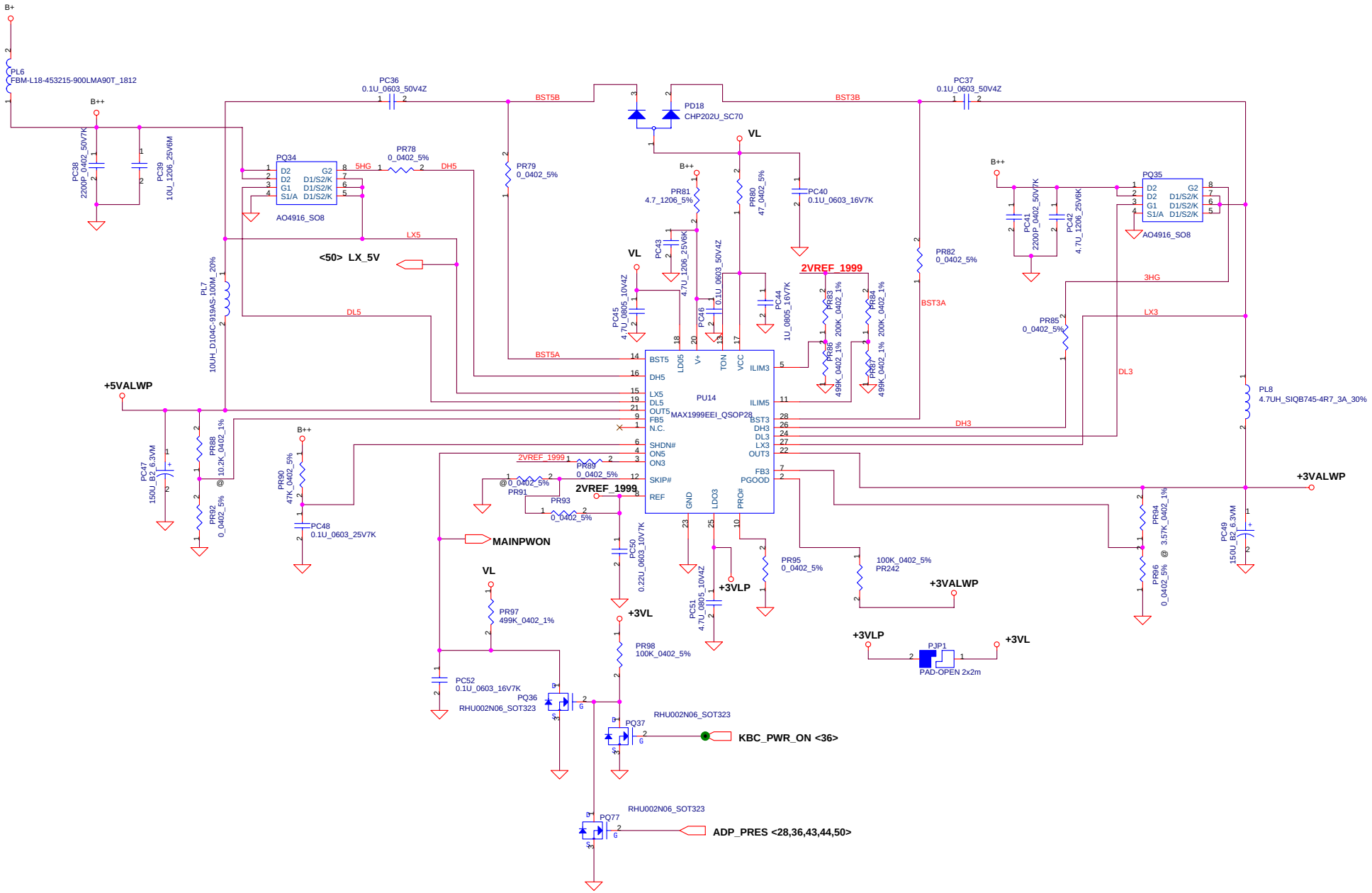
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Battery selector**

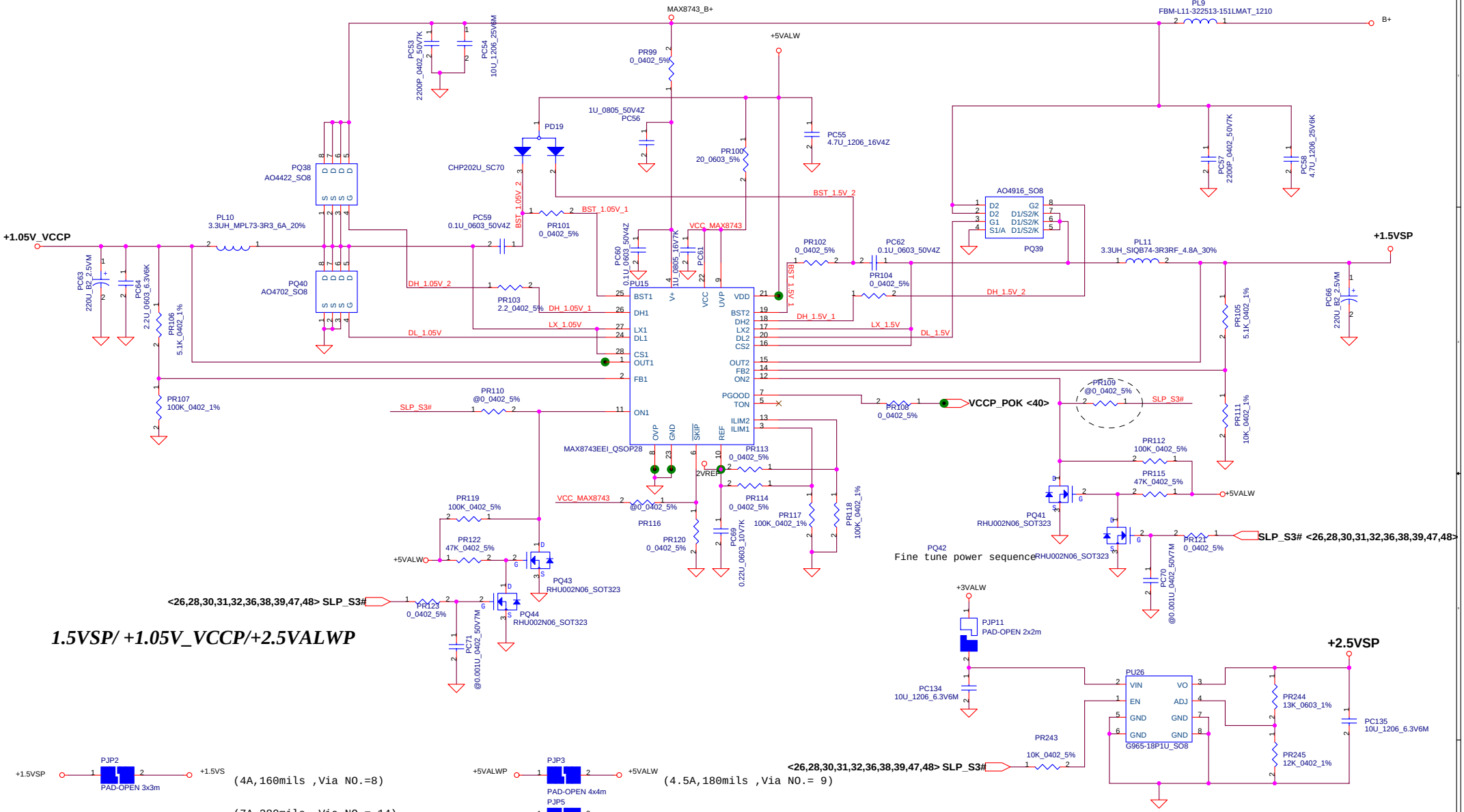
Size: Custom	Document Number: LA-2821	Rev
Date: Friday, April 28, 2006	Sheet 44 of 54	

+3.3V/+5V



Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2006/03/01

Title	3.3V / 5V	
Size: B	Document Number: LA-2541	Rev: 1.0
Date: Friday, April 28, 2006	Sheet 45 of 54	



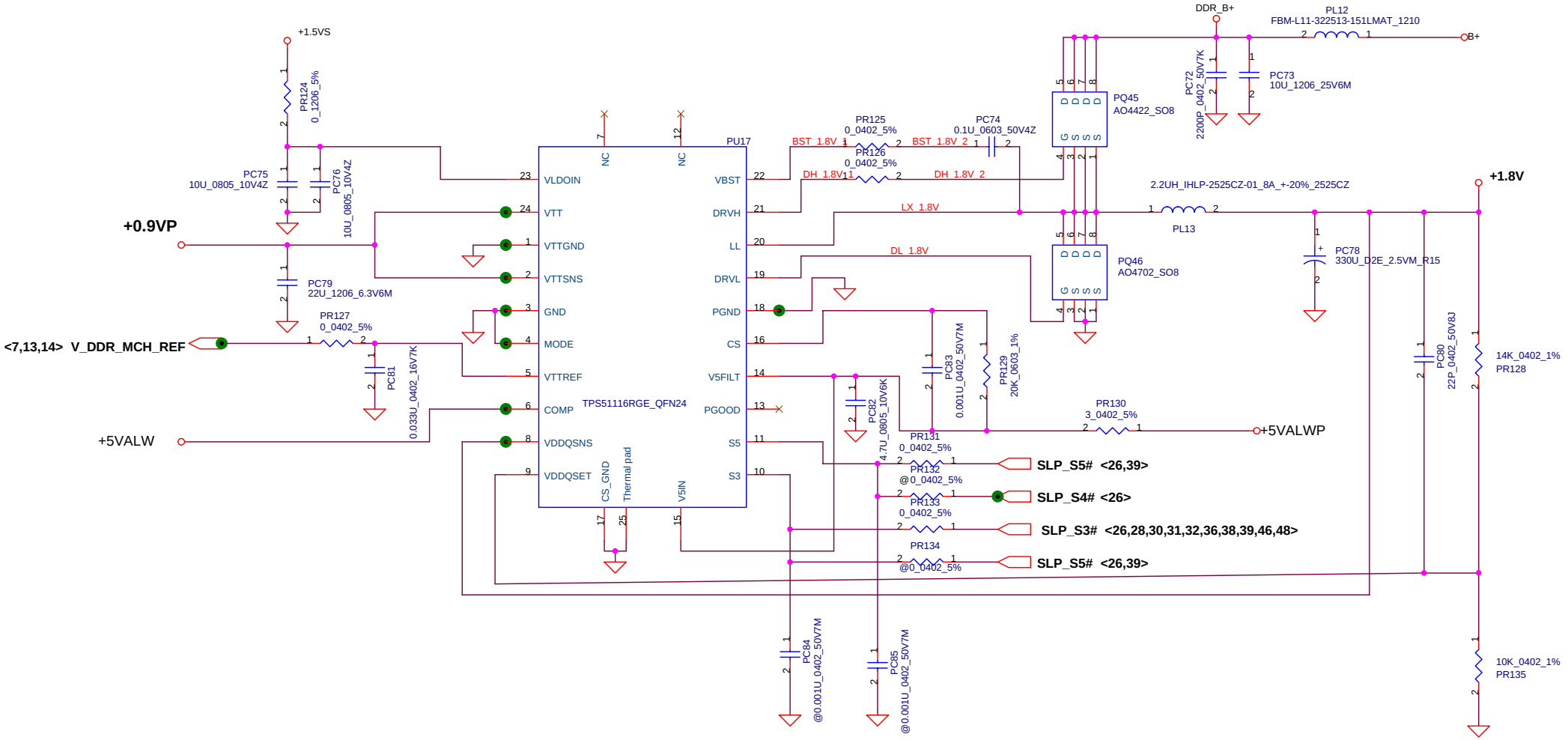
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: 2.5VALW/1.5VS/1.05VCCP

Size: Custom | Document Number: LA-2821 | Rev:

Date: Friday, April 28, 2006 | Sheet 46 of 54



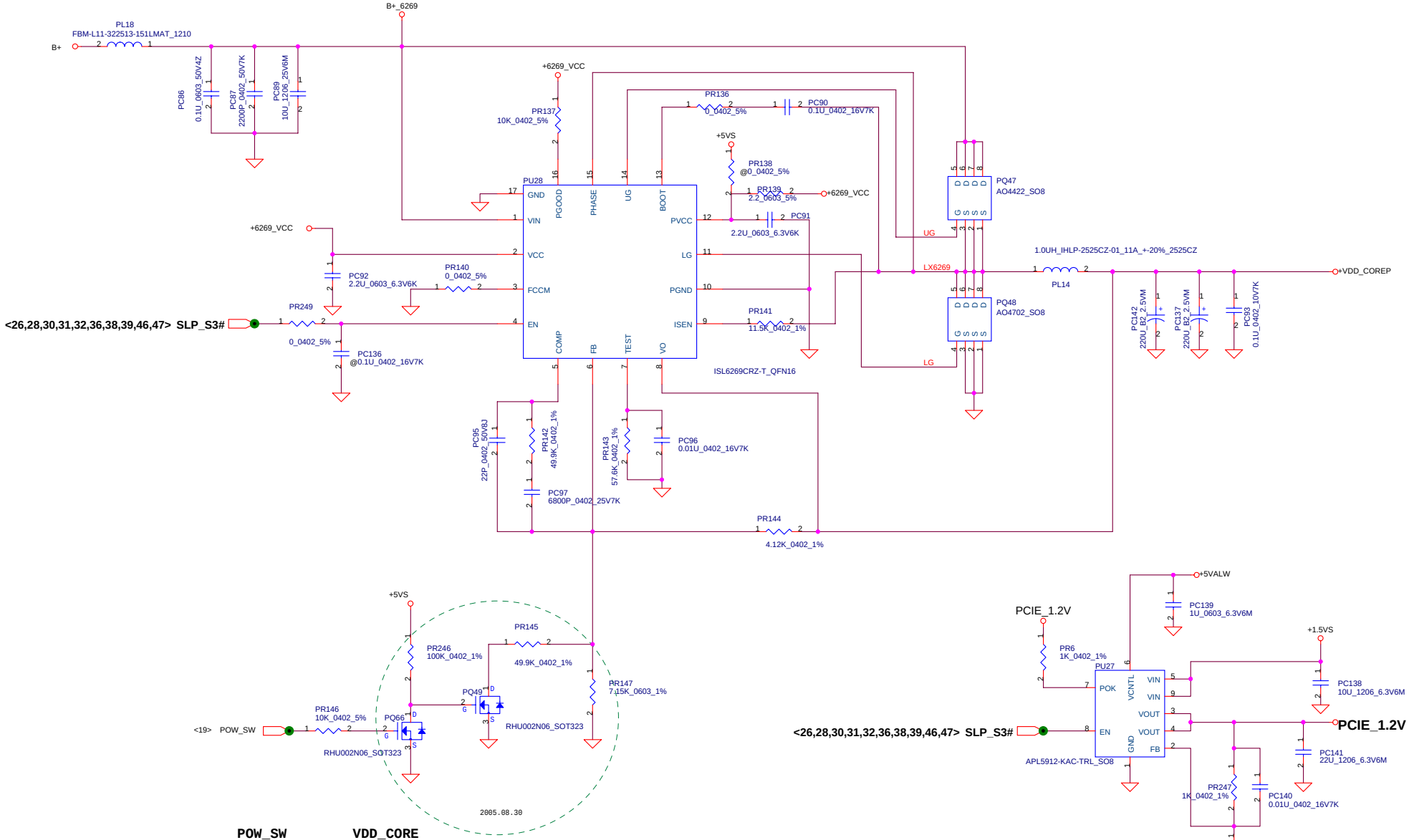
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **1.8V/0.9VS**

Size	Document Number	Rev
B	LA-2821	

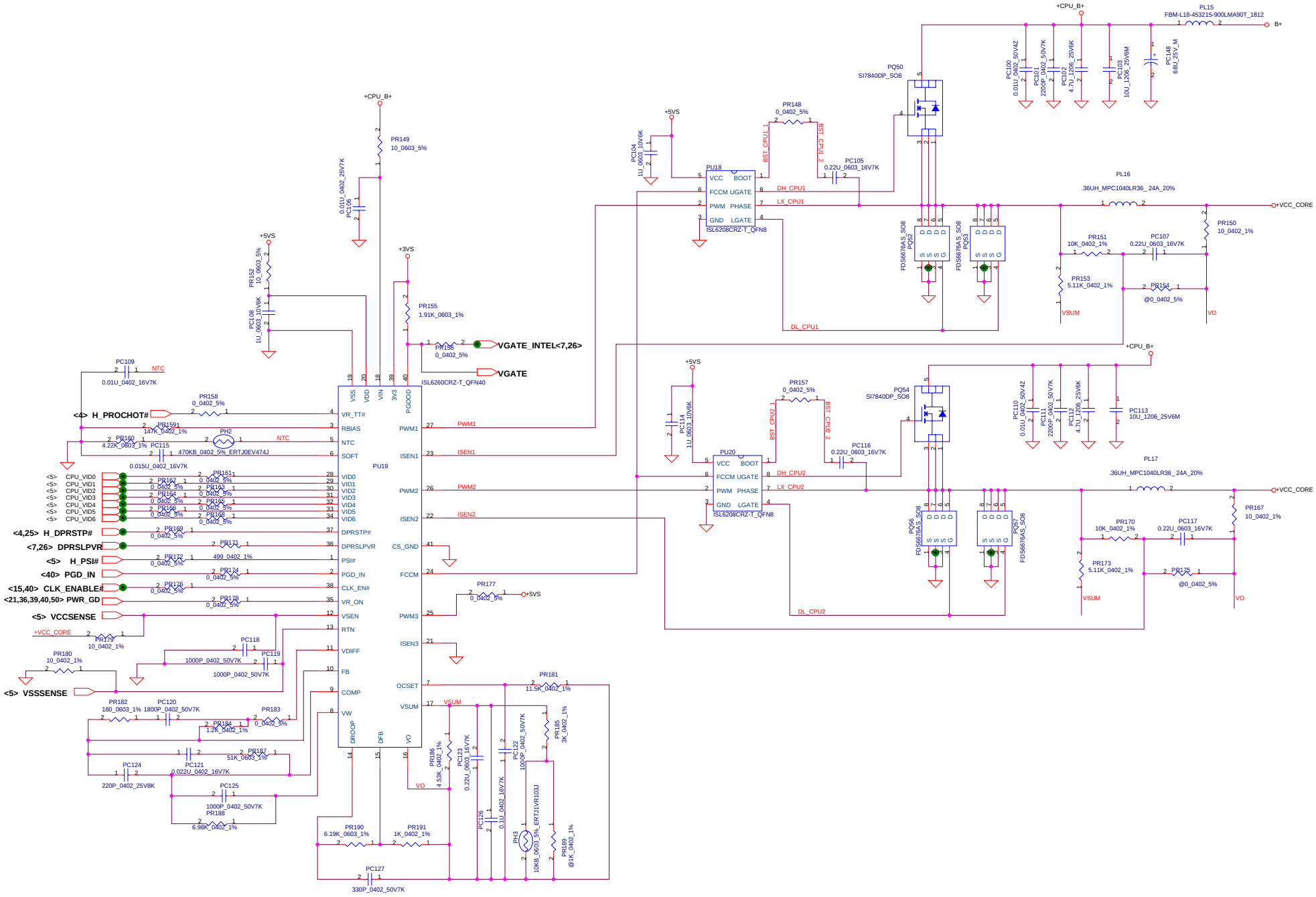
Date: Friday, April 28, 2006 Sheet 47 of 54



POW_SW	VDD_CORE
High	0.95V
Low	1V

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.			
Title	VDD_CORE		
Size: Custom	Document Number: LA-2821		Rev
Date: Friday, April 28, 2006	Sheet 48 of 54		



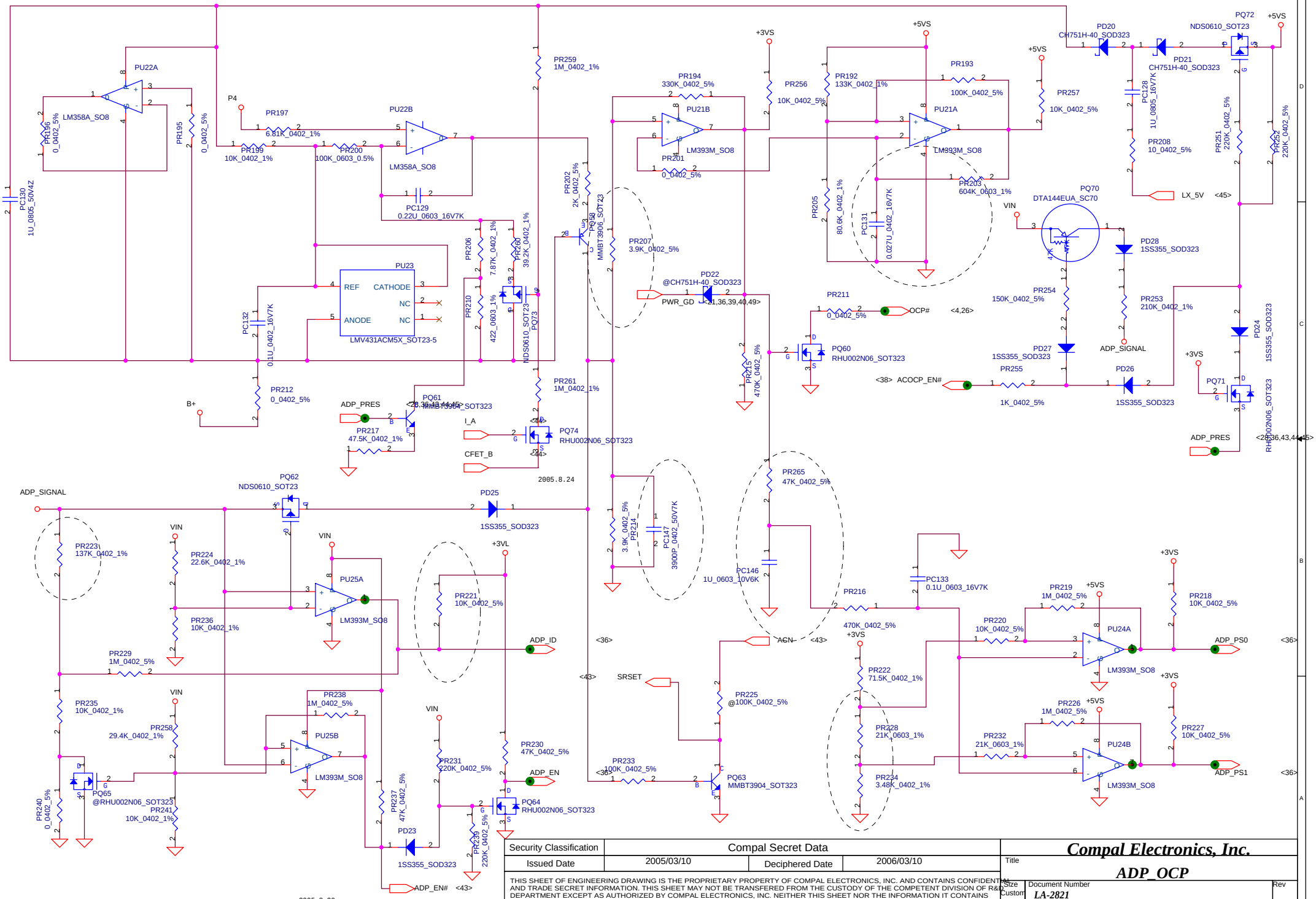
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **CPU_CORE**

Size: C | Document Number: **LA-2821** | Rev:

Date: Friday, April 28, 2006 | Sheet 49 of 54



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **ADP_OCP**

Size: Custom | Document Number: **LA-2821** | Rev:

Date: Friday, April 28, 2006 | Sheet 50 of 54

EE PIR list

06/01/2005 schematics review start :

06/02/2005

Page38 : Add R58,R59,R60 ,those are removed from daughter board

Page39 : JP18 pin3 change from ground to BT_LED

Page37 : Remove JP16 & change debug port interface to JP44

Page27 : ICH7M pin R7 change to +3VS

Page32 : JP44 PLT_RST# change to PLT_RST_B# to reduce the loading

Page33 : Update audio amp to MAX9710

06/03/2005

Page10 : Add R260 to reduce one 330U cap C666

Page25 : 1. R27 change to +3VS
2..Add R1035 for H_DPSLP#

Page26 : 1.Add T80 for GPIO25
2. GPIO21 change net name to VGARST#
3. Add T88 for GPIO23
4. Add T89 for GPIO26
5. GPIO30 change net name to USB_OC#6
6. GPIO31 change net name to USB_OC#7
7. Add R1036/7 for RESET option
8. Remove the connection of USB_OC#3/4/5

Page24 : Add ALS_EN on JP35 pin24 for light sensor

Page32 : 1.JP13 change to 90 pins connector
2.Add U72 for ESD protection

06/04/2005

Page10 : A. U71 change to U43D (the fourth gate in U43)
B. Add +3VS_TVBG R/C filters & voltage follower D12,D21,R127,R520

Page34 : audio change-- add R1419 ,R431,R434,R435 for BIASA/B/C

Page35 : Add JP3 for Smart card FFC connector

Page18 : 1.R1365 CHANGE TO 2K_0402_1%
2. R1366 change to 562_0402_1%
3. R1367 change to 1.47K_0402_1%

Page31 : JP4 update to RJ45 connector

Page15 :Add the connection for UMA VGA clock , & SRC0/2 SWAP
1.Add R1148/R1149 , R1129/R1132 , R1118/R1121
2.Add R1242/R1248,R1253/R1272

Page09 : Change 0 ohm resistors before filters ,
and delete the other group of filtes at page 19

Page16 : add R671~R678 ,R530,R531 for DVI

Page19 : Swap I2C bus for LVDS/Thermal sensor

06/07/2005

Page47 : PQ34 pin5/6/7 change netname to LX_5V

Page38 : Pin96: INVPWM rename to OUT9 & add T90

Page36 : Delete R500 & rename to EXPCRD_RST#

Page35 : Add JP3 for Smart card FFC connector

06/08/2005

Page7 : Delete PD resistor R1340~R1343.

Page17 : Update JP35 LVDS connector

Page26 : A. GPIO28 ==Delete R1321 & A_SD , change to VGA_RST#
B. GPIO21 ==Change to MB_PWR
C. GPIO19 ==Change to PD

06/09/2005

Page17 : Delete Q56 ,R510 ,Caymus support 3V PWM

Page25 : Update Q92 to AOS4407

Page26 : Delete R252

Page37 : Add PD RP42,R273

Delete Cardbus 6612 circuit & move to daughter board LS-2953

06/10/2005

Page17 : Add R458,R459 for ch_data,ch_clk

Page33 : Add C367 0.1U for +SC_PWR

06/11/2005

Page28: 1.Delete R15 ,due to Internal PD
2.Delete R69 ,due to Internal PD
3. Add U70,U71,R69,R92 R1297 for serial falsh support.

Page19 : Add T8/T9 for GPIO10/14

Page23 : Change L1,L2,L63,L6,L7,L9,L11-16,L65,L66 to FB

Page30 : Disconnect the I2C bus / WL_LED#/WP_LED# on JP46

Page10 : 1. Add R504/R505 for VCC_SYNC
2. Add R490/R491 for VCCTX_LVDS
3. Add R494 for VCCA_CRTDAC
4. Add R492/R493 for VCCA_LVDS
5. Add R495 for +3VS_TVBG
6. Add R500 for +3VS_TVDACA
7. Add R502 for +1,5VS_TVDAC
7. Add R499 for +3VS_TVDACB
8. Add R496 for +3VS_TVDACC

Page09 : 1.Add R460,R461, R550,R552,R553 for CRT discrete/uma option
2. Add R462,R463,R464 for TV discrete/uma option

06/13/2005

Page23 : Add R6 R15,R106,R128,R129 GPIO PD

06/14/2005

Page21 : Change L1,L2,L63 to FB

Page16 : 1. Add C174,C150,C142,C371,C358 for DVI
2. R103 change to 1%

Page35 : U69 pin7 change to PD

06/15/2005

Page04 : R1265 change to 51_0402_5% & install

Page07 : Install R1344

Page28 : Delete U70 ,reserve U71 for 200 mil

Page35 : Delete U61 , resevre U66 for 200 mil

Page29 : Update U7 symbol pinB7/B8/C8

06/16/2005

Page36 : Delete R32 ,double PU

Page41 : Delete R180,Q49 ,the same function for +1.8VS

Page10 : Delete C982 for Lead-free

Page20 : Add C570 for Lead free

Page32 : 1,Delete Q28 .
2. D49,D50 change to U73
3. Add C577,C581 for Lead free

Page33 : Add R163,R164,R165 for USB power switch PU

Page26 : Separate PCIE_WAKE# to NIC/Mini-card PCIE_WAKE# to avoid battery mode can't enter S3 issue

Page23 : Delete L65,C270,C269,C271 for M52-T

Page18~23 : ATI VGA controller change to M52T

06/22/2005

Page09 : Add R554 , R555 for CRT disable

Page10 : 1. Add R508,R510 for VCCD_LVDS1/1/2
2. R504,R505 chnage for +2.5VS_GMCH,&delete R490,R491,R492,R493

Page30 : Delete JP48,49 & change screw holes

06/23/2005

Page16 : Change SDVOB_INT+/- net name to PEG_RXP1/N1

Page10 : 1.R505 / R510 for M52 , R504 / R508 for UMA
2. R499,R500,R496 connect to +1.5VS for diable CRT

Page36: Delete R49 & CB_CLK

Page25: JP42 change to wire to board connector

Page19: 1.Add CRT,TV filters for M52T
2. Add DVI BOM option 0 ohm

Page16 : Move 0 ohm to TV-out connector for TV

Page38 : Move 0 ohm to docking connector for CRT

06/24/2005

Page19 : Add LVDS L-shape BOM option resistors

Page10 : Enable TV/ CRT when using 945PM

Page9 : Enable TV/ CRT when using 945PM

06/25/2005

Page33 : Delete U58, R165,C568,C1,C312,C311 FOR LAYOUT SPACE

06/27/2005

Change All 2N7002_SOT23 to RHU002N06_SOT323 to save layout space

06/28/2005

Page40 : Change Q10,Q11,Q15,Q26 from SOT23 to SOT323
to save layout space

Page37 : 1 . Update JP20 to 6 pin connector
2. Update JP20 & JP18 pin assignments to follow Taos

06/30/2005

Page28 : Y1 update to smaller package 6x3.5

Page25 : Y4 update to smaller package 14M-J

Page15 : Y3 update to smaller package 6x3.5

07/01/2005

Page23 : Add HW strpping pin on DVPDATA20,21,22,23 for VRAM ID0,1,2,3

Page33 : U57 change to 2A current limit power switch G548

07/04/2005

Page17 : Add R131 for inverter PWM when ATI PWM issue

Page19 : 1. Add R49 , R189 for 1.2V voltage divider
2. Add Q12 for M52_therm# & change to GPIO14

Page32 : The limitation for 5 pin audio jack can't switch
headphone/docking line-out ,so add R1420,R1421,C526,R252
Delete R256,R255,C536.

Page39 : Delete C984~C988

Page33 : Delete C527

Page10 : Delete C823 reserved pad

Page25 : Add JP5 slim type ODD connector

07/12/2005

Page25 : Add C629,C630,C631 for SATA connector

Page33 : Swap JP3 samrt card pin assignment for FFC

07/14/2005

Page25 : Add R133 100 ohm to avoid RTC short

Page15 : 1. clock gen. pin 5 change to connect to +ck_vdd_dp
2. C731,C732,C733 change from 0.1u to 0.01u
3. C361,C364 change from 33p to 27p

07/19/2005

Page39 : Add C91,C93,C181 for low speed signal

07/20/2005

Page30 : Add R1422 pad for XMIT_OFF

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.		
Title: H/W2 EE Dept. PIR SHEET		
Size	Document Number: LA-2951	Rev: 1.0
Date: Friday, April 28, 2006	Sheet 51 of 54	

For DB2 Modification

08/11/2005

Page31/32 : Update Audio portion for jack sensing
Page35 : Delete LED circuit & connect to LS-2953 directly
Page11 : Change R1154 to NI
Page30 : Add C554 for UIM power
Page25 : Delete JP37 MB2 conector
Page19 : Change C611 to NI ,R662 to 0 ohm for clcok spectrum
Page15 : Add R1136 PD for clk_pcie_m52 ,R1084 change to NI
Page24 : R1388 change to Install
Page26 : R1364 change to NI
Page36 : R1354 change to NI

08/15/2005

Page30 : R1418 , R1360 change to NI

08/19/2005

Page35 : Delete FWH , SPI change to +3VALW
Page36 :Delete R538
Page10 : Delete L39
Page25 : Add D15, D16 , R90 , R88 for HDD LED

08/20/2005

Page30 : Change +3VL / Caps_LED# to Pin45/51
Page38 : Delete R551 ,R548,R549,R541
Page25 : Add D15,D16,R88,R90 for HDD_LED
Page30 : Add SW1 C986, R521 , D65,D66 for SIM power off

08/24/2005

Page15 : Add C353~C372 for clk cap

08/25/2005

Page31/32 : Add JP16 for audio cable
Page30 : Internal MIC signal change to JP13

08/26/2005

Page32 : Add R427,R429,C492 for J_MIC_REF

08/29/2005

Page32 : Add 1423,R1424 for MIC_REF , & MIC_SENSE connection
Page23 : R154 change to NI
Page29 : Add C333 for NIC

08/30/2005

Page15 : Add C373 for clk_debug_port
Page23 : Add R173 for Therm_SCI#
Page36 : R538 change to NI
Page21 : Add C140, C172 , C141 , L17 for VDDPLL

08/31/2005

Page32 : Delete R1419, R1420
Page19 : R189 change to 56_0402_1%

09/07/2005

Page23 : Add R174 for ATI GPIO5

10/06/2005

Page24: NI D64 ,install R1355
Page07: NI R1202,R1203
Page15: Del R1148,R1149,R1129,R1132
Page07: Add R103,R105,R107,R110.
Page10: Del R1337
Page28: NI R1397,U36 ; Install Q94 ; Add R1039
Page35: Reserve U61
Page36: Install R91
Page30: Add R1383 ; Reserve R1382

10/07/2005

Page30: Add R1071,R1073
Page07: NI R1209

10/07/2005

Page28 : Install R275,R289 ; NI R1396,R1398
Page28 : Del Q71,R1345 ; Install R1395,R1384
NI R1425,R1385
Page29 : Add R1040,R871 ; Del R1404 ; Reserve Q106
Page28 : Add R1091,R1082,R1088,R1085,Q105,R1023,
R1024,D63,C1042,U55,R1021,R1076 ;
Reserve Q103,Q104,R1090,
Del R601.
Page15 : Del R1084,R1136

10/08/2005

Page28 :Install Q103 ; NI R1091

10/13/2005

Page24 :Delete BIOS_SEL jump
Page39 :Delete J33

10/26/2005

Page5 :NI R243
Page32 :NI C526
Page19 :R11 and R13 change to 499 ohm
Page37 :Install CP1~CP6

10/31/2005

Page06 :NI C933 ; Modify 330U cap from ESR9 to ESR7.

11/01/2005

Page19 :Change R124,R126,R132 and R178 to 150 ohm.

For SI2 Modification

12/06/2005

Page06 :Del C938.
Page19 :Change R126,R124,R132,R178 to 100ohm
Page25 :Del C646
Page26 :Del R1384,R1385,R1425 ; Connect LP_EN# to GPIO8
Page30 :NI R1355 , Install D64
Page34 :Del U45,U48,R1306,R117,R1307,C33,C993,C87
Page36 :Change RP43,44 to 10K ohm
Page37 :exchange netname between JP18's pin 25 and 24

12/13/2005

Page15 :Add C740,C741,C744,C745 for EMI request

12/14/2005

Page26 :Add Q43 to be a HALT LED inverter.
Page37 :Add R1084 and reserve R1094

12/16/2005

Page28 :Del U71,R69,R92,R1297 footprint
Page30 :NI R1364,Install R1363
Page37 :Add C749,C750,C751
Page38 :Add C746,C747,C748 and
change R1404,R1428,R1429 to 0603 size

12/21/2005

Page37 :Add D67 for EMI request
Connect JP20's pin 1 to +3valws directly
Page38 :Add D59
Page15 :Change C361,C364 to 18pF
Page36 :Change C350,C349 to 18pF
Page25 :Change C516,C528 to 15pF
Page19 :Change C610,C611 to 18pF

12/22/2005

Page06 :Del C934,install C933

12/27/2005

Page07 :Install R1201,R1204
Page15 :Change R1111,R1115,R1075,R1081 to 22 ohm.

For PV Modification

01/16/2006

Page07 : UI R1201,R1204 for SI2 shut down issue
Page15 : Change R1070,R1072,R1075,R1081,R1093,R1095,
R1118,R1121,R1257,R1259,R1144,R1145,R1123
R1126,R1113,R1111,R1115,R1143,R1249,R1251
to 24Ω for CLK GEN vendor's recommand.
Page30 : Change R996 to SM010014500(220Ω impedance)
for improve WLAN performance

02/07/2006

Page30 : Modify R996 to 1000ohm/100MHz bead
Modify R996's location to L78
For power noise impact WLAN performance

Page30 : Connect R1363.2 to V_3P3_LAN
INSTALL R1363, UI R1364
For support wake on WLAN from S3.
Page15 : Install R1245 and UI R1247
Page37 : Change Num_LED# and CAPS_LED#
For LED reverse issue

02/13/2006

Page35 : Del U61. (150mil SPI ROM)

02/14/2006

Page26 : Add R1437
For HALTLED turn on 100ms when power on.
Page15 : Add C355,C356,C357,C358,C368,C369,C371,C372
To improve WWAN performance

02/20/2006

Page21 : Add C143,L21.Change C109 and C112 to 1u cap.
For PCIE_1.2V power noise.
Page23 : Change C195 to 1U cap.
For PCIE_1.2V power noise.
Page32 : Connect JP24 and JP15's 7 and 8 pin to DGND.
For ESD concern.

02/23/2006

Page33 : Add D51,D52,D61 for ESD issue.

03/02/2006

Page21 : Change C143,C116 to 22u for PCIE_1.2V noise
Page23 : Change C190 to 22U for PCIE_1.2V noise

03/08/2006

Page30 : Change R521 to 1K for SW function error
Page32 : Change R1405 and R1406 to 12.1K

For MV1 Modification

03/22/2006

Page19:Change R189 to 75Ω(Improve clock amplitude)
Page21:Change C103,C104,C105 to 1U, Add C144
Improve DVI signal
Page25:Change Y4 to MC-146 (Original is non LF part)
Page28:Change R70 to 1.21KΩ

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Title	*Compal Electronics, Inc.*	
	H/W2 EE Dept. PIR SHEET	
Size	Document Number *LA-2951*	Rev 1.0
Date: Friday, April 28, 2006	Sheet 52 of 54	

04/07/2006

Page16 : Change C310,C313,C314 to 18P
For CRT EMI issue

Page19 : Change L23,L24,L25 to 0 ohm；C182,C180,C181 to 12P
Change L18,L19,L20 to 39nH inductor
For CRT EMI issue

04/19/2006

Page16 : change R542,R543,R544 to 56ohm bead for EMI issue

04/28/2006

Page17 : UnIstall R501, duplicate PD resistor

Page28 : Install R1022 and UI R1021
For clock can't shut down under DC mode

	Compal Electronics, Inc.	
Title	H/W2 EE Dept. PIR SHEET	
Size	Document Number: LA-2951	Rev 1.0
Date: Friday, April 28, 2006	Sheet 53 of 54	

Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	42,44,50		8/26/2005 (DB)	HP	To implement 4 cell main battery	Add PR2,PR259,PR261(1M ohm), Add PQ73,PQ74,PQ75,PQ76(RHU002N06_SOT323) Add PR260(39.2k)	DB
2	48		8/30/2005 (DB)	HP	To fix VDD_CORE in 1V.	Remove PQ49,PQ66	DB
3	50		10/18/2005 (SI)	HP	Changes for OCP circuit	Add PC147 3900pF capacitor across PR214 Change PR207 from 0 Ohm to 3.9K_5% Change PC131 from 0.22uF to 0.027uF Change PR203 from 649K to 604K_1% Change PR221 from 47K to 10K_5% Add a newPR265 47K_5% resistor in series with PR216-2 Add a new PC146 1uF X7R capacitor from PR216-2 to GND Change PC133 from 10uF to 0.1uF X7R Change PR228 from 10K to 21K_1% Change PR234 from 11.5K to 3.48K_1% Change PR232 from 3.3K to 21K_1%	SI
4	43		10/18/2005 (SI)	HP	sets Max charge current to 3.75A)	Change PR29 from 100K to 143K_1%	SI
5	50 43		12/06/2005 (SI2)	HP	Changes for OCP circuit	PR225 is open and PR26.2 connects to PQ63.1	SI
6	50		12/12/2005 (SI2)	Compal	Correct PR223 value.	Correct PR223 from 180K to 137K	SI2
7	47		12/19/2005 (SI2)	Compal	DRR2 issue	Change PC78 from 220u to 330u Delete PC81,PR127	SI2
8	49		12/21/2005 (SI2)	Compal	OTS#181928 Electrical printed circuit assembly acoustic noise test fail	Add PC148(68uF)	SI2
9	47		01/16/2006 (PV)	Compal	For 1.8V thermal shut down issue	Add PC81,PR127	PV
10			02/08/2006 (PV)	compal	OTS#184638 SVTP_SI1:PC Card Wireless Radio Interference fail on GSM 850 and GSM 900 channel.	Change PL8,PL11 to shielded inductors	PV
11	43		02/17/2006 (PV)	HP	This change will slightly increase the battery life	Change PR38 to 866_1% Ohms Change PR41 to 100K_0.1% Change PR44 to 7.68K_0.1% Change PR53 to 2.80K_0.5% Add a 39.2_1% resistor in series with PR53. Connect one end to PR53.2 and the other end to GND.	PV

Title	PWR PIR Sheet (1)		
Size: Custom	Document Number: LA-2541		Rev: 1.0
Date: Friday, April 28, 2006	Sheet 54 of 54		