

Compal confidential

Schematics Document

Mobile Yonah uFCPGA with Intel
Calistoga_GM/PM+ICH7-M core logic

2006-05-19

REV:0.1

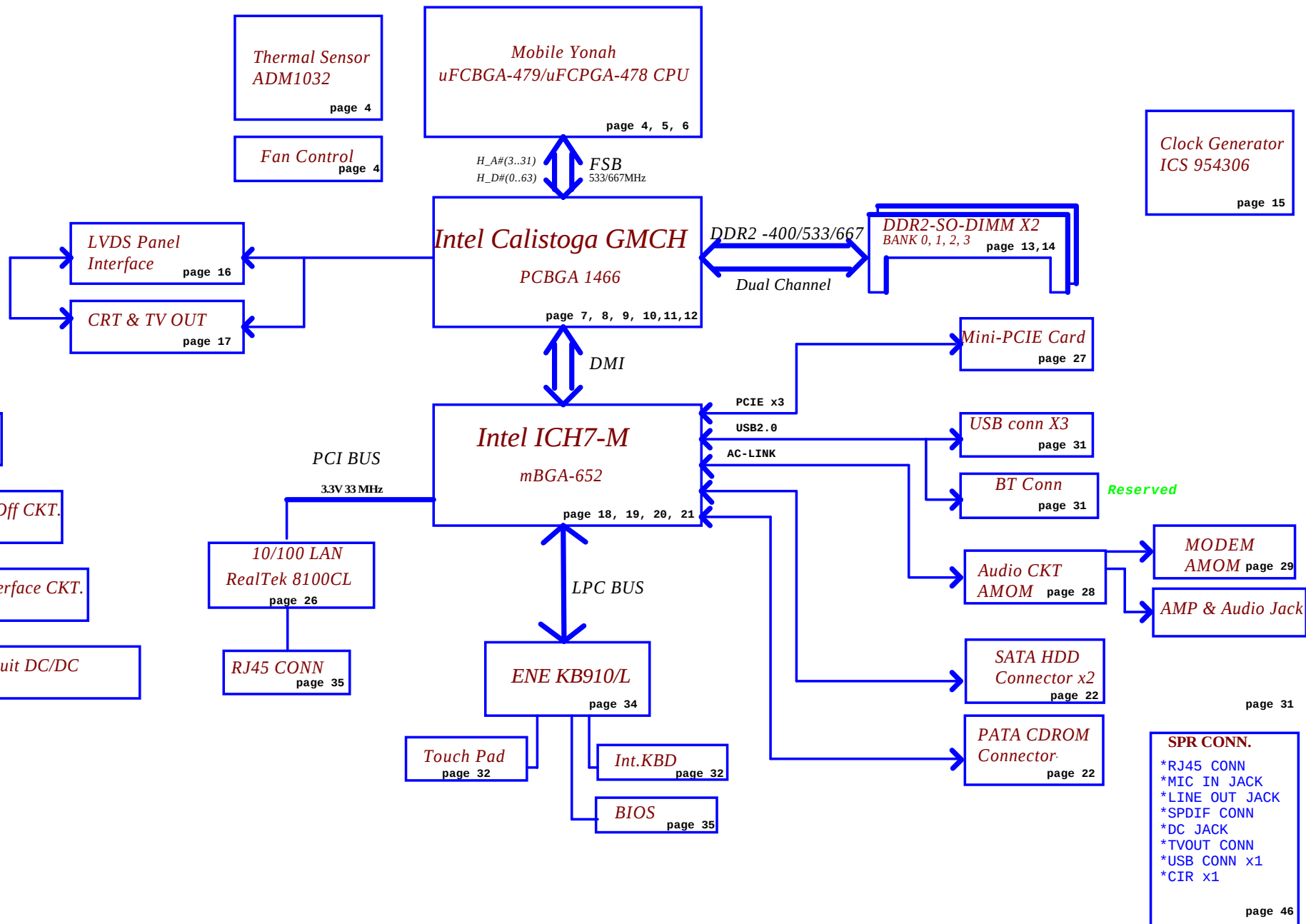
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Voltage Rails

power plane State	+B LD03 LD05	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.5VS +0.9VS +CPU_CORE +VCCP
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

0 MEANS ON
X MEANS OFF

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G
RealTekK 8100CL	AD24	1	E

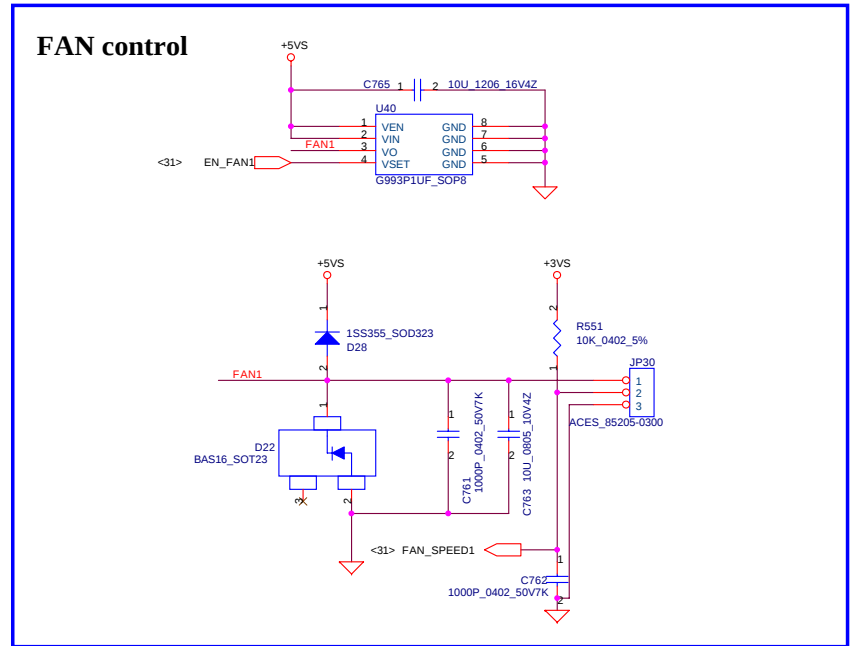
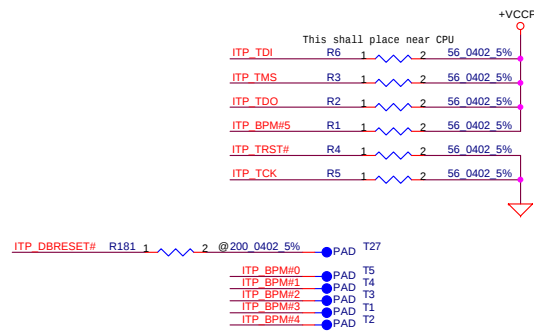
Load BOM check item

- 1.U31 GM/PM/GML part number
- 2.U6 ICH7 part number

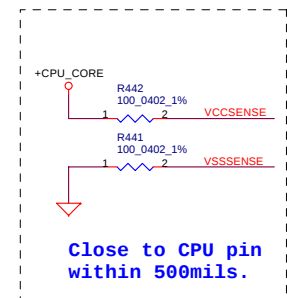
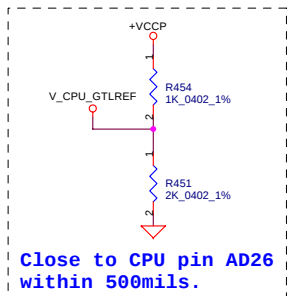
BOM: 43144132L01 (GM)
43144132L02 (GML)

Jump-Short:

PJP4,PJP6,PJP7,PJP8,PJP10,PJP12,PJP14,PJP18,PJP19,PJP20,PJP25



Security Classification	Compal Secret Data			Compal Electronics, Inc. Yonah CPU in mFCPGA479		
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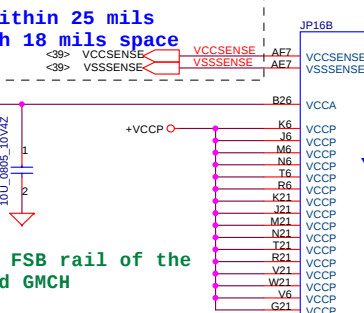
+1.5vs is a power source required by the PL clock generator on the processorsilicon

Length match within 25 mils
The trace width 18 mils space
7 mils

+VCCP is the FSB rail of the processor and GMCH

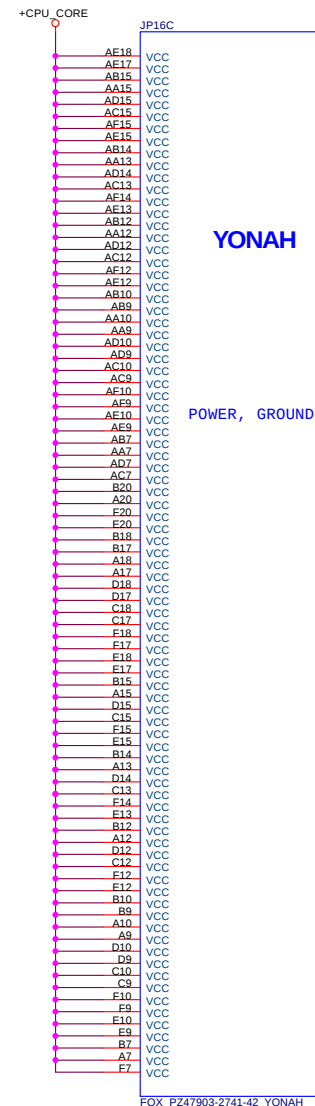
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal.



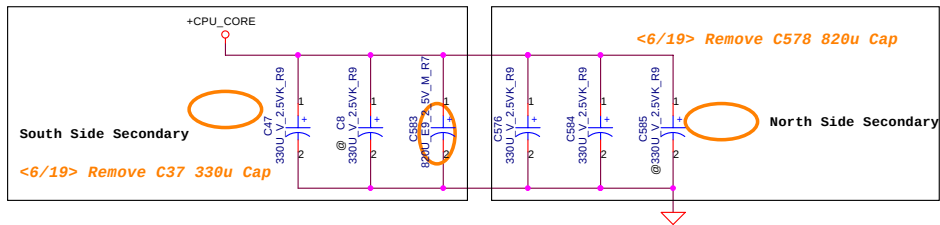
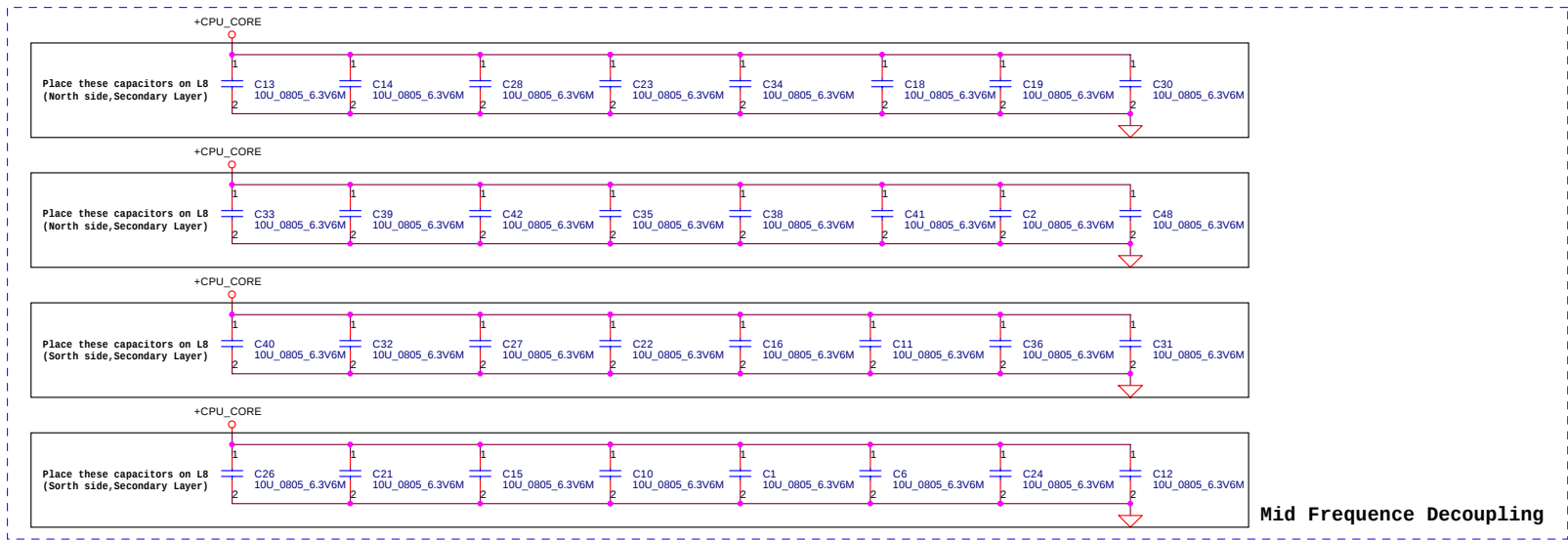
YONAH

POWER, GROUND, RESERVED SIGNALS AND NC

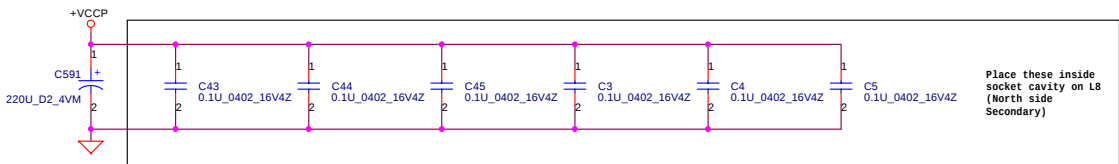


YONAH

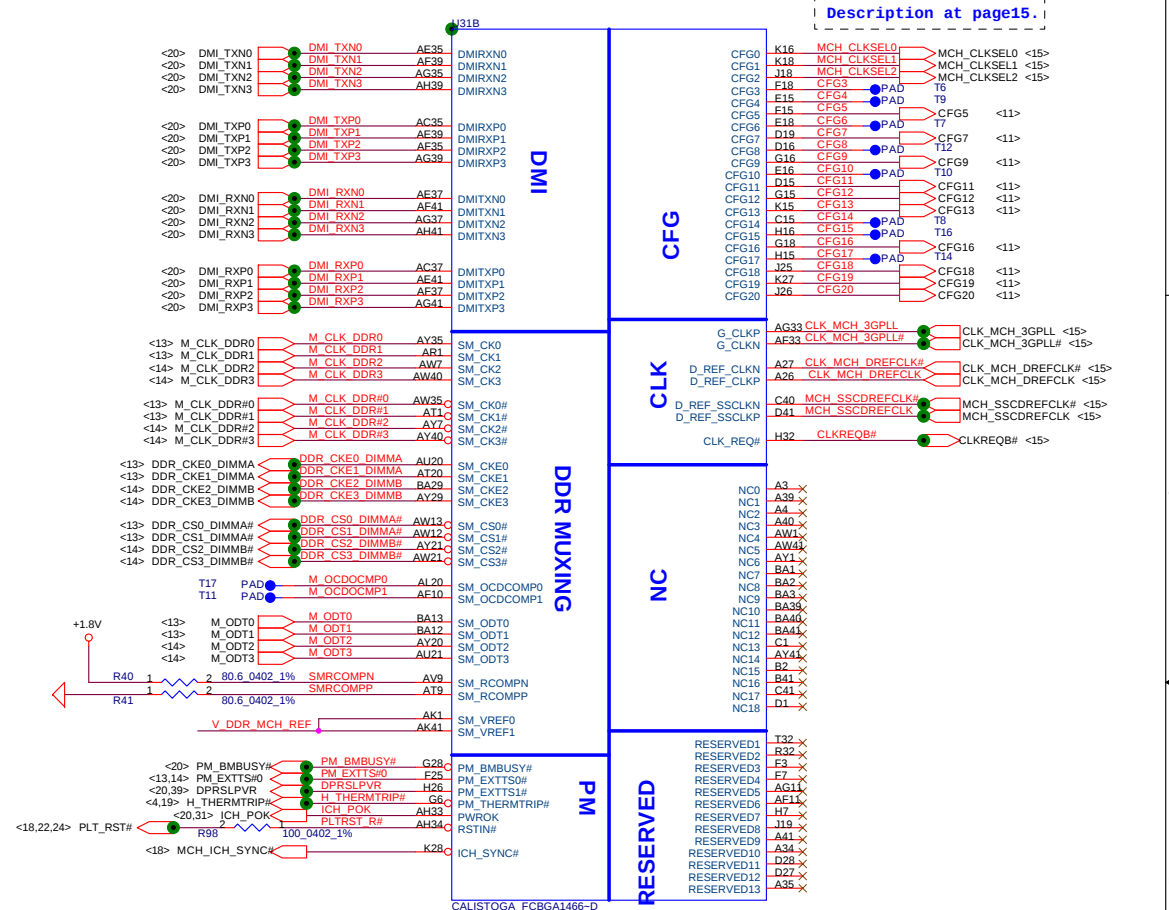
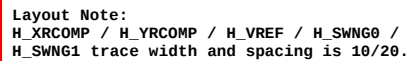
POWER, GROUND



ESR <= 1.5m ohm
Capacitor > 1980uF



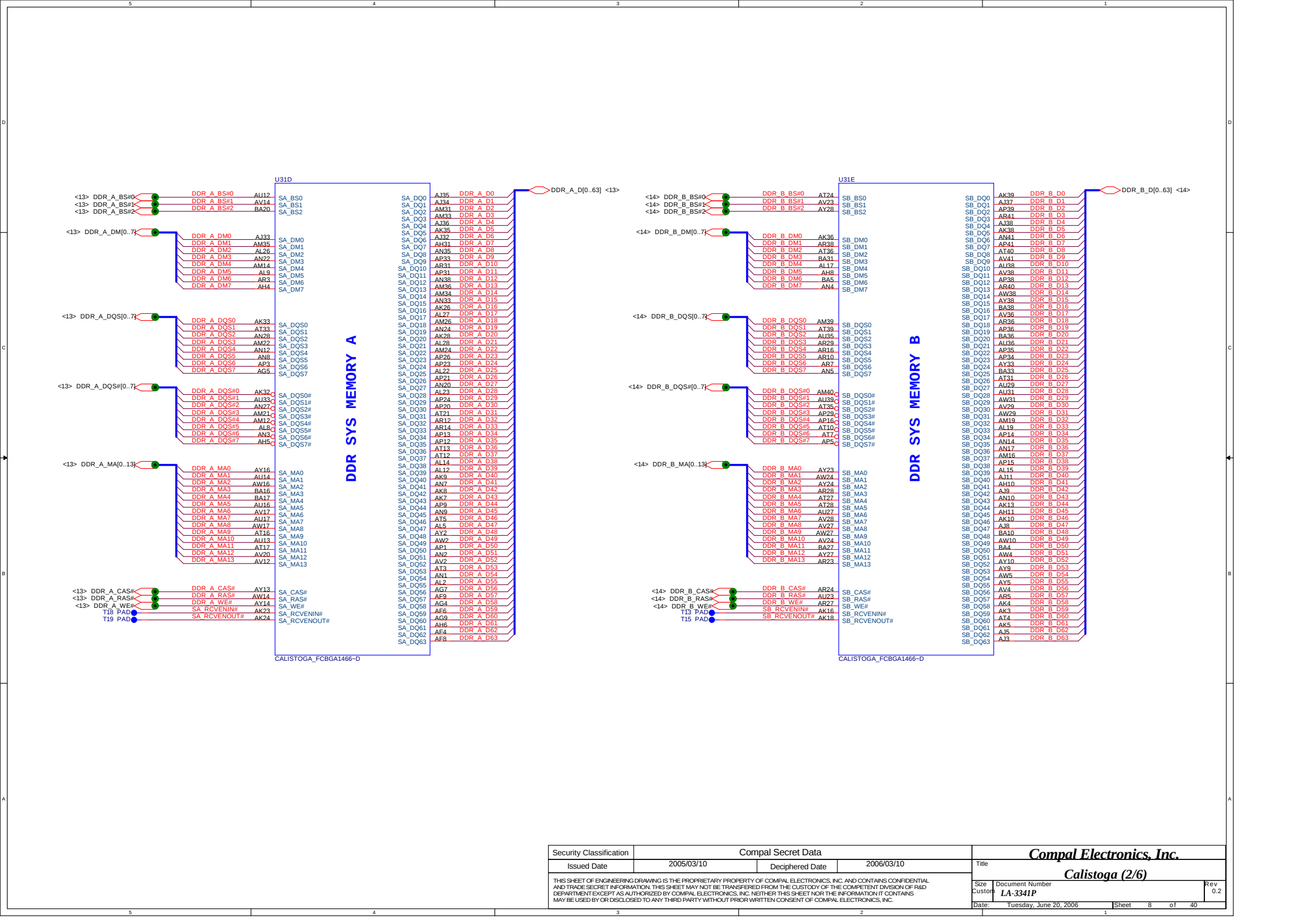
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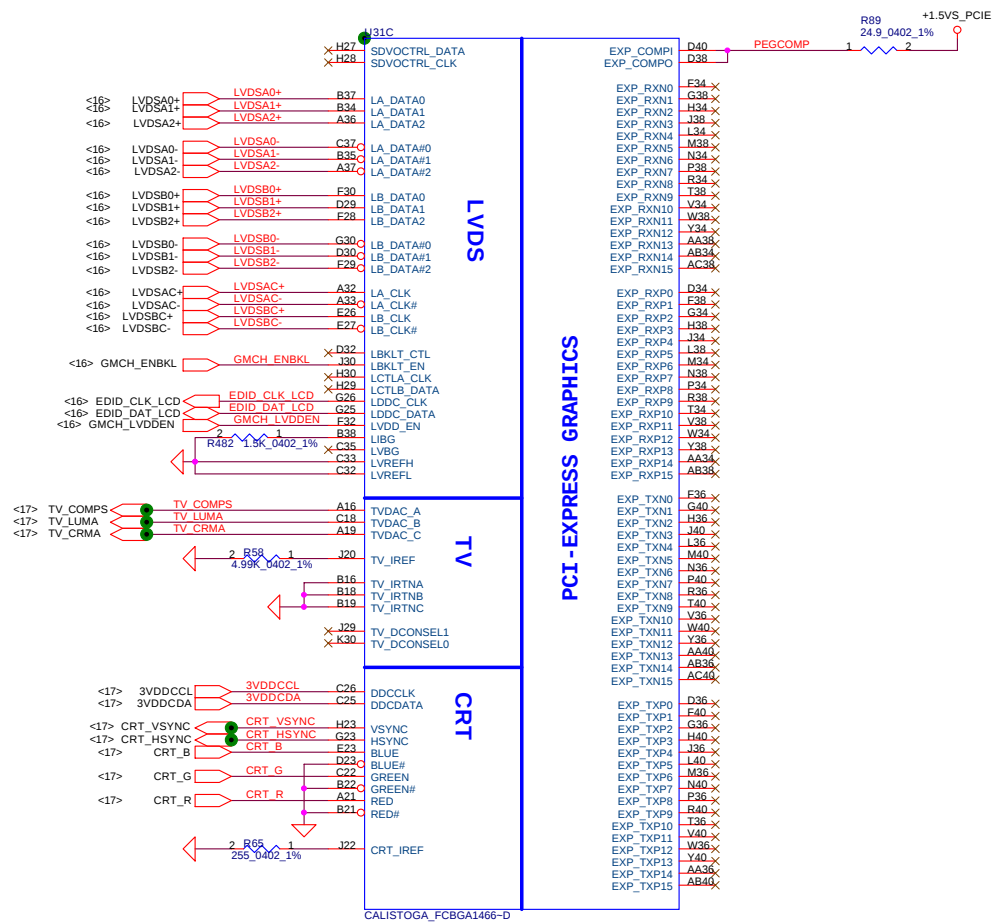


Layout Note:
V_DDR_MCH_REF
trace width and
spacing is 20/20.

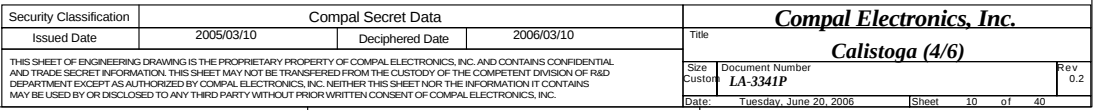


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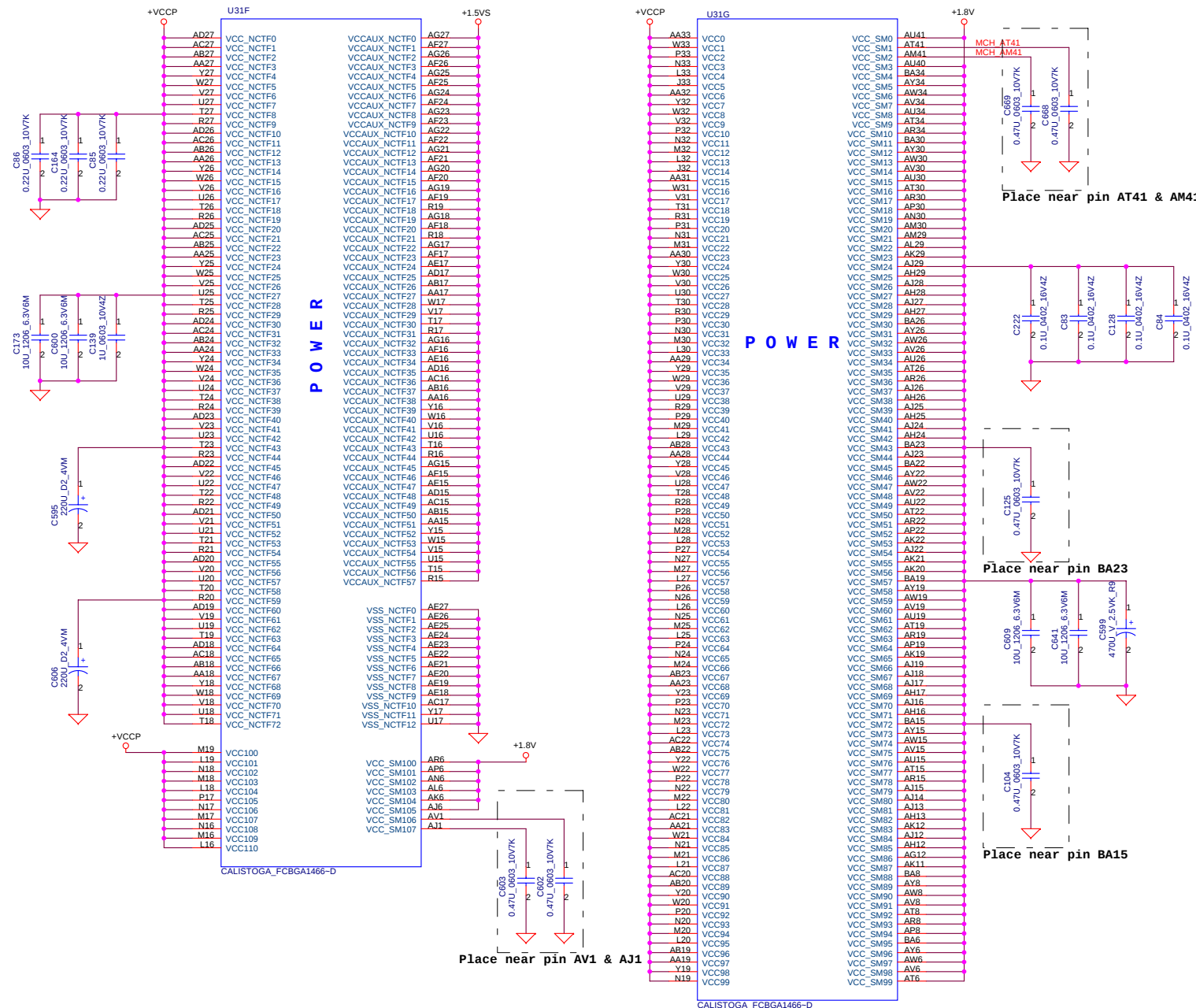
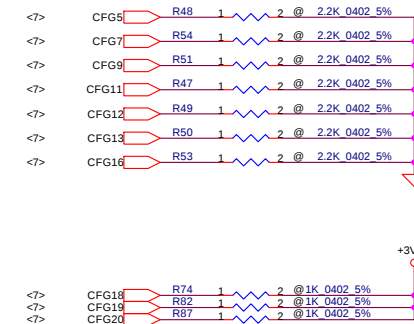
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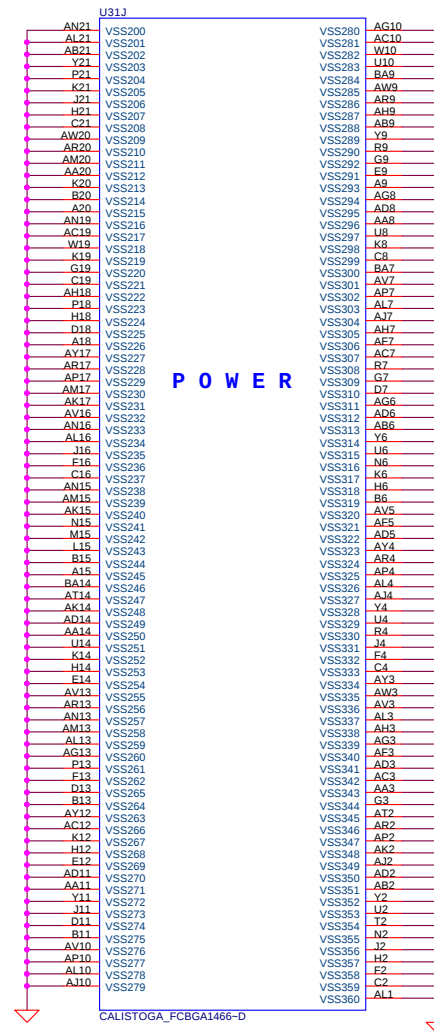
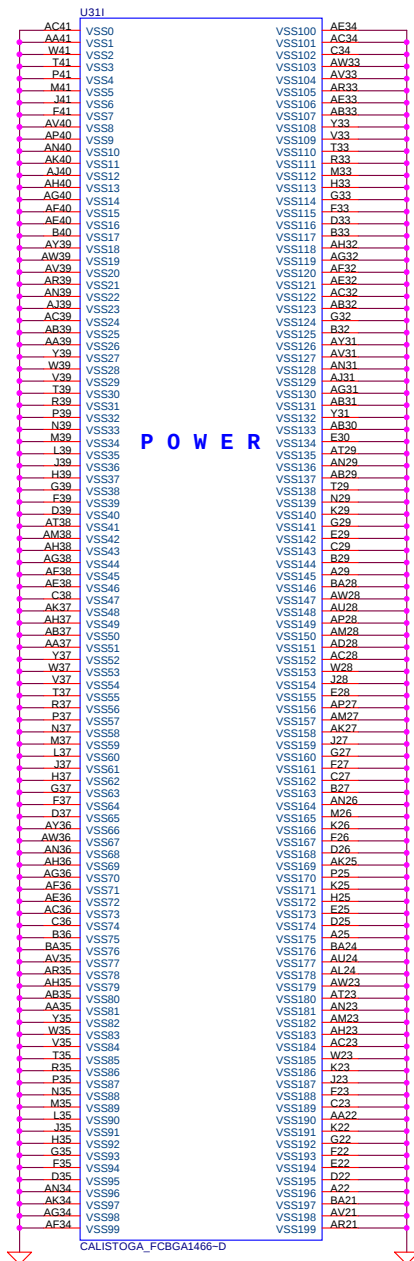
Strap Pin Table

CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

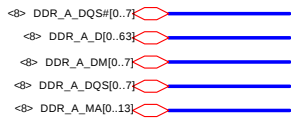
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V*(Default) 01 = 1.5V
CFG19	0 = No SDVO Device Present *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



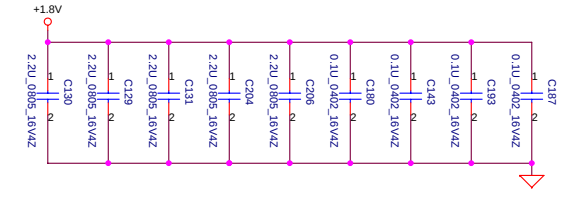
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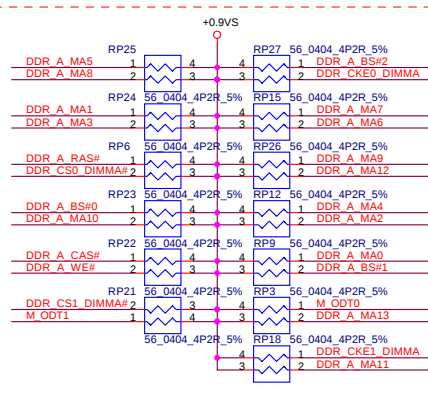
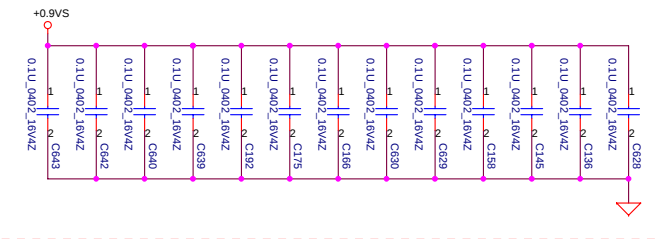
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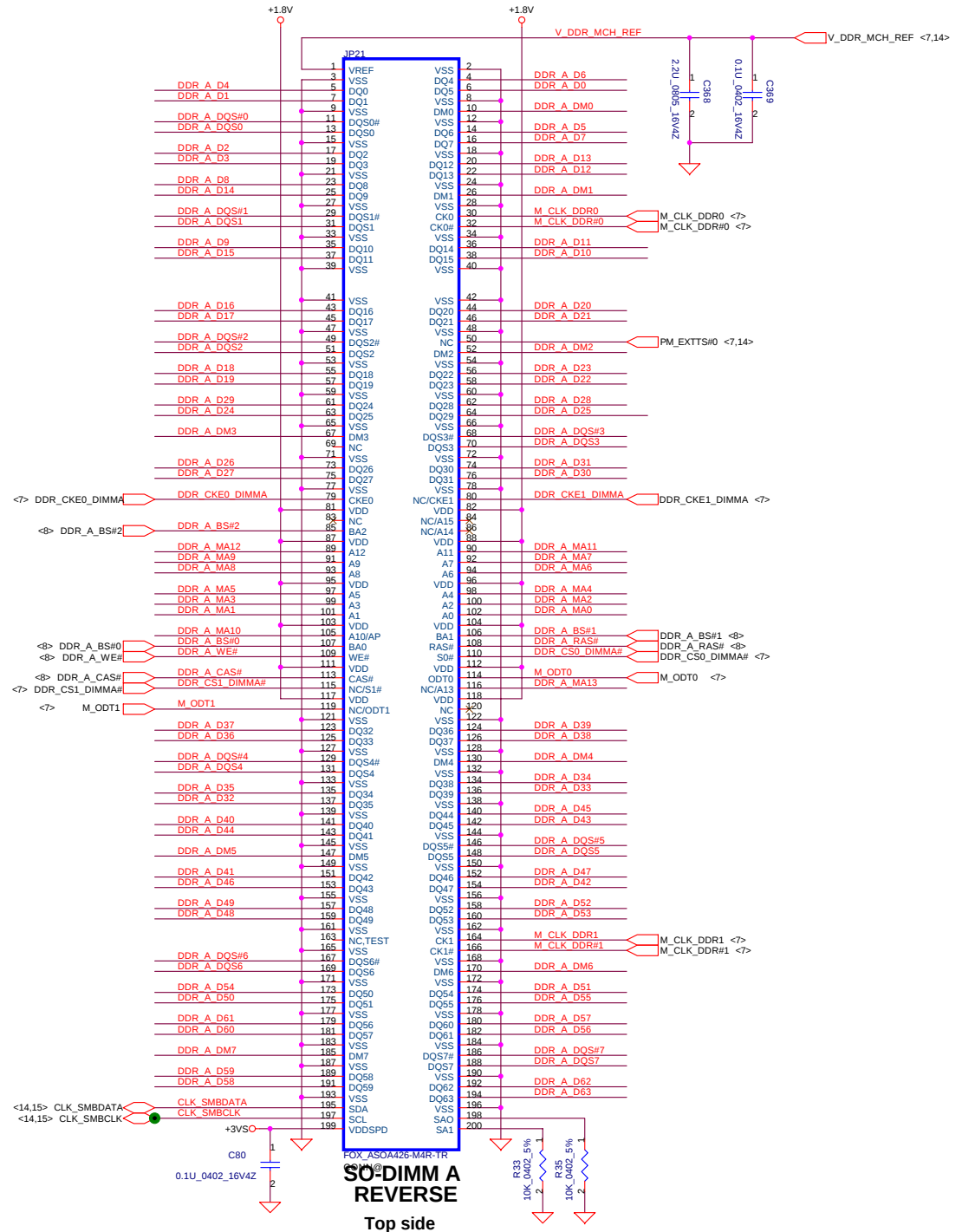
Layout Note:
Place near JP41



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



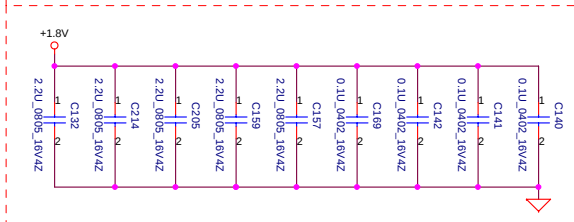
Layout Note:
Place these resistor
closely JP41,all
trace length Max=1.5"



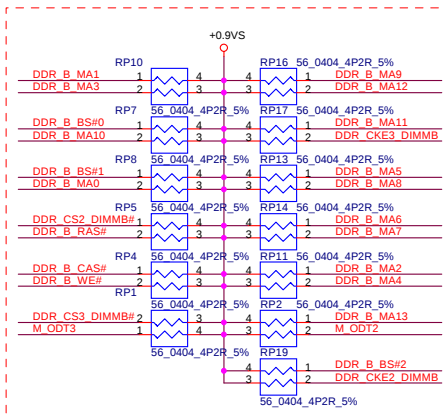
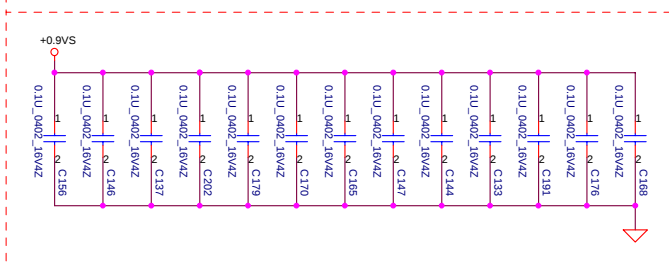
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				DDR II-SODIMM SLOT1			
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<> DDR_B_DQS#[0..7] <>
 <> DDR_B_D[0..63] <>
 <> DDR_B_DM[0..7] <>
 <> DDR_B_DQS[0..7] <>
 <> DDR_B_MA[0..13] <>

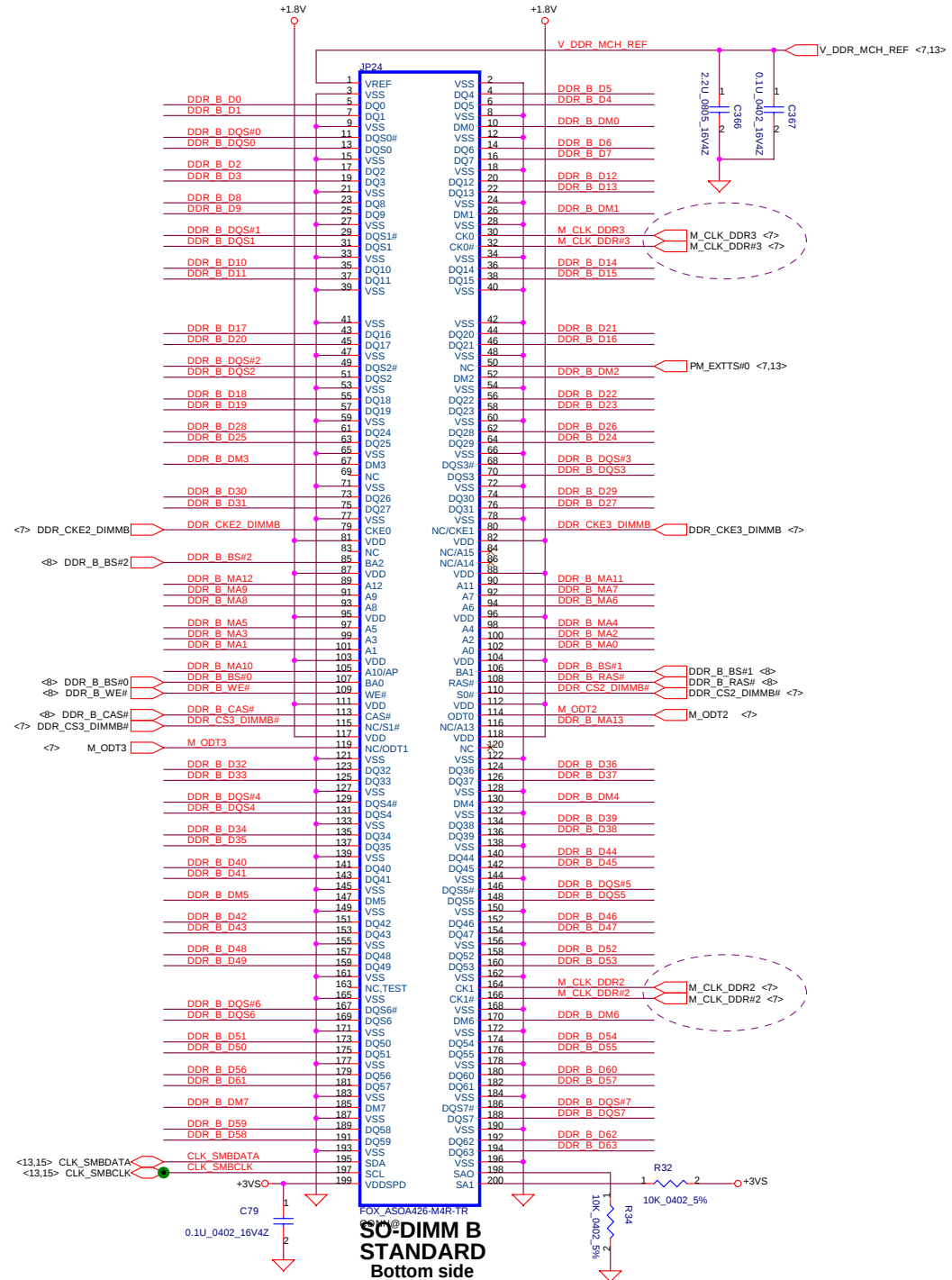
Layout Note:
Place near JP42



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor
closely JP42, all
trace length Max=1.5"



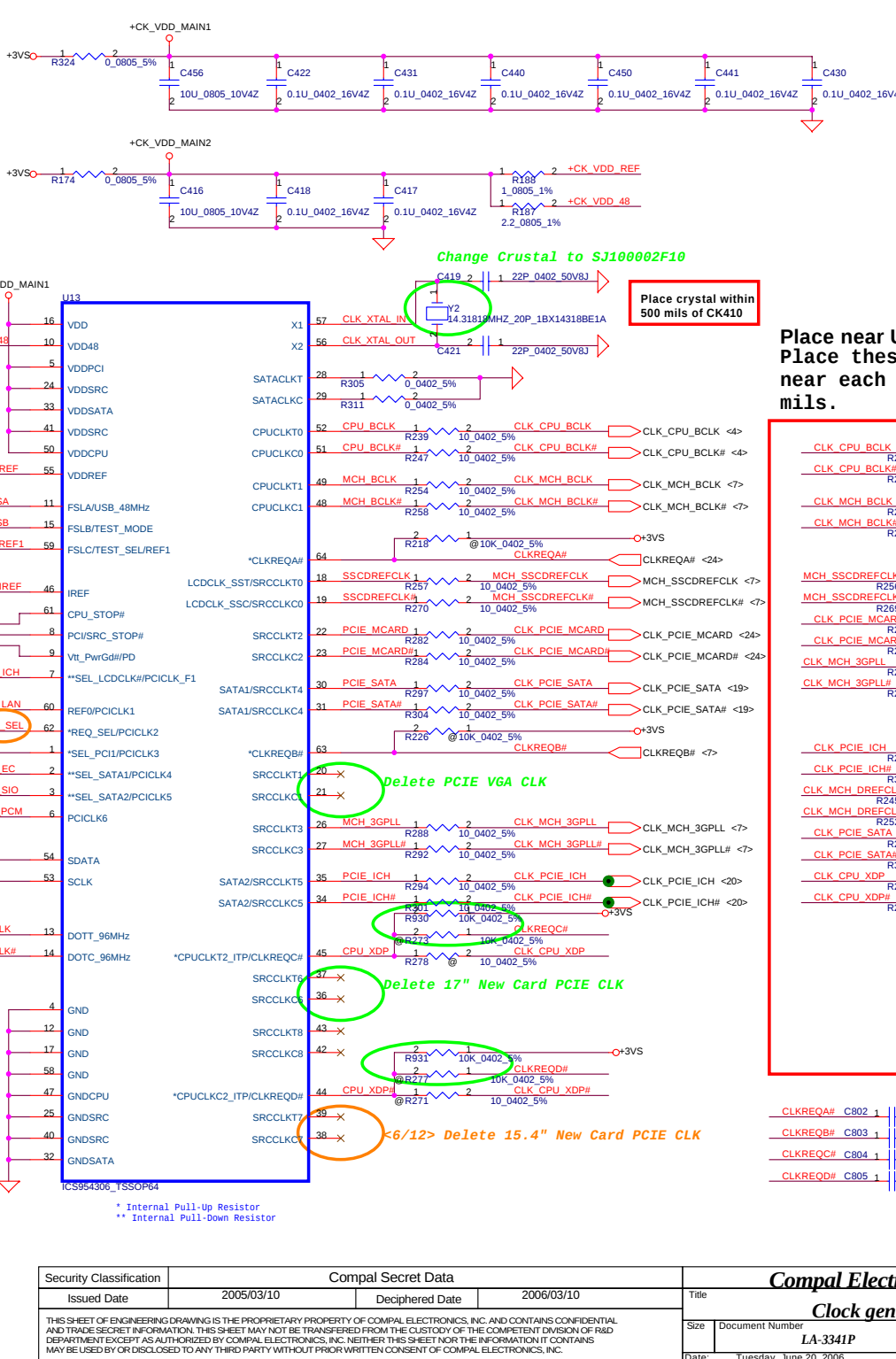
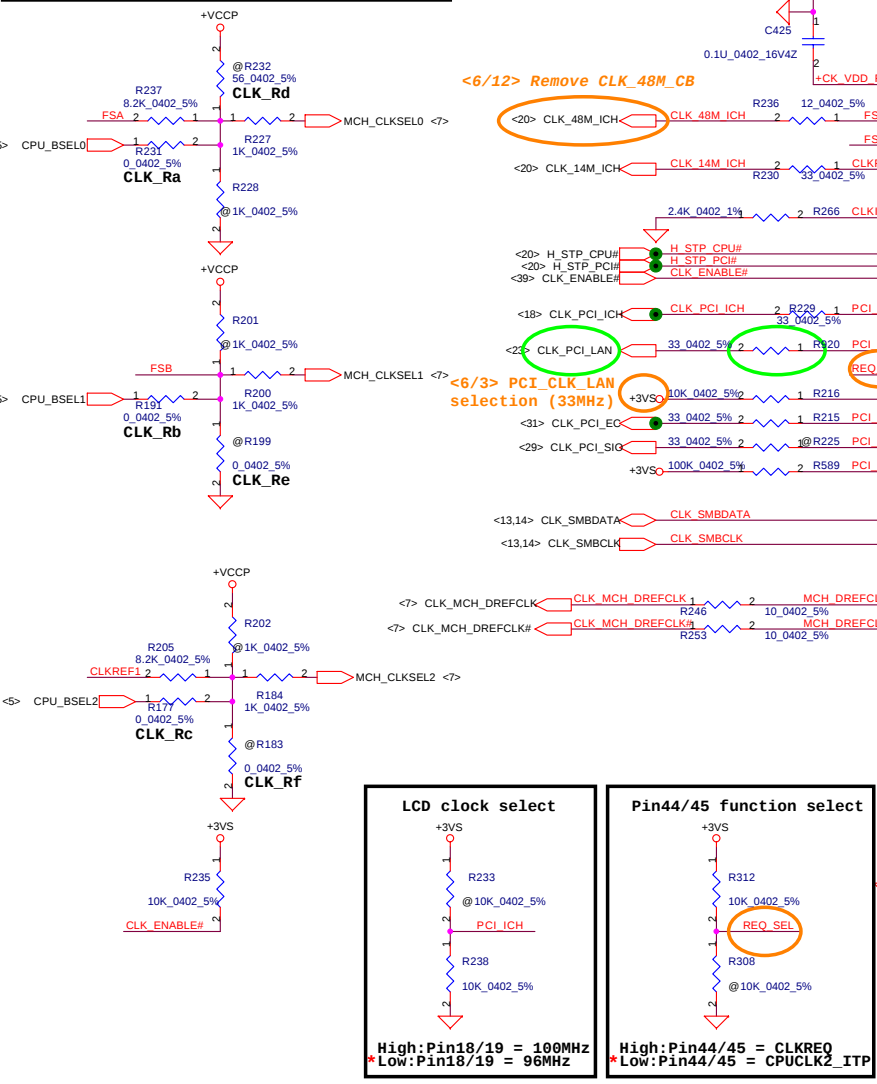
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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHZ	SRC MHZ	PCI MHZ
0	0	1	133	100	33.3
0	1	1	166	100	33.3

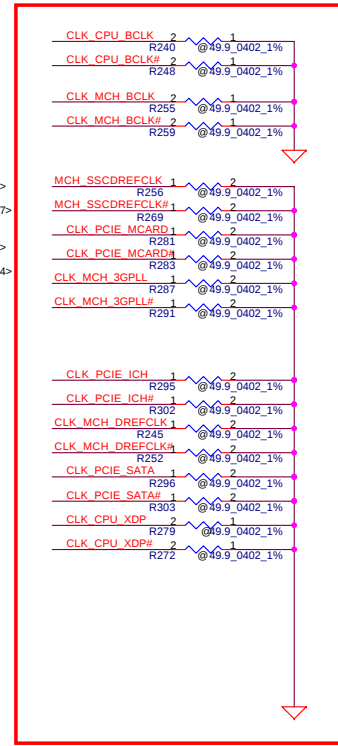
Table : ICS954306

FSB Frequency Selet:

CPU Driven *(Default)	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
	No Stuff	CLK_Rd	CLK_Re	CLK_Rf
533MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
667MHz	Stuff	CLK_Rd	CLK_Rf	
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc



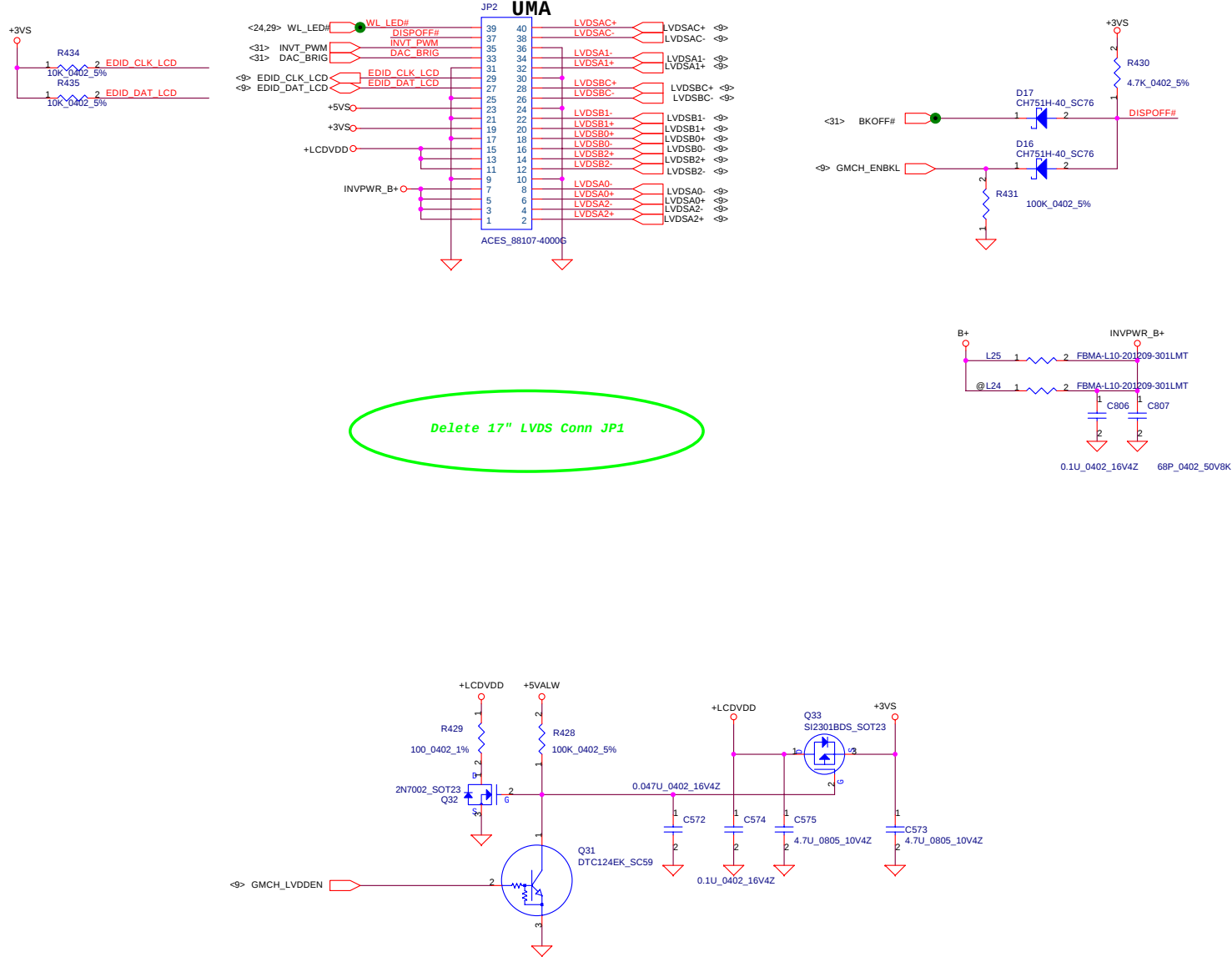
Place near U54
Place these components
near each pin within 40
mils.



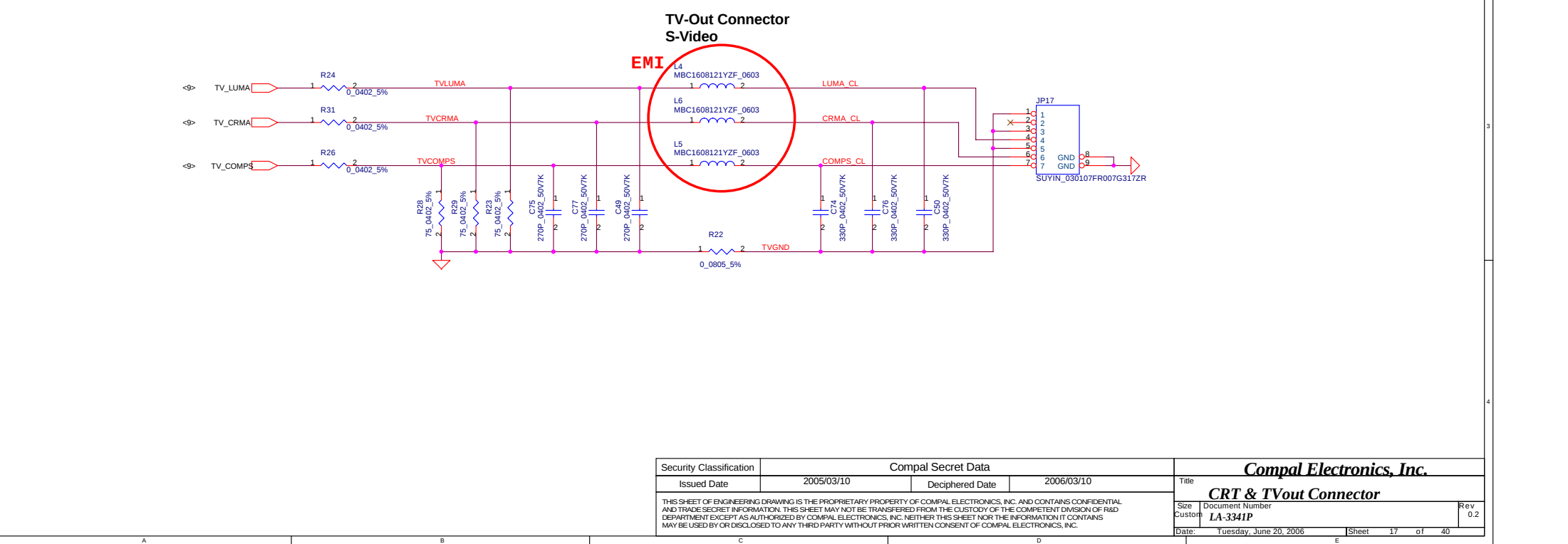
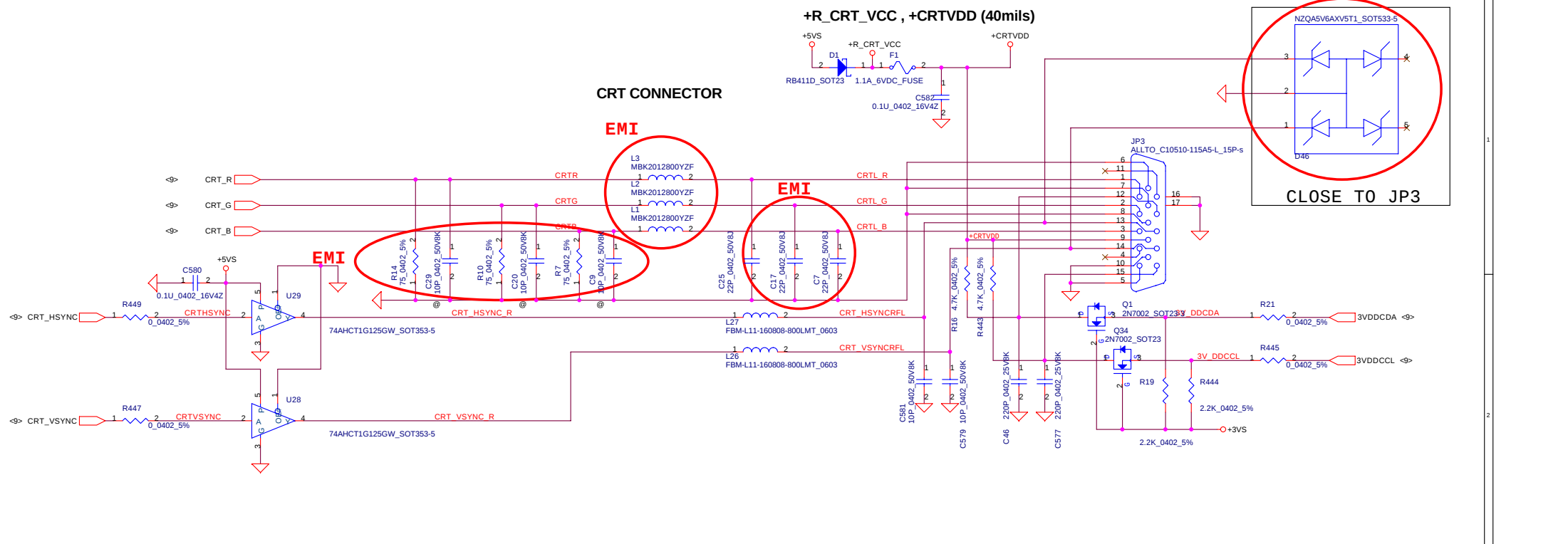
LCD clock select
High: Pin18/19 = 100MHz
Low: Pin18/19 = 96MHz

Pin44/45 function select
High: Pin44/45 = CLKREQ
Low: Pin44/45 = CPUCLK2_ITP

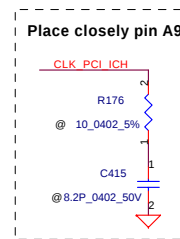
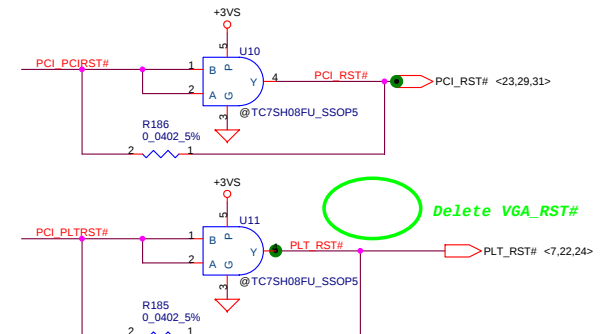
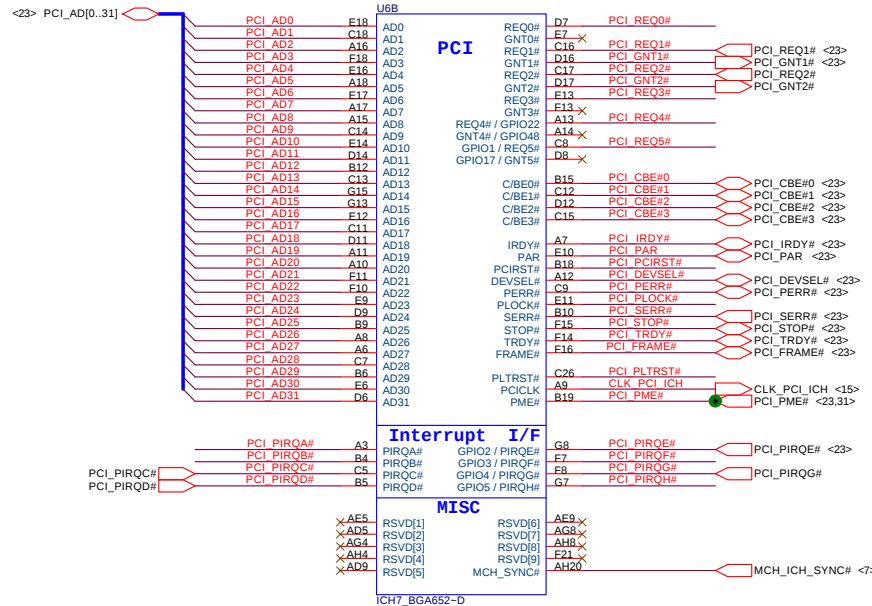
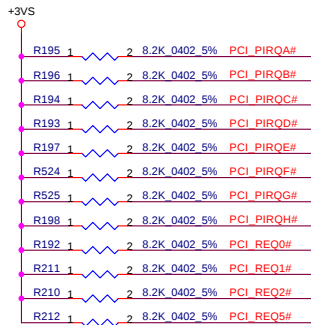
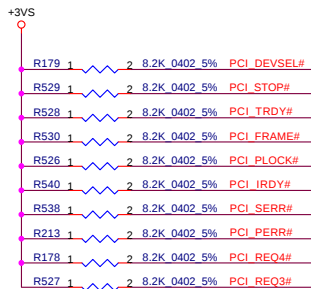
LCD Panel & inverter Connector



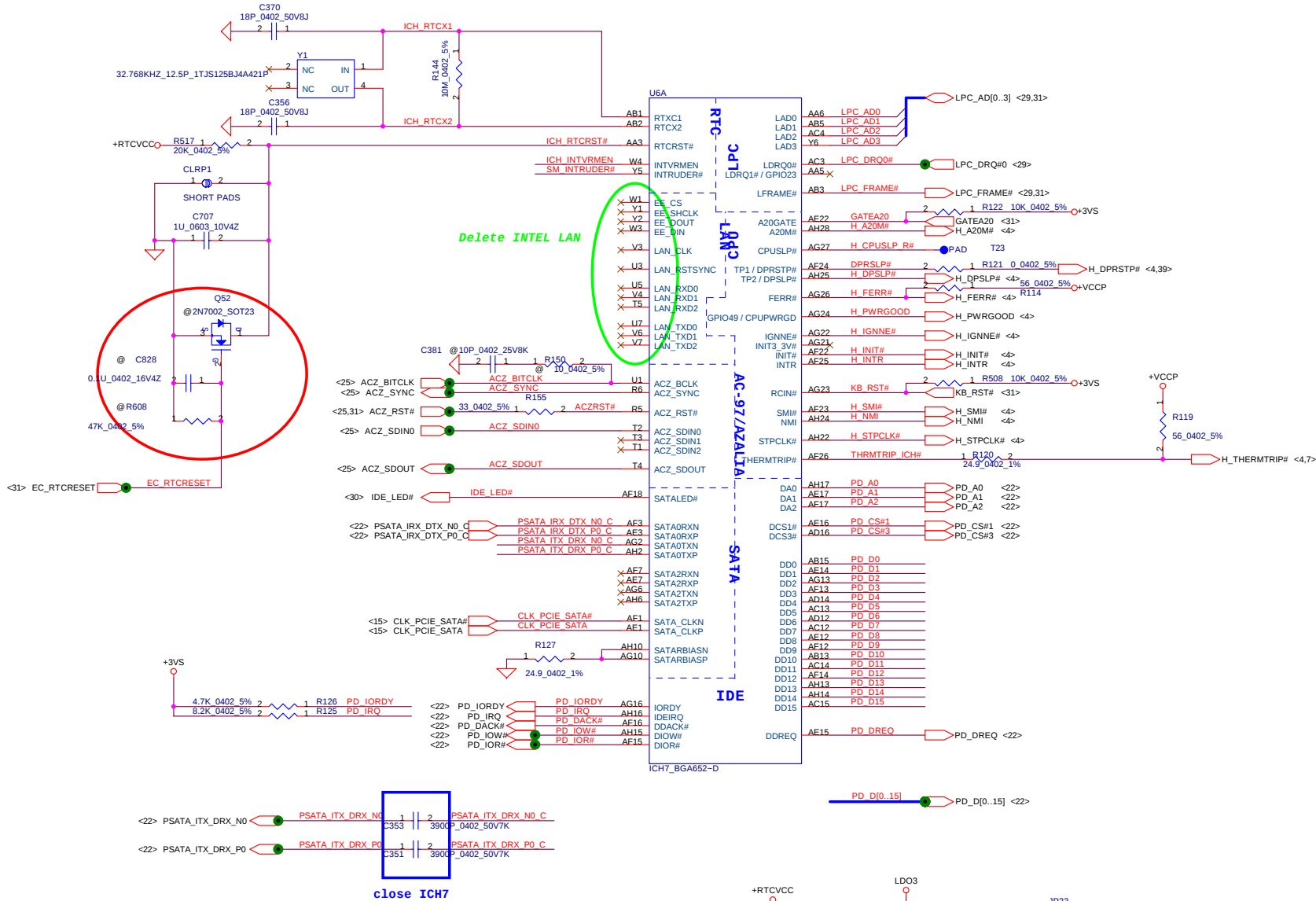
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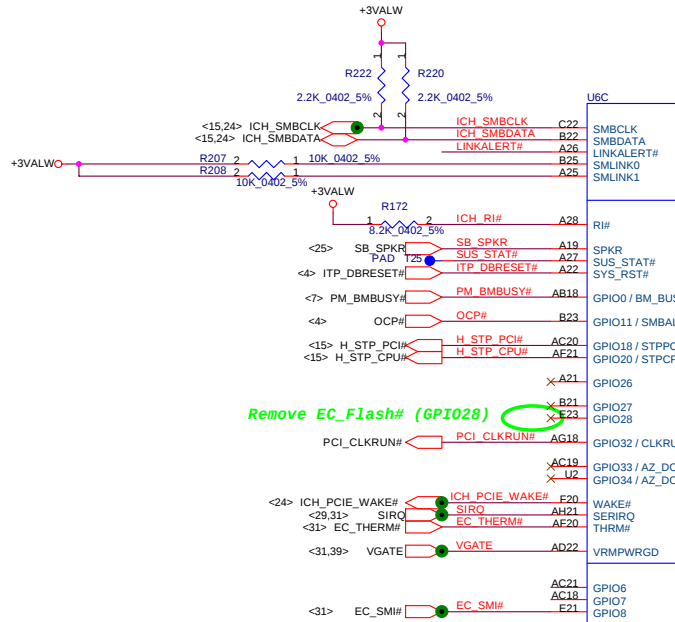
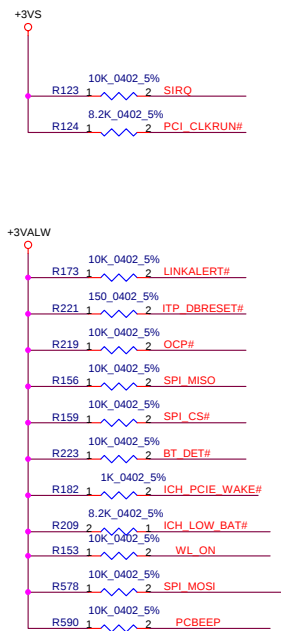
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					LA-3341P
				Date:	Tuesday, June 20, 2006
				Sheet	18 of 40
				Rev	0.2
				ICH7-M(1/4)	



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						Size		Document Number		Rev	
						Custom		LA-3341P		0.2	
						Date:		Tuesday, June 20, 2006		Sheet 19 of 40	



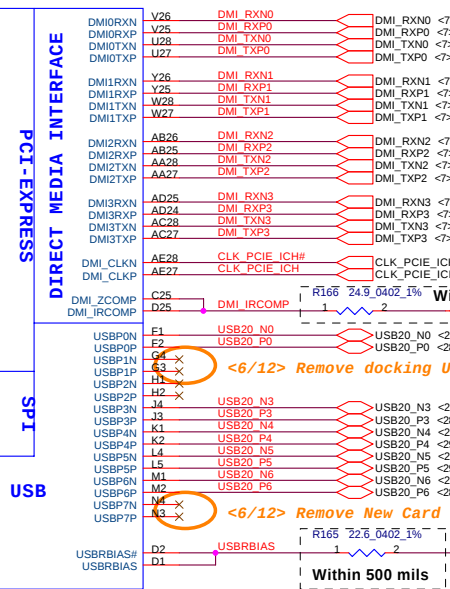
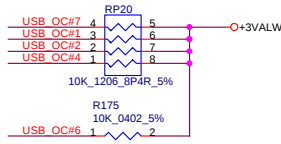
Remove EC Flash# (GPIO28)

Need update symbol

Delete 17" New Card PCIE traces

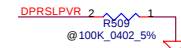
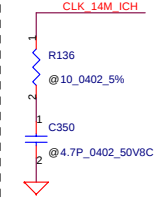
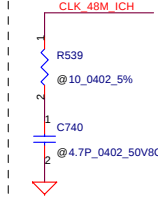
<6/20> Remove New Card trace

To mini PCIE Card



Place closely pin B2

Place closely pin AC1



Within 500 mils

Left side USB port

<6/12> Remove docking USB traces

Left side USB port

Audio Board USB port

Audio Board USB port

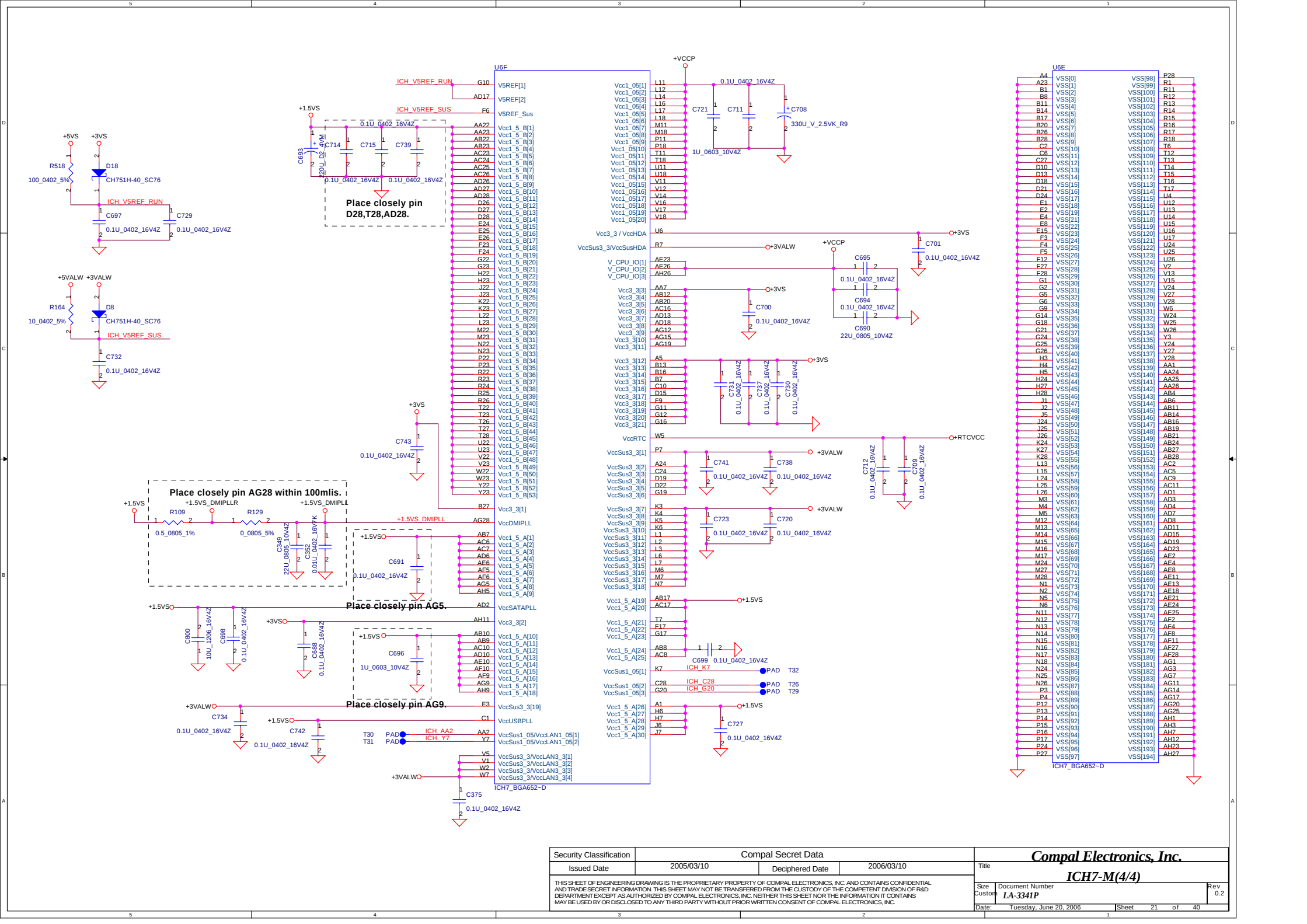
BT module

<6/12> Remove New Card

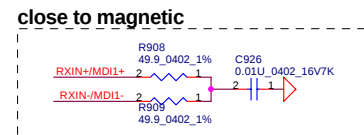
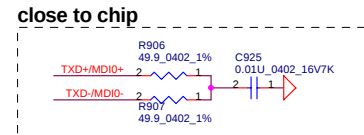
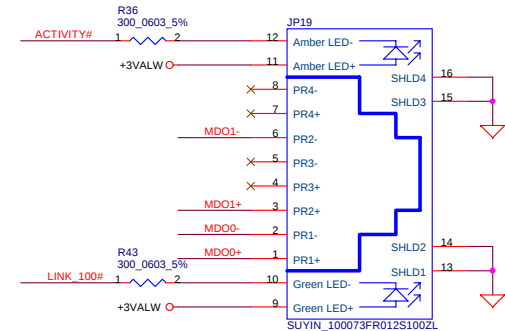
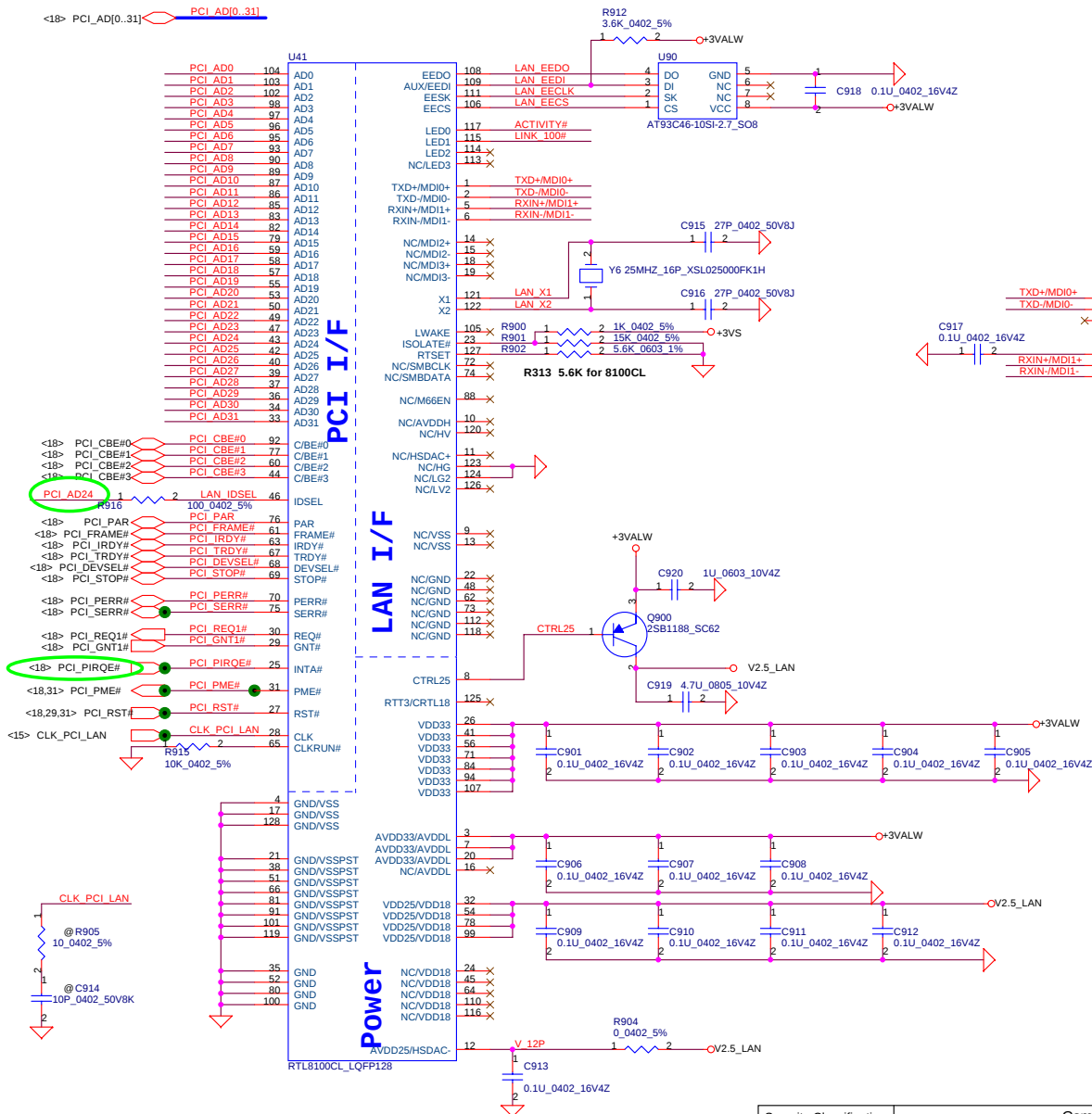
Within 500 mils

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				Custom	LA-3341P
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				Sheet	20 of 40
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ICH7-M(3/4)

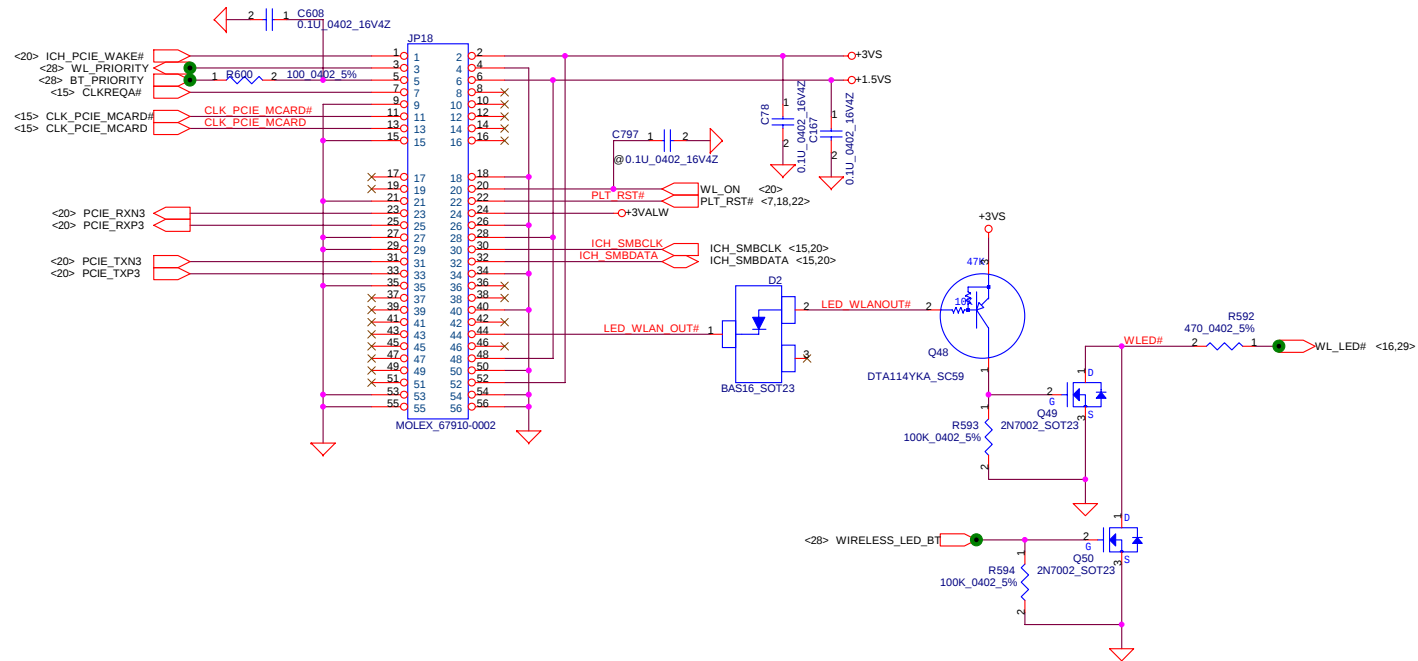


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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title	HDD & CDROM	
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				Date:	Tuesday, June 20, 2006	Sheet 22 of 40



Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2005/04/06	LAN-8100CL	
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Mini-Express Card(Slot 1-WLAN)



Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Mini Card	
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				Custom	LA-3341P
				Date:	Tuesday, June 20, 2006
				Sheet	24 of 40
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<6/12> Remove PCM_SPK

For Layout:

Place decoupling caps near the power pins of SmartAMC device.

Delete CD traces

<6/12> Remove Docking line out

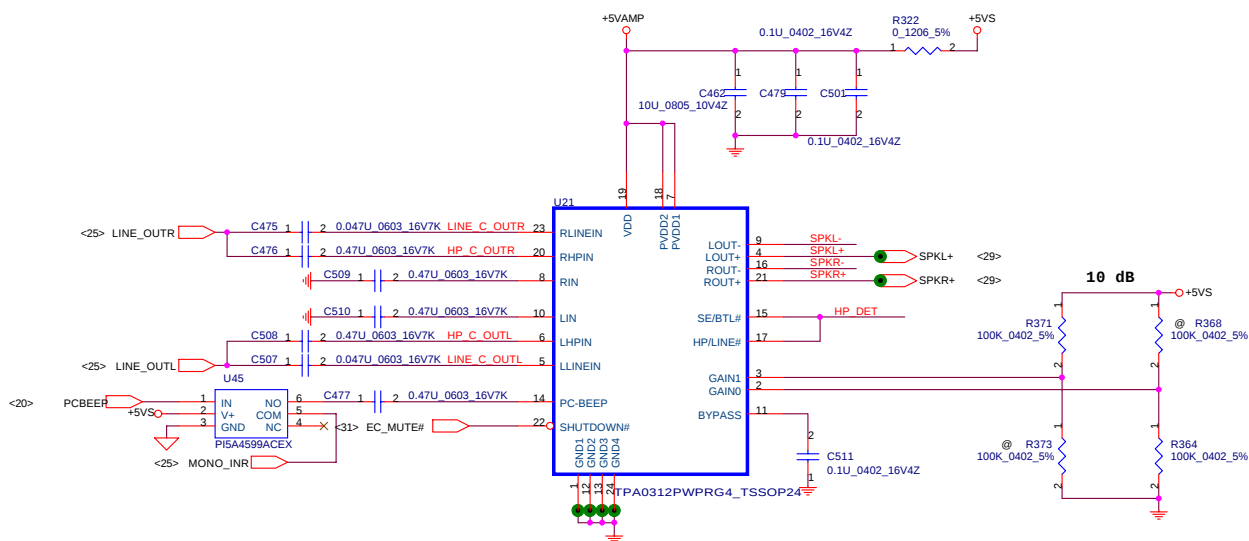
<6/12> Remove Docking MIC

<6/12> Remove JACK_DET from Docking

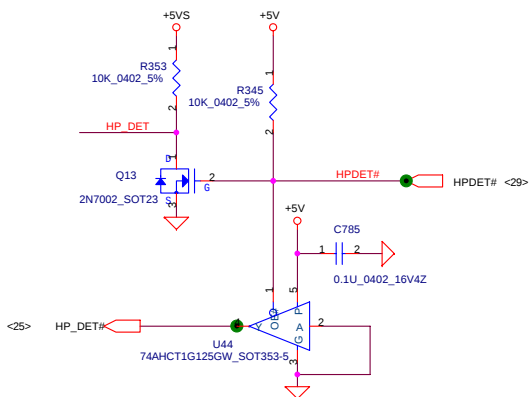
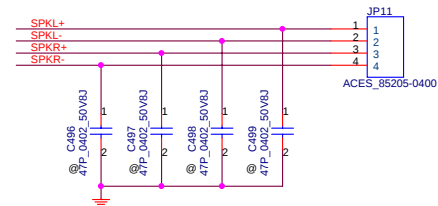
HP_DET#	JACK_DET#	PORT-A	PORT-B	EQ
0	0	ON	OFF	Disable
0	NC	ON	OFF	Disable
NC	0	OFF	ON	Disable
NC	NC	ON	OFF	Enable

MIC_DET	PORT-C	PORT-F
0	ON	OFF
NC	OFF	ON

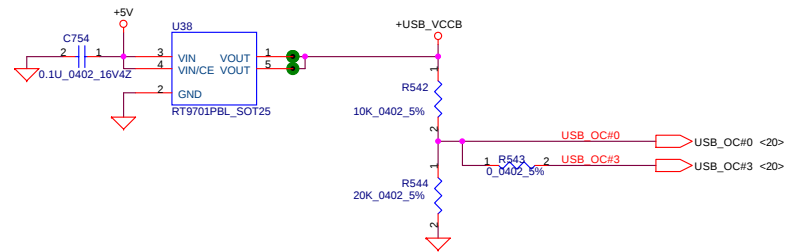
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title	AMOM_codec
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Date: Tuesday, June 20, 2006				Sheet	25 of 40
				Rev	0.2



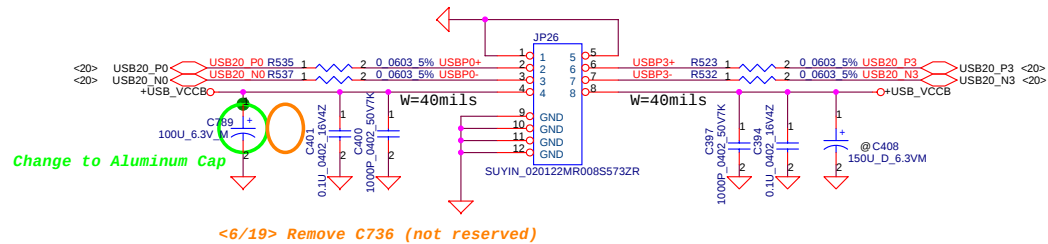
Gain Settings			
GAIN0	GAIN1	SE/BTL#	Av(inv)
0	0	0	6 dB
0	1	0	* 10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB



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Issued Date	2005/03/10	Deciphered Date	2006/03/10	AMP & Audio Jack	
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				Date	Rev
				Tuesday, June 20, 2006	0.2
				Sheet	27 of 40

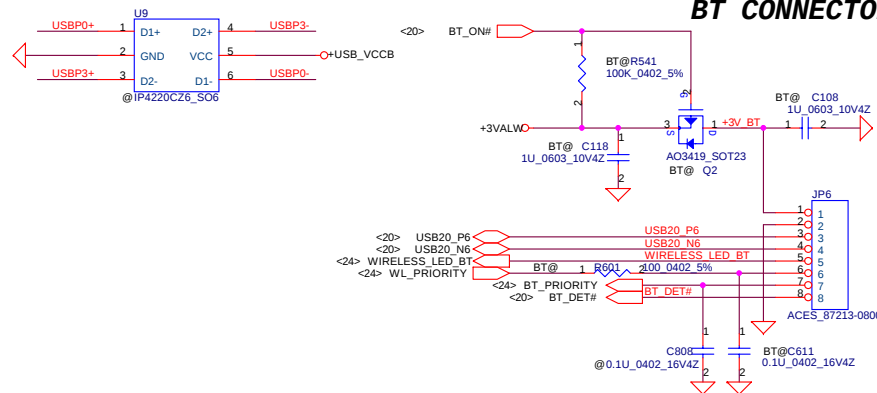


USB CONNECTOR (Left side)

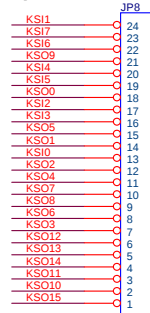
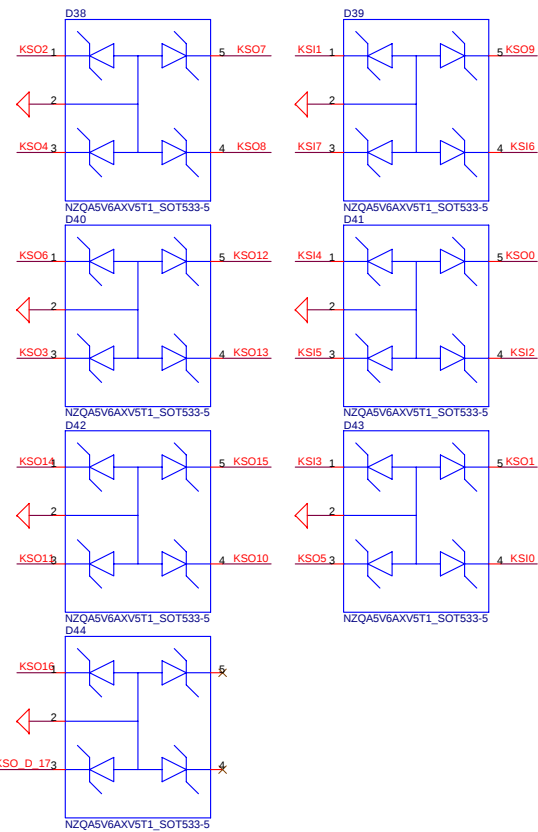
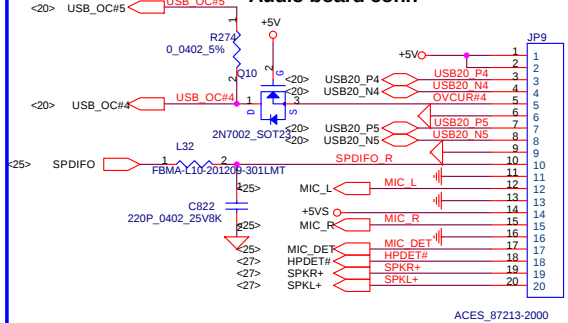
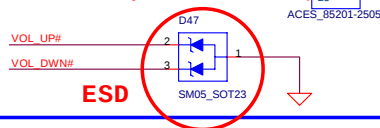
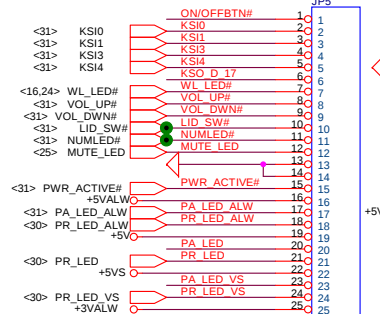
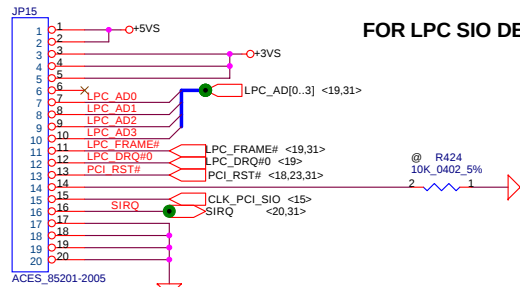
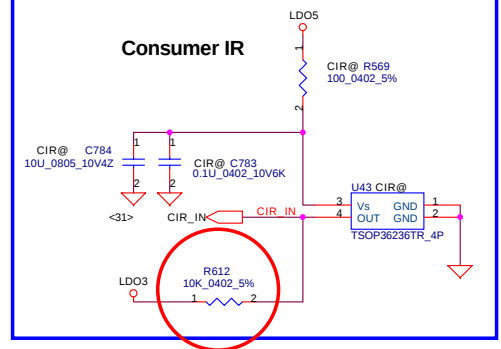
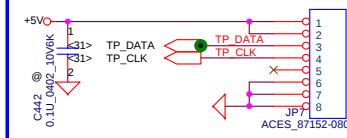


BT CONNECTOR

Reserve Bluetooth



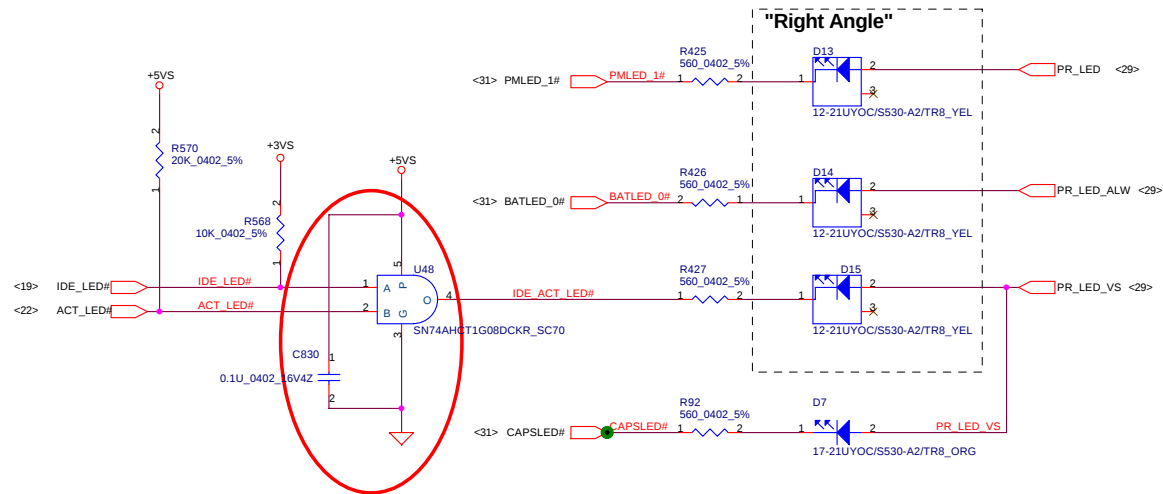
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title	Bluetooth & USB CONN.
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				Custom	0.2
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[illegible]

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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title		
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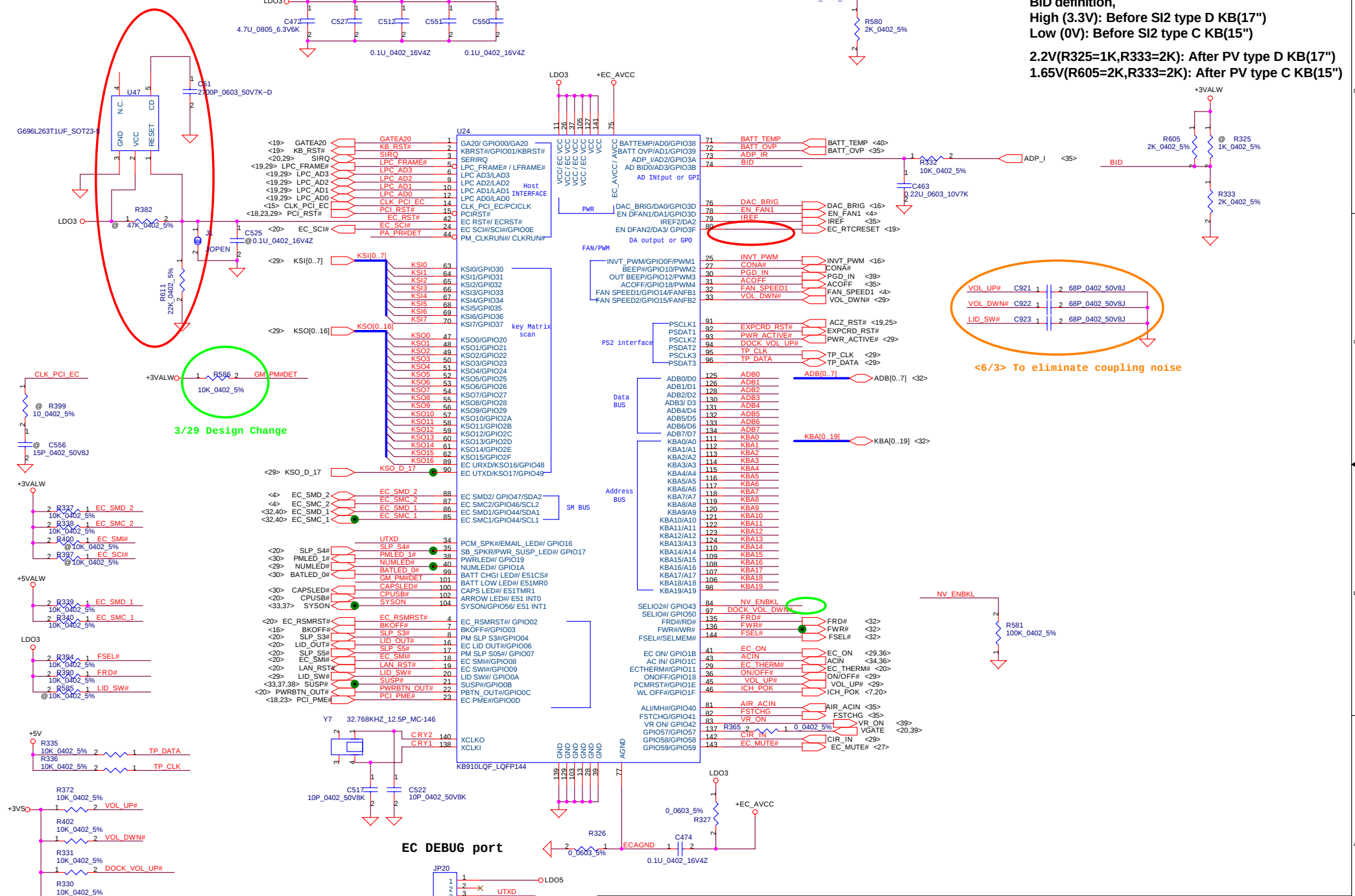
For PR

FOR POWER BUTTON BACKLIGHT SYSTEM POWER



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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title		
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Cd(uF)=T(ms) / 1685
Cd=2700PF -----> T=3.6ms

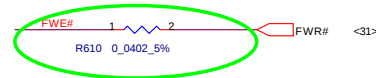
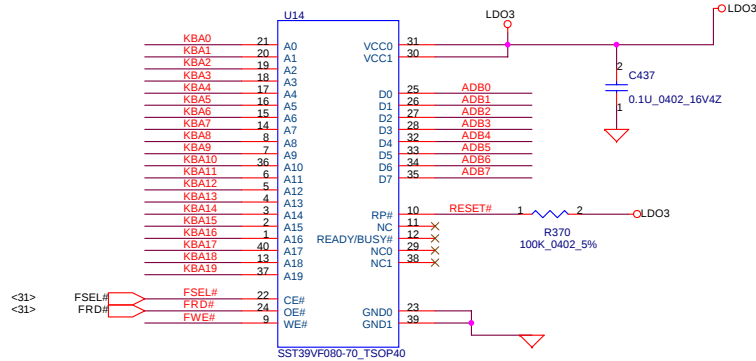
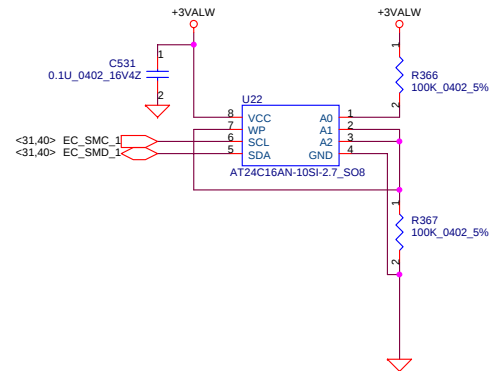
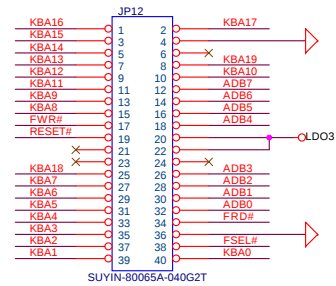


BID definition,
High (3.3V): Before SI2 type D KB(17")
Low (0V): Before SI2 type C KB(15")

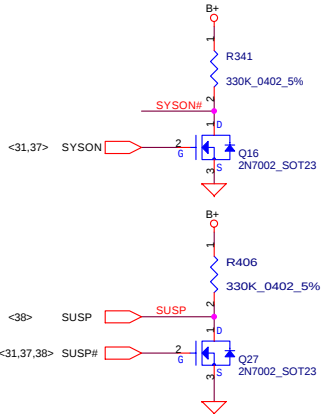
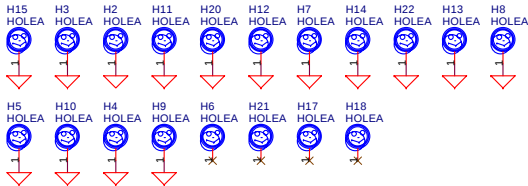
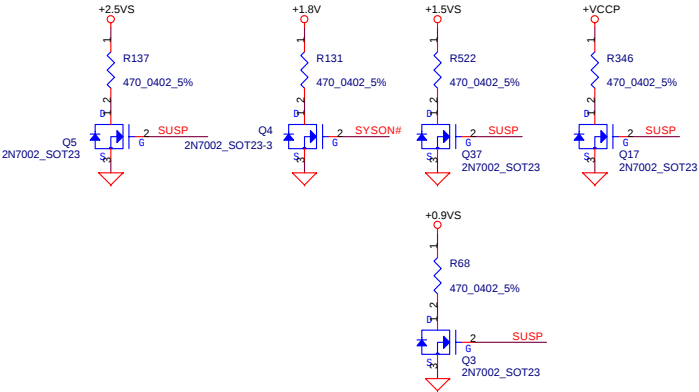
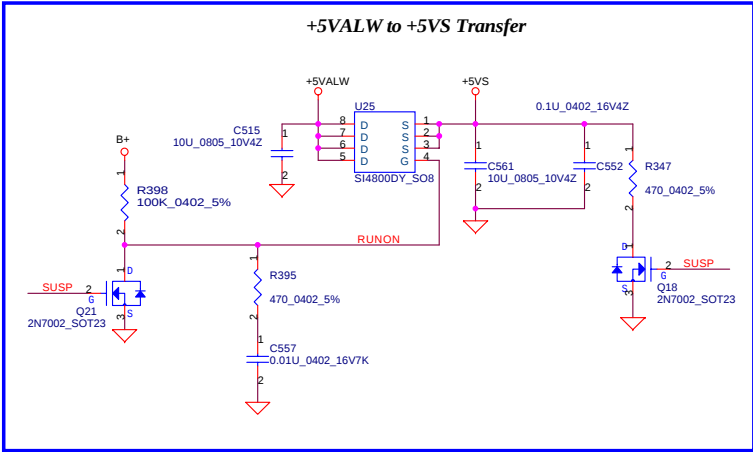
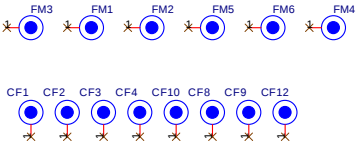
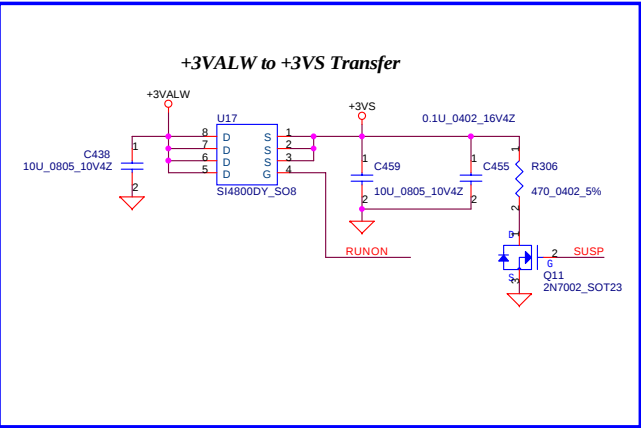
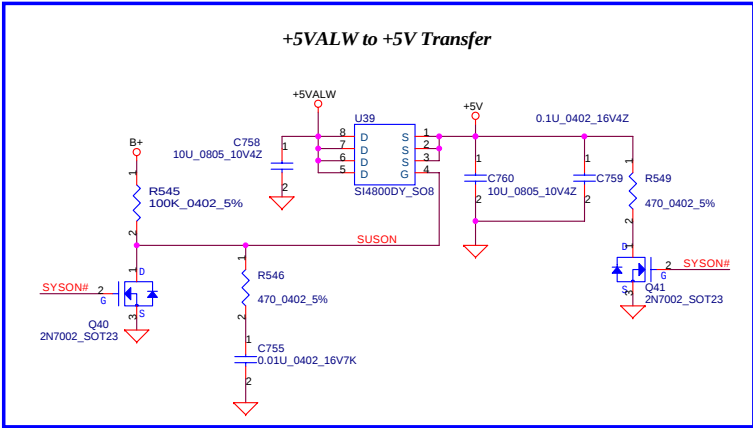
2.2V(R325=1K,R333=2K): After PV type D KB(17")
1.65V(R605=2K,R333=2K): After PV type C KB(15")

Security Classification		Compal Secret Data		Title	
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				Date	Rev
				Tuesday, June 20, 2006	0.2
				Sheet	31 of 40

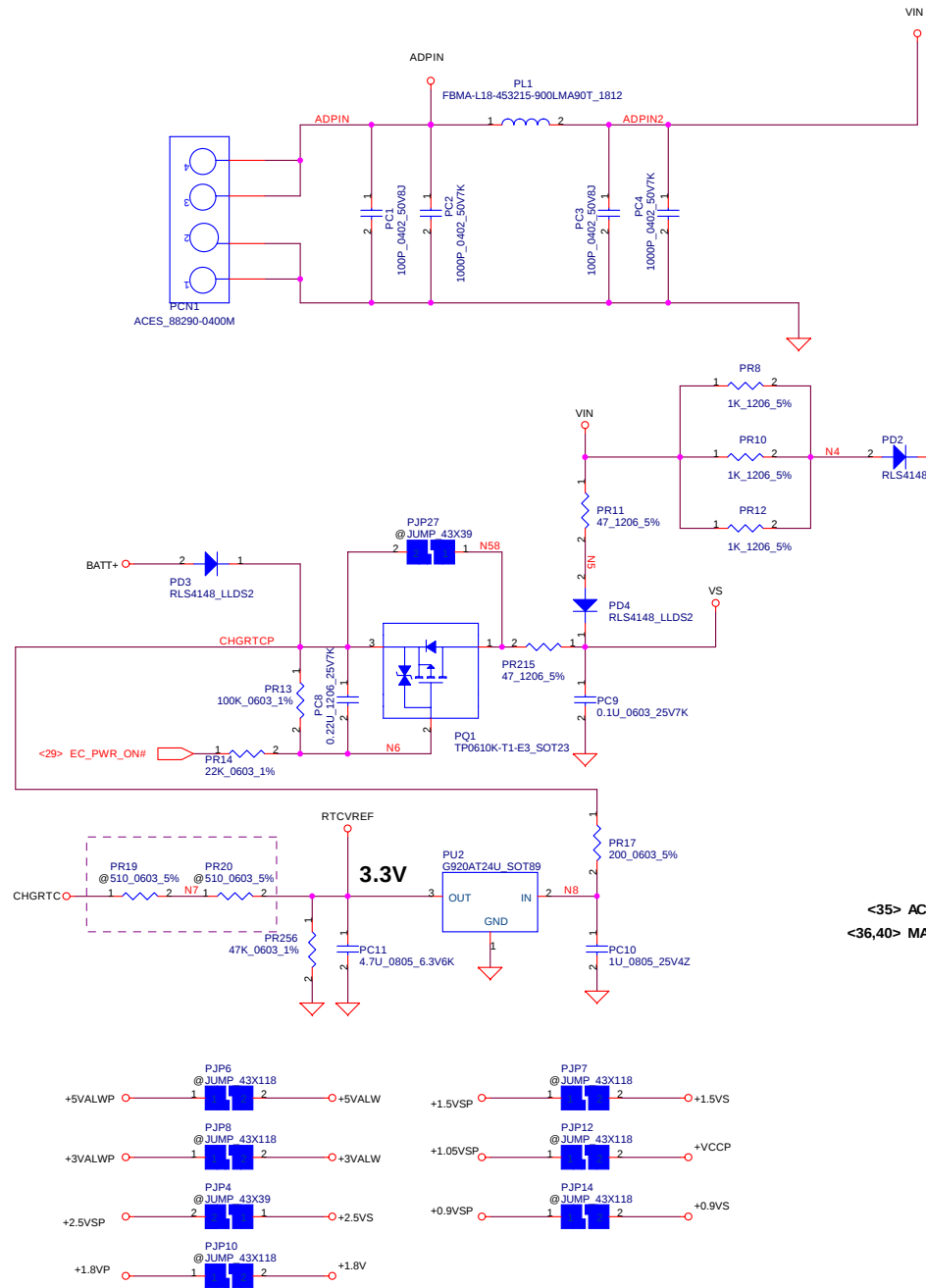
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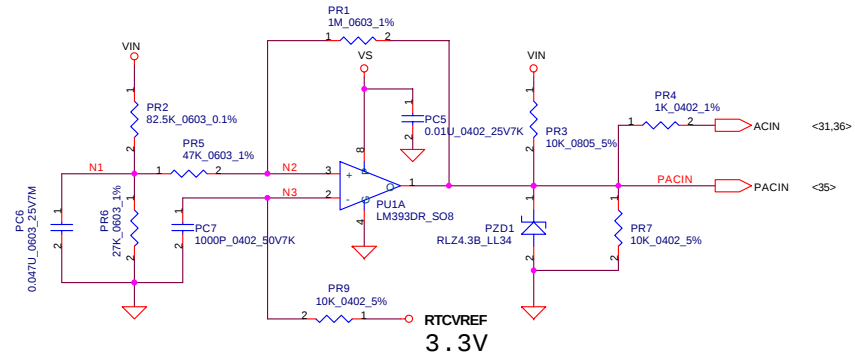
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2005/03/10				Deciphered Date			
2005/03/10				2006/03/10				Title			
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								Document Number			
								LA-3341P			
								Rev			
								0.2			
								Date:			
								Tuesday, June 20, 2006			
								Sheet			
								32 of 40			



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title	DC/DC Circuit
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				Custom	LA-3341P
				Date:	Tuesday, June 20, 2006
				Sheet	33 of 40
				Rev	0.2

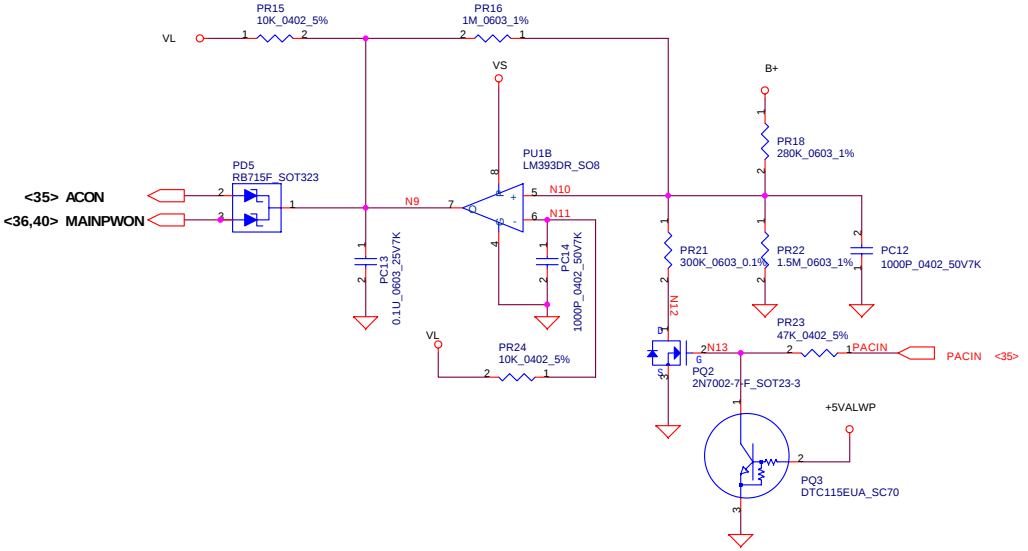


Vin Detector :			
14.698	14.285	13.879	
13.818	13.411	13.000	

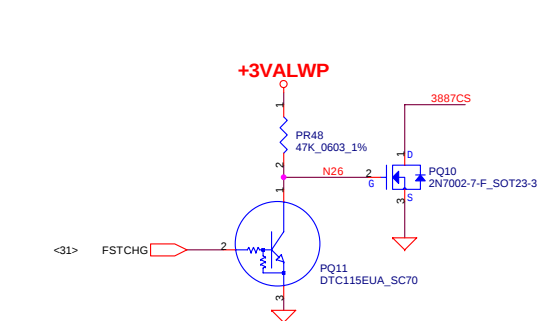
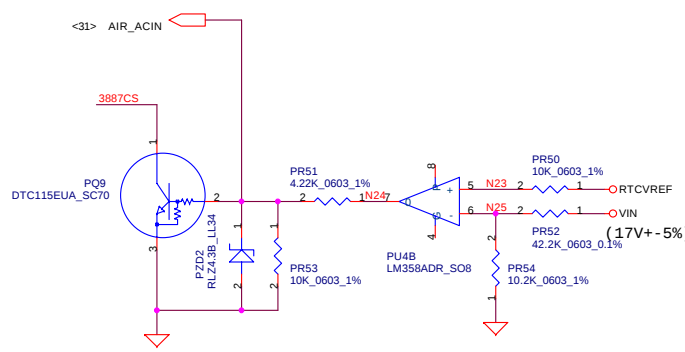
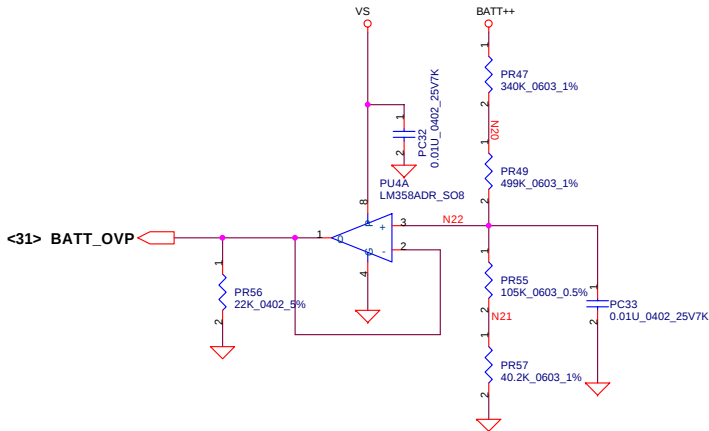
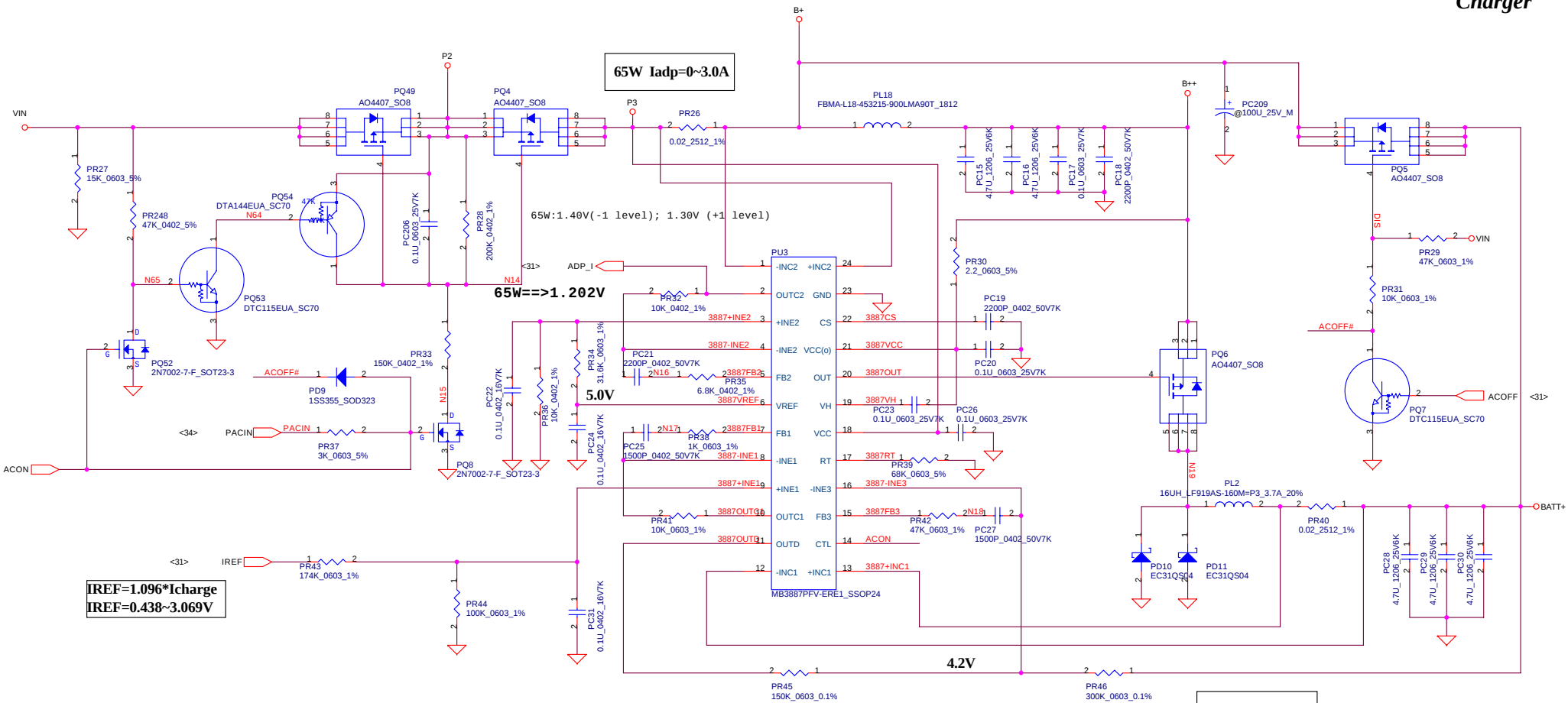


ACIN:			
Precharge detector			
12.384	12.000	11.624	
10.927	10.600	10.223	

BATT			
Precharge detector			
7.558	7.333	7.112	
6.108	5.933	5.704	

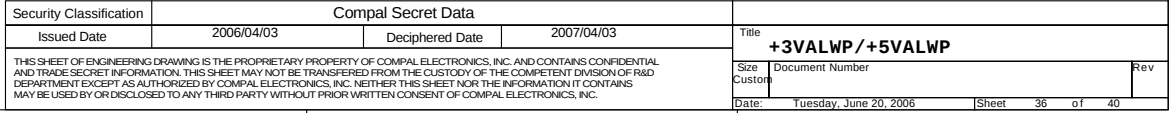


Charger



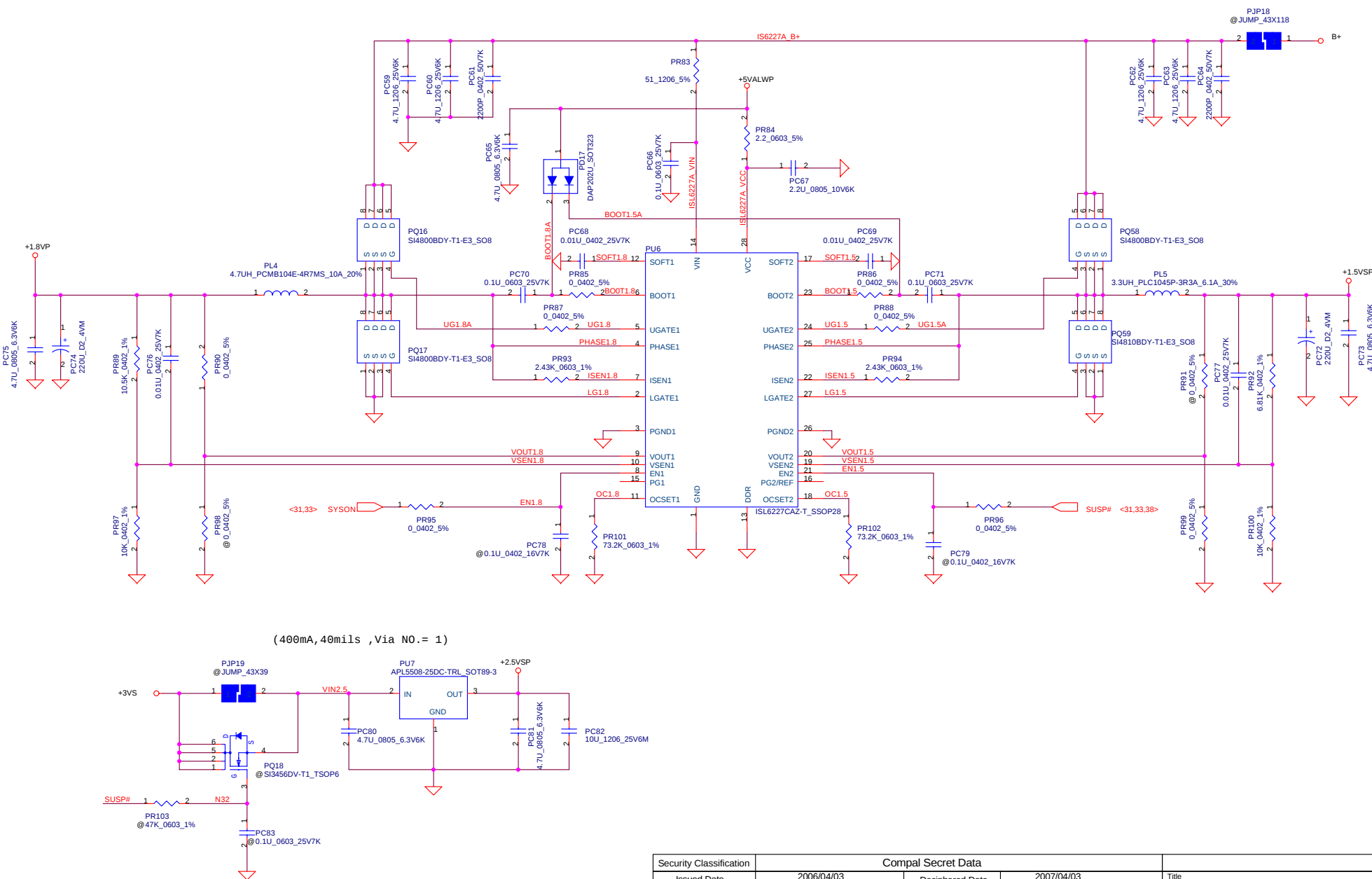
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Title	+3VALWP/+5VALWP
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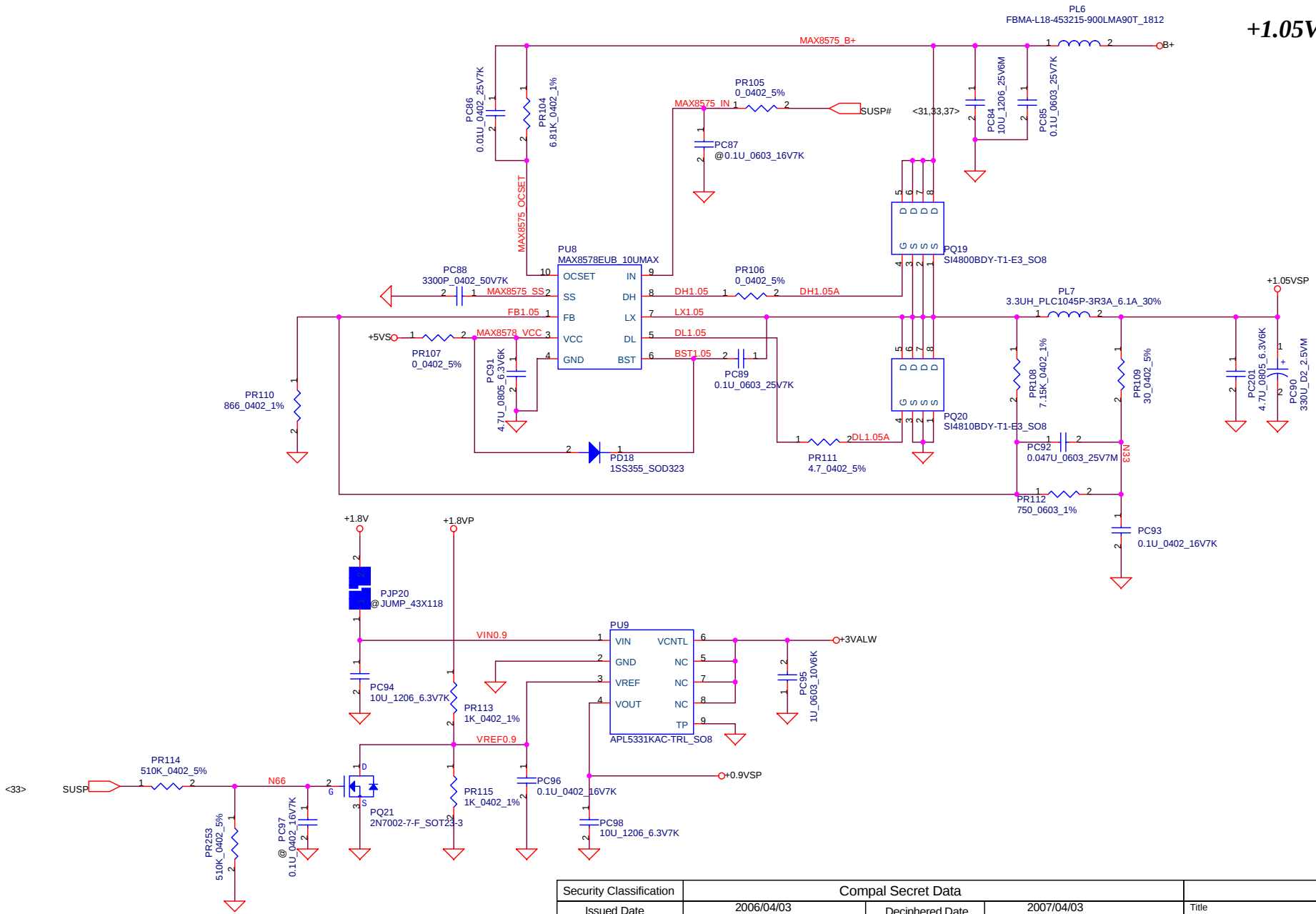
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+2.5VSP/+1.8VP/+1.5VSP

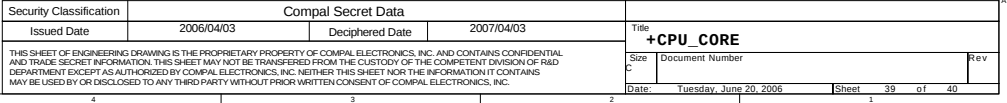


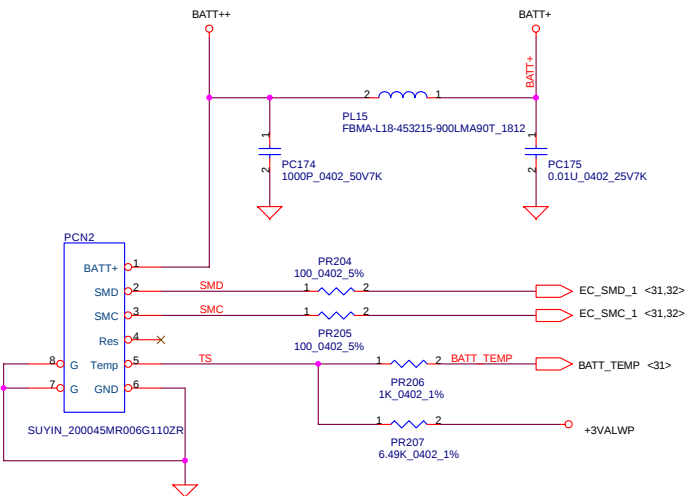
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+1.05V_VCCPP/+0.9VSP



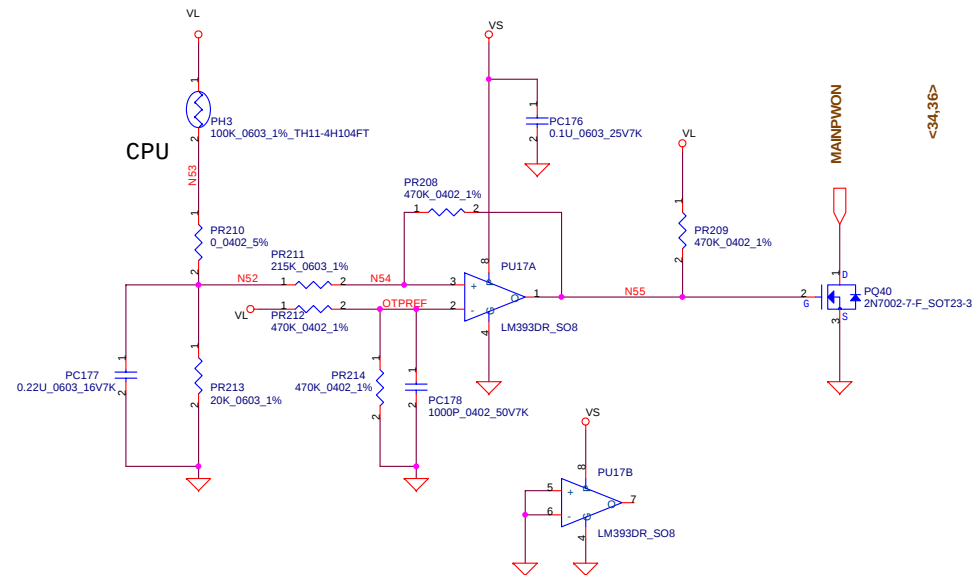
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PJPB1 battery connector
SMART
Battery:
1.BATT+
2.SMBD
3.SMBC
4.Res
5.Temp
6.GND

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C



Security Classification		Compal Secret Data		Title Battery Connect/OTP										
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