

Compal confidential

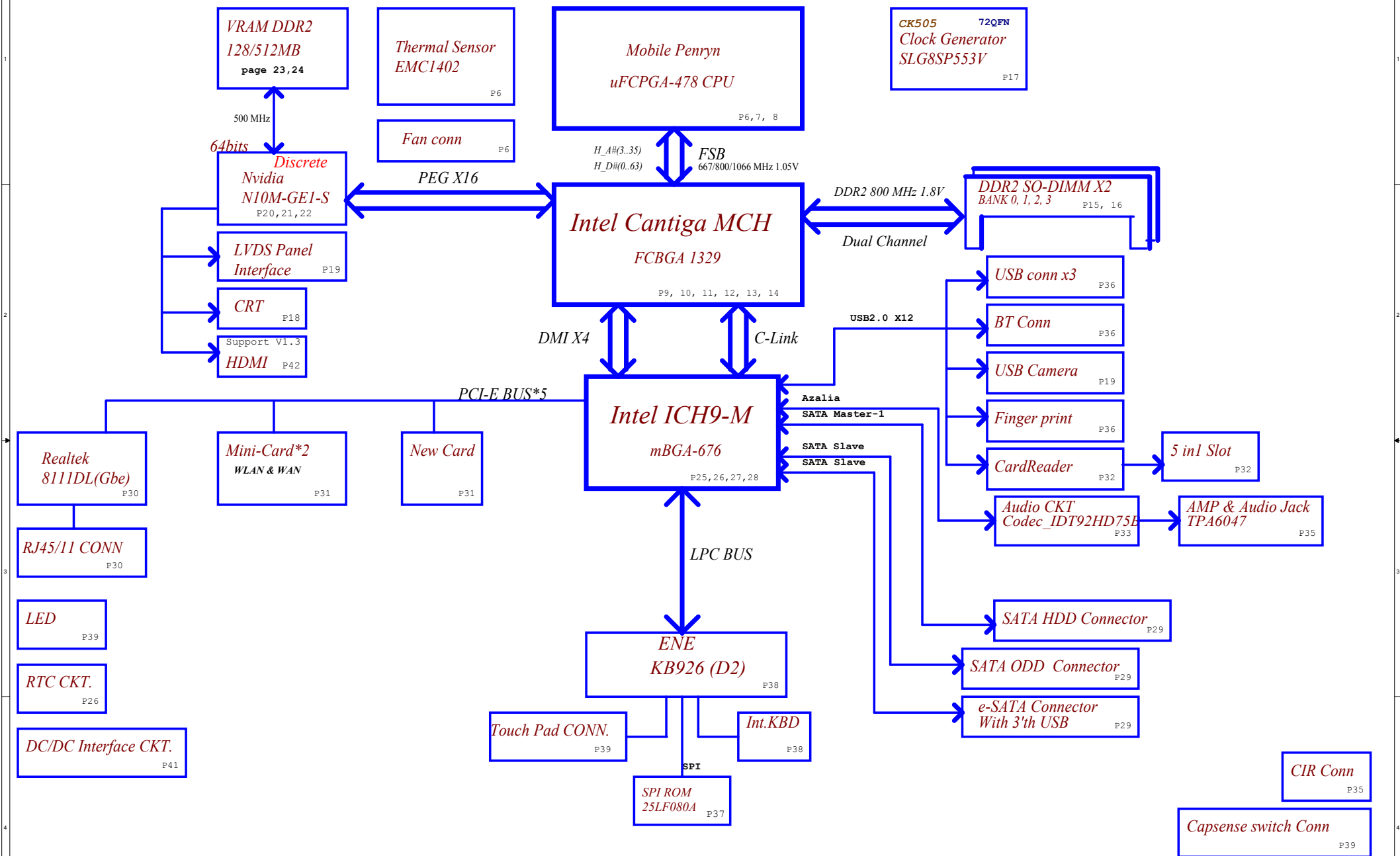
Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_PM+ICH9-M core logic

2009-02-13

REV : 1.0

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Voltage Rails

O MEANS ON

X MEANS OFF

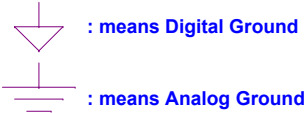
power plane	+B	+5VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS +NVVDD +PCIE
State		+3VALW		
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM

NB	SA00002JJ80	R1	FRU
NB	SA00002JJE0	R3	
SB	SA00002JH50	R1	FRU
SB	SA00002JHB0	R3	

@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
NewC@ :	means just reserve for New card
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot
PA @ :	means just reserve for PA
PR @ :	means just reserve for PR

Symbol Note :



USB assignment:

- USB-0 Right side(with ESATA)
- USB-1 Left side
- USB-2 Left side
- USB-3 Dock
- USB-4 Camera
- USB-5 WLAN
- USB-6 Bluetooth
- USB-7 Finger Printer
- USB-8 MiniCard(WWAN/TV)
- USB-9 Express card
- USB-10 X
- USB-11 X

PCIe assignment:

- PCIe-1 TV tuner/WWAN/Robeson
- PCIe-2 X
- PCIe-3 WLAN
- PCIe-4 GLAN (Marvell)
- PCIe-6 New Card

SMBUS Control Table

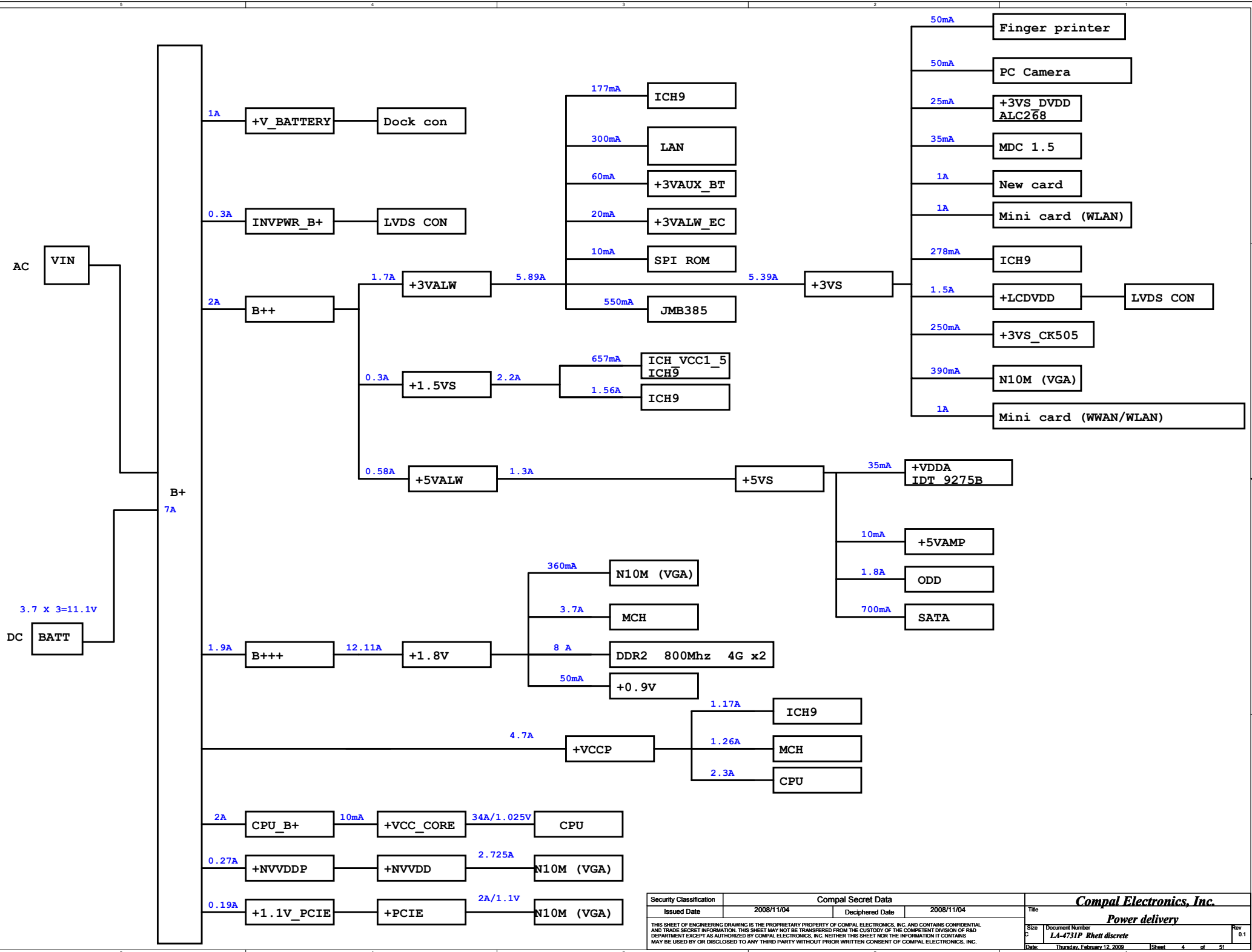
	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	Sensor board	N10M Thermal Sensor	N10M	G-sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	V	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	V	V	X
ICH_SMBCLK ICH_SMBDATA	ICH9	X	X	X	X	V	V	V	X	X	X	V

NB9M SMBUS Control Table

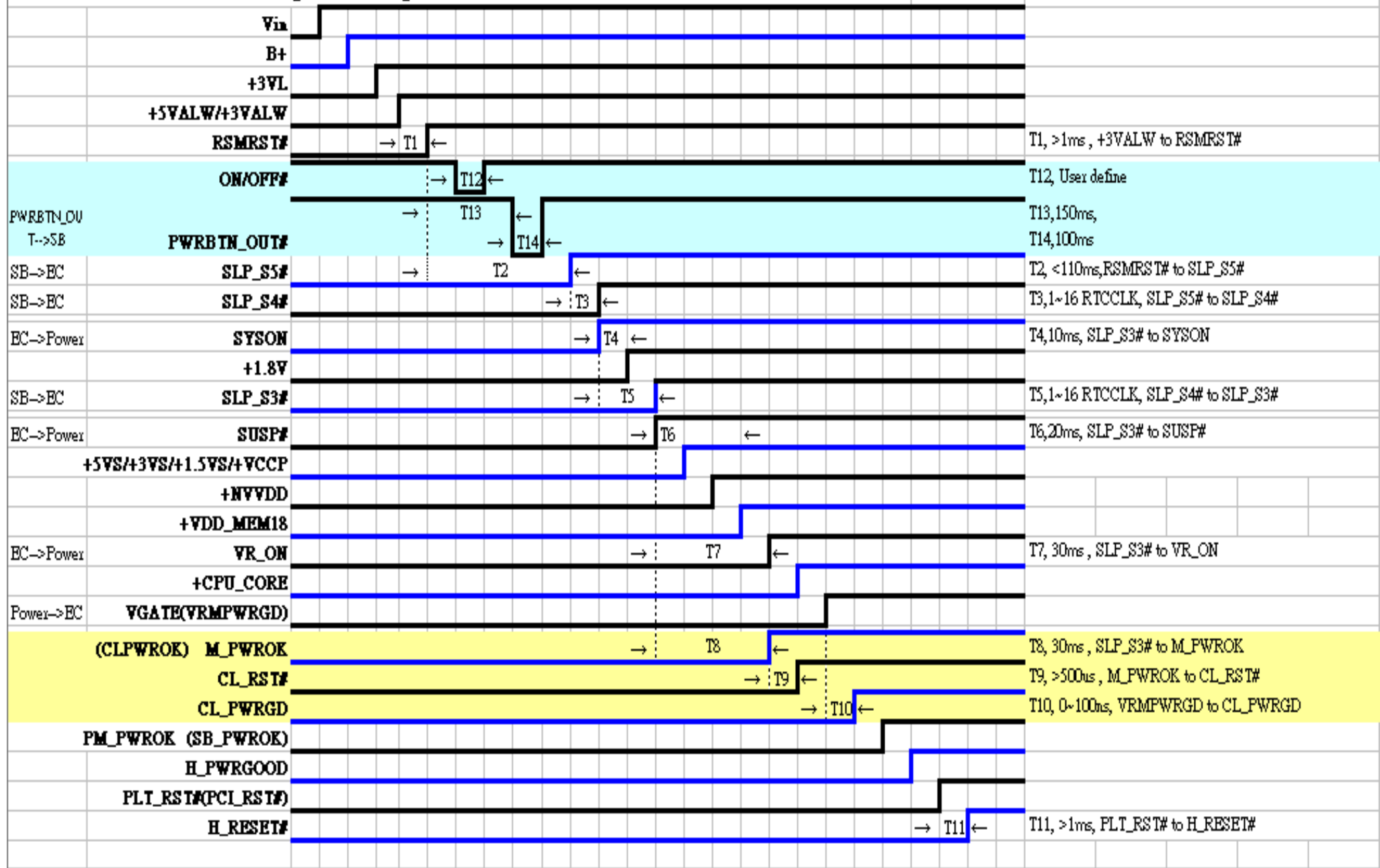
	SOURCE	LVDS	CRT	HDMI	HDCP
DDC2_DATA DDC2_CLK	N10M	V	X	X	X
3VDDCDA 3VDDCCL	N10M	X	V	X	X
HDMIDAT_VGA HDMICLK_VGA	N10M	X	X	V	X
HDCP_SDA HDCP_SCL	N10M	X	X	X	V

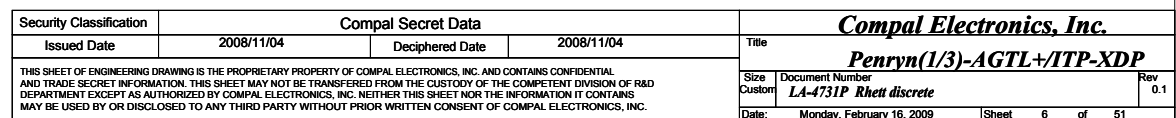
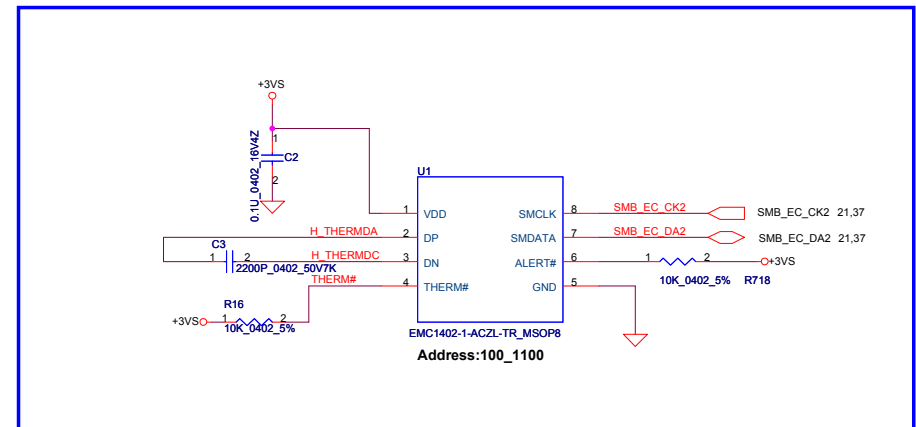
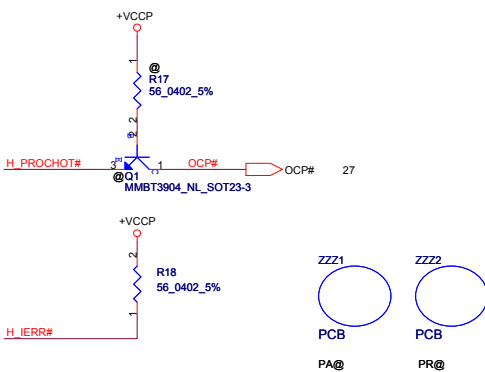
I2C / SMBUS ADDRESSING

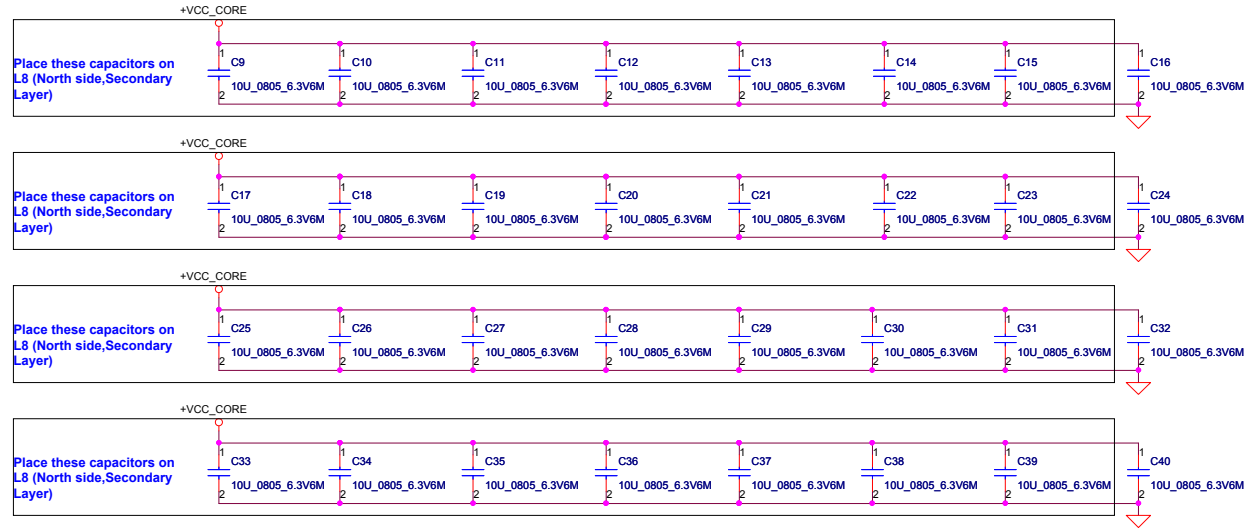
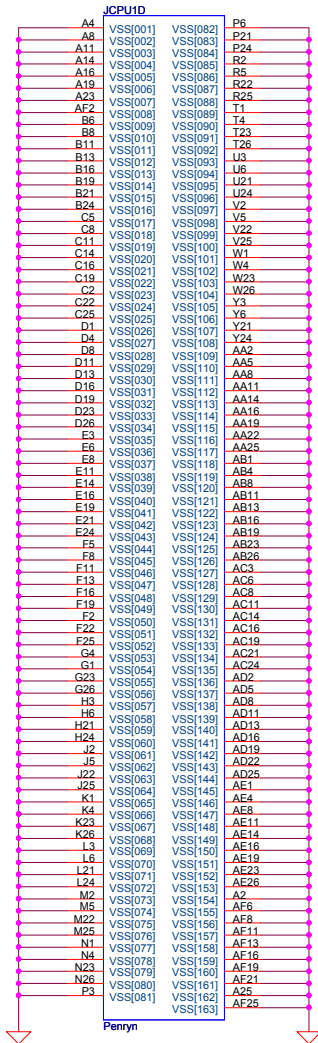
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0



JAL50 Discrete power sequence AC mode



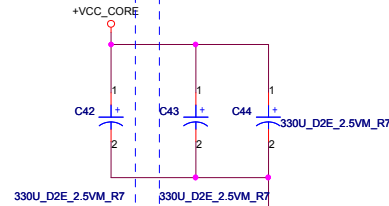




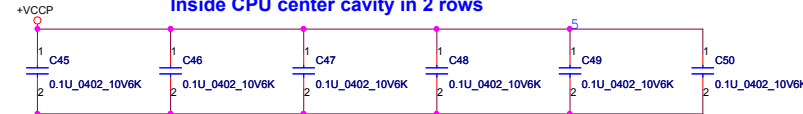
Mid Frequency Decoupling

Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF

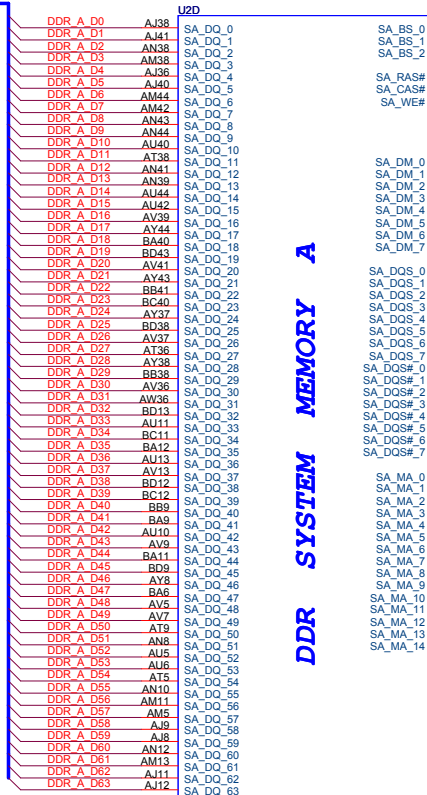


Inside CPU center cavity in 2 rows



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15 DDR_A_D[0..63]



U2D

DDR SYSTEM MEMORY A

CANTIGA ES_FCBGA1329

SA_BS_0
SA_BS_1
SA_BS_2

SA_RAS#
SA_CAS#
SA_WE#

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7

SA_DQS#_0
SA_DQS#_1
SA_DQS#_2
SA_DQS#_3
SA_DQS#_4
SA_DQS#_5
SA_DQS#_6
SA_DQS#_7

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14

BD21 DDR_A_BS0
BG18 DDR_A_BS1
AT25 DDR_A_BS2

BB20 DDR_A_RAS#
BD20 DDR_A_CAS#
AY20 DDR_A_WE#

DDR_A_DM[0..7] 15

DDR_A_DQS[0..7] 15

DDR_A_DQS#[0..7] 15

DDR_A_MA[0..14] 15

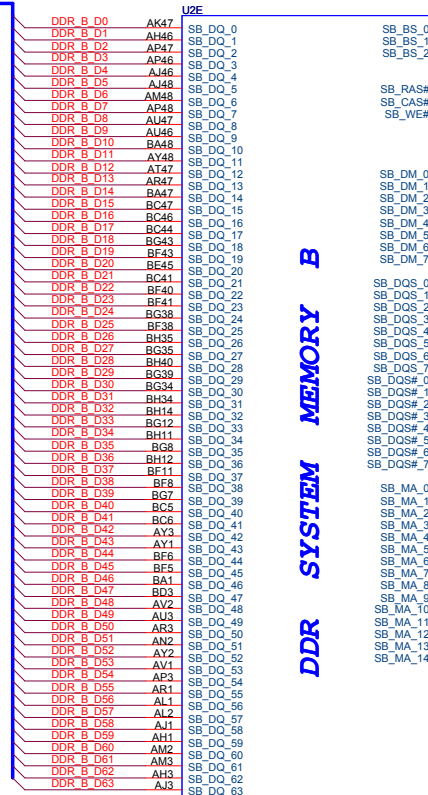
AM37 DDR_A_DM0
AT41 DDR_A_DM1
AY41 DDR_A_DM2
AU39 DDR_A_DM3
BB12 DDR_A_DM4
AT6 DDR_A_DM5
AT7 DDR_A_DM6
AJ5 DDR_A_DM7

AJ44 DDR_A_DQS0
AT44 DDR_A_DQS1
BA43 DDR_A_DQS2
BC37 DDR_A_DQS3
AW12 DDR_A_DQS4
BC1 DDR_A_DQS5
AU8 DDR_A_DQS6
AM7 DDR_A_DQS7

AJ43 DDR_A_DQS#0
AT43 DDR_A_DQS#1
BA44 DDR_A_DQS#2
BD37 DDR_A_DQS#3
AY12 DDR_A_DQS#4
BD8 DDR_A_DQS#5
AU9 DDR_A_DQS#6
AM8 DDR_A_DQS#7

BA21 DDR_A_MA0
BC24 DDR_A_MA1
BG24 DDR_A_MA2
BH24 DDR_A_MA3
BG25 DDR_A_MA4
BA24 DDR_A_MA5
BD24 DDR_A_MA6
BG27 DDR_A_MA7
BF25 DDR_A_MA8
AW24 DDR_A_MA9
BC21 DDR_A_MA10
BG26 DDR_A_MA11
BH26 DDR_A_MA12
BH17 DDR_A_MA13
AY25 DDR_A_MA14

16 DDR_B_D[0..63]



U2E

DDR SYSTEM MEMORY B

CANTIGA ES_FCBGA1329

SB_BS_0
SB_BS_1
SB_BS_2

SB_RAS#
SB_CAS#
SB_WE#

SB_DM_0
SB_DM_1
SB_DM_2
SB_DM_3
SB_DM_4
SB_DM_5
SB_DM_6
SB_DM_7

SB_DQS_0
SB_DQS_1
SB_DQS_2
SB_DQS_3
SB_DQS_4
SB_DQS_5
SB_DQS_6
SB_DQS_7

SB_DQS#_0
SB_DQS#_1
SB_DQS#_2
SB_DQS#_3
SB_DQS#_4
SB_DQS#_5
SB_DQS#_6
SB_DQS#_7

SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
SB_MA_7
SB_MA_8
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14

BC16 DDR_B_BS0
BB17 DDR_B_BS1
BB33 DDR_B_BS2

AU17 DDR_B_RAS#
BG16 DDR_B_CAS#
BF14 DDR_B_WE#

DDR_B_DM[0..7] 16

DDR_B_DQS[0..7] 16

DDR_B_DQS#[0..7] 16

DDR_B_MA[0..14] 16

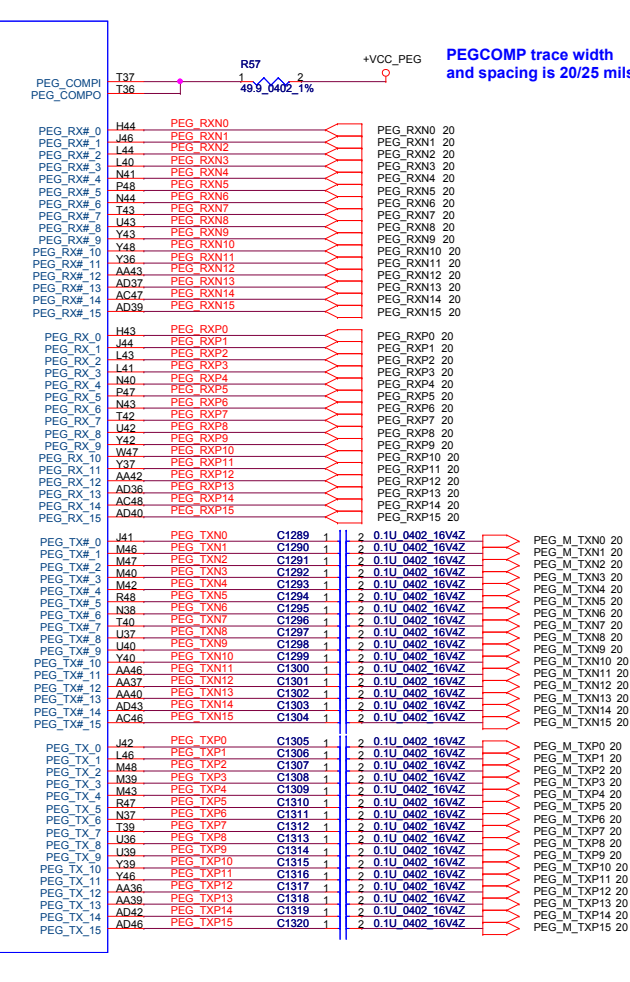
AM47 DDR_B_DM0
AY47 DDR_B_DM1
BD40 DDR_B_DM2
BF35 DDR_B_DM3
BG11 DDR_B_DM4
BA3 DDR_B_DM5
AP1 DDR_B_DM6
AK2 DDR_B_DM7

AL47 DDR_B_DQS0
AV48 DDR_B_DQS1
BG41 DDR_B_DQS2
BG37 DDR_B_DQS3
BH9 DDR_B_DQS4
BB2 DDR_B_DQS5
AU1 DDR_B_DQS6
AN6 DDR_B_DQS7

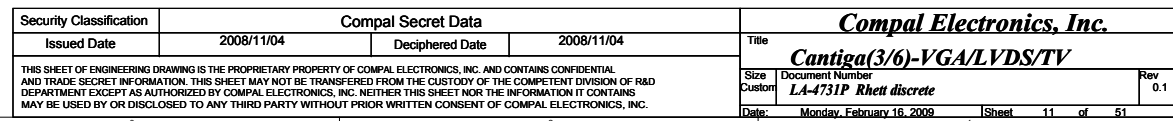
AL46 DDR_B_DQS#0
AV47 DDR_B_DQS#1
BH41 DDR_B_DQS#2
BH37 DDR_B_DQS#3
BG9 DDR_B_DQS#4
BC9 DDR_B_DQS#5
AT2 DDR_B_DQS#6
AN5 DDR_B_DQS#7

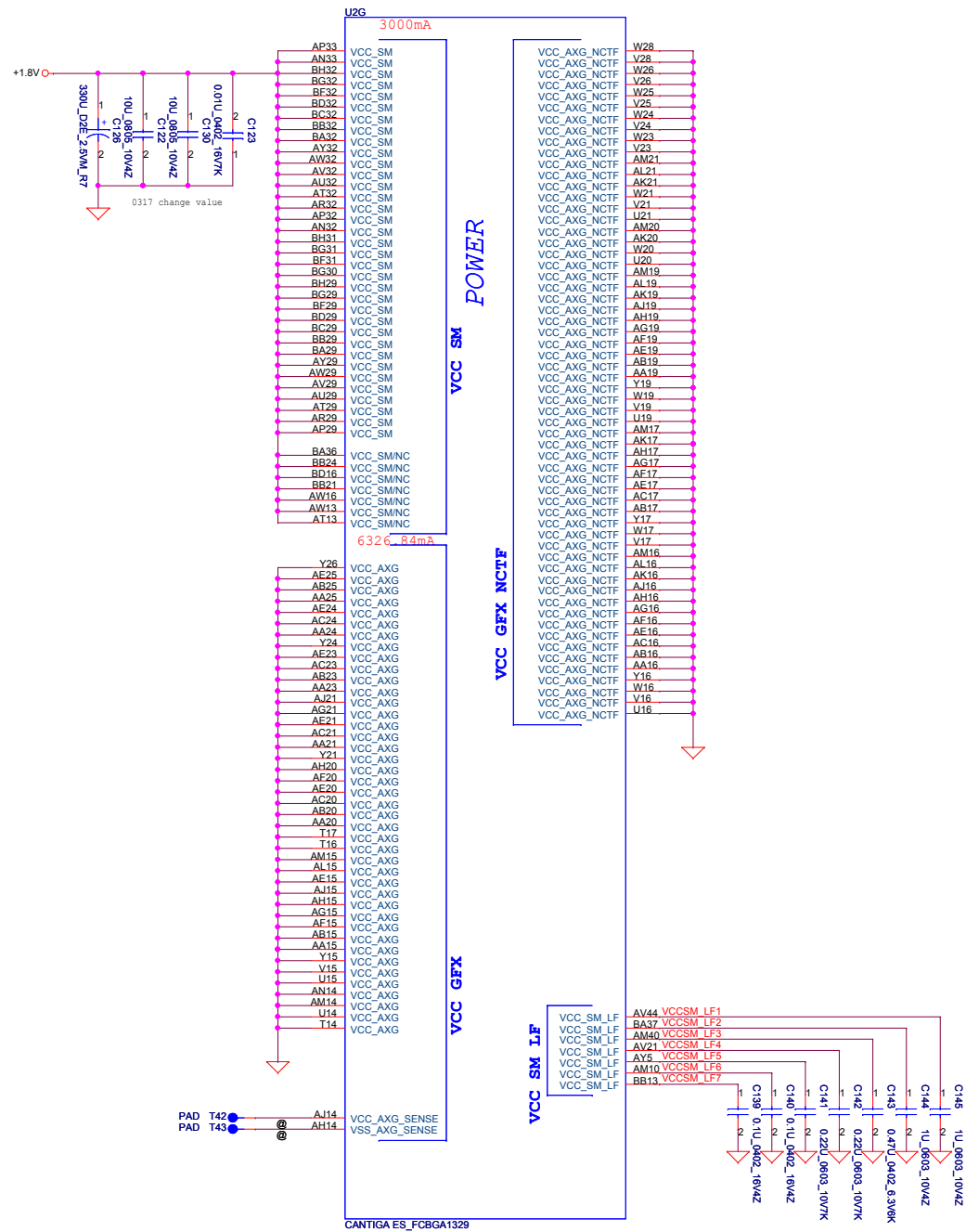
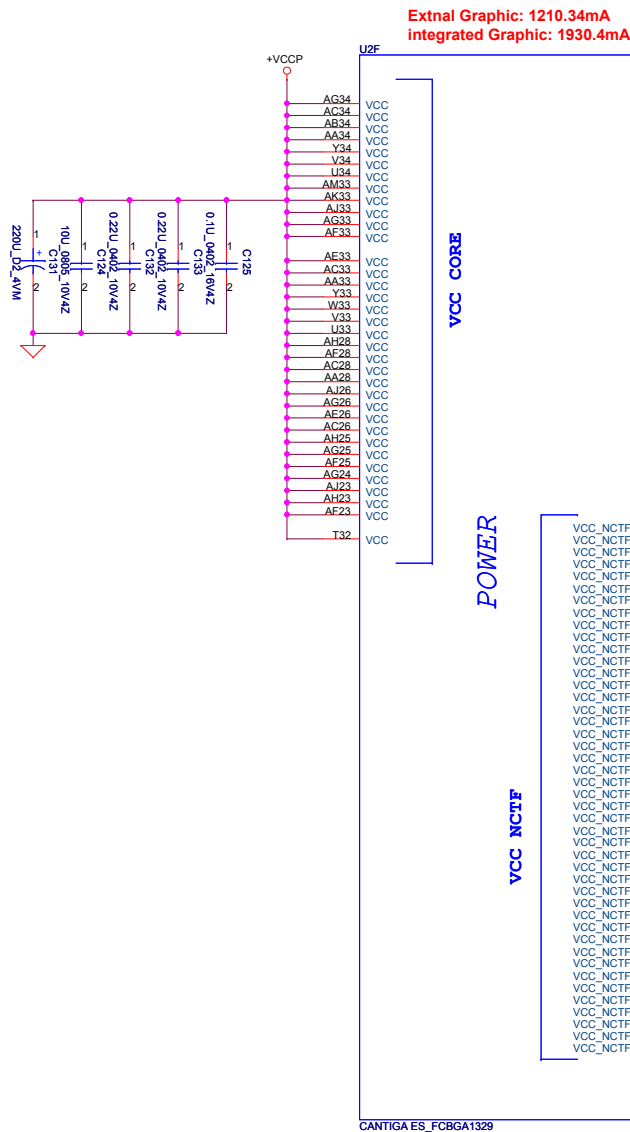
AV17 DDR_B_MA0
BA25 DDR_B_MA1
BC25 DDR_B_MA2
AU25 DDR_B_MA3
AW25 DDR_B_MA4
BB28 DDR_B_MA5
AU28 DDR_B_MA6
AW28 DDR_B_MA7
AT33 DDR_B_MA8
BD33 DDR_B_MA9
BB16 DDR_B_MA10
AW33 DDR_B_MA11
AY33 DDR_B_MA12
BH15 DDR_B_MA13
AU33 DDR_B_MA14

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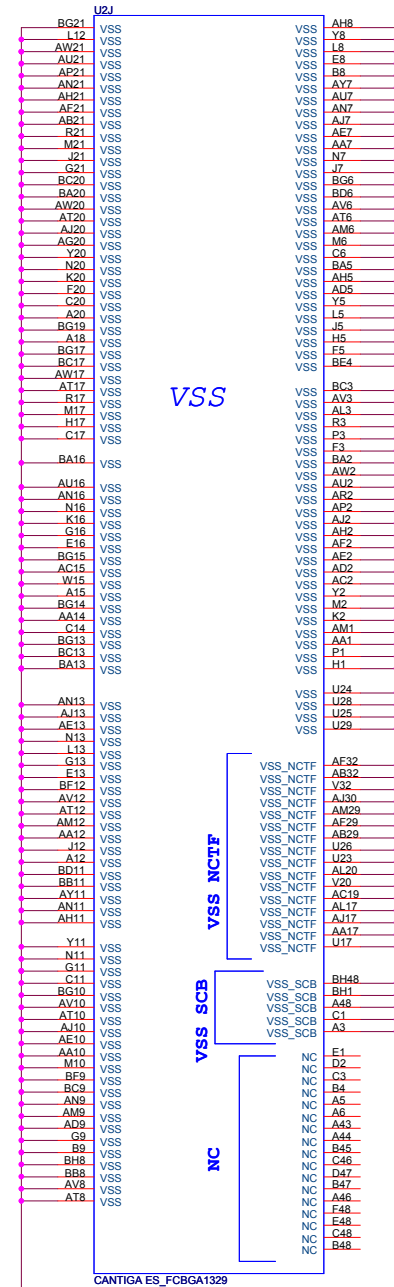
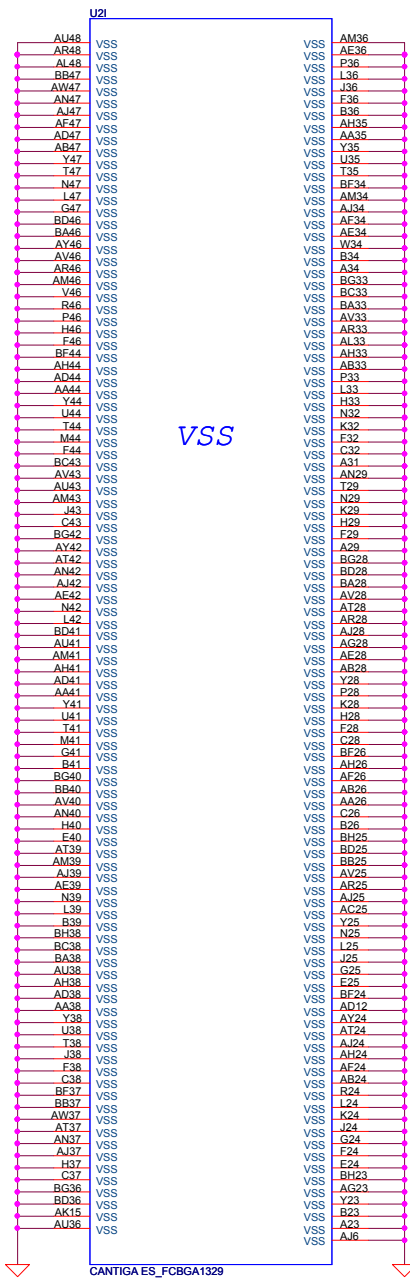


CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chipser suite with no confidentiality 1=(TLS)chipser suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

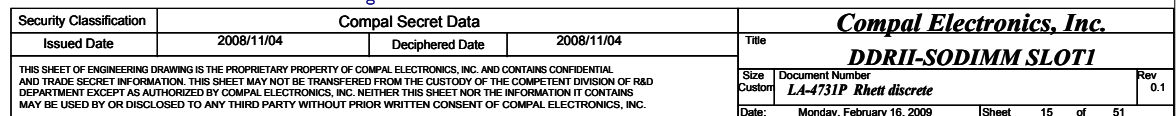
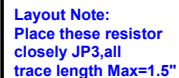
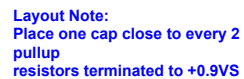


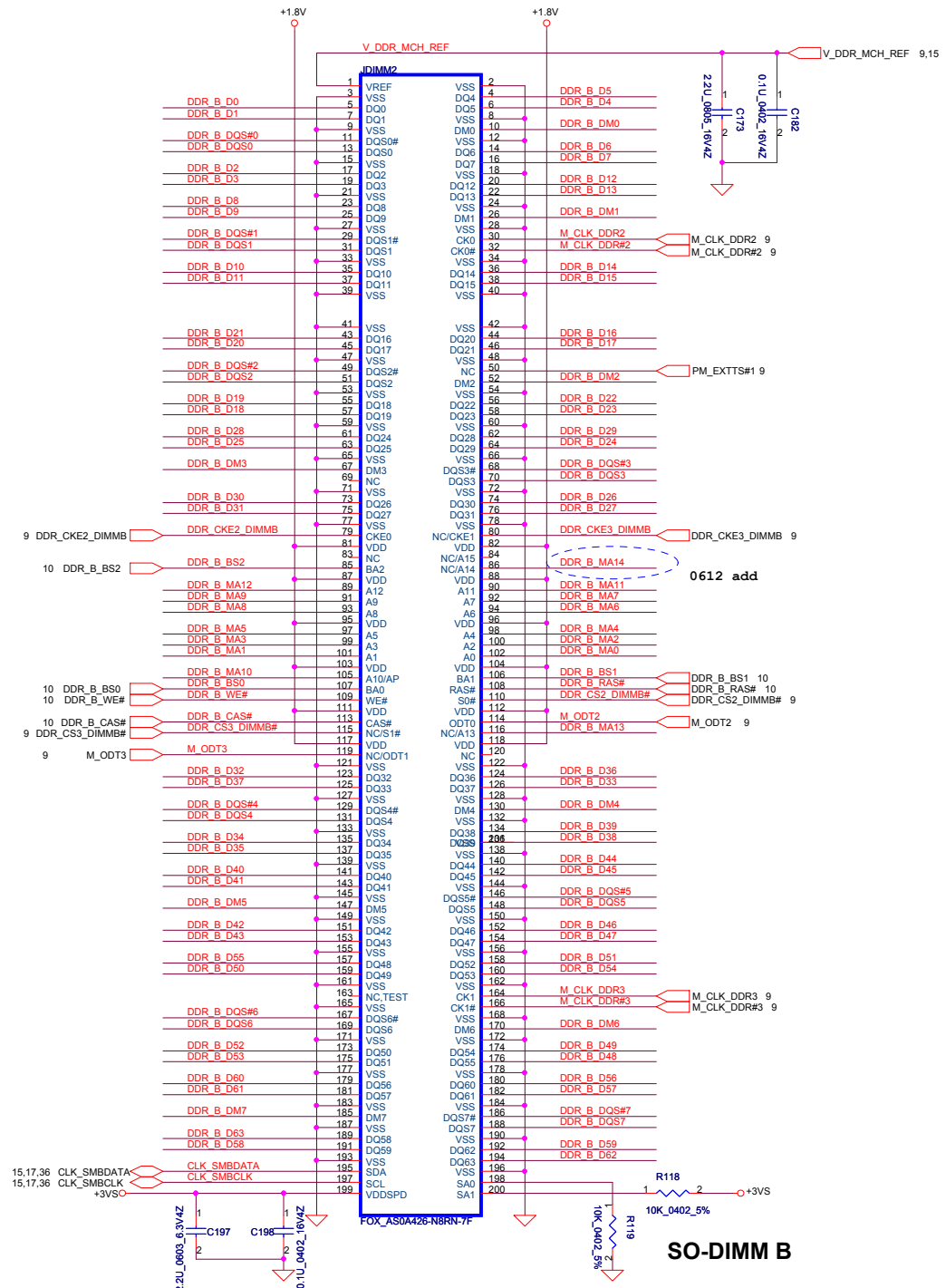
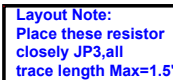
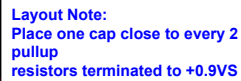


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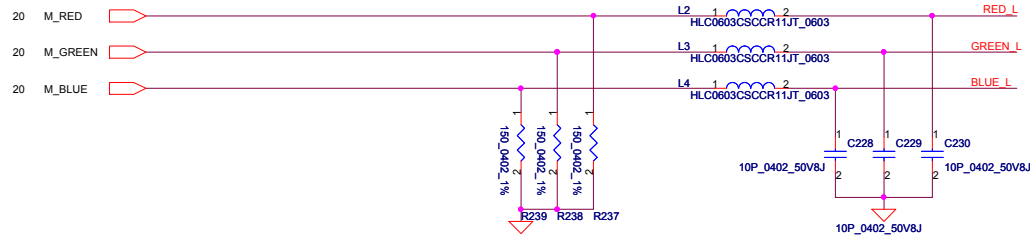
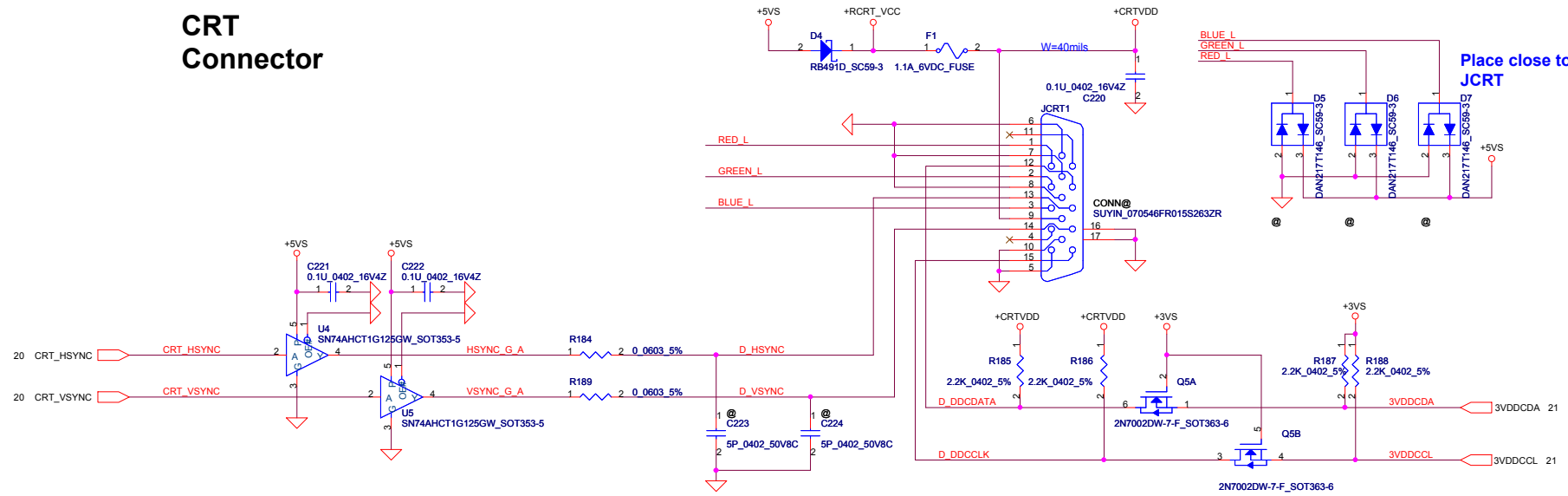
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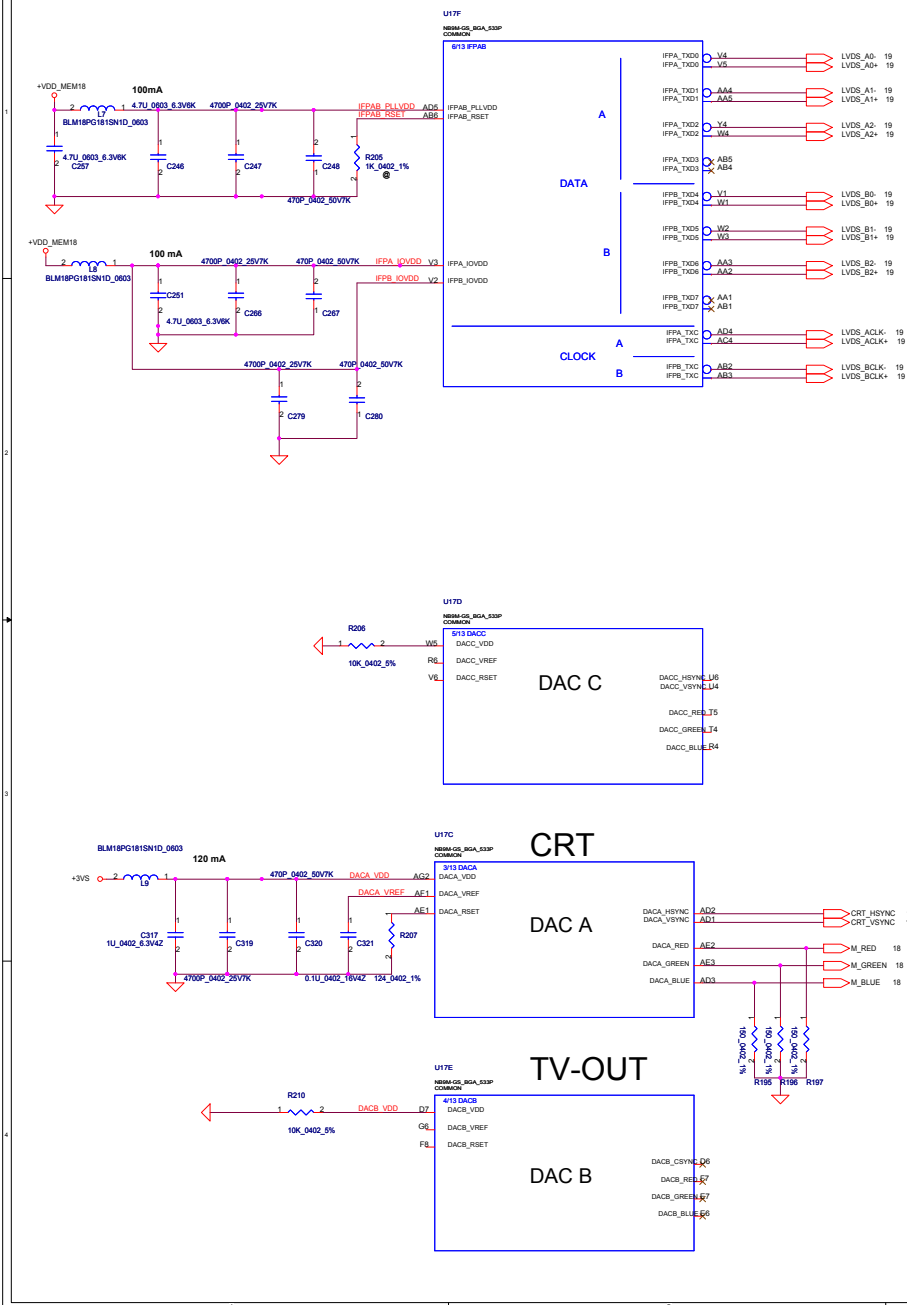
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CRT Connector

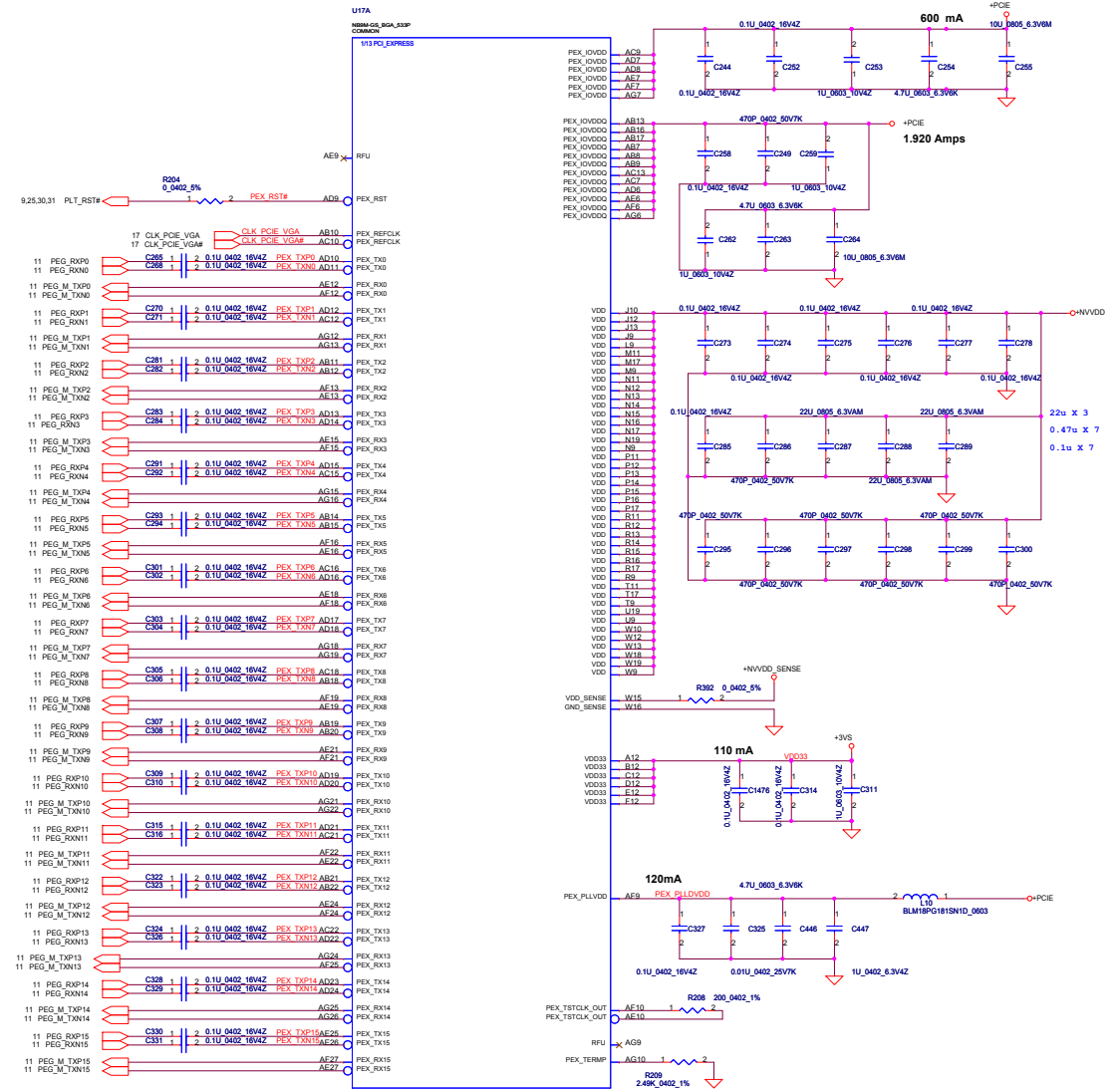


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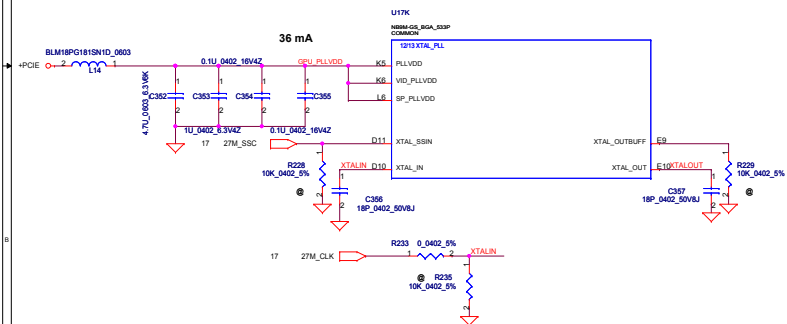
LVDS & DAC Interface



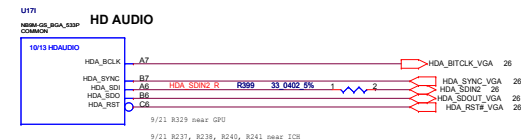
PEG Interface



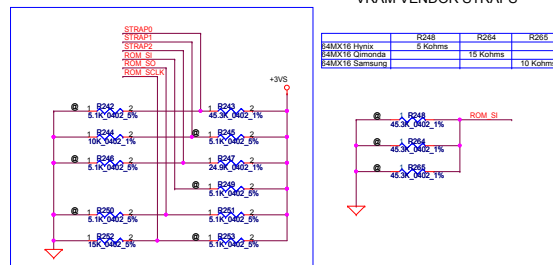
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GPU_VID1	GPU_VID0	+NVVDD
0	0	0.9V
0	1	1.09V
1	0	unused



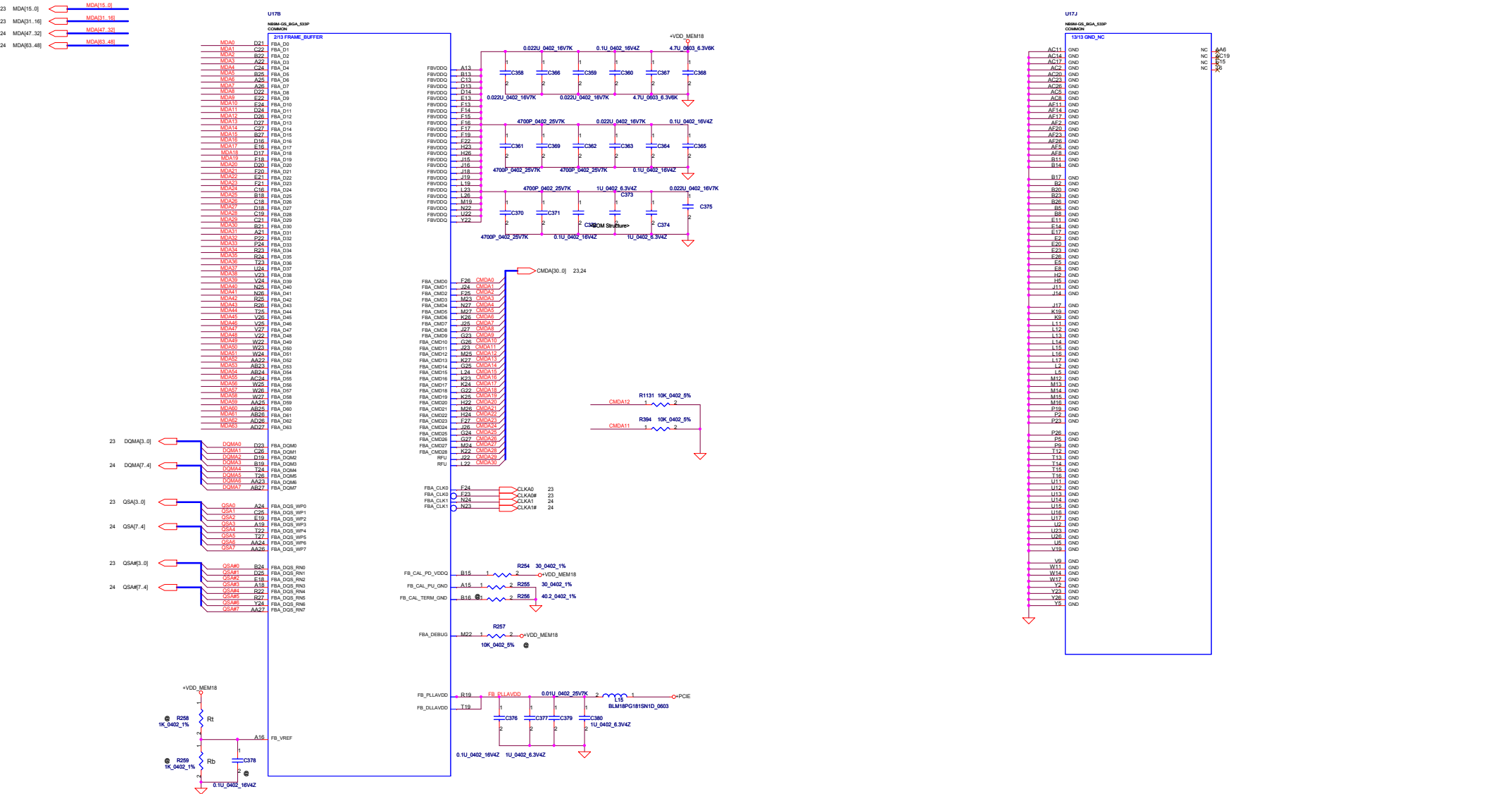
VRAM VENDOR STRAPS



	R248	R264	R265
64MX16 Hynix	5 Kohms		
64MX16 Qimonda		15 Kohms	
64MX16 Samsung			10 Kohms

Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/04	Deciphered Date	2008/11/04	Compal Electronics, Inc. Straps & HDMI LA-4731P Retht design	
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				A3	01
				DATE	BY
				11/04/2008	WJ

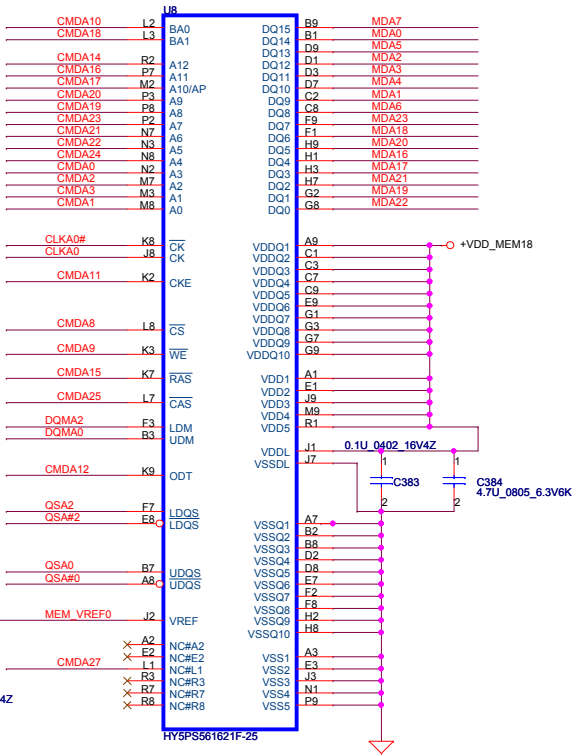
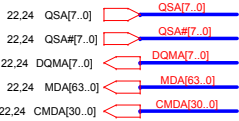
VRAM Interface



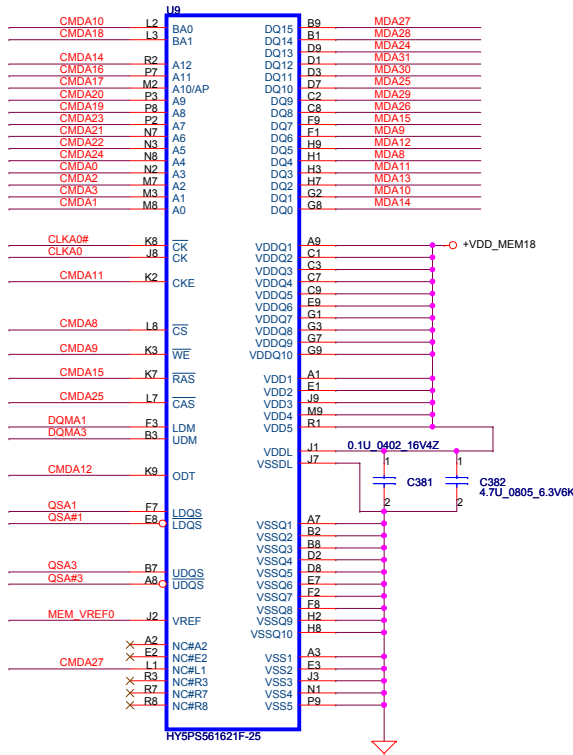
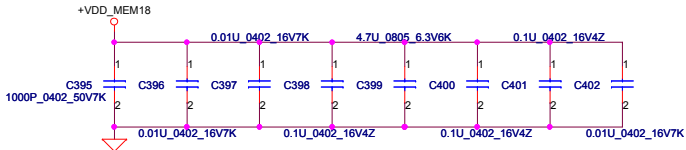
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

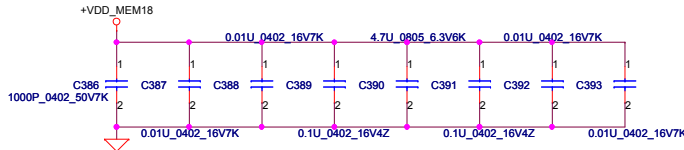
64Mx16 DDR2 400MHz*4==>512MB



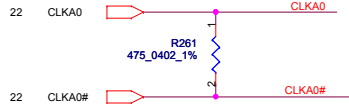
DDR2 BGA MEMORY



DDR BGA MEMORY



DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

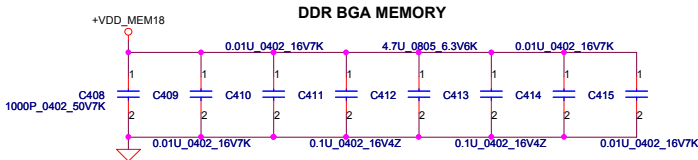
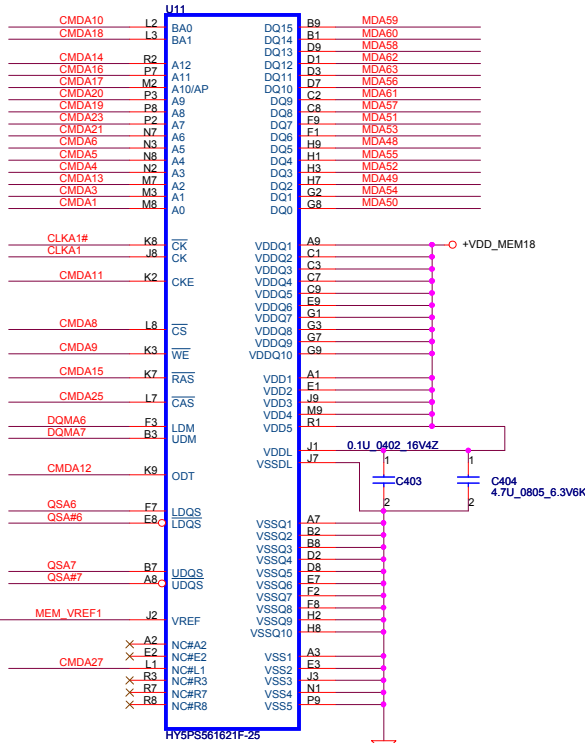
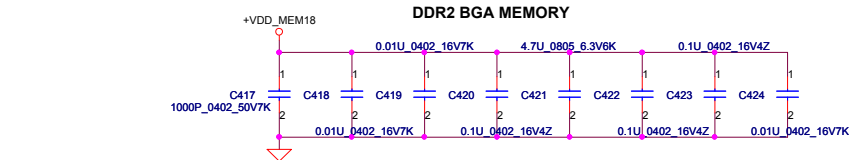
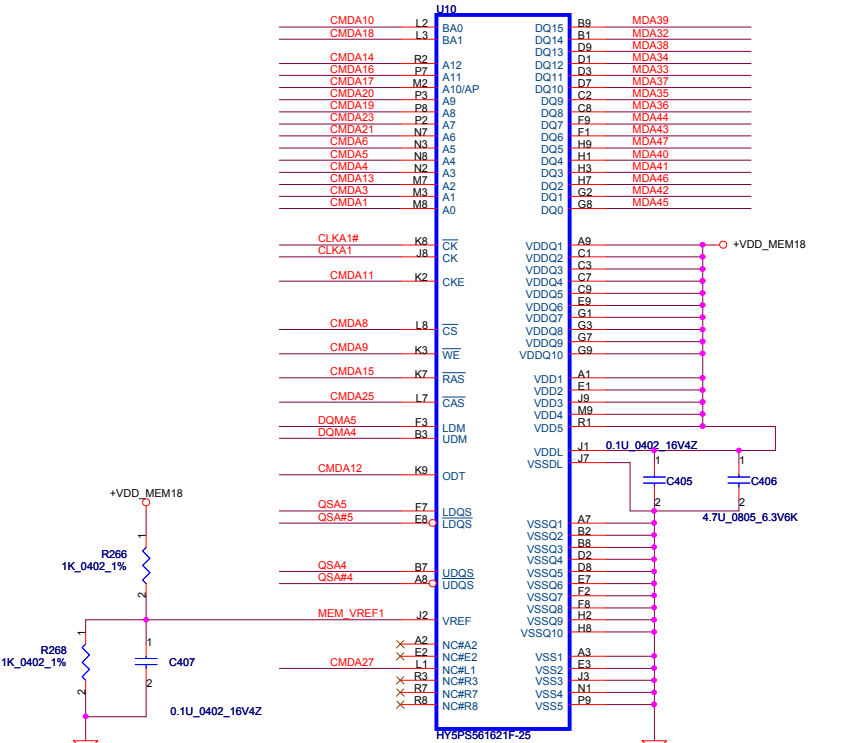
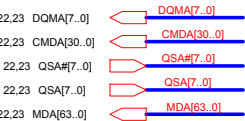


Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date	2008/11/04	Deciphered Date	2008/11/04	Title CHANNEL A EXT. 256M_1				
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				CHANNEL A EXT. 256M_1			0.1	
				Date	Monday, February 16, 2009	Sheet	7	of

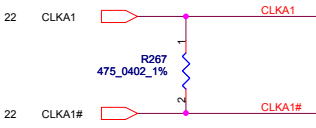
VRAM DDR2 chips (256MB & 512MB)

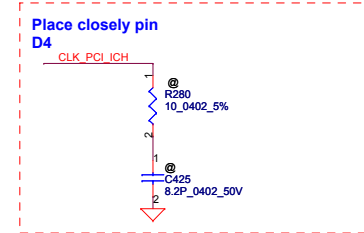
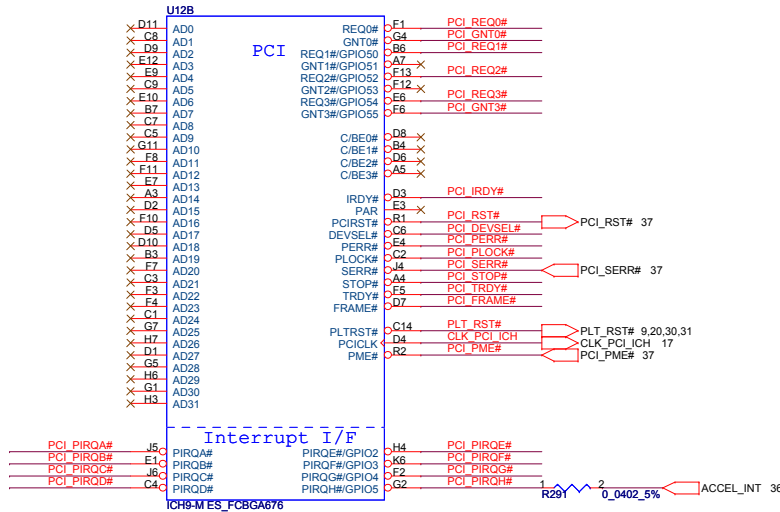
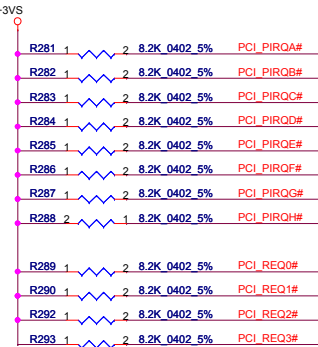
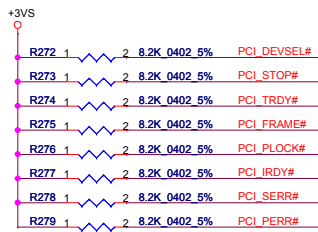
32Mx16 DDR2 400MHz *4==>256MB

64Mx16 DDR2 400MHz*4==>512MB



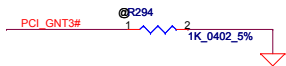
DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		





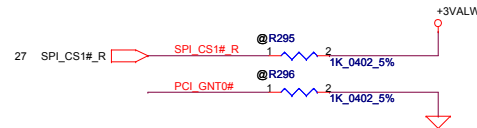
A16 swap override Strap

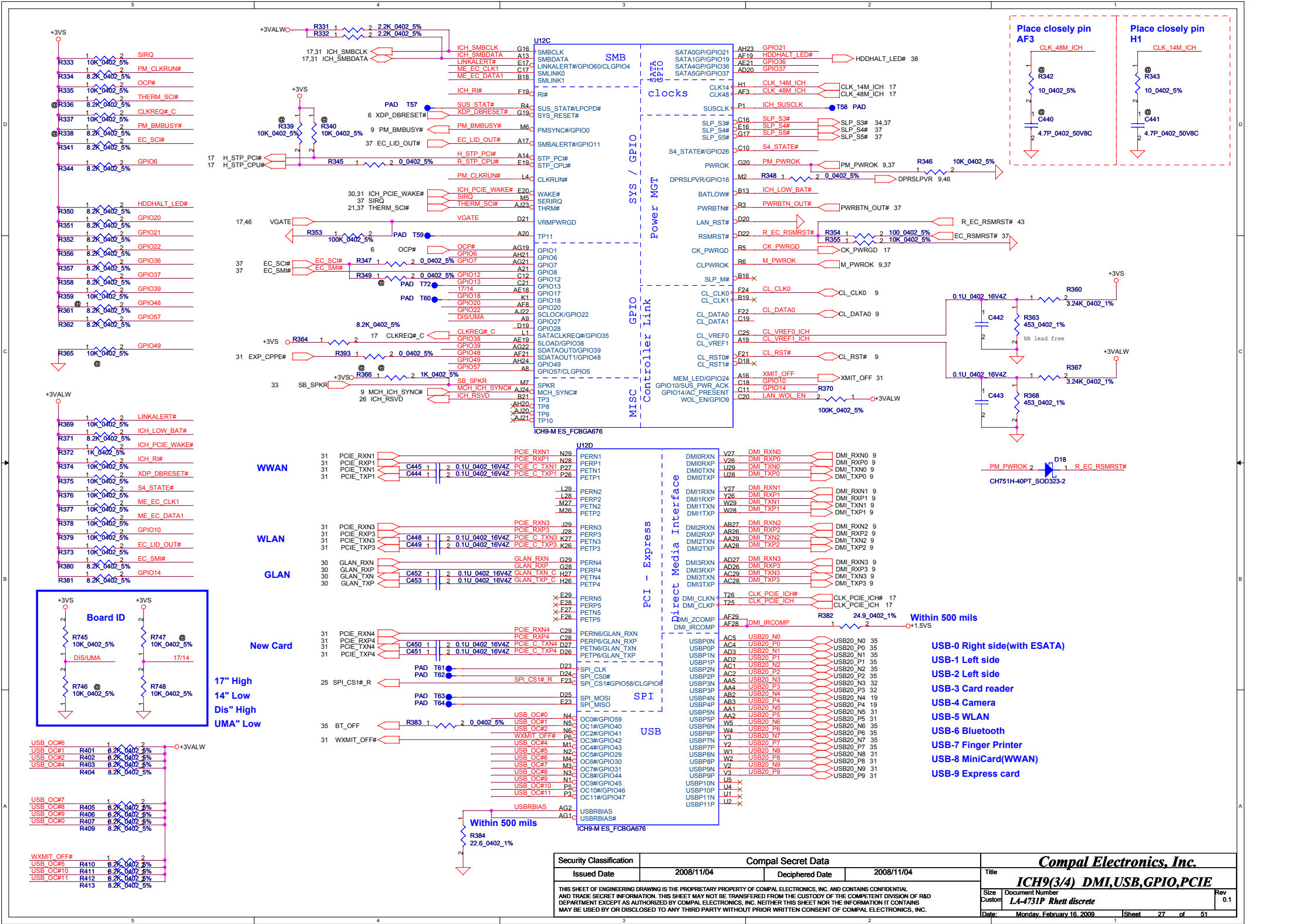
PCI_GNT3#	Low= A16 swap override Enble High= Default *
-----------	---

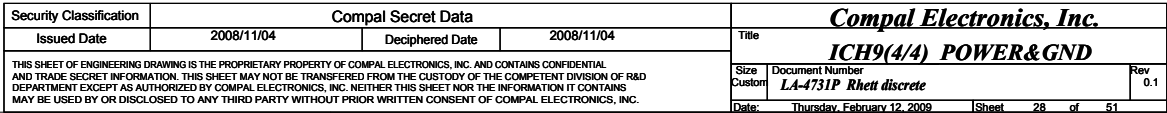


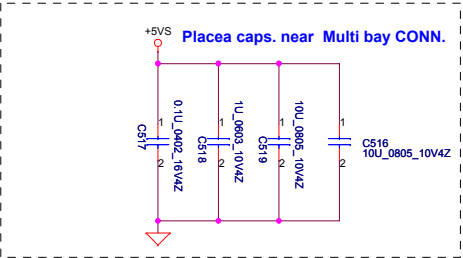
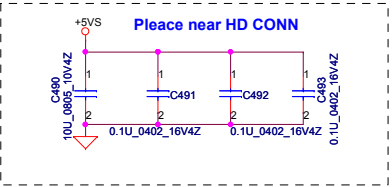
Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

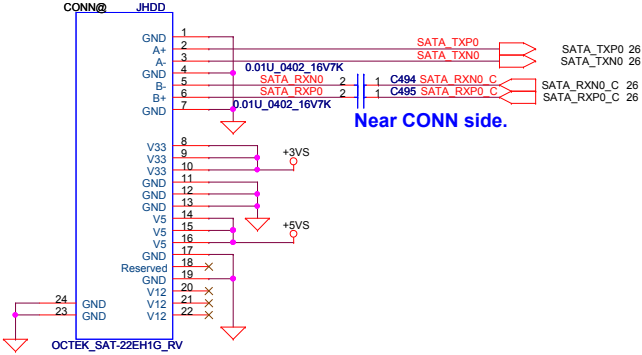




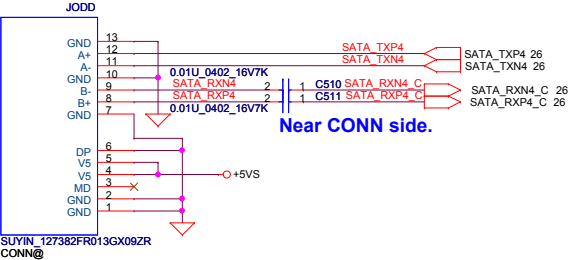


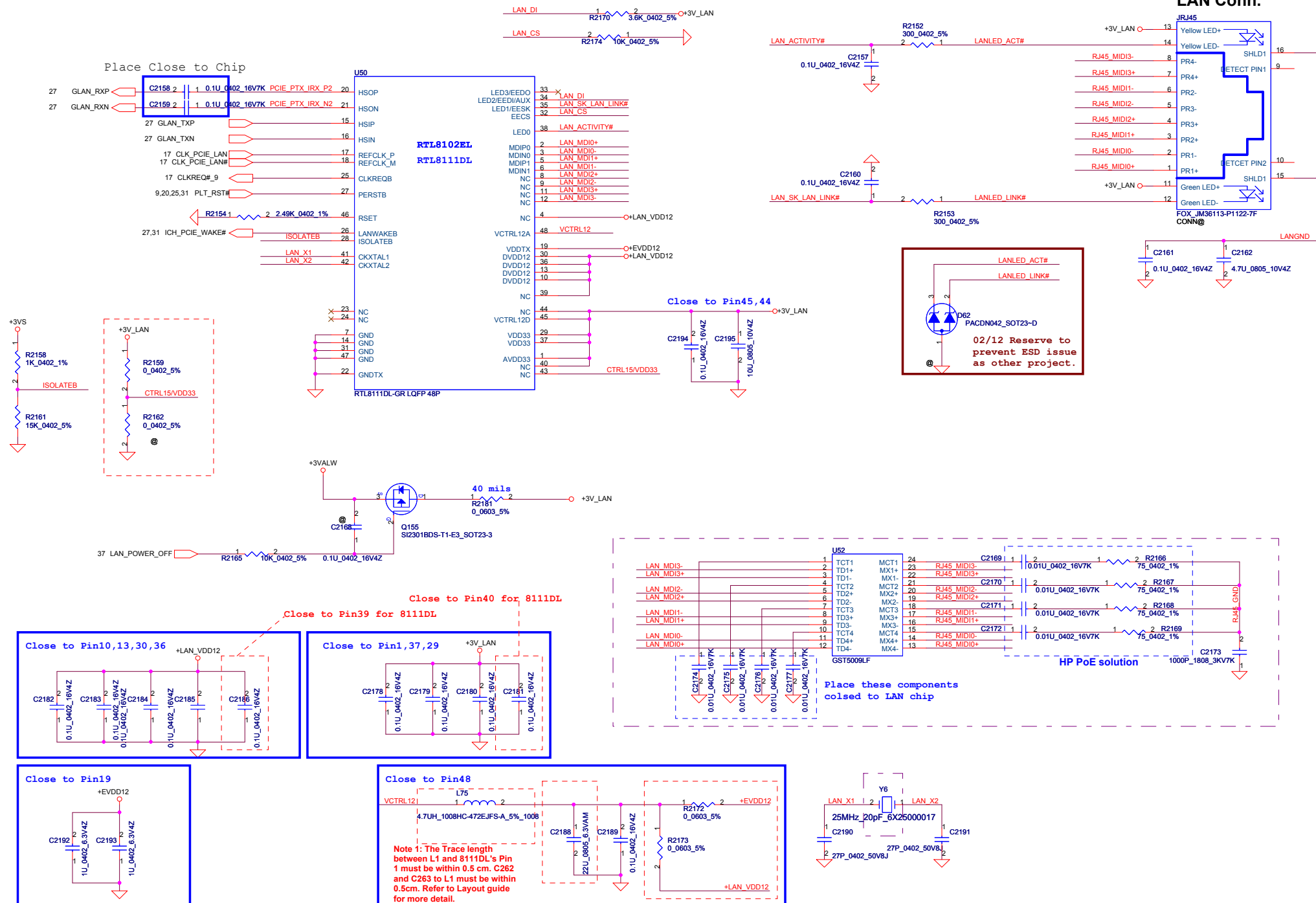


HDD Connector



CD-ROM Connector

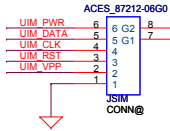
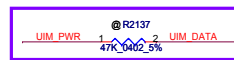


LAN Conn.

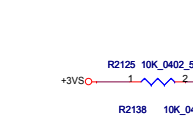
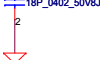
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2008/11/04	Deciphered Date	2008/11/04	Title Realtek 8111DL Giga_LAN		
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				Custom	LA-4731P Rhett discrete	0.
Date:				Monday, February 18, 2009	Sheet	20 of 54

SIM card Connector

11/17 Reserve UIM_DATA
PU to UIM_PWR



UIM_CLK



37 WWAN_POWER_OFF



37 WWAN_POWER_OFF



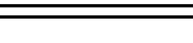
37 WWAN_POWER_OFF



37 WWAN_POWER_OFF



37 WWAN_POWER_OFF



37 WWAN_POWER_OFF



37 WWAN_POWER_OFF



37 WWAN_POWER_OFF



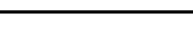
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37 WWAN_POWER_OFF



37 WWAN_POWER_OFF



37 WWAN_POWER_OFF



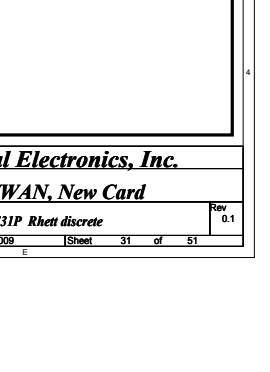
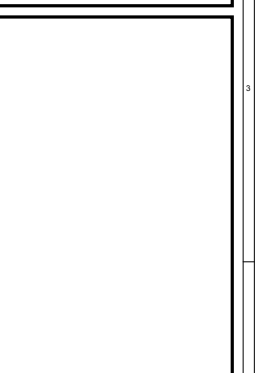
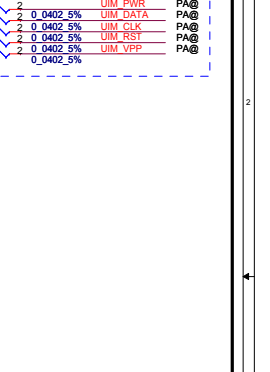
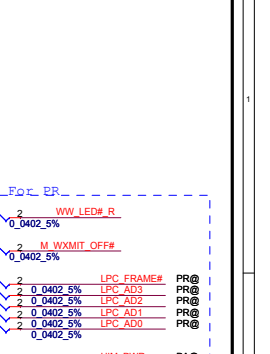
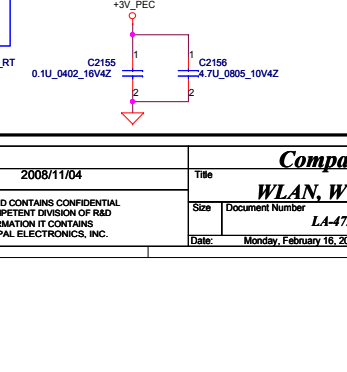
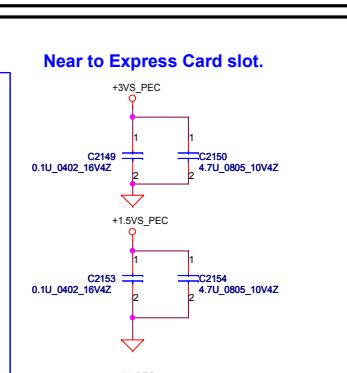
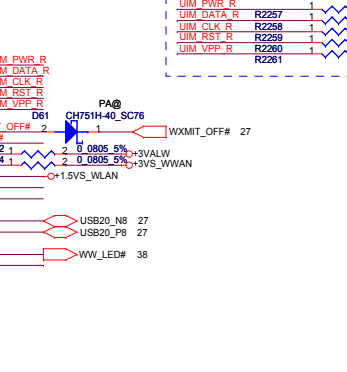
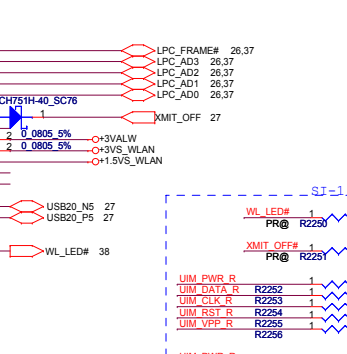
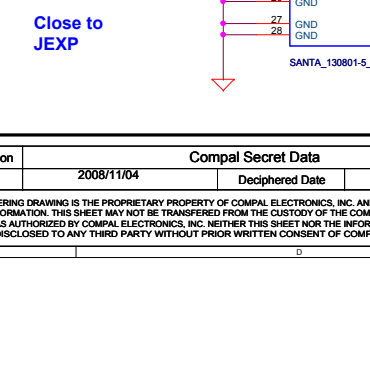
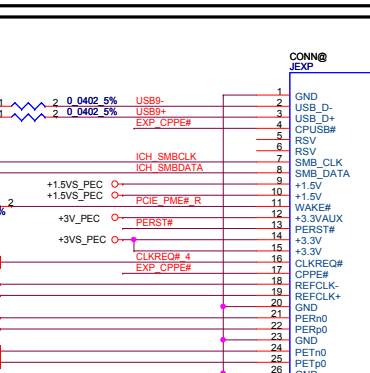
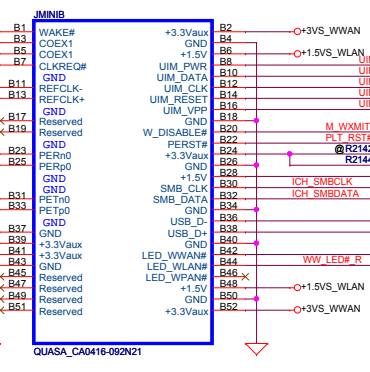
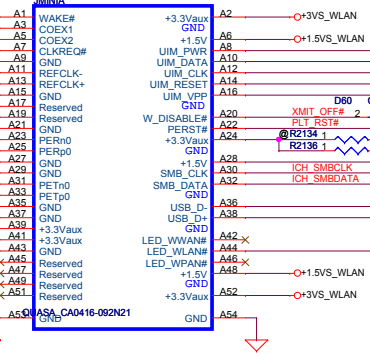
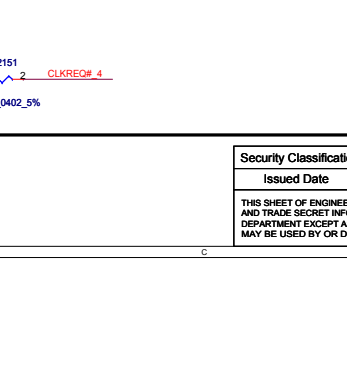
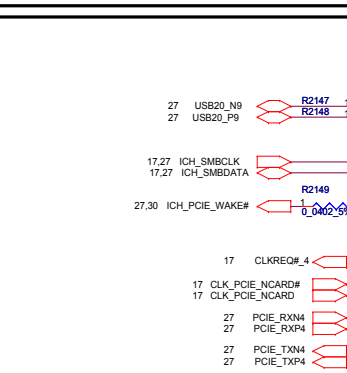
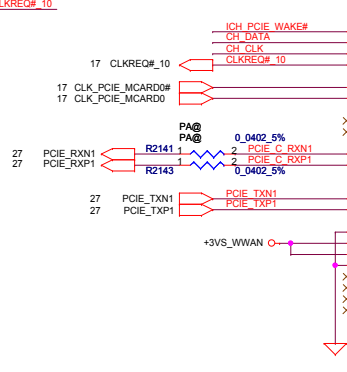
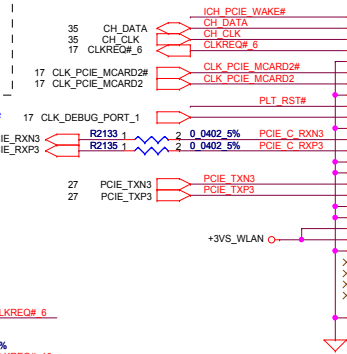
37 WWAN_POWER_OFF



37 WWAN_POWER_OFF

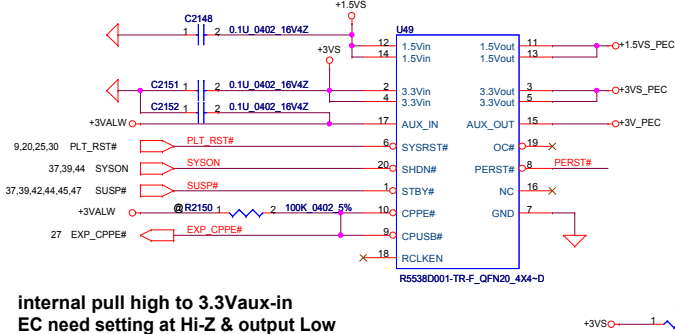


Mini Card Slot ---WLAN,WWAN



New Card

Express Card Power Switch



internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low



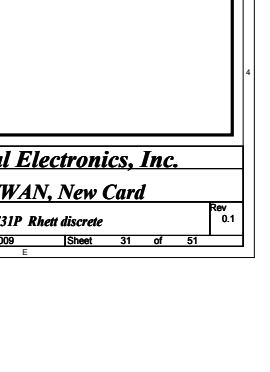
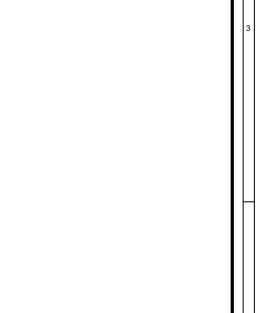
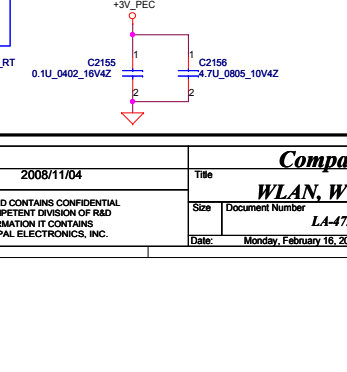
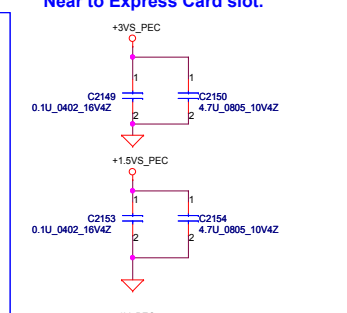
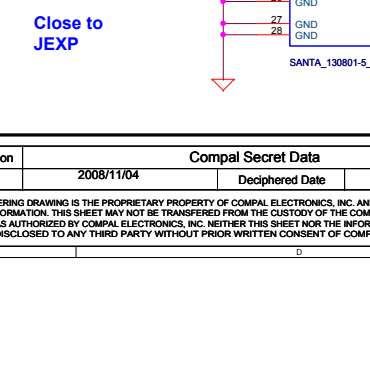
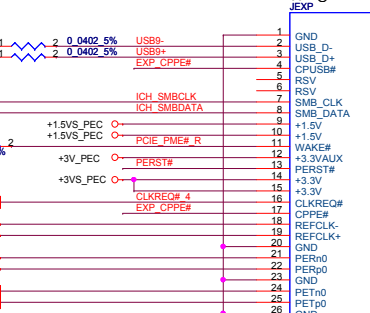
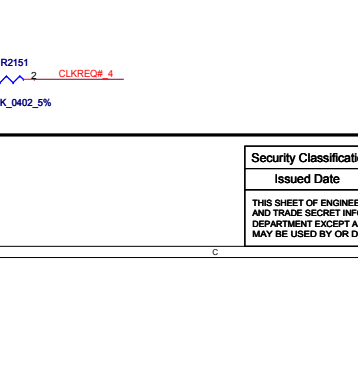
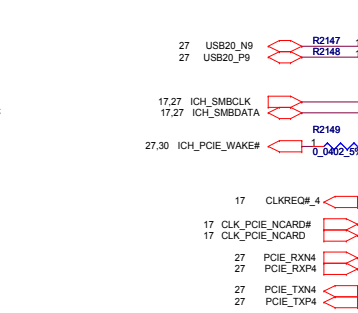
internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low



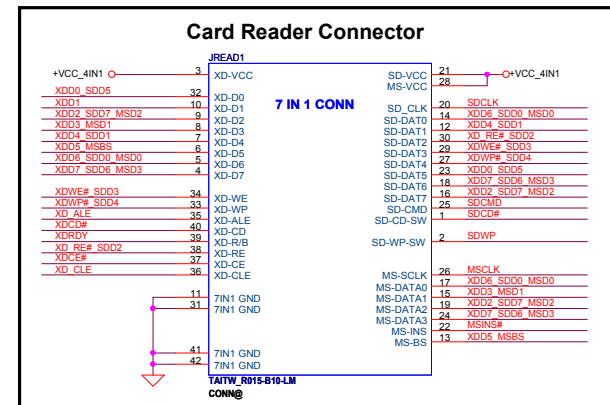
internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low



internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low



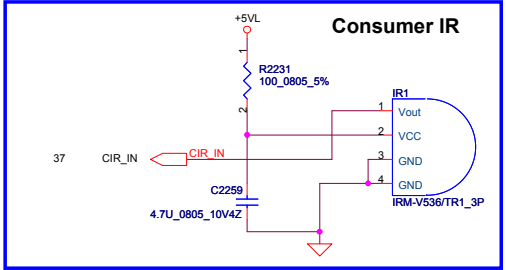
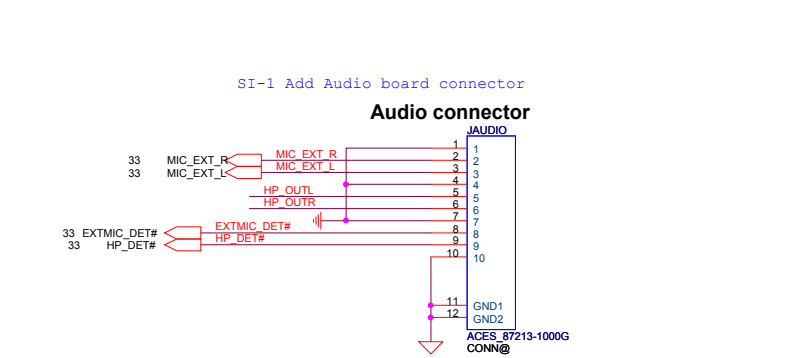
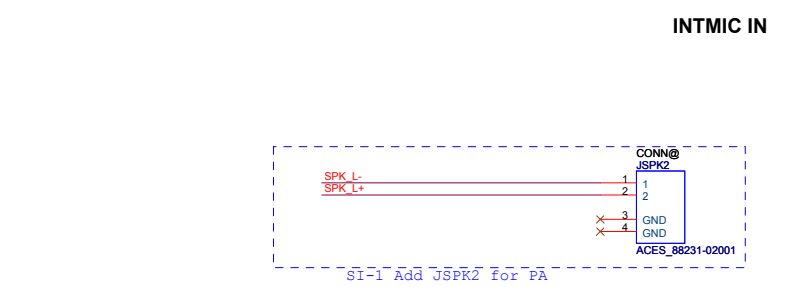
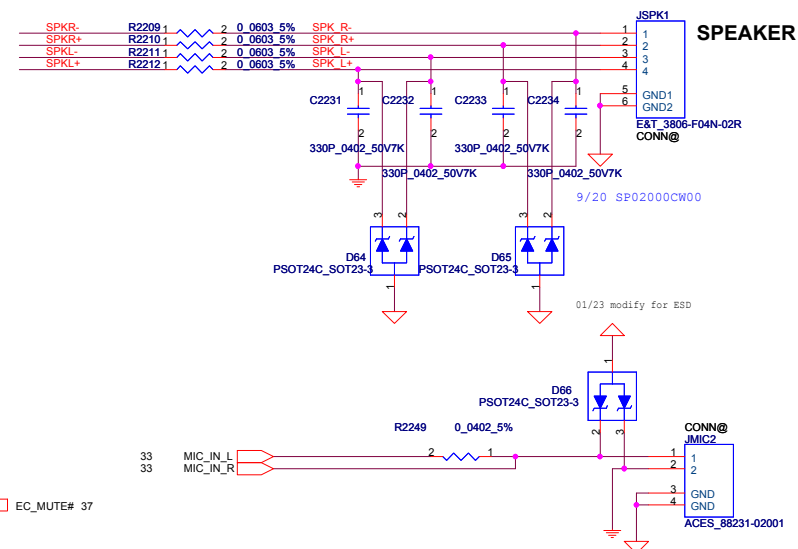
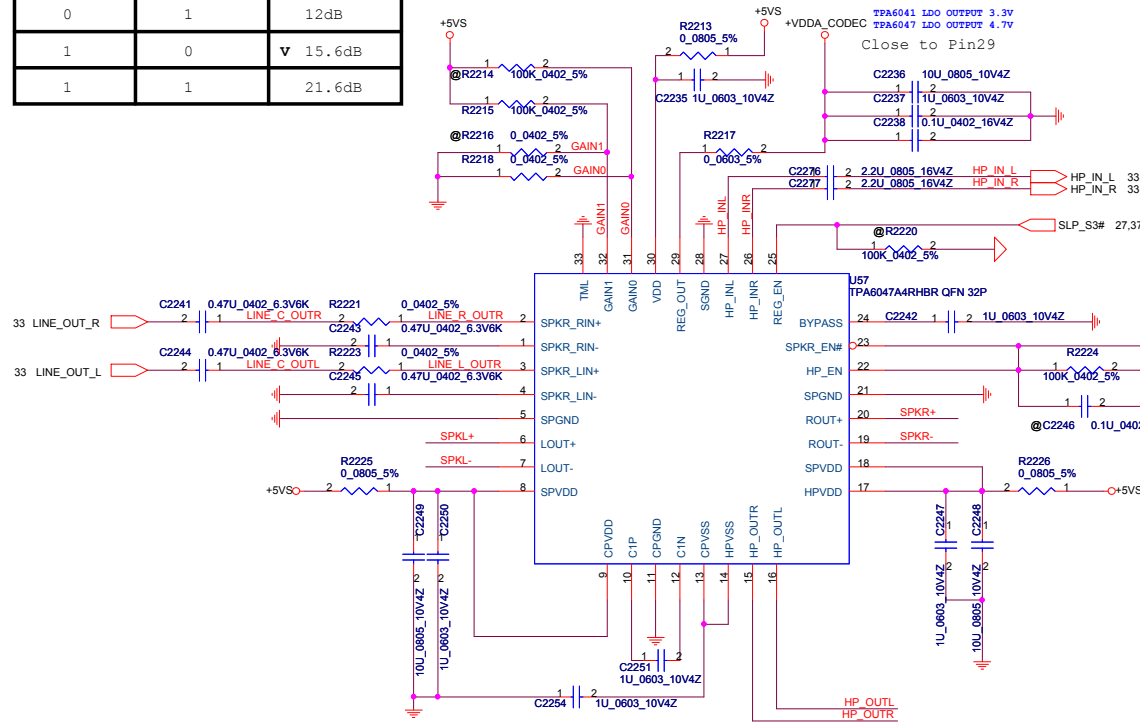
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2008/11/04		2008/11/04		WLAN, WWAN, New Card	
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		LA-4731P Rhett discrete		Rev	
				0.1	
Date: Monday, February 16, 2009		Sheet		31 of 51	



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Issued Date	2008/11/04	Deciphered Date	2008/11/04	Title	
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				Custom	0.1
				Document Number LA-4731P Rhett discrete	
Date:		Monday, February 16, 2009		Sheet	32 of 51

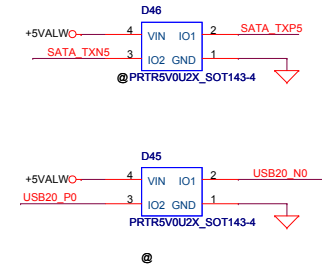
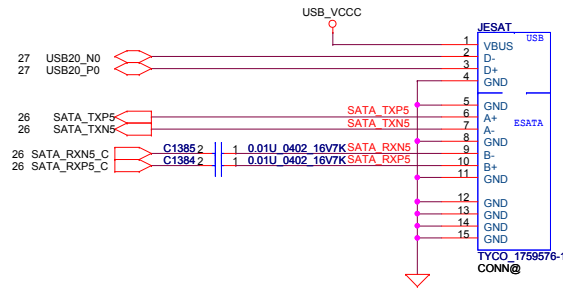
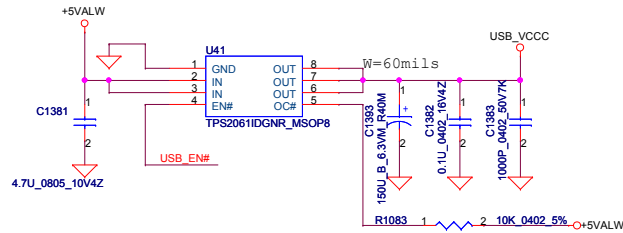
AMP. FOR INTERNAL SPEAKER

GAIN1	GAIN0	Av (inv)
0	0	10dB
0	1	12dB
1	0	15.6dB
1	1	21.6dB

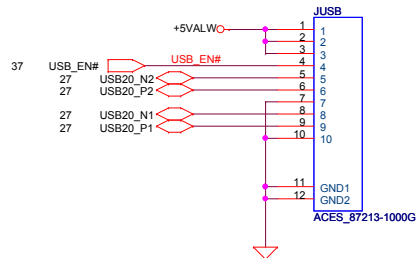


Security Classification	Compal Secret Data		Title	
Issued Date	2008/11/04	Deciphered Date	2008/11/04	AMP & Audio Jack
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				LA-4731P Rhett discrete
				Rev 0.1
				Date: Monday, February 16, 2009 Sheet 34 of 51

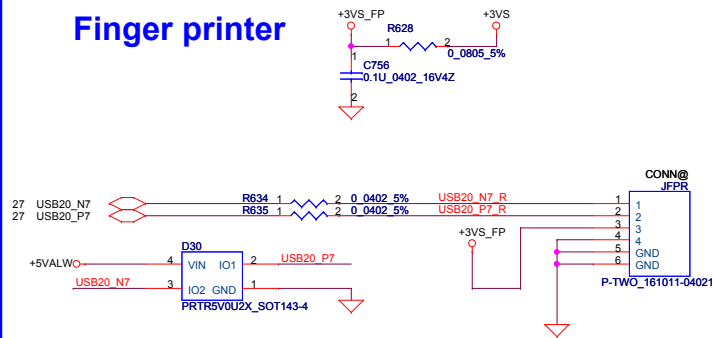
Right side ESATA/USB combination Connector



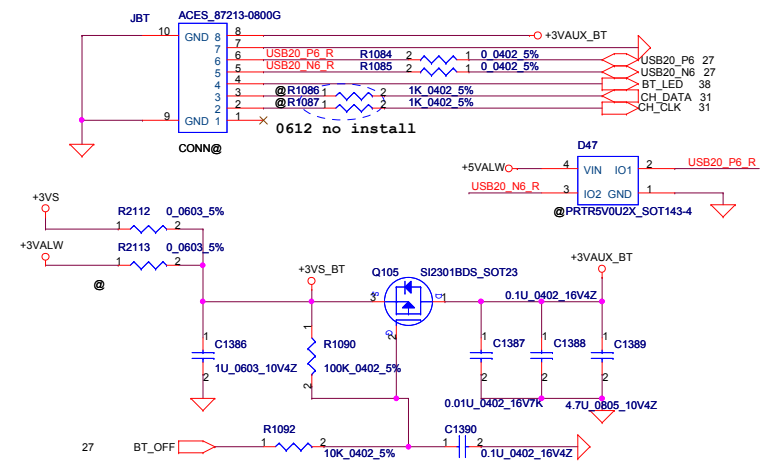
USB cable connector for Right side



Finger printer



BT Connector



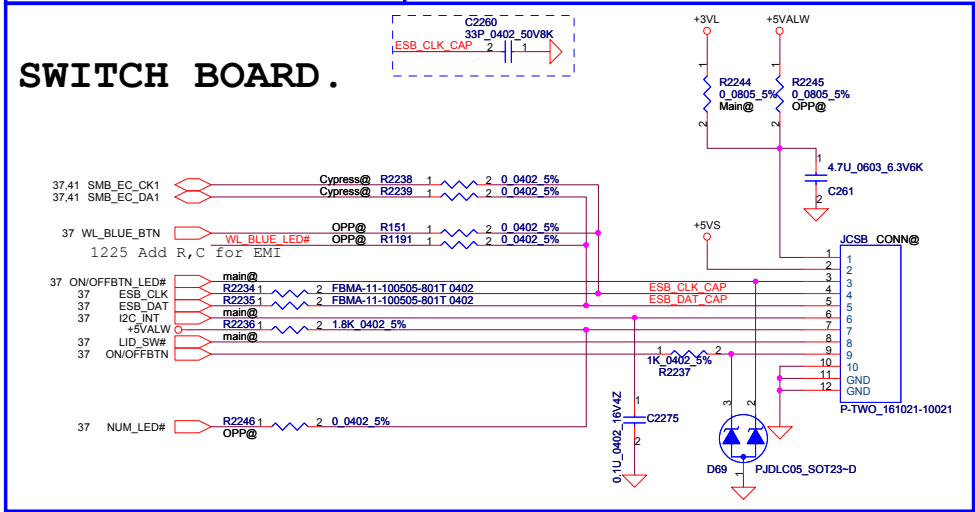
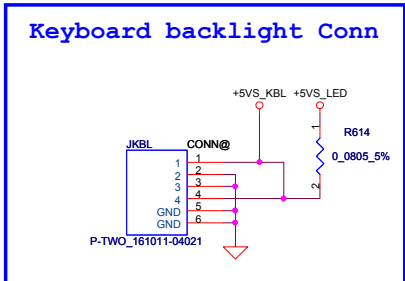
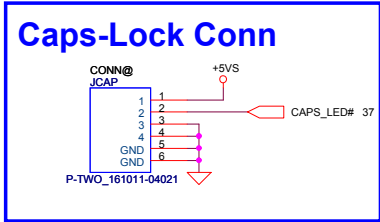
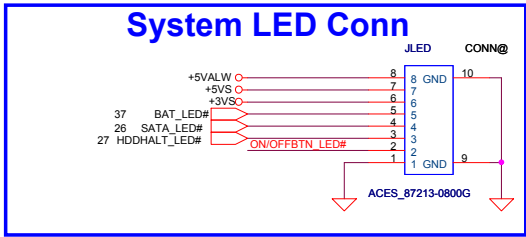
Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/04	Deciphered Date	2008/11/04	USB, BT, eSATA	
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Accelerometer-1

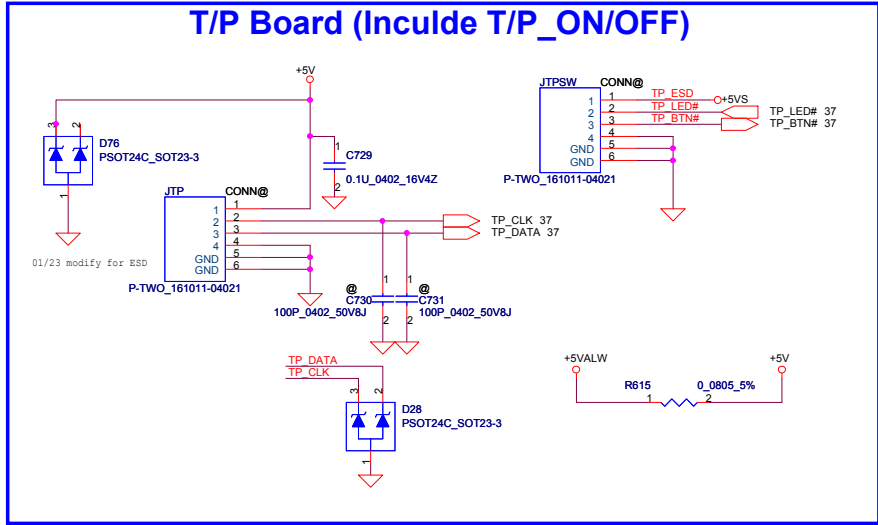
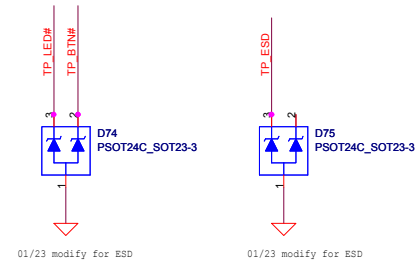
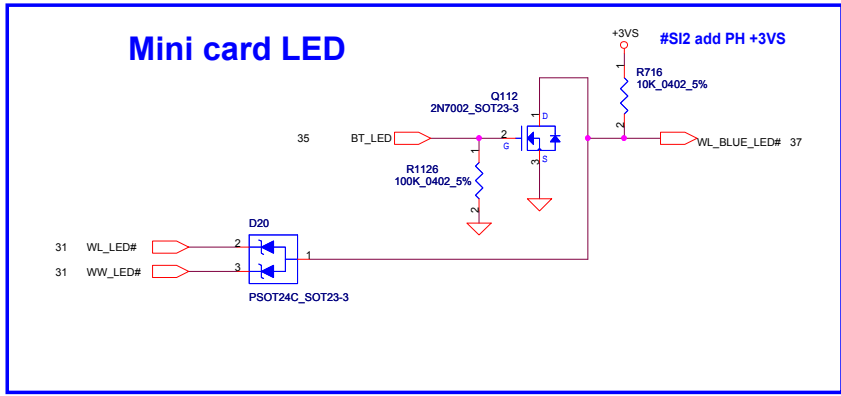


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Issued Date	2008/11/04	Deciphered Date	2008/11/04	Title BIOS ROM		
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				Size	Document Number	Rev
					LA-4731P Rhett discrete	0.1
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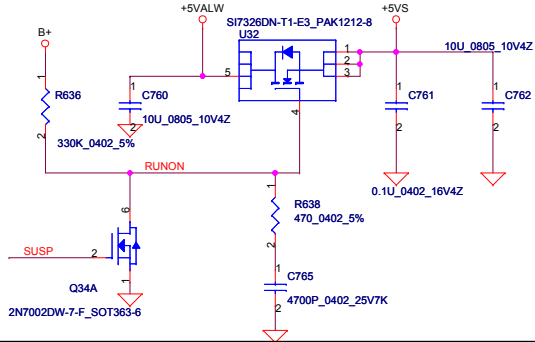


01/23 modify for ESD

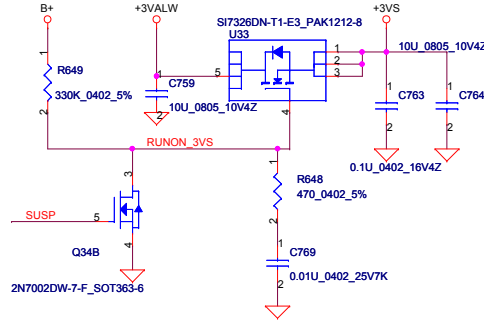


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Issued Date			Deciphered Date			Title		
2008/11/04			2008/11/04			LED, TP,KBL,Cab sensor board		
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						LA-4731P Rhett discrete		
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						38 of 51		

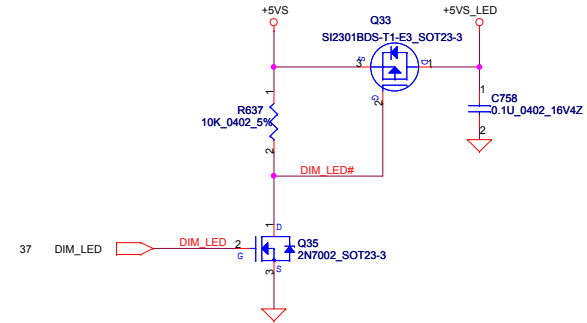
+5VALW to +5VS Transfer



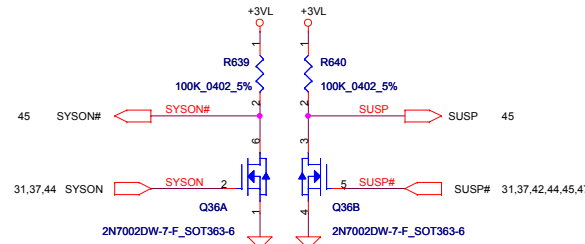
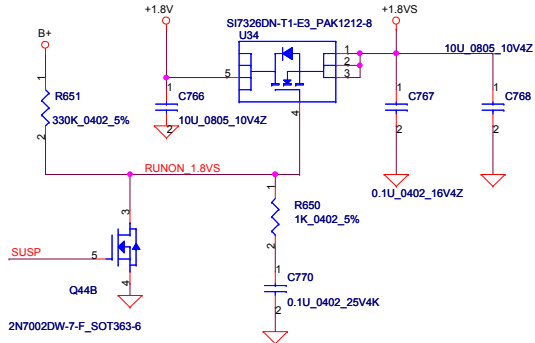
+3VALW to +3VS Transfer



DIM LED

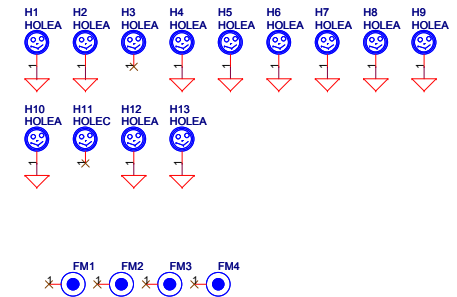
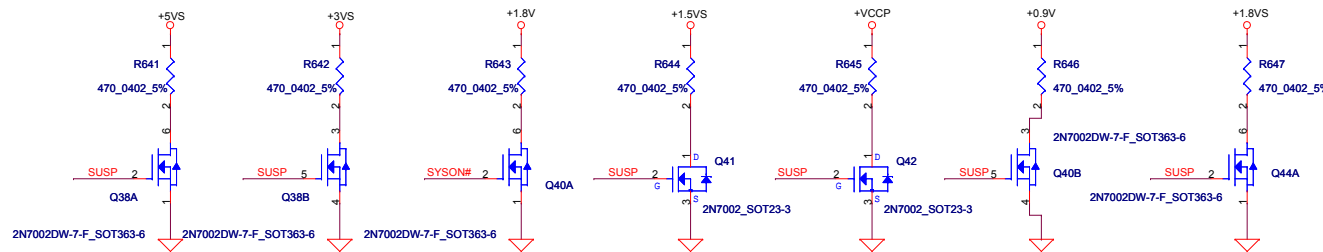


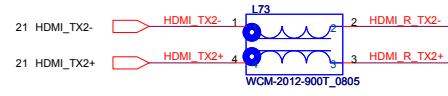
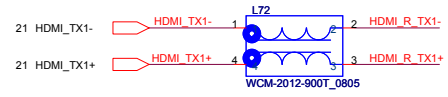
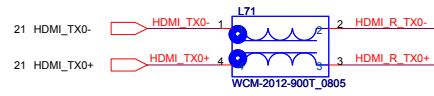
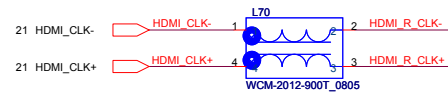
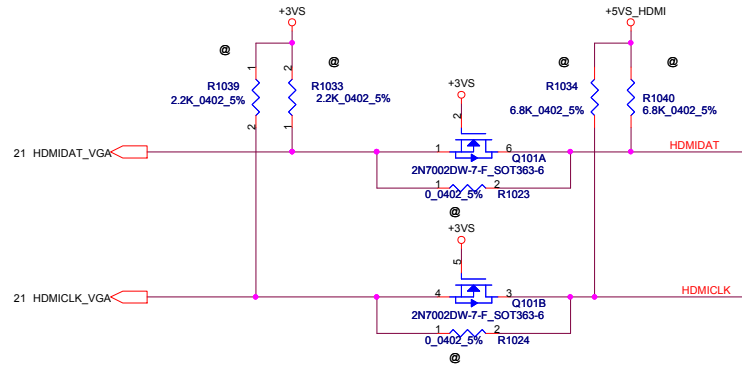
+1.5V to +1.5VS Transfer



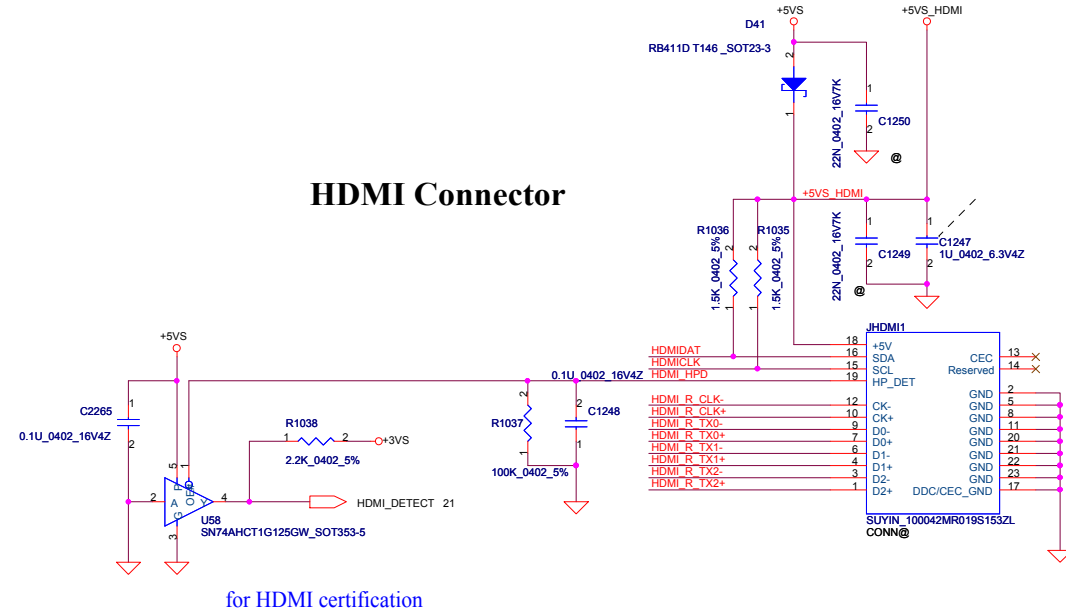
- | | | |
|-----|---|---|
| T73 | ● | × |
| T76 | ● | × |
| T79 | ● | × |
| T81 | ● | × |
| T83 | ● | × |
| T85 | ● | × |
| T87 | ● | × |
| T89 | ● | × |
- | | | |
|-----|---|---|
| T74 | ● | × |
| T77 | ● | × |
| T80 | ● | × |
| T82 | ● | × |
| T84 | ● | × |
| T86 | ● | × |
| T88 | ● | × |
| T90 | ● | × |
- | | | |
|-----|---|---|
| T75 | ● | × |
| T78 | ● | × |

Discharge circuit

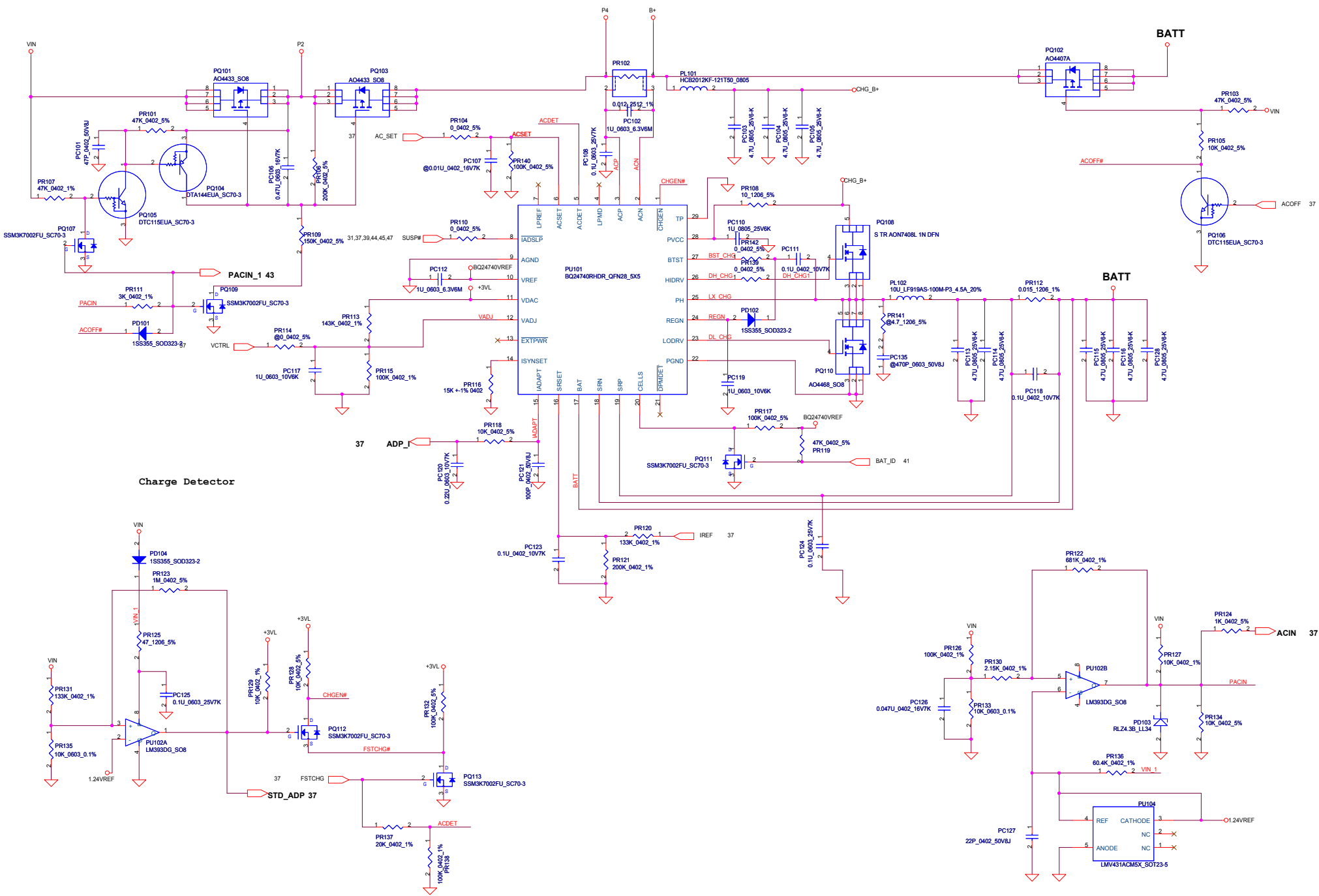


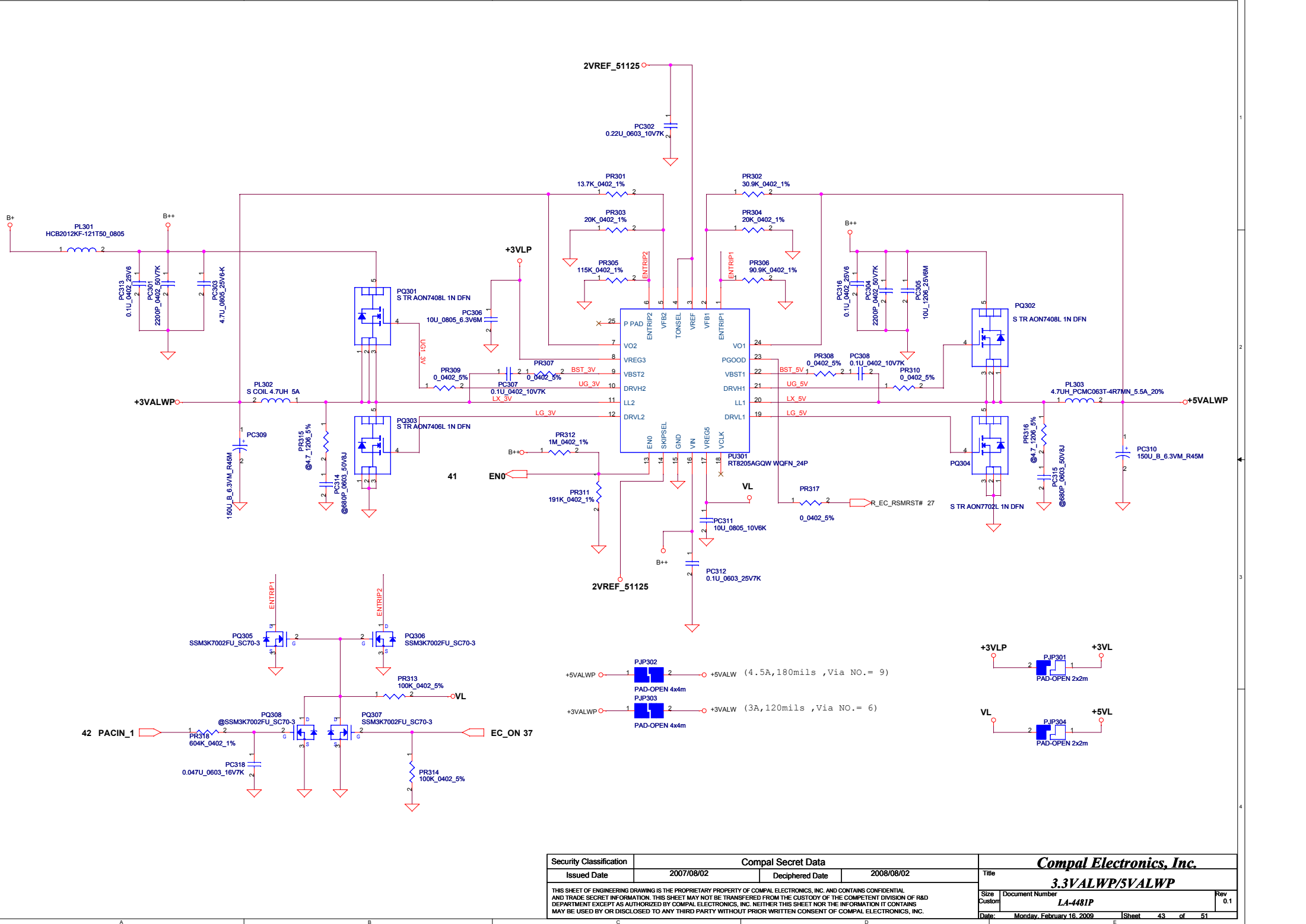


HDMI Connector

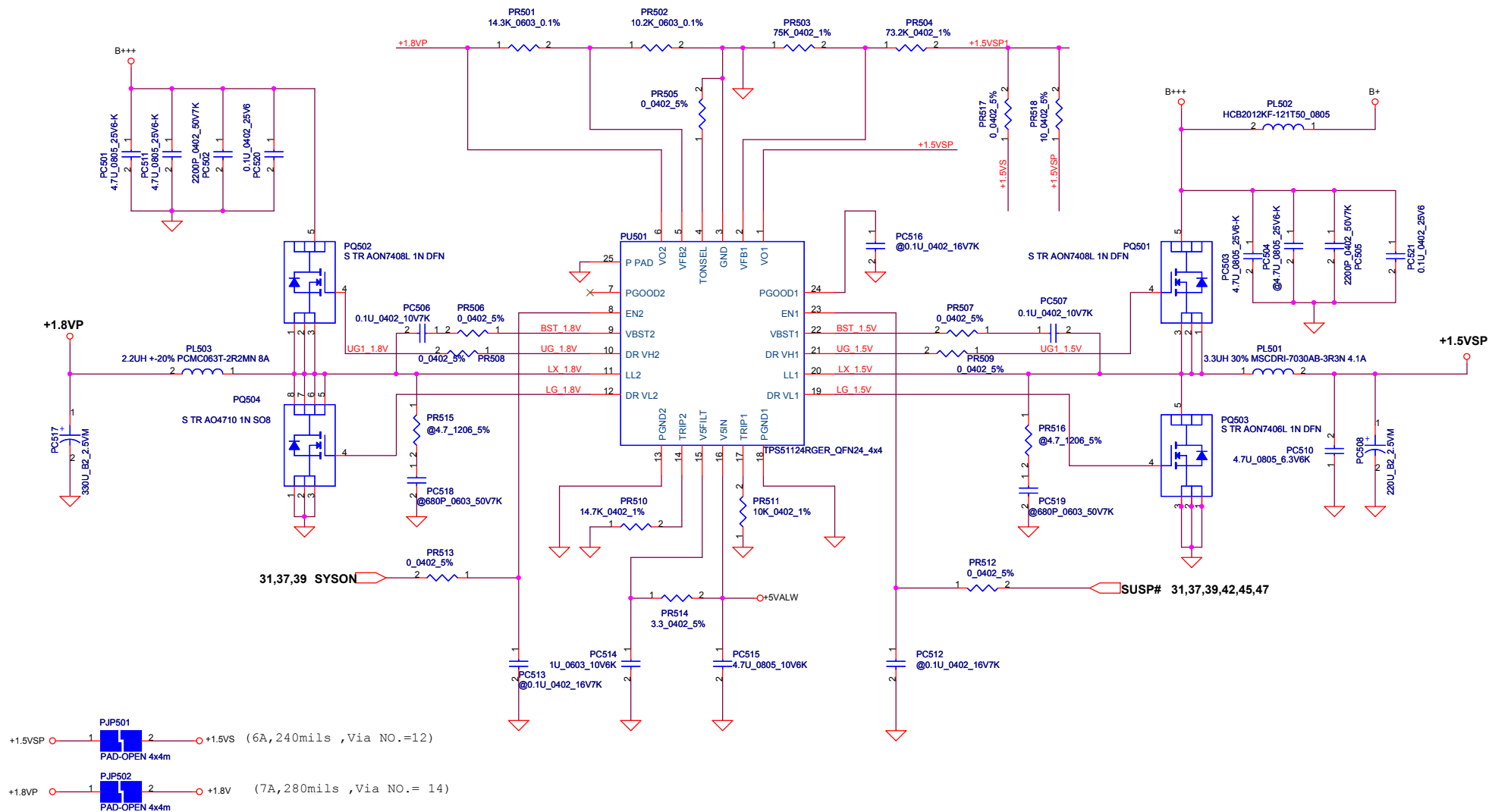


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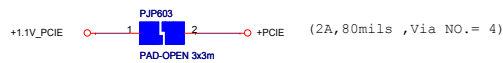
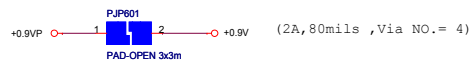
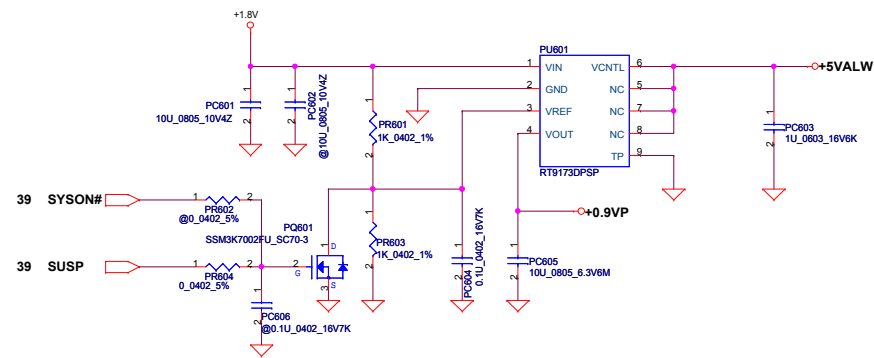




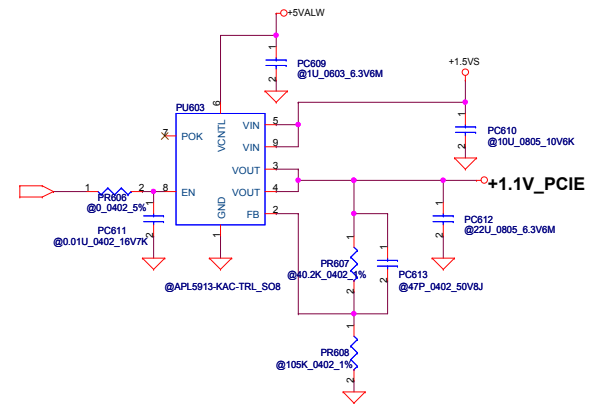
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		3.3VALWP/5VALWP	
2007/08/02		2008/08/02		LA-4481P	
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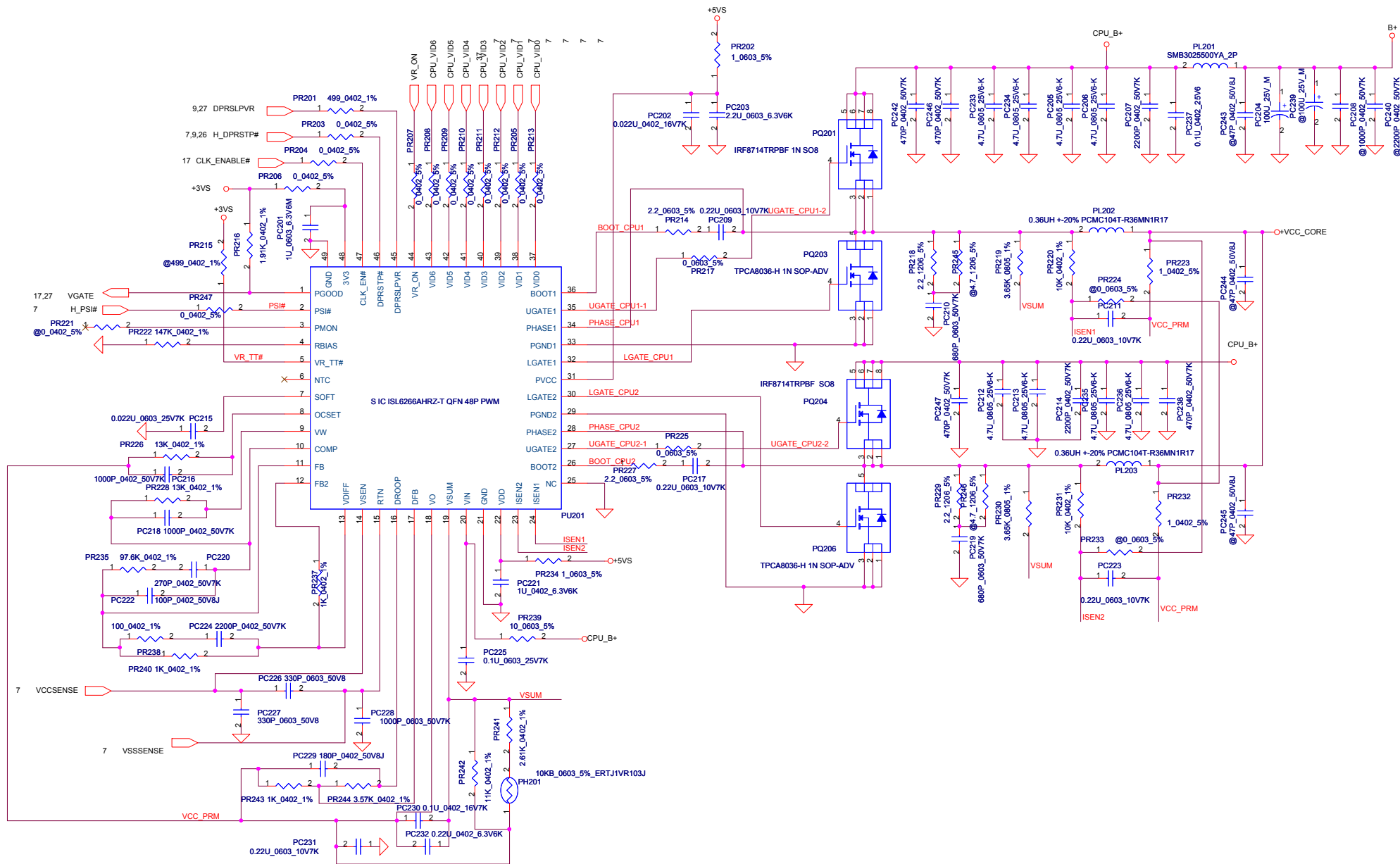
Security Classification		Compal Secret Data		Title	
Issued Date	2007/05/29	Deciphered Date	2008/05/29	1.5VSP/1.8VP	
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31,37,39,42,44,47 SUSP#



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Issued Date	2006/11/23	Deciphered Date	2007/11/23	Title	0.9VP/1.1V PCIE	
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					LA-4102P Blade discrete	0.1
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Compal Electronics, Inc.			
Title		+CPU_CORE	
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Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1							
2							
3							
4							

Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Power Changed-List History-1			
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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	CardReader clock issue	17	Using USB_0 for CLK_48M_CR	2008/10/08	SI-1
2	Debug Card issue	31	Connect PLT_RST# to JP7.A17	2008/10/08	SI-1
3	delete VGA external thermal sensor layout location for layout space limitation	29	Del U6,C348,C350	2008/10/08	SI-1
4	Add Audio board	34	Add JAUDIO connector for audio board	2008/10/08	SI-1
5	delete VGA JTAG for layou space limitation	29	Delete T47,T48,T49,T50,T51	2008/10/08	SI-1
6	Cap board issue	38	Change Cap board power rail to +3VL	2008/10/08	SI-1
7	Change JFPR to 6 pin connector	35	change JFPR	2008/10/08	SI-1
8	Change FAN control circuit to voltage control	6	Add U51,D17,R50,C41	2008/10/08	SI-1
9	Delete HDA SSC	26	Remove U44 for layout spacing	2008/10/08	SI-1
10	For PR mini card connector	31	Add R2252 -- R2261	2008/10/08	SI-1
11	PA/PR CardReader LED	32	D72 for PA, D71 for PR	2008/10/08	SI-1
12	EMI request	33	Change R2205 to L76	2008/10/08	SI-1
13	change MIC to 2pin and add SPK connector	34		2008/10/08	SI-1
14	Speaker L & R reverse	34		2008/11/20	SI-2
15	JFPR change to 4 pin	40	Add U58,C2265	2008/11/20	SI-2
16	add buffer on detect pin for certification item 7-12	34		2008/11/20	SI-2
17	Bom Error [Bug: BT led fail]	38	Change D20's Part number to SCA00000G00	2008/12/10	PV
18	Realtek suggest us to change Cap value	30	Change C2193 value from 0.1uF to 1uF	2008/12/10	PV
19	Slove WWLAN Noise : Add Cap X4 [to GND]	26	C499 and C2130 default mount, Add C2266 and C2267 [12 PF]	2008/12/10	PV
20	Slove WWLAN Noise:Add Cap,change R191val	37	Add C2268 [22PF] on R191.2 to GND and R191 change to 47 ohm	2008/12/10	PV
21	Slove WWLAN Noise:C356,C357 default mou	21	C356 and C357 default mount	2008/12/10	PV
22	Slove SMT issue	37	Change U30 FOOTPRINT [fromKB926QFA1_LQFP128_14X14 change to ECE5028-NU_VTQFP128_14X14]		PV
23	Slove SMT issue	37	Change JKB FOOTPRINT [from ACES_85202-24051_24P change to ACES_85202-24051_24P-S]	2008/12/10	PV
24	Slove ESD issue	26	ADD C2269 [0.1uF] on BATT1.1 trace (pin 1)	2008/12/17	PV
25	Slove ESD issue	33	Add one Diode [D73] on MIC_EXTR, MIC_EXTL (near chip side)	2008/12/17	PV
26	Slove ESD issue	33	Change cap value [C2270,C2271,C2272,C2273] to 0.1uF	2008/12/17	PV
27	Slove Audio issue	34	Change cap value to 2.2uF [C2239,C2240]	2008/12/17	PV
28	Slove non-RoHS Part	30	Change C2157,C2160,C2215 and C2217 Part number [from SE070104Z00 to SE070104Z80]	2008/12/17	PV

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				HW PIR				
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