

Compal confidential

Schematics Document

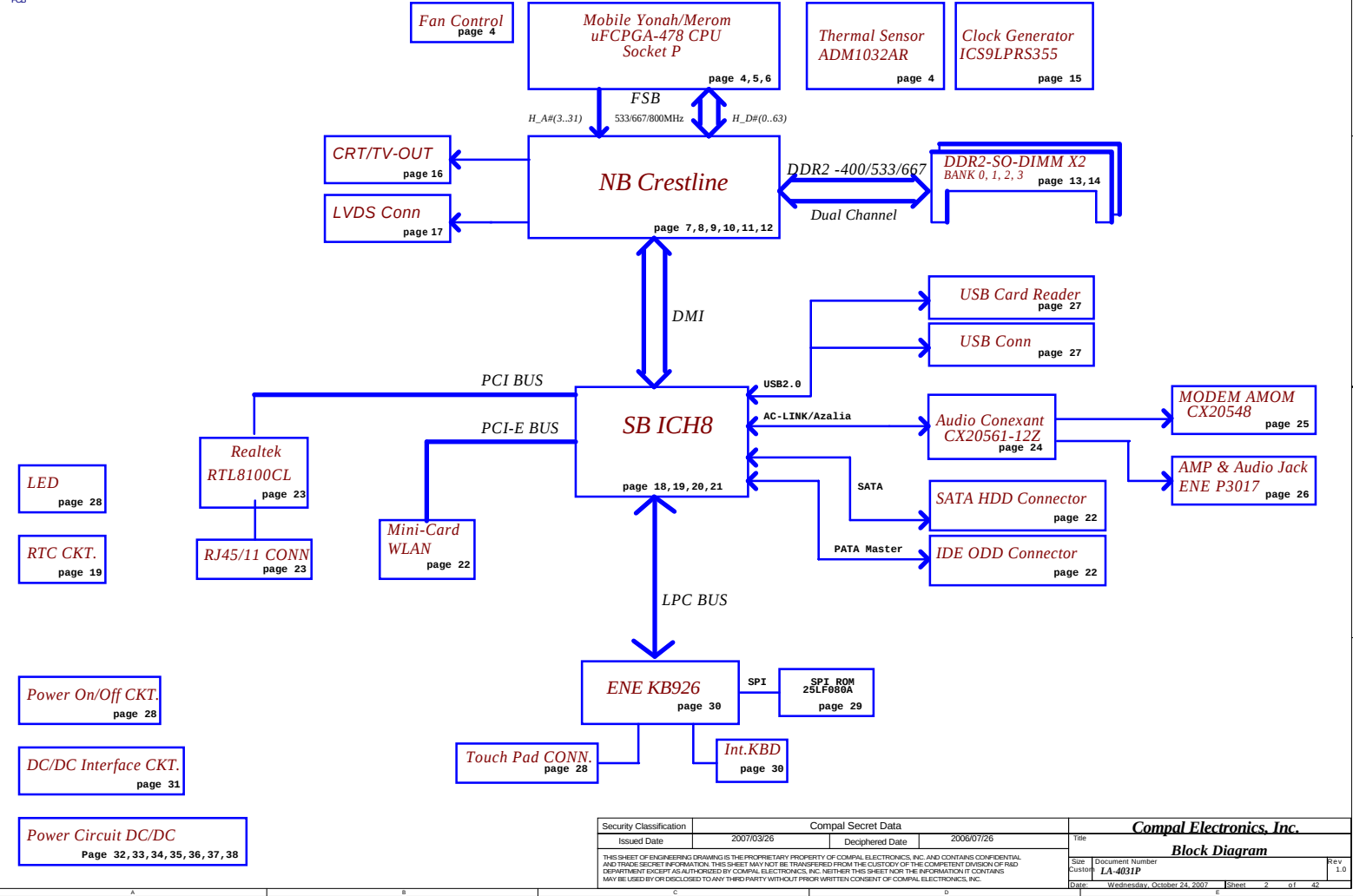
Mobile Merom uFCPGA with Satna Rosa Platform

2007-07-30
REV:0.2

Security Classification	Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/07/26	
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			Cover Sheet	
			Size	Document Number
			Custody	LA-4031P
			Date	Wednesday, October 24, 2007
			Sheet	1 of 42
			Rev	1.0



Spartan 1.1 (Merom +Crestline+ICH8)



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				Customer	LA-4031P
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Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD17	0	A

SMBUS Control Table

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

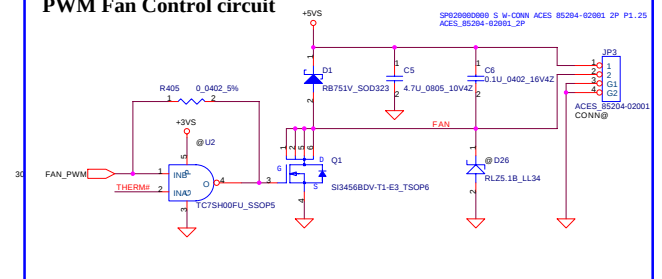
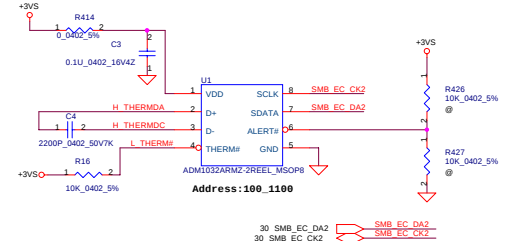
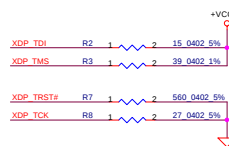
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADW1832	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

BOM: 43152432L03(965GM) & 43152432L04(960GML) with card reader

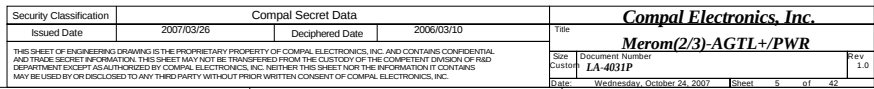
BOM: 43152432L01(965GM) & 43152432L02(960GML) without card reader

Jump-Short: PJP?

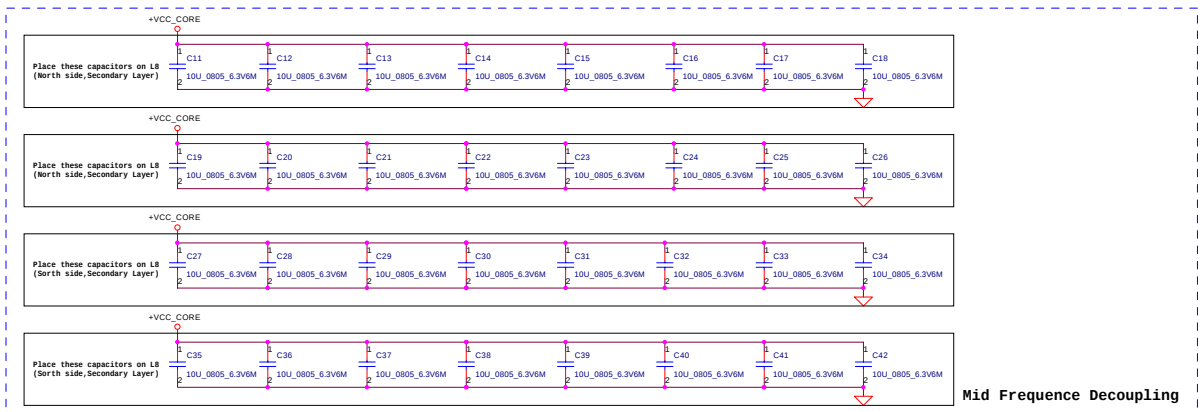
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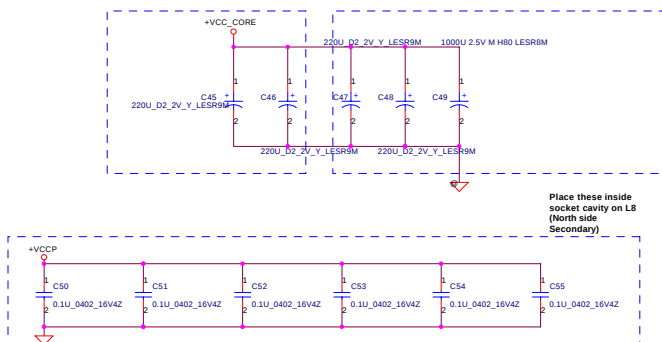


JP2D	
A4	VSS[001]
A6	VSS[002]
A11	VSS[003]
A14	VSS[004]
A16	VSS[005]
A18	VSS[006]
A22	VSS[007]
AE2	VSS[008]
B6	VSS[009]
B8	VSS[010]
B11	VSS[011]
B13	VSS[012]
B16	VSS[013]
B19	VSS[014]
B21	VSS[015]
B24	VSS[016]
C2	VSS[017]
C4	VSS[018]
C11	VSS[019]
C16	VSS[020]
C18	VSS[021]
C2	VSS[022]
C22	VSS[023]
C24	VSS[024]
D1	VSS[025]
D4	VSS[026]
D8	VSS[027]
D11	VSS[028]
D16	VSS[029]
D18	VSS[030]
D19	VSS[031]
D22	VSS[032]
D24	VSS[033]
E2	VSS[034]
E6	VSS[035]
E8	VSS[036]
E11	VSS[037]
E14	VSS[038]
E16	VSS[039]
E19	VSS[040]
E21	VSS[041]
E24	VSS[042]
F2	VSS[043]
F6	VSS[044]
F8	VSS[045]
F11	VSS[046]
F13	VSS[047]
F16	VSS[048]
F19	VSS[049]
F22	VSS[050]
F24	VSS[051]
G2	VSS[052]
G4	VSS[053]
G11	VSS[054]
G16	VSS[055]
G22	VSS[056]
H2	VSS[057]
H16	VSS[058]
H21	VSS[059]
H24	VSS[060]
I2	VSS[061]
J2	VSS[062]
J6	VSS[063]
K1	VSS[064]
K4	VSS[065]
K22	VSS[066]
K26	VSS[067]
L2	VSS[068]
L6	VSS[069]
L11	VSS[070]
L24	VSS[071]
M2	VSS[072]
M6	VSS[073]
M22	VSS[074]
M26	VSS[075]
N1	VSS[076]
N16	VSS[077]
N21	VSS[078]
N24	VSS[079]
N26	VSS[080]
P1	VSS[081]
Merom Ball-out Rev 1a	
CONN	

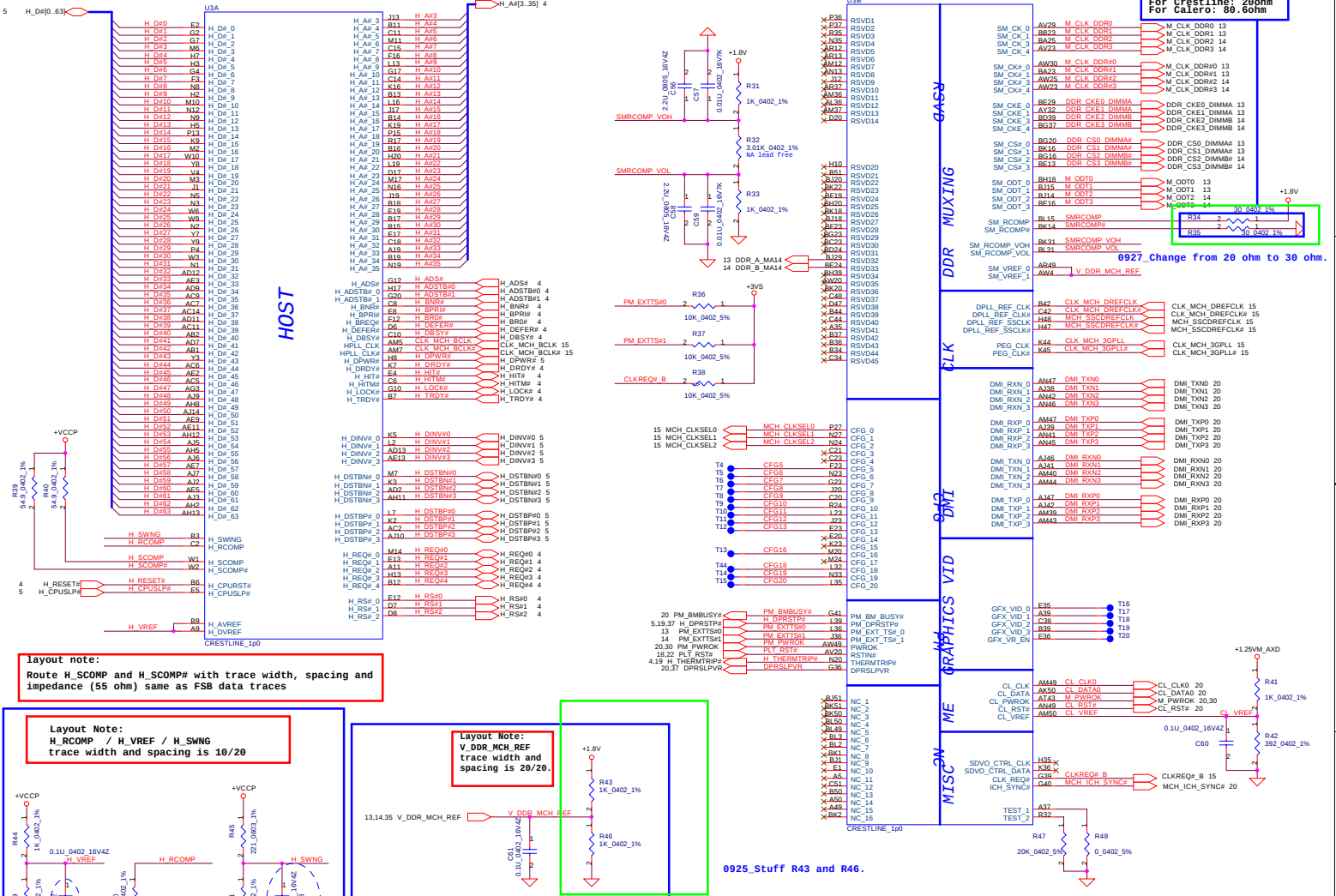


Near CPU CORE regulator

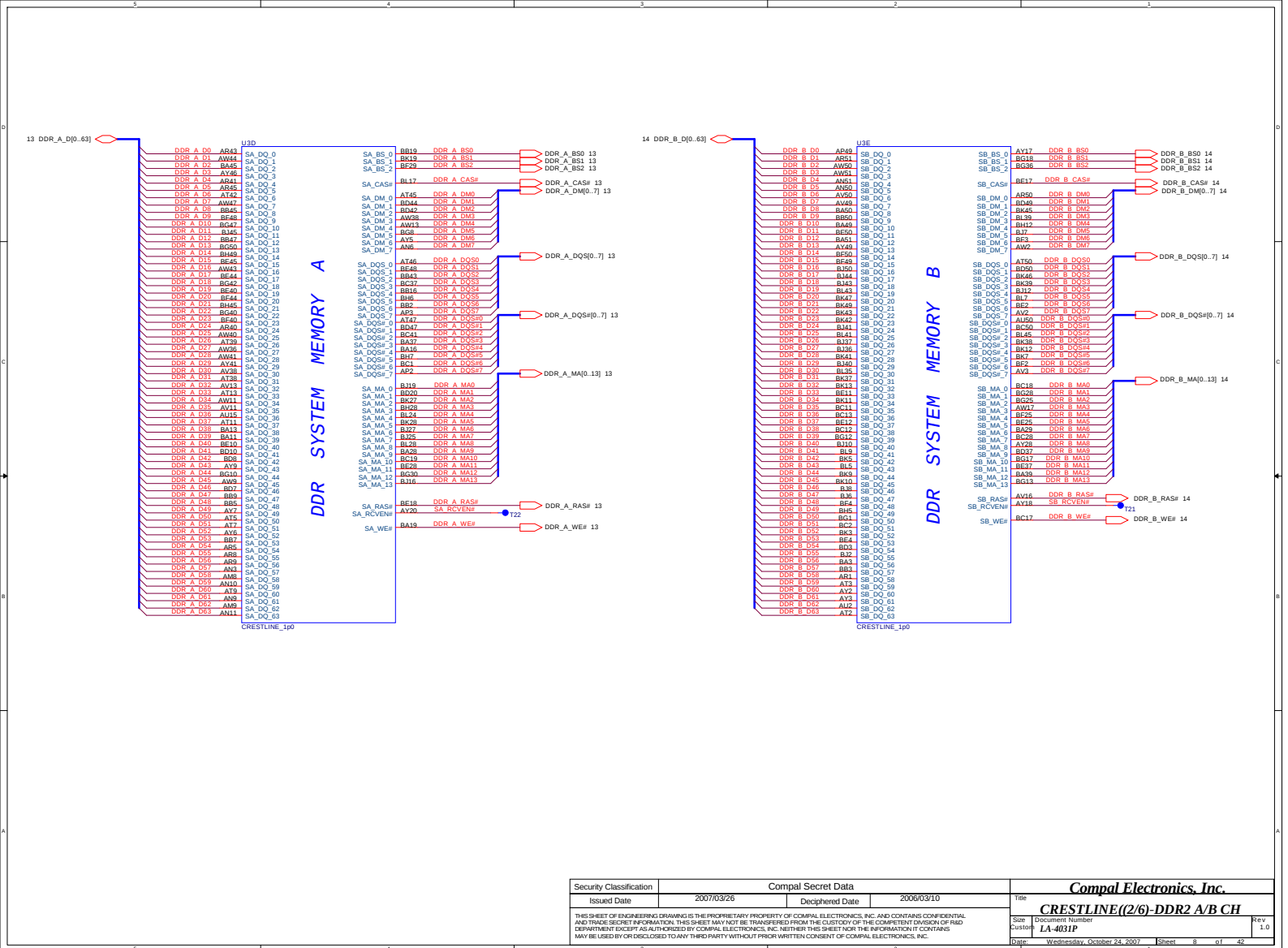
ESR <= 1.5m ohm
Capacitor > 1980uF

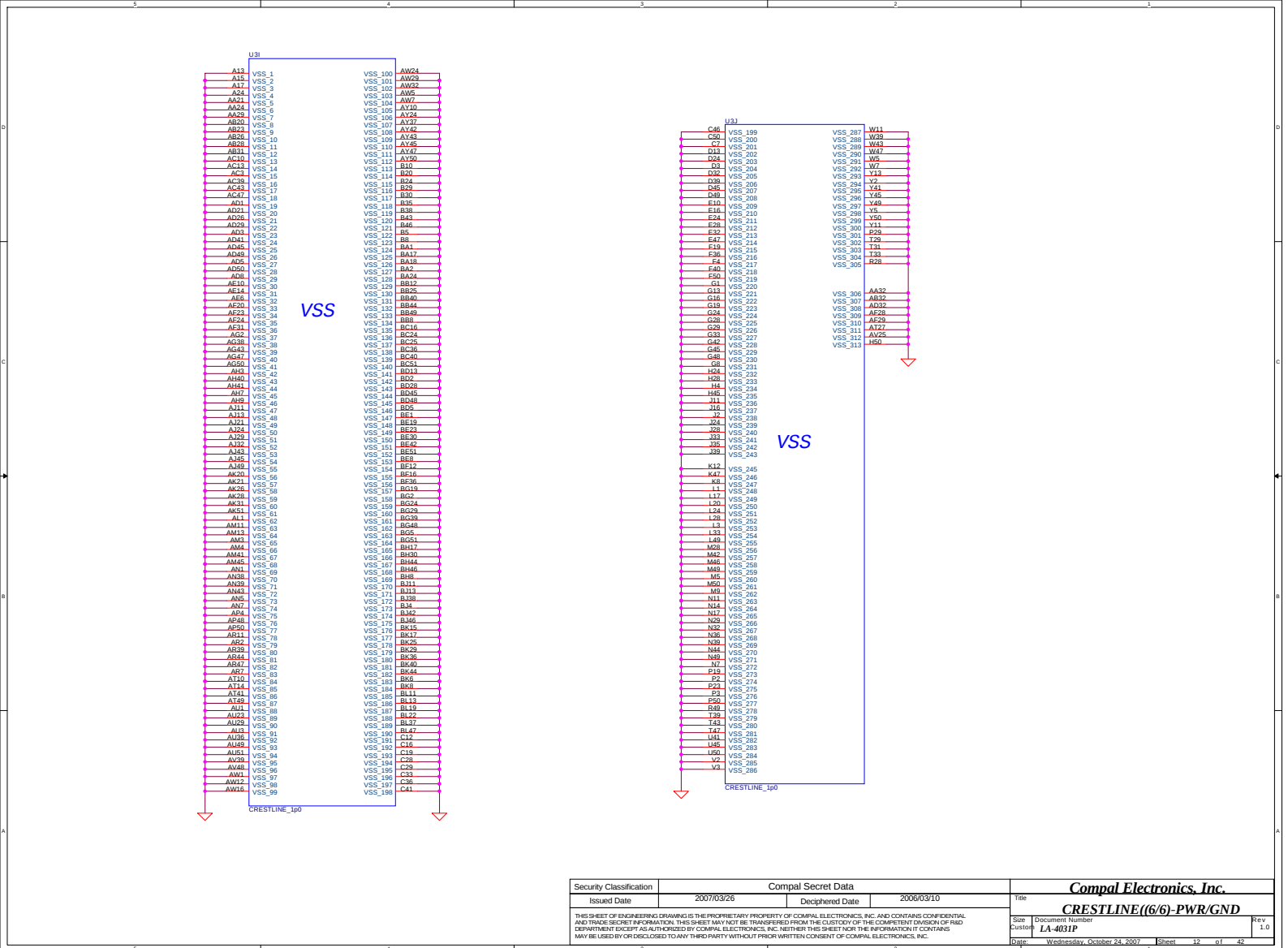


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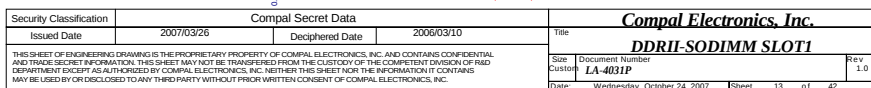


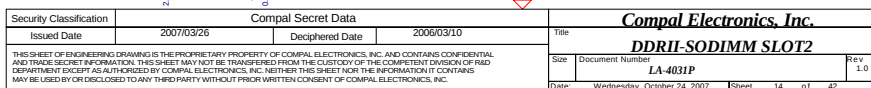
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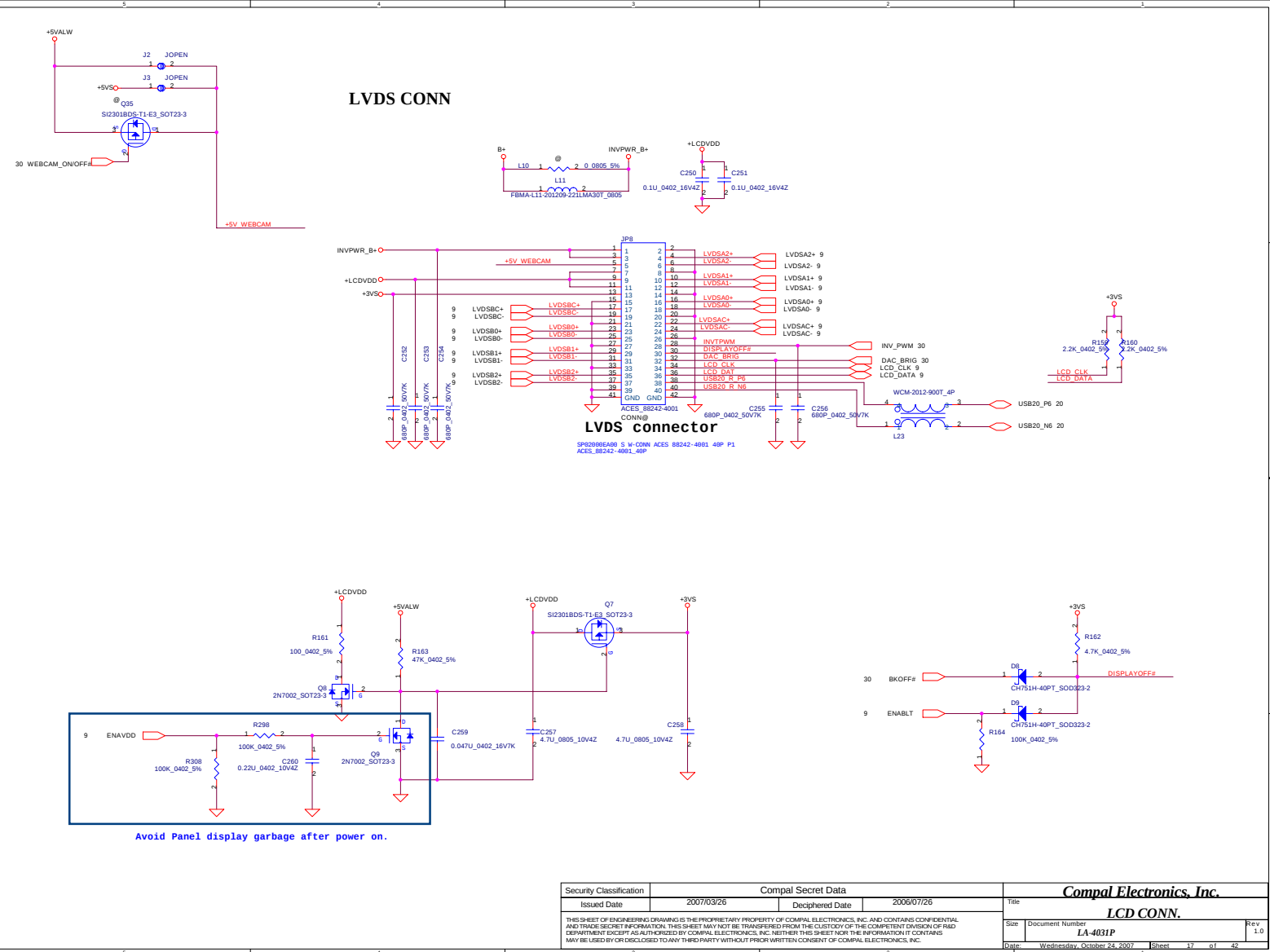
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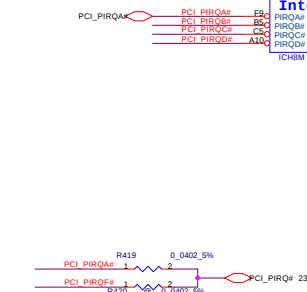
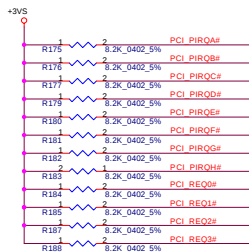


```
For ITP_EN, 0 =SRC8/SRC#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable D0T96 & SRC1,
            1= Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
            1 = Overclocking of CPU and SRC NOT allowed
```





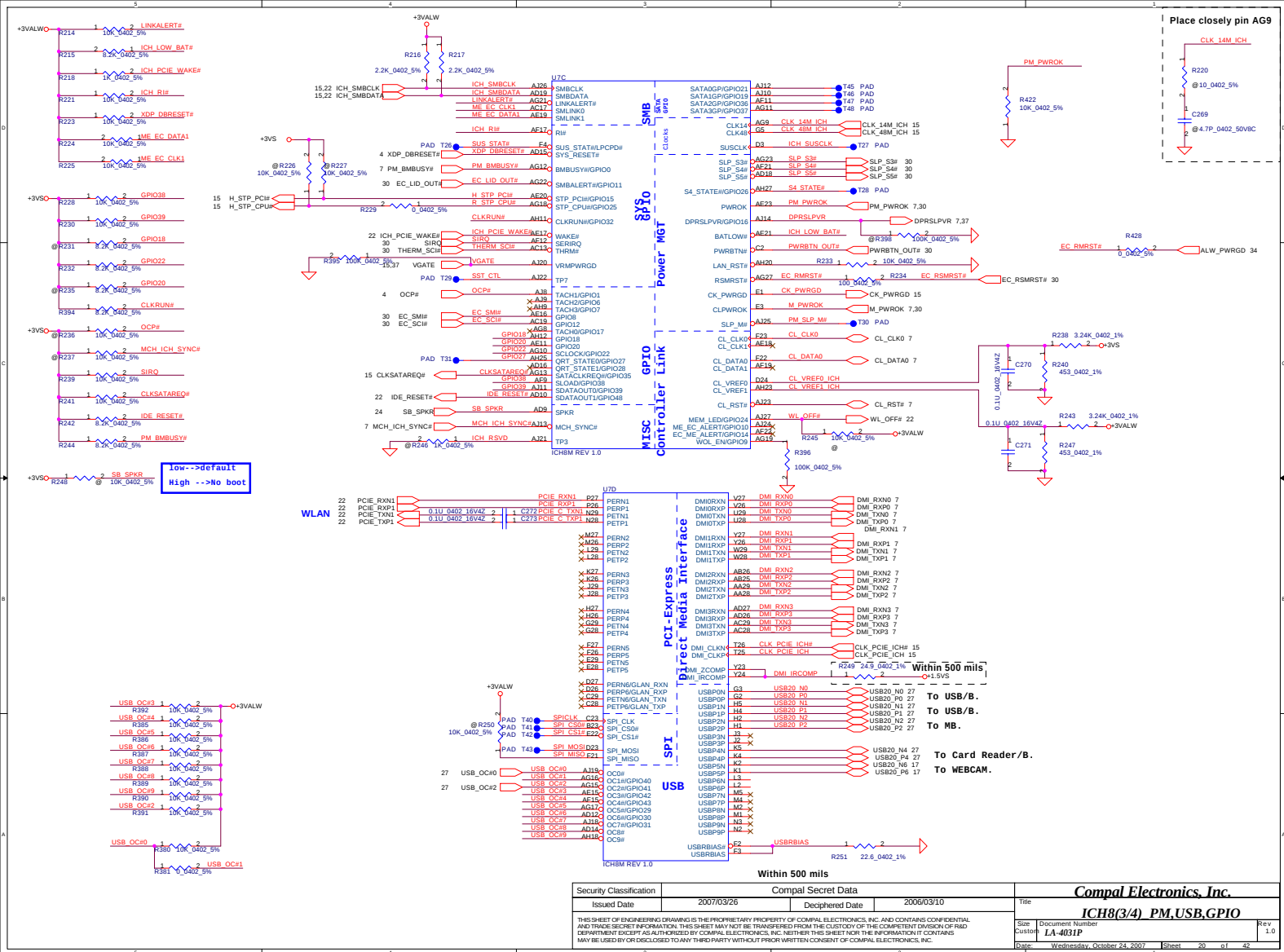
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Size		Document Number		LA-403P	
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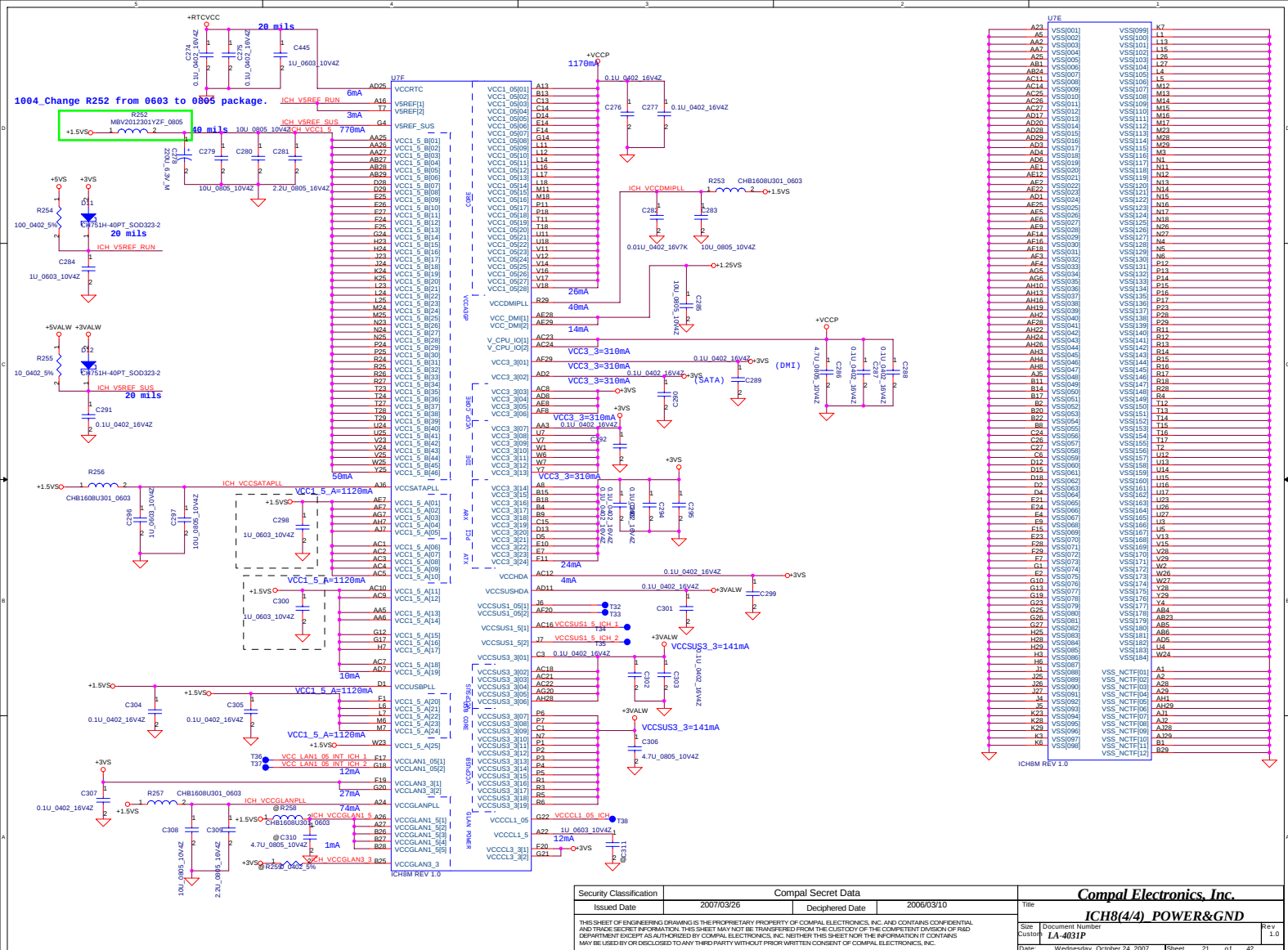


A16 swap override Strap	
PCI_GNT3#	*Low= A16 swap override Enable High= Default

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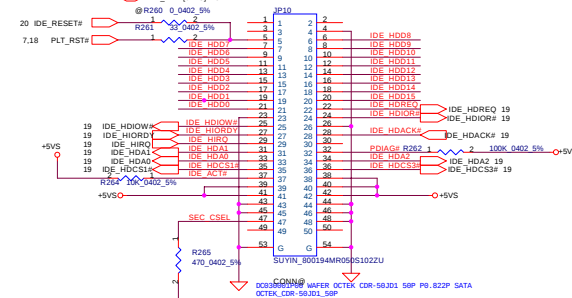
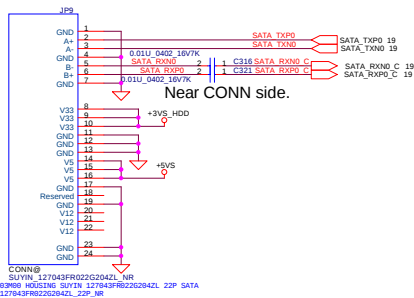
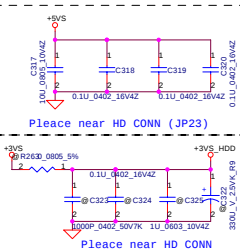


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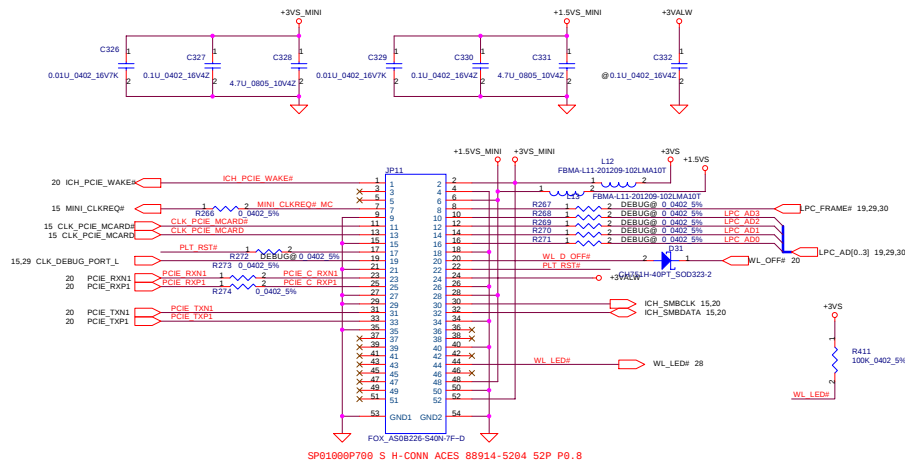
HDD Connector

CD-ROM Connector

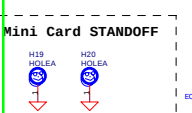
Place caps. near ODD CONN.



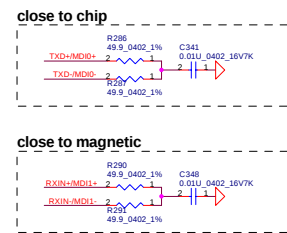
Mini-Express Card---WLAN



7/13 Update HX footprint



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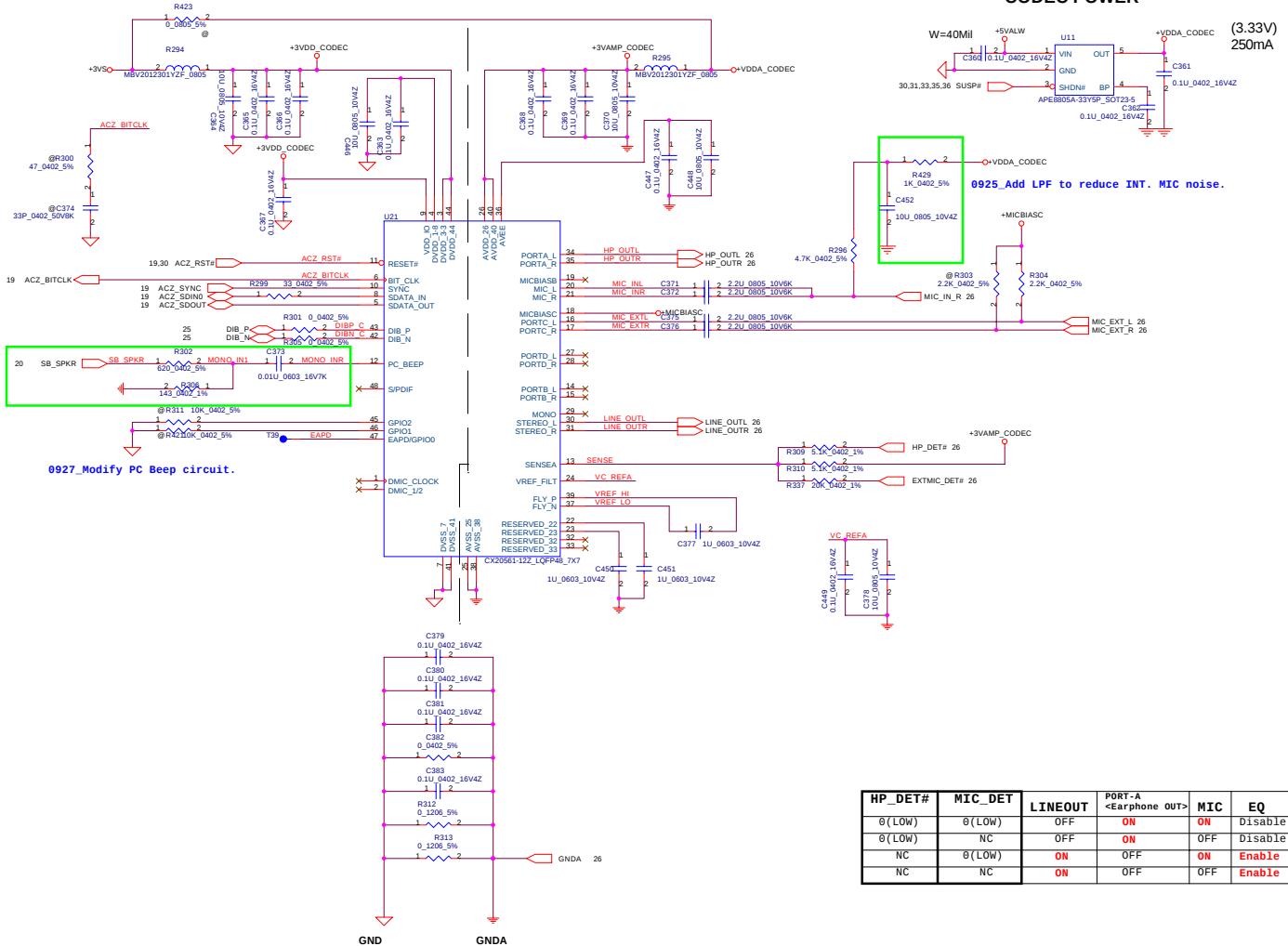
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In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

AUDIO CODEC

For Layout:
Place decoupling caps near the power pins of SmartAMC device.

CODEC POWER



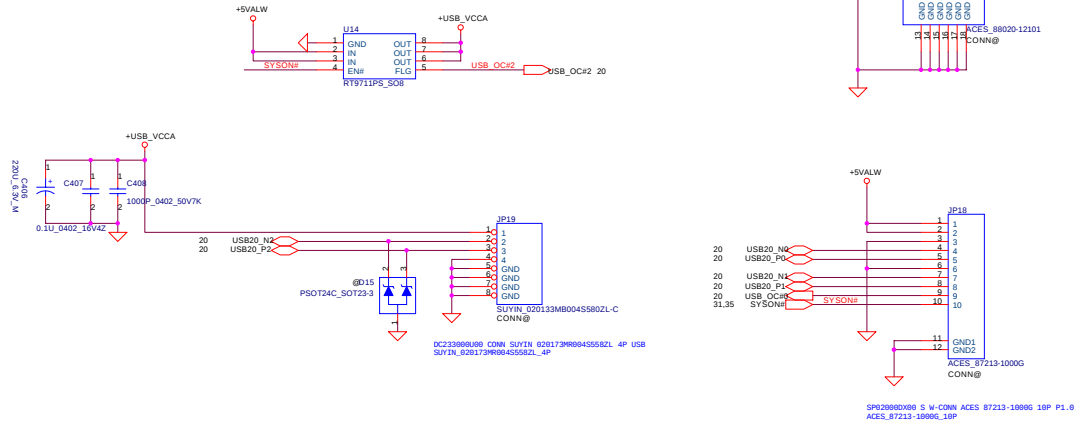
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REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -009. Updated footprints and corrected via spacing errors.	August 31, 2005
2	Changed MCB and M9S pads. No schematic changes. PCB updated to -005.	November 1, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 18, 2005
4	Added MR13 and PCB updated to -009.	January 1, 2006
4.01	AVL update only.	April 20, 2006

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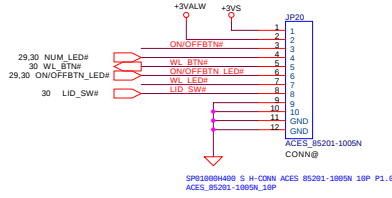
USB Port



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1015_Remove U22 and U23.

M/BtoS/B



POWER LED(Left 1)

BLUE



Battery Charge LED(Left 2)

BLUE

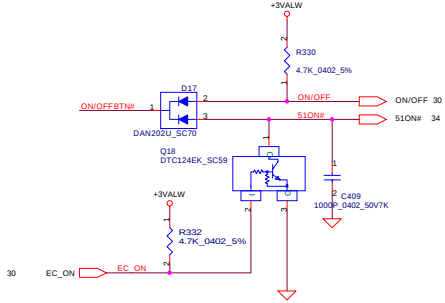


HDD LED(Left 3)

BLUE

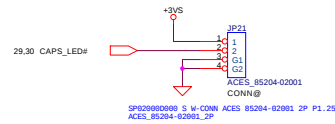


Power ON/OFF

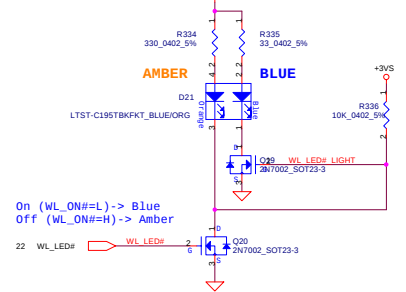


0426_Change all LED power source from 5V to 3V.

M/B to SB(Caps Lock LED)

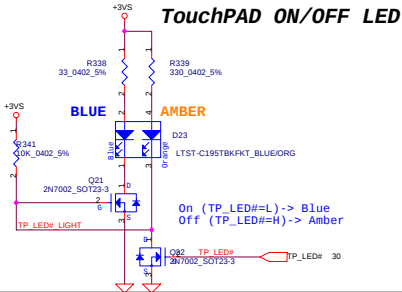


Wireless ON/OFF LED(Left 4)

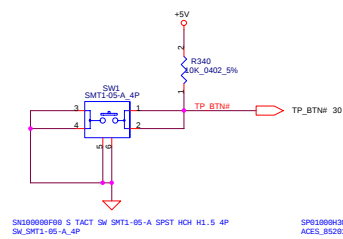


D21, D25, D23 Footprint can not match part number.

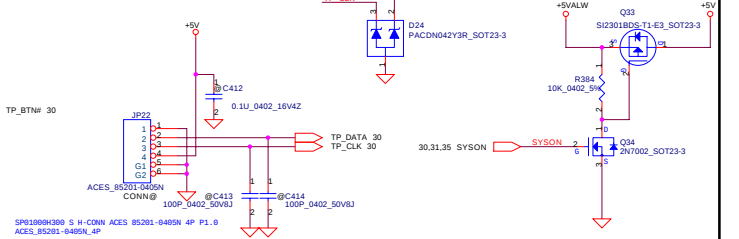
TouchPAD ON/OFF LED



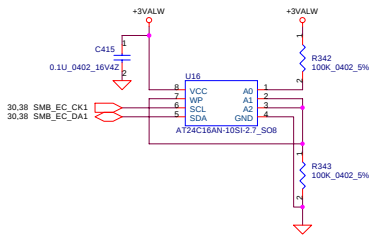
TP ON/OFF



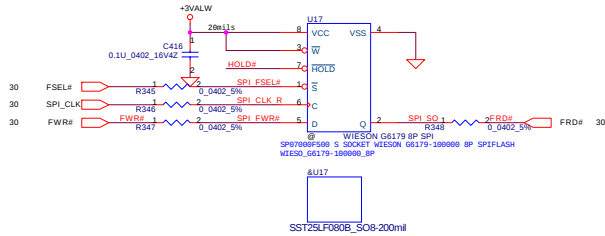
T/P Board



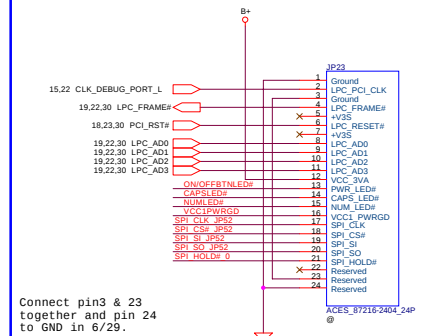
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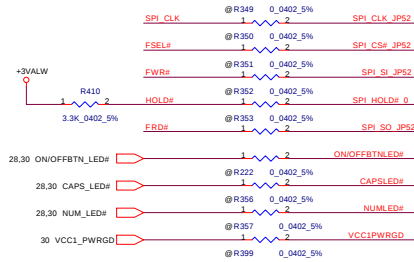
SPI ROM



LPC Debug Port

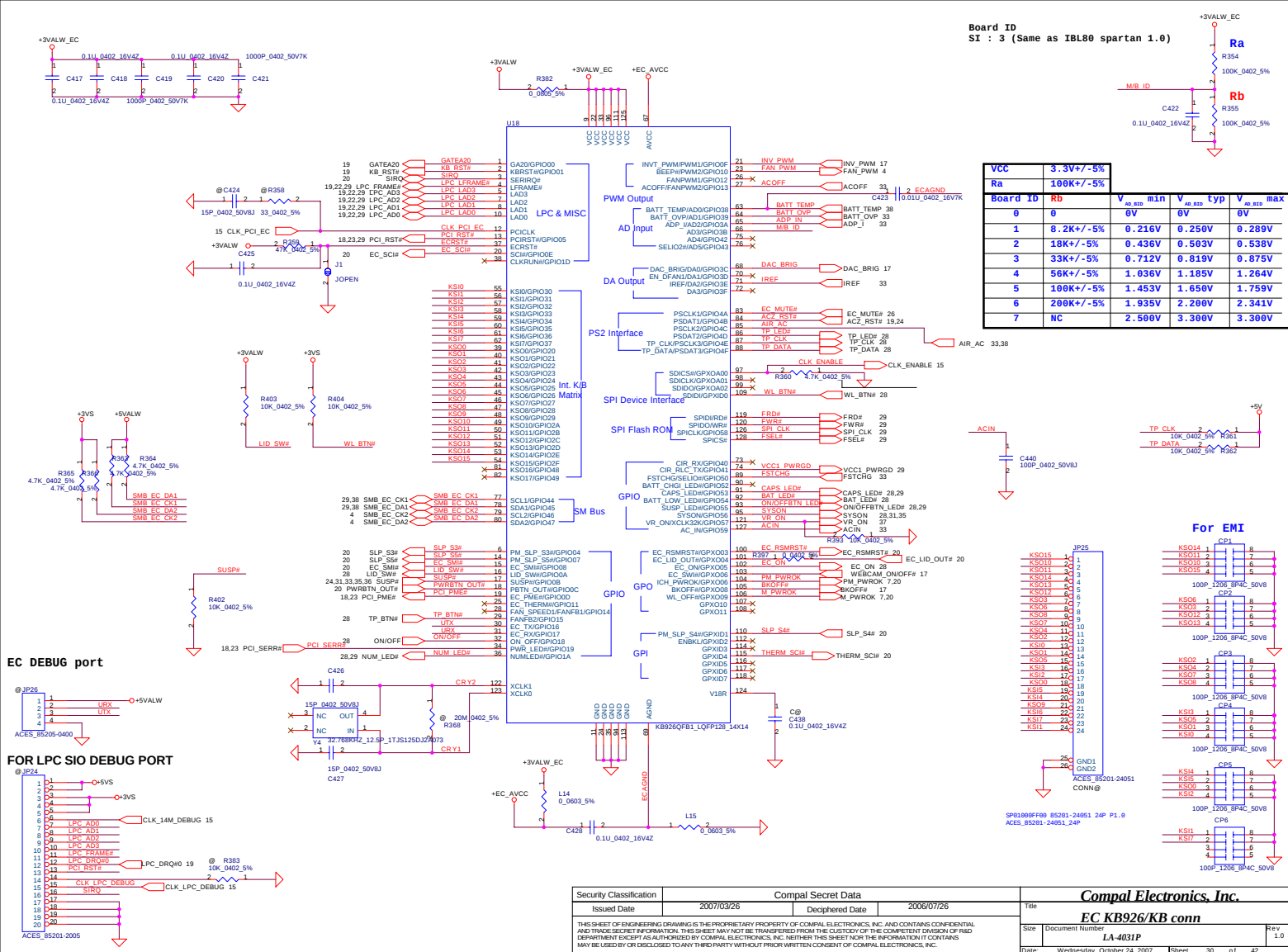


Connect pin3 & 23
together and pin 24
to GND in 6/29.

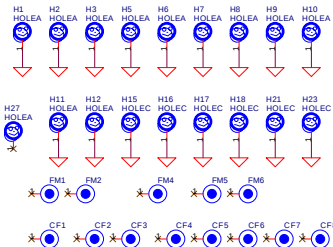
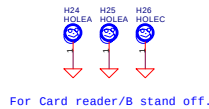
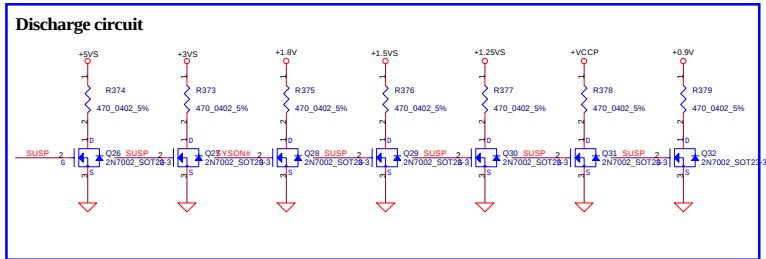
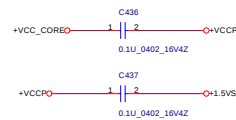
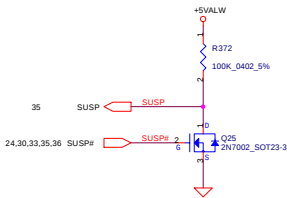
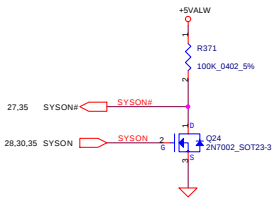
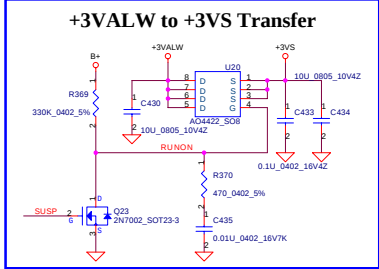
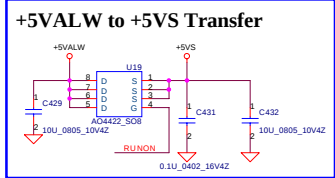


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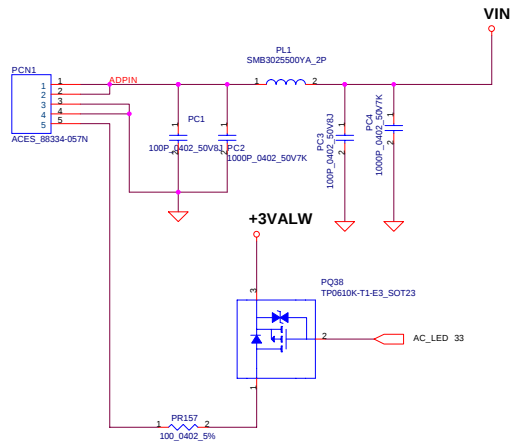
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				LA-4031P	1.0
				Date: Wednesday, October 24, 2007	Sheet 30 of 42

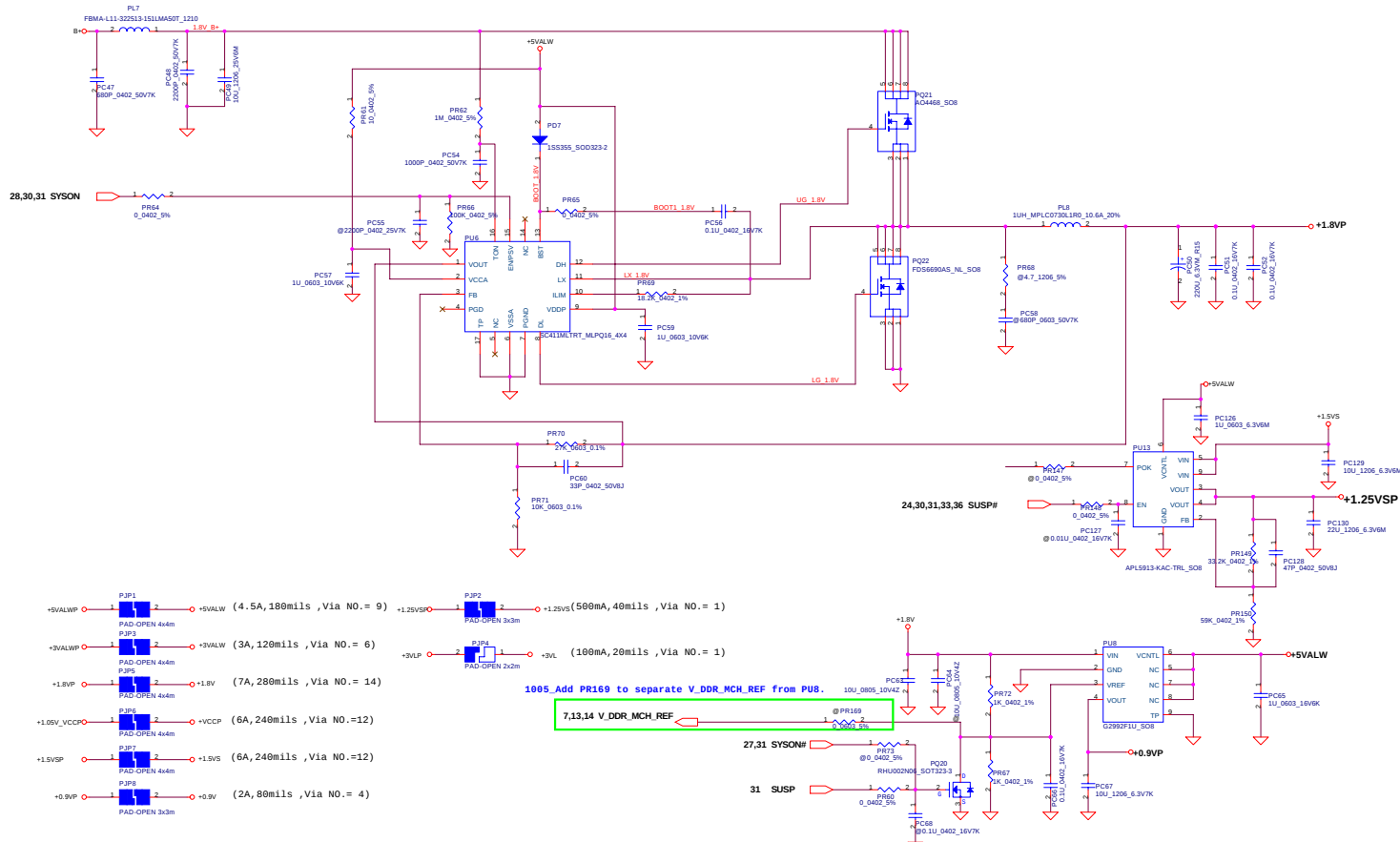


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Date: Wednesday, October 24, 2007				Sheet 38 of 42

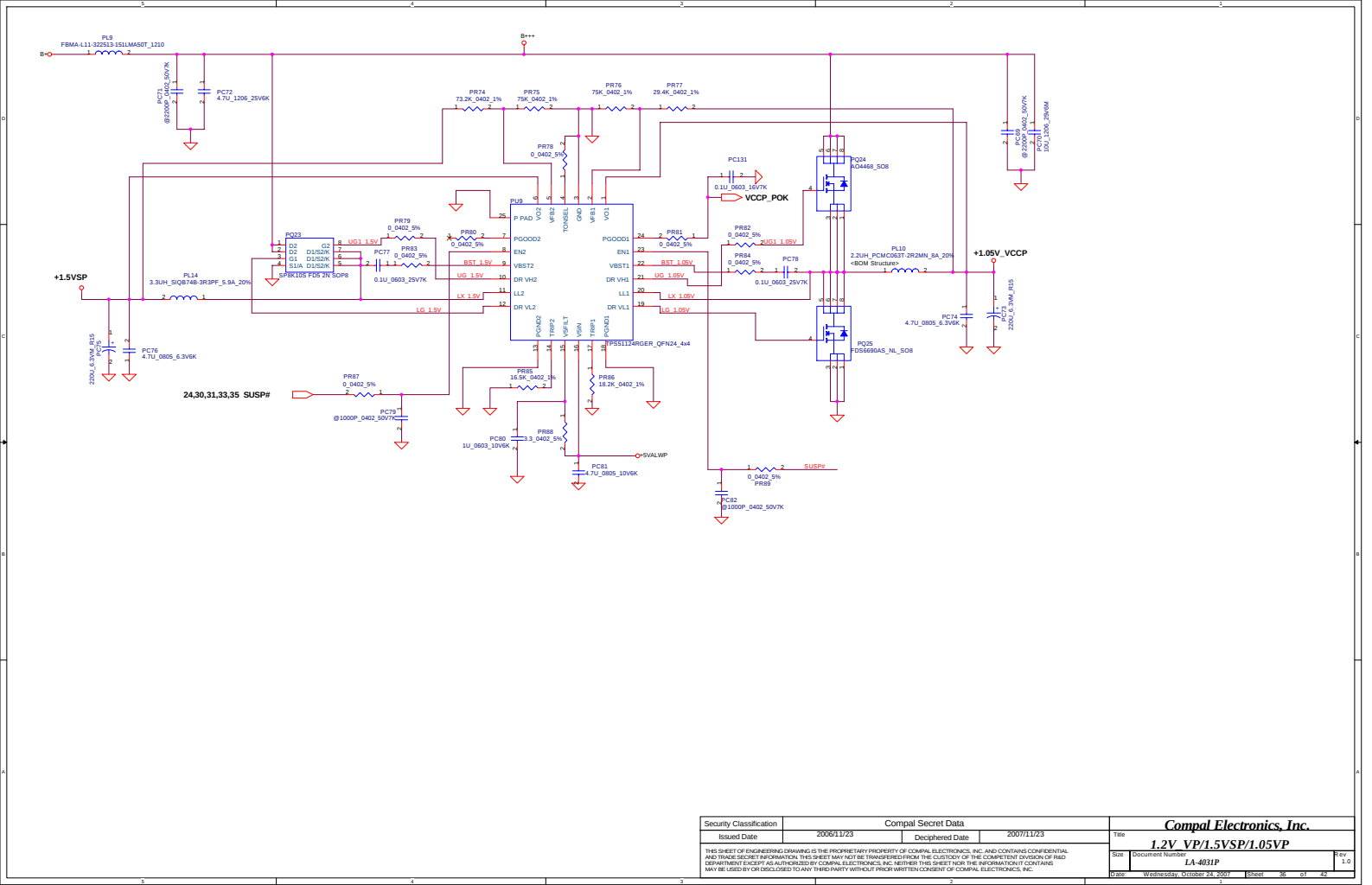


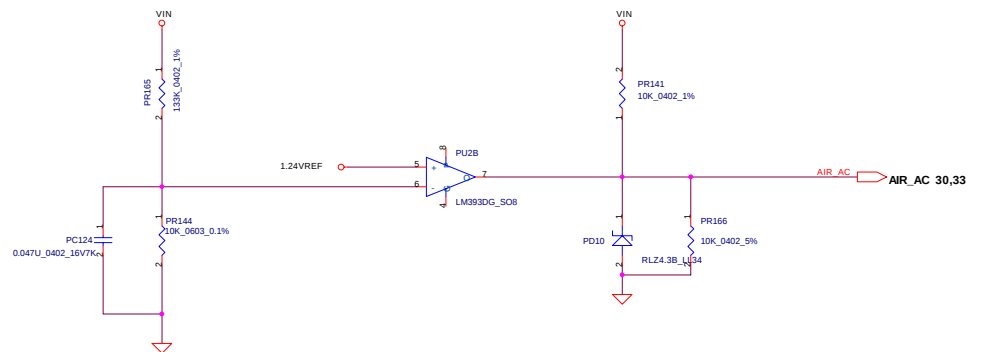
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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					

Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page		Date	Phase
1	Change R296 2.2K to 4.7K and Reserved R303	24	Follow conexant new design rule	8/6	SI-->PV
2	Add R424 R425 100ohm on MIC_EXT_R and MIC_EXT_L	26	Follow conexant new design rule	8/6	SI-->PV
3	Fine tune R298 C260 value	17	Reduce surge current on power on	8/6	SI-->PV
4	Change PIRQ from F to A	18	Choose R419 then control PIRQ A	8/14	SI-->PV
5	Connect PCI_SERR# to EC GPIO pin.	18	Connect PCI_SERR# to EC GPIO pin.	8/31	SI-->PV
6	Modify PC BEEP circuit.	20	Modify PC BEEP circuit.	8/31	SI-->PV
7	For support Intel Penryn CPU.	04	Reserve R426 and R427 for support Intel Penryn CPU.	9/3	SI-->PV
8	For ESD request.	28	Add U22 and U23 for ESD request.	9/3	SI-->PV
9	For EMI request.	26	Add L24-L27	9/5	SI-->PV
10	Change C391, C393, C395, C396 from 0.47uF to 0.047uF.	26	Change C391, C393, C395, C396 from 0.47uF to 0.047uF.	9/7	SI-->PV
11	Add R417 and R418 to fine-tune Vp-p.	26	Add R417 and R418 to fine-tune Vp-p.	9/7	SI-->PV
12	For ESD request.	20	Add U22 and U23 for ESD request.	9/7	SI-->PV
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Version Change List (P. I. R. List) for HW Circuit

[illegible]

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