

Compal confidential

Schematics Document

Mobile Merom uFCPGA with Satna Rosa Platform

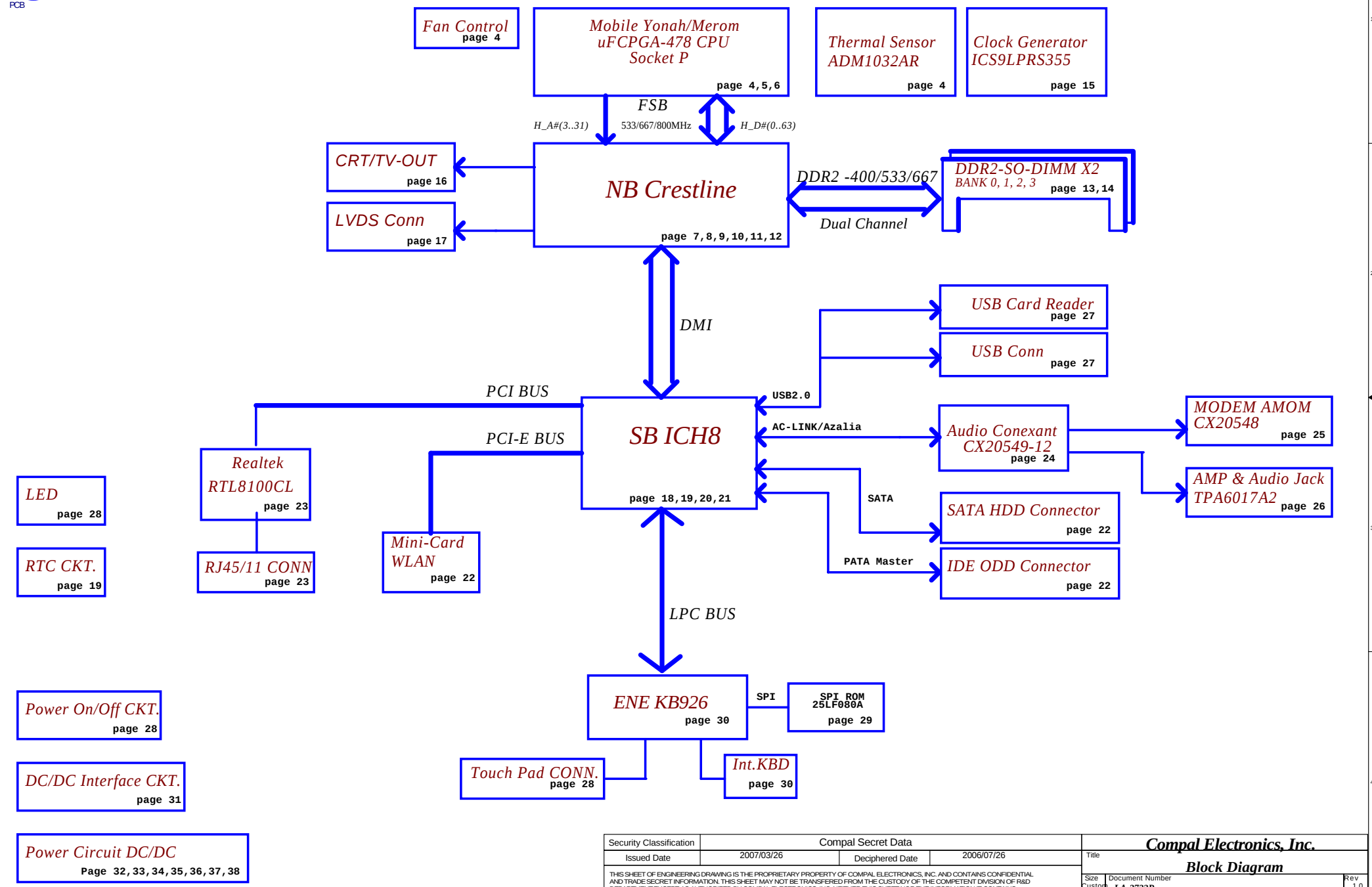
2007-05-29

REV:1.0

Security Classification		Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/07/26	Cover Sheet	
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Spartan 1.0 (Merom +Crestline+ICH8)

ZZZ1
PCB



Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD22	0	A

I2C / SMBUS ADDRESSING

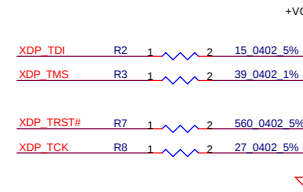
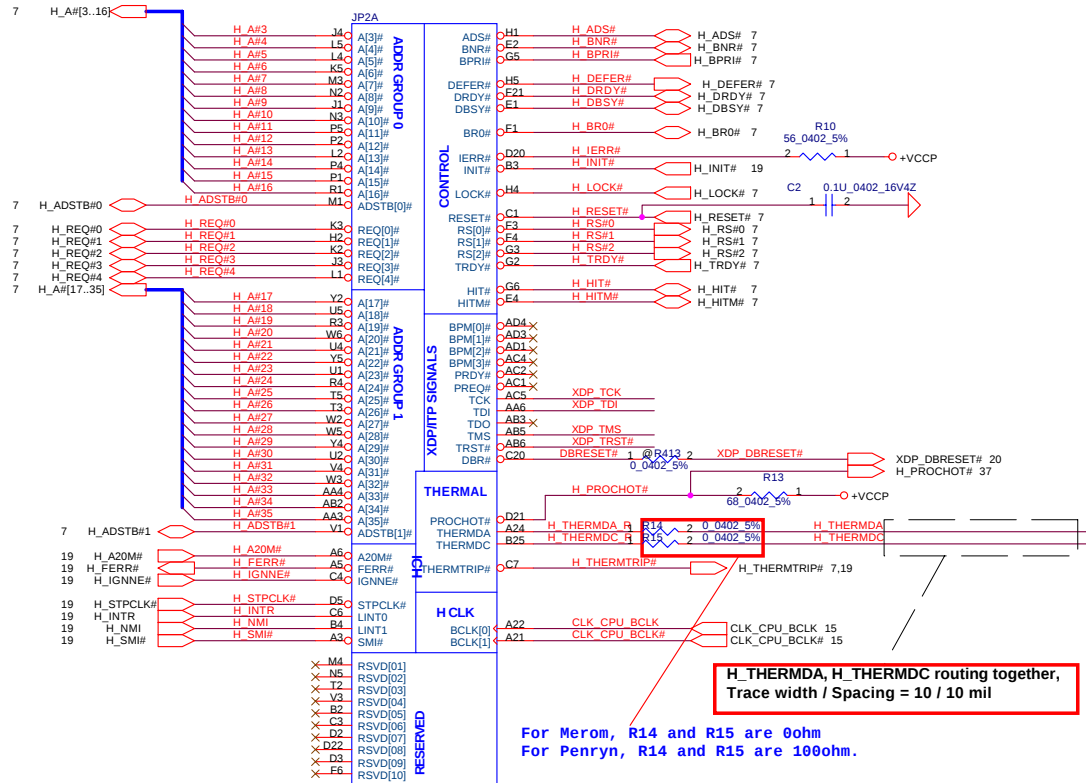
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

SMBUS Control Table

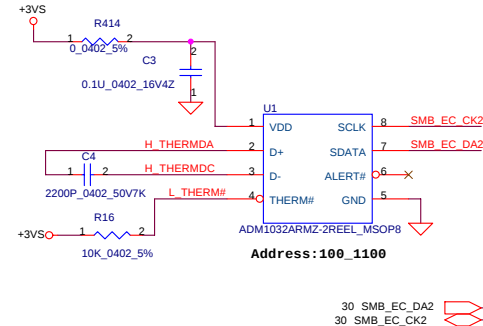
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

BOM: 43148632L01(965GM) & 43148632L02(960GML)

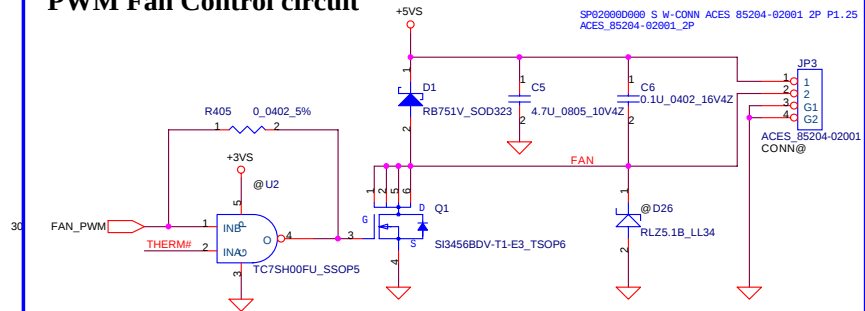
Jump-Short: PJP?



Thermal Sensor ADM1032ARMZ

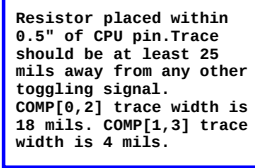


PWM Fan Control circuit

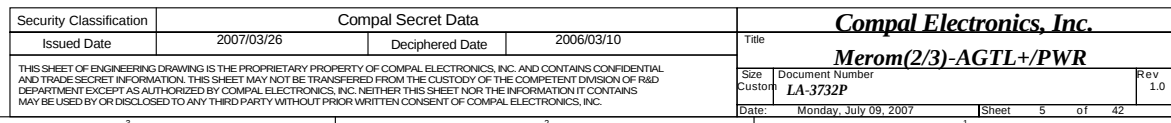
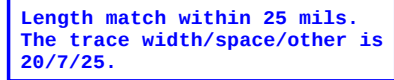


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						Merom(1/3)-AGTL+XDP	
						Size	Document Number
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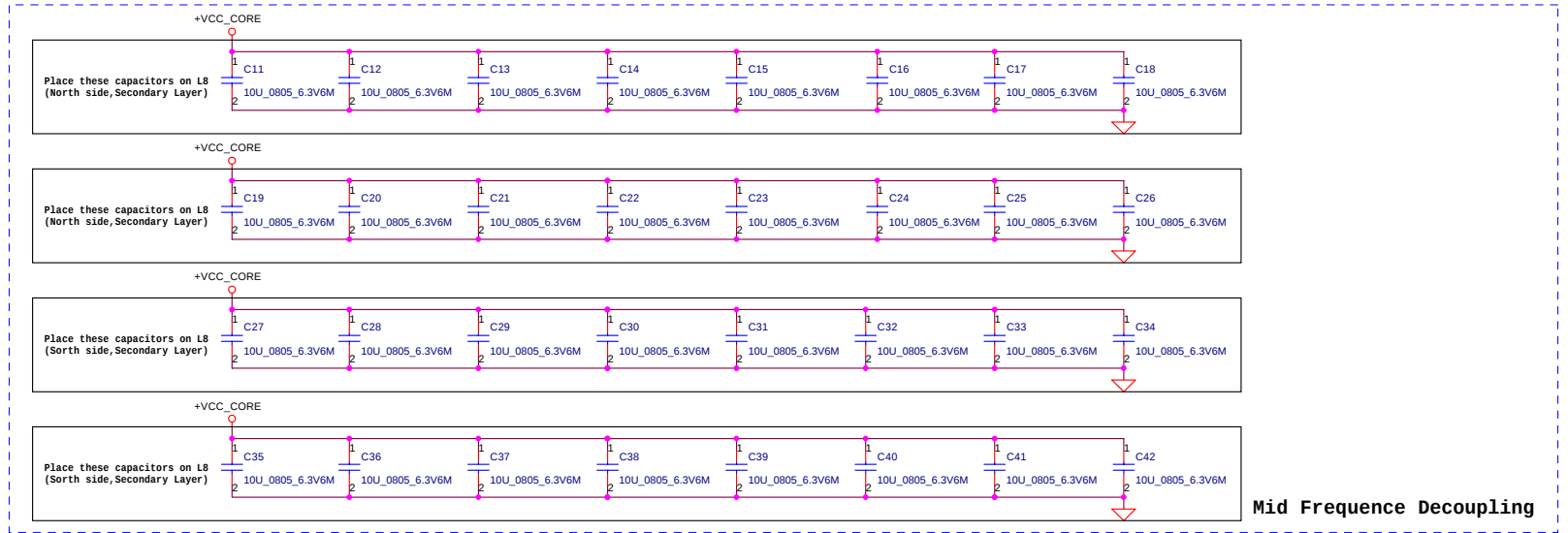


CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0



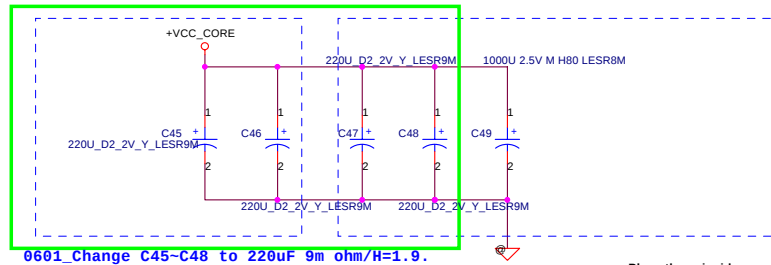
A4	JP2D	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	P25
A16	VSS[005]	P26
A19	VSS[006]	P27
A23	VSS[007]	P28
A27	VSS[008]	P29
B5	VSS[009]	P30
B8	VSS[010]	P31
B11	VSS[011]	P32
B12	VSS[012]	P33
B16	VSS[013]	P34
B19	VSS[014]	P35
B21	VSS[015]	P36
B24	VSS[016]	P37
C5	VSS[017]	P38
C9	VSS[018]	P39
C11	VSS[019]	P40
C14	VSS[020]	P41
C16	VSS[021]	P42
C19	VSS[022]	P43
C2	VSS[023]	P44
C22	VSS[024]	P45
C25	VSS[025]	P46
D1	VSS[026]	P47
D4	VSS[027]	P48
D8	VSS[028]	P49
D11	VSS[029]	P50
D13	VSS[030]	P51
D16	VSS[031]	P52
D19	VSS[032]	P53
D23	VSS[033]	P54
D26	VSS[034]	P55
E3	VSS[035]	P56
E6	VSS[036]	P57
E8	VSS[037]	P58
F11	VSS[038]	P59
F14	VSS[039]	P60
F16	VSS[040]	P61
F19	VSS[041]	P62
F21	VSS[042]	P63
F24	VSS[043]	P64
F5	VSS[044]	P65
F8	VSS[045]	P66
F11	VSS[046]	P67
F13	VSS[047]	P68
F16	VSS[048]	P69
F19	VSS[049]	P70
F2	VSS[050]	P71
F22	VSS[051]	P72
F25	VSS[052]	P73
G4	VSS[053]	P74
G1	VSS[054]	P75
G23	VSS[055]	P76
G26	VSS[056]	P77
H3	VSS[057]	P78
H6	VSS[058]	P79
H21	VSS[059]	P80
H24	VSS[060]	P81
J2	VSS[061]	P82
J5	VSS[062]	P83
J22	VSS[063]	P84
J25	VSS[064]	P85
K1	VSS[065]	P86
K4	VSS[066]	P87
K23	VSS[067]	P88
K26	VSS[068]	P89
L3	VSS[069]	P90
L6	VSS[070]	P91
L21	VSS[071]	P92
L24	VSS[072]	P93
M2	VSS[073]	P94
M5	VSS[074]	P95
M22	VSS[075]	P96
M25	VSS[076]	P97
N1	VSS[077]	P98
N4	VSS[078]	P99
N23	VSS[079]	P100
N26	VSS[080]	P101
P3	VSS[081]	P102

Merom Ball-out Rev 1a
CONN@

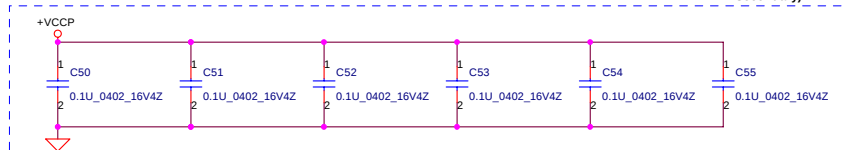


Near CPU CORE regulator

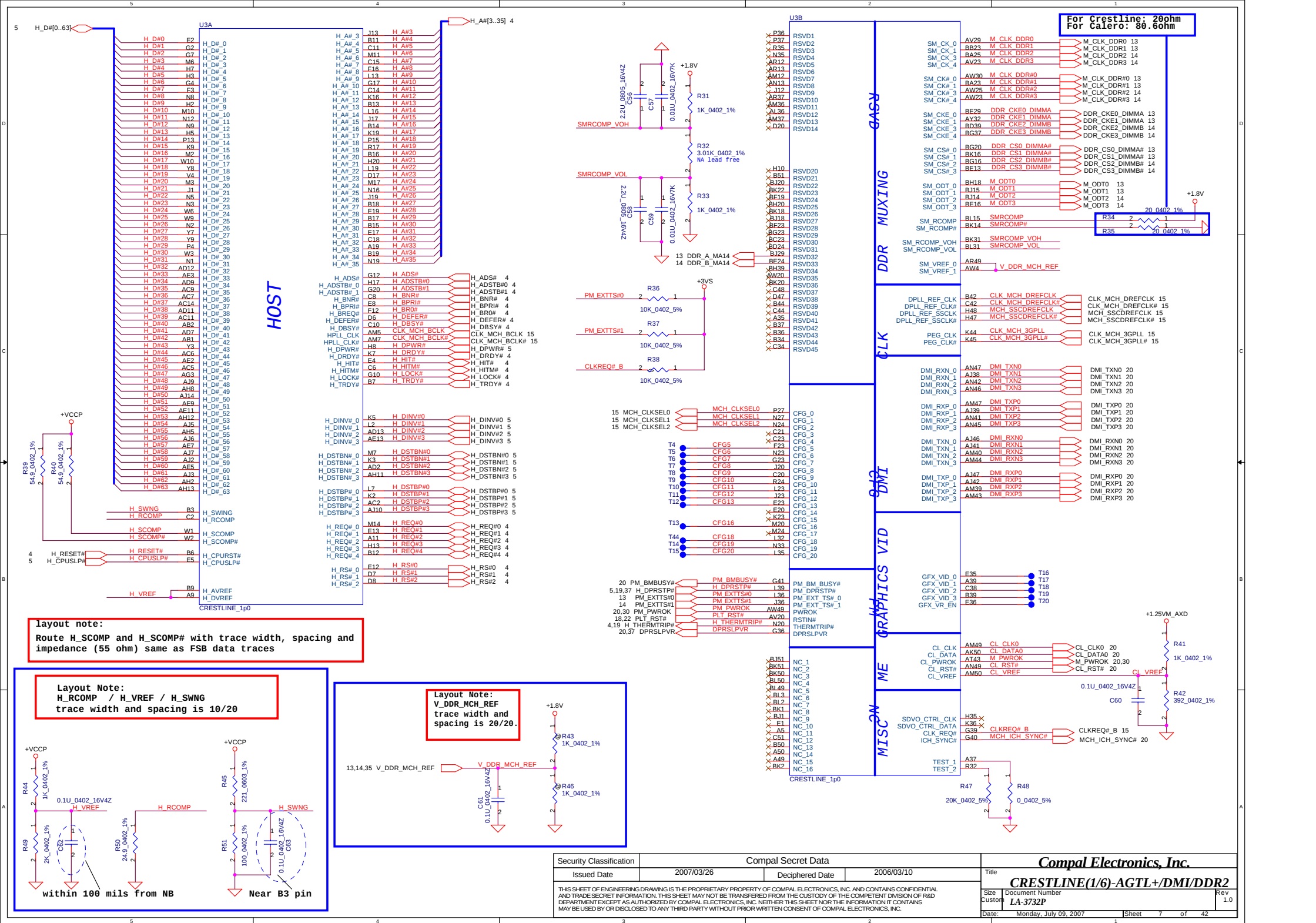
ESR <= 1.5m ohm
Capacitor > 1980uF



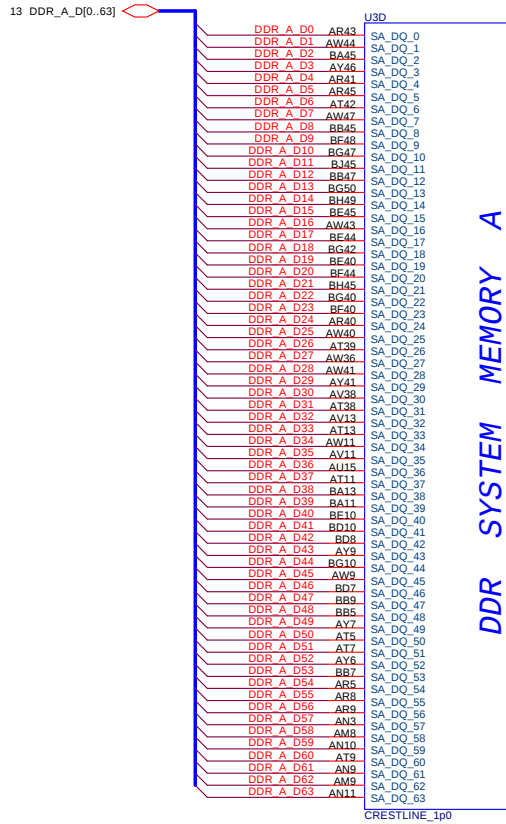
Place these inside
socket cavity on L8
(North side
Secondary)



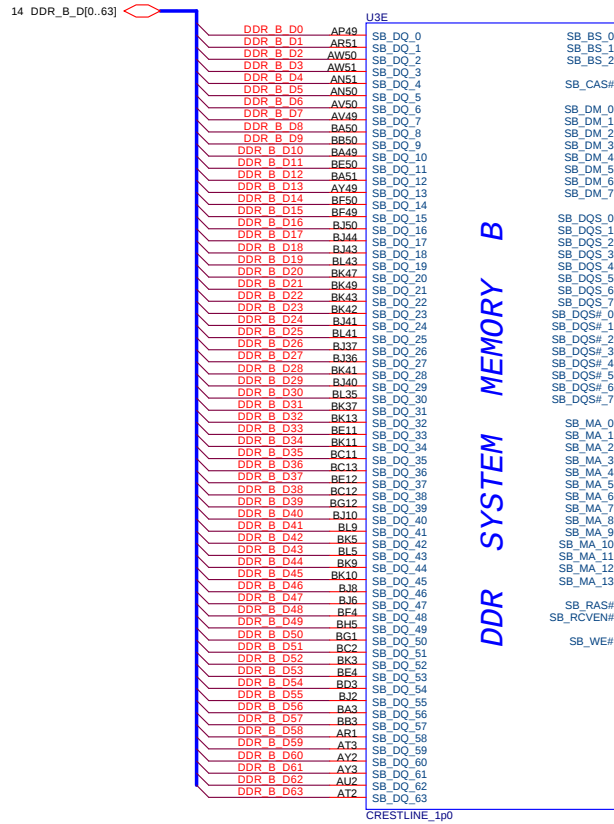
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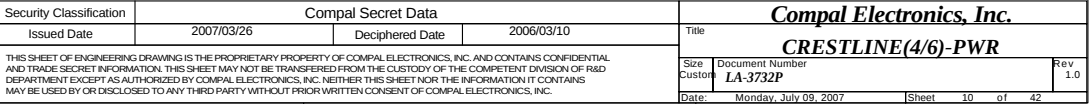


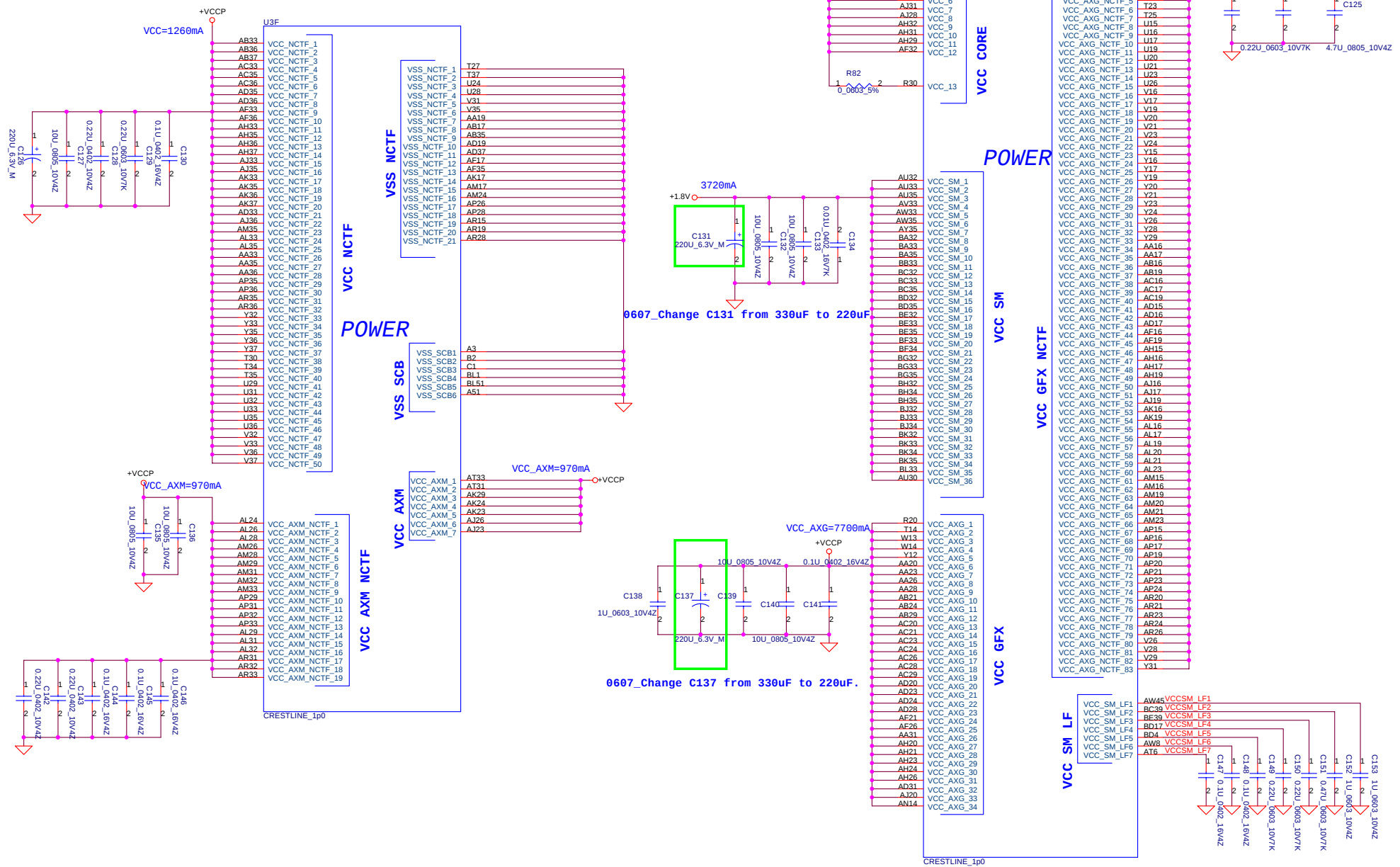
DDR SYSTEM MEMORY A



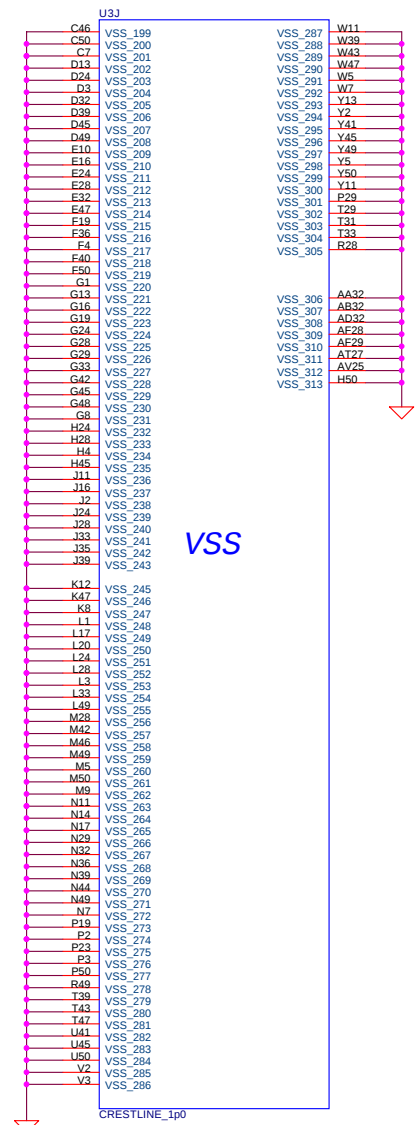
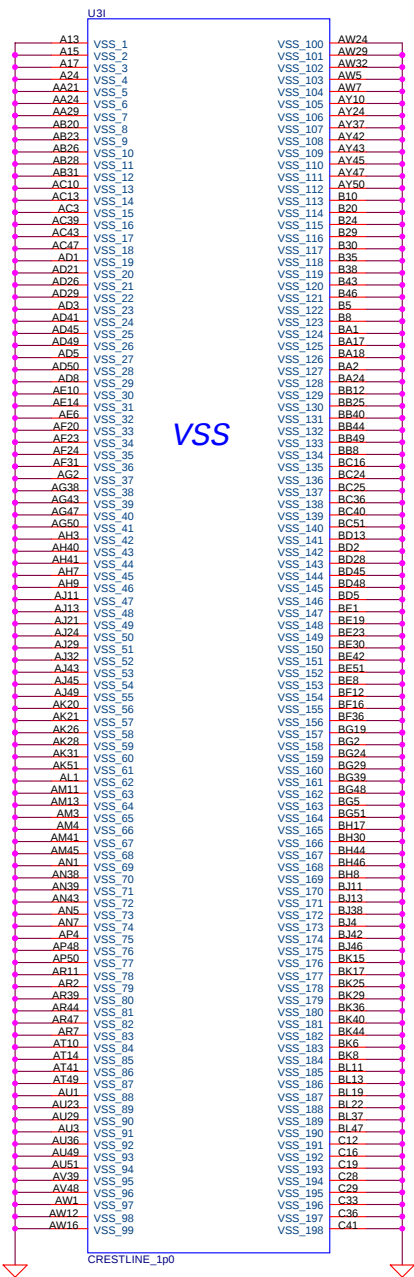
DDR SYSTEM MEMORY B

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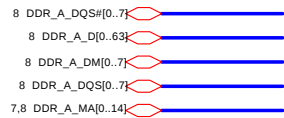




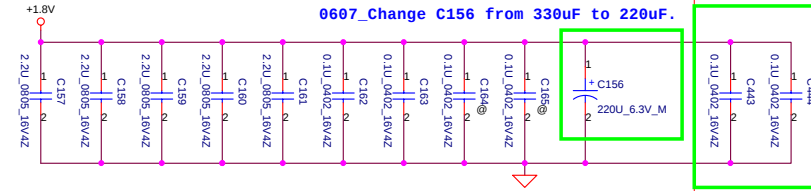
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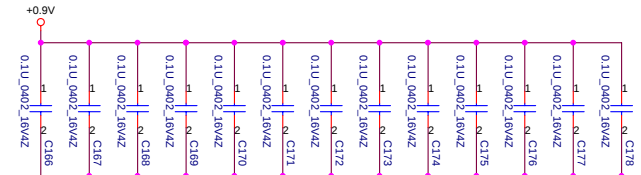


Layout Note:
Place near JP34

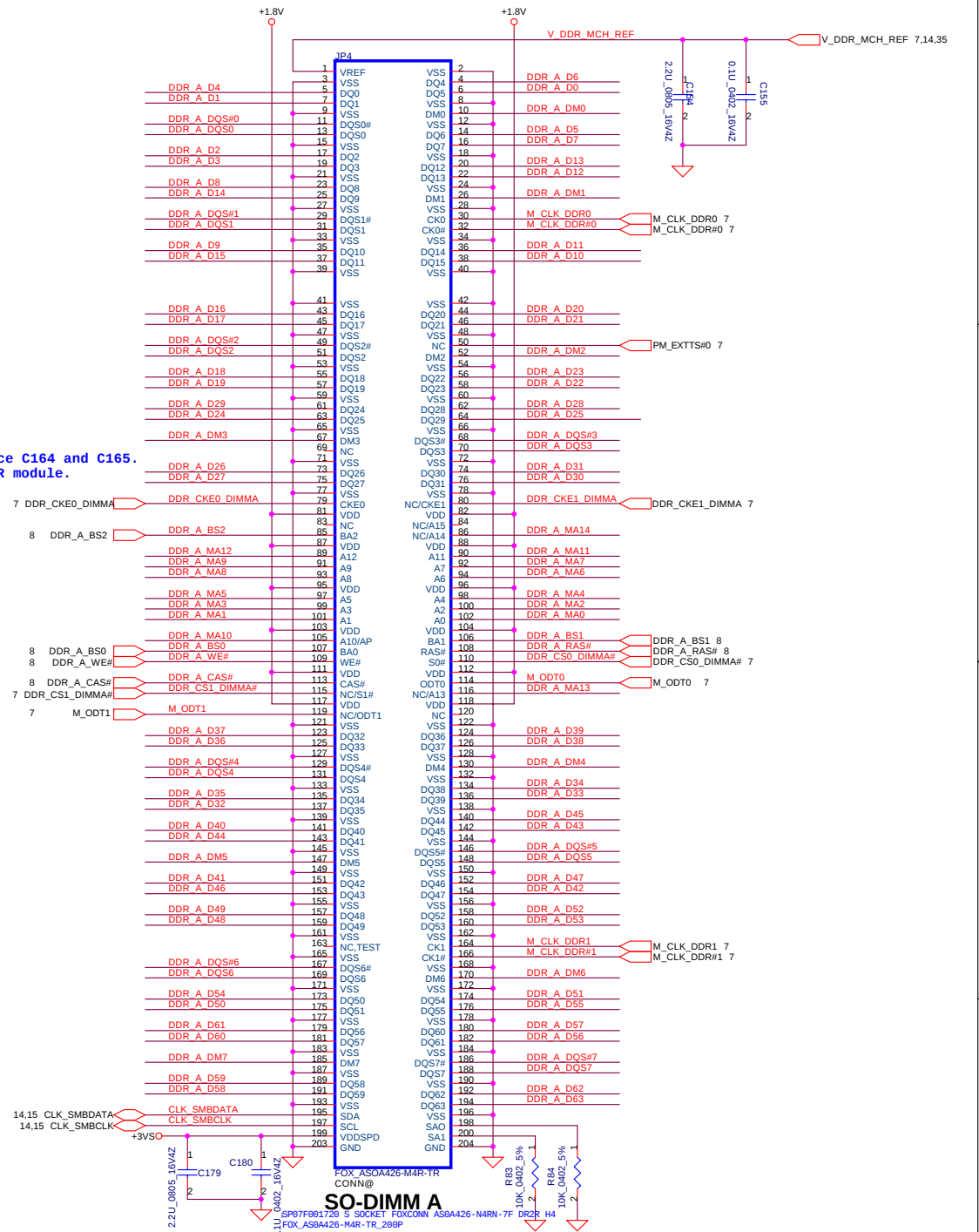
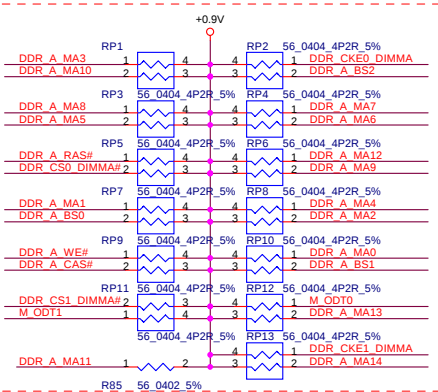


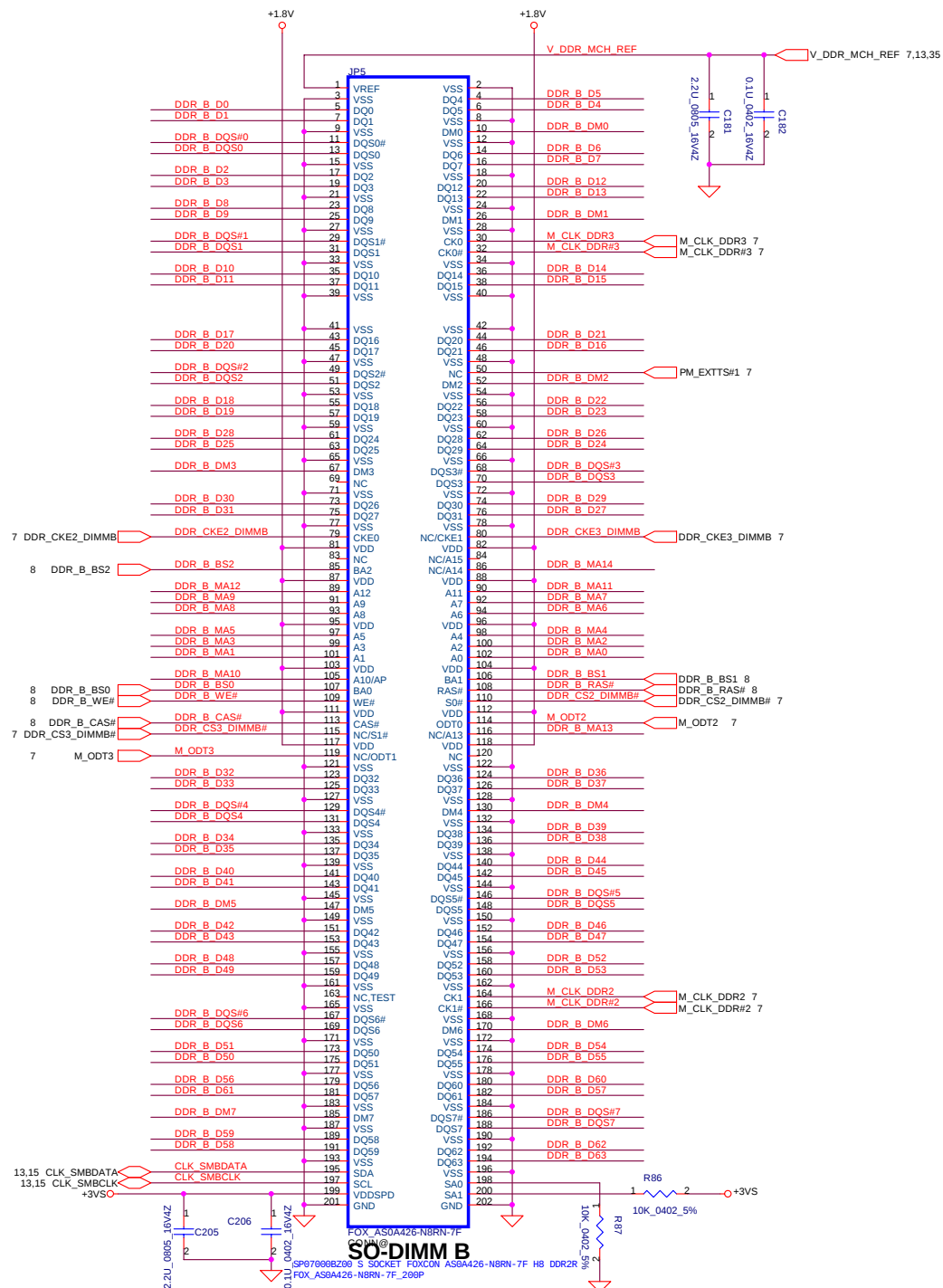
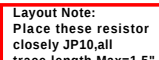
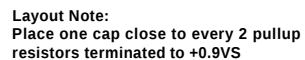
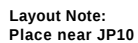
0605_Add C443 and C444 to replace C164 and C165.
To solve interfere with DDR module.

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP34, all trace length Max=1.5"



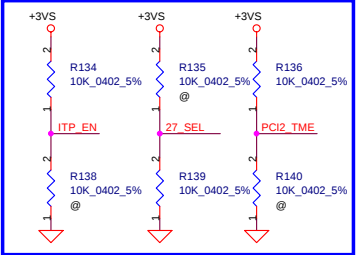
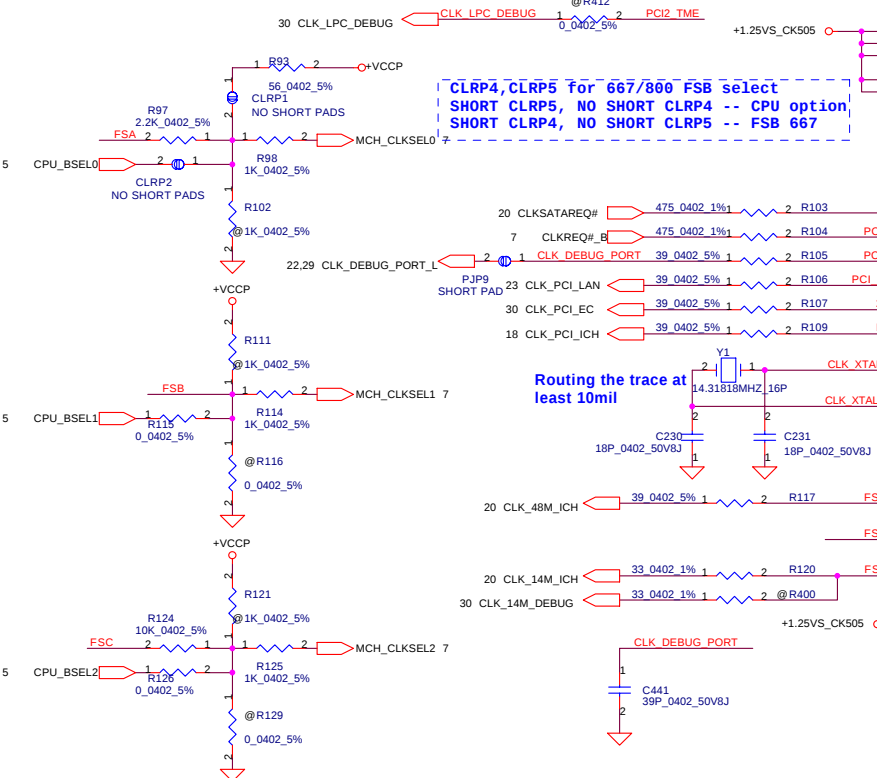


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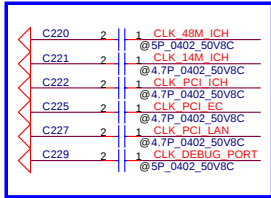
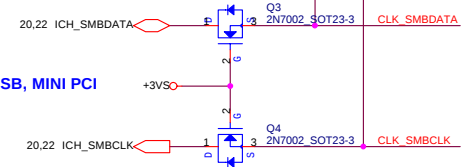
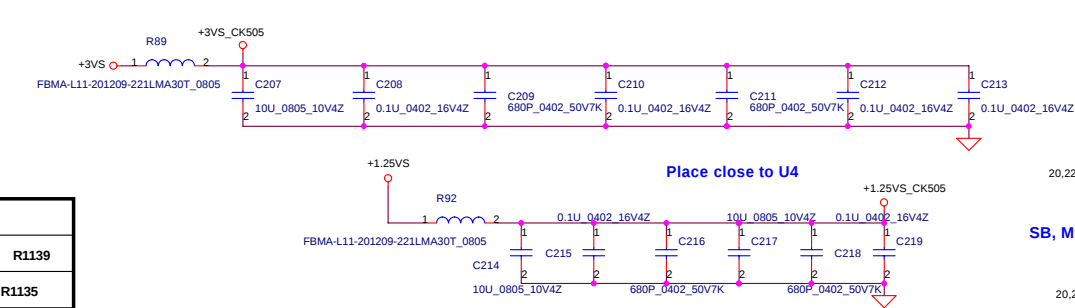
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHZ	SRC MHZ	PCI MHZ
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

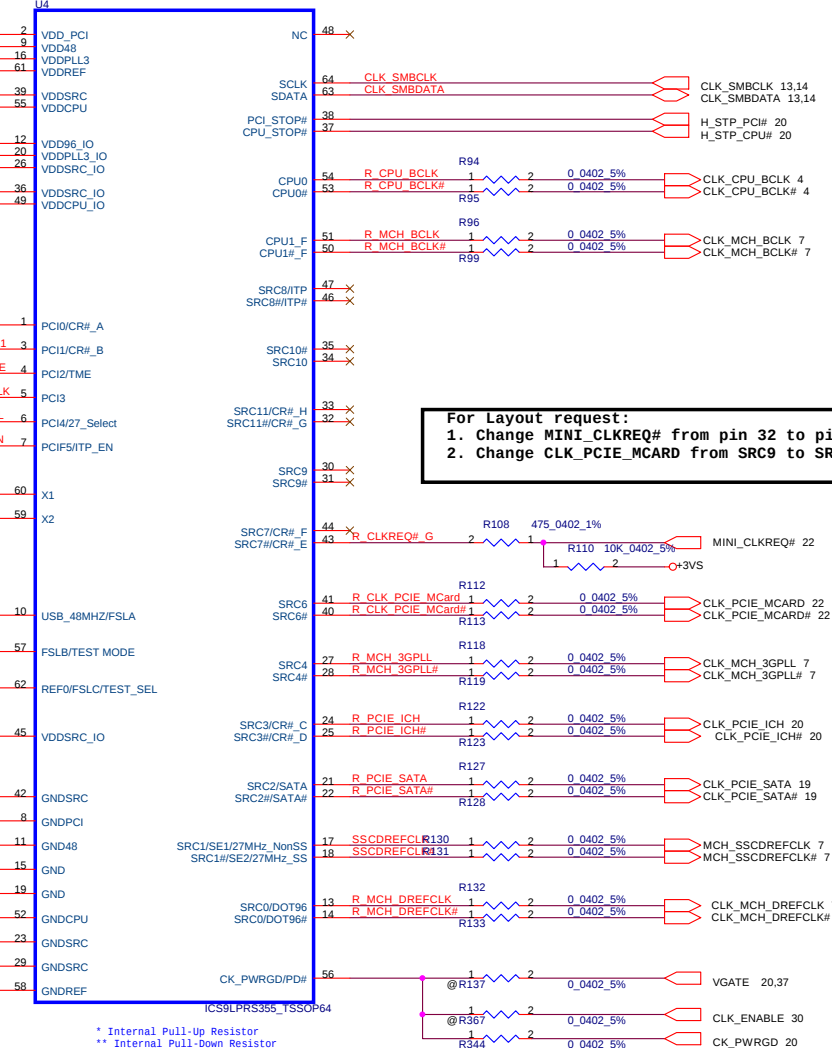
CPU Driven	Stuff	R1107	R1135	R1083			
*(Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139
	Stuff	R1086	R1139	R1135	R1074	R1139	R1135
667MHz	No Stuff	R1083	R1107	R1128			
		R1113	R1098				
800MHz	Stuff	R1135	R1139				
	No Stuff	R1083	R1086	R1098	R1128		
		R1074	R1107	R1113			



For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1 = Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

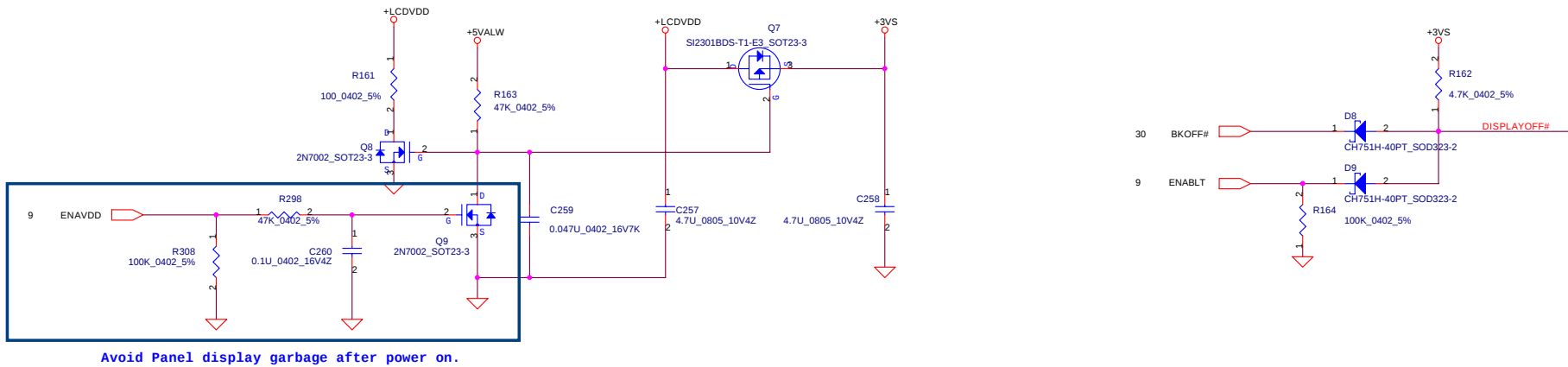
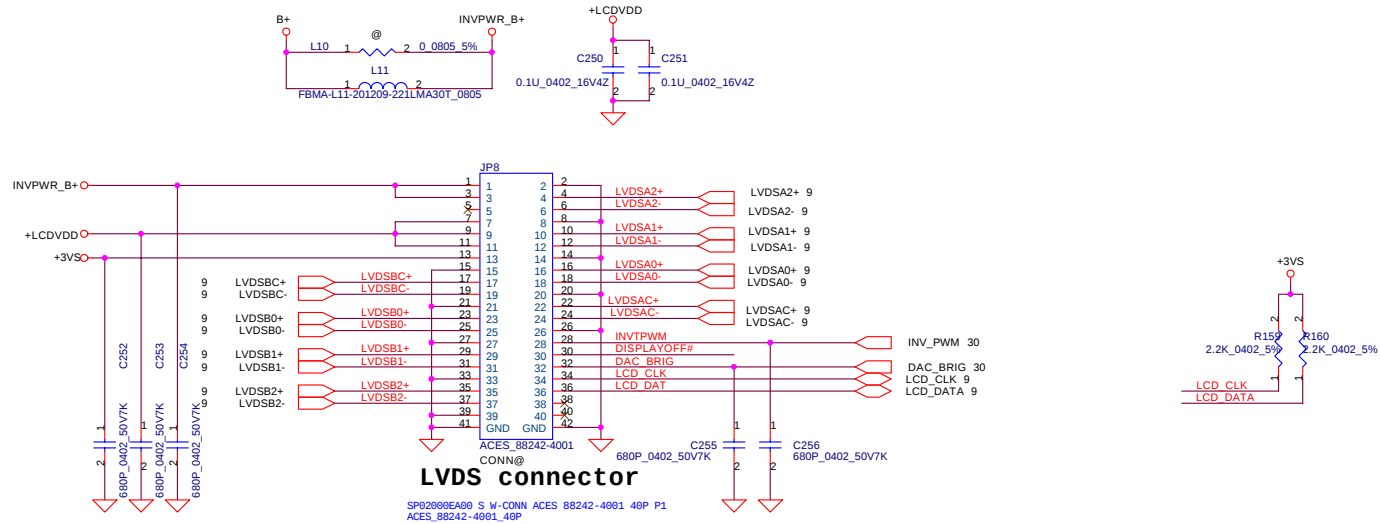


For Layout request:
1. Change MINI_CLKREQ# from pin 32 to pin 43.
2. Change CLK_PCIE_MCARD from SRC9 to SRC6.



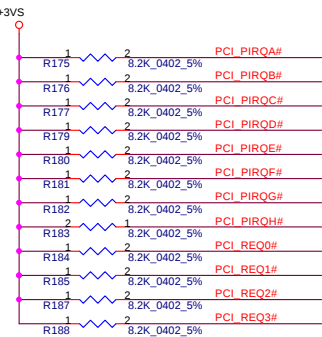
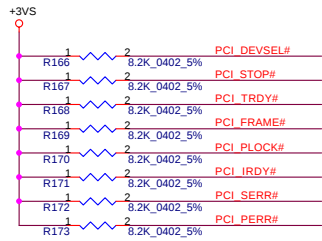
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LVDS CONN



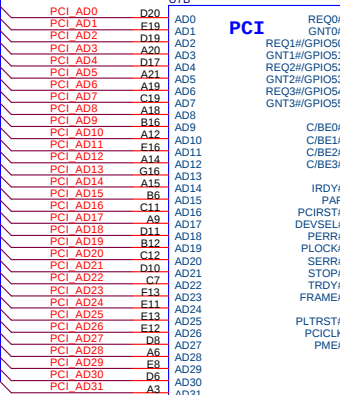
Avoid Panel display garbage after power on.

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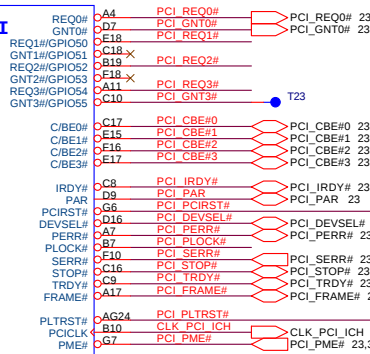
23 PCI_AD[0..31]

23 PCI_PIRQA#

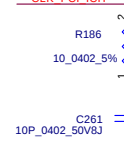


Interrupt I/F
ICH8M REV 1.0

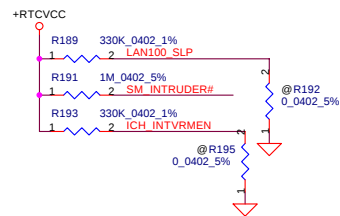
PCI



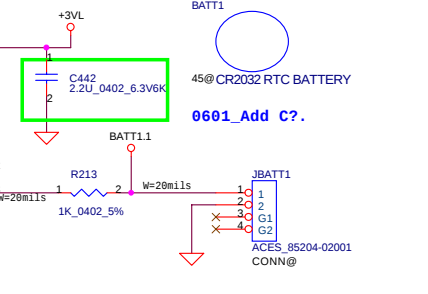
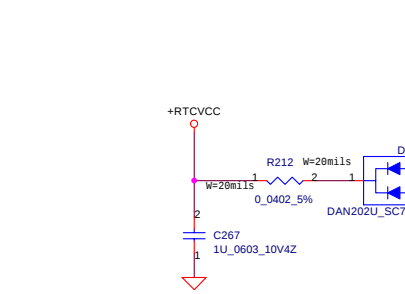
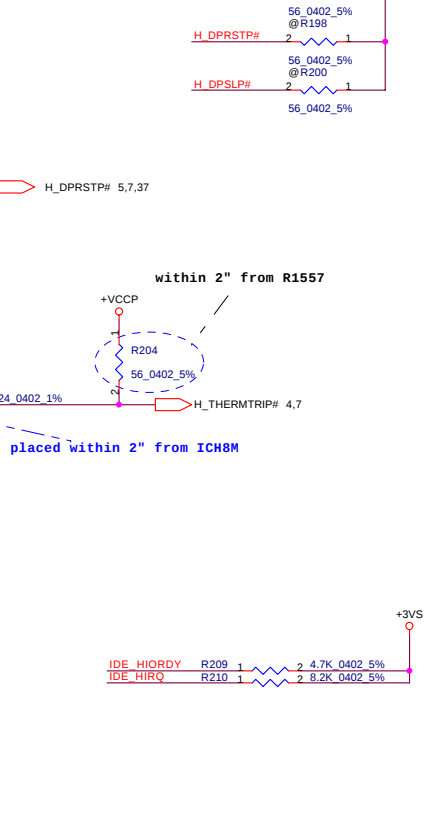
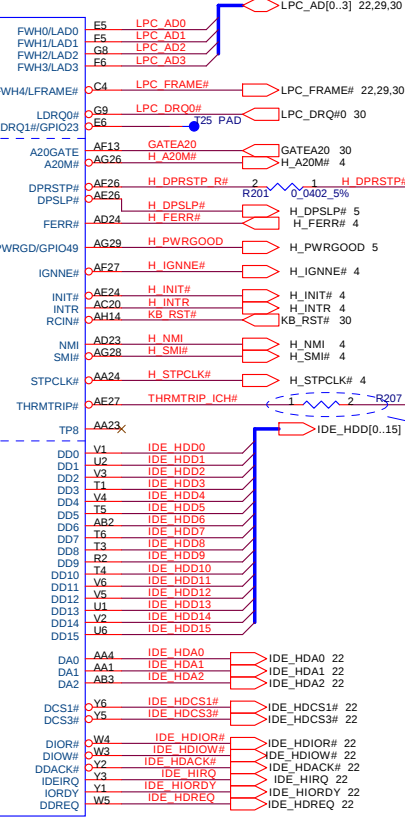
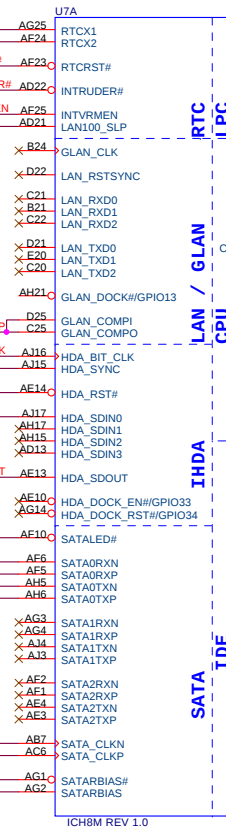
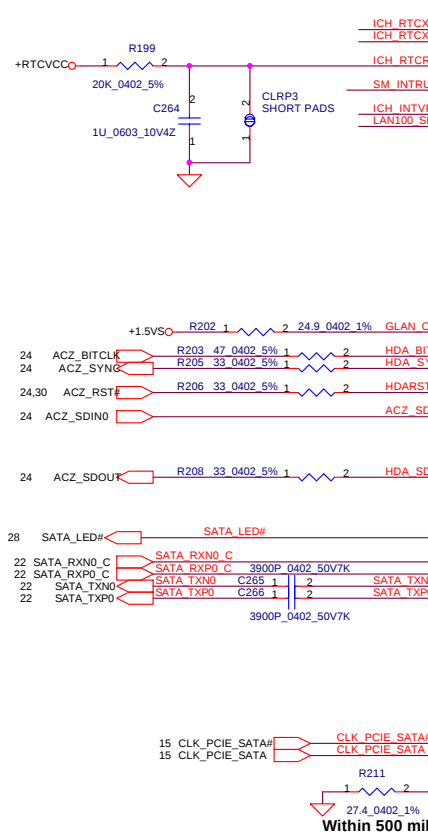
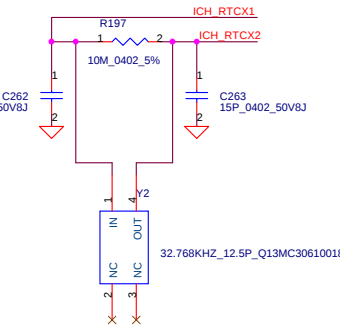
Place closely pin B10



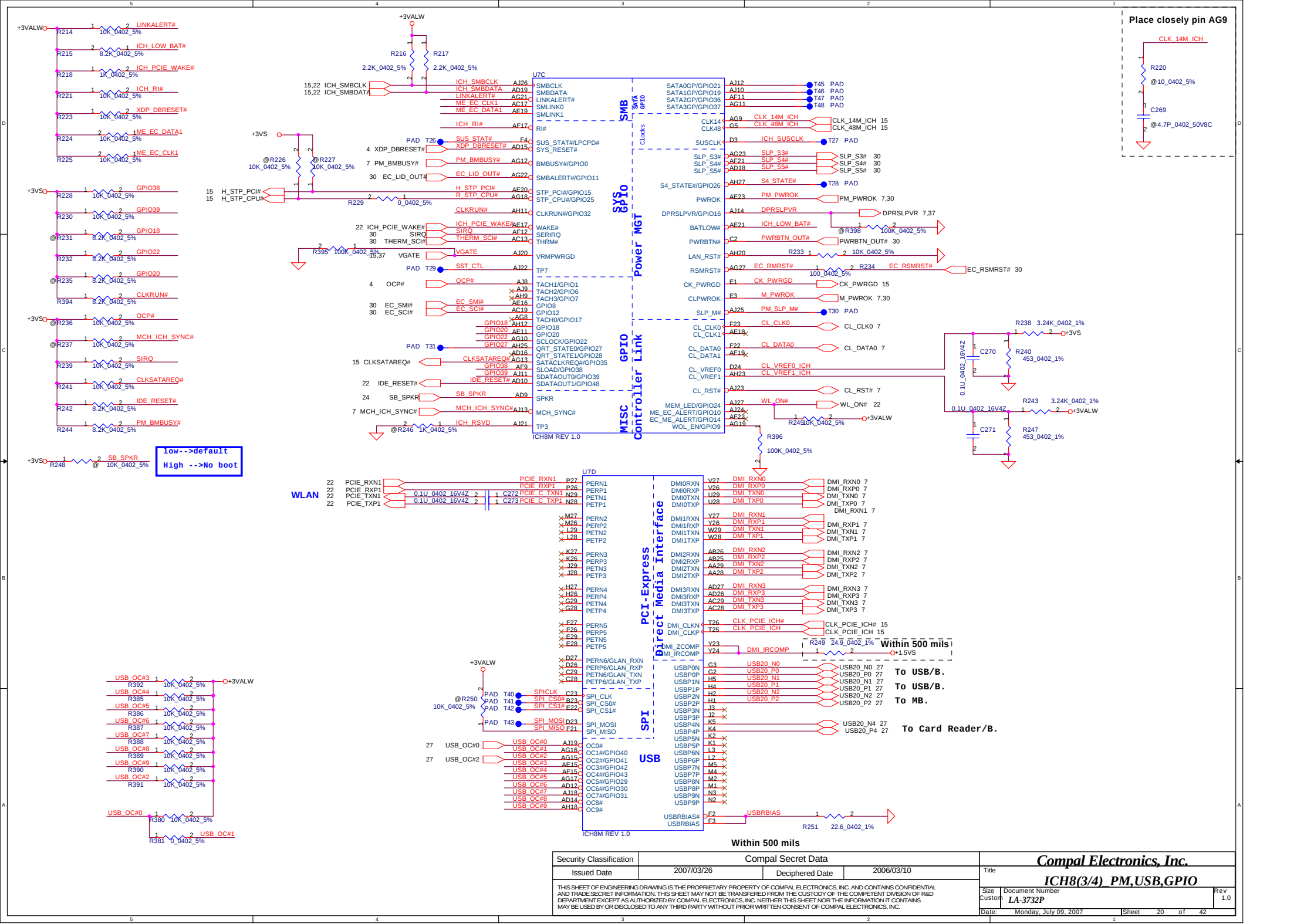
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *
A16 swap override Strap		
PCI_GNT3#	*Low= A16 swap override Enble High= Default	

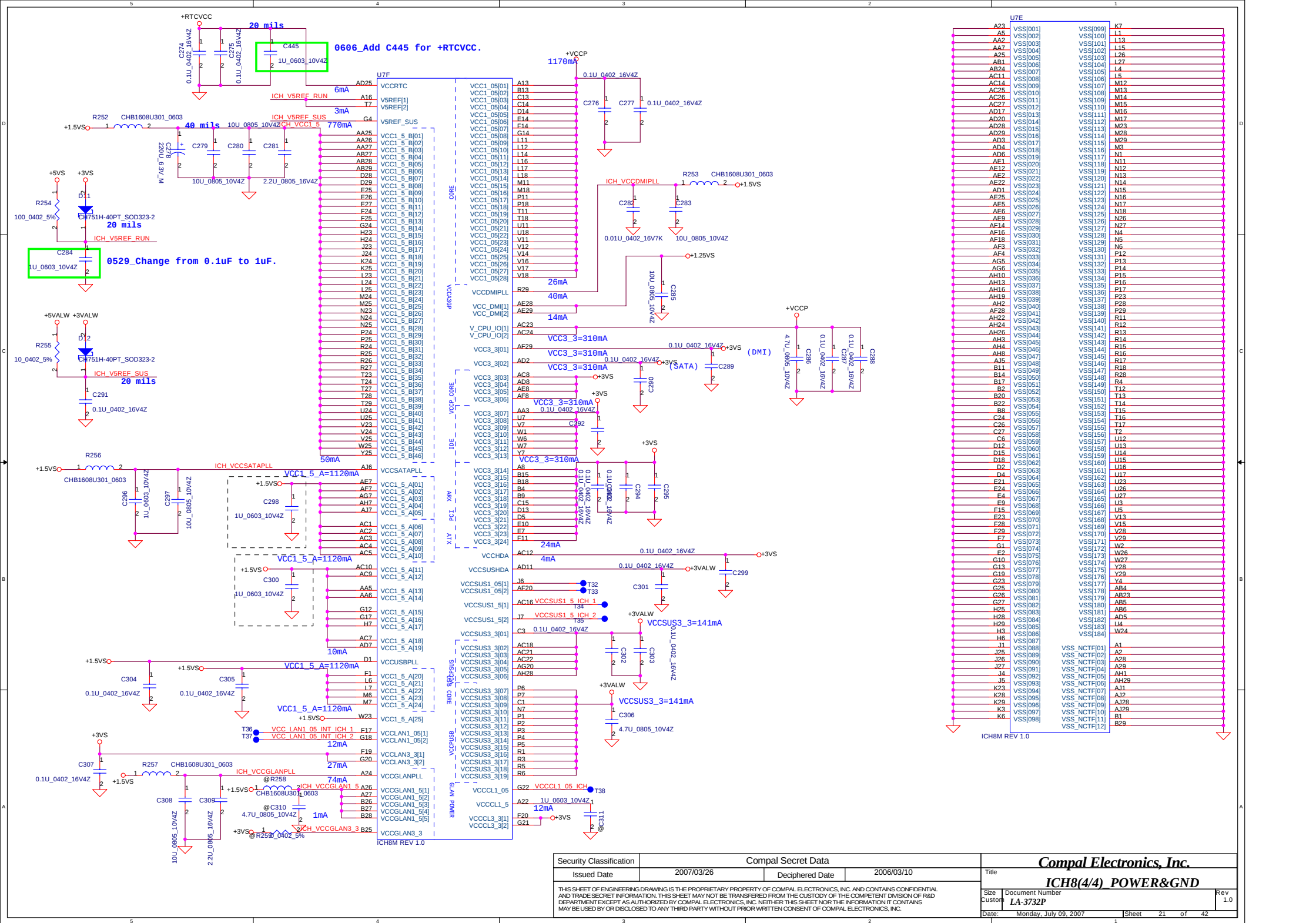


ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



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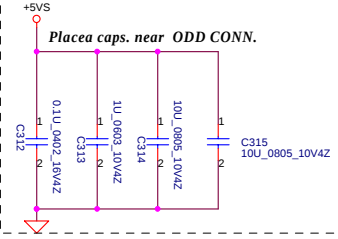
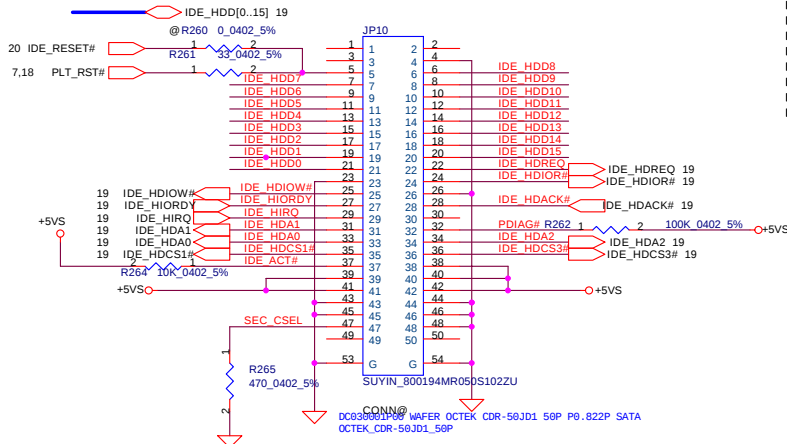
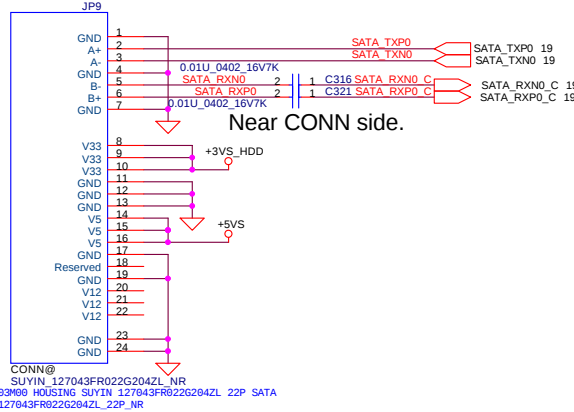
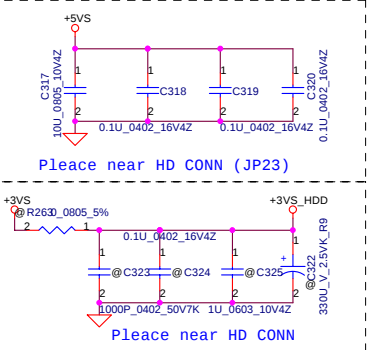




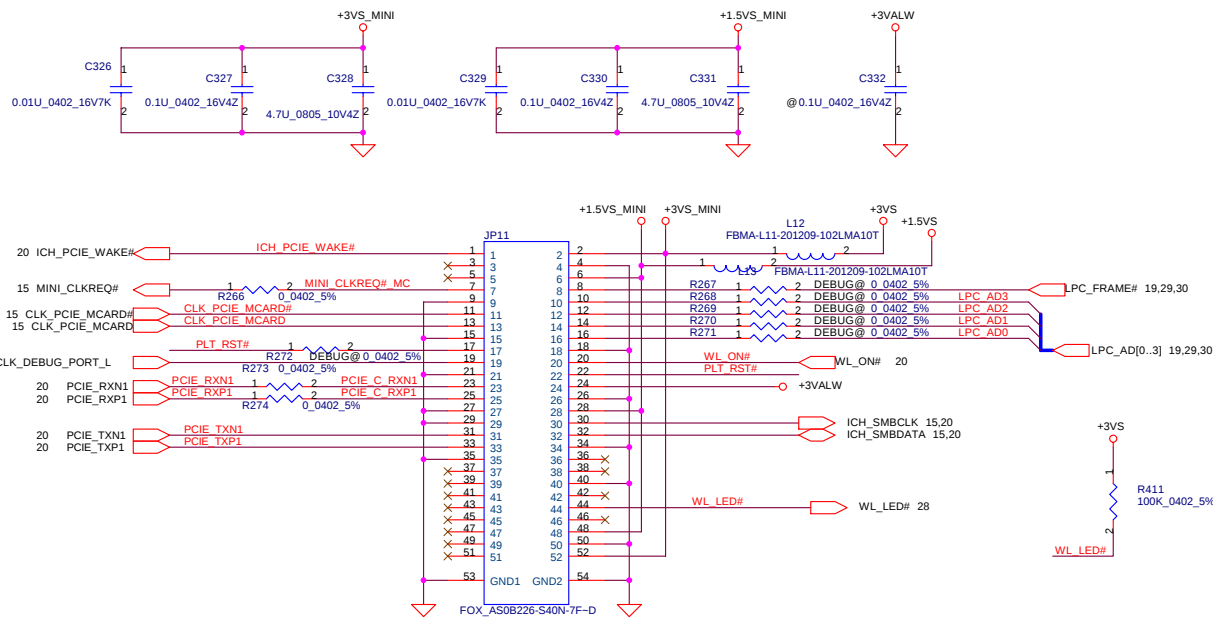
HDD Connector

CD-ROM Connector

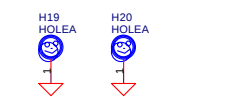
Place caps. near ODD CONN.



Mini-Express Card---WLAN



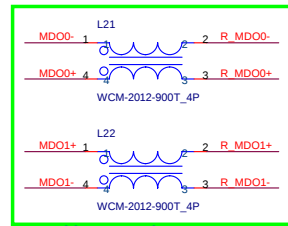
Mini Card STANDOFF



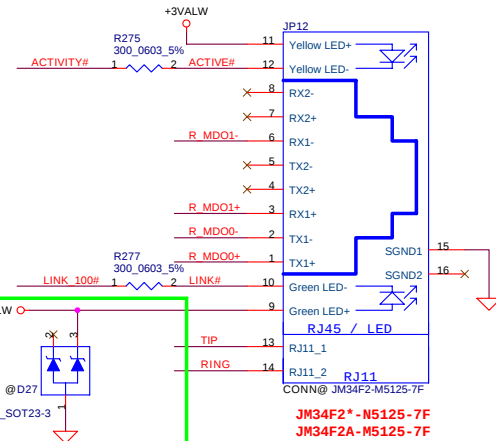
EC829000100 MINICARD_STANDOFF_8

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Close to JP12.



0601_Add L21 and L22 For EMI request.



0611_Reserve D27 and D28 For EMI request.

close to chip

close to magnetic

0310_Dammy by safty request.
Footprint can not match part number.

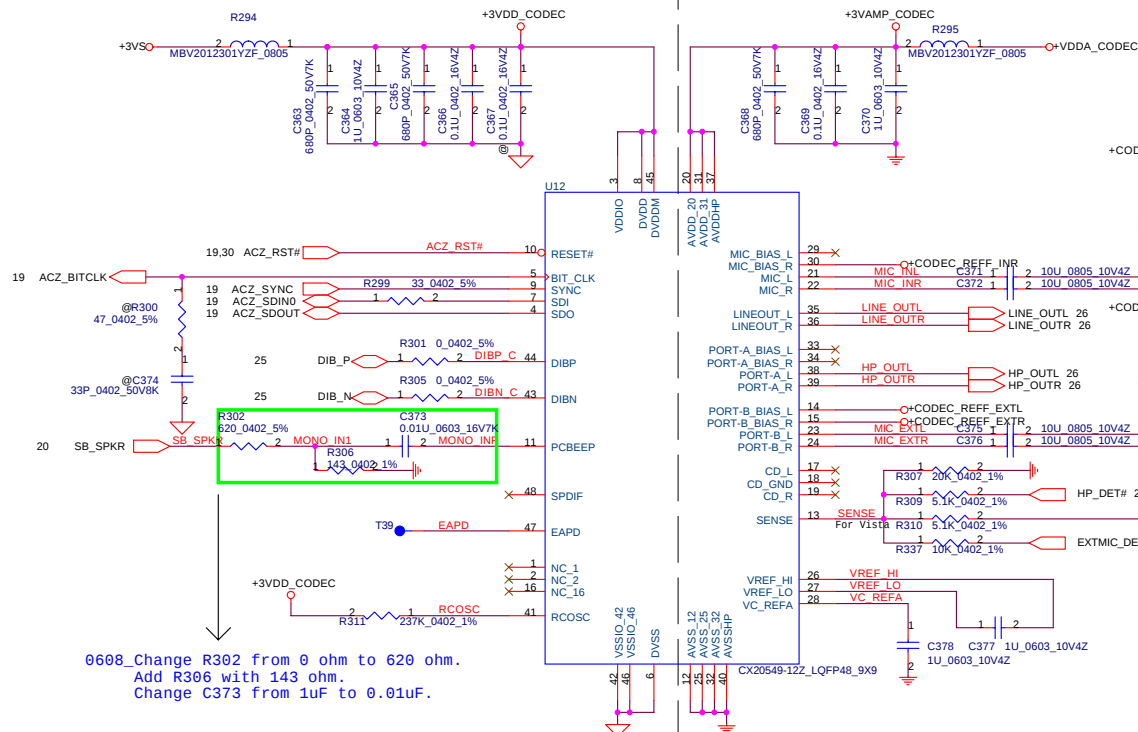
0601_For EMI request.

RJ11

Security Classification		Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2007/08/29	LAN-8100CL	
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AUDIO CODEC

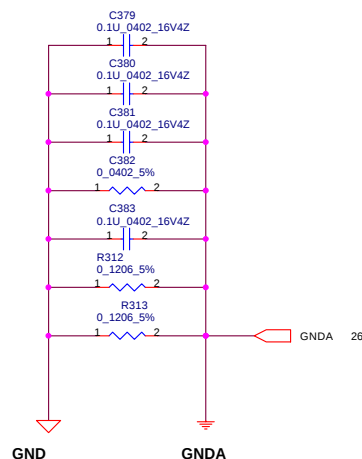
In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.



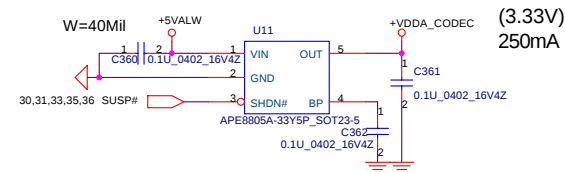
0608_Change R302 from 0 ohm to 620 ohm.
Add R306 with 143 ohm.
Change C373 from 1uF to 0.01uF.

DIGITAL

ANALOG

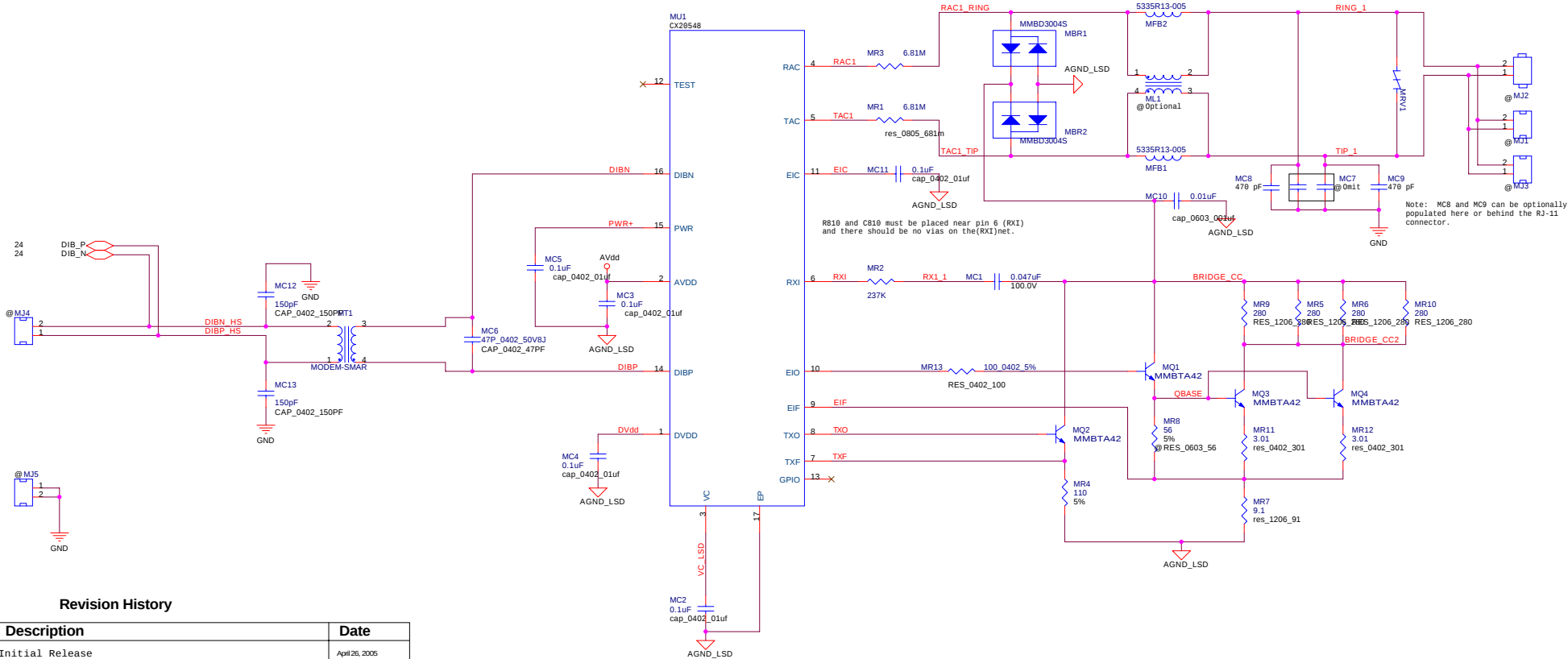


CODEC POWER



HP_DET#	MIC_DET	LINEOUT	PORT-A <Airphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

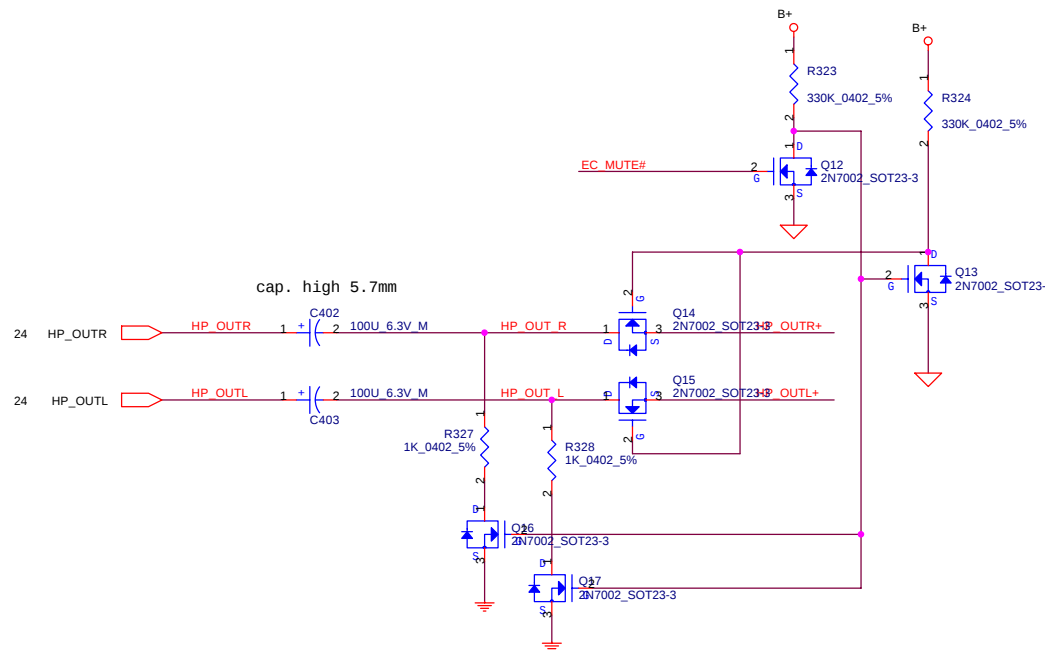
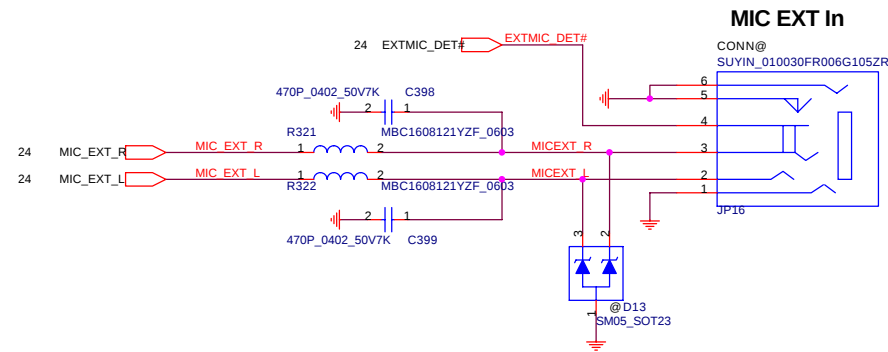
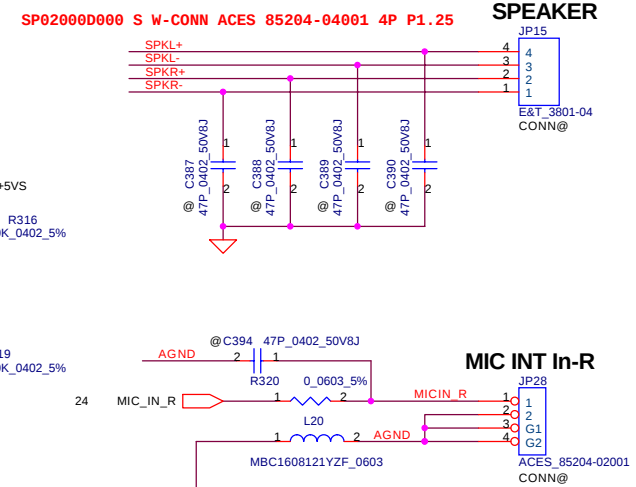
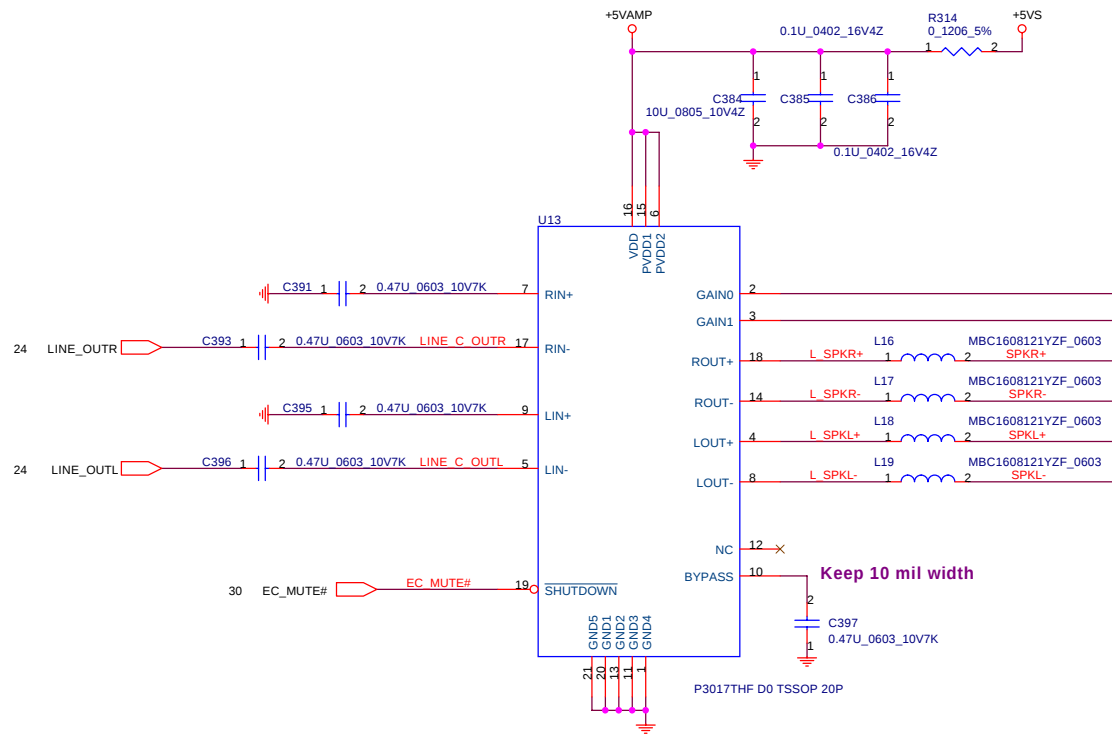
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2007/03/26	Deciphered Date	2006/03/10	Title	AMOM codec	
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Revision History

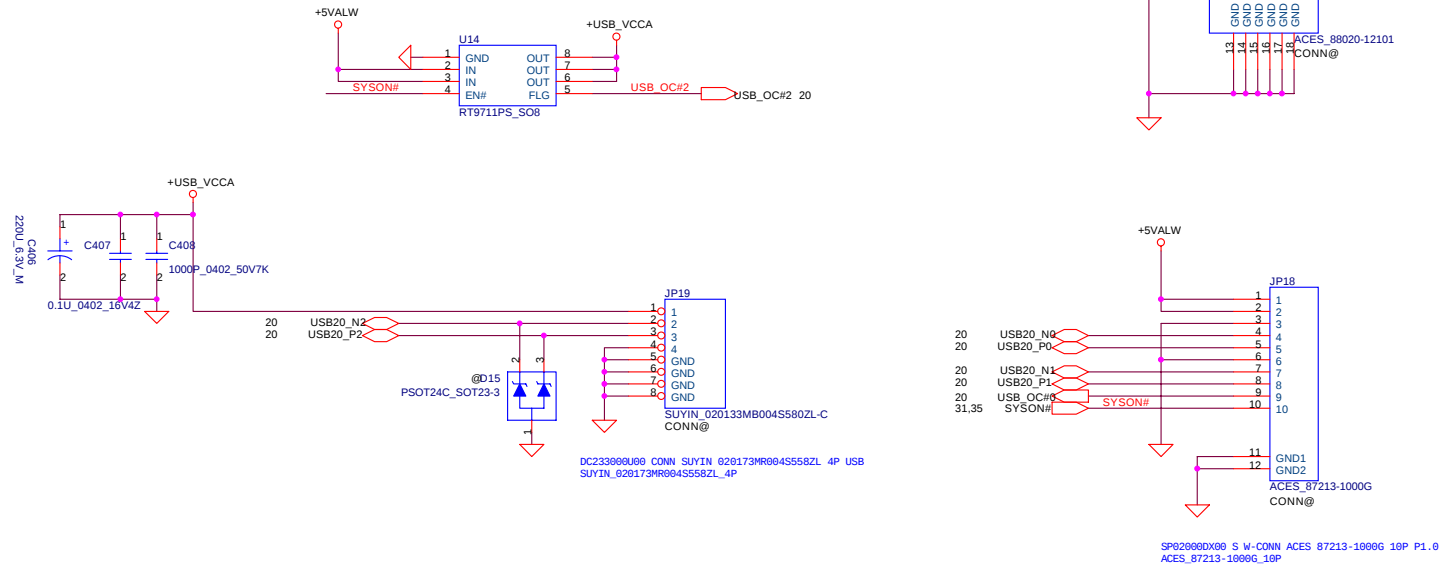
REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	August 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 18, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

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				AMOM-CX20548		
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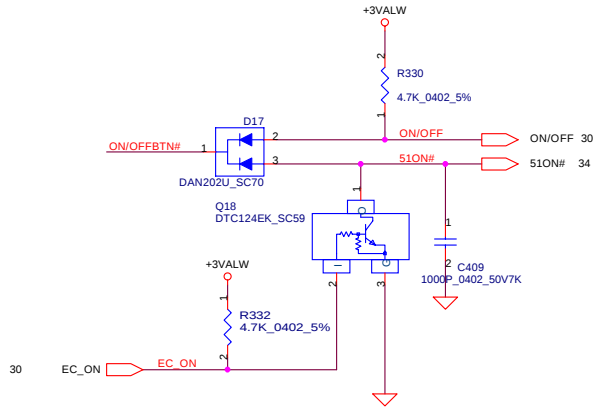
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Issued Date	2007/03/26	Deciphered Date	2007/08/29	Title	
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USB Port

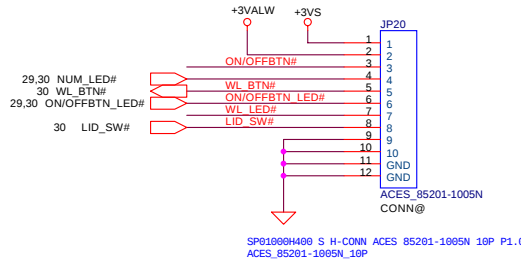


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					Size	Document Number	Rev
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Power ON/OFF

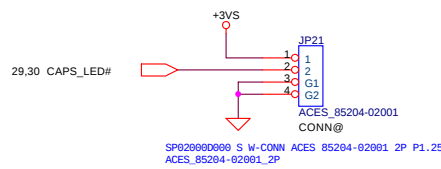


M/BtoS/B



0426_Change all LED power source from 5V to 3V.

M/B to SB(Caps Lock LED)



POWER LED(Left 1)

BLUE



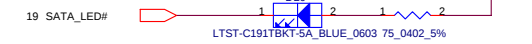
Battery Charge LED(Left 2)

BLUE

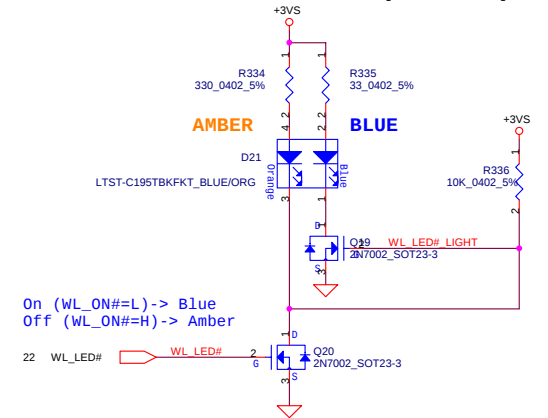


HDD LED(Left 3)

BLUE



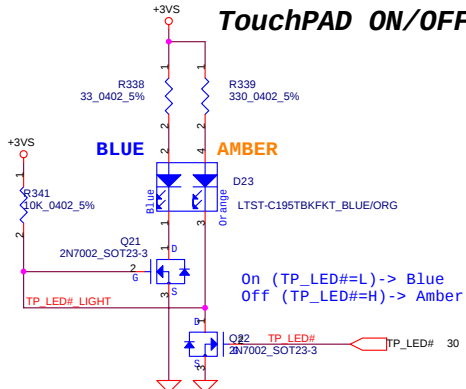
Wireless ON/OFF LED(Left 4)



On (WL_ON#=L) -> Blue
Off (WL_ON#=H) -> Amber

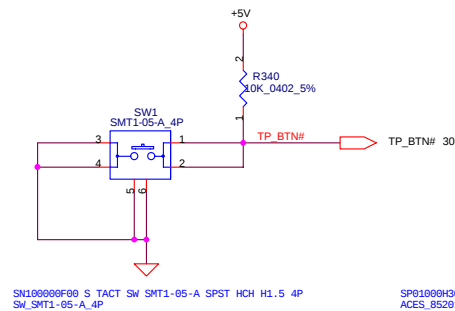
D21, D25, D23 Footprint can not match part number.

TouchPAD ON/OFF LED

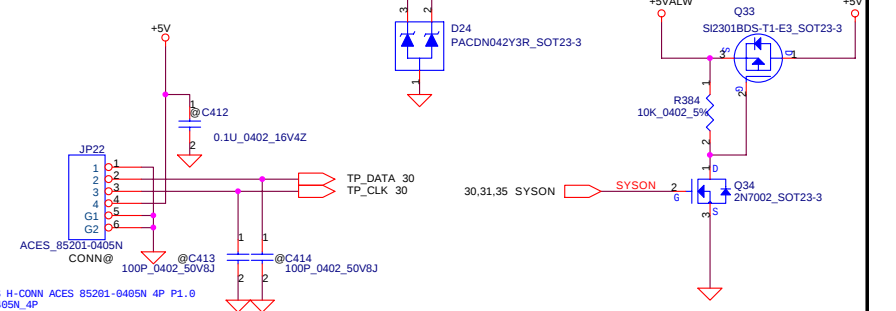


On (TP_LED#=L) -> Blue
Off (TP_LED#=H) -> Amber

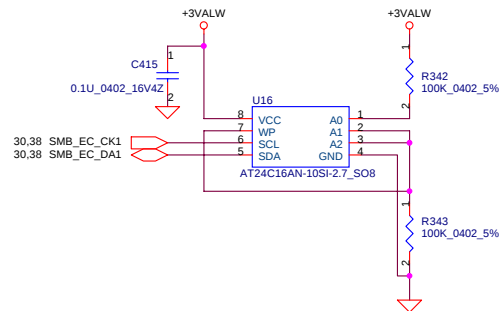
TP ON/OFF



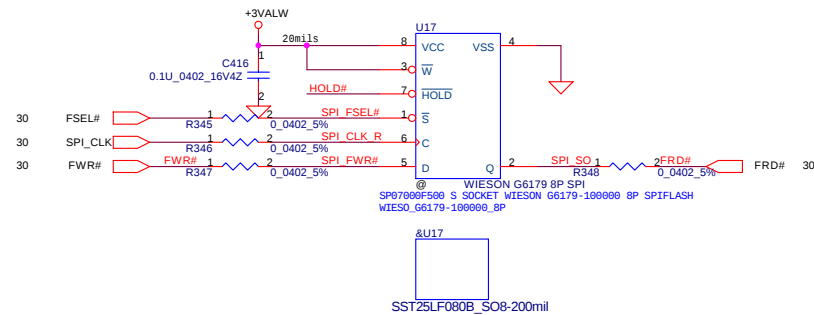
T/P Board



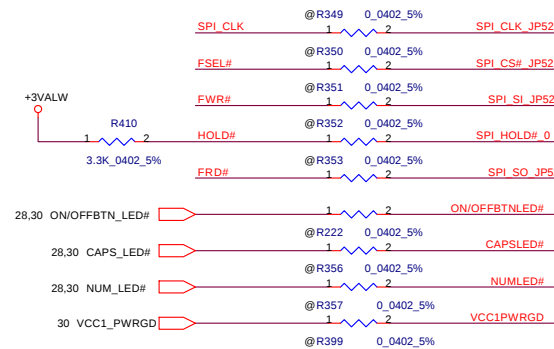
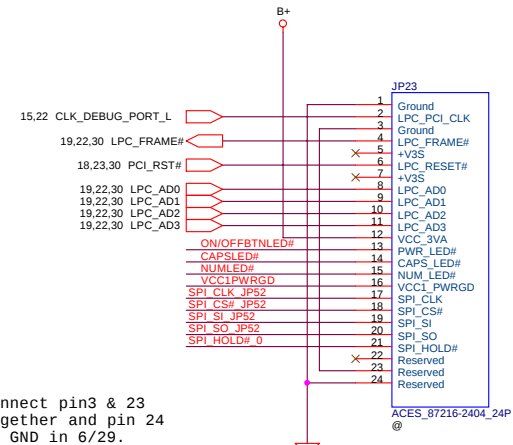
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Issued Date	2007/03/26	Deciphered Date	2006/07/26	Title	LED/SW
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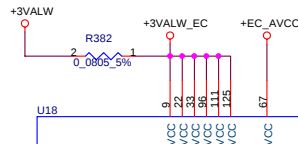
SPI ROM



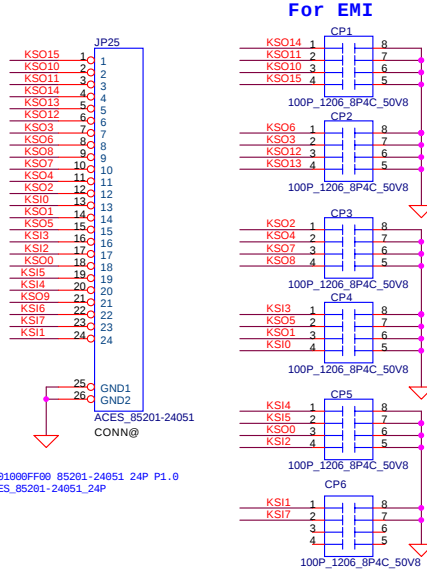
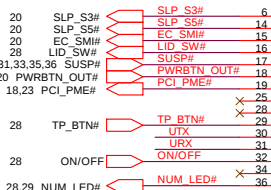
LPC Debug Port



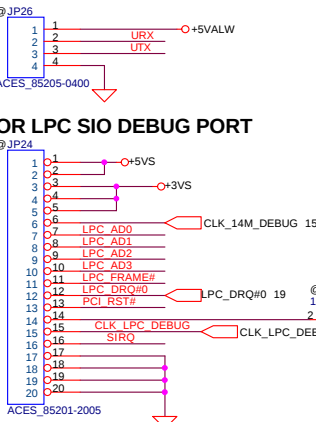
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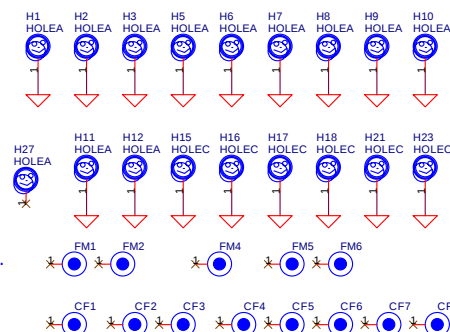
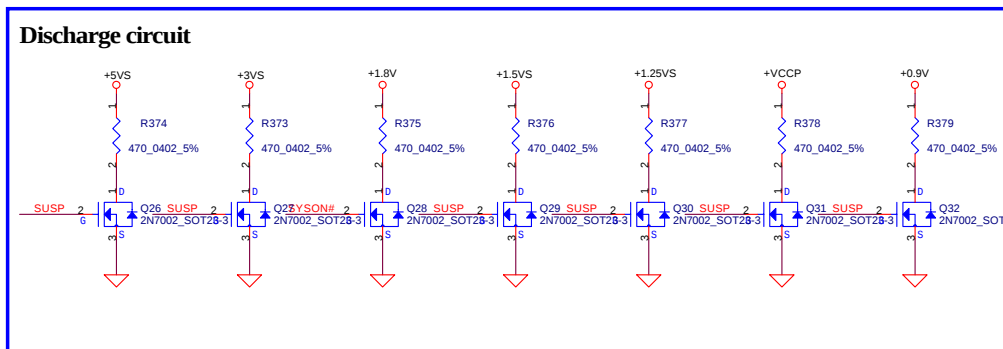
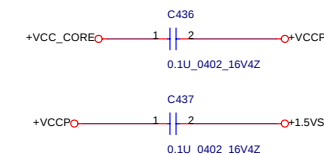
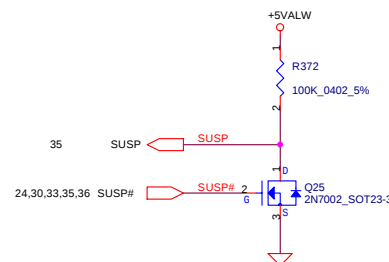
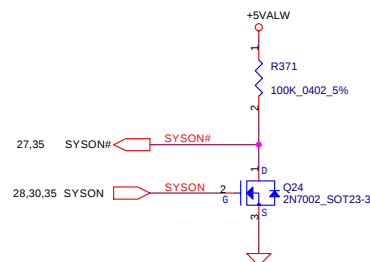
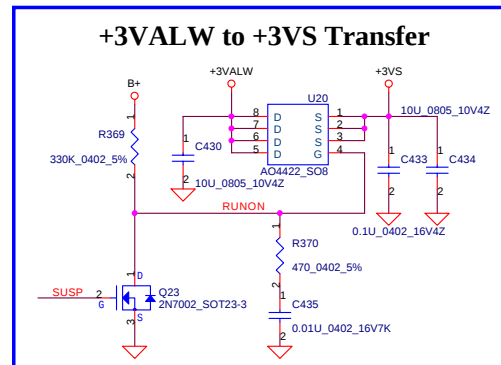
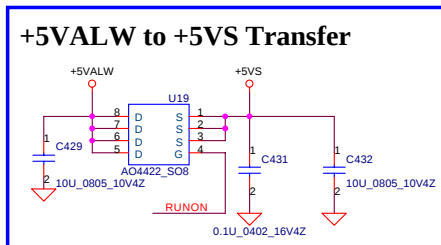
The timing diagram shows three signals over time. The ACIN signal is a red square wave. The TP_CLK signal is a blue square wave. The TP_DATA signal is a green square wave. The TP_CLK signal is shown with a period of 10K_0402_5% and a resistance of R361. The TP_DATA signal is shown with a period of 10K_0402_5% and a resistance of R362. The signals are connected to a +5V supply.



FOR LPC SIO DEBUG PORT

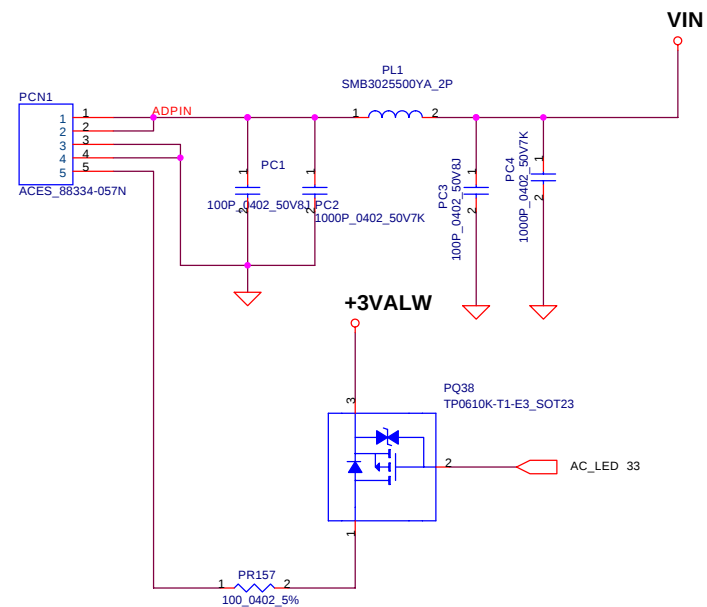


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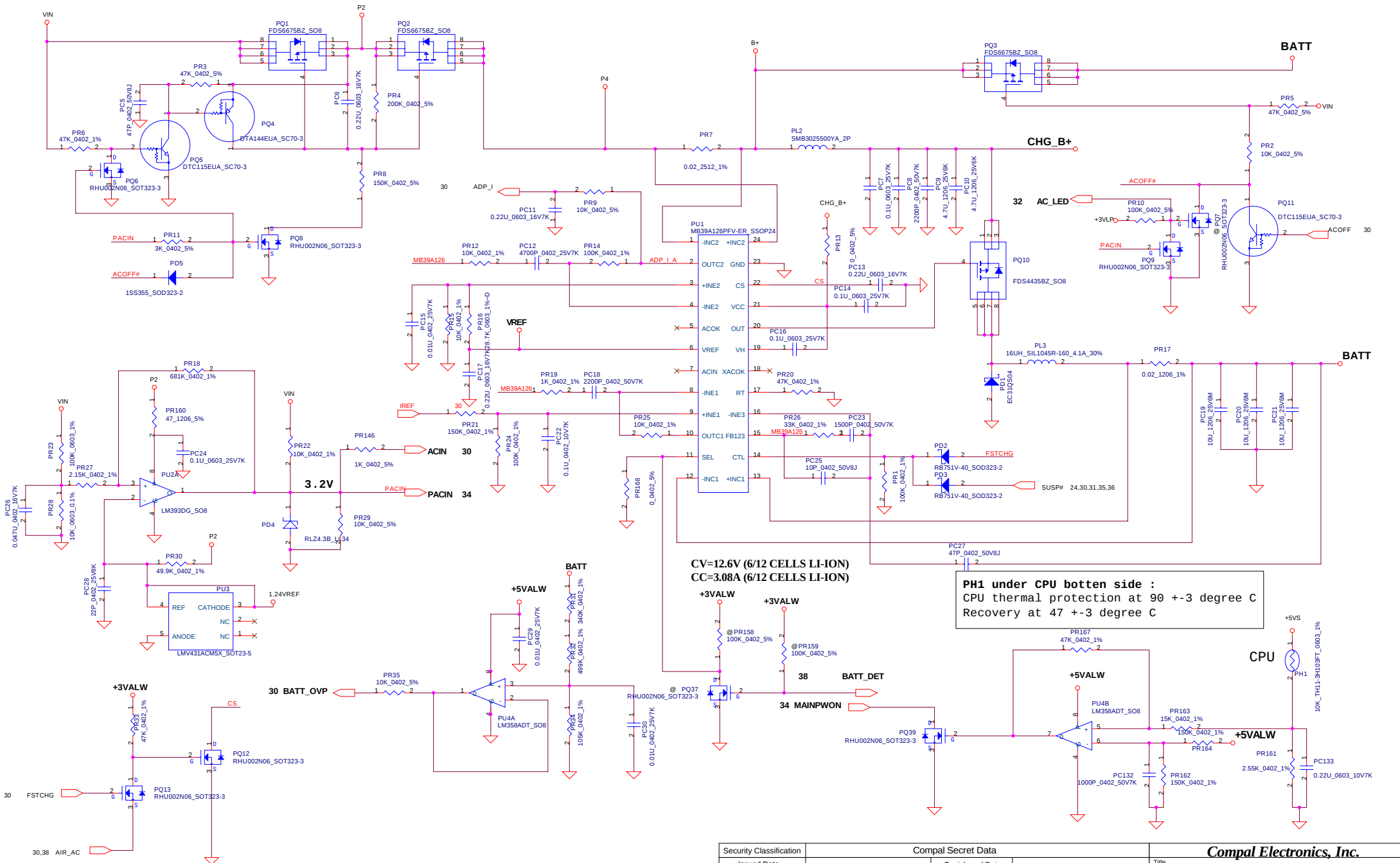
For Card reader/B stand off.

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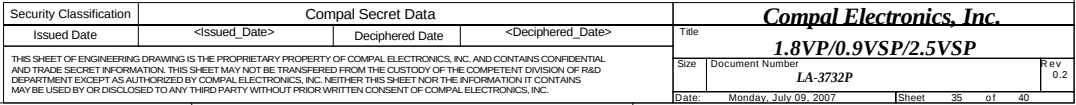


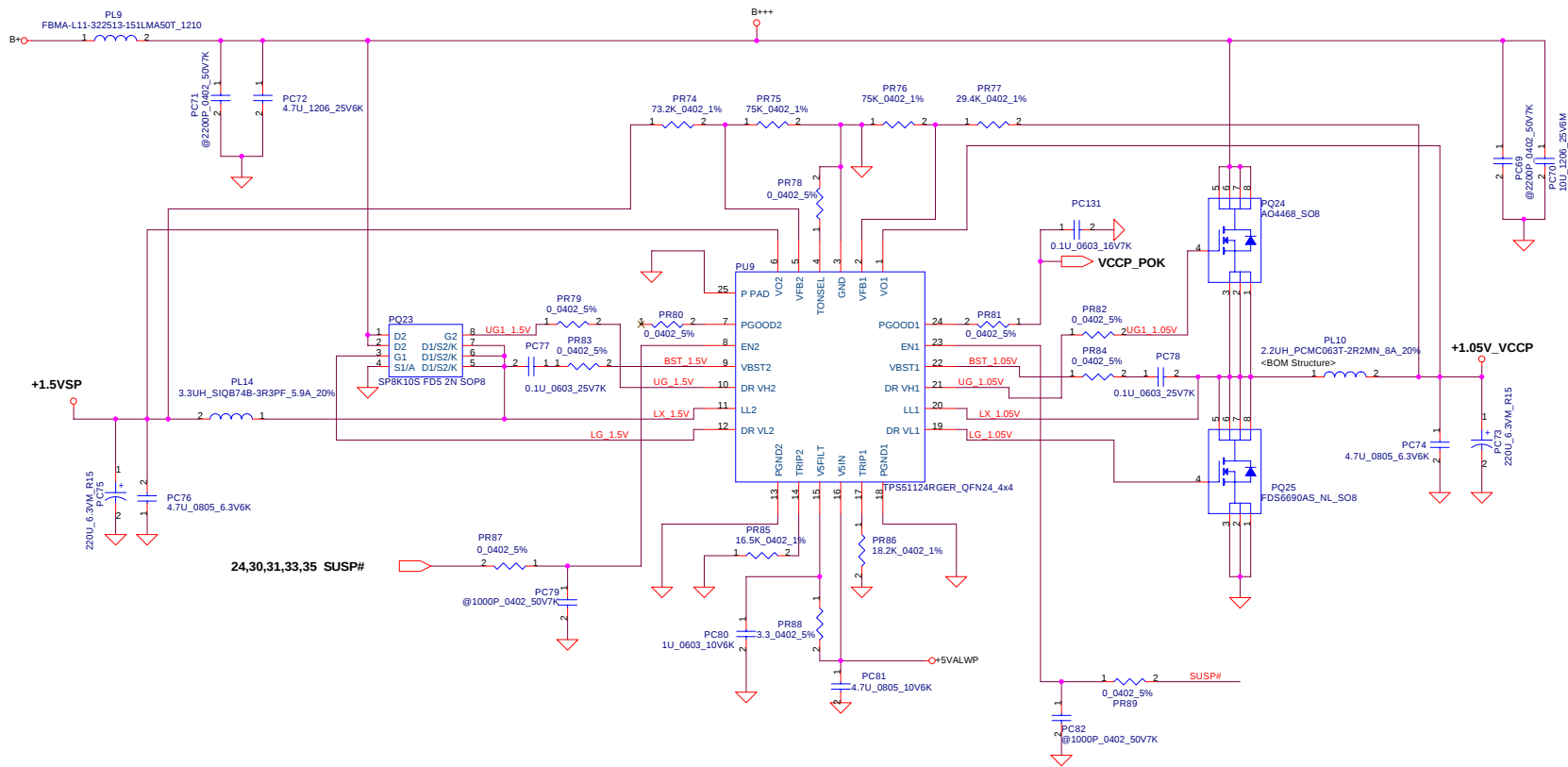
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DC CONN

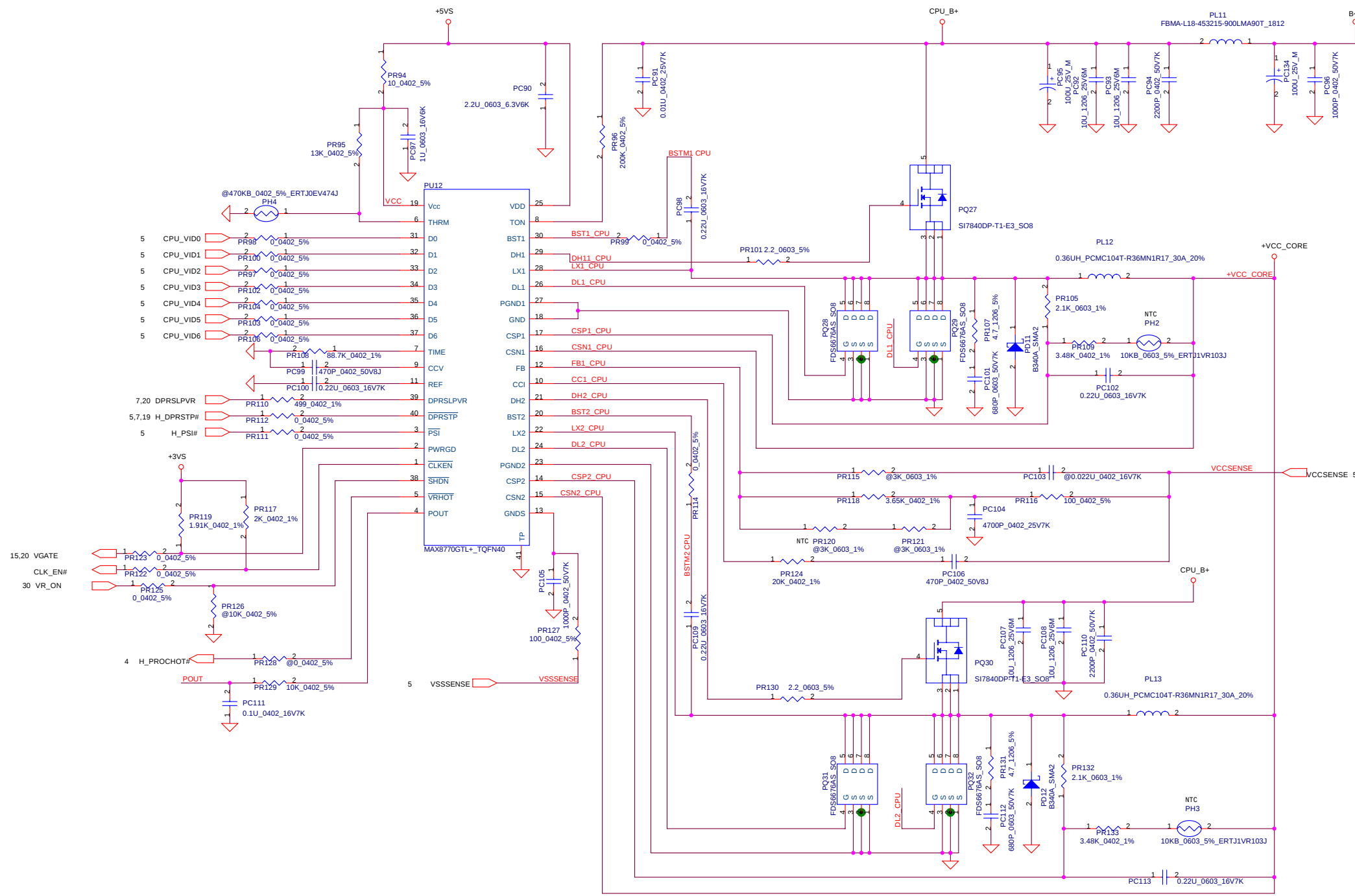


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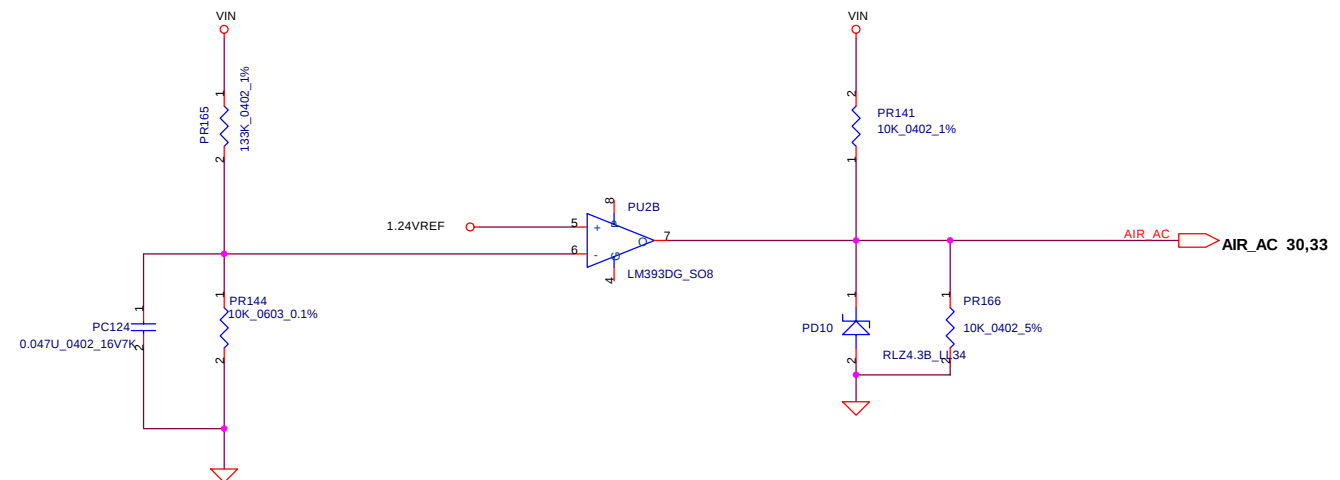
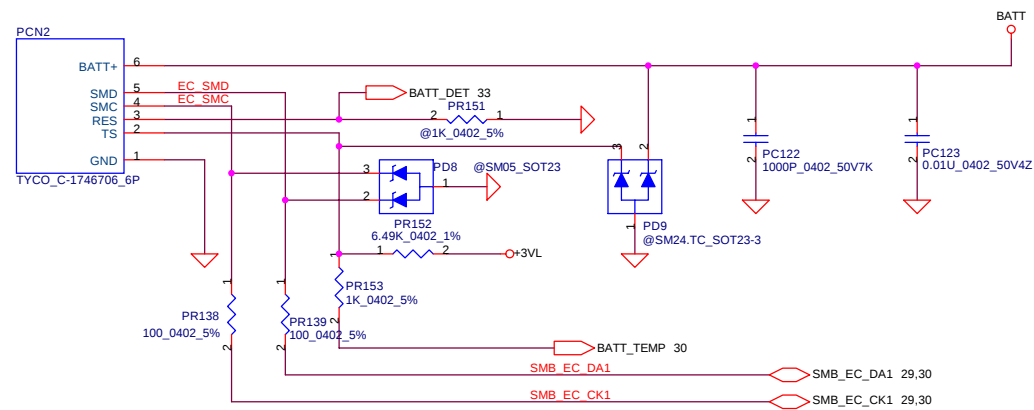


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Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page	Date	Phase
1	Change C117 from 220uF to 10uF.	10	2/8	DB --> SI
2	Remove R401.	19	2/5	DB --> SI
3	Change Crystal Y2 type (the same as Abita).	19	2/5	DB --> SI
4	Connect LAN_RST# from EC_RAMRST# to GND.	20	2/5	DB --> SI
5	Change ODD connector type.	22	2/13	DB --> SI
6	Change U11 power from +5VS to +5VALW.	24	2/12	DB --> SI
7	Change U11 enable signal from SLP_S3# to SUSP#.	24	2/8	DB --> SI
8	Reverse JP19 USB Connector and need to double check layout symbol.	27	2/12	DB --> SI
9	Change Power and Battery charge LED power from +3VALW to +5VALW.	28	2/8	DB --> SI
10	Change HDD LED power from +3VS to +5VS.	28	2/8	DB --> SI
11	Delete reserve component (D25 BSW2) for 14.1".	28	2/8	DB --> SI
12	Change R329, R333, R470 from 200 ohm to 470 ohm.	28	2/8	DB --> SI
13	Change R334, R339 from 200 ohm to 820 ohm.	28	2/8	DB --> SI
14	Add pull down resistor R402 (100k ohm) for SUSP#.	30	2/5	DB --> SI
15	Change C44, C49 type from DIP to SMD.	06	2/14	DB --> SI
16	Add R402 pull high resistor for LID_Sw#.	30	2/14	DB --> SI
17	Add R403 pull high resistor for WL_BTN#.	30	2/14	DB --> SI
18	Delete D19.	28	2/16	DB --> SI
19	Change R300 from 10 ohm to 47 ohm and C374 from 10pF to 33pF.	24	2/16	DB --> SI
20	Delete JP27, R317, C392.	26	2/16	DB --> SI
21	Delete R297.	24	2/16	DB --> SI
22	Change RTC battery and connector.	19	2/26	DB --> SI
23	Change C413 and 414 package from 0603 to 0402.	28	2/26	DB --> SI
24	Add JP28 for USB card reader.	27	2/28	DB --> SI
25	Change R105 from 22 ohm to 0 ohm.	15	3/1	DB --> SI
26	Delete C49 and remount C46.	06	3/1	DB --> SI
27	Change JP16 and JP17 Audio Jack.	26	3/2	DB --> SI
28	Add R405.	04	3/6	DB --> SI
29	Change USB connector (JP19) type.	27	3/8	DB --> SI

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Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page	Date	Phase
1	Connect R323.1 from B+ to +3VALW. (Cancel in 4/24)	26	4/9	SI --> PV
2	Add R406 between H_OUT_R and H_OUTR+, R407 between H_OUT_L and H_OUTL+	26	4/9	SI --> PV
3	Swap channel L and R.	26	4/9	SI --> PV
4	Add R408 and R409. (Cancel in 4/24)	26	4/9	SI --> PV
5	Reverse JP22 pin define.	28	4/10	SI --> PV
6	Change R360 from 10K to 4.7K ohm for KB926 C0 version.	31	4/10	SI --> PV
7	Reserve C438 for KB926 C0 version.	31	4/10	SI --> PV
8	Change C45-C48 to 9m ohm and reserve C49.	06	4/16	SI --> PV
9	Change R233 from 0 ohm to 10K ohm.	20	4/16	SI --> PV
10	Change R233 from 0 ohm to 10K ohm.	30	4/16	SI --> PV
11	Reverse JP15 pin define.	26	4/16	SI --> PV
12	Add pull high R410 (3.3K ohm) for HOLD#.	29	4/17	SI --> PV
13	Change R211 from 24.9 to 27.4 ohm.	19	4/17	SI --> PV
14	Add CP1-CP6 for EMI.	30	4/17	SI --> PV
15	Add R186 and C261 for EMI.	18	4/17	SI --> PV
16	Add R292 and C356 for EMI.	23	4/17	SI --> PV
17	Add D24 for EMI.	28	4/17	SI --> PV
18	Add C233, C234, C235 for EMI.	16	4/17	SI --> PV
19	Add R411 to pull high for WL_LED#.	22	4/17	SI --> PV
20	Remove XDP circuit for EMI request. Change R2 to 15 ohm R3 to 39 ohm R7 to 560 ohm R8 to 27 ohm	04	4/17	SI --> PV
21	Change R223 from 1K to 10K ohm when remove XDP.	20	4/17	SI --> PV
22	Add reserve resistor R412 for LPC debug port.	15	4/17	SI --> PV
23	Add C439 to avoid wavelike display.	10	4/20	SI --> PV
24	Change C262 and C263 from 15pF to 12pF.	19	4/23	SI --> PV
25	Per ENE request, change C426 and C427 from 10pF to 27pF from now.	30	4/23	SI --> PV
26	Reserve R300 and C374 for EMI request.	24	4/24	SI --> PV
27	Add C440 for AC_IN.	31	4/24	SI --> PV
28	Change R355 from 8.2K to 18K ohm.	31	4/25	SI --> PV
29	Add L16-19 for EMI request.	26	4/25	SI --> PV
30	Change C336-C338 from 22p to 10pF.	16	4/25	SI --> PV
31	Add R415 and R416 for thermal second solution.	04	4/25	SI --> PV
32	Change R320 from 0 ohm to bead. Add L20.	26	4/25	SI --> PV
33	Change R321 and R322 from 0 ohm to bead. Add C398 and C399.	26	4/25	SI --> PV
34	Add C401 and C404.	26	4/25	SI --> PV
35	Connect AIR_AC to U18 pin85 to support AIR adapter.	31	4/26	SI --> PV
36	Add C441.	15	4/26	SI --> PV
37	Add R417 and R418 to fine tune Headphone output voltage	26	4/26	SI --> PV
38	Delete R219 and C268 for EMI request.	20	4/26	SI --> PV

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