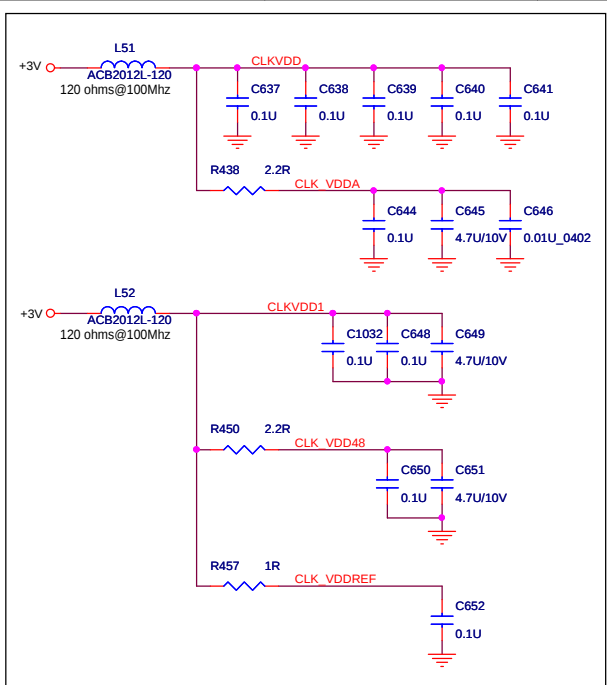


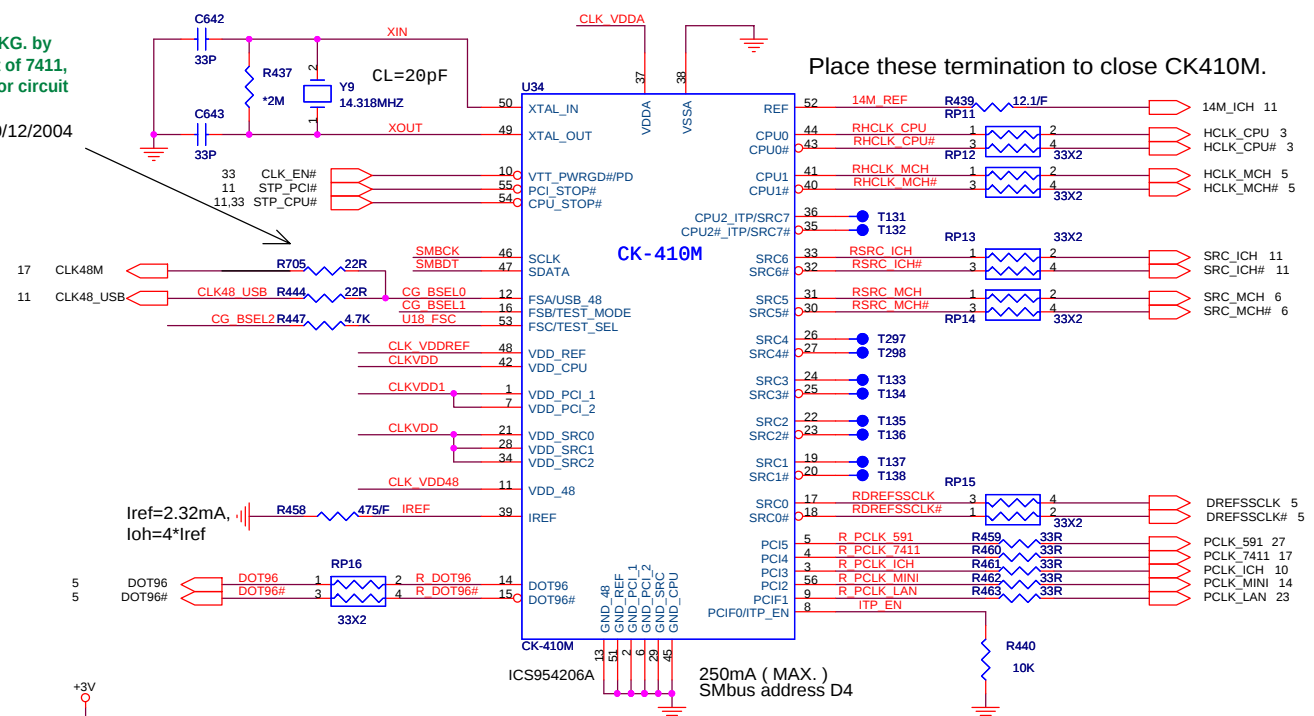
MODEL	REV	CHANGE LIST	Model	CT3/5 MB BOARD	
			Page	FROM	TO
CT3/5 MB 31CT3MB0015 31CT3MB0031	1A	PAGE 2 --- Enable CLK48M from cloc k generator for the PLL circuit of 7411, and disable the ocsillator circuit of PCI7411 PLL. PAGE 3 --- Remove H/W shutdown circuit that supported ADM1032. PAGE 4 --- Use X7R type to replace Y5V type for CPU Decoupling/Bypass capacitor. PAGE 10 --- Add a terminal resistor R706 for -CODE_RST# to improve signal quality. PAGE 11 --- 1. Add a 10K pull-up resistor on MCH_SYNC# for booting. 2. Change the power plane of PCIE_WAKE# from 3VSUS to 3V_S5 to solve system can't turn off issue. 3. Change the power plane of ICH_THRM# and SCI_# from 3VSUS to +3V to reduce leakage. PAGE 12 --- We can also use 5VSUS to instead of 5V_S5 to save cost of MOSFET(A06402). PAGE 15 --- Add a level-shift cicuit for EDID interface. PAGE 17 --- 1. Add a off-page and a EMI solution for CLK48M. 2. Remove the reserve resistors (R693~R695) of parallel interface for PCI1510. PAGE 18 --- Remove R696, connect controller and power switch directly . PAGE 19 --- Change R682&R683 value from 56 ohms to 0 ohm cause of BOM error at A-test. PAGE 22 --- 1. Change MC3 type from Y5V to X7R to improve singal quality. 2. Connect H1/H3 to AGND via a 0 ohm resistor by Conexant's comment. PAGE 23 --- 1. Add a terminal resistor R707 for RTL8100/8110 id selection. 2. Add a 0.1uF to make Q40 turn on slowly to aviod 3VPCU drop issue. PAGE 24 --- Modified transformer circuit cause of CT can't connect each other on 10/100M application. PAGE 26 --- Add a flashrom as PLCC32 type for BIOS debugging. PAGE 27 --- 1. Change R352 value from 120K ohms to 20M ohms. 2. Add a LPC debug port for software team to debug convenient. PAGE 30 --- Add GMT fan controller for B-test to costdown. PAGE 31 --- 1. Add ESD protection circuit for S-VIDEO signal to Docking. 2. Add R713 to enable the mux in the Tampa-2 cable PAGE 33 --- Change PR143 value from 100K to 10K to solve display abnormal issue. PAGE 35 --- 1. Move 5V_S5 circuit to Page 36. 2. De-popuplate PQ129 and PR182. 3. Change PR178 value from 22 ohm to 47 ohm. PAGE 36 --- Remove PC170 and PQ127 but reserve 5V_S5 power circuit.	1	1A	
			2	1A	2A
			3	1A	2A
			4	1A	2A
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	2A
			11	1A	2A
			12	1A	2A
			13	1A	
			14	1A	
			15	1A	2A
			16	1A	
			17	1A	2A
			18	1A	2A
			19	1A	2A
			20	1A	
			21	1A	
			22	1A	2A
			23	1A	2A
			24	1A	2A
			25	1A	
			26	1A	2A
			27	1A	2A
			28	1A	
			29	1A	
			30	1A	2A
			31	1A	2A
			32	1A	
			33	1A	2A
			34	1A	
			35	1A	2A
			36	1A	2A
			37	1A	
			38	1A	
			39	1A	

MODEL	REV	CHANGE LIST	Model	CT3/5 MB BOARD	
			Page	FROM	TO
CT3/5 MB 31CT3MB0015 31CT3MB0031	2A	PAGE 2 --- 1. Add C1048 for CLK48M to get better EMI performance. PAGE 3 --- 1. Add R733 as pull-up resistor for PREQ#. PAGE 11 --- 1. Add RF_OFF# and BT_OFF# circuit. PAGE 17 --- 1. Populate R704 and C1046 to get better EMI performance. 2. Remove R701 & R702 for unused PCI1510RVGF circuit. PAGE 18 --- 1. Disconnect SM_PHYS_WP on controller side. 2. Tie SM_EL_WP with SM_PHYS_WP on conn side to allow for normal operation of SD and SM. 3. Add a discharge circuit for media card power. 4. Add R718 to solve cross-talk issue of MS-Pro card. 5. Add R717 to solve SM card can't write protect issue. 6. Add R719~R736 as terminal on all multi-function pins. 7. Add pull-up circuit. PAGE 27 --- 1. Reserve 0R for RF_OFF# and BT_OFF# circuit. 2. Modify LPC pin name. PAGE 28 --- 1. Change HDD and ODD select definition. PAGE 30 --- Adjust Capacitors and Bead to improve CRT timing issue. 1. Change L66, L67, L68 from BK1608HM470 to 0R. 2. Remove C931, C932, C933. 3. Change C934, C935, C936 from 22P to 5.6P. 4. Change C6, C14, C350 from 10P to 5.6P. 5. Change L1, L26, L27 from BK1608HM470 to BLM18BA750SN1T. PAGE 31 --- 1. Change L5,L6,L7,C57,C58,C64,C77,C113,C121 value to improve S-video quality. 2. Reserve S-video impedance match circuit.	1	1A	
			2	2A	3A
			3	2A	3A
			4	2A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	2A	
			11	2A	
			12	1A	
			13	1A	
			14	1A	
			15	2A	
			16	1A	
			17	2A	3A
			18	2A	3A
			19	2A	
			20	1A	
			21	1A	
			22	2A	
			23	2A	
			24	2A	
			25	1A	
			26	2A	2A
			27	2A	
			28	1A	2A
			29	1A	
			30	2A	
			31	2A	
			32	1A	
			33	2A	
			34	2A	
			35	2A	
			36	2A	
			37	2A	
			38	2A	
			39	2A	



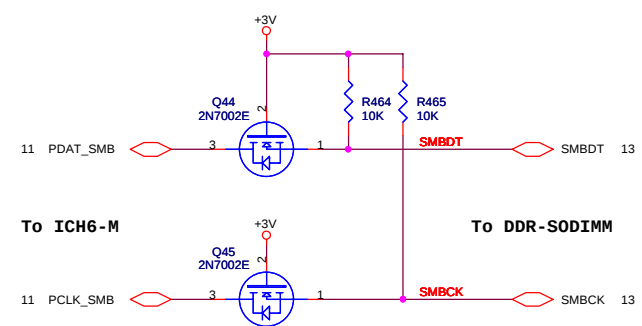
SI stage:
Enable CLK48M from CKG. by
R705 for the PLL circuit of 7411,
and disable the oscillator circuit
at PCI7411 side.

Sting 10/12/2004



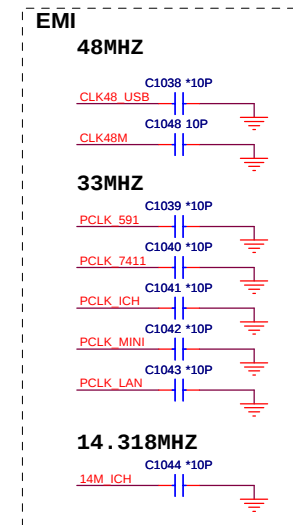
FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	DOOTHAN FSB 400
0	0	1	133	100	33	DOOTHAN FSB 533
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	RESERVED			

* Frequency select by CPU auto sense.

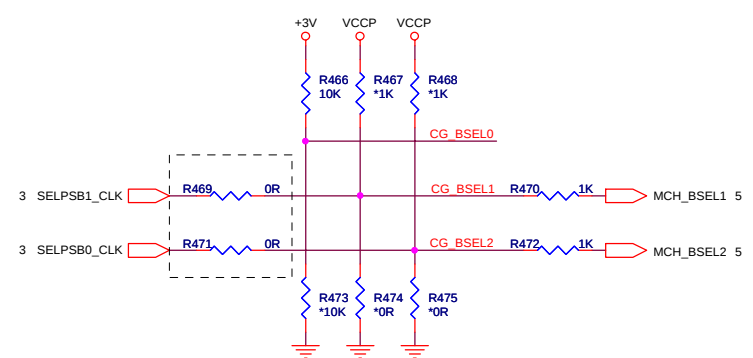
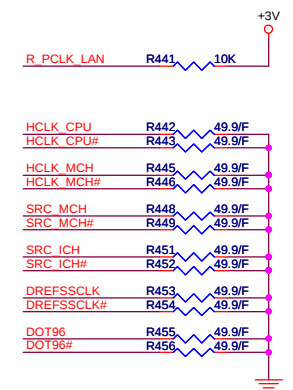


PV stage:
Add C1048 for CLK48M to get better EMI
performance.

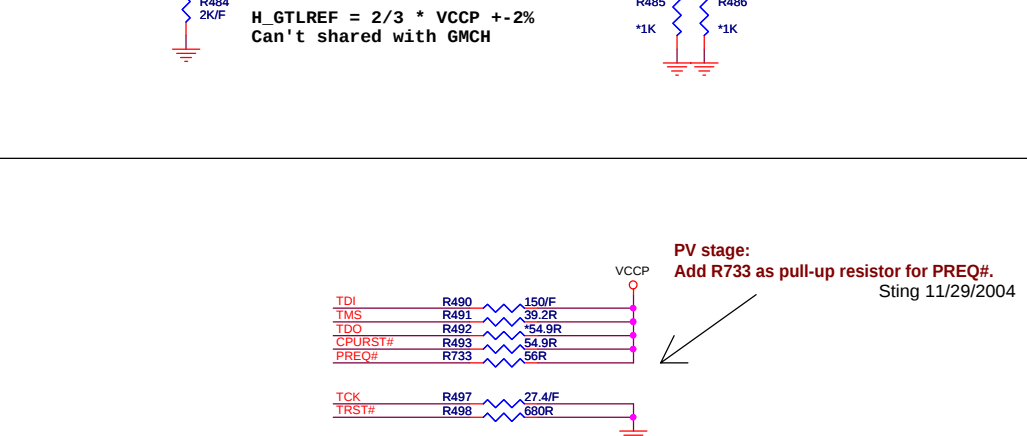
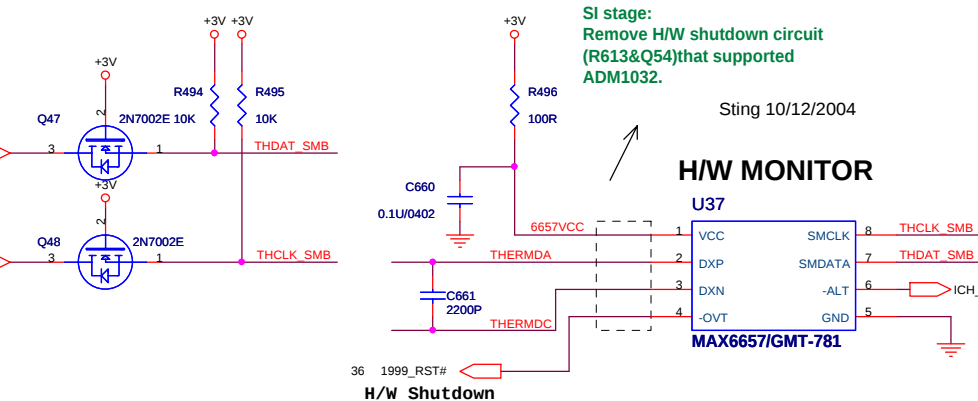
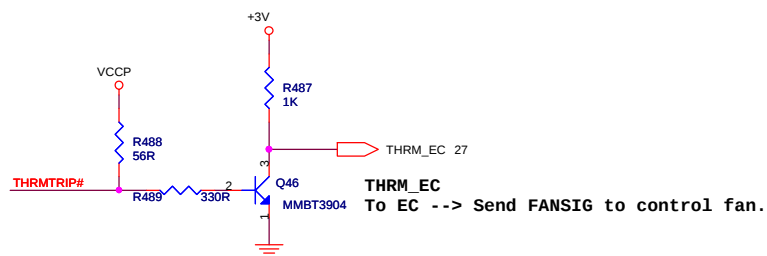
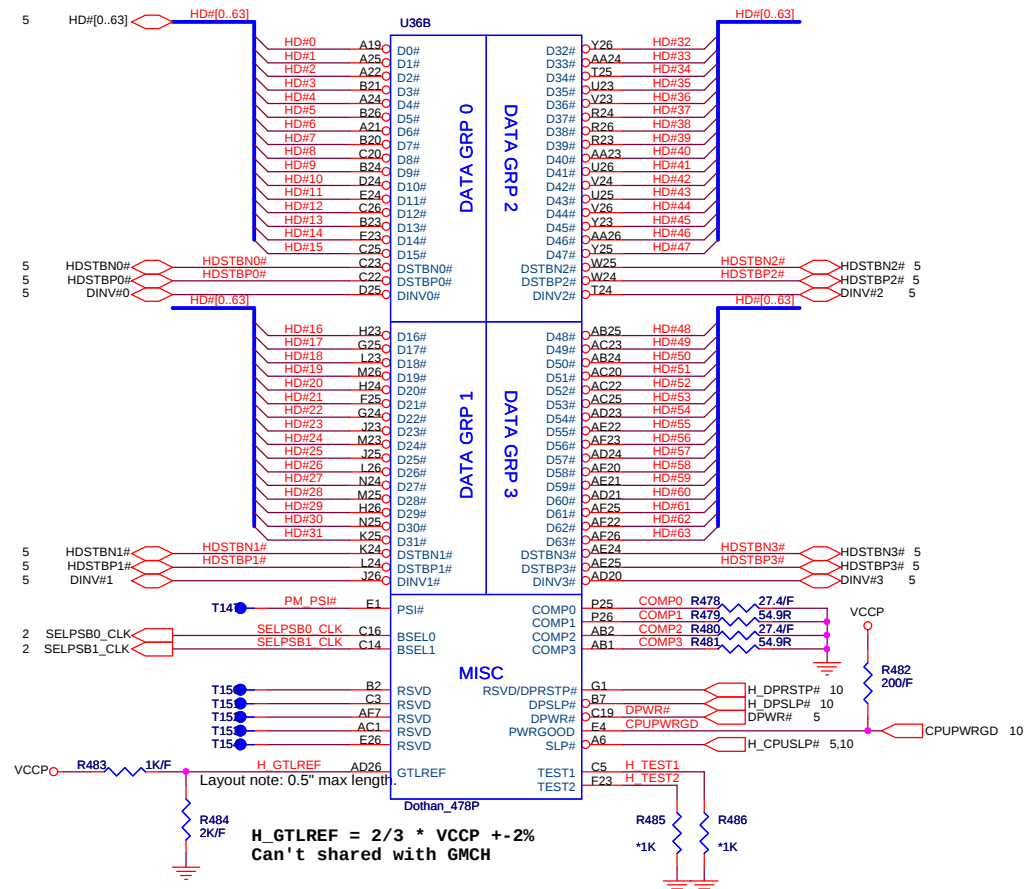
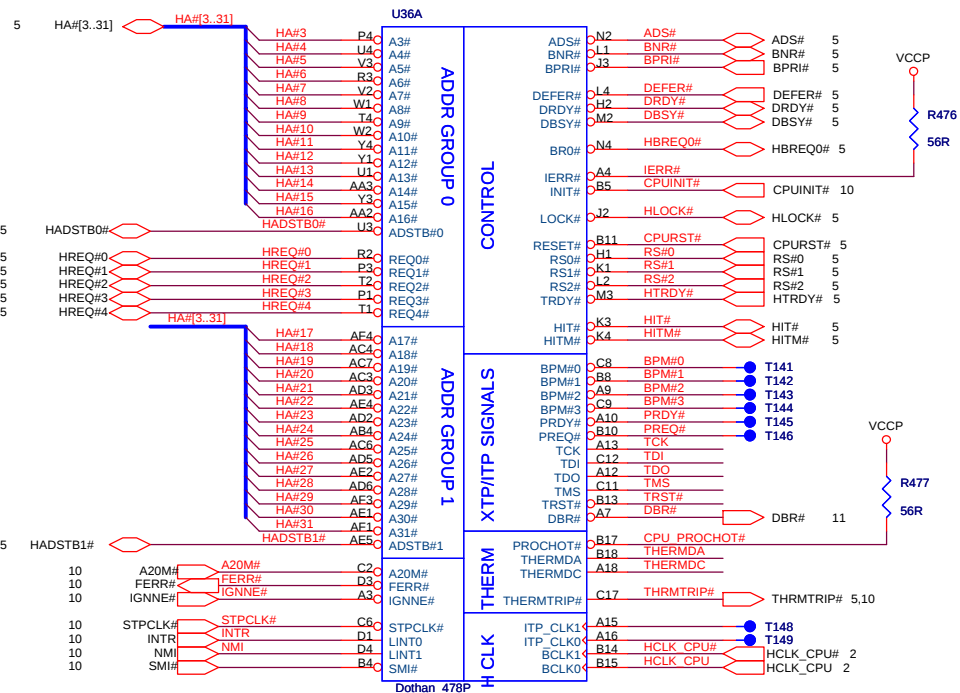
Sting 11/29/2004



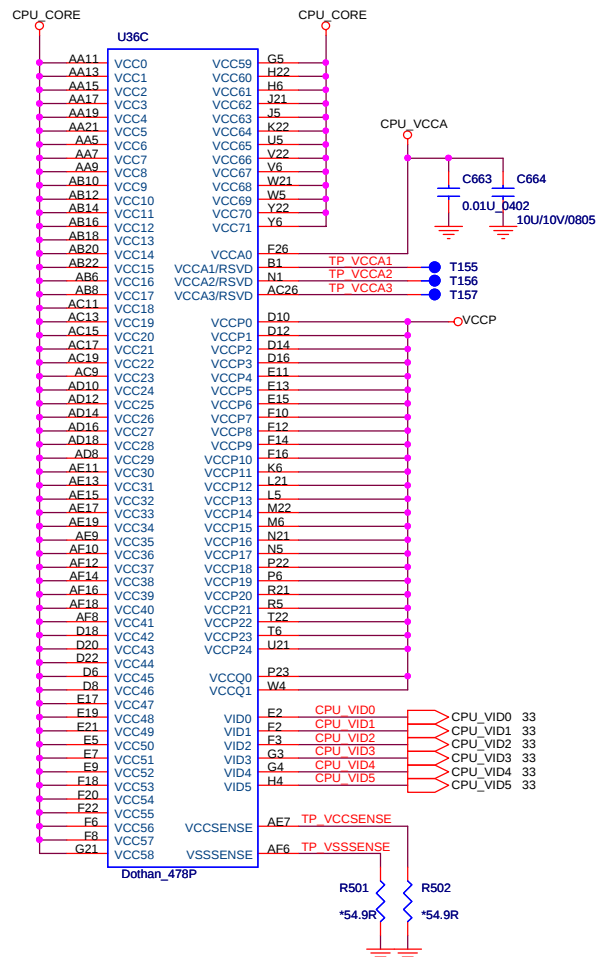
R_PCLK_LAN ITP_EN
0: SRCCLK=96MHZ 0: SRC_7 Pair
1: SRCCLK=100MHZ 1: CPU_2 ITP Pair



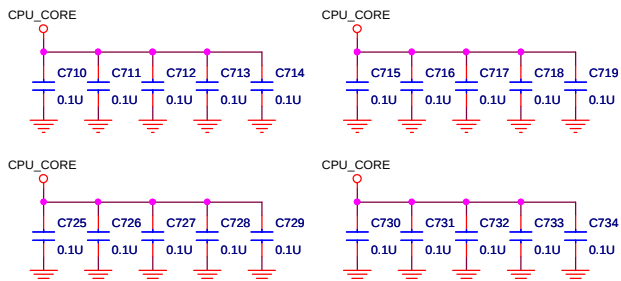
R469,R471
Dothan-A can remove so that the FSB frequency will be selected by
hardware setting(R474,R475,R467,R468).
Dothan-B should be populated.



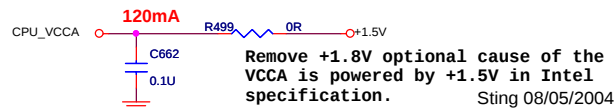
ICH_THRM#
To SB --> System throttling



CPU de-coupling capacitor

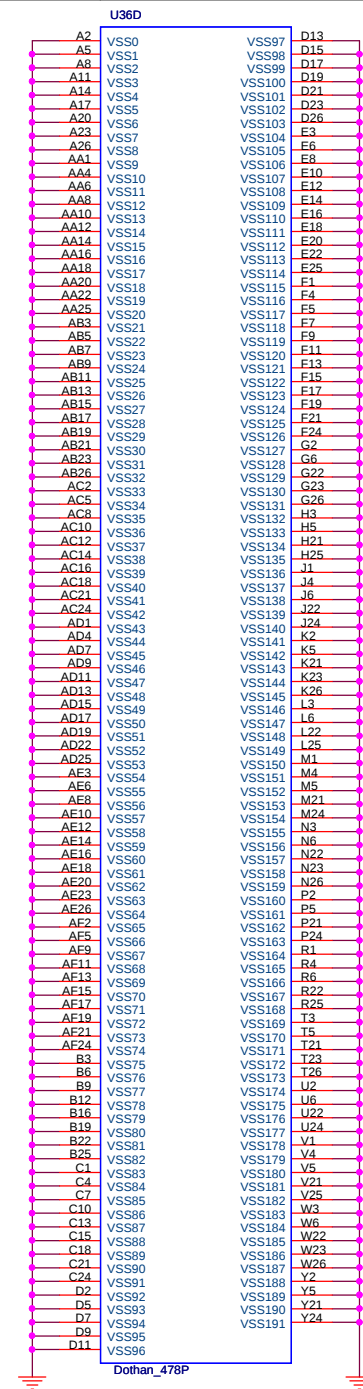
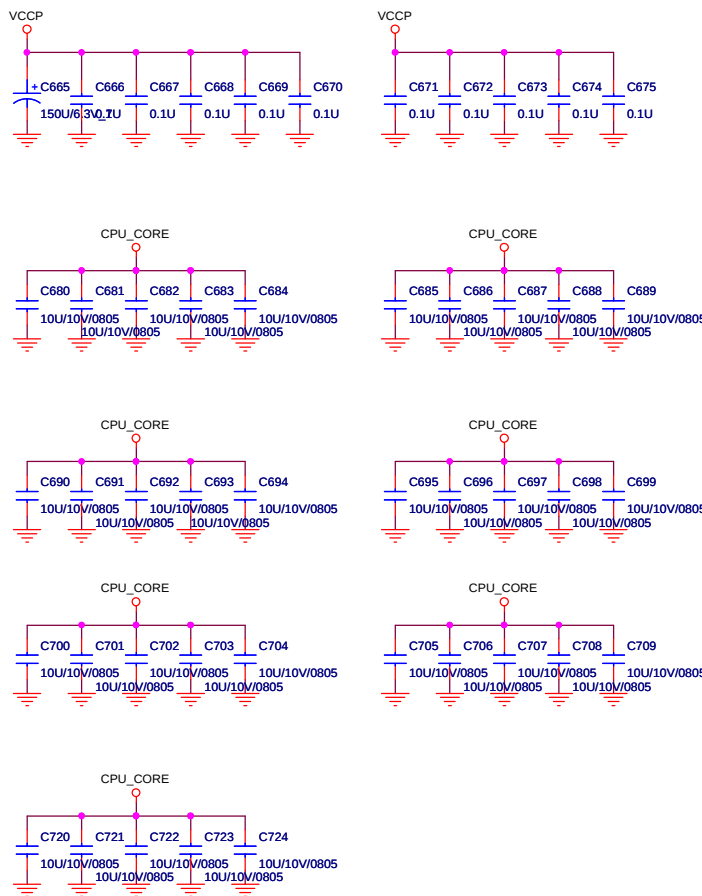


**CPU Bypass
capacitor**



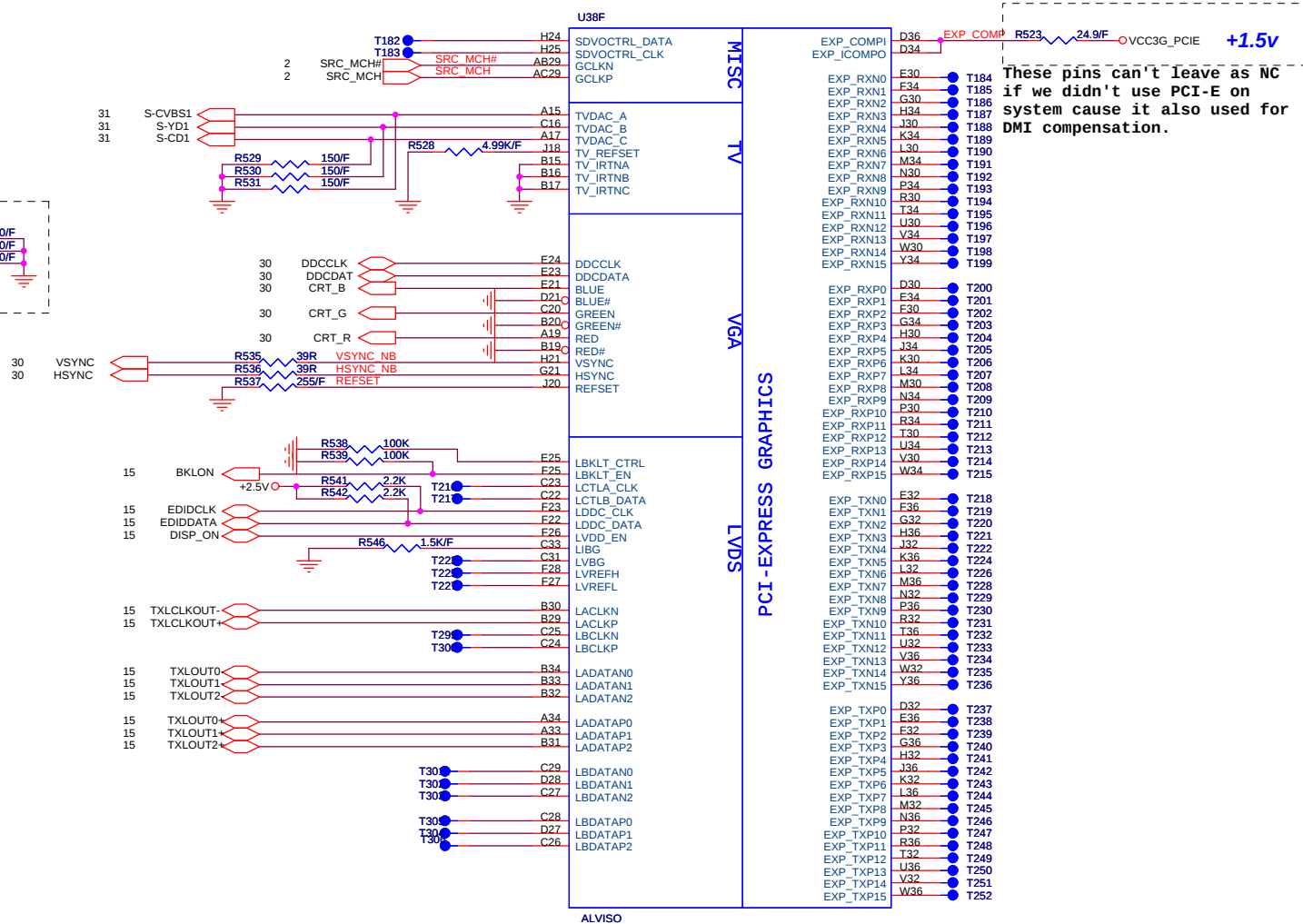
SI stage:
Use X7R type to replace Y5V type
for Decoupling/Bypass capacitor.

Sting 10/12/2004

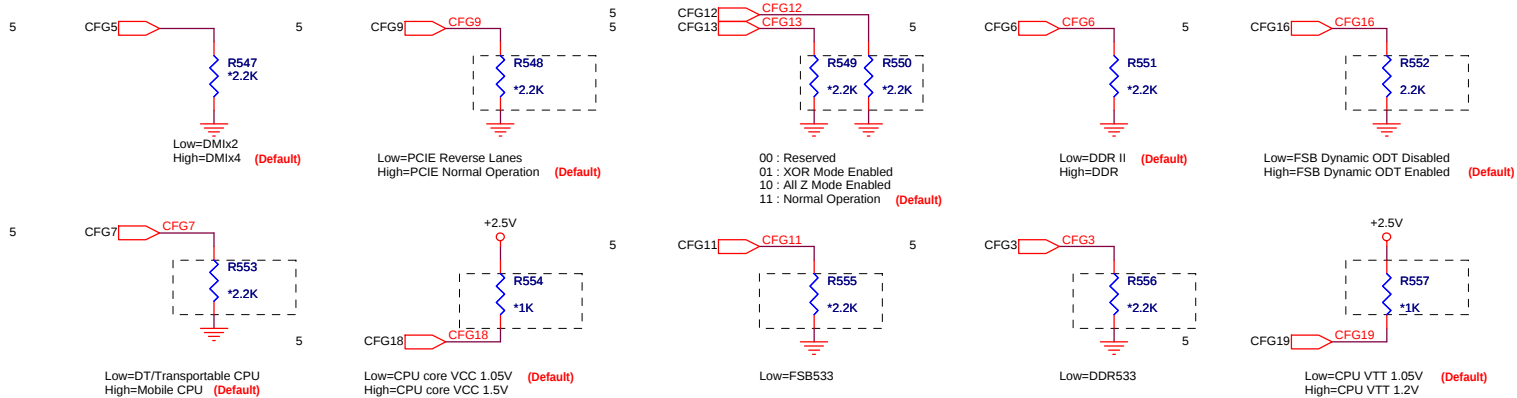


PROJECT : CT3
Quanta Computer Inc.

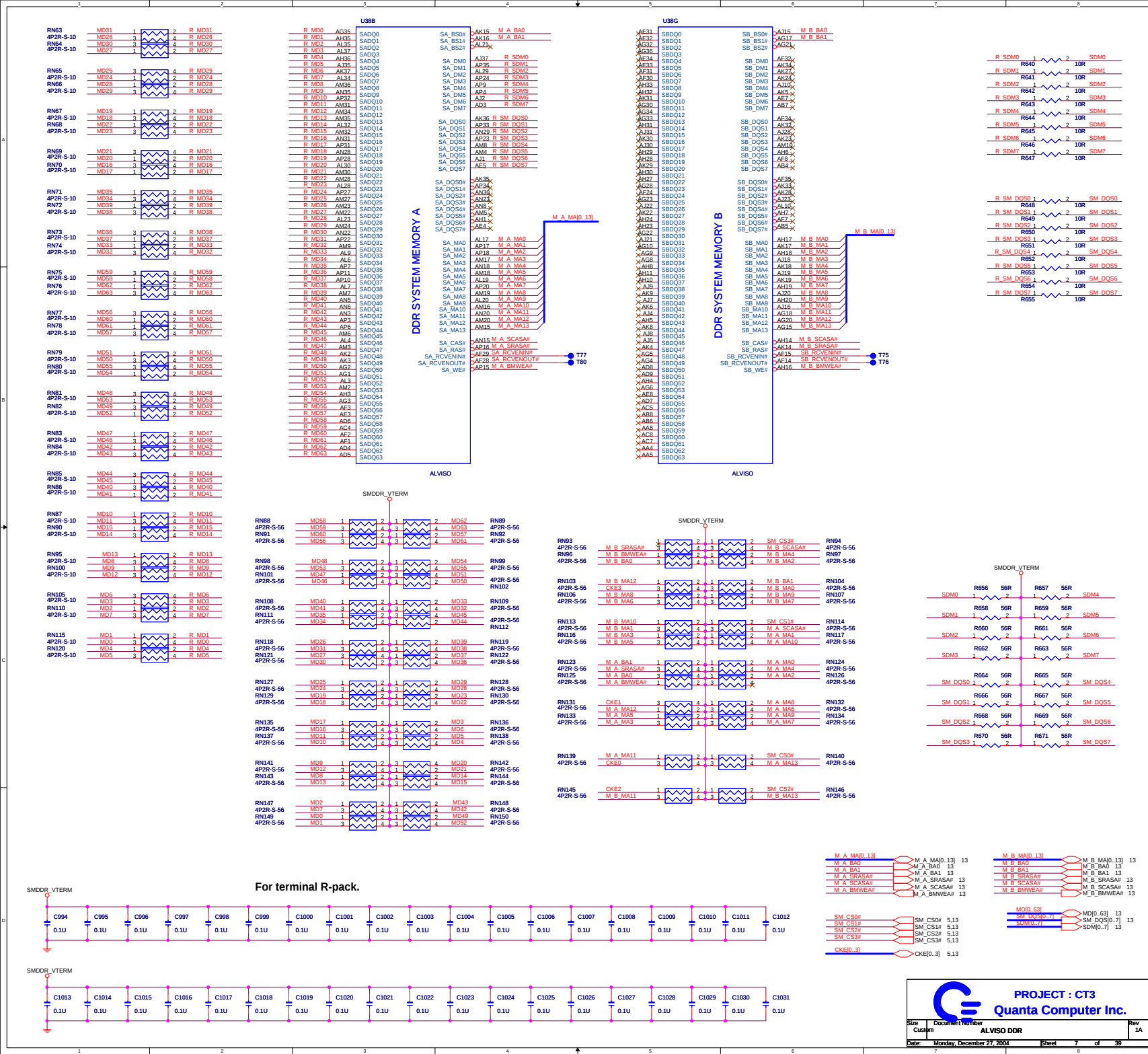
Size	Document Number	Rev
Custom	CPU POWER / GND	2A
Date:	Monday, December 27, 2004	Sheet 4 of 39



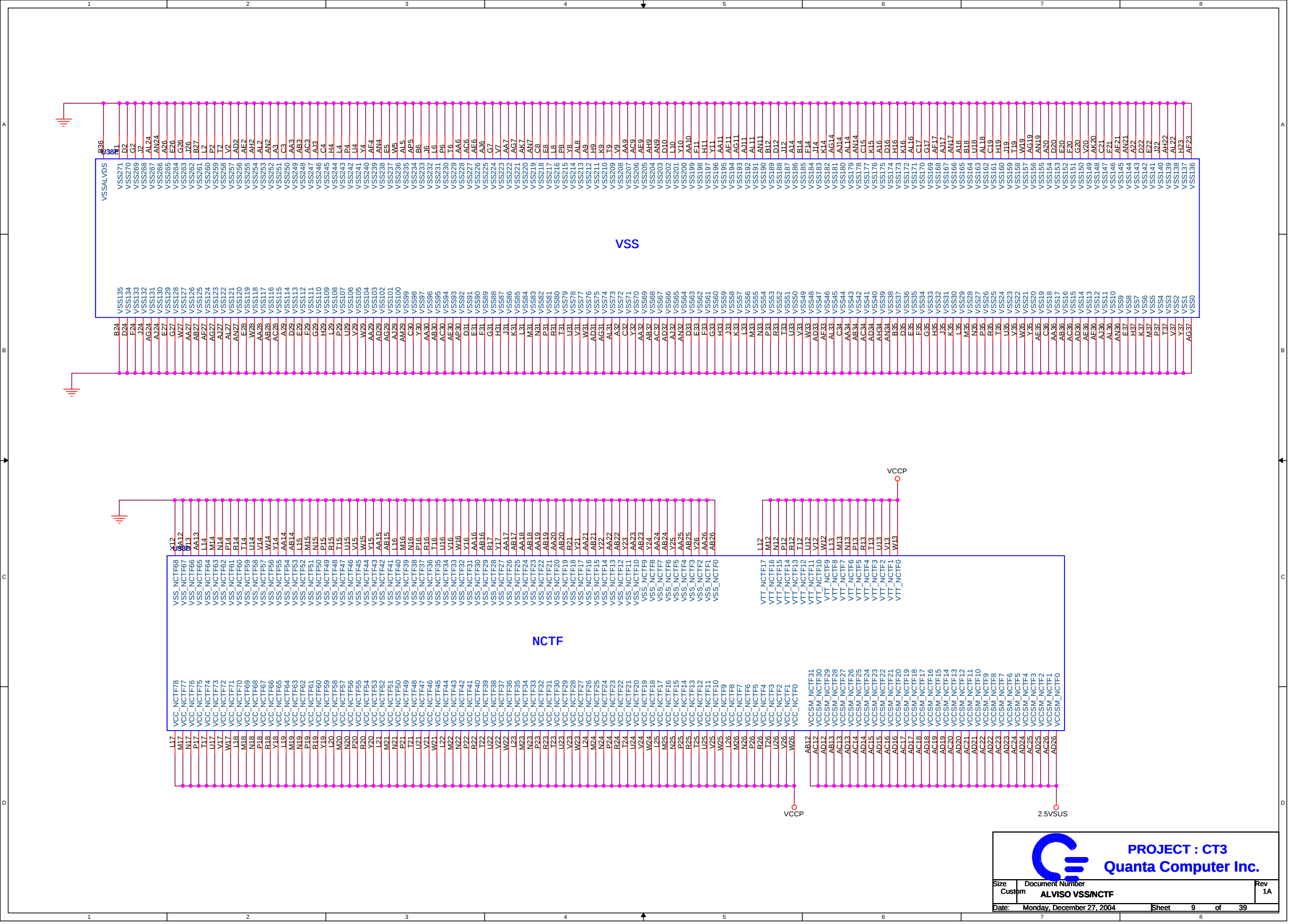
Strapping

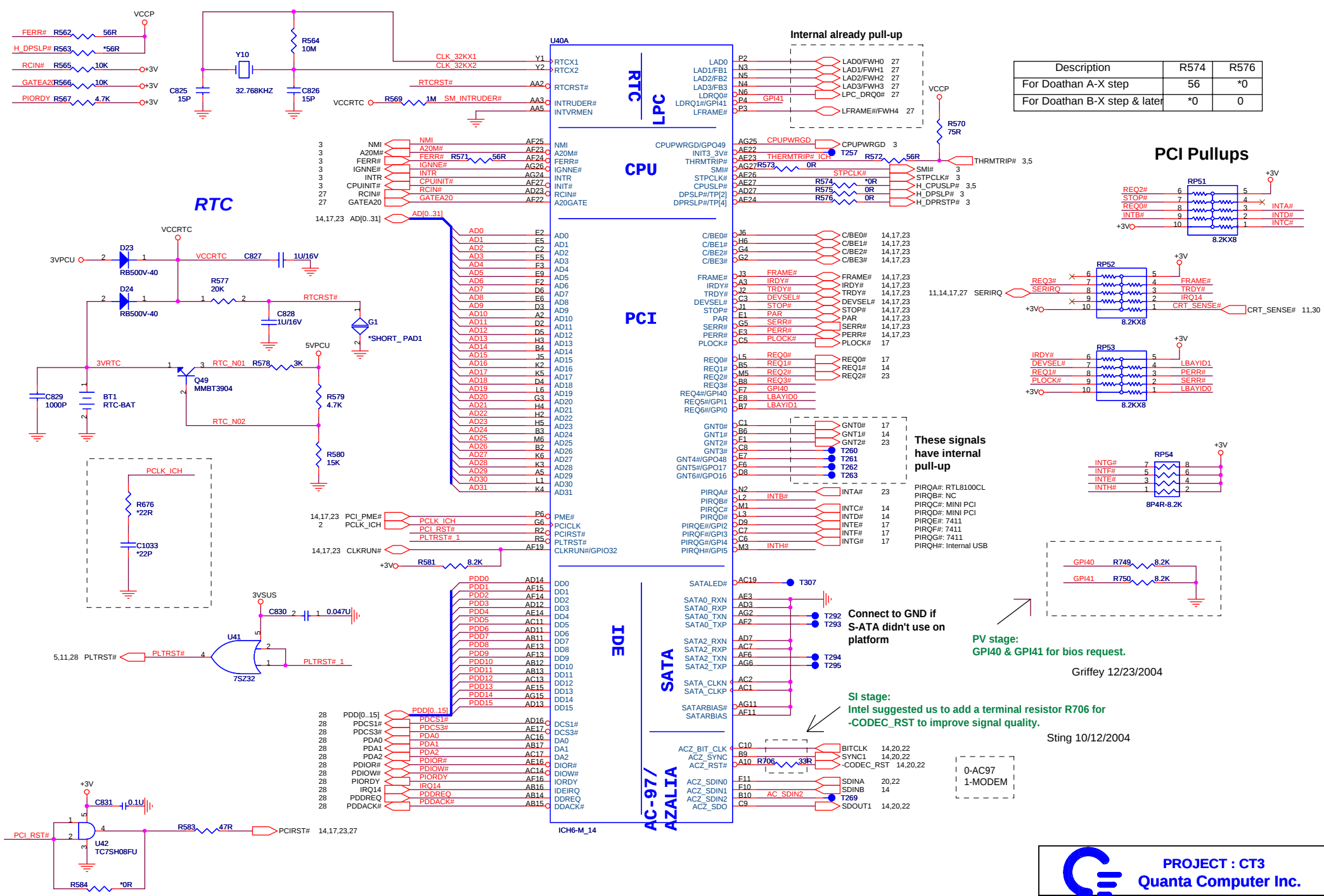


CFG[2:0]
001=533MT/S FSB
101=400MT/S FSB
CFG[3:17] have internal pullup.
CFG[18:19] have internal pulldown.



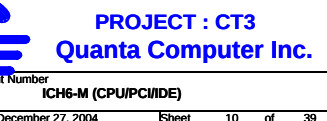
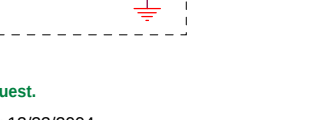
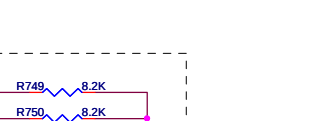
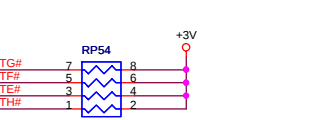
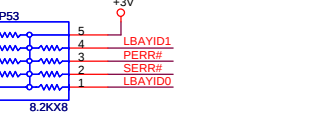
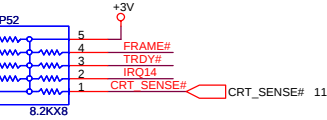
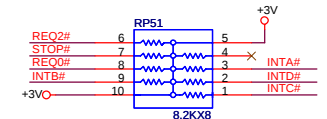
For terminal R-pack.





Description	R574	R576
For Doathan A-X step	56	*0
For Doathan B-X step & later	*0	0

PCI Pullups



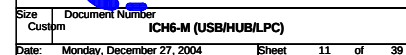
These signals have internal pull-up

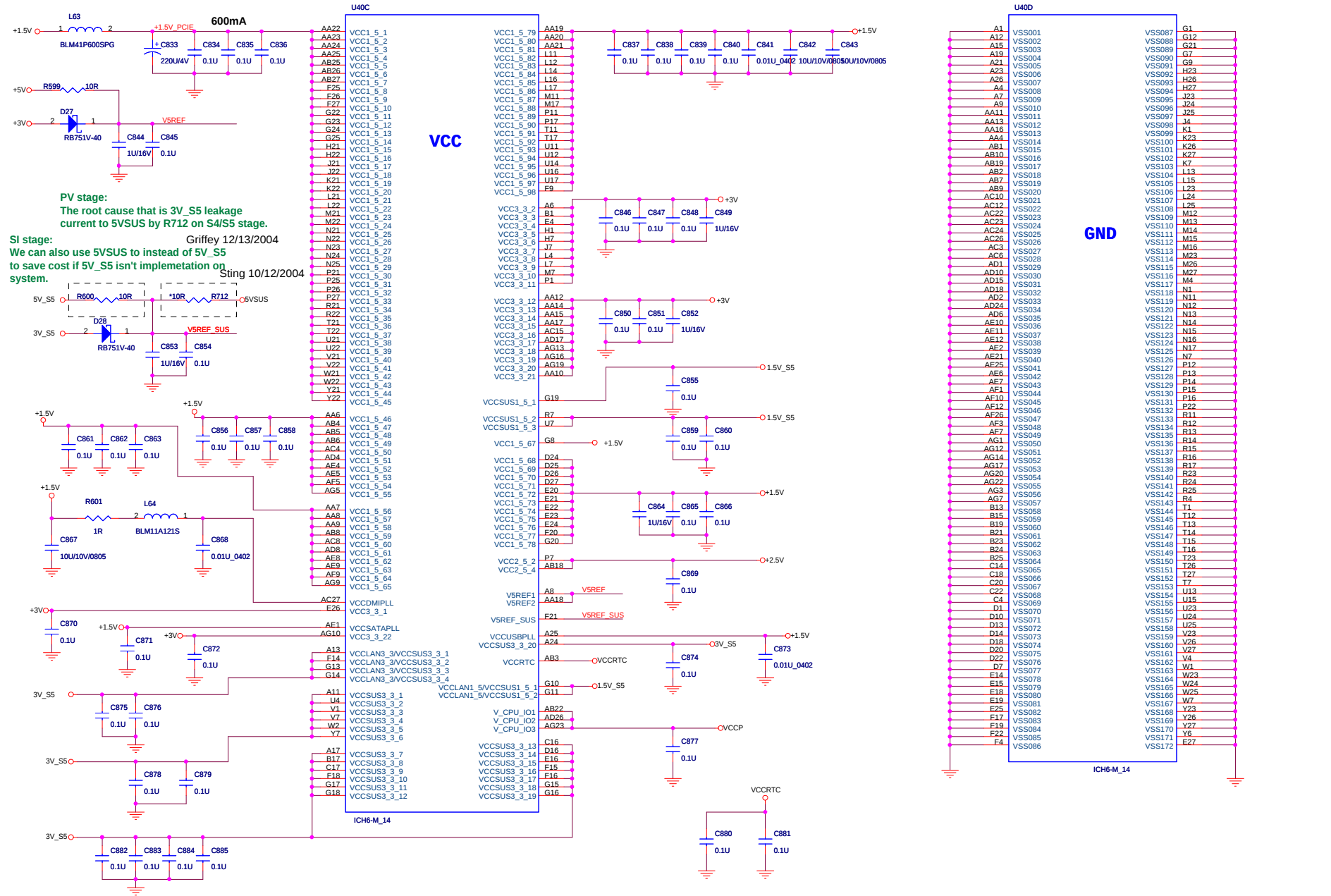
- PIRQA#: RTL8100CL
- PIRQB#: NC
- PIRQC#: MINI PCI
- PIRQD#: MINI PCI
- PIREQ#: 7411
- PIRQF#: 7411
- PIRQG#: 7411
- PIRQH#: Internal USB

Connect to GND if S-ATA didn't use on platform

SI stage: Intel suggested us to add a terminal resistor R706 for -CODEC_RST to improve signal quality.

Sting 10/12/2004

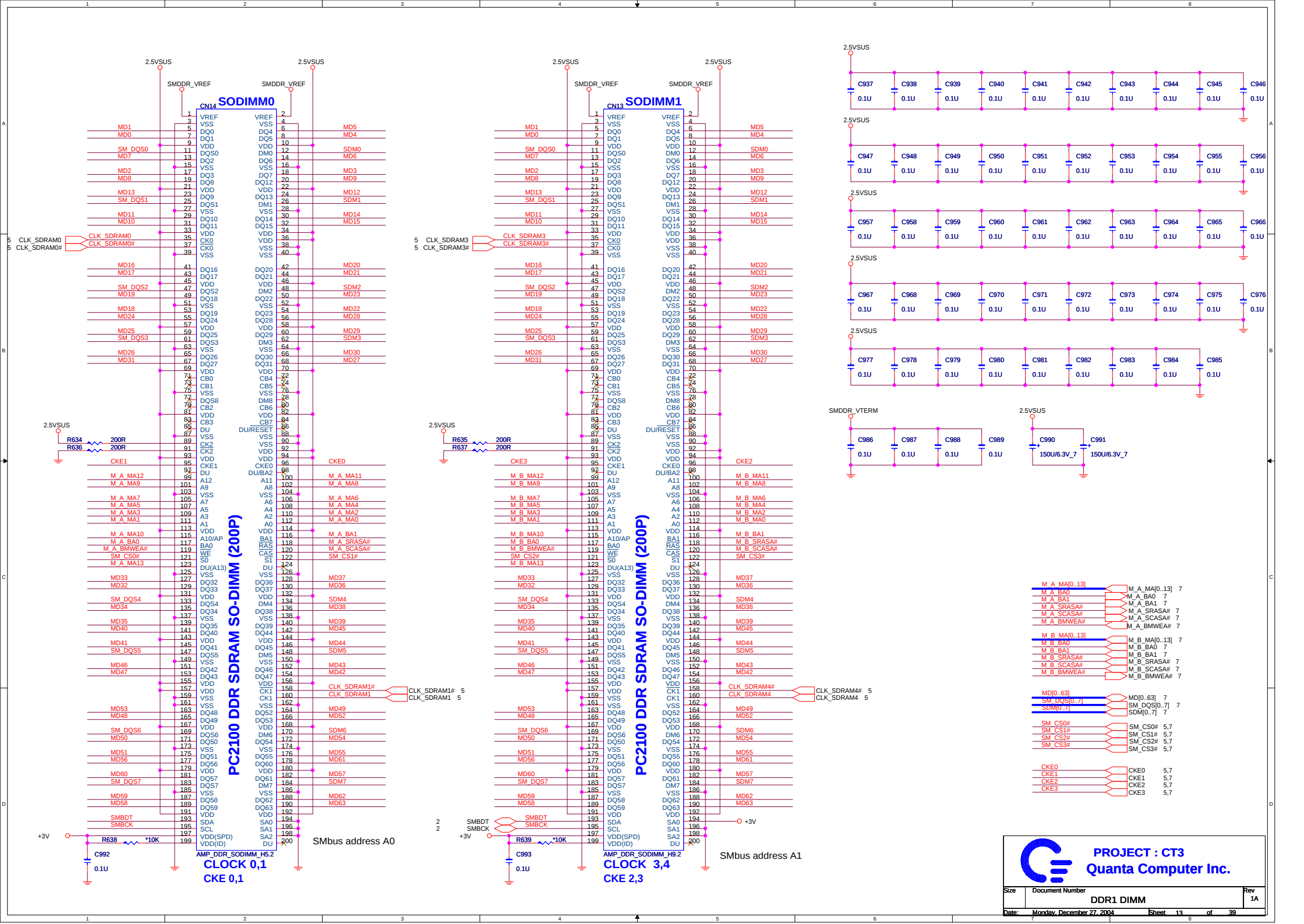




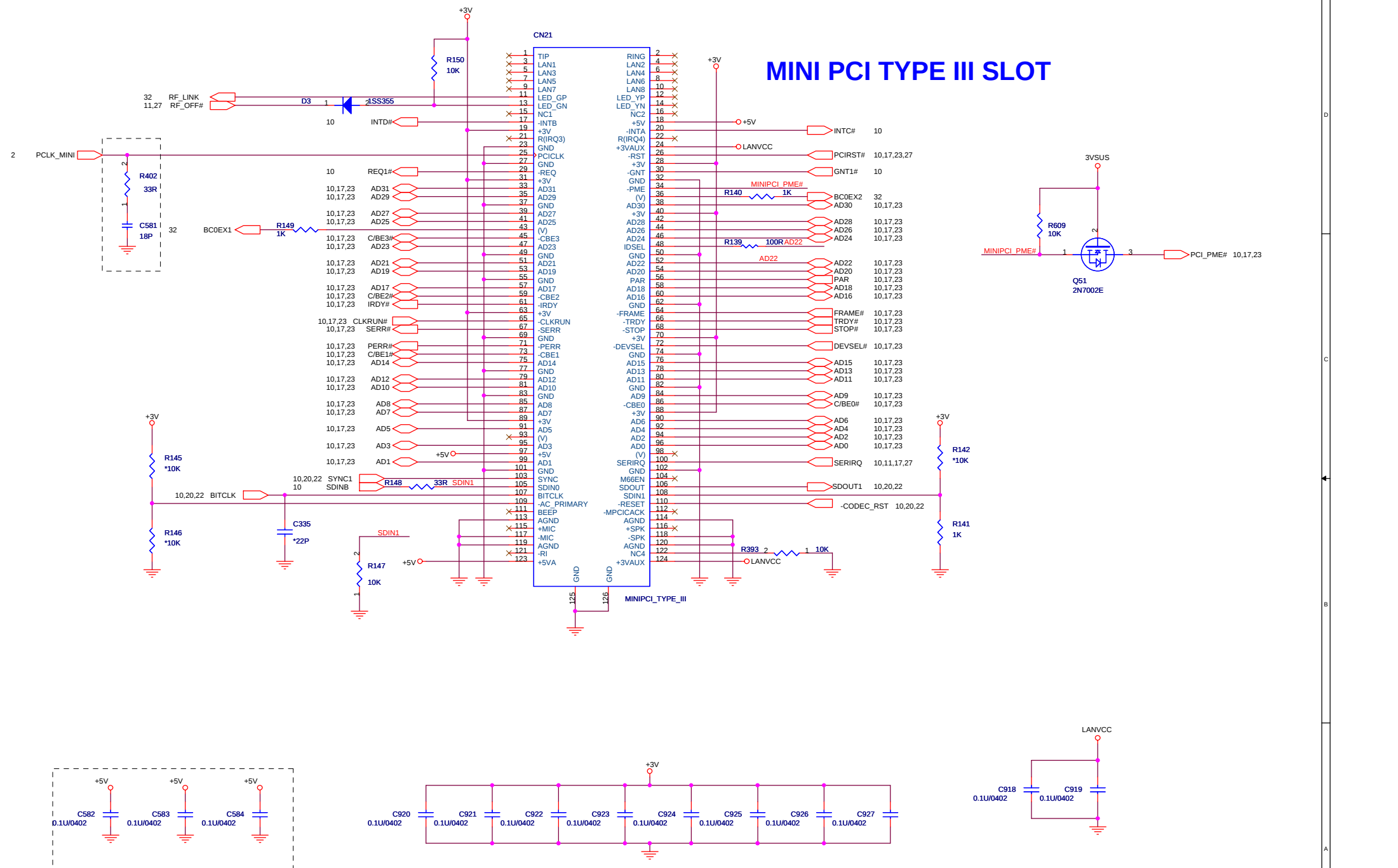
PV stage:
The root cause that is 3V_S5 leakage current to 5VSUS by R712 on S4/S5 stage.

SI stage:
We can also use 5VSUS to instead of 5V_S5 to save cost if 5V_S5 isn't implementation on system.

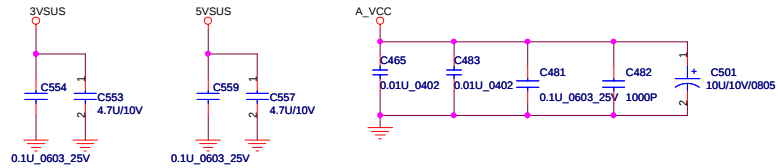
Griffey 12/13/2004
Sting 10/12/2004



MINI PCI TYPE III SLOT

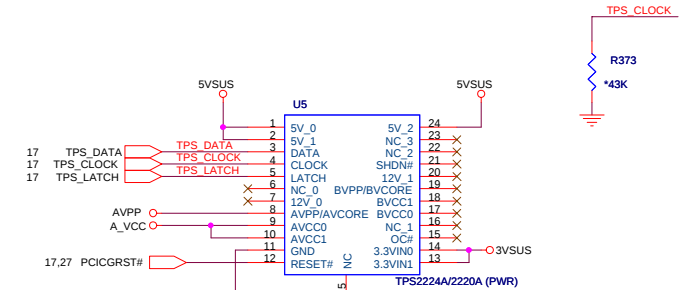


CardBus Connector



CARDBUS POWER SWITCH

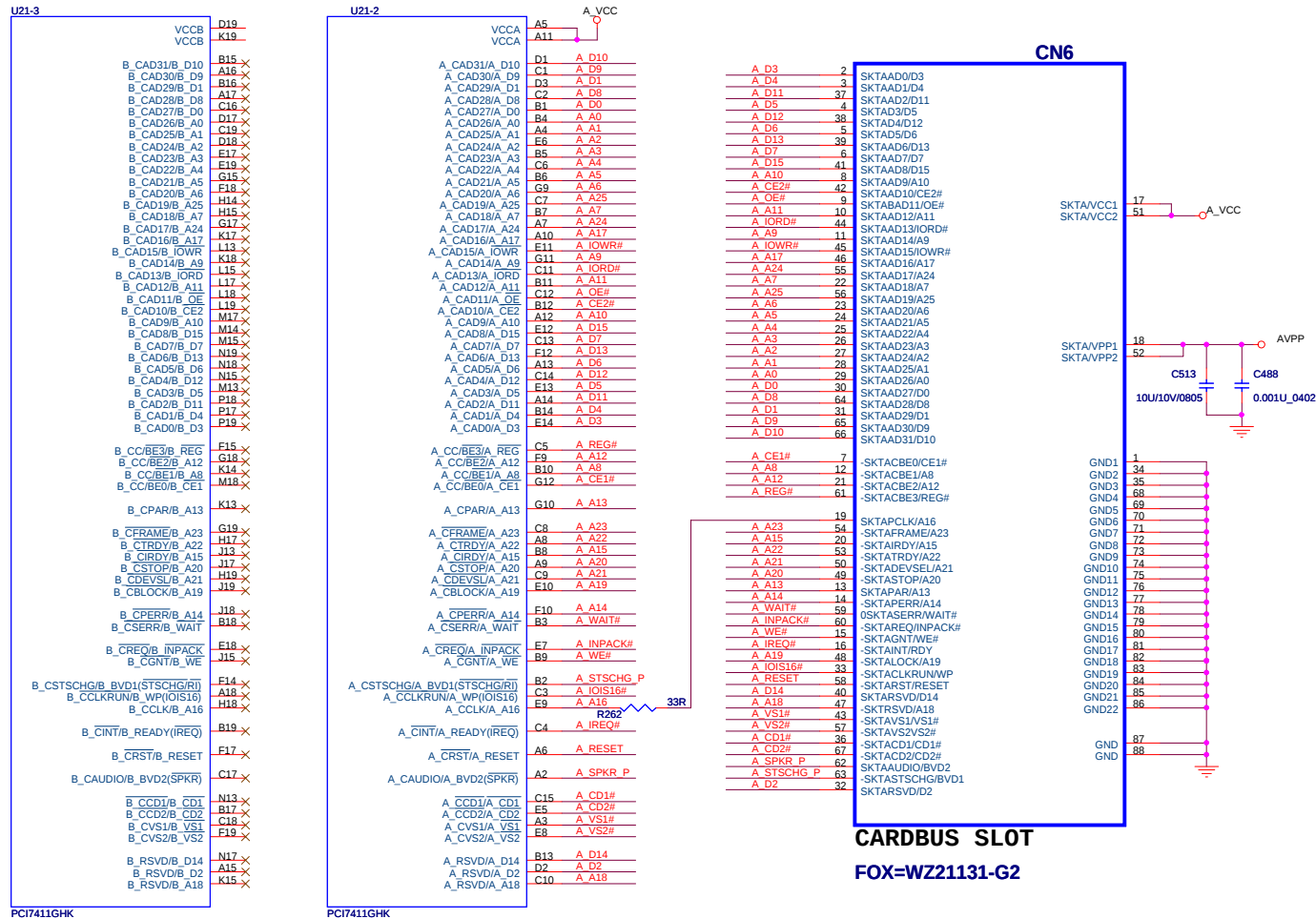
For PCI7411



For PCI1510

PV stage:
Remove unused PCI1510RVGF circuit.

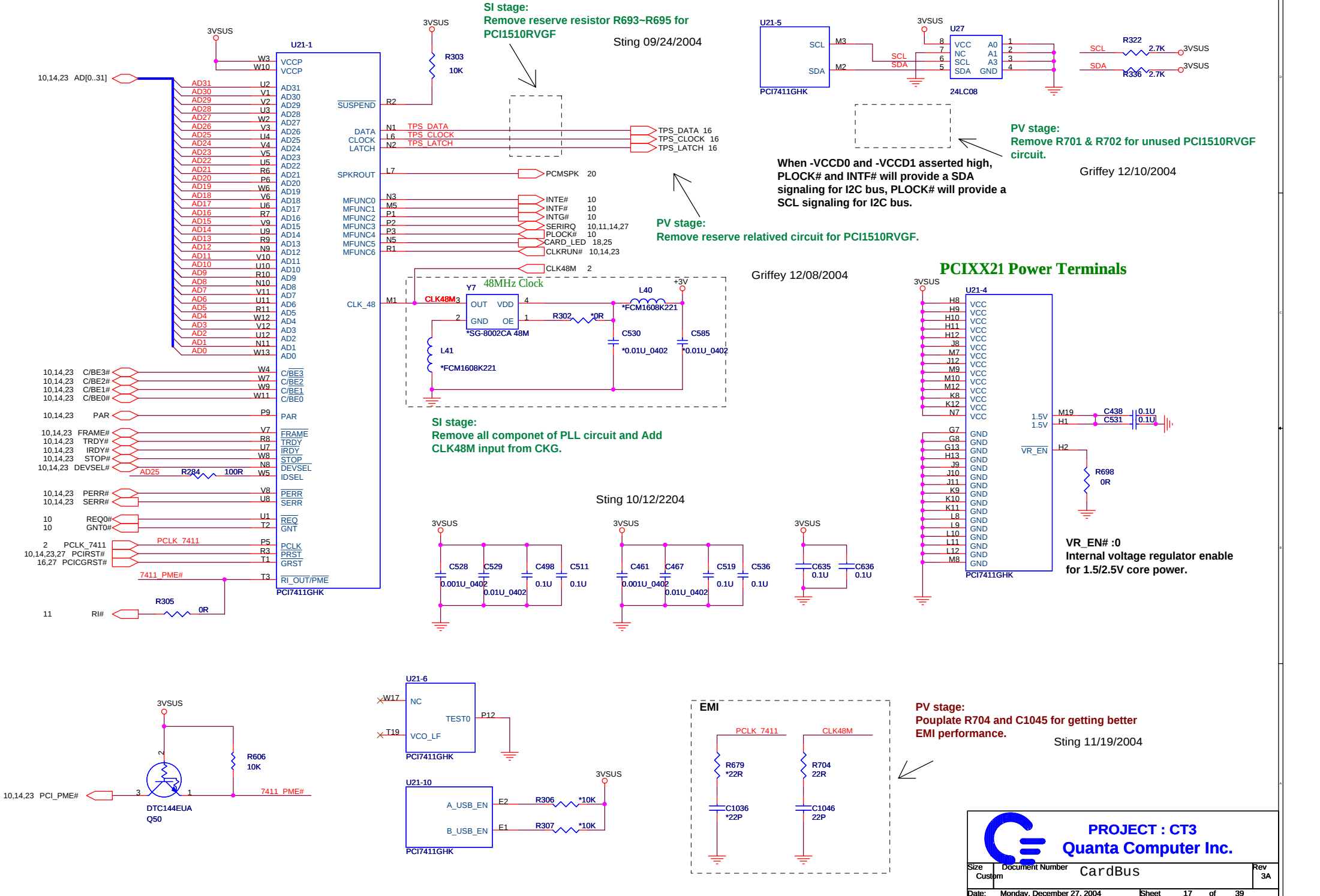
Griffey 12/08/2004



CARDBUS SLOT

FOX=WZ21131-G2

CardBus



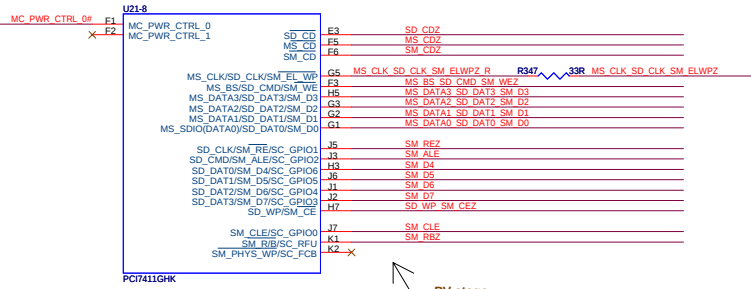
CARD POWER CONTROL

PV stage:
Remove reserve related circuit for
PC1510RVGF.
Griffey 12/08/2004

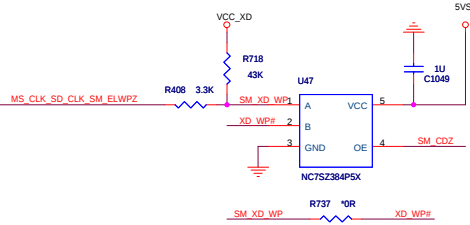
SI stage:
Remove reserve resistor R696 fro
PC1510RVGF.
Sting 10/12/2004

Reserve for smart card which is powered by 5V.

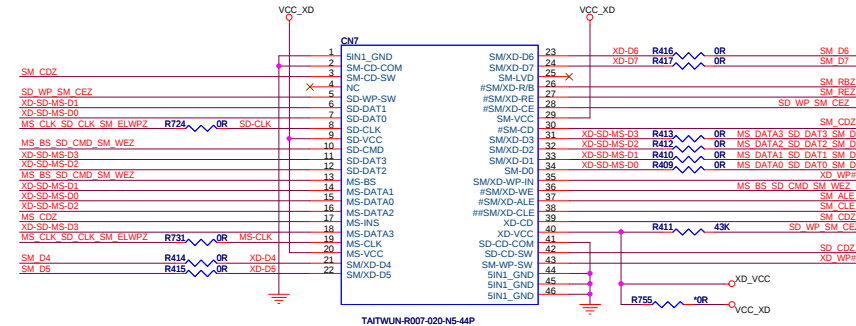
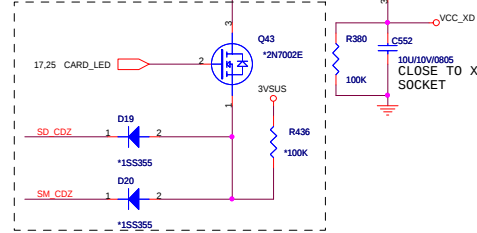
PV stage:
Add a discharge circuit for media
card power.
Sting 11/19/2004



PV stage:
1. Disconnect SM_PHYS_WP.
2. Tie SM_EL_WP with SM_PHYS_WP of SM card to allow
for normal operation of SD and SM.
Sting 11/19/2004



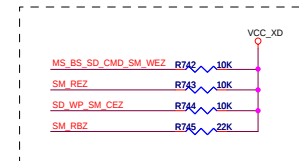
PV stage:
1. Add quick switch circuit.



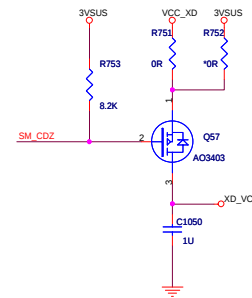
5 IN1 CARD READER

PV stage:
1. Add pull-up circuit.

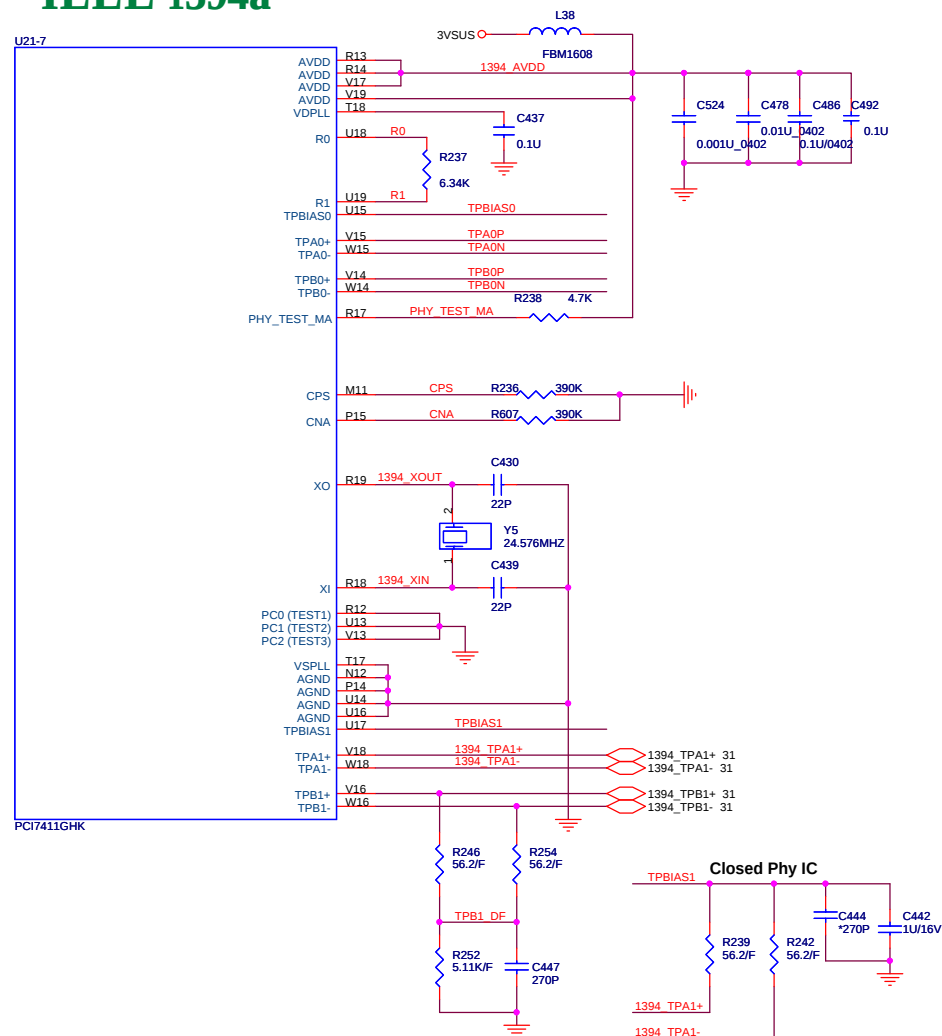
Griffey 12/20/2004



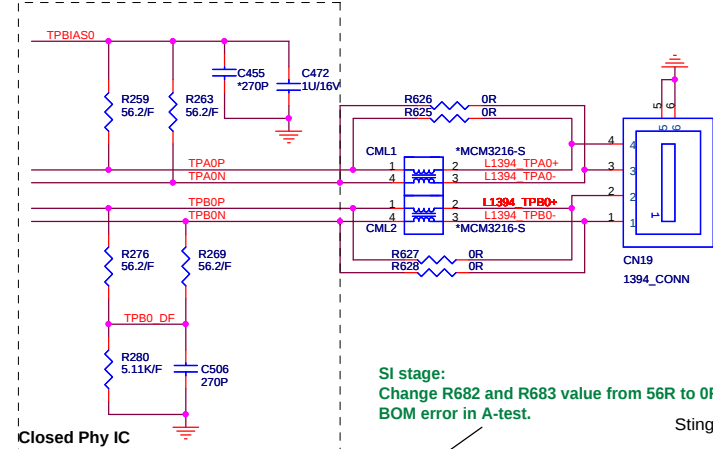
PV stage:
1. Add R717 to solve SM card can't write protect issue.
2. Add R718 to solve cross-talk issue of MS-PRO card.
3. Add R719-R736 as terminal on all multi-funtn pin.
Sting 11/19/2004



IEEE 1394a



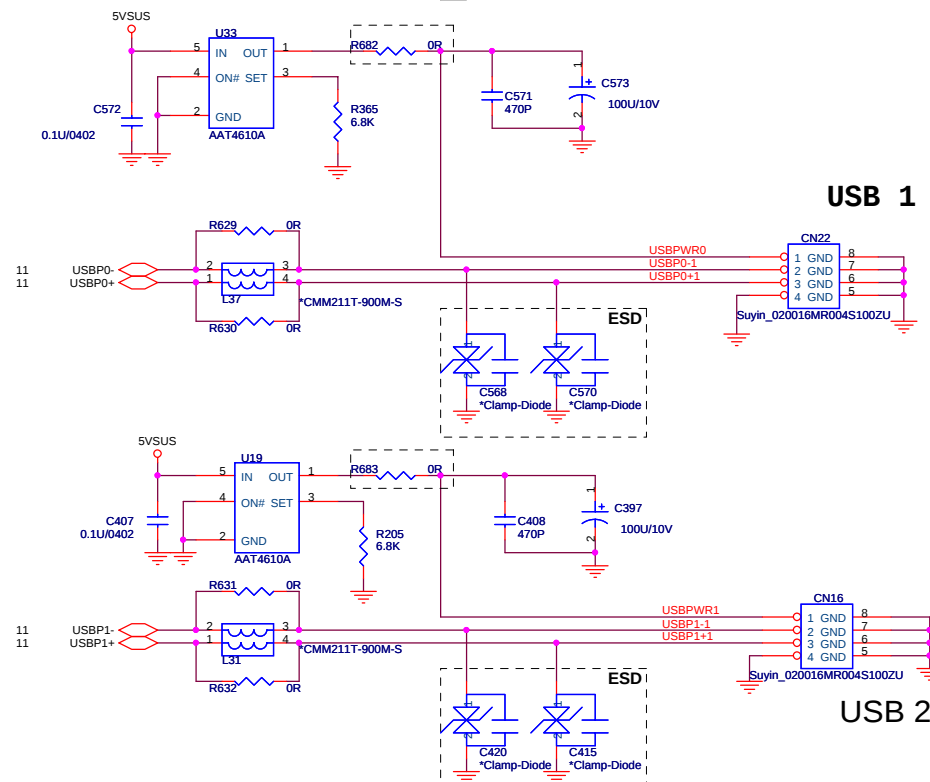
IEEE 1394 CONNECTOR



SI stage:
Change R682 and R683 value from 56R to 0R cause of
BOM error in A-test.

Sting 09/24/2004

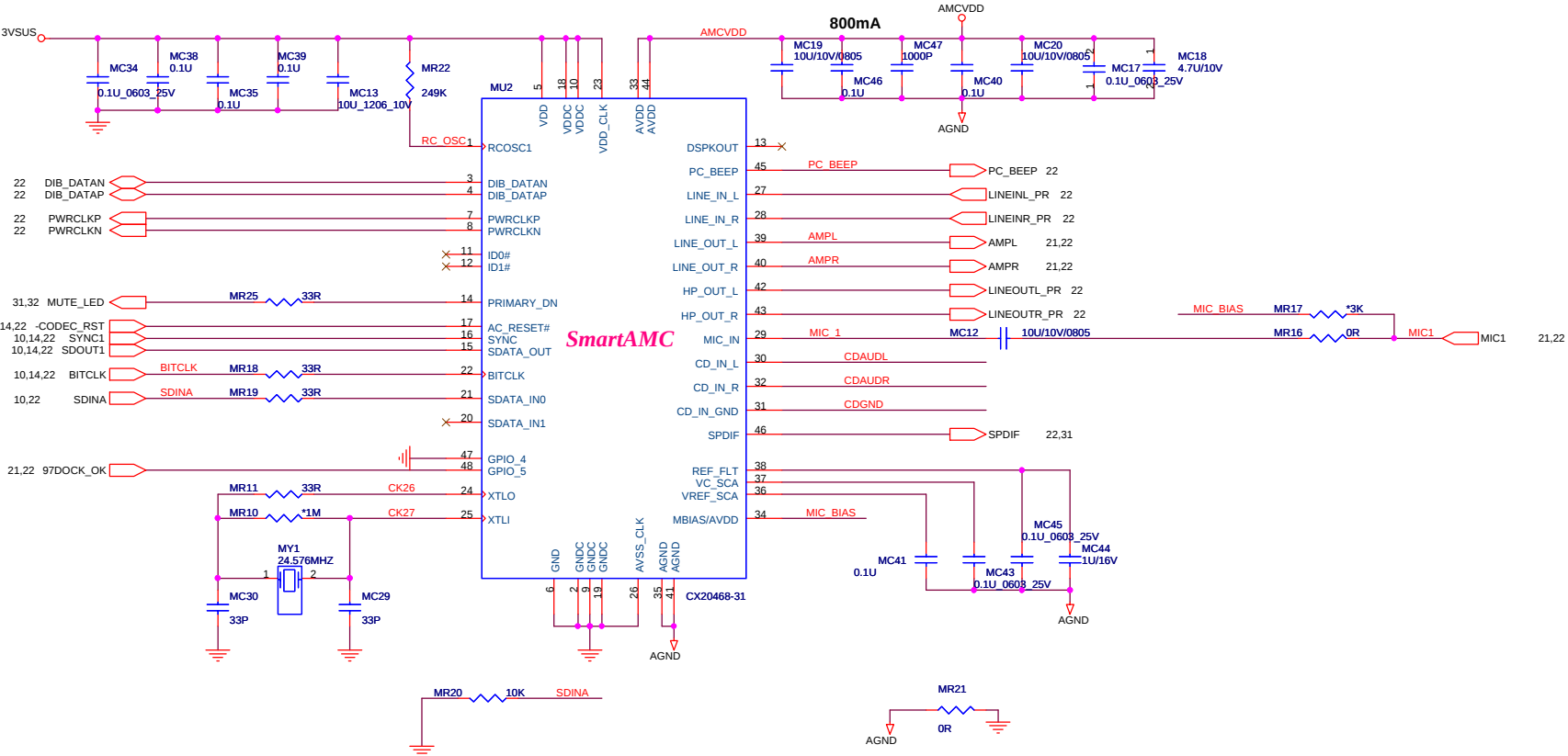
Closed Phy IC



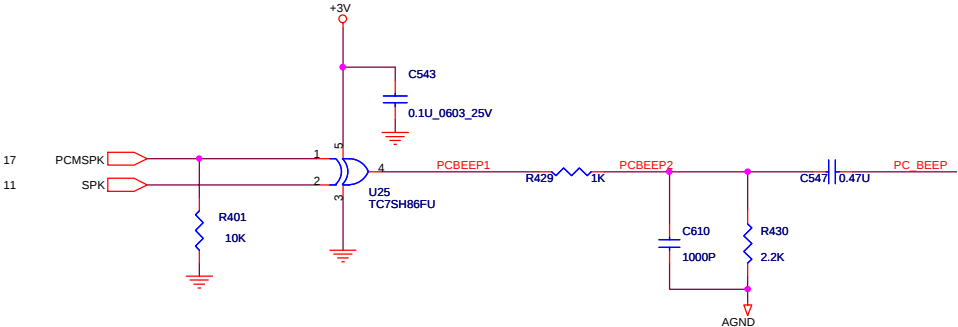
USB 1

USB 2

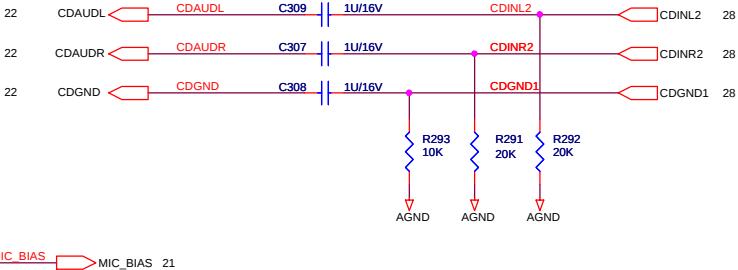
The AMC20493-001 modem is used for mother board family MBAMC20493-010.



PC SPEAKER



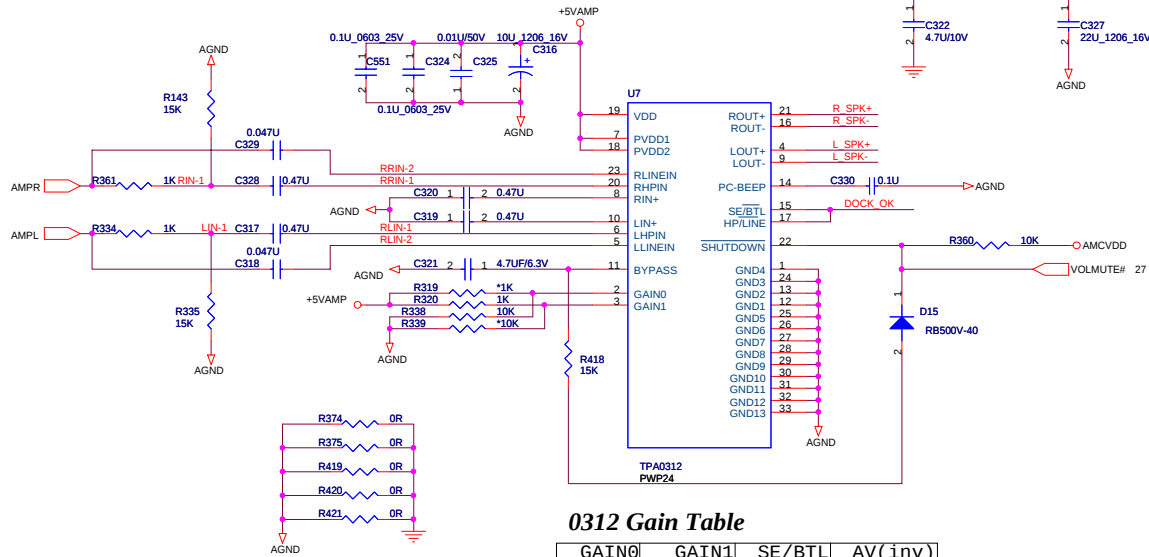
FROM CD-ROM



PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
	AMC97 CODEC	1A
Date:	Monday, December 27, 2004	Sheet 20 of 39

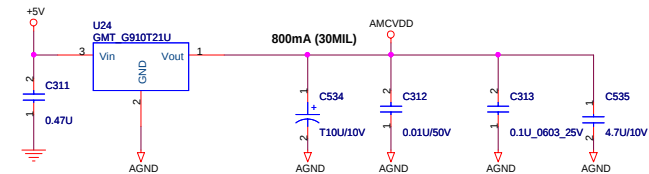
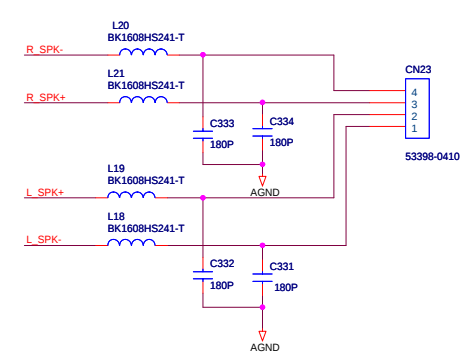
AUDIO AMPLIFIER



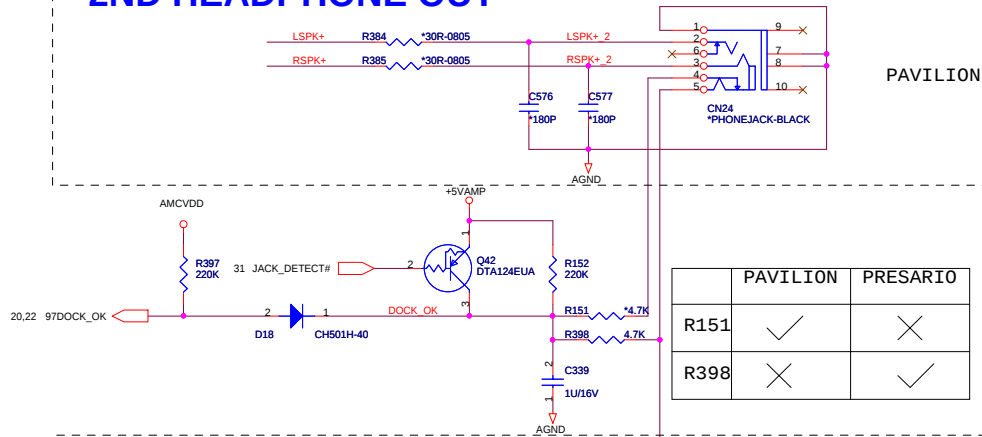
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

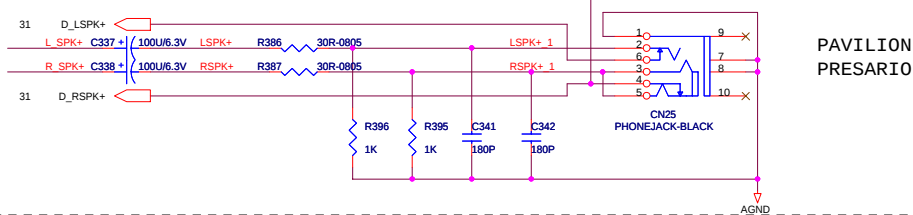
SPEAKER OUT



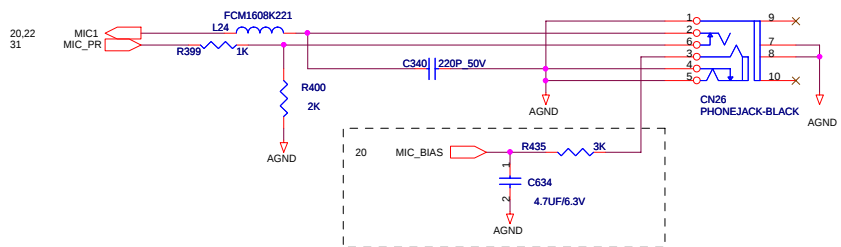
2ND HEADPHONE OUT



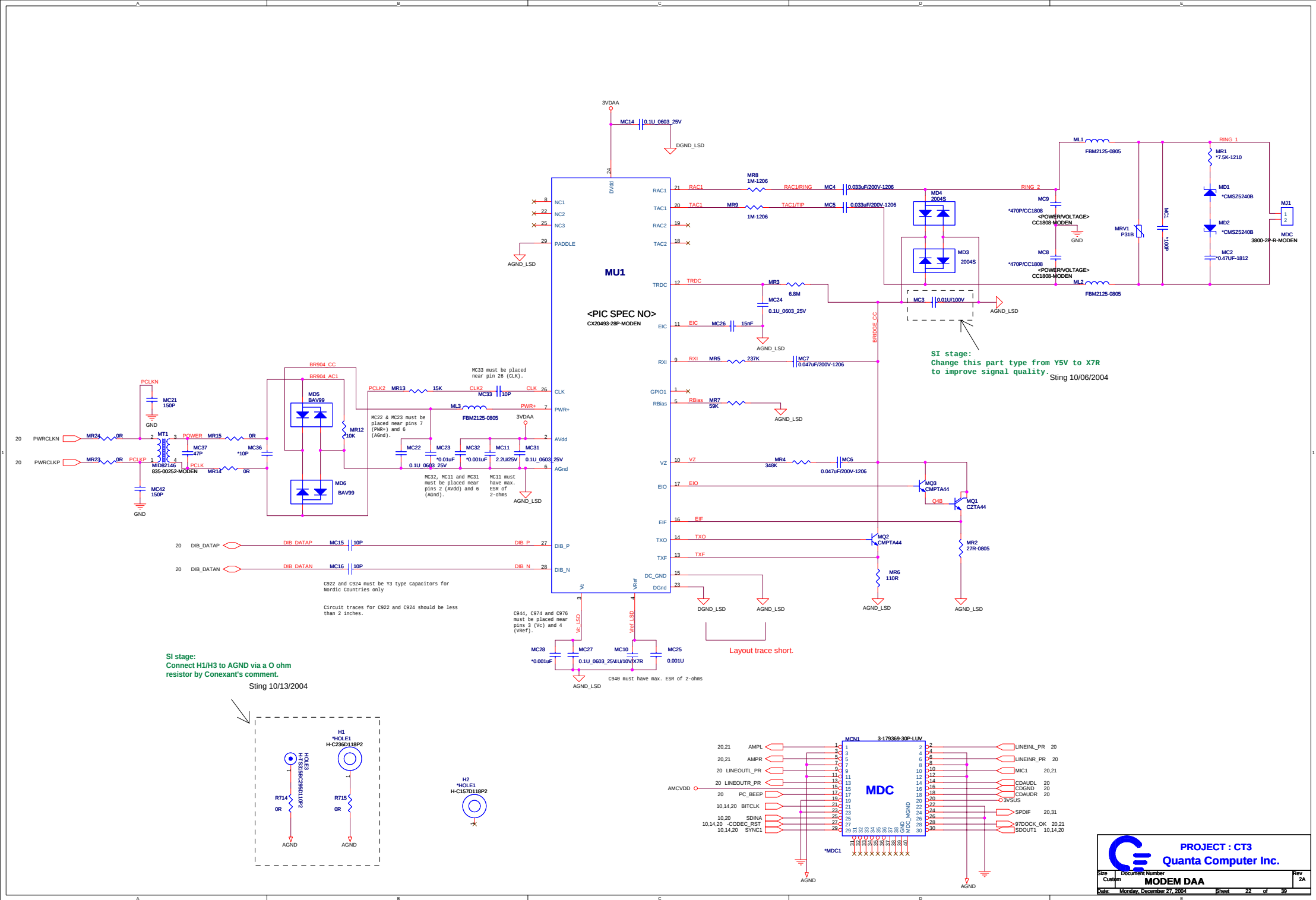
HEADPHONE OUT



MICROPHONE



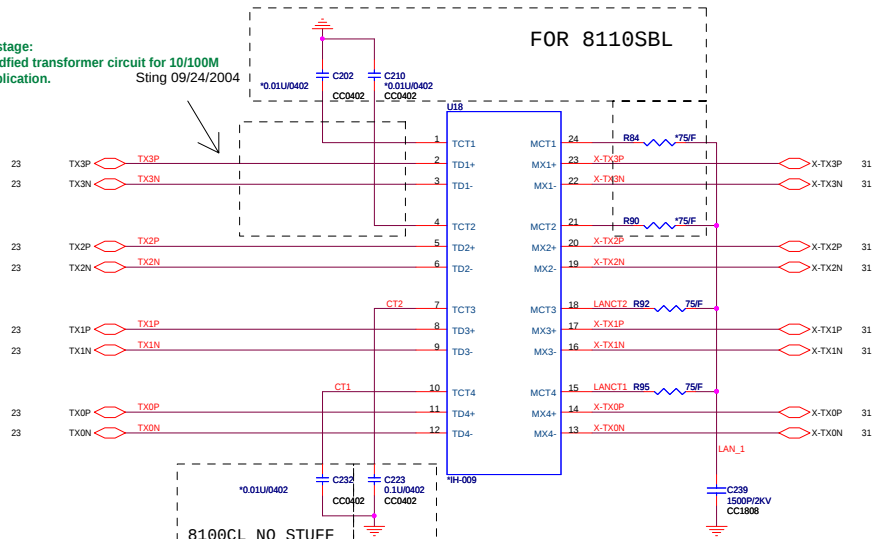
	PAVILION	PRESARIO
R151	✓	✗
R398	✗	✓



SI stage:
Modified transformer circuit for 10/100M application.

Sting 09/24/2004

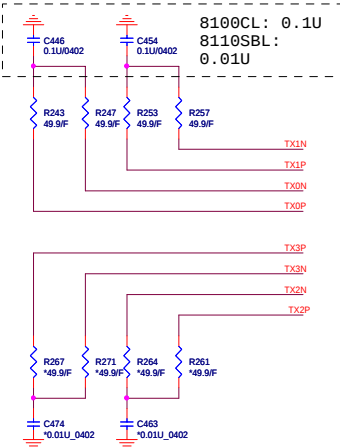
FOR 8110SBL



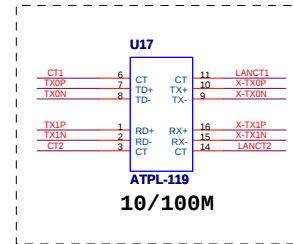
16

8100CL: 0.1U
8110SBL: 0.01U

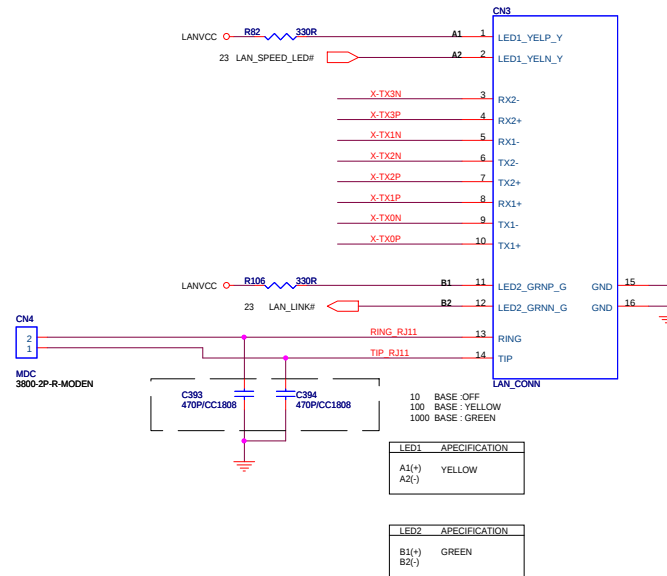
Close to Chip



8100CL: 0.1U
8110SBL: 0.01U

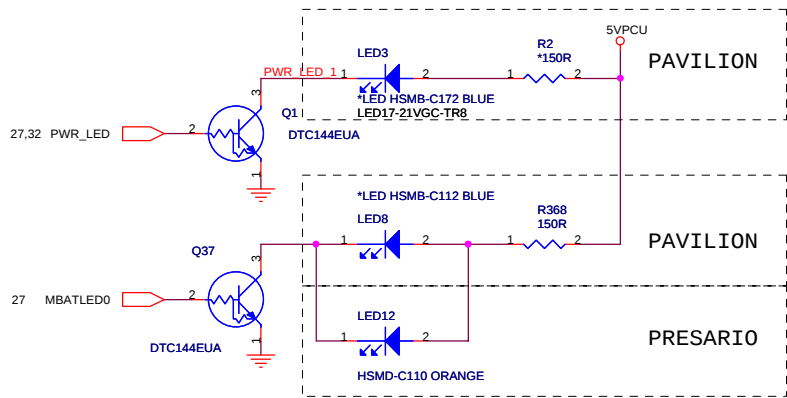


U17
ATPL-119
10/100M

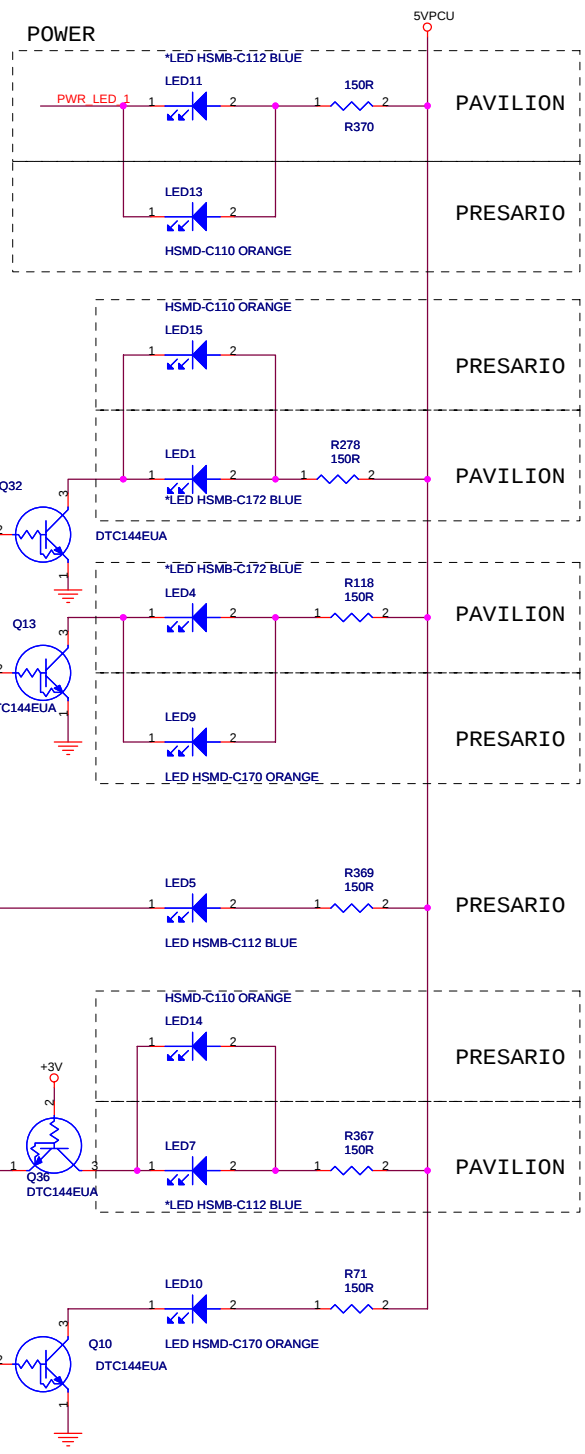
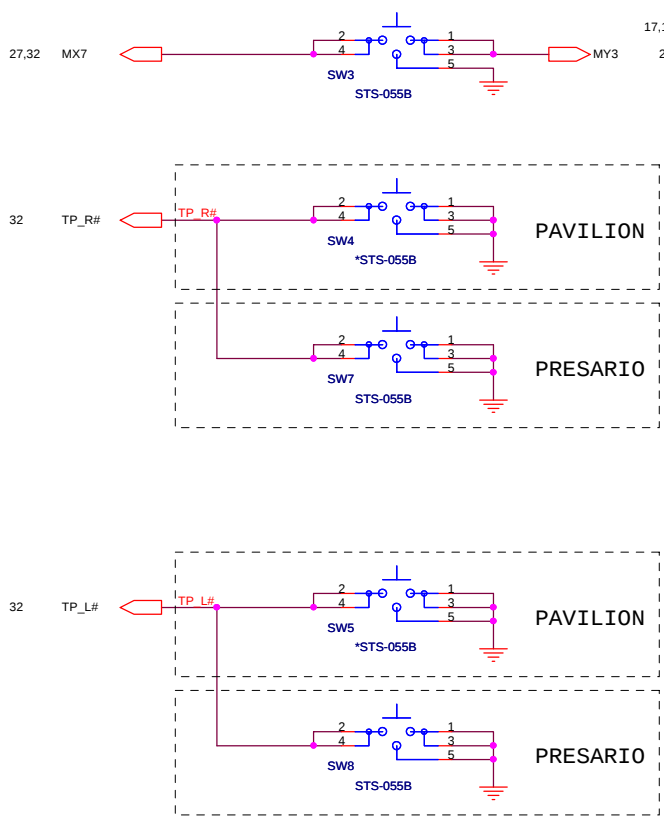


LED1 APECIFICATION	
A1(+)	YELLOW
A2(-)	

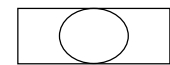
LED2 APECIFICATION	
B1(+)	GREEN
B2(-)	



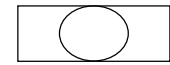
Touchpad control



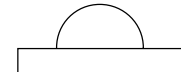
LED HSMD-C170 ORANGE



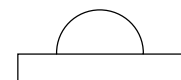
LED HSMB-C172 BLUE



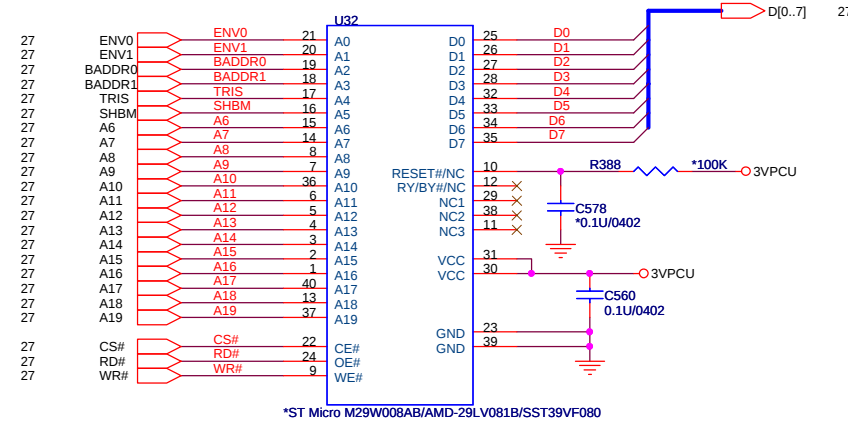
LED HSMD-C110 ORANGE



LED HSMD-C112 BLUE



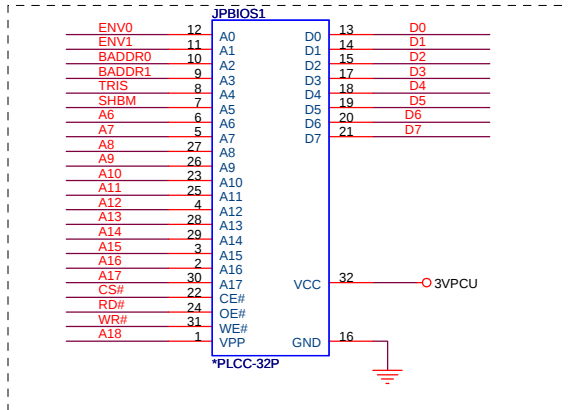
8Mbit (1M Byte), TSSOP40



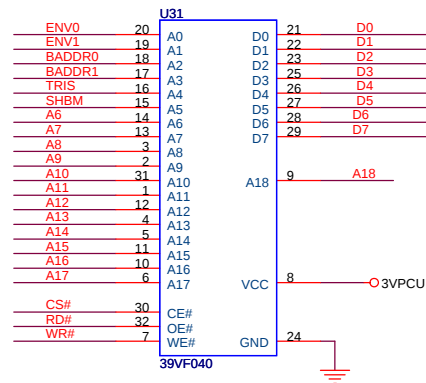
- 1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326 UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
- 2.SIO has internal 20 mS delay of VCC1_PWROK

AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

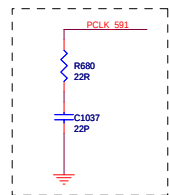
SI stage:
Add PLCC32 cause of it is convenient for Bios debugging.
Sting 10/01/2004



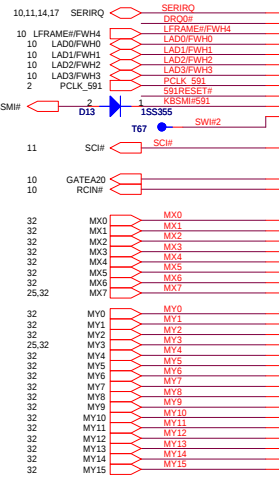
4Mbit (512k Byte), TSSOP32



KBC-NS87551L



LDRQ#(pin 8) internal is no use

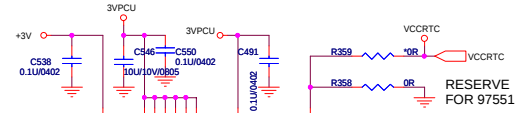
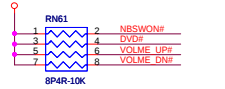
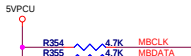
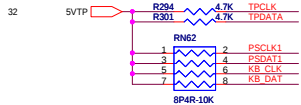
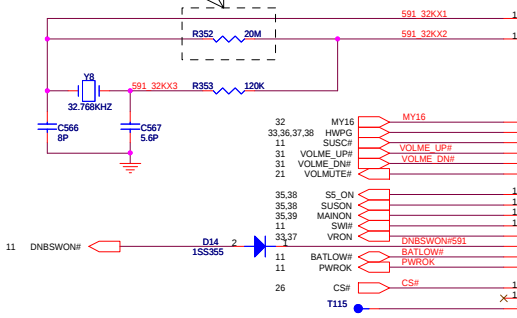
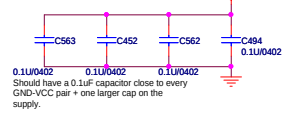


SI stage:
Change R352 value from 120K to 20M.
Sting 09/24/2004

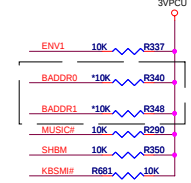
32 TPCLK

PSDAT1
KB CLK
KB DAT
TPCLK
TPDATA

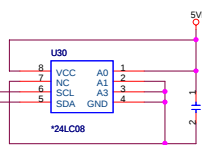
Sting 09/24/2004

RESERVE
FOR 97551

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.



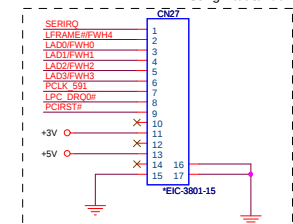
SHBM=1: Enable shared memory with host BIC



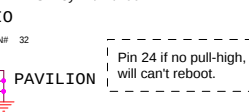
CLOSE TO U23 

SI stage:
Add LPC debug port for software team
to debug convenient.

Sting 10/06/2004

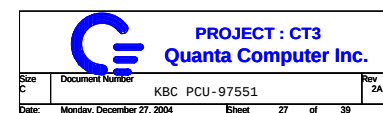
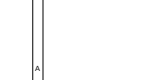
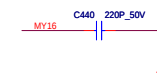
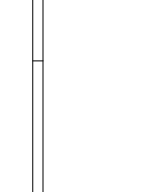
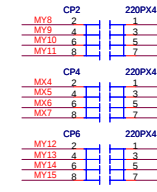
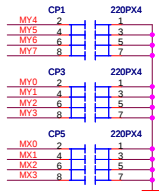
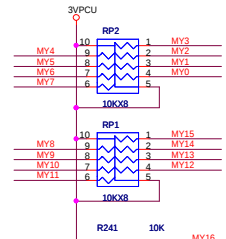


PV stage:
Modify pin name. Griffey 12/10/2004

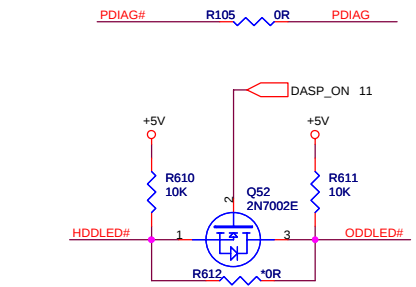


Pin 24 if no pull-high,
will can't reboot.

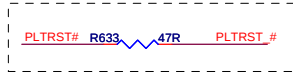
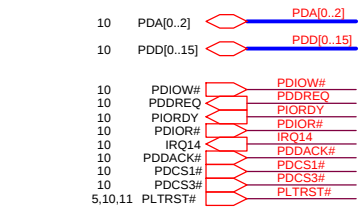
Pin 24 if no pull-high,
will can't reboot.



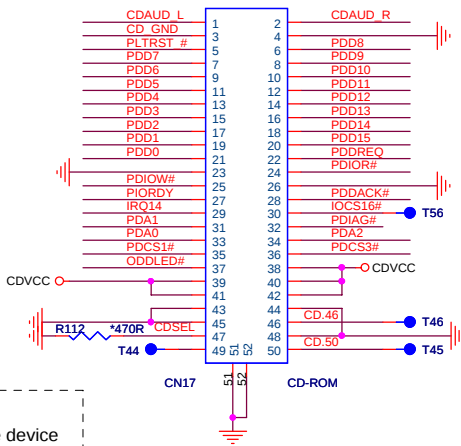
HDD, CD-ROM



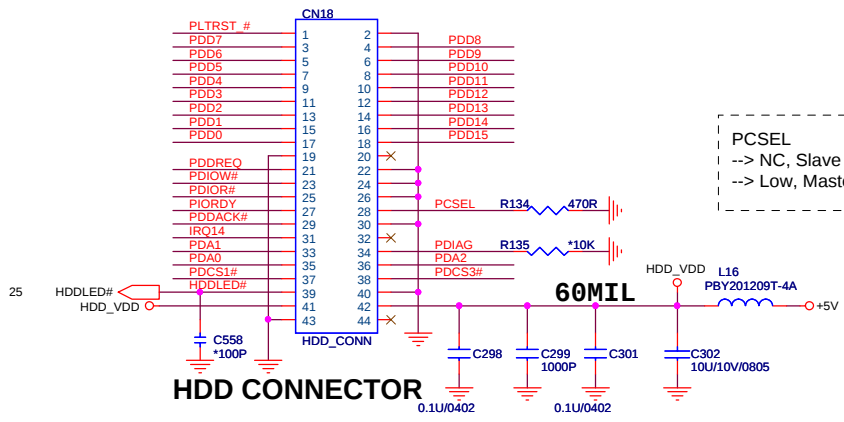
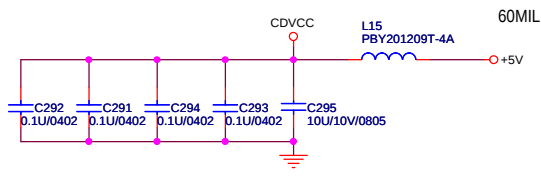
ADD DASP_ON FOR IDE CABLE SELECT



CD-ROM

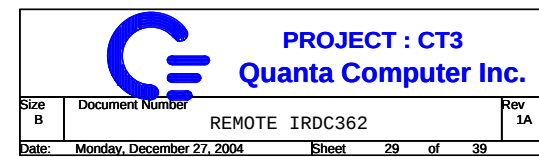


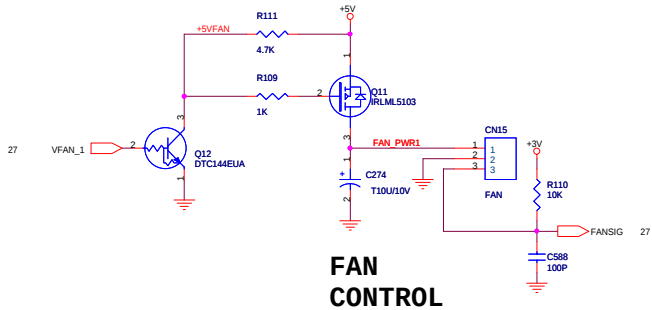
CDSEL
--> NC, Slave device
--> Low, Master device



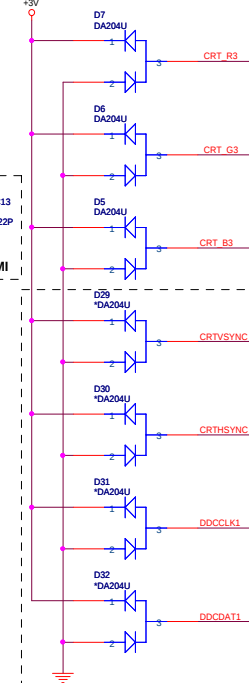
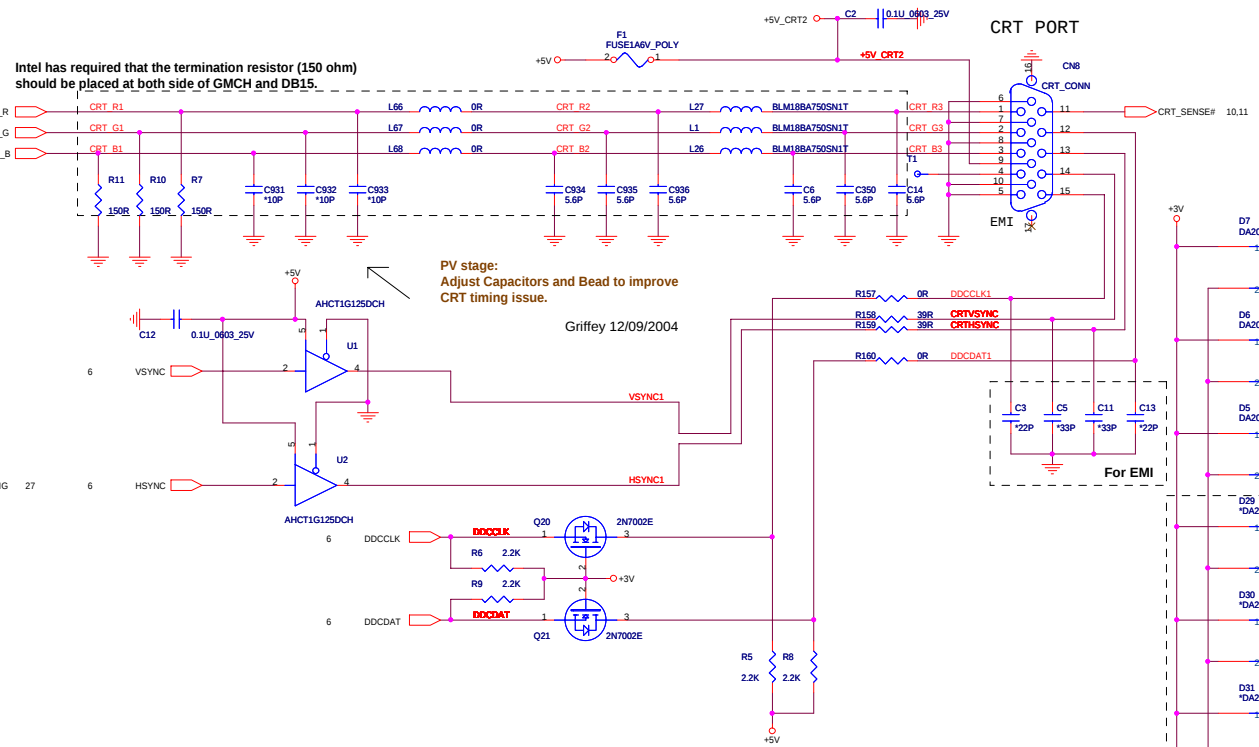
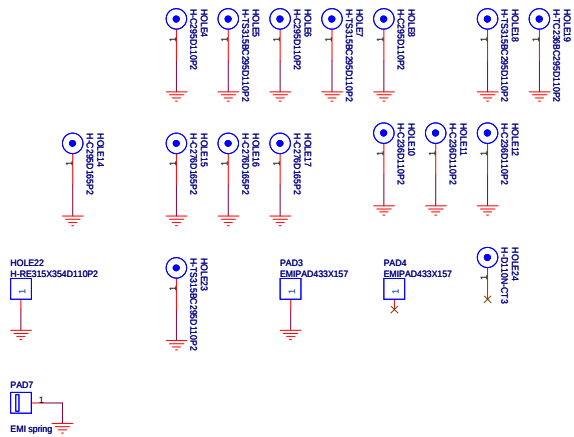
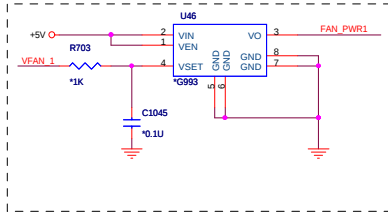
PCSEL
--> NC, Slave device
--> Low, Master device

HDD CONNECTOR

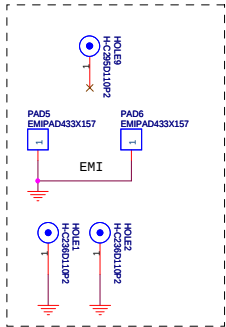




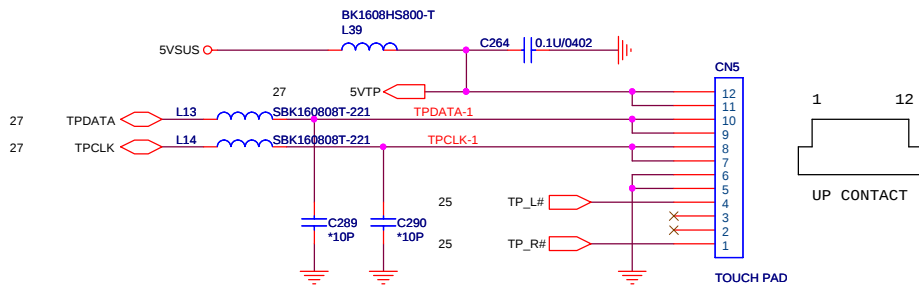
SI stage:
Add GMT solution for B-test to costdown.
Sting 09/24/2004



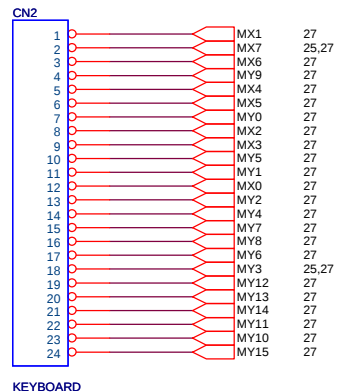
Add ESD protection by Sting 08/03/2004



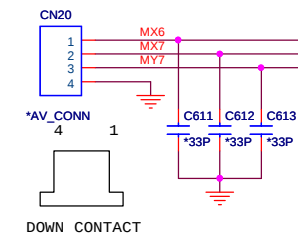
TOUCH PAD CONNECTOR



KEYBOARD CONNECTOR

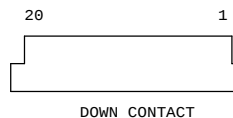
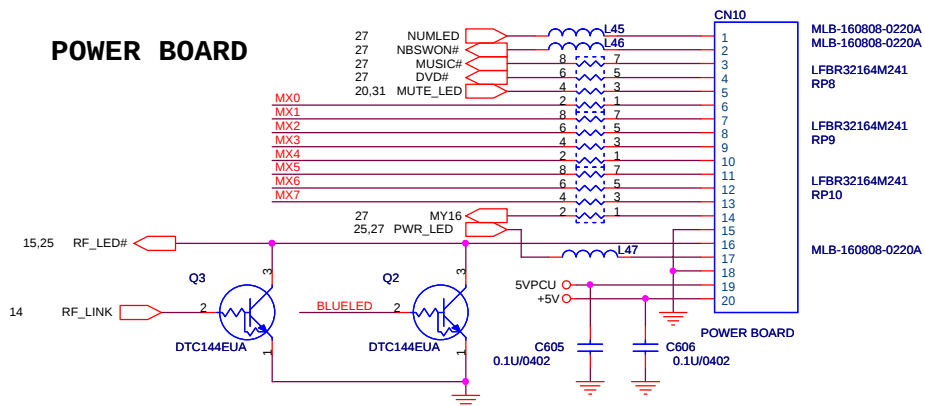


AV BOARD



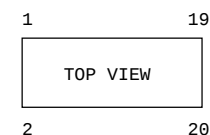
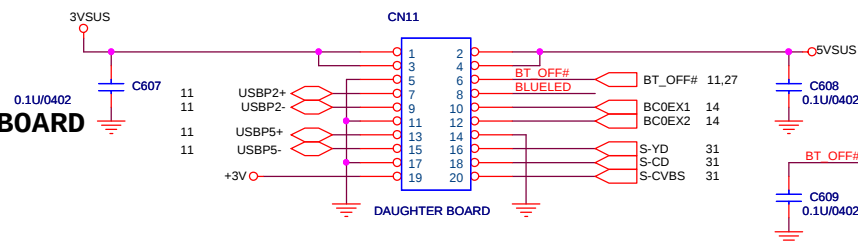
MX6	MX7
ENTER	MENU

POWER BOARD



MX0	MX1	MX2	MX3	MX4	MX5	MX6	MX7
BACK	PLAY/PAUSE	FORWARE	STOP	VOL UP	MUTE	VOL DN	WIRELESS

DAUGHTER BOARD



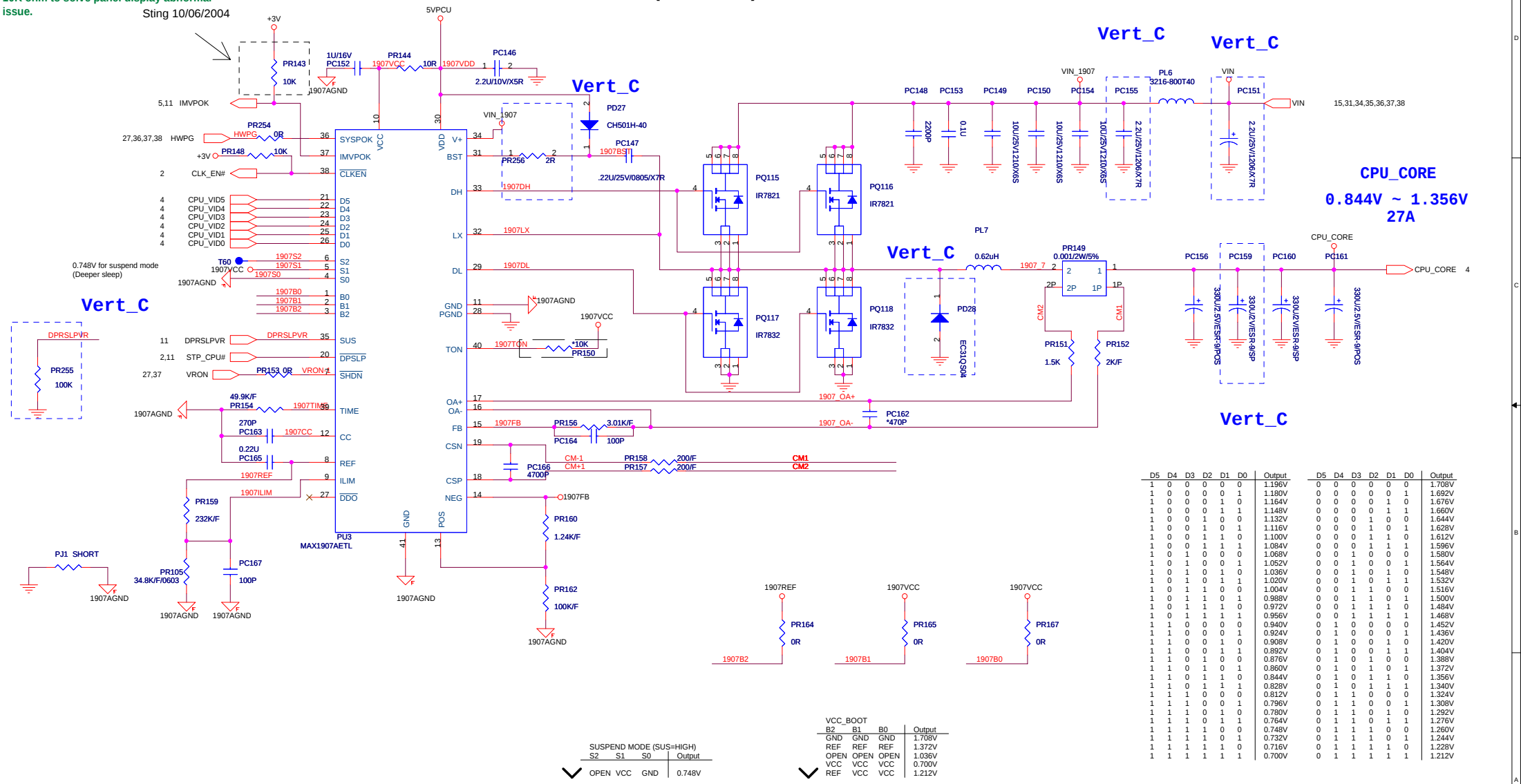
PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLUETOOTH/TP/BTB	1A
Date:	Monday, December 27, 2004	Sheet 32 of 39

SI stage:
Change PR143 value from 100K ohms to
10K ohm to solve panel display abnormal
issue.

Sting 10/06/2004

CPU VCC_CORE
(MAX1907)



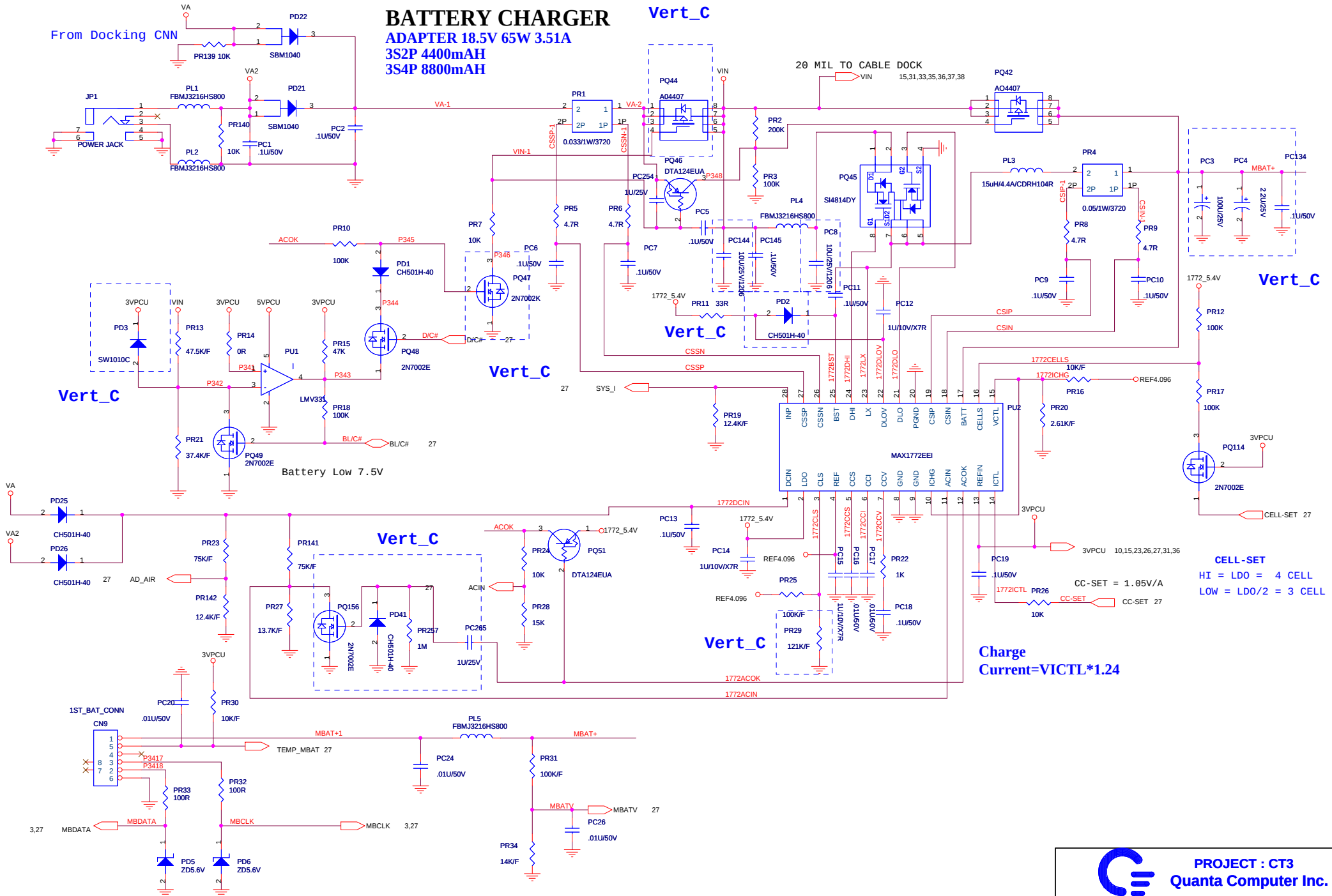
D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	1	0	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	0	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	0	1	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V

SUSPEND MODE (SUS=HIGH)	S2	S1	S0	Output
OPEN	VCC	GND	GND	0.748V

VCC_BOOT	B2	B1	B0	Output
GND	GND	GND	GND	1.708V
REF	REF	REF	REF	1.372V
OPEN	OPEN	OPEN	OPEN	1.036V
VCC	VCC	VCC	VCC	0.700V
REF	VCC	VCC	VCC	1.212V

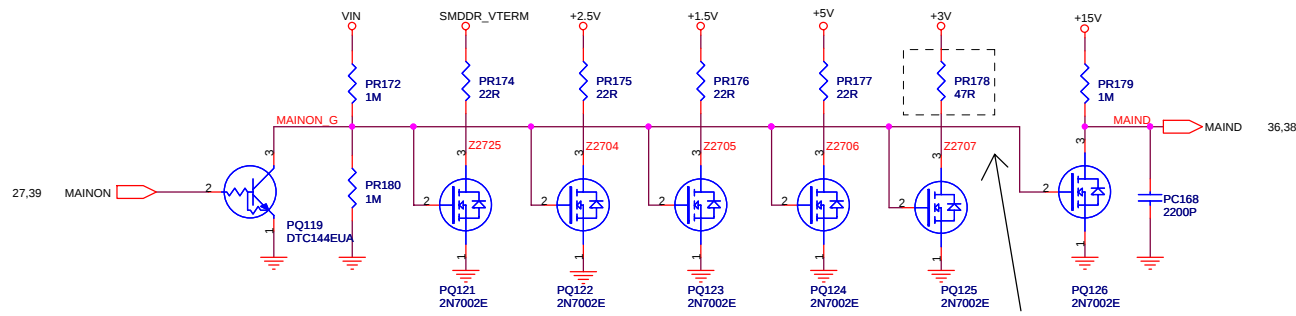
BATTERY CHARGER

ADAPTER 18.5V 65W 3.51A
3S2P 4400mAh
3S4P 8800mAh



Charge
Current=VICTL*1.24

CELL-SET
HI = LDO = 4 CELL
LOW = LDO/2 = 3 CELL

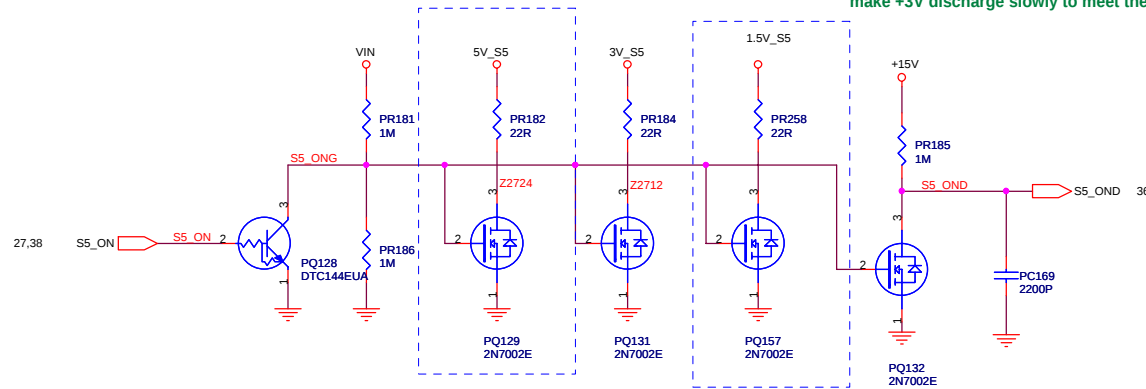


Vert_c

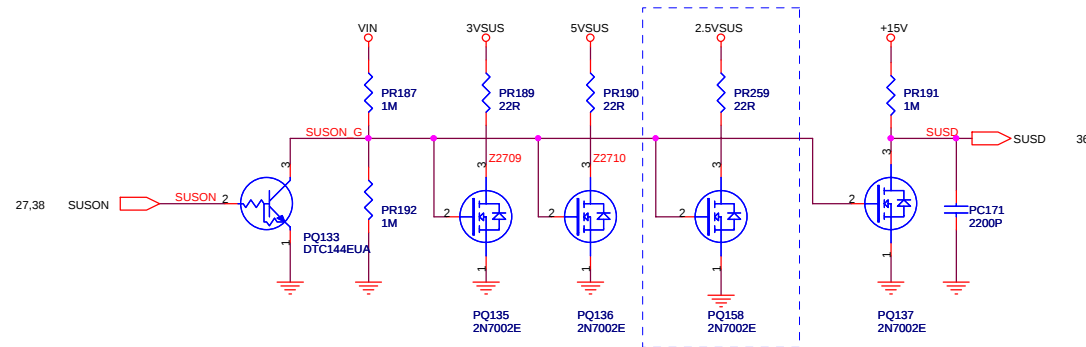
Vert_c

SI stage:
Change PR178 value from 22 ohm to 47 ohm, Intel has required the timing sequence of +1.5V and +3V in the system, we'd like to increase the value to make +3V discharge slowly to meet the specification of falling time.

Sting 10/19/2004

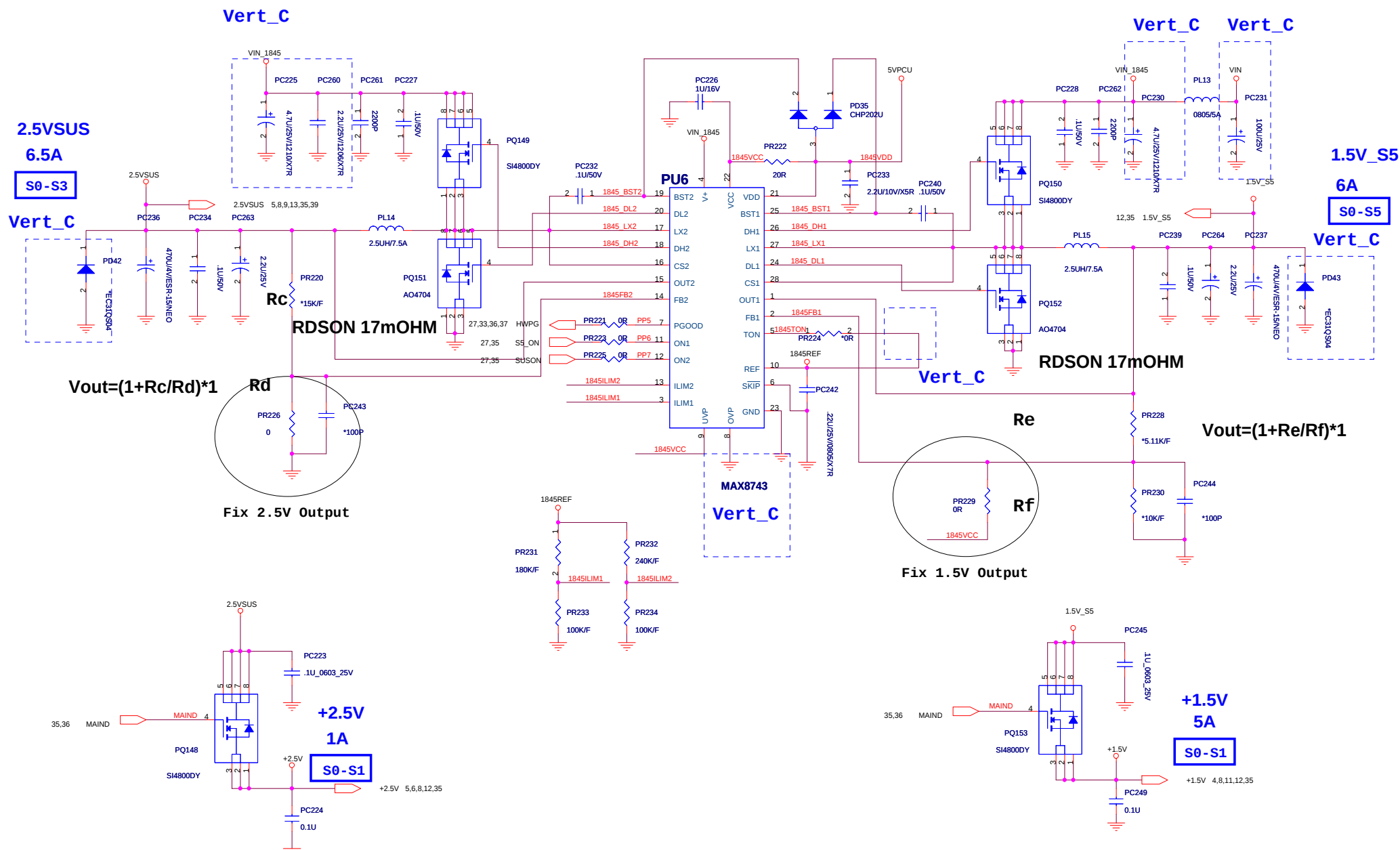


Vert_c



PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom		2A
DISCHARGE		
Date:	Monday, December 27, 2004	Sheet 35 of 39



[illegible]