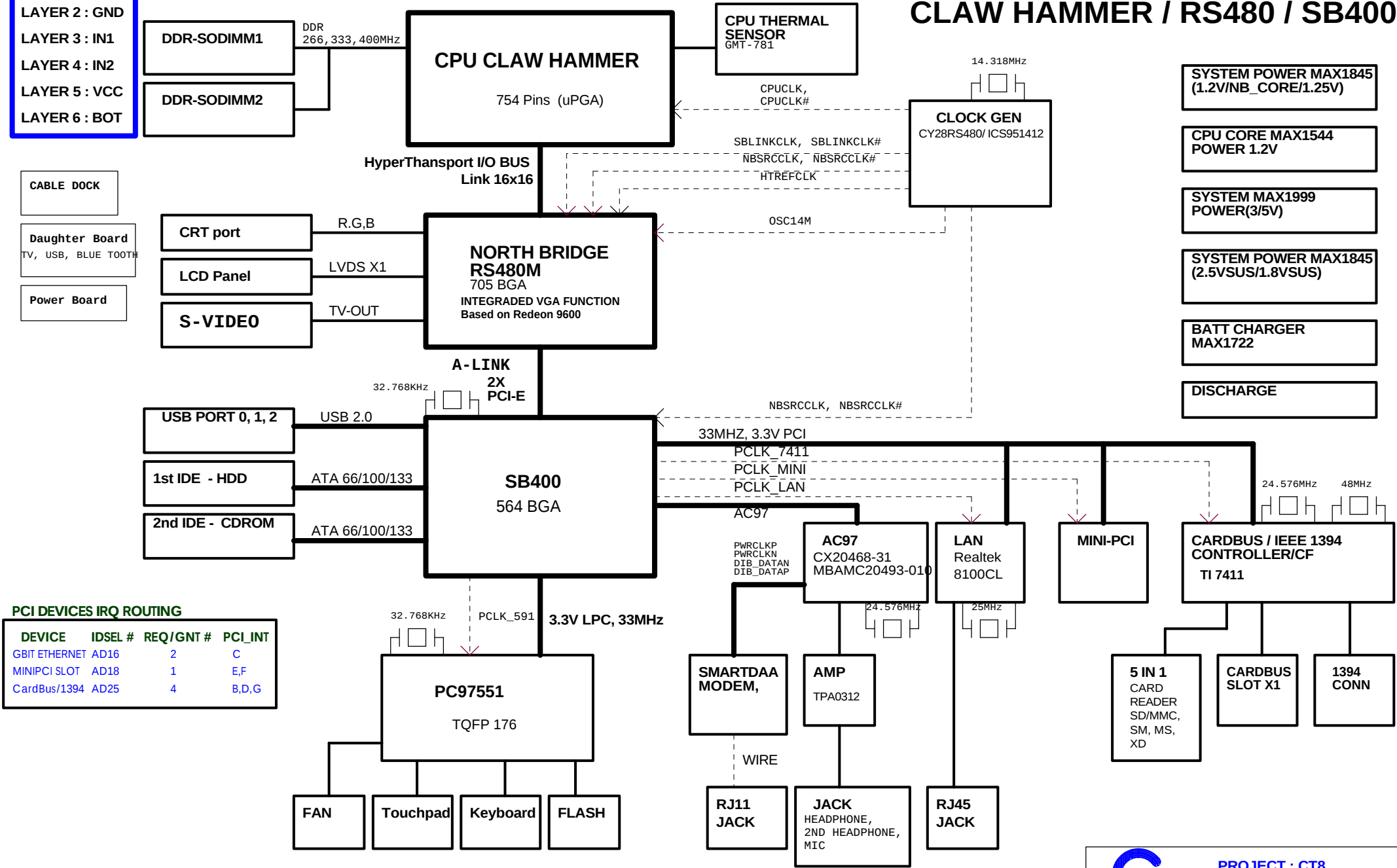
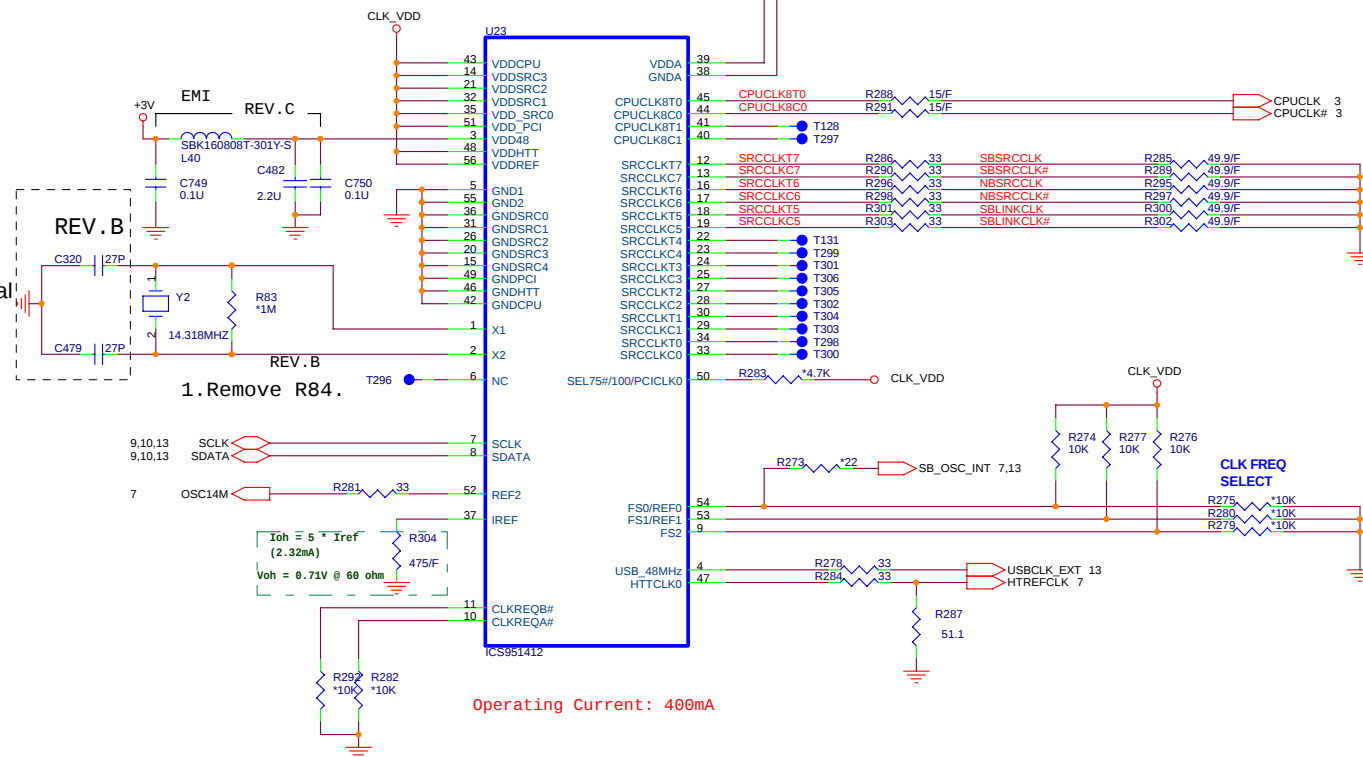


PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

CT8 BLOCK DIAGRAM
CLAW HAMMER / RS480 / SB400



[illegible]

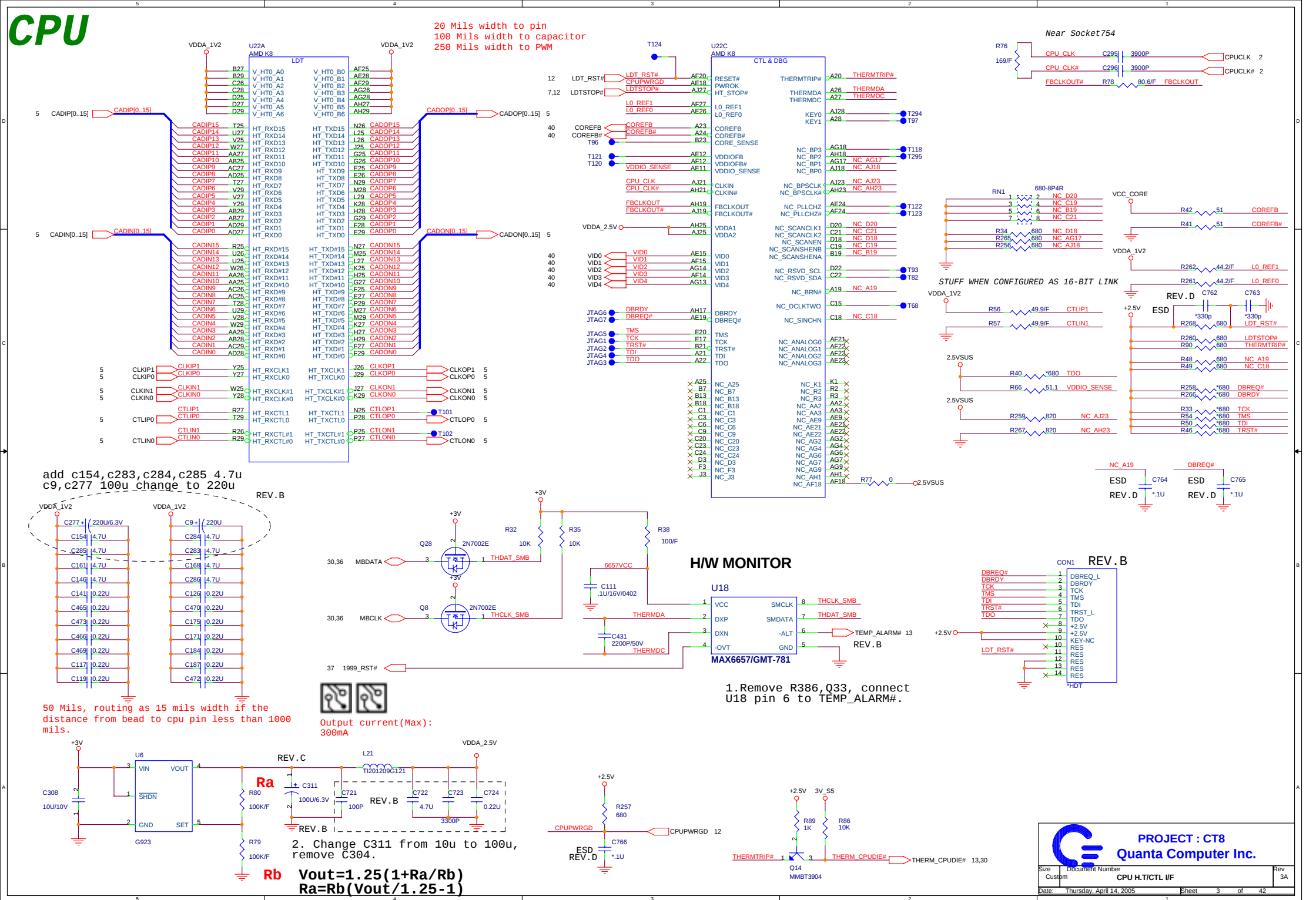
1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS
PKG. AS POSSIBLE

2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, SBSRCCLK/#, SBLINKCLK/# AS DIFFERENT PAIR RULE

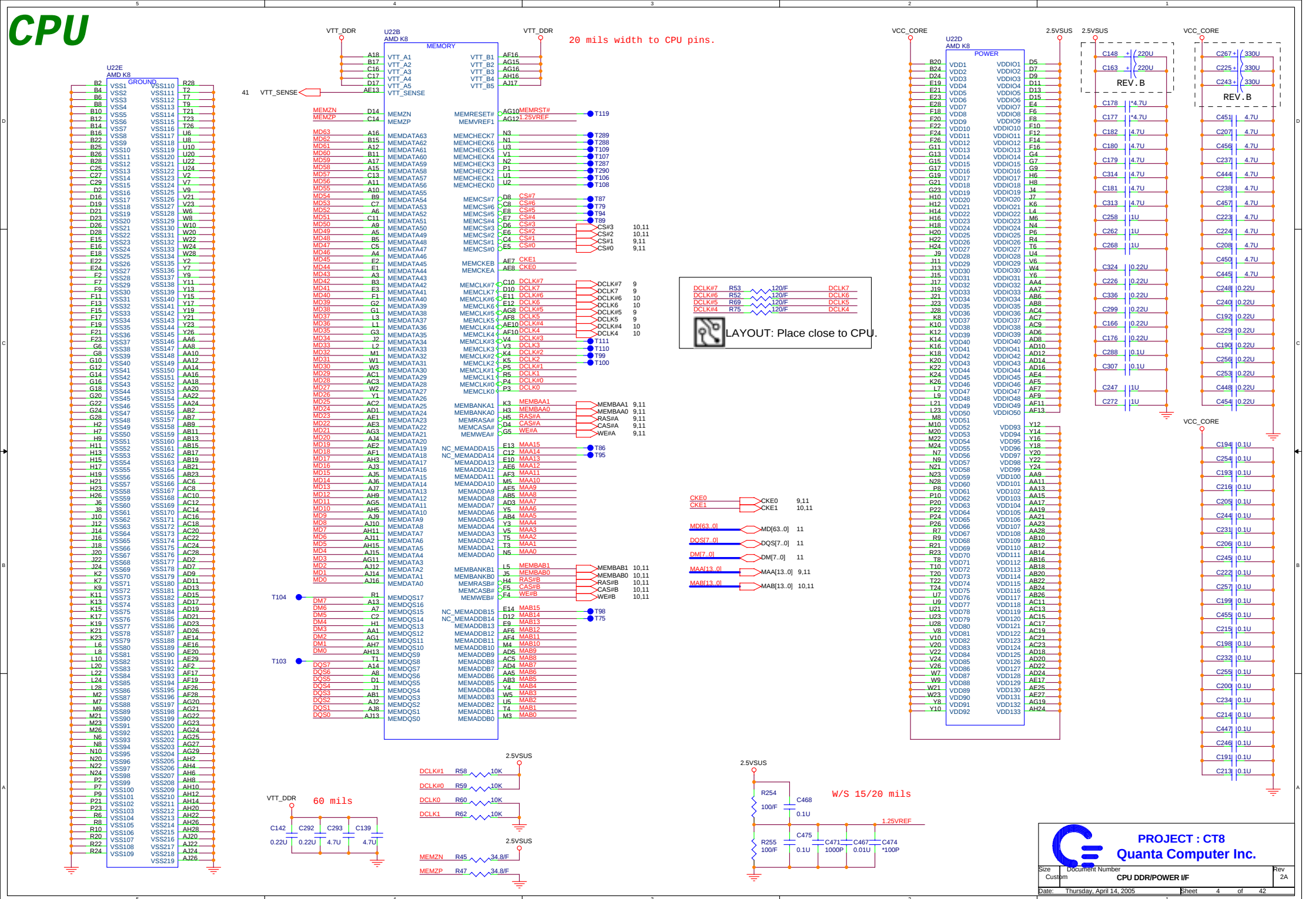
3- PUT DECOUPLING CAPS CLOSE TO CKG. POWER PIN

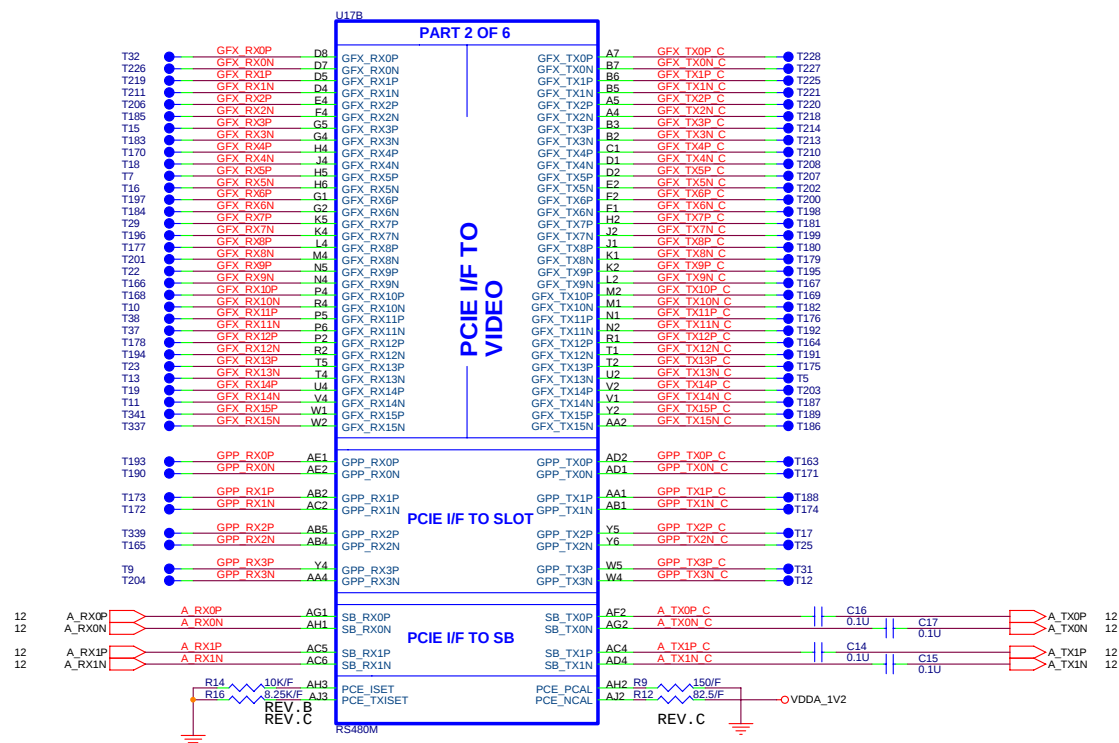
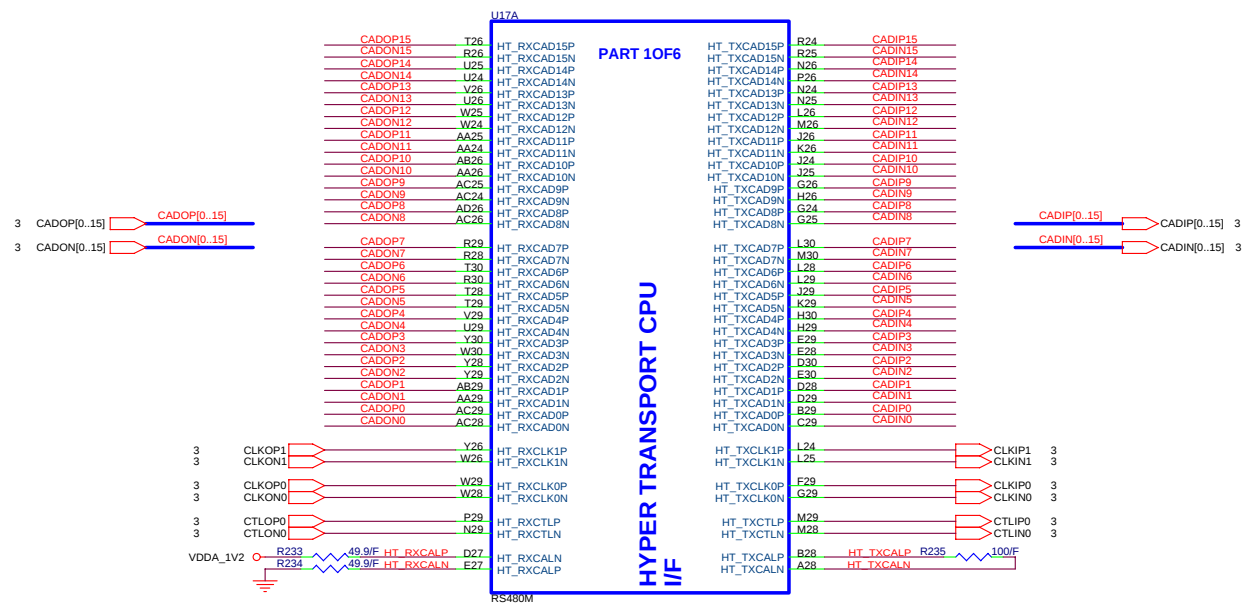
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

CPU

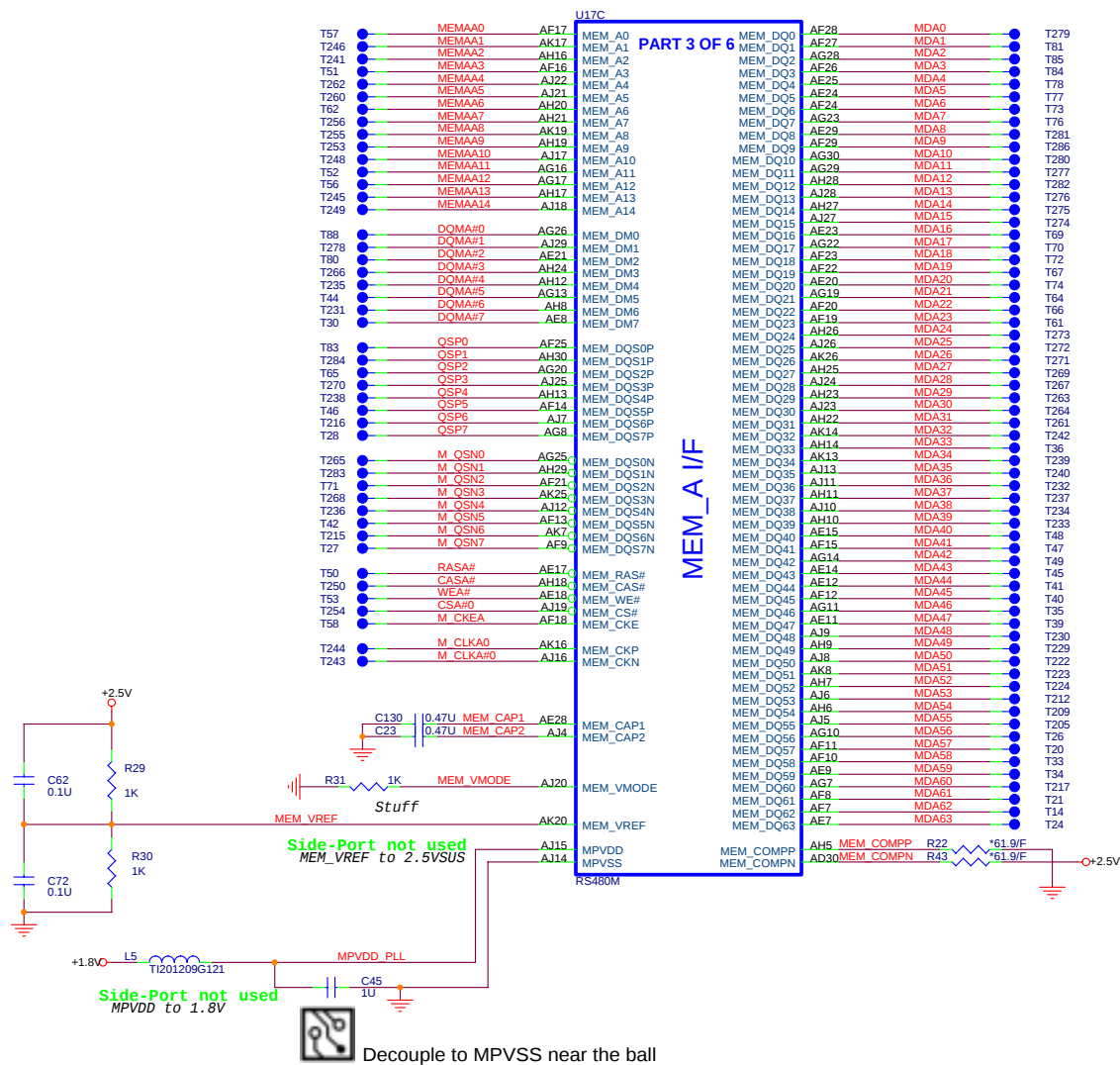


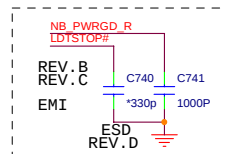
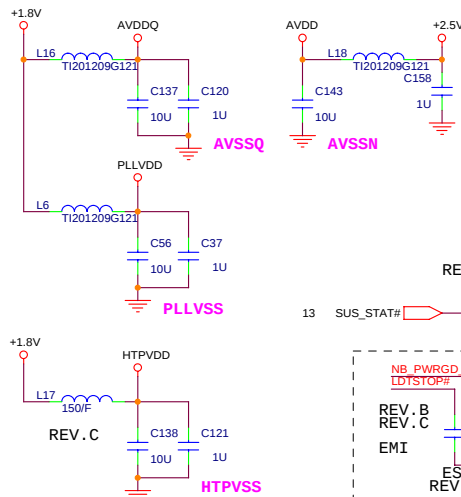
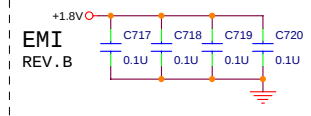
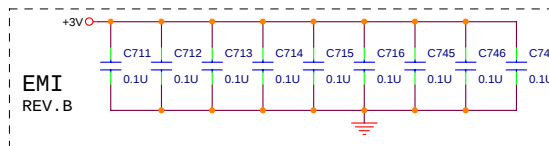
CPU





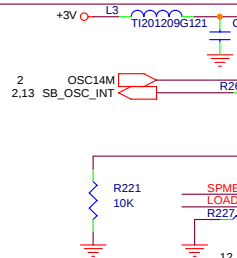
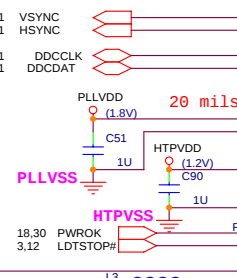
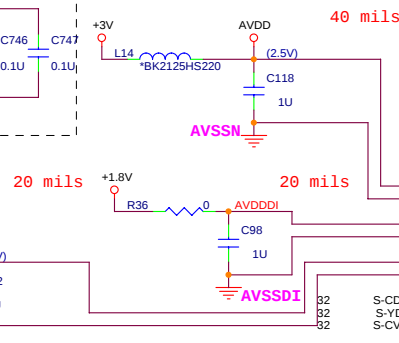
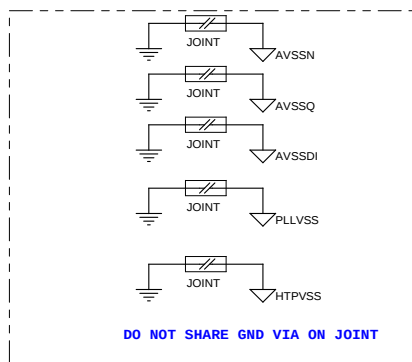
PROJECT : CT8
Quanta Computer Inc.





AVDD DAC VDD (2.5V)
 AVDDDI DIGITAL VDD (1.8V)
 AVDDQ DAC2 BANDGAP REF (1.8V)
 PLLVDD PLL VDD (1.8V)
 HTPVDD HT PLL VDD (1.8V)

PUT AVDD, AVDDDI, AVDDQ, PLLVDD, HTPVDD
 DECOUPLING CAPS ON THE BOTTOM, CLOSE
 TO BALLS



ROUTING H_THRMDA AND HW_AGND AS DIFFERENTIAL PAIR

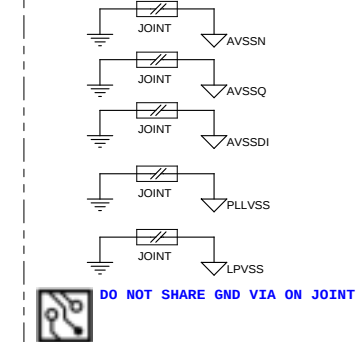
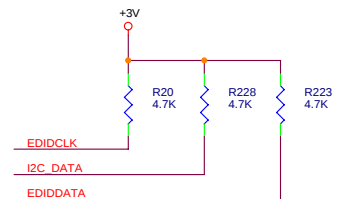
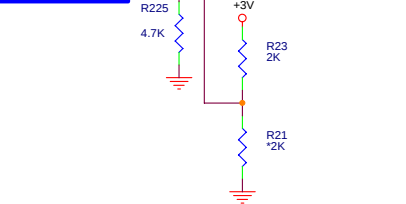
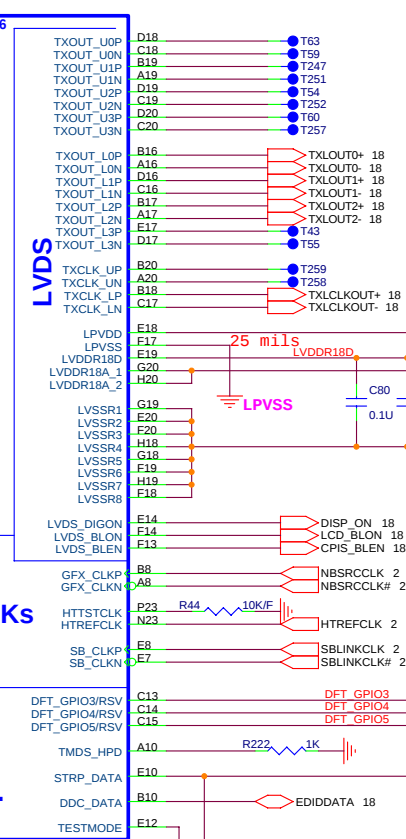
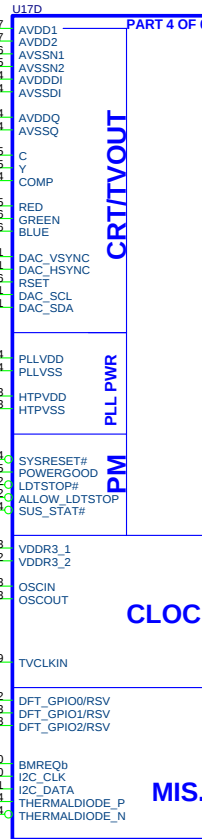
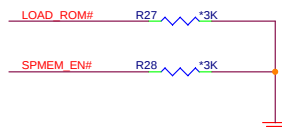
REV.B DEL Y1 AND U3 CIRCUIT.

LOAD_ROM#:LOAD ROM STRAP ENABLE strap

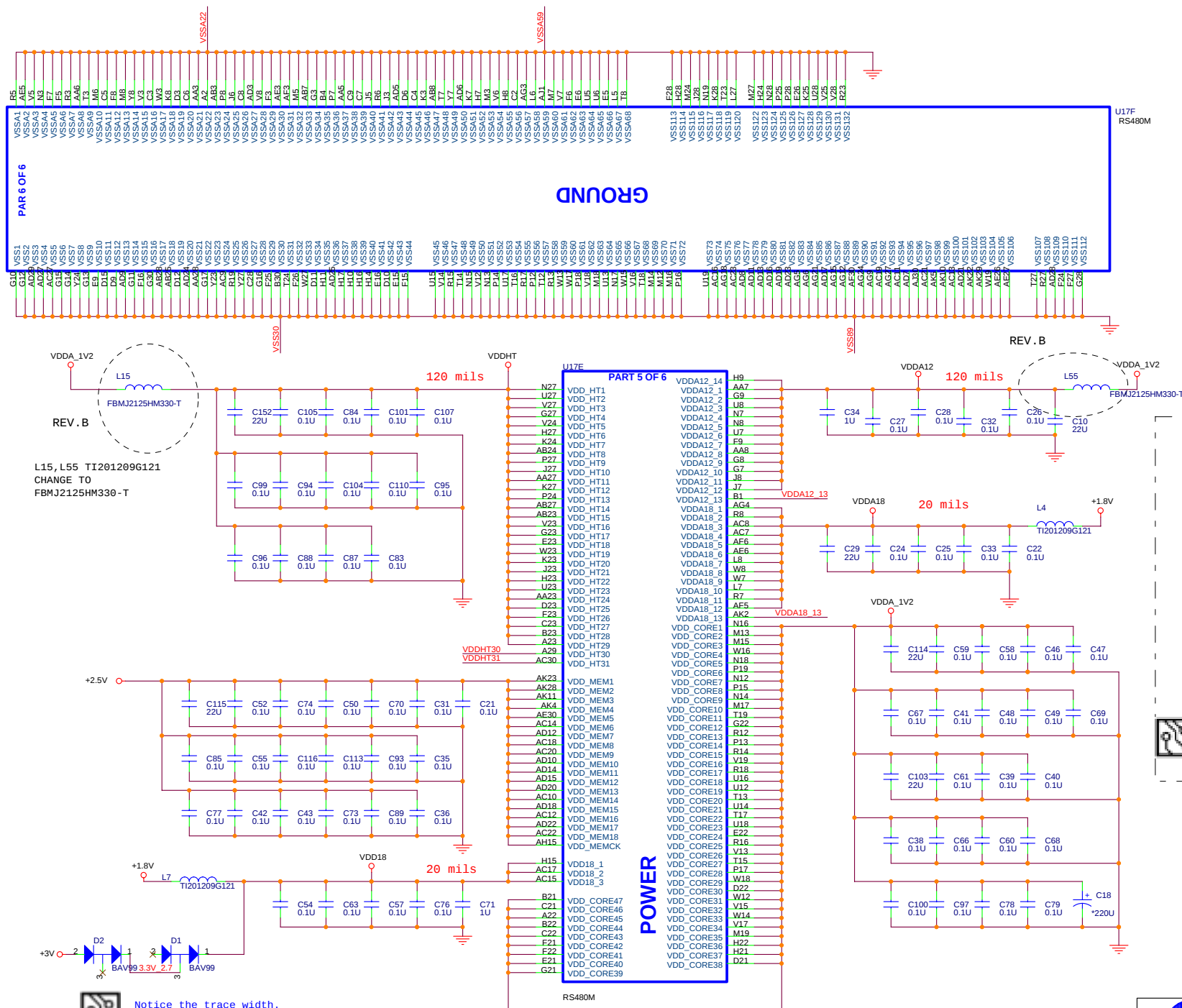
High, LOAD ROM STRAP DISABLE
 Low, LOAD ROM STRAP ENABLE

SPMEM_EN#:SIDE PORT MEMORY ENABLE strap

NC, SIDE PORT MEMORY DISABLE
 Low, SIDE PORT MEMORY ENABLE



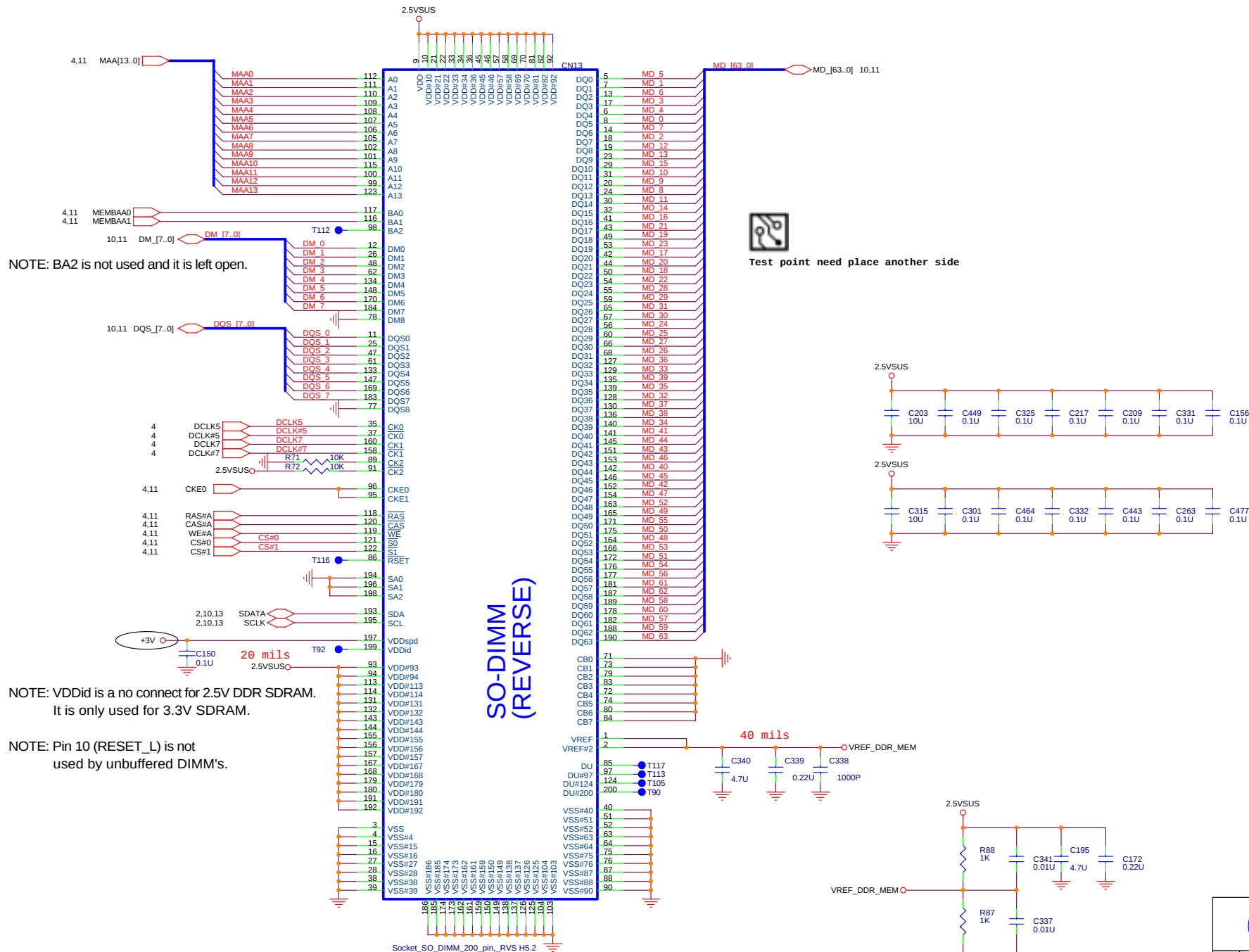
CLG

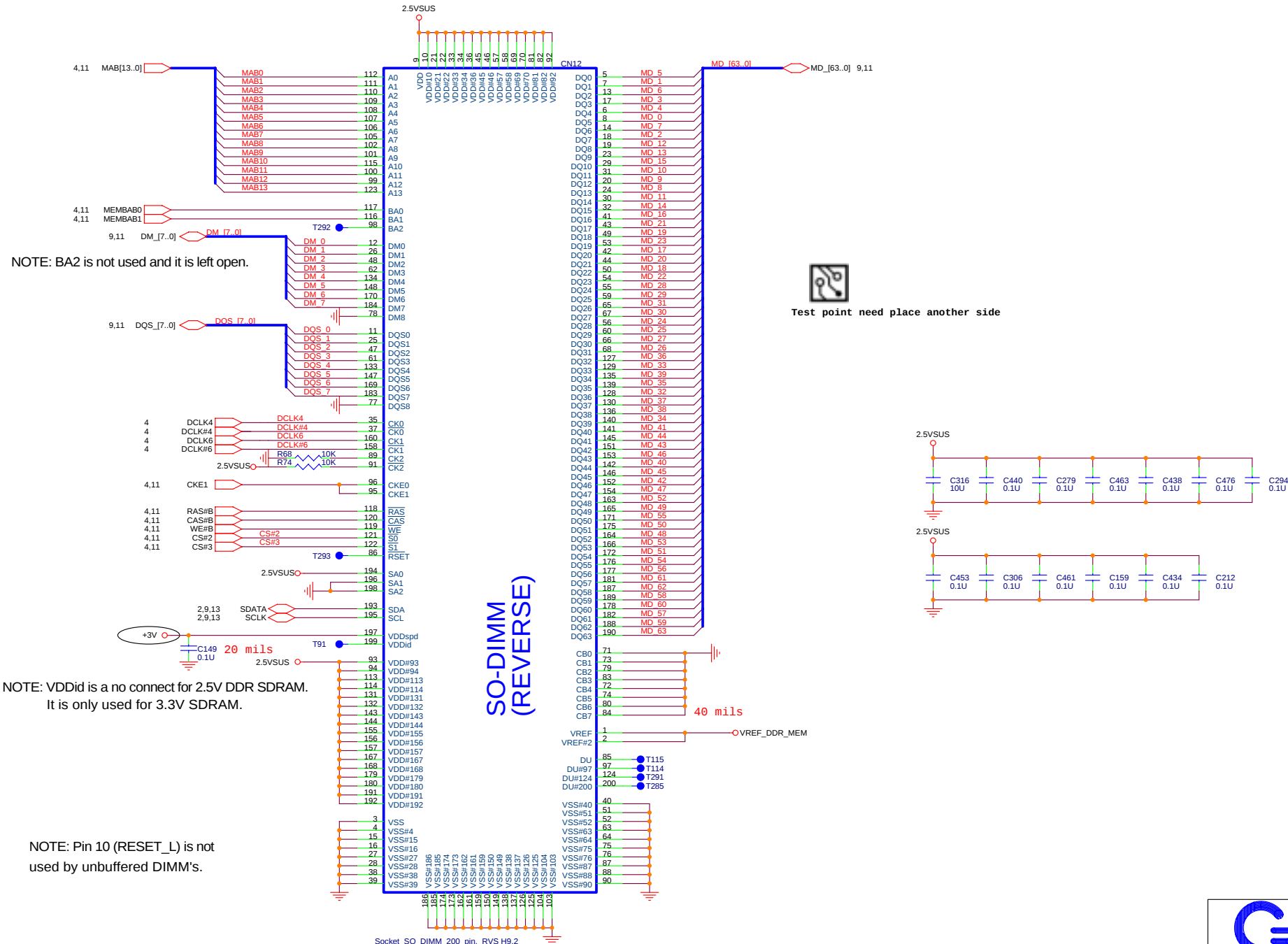


NB RS480 POWER STATES						
Power Signal	S0	S1	S3	S4/S5	63	
VDDHT	ON	ON	OFF	OFF	OFF	
VDDR, VDDRCK	ON	ON	ON	ON	OFF	
VDD18	ON	ON	OFF	OFF	OFF	
VDDC	ON	ON	OFF	OFF	OFF	
VDDA18	ON	ON	OFF	OFF	OFF	
VDDA12	ON	ON	OFF	OFF	OFF	
AVDD	ON	ON	OFF	OFF	OFF	
AVDDDI	ON	ON	OFF	OFF	OFF	
PLLVD	ON	ON	OFF	OFF	OFF	
HTPVDD	ON	ON	OFF	OFF	OFF	
VDDR3	ON	ON	OFF	OFF	OFF	
LPVDD	ON	ON	OFF	OFF	OFF	
LVDDR18D	ON	ON	OFF	OFF	OFF	
LVDDR18A	ON	ON	OFF	OFF	OFF	

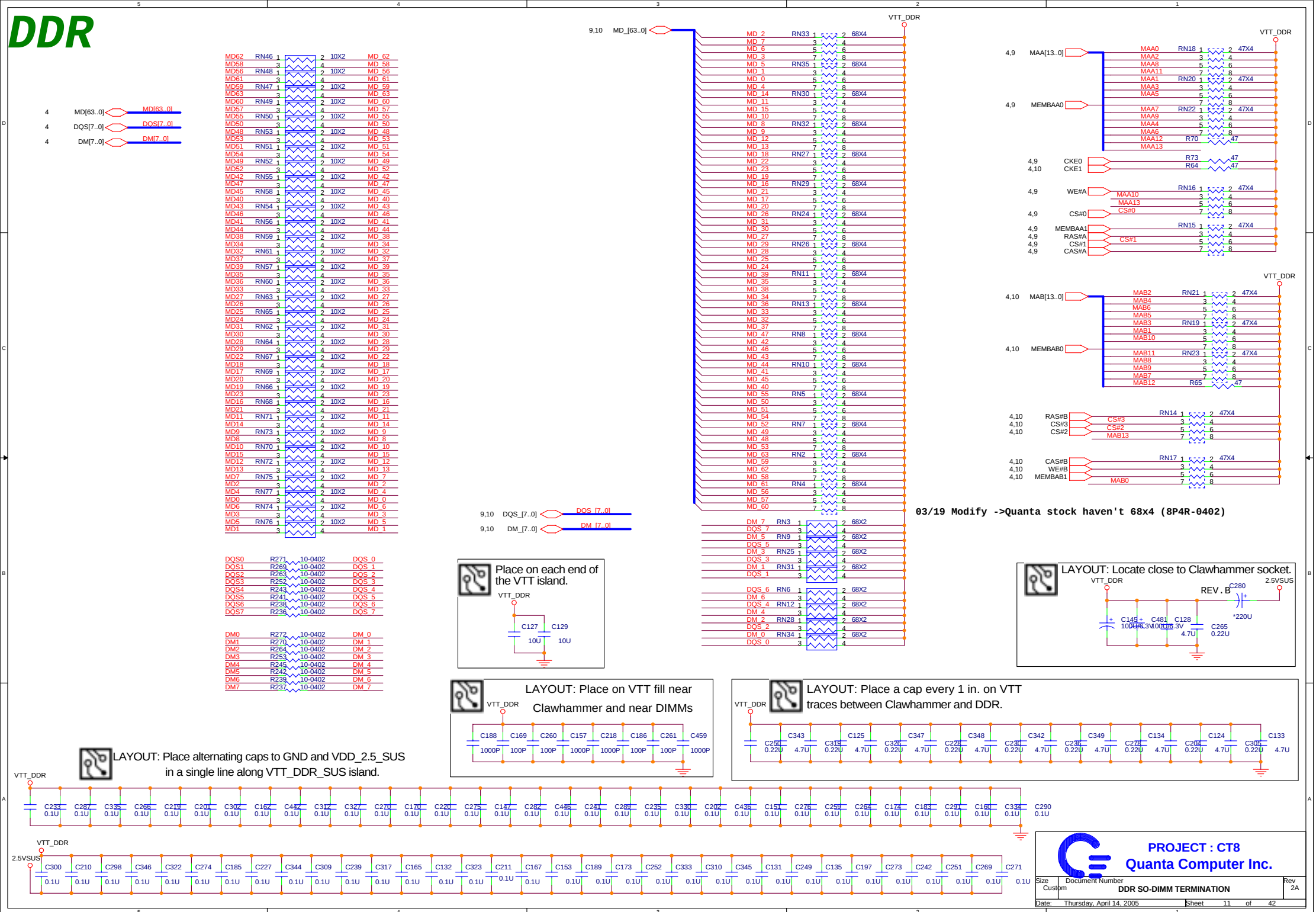


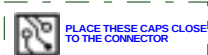
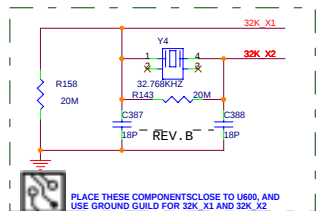
PUT DECOUPLING CAPS ON THE TOP, CLOSE TO BALLS
CONNECT VSSA22,VSSA59,VSS30,VSS89 to the ground.





Test point need place another side





REV.C

A_RX0P

A_RX0N

A_RX1P

A_RX1N

A_TX0P

A_TX0N

A_TX1P

A_TX1N

A_TX2P

A_TX2N

A_TX3P

A_TX3N

A_TX4P

A_TX4N

A_TX5P

A_TX5N

A_TX6P

A_TX6N

A_TX7P

A_TX7N

A_TX8P

A_TX8N

A_TX9P

A_TX9N

A_TX10P

A_TX10N

A_TX11P

A_TX11N

A_TX12P

A_TX12N

A_TX13P

A_TX13N

A_TX14P

A_TX14N

A_TX15P

A_TX15N

A_TX16P

A_TX16N

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A_TX18P

A_TX18N

A_TX19P

A_TX19N

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A_TX21P

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A_TX30N

A_TX31P

A_TX31N

A_TX32P

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A_TX162P

A_TX162N

A_TX163P

A_TX163N

A_TX164P

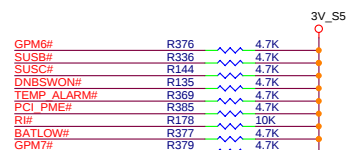
A_TX164N

A_TX165P

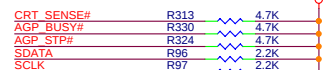
A_TX165N

A_TX166P

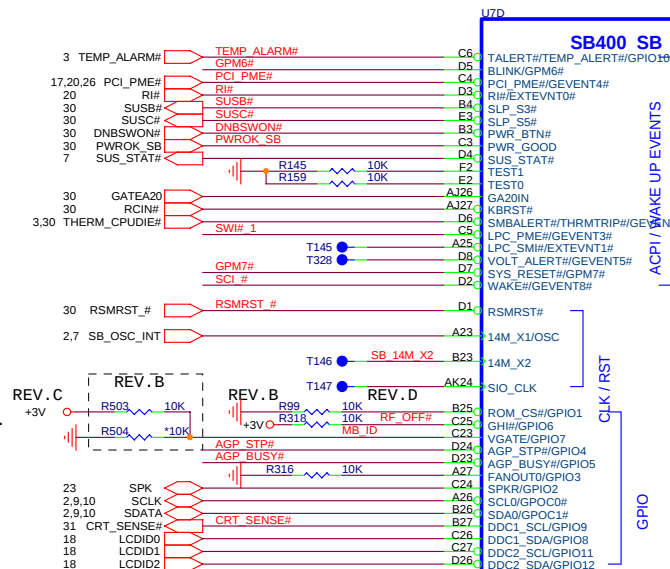
Please double check SB400 pin D5 & pin A27 define, because can't meet ATI library/symbols.



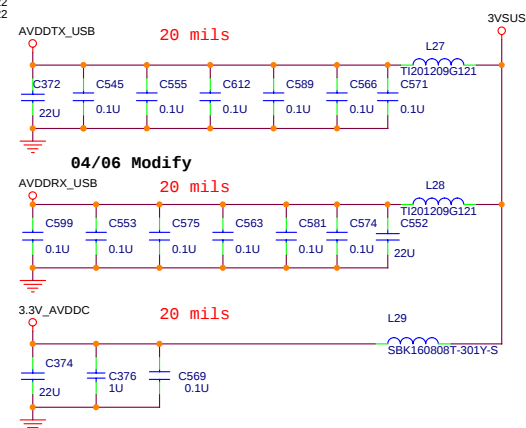
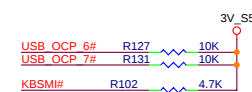
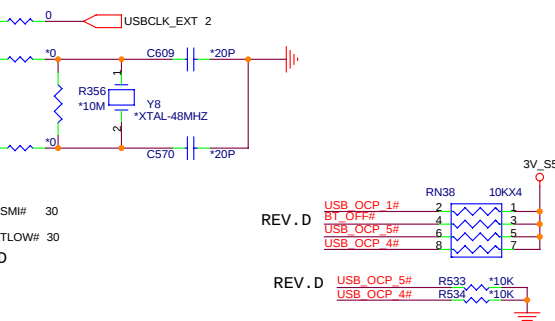
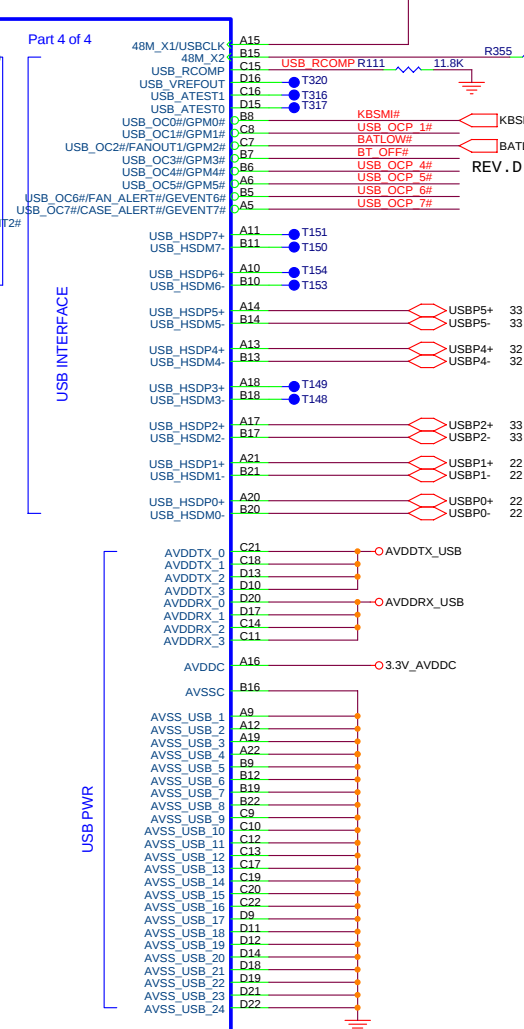
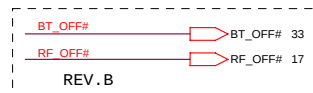
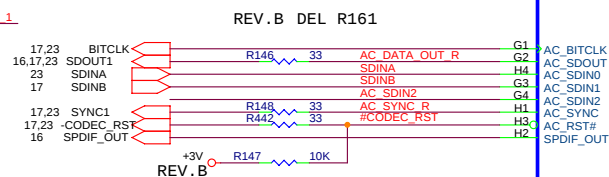
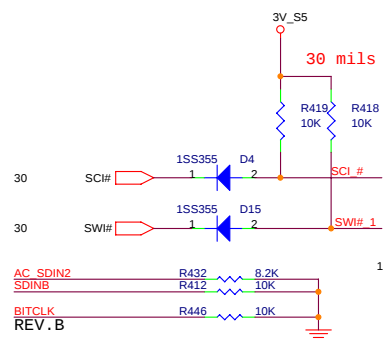
REV.B 1. Remove R400.



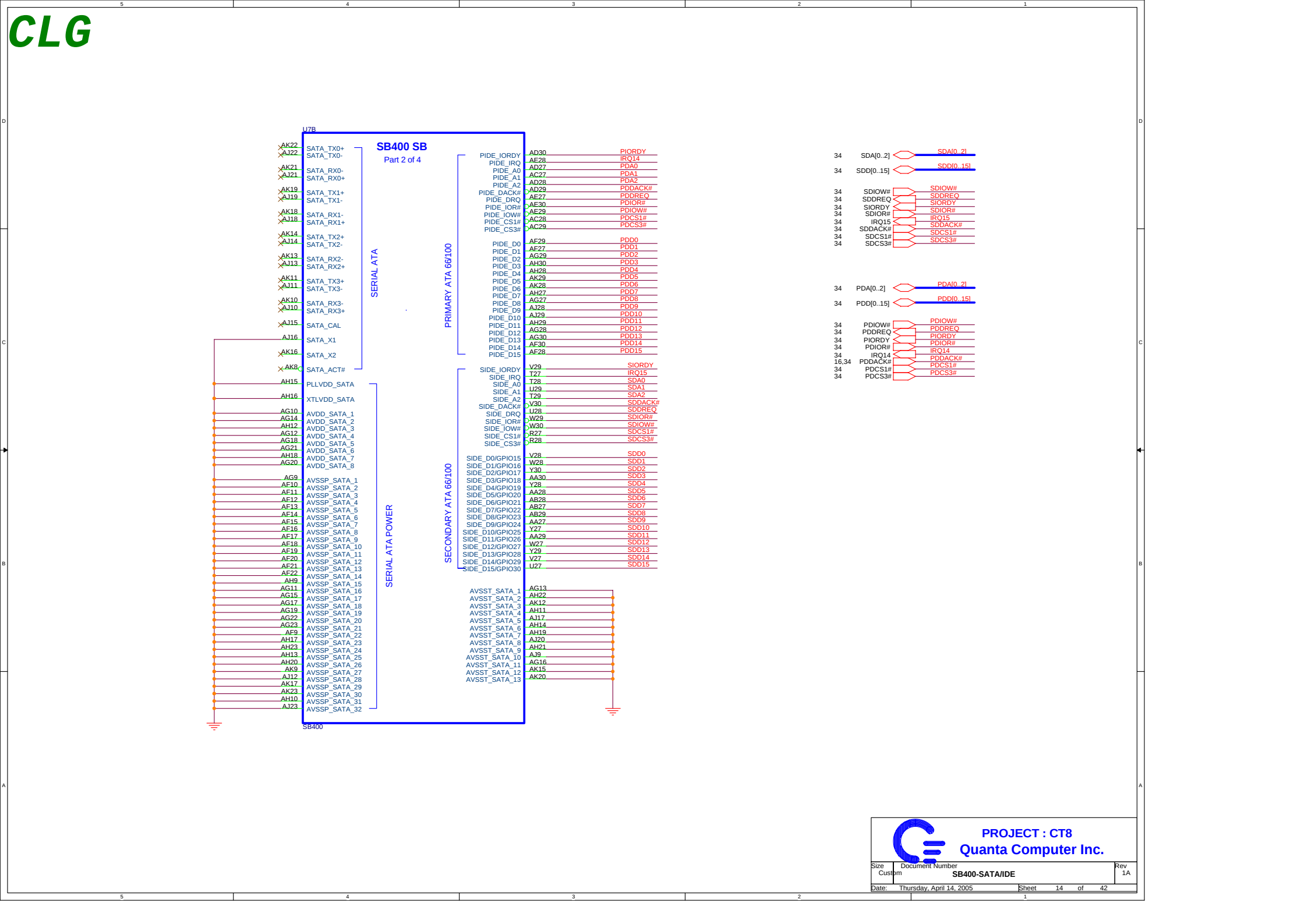
PWR0K_SB is 33ms ~
500ms after NB_PWRGD



R503 STUFF IS FULL FEATURE.
R504 STUFF IS DE-FEATURE.

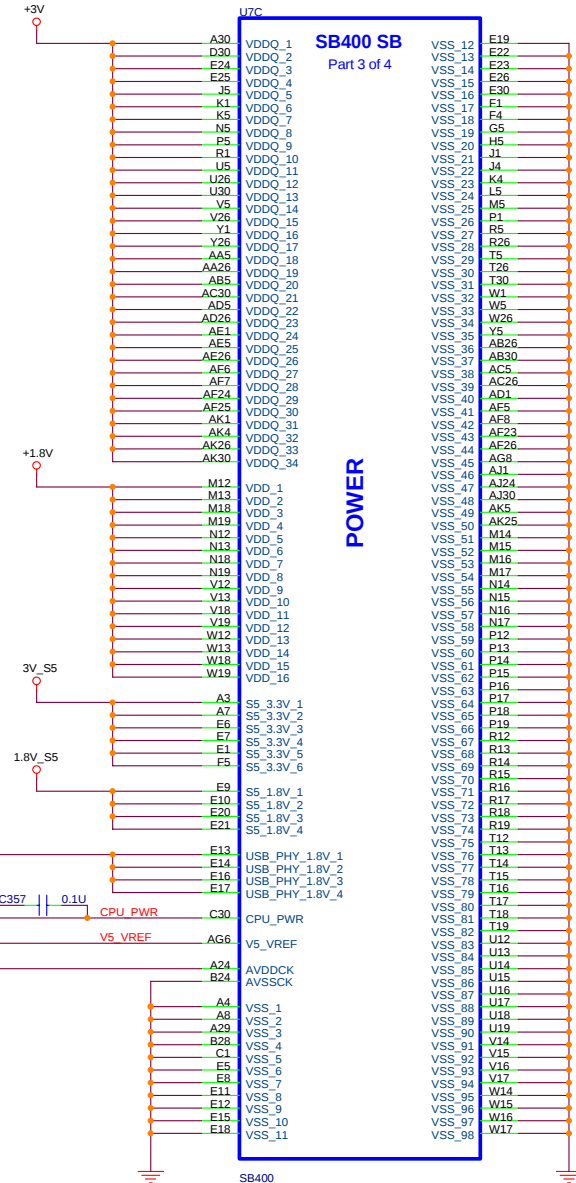
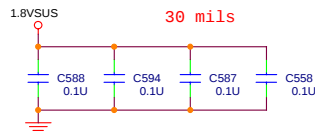
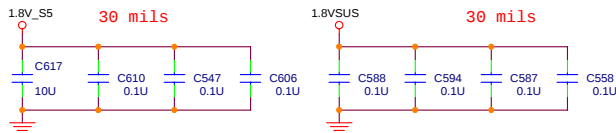
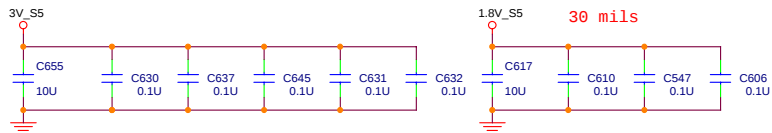
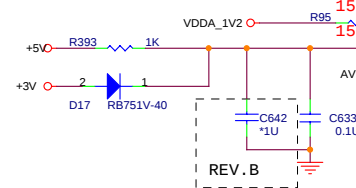
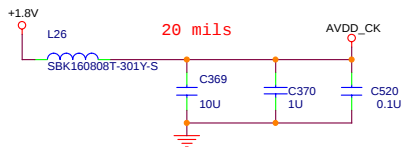
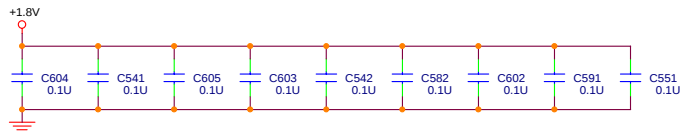
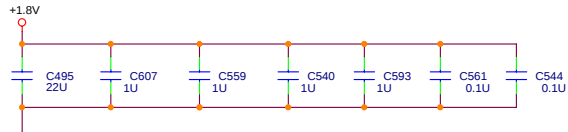
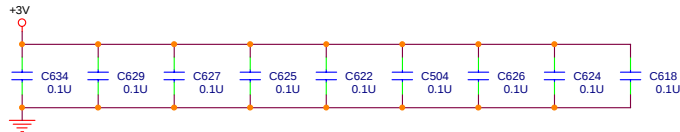
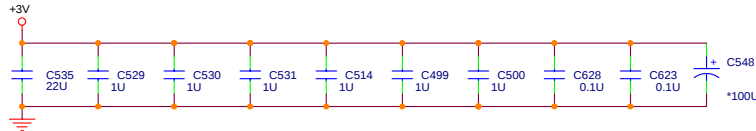


C641 AND C642 CLOSE
THE BALL A16 OF U60



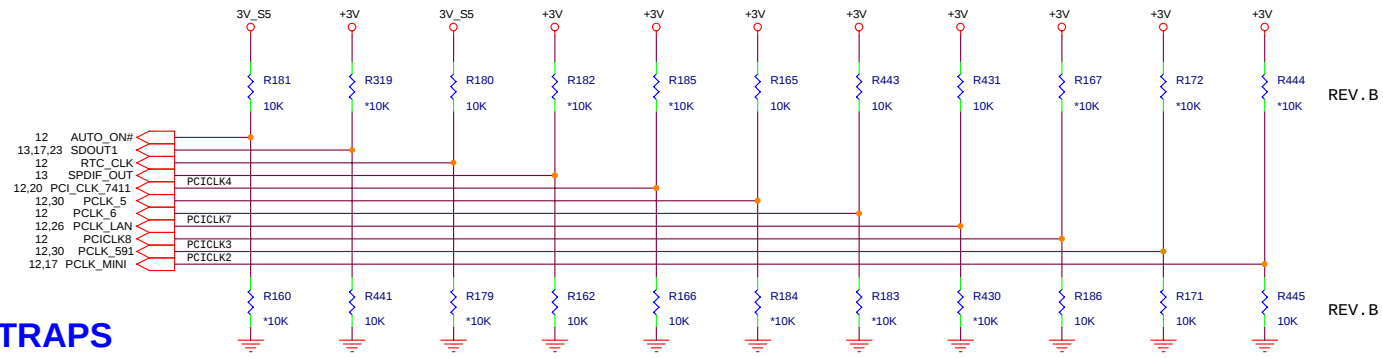


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



PROJECT : CT8
Quanta Computer Inc.

Size Custom	Document Number SB400-POWER & DECOUPLING	Rev 2A
Date: Thursday, April 14, 2005	Sheet 15 of 42	

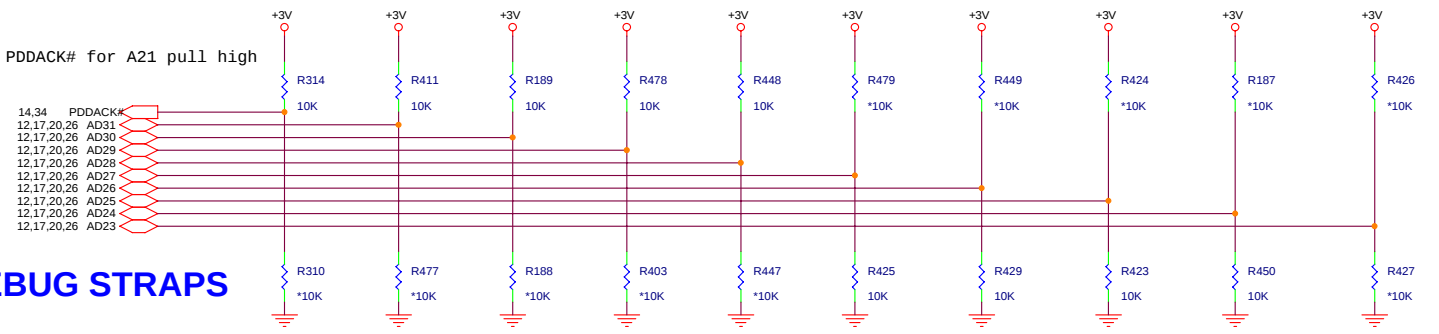


REQUIRED STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK_7411	PCLK_5	PCLK_6	PCLK_LAN	PCI_CLK8	PCLK_591
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz OSC MODE DEFAULT	14MHz OSC MODE DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM L,H = NORMAL LPC ROM L,L = FWH ROM	USB PHY PWRDOWN DISABLE DEFAULT	USB PHY PWRDOWN ENABLE
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz XTAL MODE	14MHz XTAL MODE	CPU I/F = P4			

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

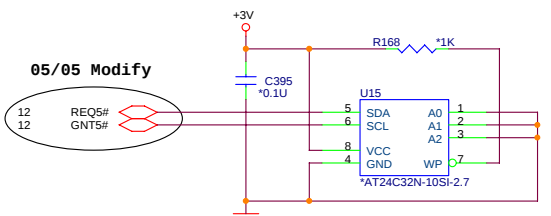
Need to check



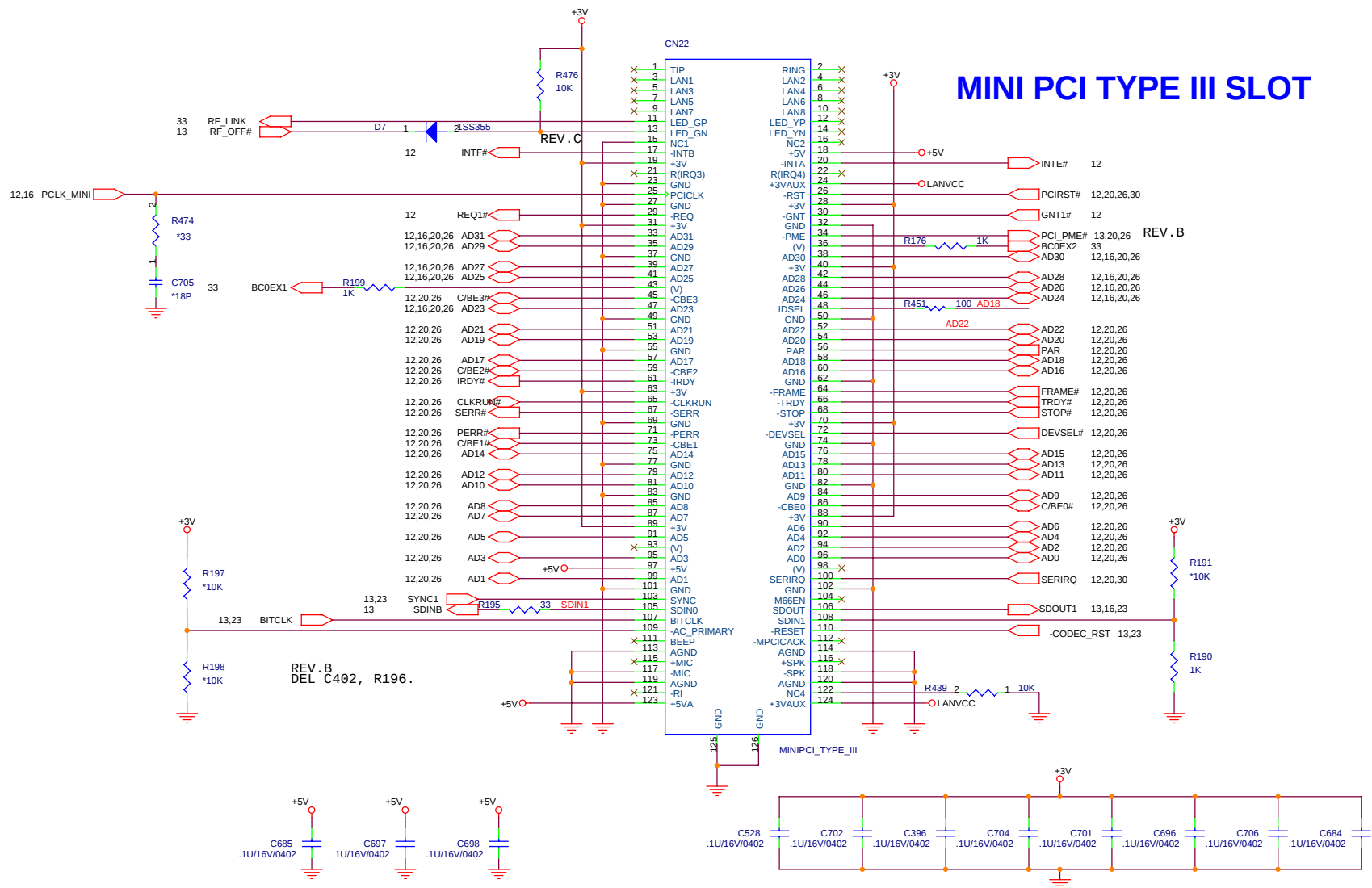
DEBUG STRAPS

	PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE SHORT RESET	PLL CHARGE PUMP CTRL BIT 1 HI DEFAULT	PLL CHARGE PUMP CTRL BIT 0 HI DEFAULT	PLL VCO CTRL BIT 1 HI DEFAULT	PLL VCO CTRL BIT 0 HI DEFAULT	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BY PASS USB PLL
PULL LOW	USE LONG RESET DEFAULT	PLL CHARGE PUMP CTRL BIT 1 LO	PLL CHARGE PUMP CTRL BIT 0 LO	PLL VCO CTRL BIT 1 LO	PLL VCO CTRL BIT 0 LO	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	USE USB PLL DEFAULT

Need to check

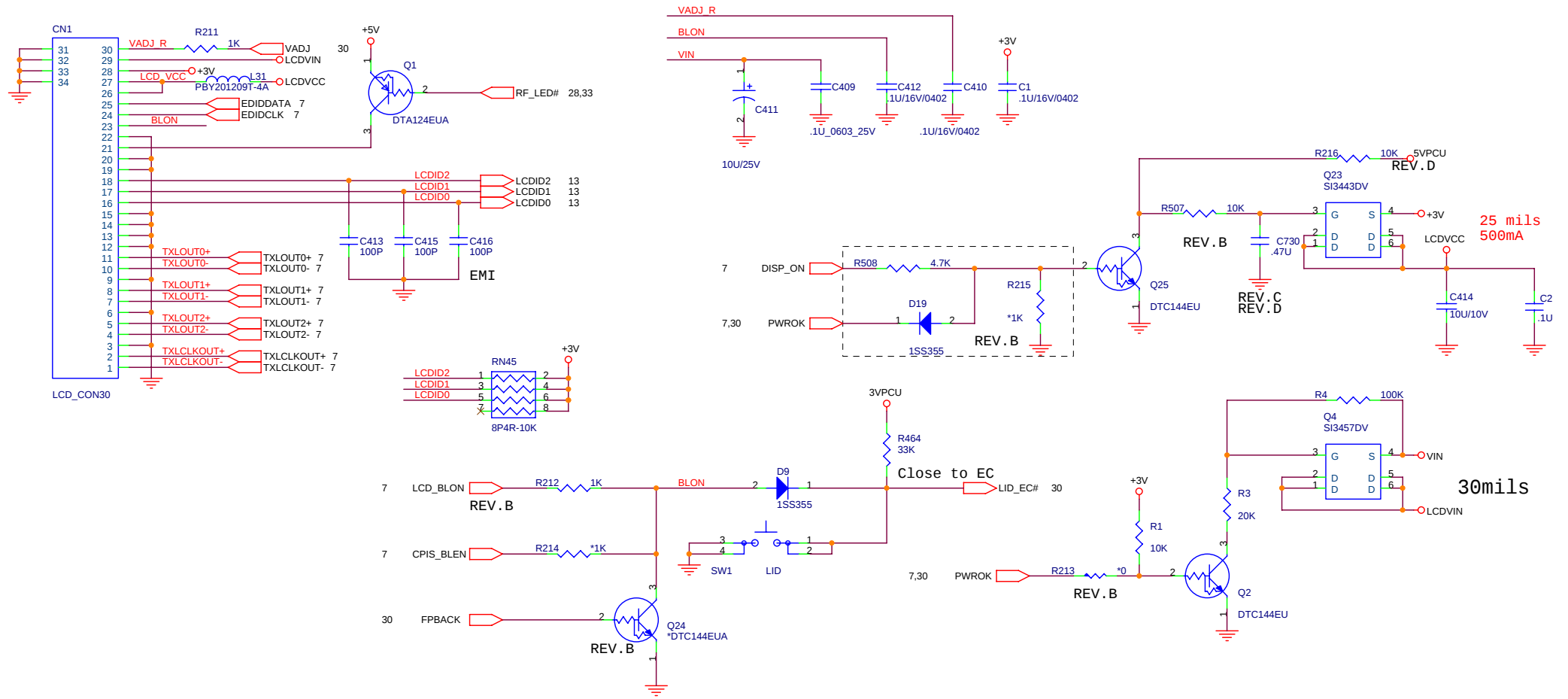


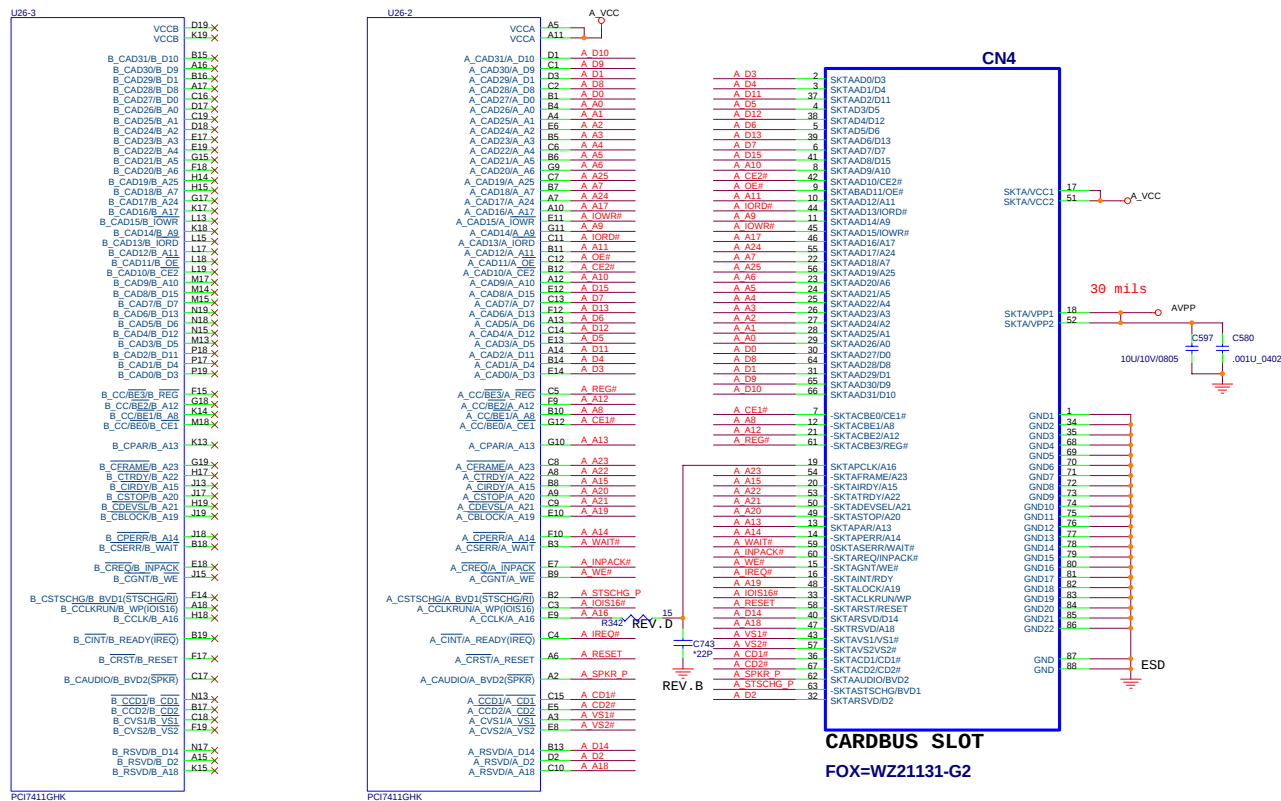
SB PCIE EEPROM STRAPS



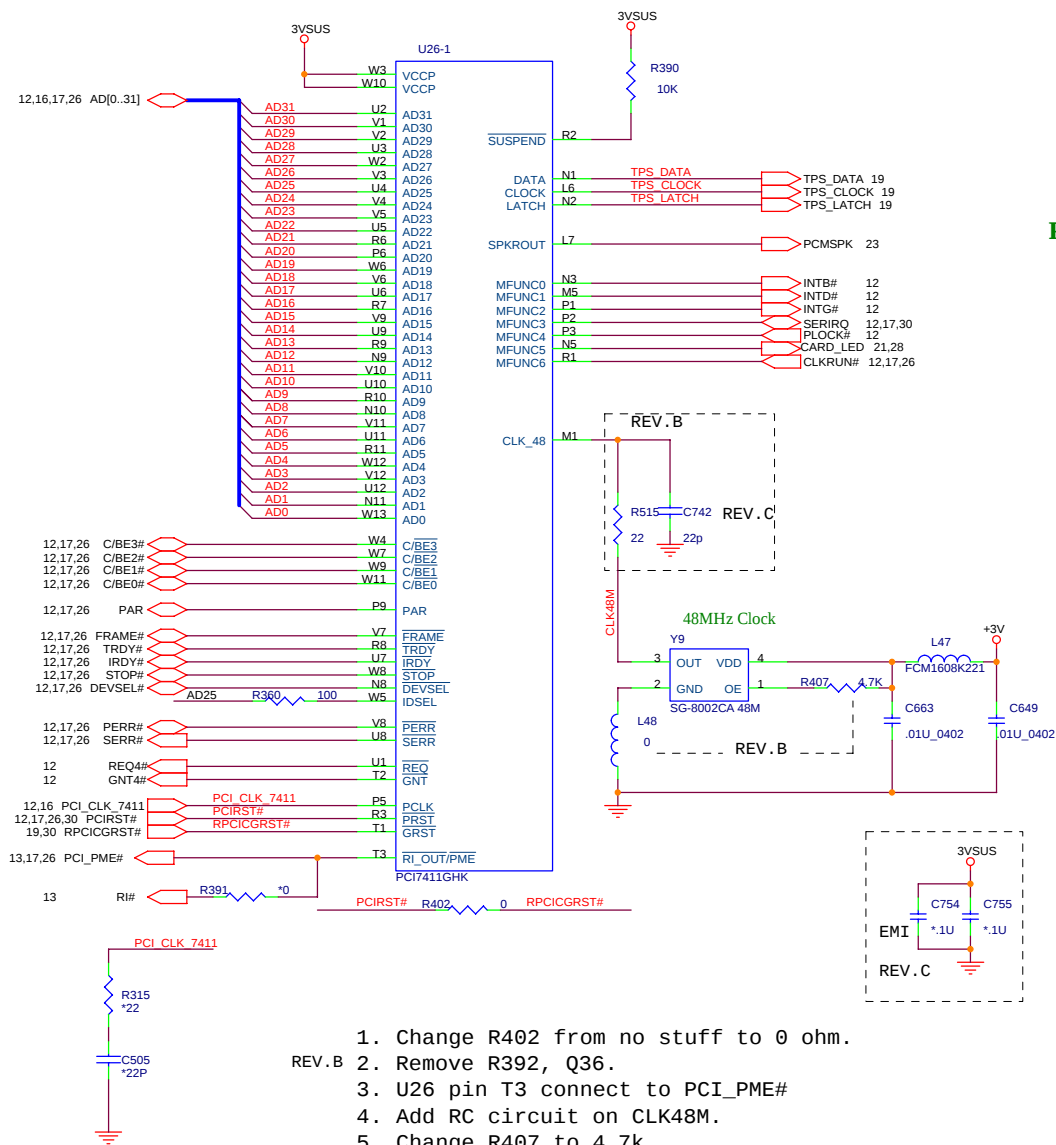
REV.B

1. Remove R175, Q19.
2. CN22 pin 34 connect to PCI_PME#.



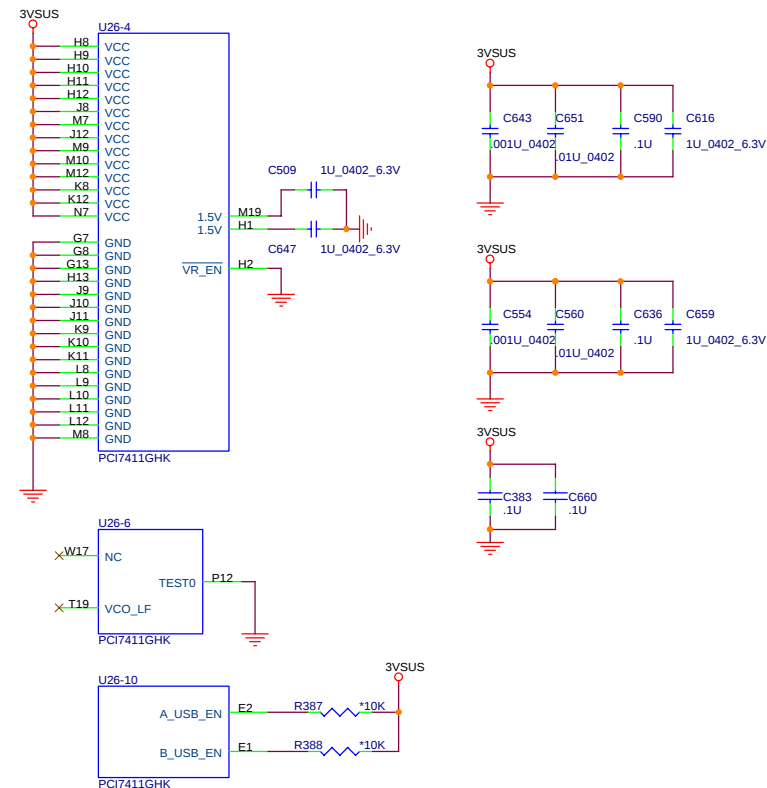


CardBus

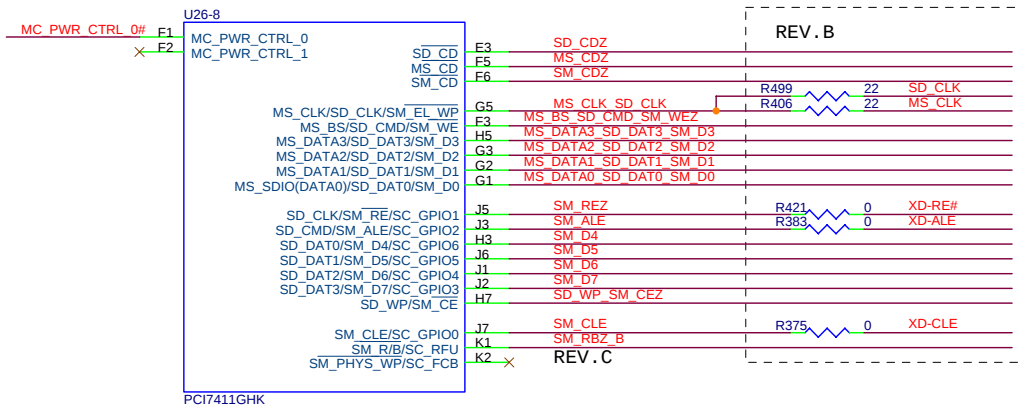


- REV.B
1. Change R402 from no stuff to 0 ohm.
 2. Remove R392, Q36.
 3. U26 pin T3 connect to PCI_PME#
 4. Add RC circuit on CLK48M.
 5. Change R407 to 4.7k.
 6. Change L48 to 0 ohm.

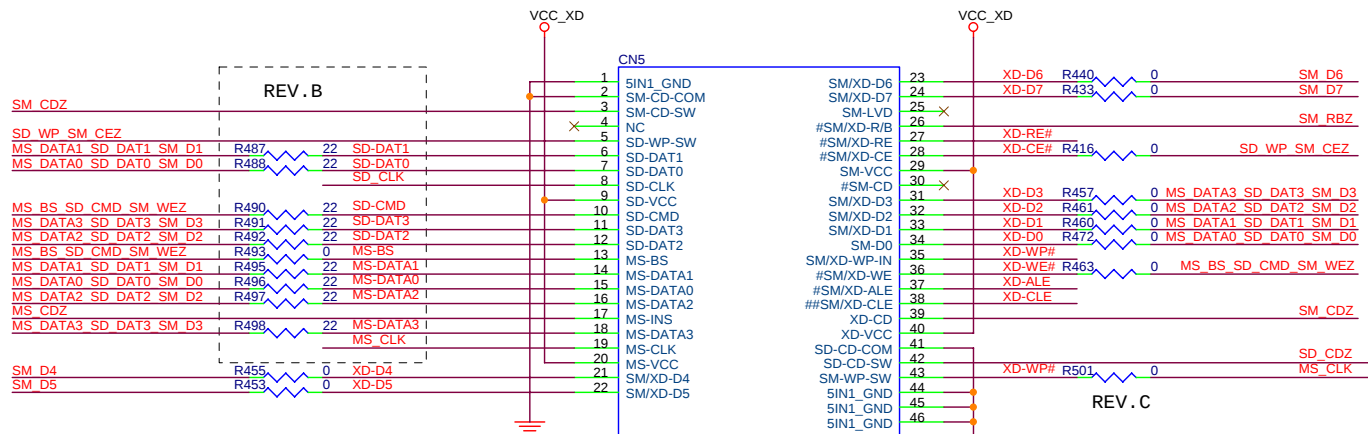
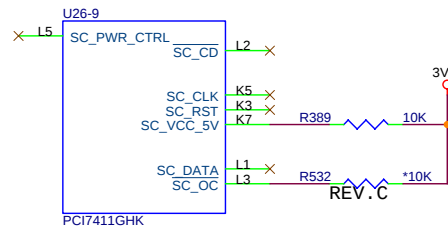
PCIXX21 Power Terminals



CARD POWER CONTROL



R499,421,383,375 move to chip side.

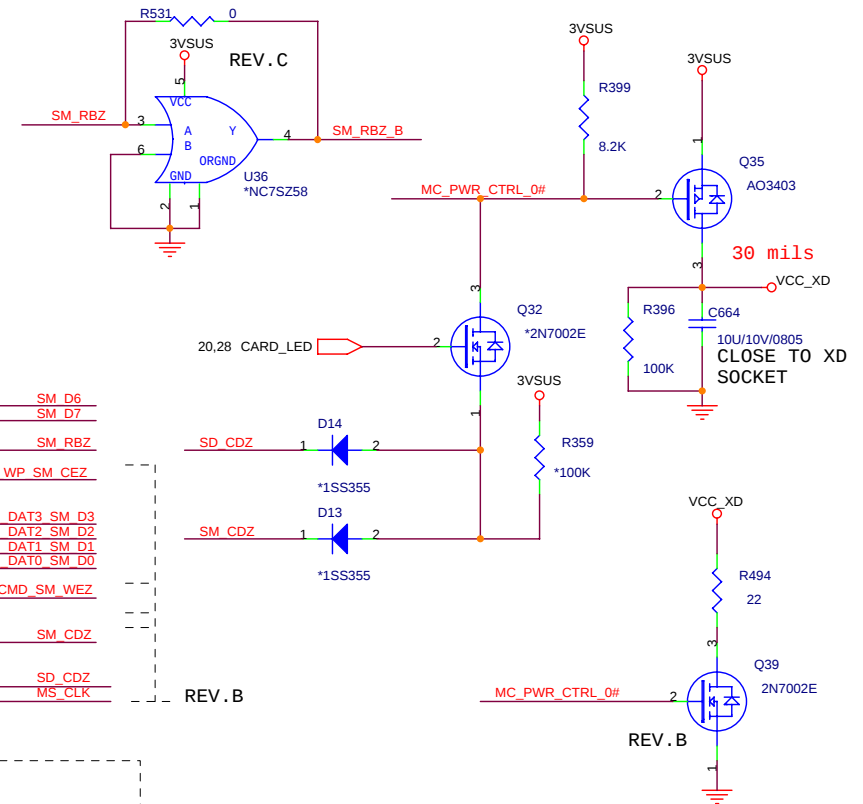
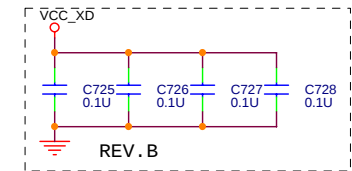
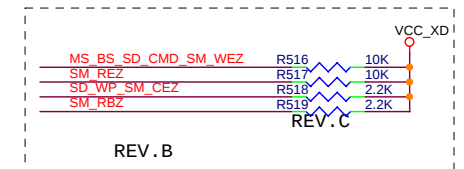


5 IN1 CARD READER

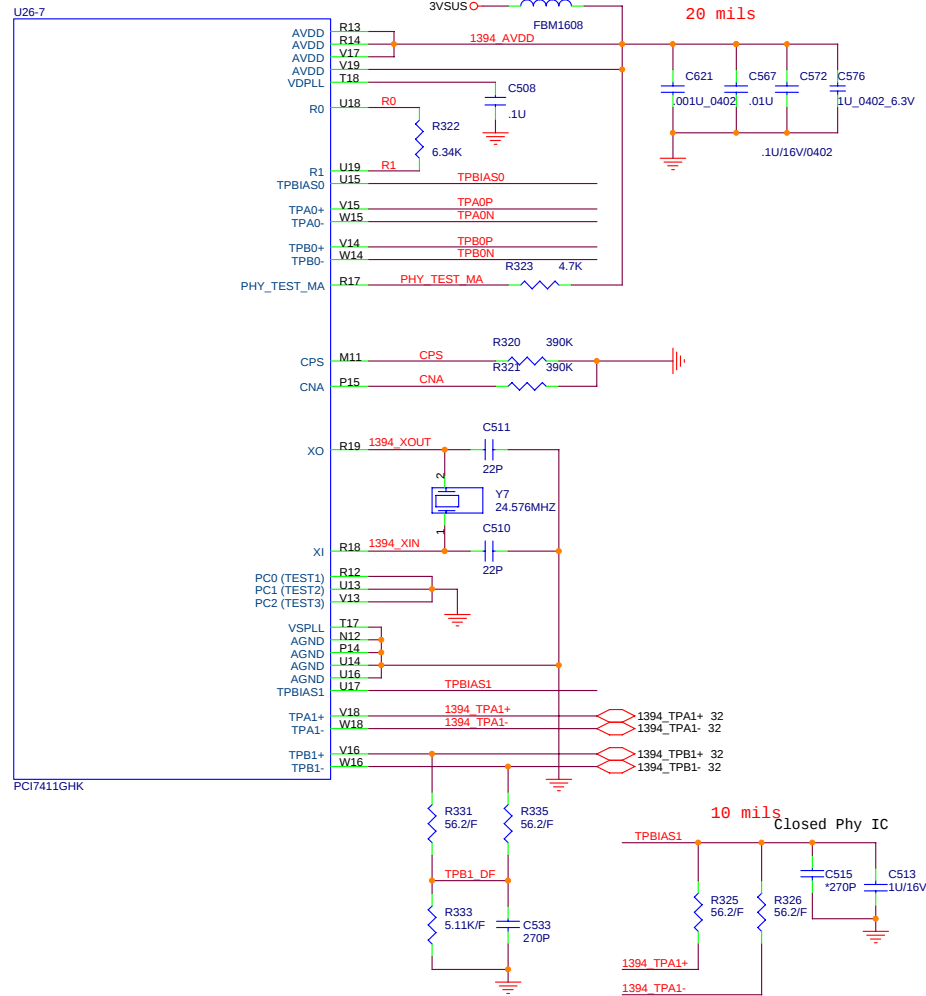
TAIWUN-R007-020-N5-44P rev.f

REV.B

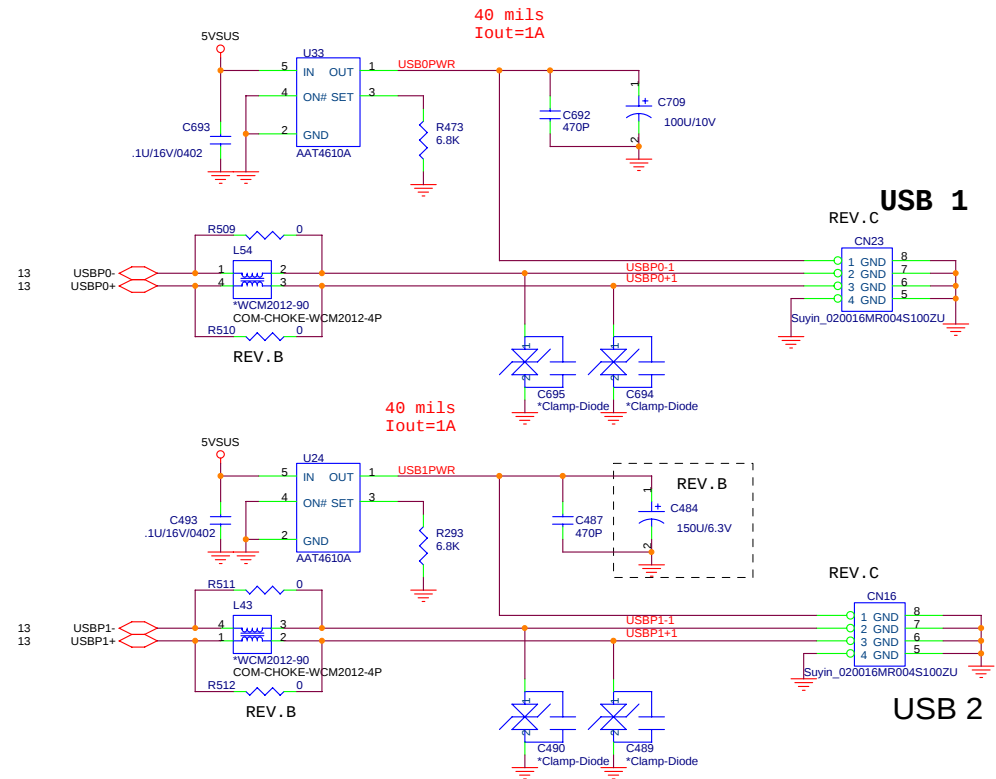
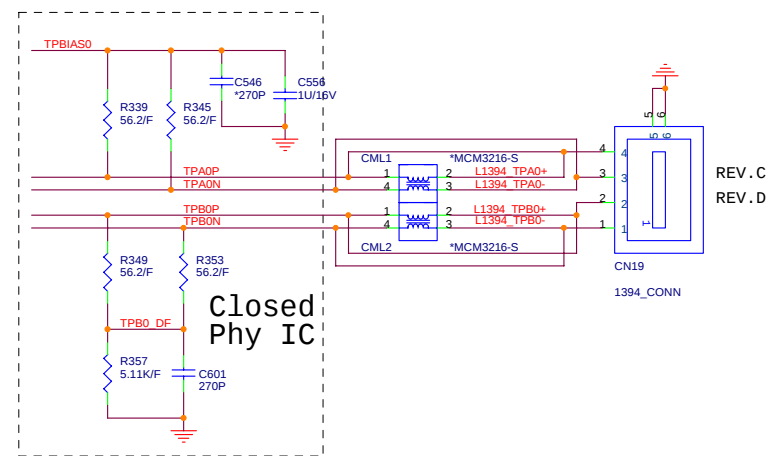
1. Remove R397, D16, R489.
2. Add a Quick Switch U34 to isolate clock.
3. Change R501 to 0 ohm.
4. CN5 pin 35, 43 connect to the same net.
5. ADD R516, R517, R518, R519.

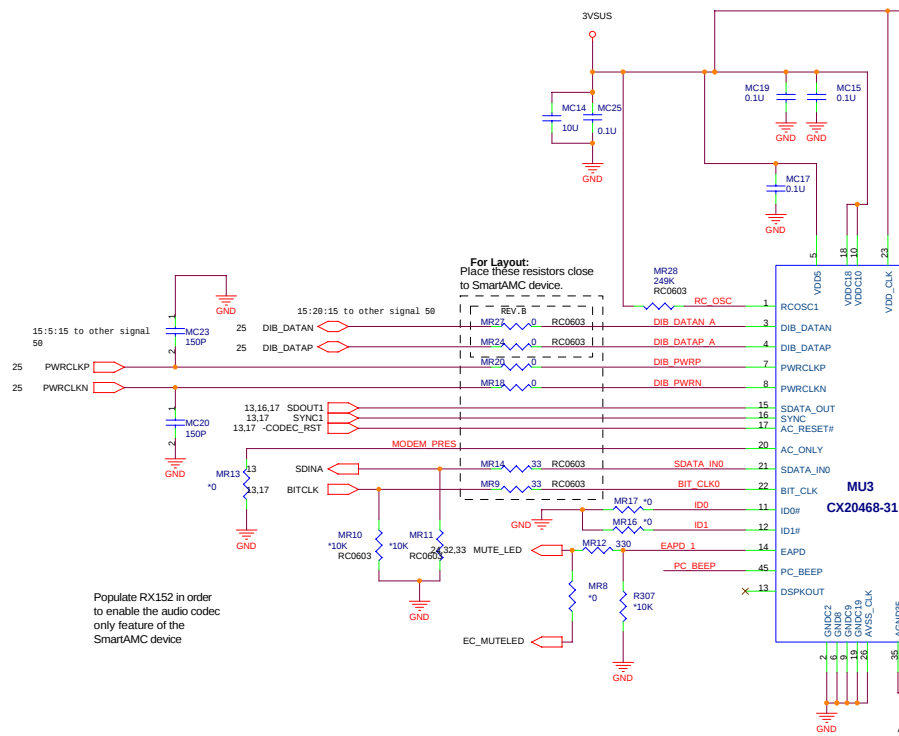


IEEE 1394a



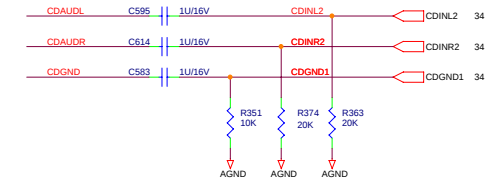
IEEE 1394 CONNECTOR



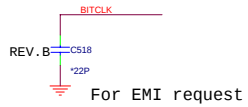
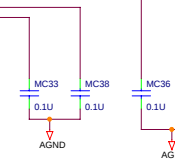


For Layout:
Place decoupling caps near the power pins of SmartAMC device.

FROM CD-ROM



For Layout:
Place CX132, CX133, CX135, CX136 near SmartAMC device

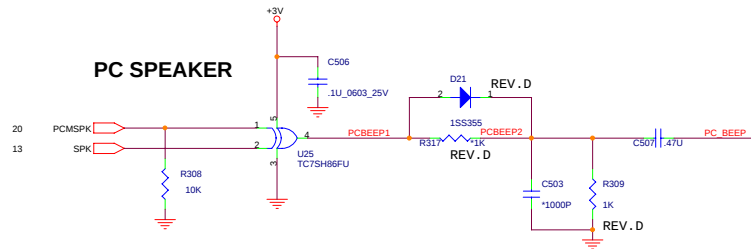


For Layout:

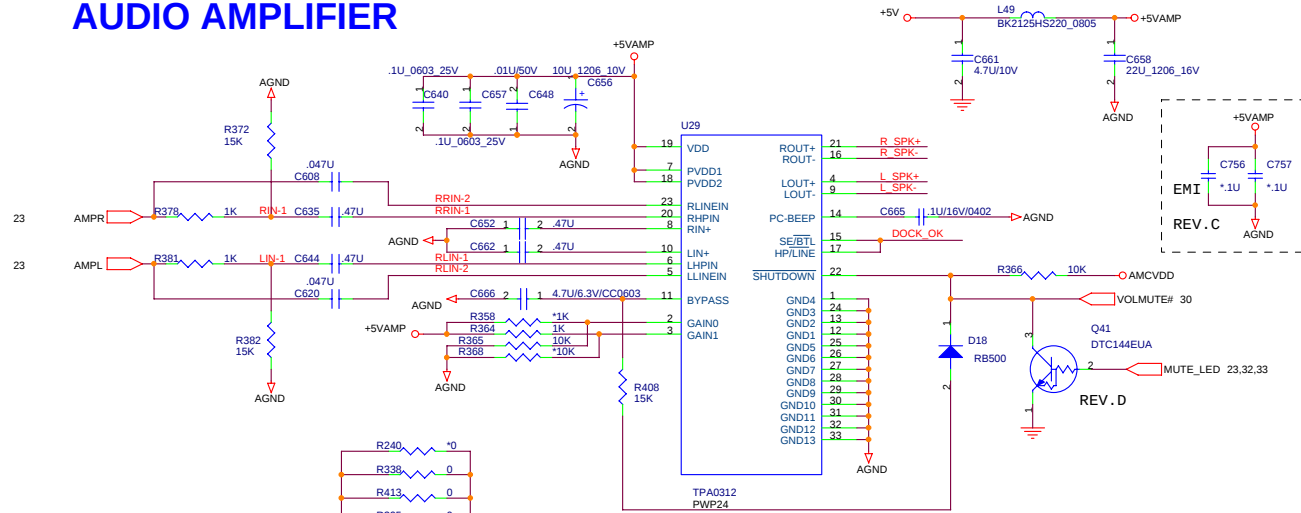
Place crystal and associated circuitry very near SmartAMC Device.

CX20468-21: ADD R20, MR8 REMOVE MR12, R413, D24, MR30, MR31 REV:B SETTING
CX20468-31: ADD MR12, R413, D24, MR30 REMOVE R20, MR31, MR8
CX20468-31 without software EQ: ADD MR12, MR31, MR30 REMOVE R413, D24, MR8, R20

PC SPEAKER



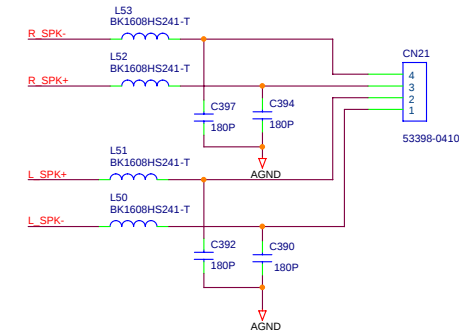
AUDIO AMPLIFIER



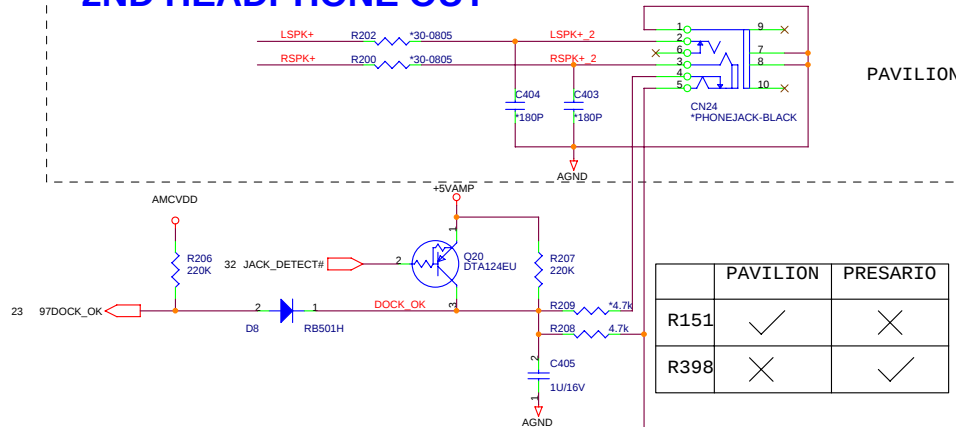
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

SPEAKER OUT

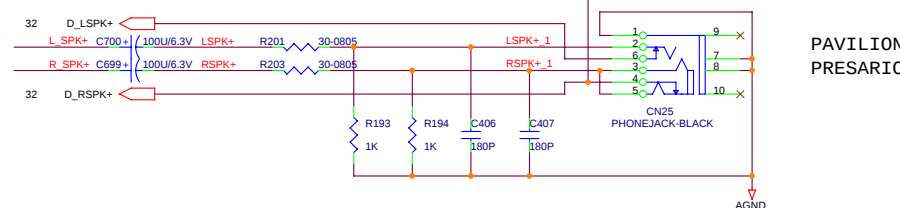


2ND HEADPHONE OUT

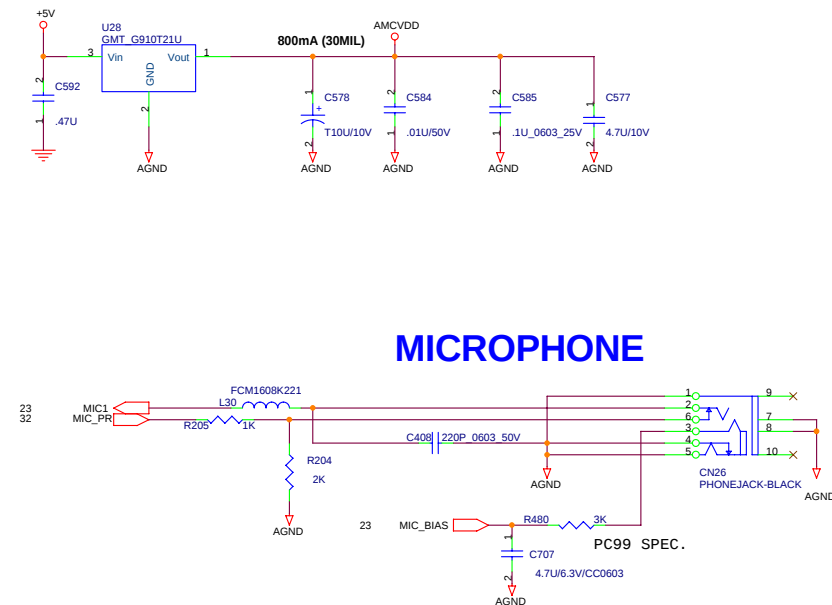


	PAVILION	PRESARIO
R151	✓	✗
R398	✗	✓

HEADPHONE OUT



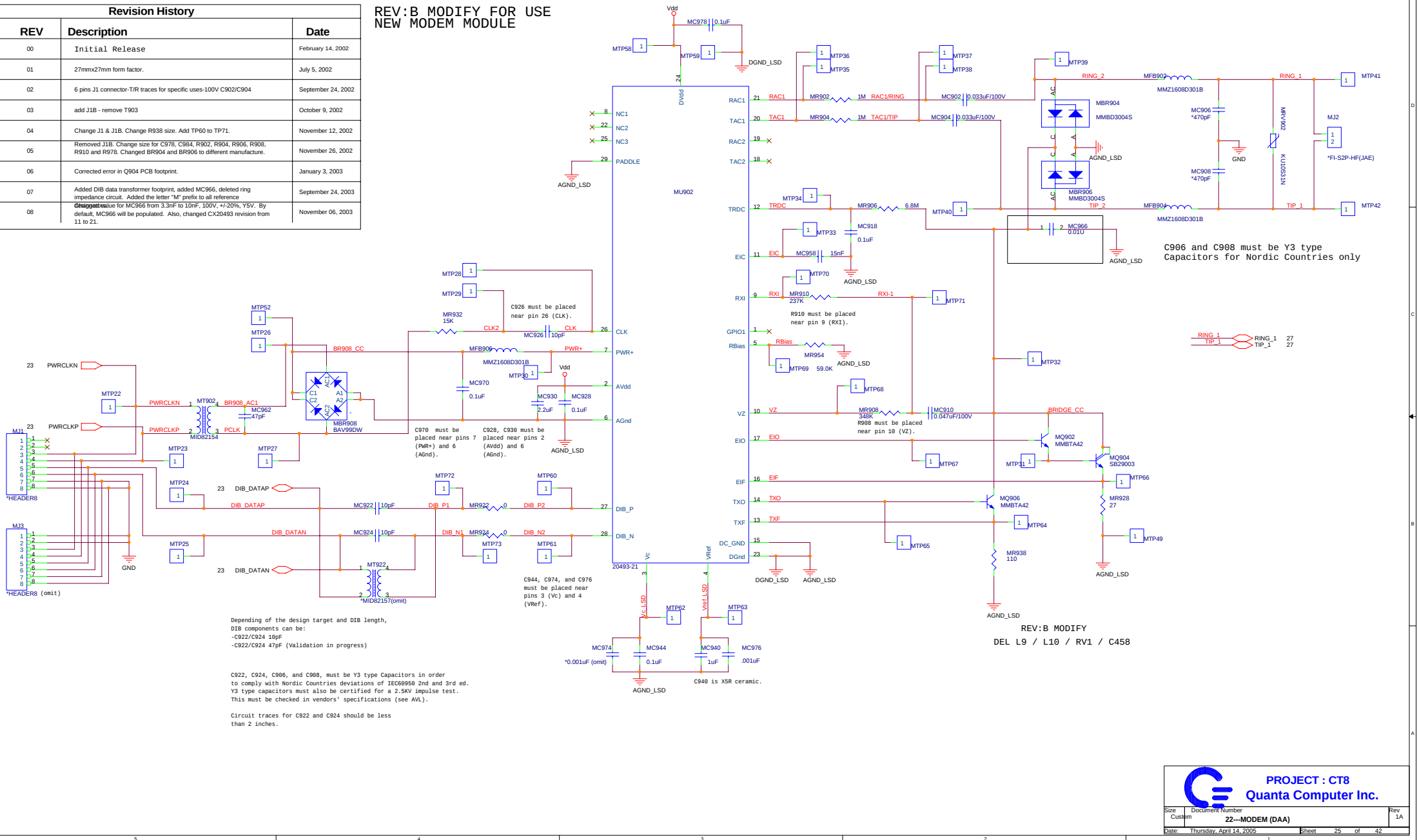
MICROPHONE

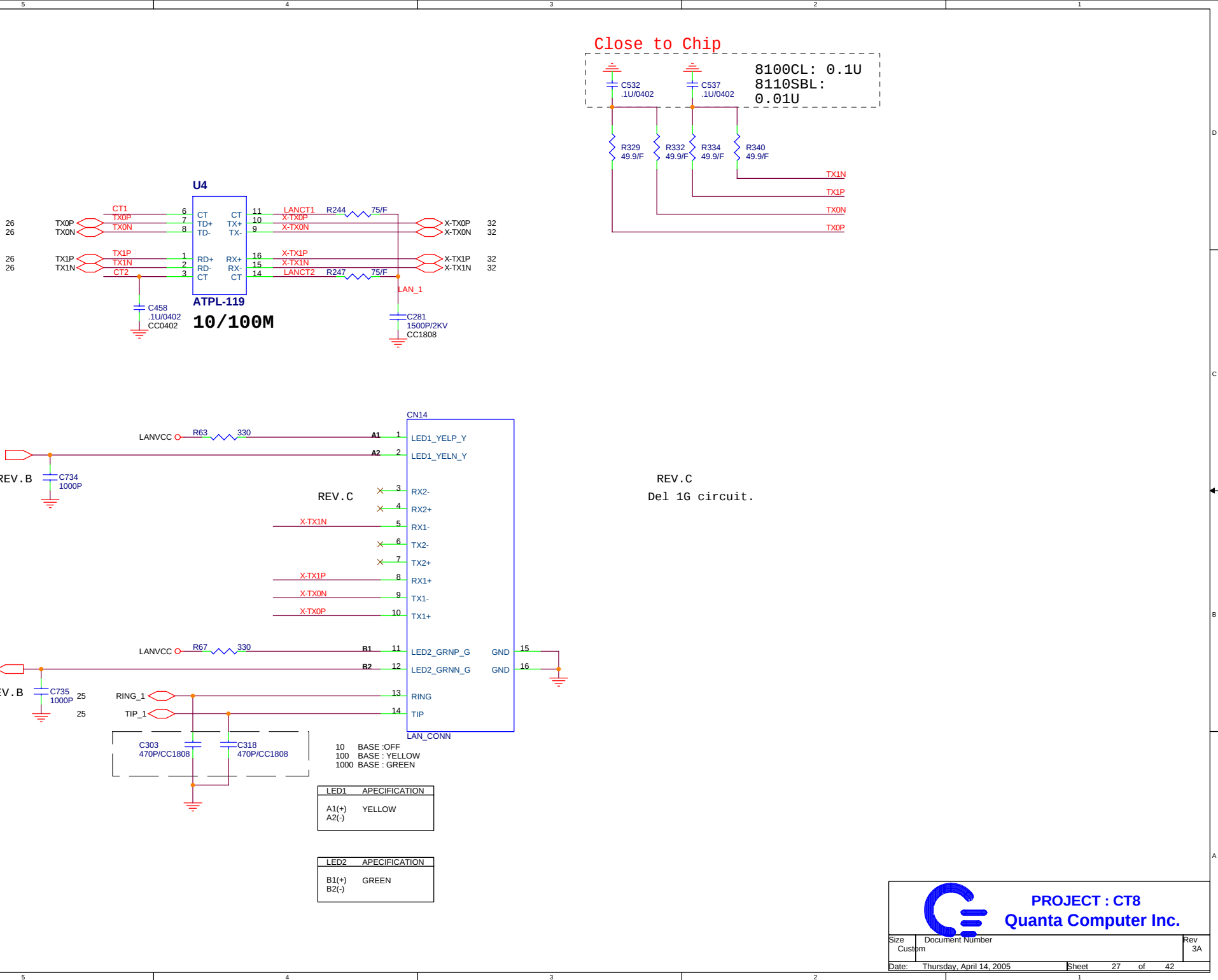


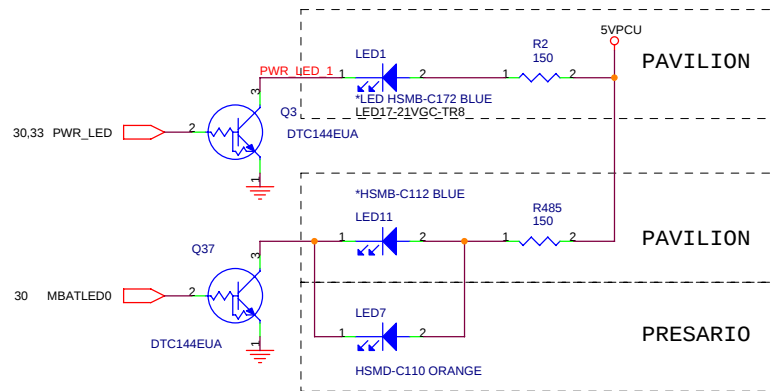
PROJECT : CT8
Quanta Computer Inc.

Revision History		
REV	Description	Date
00	Initial Release	February 14, 2002
01	27mmx27mm form factor.	July 5, 2002
02	6 pins J1 connector-T/R traces for specific uses-100V C902/C904	September 24, 2002
03	add J1B - remove T903	October 9, 2002
04	Change J1 & J1B. Change R938 size. Add TP60 to TP71.	November 12, 2002
05	Removed J1B. Change size for C978, C984, R902, R904, R906, R908, R910 and R978. Changed BR904 and BR906 to different manufacture.	November 26, 2002
06	Corrected error in Q904 PCB footprint.	January 3, 2003
07	Added DIB data transformer footprint, added MC966, deleted ring impedance circuit. Added the letter "M" prefix to all reference designators for MC986 from 3.3nF to 10nF, 100V, +/-20%, Y5V. By default, MC966 will be populated. Also, changed CX20493 revision from 11 to 21.	September 24, 2003
08		November 06, 2003

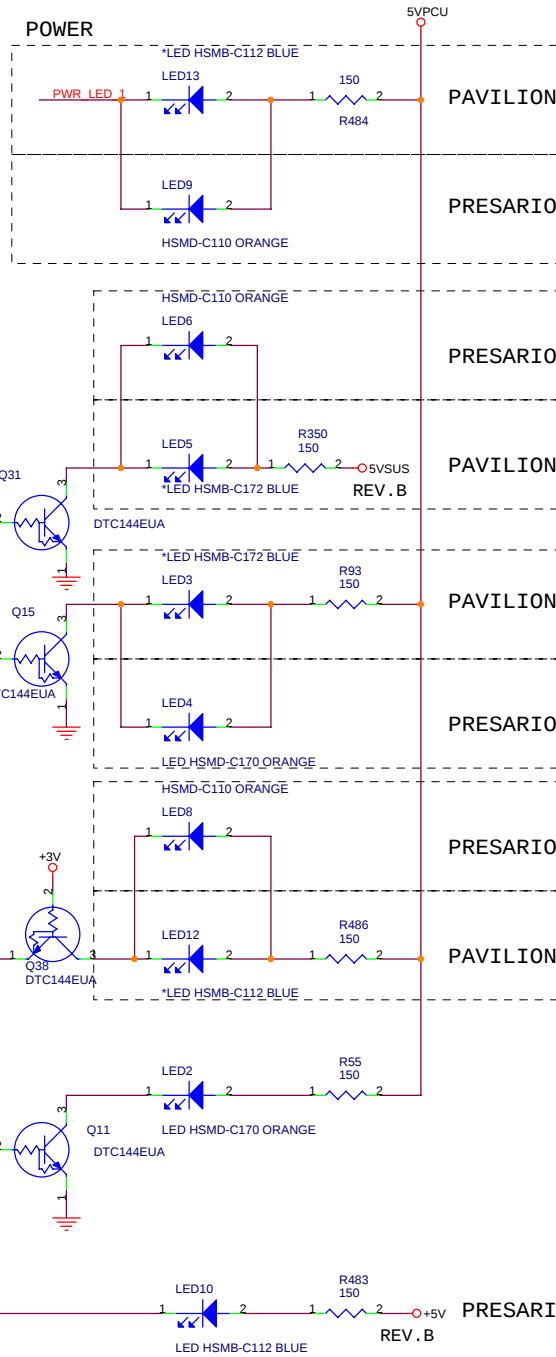
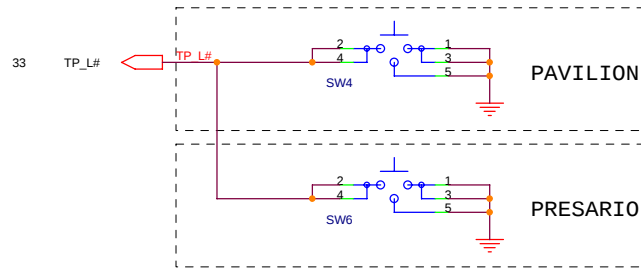
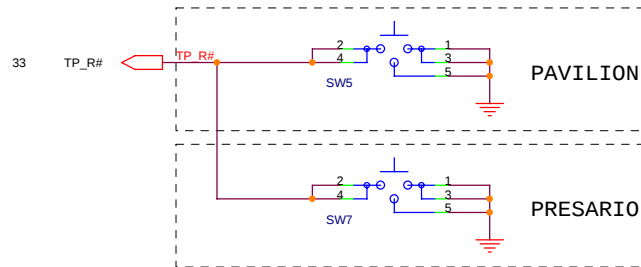
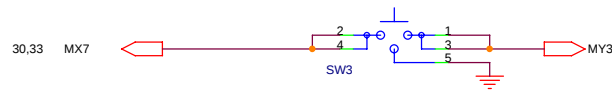
REV:B MODIFY FOR USE
NEW MODEM MODULE



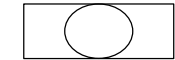




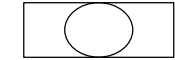
Touchpad control



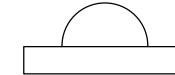
LED HSMD-C170 ORANGE



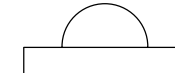
LED HSMB-C172 BLUE



LED HSMD-C110 ORANGE

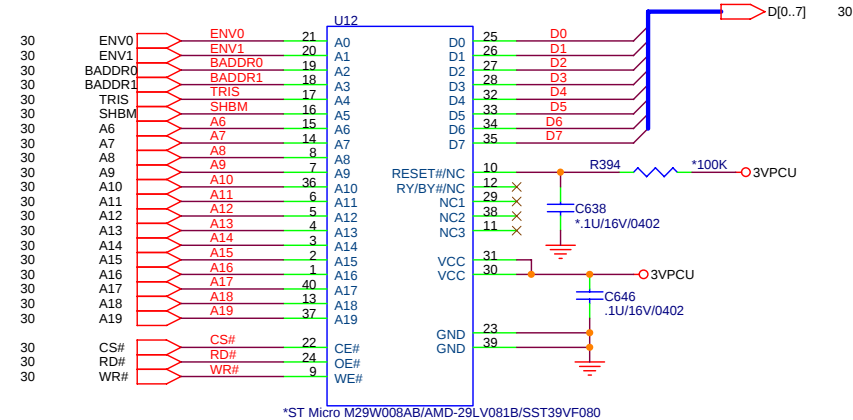


LED HSMD-C112 BLUE



REV.B: LED7 AND LED8 SWAP

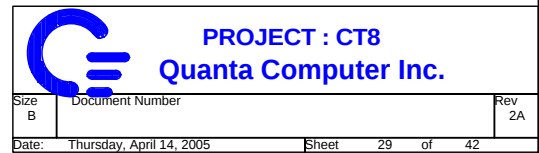
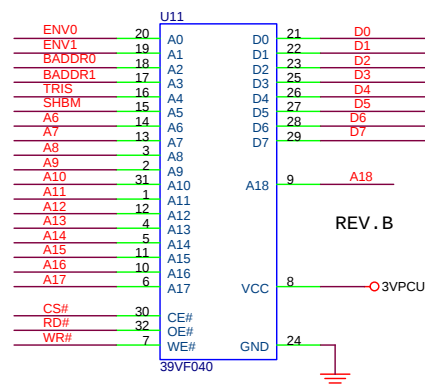
8Mbit (1M Byte), TSSOP40



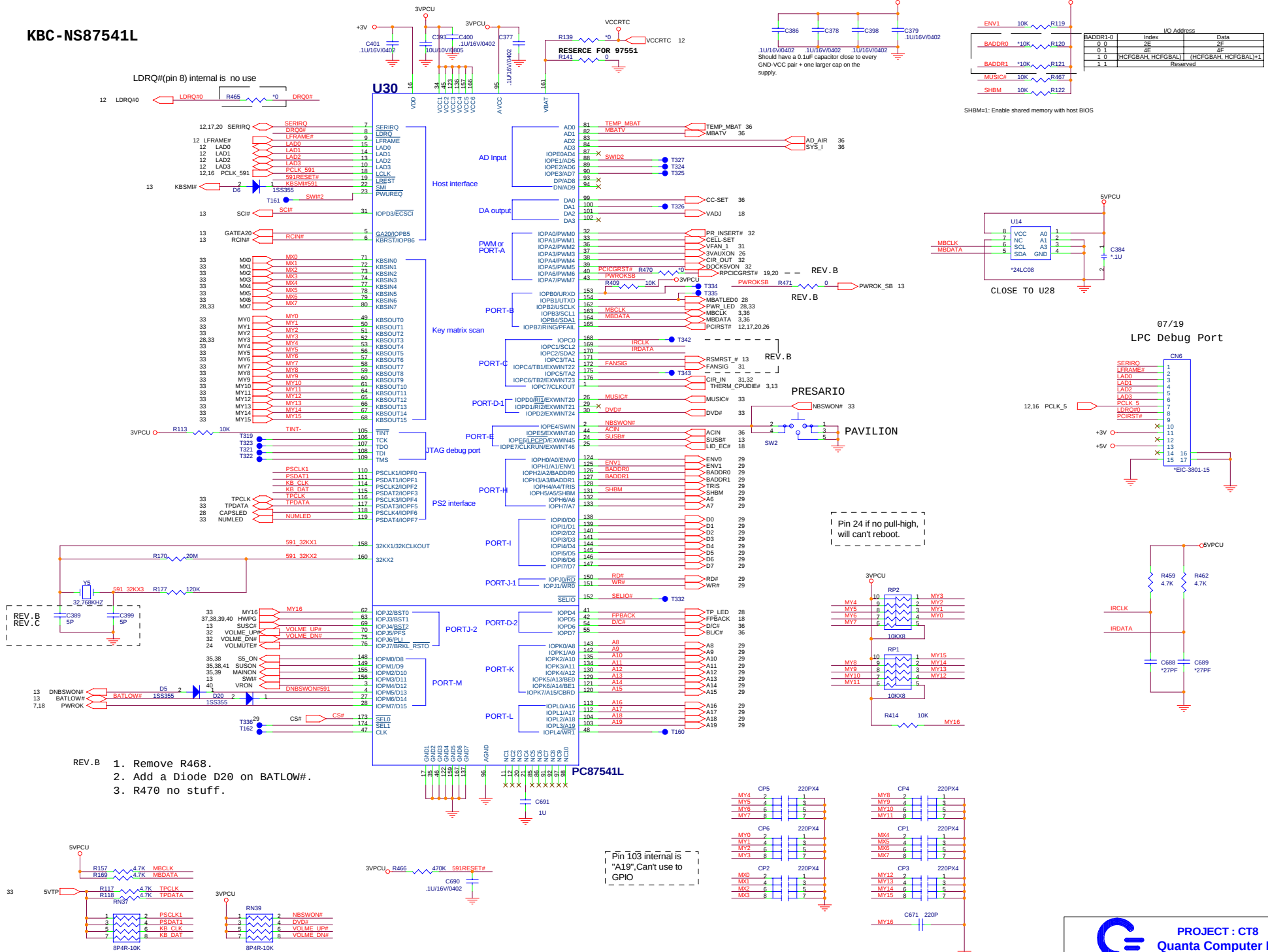
AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

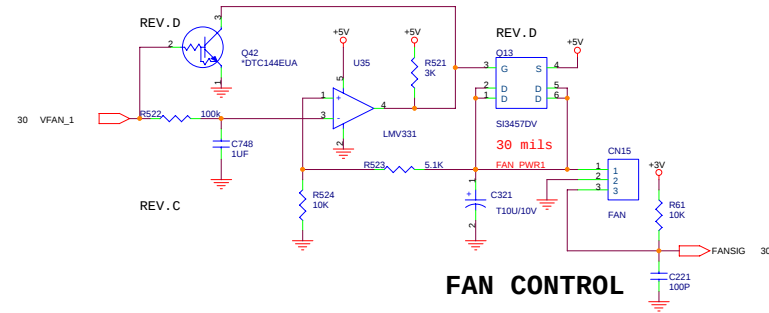
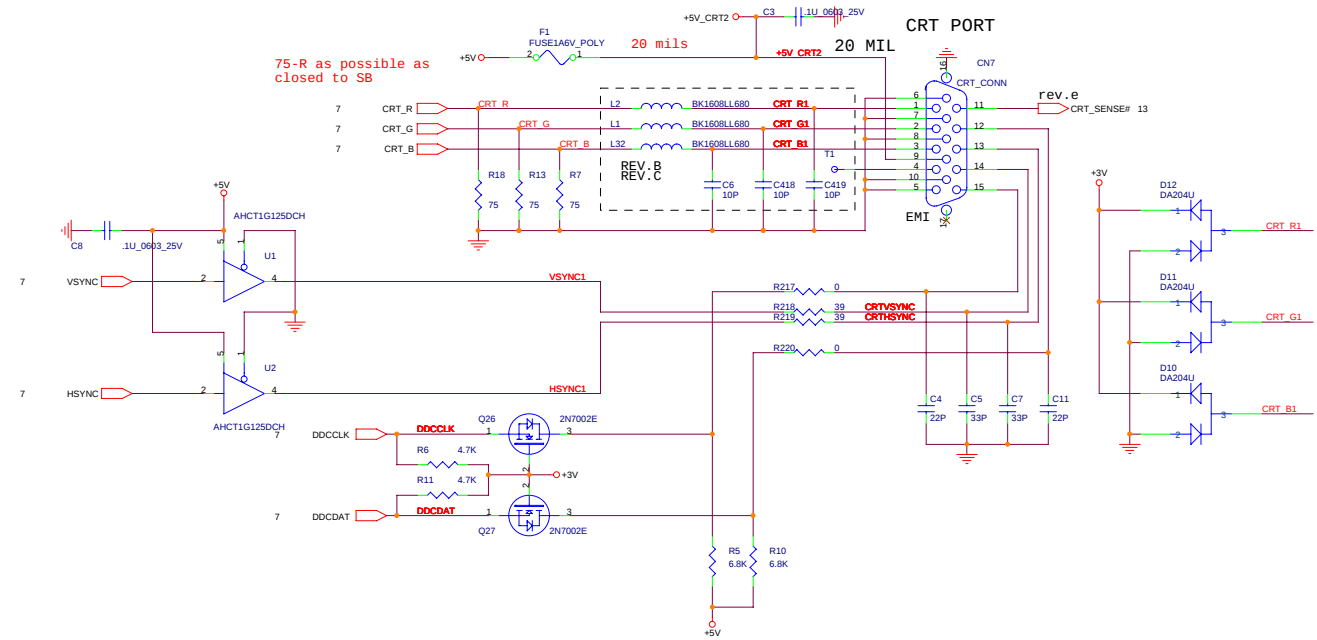
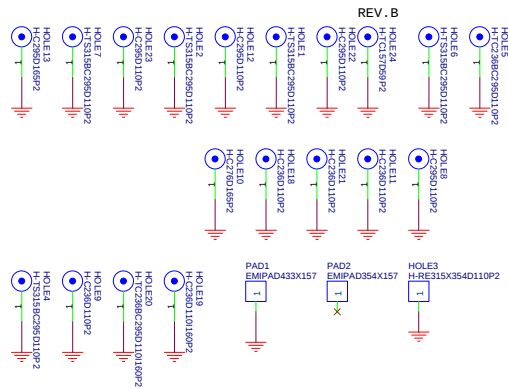
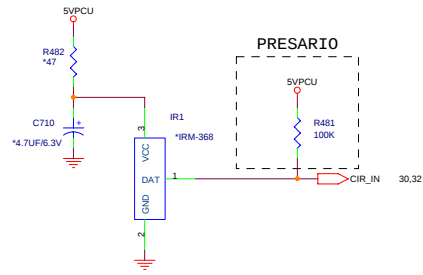
1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326 UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALV directly.
2.SiO has internal 20 mS delay of VCC1_PWROK

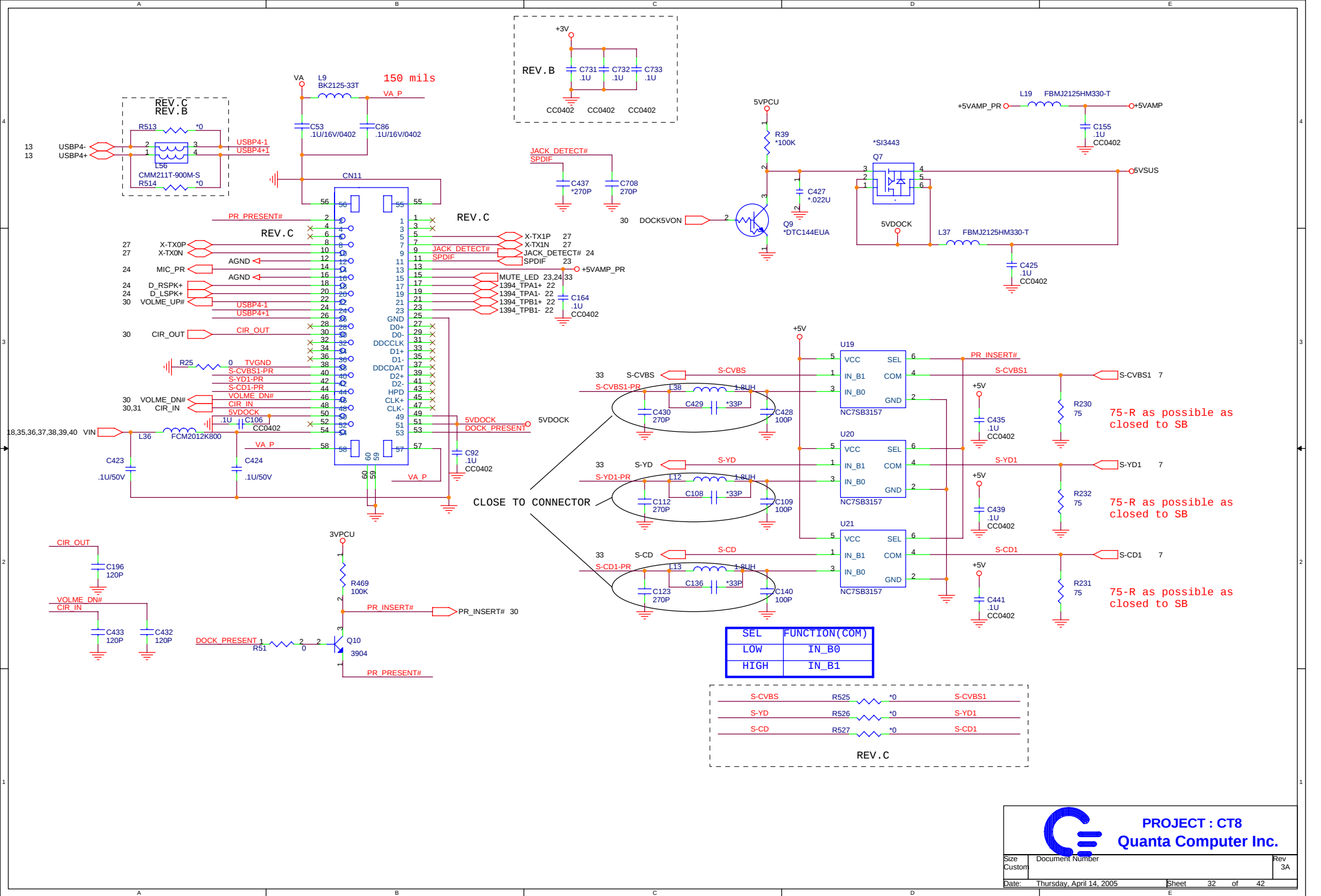
4Mbit (512k Byte), TSSOP32



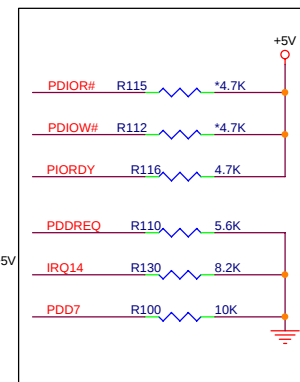
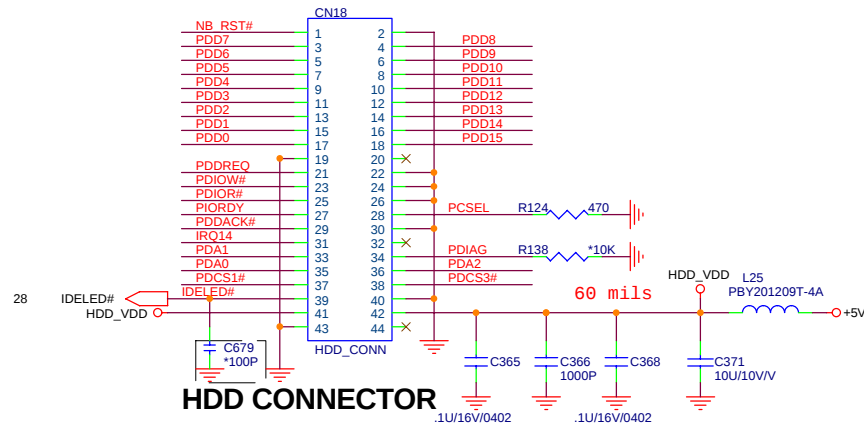
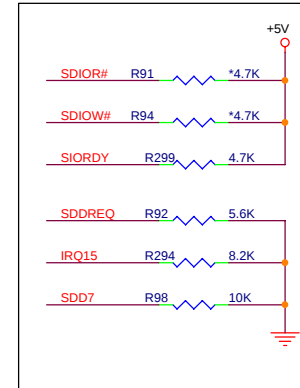
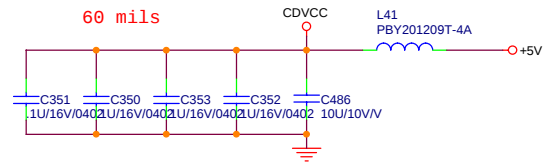
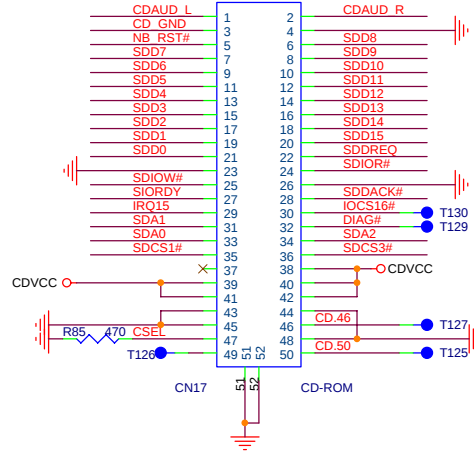
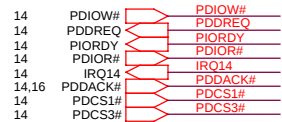
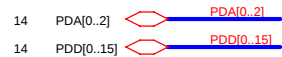
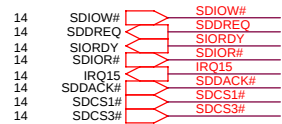
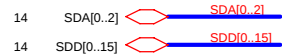
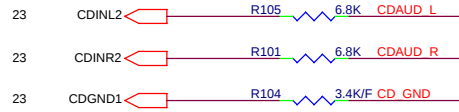
KBC-NS87541L



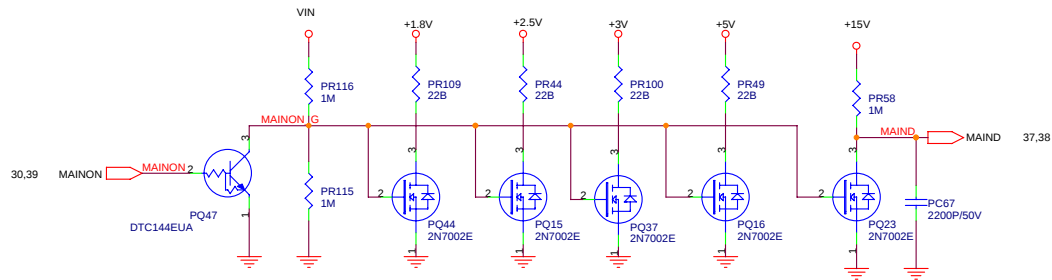




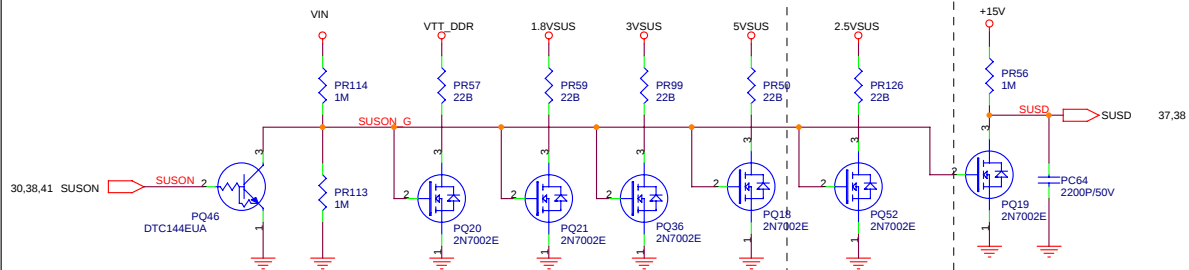
CD-ROM



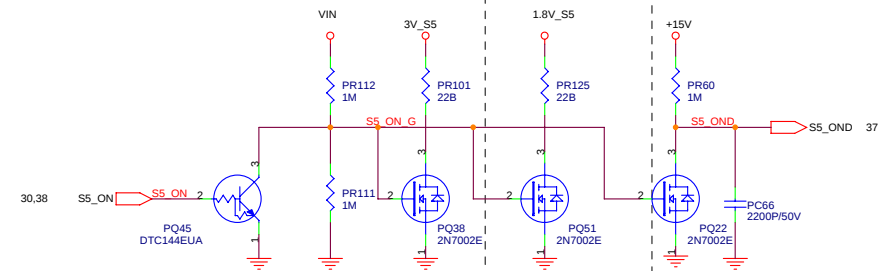
PROJECT : CT8
Quanta Computer Inc.



REV . B



REV . B

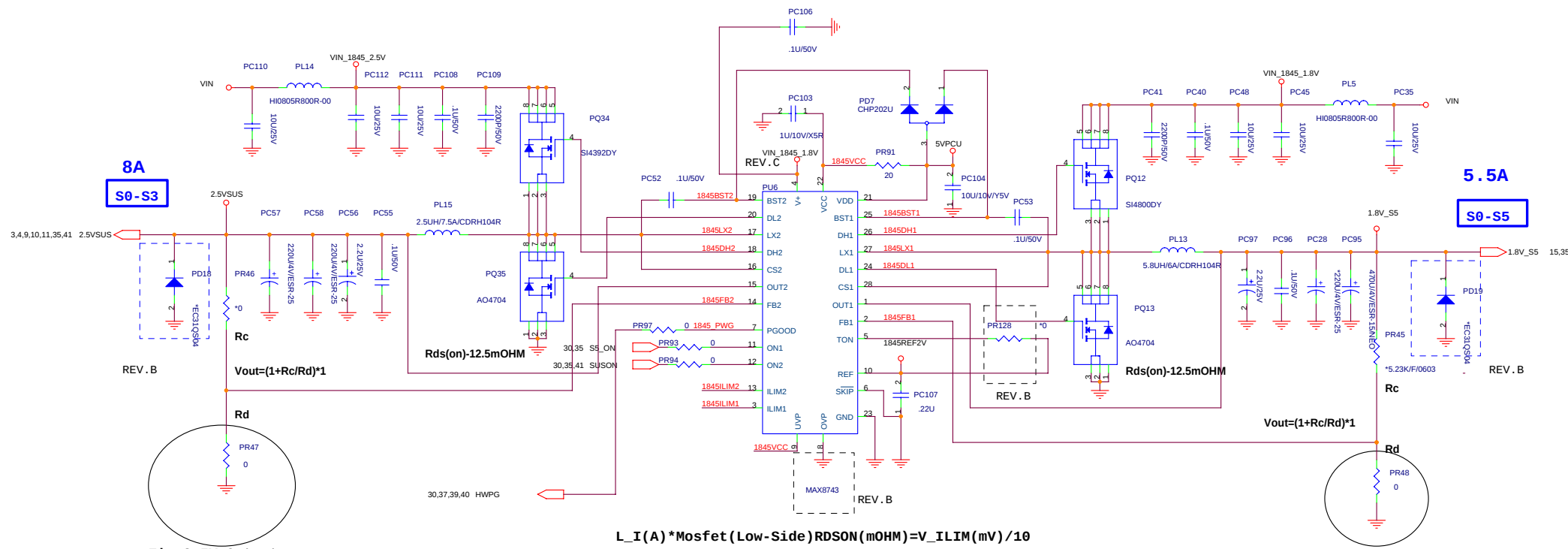


PROJECT : CT8
Quanta Computer Inc.

ADAPTER 18.5V 65W 3.51A



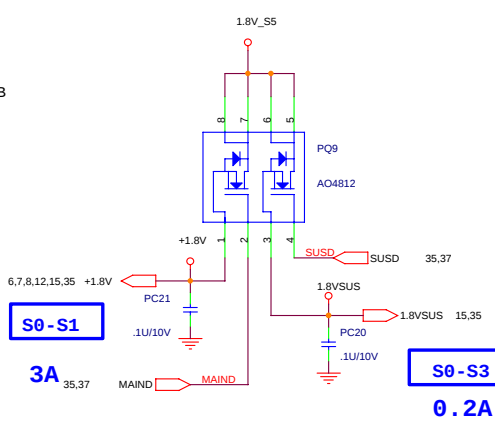
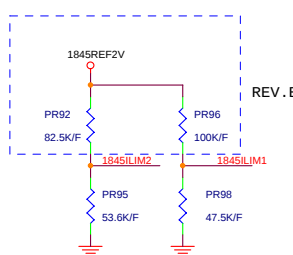
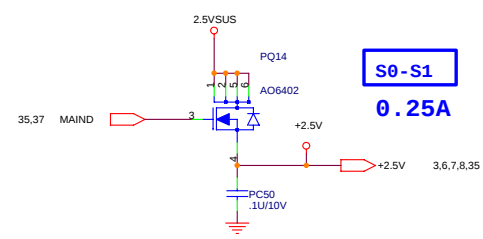
Size Custom	Document Number MAX1772/CHARGING	Rev 3A
Date:	Thursday, April 14, 2005	Sheet 36 of 42

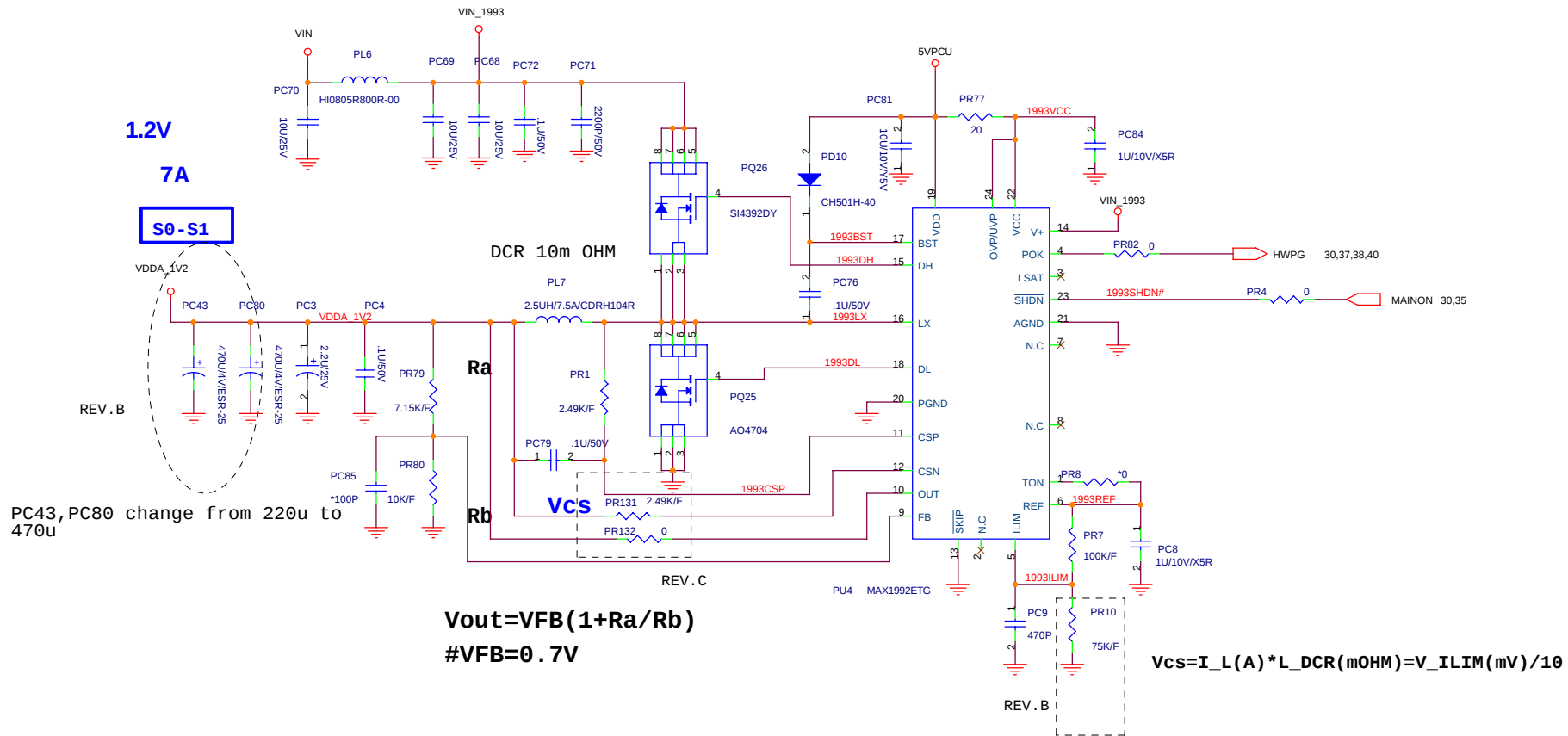


Fix 2.5V Output

Fix 1.8V Output

$$L_I(A) * \text{Mosfet (Low-Side) RDS(on)(mOHM)} = V_{ILIM}(mV) / 10$$





MODEL		REV	CHANGE LIST		Model1		CT8 Mother Board	
					Page	FROM	TO	
CT8 M/B		1A	First Release		1	1A		
					2	3A		
					3	3A	3B	
					4	2A		
		2A	PAGE 2 : 1. C330, C479 CHANGE VALUE FROM 33p to 27p for meet 35ppm. 2. DEL R84 0ohm (don't need reserve) 3. Add CN11 HOT CONNECTOR for AND requirement. 4. Add C721 100p, C722 4.7U, C723 3300p, C724 0.22u for high frequency decoupling. 5. Remove R386 Q33, connect U18 pin 6 to TEMP_ALARM# (no need level shift). 6. Change C336 Q33, connect U18 pin 16 to 100u and remove C384, that ensures VDD to VDDA power down sequence is met. 7. Add C154,C283,C284,C285 4.7u, C9,C277 100u change to 220u for VDDA 1V2 power noise. 8. C148, C163 VALUE CHANGE FROM 330u to 220u for Mechanic interference. 9. C166 VALUE CHANGE FROM 10K to 0.8.5K for ATI requirement. 10. R16 VALUE CHANGE FROM 10K to 0.8.5K for ATI requirement. 11. Add C711-C720, C745-C747 0.1u FOR EMI 12. C191 CHANGE R17 VALUE TO 2.7K PULL +1.8V for side-port memory is not used. 13. DEL C191 CIRCUIT because no need reserve is ATI requirement. 14. Add C740, C741 FOR EMI 15. CHANGE NET NAME FROM PWROK NB TO PWROK for meet ATI power OK sequence. 16. Add L55 for VDDA 1V2 frequency decoupling. 17. L15 L55 IT201209G121 CHANGE TO FBM12125HM330-T. 18. C280 VALUE CHANGE FROM 330u to 220u for Mechanic interference. 19. DEL R129, C391, C382, U9, D3, because no need reserve is ATI requirement. 20. Remove RTC charge circuit Q16, R133, R137, R140. because RTC battery is not support charge function. 21. C387, C388 CHANGE VALUE FROM 12p to 18p for meet 10ppm SPEC. 22. ADD RN40, RN41, R520 for PCI command signal pull high. 23. CHANGE R99 for blue tooth on/off and R318 for wire less on/off function. 24. DEL R401, C668, R400 for ATI power OK sequence. 25. DEL R161 0ohm for BITCLK 26. Add R503, R504 FOR E77 AND D/F 27. CHANGE R147 PULL HIGH FROM 3V_S5 TO +3V for leakage current. and R446 contact to BITCLK because change net name. 28. 1. Del C642 for meet IXP power on sequence. 29. 1. Del R444 10K, Add R445 10K for ATI USB clock from outside. 30. 1. DEL R175, Q19 and CN22 PIN34 CONNECT TO PCI_PME#. because no need LANVCC to control PME signal. 31. 2. Del R196, C402, no need reserve. 32. CHANGE R213 SIGNAL to PWROK and DEL Q21, Q22, Q24, R210for ATI LCD back light bug. 33. Reserve R215 1K PULL DOWN 34. Add R508, R509, C19 for ATI LCD back light bug. 35. 1. DEL PC11518 CIRCUIT AND PARTS 36. Add C743 for tune clock waveform. 37. R402 still for PCI reset timing 38. Remove R392, Q36 and U26 pin 13 connect to PCI_PME# for PME timing. 39. Add R515, C742 circuit on CLK48M for tune clock waveform. 40. Change R401 to 4.7K for limit current. 41. Change L48 to 0 ohm for EMI 42. Add R494 22ohm AND Q39 2N7002E for VCC_XD discharge. 43. 2. CHANGE R487, R488, R490, R491, R492, R493, R495, R496, R497, R498, R499 VALUR FROM 0 TO 22 for signal waveform.. 44. 3. Add R516, R517, R518 for TI requirement. 45. Remove R397, D16, R489. 46. Add a Quick Switch U34 to isolate clock. 47. Change R501 to 0 ohm. 48. CNS pin 39, 43 connect to the same net. 49. C725-C728 0.1u for power noise. PAGE11 : 1. C280 VALUE CHANGE FROM 330u to 220u for Mechanic interference. PAGE12 : 2. Remove RTC charge circuit Q16, R133, R137, R140. because RTC battery is not support charge function. PAGE13 : 3. C387, C388 CHANGE VALUE FROM 12p to 18p for meet 10ppm SPEC. 4. ADD RN40, RN41, R520 for PCI command signal pull high. 5. CHANGE R99 for blue tooth on/off and R318 for wire less on/off function. 6. DEL R401, C668, R400 for ATI power OK sequence. 7. DEL R161 0ohm for BITCLK 8. Add R503, R504 FOR E77 AND D/F 9. CHANGE R147 PULL HIGH FROM 3V_S5 TO +3V for leakage current. and R446 contact to BITCLK because change net name. PAGE15 : 1. Del C642 for meet IXP power on sequence. PAGE16 : 1. Del R444 10K, Add R445 10K for ATI USB clock from outside. PAGE17 : 1. DEL R175, Q19 and CN22 PIN34 CONNECT TO PCI_PME#. because no need LANVCC to control PME signal. PAGE18 : 2. Del R196, C402, no need reserve. 3. CHANGE R213 SIGNAL to PWROK and DEL Q21, Q22, Q24, R210for ATI LCD back light bug. PAGE19 : 1. Reserve R215 1K PULL DOWN 2. Add R508, R509, C19 for ATI LCD back light bug. PAGE20 : 1. DEL PC11518 CIRCUIT AND PARTS 2. Add C743 for tune clock waveform. 3. R402 still for PCI reset timing 4. Remove R392, Q36 and U26 pin 13 connect to PCI_PME# for PME timing. 5. Add R515, C742 circuit on CLK48M for tune clock waveform. 6. Change R401 to 4.7K for limit current. 7. Change L48 to 0 ohm for EMI 8. Add R494 22ohm AND Q39 2N7002E for VCC_XD discharge. PAGE21 : 2. CHANGE R487, R488, R490, R491, R492, R493, R495, R496, R497, R498, R499 VALUR FROM 0 TO 22 for signal waveform.. 3. Add R516, R517, R518 for TI requirement. 4. Remove R397, D16, R489. 5. Add a Quick Switch U34 to isolate clock. 6. Change R501 to 0 ohm. 7. CNS pin 39, 43 connect to the same net. 8. C725-C728 0.1u for power noise.		PAGE22 : 1. C484 VALUE CHANGE FROM 100U to 150U for USB power meet SPEC. 2. ADD R509, R510, R511, R512 FOR EMI PAGE23 : 1. MC13, MC18 CHANGE VALUE FROM 33p to 22p for tune clock range. 2. CHANGE MR24, MR27 FROM 1K to 0ohm for Conexant requirement. 3. ADD SPDIF 4. Del MR26 for meet PC99 SPEC. 5. Del C518 for tune BITCLK waveform.. PAGE26 : 1. ADD R502 15K pull low for tune ISOLATES voltage. 2. R341 change 4.7K to 5.6K for REALTEK recommend. 3. Add C729 10u and C650 change value from 10u to 22u for REALTEK recommend. 4. Change C388 from 2200p to 3300p for tune 3VPCU drop level. 5. Add C736, C737, C738, C739 for EMI 6. DEL R134 no need reserve. ADD Q40 for leakage current. PAGE27 : 1. ADD C734, C735 1000p FOR EMI. 2. DEL R246, R249 for 1G LAN. PAGE28 : 1. R483 change signal from 5VPCU to +5V and R350 pull 5VSUS for leakage current. PAGE29 : 1. U11 change package to TSSOP32 for Mechanic interference. PAGE30 : 1. C389 8p, C399 5.6p change value to 15p for clock tolerance. 2. Del signal_BT OFF# RF_OFF# for HP implement guide. 3. Add R471 and DEL R468, R470 for ATI power OK sequence. 4. Add D20 for EC leakage current. PAGE31 : 1. ADD R512, R514 2, C731, C732, C733 FOR EMI. 2. CHANGE L1, L2, L32 to BK1608L1121 C6, C418, C419 to 10P for CRT timing. PAGE32 : 1. ADD R513, R514 2, C731, C732, C733 FOR EMI. PAGE33 : 1. DEL CN29, C681, C677, C6679 because no need AV function. PAGE35 : 1. ADD PR126, PR125, P051, P052 for 2.5VSUS and 1.8V S5 discharge circuit PAGE36 : 1. CHANGE P024 FROM SI4425 TO A04407, CHANGE PQ33 FROM A04411 TO A04407, CHANGE PR36 FROM 130K TO 121K, PQ11 CHANGE TO 2N7002K, PD6 CHANGE TO CH501H-40. and add PQ53, PD17, PR127, PC144 for prevent AC discharge MOSFET damage when adapter over watt. PAGE37 : 1. CHANGE P041 FROM A04704 TO A04702, CHANGE PR102 FROM 47.5K TO 80.6K, CHANGE PQ43 FROM SI4834 TO A04914 for Modify 5VPCU OCP point. PAGE38 : 1. Change PWM IC from MAX1845 to MAX8743 to avoid negative voltage.Modify 2.5VSUS, 1.8V_S5 OCP point. 2. ADD PR128 NO STUFF for adjust work frequency. PAGE39 : 1. CHANGE PR18 FROM 60.4K TO 75K for change VCCA_1V2 OCP point. PAGE40 : 1. ADD PR124 15K, DEL PR70, PC2 for VR_ON signal add pull down resistor. PAGE41 : 2. Change PR64 from 37.4k to 49.9k for update over current from 32A to 39A. 3. Add R505, R506 and Change VSENSE from VIT_DDR to CPU_VIT_SENSE 4. Change PR52 to 33K, PR51 to 100K for timing. 5. PC61,PC62 no stuff.	5	3A	
					6	1A		
					7	3A	3B	
					8	2A		
					9	1A		
					10	1A		
					11	2A		
					12	3A	3B	
					13	3A		
					14	1A		
					15	2A		
					16	2A		
					17	3A		
					18	3A	3B	
					19	2A	3B	
					20	3A		
					21	3A		
					22	3A		
					23	2A	3B	
					24	3A	3B	
					25	1A		
					26	3A	3B	
					27	3A		
					28	2A		
					29	2A		
					30	3A		
					31	3A	3B	
					32	3A		
					33	2A		
					34	1A		
					35	2A		
					36	3A	3B	
					37	3A		
38	3A							
39	3A							
40	3A	3B						
41	2A							
		3A	PAGE 2 : 1. Add CAP C749, C750 0.1u for EMI. PAGE 3 : 1. Modify C311 component. PAGE 5 : 1. Change R16 to 8.25k/F and R12 to 82.5 ohm for A-link drive. PAGE 7 : 1. Del C740 for VGA Clock waveform 2. L17 change from bead to 150ohm for ATI VCO issue(PA_RS480L1). PAGE12 : 1. Add D3 for meet SVTP SPEC 2. Change C674, C675, C676, C683 value from 15p to 33p for EMI 3. C358, C359, C360, C361 change value from 0.1u to 0.01u for ATI PA_IXP400AC11. PAGE13 : 1. R503 change pull up source from 3VPCU to +3V for real power plane. PAGE17 : 1. CN22 pin15 pull down for customer request. PAGE18 : 1. Change C730 from 3300p to 0.1u for power drop. PAGE20 : 1. Add R529, R530 2.7K pull down for option FF and DF. 2. Reserve C754, C755 for EMI. 3. Change C742 to 22p for waveform quality. PAGE21 : 1. Add C758-C761 0.1u for bypass noise. 2. Change R501 from 3.3K to 0 for signal level. 3. Add R506, R531, use for signal driving. 4. Change R518, R519 to 2.2K for signal level. PAGE22 : 1. change CN19, CN23, CN16 footprint for new part. PAGE24 : 1. reserve C751, C752, C753, C756, C757 0.1u for EMI.		PAGE26 : 1. Del 1G signal. 2. Change C385 from 3300p to 0.1u for power drop. PAGE27 : 1. Del 1G circuit, because no support 1G function. PAGE30 : 1. C89, C390 change value from 15p to 5p for frequency tolerance. PAGE31 : 1. Modify FAN circuit for diminish electronic magnetic noise. 2. Change L1, L2, L32 to BK1608L1680 for CRT waveform can meet SPEC. PAGE32 : 1. Del 1G signal 2. Change R525, R526, R527 0ohm for option FF or DF TV. 3. Add common choke for USB. PAGE36 : 1. Change PC47 to 0.47U,PC37 to 0.047U for reduce Adapter in inrush current. 2. Del P049 for fix 3 CELL battery and cost down. 3. Change P053 for 2N7002K for ESD protect. 4. Add PR130,P054 for delay AD_AIR signal to EC After 3VPCU ready. PAGE37 : 1. Change PR53 to 150K for Meet MAX1999 SHDN signal input trip Max level. 2. Del PC122 for meddle mechanic. PAGE38 : 1. Modify VIN_1845 1.8V signal, because that is single net. PAGE39 : 1. Add PR132 0 ohm,PR131 2.49K/F for reserve debug. PAGE40 : 1. Change PR64 to 60.4K Modify CPU over current protect point. 2. Change PR71 to 80.6K for Modify CPU power slew rate	9	1A	
					10	1A		
					11	2A		
					12	3A	3B	
		3B	PAGE 3 : 1. Add C762-C767 0.1u for ESD. PAGE 7 : 1. Change C740 value from 1000p to 330p for ESD. PAGE13 : 1. Modify BT_OFF# from GPIO1 to GPM3 for keep status in S3. 2. Add R531, R534 10K pull low for M/B ID. PAGE18 : 1. Change R216 power source from +3V to 5VPCU and change C730 value to .47u for glitch. PAGE19 : 1. Change R342 value from 330hm to 150hm for meet PCMCIA SPEC timing. PAGE21 : 1. Add C21, C355 and change R309 value from 2.2K to 1K for eliminate GPRS card noise. PAGE24 : 1. Del R311 for GPRS noise. PAGE26 : 1. Add Q41 DTC144EU for GPRS noise. PAGE27 : 1. Change R156 power source from 3VPCU to 5V_AL and change C385 value from .1u to .47u for power glitch. PAGE31 : 1. Add Q43 (no stuff) DTC144EU and Q13 SI3457 for FAN driver. PAGE33 : 1. Add R133 (No stuff) for power saving. PAGE40 : 2. Del PC7, PR9, PC83 for ESD.					



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SHEET 1 OF 1