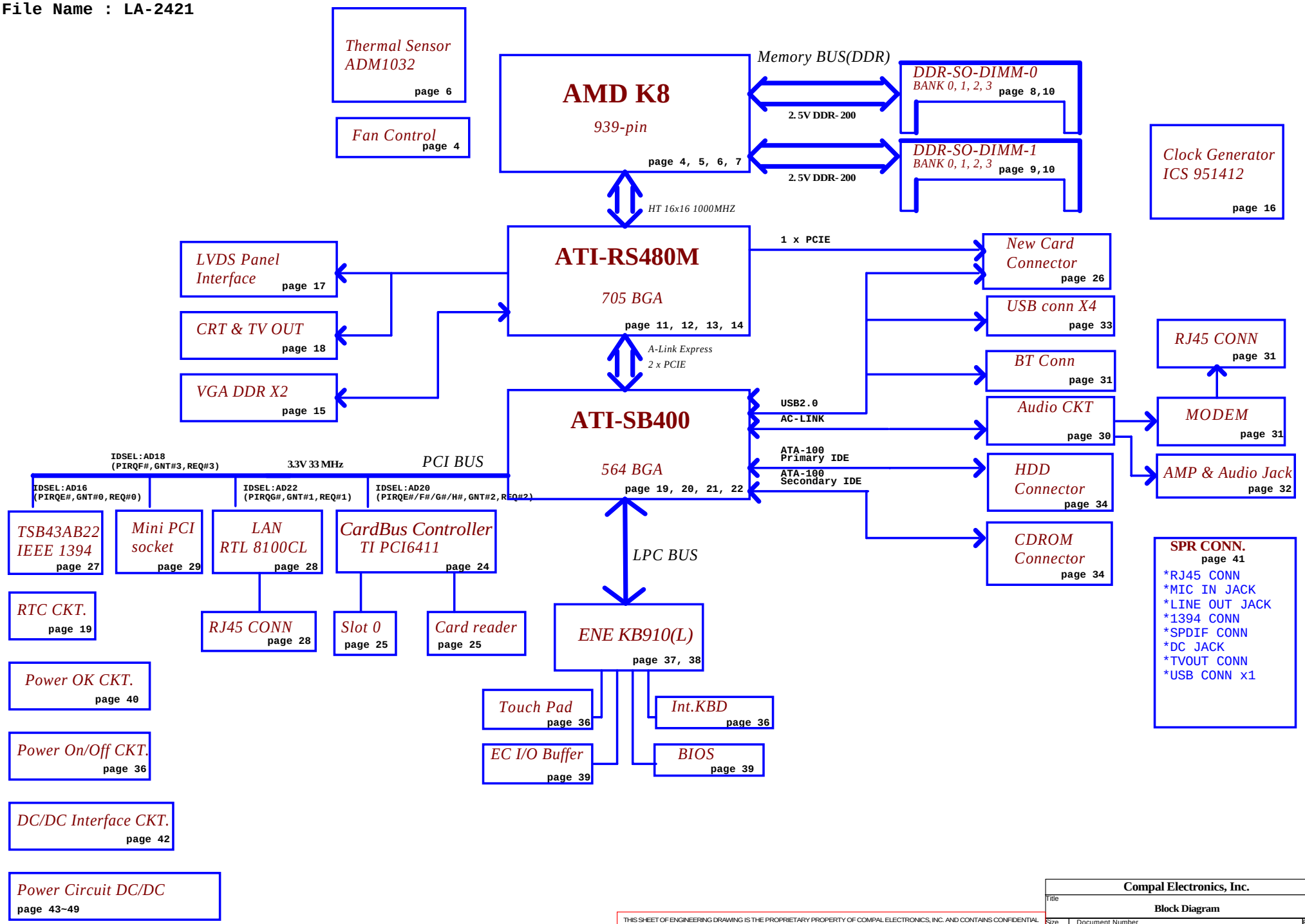
Compal confidential

Schematics Document

AMD K8 with
ATI RS480M+ATI SB400

2005-01-04
REV:0.6

Compal Electronics, Inc.		
Title: Cover Sheet		
Size	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 1 of 56	



Compal Electronics, Inc.		
Title: Block Diagram		
Size	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 2 of 56	

Voltage Rails

power plane / State	+12VALW +5VALW +3VALW +1.8VALW	+5V +2.5V +1.25V	+5VS +3VS +2.5VS +1.8VS +1.5VS +2.5VDDA +CPU_CORE +1.2V_HT
S0	O	O	O
S1	O	O	O
S3	O	O	X
S5 S4/AC	O	X	X
S5 S4/AC don't exist	X	X	X

O MEANS ON
X MEANS OFF

PCI Devices

INTERNAL DEVICE	IDSEL #	REQ/GNT #	PIRQ
SMBUS			
IDE			A
LPC I/F			
PCI to PCI			
AC97 AUDIO			B
AC97 MODEM			B
OHCI#1 USB			D
OHCI#1 USB			D
EHCI USB			D
SATA#1			A
SATA#2			A

EXTERNAL			
1394	AD16	0	E
Wireless LAN	AD18	3	F
LAN	AD22	1	G
CARD BUS	AD20	2	E,F,G,H
Mini-PCI (no use)	AD19	4	F

ZZZ

LA-2421 REV 0

<11> H_CADIP[0..15] → H_CADIP[0..15]

<11> H_CADIN[0..15] → H_CADIN[0..15]

H_CADOP[0..15] → H_CADOP[0..15] <11>

H_CADON[0..15] → H_CADON[0..15] <11>

+1.2V_HT

0.22U_0603_10V7K C18 100U_6.3V_M

0.22U_0603_10V7K C9

0.22U_0603_10V7K C10

0.22U_0603_10V7K C11

0.22U_0603_10V7K C14

250 mil/20 mil

U22A

HT Interface

FOX_PZ39903-314503

VLDT E2, E1, F1, F2

C17 150 mil 4.7U_0805_6.3V6K

VLDT AG4, AG3, AG1, AG2

H_CADIP15 R5 … H_CADIP0 G3, H_CADIN0 G2

L0_CADIN_H15 … L0_CADIN_L0

L0_CADOUT_H15 V4 … L0_CADOUT_L0 AE1

H_CADOP15 … H_CADOP0, H_CADON15 … H_CADON0

<11> H_CLKIP1 L5, H_CLKIN1 M5 → L0_CLKIN_H1, L0_CLKIN_L1

L0_CLKOUT_H1 AB4, L0_CLKOUT_L1 AB3 → H_CLKOP1, H_CLKON1 <11>

<11> H_CLKIP0 L3, H_CLKIN0 L2 → L0_CLKIN_H0, L0_CLKIN_L0

L0_CLKOUT_H0 AB1, L0_CLKOUT_L0 AA1 → H_CLKOP0, H_CLKON0 <11>

<11> H_CTLIP0 R1, H_CTLIN0 T1 → L0_CTLIN_H0, L0_CTLIN_L0

L0_CTLOUT_H0 U2, L0_CTLOUT_L0 U3 → H_CTLOP0, H_CTLON0 <11>

L0_REF1 D1, L0_REF0 C1

+1.2V_HT

R23 44.2_0603_1% LVREF1

C22 1000P_0402_50V7K

LVREF0

R25 44.2_0603_1%

C23 1000P_0402_50V7K

Fan Control Circuit 1

+5VS, +12VS_FAN

R150 0_0805_5%

C251 10U_1206_16V4Z

+12VALW

C614 0.1U_0402_16V4Z

<37,38> EN_FAN1

U37A LM358A_SO8

FAN1_ON

Q14 SI3456DV-T1_TSOP6

FAN1

JP24 ACES_85205-0300

R433 100K_0402_5%

R432 150K_0402_5%

D29 1N4148_SOT23

C68 10U_0805_10V4Z

C61 1000P_0402_50V7K

R1151 0_0603_5%

+3VS

R437 10K_0402_5%

<37,38> FAN_SPEED1

C618 1000P_0402_50V7K

Fan Control Circuit 2

+5VS, +12VS_FAN

R147 FAN2@ 0_0805_5%

C269 FAN2@ 10U_1206_16V4Z

U37B LM358A_SO8

<37,38> EN_FAN2

FAN2_ON

Q16 FAN2@ SI3456DV-T1_TSOP6

FAN2

JP29 ACES_85205-0300

R139 FAN2@ 100K_0402_5%

R137 FAN2@ 150K_0402_5%

D17 FAN2@ 1N4148_SOT23

C241 FAN2@ 1000P_0402_50V7K

C268 FAN2@ 10U_0805_10V4Z

R1152 FAN2@ 0_0603_5%

+3VS

R138 10K_0402_5%

<37,38> FAN_SPEED2

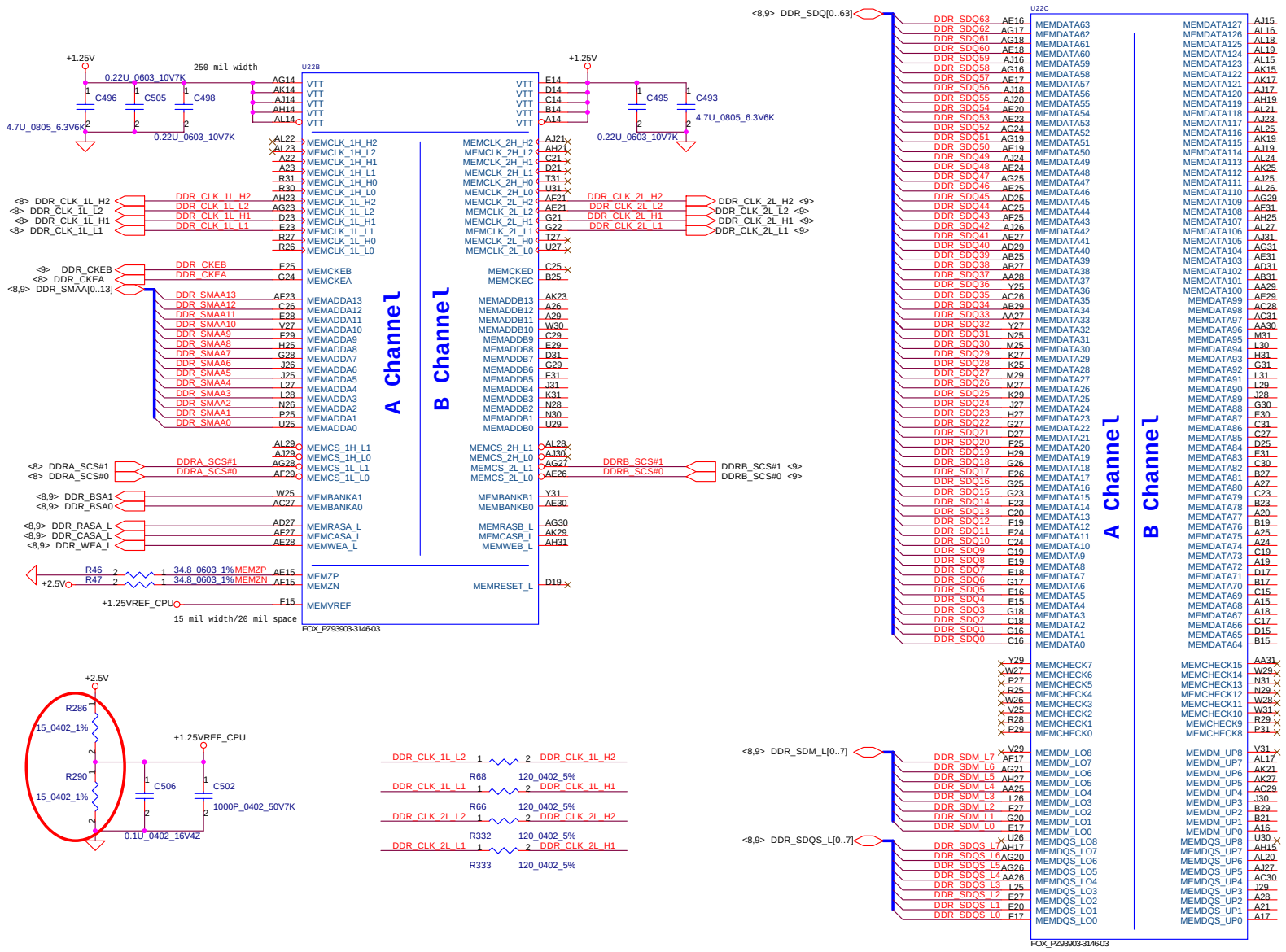
C240 1000P_0402_50V7K FAN2@

Compal Electronics, Inc.

Title: **Claw Harmmer CPU (Host Bus)**

Size: Custom | Document Number: **LA-2421** | Rev: 0.6

Date: Wednesday, January 05, 2005 | Sheet 4 of 56

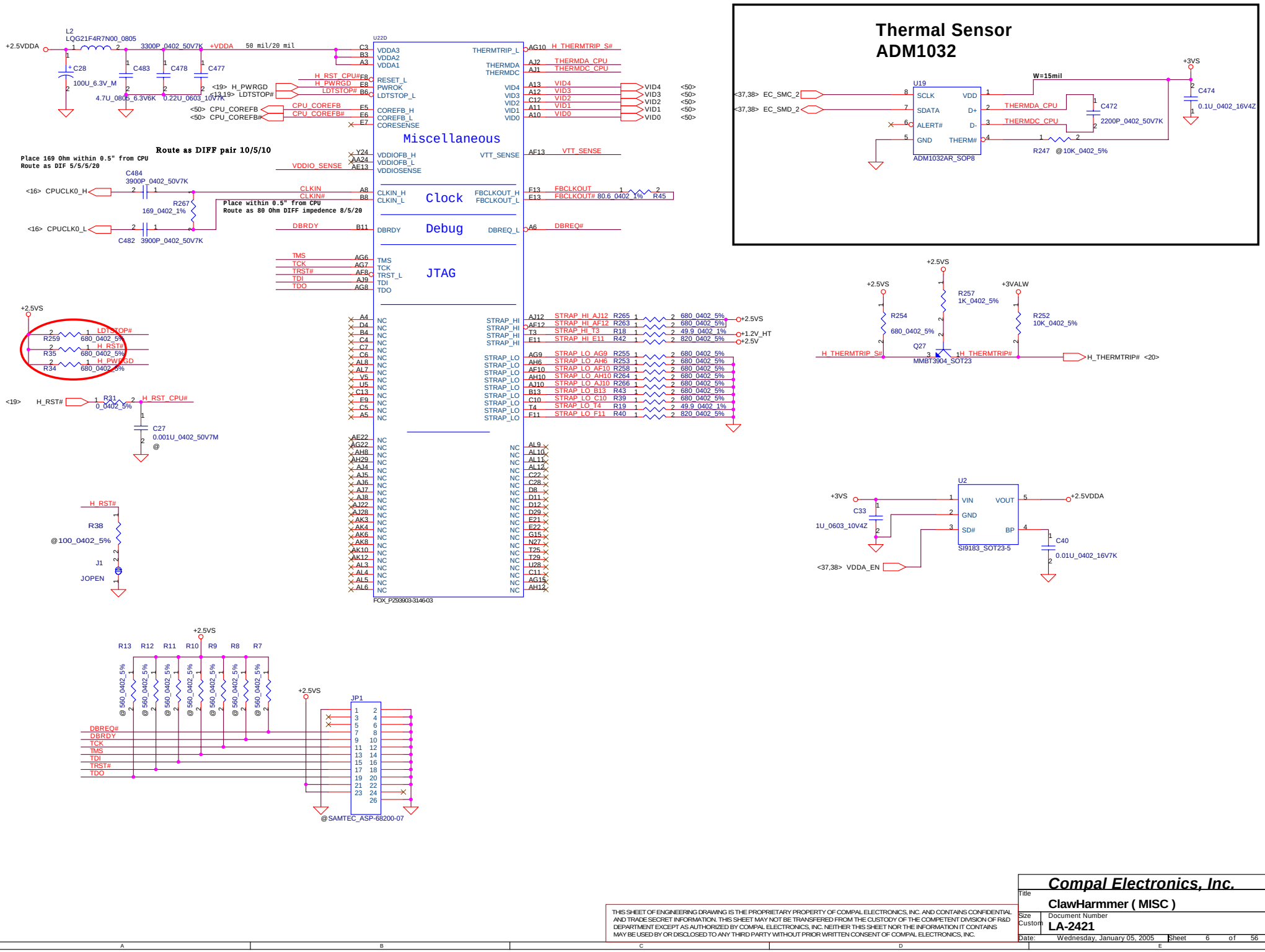


Compal Electronics, Inc.

Title: **Claw Harmmer (MEMORY BUS)**

Size: Custom | Document Number: **LA-2421** | Rev: 0.6

Date: Wednesday, January 05, 2005 | Sheet 5 of 56

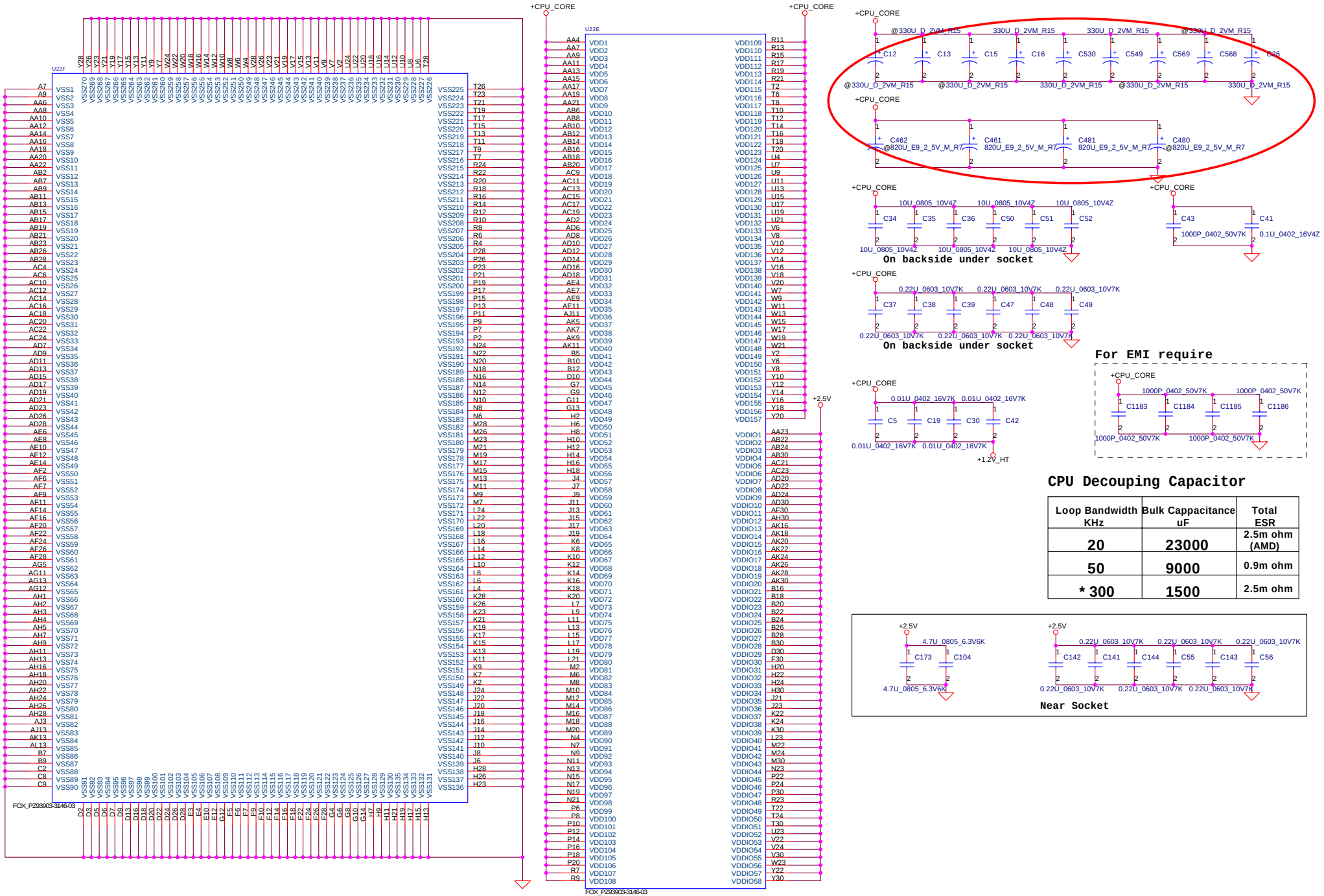


Compal Electronics, Inc.

Title: ClawHammer (MISC)

Size: Custom | Document Number: LA-2421 | Rev: 0.6

Date: Wednesday, January 05, 2005 | Sheet 6 of 56



CPU Decouping Capacitor

Loop Bandwidth KHz	Bulk Cappacitance uF	Total ESR
20	23000	2.5m ohm (AMD)
50	9000	0.9m ohm
* 300	1500	2.5m ohm

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Title: Claw Harmmer (Power & Ground)

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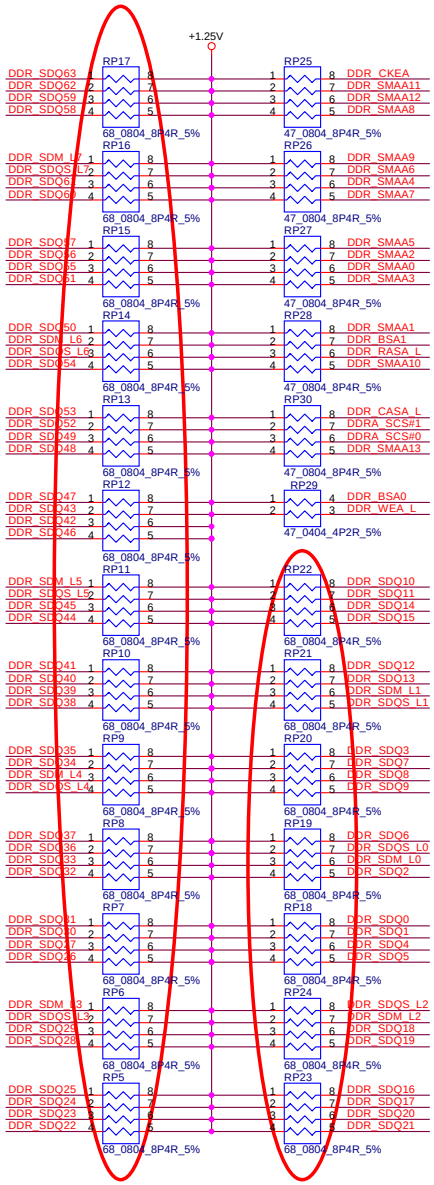
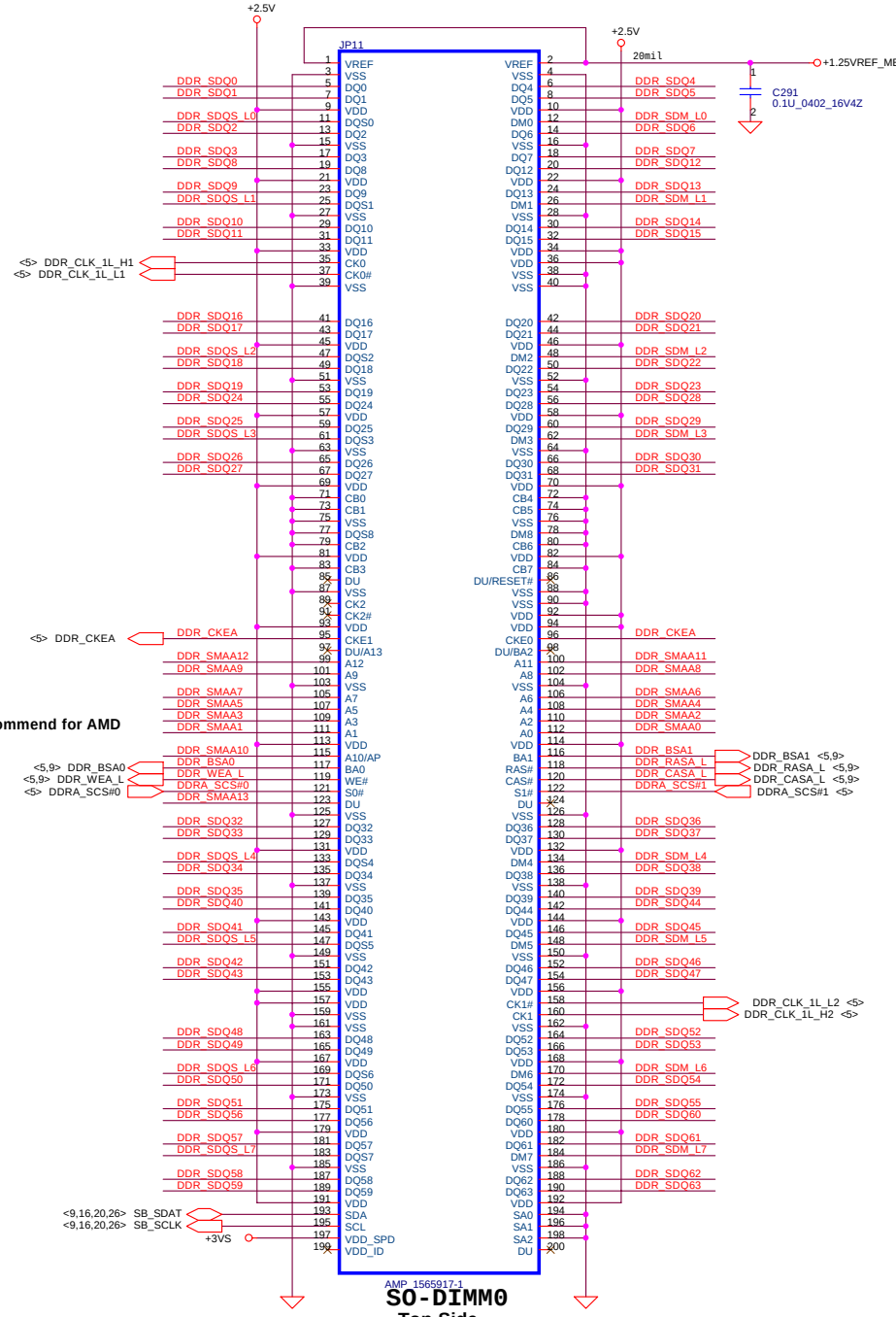
Date: Wednesday, January 05, 2005 | Sheet 7 of 56



Note:
DDR_SMAA13 Recommend for AMD



SO-DIMM0
Top Side

<5,9> DDR_SDQ[0..63] — DDR_SDQ[0..63]
<5,9> DDR_SDQS_L[0..7] — DDR_SDQS_L[0..7]
<5,9> DDR_SDM_L[0..7] — DDR_SDM_L[0..7]
<5,9> DDR_SMAA[0..13] — DDR_SMAA[0..13]

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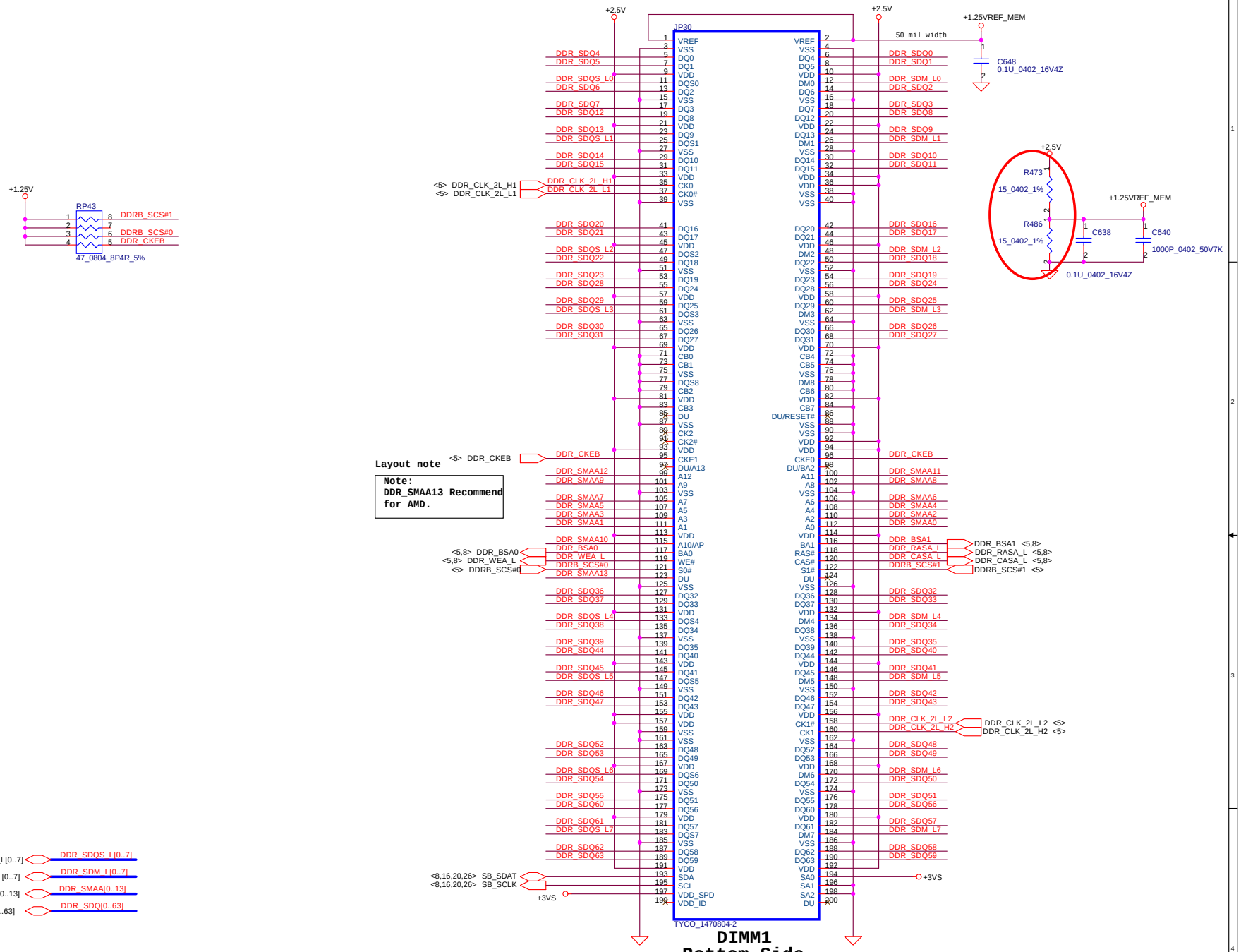
Title: DDR-SODIMM SLOT0		
Size: Custom	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 8 of 56	



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Title: DDR-SODIMM SLOT1

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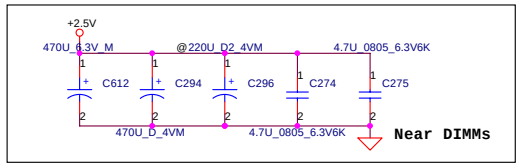
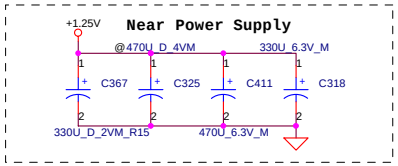
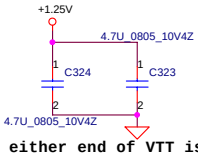
Date: Wednesday, January 05, 2005 | Sheet 9 of 56



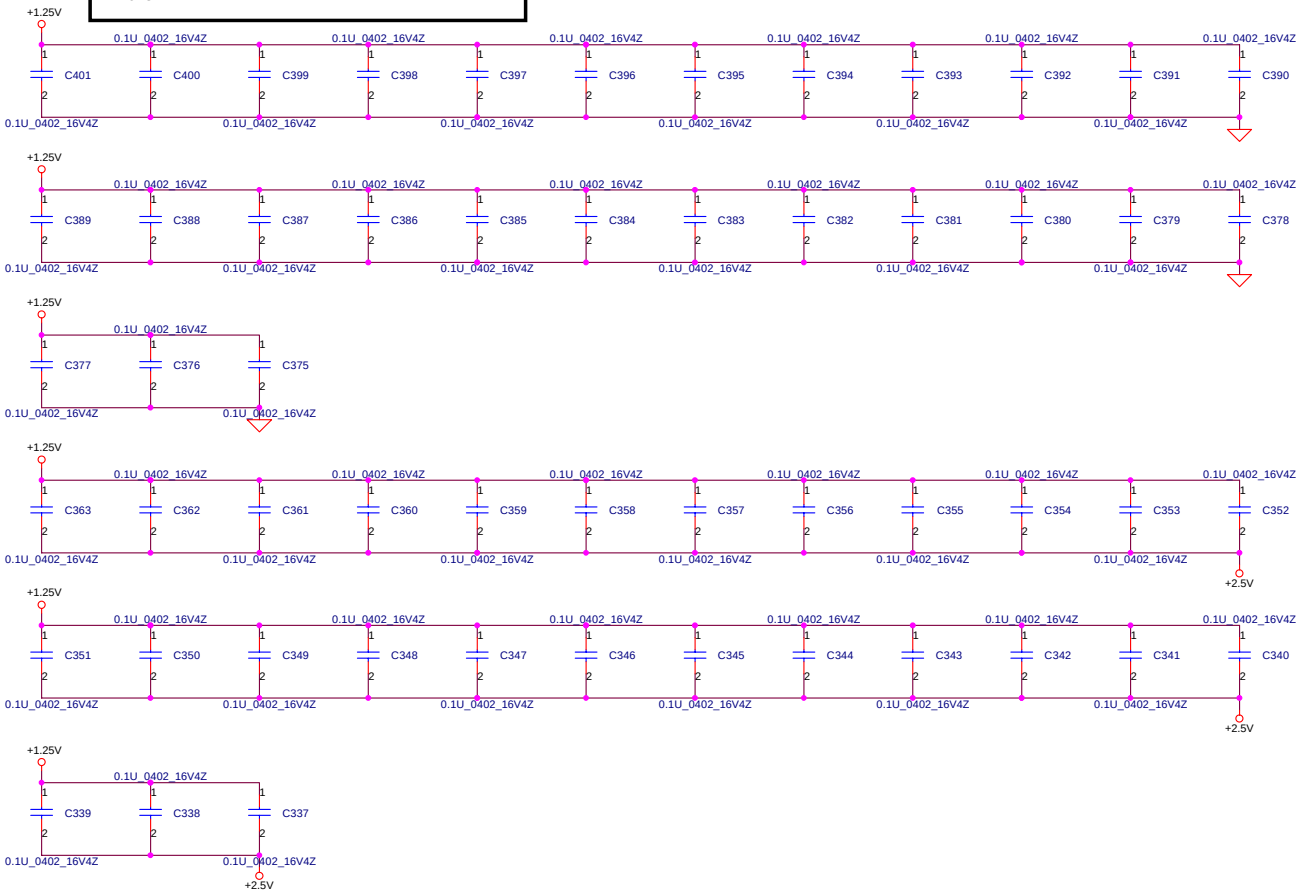




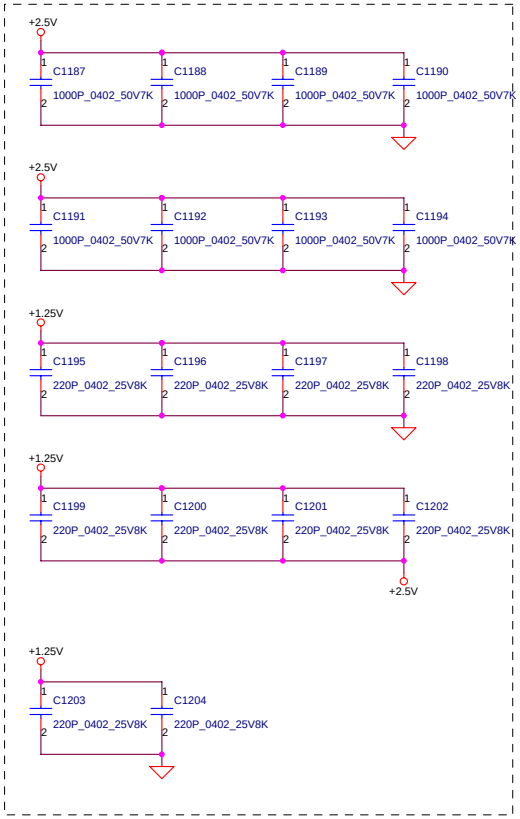
At either end of VTT island (=250 mil)

Layout note :

Place one cap close to every 2 pull up resistors termination to +1.25VS



For EMI require



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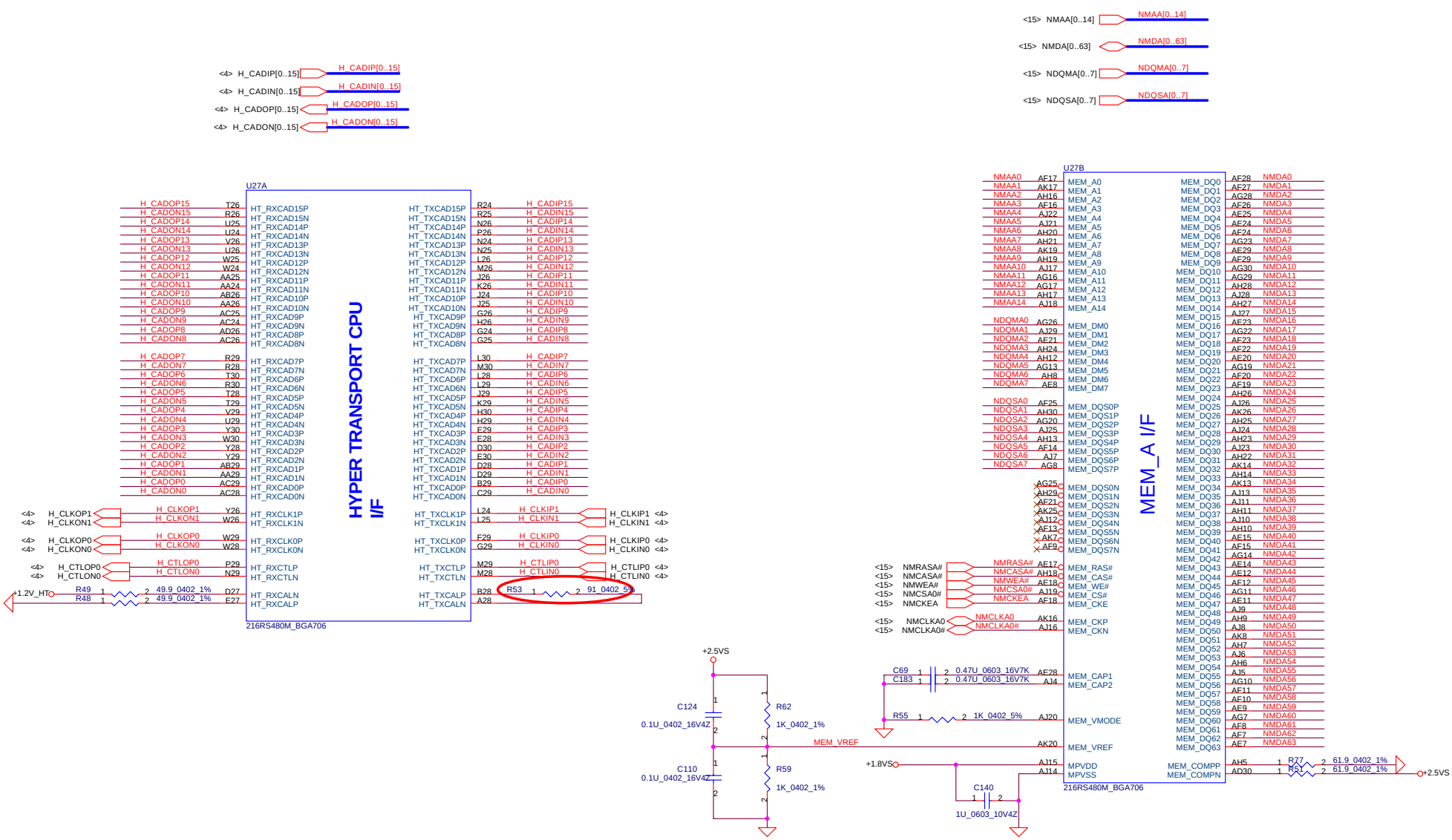
Title: DDR SODIMM Decoupling		
Size: Custom	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 10 of 56	



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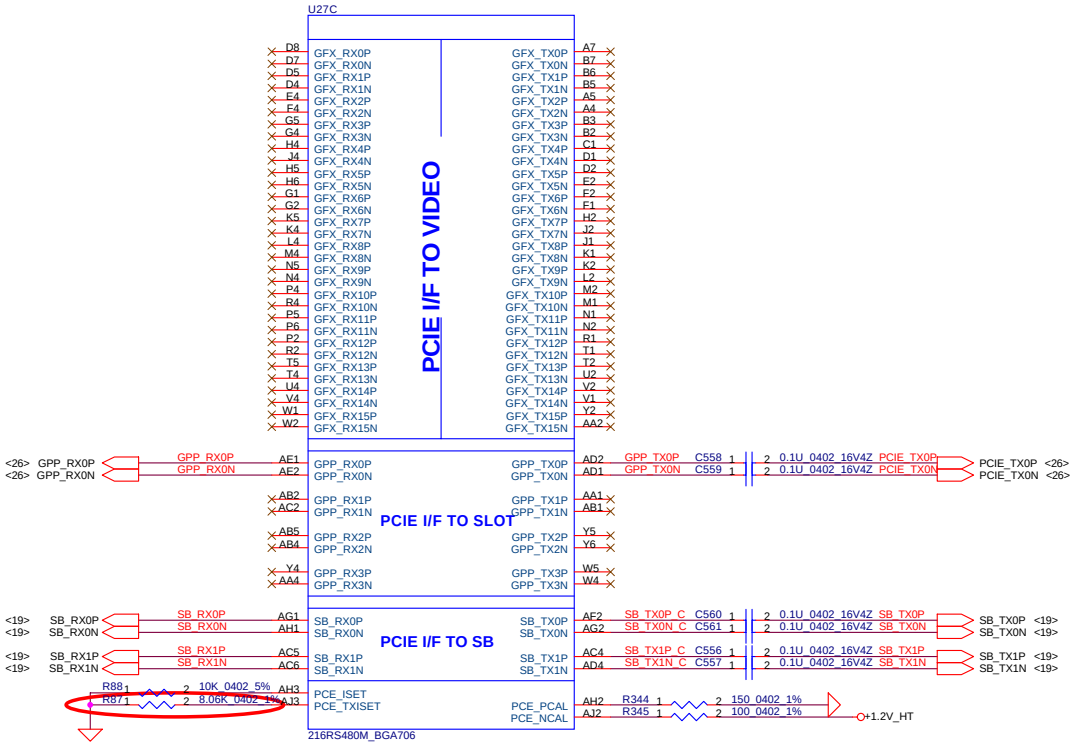
Title	RS480M HT/MEM	
Size	Document Number LA-2421	Rev 0.6
Date: Wednesday, January 05, 2005	Sheet 11 of 56	



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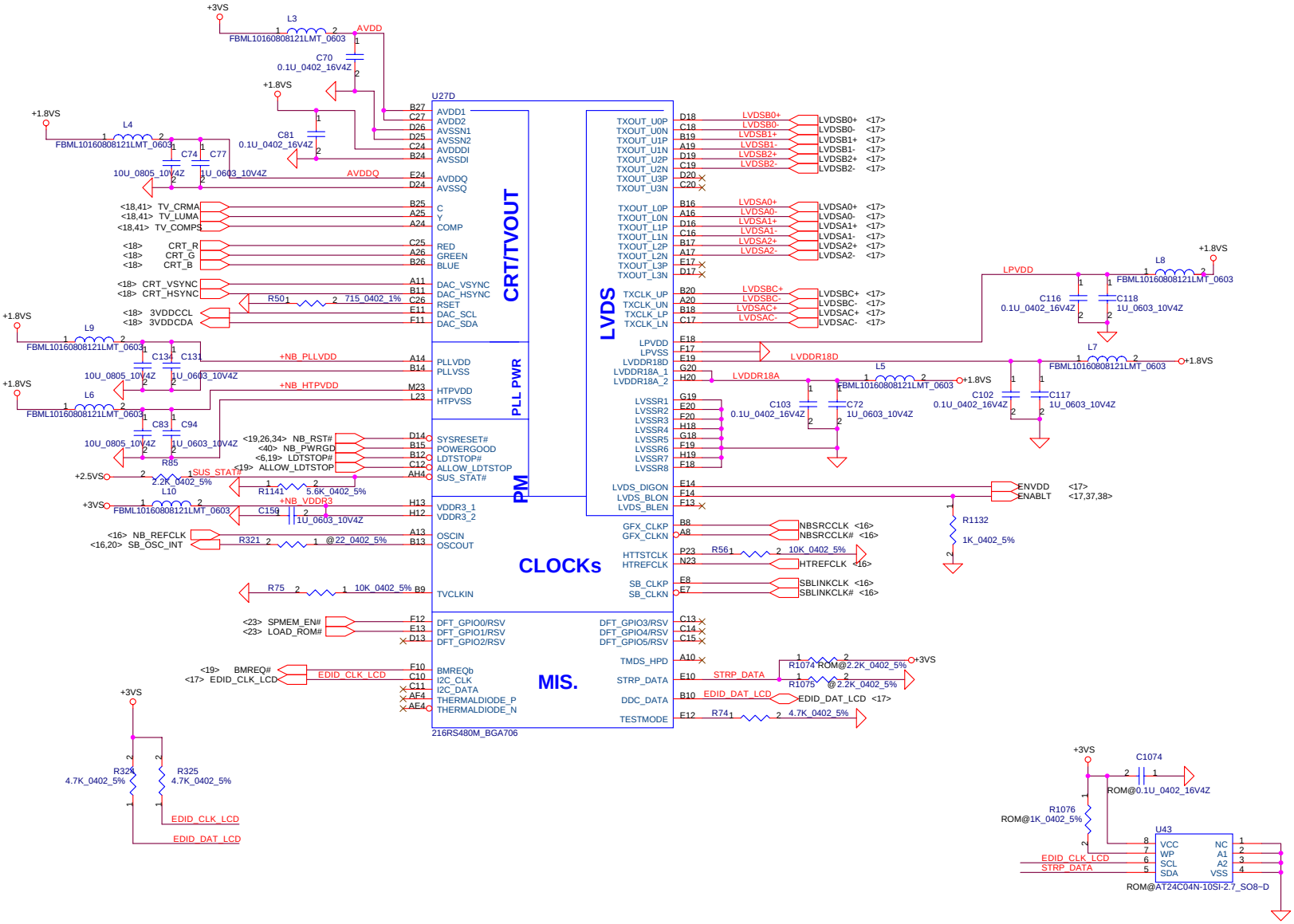
Title: **PCIE**

Size | Document Number: **LA-2421** | Rev: 0.6

Date: Wednesday, January 05, 2005 | Sheet 12 of 56



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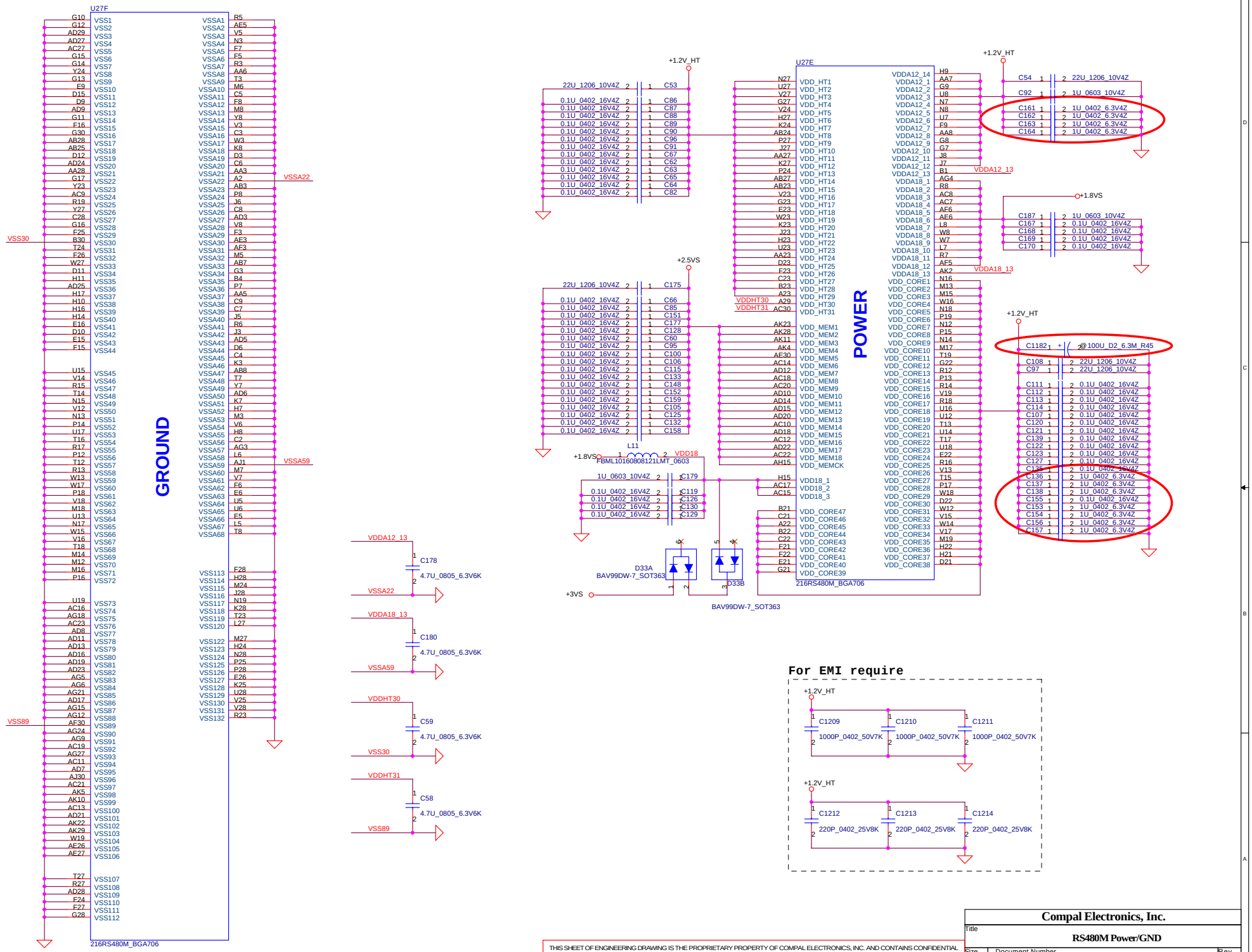
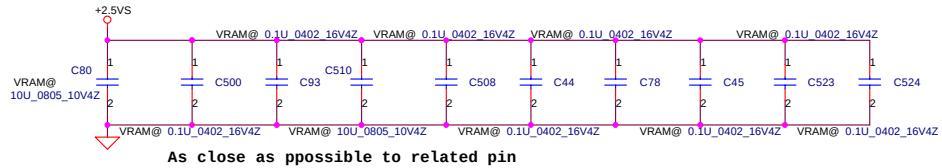
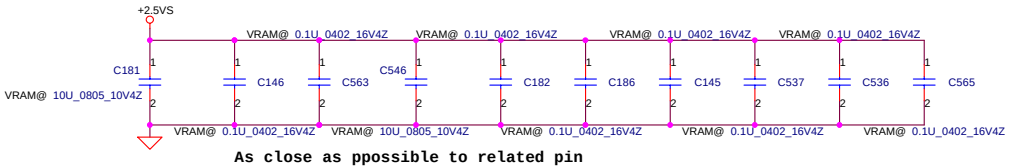
Title	Power/GND	
Size	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 13 of 56	



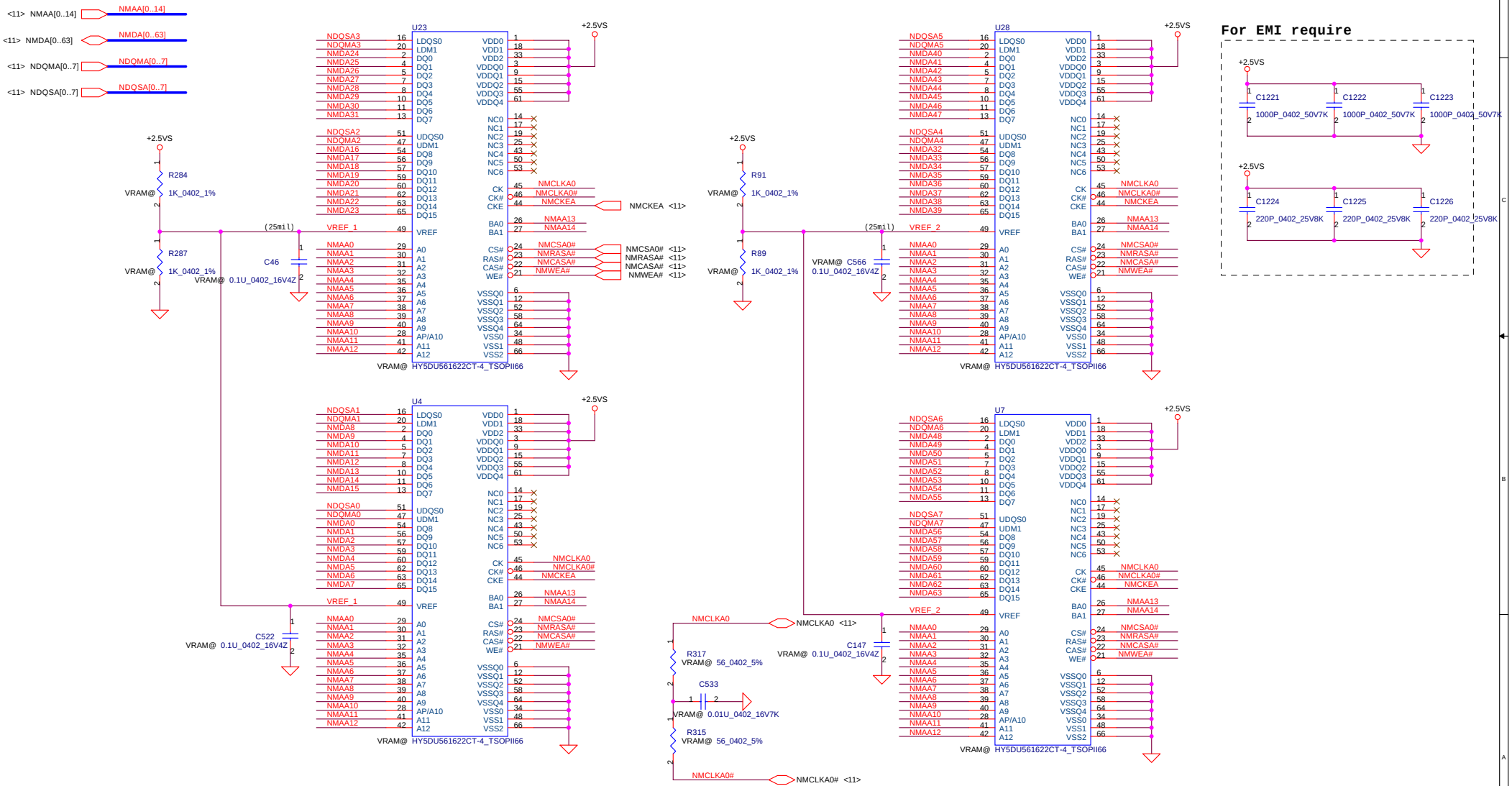
Compal Electronics, Inc.	
Title	RS480M Power/GND
Size	Document Number: LA-2421
Rev	0.6
Date:	Wednesday, January 05, 2005
Sheet	14 of 56



As close as ppossible to related pin



As close as ppossible to related pin



For EMI require

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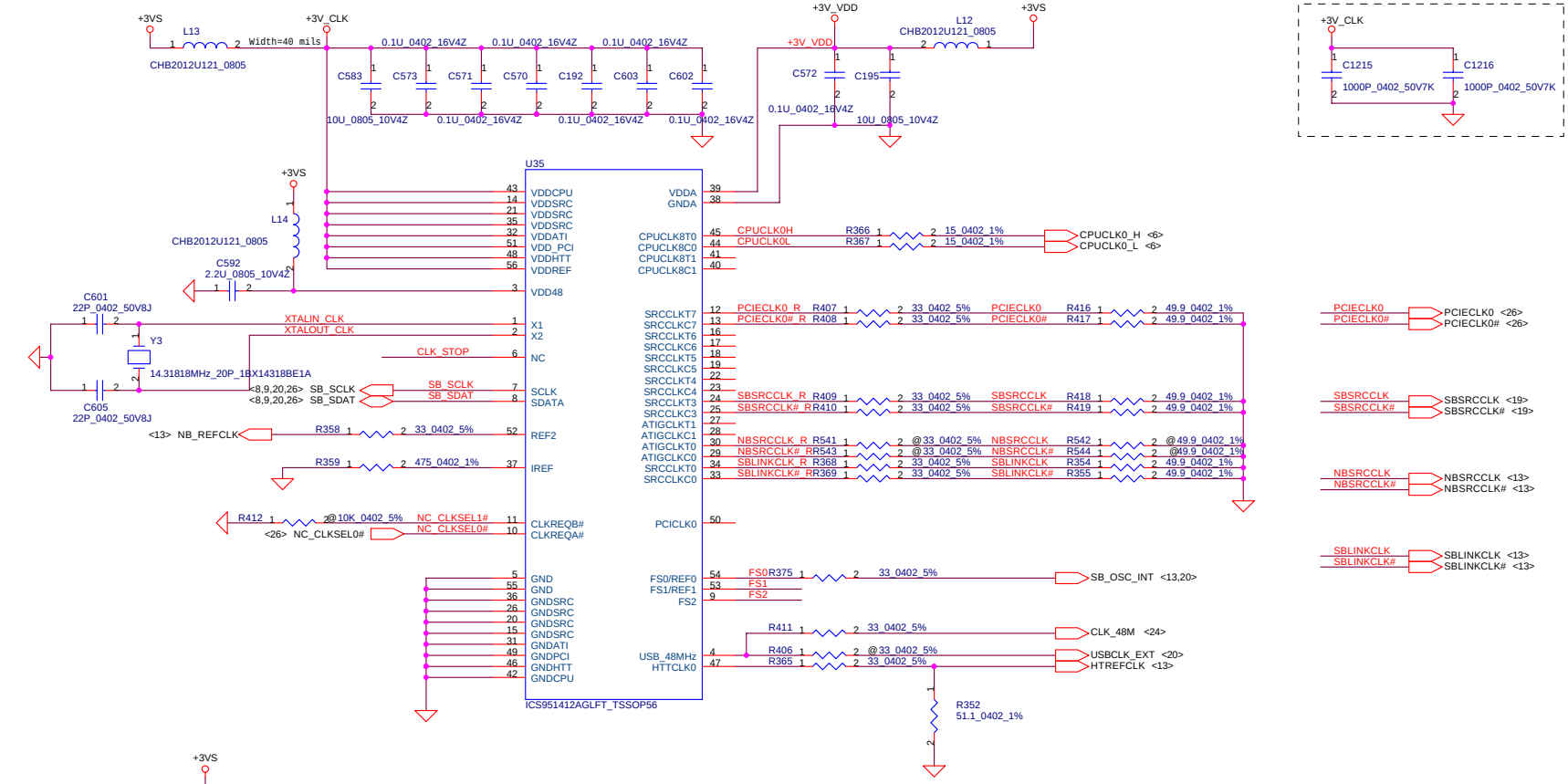
Title: VGADDR		
Size	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 15 of 56	



EXT CLK FREQUENCY SELECT TABLE(MHZ)

	FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
	0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
	0	0	1	X	100.00	X/3	X/6	48.00	Reserved
	0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
	0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
	1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
	1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
*	1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

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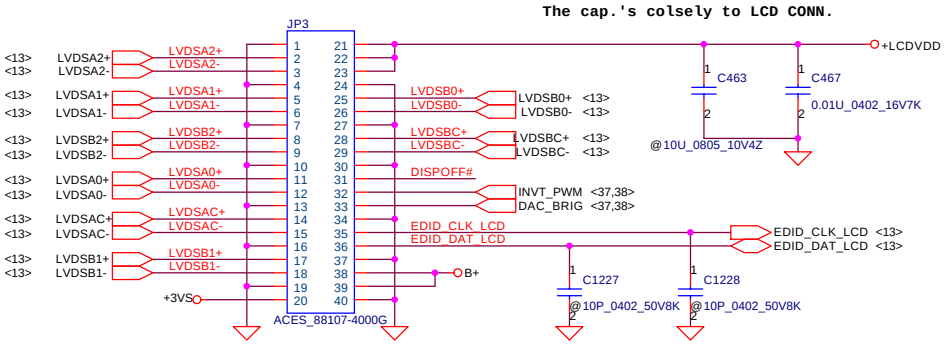
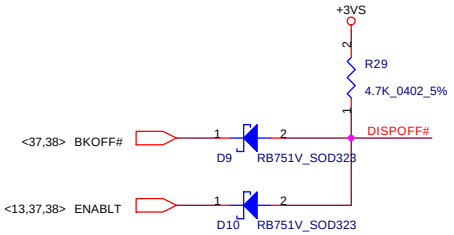
Title: **Clock Generator**

Size: | Document Number: **LA-2421** | Rev: 0.6

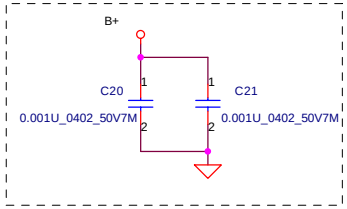
Date: Wednesday, January 05, 2005 | Sheet 16 of 56

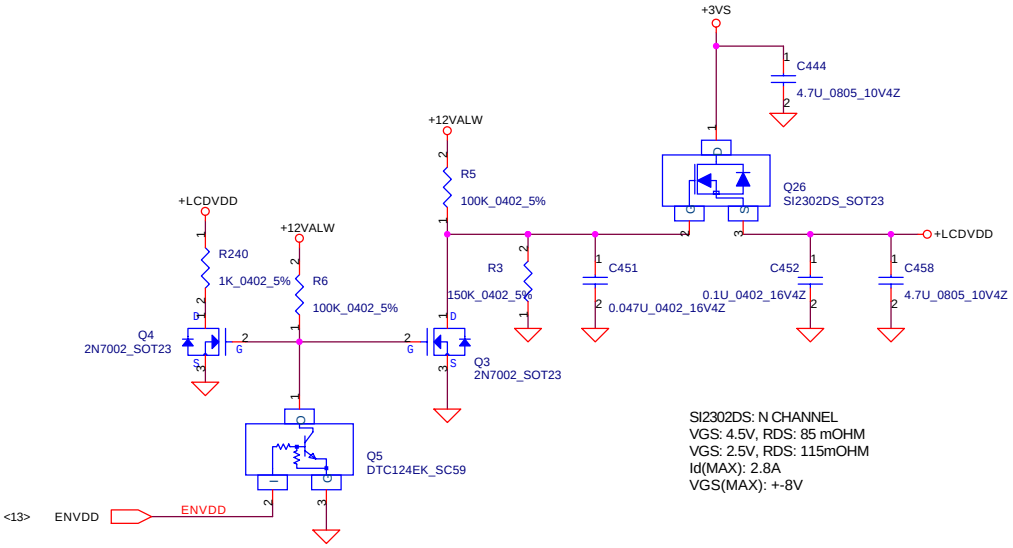
LCD Panel Connector





EMI require





SI2302DS: N CHANNEL
VGS: 4.5V, RDS: 85 mOHM
VGS: 2.5V, RDS: 115mOHM
Id(MAX): 2.8A
VGS(MAX): +-8V

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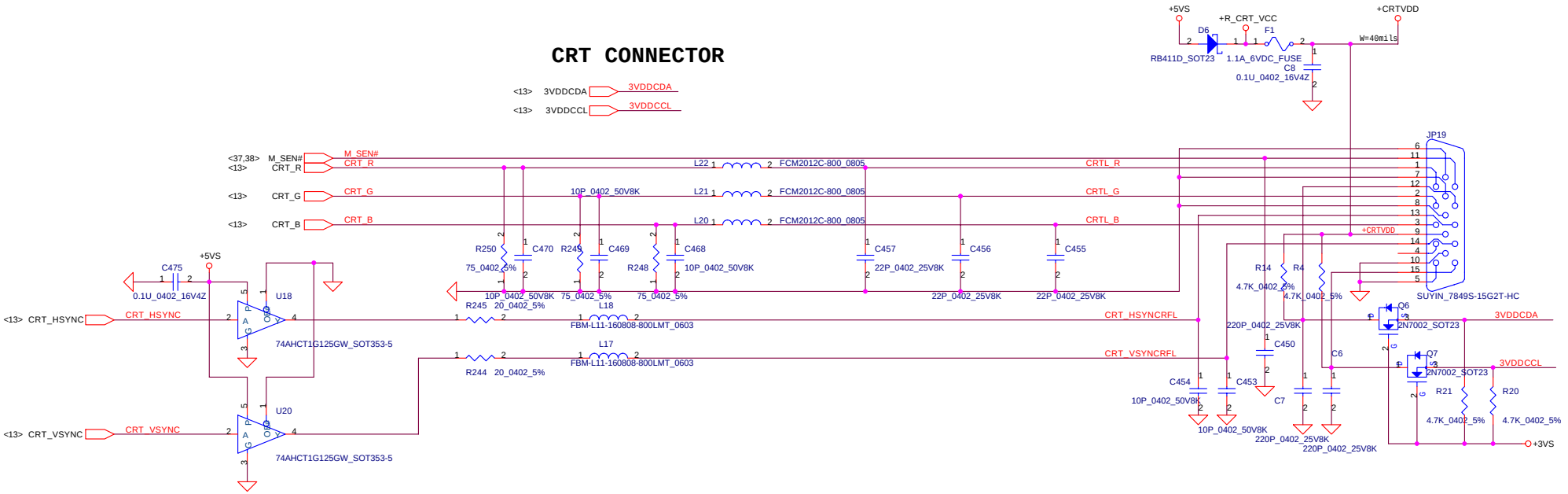
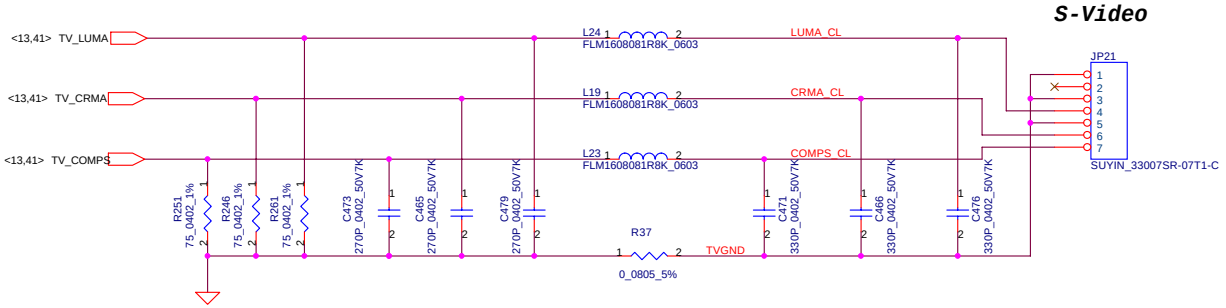
Title: LVDS Connector		
Size	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 17 of 56	

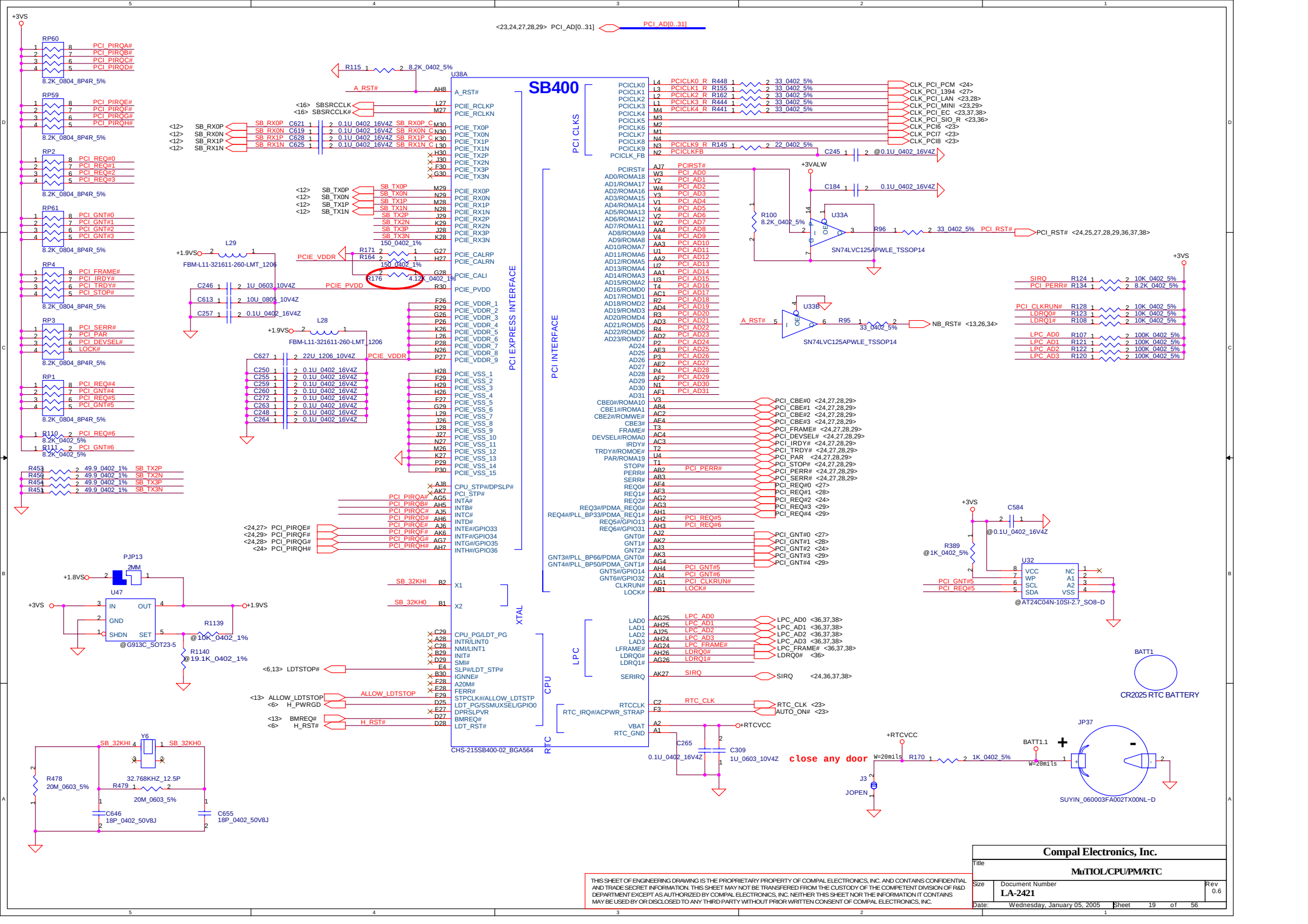
CRT CONNECTOR



TV-Out Connector



Compal Electronics, Inc.		
Title: CRT & TVout Connector		
Size	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 18 of 56	



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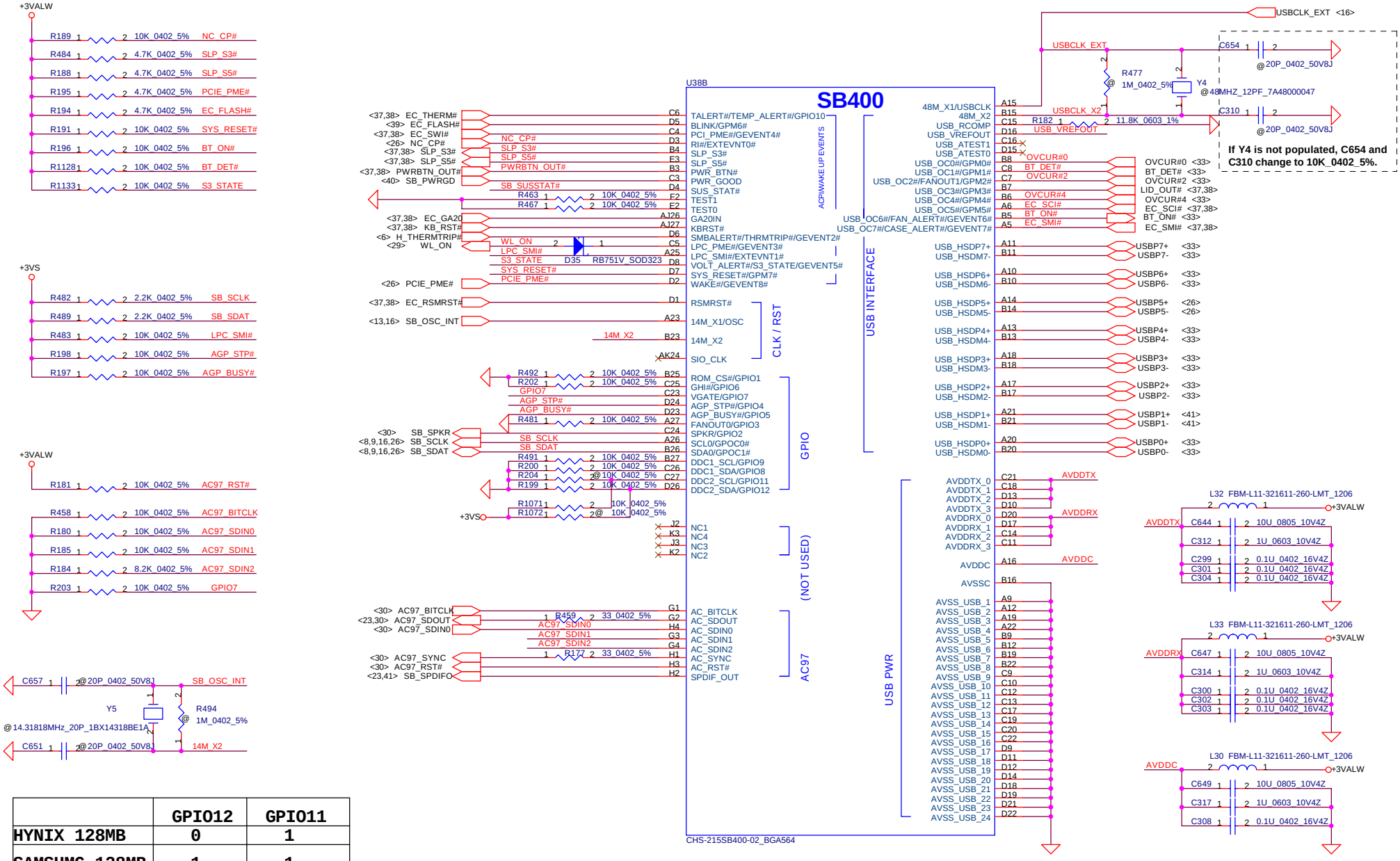
Title	MuTIOL/CPU/PM/RTC
Size	Document Number: LA-2421
Rev	0.6
Date:	Wednesday, January 05, 2005
Sheet	19 of 56



	GPIO12	GPIO11
HYNIX 128MB	0	1
SAMSUMG 128MB	1	1
No VRAM	0	0
Reserved	1	0

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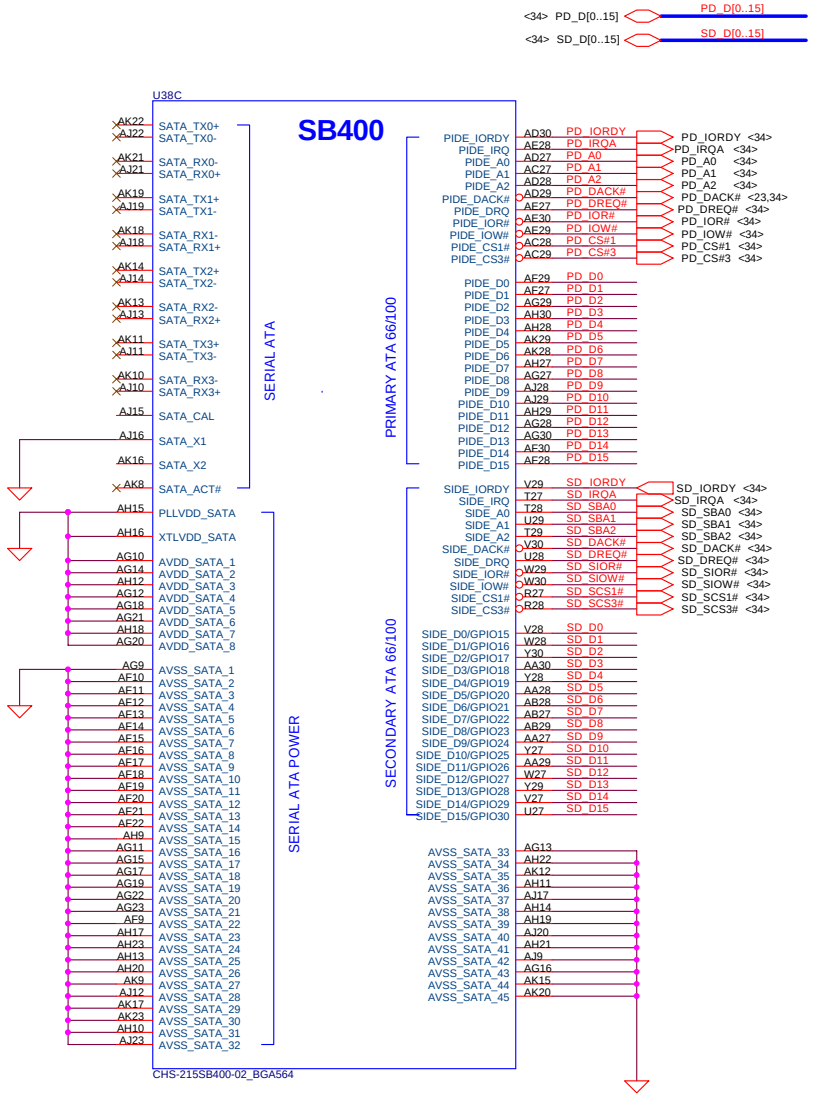
Title: USB/LPC/AC97/MAC

Size | Document Number: LA-2421 | Rev: 0.6

Date: Wednesday, January 05, 2005 | Sheet 20 of 56

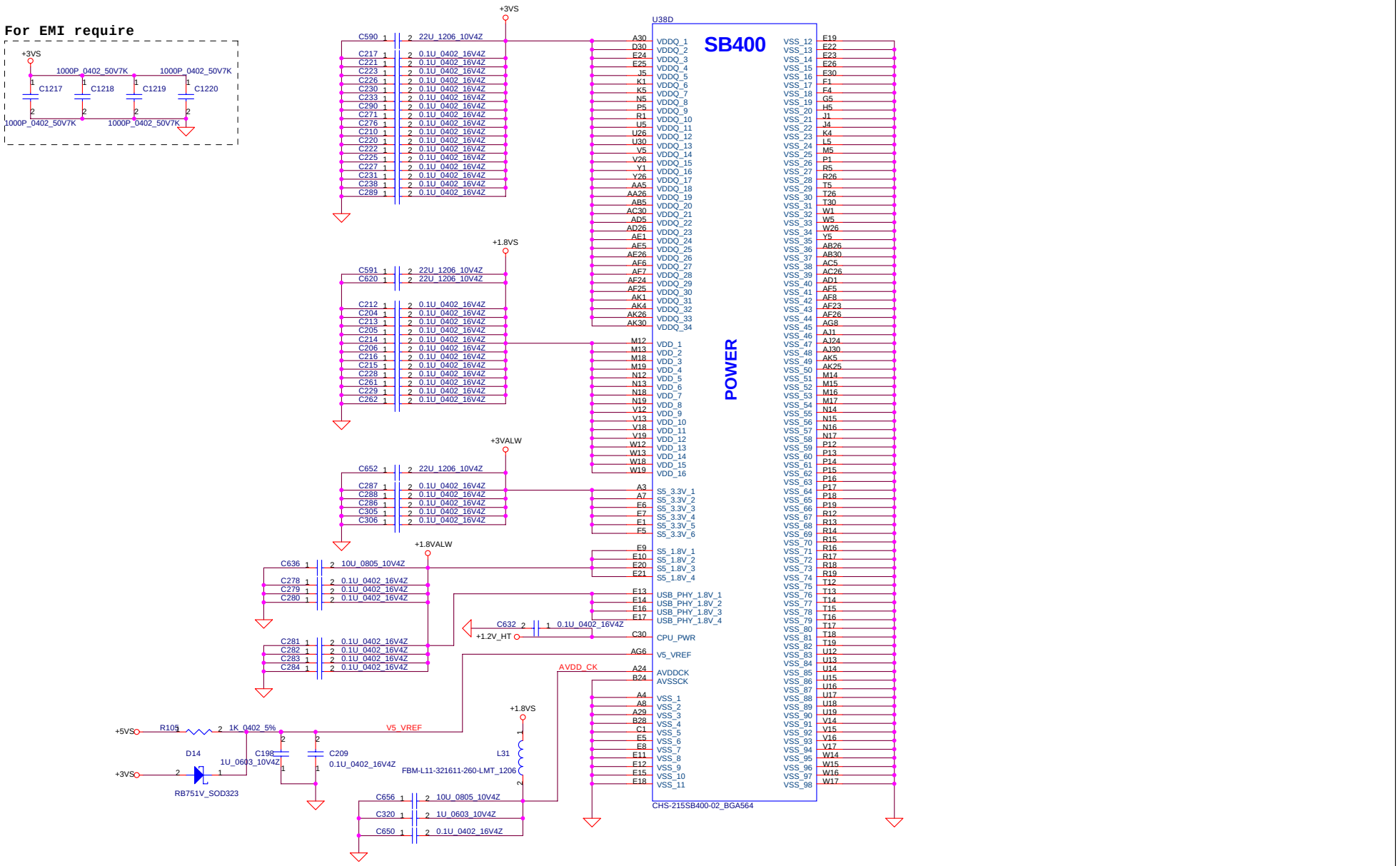


Compal Electronics, Inc.

Title: **IDE/SATA**

Size	Document Number	Rev
Custom	LA-2421	0.6

Date: Wednesday, January 05, 2005 | Sheet 21 of 56



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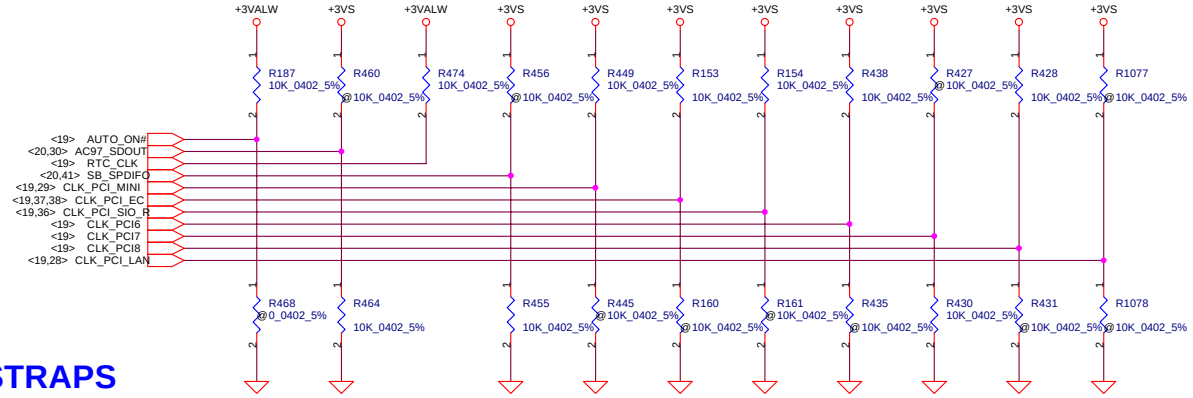
Title	Power/GND	
Size	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 22 of 56	

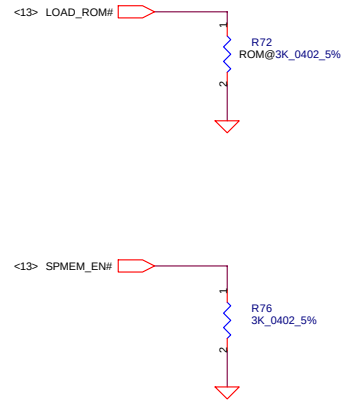
REQUIRED STRAPS



ACPWRON

	AUTO_ON#	AC97_SDOUT	RTC_CLK	SB_SPDIFO	CLK_PCI_LAN	CLK_PCI_MINI	CLK_PCI_EC	CLK_PCI_SIO	CLK_PCI6	CLK_PCI7 PCI_CLK8
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz XTAL MODE	USB PHY PWRDOWN DISABLE DEFAULT	INTERNAL 48MHz DEFAULT	14MHz OSC MODE DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM L,H = NORMAL LPC ROM DEFAULT L,L = FWH ROM
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz OSC MODE DEFAULT	USB PHY PWRDOWN ENABLE	EXTERNAL 48MHz	14MHz XTAL MODE	CPU I/F = P4	

NB STRAPS



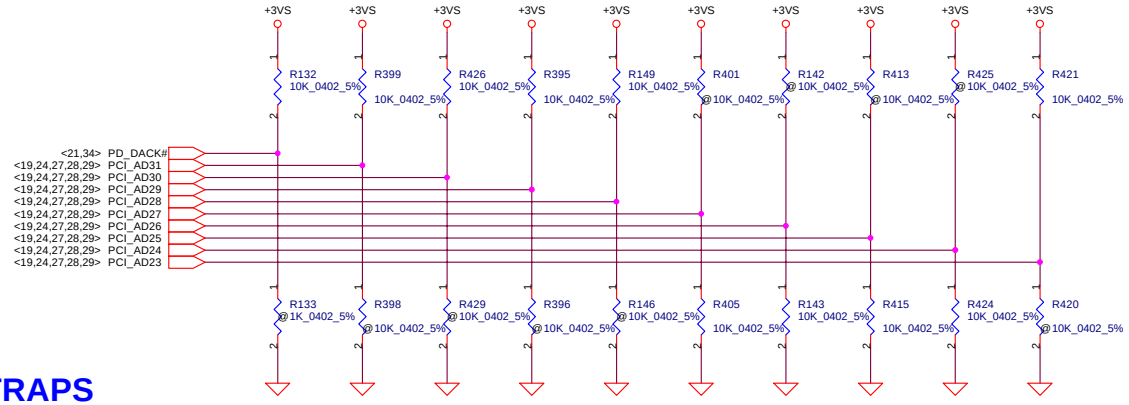
LOAD_ROM#:LOAD ROM STRAP ENABLE strap

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

SPMEM_EN#:SIDE PORT MEMORY ENABLE strap

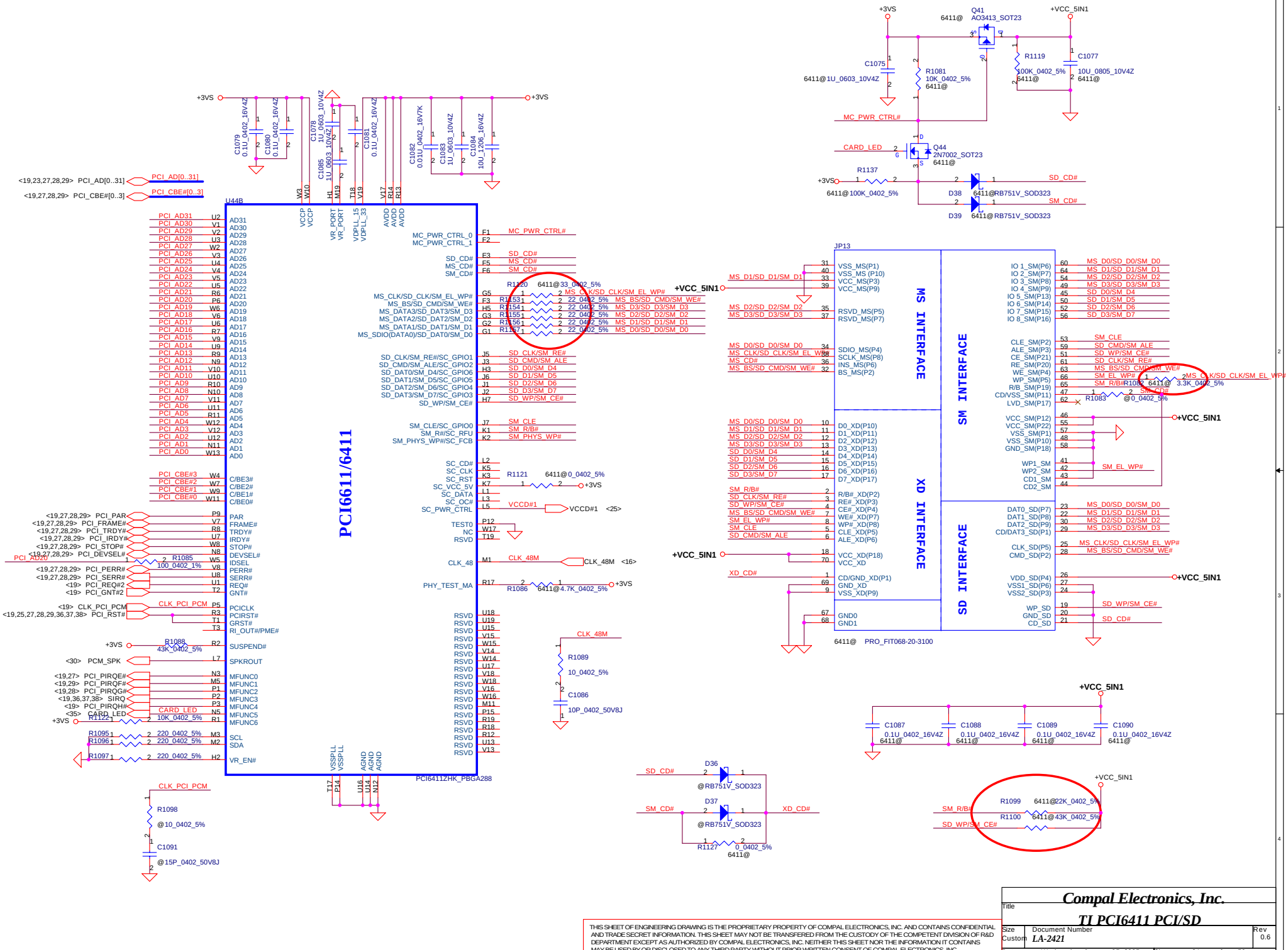
High, SIDE PORT MEMORY DISABLE
Low, SIDE PORT MEMORY ENABLE

DEBUG STRAPS



	PD_DACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

Compal Electronics, Inc.
Title: Hardware Trap
Size: Document Number: LA-2421
Rev: 0.6
Date: Wednesday, January 05, 2005
Sheet 23 of 56

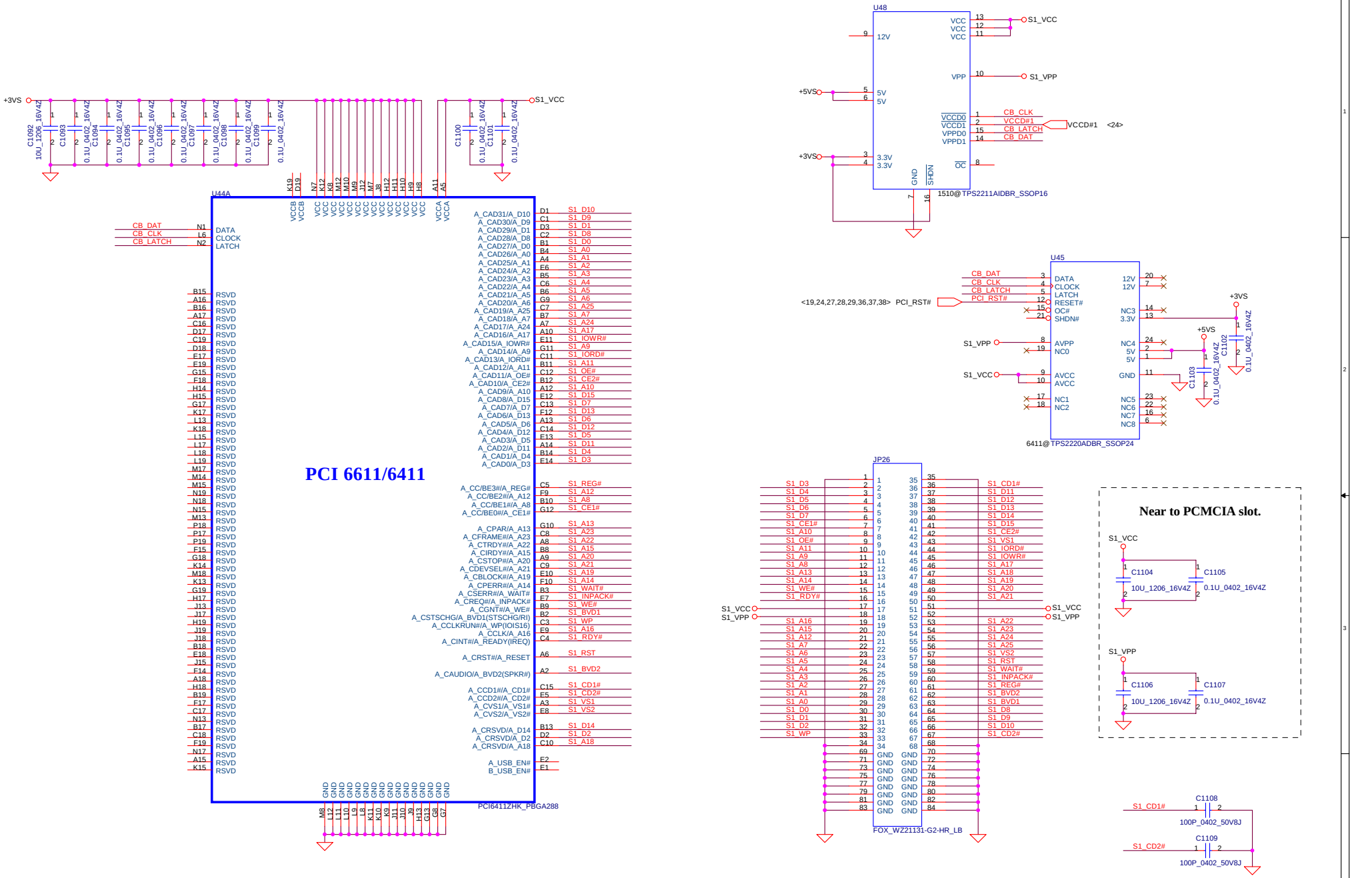


Compal Electronics, Inc.

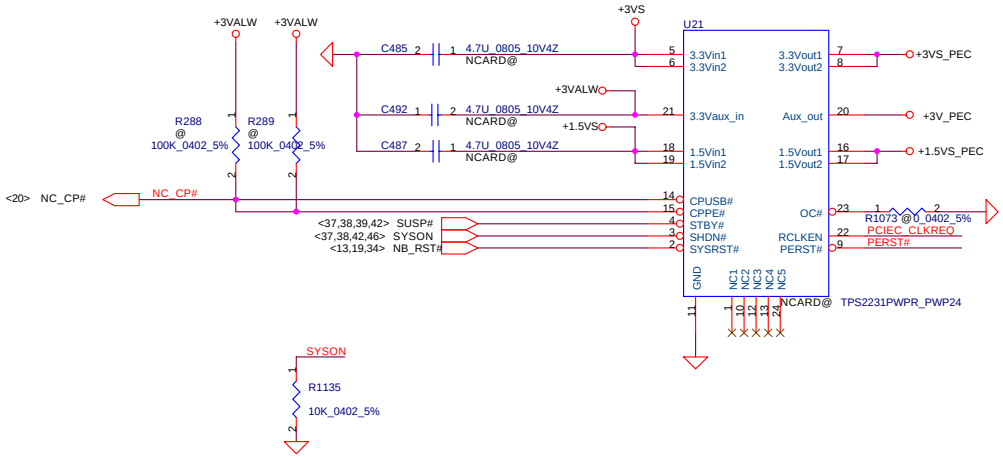
Title: TI PCI6411 PCI/SD

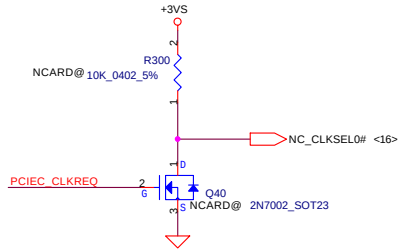
Size: Custom | Document Number: LA-2421 | Rev: 0.6

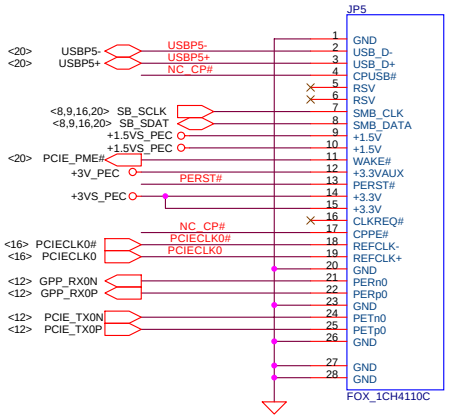
Date: Wednesday, January 05, 2005 | Sheet 24 of 56



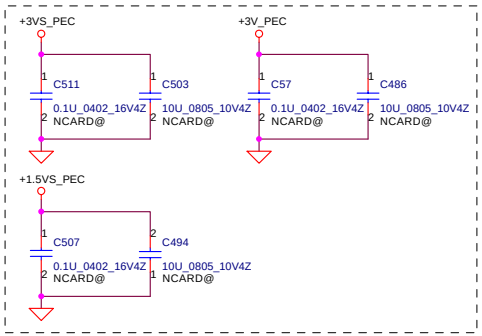
Compal Electronics, Inc.		
Title: TI PCI6411 CB socket		
Size: Custom	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 25 of 56	







Near to Express Card slot.

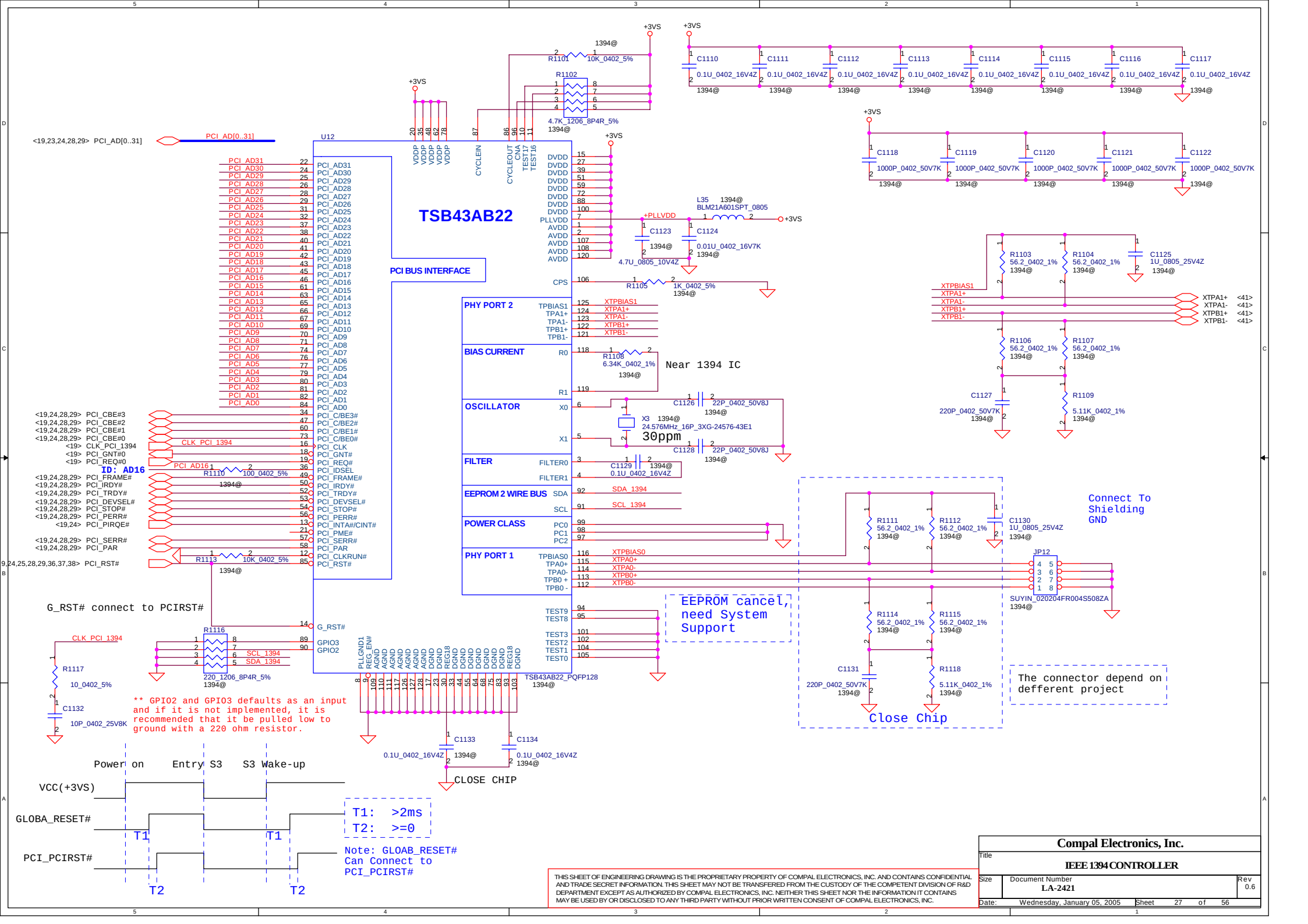


Compal Electronics, Inc.

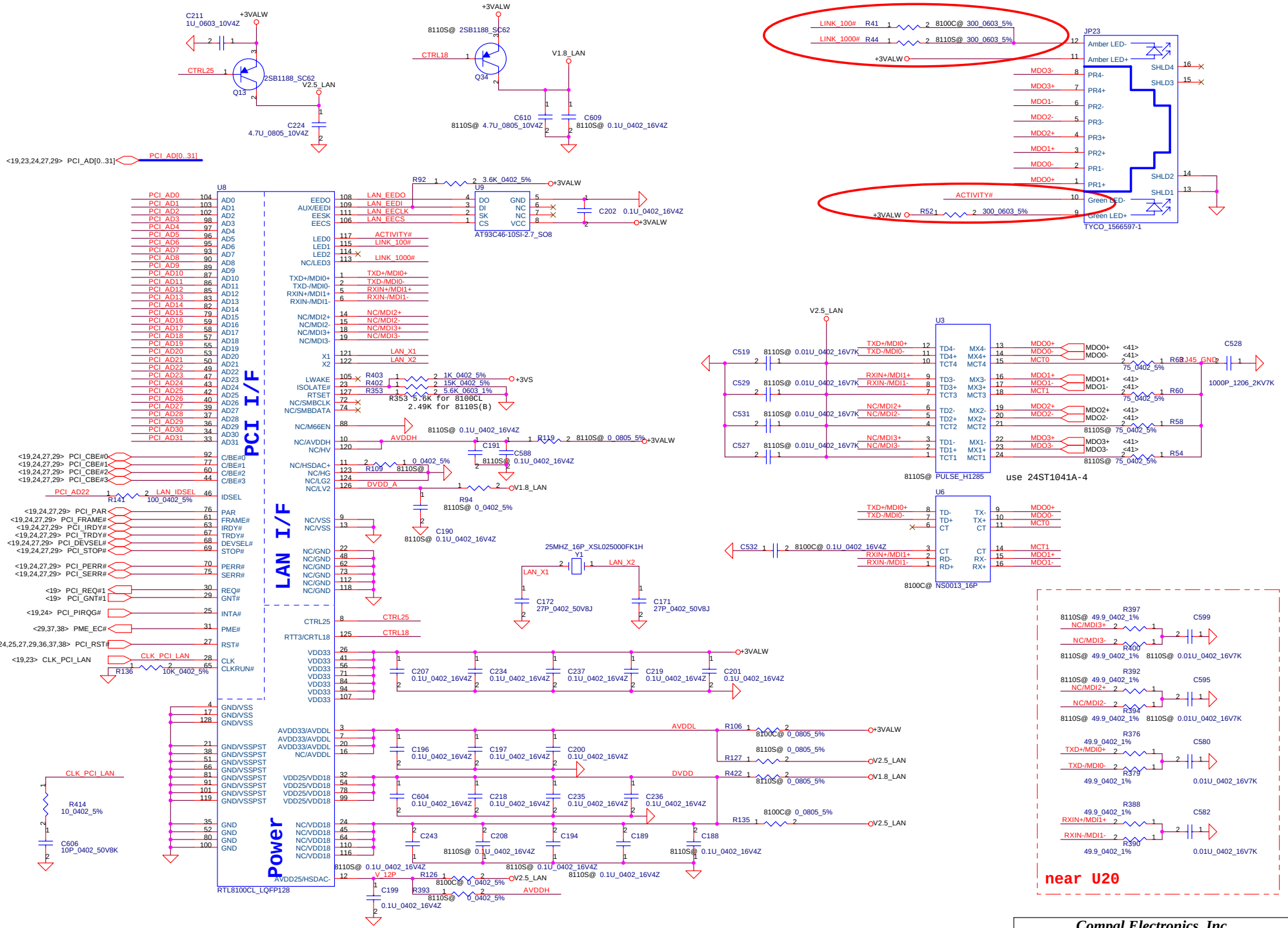
Title: Express Card socket

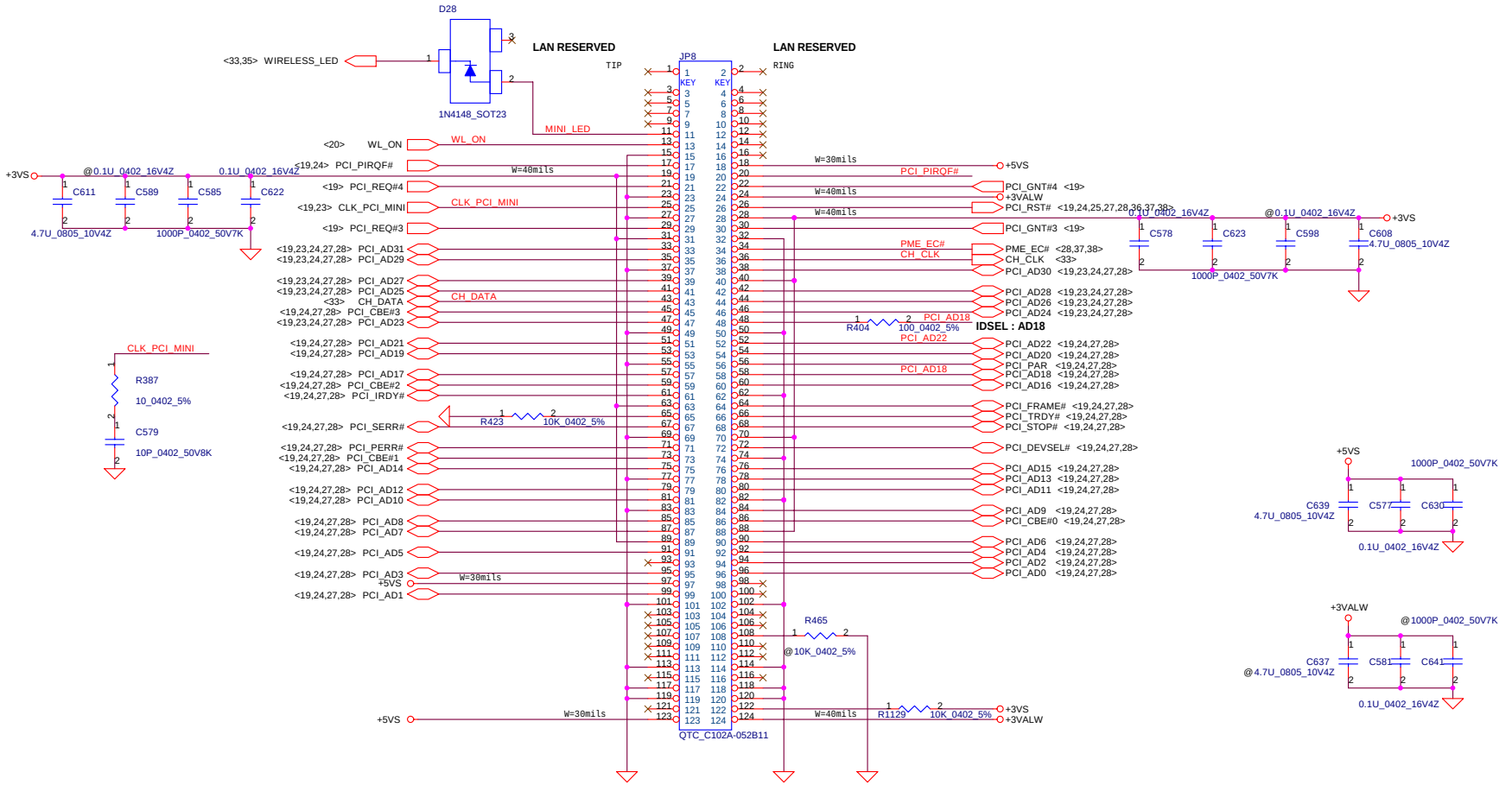
Size: Custom | Document Number: LA-2421 | Rev: 0.6

Date: Wednesday, January 05, 2005 | Sheet 26 of 56



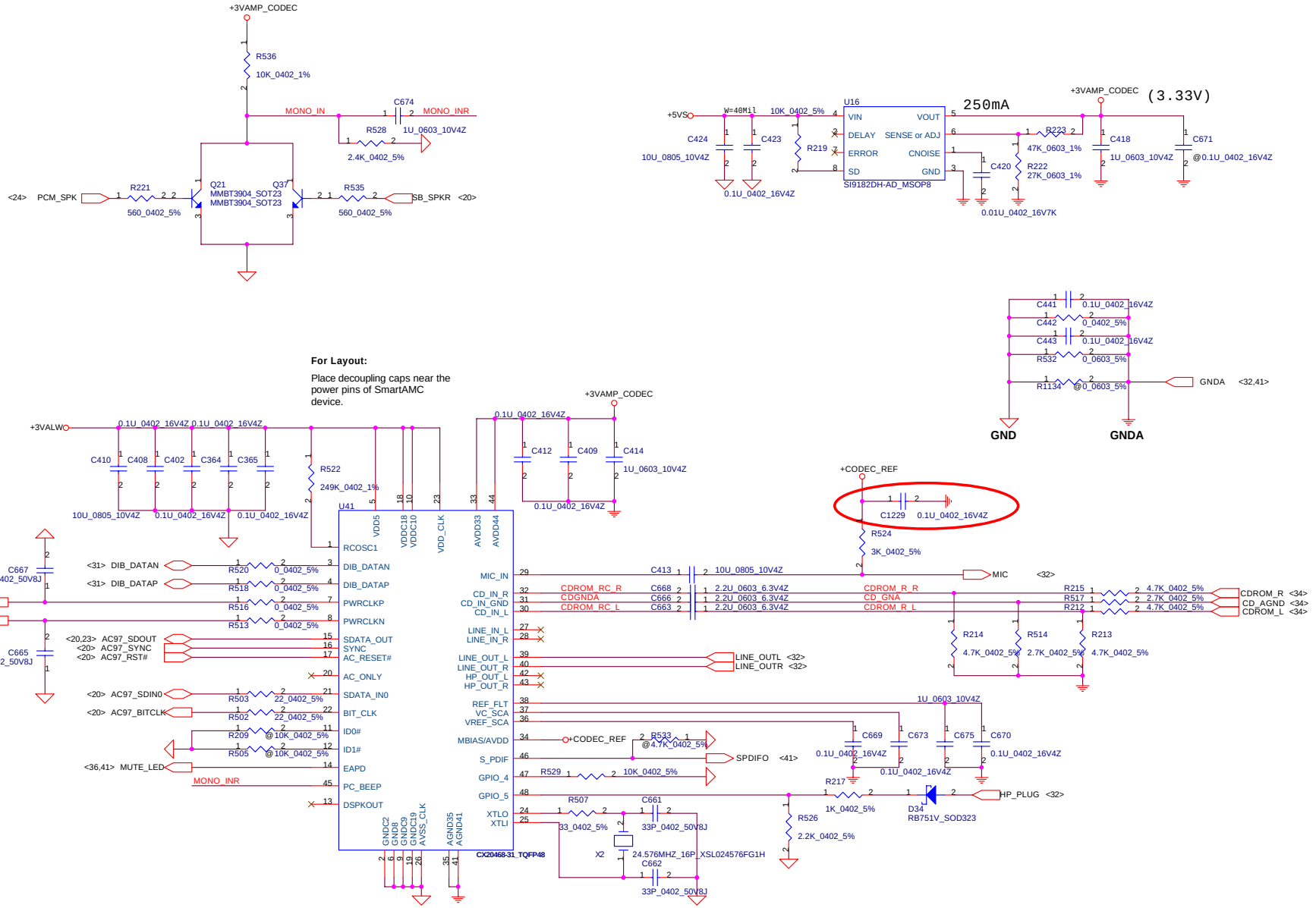
Compal Electronics, Inc.	
Title	IEEE 1394 CONTROLLER
Size	Document Number: LA-2421
Rev	0.6
Date:	Wednesday, January 05, 2005
Sheet	27 of 56



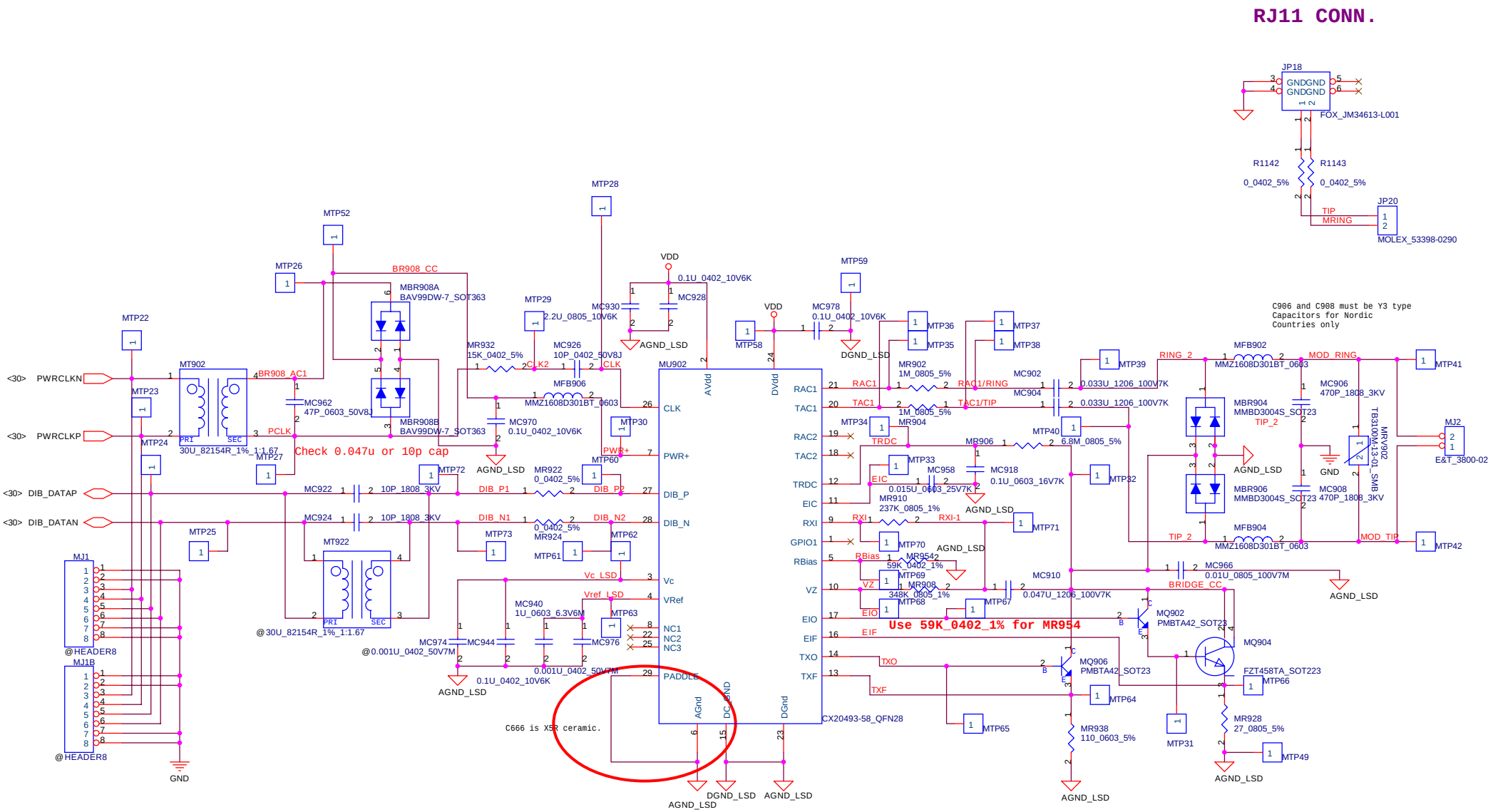


Compal Electronics, Inc.

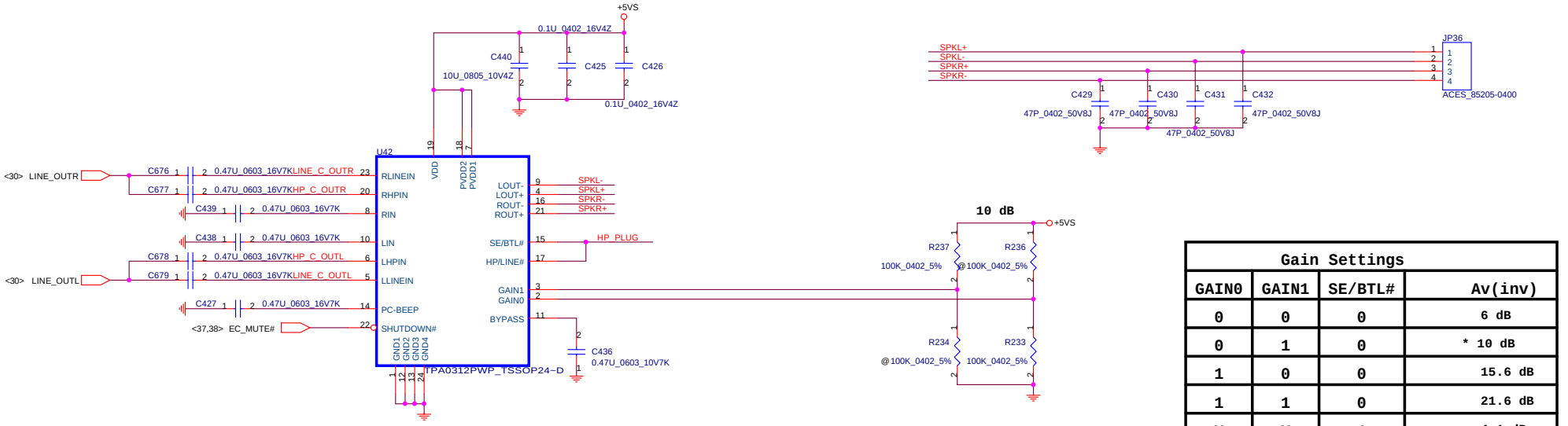
Title	Mini PCI Slot	
Size	Document Number LA-2421	Rev 0.6
Date: Wednesday, January 05, 2005	Sheet 29 of 56	



Compal Electronics, Inc.		
Title: Codec CX20468-31		
Size	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 30 of 56	

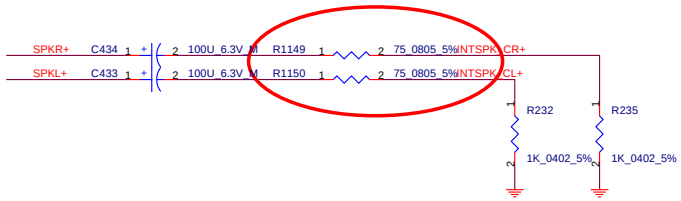


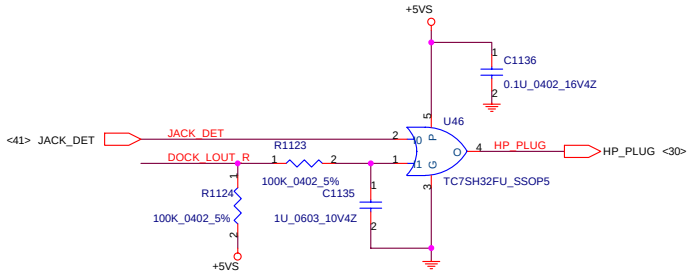
Compal Electronics, Inc.		
Title: AMOM_modem		
Size	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 31 of 56	

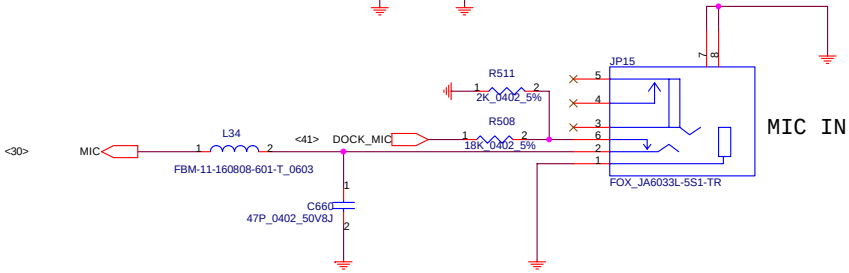


Gain Settings			
GAIN0	GAIN1	SE/BTL#	Av(inv)
0	0	0	6 dB
0	1	0	* 10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

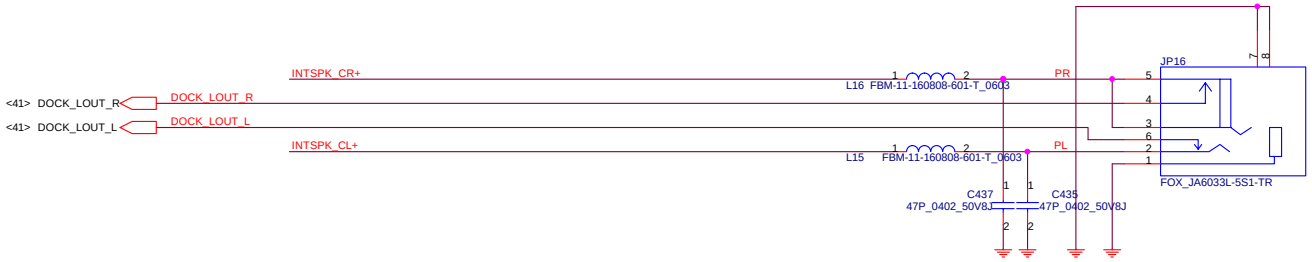
HEADPHONE OUT/LINE OUT







MIC IN

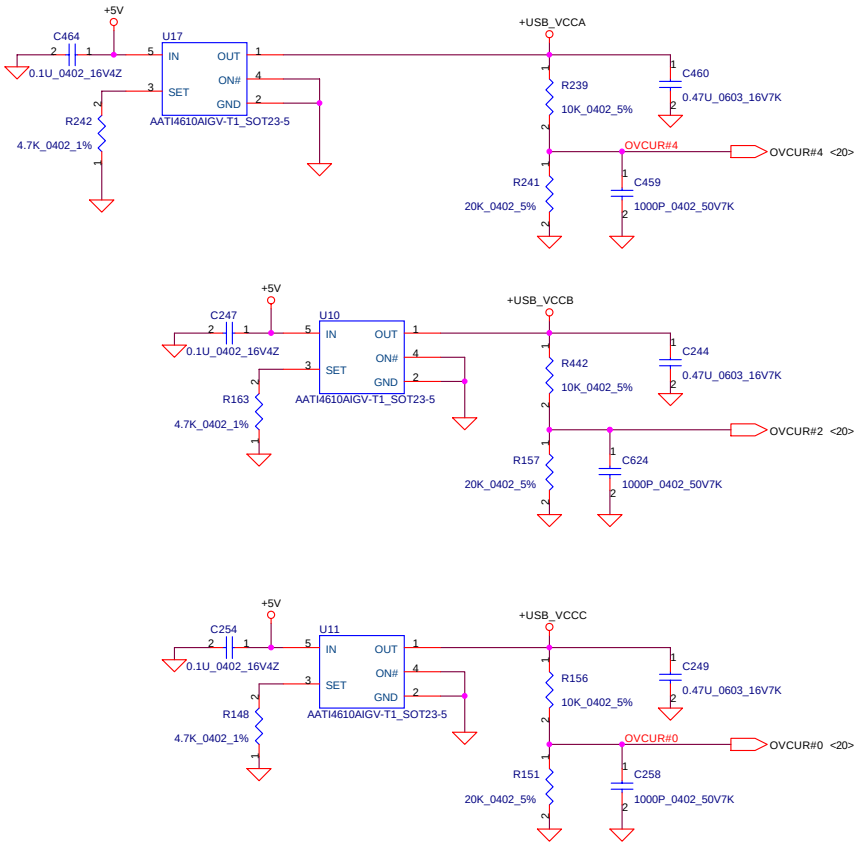


Compal Electronics, Inc.

Title: AMP & Audio Jack

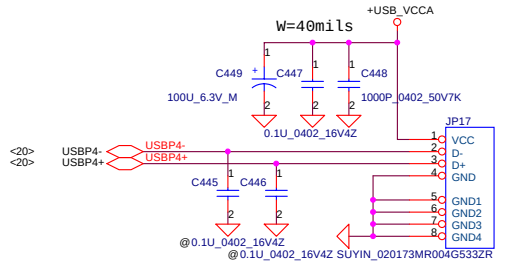
Size: Custom | Document Number: LA-2421 | Rev: 0.6

Date: Wednesday, January 05, 2005 | Sheet 32 of 56

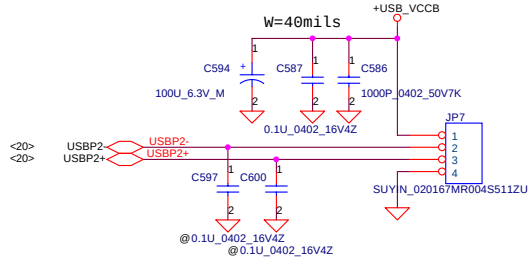


Note: PLACE CLOSE TO EACH USB PORT

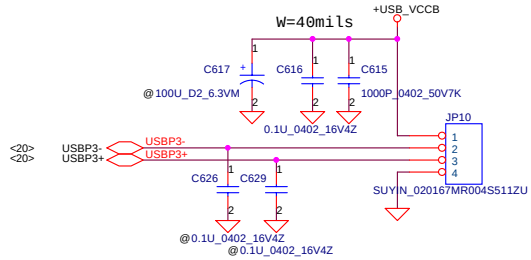
USB CONNECTOR 1(Rear side)



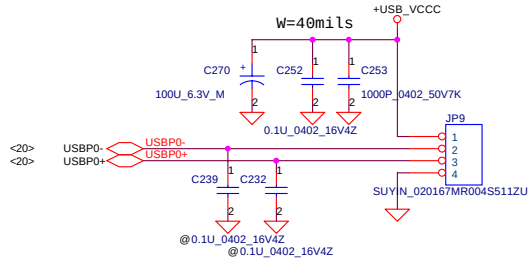
USB CONNECTOR 2(Left side)



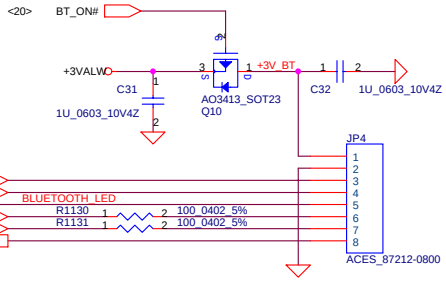
USB CONNECTOR 3(Left side)



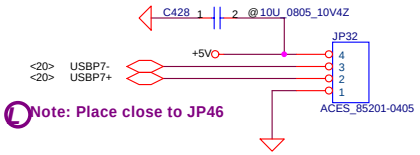
USB CONNECTOR 4(Right side)



BT CONNECTOR



USB KEY

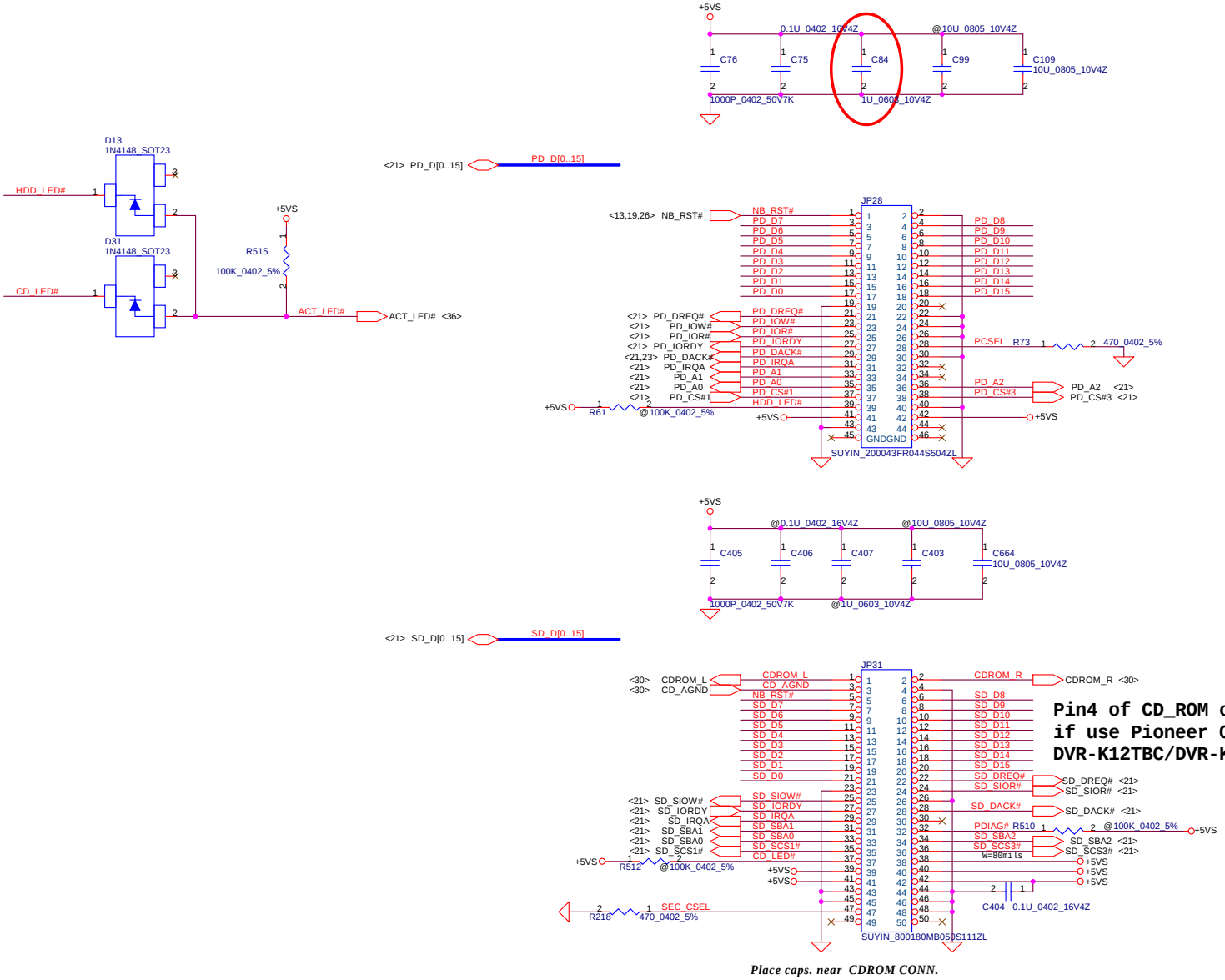


Note: Place close to JP46

Compal Electronics, Inc.		
Title: Bluetooth & USB CONN.		
Size	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 33 of 56	

HDD/CD-ROM Module

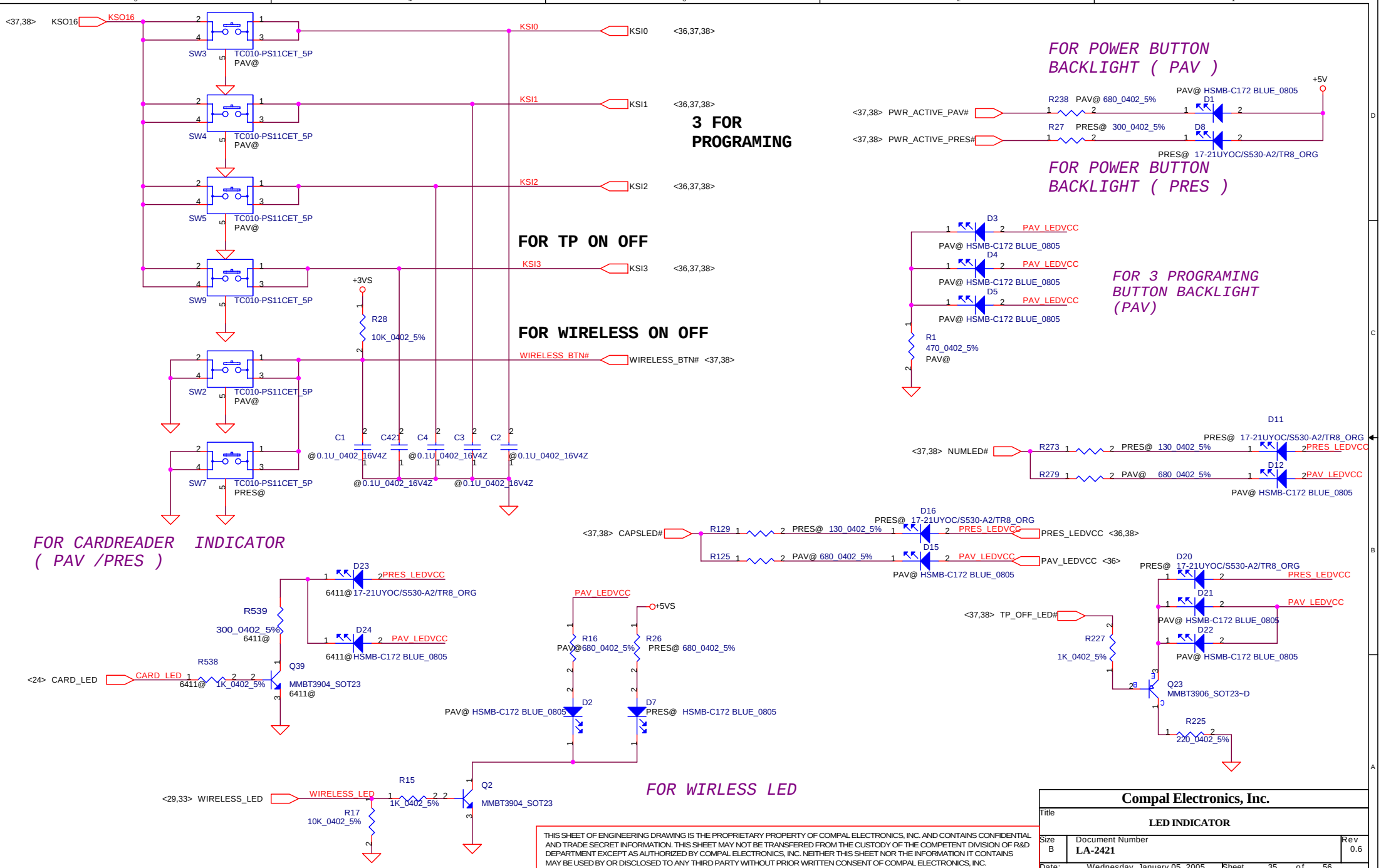
Placea caps. near HDD CONN.



Pin4 of CD_ROM connector is NC if use Pioneer ODD(DVD Dual DVR-K12TBC/DVR-K13TBC)

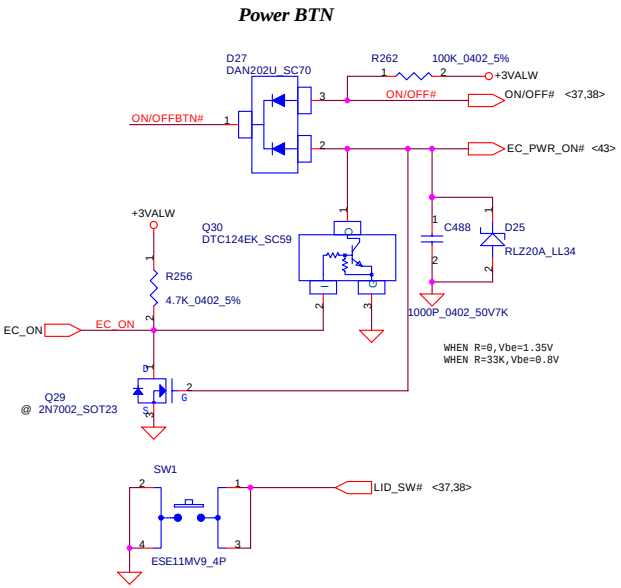
Place caps. near CDROM CONN.

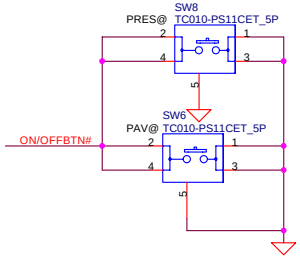
Compal Electronics, Inc.		
Title: HDD & CDROM Connector		
Size	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 34 of 56	



INT_KBD CONN.

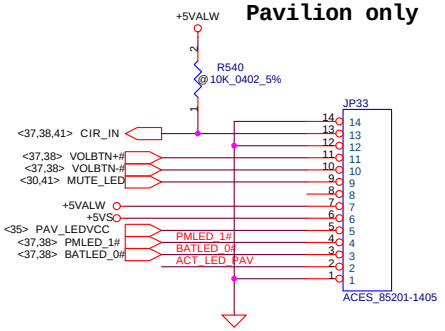
Power BTN



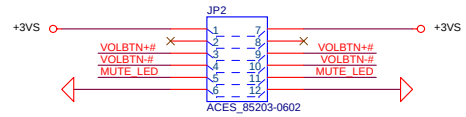


Front Board CONNECTOR

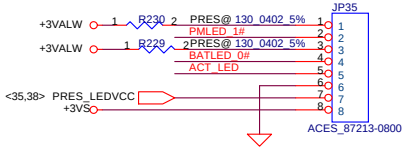
Pavilion only



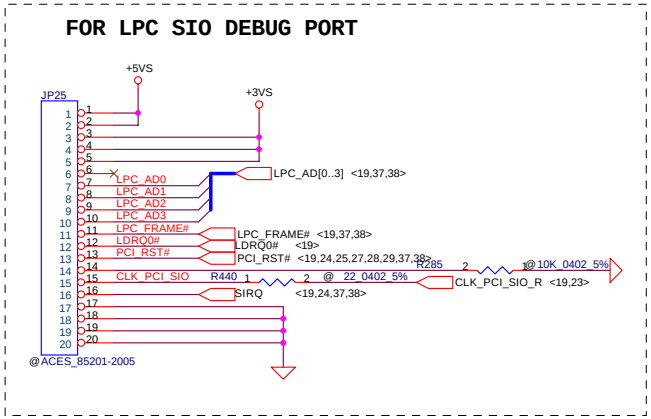
PRESARIO only

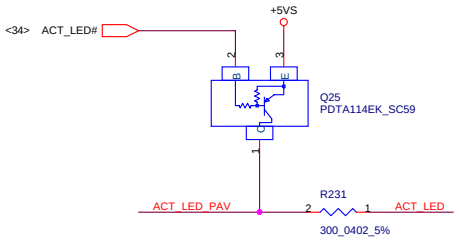


PRESARIO only

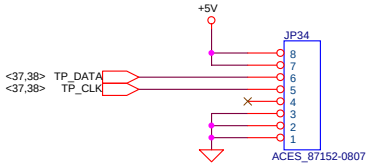


FOR LPC SIO DEBUG PORT

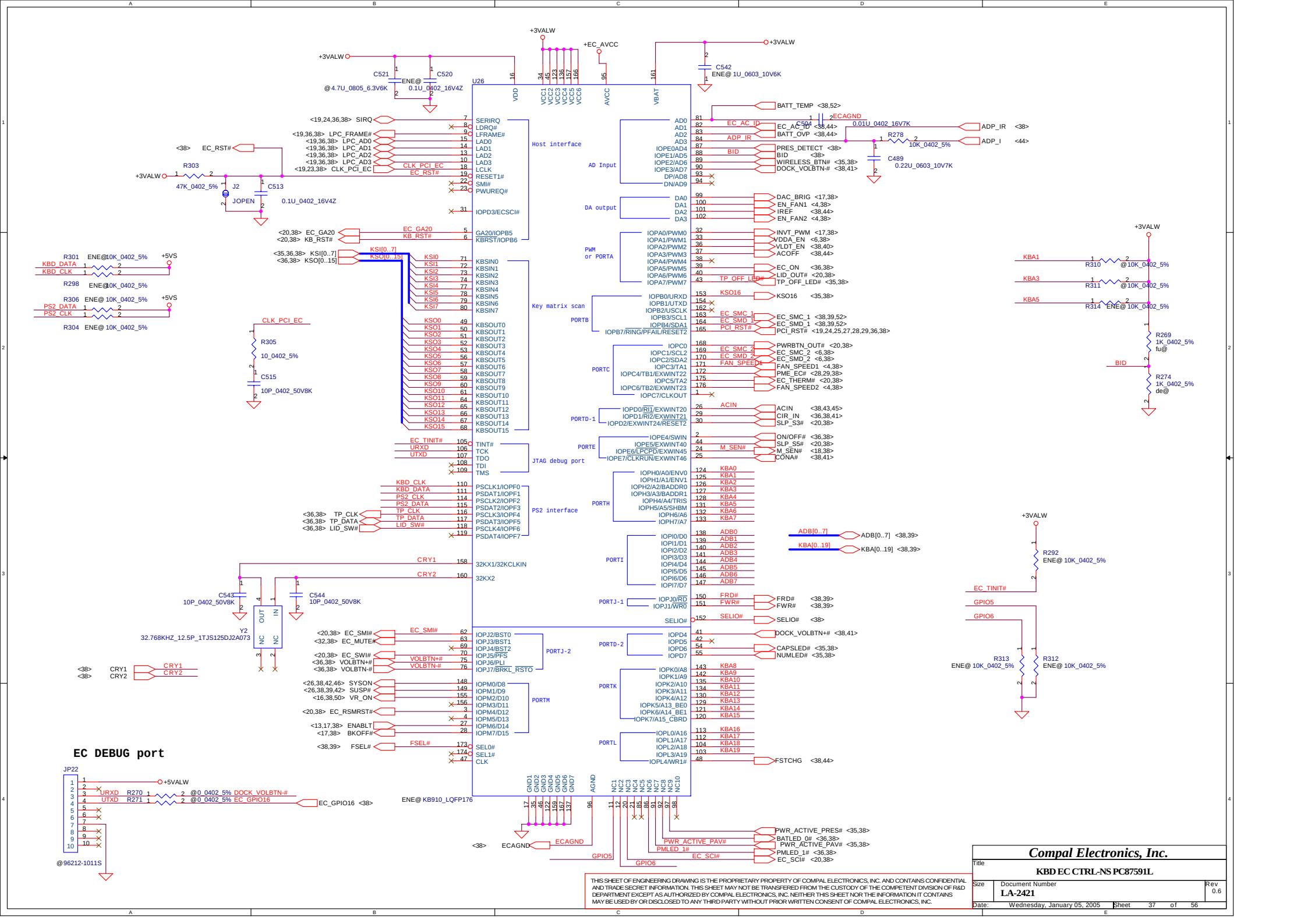




TP CONNECTOR



Compal Electronics, Inc.		
Title: KBD,ON/OFF,T/P,LED/B		
Size	Document Number: LA-2421	Rev: 0.6
Date: Wednesday, January 05, 2005	Sheet 36 of 56	


U26
ENE@ KB910_LQFP176
EC DEBUG port
JP22
@96212-1011S
Host interface
AD Input
DA output
PWM or PORTA
Key matrix scan
PORTB
PORTC
PORTD-1
PORTE
JTAG debug port
PS2 interface
PORTH
PORTI
PORTJ-1
PORTJ-2
PORTD-2
PORTK
PORTL
PORTM
Compal Electronics, Inc.
KBD EC CTRL-NS PC87591L
LA-2421
Wednesday, January 05, 2005
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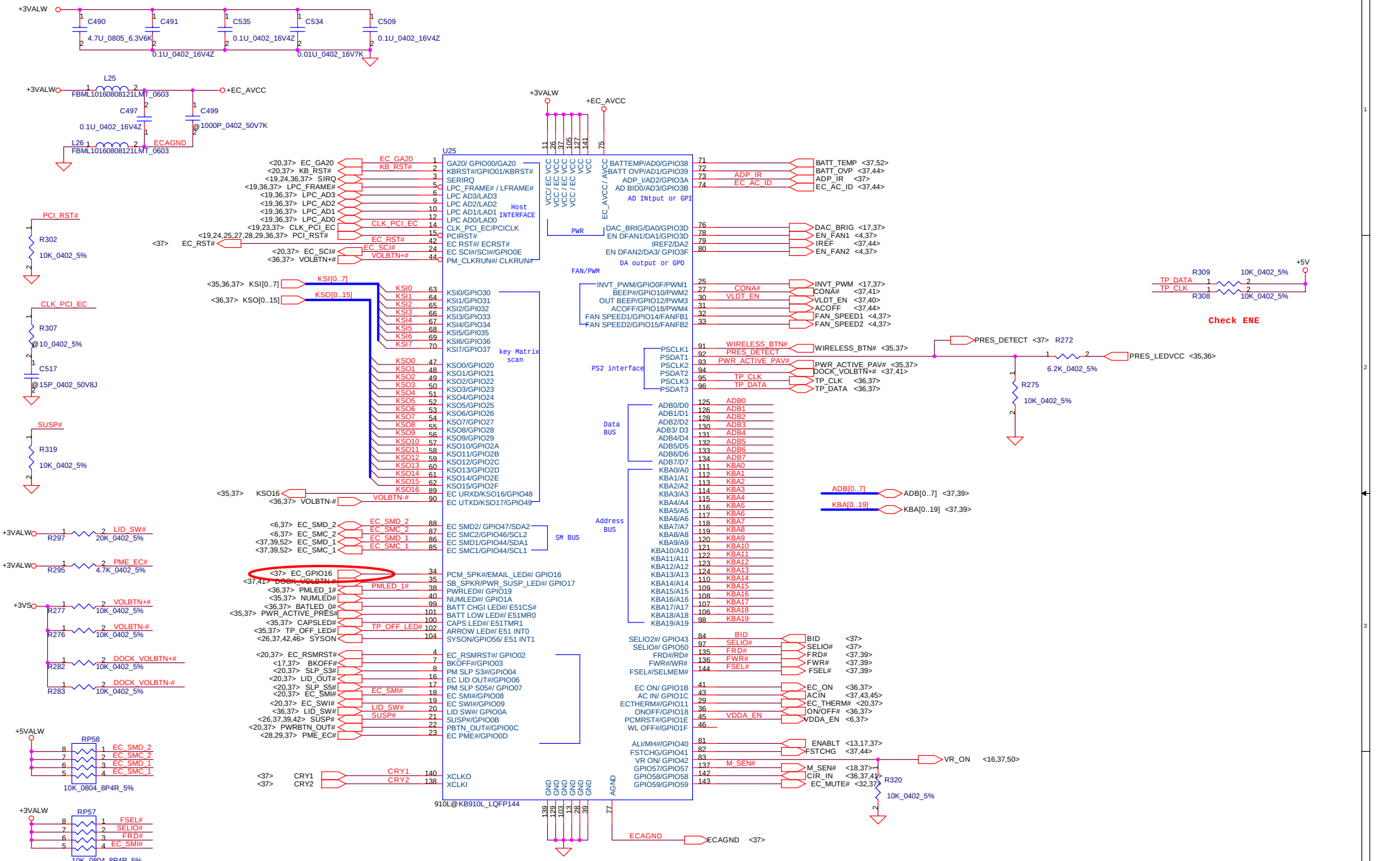
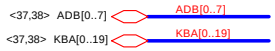
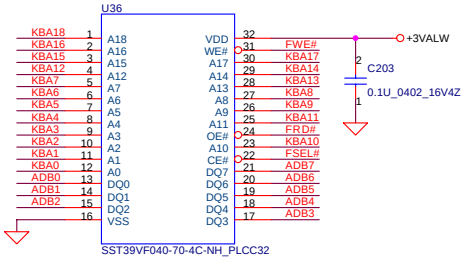
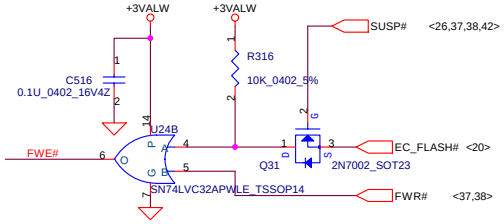


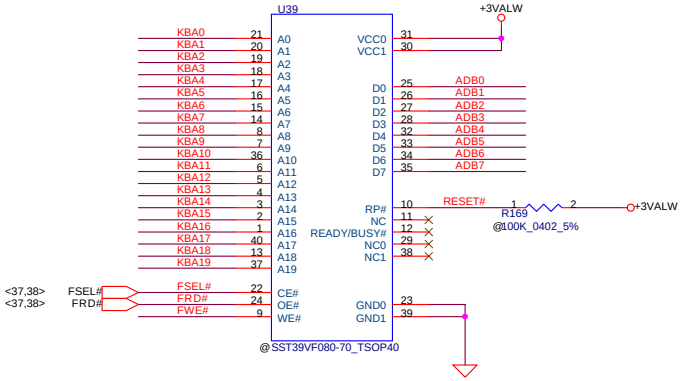
Compal Electronics, Inc.

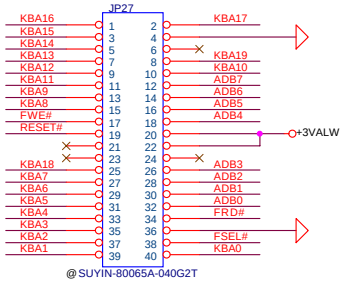
Title	KBD EC CTRL-KB910L	
Size	Document Number LA-2421	Rev 0.6
Date: Wednesday, January 05, 2005	Sheet 38 of 56	

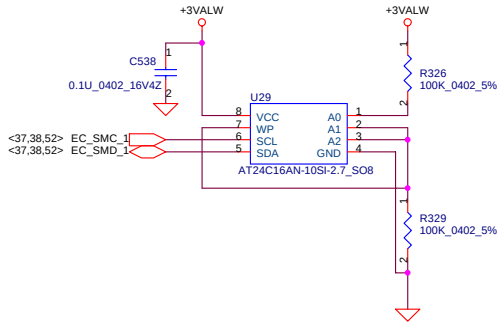










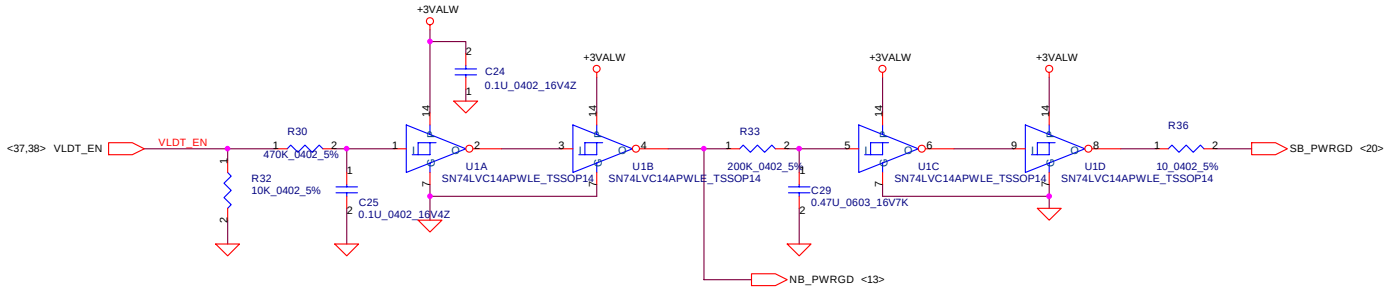


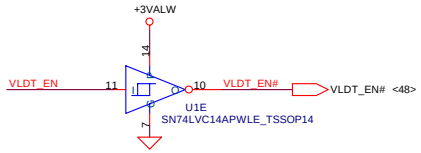
Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

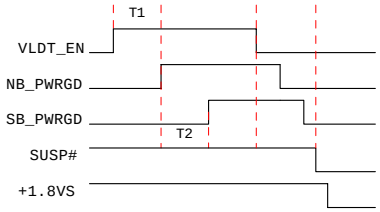
Size | Document Number: **LA-2421** | Rev: 0.6

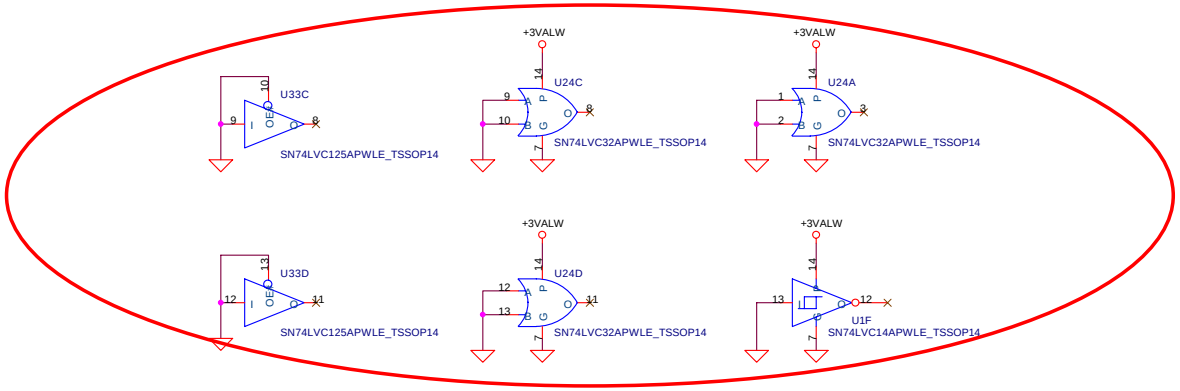
Date: Wednesday, January 05, 2005 | Sheet 39 of 56





note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,
SUSP# goes to low after SB_PWRGD goes to low for power
down.



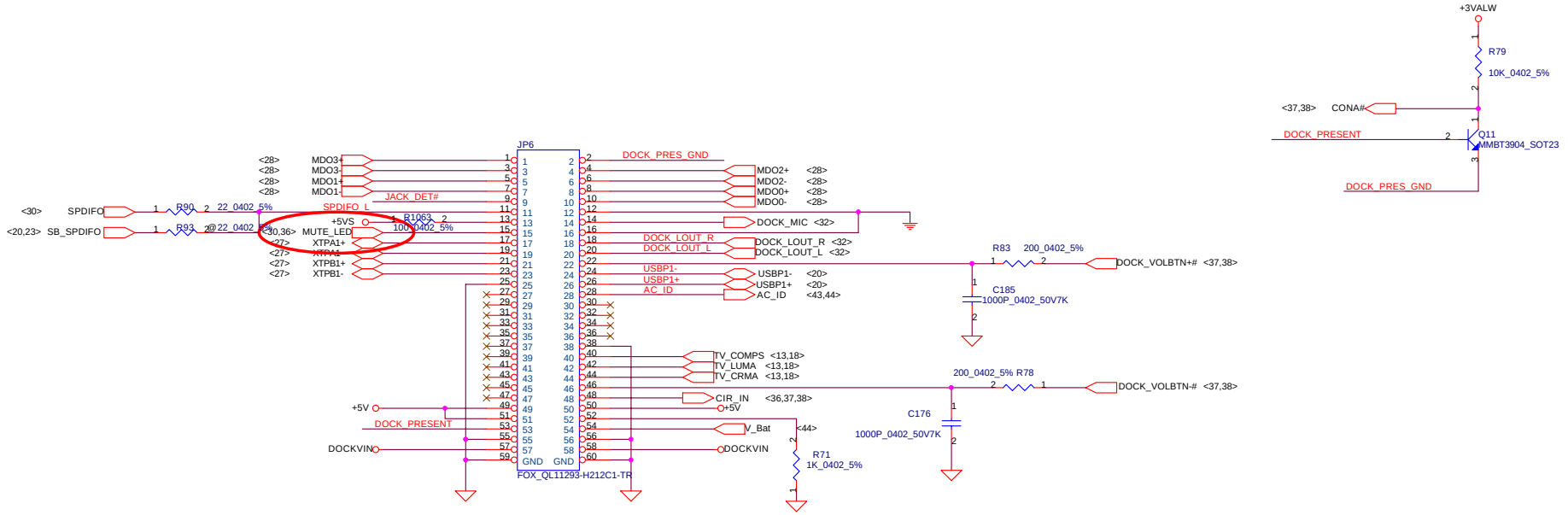


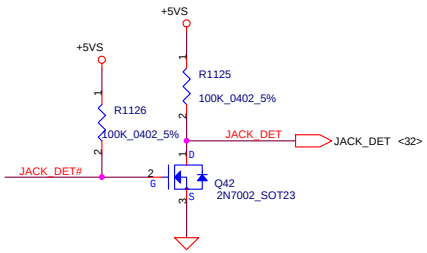
Compal Electronics, Inc.

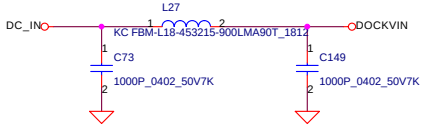
Title: **Power OK/Reset Conn.& MUTE Switch**

Size	Document Number	Rev
Custom	LA-2421	0.6

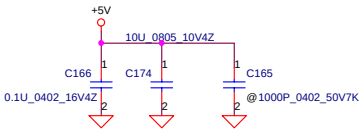
Date: Wednesday, January 05, 2005 Sheet 40 of 56







Note: PLACE CLOSE TO SPR PORT (JP33)

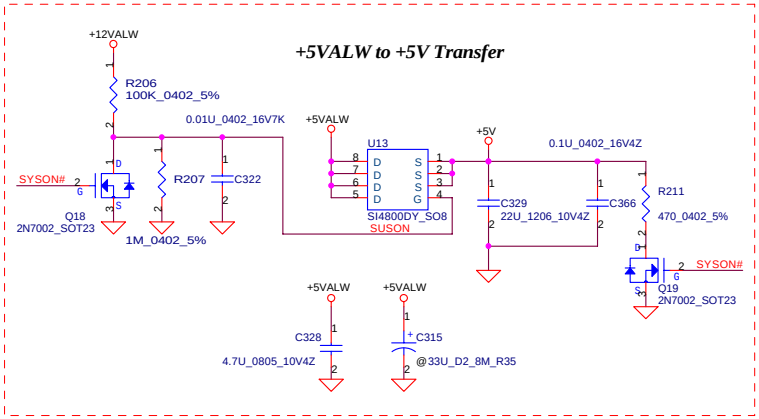


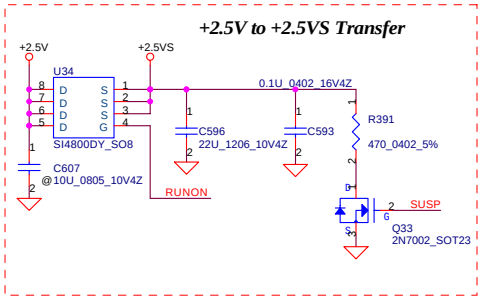
Compal Electronics, Inc.

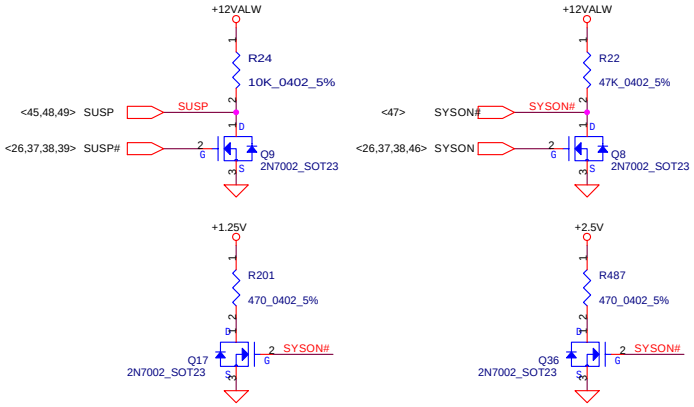
Title: **SPR Connector**

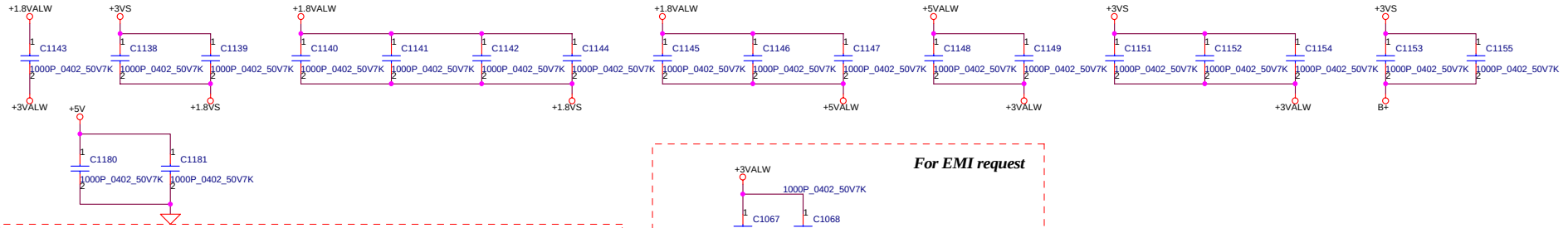
Size	Document Number	Rev
Custom	LA-2421	0.6

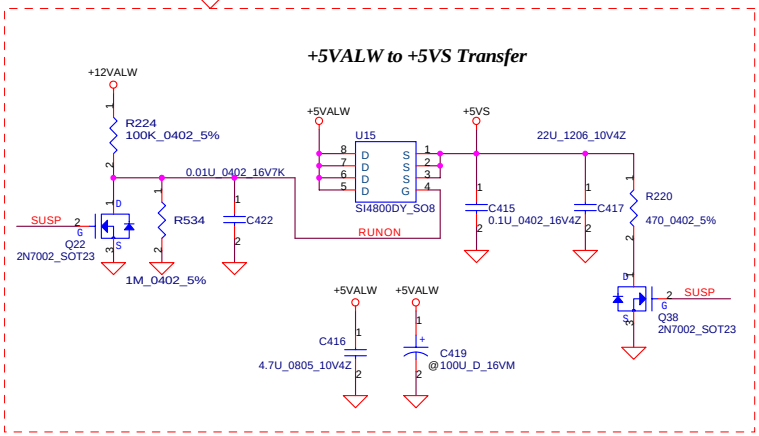
Date: Wednesday, January 05, 2005 Sheet 41 of 56

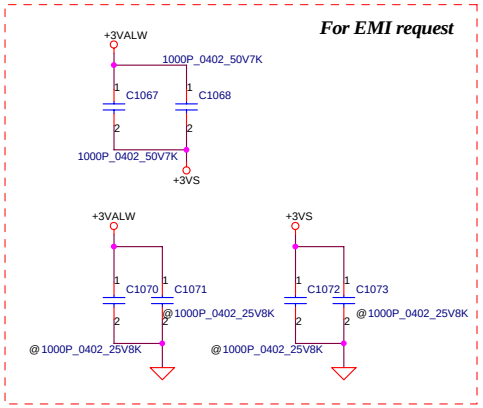


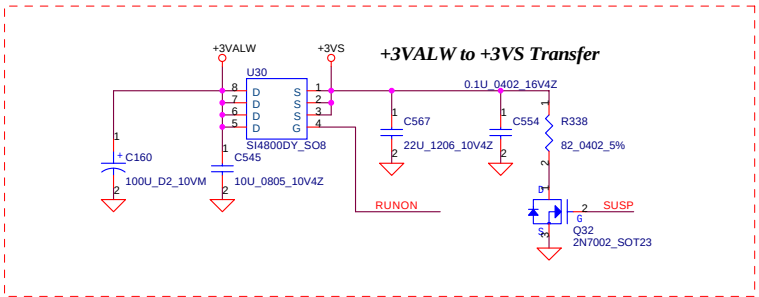


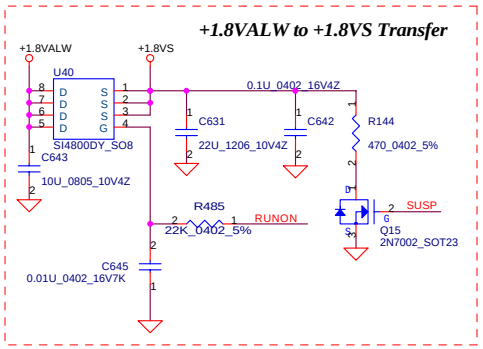


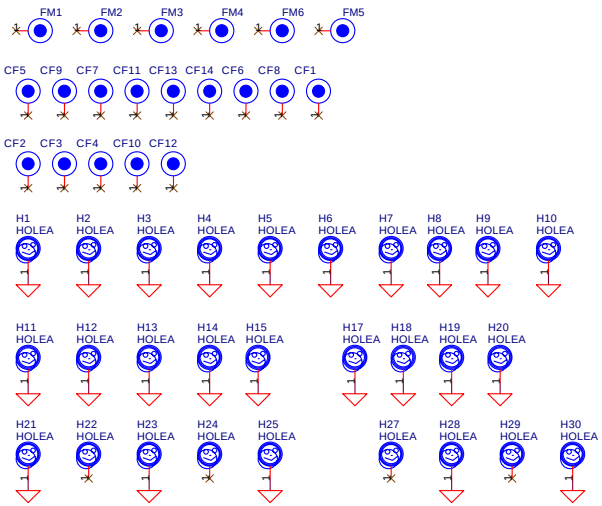












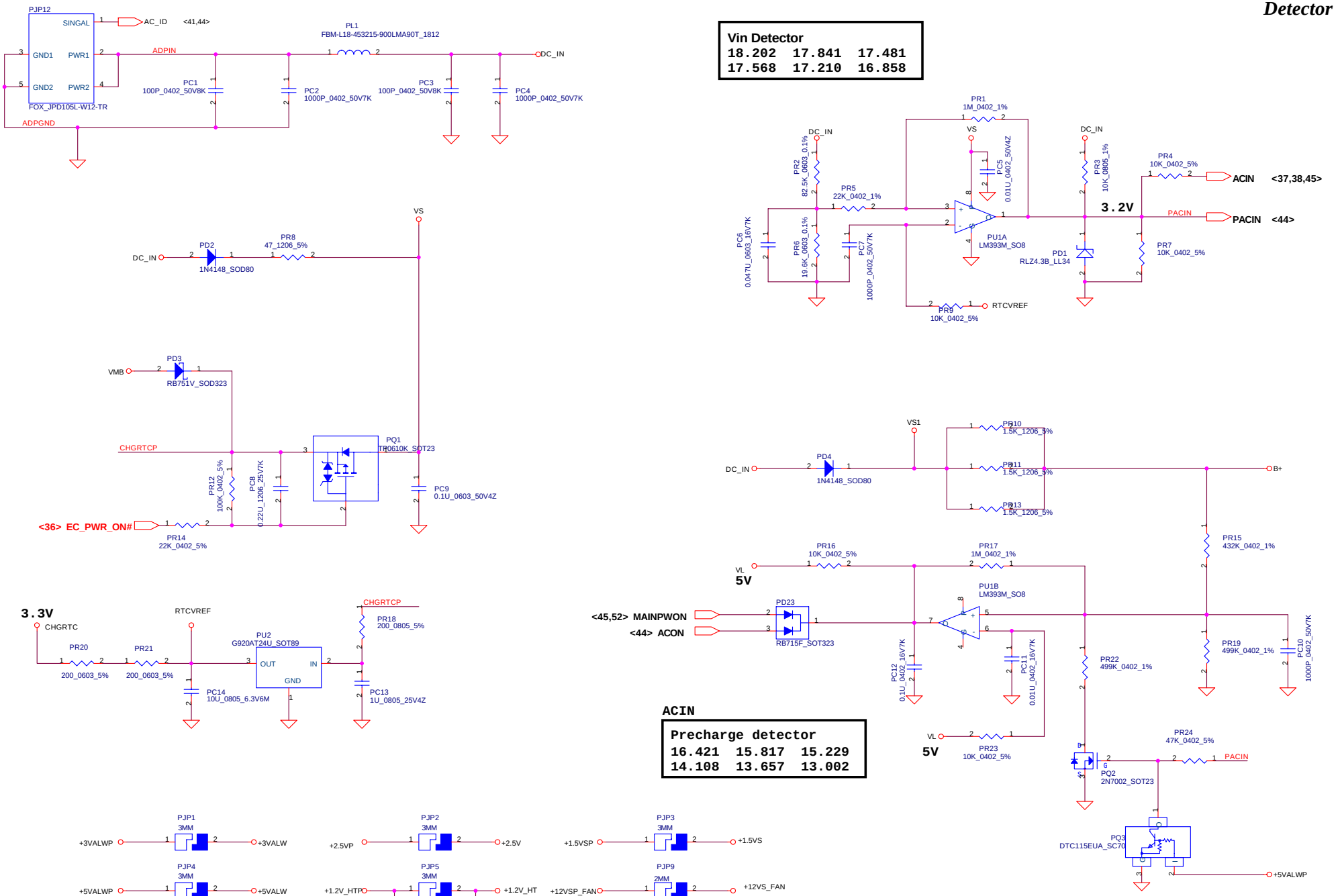
Compal Electronics, Inc.

Title: **DC/DC Circuit**

Size: Custom | Document Number: **LA-2421** | Rev: 0.6

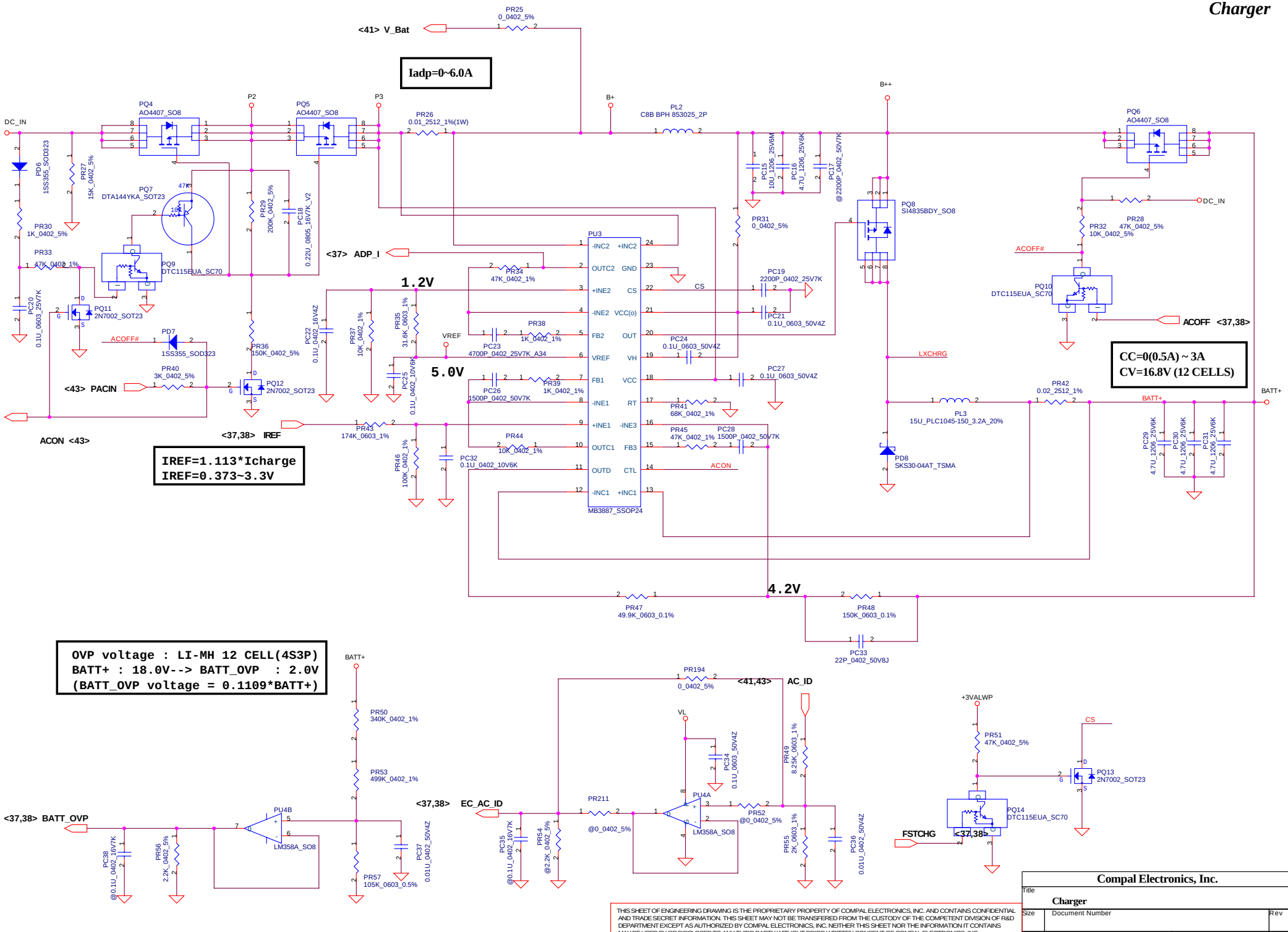
Date: Wednesday, January 05, 2005 | Sheet 42 of 56

Detector



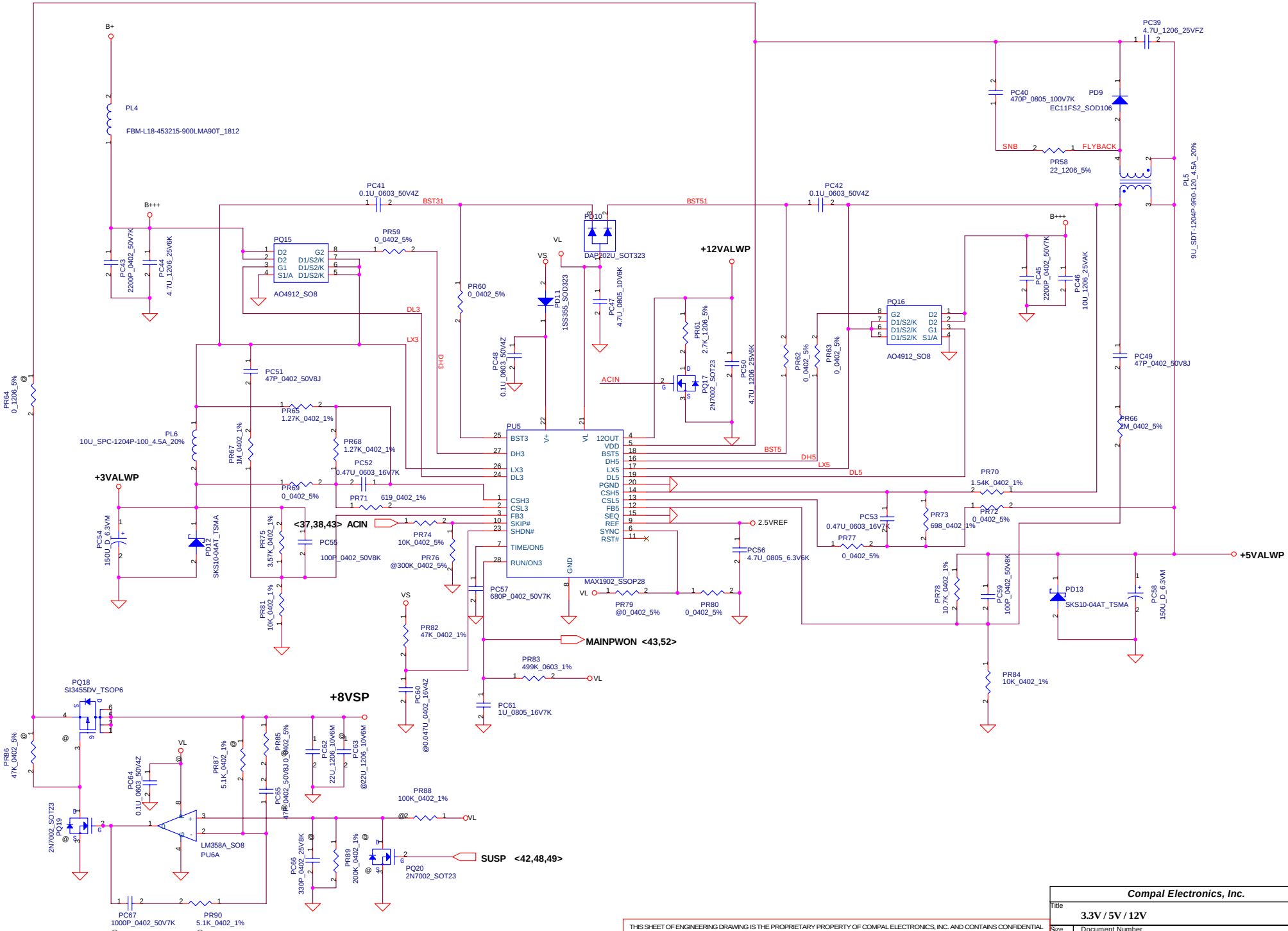
Compal Electronics, Inc.			
Title: Detector			
Size	Document Number		Rev
Date: Thursday, January 06, 2005	Sheet 43 of 55		

Charger

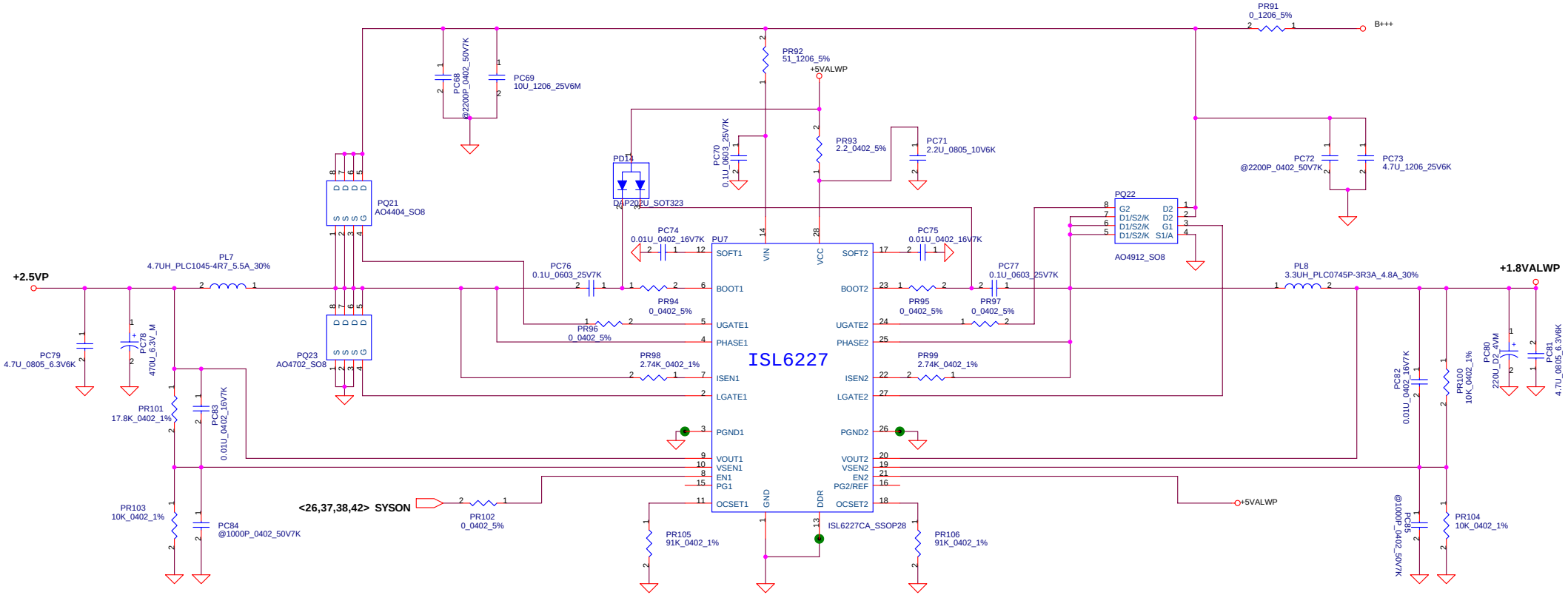


Compal Electronics, Inc.		
Title: Charger		
Size	Document Number	Rev
Date: Wednesday, January 05, 2005	Sheet 44 of 55	

+3.3V/+5V/+12V



Compal Electronics, Inc.	
Title	3.3V / 5V / 12V
Size	Document Number
Rev	1.0
Date:	Thursday, January 06, 2005
Sheet	45 of 55



Iimit=10.3/RILIM*(140+Rsense)/Rds(on)
Rsense=1K,RILM=51K,Rds(on) tpy.=19.7mΩ,Max=24mΩ.
Iimit Min=9.6/51K*(100+1K)/(24mΩ*1.3)=6.636A
Iimit Max=9.6/51K*(100+1K)/19.7mΩ=10.897A
+VCCP O.C.P. = 6.636A ~ 10.897A

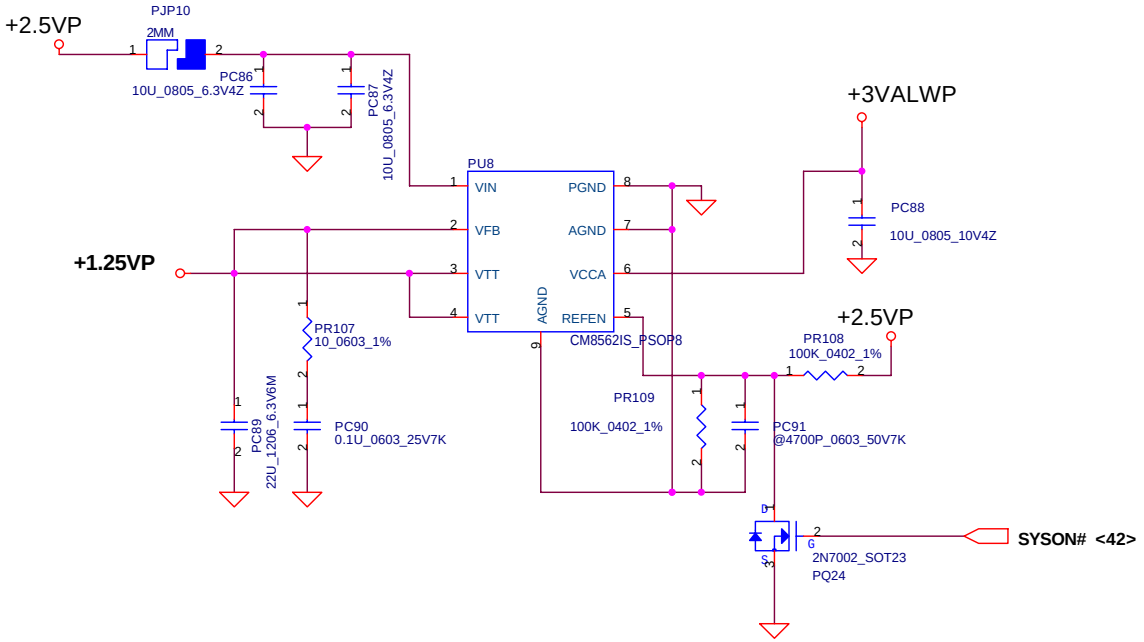
Iimit=9.6/RILIM*(100+Rsense)/Rds(on)
Rsense=2K,RILM=107K,Rds(on) tpy.=19.7mΩ,Max=24mΩ.
Iimit Min=9.6/107K*(100+2K)/(24mΩ*1.3)=6.0388A
Iimit Max=9.6/107K*(100+2K)/19.7mΩ=9.564A
+VCCP O.C.P. = 6.038A ~ 9.564A

COMPAL ELECTRONICS, INC

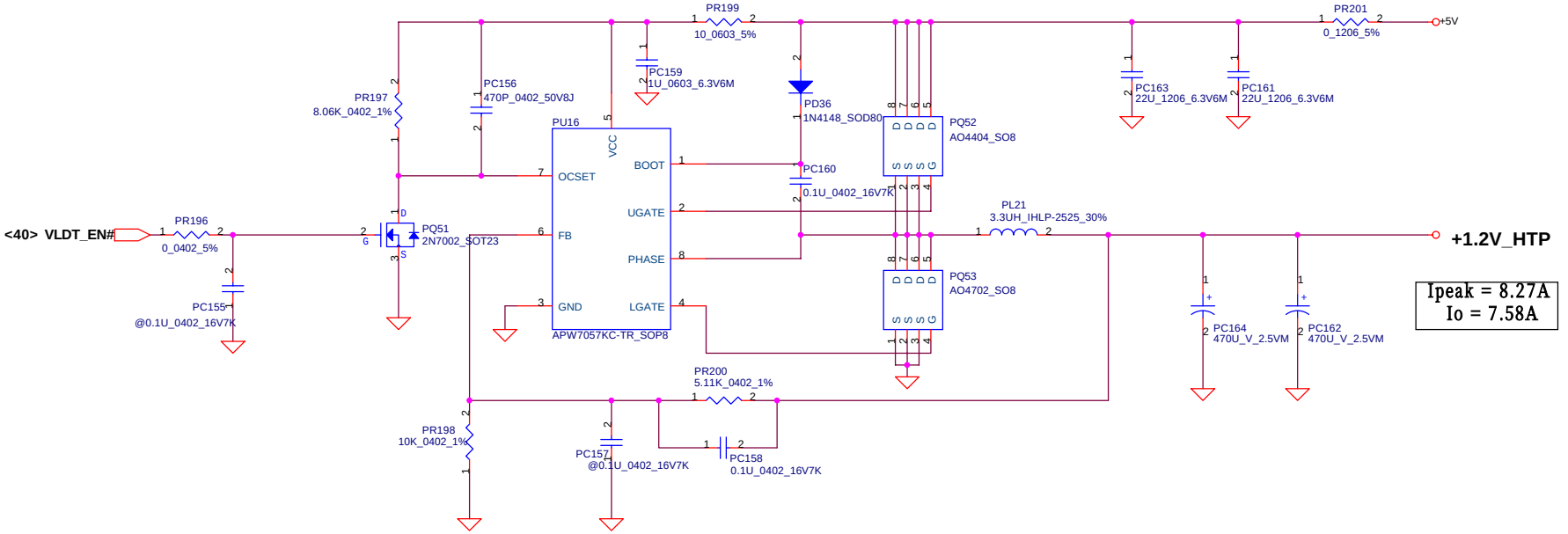
Title: DDR POWER 2.5VP & +1.8VALWP

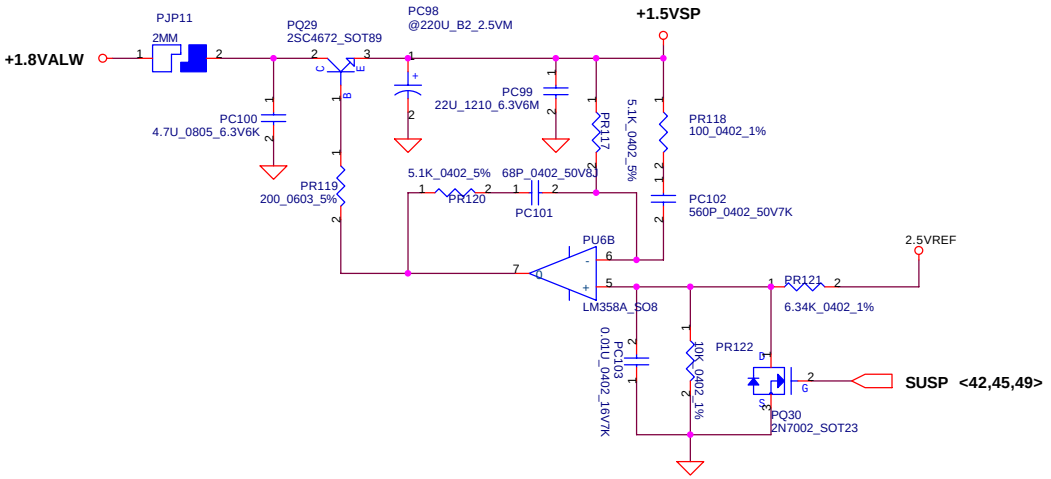
Size: B | Document Number | Rev: 0.1

Date: Wednesday, January 05, 2005 | Sheet 46 of 55



COMPAL ELECTRONICS, INC	
Title	+1.25VP
Size	Document Number / Rev
Date: Wednesday, January 05, 2005	Sheet 47 of 55



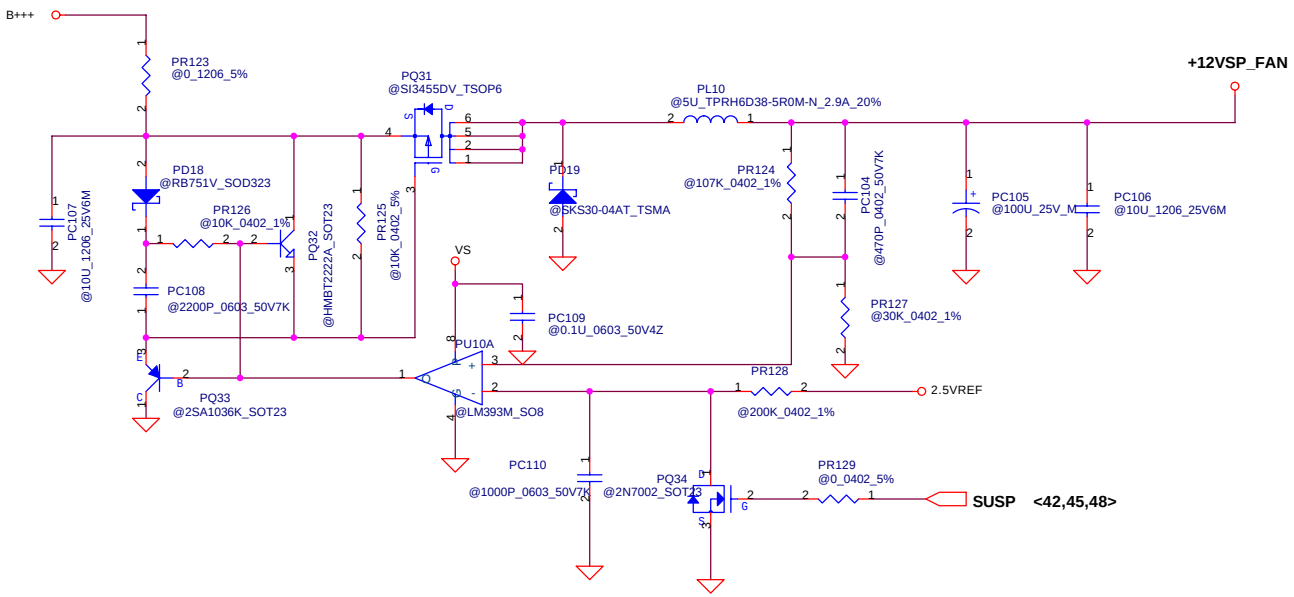


COMPAL ELECTRONICS, INC

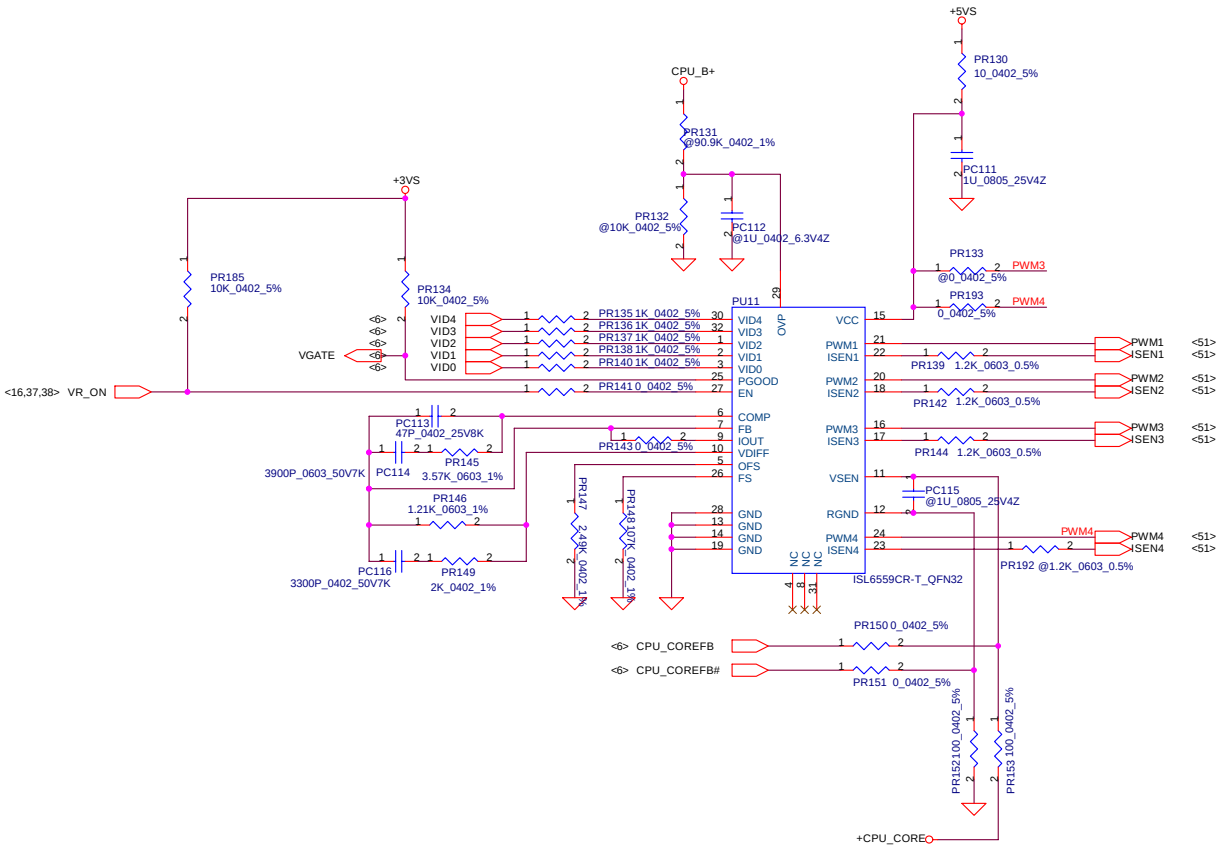
Title: 1.2V_HTP / +1.5VSP

Size | Document Number | Rev

Date: Wednesday, January 05, 2005 | Sheet 48 of 55



COMPAL ELECTRONICS, INC	
Title	FAN 12V
Size	Document Number / Rev
Date:	Wednesday, January 05, 2005
Sheet	49 of 55

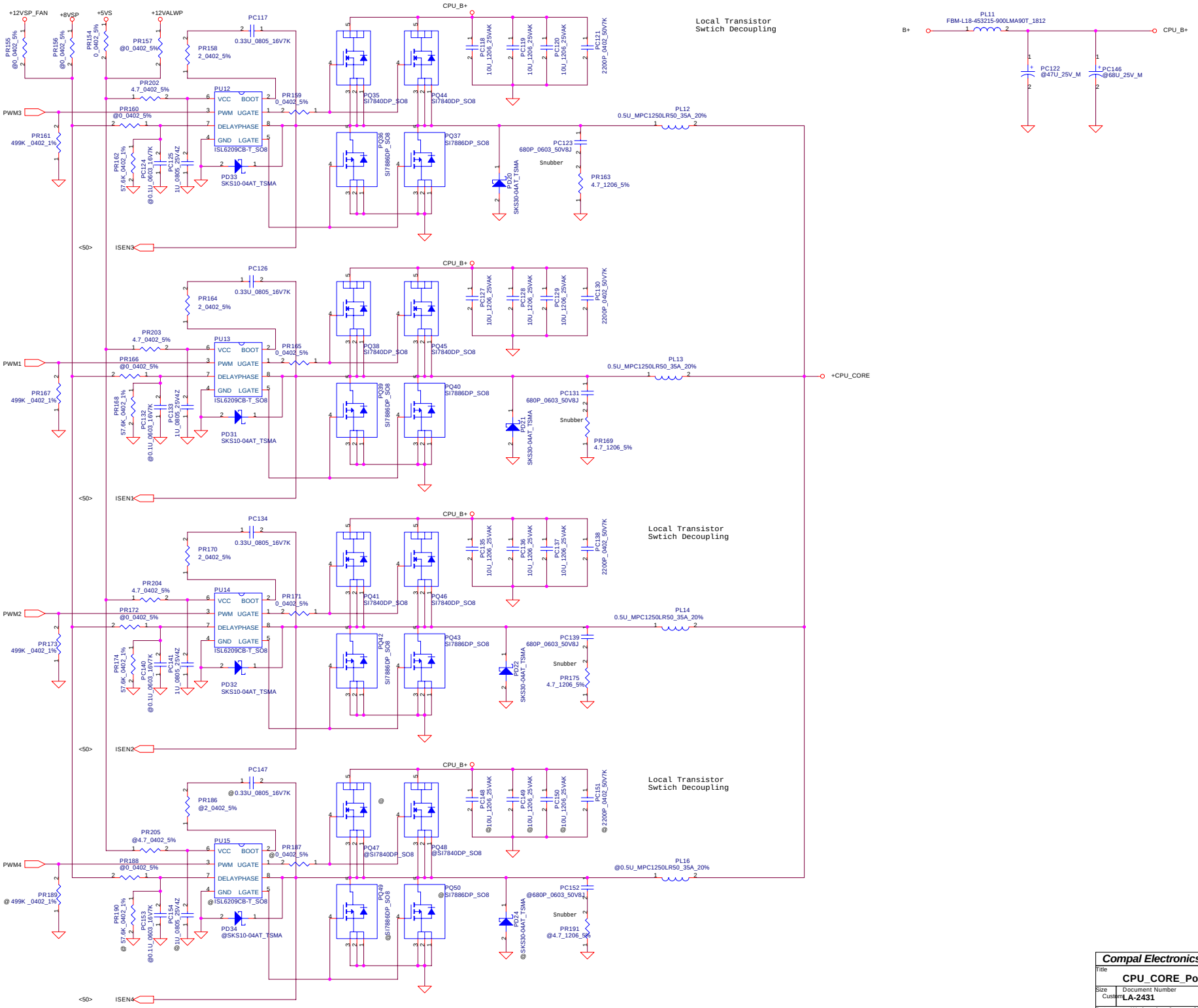


COMPAL ELECTRONICS, INC

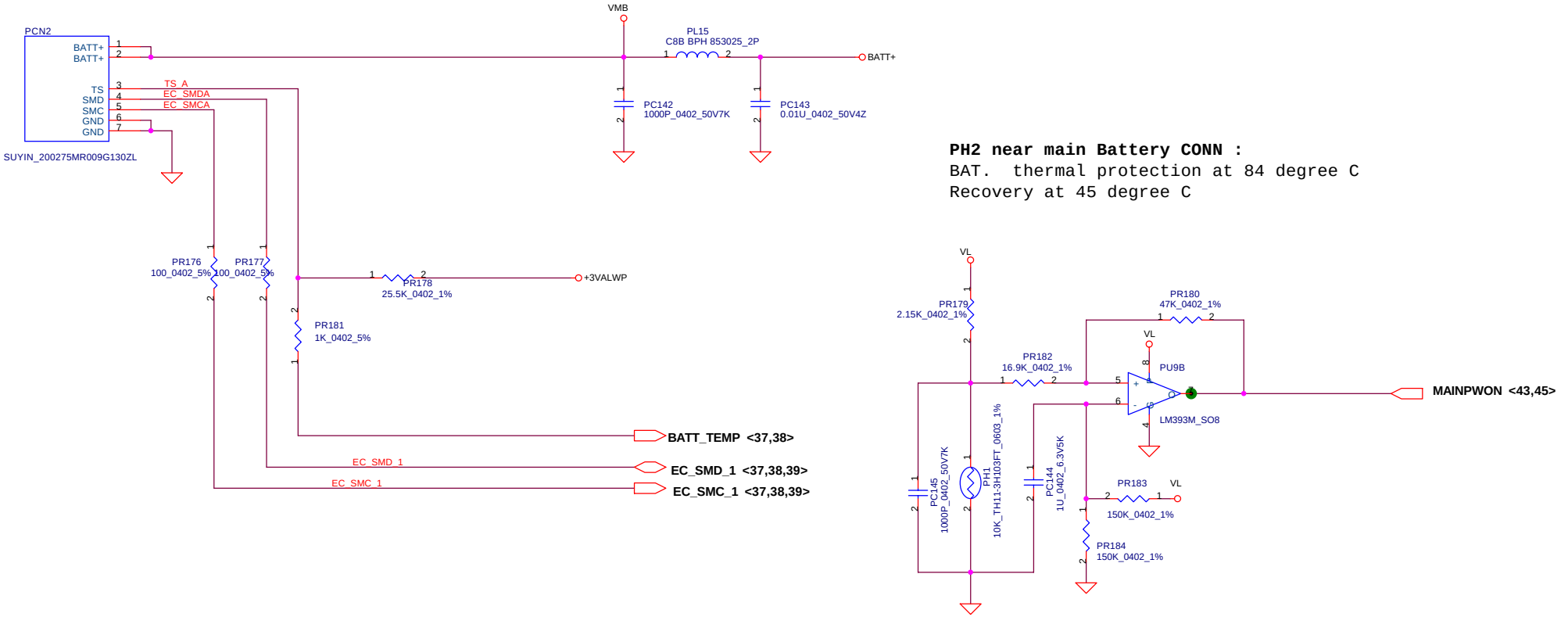
Title: **+CPU_CORE**

Size	Document Number	Rev
B		1.0

Date: Wednesday, January 05, 2005 | Sheet 50 of 55



Compal Electronics, Inc.			
Title: CPU_CORE_Power-Stage			
Size: Custom	Document Number: LA-2431		Rev: 0.1
Date: Wednesday, January 05, 2005	Sheet 51 of 55		



PH2 near main Battery CONN :
BAT. thermal protection at 84 degree C
Recovery at 45 degree C

	COMPAL ELECTRONICS, INC
Title	**BATTERY CONN / OTP**
Size	Document Number / Rev
Date: Wednesday, January 05, 2005	Sheet 52 of 55

POWER PIR LIST

PIR LIST

Pre-DB

2004/6/05

1.page16 add R541/R542/R543/R544 and net NBSRCCLK_R/ NBSRCCLK/ NBSRCCLK#_R/ NBSRCCLK#.
2.page13 add net NBSRCCLK/NBSRCCLK#.
3.page13 change R85 pin2 from +2.5VS to +2.5V.
4.page14 add D33.
5.page19 del D18 and remove C265 to U38 pinA2.

2004/6/08

1.page13 del R82 change net name from SUS_STAT# to NB_SUSSTAT#.

2004/6/19

1.page19 Change U32,C584,R389 to @.
2.page23 Change R460 to @ and Add R464.

2004/6/25

1.page40 Change R30 from 10K_0402 to 340K_0402_1%.
2.Page4/6 change C18, C28 to SF10001M100 ELE CAP 100U 6.3V M B (6.3X6.0) CV-AX.
3.Page19 Add JP37, del BATT1

2004/6/28

1.Page26 Change U2 from R5535 to TPS2231.
2.Page26 Change C485/C487 to 4.8U_0805,change C486 to 10U_0805.
3.Page26 Change C503/C494 to 10U_0805,C492 to 4.7U_0805.
4.Page26 Del R268,Add Q40 2N7002.

Update for DB2

1.page34 change IDE Resistor from 0402 to 8P4R.
4.page27 change DOCK@ to 1394@.
5.ME update connector check and sub-board connector change to hot bar.
6.change 470U placement for +1.25V.
7.page40 change R33 from 0603 to 0402 type and R30 to 470k_0402_5%.
8. change C18, C28 to SF10001M100 ELE CAP 100U 6.3V M B (6.3X6.0) CV-AX.
9. change C318 to bottom side SF33001M100 ELE CAP 330U 6.3V M B (6.3X7.7) CV-AX
10. change C411 to bottom side SF47001M000 ELE CAP 470U 6.3V M B (10X10.5) CV-EX
11. change C325 to SGA19471D20.
13. change BATT1 to SP07S00080L(socket) + GC20323MX00(battery) (Page 19)
14. change new card power switch from RICOH to TI.
15. Remove PME_EC# from SB and pin C4 wire to EC_SWI#
16. Disconnect UTXD from U26.154
17. Page 23 update hardware strap for SB400 A21 (PA_IXP400AD1 & 105-A27800-00C R1.1)
18. Page 13 add EEPROM for NB to solve boot up intermittently
19. Page 23 strap select 14 MHz OSC mode, it is generated from NB to SB and delete 14 MHz crystal at SB
20. 1394 controller change to TI
21. Update PIRQ routing
22. X2 change size.
23. Cardbus controller change to TI
24. Fan circuit change to MOS
25. Change AMP to TPA0312 and add TC7SH32FU to solve HP_PLUG issue
26. Implement HP wireless/bluetooth control requirement. Change host to SB. (Page 20)
27. Change CRT connector JP19 (Page18)
28. Modify KB910L debug pin RXD=pin#35 & TXD=pin#34
29. No need PWR_BACK# from EC controller
30. DFX review: Change blue LED footprint to be same as amber LED footprint.
31. AC97 primary codec SDATA_IN0 should connect to SB's AC97_SDIN0 (Page 30)
32. R182 change to 11.8 k (Page 20)
33. Reserve D36, D37, and R1127 for XD detect issue. (Page24)
34. PCIE_PME# change to pin #D2 of SB. (Page 20)
35. WL_ON connect to pin #C5 of SB/ BT_ON# connect to pin #B5/ BT_DET# connect to pin #C8. (Page 20)
36. Add R1132 to ensure ENABLT is low during power up.(Page 13)
37. AGP_BUSY# and AGP_STP# pull up to solve shut down issue. (Page 20)
38. Delete R159 (OVCUR#3) and LID_OUT# change to GPM3# and add R1133 pull up S3_STATE to +3VALW (Page20)
39. Change all blue LED's footprint to LED_17-21UYOC-S530-A2-TR8_2P
40. Change R532 to 0603 size and add R1134 (Page 30)
41. Add AC-caps for PCI and LPC bus turn path. (Page 42)
42. Delete R541, R542, R543 and R544. (Page 16)

Update for SI

1. Applying CLK_STOP of ICS951418. (Page 16)
2. R176 change to 4.12k 1% (page 19)
3. Add pull down resistor for SYSON (R1135) and SUSP# (R319), due to TPS2231 internal pull-up when +3VALW present, EC can not control at the first 10 ms.
4. Reverse JP33 and JP34
5. TI CardReader workaround: add Q44, R1137, D38, and D39 to prevent signal output earlier than power up (page 24)
7. MU902's pin29 connect to AGND_LSD (page 31)
9. Change C621, C619, C628, and C625 to 0.01U from 0.1U (page 19)
10. DDR change to single channel from dual channel.
11. Swap pin40 and 44 of docking connector (JP6) for TV-out signal. (page 41)
12. Update from ATi AP note of SB, unsed SATA pins connect to GND. (page21).
13. Reserve R1138 for XD_WP# pin at socket side. (page 24)
14. Reserve U47 to generate independent +1.9VS to PCIE_PVDD and PCIE_VDDR. (page 19)
15. For KB910L, pin #94 is for DOCK_VOLBTN+# and pin #34 is for EC_GPIO16. (page 38)
16. Add R1141 on SUS_STAT# per ATI recommend. (page 13)
17. PR110 connect to +5V due to +3VS too dirty that will cause TV display garbage. (page 48)
18. Update PCIE connector (JP5) pin defined of #7, #8, and #9 and reserve backward compatible due to there are two different version of NewCard spec. (page 26)
19. GPP_RX0N/P connect to JP5.21/22 and PCIE_TX0N/P connect to JP5.24/25 (page 26)
20. Reserve D40 and D41 for NewCard hot-plug detected. (page 26)
21. Adjust AMP output to 10 dB: Add R237/R233, delete R236/R234. (page 32)
22. Change CP1 ~ CP6 to C1156 ~ C1179 due to cost saving. (page 36)
23. Add C1180 and C1181 for EMI requirement. (page 42)
24. Add C160 due to +3VS unstable. (page 42)
25. R1121 change to 0_0402_5% per TI recommend (page 24)

Update for SI-R (Rev 0.4)

1. DDR_SDM_L2 length mismatch (page 9)
2. Add U48 (TPS2211A) for PCI1510RGVF (page 25)
3. NC_CP# connects to U38.D3 for New Card hot-plug (page 20)
4. R51 and R77 change from 49.9_0402_1% to 61.9_0402_1% (page 11)
5. Change C621, C619, C628, and C625 to 0.1U from 0.01U --- ATI final decision for SB A22 RPO3 and future (page 19)
6. Q25 change from MMBT3906 to PDTA114EK and R228 change to 0_0402_5% due to Hitach HDD LED will not be turn off light. (page 36)

Update for SI-2 (Rev 0.4B)

1. Remove C27 due to Sempron CPU intermittent boot-up issue. (page 6)
2. Change Q39 to MMBT3904 due to CARD_LED is high active signal. (page 35)
3. D40 and D41 replace by R1146 and R1148 due to TPS2231 truth table treat both CPUUSB# andCPPE# as the same. (page 26)
4. R87 change to 8.06k_1% due to New Card eye-diagram issue. (page 12)

Update for PV (Rev 0.5)

1. Add R1149 and R1150 for headphone gain degrading. (page 32)
2. Modify AVDDTX and AVDDRX layout to improve USB signal quality.
3. Change wireless LED power from +5V to +5VS (page 35)
4. Follow TI layout guideline.
5. Change R1099 and R1100 to 2.2k per TI recommend for XD certification. (page 24)
6. Change LAN LED indicator color, Green is for link and Amber is for activity. (page 28)
7. Change R34, R35 and R259 from 1k to 680 base on AMD design guide. (page 6)
8. Change R286, R290, R473, and R486 from 100 to 15 base on AMD recommendation. (page 5/ 9)
9. Reserve C1182 at NB VDD_CORE and change C161 ~ C164, C136 ~C138, C153, C154, C156, C157 from 0.1uF to 1uF due to +1.2V_HT is not stable and clean. (page 14)
10. Delete R1083 due to SM card detect issue (quick or slow). (page 24)
11. Add C1183 ~ C1220, 1000pF or 220pF, on +2.5V, +1.25V, +CPU_CORE, +3V_CLK, +3VS, and +1.2V_HT for EMI require. (page 7/ 10/ 14/ 16/ 22)
12. Change R155, R162, R441, R444, and R448 from 22 ohm to 33 ohm due to EMI require. (page 19)
13. Wire MUTE_LED to JP6.15 due to HP docking spec V0.8 update (page 41)
14. Add C1151 and C1152 to isolate GND and change C61 and C241 from 0.1uF to 1000pF for EMI. (page 4)
15. Add C1221 ~ C1226 on +2.5VS for EMI (page 15)
16. Reserve C1227 and C1228 on EDID_CLK/DAT for EMI. (page 17)
17. Remove R64, R65, R69, and R70 due to EMI. (page 5)
18. RTC battery change to CR2025 (165mAh) due to power consumption less than 5uA. (page 19)

Title	<Title>	
Size: Custom	Document Number: LA-2421	Rev: 0.6
Date: Thursday, January 06, 2005	Sheet 55 of 56	

Update for PV-2 (Rev 0.6)

1. Delect R1138, wire WP# pins of XD and SM together (SM_EL_WP#) and series 3.3k ohm (R1082) to CLK per HP recommendation. (page 24)
2. Tie un-used inputs of U24 and U33 to GND. (page 40)
3. Delect all reserve 0 ohm resistors. (page 34)
4. Add C1229 for power (+CODEC_REF) stable on MIC_IN. (page 30)
5. R53 change to 91_0402_5% due to HT output from RS480 need to improve rising and falling time. (page 11)
6. Reserve R1153 ~ R1157 for SanDisk 256MB SD card overshoot and undershoot issue. (page 24)
7. De-feature mother board populate R274, and full-feature mother board populate R269 for 90W adapter protection. (page 37)

Title <Title>		
Size Custom	Document Number <Doc>	Rev 0.6
Date: Wednesday, January 05, 2005	Sheet 56 of 56	