

Compal confidential

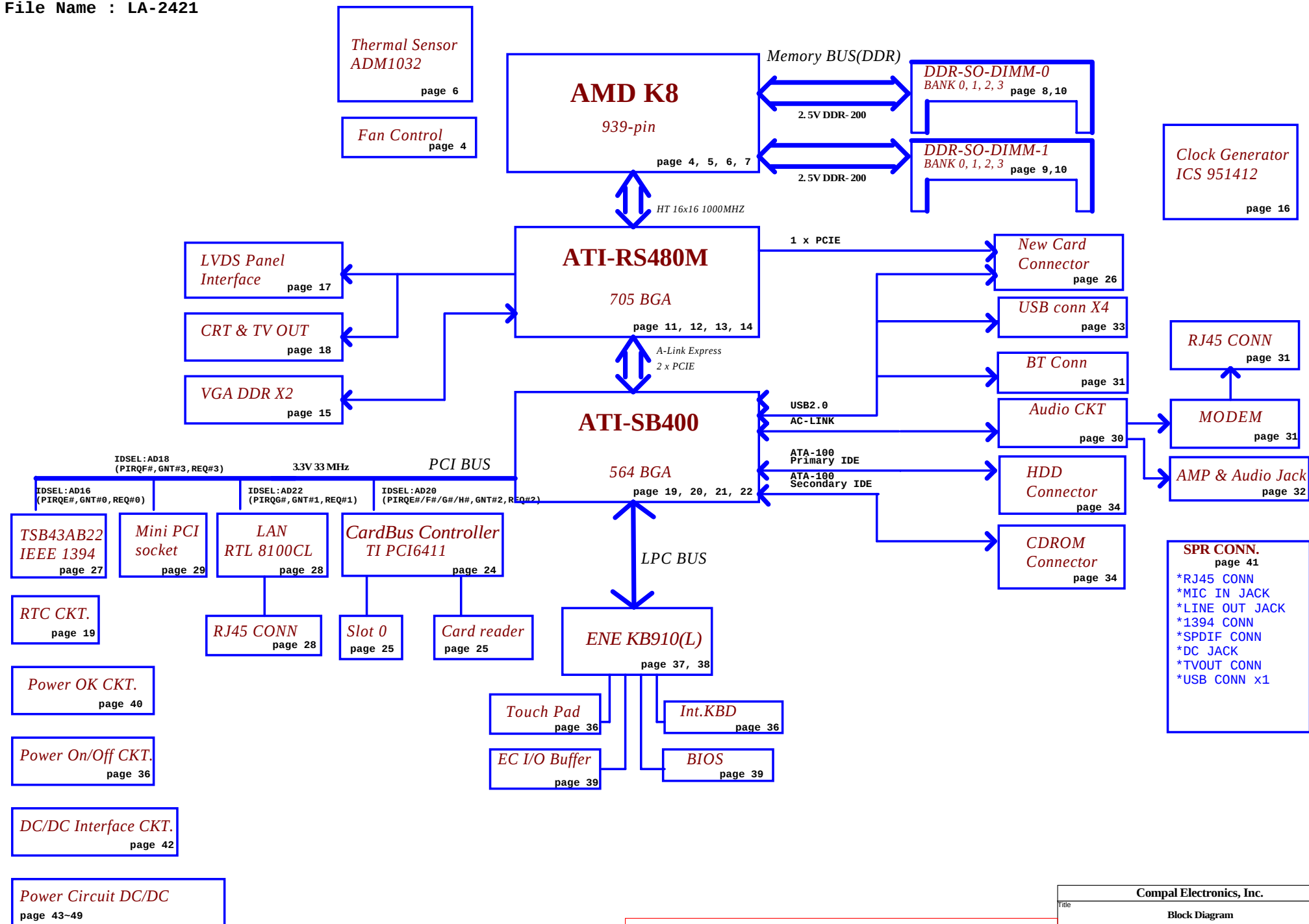
Schematics Document

AMD K8 with
ATI RS480M+ATI SB400

2005-01-04
REV:0.6

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Voltage Rails

power plane \ State	+12VALW +5VALW +3VALW +1.8VALW	+5V +2.5V +1.25V	+5VS +3VS +2.5VS +1.8VS +1.5VS +2.5VDDA +CPU_CORE +1.2V_HT
S0	0	0	0
S1	0	0	0
S3	0	0	X
S5 S4/AC	0	X	X
S5 S4/AC don't exist	X	X	X

0 MEANS ON
X MEANS OFF

PCI Devices

INTERNAL DEVICE	IDSEL #	REQ/GNT #	PIRQ
SMBUS			
IDE			A
LPC I/F			
PCI to PCI			
AC97 AUDIO			B
AC97 MODEM			B
OHCI#1 USB			D
OHCI#1 USB			D
EHCI USB			D
SATA#1			A
SATA#2			A

EXTERNAL			
1394	AD16	0	E
Wireless LAN	AD18	3	F
LAN	AD22	1	G
CARD BUS	AD20	2	E,F,G,H
Mini-PCI (no use)	AD19	4	F

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Title			
Notes List			
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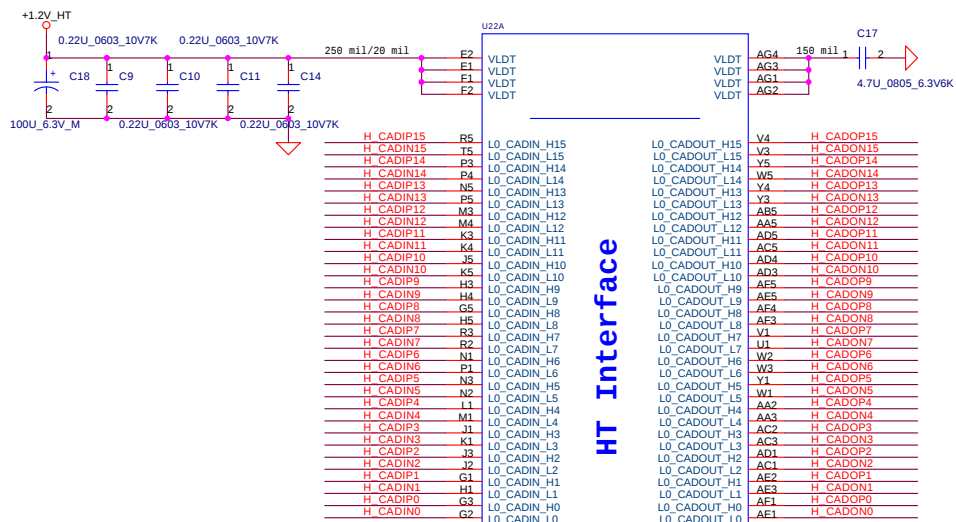
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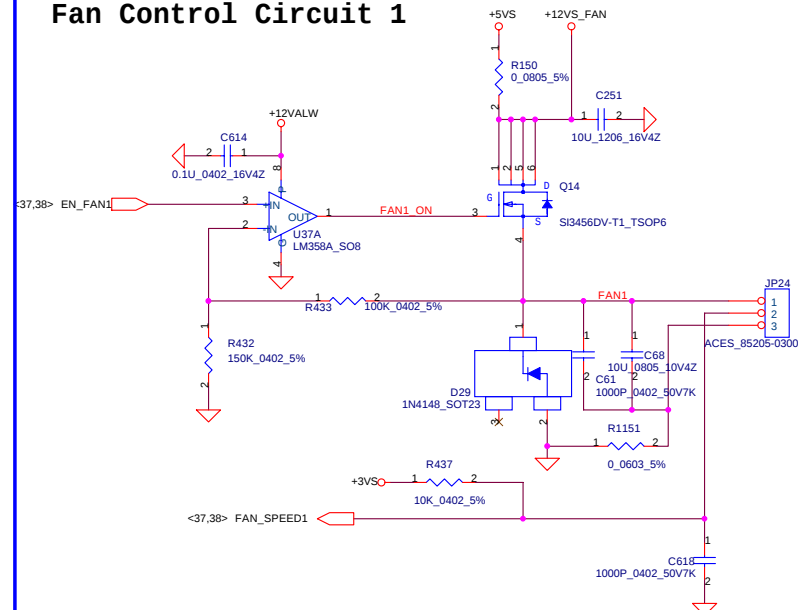
LA-2421 REV 0

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 <11> H_CADIN[0..15] → H_CADIN[0..15]

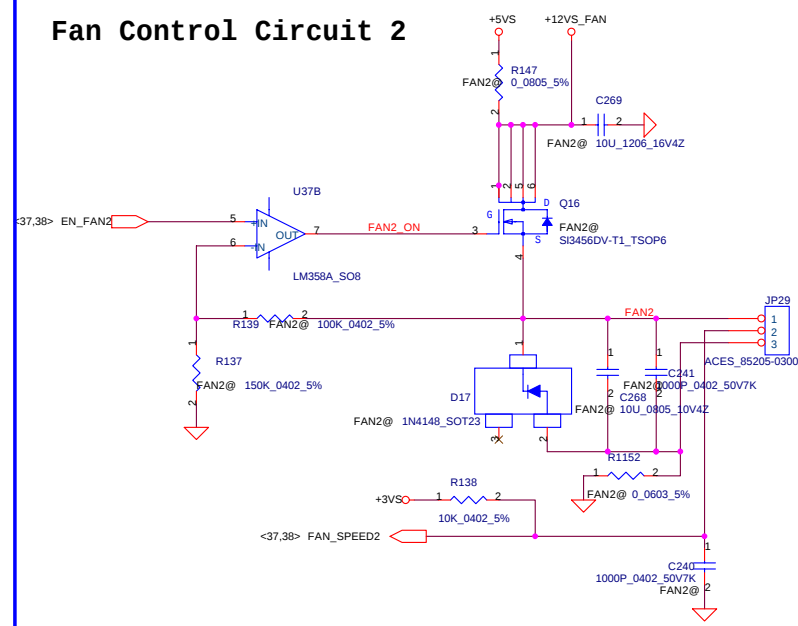
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 H_CADON[0..15] → H_CADON[0..15] <11>



Fan Control Circuit 1



Fan Control Circuit 2



Compal Electronics, Inc.

Title

Claw Hammer CPU (Host Bus)

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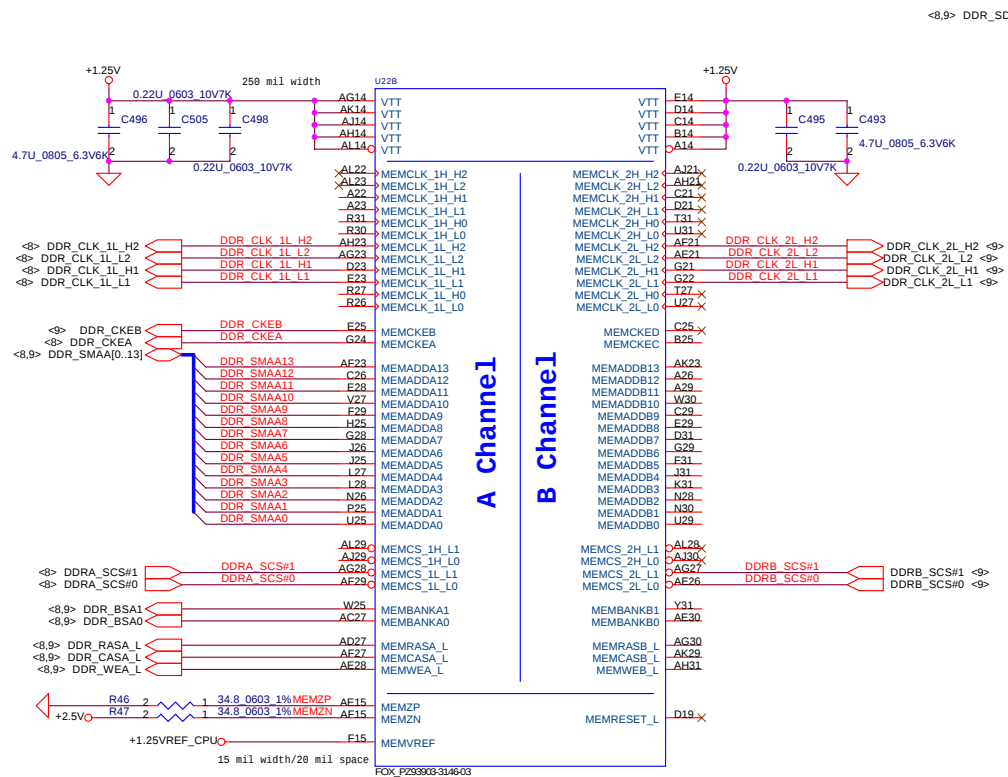
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56

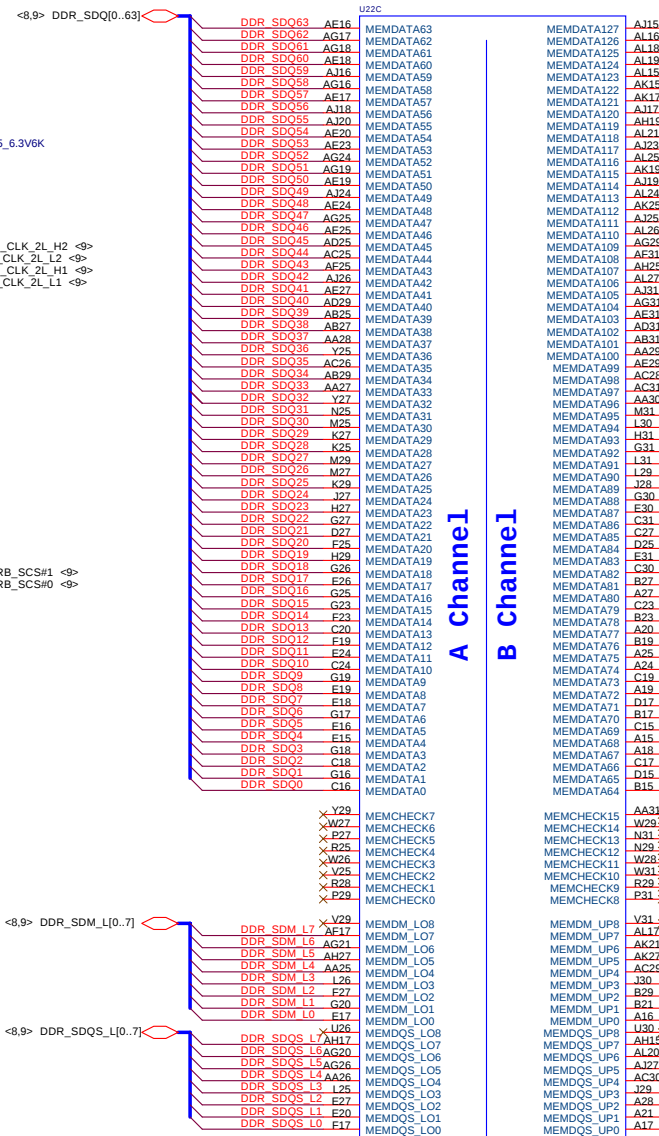
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0.6

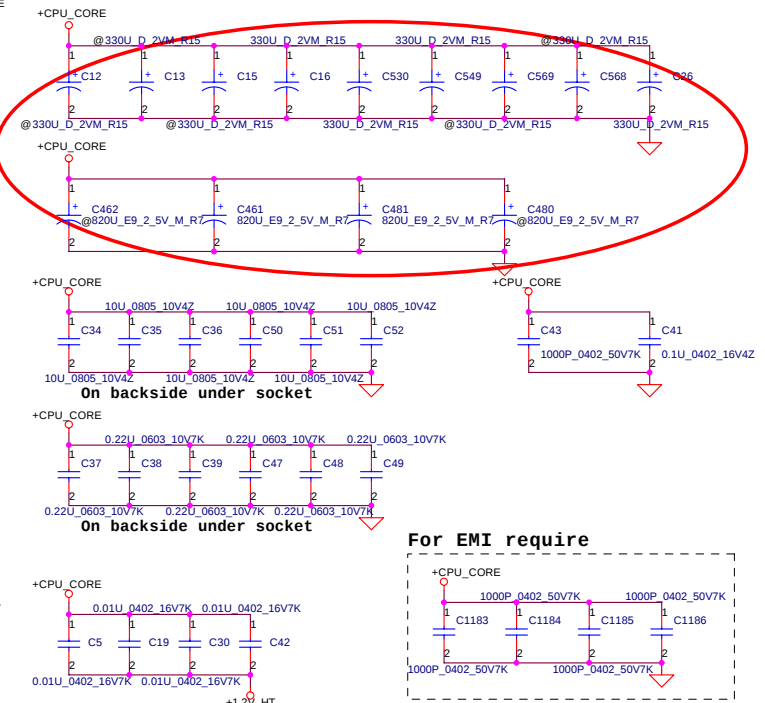
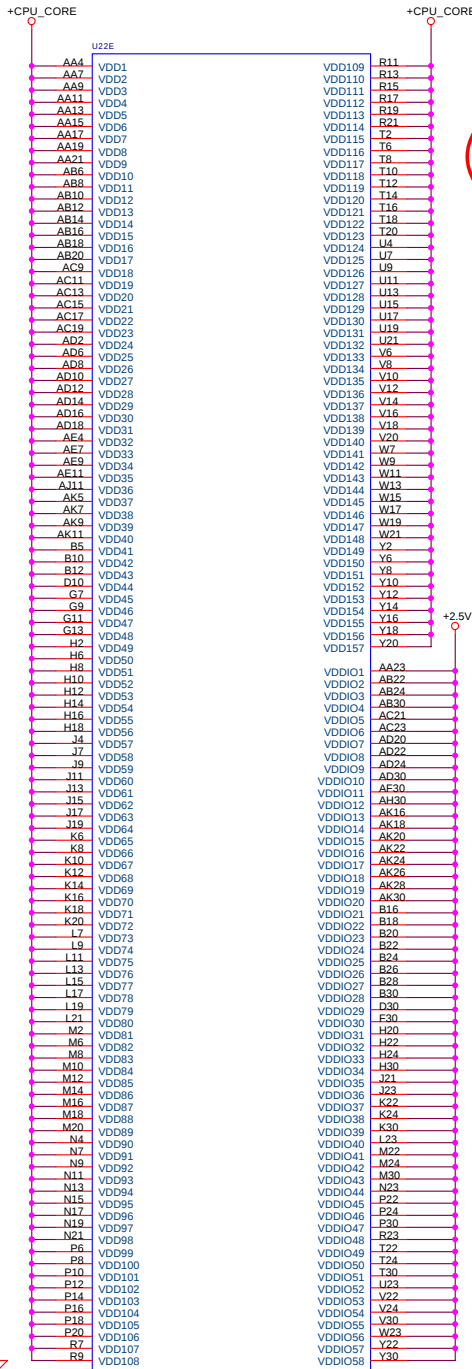
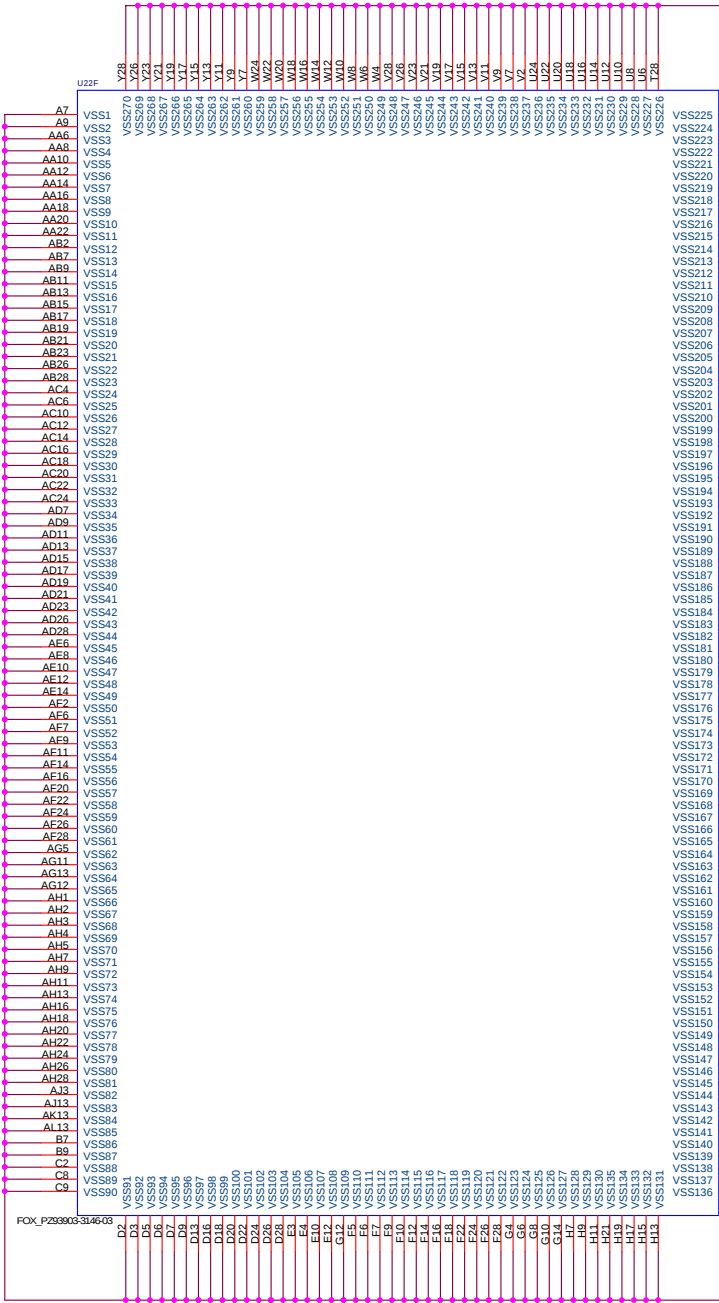
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FOX_P293903-314603

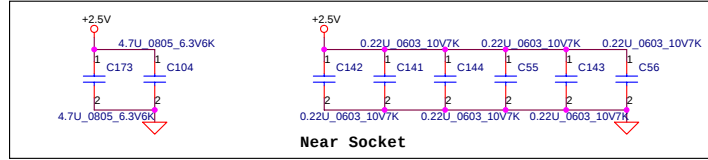


FOX_P293903-314603



CPU Decoupling Capacitor

Loop Bandwidth KHz	Bulk Cappacitance uF	Total ESR ohm
20	23000	2.5m ohm (AMD)
50	9000	0.9m ohm
* 300	1500	2.5m ohm



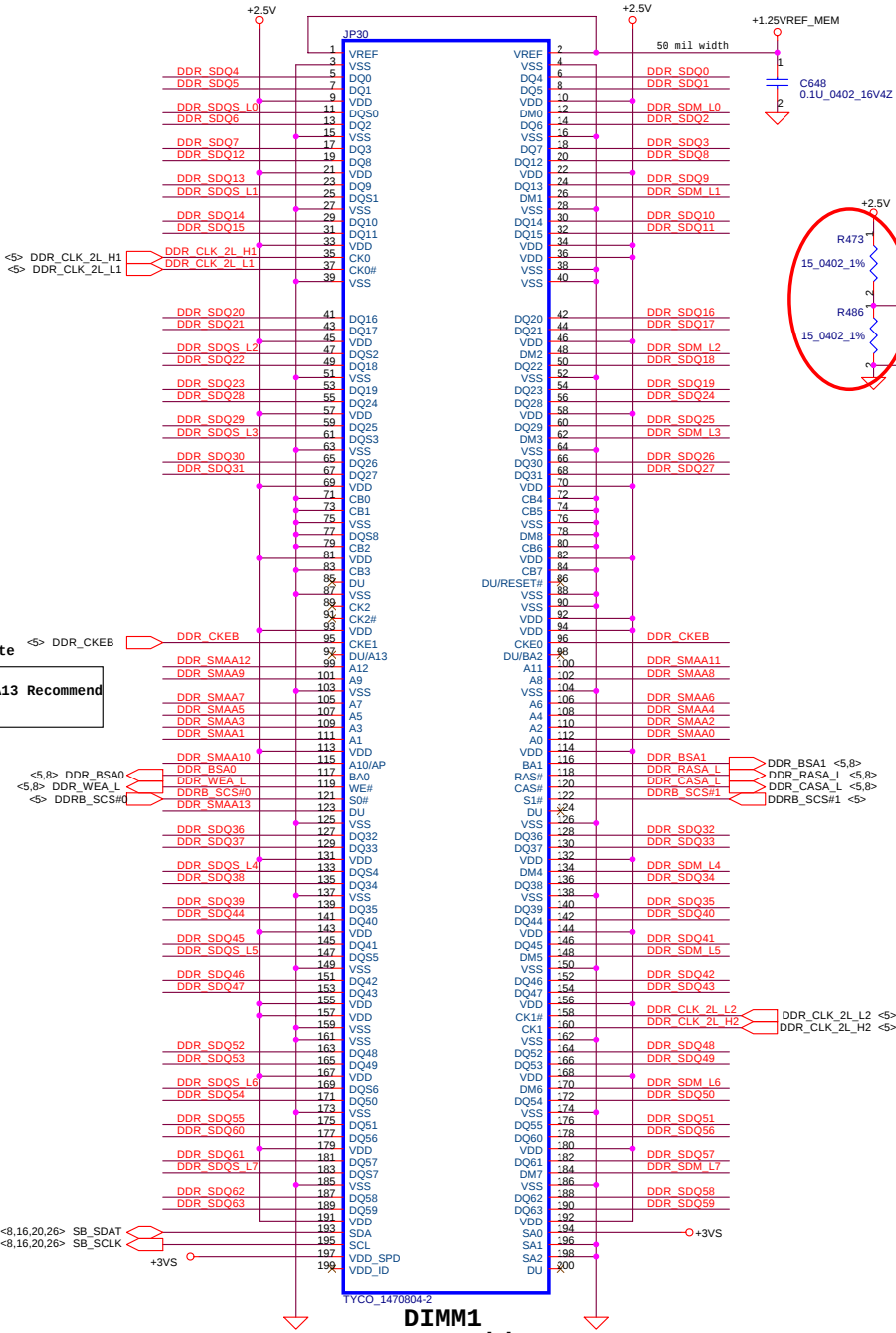
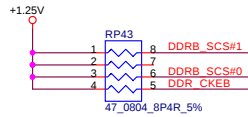
Near Socket

Compal Electronics, Inc.			
Claw Hammer (Power & Ground)			
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Compal Electronics, Inc.			
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DDR-SODIMM SLOT0			
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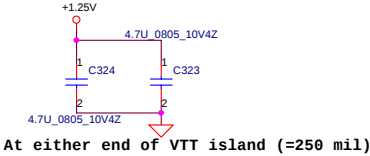
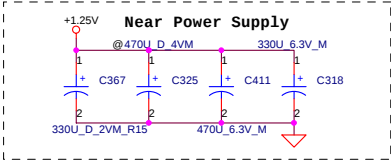
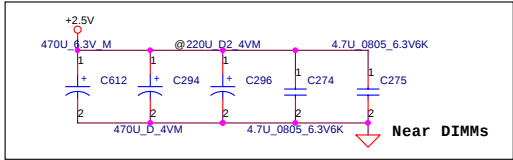
Layout note
Note:
DDR_SMAA13 Recommend
for AMD.

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<5,8> DDR_SDM_L[0..7] <DDR_SDM_L[0..7]>
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<5,8> DDR_SDQ[0..63] <DDR_SDQ[0..63]>

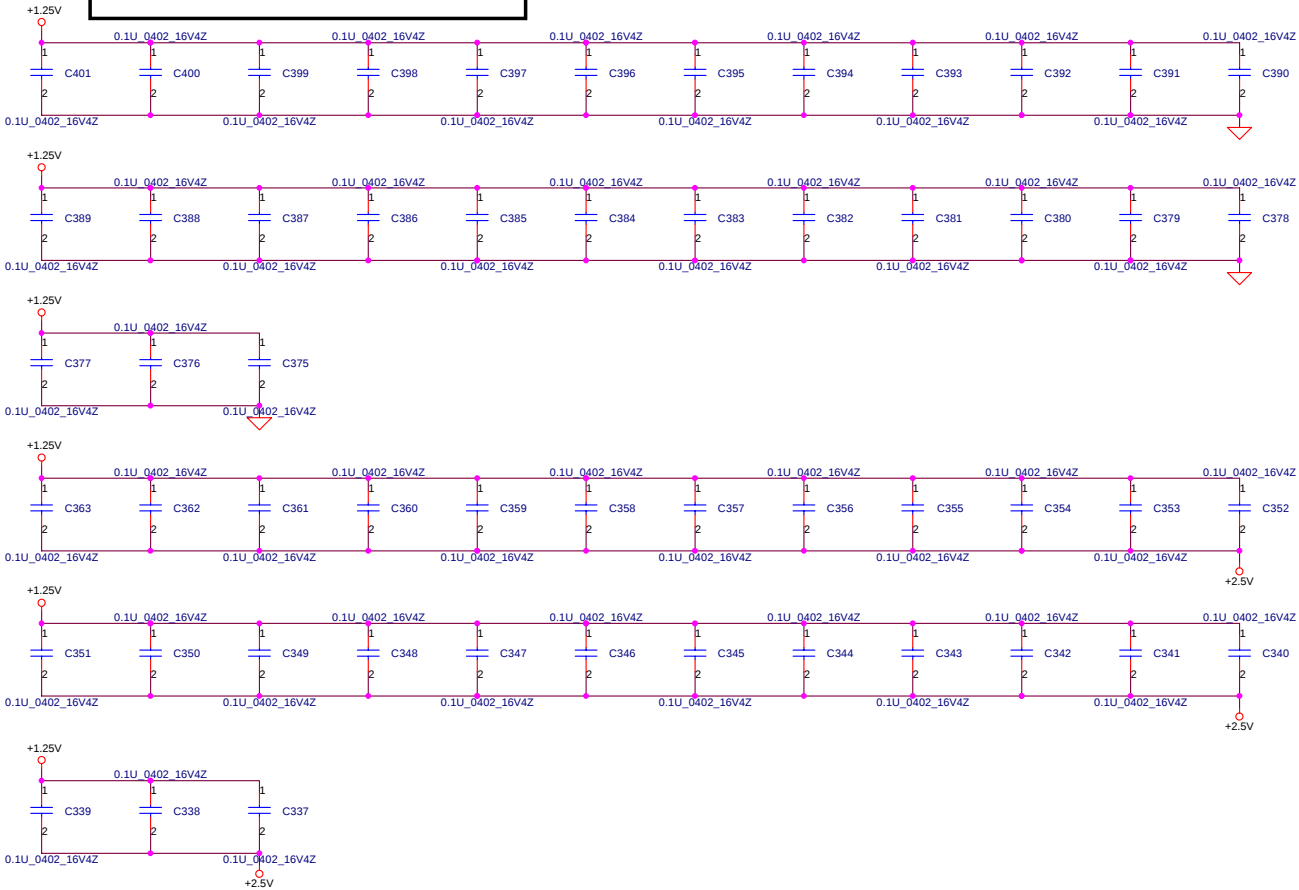
<8,16,20,26> SB_SDAT
<8,16,20,26> SB_SCLK

Compal Electronics, Inc.			
DDR-SODIMM SLOT1			
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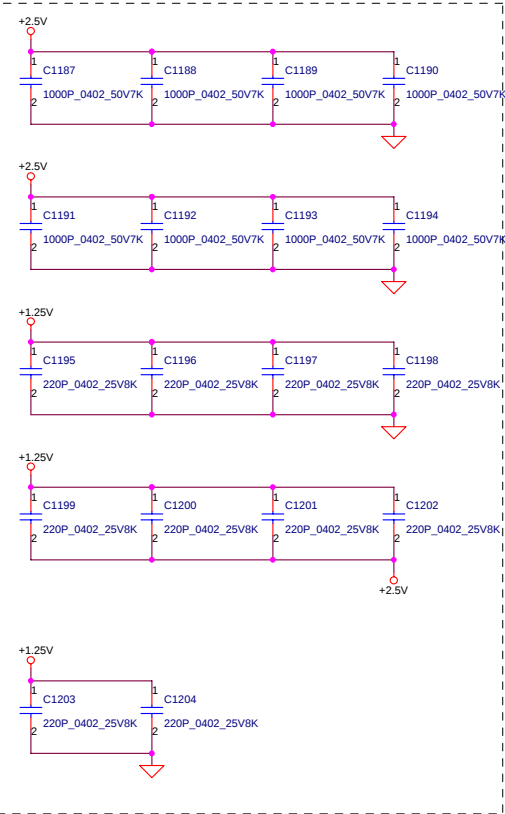
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Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25VS



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DDR SODIMM Decoupling			
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<4> H_CADIP[0..15] H_CADIP[0..15]
<4> H_CADIN[0..15] H_CADIN[0..15]
<4> H_CADOP[0..15] H_CADOP[0..15]
<4> H_CADON[0..15] H_CADON[0..15]

<15> NMAA[0..14] NMAA[0..14]
<15> NMDA[0..63] NMDA[0..63]
<15> NDQMA[0..7] NDQMA[0..7]
<15> NDQSA[0..7] NDQSA[0..7]

U27A
H_CADOP15 T26 HT_RXCAD15P
H_CADON15 R26 HT_RXCAD15N
H_CADOP14 U25 HT_RXCAD14P
H_CADON14 V25 HT_RXCAD14N
H_CADOP13 V26 HT_RXCAD13P
H_CADON13 U26 HT_RXCAD13N
H_CADOP12 W25 HT_RXCAD12P
H_CADON12 W24 HT_RXCAD12N
H_CADOP11 AA25 HT_RXCAD11P
H_CADON11 AA24 HT_RXCAD11N
H_CADOP10 AB26 HT_RXCAD10P
H_CADON10 AA26 HT_RXCAD10N
H_CADOP9 AC25 HT_RXCAD9P
H_CADON9 AC24 HT_RXCAD9N
H_CADOP8 AD26 HT_RXCAD8P
H_CADON8 AC26 HT_RXCAD8N
H_CADOP7 R29 HT_RXCAD7P
H_CADON7 R28 HT_RXCAD7N
H_CADOP6 T30 HT_RXCAD6P
H_CADON6 T30 HT_RXCAD6N
H_CADOP5 T28 HT_RXCAD5P
H_CADON5 T29 HT_RXCAD5N
H_CADOP4 V29 HT_RXCAD4P
H_CADON4 U29 HT_RXCAD4N
H_CADOP3 Y30 HT_RXCAD3P
H_CADON3 W30 HT_RXCAD3N
H_CADOP2 Y28 HT_RXCAD2P
H_CADON2 Y29 HT_RXCAD2N
H_CADOP1 AB29 HT_RXCAD1P
H_CADON1 AA29 HT_RXCAD1N
H_CADOP0 AC29 HT_RXCAD0P
H_CADON0 AC28 HT_RXCAD0N

HYPER TRANSPORT CPU
I/F

HT_TXCAD15P R24 H_CADIP15
HT_TXCAD15N R25 H_CADIN15
HT_TXCAD14P N26 H_CADIP14
HT_TXCAD14N N24 H_CADIN14
HT_TXCAD13P N25 H_CADIP13
HT_TXCAD13N L26 H_CADIN12
HT_TXCAD12P L26 H_CADIP12
HT_TXCAD12N J26 H_CADIP11
HT_TXCAD11P J26 H_CADIN11
HT_TXCAD11N K26 H_CADIP10
HT_TXCAD10P J24 H_CADIP10
HT_TXCAD10N G26 H_CADIN10
HT_TXCAD9P G26 H_CADIP9
HT_TXCAD9N H26 H_CADIN9
HT_TXCAD8P G24 H_CADIP8
HT_TXCAD8N G25 H_CADIN8
HT_TXCAD7P L30 H_CADIP7
HT_TXCAD7N M30 H_CADIN7
HT_TXCAD6P L28 H_CADIP6
HT_TXCAD6N L23 H_CADIN6
HT_TXCAD5P J29 H_CADIP5
HT_TXCAD5N K29 H_CADIN5
HT_TXCAD4P H30 H_CADIP4
HT_TXCAD4N H29 H_CADIN4
HT_TXCAD3P E29 H_CADIP3
HT_TXCAD3N E28 H_CADIN3
HT_TXCAD2P D30 H_CADIP2
HT_TXCAD2N E30 H_CADIN2
HT_TXCAD1P D29 H_CADIP1
HT_TXCAD1N D28 H_CADIN1
HT_TXCAD0P B29 H_CADIP0
HT_TXCAD0N C29 H_CADIN0

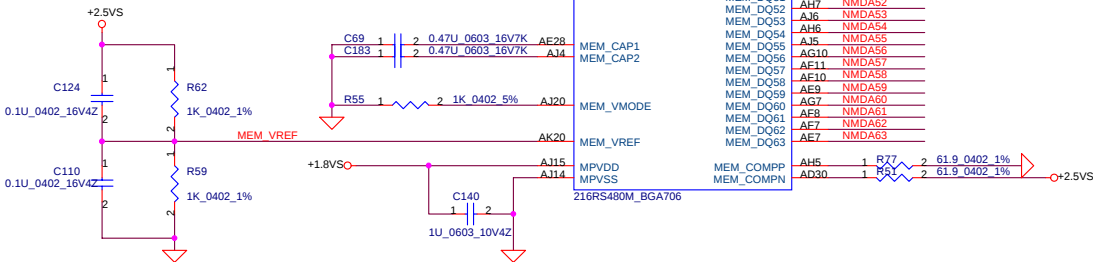
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<4> H_CLKON1 H_CLKON1 W26 HT_RXCLK1N
<4> H_CLKOP0 H_CLKOP0 W29 HT_RXCLK0P
<4> H_CLKON0 H_CLKON0 W28 HT_RXCLK0N
<4> H_CTLPO0 H_CTLPO0 P29 HT_RXCTLTP
<4> H_CTLNO0 H_CTLNO0 N29 HT_RXCTLN
R49 1 2 49.9 0402 1% D27
R48 1 2 49.9 0402 1% E27

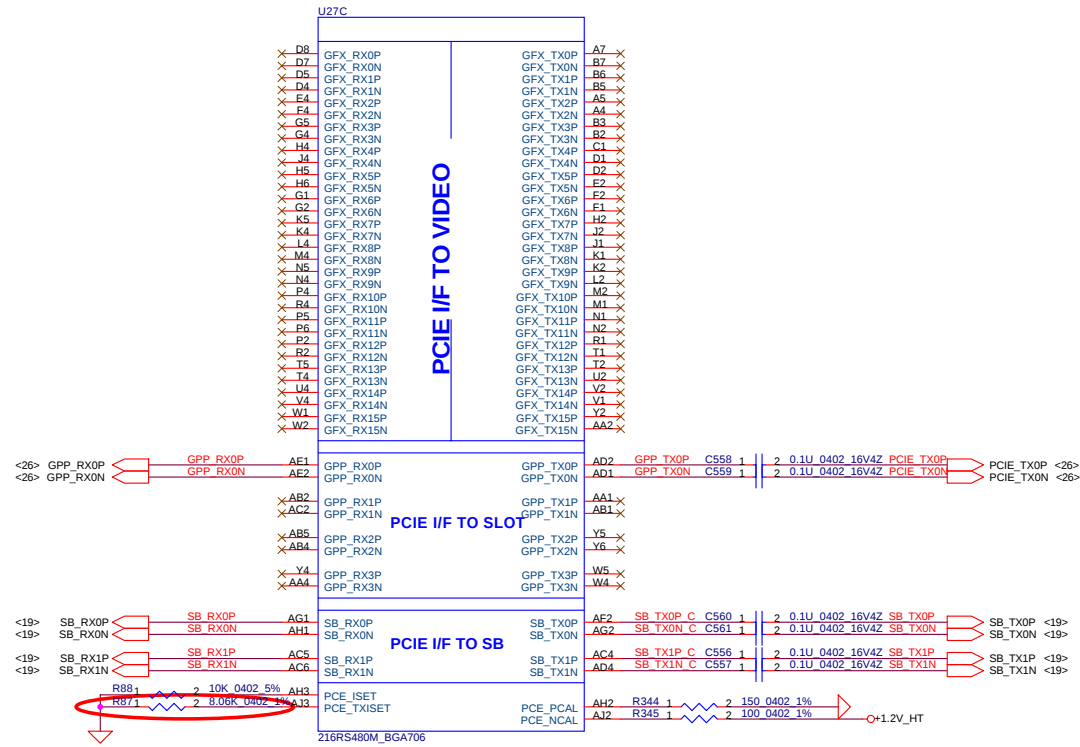
216RS480M_BGA706

HT_TXCLK1P L24 H_CLKIP1 H_CLKIP1 <4>
HT_TXCLK1N L25 H_CLKIN1 H_CLKIN1 <4>
HT_TXCLK0P F29 H_CLKIP0 H_CLKIP0 <4>
HT_TXCLK0N G29 H_CLKIN0 H_CLKIN0 <4>
HT_TXCTLTP M29 H_CTLIPO H_CTLIPO <4>
HT_TXCTLN M28 H_CTLINO H_CTLINO <4>
HT_TXCALP B28 R53 1 2 91 0402 5%
HT_TXCALN A28

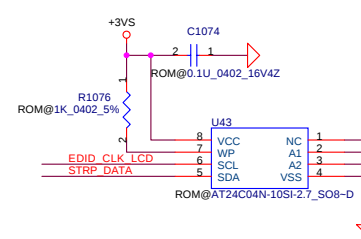
U27B
NMAA0 AF17 MEM_A0 MEM_DQ0 AF28 NMDA0
NMAA1 AK17 MEM_A1 MEM_DQ1 AF27 NMDA1
NMAA2 AH16 MEM_A2 MEM_DQ2 AG28 NMDA2
NMAA3 AE16 MEM_A3 MEM_DQ3 AF26 NMDA3
NMAA4 AJ22 MEM_A4 MEM_DQ4 AE25 NMDA4
NMAA5 AJ21 MEM_A5 MEM_DQ5 AE24 NMDA5
NMAA6 AH21 MEM_A6 MEM_DQ6 AE23 NMDA6
NMAA7 AH20 MEM_A7 MEM_DQ7 AE29 NMDA7
NMAA8 AK19 MEM_A8 MEM_DQ8 AE29 NMDA8
NMAA9 AH19 MEM_A9 MEM_DQ9 AE29 NMDA9
NMAA10 AJ17 MEM_A10 MEM_DQ10 AG30 NMDA10
NMAA11 AG16 MEM_A11 MEM_DQ11 AG29 NMDA11
NMAA12 AG17 MEM_A12 MEM_DQ12 AH28 NMDA12
NMAA13 AH17 MEM_A13 MEM_DQ13 AJ28 NMDA13
NMAA14 AJ18 MEM_A14 MEM_DQ14 AH27 NMDA14
NDQMA0 AG26 MEM_DM0 MEM_DQ15 AE23 NMDA15
NDQMA1 AJ29 MEM_DM1 MEM_DQ16 AG22 NMDA16
NDQMA2 AE21 MEM_DM2 MEM_DQ17 AG22 NMDA17
NDQMA3 AH24 MEM_DM3 MEM_DQ18 AF22 NMDA18
NDQMA4 AH12 MEM_DM4 MEM_DQ19 AE20 NMDA19
NDQMA5 AG13 MEM_DM5 MEM_DQ20 AG19 NMDA20
NDQMA6 AH8 MEM_DM6 MEM_DQ21 AE20 NMDA21
NDQMA7 AE8 MEM_DM7 MEM_DQ22 AE20 NMDA22
NDQSA0 AE25 MEM_DQSON AE26 NMDA23
NDQSA1 AH30 MEM_DQS1P AK26 NMDA24
NDQSA2 AG20 MEM_DQS2P AH25 NMDA25
NDQSA3 AJ25 MEM_DQS2P AJ24 NMDA26
NDQSA4 AH13 MEM_DQS3P AH23 NMDA27
NDQSA5 AE14 MEM_DQS4P AH23 NMDA28
NDQSA6 AJ7 MEM_DQSSP AJ23 NMDA29
NDQSA7 AG8 MEM_DQSS6 AJ22 NMDA30
AG25 MEM_DQSS7 AK14 NMDA31
AH29 MEM_DQSSN AK13 NMDA32
AE21 MEM_DQS1N AK13 NMDA33
AK25 MEM_DQS2N AK11 NMDA34
AJ12 MEM_DQS3N AK11 NMDA35
AE13 MEM_DQS4N AK10 NMDA36
AK20 MEM_DQSSN AK10 NMDA37
AK20 MEM_DQSS6 AK15 NMDA38
AE9 MEM_DQSS7 AK15 NMDA39
MEM_RAS# MEM_DQ42 AE14 NMDA40
MEM_CAS# MEM_DQ43 AE14 NMDA41
MEM_WE# MEM_DQ44 AE12 NMDA42
MEM_CS# MEM_DQ45 AE12 NMDA43
MEM_CKE MEM_DQ46 AE11 NMDA44
NMCLKA0 AK16 MEM_CKP AE11 NMDA45
NMCLKA0# AJ16 MEM_CKN AE11 NMDA46
MEM_CAP1 MEM_DQ52 AH7 NMDA47
MEM_CAP2 MEM_DQ53 AH6 NMDA48
MEM_VMODE MEM_DQ54 AJ5 NMDA49
MEM_VREF MEM_DQ55 AG10 NMDA50
MPVDD MEM_DQ56 AE11 NMDA51
MPVSS MEM_DQ57 AE10 NMDA52
MEM_COMP MEM_DQ58 AE9 NMDA53
MEM_COMP# MEM_DQ59 AG7 NMDA54
MEM_COMP# MEM_DQ60 AE6 NMDA55
MEM_COMP# MEM_DQ61 AE7 NMDA56
MEM_COMP# MEM_DQ62 AE7 NMDA57
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AH5 1 R77 2 61.9 0402 1%
AD30 1 R54 2 61.9 0402 1%

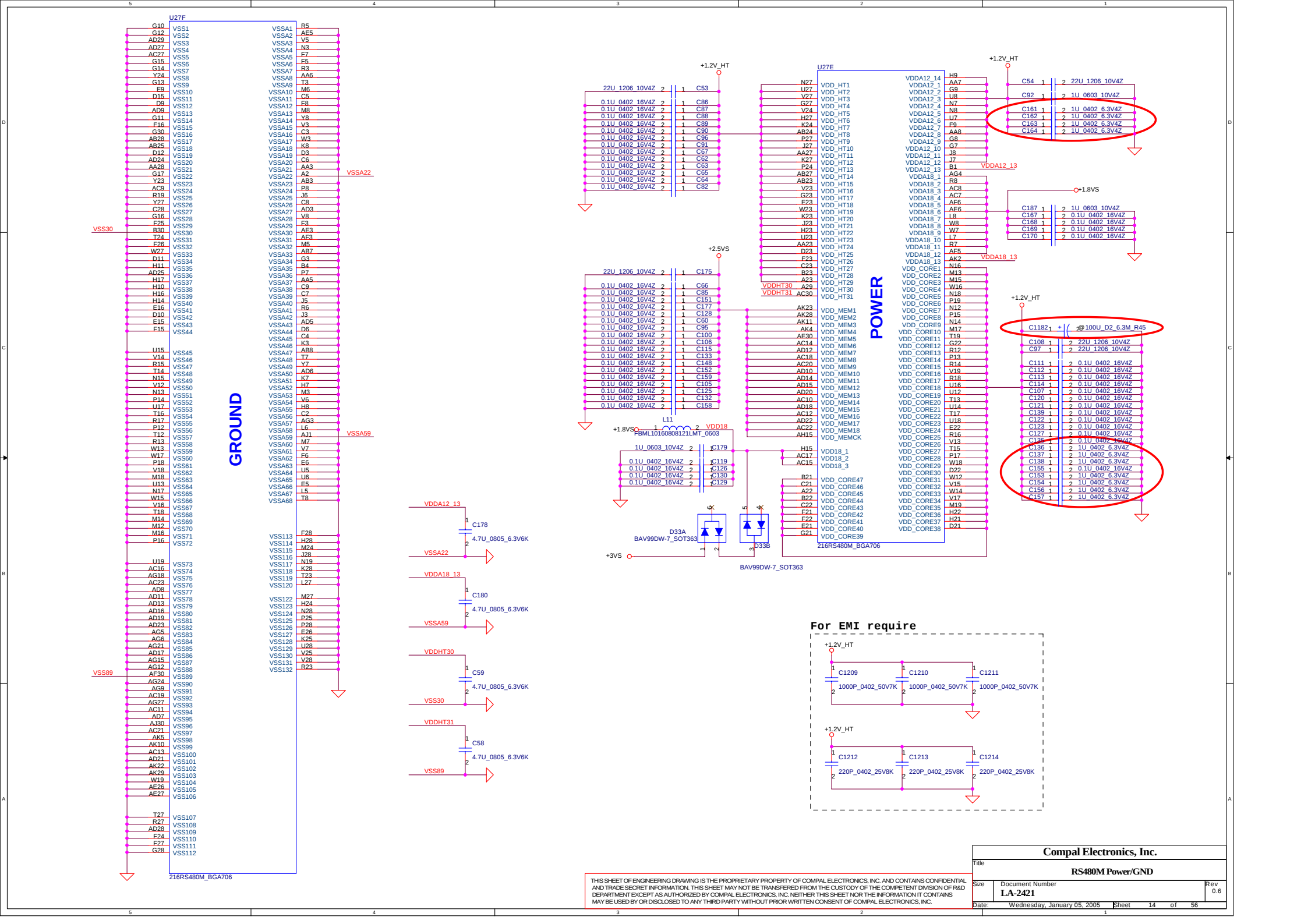
MEM_A I/F

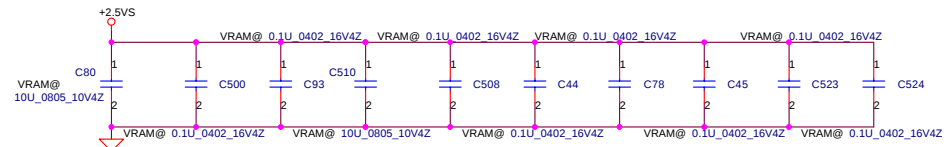




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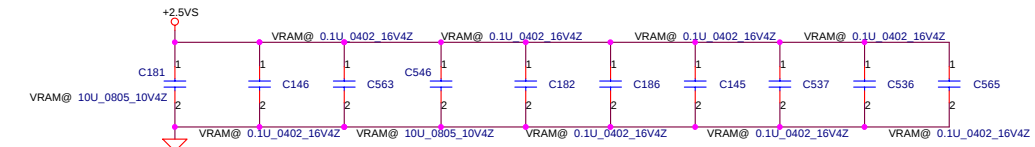
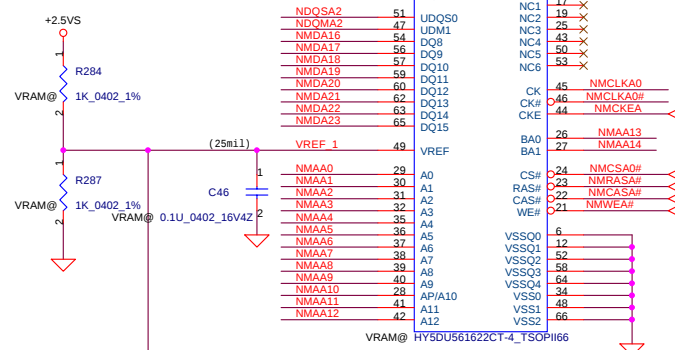






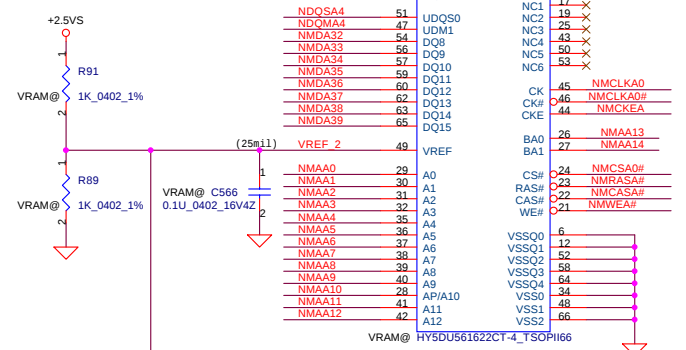
As close as possible to related pin

- <11> NMAA[0..14] NMAA[0..14]
- <11> NMDA[0..63] NMDA[0..63]
- <11> NDQMA[0..7] NDQMA[0..7]
- <11> NDQSA[0..7] NDQSA[0..7]

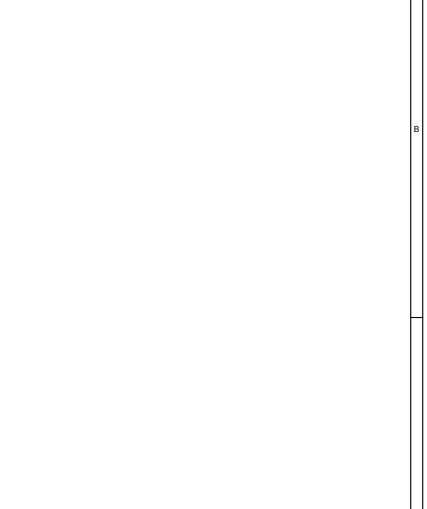
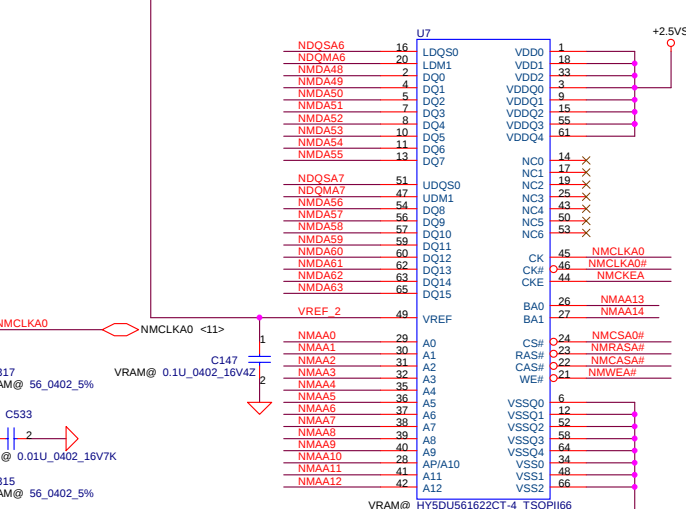
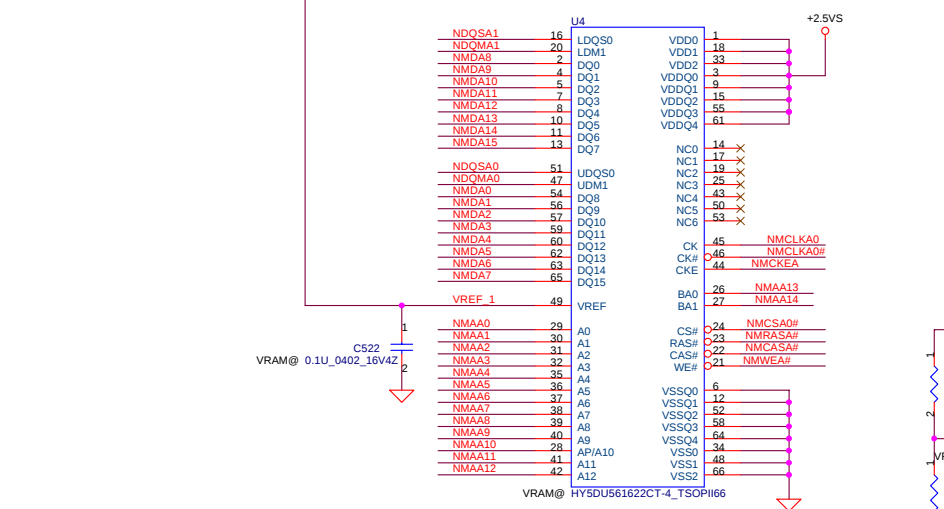
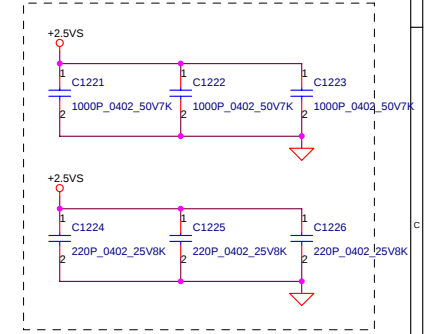


As close as possible to related pin

- <11> NMAA[0..14] NMAA[0..14]
- <11> NMDA[0..63] NMDA[0..63]
- <11> NDQMA[0..7] NDQMA[0..7]
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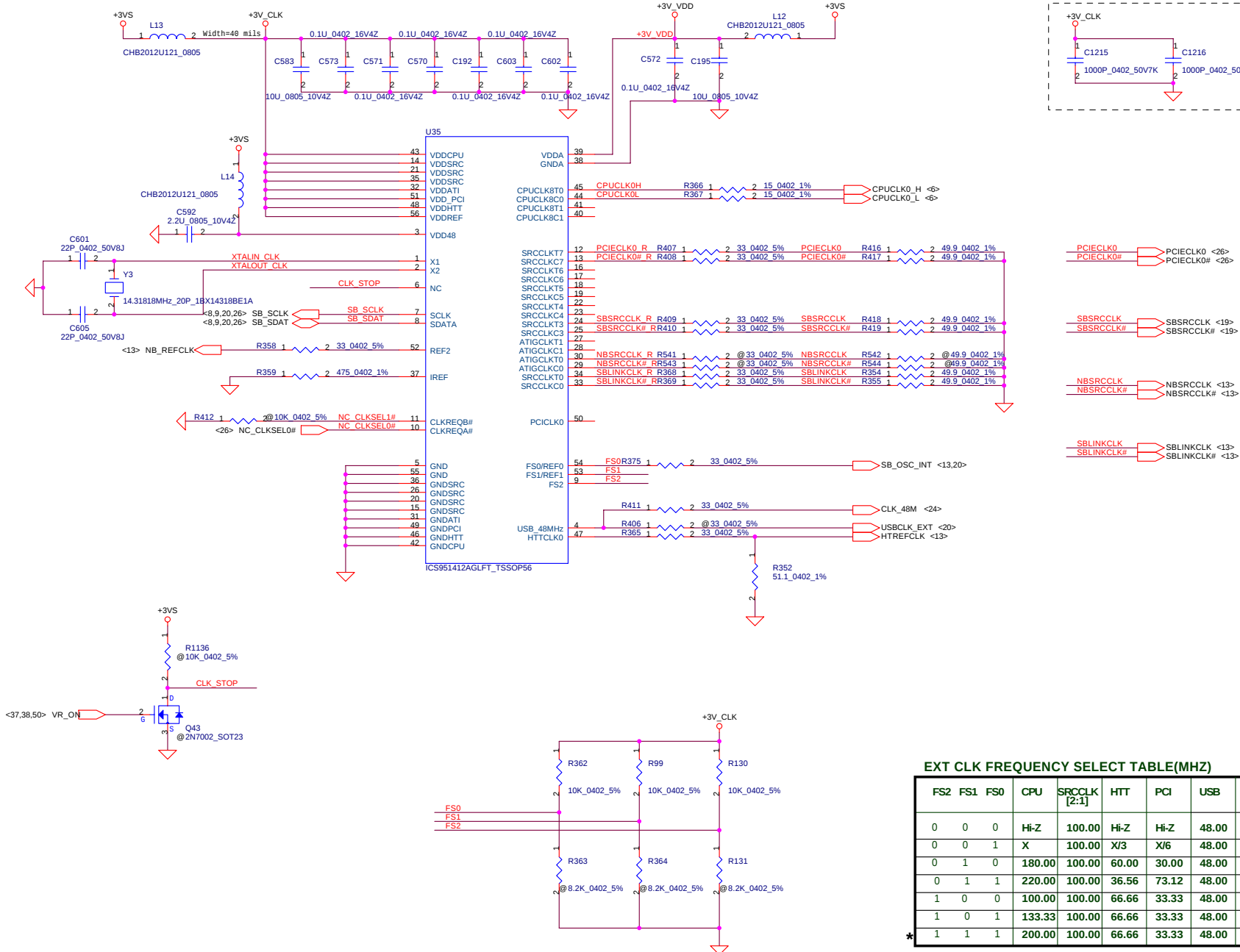


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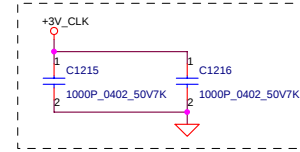


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EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
* 1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

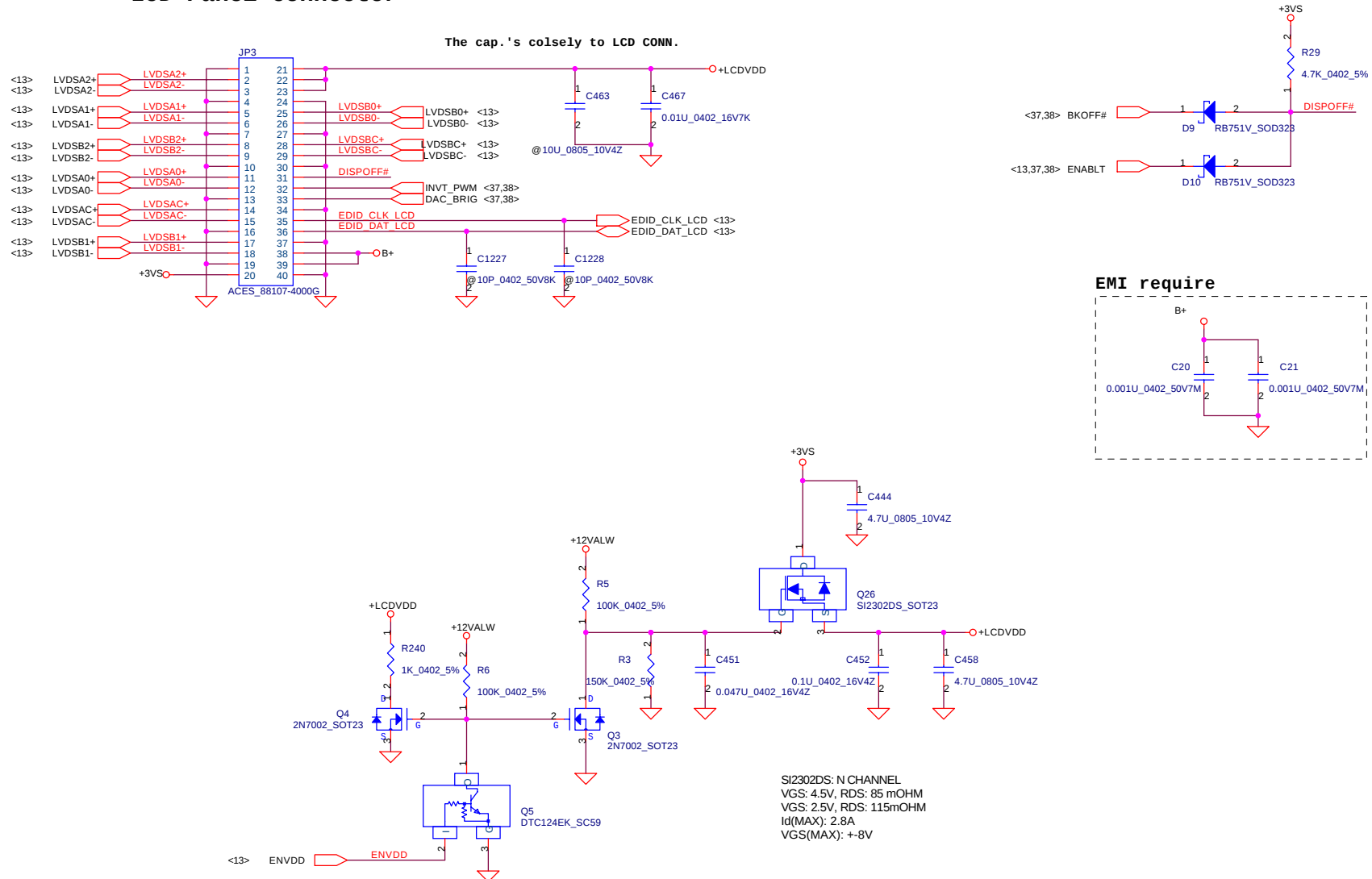
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Clock Generator

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Size	L/A-2421	0.6
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LCD Panel Connector



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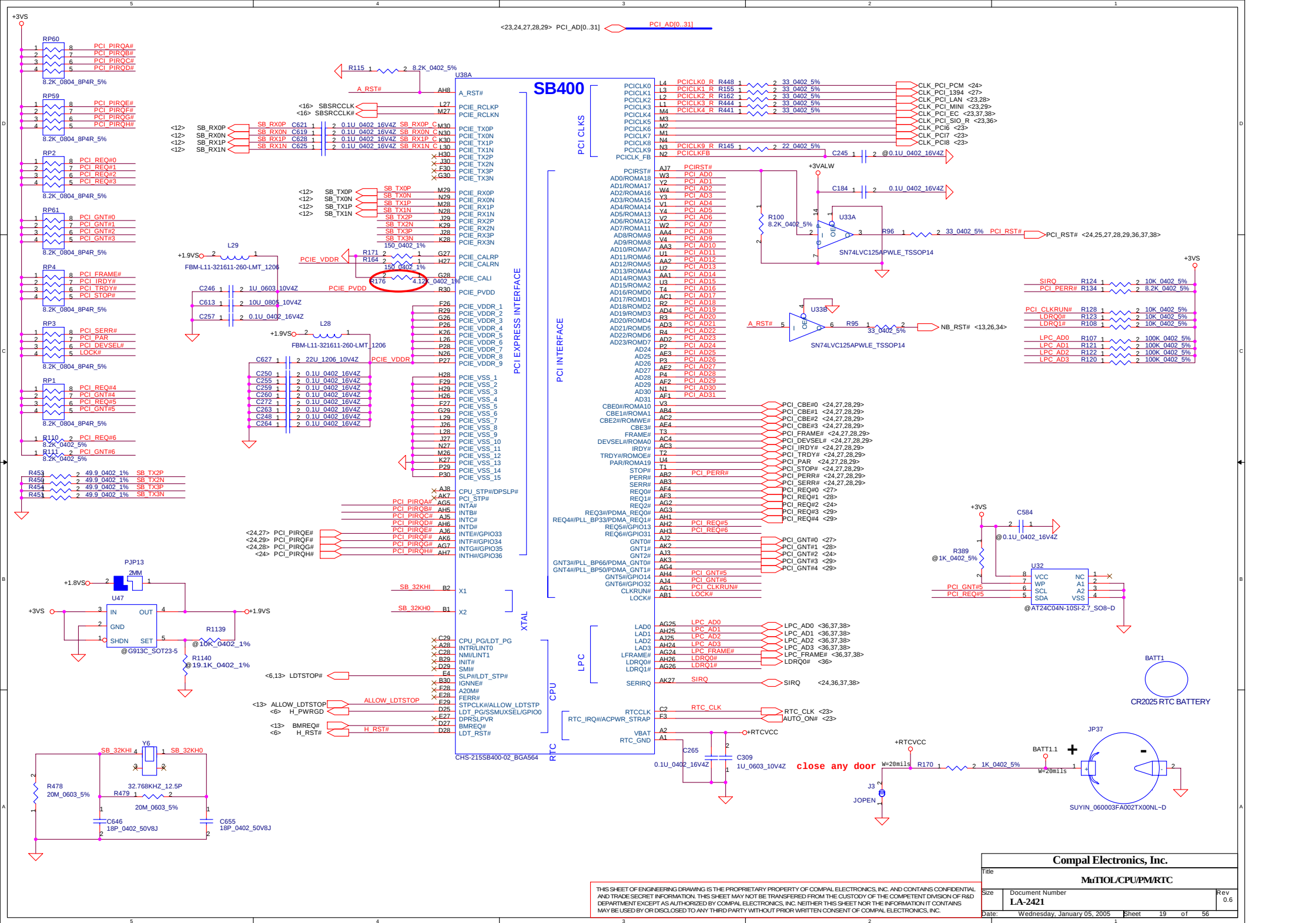
Compal Electronics, Inc.		
Title		
LVDS Connector		
Size	Document Number	Rev
	LA-2421	0.6
Date:	Wednesday, January 05, 2005	Sheet 17 of 56

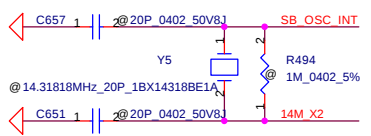
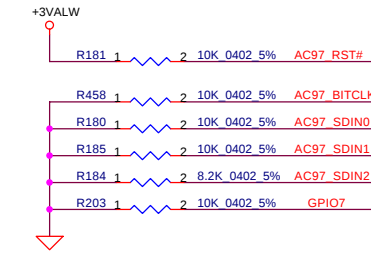
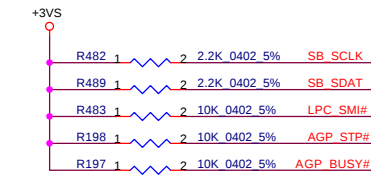
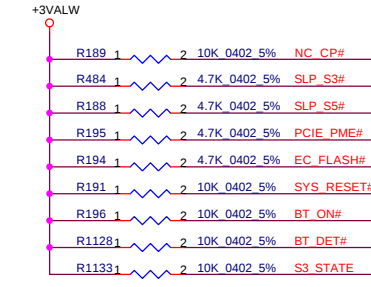
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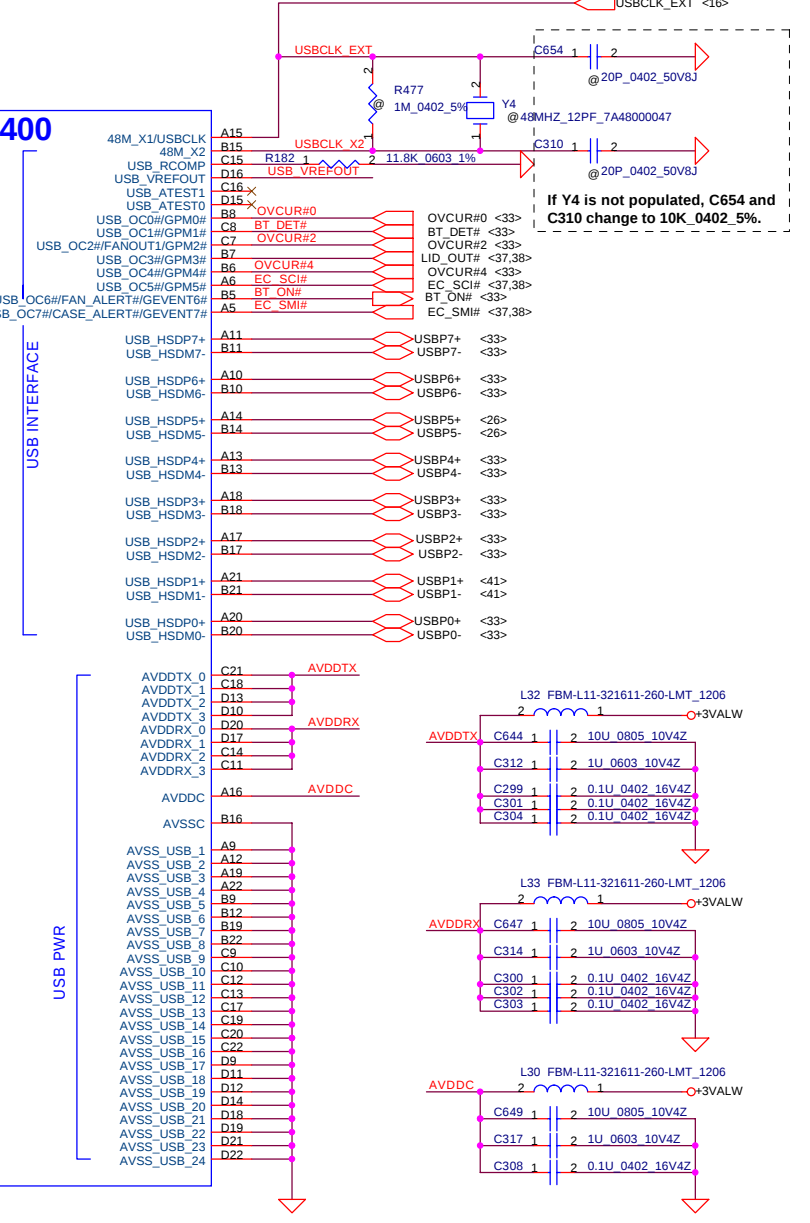
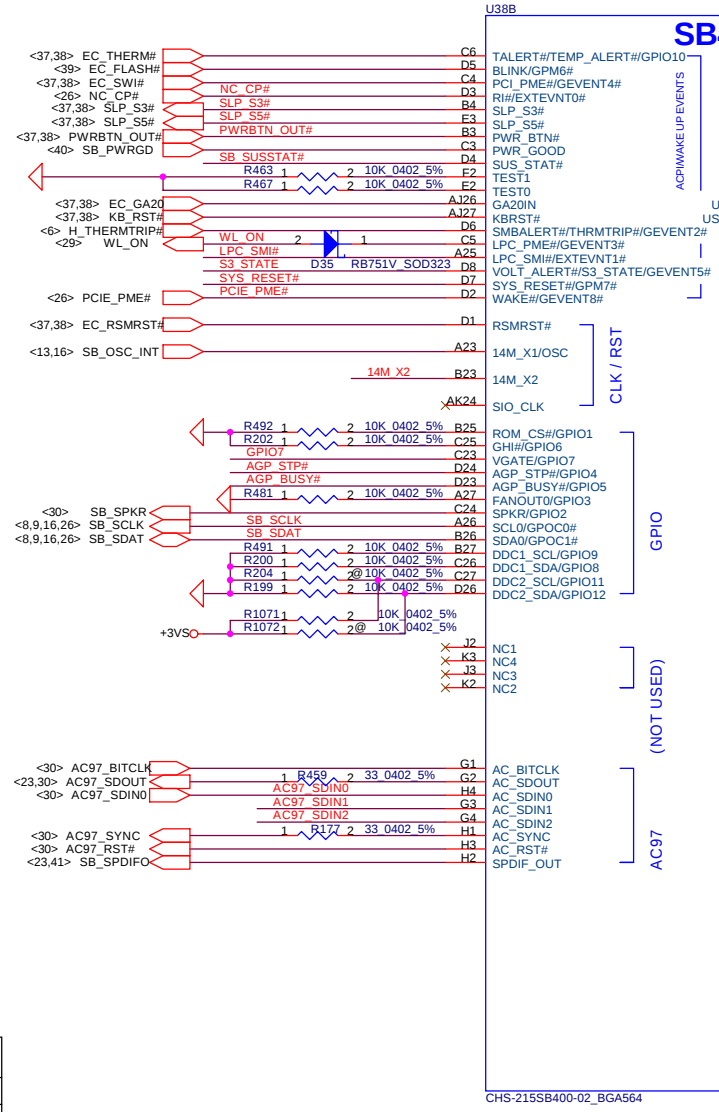


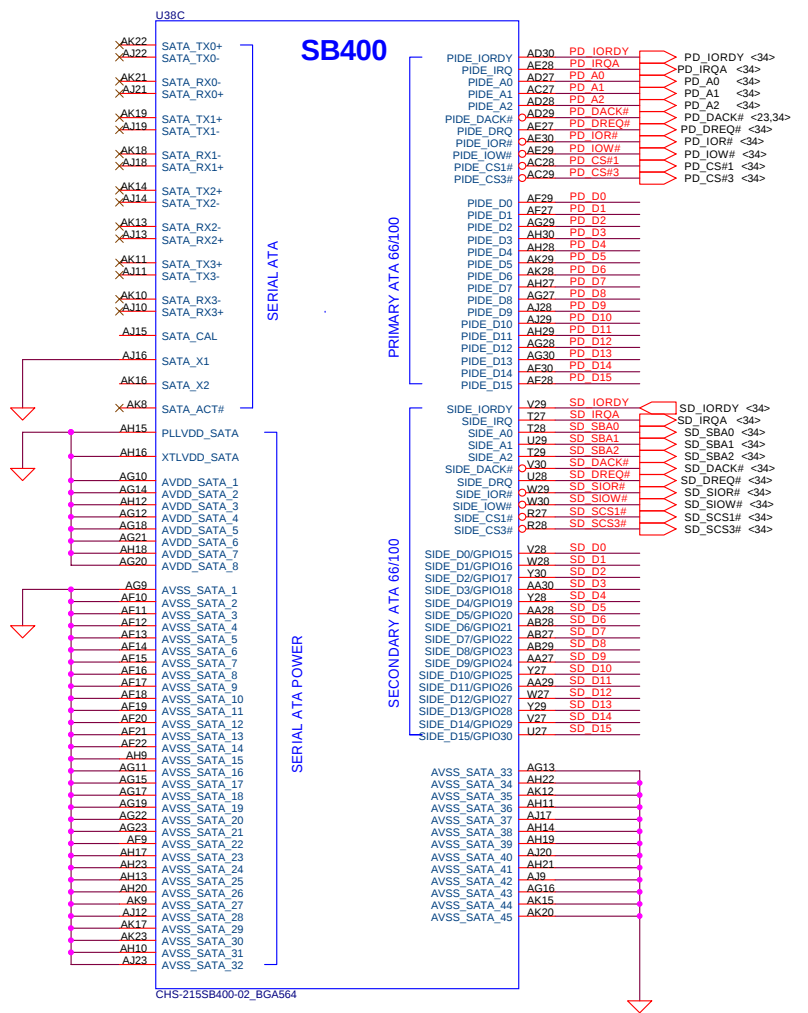
Compal Electronics, Inc.			
Title CRT & TVout Connector			
Size	Document Number LA-2421		Rev 0.6
Date: Wednesday, January 05, 2005 Sheet 18 of 56			





	GPI012	GPI011
HYNIX 128MB	0	1
SAMSUNG 128MB	1	1
No VRAM	0	0
Reserved	1	0

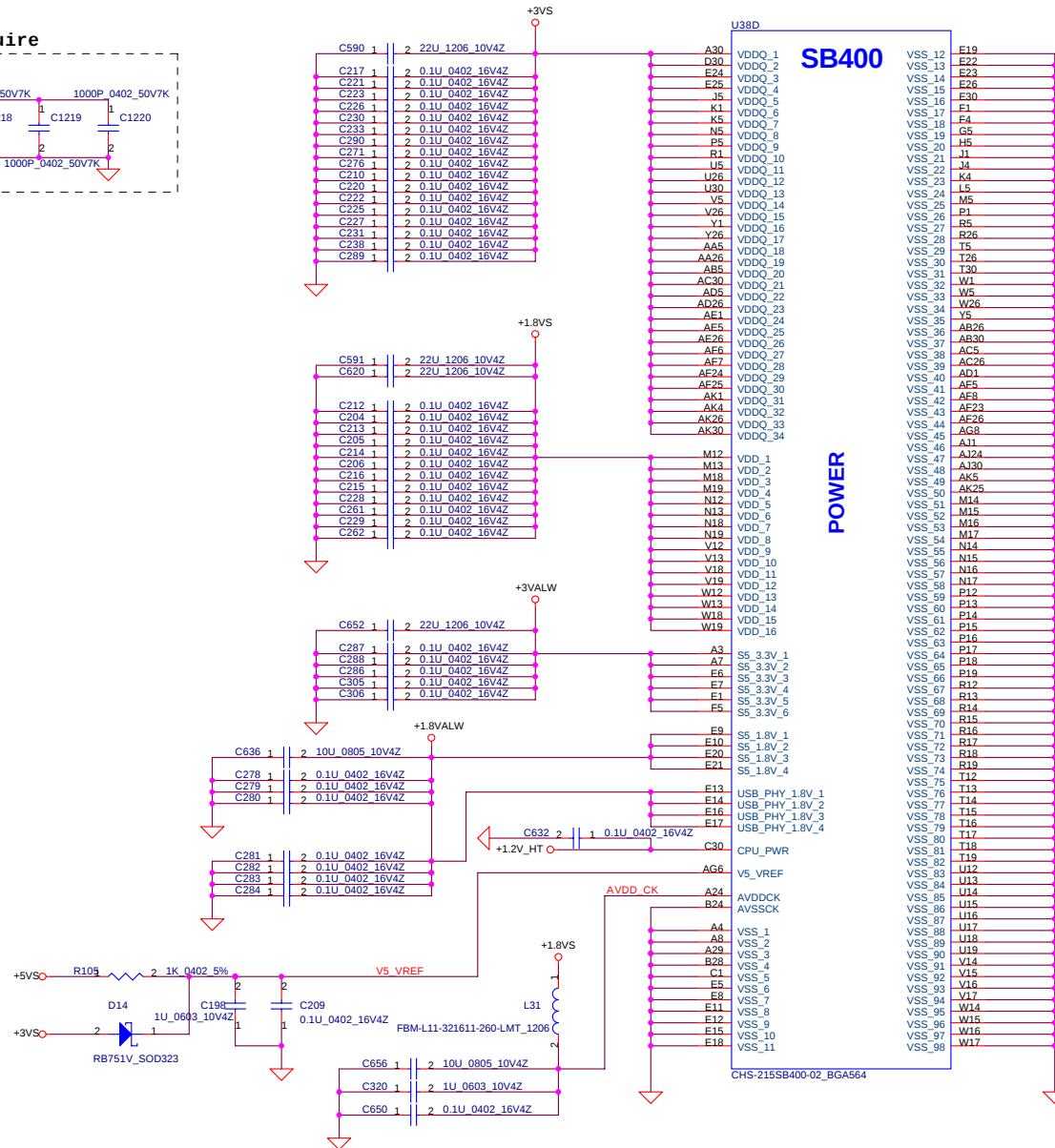
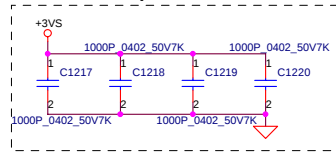




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Compal Electronics, Inc.			
Title			
IDE/SATA			
Size	Document Number	Rev	
Custom	LA-2421	0.6	
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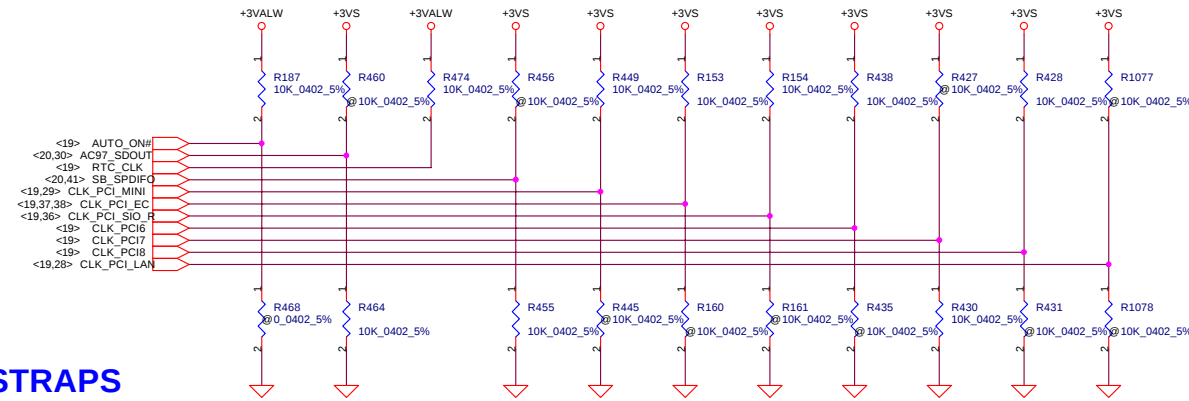
For EMI require



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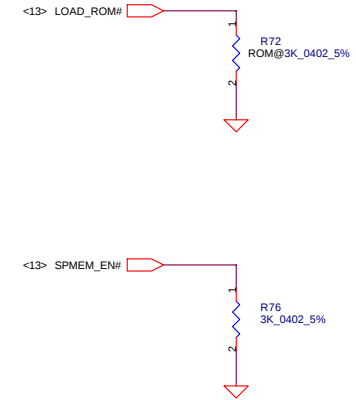
Compal Electronics, Inc.			
Title		Power/GND	
Size	Document Number	Rev	
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REQUIRED STRAPS



	AUTO_ON#	AC97_SDOOUT	RTC_CLK	SB_SPDIFO	CLK_PCI_LAN	CLK_PCI_MINI	CLK_PCI_EC	CLK_PCI_SIO	CLK_PCI6	CLK_PCI7	CLK_CLK8
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz XTAL MODE	USB PHY PWRDOWN DISABLE DEFAULT	INTERNAL 48MHz DEFAULT	14MHz OSC MODE DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM	
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz OSC MODE DEFAULT	USB PHY PWRDOWN ENABLE	EXTERNAL 48MHz	14MHz XTAL MODE	CPU I/F = P4	L,H = NORMAL LPC ROM L,L = FWH ROM DEFAULT	

NB STRAPS



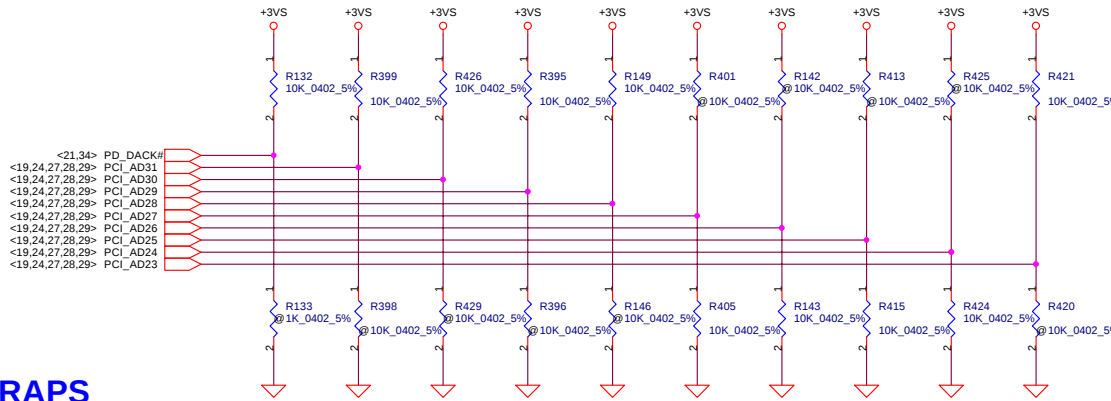
LOAD_ROM#:LOAD ROM STRAP ENABLE strap

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

SPMEM_EN#:SIDE PORT MEMORY ENABLE strap

High, SIDE PORT MEMORY DISABLE
Low, SIDE PORT MEMORY ENABLE

DEBUG STRAPS



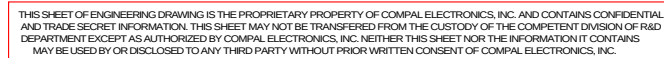
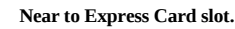
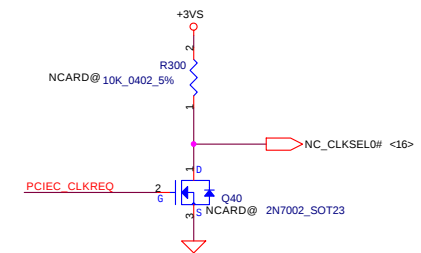
	PD_DACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

Compal Electronics, Inc.

Hardware Trap

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<19,23,24,28,29> PCI_AD[0..31]

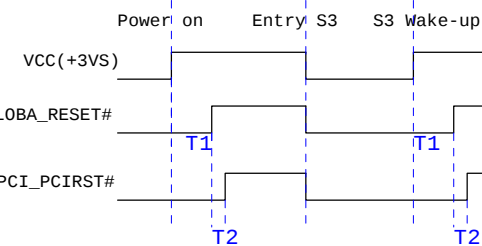
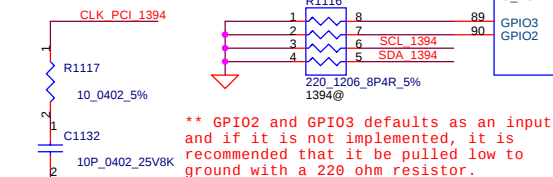
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
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PCI_AD23
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PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0

<19,24,28,29> PCI_CBE#3
<19,24,28,29> PCI_CBE#2
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<19> CLK_PCI_1394
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<19,24,28,29> PCI_STOP#
<19,24,28,29> PCI_PERR#
<19,24,29> PCI_PIRQE#
<19,24,28,29> PCI_SERR#
<19,24,28,29> PCI_PAR

<19,24,25,28,29,36,37,38> PCI_RST#

G_RST# connect to PCIRST#



T1: >2ms
T2: >=0

Note: GPIOA_RESET#
Can Connect to
PCI_PCIRST#

TSB43AB22

PCI BUS INTERFACE

PHY PORT 2

BIAS CURRENT

OSCILLATOR

FILTER

EEPROM 2 WIRE BUS

POWER CLASS

PHY PORT 1

EEPROM cancel,
need System
Support

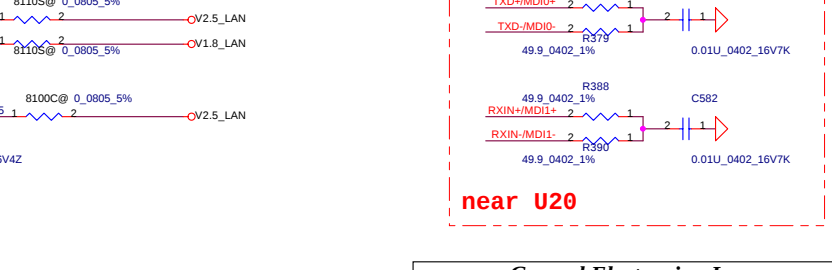
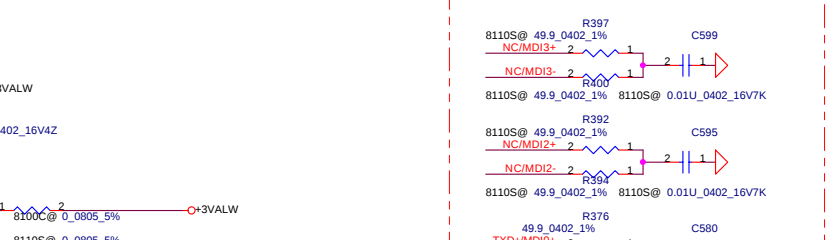
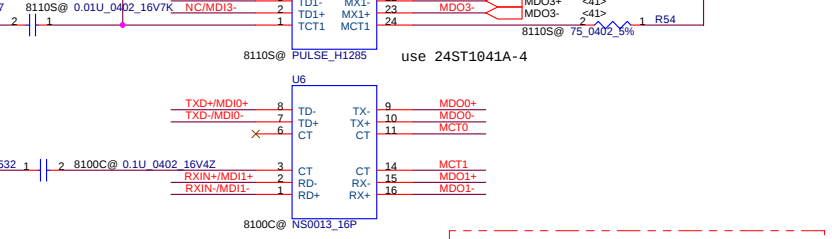
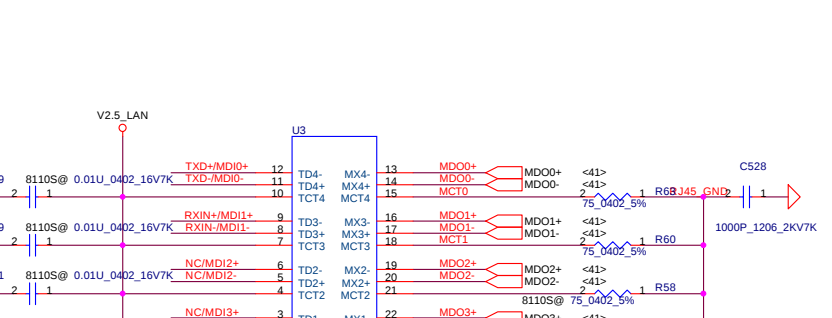
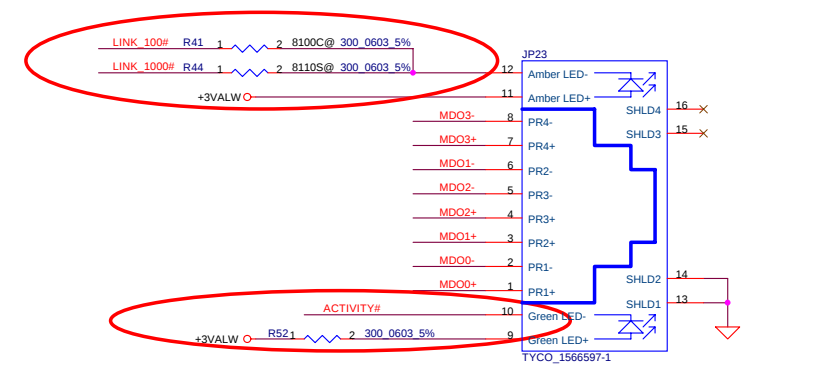
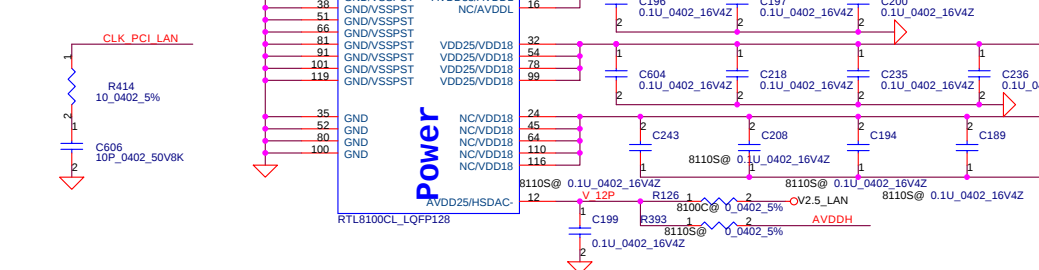
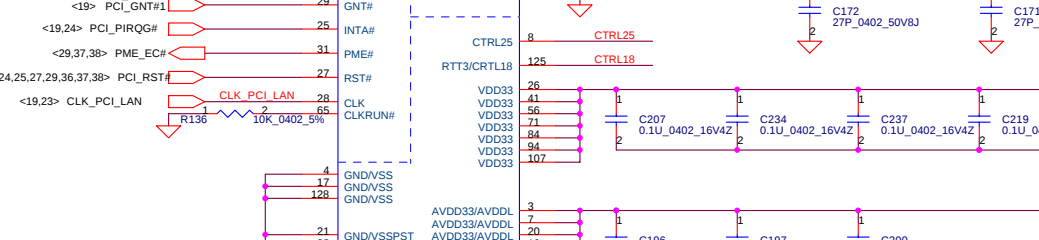
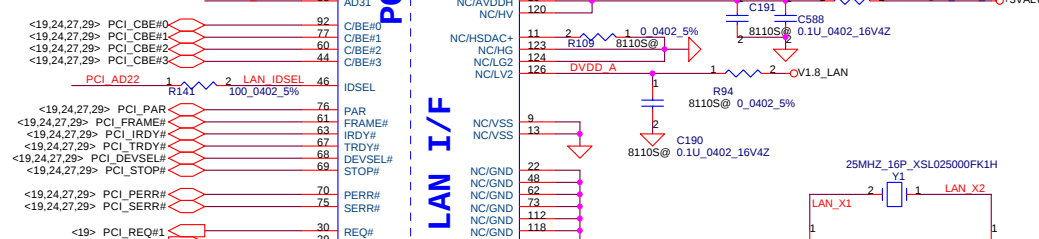
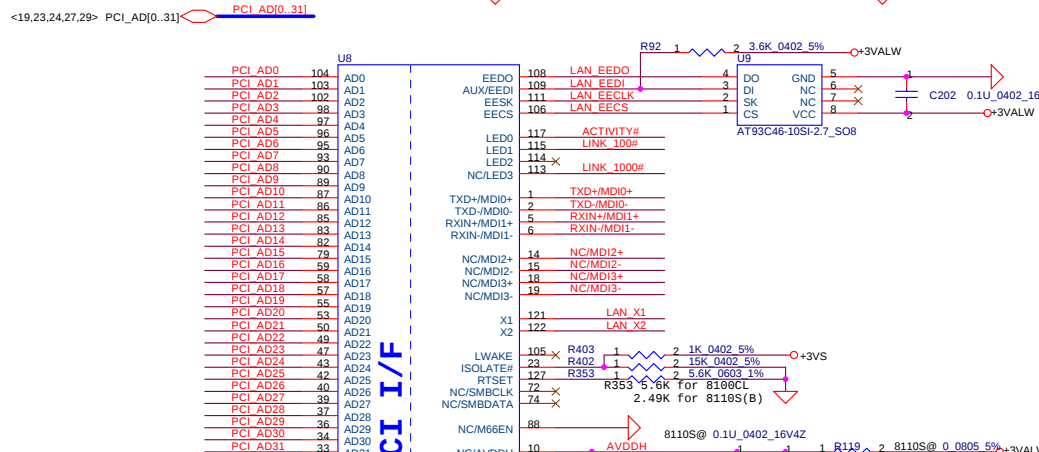
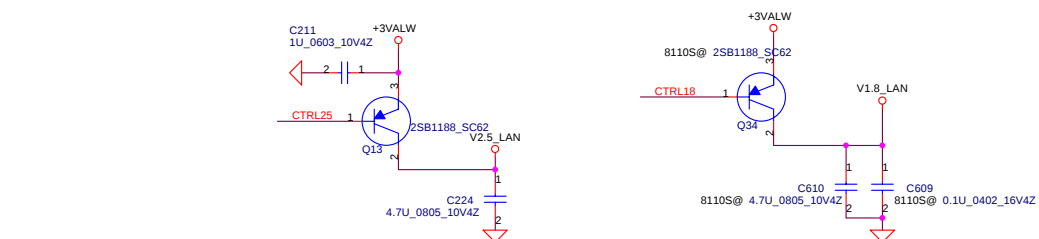
Close Chip

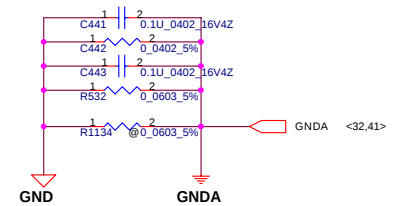
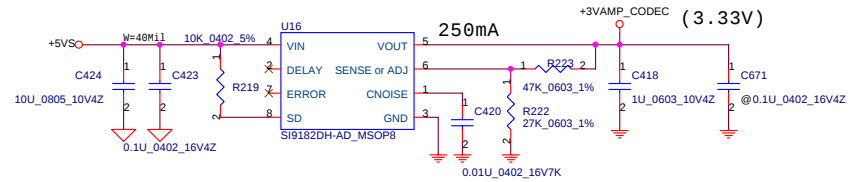
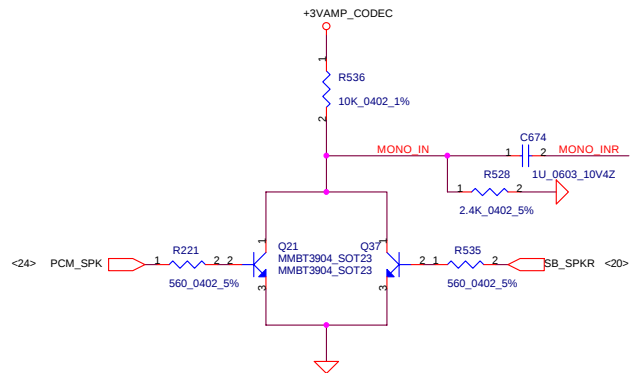
The connector depend on
defferent project

Connect To
Shielding
GND

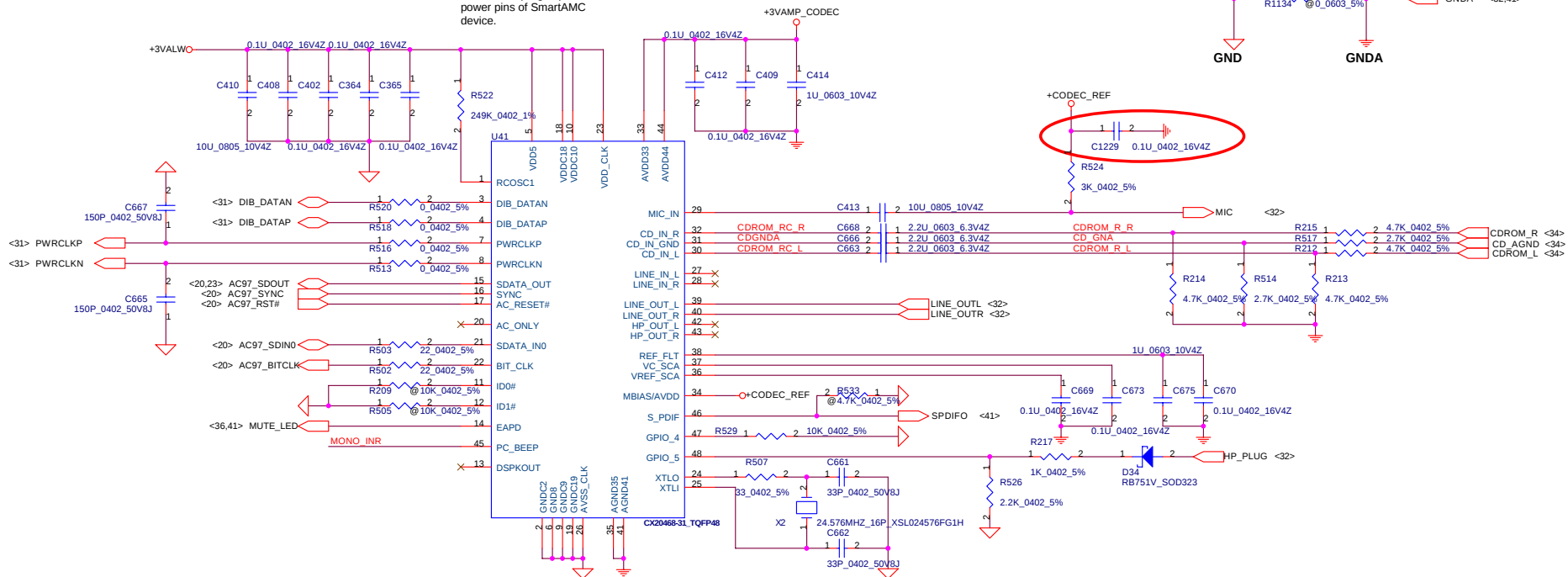
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Title			
IEEE 1394 CONTROLLER			
Size	Document Number		Rev
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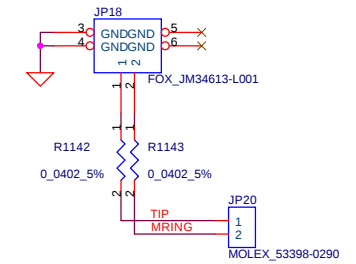
For Layout:
Place decoupling caps near the power pins of SmartAMC device.



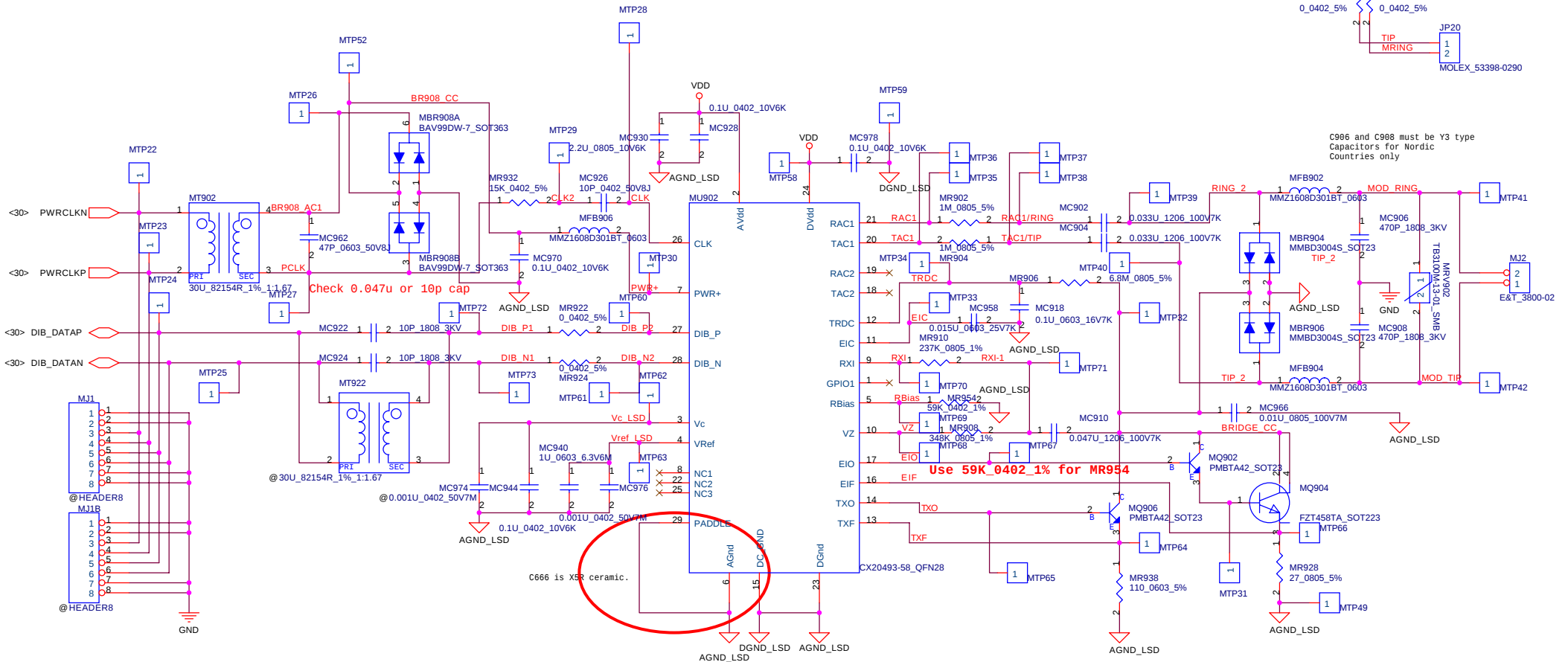
Compal Electronics, Inc.			
Title			
Code: CX20468-31			
Size	Document Number	Rev	
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RJ11 CONN.

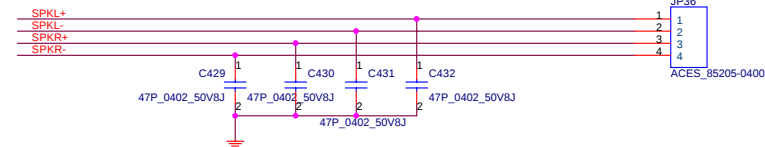
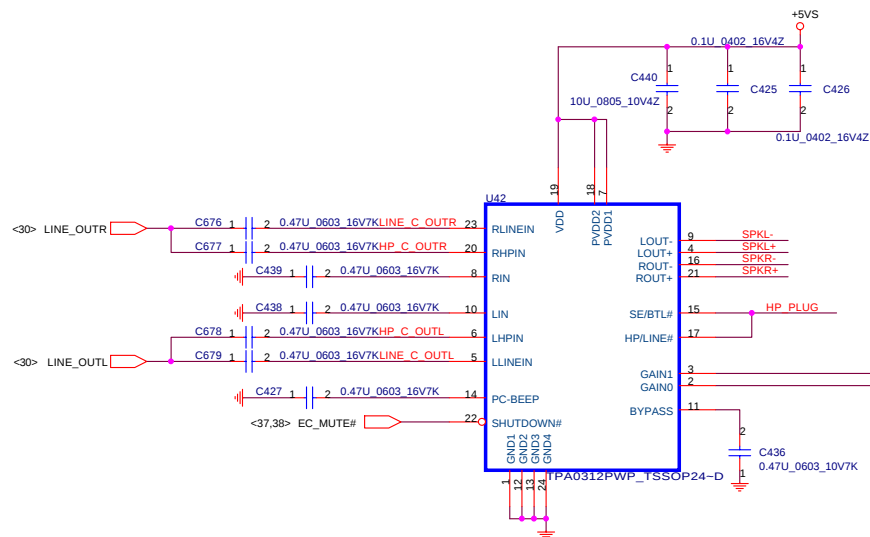


C996 and C998 must be Y3 type
Capacitors for Nordic
Countries only



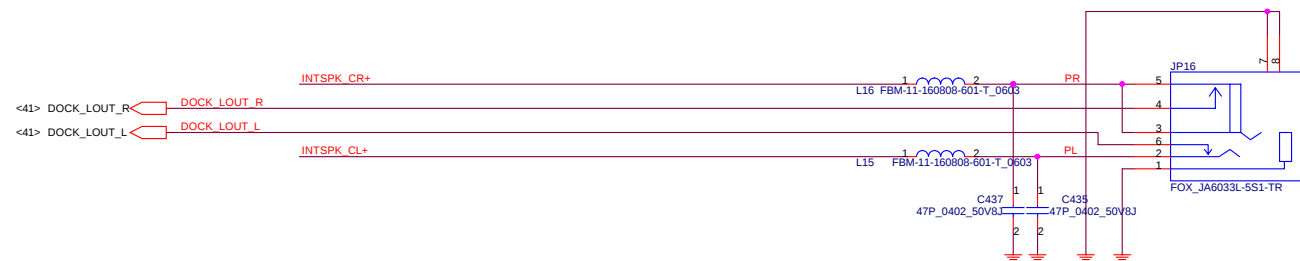
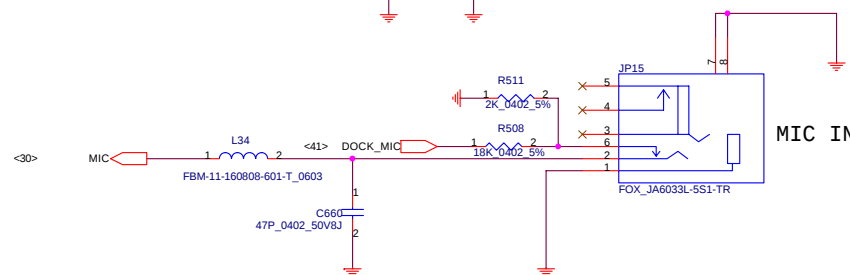
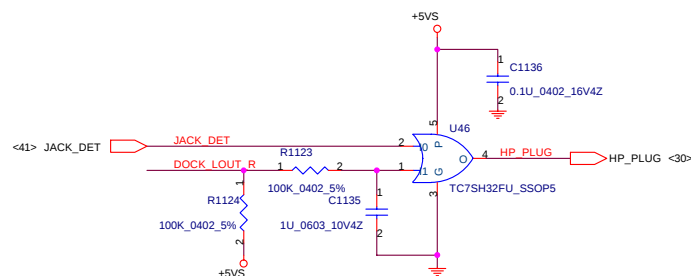
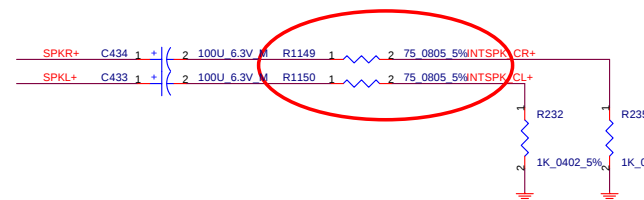
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Compal Electronics, Inc.			
Title			
AMOM_modem			
Size	Document Number	Rev	
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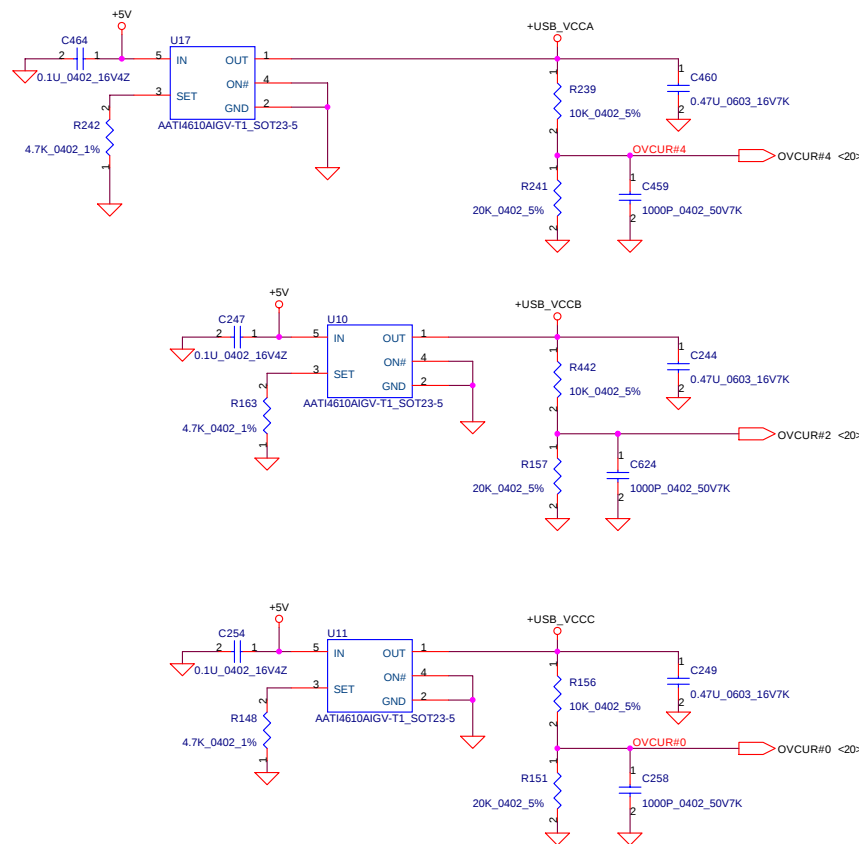
Gain Settings			
GAIN0	GAIN1	SE/BTL#	Av(inv)
0	0	0	6 dB
0	1	0	* 10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

HEADPHONE OUT/LINE OUT



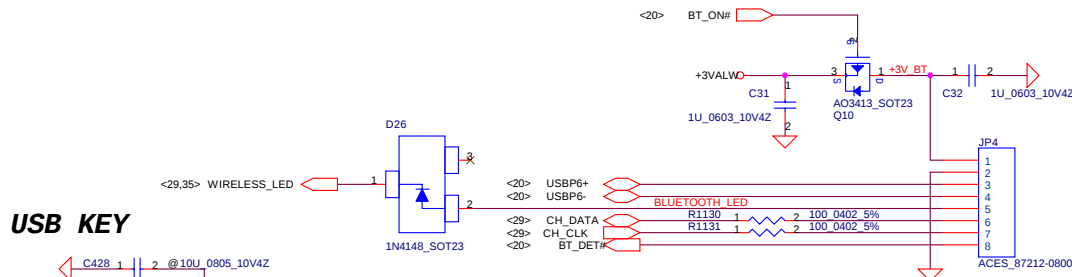
Compal Electronics, Inc.			
Title			
AMP & Audio Jack			
Size	Document Number	Rev	
Custom	LA-2421	0.6	
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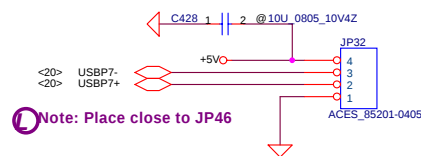


Note: PLACE CLOSE TO EACH USB PORT

BT CONNECTOR

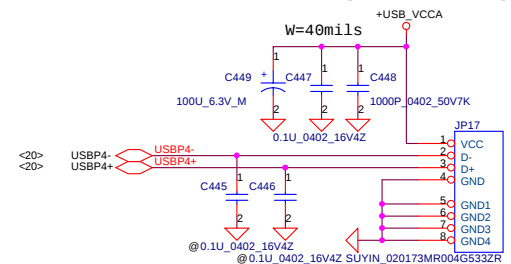


USB KEY

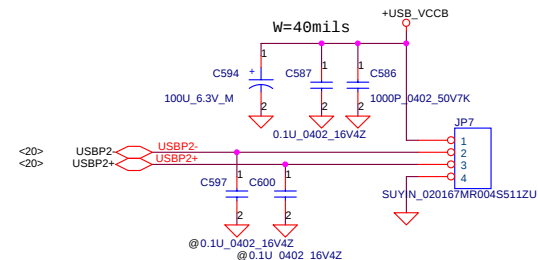


Note: Place close to JP46

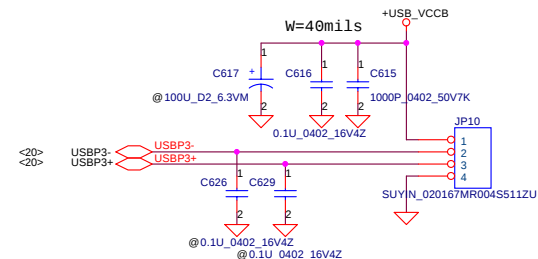
USB CONNECTOR 1(Rear side)



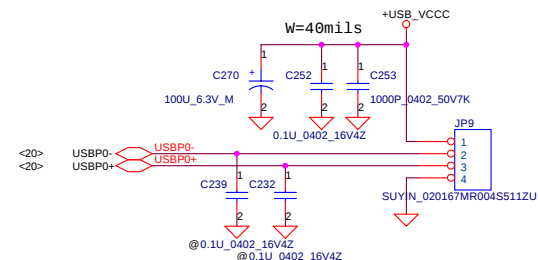
USB CONNECTOR 2(Left side)



USB CONNECTOR 3(Left side)



USB CONNECTOR 4(Right side)



Compal Electronics, Inc.

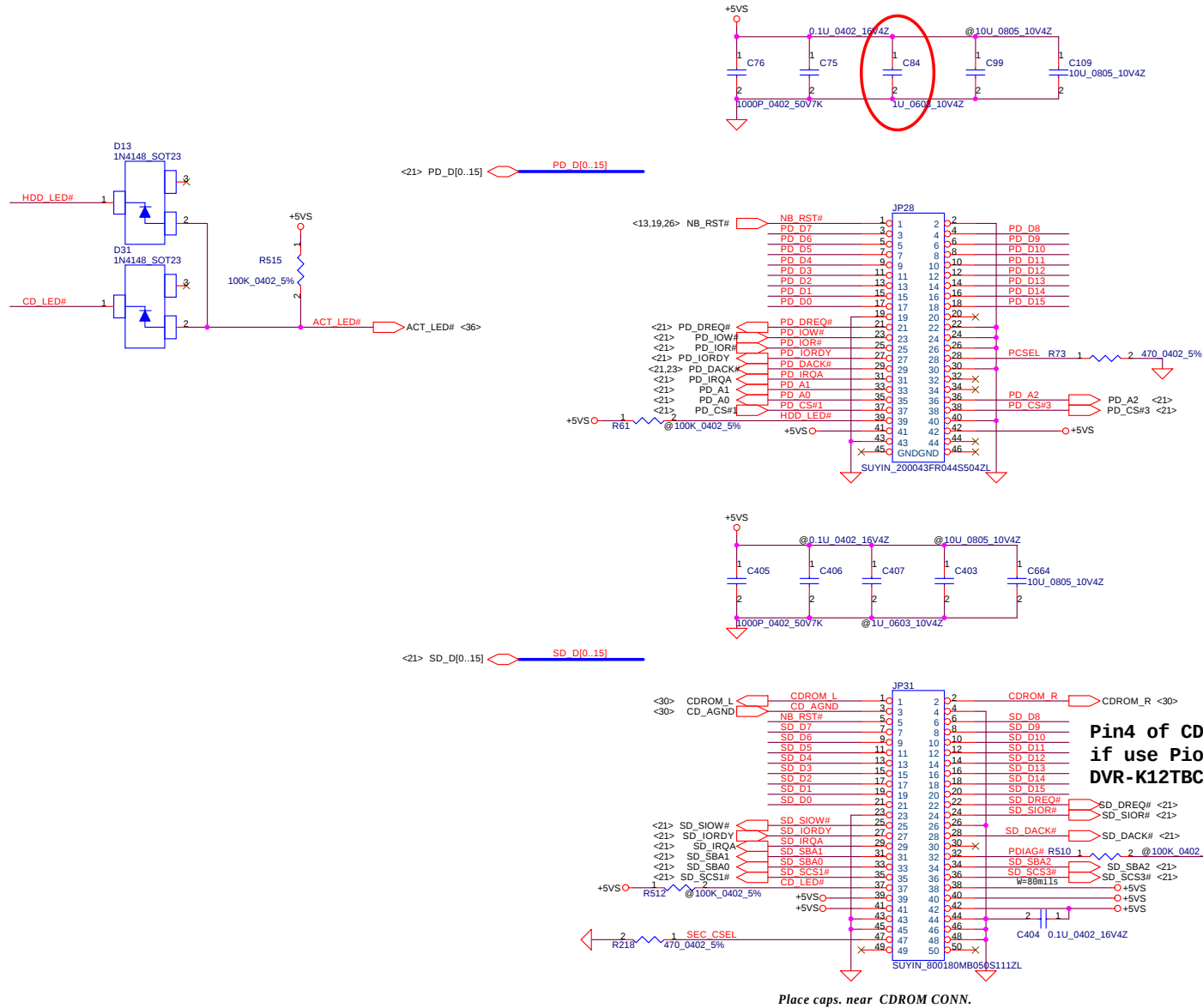
Bluetooth & USB CONN.

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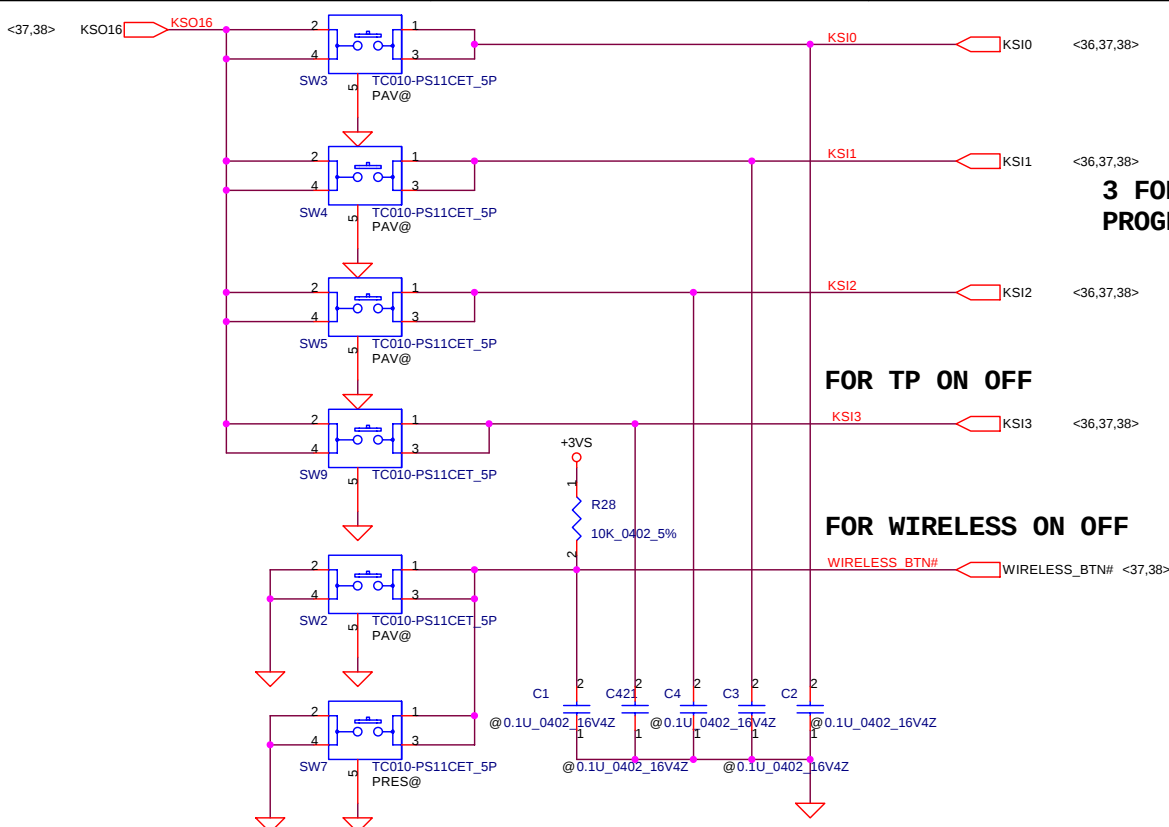
Place caps. near HDD CONN.

HDD/CD-ROM Module



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Compal Electronics, Inc.			
HDD & CDROM Connector			
Title	Size	Document Number	Rev
		L.A-2421	0.6
Date:	Wednesday, January 05, 2005	Sheet	34 of 56

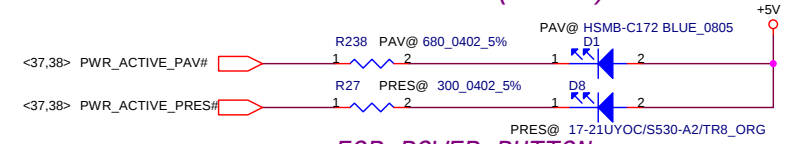


3 FOR PROGRAMMING

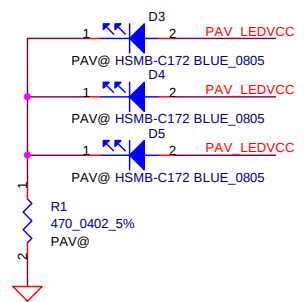
FOR TP ON OFF

FOR WIRELESS ON OFF

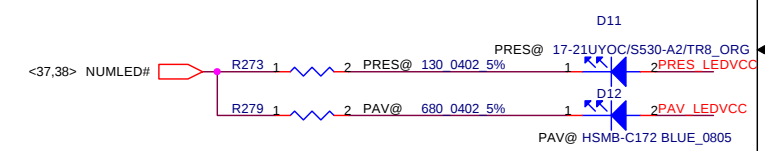
FOR POWER BUTTON BACKLIGHT (PAV)



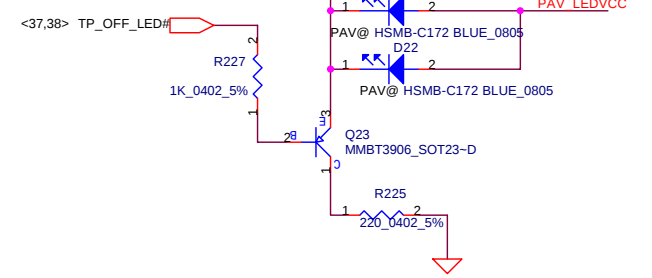
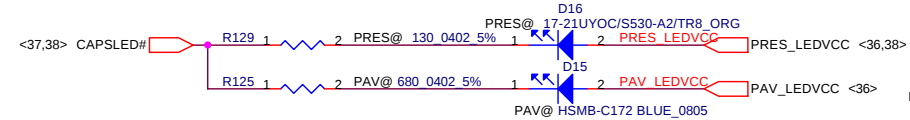
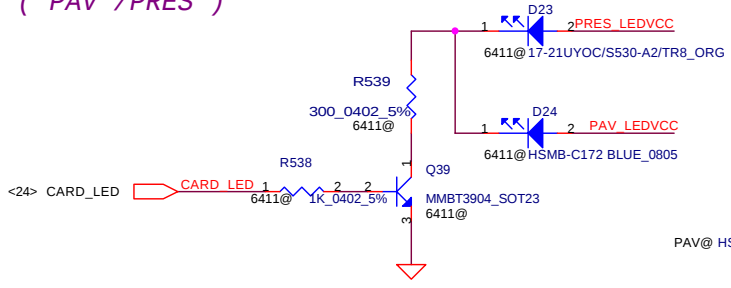
FOR POWER BUTTON BACKLIGHT (PRES)



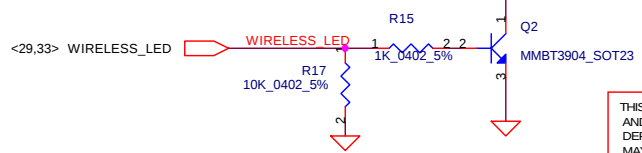
FOR 3 PROGRAMING BUTTON BACKLIGHT (PAV)



FOR CARDREADER INDICATOR (PAV /PRES)



FOR WIRLESS LED



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Title			
LED INDICATOR			
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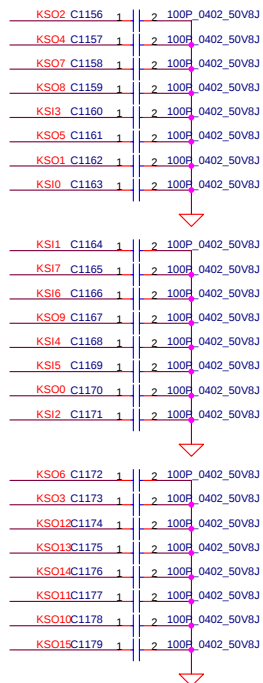


Diagram illustrating the pin connections for the LPC1114 microcontroller. The pins are numbered 1 through 20 on the left. Power pins are connected to +5V and +3V3. Signal pins are connected to various components:

- Pins 6-9: LPC_AD[0..3]
- Pin 10: LPC_FRAME#
- Pin 12: LDRQ0#
- Pin 13: PCI_RST#
- Pin 15: CLK_PCI_SIO
- Pin 16: SIRQ

A 10K 0402 5% resistor is connected between pins 14 and 15. The bottom left corner contains the text "@ ACES_85201-2005".

The schematic diagram illustrates the power management section of the TDA19841, specifically the connection of the EC power switch, the EC power MOSFET, the EC power diode, and the EC power inductor.

EC Power Switch: The switch is controlled by the **ON/OFFBTN#** signal. It is connected to the **ON/OFF#** signal, which is also connected to the **ON/OFF#** signal. The switch is connected to the **ON/OFF#** signal, which is also connected to the **ON/OFF#** signal.

EC Power MOSFET: The MOSFET is controlled by the **ON/OFFBTN#** signal. It is connected to the **ON/OFF#** signal, which is also connected to the **ON/OFF#** signal. The MOSFET is connected to the **ON/OFF#** signal, which is also connected to the **ON/OFF#** signal.

EC Power Diode: The diode is connected to the **ON/OFF#** signal, which is also connected to the **ON/OFF#** signal. The diode is connected to the **ON/OFF#** signal, which is also connected to the **ON/OFF#** signal.

EC Power Inductor: The inductor is connected to the **ON/OFF#** signal, which is also connected to the **ON/OFF#** signal. The inductor is connected to the **ON/OFF#** signal, which is also connected to the **ON/OFF#** signal.

EC Power MOSFET: The MOSFET is controlled by the **ON/OFFBTN#** signal. It is connected to the **ON/OFF#** signal, which is also connected to the **ON/OFF#** signal. The MOSFET is connected to the **ON/OFF#** signal, which is also connected to the **ON/OFF#** signal.

EC Power Diode: The diode is connected to the **ON/OFF#** signal, which is also connected to the **ON/OFF#** signal. The diode is connected to the **ON/OFF#** signal, which is also connected to the **ON/OFF#** signal.

EC Power Inductor: The inductor is connected to the **ON/OFF#** signal, which is also connected to the **ON/OFF#** signal. The inductor is connected to the **ON/OFF#** signal, which is also connected to the **ON/OFF#** signal.

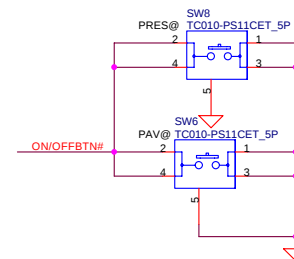
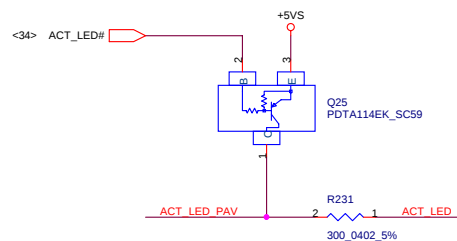
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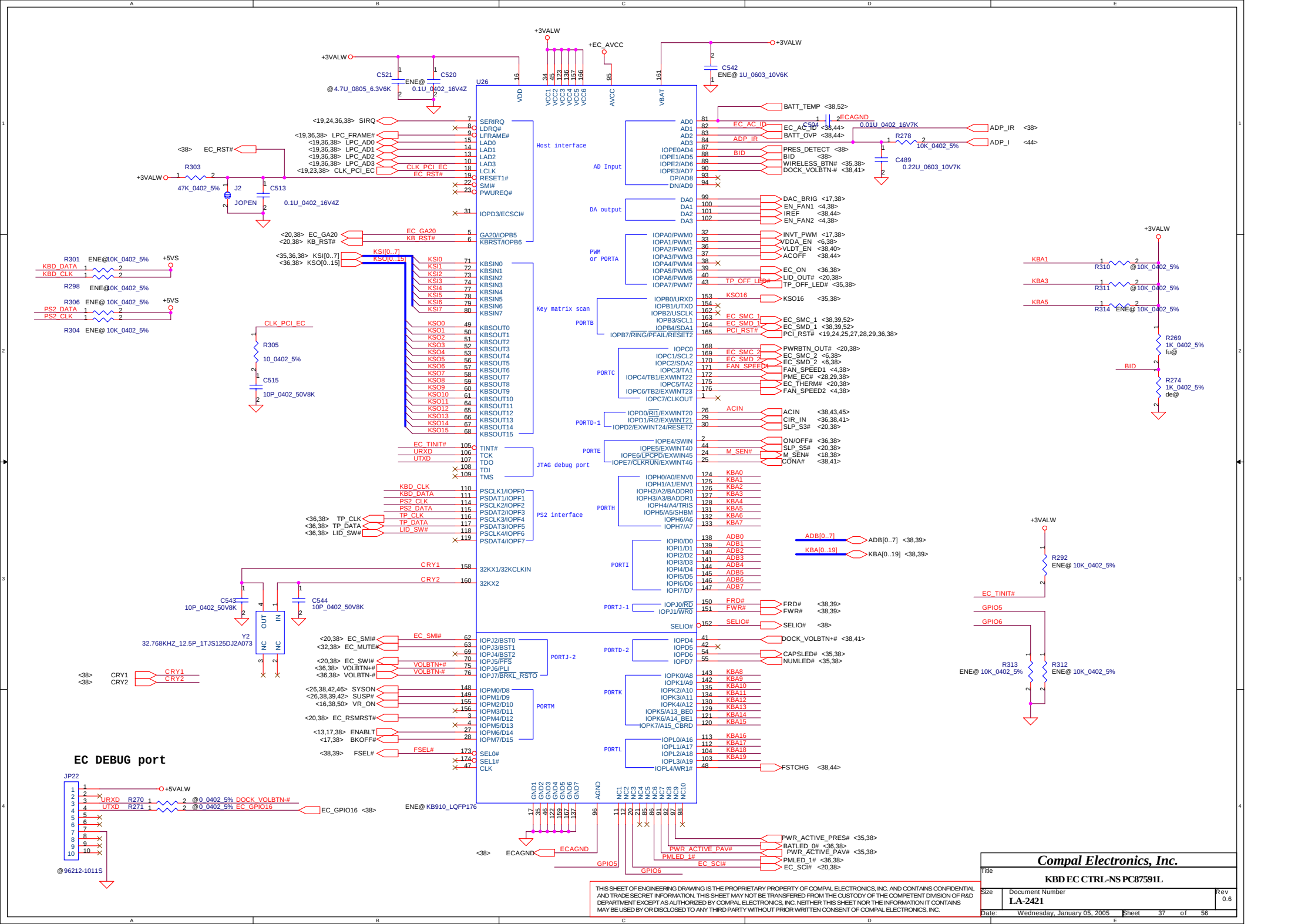
Diagram of the JP2 connector pinout. The connector is a 12-pin header. Pins 1, 3, 5, 7, 9, 11, and 12 are connected to +3VS. Pins 2, 4, 6, 8, 10, and 12 are connected to VOLBTN+ and VOLBTN- (indicated by an 'X' and a red line). Pins 10 and 11 are connected to MUTE_LED (indicated by a red line). The diagram is labeled 'JP2' at the top and 'ACES 85203-0602' at the bottom.

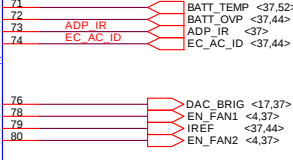
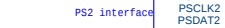
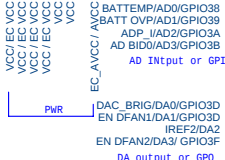
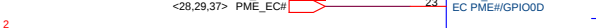
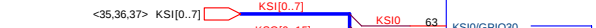
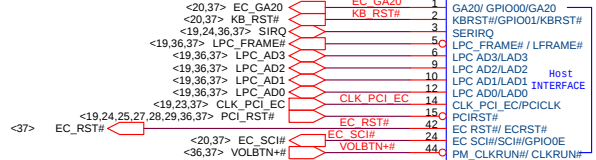
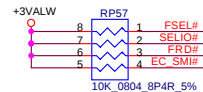
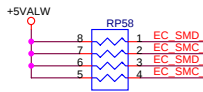
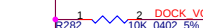
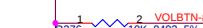
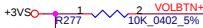
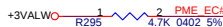
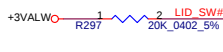
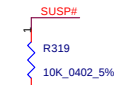
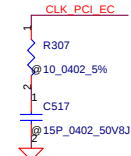
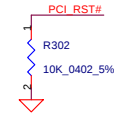
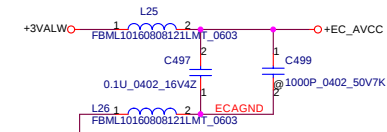
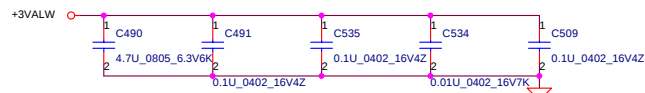
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Diagram illustrating the pin connections for the ACES 87152-0807 module. The module is connected to a 34-pin connector (JP34). The connections are as follows:

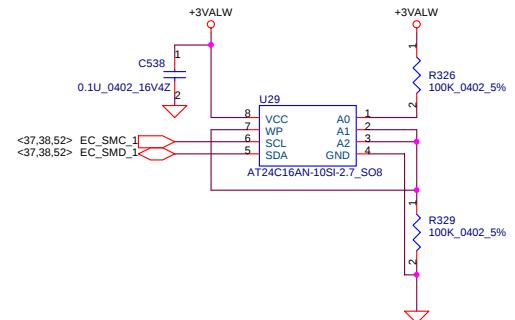
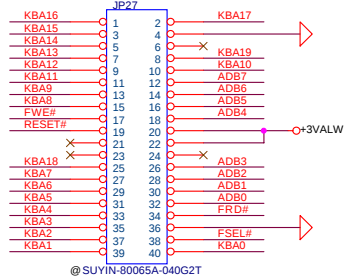
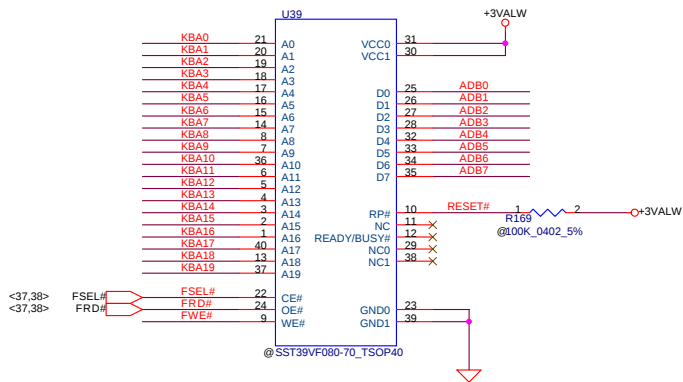
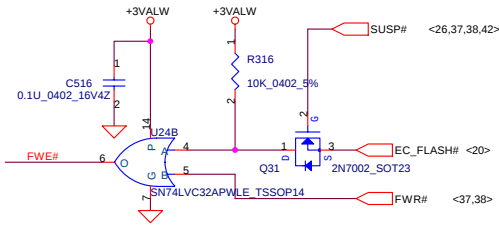
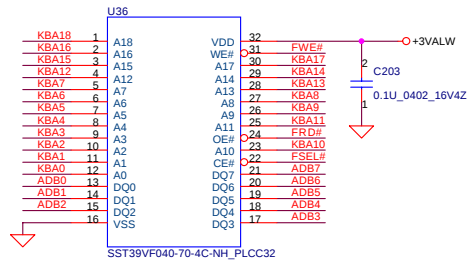
- Pin 8: +5V
- Pin 7: TP_DATA
- Pin 6: TP_CLK
- Pin 5: TP_DATA
- Pin 4: (Marked with an 'X')
- Pin 3: TP_CLK
- Pin 2: TP_DATA
- Pin 1: TP_CLK

ACES 87152-0807



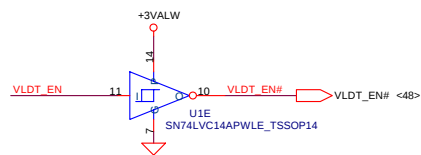
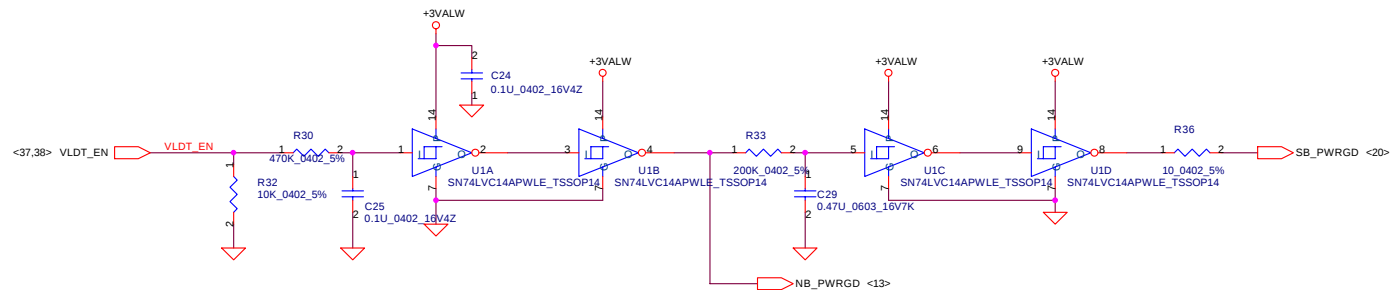


<37,38> ADB[0..7] ADB[0..7]
<37,38> KBA[0..19] KBA[0..19]

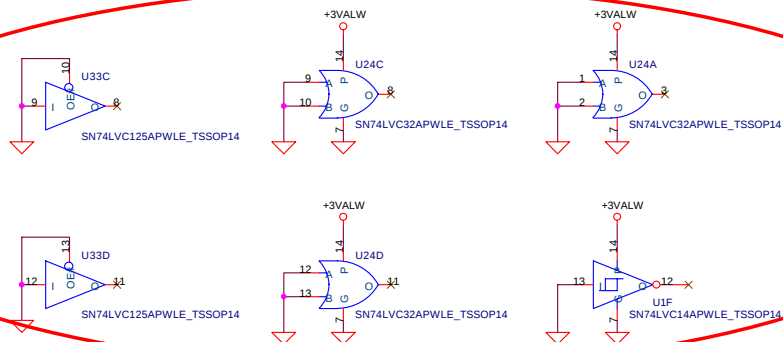
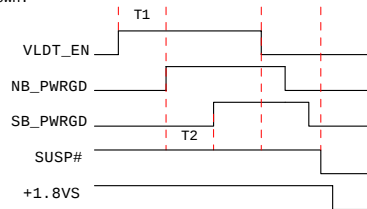


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BIOS & EC I/O Port			
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note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,
SUSP# goes to low after SB_PWRGD goes to low for power
down.

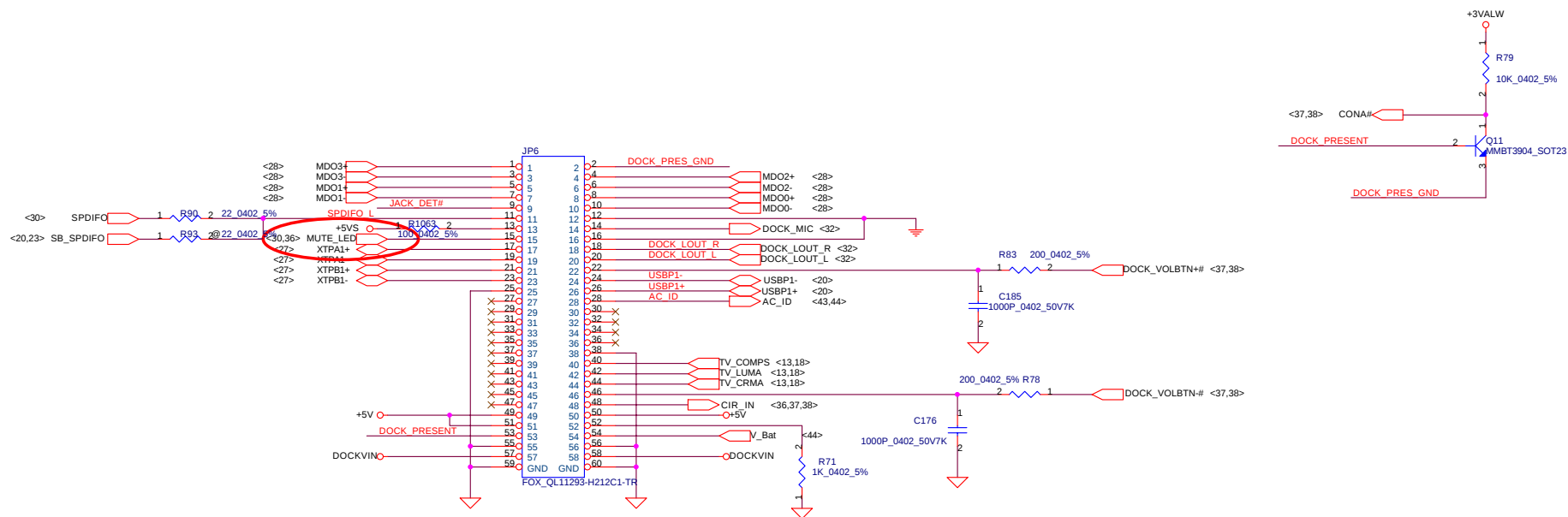


Compal Electronics, Inc.

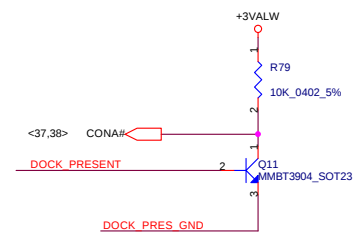
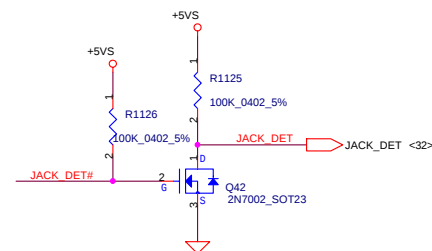
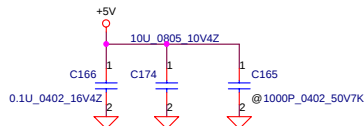
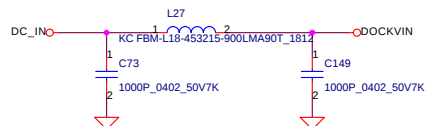
Power OK/Reset Conn.& MUTE Switch

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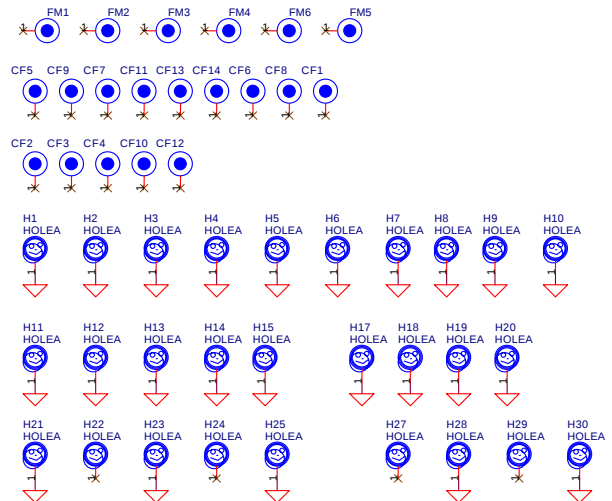
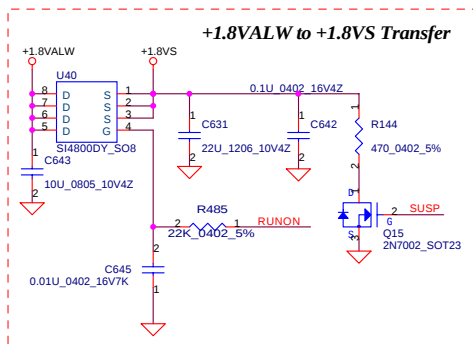
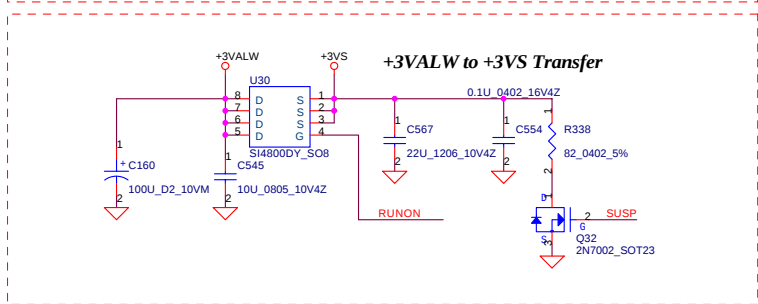
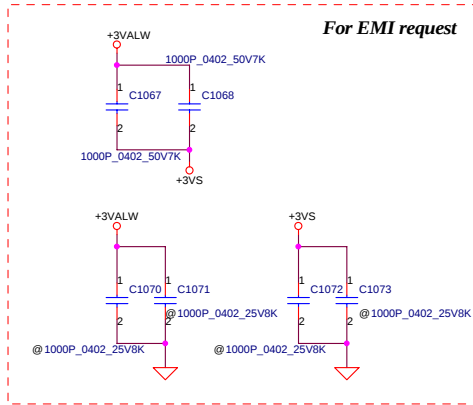
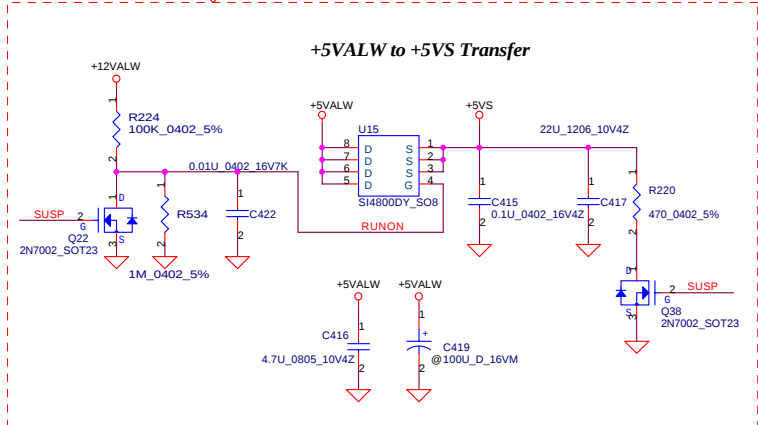
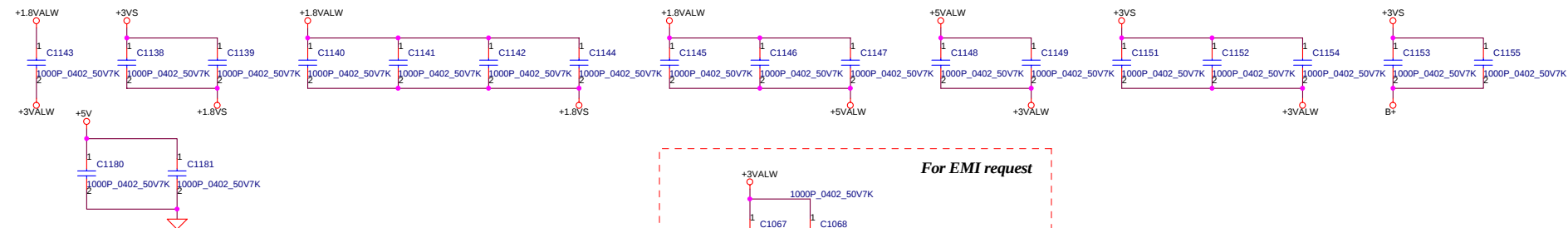
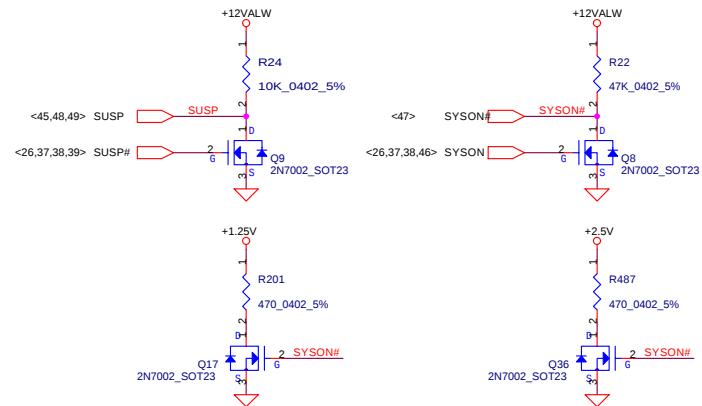
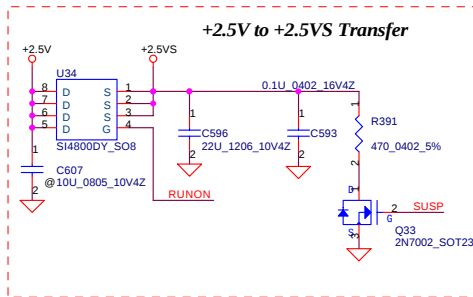
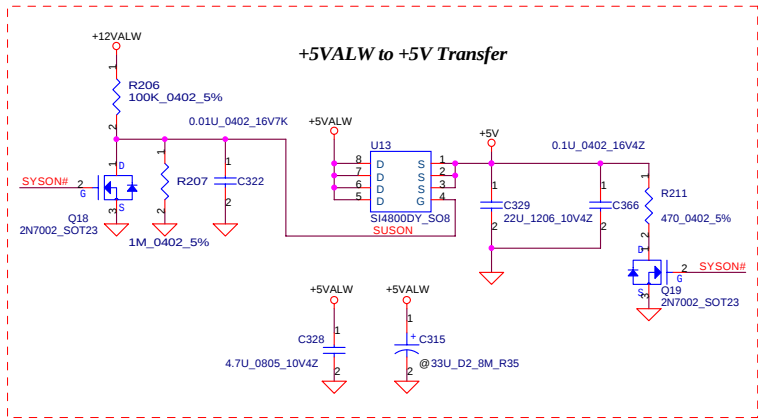


Note: PLACE CLOSE TO SPR PORT (JP33)



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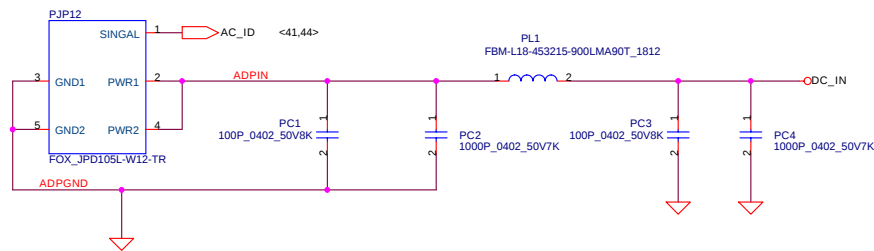
Compal Electronics, Inc.			
SPR Connector			
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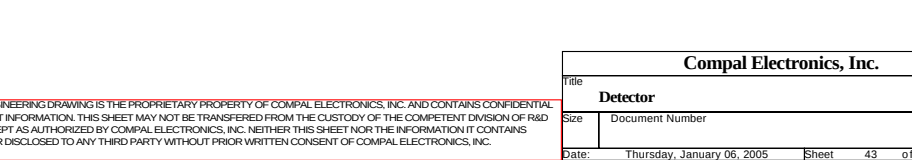
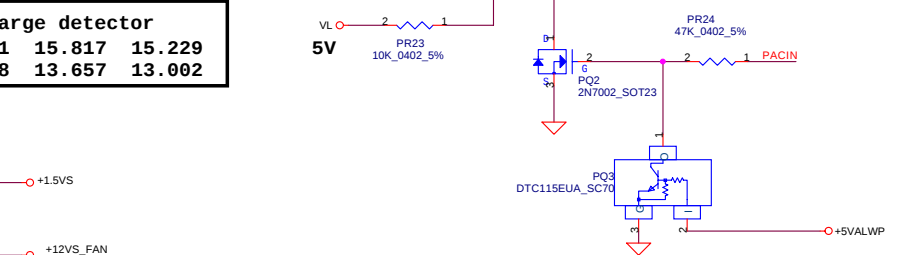
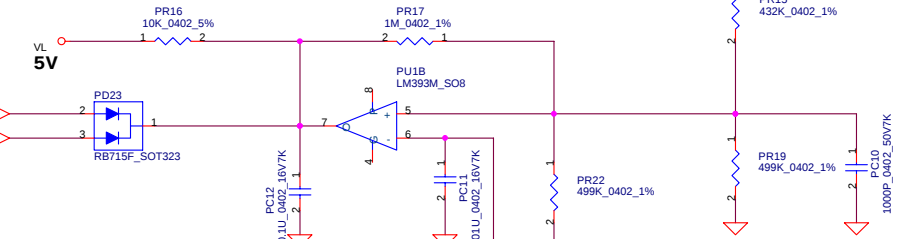
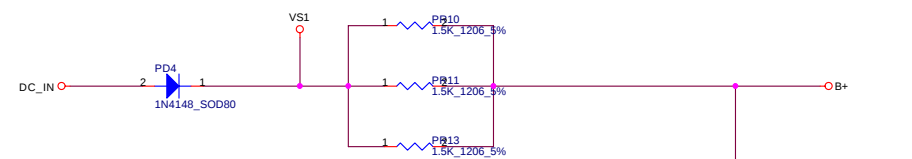
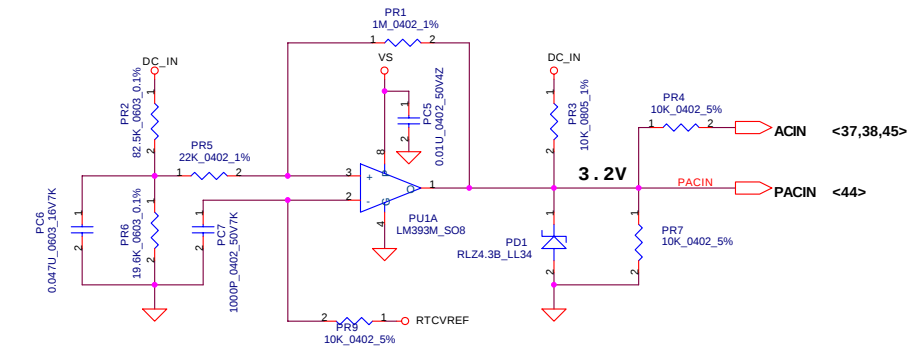
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DC/DC Circuit		
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Detector

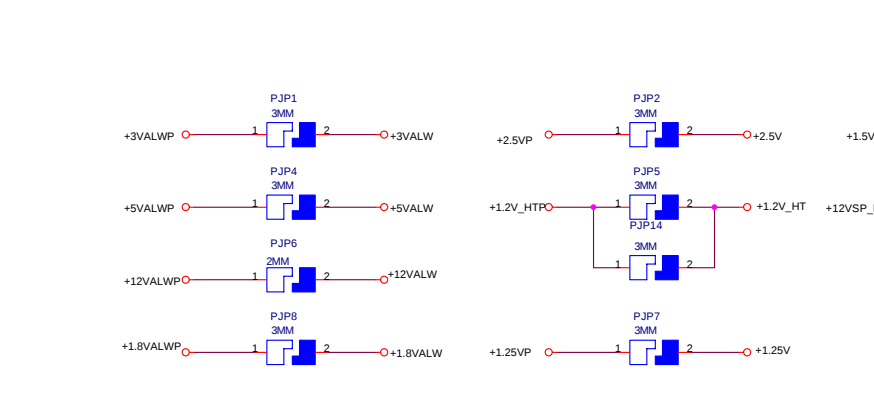
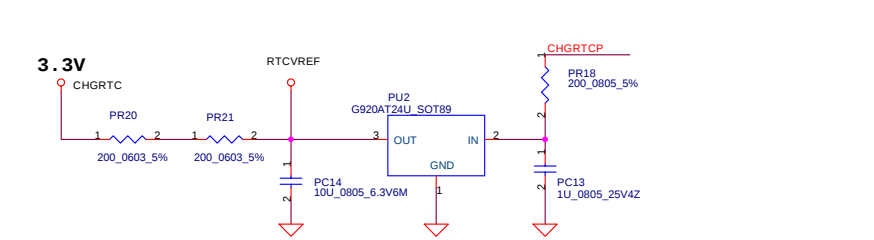
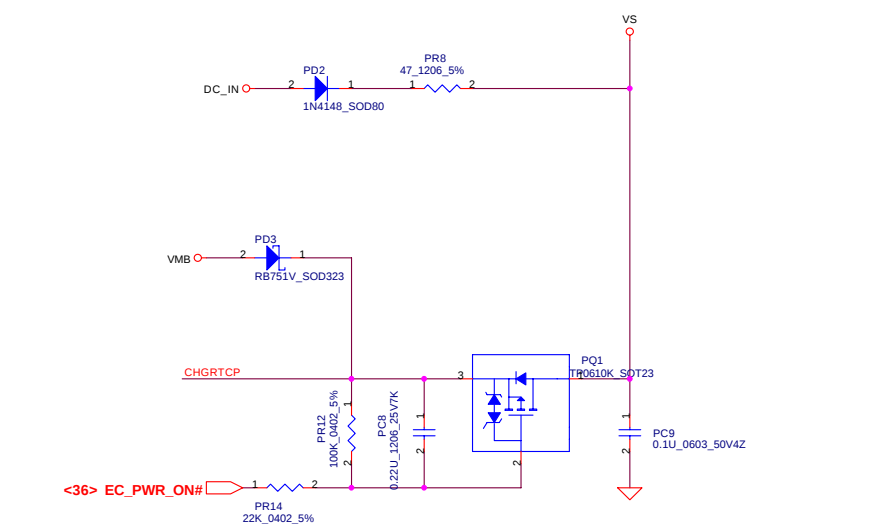


Vin Detector
 18.202 17.841 17.481
 17.568 17.210 16.858

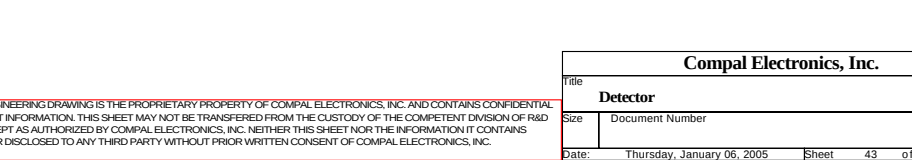
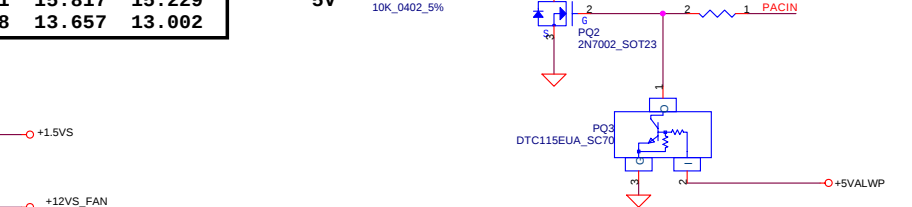


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Detector			
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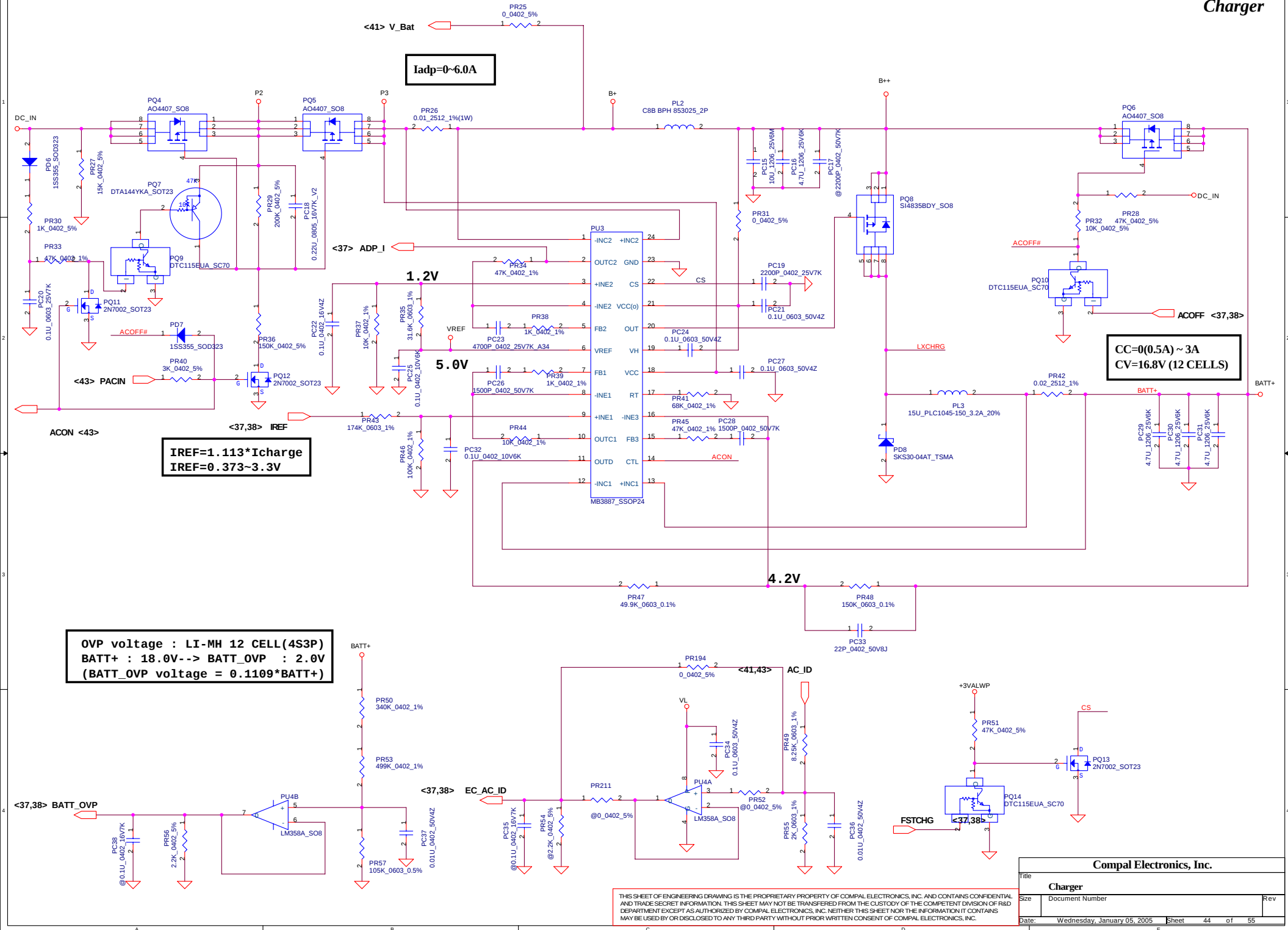
ACIN
 Precharge detector
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 14.108 13.657 13.002



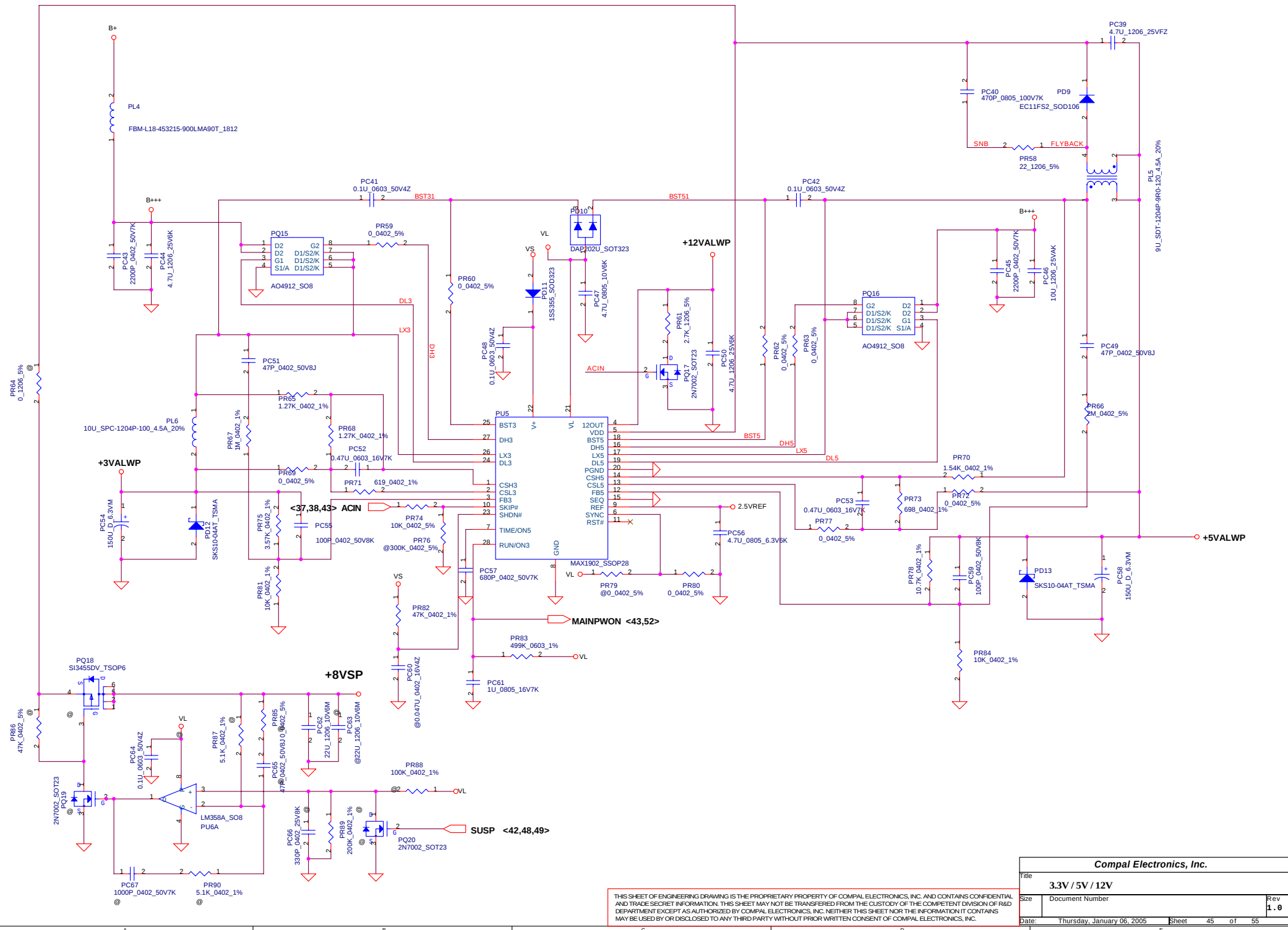
Compal Electronics, Inc.			
Detector			
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Charger

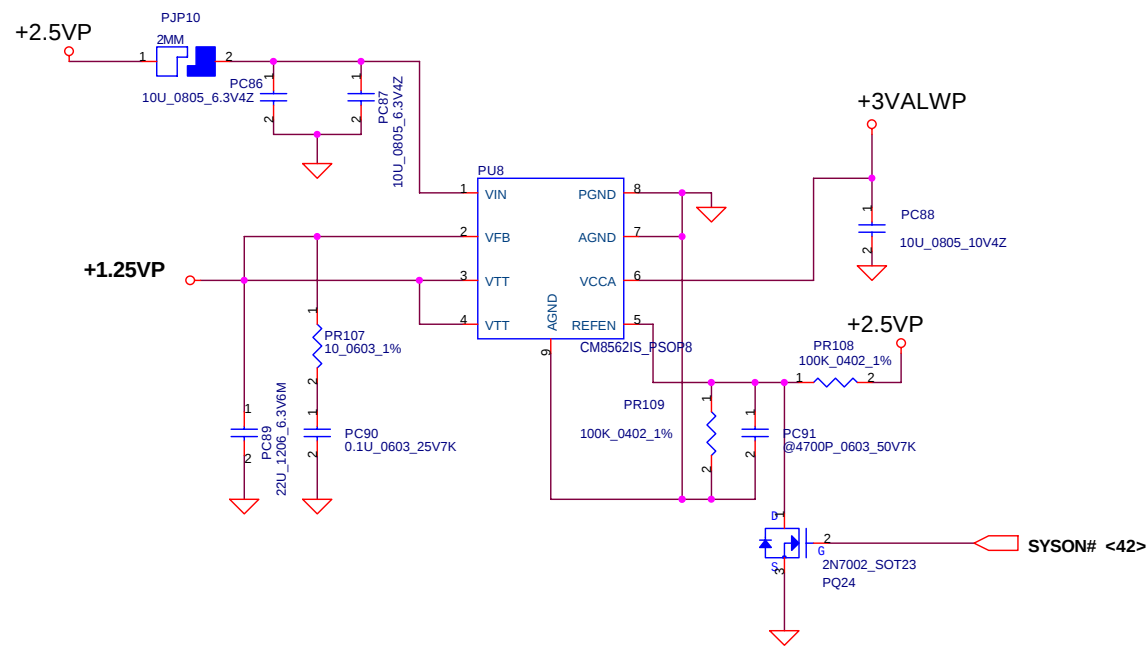


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Charger			
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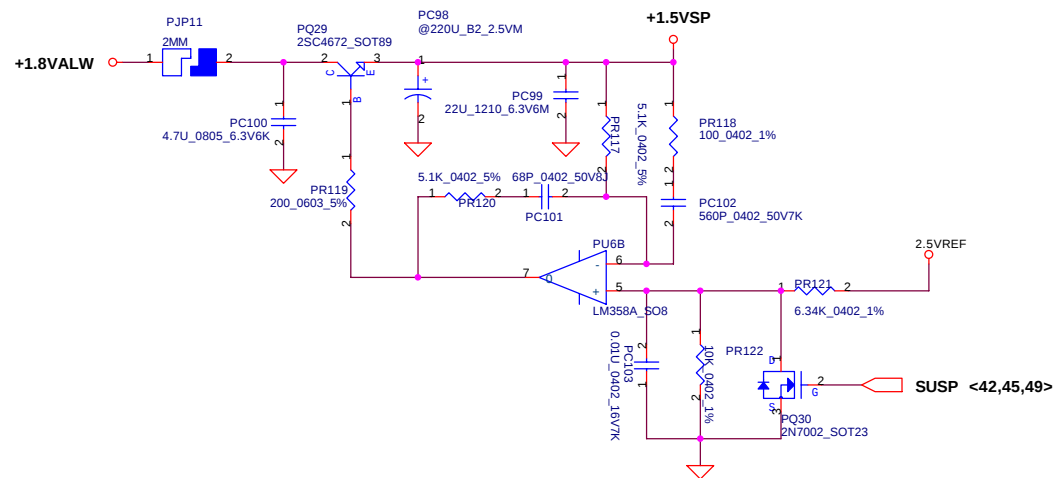
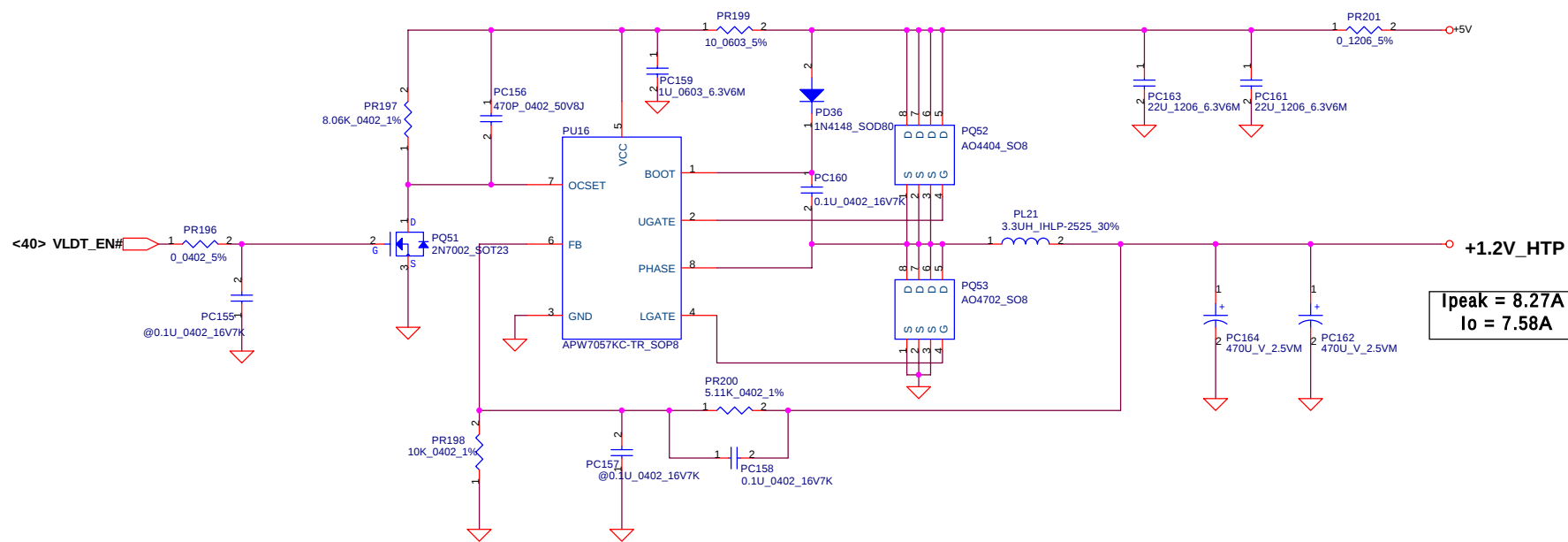
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3.3V / 5V / 12V			
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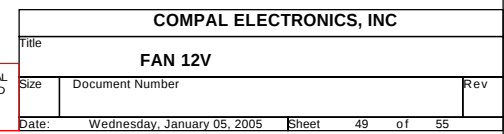
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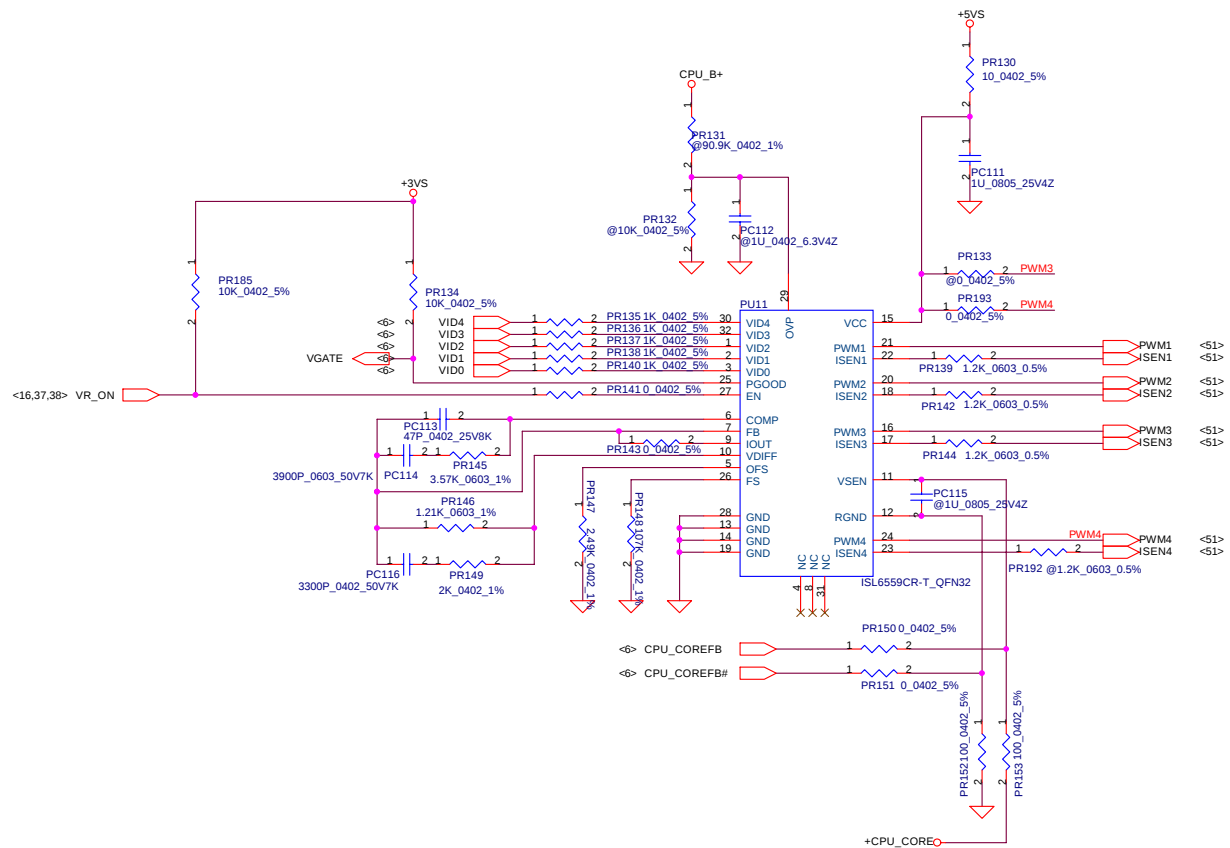


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1.2V_HTP / +1.5VSP		
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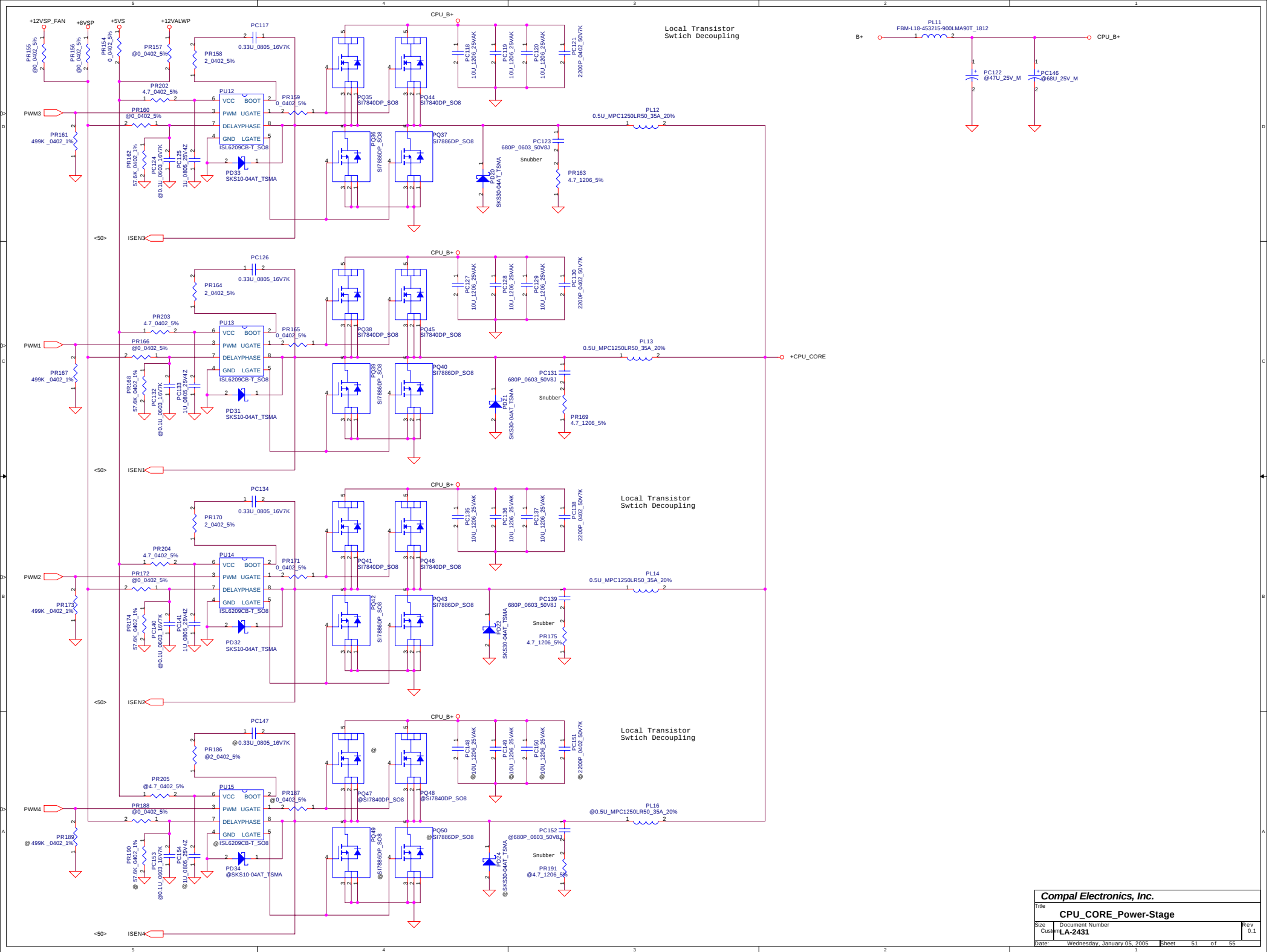


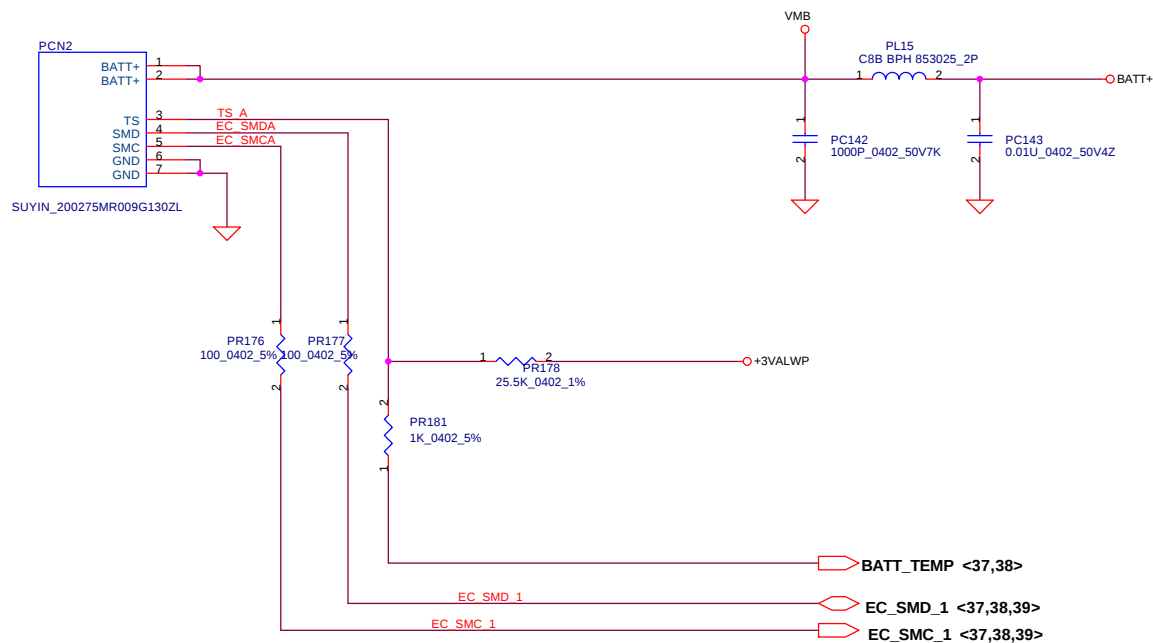
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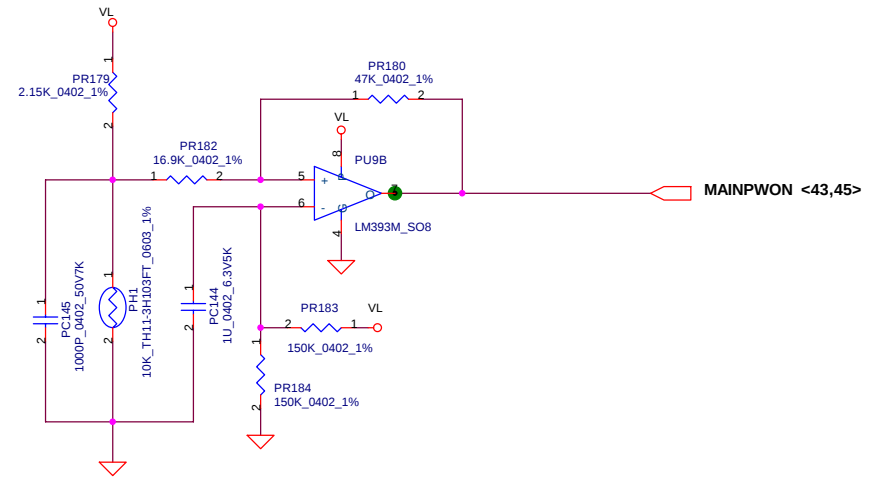
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+CPU_CORE			
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PH2 near main Battery CONN :
 BAT. thermal protection at 84 degree C
 Recovery at 45 degree C



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BATTERY CONN / OTP			
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4

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2

1

POWER PIR LIST

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4

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2

1

PIR LIST
Pre-DB

2004/6/05
1.page16 add R541/R542/R543/R544 and net NBSRCCLK_R/ NBSRCCLK/ NBSRCCLK#_R/ NBSRCCLK#.
2.page13 add net NBSRCCLK/NBSRCCLK#.
3.page13 change R85 pin2 from +2.5VS to +2.5V.
4.page14 add D33.
5.page19 del D18 and remove C265 to U38 pinA2.

2004/6/08
1.page13 del R82 change net name from SUS_STAT# to NB_SUSSTAT#.

2004/6/19
1.page19 Change U32,C584,R389 to @.
2.page23 Change R460 to @ and Add R464.

2004/6/25
1.page40 Change R30 from 10K_0402 to 340K_0402_1%.
2.Page4/6 change C18, C28 to SF10001M100 ELE CAP 100U 6.3V M B (6.3X6.0) CV-AX.
3.Page19 Add JP37, del BATT1

2004/6/28
1.Page26 Change U2 from R5535 to TPS2231.
2.Page26 Change C485/C487 to 4.8U_0805,change C486 to 10U_0805.
3.Page26 Change C503/C494 to 10U_0805,C492 to 4.7U_0805.
4.Page26 Del R268,Add Q40 2N7002.

Update for DB2

1.page34 change IDE Resistor from 0402 to 8P4R.
4.page27 change DOCK@ to 1394@.
5.ME update connector check and sub-board connector change to hot bar.
6.change 470U placement for +1.25V.
7.page40 change R33 from 0603 to 0402 type and R30 to 470k_0402_5%.
8. change C18, C28 to SF10001M100 ELE CAP 100U 6.3V M B (6.3X6.0) CV-AX.
9. change C318 to bottom side SF33001M100 ELE CAP 330U 6.3V M B (6.3X7.7) CV-AX
10. change C411 to bottom side SF47001M000 ELE CAP 470U 6.3V M B (10X10.5) CV-EX
11. change C325 to SGA19471D20.
13. change BATT1 to SP07S00080L(socket) + GC20323MX00(battery) (Page 19)
14. change new card power switch from RICOH to TI.
15. Remove PME_EC# from SB and pin C4 wire to EC_SWI#
16. Disconnect UTXD from U26.154
17. Page 23 update hardware strap for SB400 A21 (PA_IXP400AD1 & 105-A27800-00C R1.1)
18. Page 13 add EEPROM for NB to solve boot up intermittently
19. Page 23 strap select 14 MHz OSC mode, it is generated from NB to SB and delete 14 MHz crystal at SB
20. 1394 controller change to TI
21. Update PIRQ routing
22. X2 change size.
23. Cardbus controller change to TI
24. Fan circuit change to MOS
25. Change AMP to TPA0312 and add TC7SH32FU to solve HP_PLUGIN issue
26. Implement HP wireless/bluetooth control requirement. Change host to SB. (Page 20)
27. Change CRT connector JP19 (Page18)
28. Modify KB910L debug pin RXD=pin#35 & TXD=pin#34
29. No need PWR_BACK# from EC controller
30. DFX review: Change blue LED footprint to be same as amber LED footprint.
31. AC97 primary codec SDATA_IN0 should connect to SB's AC97_SDIN0 (Page 30)
32. R182 change to 11.8 k (Page 20)
33. Reserve D36, D37, and R1127 for XD detect issue. (Page24)
34. PCIE_PME# change to pin #D2 of SB. (Page 20)

35. WL_ON connect to pin #C5 of SB/ BT_ON# connect to pin #B5/ BT_DET# connect to pin #C8. (Page 20)
36. Add R1132 to ensure ENABLT is low during power up.(Page 13)
37. AGP_BUSY# and AGP_STP# pull up to solve shut down issue. (Page 20)
38. Delete R159 (OVCUR#3) and LID_OUT# change to GPM3# and add R1133 pull up S3_STATE to +3VALW (Page20)
39. Change all blue LED's footprint to LED_17-21UY0C-S530-A2-TR8_2P
40. Change R532 to 0603 size and add R1134 (Page 30)
41. Add AC-caps for PCI and LPC bus turn path. (Page 42)
42. Delete R541, R542, R543 and R544. (Page 16)

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Update for SI

1. Applying CLK_STOP of ICS951418. (Page 16)
2. R176 change to 4.12k 1% (page 19)
3. Add pull down resistor for SYSON (R1135) and SUSP# (R319), due to TPS2231 internal pull-up when +3VALW present, EC can not control at the first 10 ms.
4. Reverse JP33 and JP34
5. TI CardReader workaround: add Q44, R1137, D38, and D39 to prevent signal output earlier than power up (page 24)
7. MU902's pin29 connect to AGND_LSD (page 31)
9. Change C621, C619, C628, and C625 to 0.01U from 0.1U (page 19)
10. DDR change to single channel from dual channel.
11. Swap pin40 and 44 of docking connector (JP6) for TV-out signal. (page 41)
12. Update from ATi AP used note of SB, unused SATA pins connect to GND. (page21).
13. Reserve R1138 for XD_WP# pin at socket side. (page 24)
14. Reserve U47 to generate independent +1.9VS to PCIE_PVDD and PCIE_VDDR. (page 19)
15. For KB910L, pin #94 is for DOCK_VOLBTN+# and pin #34 is for EC_GPI016. (page 38)
16. Add R1141 on SUS_STAT# per ATi recommend. (page 13)
17. PR110 connect to +5V due to +3VS too dirty that will cause TV display garbage. (page 48)
18. Update PCIE connector (JP5) pin defined of #7, #8, and #9 and reserve backward compatible due to there are two different version of NewCard spec. (page 26)
19. GPP_RX0N/P connect to JP5.21/22 and PCIE_TX0N/P connect to JP5.24/25 (page 26)
20. Reserve D40 and D41 for NewCard hot-plug detected. (page 26)
21. Adjust AMP output to 10 dB: Add R237/R233, delete R236/R234. (page 32)
22. Change CP1 ~ CP6 to C1156 ~ C1179 due to cost saving. (page 36)
23. Add C1180 and C1181 for EMI requirement. (page 42)
24. Add C160 due to +3VS unstable. (page 42)
25. R1121 change to 0_0402_5% per TI recommend (page 24)

Update for SI-R (Rev 0.4)

1. DDR_SDM_L2 length mismatch (page 9)
2. Add U48 (TPS2211A) for PCI1510RGVF (page 25)
3. NC_CP# connects to U38.D3 for New Card hot-plug (page 20)
4. R51 and R77 change from 49.9_0402_1% to 61.9_0402_1% (page 11)
5. Change C621, C619, C628, and C625 to 0.1U from 0.01U --- ATi final decision for SB A22 RP03 and future (page 19)
6. Q25 change from MMBT3906 to PDTA114EK and R228 change to 0_0402_5% due to Hitach HDD LED will not be turn off light. (page 36)

Update for SI-2 (Rev 0.4B)

1. Remove C27 due to Sempron CPU intermittent boot-up issue. (page 6)
2. Change Q39 to MMBT3904 due to CARD_LED is high active signal. (page 35)
3. D40 and D41 replace by R1146 and R1148 due to TPS2231 truth table treat both CPUUSB# andCPPE# as the same. (page 26)
4. R87 change to 8.06k_1% due to New Card eye-diagram issue. (page 12)

Update for PV (Rev 0.5)

1. Add R1149 and R1150 for headphone gain degrading. (page 32)
2. Modify AVDDTX and AVDDRXL layout to improve USB signal quality.
3. Change wireless LED power from +5V to +5VS (page 35)
4. Follow TI layout guideline.
5. Change R1099 and R1100 to 2.2k per TI recommend for XD certification. (page 24)
6. Change LAN LED indicator color, Green is for link and Amber is for activity. (page 28)
7. Change R34, R35 and R259 from 1k to 680 base on AMD design guide. (page 6)
8. Change R286, R290, R473, and R486 from 100 to 15 base on AMD recommendation. (page 5/ 9)
9. Reserve C1182 at NB VDD_CORE and change C161 ~ C164, C136 ~C138, C153, C154, C156, C157 from 0.1uF to 1uF due to +1.2V_HT is not stable and clean. (page 14)
10. Delete R1083 due to SM card detect issue (quick or slow). (page 24)
11. Add C1183 ~ C1220, 1000pF or 220pF, on +2.5V, +1.25V, +CPU_CORE, +3V_CLK, +3VS, and +1.2V_HT for EMI require. (page 7/ 10/ 14/ 16/ 22)
12. Change R155, R162, R441, R444, and R448 from 22 ohm to 33 ohm due to EMI require. (page 19)
13. Wire MUTE_LED to JP6.15 due to HP docking spec V0.8 update (page 41)
14. Add C1151 and C1152 to isolate GND and change C61 and C241 from 0.1uF to 1000pF for EMI. (page 4)
15. Add C1221 ~ C1226 on +2.5VS for EMI (page 15)
16. Reserve C1227 and C1228 on EDID_CLK/DAT for EMI. (page 17)
17. Remove R64, R65, R69, and R70 due to EMI. (page 5)
18. RTC battery change to CR2025 (165mAh) due to power consumption less than 5uA. (page 19)

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Update for PV-2 (Rev 0.6)

1. Delect R1138, wire WP# pins of XD and SM together (SM_EL_WP#) and series 3.3k ohm (R1082) to CLK per HP recommendation. (page 24)
2. Tie un-used inputs of U24 and U33 to GND. (page 40)
3. Delect all reserve 0 ohm resistors. (page 34)
4. Add C1229 for power (+CODEC_REF) stable on MIC_IN. (page 30)
5. R53 change to 91_0402_5% due to HT output from RS480 need to improve rising and falling time. (page 11)
6. Reserve R1153 ~ R1157 for SanDisk 256MB SD card overshoot and undershoot issue. (page 24)
7. De-feature mother board populate R274, and full-feature mother board populate R269 for 90W adapter protection. (page 37)

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