

Compal confidential

JBK00 LA-4093P Schematics Document

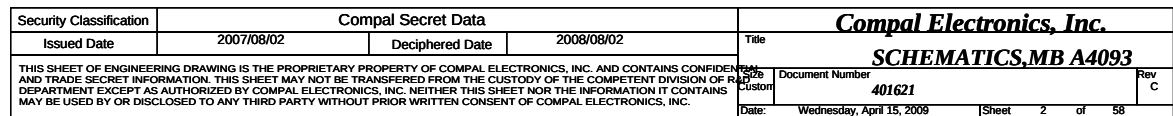
Mobile AMD S1G2 CPU with ATI
RX781 & SB700 core logic with M86-M

2009-03-25

REV:1.0

Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	SCHEMATICS,MB A4093	
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Consumer AMD Discrete 17"



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Voltage Rails

State \ power plane				+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
	+B +3VL +5VL	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V	
	S0	0	0	0
	S1	0	0	0
	S3	0	0	X
	S5 S4/AC	0	0	X
	S5 S4/ Battery only	0	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

0 MEANS ON X MEANS OFF

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0
ACCELEROMETER	3A	0 0 1 1 1 0 1 0

EC SM Bus1 address

EC SM Bus2 address

Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X b	ADI1032-2 CPU	9AH	1001 101X b
24C16	A0H	1010 000X b	ADI1032-1 VGA	98H	1001 100X b
CPU SIC interface	98H	1001 100X b			

Symbol Note :

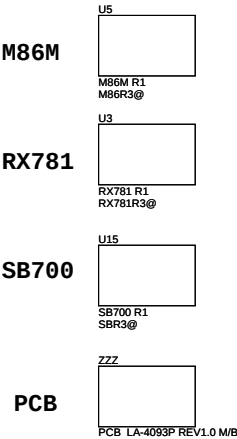
 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

Layout Notes

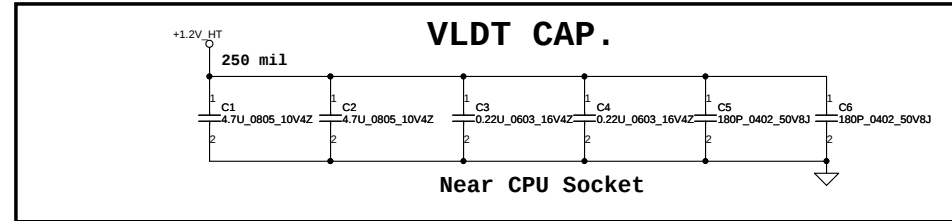
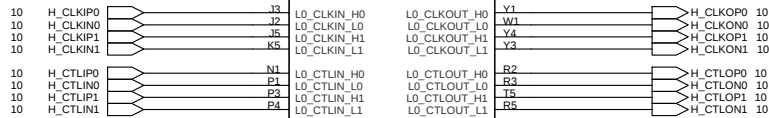
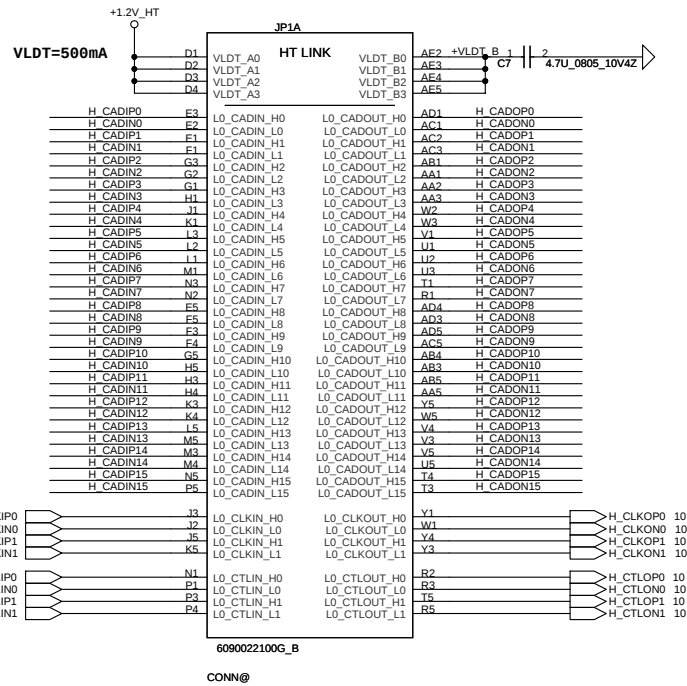
@ : means just reserve , no build
45@ : means need be mounted when 45 level assy or rework stage.
RX781R1@ : means just reserve for R1 FRU BOM
SBR1 @ : means just reserve for R1 FRU BOM
M86R1@ : means just reserve for R1 FRU BOM



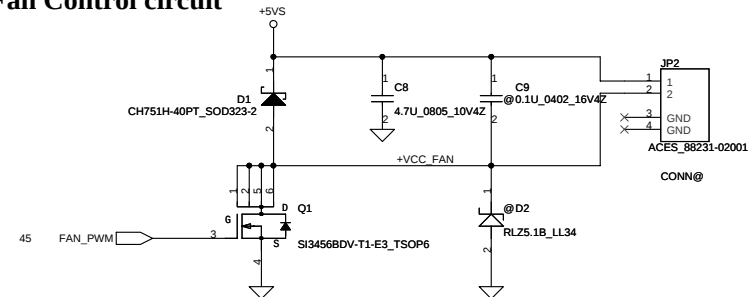
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR CPU & ADM1032	SODIMM I / II	CLK CHIP	MINI CARD Slot 2	LCD	HDMI	G-Sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X
I2C_CLK I2C_DATA	RS780M	X	X	X	X	X	X	X	V	X	X
DDC_CLK0 DDC_DATA0	RS780M	X	X	X	X	X	X	X	X	V	X
DDC_CLK1 DDC_DATA1	RS780M	X	X	X	X	X	X	X	X	X	X
SCL0 SDA0	SB700	X	X	X	X	V	V	X	X	X	V
SCL1 SDA1	SB700	X	X	X	X	X	X	V	X	X	X
SCL2 SDA2	SB700	X	X	X	X	X	X	X	X	X	X
SCL3 SDA3	SB700	X	X	X	X	X	X	X	X	X	X

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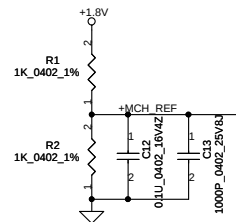


PWM Fan Control circuit

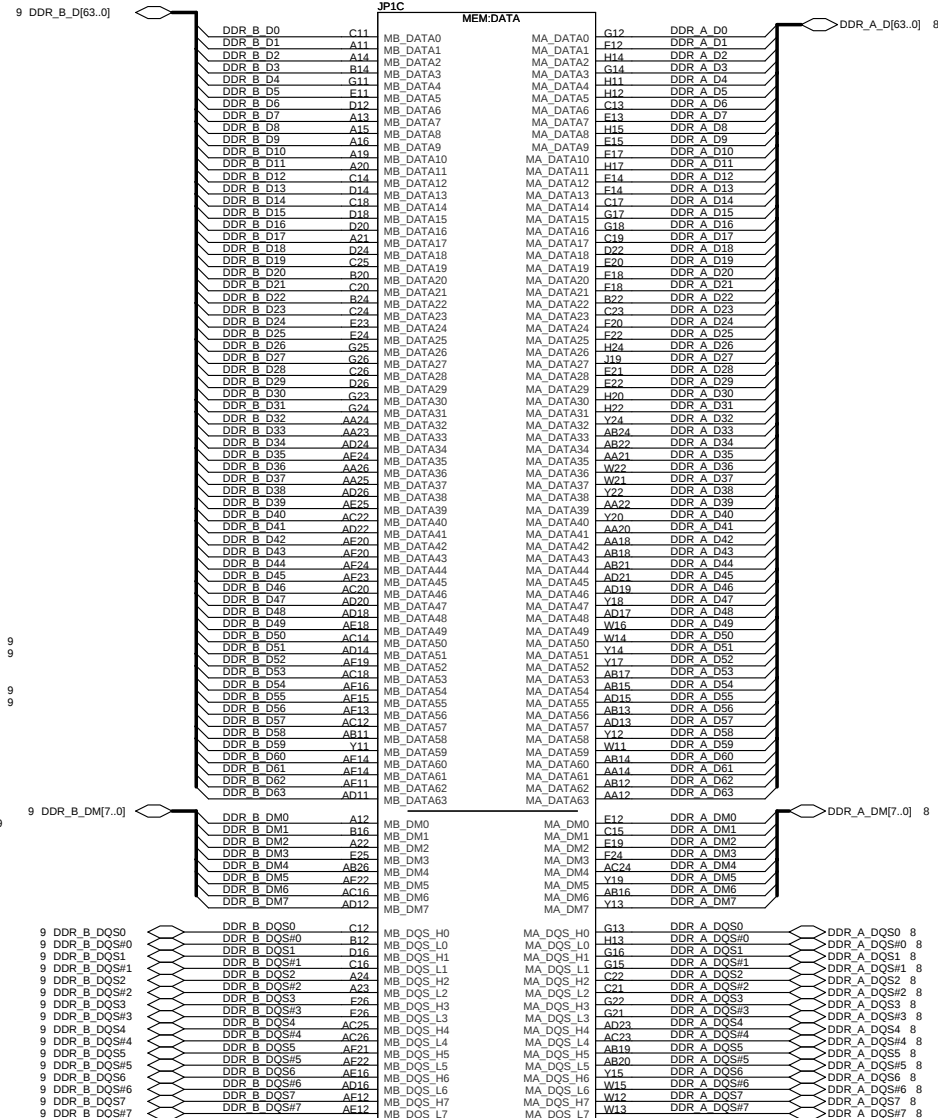
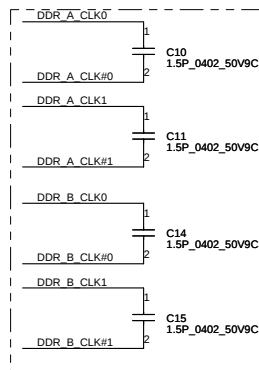


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Processor DDR2 Memory Interface



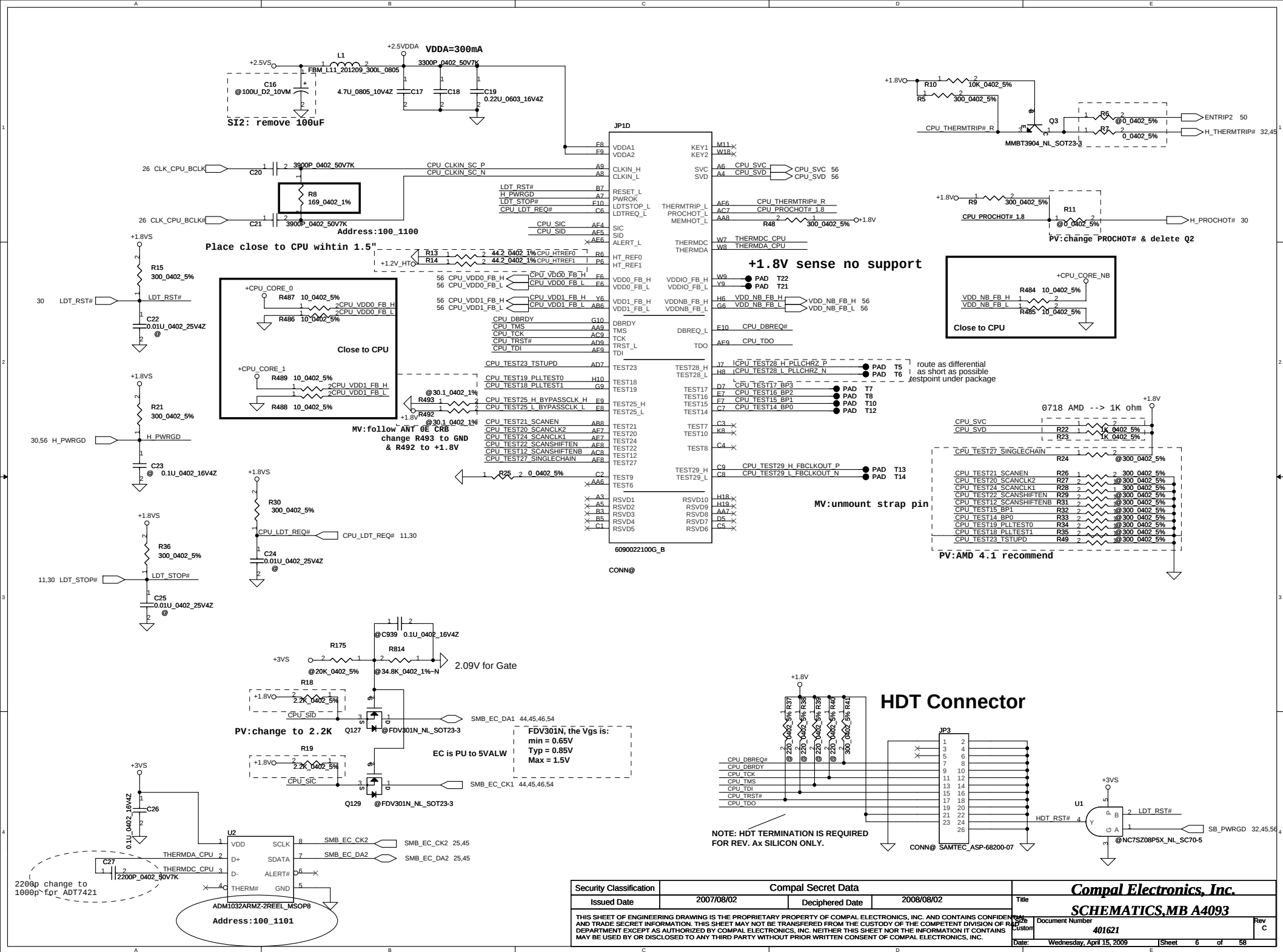
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



CONN®

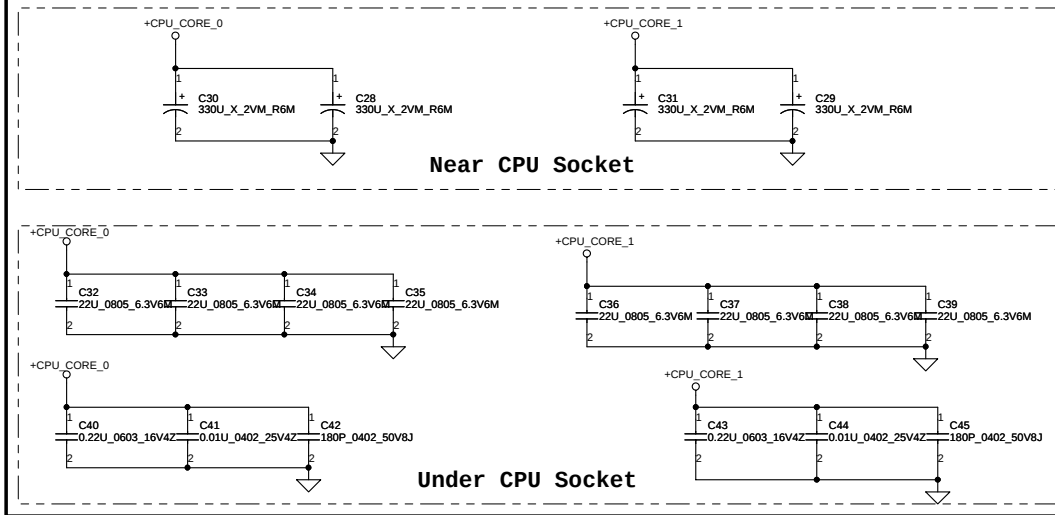
6090022100G B

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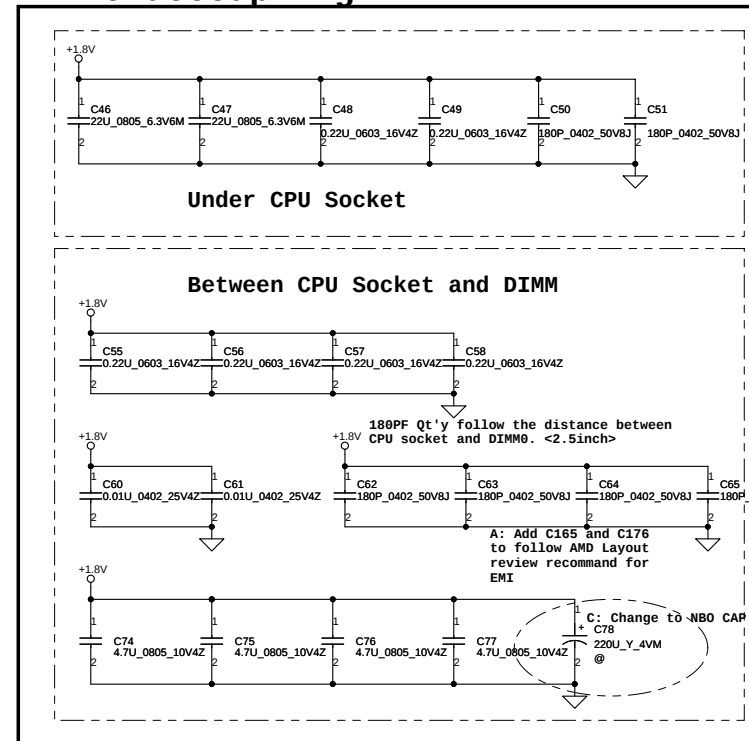


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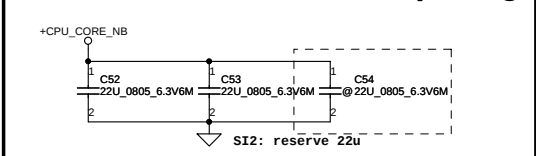
VDD(+CPU_CORE) decoupling.



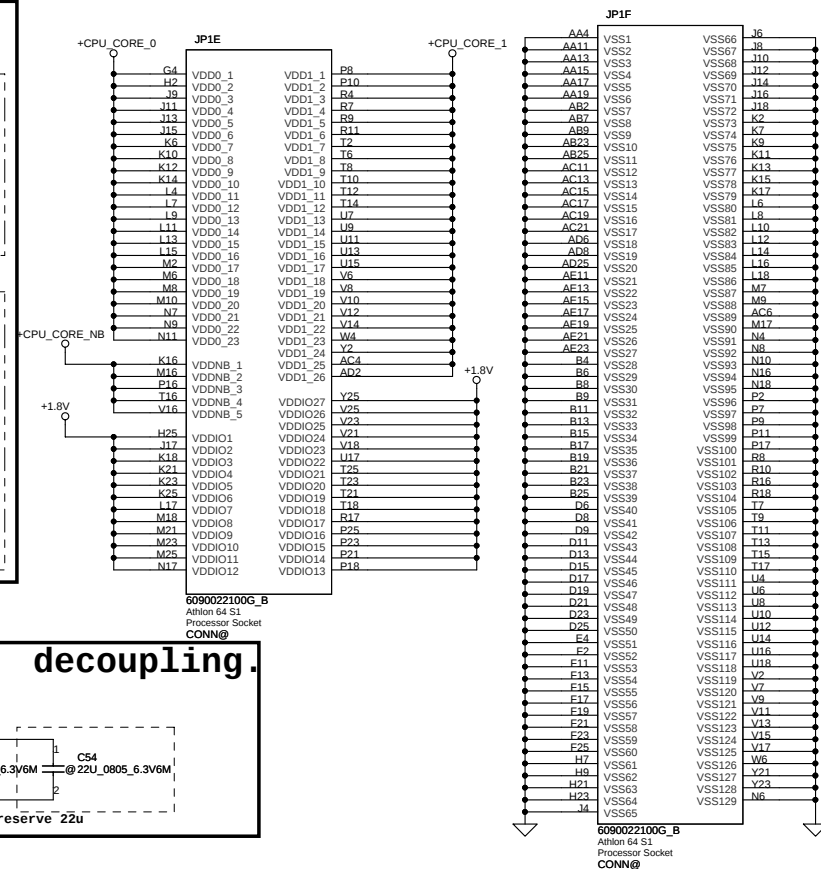
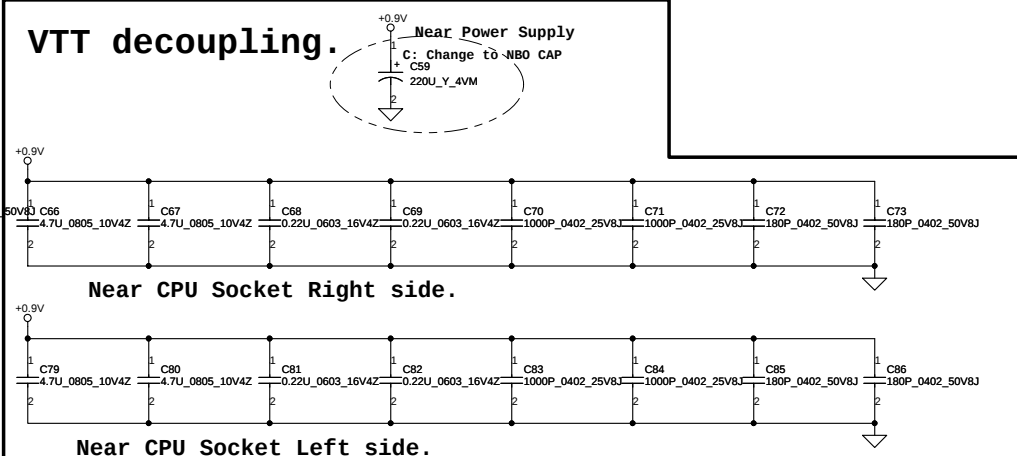
VDDIO decoupling.



+CPU_CORE_NB decoupling.

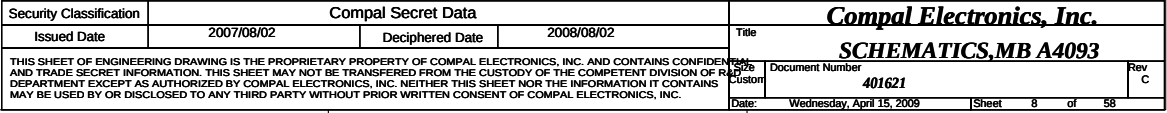


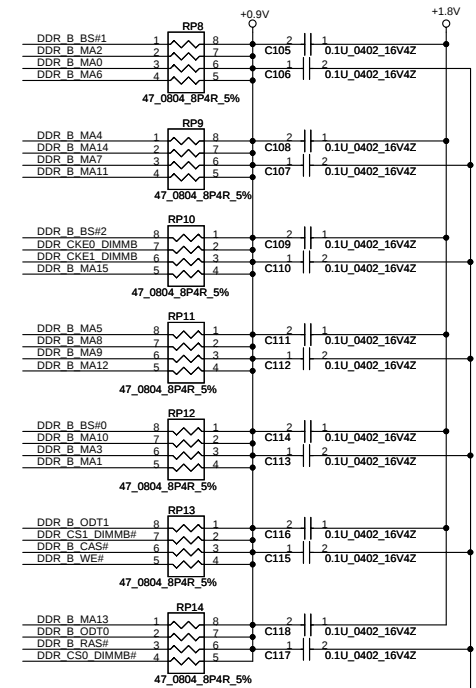
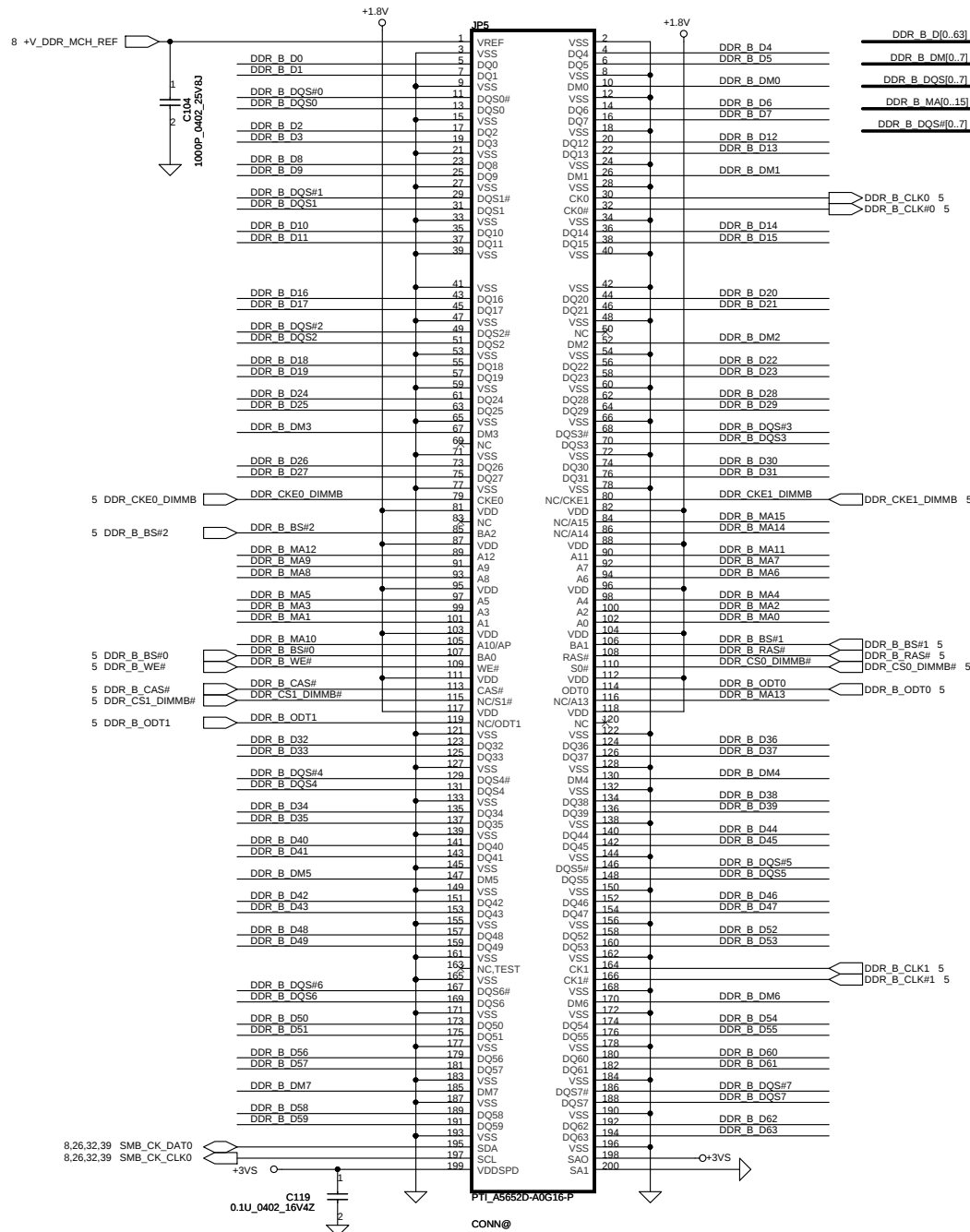
VTT decoupling.



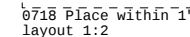
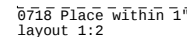
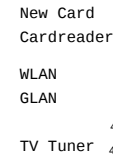
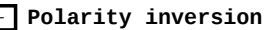
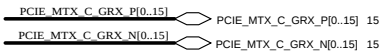
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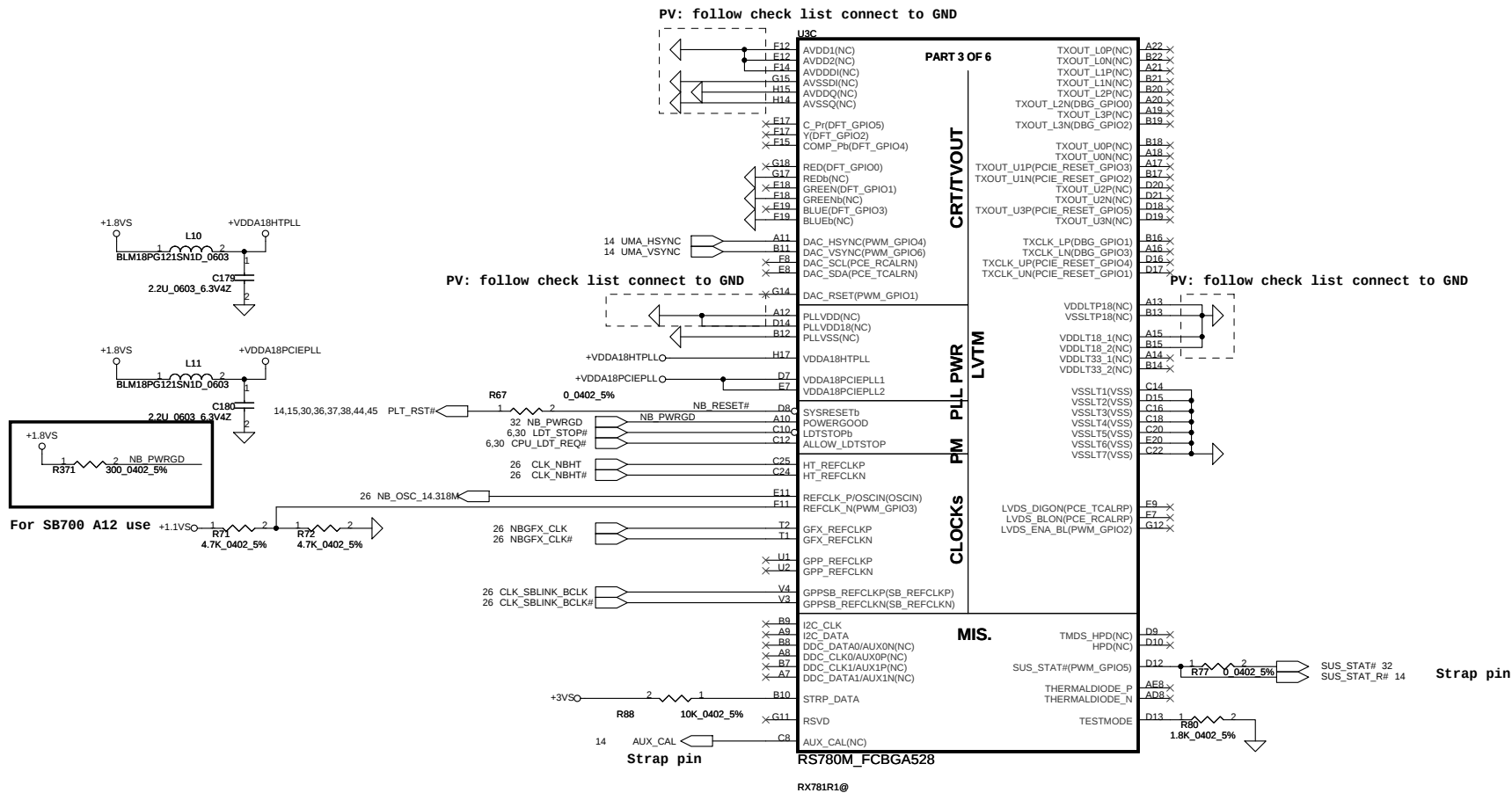


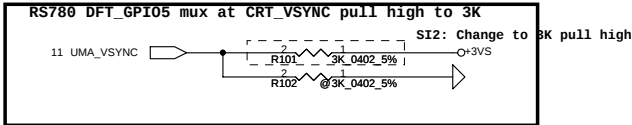


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DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

1 : Enable (RX780, RS780)

0 : Disable (RX780, RS780)

PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#

RS780 use register to control PCI-E configure

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.

000 : 00001

001 : 00010

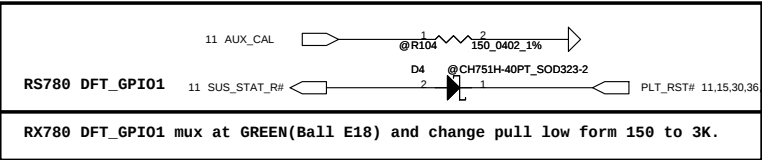
010 : 01011

011 : 00100

100 : 01010

101 : 01100

111 : 01011



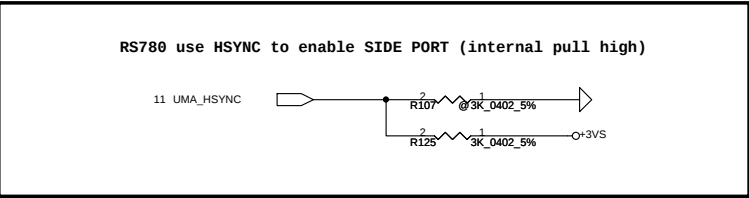
DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values

0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

RX780: Enables the Test Debug Bus using PCIE bus

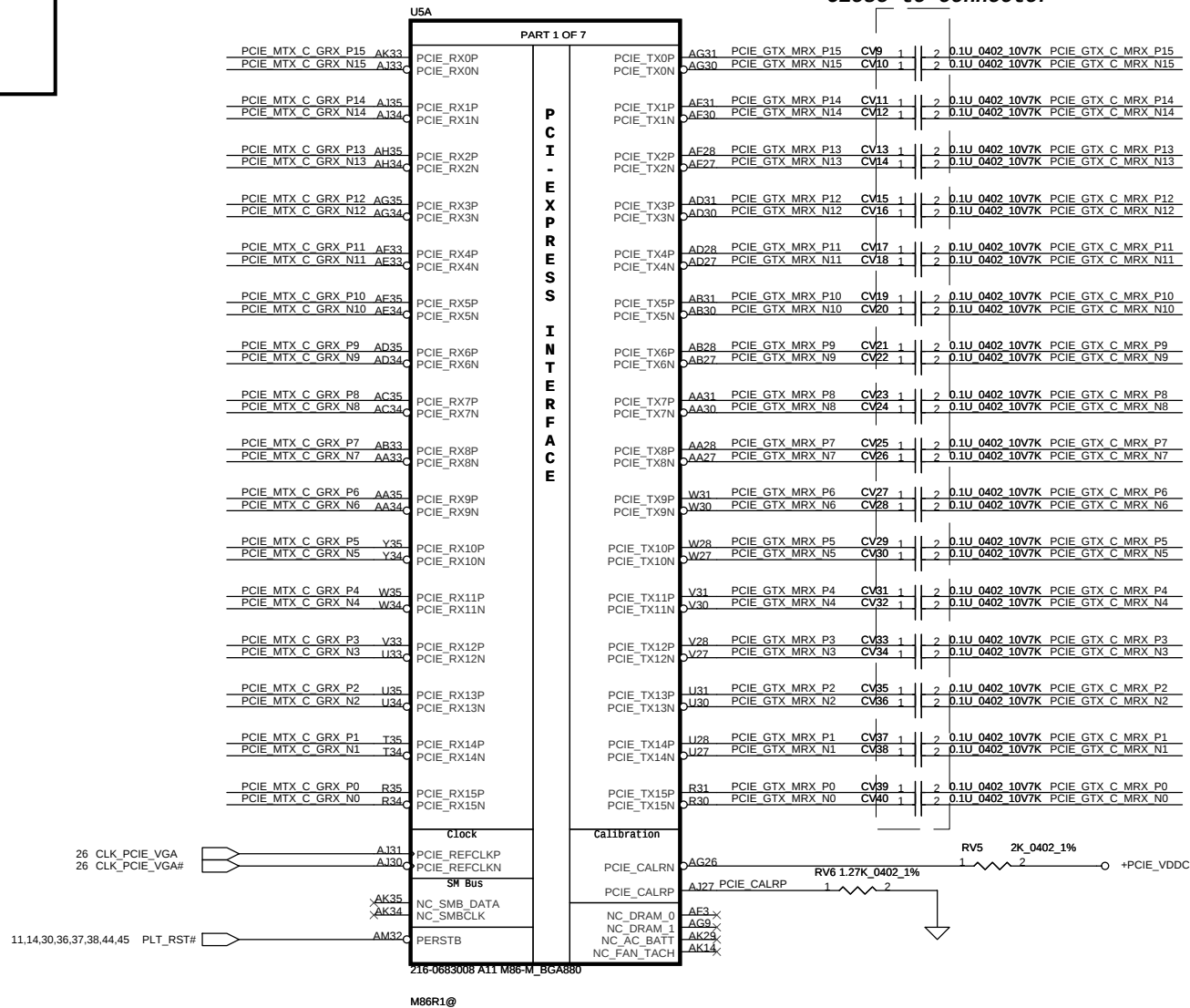
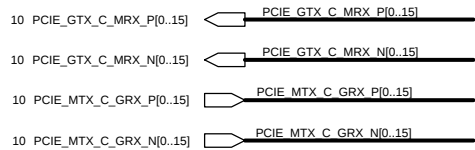
1 : Disable (Can still be enabled using nbcfg register access)

0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)

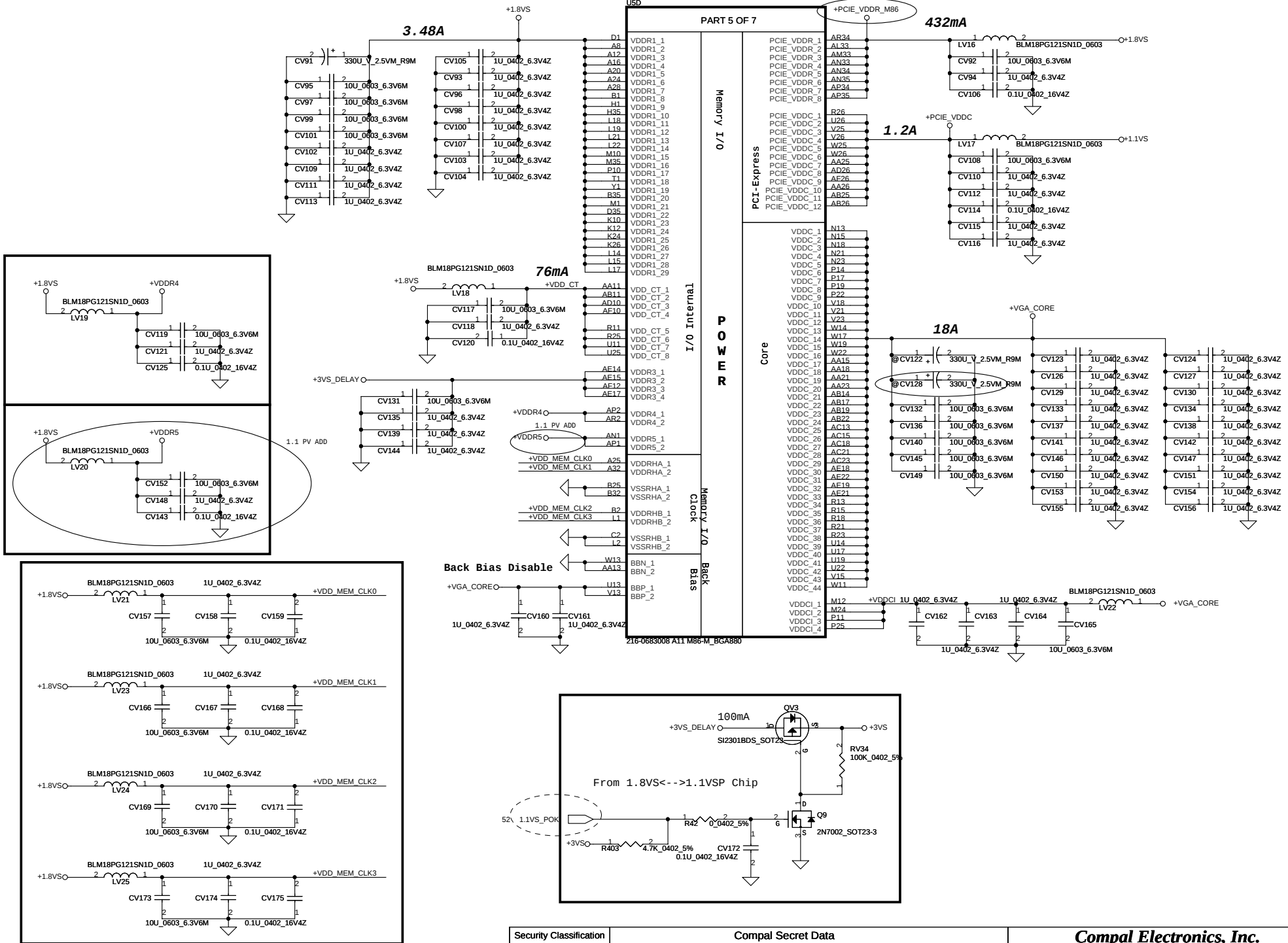
1. Disable (RS780)

0 : Enable (RS780)

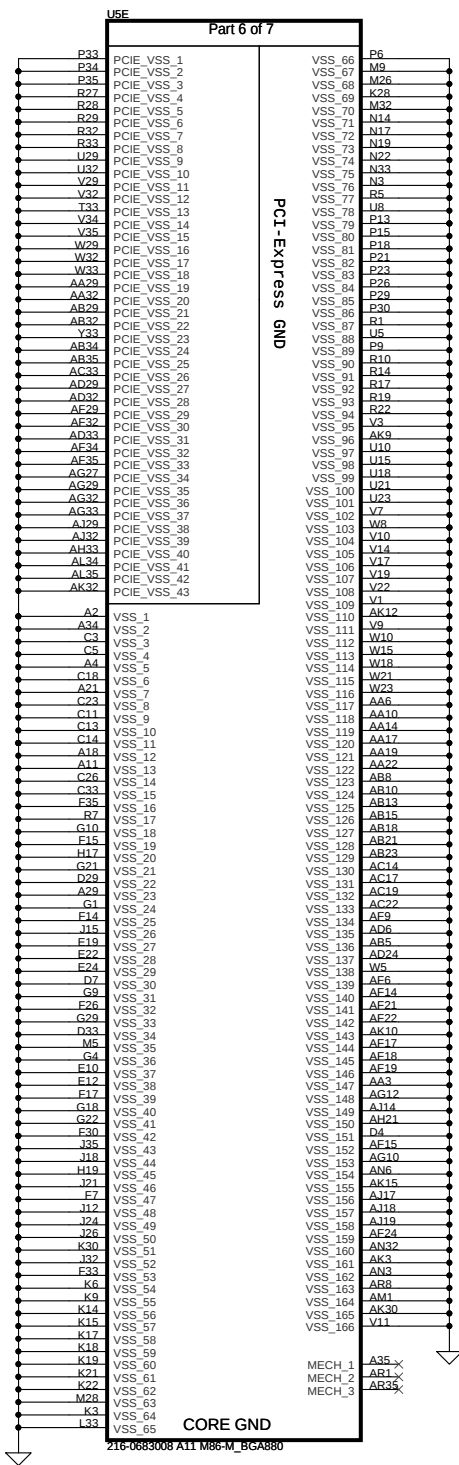


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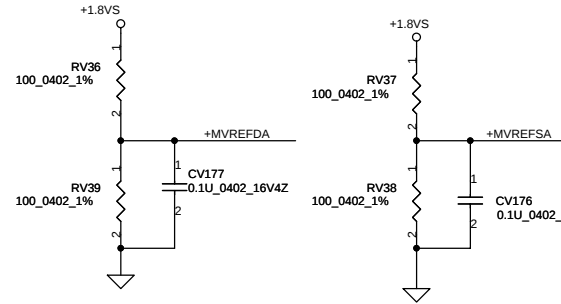
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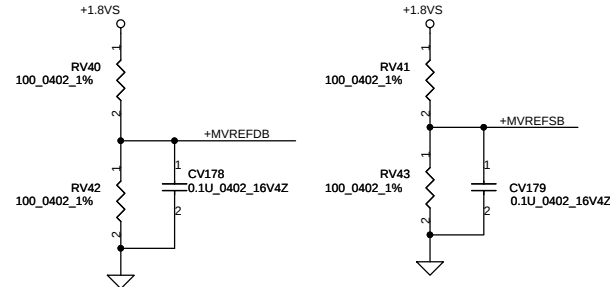
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DQMA#7..0]	<< DQMA#7..0]	21,22
QSA[7..0]	<< QSA[7..0]	21,22
QSA#7..0]	<< QSA#7..0]	21,22
MAA[12..0]	<< MAA[12..0]	21,22
BA[2..0]	<< BA[2..0]	21,22
MDA[63..0]	<< MDA[63..0]	21,22

Close to pin N34, N35



Close to pin A13, B14



MDB[63..0]	<< MDB[63..0]	23,24
MAB[12..0]	<< MAB[12..0]	23,24
BB[2..0]	<< BB[2..0]	23,24
DQMB#7..0]	<< DQMB#7..0]	23,24
QSB[7..0]	<< QSB[7..0]	23,24
QSB#7..0]	<< QSB#7..0]	23,24

Part 3 of 7			
MDA0 P27	DQA_0	MAA_0	C27 MAA0
MDA1 P28	DQA_1	MAA_1	B28 MAA1
MDA2 P31	DQA_2	MAA_2	B27 MAA2
MDA3 P32	DQA_3	MAA_3	G26 MAA3
MDA4 M27	DQA_4	MAA_4	E27 MAA4
MDA5 K29	DQA_5	MAA_5	D27 MAA5
MDA6 K31	DQA_6	MAA_6	J27 MAA6
MDA7 K32	DQA_7	MAA_7	F29 MAA7
MDA8 M33	DQA_8	MAA_8	C30 MAA8
MDA9 M34	DQA_9	MAA_9	E26 MAA9
MDA10 L34	DQA_10	MAA_10	G27 MAA10
MDA11 L35	DQA_11	MAA_11	D26 MAA11
MDA12 L33	DQA_12	MAA_12	C28 BA0
MDA13 L34	DQA_13	MAA_13	B29 BA1
MDA14 H33	DQA_14	MAA_14	
MDA15 H34	DQA_15	MAA_15	
MDA16 K27	DQA_16	MAA_16	
MDA17 J29	DQA_17	MAA_17	
MDA18 J30	DQA_18	MAA_18	
MDA19 J31	DQA_19	MAA_19	
MDA20 E29	DQA_20	MAA_20	
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MDA24 G33	DQA_24	MAA_24	
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MDA26 G35	DQA_26	MAA_26	
MDA27 F34	DQA_27	MAA_27	
MDA28 D34	DQA_28	MAA_28	
MDA29 C34	DQA_29	MAA_29	
MDA30 C35	DQA_30	MAA_30	
MDA31 B34	DQA_31	MAA_31	
MDA32 C24	DQA_32	MAA_32	
MDA33 B24	DQA_33	MAA_33	
MDA34 B23	DQA_34	MAA_34	
MDA35 A23	DQA_35	MAA_35	
MDA36 C21	DQA_36	MAA_36	
MDA37 B21	DQA_37	MAA_37	
MDA38 C20	DQA_38	MAA_38	
MDA39 B20	DQA_39	MAA_39	
MDA40 J22	DQA_40	MAA_40	
MDA41 H22	DQA_41	MAA_41	
MDA42 E22	DQA_42	MAA_42	
MDA43 D21	DQA_43	MAA_43	
MDA44 J19	DQA_44	MAA_44	
MDA45 G19	DQA_45	MAA_45	
MDA46 F19	DQA_46	MAA_46	
MDA47 D19	DQA_47	MAA_47	
MDA48 C19	DQA_48	MAA_48	
MDA49 B19	DQA_49	MAA_49	
MDA50 A19	DQA_50	MAA_50	
MDA51 B18	DQA_51	MAA_51	
MDA52 C16	DQA_52	MAA_52	
MDA53 B16	DQA_53	MAA_53	
MDA54 C15	DQA_54	MAA_54	
MDA55 A15	DQA_55	MAA_55	
MDA56 H18	DQA_56	MAA_56	
MDA57 F18	DQA_57	MAA_57	
MDA58 E18	DQA_58	MAA_58	
MDA59 D18	DQA_59	MAA_59	
MDA60 J17	DQA_60	MAA_60	
MDA61 G15	DQA_61	MAA_61	
MDA62 F15	DQA_62	MAA_62	
MDA63 D15	DQA_63	MAA_63	

MEMORY INTERFACE A

write strobe read strobe

216-0683008 A11 M86-M_BGA880

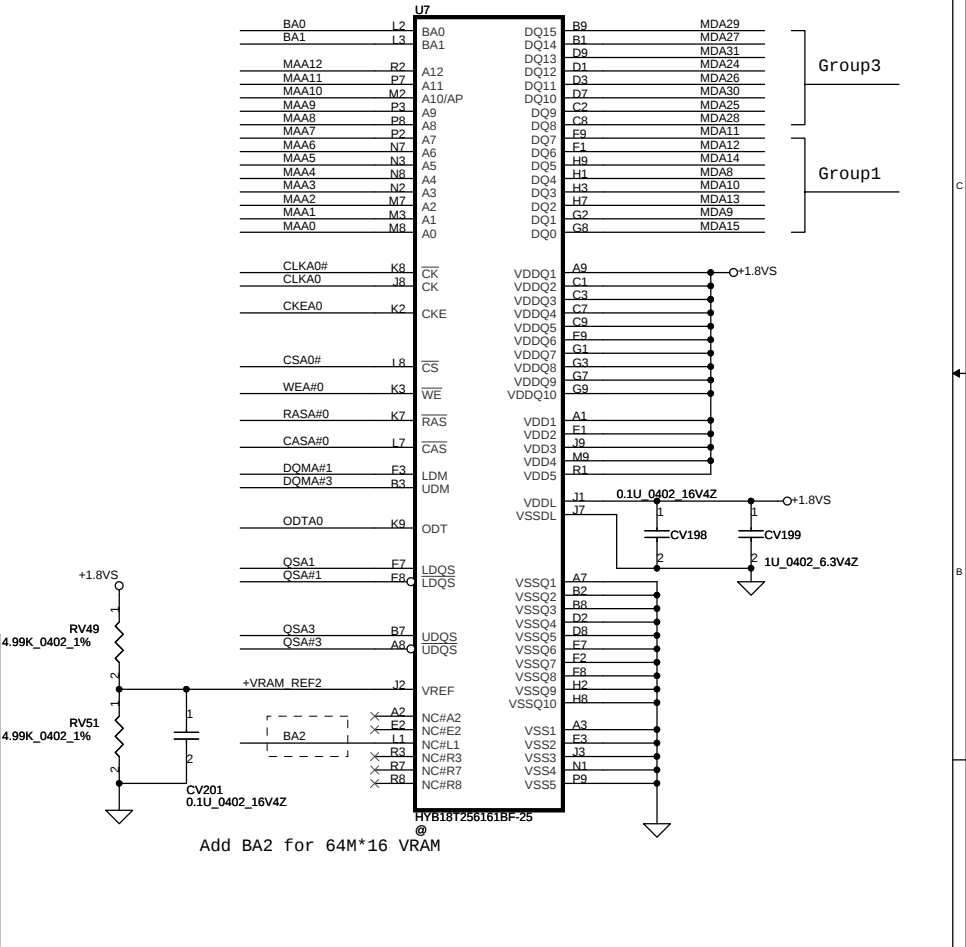
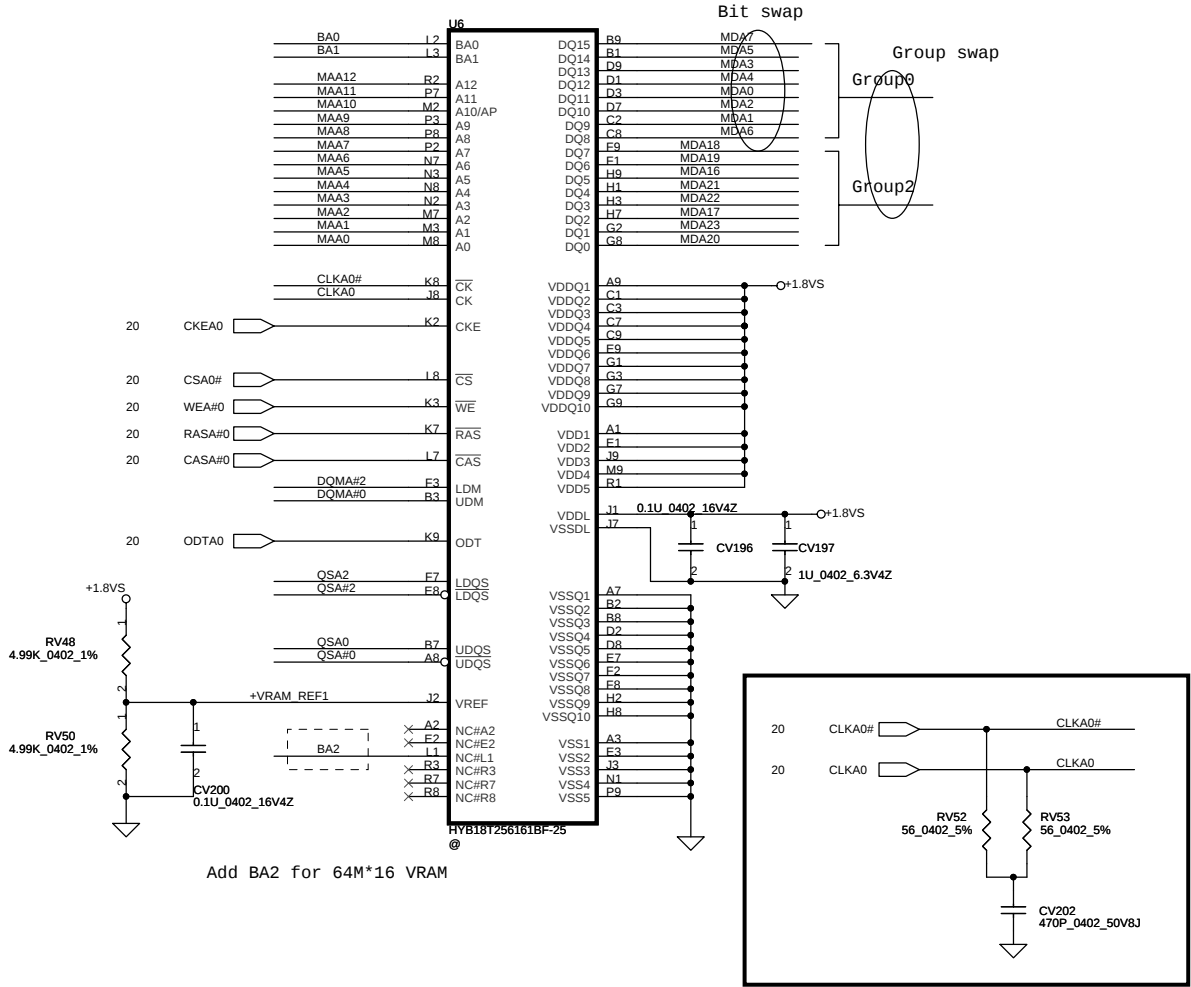
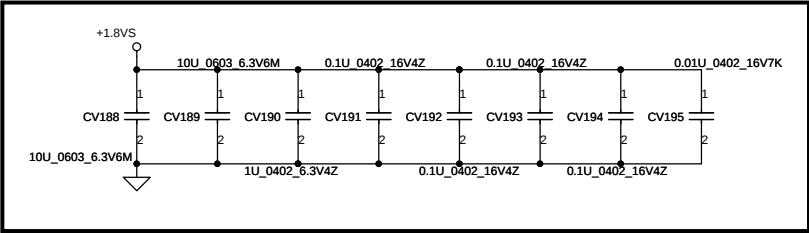
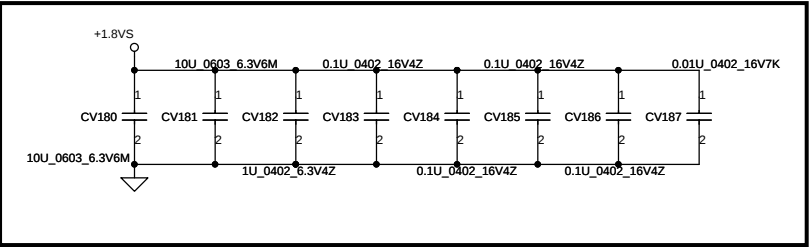
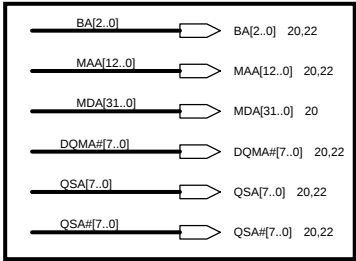
MEMORY INTERFACE B

Part 4 of 7			
MDB0 H15	DQB_0	MAB_0	H2 MAB0
MDB1 G14	DQB_1	MAB_1	H3 MAB1
MDB2 F14	DQB_2	MAB_2	J5 MAB2
MDB3 D14	DQB_3	MAB_3	J4 MAB3
MDB4 H12	DQB_4	MAB_4	J6 MAB4
MDB5 G12	DQB_5	MAB_5	G5 MAB5
MDB6 F12	DQB_6	MAB_6	E3 MAB6
MDB7 D10	DQB_7	MAB_7	J9 MAB7
MDB8 B13	DQB_8	MAB_8	E4 MAB8
MDB9 C12	DQB_9	MAB_9	J11 MAB9
MDB10 B12	DQB_10	MAB_10	J2 MAB10
MDB11 B11	DQB_11	MAB_11	J7 MAB11
MDB12 C9	DQB_12	MAB_12	F1 BB2
MDB13 B9	DQB_13	MAB_13	G2 BB0
MDB14 A9	DQB_14	MAB_14	G3 BB1
MDB15 B8	DQB_15	MAB_15	
MDB16 J10	DQB_16	MAB_16	
MDB17 H10	DQB_17	MAB_17	
MDB18 F10	DQB_18	MAB_18	
MDB19 D9	DQB_19	MAB_19	
MDB20 G7	DQB_20	MAB_20	
MDB22 G6	DQB_21	MAB_21	
MDB23 F6	DQB_22	MAB_22	
MDB24 C8	DQB_23	MAB_23	
MDB25 C7	DQB_24	MAB_24	
MDB26 B7	DQB_25	MAB_25	
MDB27 A7	DQB_26	MAB_26	
MDB28 B5	DQB_27	MAB_27	
MDB29 A5	DQB_28	MAB_28	
MDB30 C4	DQB_29	MAB_29	
MDB31 B4	DQB_30	MAB_30	
MDB32 M3	DQB_31	MAB_31	
MDB33 M2	DQB_32	MAB_32	
MDB34 N2	DQB_33	MAB_33	
MDB35 B3	DQB_34	MAB_34	
MDB37 R2	DQB_35	MAB_35	
MDB38 T3	DQB_36	MAB_36	
MDB39 T2	DQB_37	MAB_37	
MDB40 M8	DQB_38	MAB_38	
MDB41 M7	DQB_39	MAB_39	
MDB42 P5	DQB_40	MAB_40	
MDB43 P4	DQB_41	MAB_41	
MDB44 R9	DQB_42	MAB_42	
MDB45 R8	DQB_43	MAB_43	
MDB46 R6	DQB_44	MAB_44	
MDB47 U4	DQB_45	MAB_45	
MDB48 U3	DQB_46	MAB_46	
MDB49 U2	DQB_47	MAB_47	
MDB50 U1	DQB_48	MAB_48	
MDB51 V2	DQB_49	MAB_49	
MDB52 Y3	DQB_50	MAB_50	
MDB53 Y2	DQB_51	MAB_51	
MDB54 A2	DQB_52	MAB_52	
MDB55 A1	DQB_53	MAB_53	
MDB56 U9	DQB_54	MAB_54	
MDB57 U7	DQB_55	MAB_55	
MDB58 U6	DQB_56	MAB_56	
MDB59 V4	DQB_57	MAB_57	
MDB60 W9	DQB_58	MAB_58	
MDB61 W7	DQB_59	MAB_59	
MDB62 W6	DQB_60	MAB_60	
MDB63 V4	DQB_61	MAB_61	
	DQB_62	MAB_62	
	DQB_63	MAB_63	

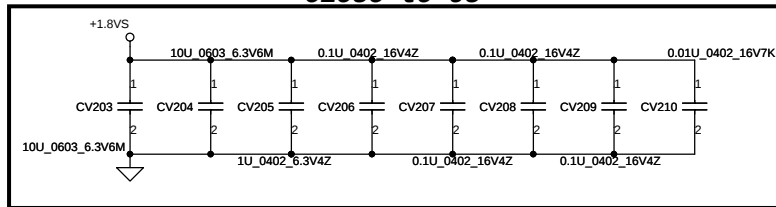
+MVREFDB	B14	MVREFDB
+MVREFSB	A13	MVREFSB
TESTEN		
TEST_MCLK		
TEST_YCLK		
MEMTEST		
PLLTEST		

216-0683008 A11 M86-M_BGA880

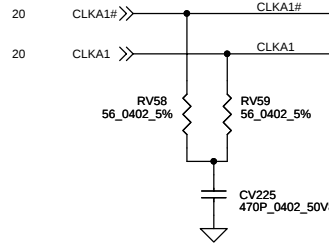
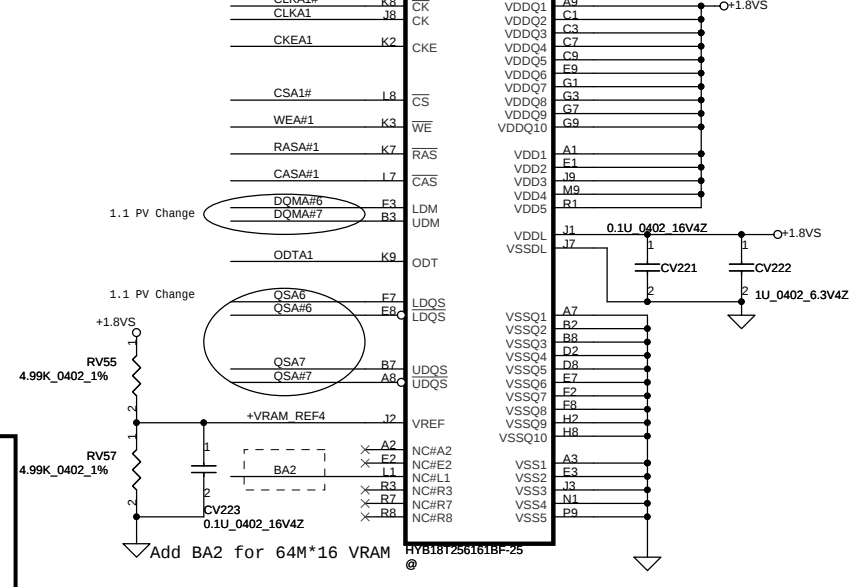
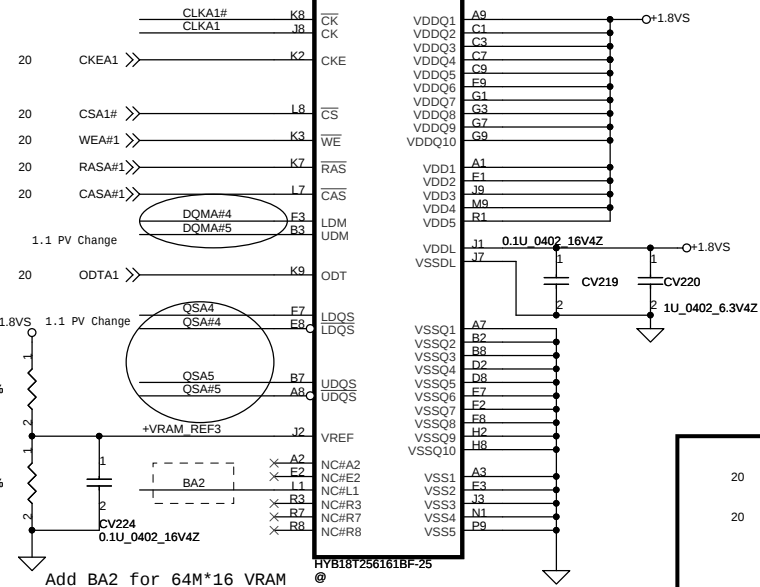
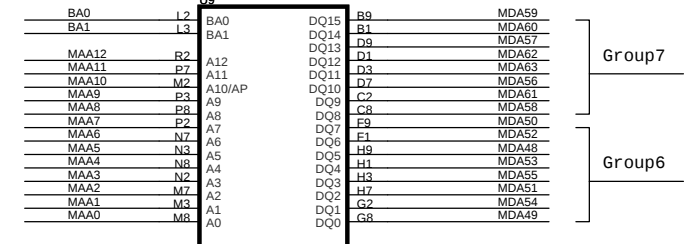
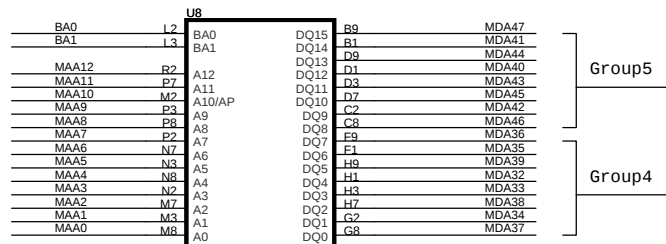
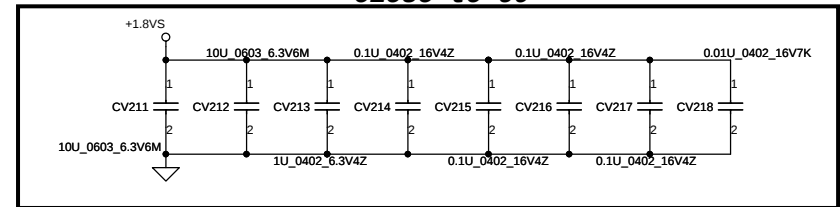
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Date	Wednesday, April 15, 2009	Sheet	20	of	58

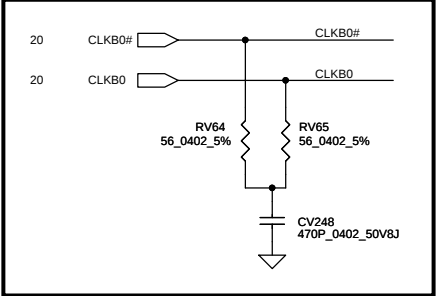
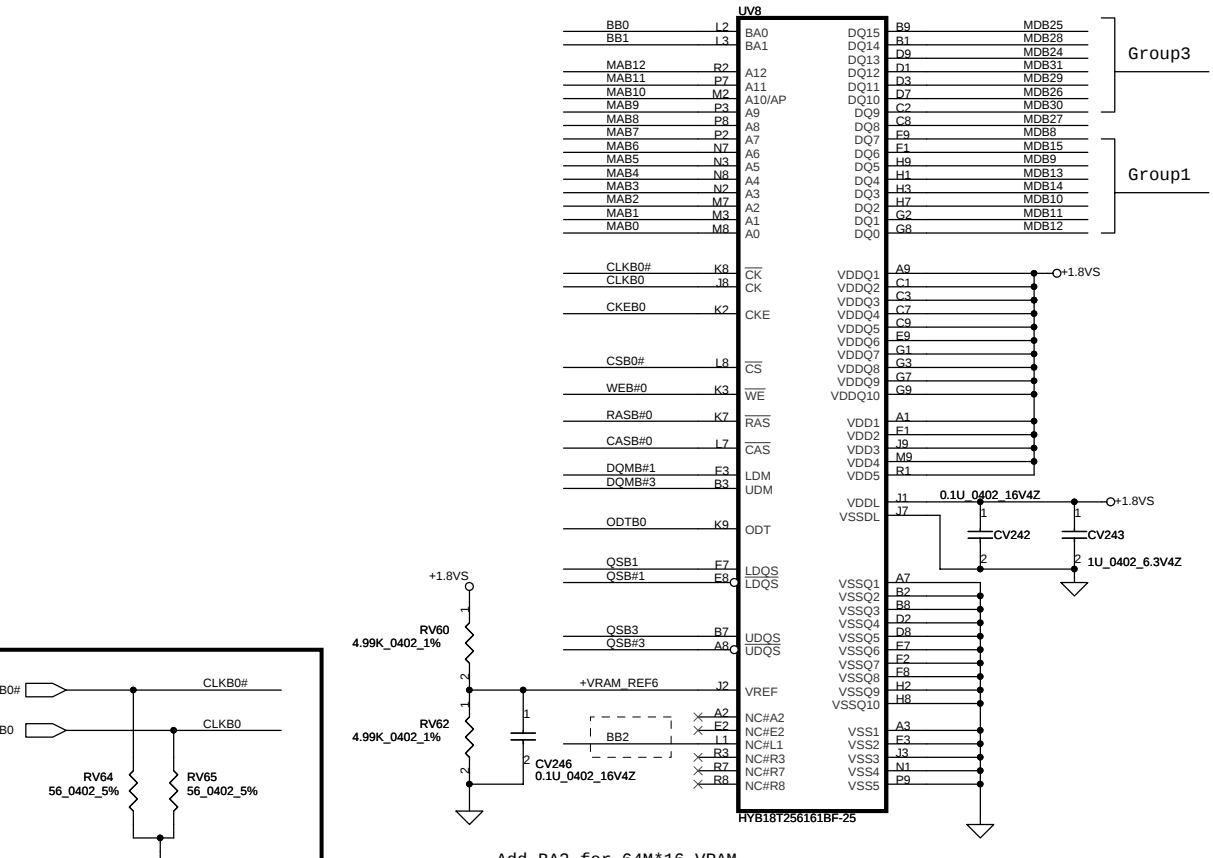
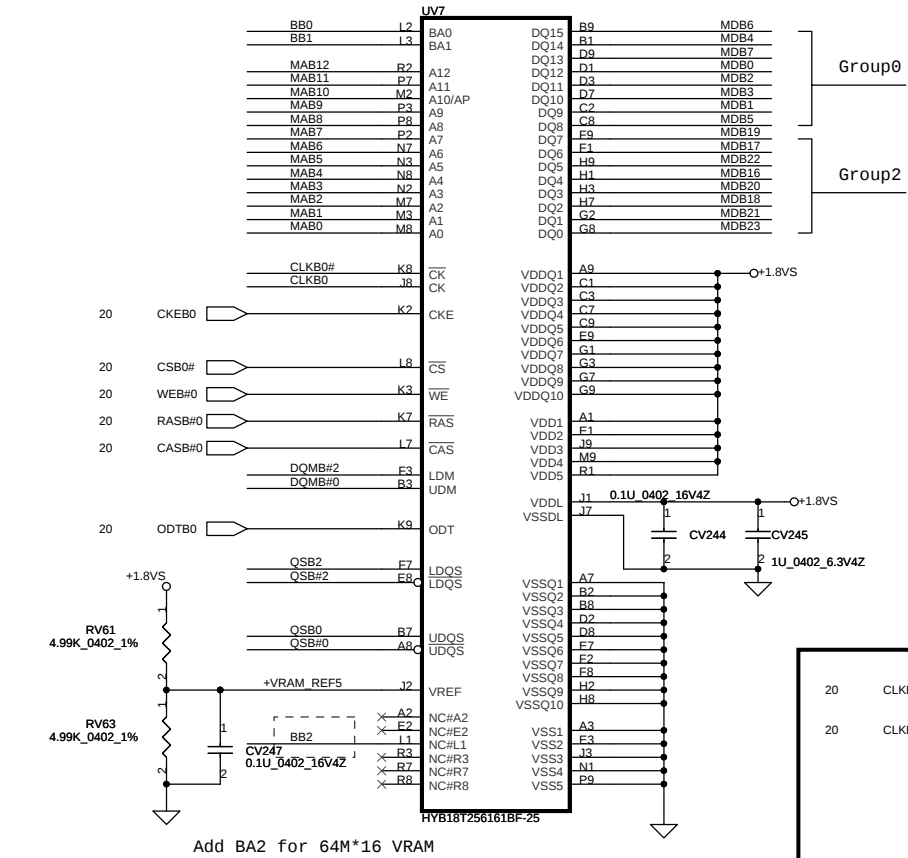
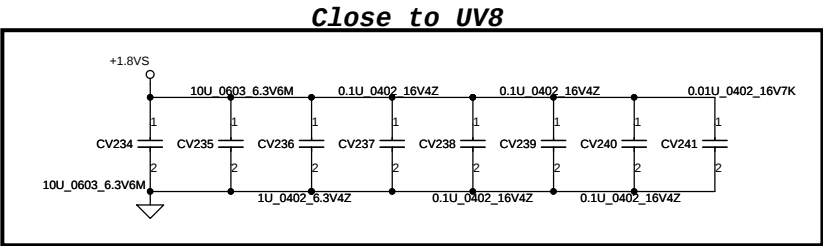
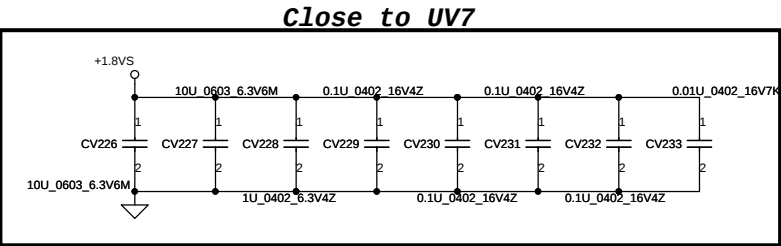
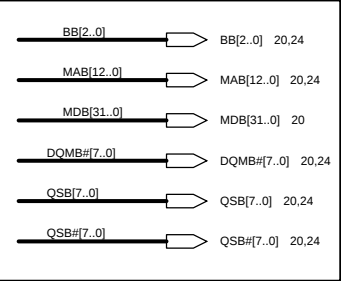


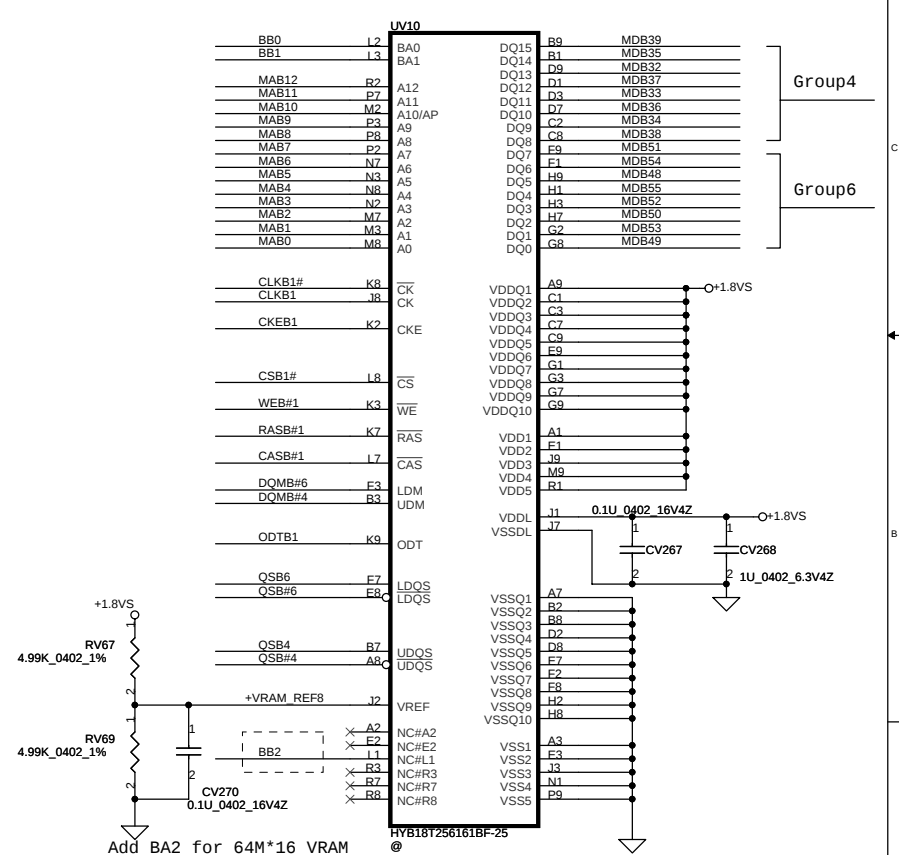
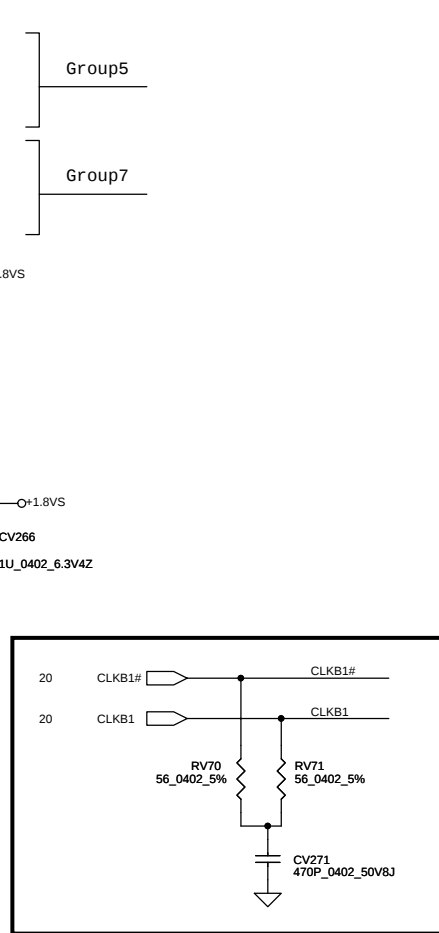
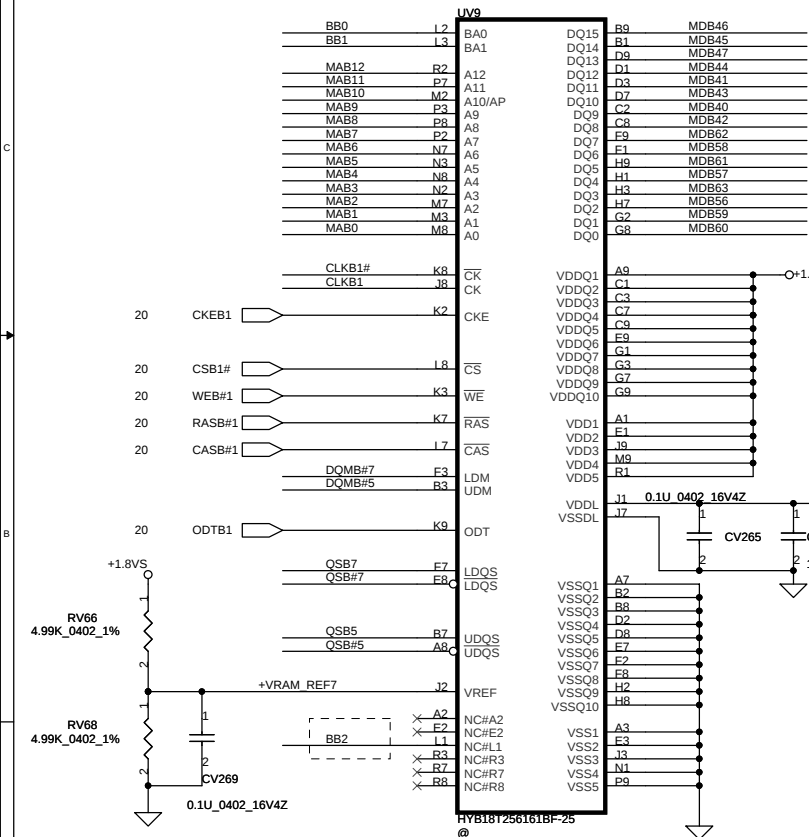
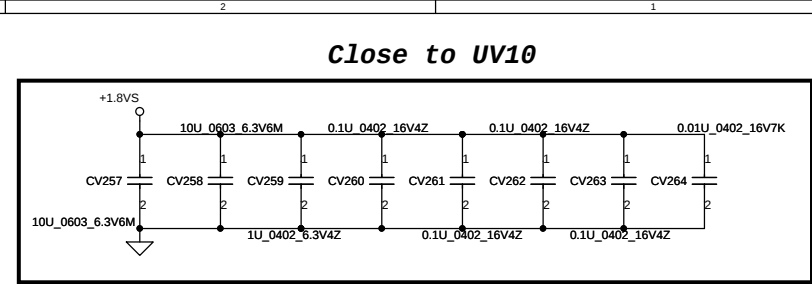
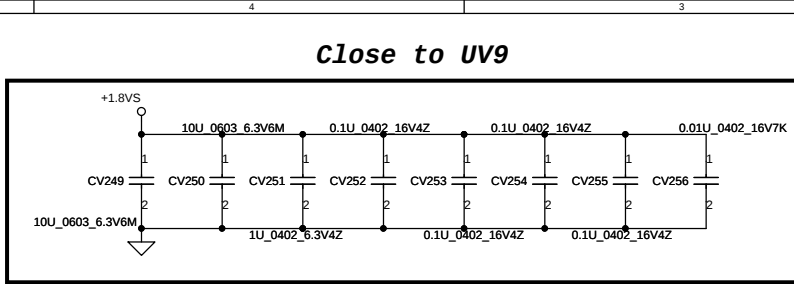
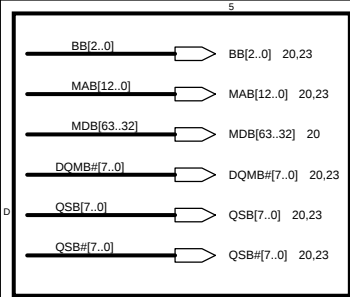
Close to U8



Close to U9

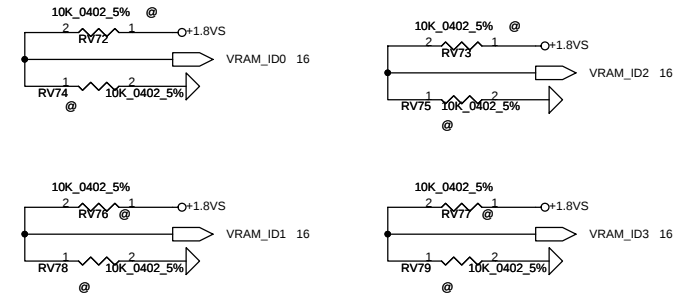




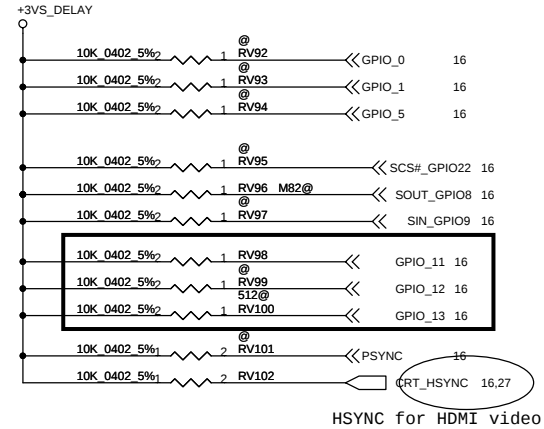


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STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (23,22,21,20)	M82M-XT	JBK00 1.0a	512M(x4)	Samsung 64Mx16 1.8V	SA00002MD00	0 0 0 0
			JBK00 1.0	256M(X4)	Samsung 32Mx16 1.8V	SA00002AJ10	0 0 0 1
				512M(x4)	Hynix 64Mx16 1.8V		0 0 1 0
			JBK00 1.0	256M(X4)	Hynix 32Mx16 1.8V	SA00002DL00	0 0 1 1
			JBK00 1.0	256M(X4)	Qimonda 32Mx16 1.8V	SA00002A600	0 1 0 0
			JBK00 1.0a	512M(x4)	Qimonda 64Mx16 1.8V	SA00002MF00	0 1 0 1
		M86M	JBK00 1.1	512M(x8)	Samsung 32Mx16 1.8V	SA00002AJ10	0 1 1 0
			JBK00 1.1	512M(x8)	Hynix 32Mx16 1.8V	SA00002DL00	0 1 1 1
			JBK00 1.1	512M(x8)	Qimonda 32Mx16 1.8V	SA00002A600	1 0 0 0
				1G(x8)	Samsung 64Mx16 1.8V	SA00002MD00	1 0 0 1
				1G(x8)	Hynix 64Mx16 1.8V		1 0 1 0
				1G(x8)	Qimonda 64Mx16 1.8V	SA00002MF00	1 0 1 1

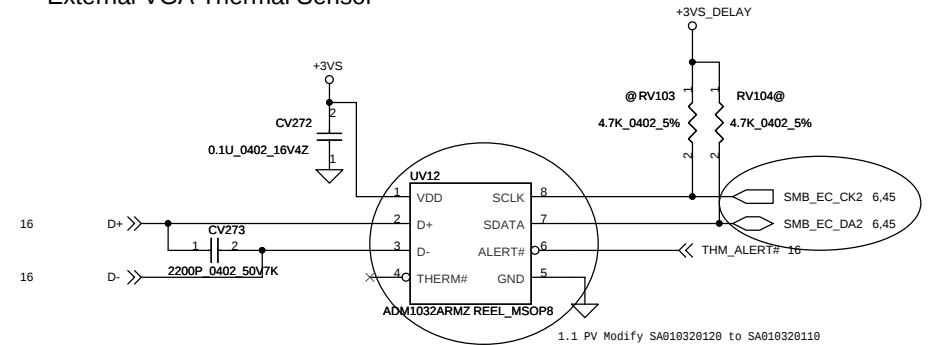


STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED M8X
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLES	0
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0
BIF_GEN2_EN_A	GPIO5	PCI-E 5.0GT/s or 2.5 GT/s select	0
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO M86-M ONLY	
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO M82-M ONLY	
ROMIDCFG[3:0]	GPIO [9,13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 0 1
BIF_VGA_DIS	PSYNC	VGA ENABLED===0 is enable	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE	1

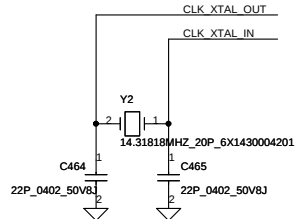
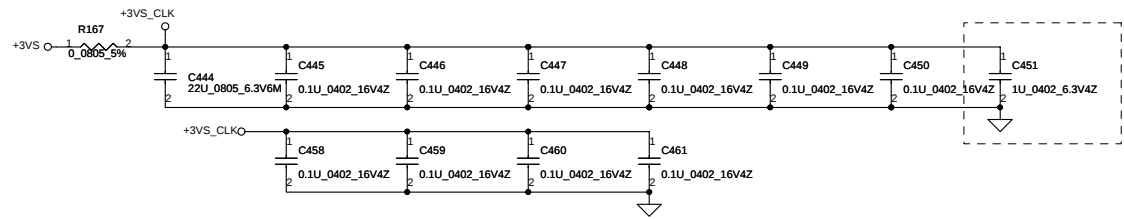
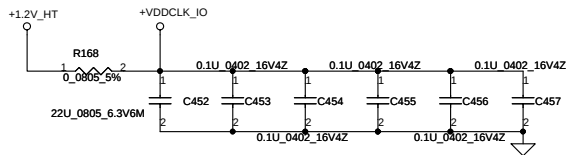


GPIO9 = 0 (BIOS_ROM_EN = 0)	
GPIO[13:11]	MEMORY SIZE
0 0 0	128MB
0 0 1	256MB
0 1 0	64MB
1 0 0	512MB

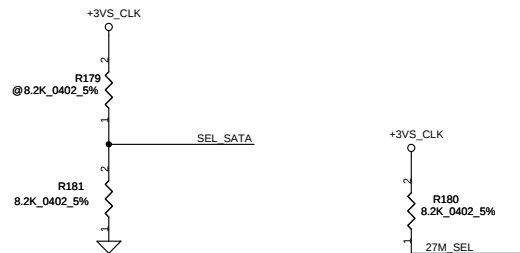
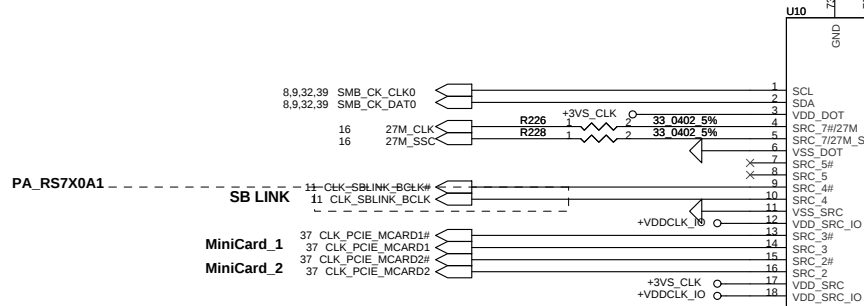
External VGA Thermal Sensor



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Routing the trace at least 10mil

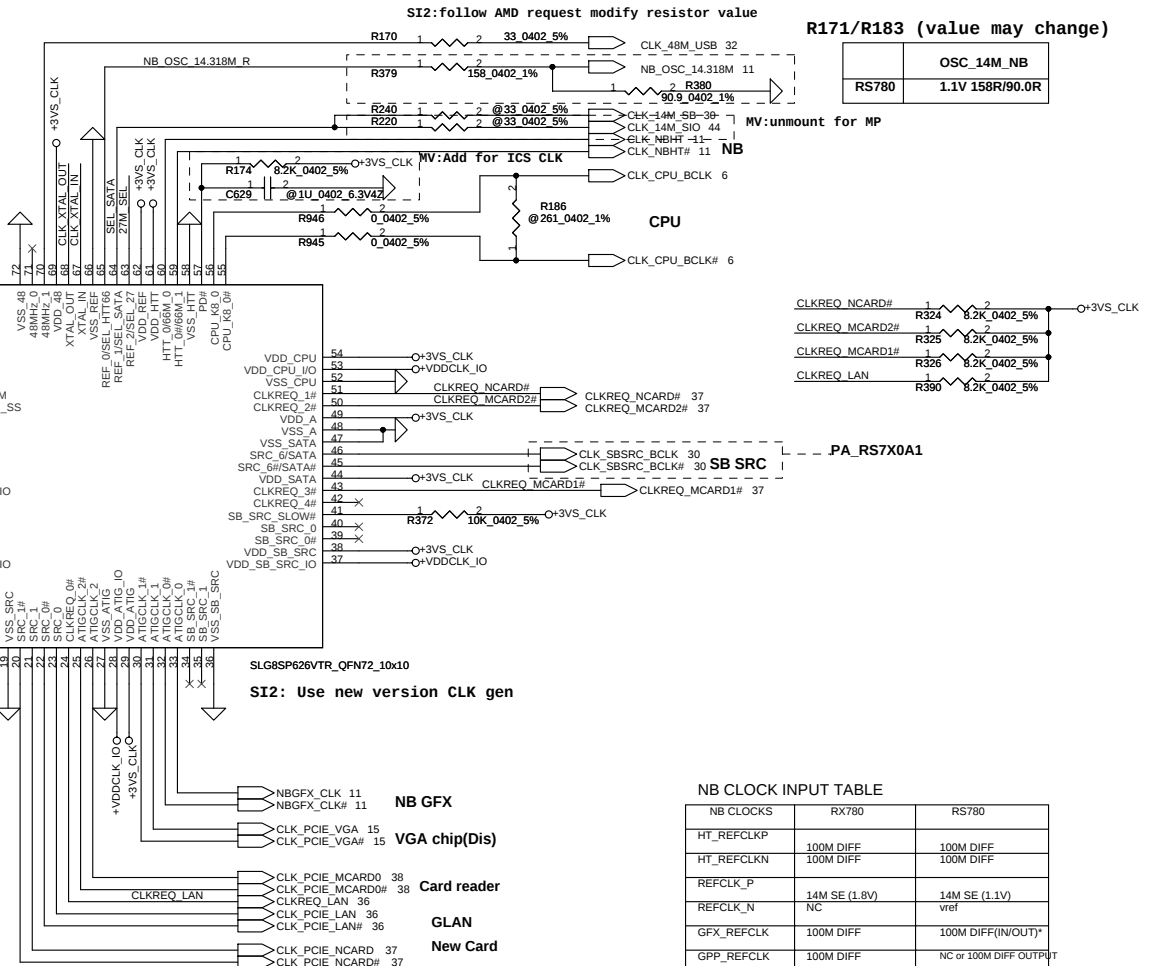


SEL_SATA	1	configure as SATA output
	0 *	configure as normal SRC(SRC_6) output * default

27M_SEL	1 *	configure as 27M and 27M_SS output
	0	configure as SRC_7 output * default

Use voltage divider resistor R379 & R380 to pull low

NB_OSC_14.318M	1	configure as single-ended 66MHz output
	0 *	configure as differential 100MHz output * default



R171/R183 (value may change)

RS780	OSC_14M_NB
	1.1V 158R/90.0R

MV:unmount for MP



PA_RS7X0A1

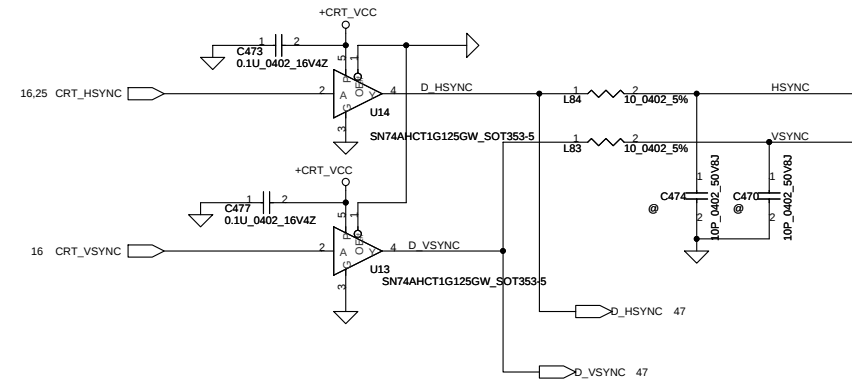
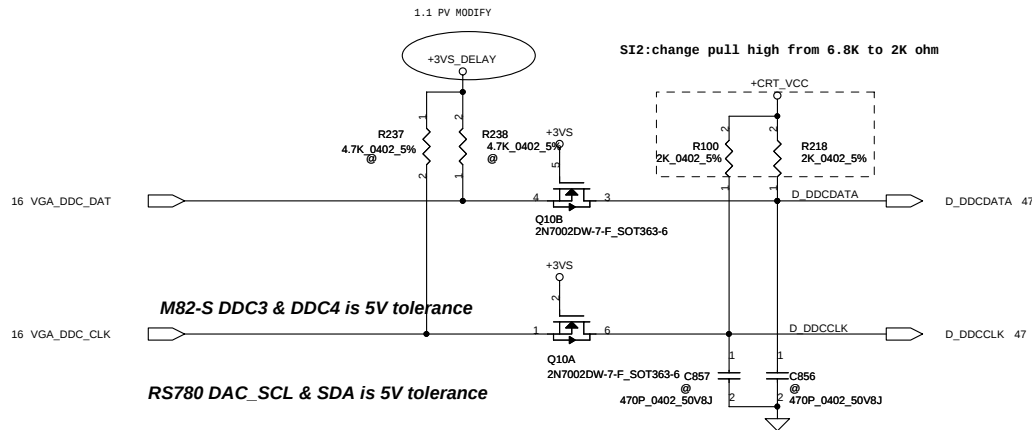
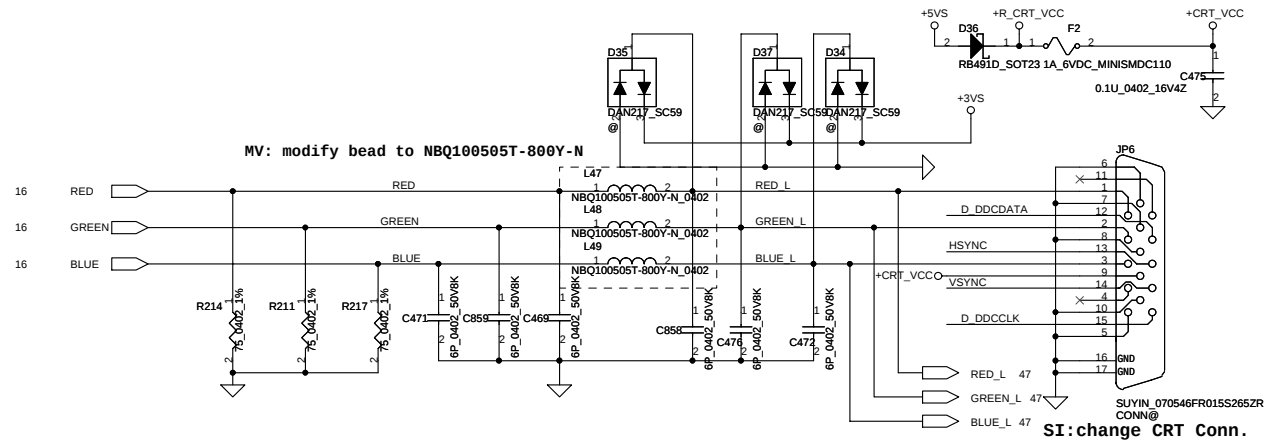
NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

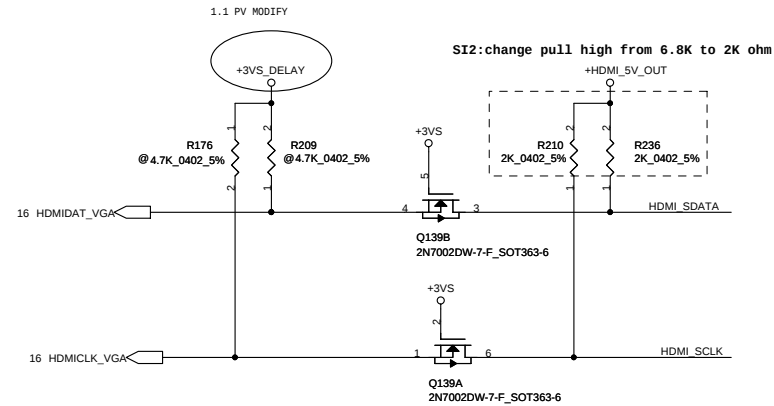
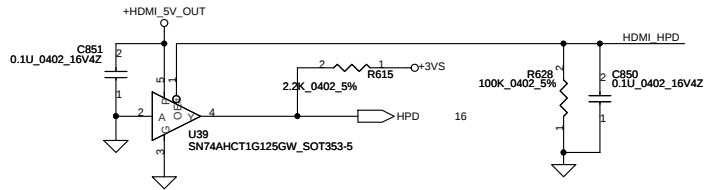
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CRT CONNECTOR

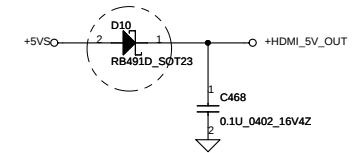


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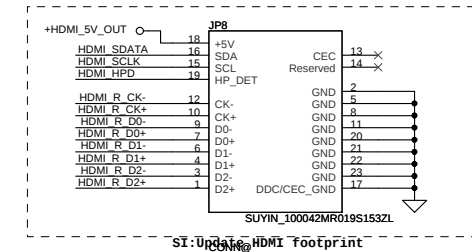


C:Chg. PN to SB770020010.

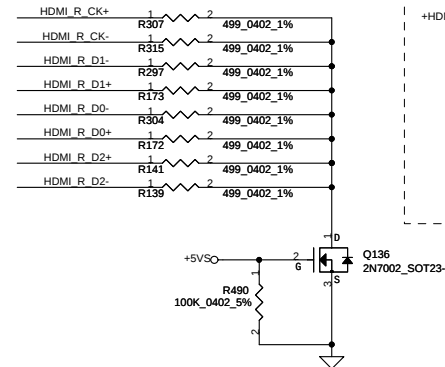
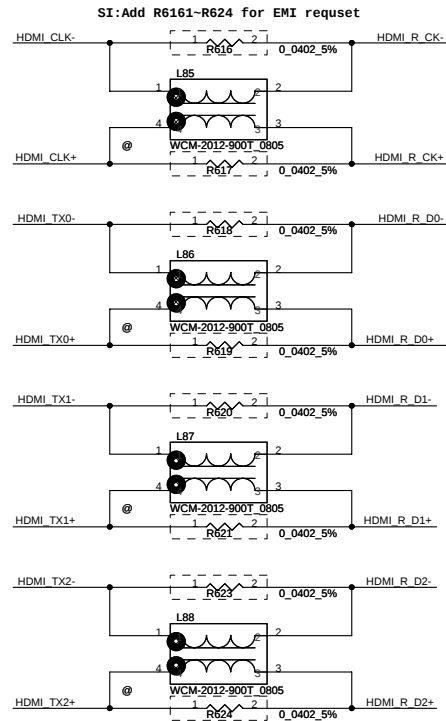
MP:Update D10 to meet HDMI.



HDMI Connector

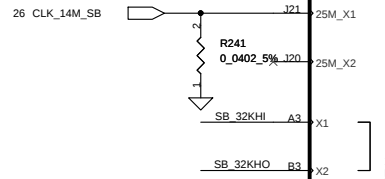
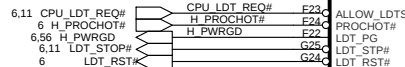
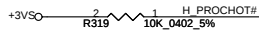
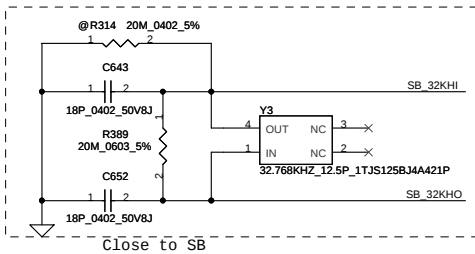
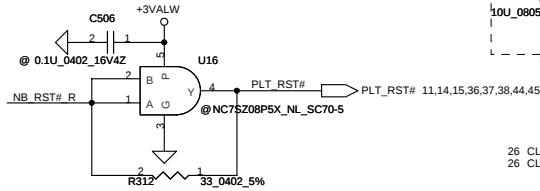
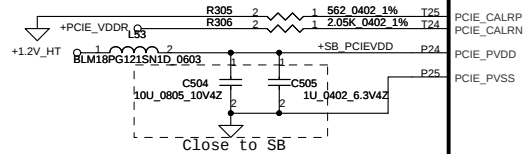
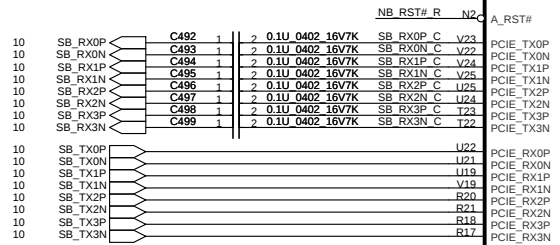
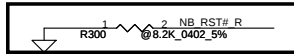


16 HDMI_CLK+ VGA	C507	1	2	0.1U_0402_16V7K	HDMI_CLK+
16 HDMI_CLK- VGA	C508	1	2	0.1U_0402_16V7K	HDMI_CLK-
16 HDMI_TX0+ VGA	C655	1	2	0.1U_0402_16V7K	HDMI_TX0+
16 HDMI_TX0- VGA	C675	1	2	0.1U_0402_16V7K	HDMI_TX0-
16 HDMI_TX1+ VGA	C804	1	2	0.1U_0402_16V7K	HDMI_TX1+
16 HDMI_TX1- VGA	C827	1	2	0.1U_0402_16V7K	HDMI_TX1-
16 HDMI_TX2+ VGA	C852	1	2	0.1U_0402_16V7K	HDMI_TX2+
16 HDMI_TX2- VGA	C853	1	2	0.1U_0402_16V7K	HDMI_TX2-



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Check AMD need pull low or not



218S7EALA11FG_BGA528_SB700
SBR1@

SB700
Part 1 of 5

PCI EXPRESS INTERFACE

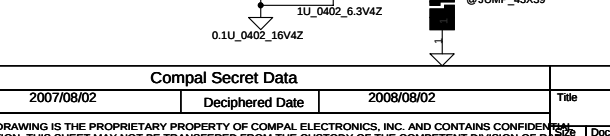
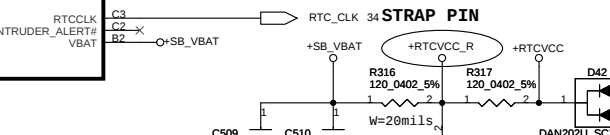
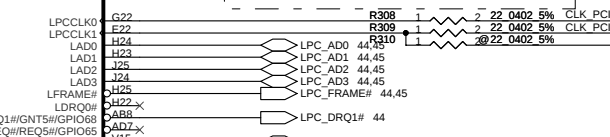
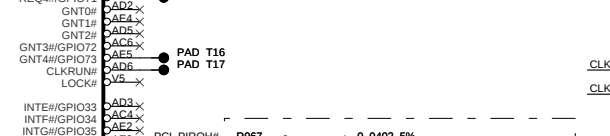
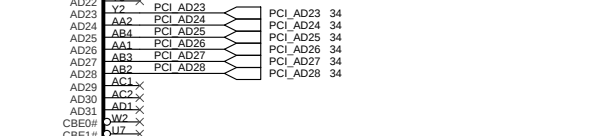
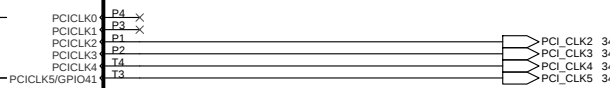
PCI INTERFACE

CLOCK GENERATOR

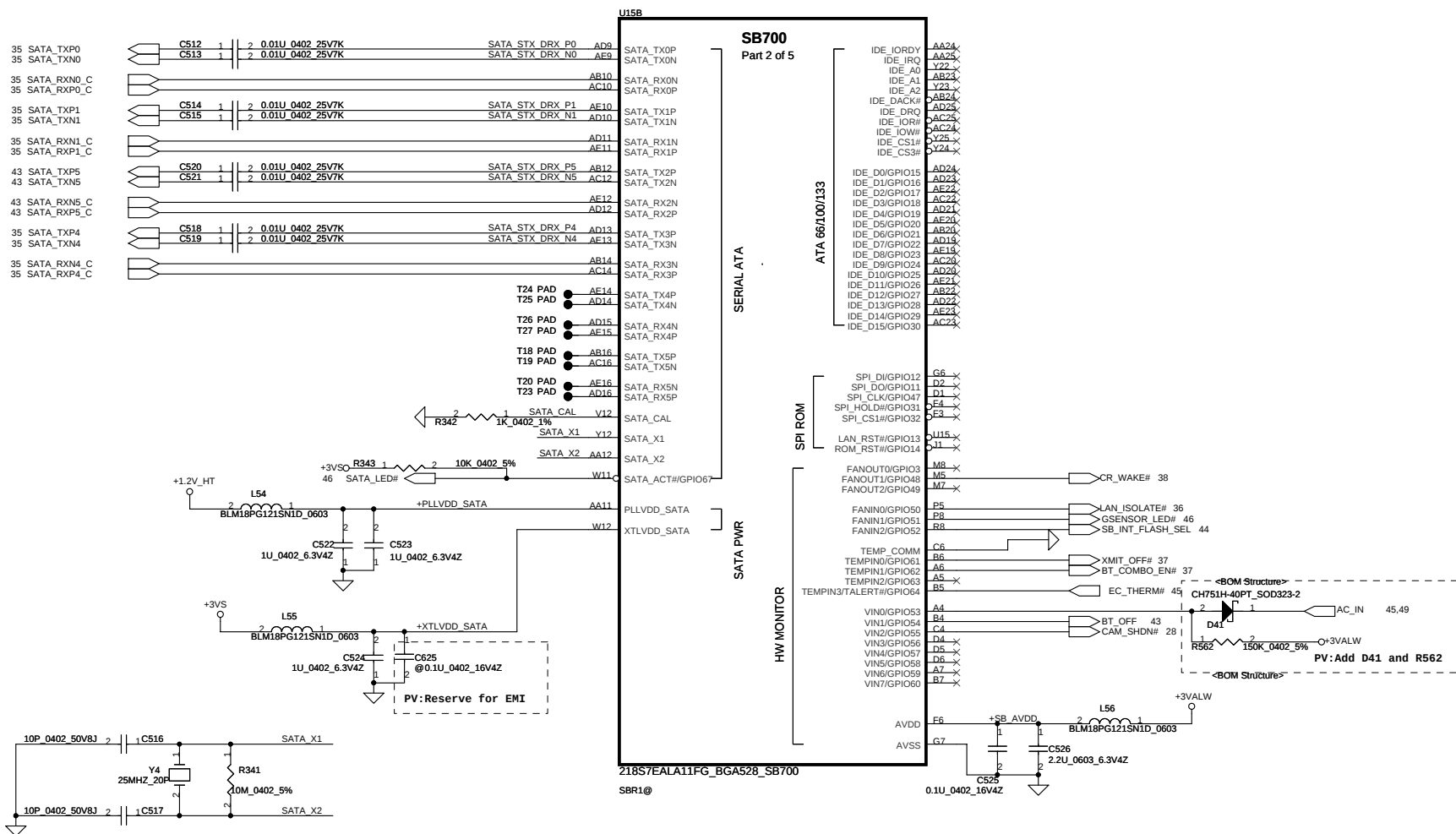
LPC

RTC XTAL

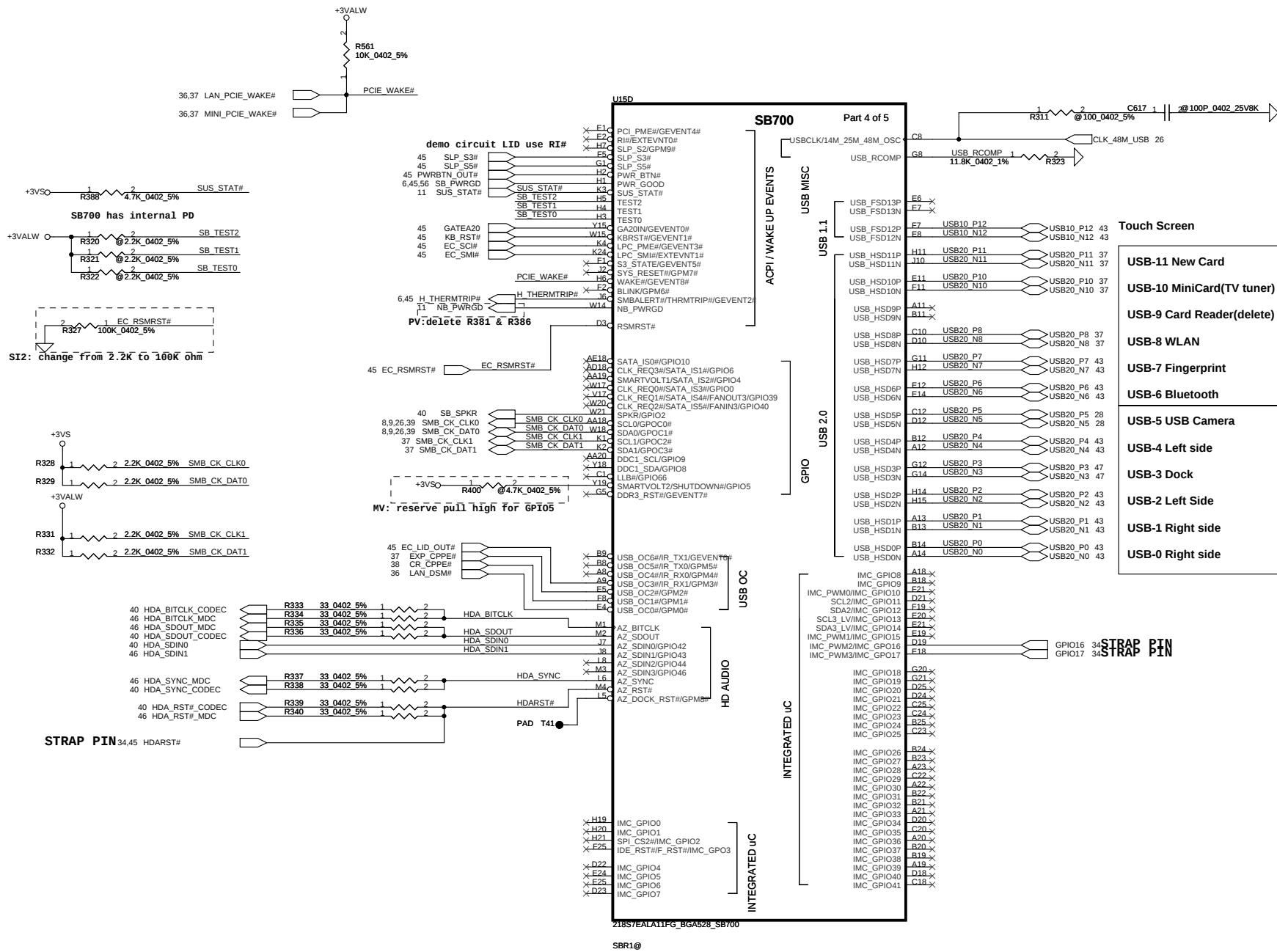
CPU



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2007/08/02				2008/08/02				Compal Electronics, Inc.			
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Touch Screen

USB-11 New Card

USB-10 MiniCard(TV tuner)

USB-9 Card Reader(delete)

USB-8 WLAN

USB-7 Fingerprint

USB-6 Bluetooth

USB-5 USB Camera

USB-4 Left side

USB-3 Dock

USB-2 Left Side

USB-1 Right side

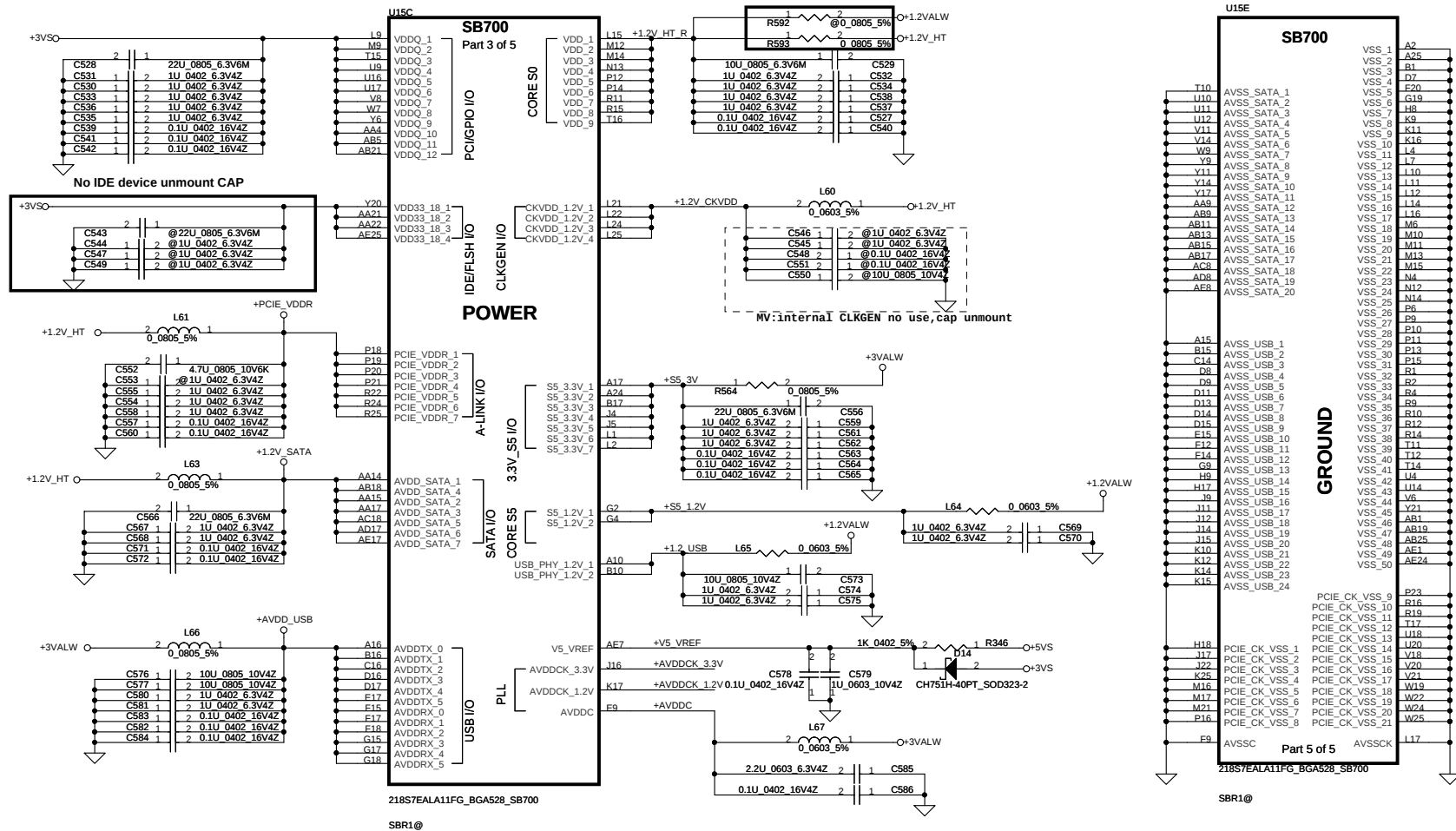
USB-0 Right side

STRAP PIN

21857EAL11FG_BGA528_SB700

SBR1@

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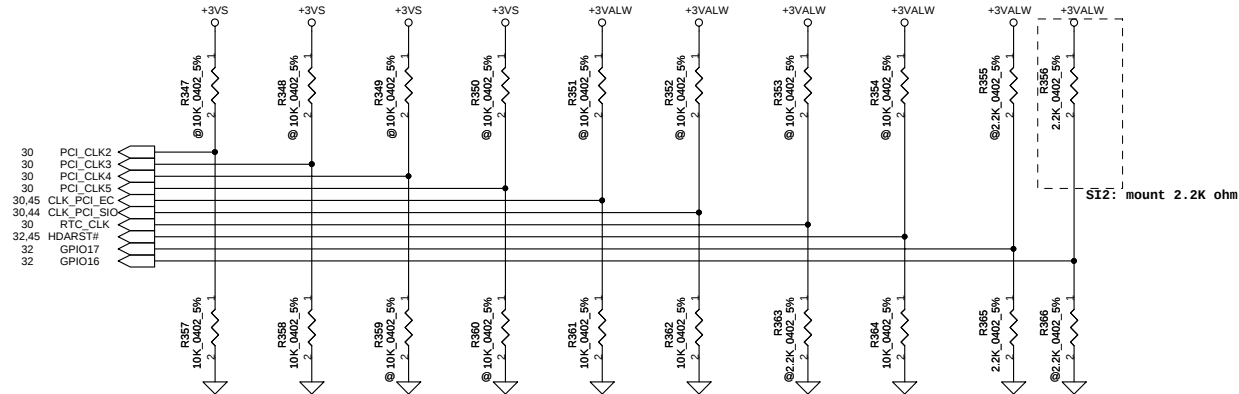
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Compal Electronics, Inc.
SCHEMATICS, MB A4093

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

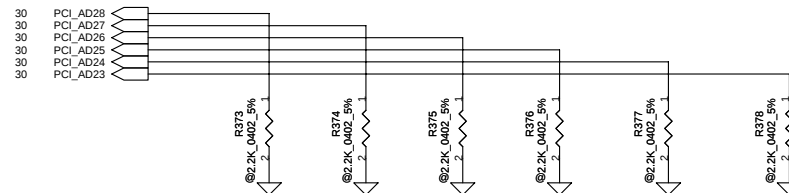
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	



DEBUG STRAPS

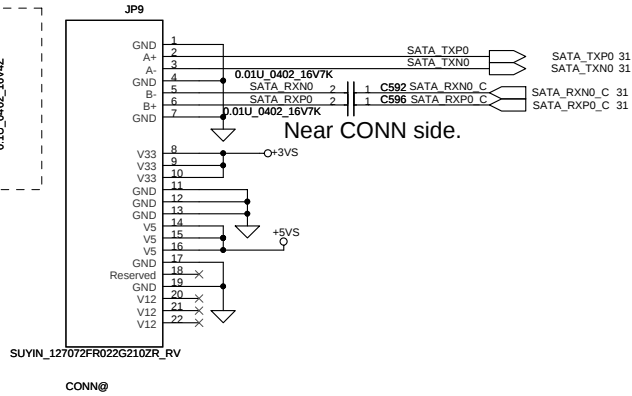
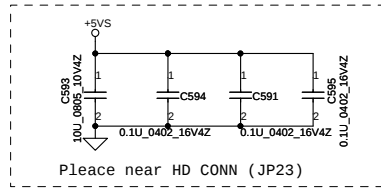
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

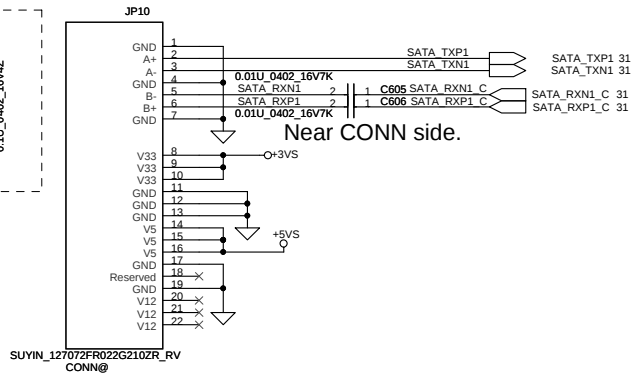
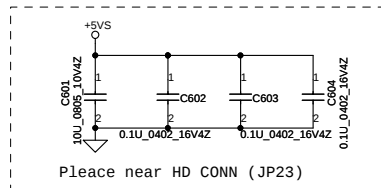


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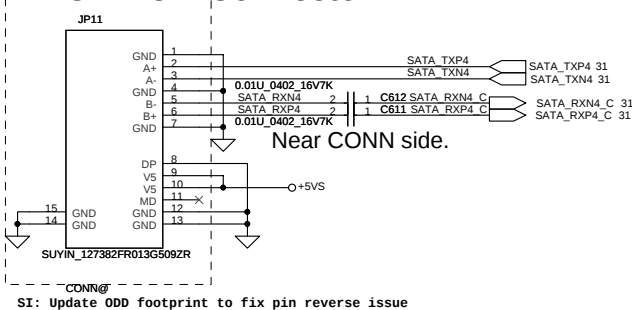
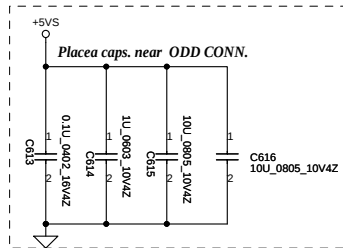
HDD Connector



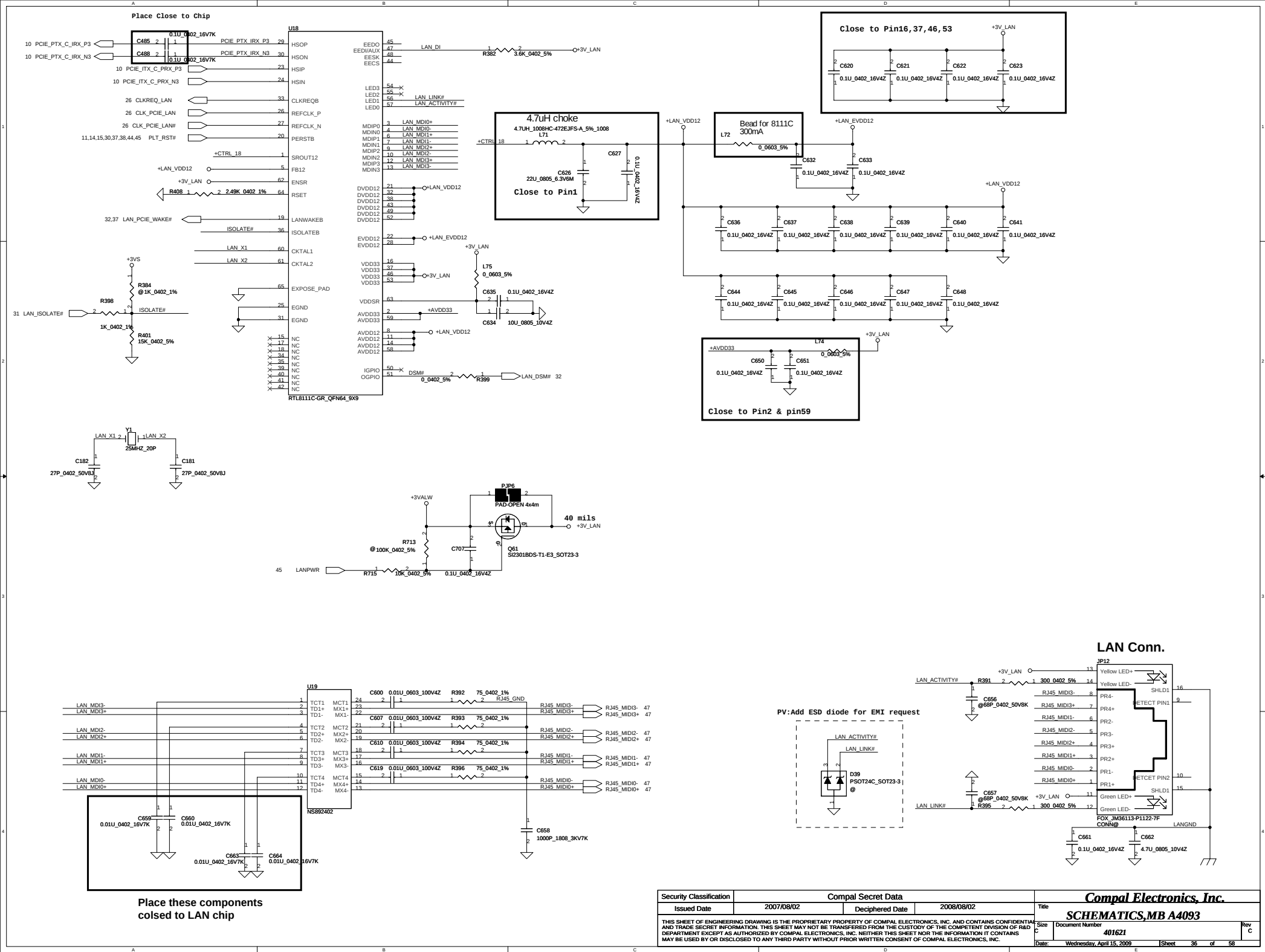
2nd HDD Connector-option



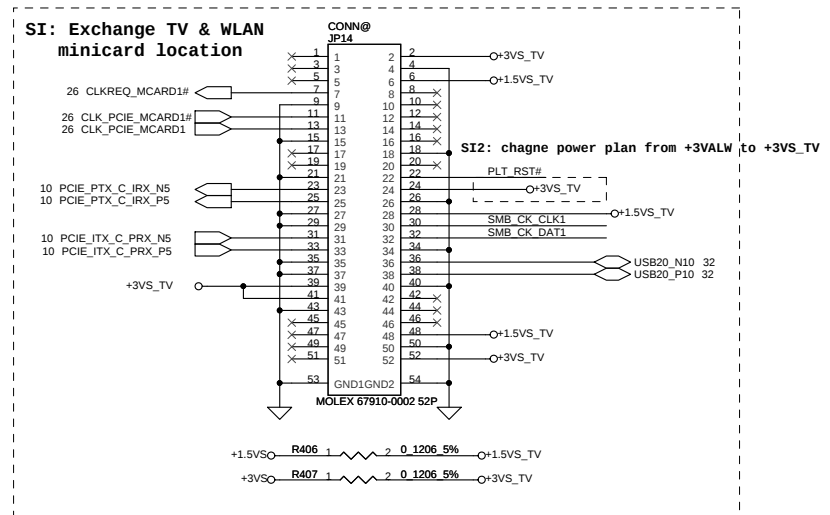
CD-ROM Connector



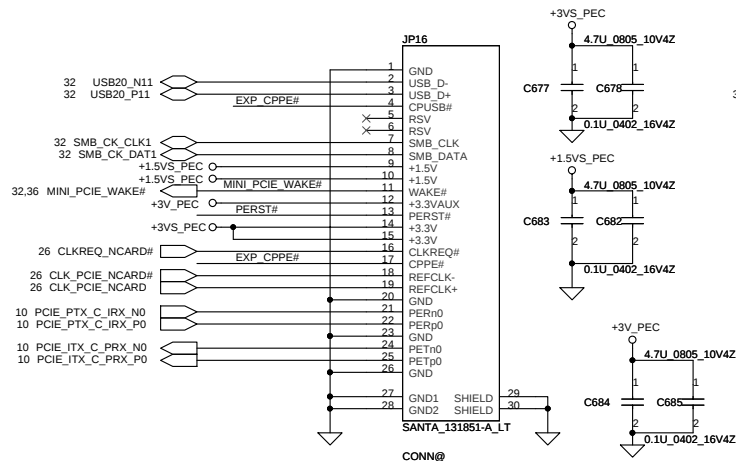
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SI2: chagne power plan from +3VALW to +3VS_TV



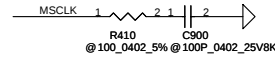
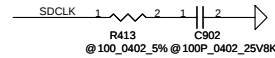
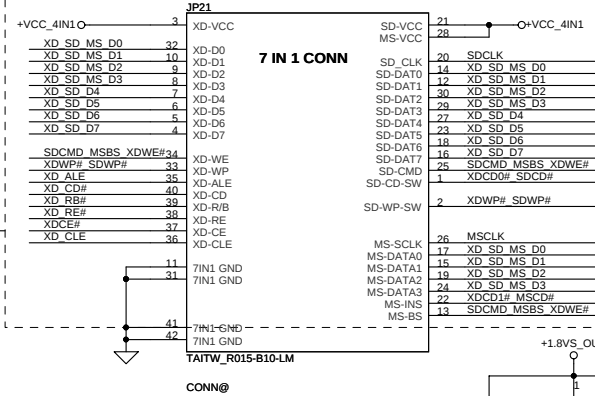
Near to Express Card slot.



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SI:Per ME request change
JP21 to new one

Card Reader Connector

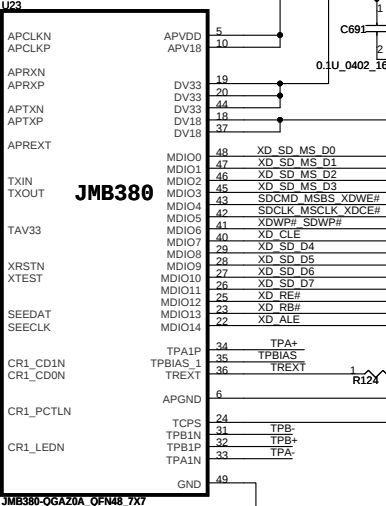


SI:Per Jmicro request change
R405 & R122 from 200K to 10K

SI2:Support D3E function

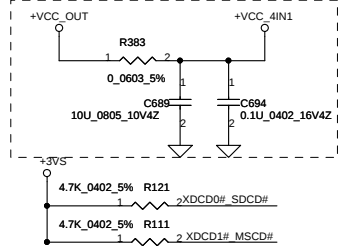
SI:Use build in Regulator
Chip unmount R387

Power Circuit



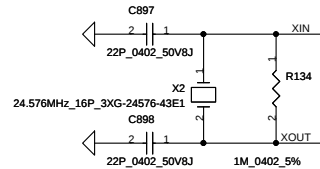
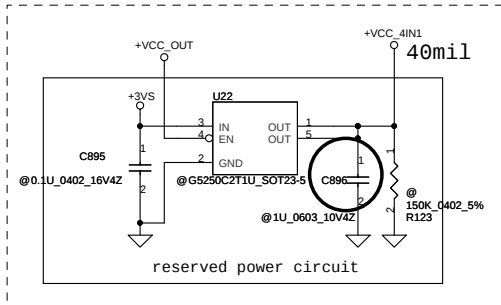
SI2: Use B version chip

SI:Use build in Regulator
Chip mount R383,C689,C694

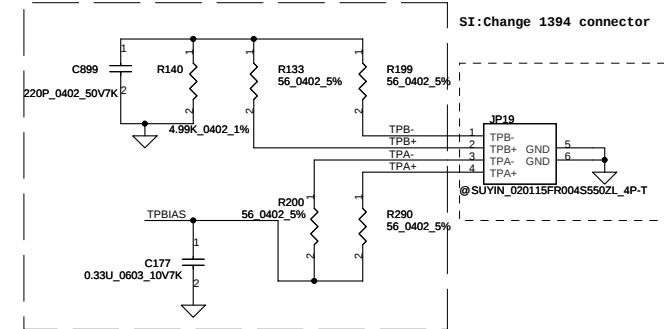


SI:Use new chip ,change to
High active control

SI:Use build in Regulator
Chip unmount U22 and relation parts



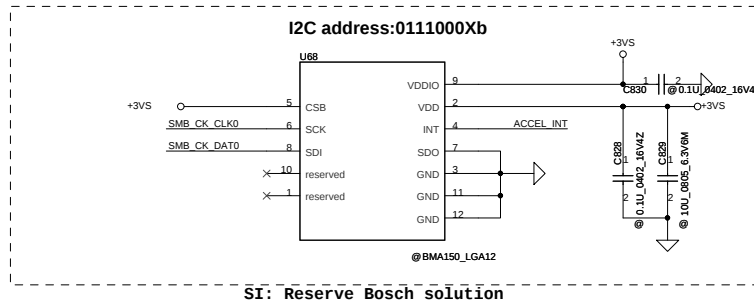
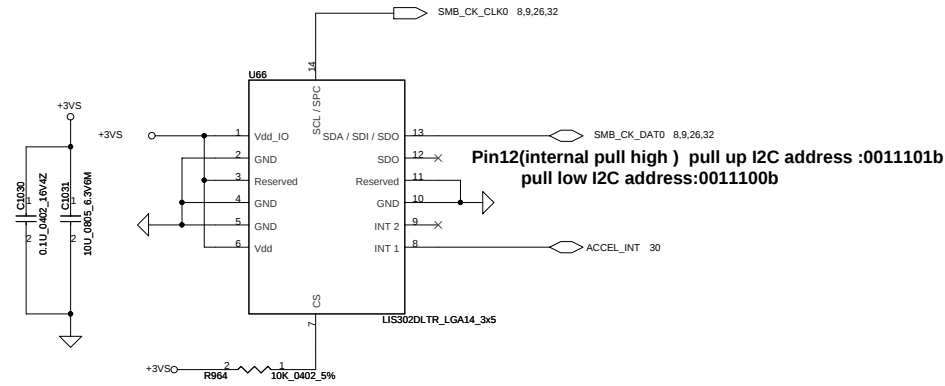
Close to Chip



SI:Change 1394 connector

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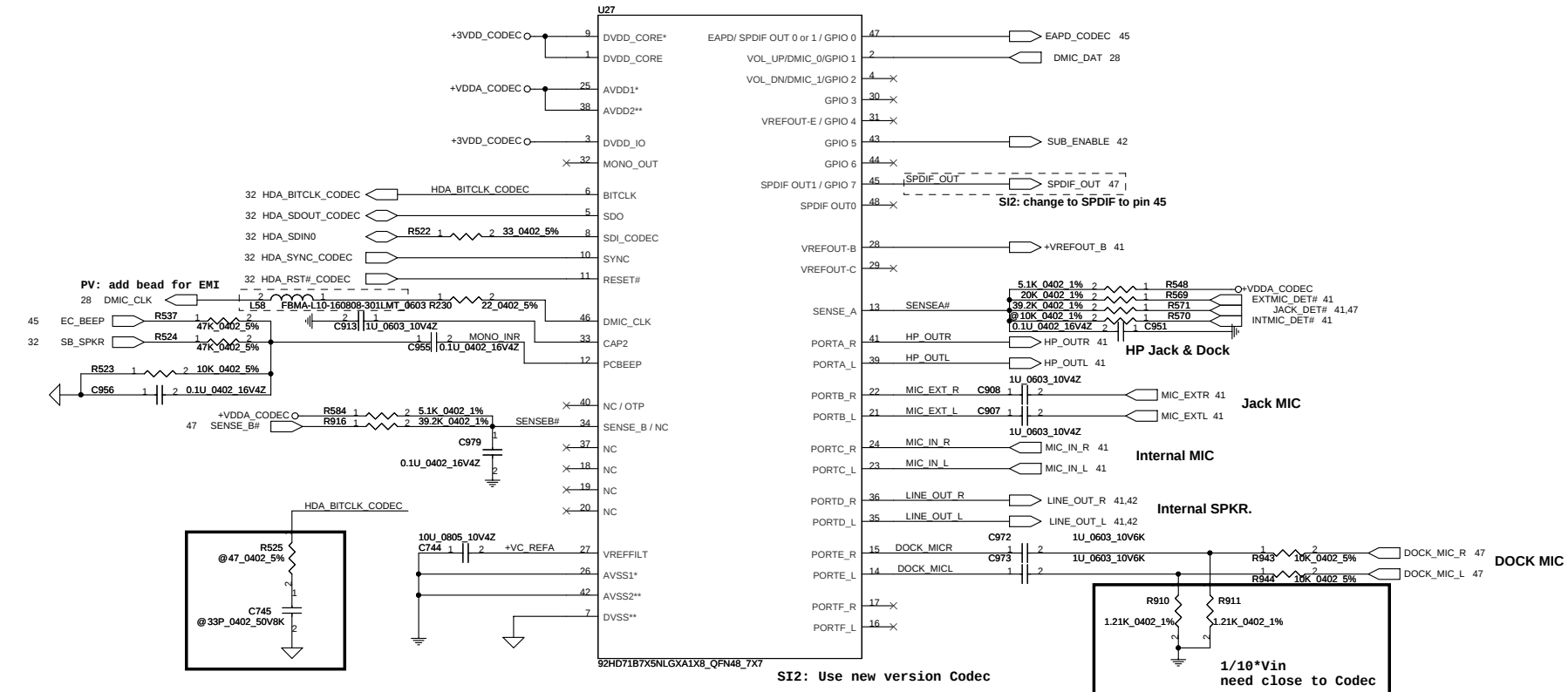
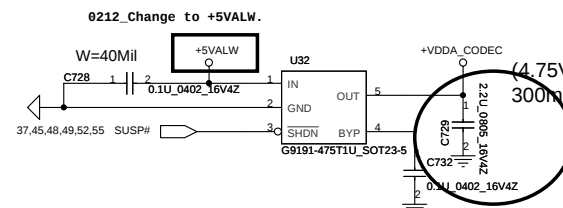
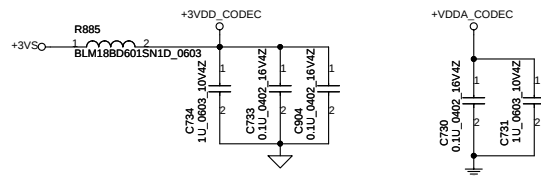
ACCELEROMETER



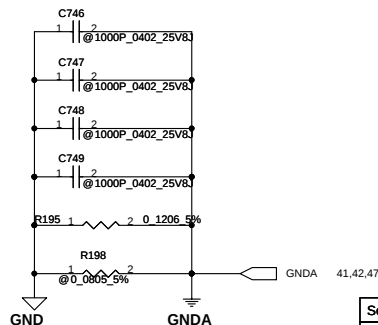
SI: Reserve Bosch solution

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CODEC POWER

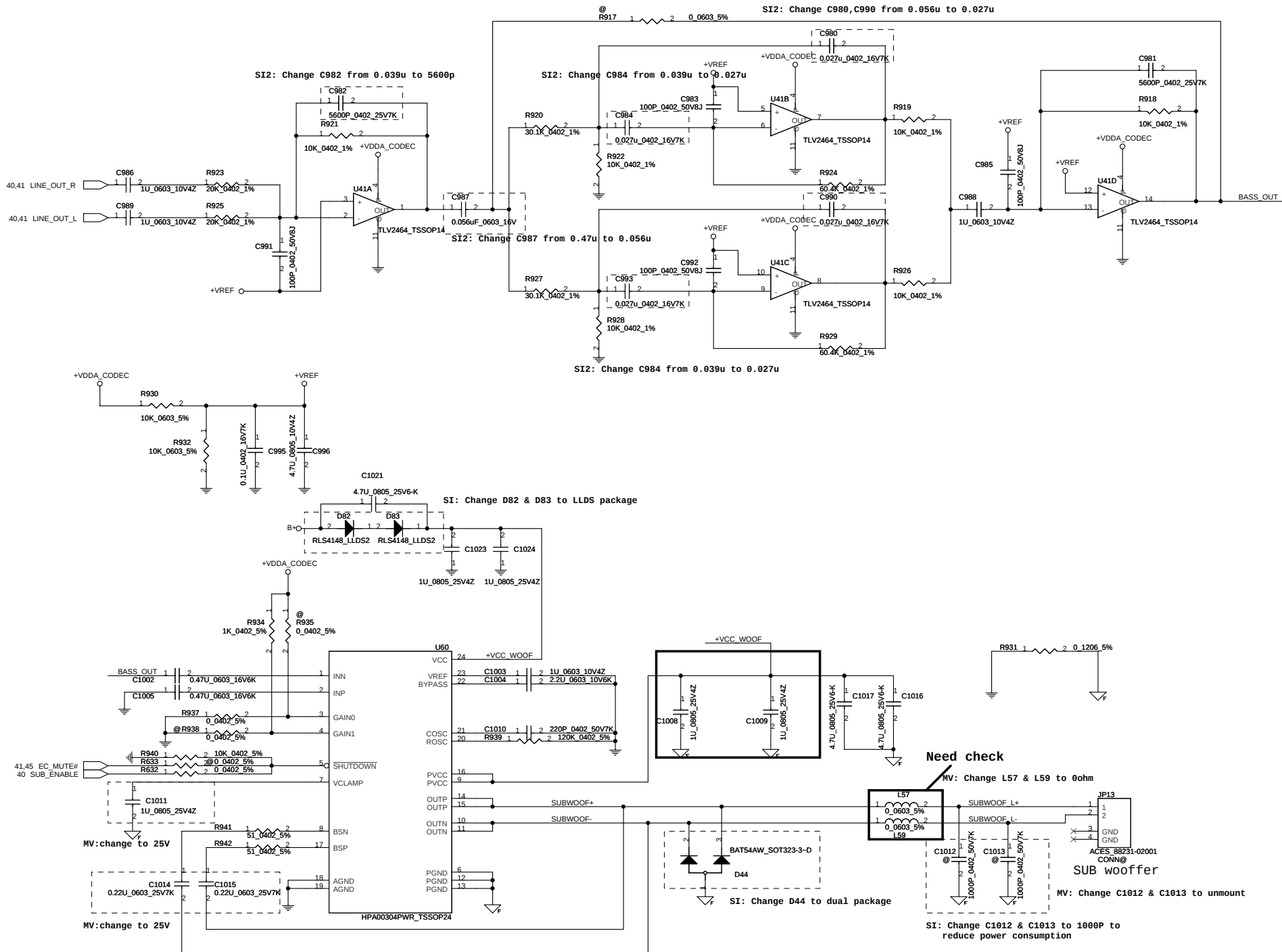


SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K



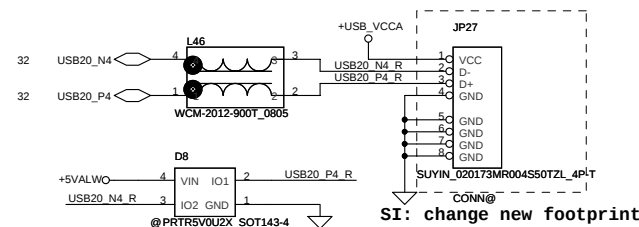
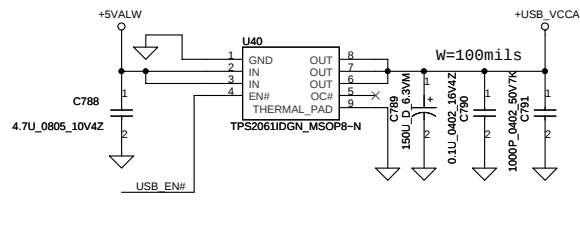
HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

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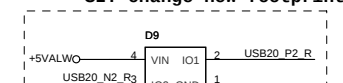
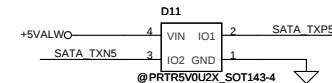
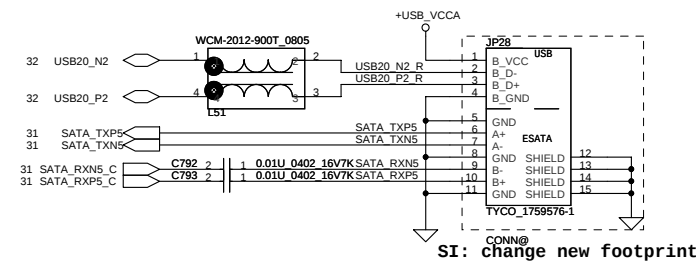


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Left side USB CONNECTOR 0

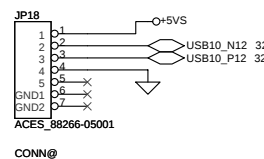


Left side ESATA/USB combination Connector

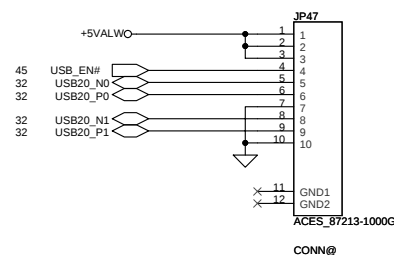


SI: new add for ESD

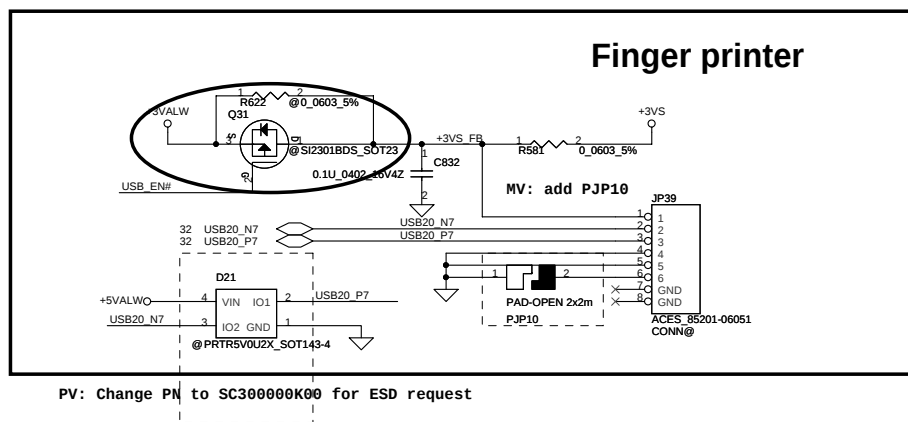
Touch screen



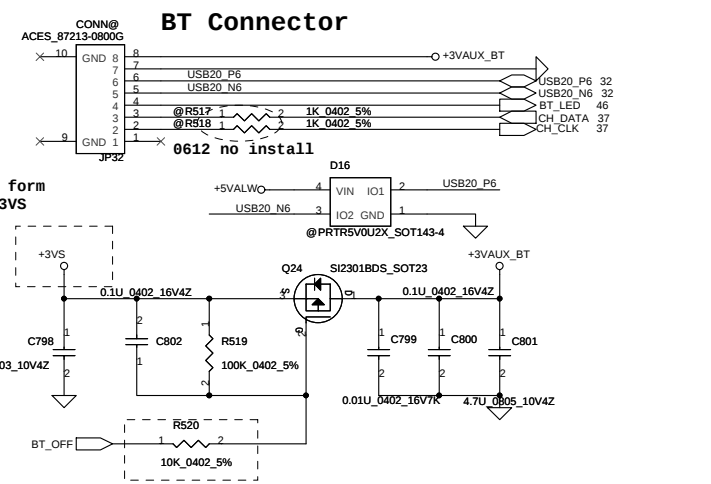
USB Board Conn



Finger printer



BT Connector

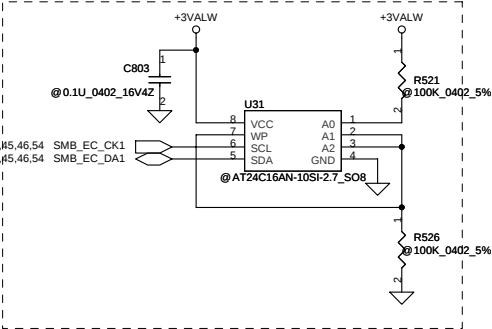


SI: change to 10K ohm to make sure MOS can turn on

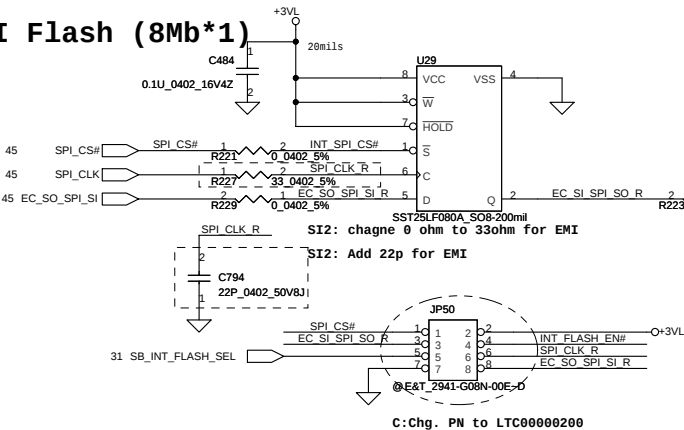
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SCHEMATICS, MB A4093

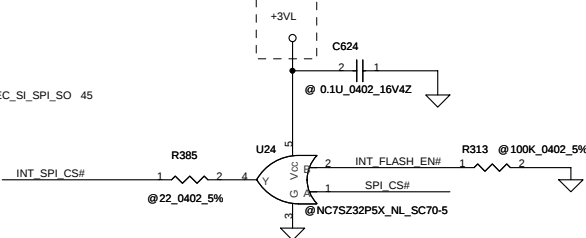
SI2: Change from +3VL to +3VALW and unmount this EEPROM



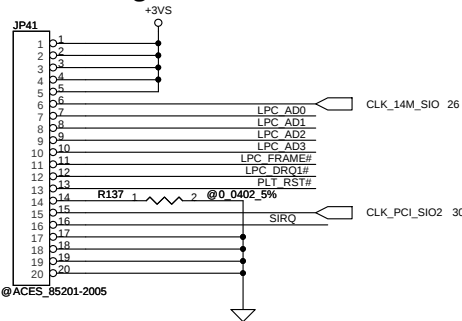
SPI Flash (8Mb*1)



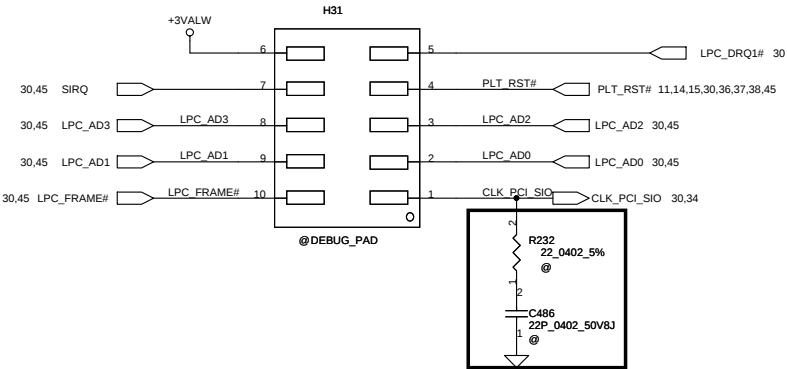
SI2: Change from +3VALW to +3VL



LPC Debug Port



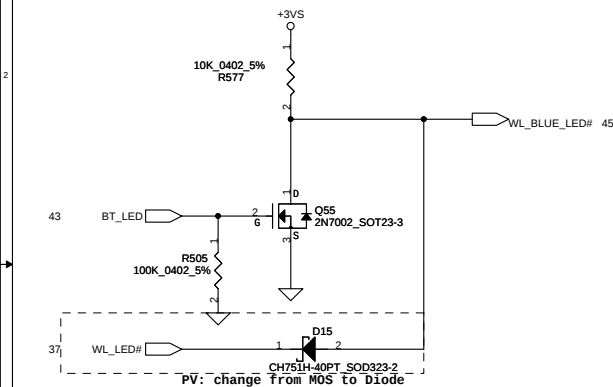
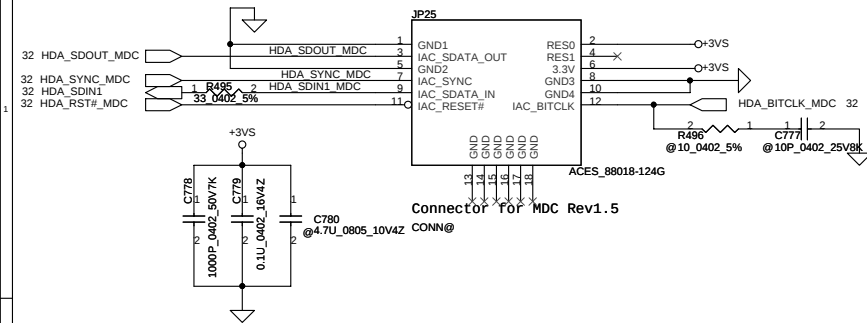
LPC Debug Port



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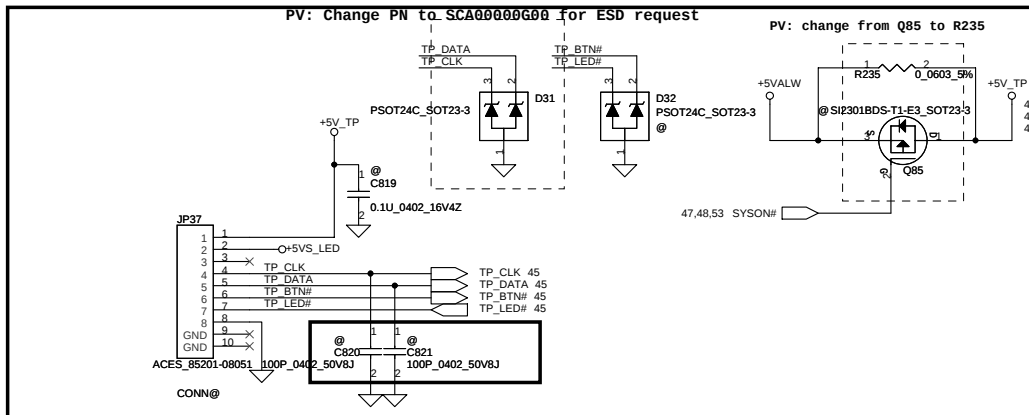
MDC 1.5 Conn.

Change type 4/25



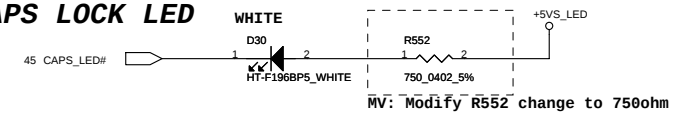
T/P Board (Include T/P_ON/OFF)

PV: Change PN to SCA0000000 for ESD request



PV: change from Q85 to R235

CAPS LOCK LED



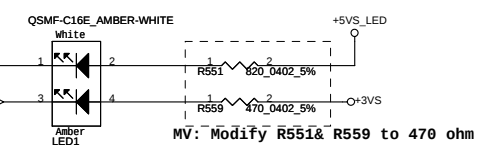
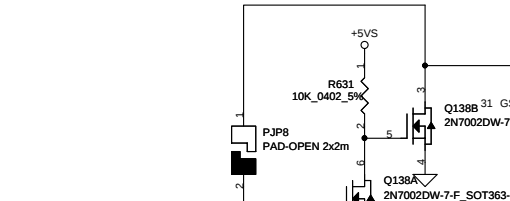
POWER LED(Left 1)



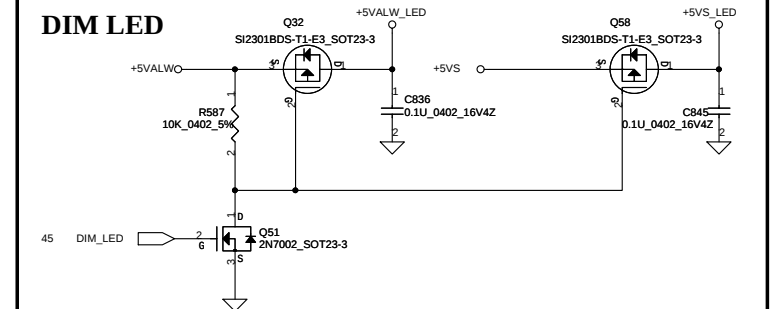
Battery Charge LED(Left 2)



HDD LED(Left 3)



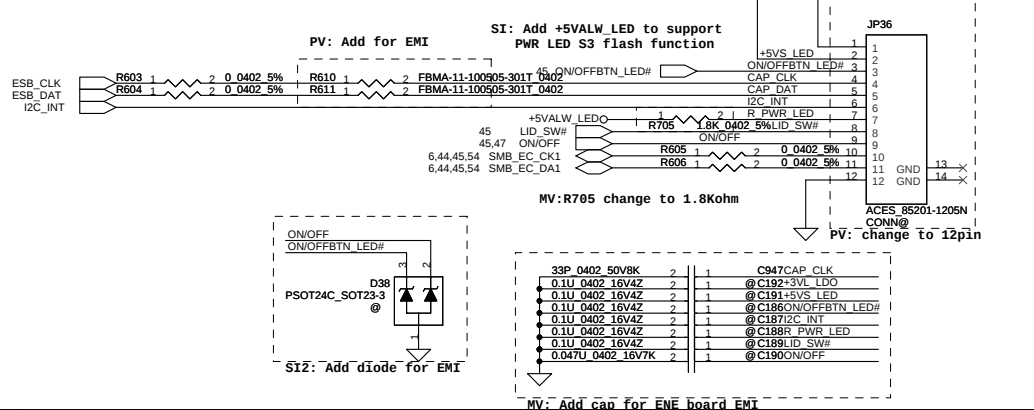
DIM LED



SI: Change to +3VL to support Qplay bottom boot in BATT mode

SWITCH BOARD.

MV: Add cap for ENE board EMI



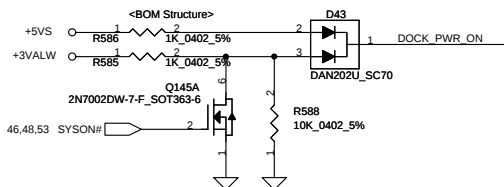
SI: Add +5VALW_LED to support PWR LED S3 flash function

33P 0402 50V8K	2	1	C947CAP CLK
0.1U 0402 16V4Z	2	1	@C192+3VL LDO
0.1U 0402 16V4Z	2	1	@C191+5VS LED
0.1U 0402 16V4Z	2	1	@C186ON/OFFBTN_LED#
0.1U 0402 16V4Z	2	1	@C187I2C INT
0.1U 0402 16V4Z	2	1	@C188R PWR LED
0.1U 0402 16V4Z	2	1	@C189LID SW#
0.047U 0402 16V7K	2	1	@C190ON/OFF

MV: Add cap for ENE board EMI

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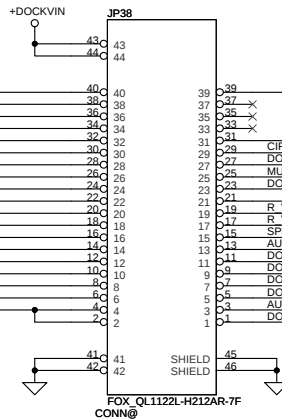
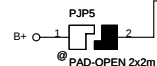
Atlas/ Saturn Dock



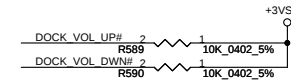
DOCK_PWR_ON Spec

0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on

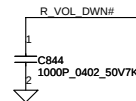
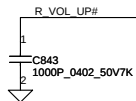
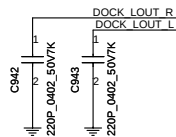
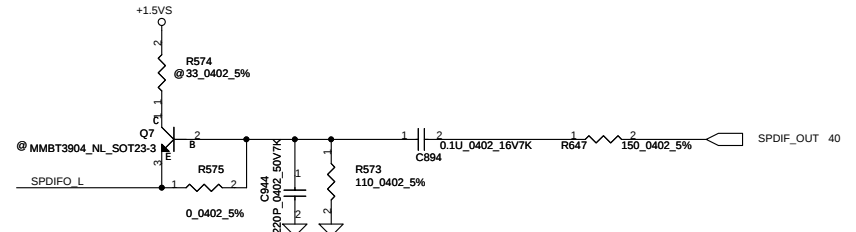
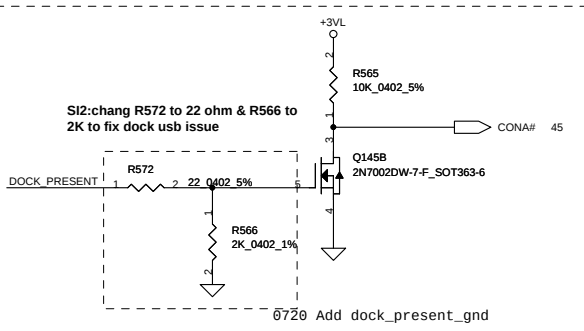
27 GREEN_L
27 RED_L
27 BLUE_L
27 D_HSYNC
27 D_DDCLK
32 USB20_N3
27 D_VSYNC
32 USB20_P3
36 RJ45_MIDI3+
36 RJ45_MIDI3-
36 RJ45_MIDI2+
36 RJ45_MIDI2-
36 RJ45_MIDI1+
36 RJ45_MIDI1-
36 RJ45_MIDI0+
36 RJ45_MIDI0-



need change to reverse type connector

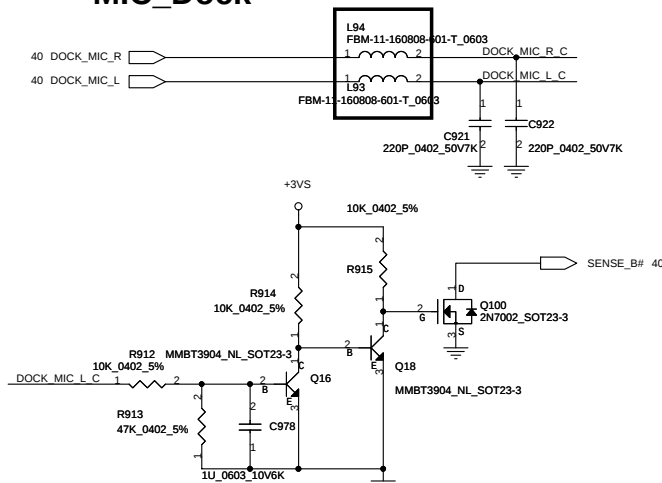


MUTE_LED 45
DOCK_SLP_BTN# 45,46
JACK_DET# 40,41
DOCK_VOL_UP# 45
DOCK_VOL_DWN# 45



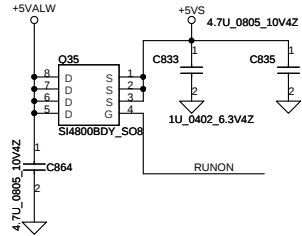
MIC_Dock

Need 600 Ohm 500 mA

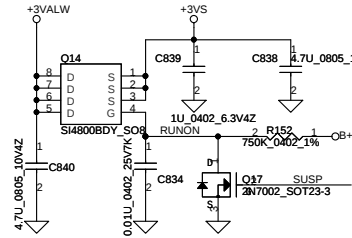


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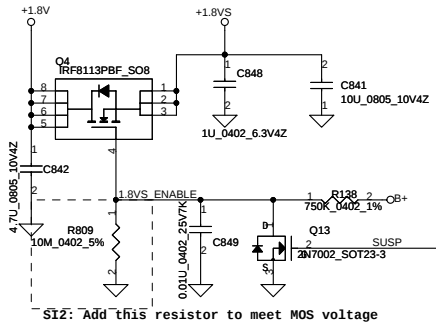
+5VALW TO +5VS



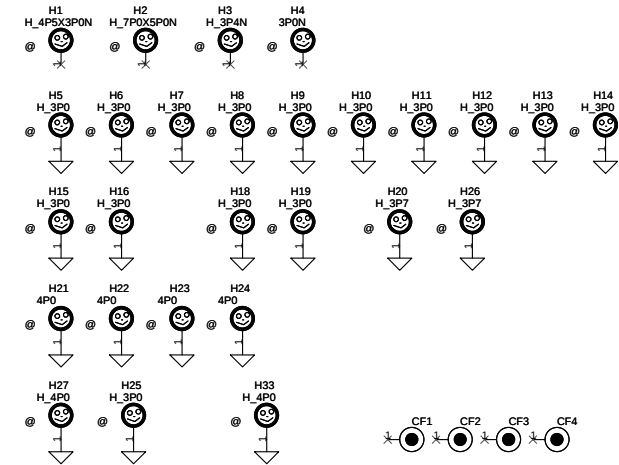
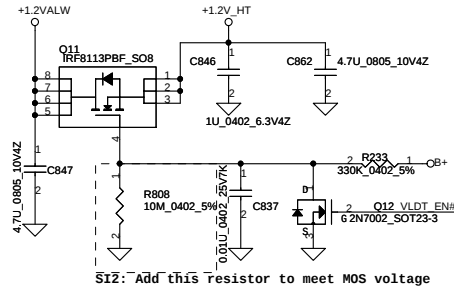
+3VALW TO +3VS



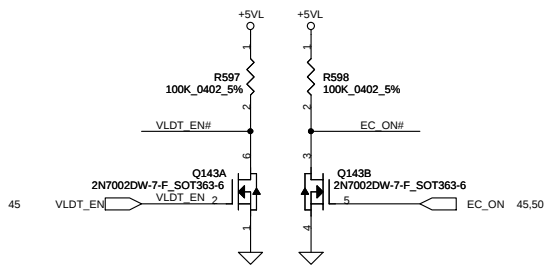
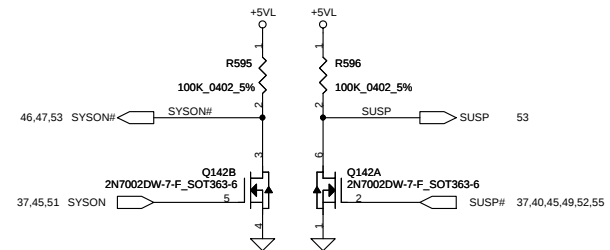
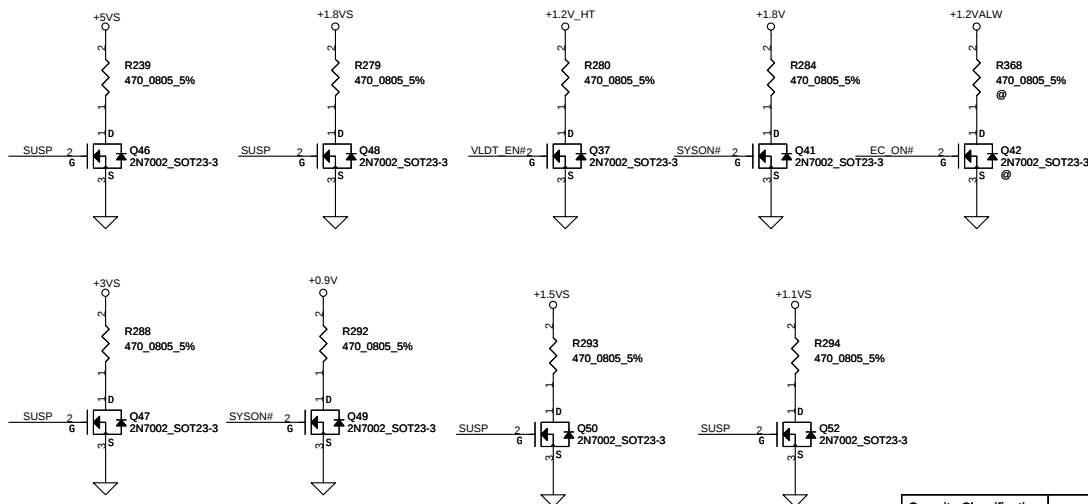
+1.8V TO +1.8VS



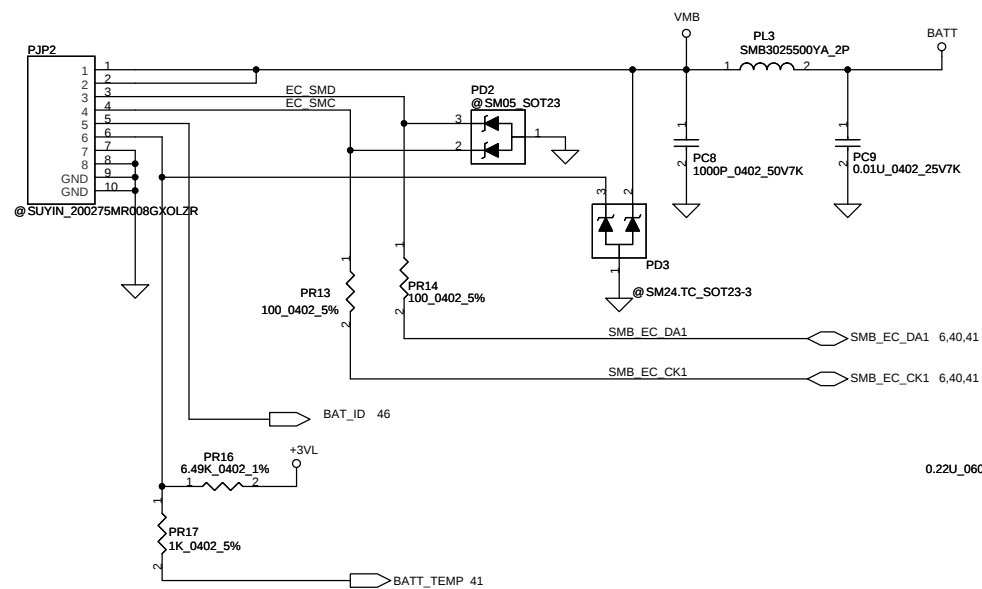
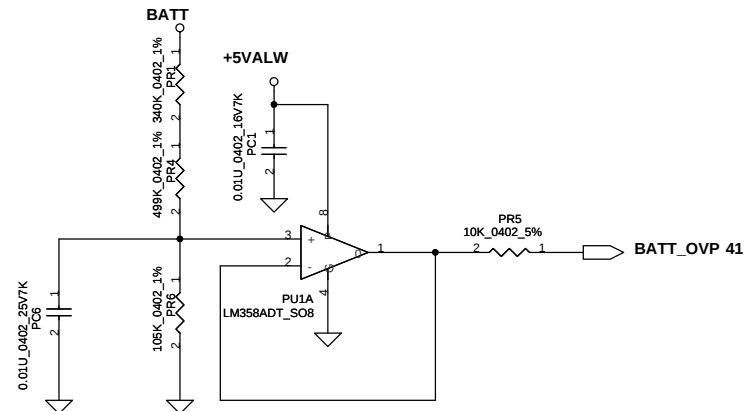
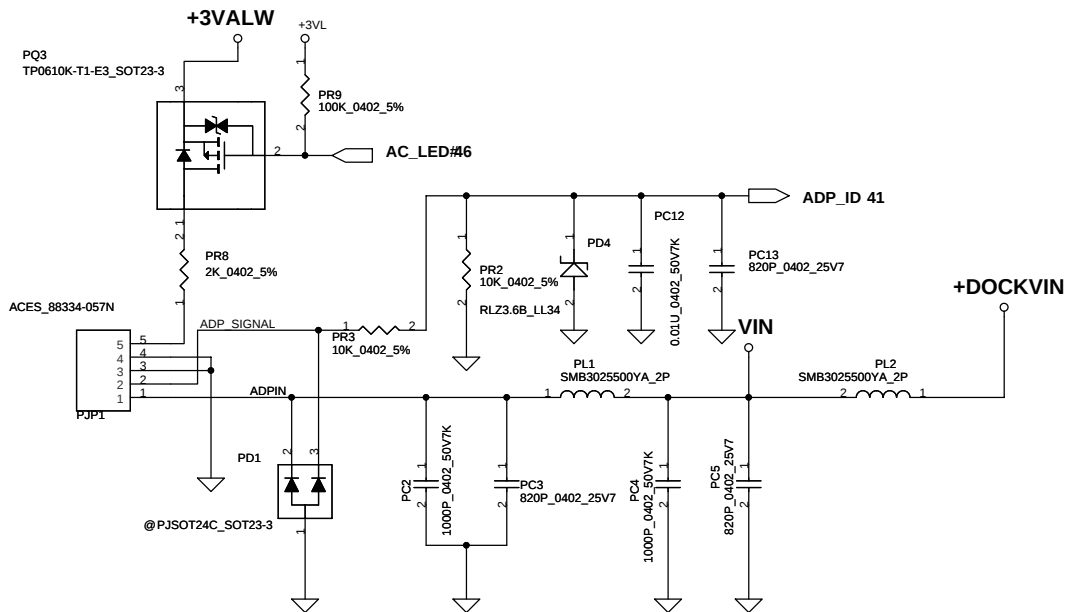
+1.2VALW TO +1.2V_HT



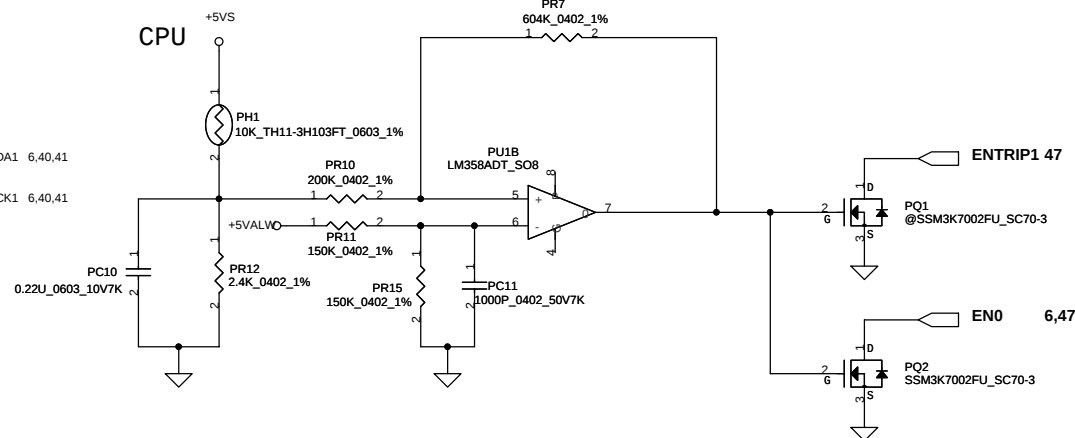
Discharge circuit



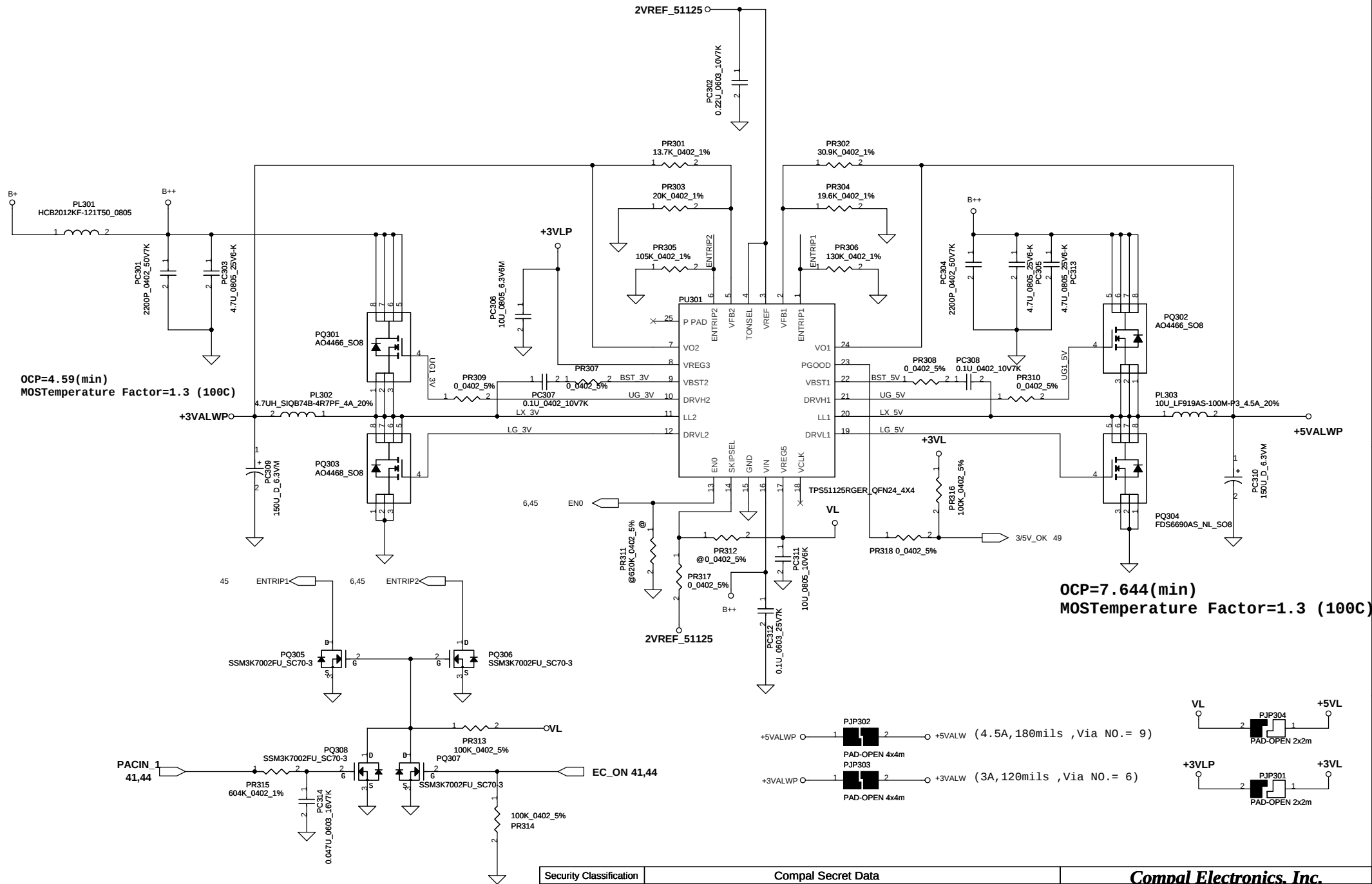
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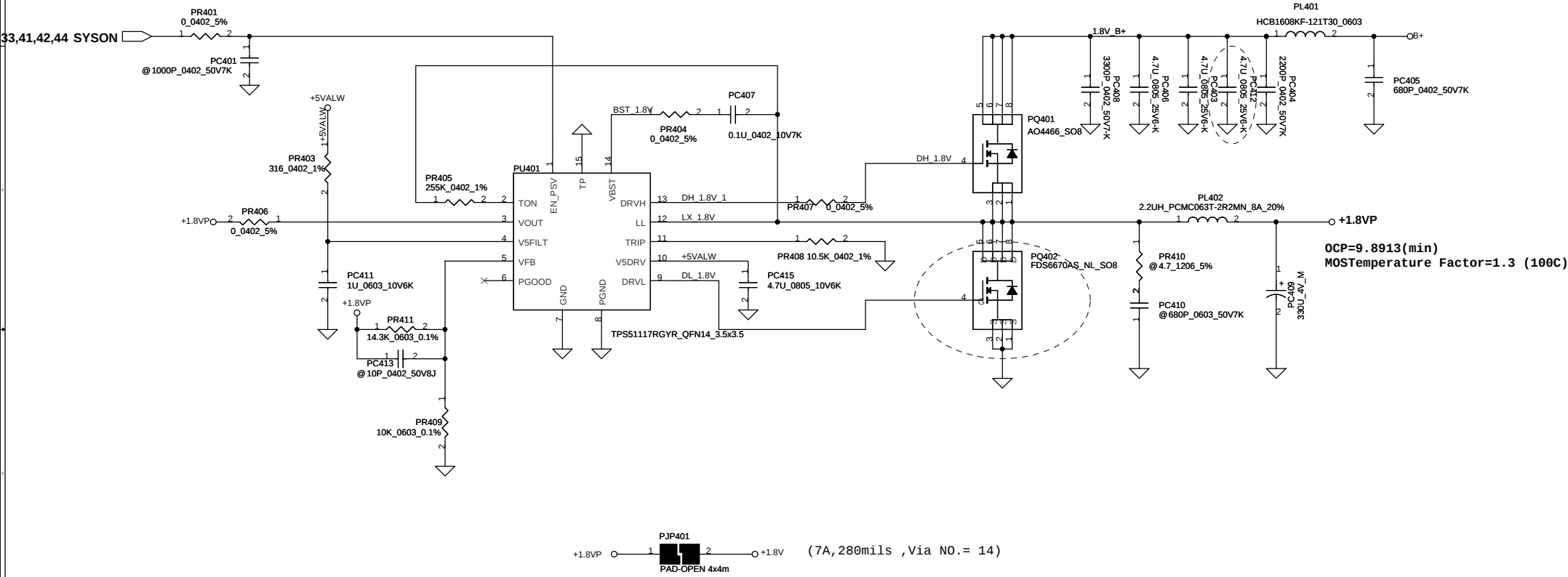
PH1 under CPU bottom side :
CPU thermal protection at 90 +-3 degree C



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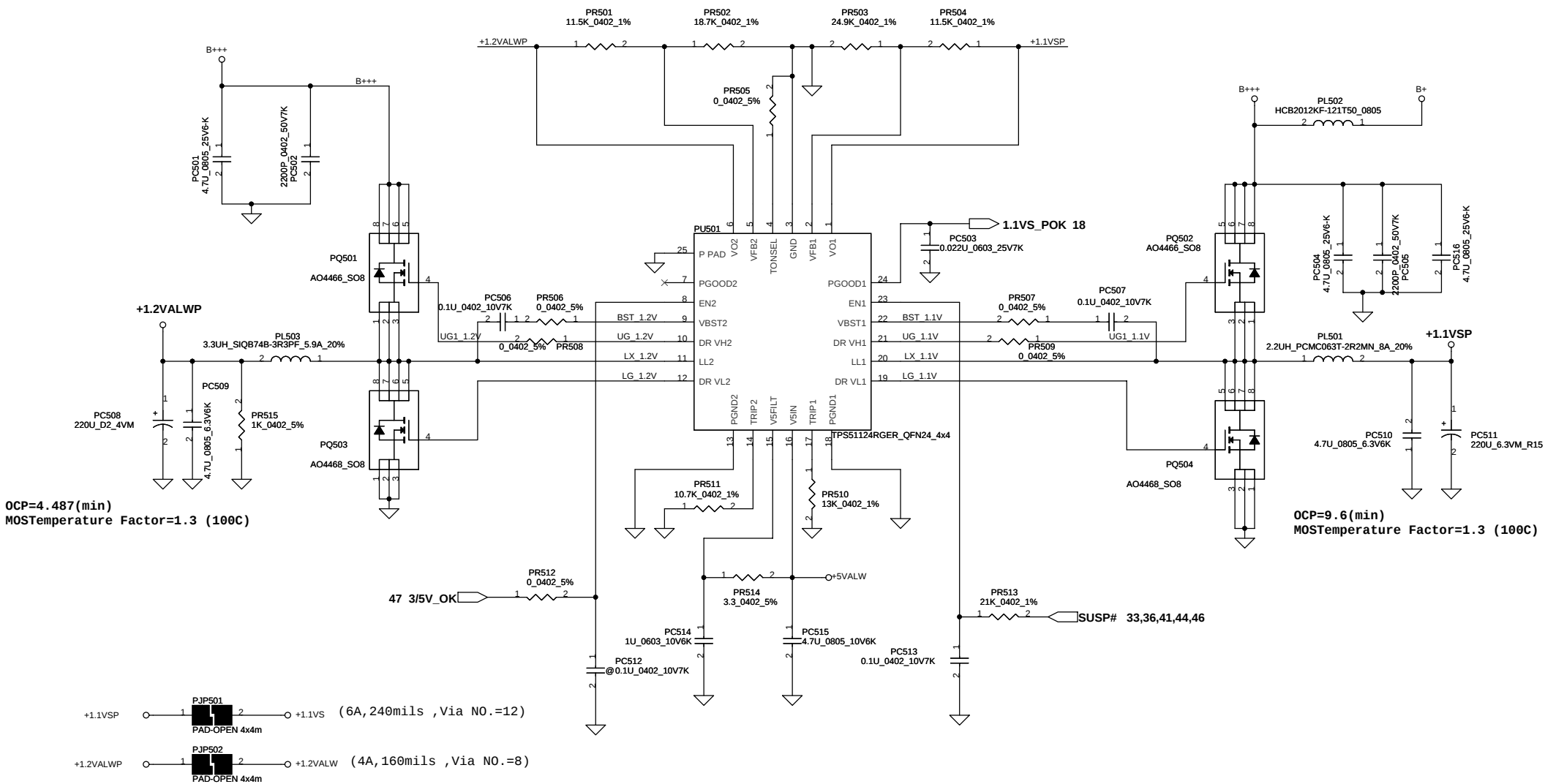


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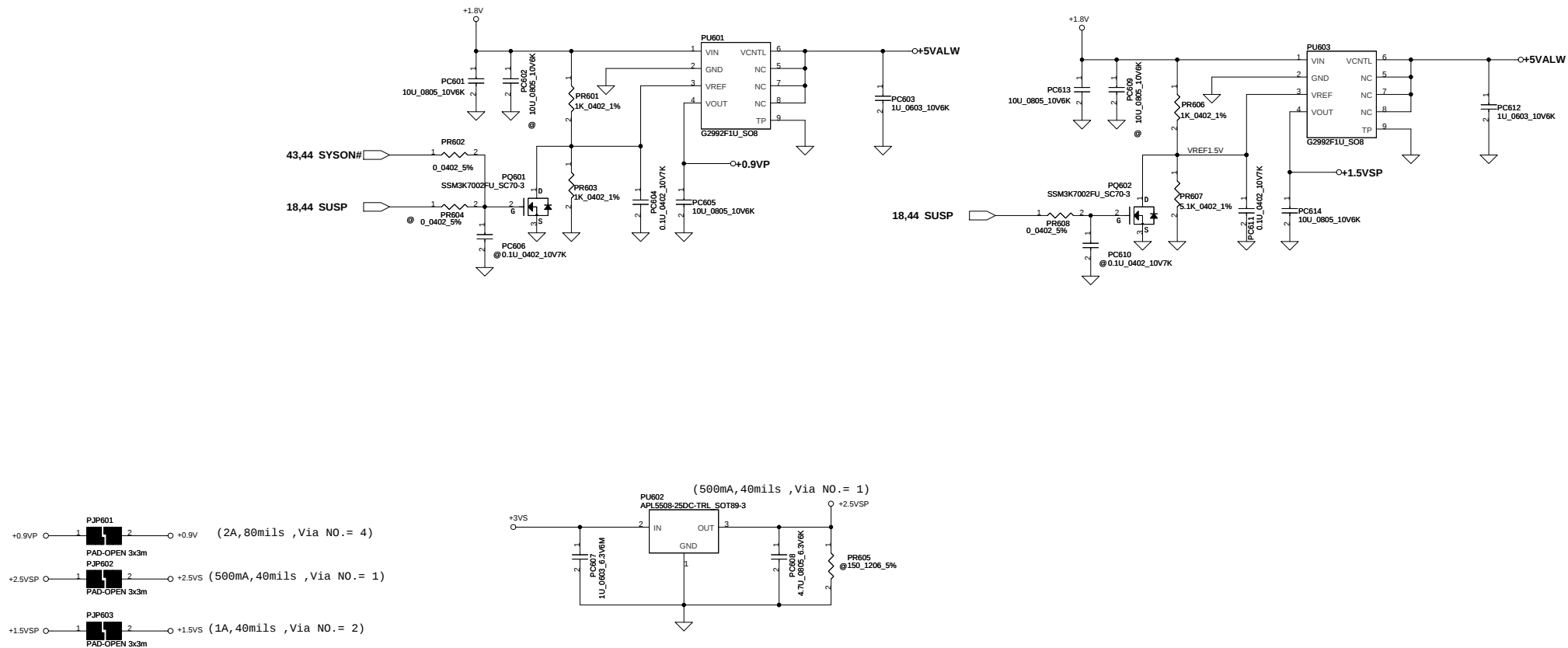


PJP401
PAD-OPEN 4x4mm
+1.8VP 1 2 +1.8V (7A,280mils ,Via N0.= 14)

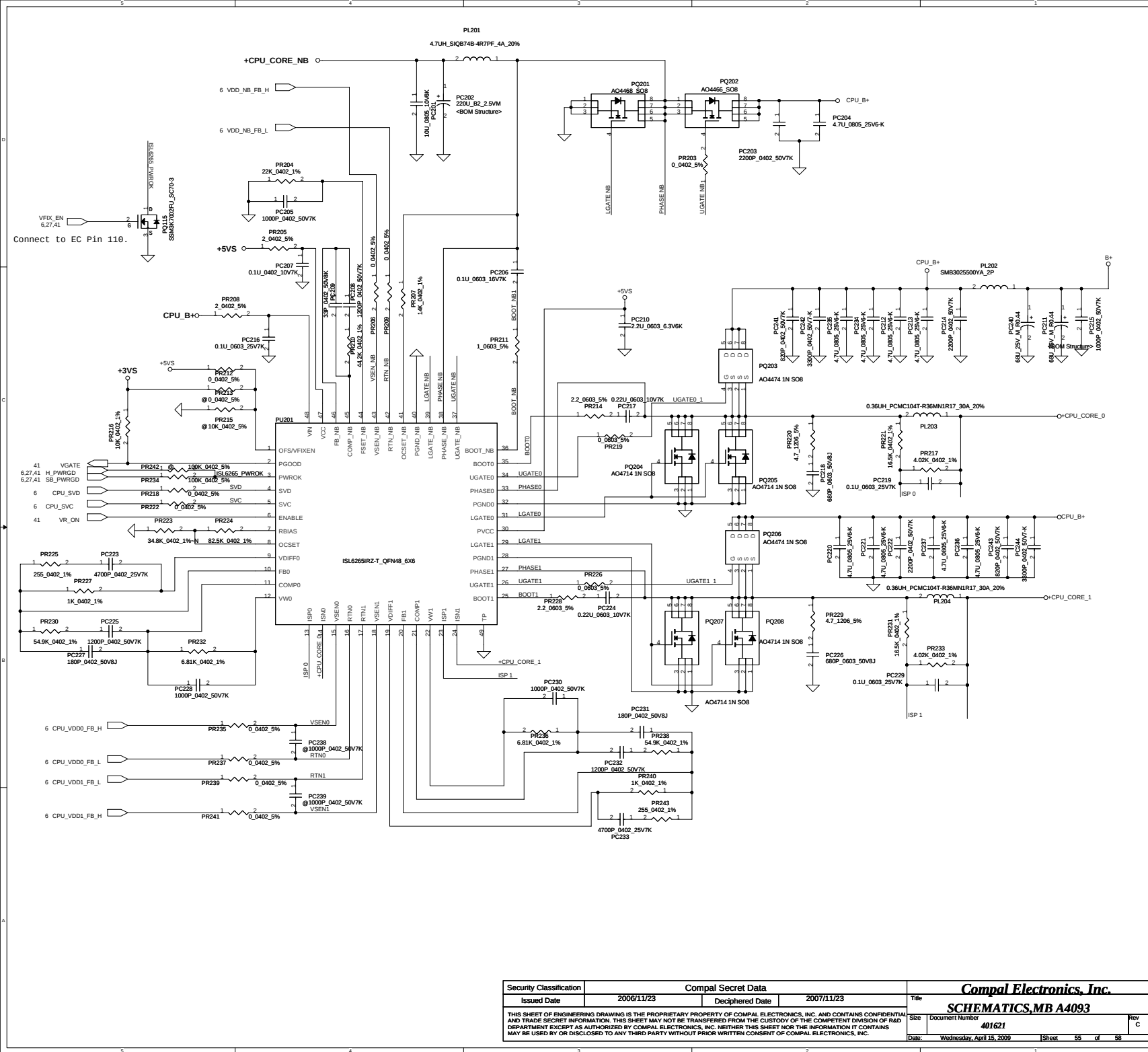
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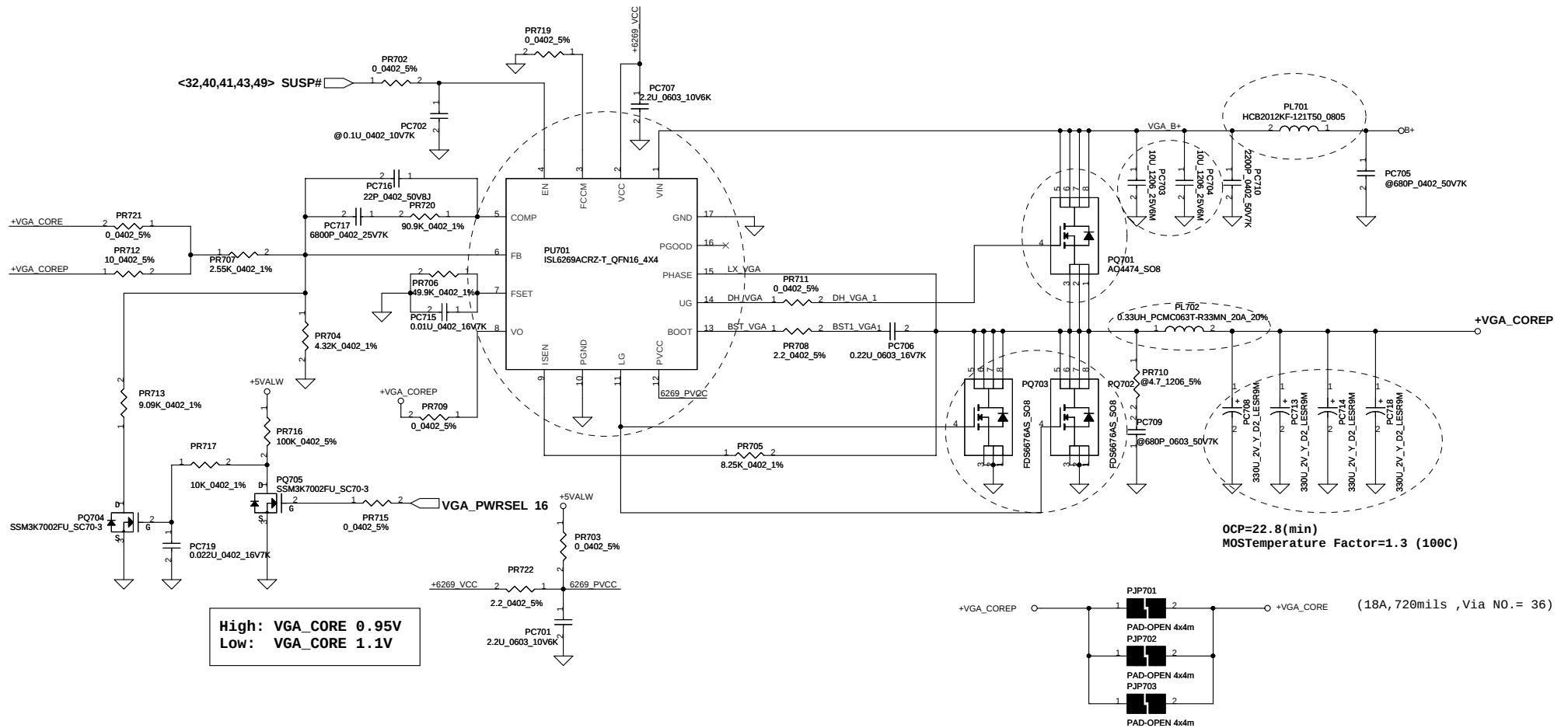
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