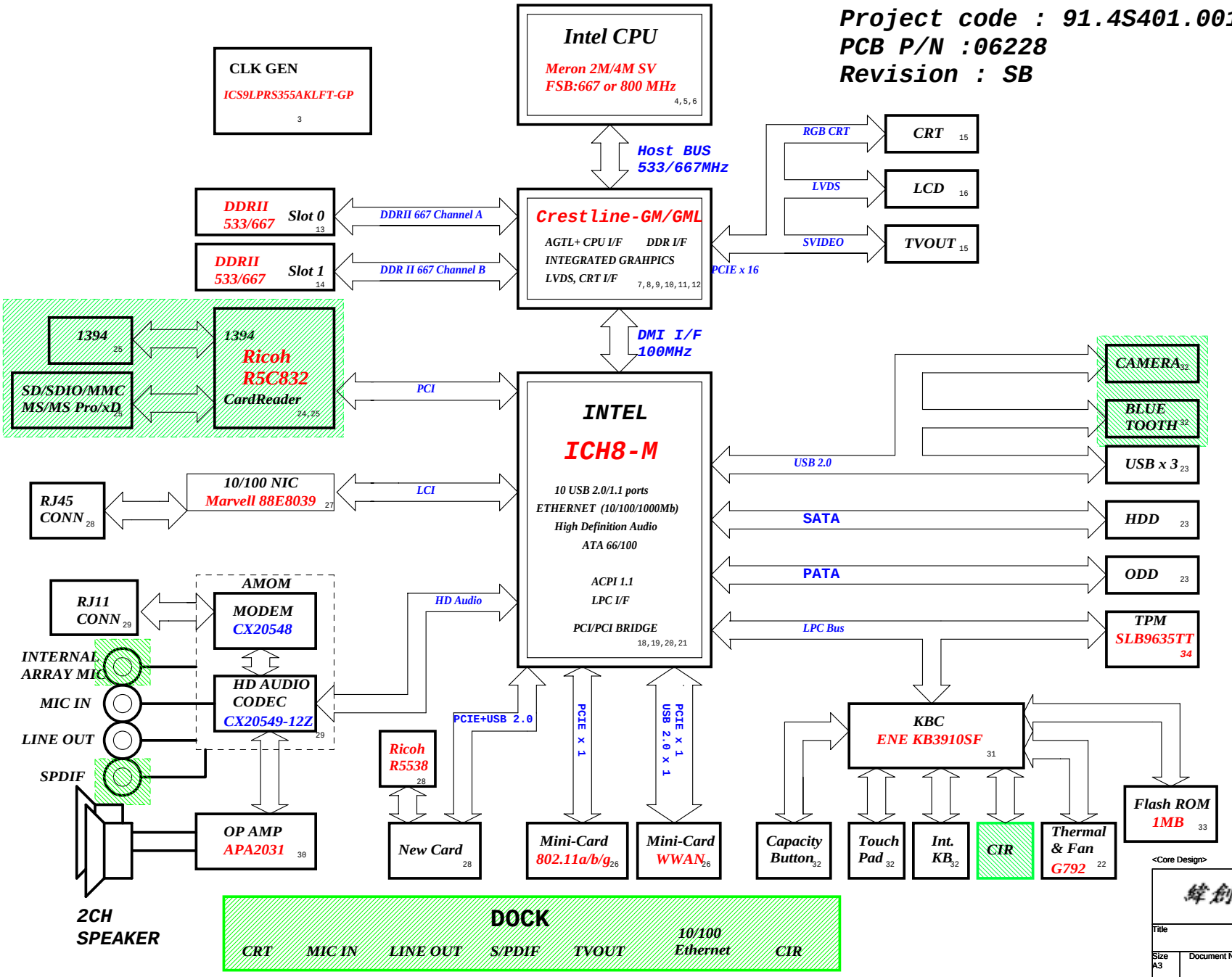
Pamirs UMA Block Diagram

Project code : 91.4S401.001
PCB P/N :06228
Revision : SB



SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_AUX_S5

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S0 1D8V_S3

SYSTEM DC/DC ISL6269CRZ	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8736ETL	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

<Core Design>

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Title: Block Diagram
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INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD	tp3	AZ_DOUT_ICH	Description
0		0	RSVD
0		1	Enter XOR Chain
1		0	Normal Operation(default)
1		1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3	
low = A16 swap override enable	
high = default	

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

19,21	+RTCVCC
4,5,6,7,9,10,11,19,21,38,41	1D05V_S0
3,7,10,21,38	1D25V_S0
27	1D2V_LAN_S5
28	1D5V_NEW_S0
5,10,17,19,20,21,26,28,37,38,41	1D5V_S0
7,10,11,13,14,37,38,41	1D8V_S3
27,28	2D5V_LAN_S5
29,30	3D3V_AUD_S0
19,31,32,33,36,39,40	3D3V_AUX_S5
27,28	3D3V_LAN_S5
3,4,7,9,10,11,13,14,15,16,18,19,20,21,22,23,24,25,26,27,28,29,31,32,33,34,35,36,41	3D3V_S0
17,18,20,21,22,26,27,28,29,31,34,36,39,41	3D3V_S5
22,29,31,34,36	5V_AUX_S5
16,23,32,33,34,36,37,38	5V_S3
15,16,17,20,21,22,23,26,29,30,31,32,33,34,35,41	5V_S0
16,21,34,37,38	5V_S5
17,39,40,41	AD+
16,17,34,35,36,37,38,39,41	DCBATOUT
13,14,38,41	DDR_VREF_S0
7,13,14,38	DDR_VREF_S3
22,31,33,39	KBC_3D3V_AUX
16	LCDVDD_S0
5,6,35	VCC_CORE_S0

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reversed	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

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Title: **Table of Content**

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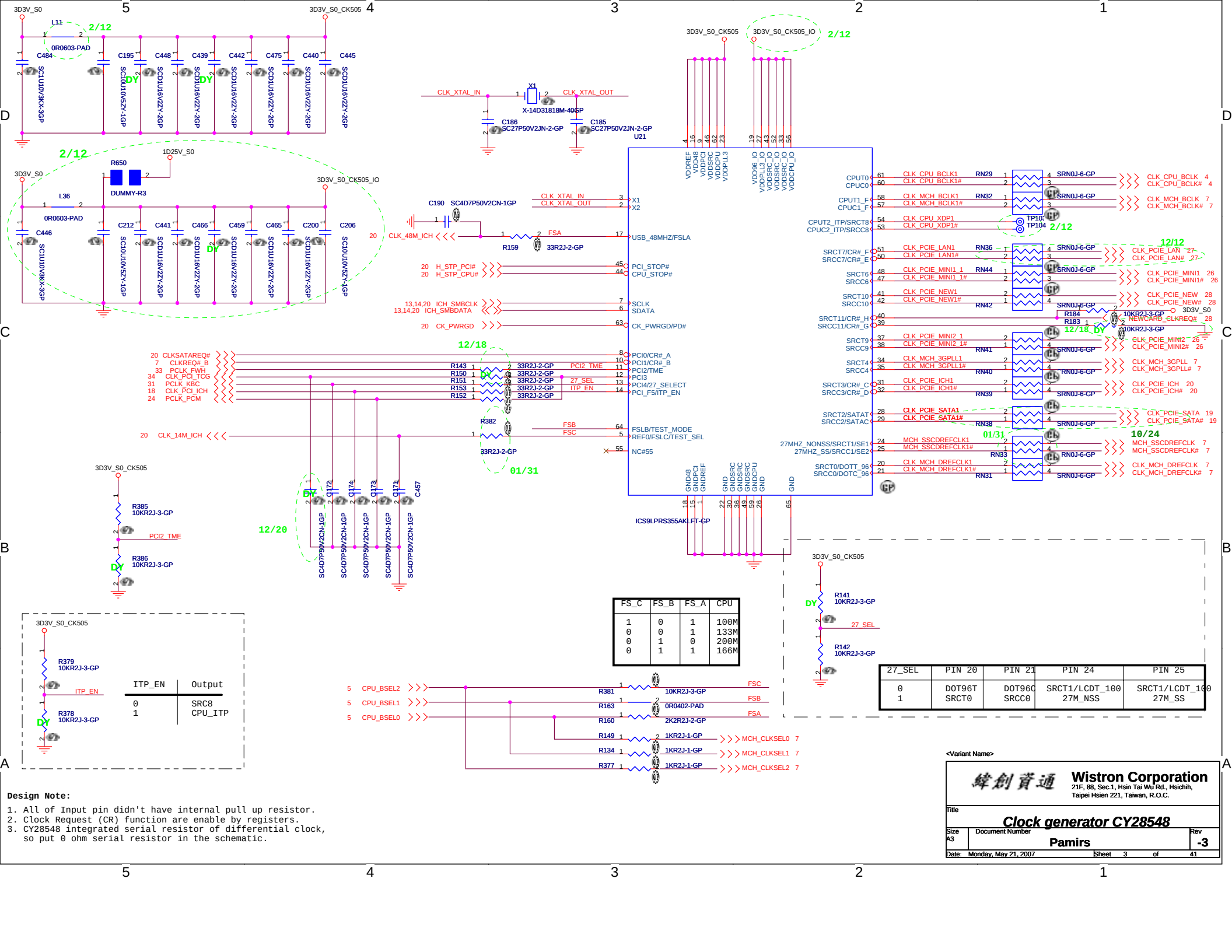

Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

<Variant Name>

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Title: Clock generator CY28548

Size: A3 | Document Number: Pamirs | Rev: -3

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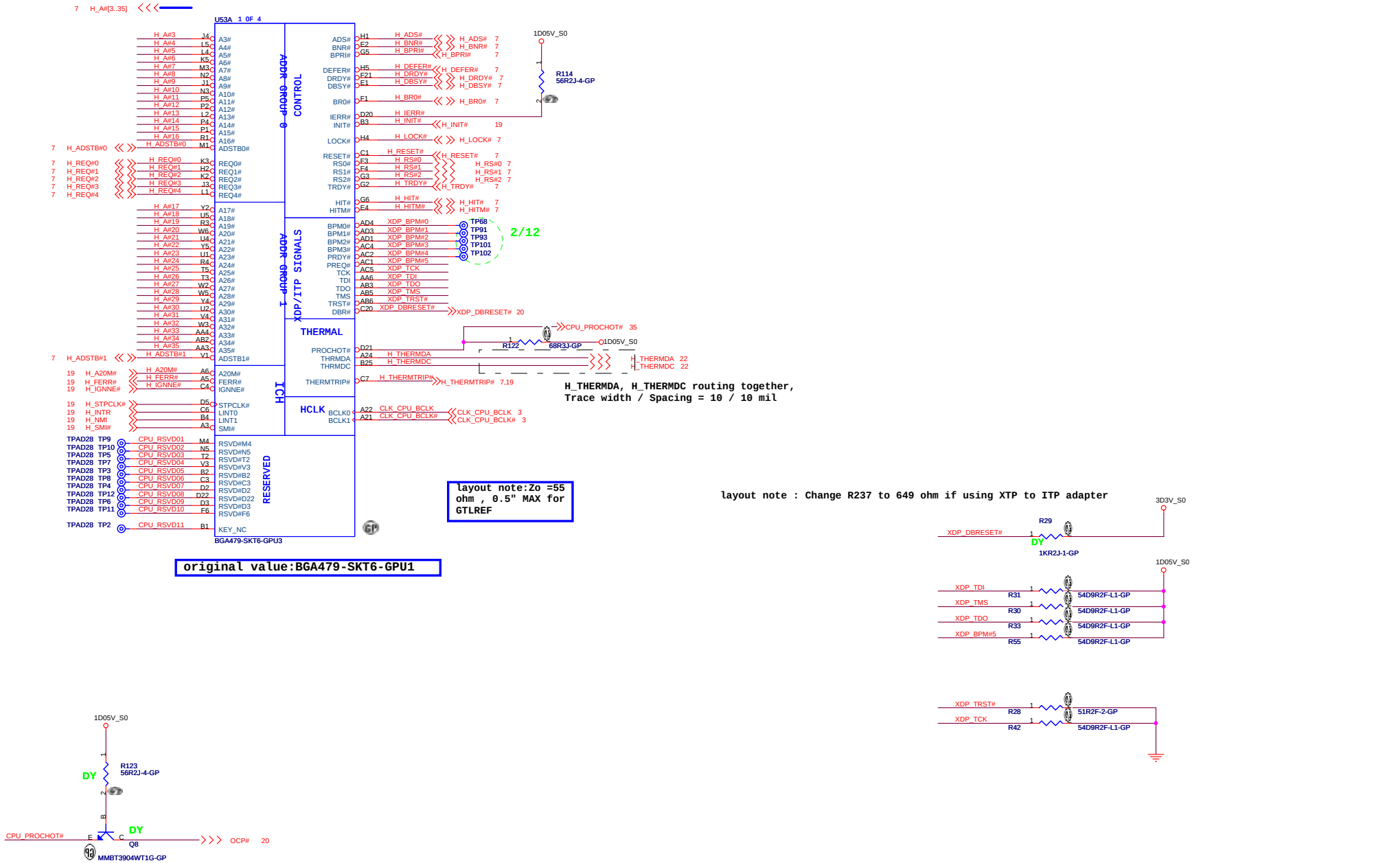

<Core Design>

蜂創資通 Wistron Corporation
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Title: *Meron(1/3)-AGTL+/XDP*

Size	Document Number	Rev
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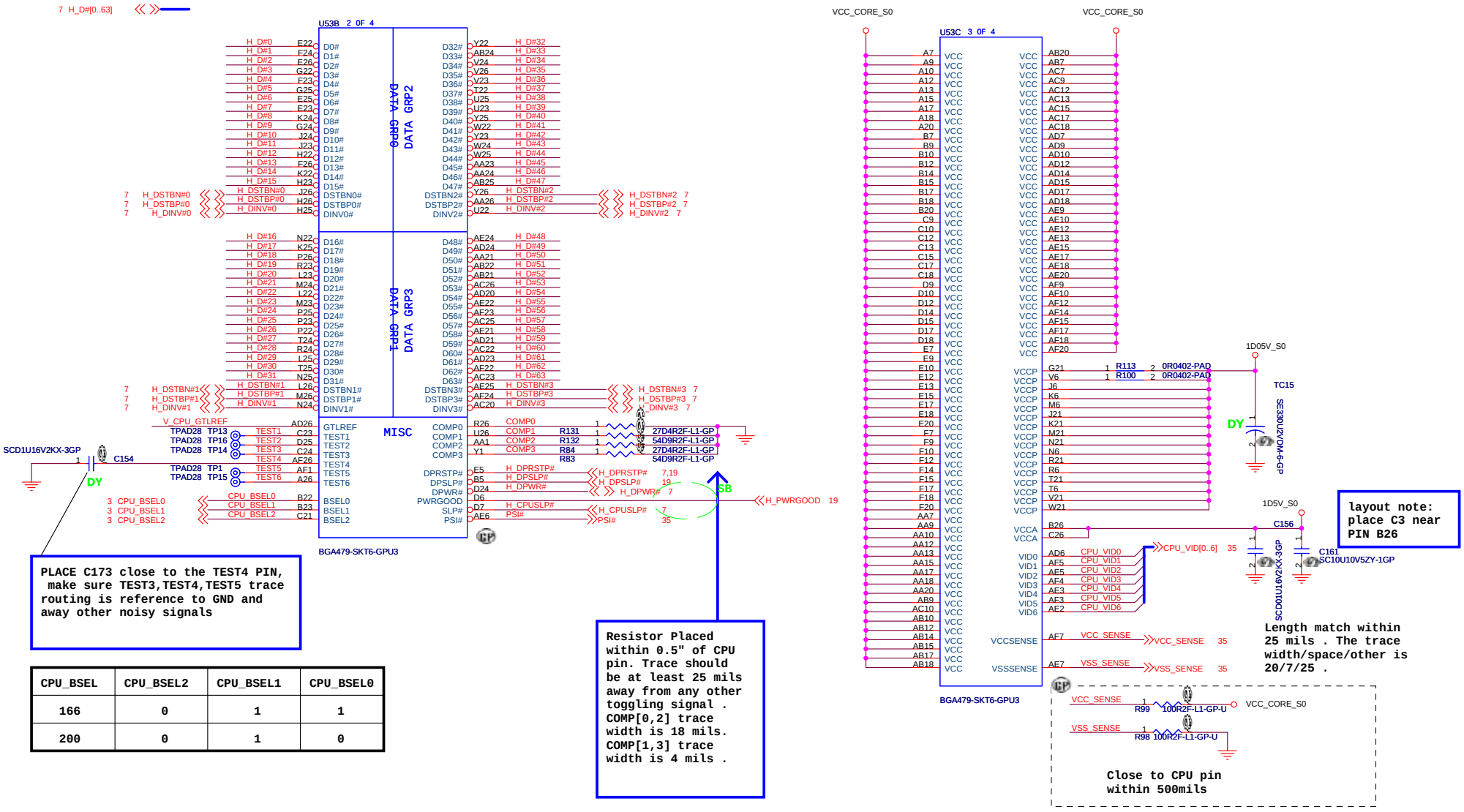
Date: Wednesday, May 23, 2007 Sheet 4 of 41



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

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Title: Meron(2/3)-AGTL+/PWR

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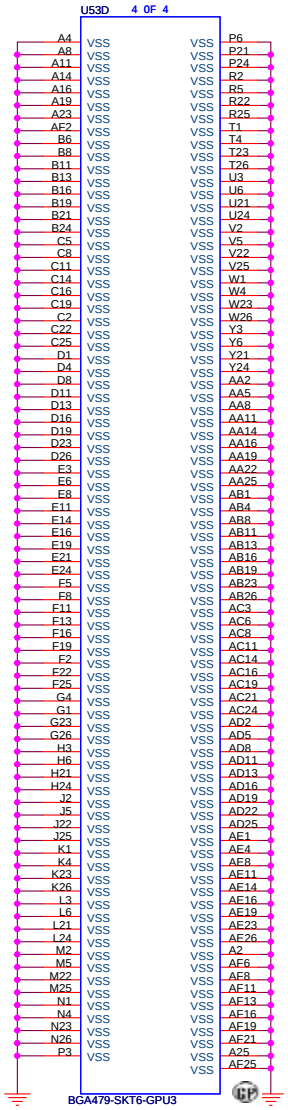

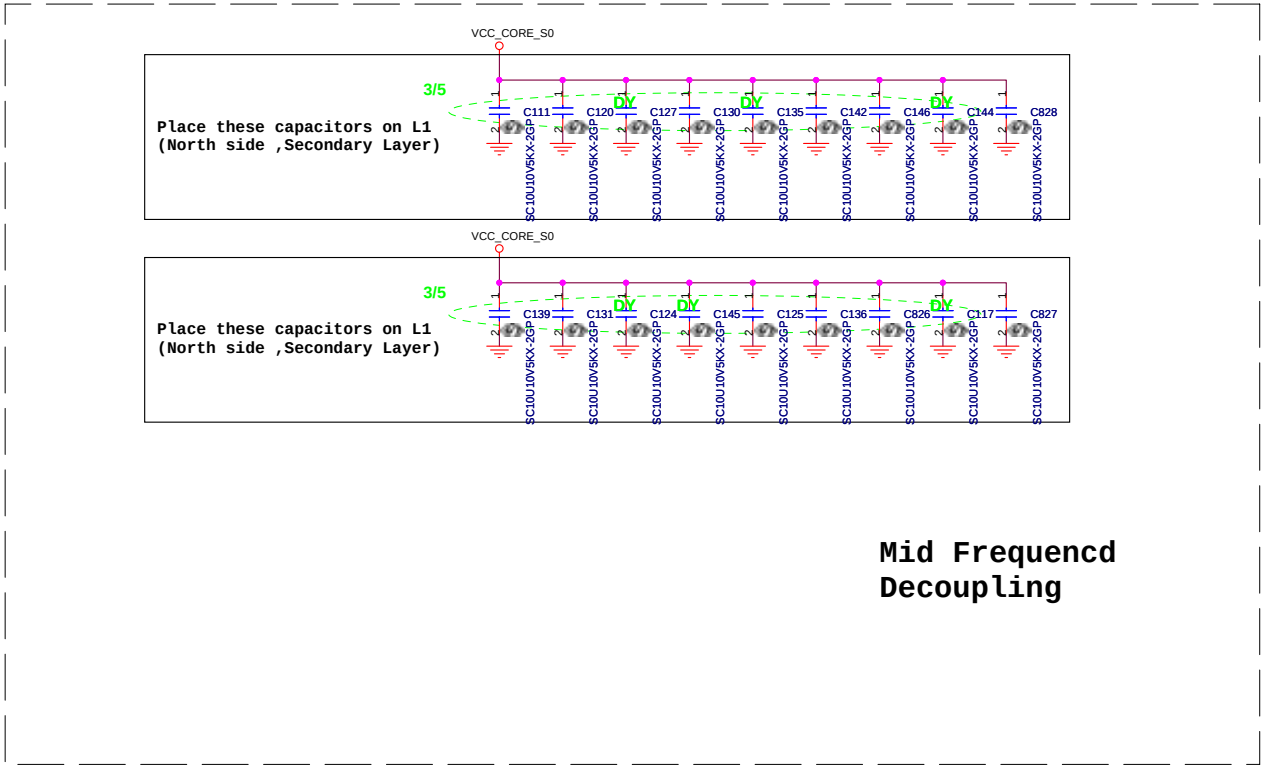

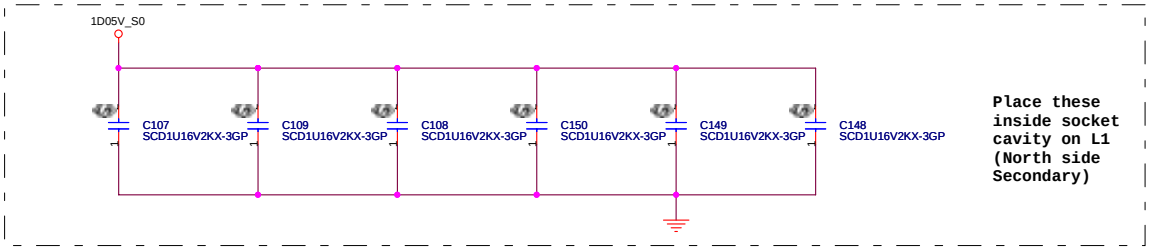

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Title: Meron(3/3)-GND&Bypass

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FOR Calero: 80.6 ohm
Crestline: 20 ohm

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

From Astro demo schematic

layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

Layout Note :
Place C32 within 100 mils of NB

Layout Note :
Place C33 near
pin B3 of NB

SB 0823

0921 P/N CHANGE TO 71.CREST.M02

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Title: CRESTLINE(1/6)-AGTL+/DMI/DDR2

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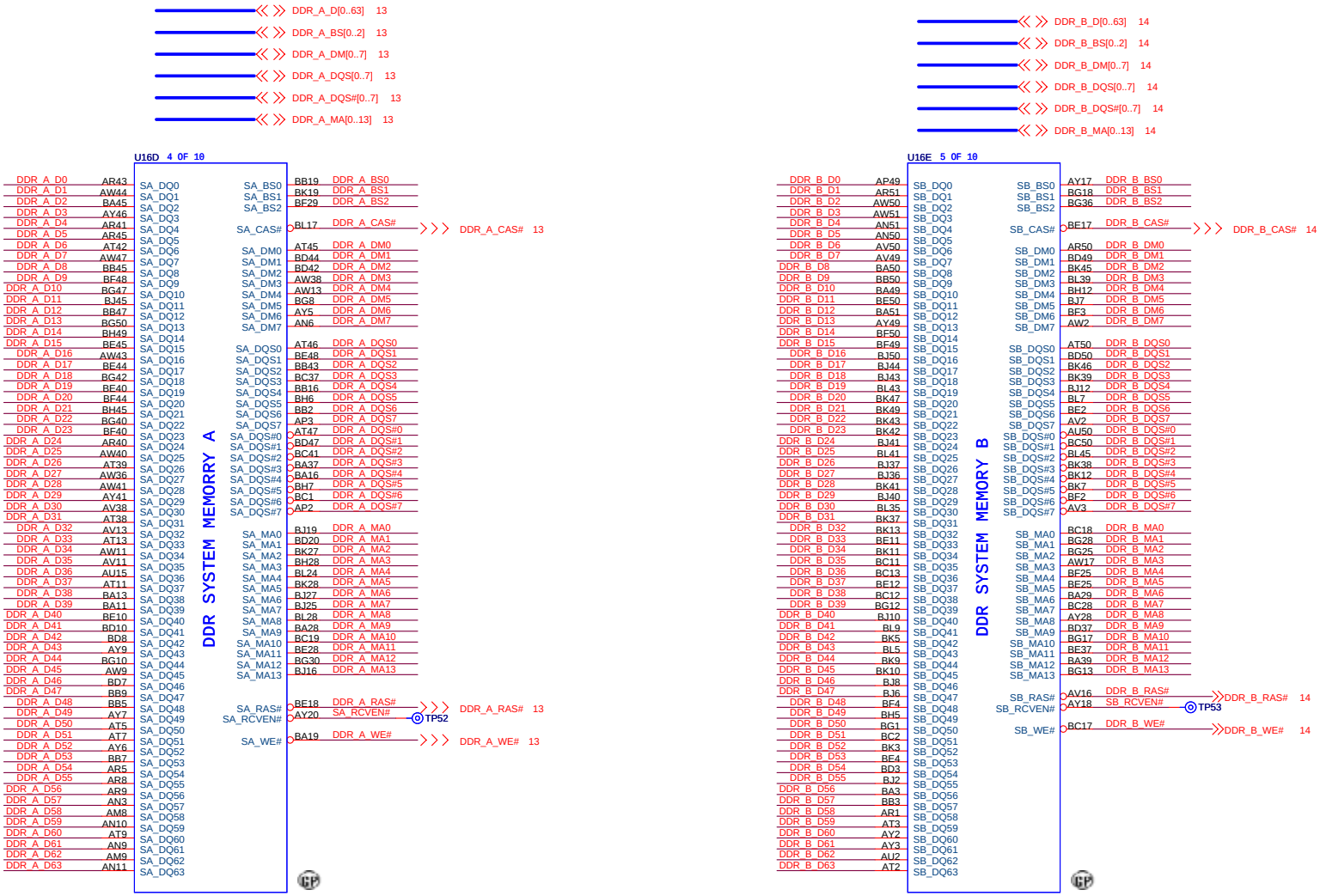

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Title: CRESTLINE(2/6)-DDR2 A/B CH

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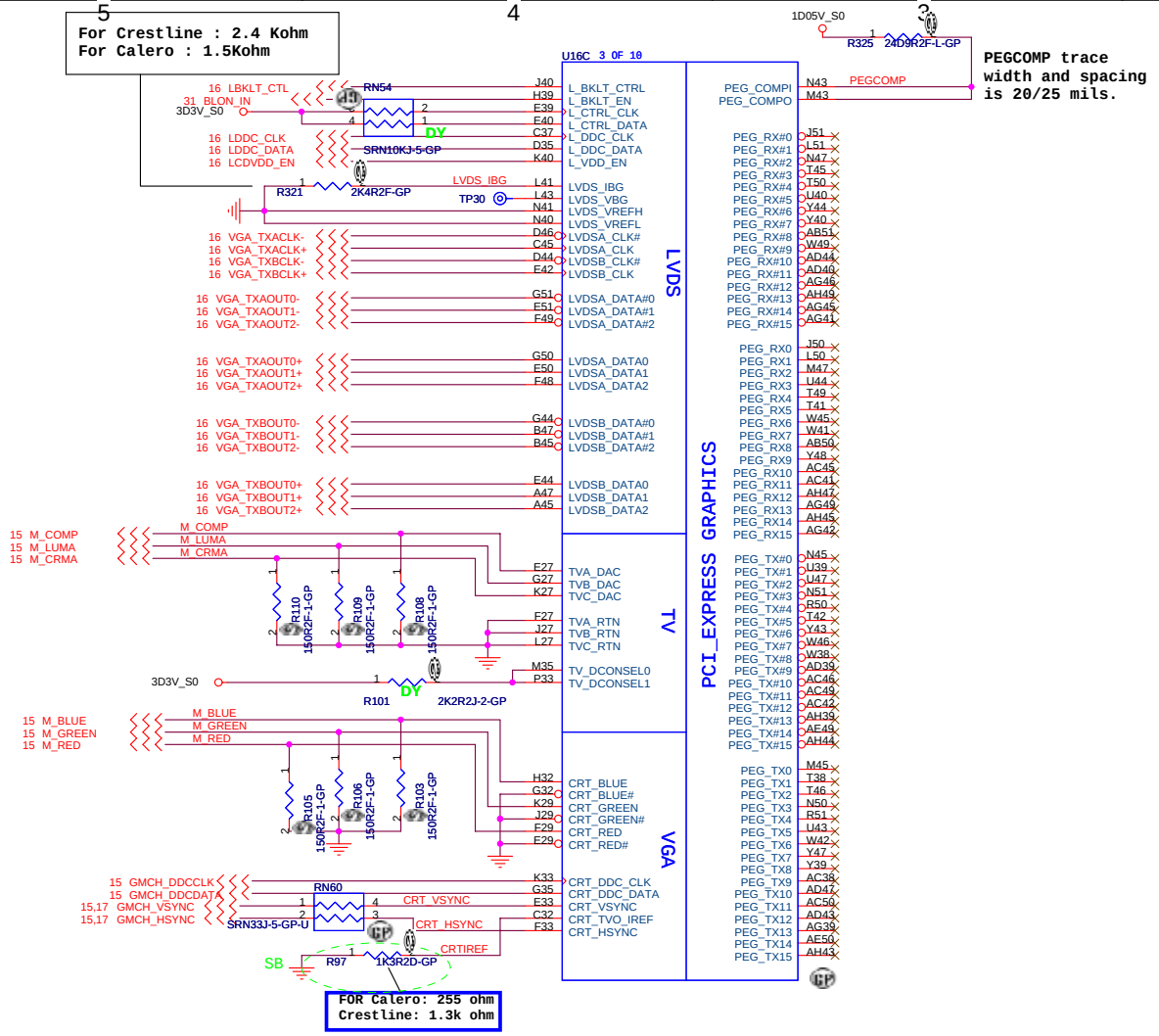

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

<Core Design>

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Title: CRESTLINE(3/6)-VGA/LVDS/TV

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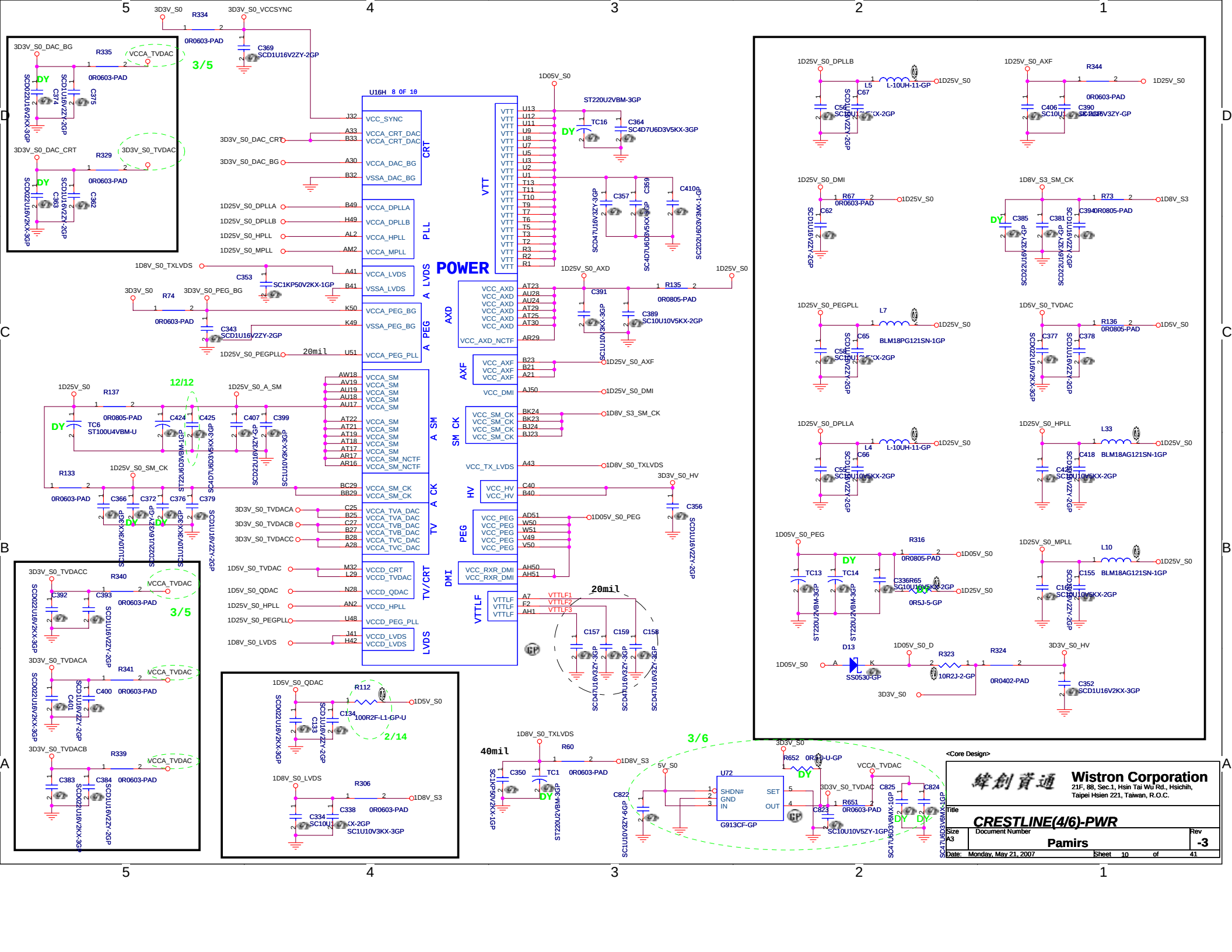
POWER
U16H 8 OF 10
VCC_SYNC
VCCA_CRT_DAC
VCCA_DAC_BG
VSSA_DAC_BG
CRT
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
PLL
VCCA_LVDS
VSSA_LVDS
A LVDS
VCCA_PEG_BG
VSSA_PEG_BG
VCCA_PEG_PLL
A PEG
VCCA_SM
VCCA_SM_NCTF
A SM
VCCA_SM_CK
A CK
VCCA_TVA_DAC
VCCA_TVB_DAC
VCCA_TVC_DAC
TV
VCCD_CRT
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
TV/CRT
VCCD_LVDS
LVDS
VTT
AXD
AXF
SM CK
HV
PEG
DMI
VTTLF
3/5
12/12
3/5
2/14
3/6
20mil
40mil
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Title
CRESTLINE(4/6)-PWR
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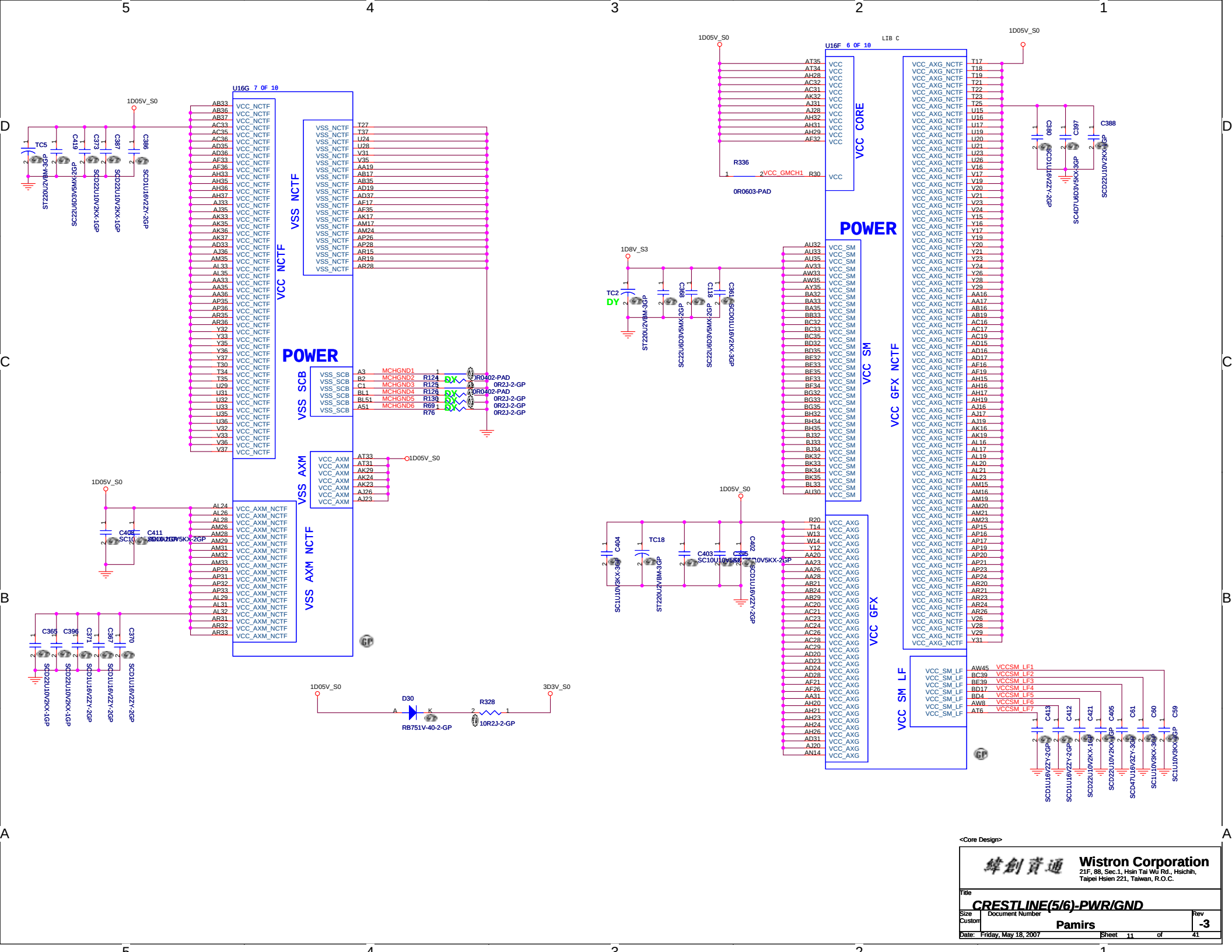

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Title: CRESTLINE(5/6)-PWR/GND

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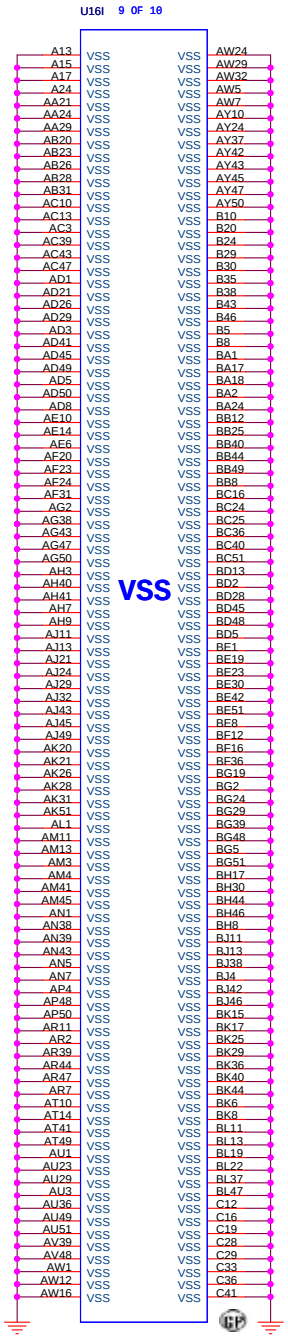

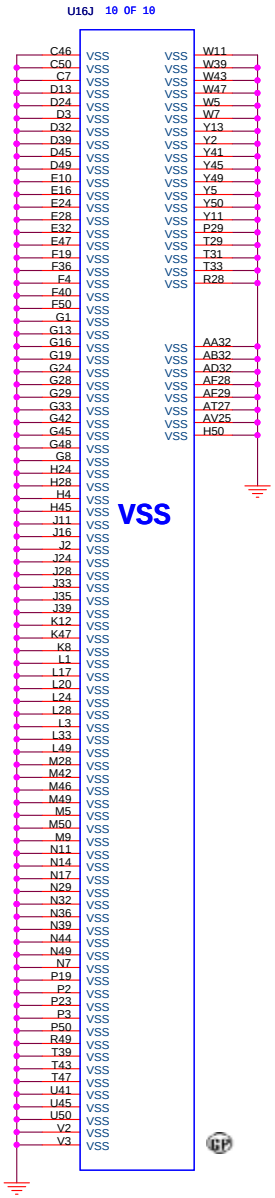

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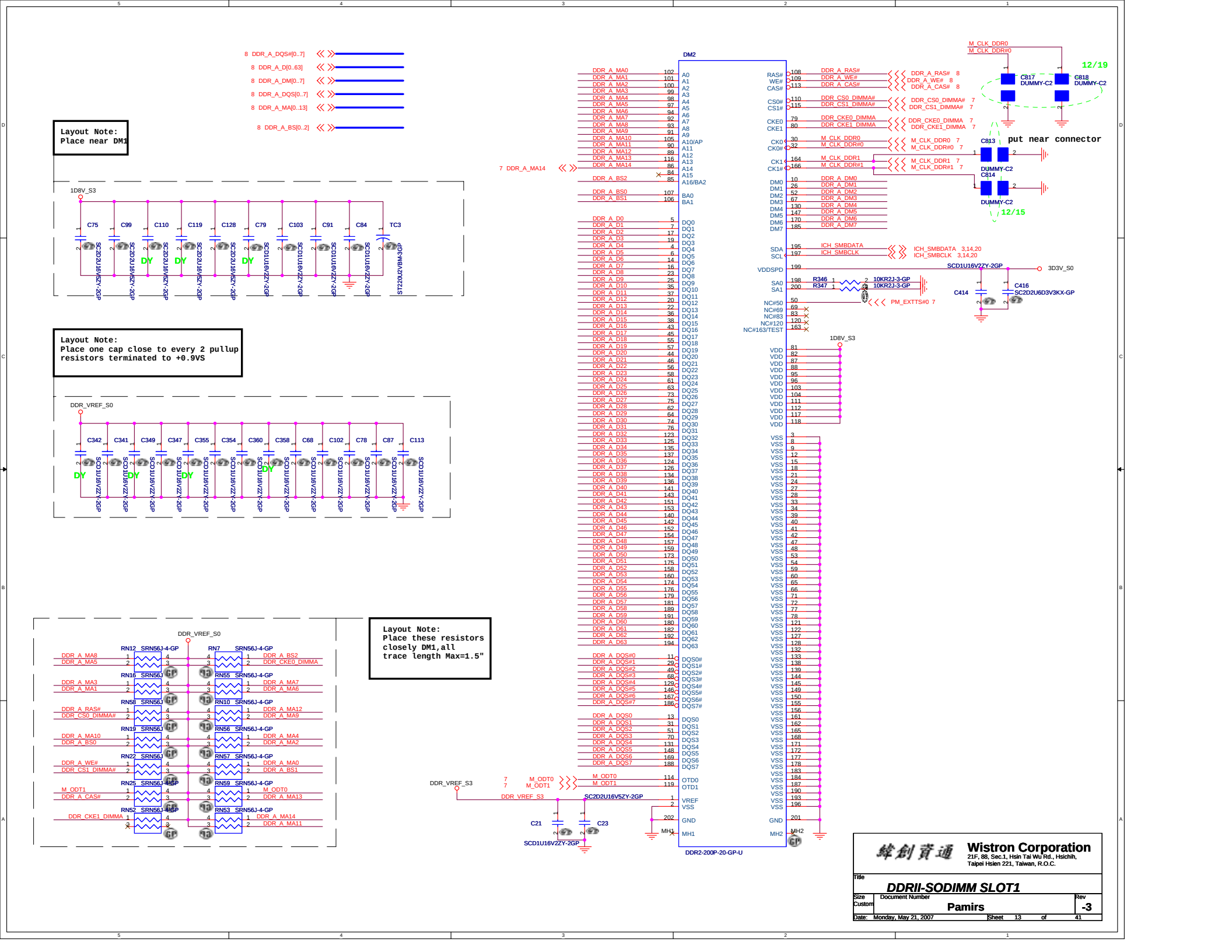
8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..13]
8 DDR_A_BS[0..2]
Layout Note:
Place near DM1
1D8V_S3
C75 C99 C110 C119 C128 C79 C103 C91 C84 TC3
DY
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C342 C341 C349 C347 C355 C354 C360 C358 C68 C102 C78 C87 C113
DY
DDR_VREF_S0
RN12 SRN56J-4-GP
RN7 SRN56J-4-GP
RN16 SRN56J-4-GP
RN55 SRN56J-4-GP
RN58 SRN56J-4-GP
RN10 SRN56J-4-GP
RN19 SRN56J-4-GP
RN56 SRN56J-4-GP
RN22 SRN56J-4-GP
RN57 SRN56J-4-GP
RN25 SRN56J-4-GP
RN59 SRN56J-4-GP
RN52 SRN56J-4-GP
RN53 SRN56J-4-GP
DDR_A_MA8 DDR_A_MA5 DDR_A_BS2 DDR_CKE0_DIMMA
DDR_A_MA3 DDR_A_MA1 DDR_A_MA7 DDR_A_MA6
DDR_A_RAS# DDR_CS0_DIMMA# DDR_A_MA12 DDR_A_MA9
DDR_A_MA10 DDR_A_BS0 DDR_A_MA4 DDR_A_MA2
DDR_A_WE# DDR_CS1_DIMMA# DDR_A_MA0 DDR_A_BS1
M_ODT1 DDR_A_CAS# M_ODT0 DDR_A_MA13
DDR_CKE1_DIMMA DDR_A_MA14 DDR_A_MA11
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
DDR_VREF_S3
SC2D2U16V5ZY-2GP
C21 C23
SCD1U16V2ZY-2GP
DM2
DDR_A_MA0 DDR_A_MA1 DDR_A_MA2 DDR_A_MA3 DDR_A_MA4 DDR_A_MA5 DDR_A_MA6 DDR_A_MA7 DDR_A_MA8 DDR_A_MA9 DDR_A_MA10 DDR_A_MA11 DDR_A_MA12 DDR_A_MA13 DDR_A_MA14
DDR_A_BS2 DDR_A_BS0 DDR_A_BS1
DDR_A_D0 DDR_A_D1 DDR_A_D2 DDR_A_D3 DDR_A_D4 DDR_A_D5 DDR_A_D6 DDR_A_D7 DDR_A_D8 DDR_A_D9 DDR_A_D10 DDR_A_D11 DDR_A_D12 DDR_A_D13 DDR_A_D14 DDR_A_D15 DDR_A_D16 DDR_A_D17 DDR_A_D18 DDR_A_D19 DDR_A_D20 DDR_A_D21 DDR_A_D22 DDR_A_D23 DDR_A_D24 DDR_A_D25 DDR_A_D26 DDR_A_D27 DDR_A_D28 DDR_A_D29 DDR_A_D30 DDR_A_D31 DDR_A_D32 DDR_A_D33 DDR_A_D34 DDR_A_D35 DDR_A_D36 DDR_A_D37 DDR_A_D38 DDR_A_D39 DDR_A_D40 DDR_A_D41 DDR_A_D42 DDR_A_D43 DDR_A_D44 DDR_A_D45 DDR_A_D46 DDR_A_D47 DDR_A_D48 DDR_A_D49 DDR_A_D50 DDR_A_D51 DDR_A_D52 DDR_A_D53 DDR_A_D54 DDR_A_D55 DDR_A_D56 DDR_A_D57 DDR_A_D58 DDR_A_D59 DDR_A_D60 DDR_A_D61 DDR_A_D62 DDR_A_D63
DDR_A_DQS#0 DDR_A_DQS#1 DDR_A_DQS#2 DDR_A_DQS#3 DDR_A_DQS#4 DDR_A_DQS#5 DDR_A_DQS#6 DDR_A_DQS#7
DDR_A_DQS0 DDR_A_DQS1 DDR_A_DQS2 DDR_A_DQS3 DDR_A_DQS4 DDR_A_DQS5 DDR_A_DQS6 DDR_A_DQS7
M_ODT0 M_ODT1
DDR_A_RAS# DDR_A_WE# DDR_A_CAS#
DDR_CS0_DIMMA# DDR_CS1_DIMMA#
DDR_CKE0_DIMMA DDR_CKE1_DIMMA
M_CLK_DDR0 M_CLK_DDR#0 M_CLK_DDR1 M_CLK_DDR#1
DDR_A_DM0 DDR_A_DM1 DDR_A_DM2 DDR_A_DM3 DDR_A_DM4 DDR_A_DM5 DDR_A_DM6 DDR_A_DM7
ICH_SMBDATA ICH_SMBCLK
SCD1U16V2ZY-2GP
3D3V_S0
R346 R347 10KR2J-3-GP
PM_EXTTS#0
C414 C416 SC2D2U6D3V3KX-GP
1D8V_S3
DDR2-200P-20-GP-U
M_CLK_DDR0
M_CLK_DDR#0
12/19
C817 C818 DUMMY-C2
C813 C814 DUMMY-C2
put near connector
12/15
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Title
DDRII-SODIMM SLOT1
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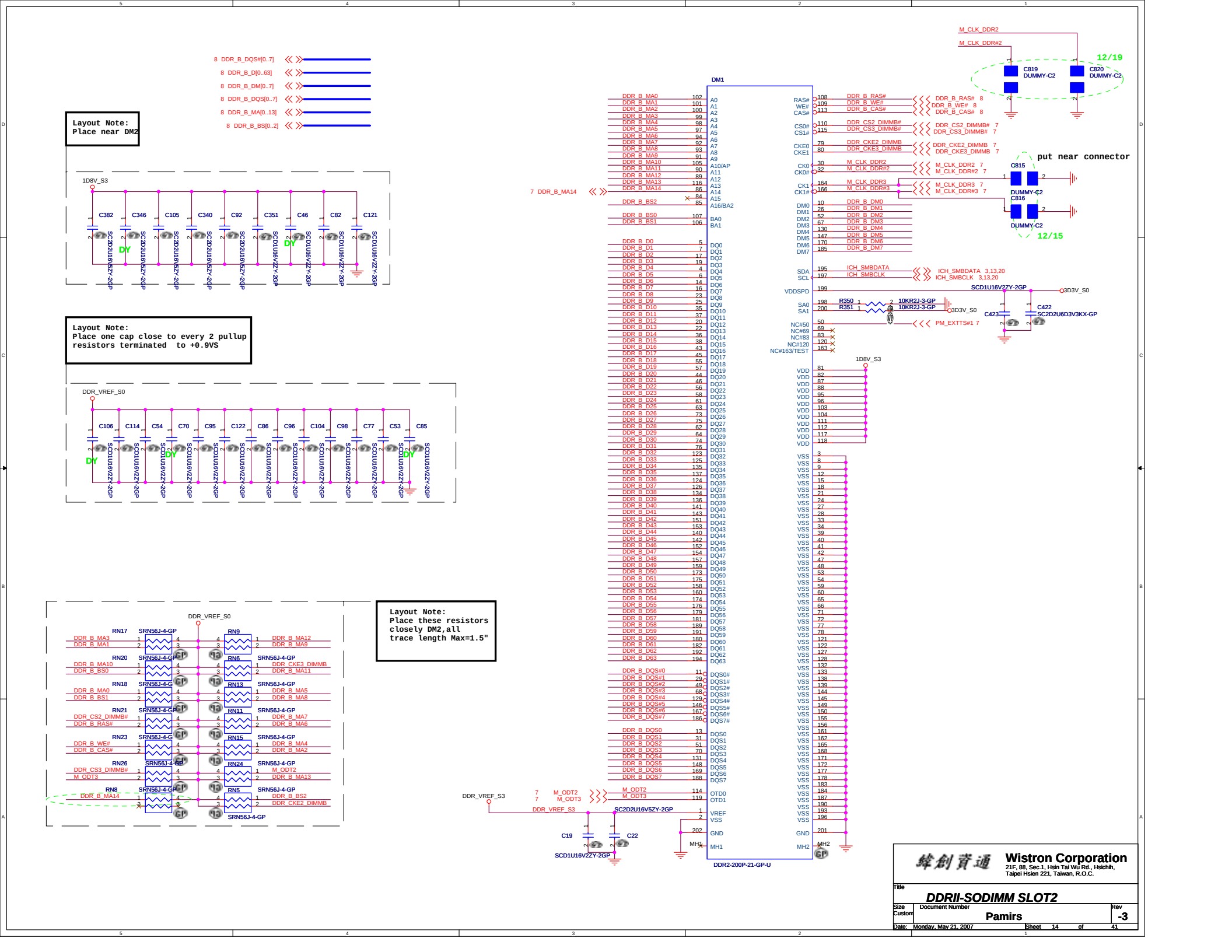
Layout Note:
Place near DM2
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
DM1
DDR2-200P-21-GP-U
put near connector
12/19
12/15
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDRII-SODIMM SLOT2
Pamirs
-3
Monday, May 21, 2007
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CRT I/F & CONNECTOR

0721

Layout Note:
Place these resistors close to the CRT-out connector

9 M_RED
9 M_GREEN
9 M_BLUE

L3 BLM18BB470SN1-GP
L2 BLM18BB470SN1-GP
L1 BLM18BB470SN1-GP

R7 150R2F-1-GP
R6 150R2F-1-GP
R5 150R2F-1-GP

C16 C13 C11 C14 C12 C10 SC10P50V2JN-4GP

CRT_R CRT_G CRT_B

CRT_R 17
CRT_G 17
CRT_B 17

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

5V_CRT_S0
C7 SCD01U16V2KX-3GP
F1 FUSE-1D1A6V-8GP
5V_S0
D4 RB751V-40-2-GP
5V_CRT1_S0
RN1 SRN2K2J-1-GP

CRT1 VIDEO-15-57-GP-U1 20.20424.015
CRT_R CRT_G CRT_B
DDC_DATA_CON
JVGA_HS
JVGA_VS
DDC_CLK_CON

C8 SC33P50V2JN-3GP DY
C9 SC33P50V2JN-3GP DY
C6 SC22P50V2JN-4GP
C5 SC22P50V2JN-4GP

D10 BAV99-7-F-GP
D12 BAV99-7-F-GP
DDC_DATA_CON
DDC_CLK_CON
5V_CRT1_S0

U2 PACDN009MR-GP-U
GMCH_HSYNC
GMCH_VSYNC
CRT_R
CRT_G
CRT_B

5V_S0
C320 SCD1U16V2ZY-2GP
PR_INSERT 17

9,17 GMCH_HSYNC
9,17 GMCH_VSYNC
U5A TSAHCT125PW-GP
U5B TSAHCT125PW-GP
HSYNC_5
VSYNC_5
RN4 SRN33J-5-GP-U
JVGA_HS
JVGA_VS

3D3V_S0
RN2 SRN2K2J-1-GP
U1 2N7002DW-1-GP
9 GMCH_DDCDATA
17 DDC_CLK_CON
DDC_DATA_CON
DDC_CLK_CON
DDC_DATA_CON 17
GMCH_DDCCLK 9

5V @ ext. CRT side

TV OUT CONN

connector

9 M_CRMA
9 M_COMP
9 M_LUMA

L23 L24 L25 BLM18BB470SN1-GP
C293 C292 C295 C294 C297 C296 SC10P50V2JN-4GP
R271 R1 R2 150R2F-1-GP

0721

TV_CRMA 17
TV_COMP 17
TV_LUMA 17

Place this 2 resistors close to the TV-out connector

TV1 MINDIN7-18-GP 22.10021.H31
TV_LUMA
TV_CRMA
TV_COMP
LUMA
CRMA
COMP
NC#2
NC#5
GND

D1 BAV99-7-F-GP
D3 BAV99-7-F-GP
D2 BAV99-7-F-GP
3D3V_S0
C1 SCD1U16V2ZY-2GP DY
C3 SCD1U16V2ZY-2GP DY
C2 SCD1U16V2ZY-2GP DY

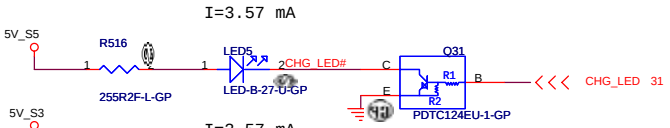
<Core Design>

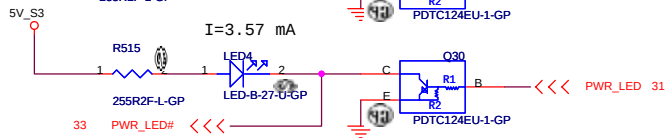
蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

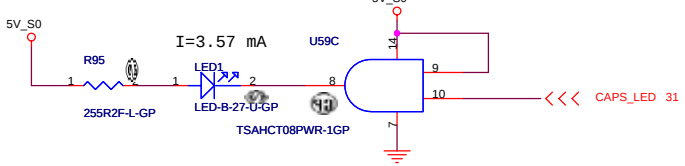
Title: **CRT/TV Connector**
Size: A3 | Document Number: **Pamirs** | Rev: **-3**
Date: Monday, May 21, 2007 | Sheet 15 of 41

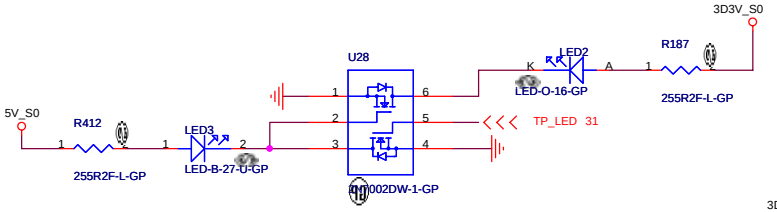
LED / INVERTER INTERFACE

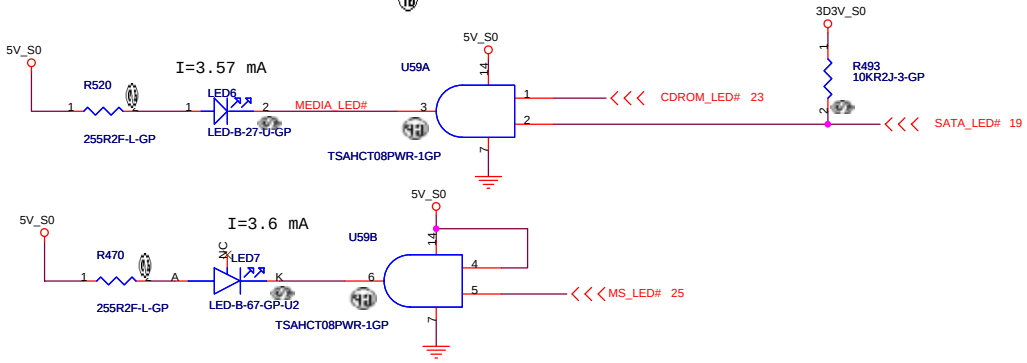
LCD/INV CONN

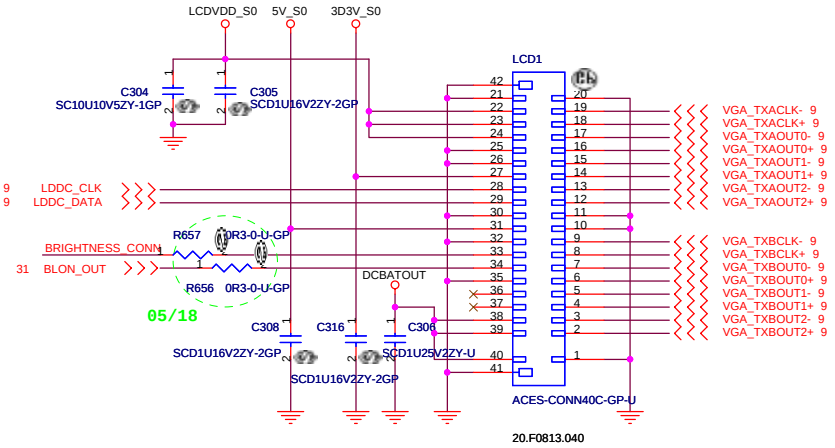


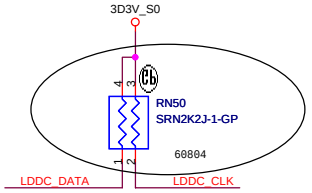


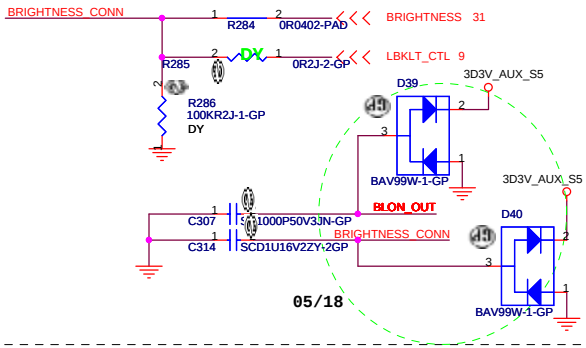


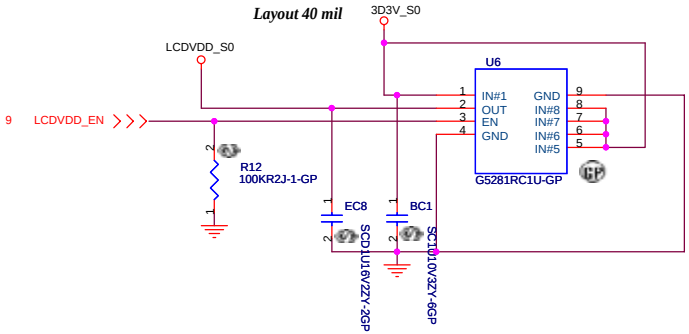


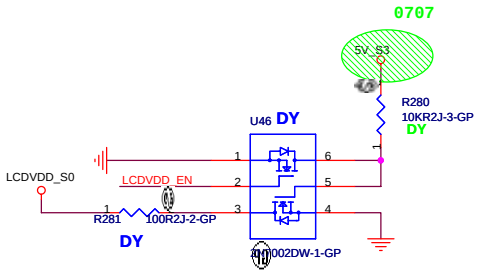










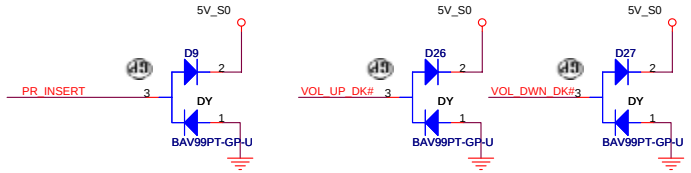


<Core Design>

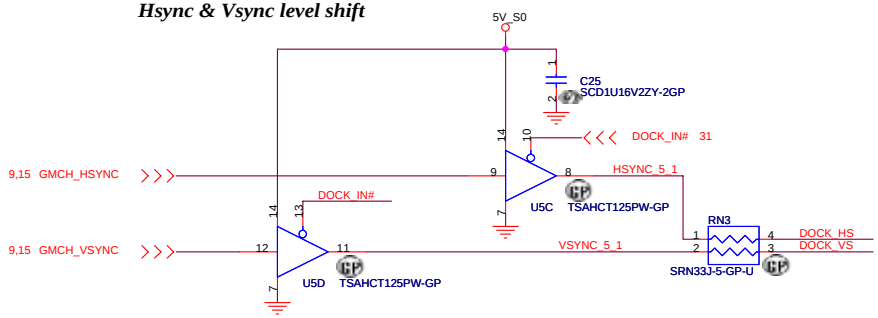
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

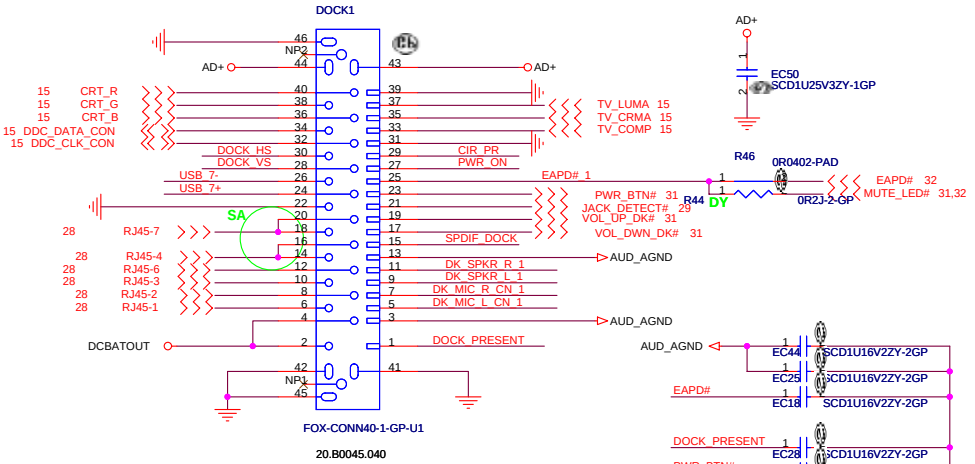
Title: **LCD/Inverter Connector**		
Size: Custom	Document Number: **Pamirs**	Rev: **-3**
Date: Monday, May 21, 2007	Sheet 16 of 41	

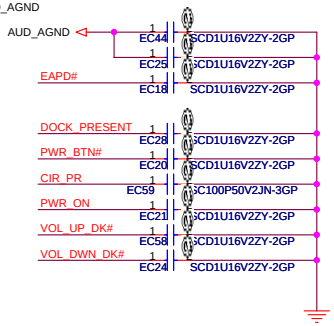
Docking Connector

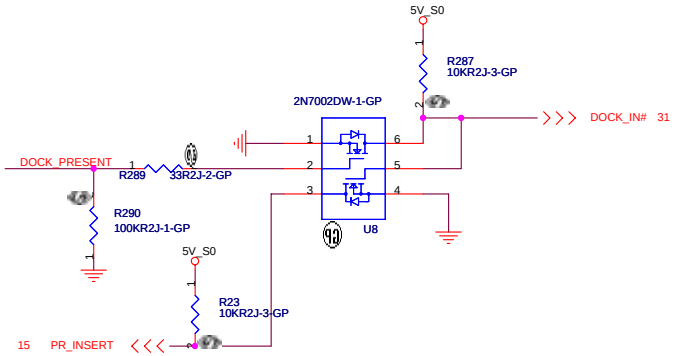


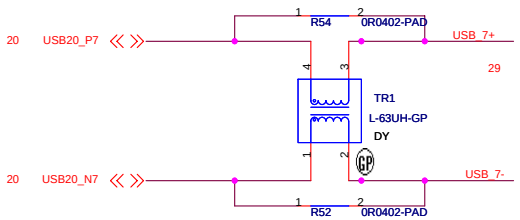
Hsync & Vsync level shift

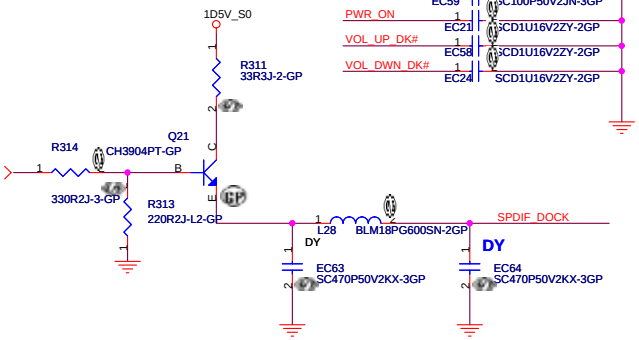


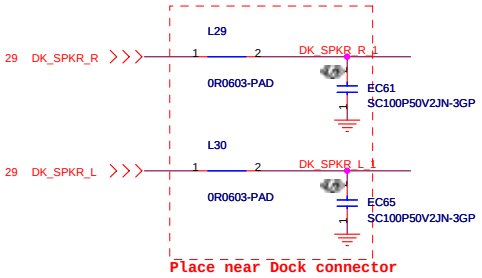


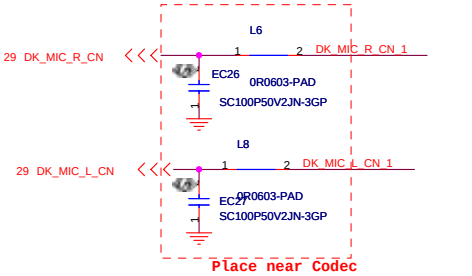


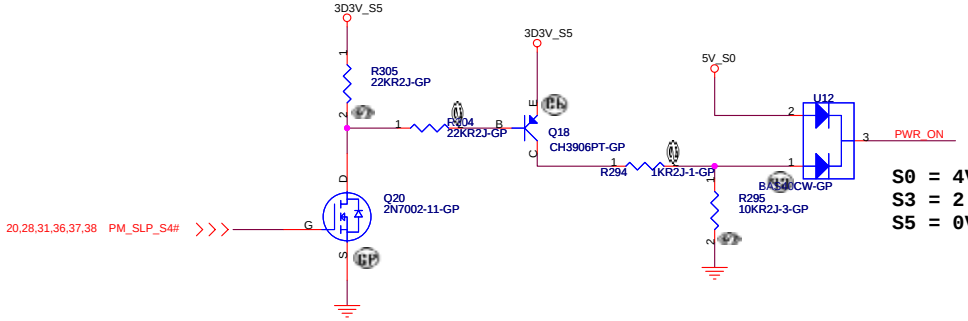












S0 = 4V
S3 = 2.5V
S5 = 0V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Board to board conn/ Docking**

Size	Document Number	Rev
A3	Pamirs	-3

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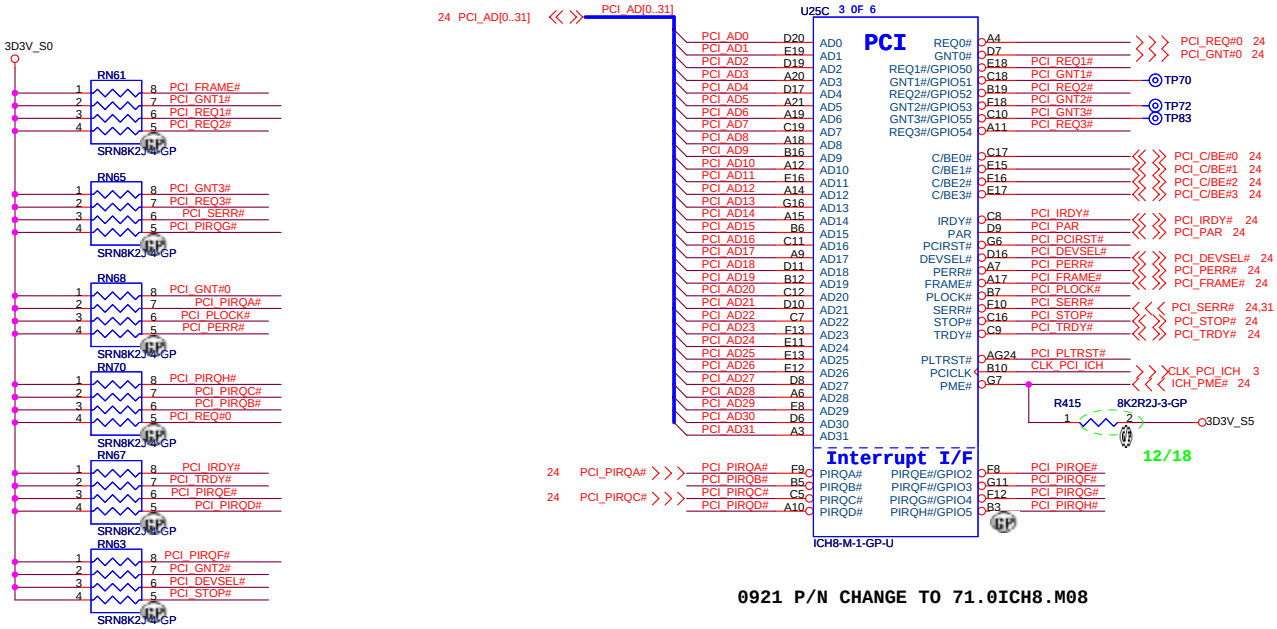
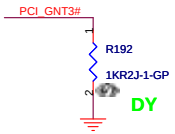
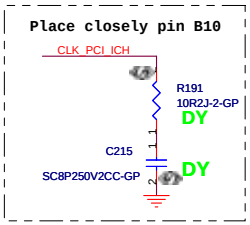


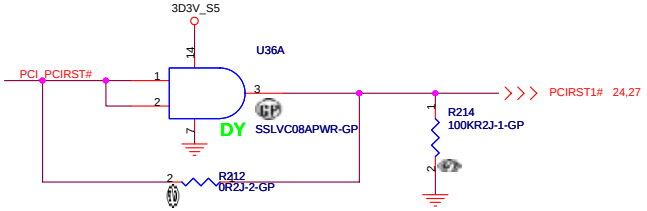
0921 P/N CHANGE TO 71.0ICH8.M08

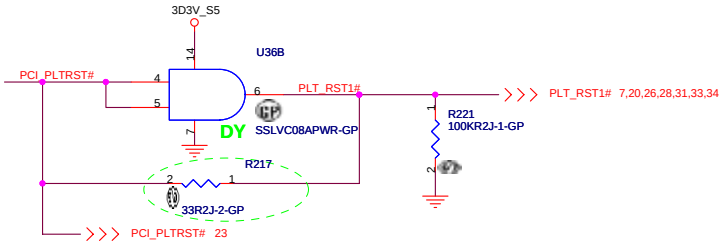


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(1/4)-PCI/INT

Size	Document Number	Rev
A3	Pamirs	-3

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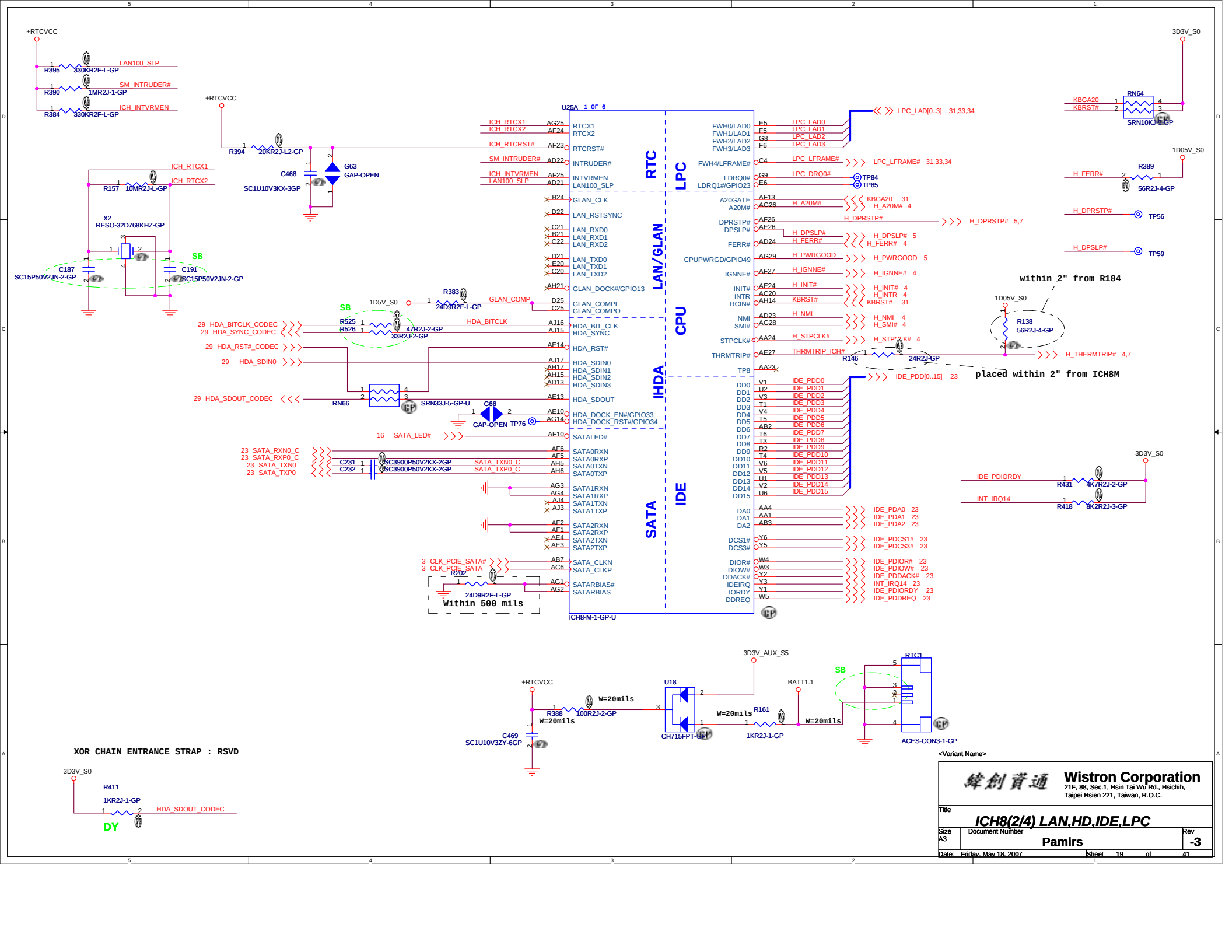
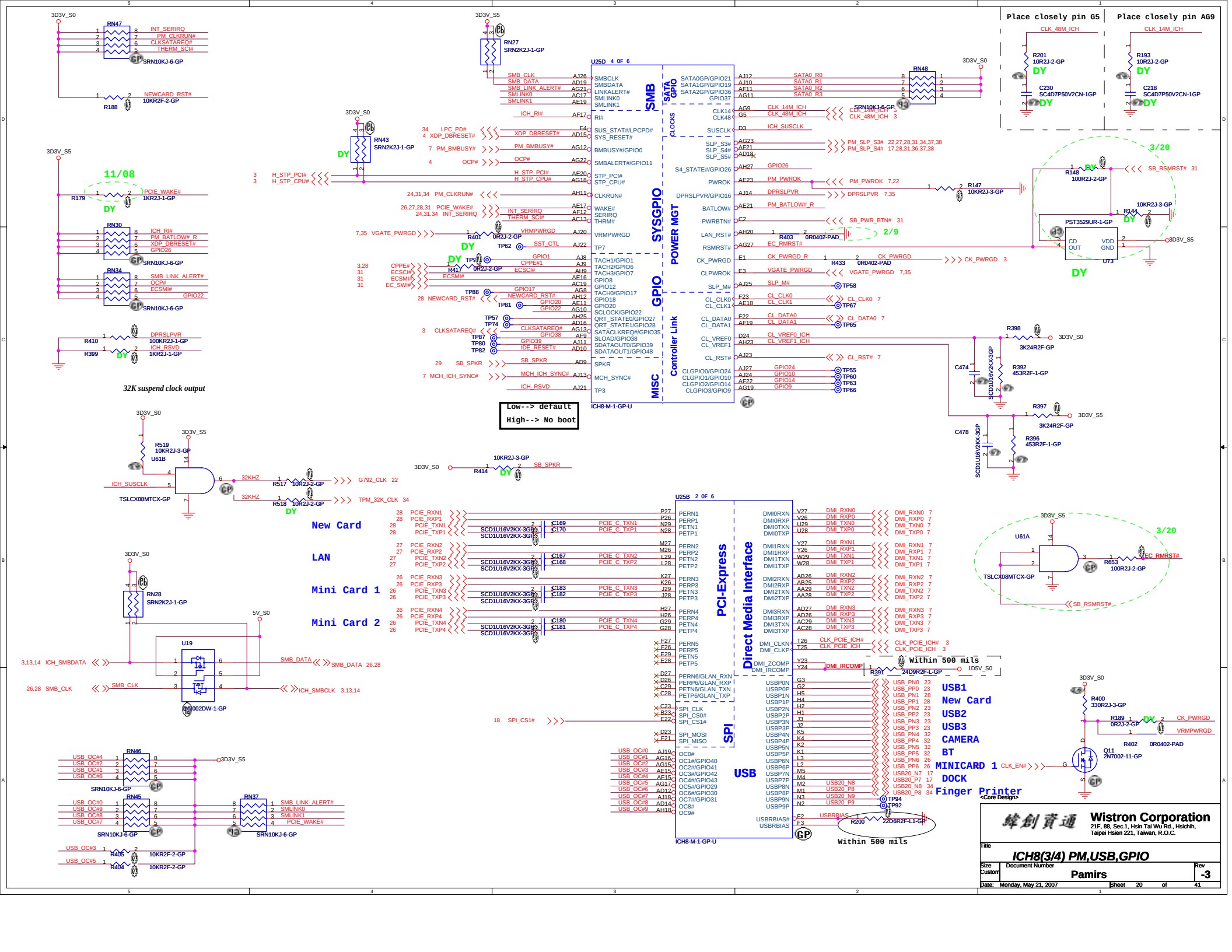
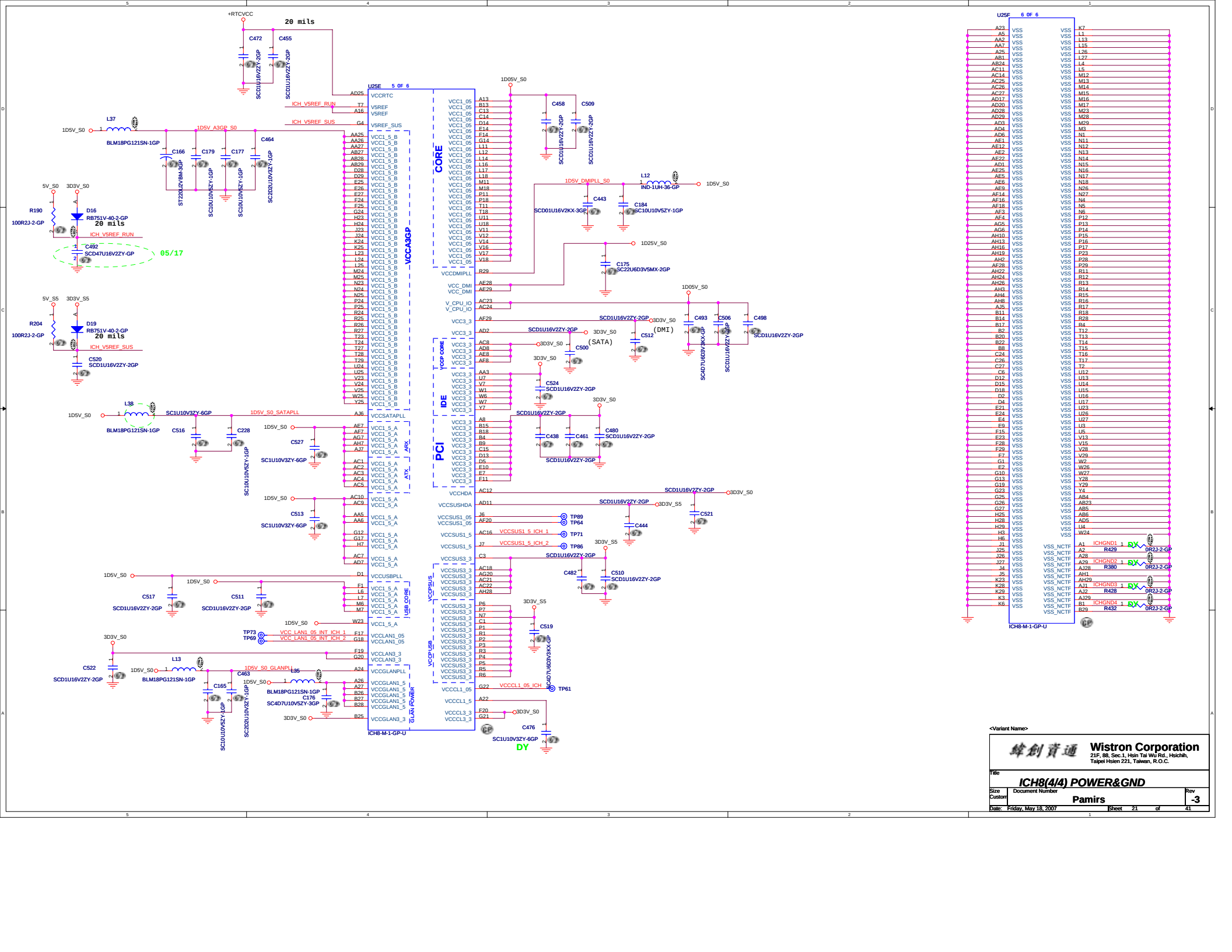
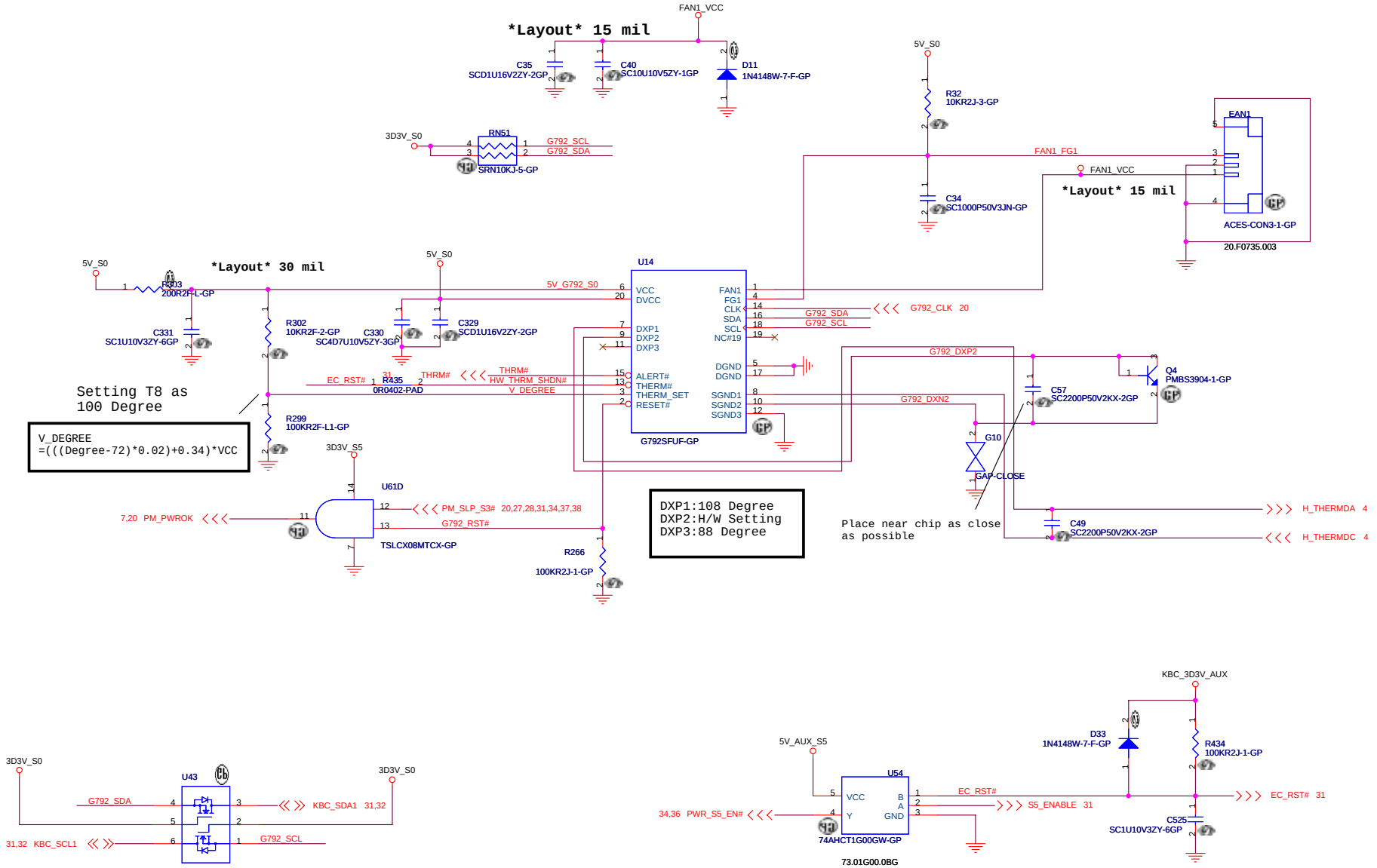

+RTCVCC
R395 330KR2F-L-GP
LAN100_SLP
R390 1MR2J-1-GP
SM_INTRUDER#
R384 330KR2F-L-GP
ICH_INTVRMEN
R394 20KR2J-L2-GP
G63 GAP-OPEN
C468 SC1U10V3KX-3GP
ICH_RTCX1
ICH_RTCX2
R157 10MR2J-L-GP
X2 RESO-32D768KHZ-GP
SB
C187 SC15P50V2JN-2-GP
C191 SC15P50V2JN-2-GP
U25A 1 0F 6
RTC
LPC
LAN/GLAN
CPU
IHDA
IDE
SATA
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH8-M-1-GP-U
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LPC_LAD[0..3] 31,33,34
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LPC_LFRAME# 31,33,34
LPC_DRQ0#
TP84
TP85
KBGA20 31
H_A20M# 4
H_DPRSTP# 5,7
H_DPSLP# 5
H_FERR# 4
H_PWRGOOD 5
H_IGNNE# 4
H_INIT# 4
H_INTR 4
KBRST# 31
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THERMTRIP# 4,7
IDE_PDD[0..15] 23
IDE_PDA0 23
IDE_PDA1 23
IDE_PDA2 23
IDE_PDCS1# 23
IDE_PDCS3# 23
IDE_PDIOR# 23
IDE_PDIOW# 23
IDE_PDDACK# 23
INT_IRQ14 23
IDE_PDIORDY 23
IDE_PDDREQ 23
3D3V_S0
RN64 SRN10KJ-GP
KBGA20
KBRST#
1D05V_S0
R389 56R2J-4-GP
H_FERR#
H_DPRSTP#
TP56
H_DPSLP#
TP59
within 2" from R184
R138 56R2J-4-GP
R146 24R2J-GP
placed within 2" from ICH8M
R383 24D9R2F-L-GP
GLAN_COMP
HDA_BITCLK
R525 47R2J-2-GP
R526 33R2J-2-GP
29 HDA_BITCLK_CODEC
29 HDA_SYNC_CODEC
29 HDA_RST#_CODEC
29 HDA_SDIN0
29 HDA_SDOUT_CODEC
RN66 SRN33J-5-GP-U
G66 GAP-OPEN
TP76
16 SATA_LED#
23 SATA_RXN0_C
23 SATA_RXP0_C
23 SATA_TXN0
23 SATA_TXP0
C231 SC3900P50V2KX-2GP
C232 SC3900P50V2KX-2GP
SATA_TXN0_C
SATA_TXP0_C
3 CLK_PCIE_SATA#
3 CLK_PCIE_SATA
R202 24D9R2F-L-GP
Within 500 mils
IDE_PDIORDY
INT_IRQ14
R431 4K7R2J-2-GP
R418 8K2R2J-3-GP
3D3V_AUX_S5
U18 CH715FPT-GP
BATT1.1
R161 1KR2J-1-GP
W=20mils
R388 100R2J-2-GP
C469 SC1U10V3ZY-6GP
RTC1 ACES-CON3-1-GP
XOR CHAIN ENTRANCE STRAP : RSVD
R411 1KR2J-1-GP
HDA_SDOUT_CODEC
DY
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(2/4) LAN,HD,IDE,LPC
Size A3
Document Number
Pamirs
Rev -3
Date: Friday, May 18, 2007
Sheet 19 of 41



Company	Wistron Corporation
Address	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ICH8(3/4) PM,USB,GPIO
Size	Custom
Document Number	Pamirs
Rev	-3
Date	Monday, May 21, 2007
Sheet	20 of 41


+RTCVCC
20 mils
C472
C455
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
U25E 5 OF 6
ICH_V5REF_RUN
ICH_V5REF_SUS
L37
1D5V_S0
BLM18PG121SN-1GP
1D5V_A3GP_S0
C166
C179
C177
C464
ST220U2V8M-3GP
SC10U10V5ZY-1GP
SC10U10V5ZY-1GP
SC22D2U10V2Z1-1GP
5V_S0
3D3V_S0
R190
100R2J-2-GP
D16
RB751V-40-2-GP
20 mils
ICH_V5REF_RUN
C492
SCD47U16V2ZY-GP
05/17
5V_S5
3D3V_S5
R204
100R2J-2-GP
D19
RB751V-40-2-GP
20 mils
ICH_V5REF_SUS
C520
SCD1U16V2ZY-2GP
L38
1D5V_S0
BLM18PG121SN-1GP
SC1U10V3ZY-6GP
C516
C228
1D5V_S0_SATAPLL
SC10U10V5ZY-1GP
C527
SC1U10V3ZY-6GP
C513
SC1U10V3ZY-6GP
1D5V_S0
D1
C517
C511
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
TP73
TP69
VCC_LAN1_05_INT_ICH_1
VCC_LAN1_05_INT_ICH_2
3D3V_S0
L13
C522
SCD1U16V2ZY-2GP
1D5V_S0
BLM18PG121SN-1GP
1D5V_S0_GLANPLL
L35
C463
C165
C176
BLM18PG121SN-1GP
SC4D7U10V5ZY-3GP
SC10U10V5ZY-1GP
SC22D2U10V2ZY-1GP
3D3V_S0
CORE
VCCA3GP
IDE
PCI
VCCP_CORE
VCCP_USB
VCCP_SUS
USB_CORE
GLAN_POWER
ICH8-M-1-GP-U
1D05V_S0
C458
C509
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
1D5V_DMIPLL_S0
L12
IND-1UH-36-GP
1D5V_S0
C443
C184
SCD01U16V2KX-3GP
SC10U10V5ZY-1GP
1D25V_S0
C175
SC22U6D3V5MX-2GP
1D05V_S0
SCD1U16V2ZY-2GP
3D3V_S0
(SATA)
(DMI)
C493
C506
C498
C512
C500
SC4D7U6D3V2KX-GP
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
3D3V_S0
C524
SCD1U16V2ZY-2GP
3D3V_S0
SCD1U16V2ZY-2GP
C438
C461
C480
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
3D3V_S0
3D3V_S0
C521
C444
TP89
TP64
VCCSUS1_5_ICH_1
TP71
VCCSUS1_5_ICH_2
TP86
3D3V_S5
SCD1U16V2ZY-2GP
C482
C510
SCD1U16V2ZY-2GP
3D3V_S5
C519
C4D7U6D3V3KX-GP
VCCCL1_05_ICH
TP61
3D3V_S0
C476
SC1U10V3ZY-6GP
DY
U25F 6 OF 6
ICH8-M-1-GP-U
ICHGND1
ICHGND2
ICHGND3
ICHGND4
R429
R380
R428
R432
0R2J-2-GP
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(4/4) POWER&GND
Size
Custom
Document Number
Pamirs
Rev
-3
Date: Friday, May 18, 2007
Sheet 21 of 41



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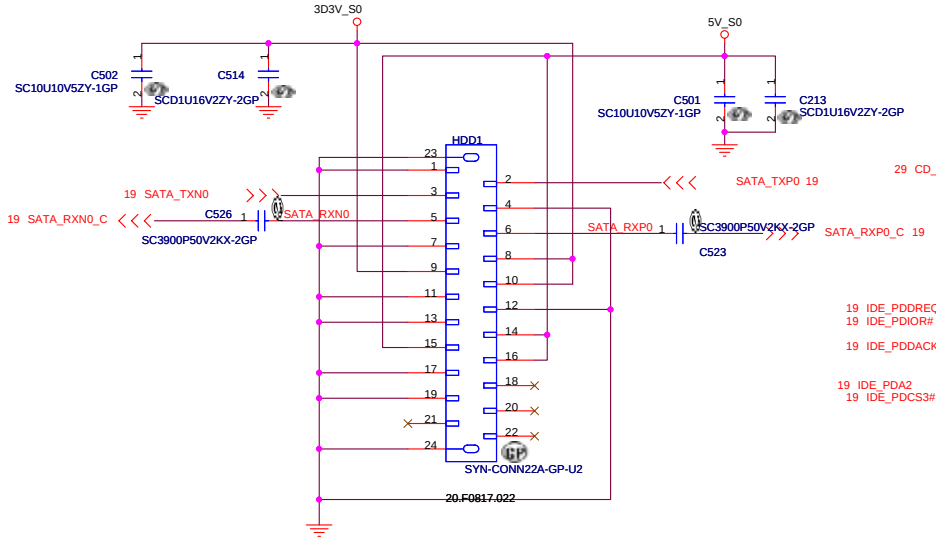
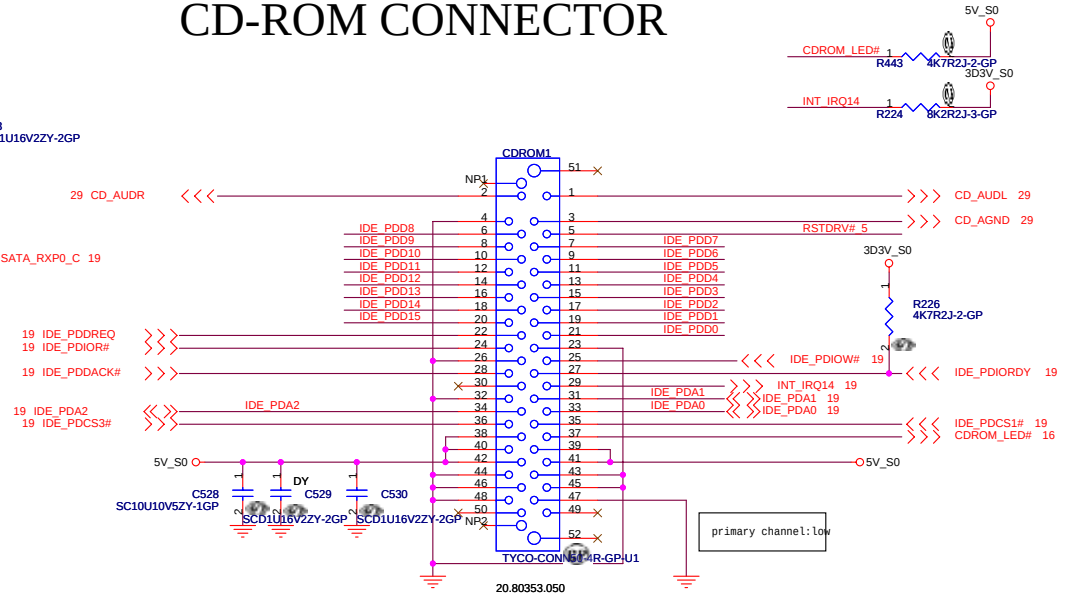
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Thermal/Fan Controllor G792***
Size: Custom	Document Number: **Pamirs**
Rev	**-3**
Date: Monday, May 21, 2007	Sheet 22 of 41

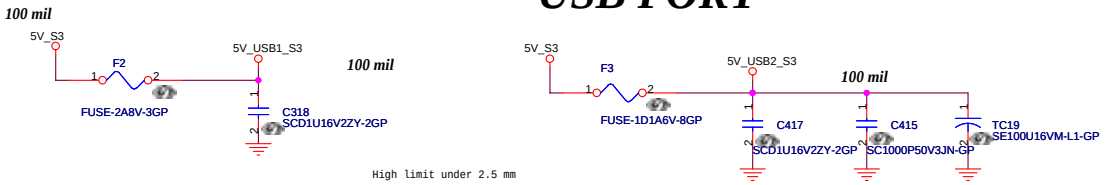
SATA HD Connector

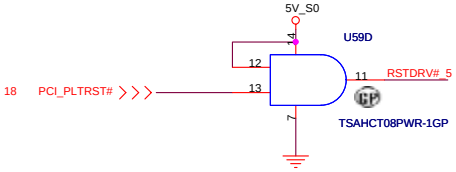


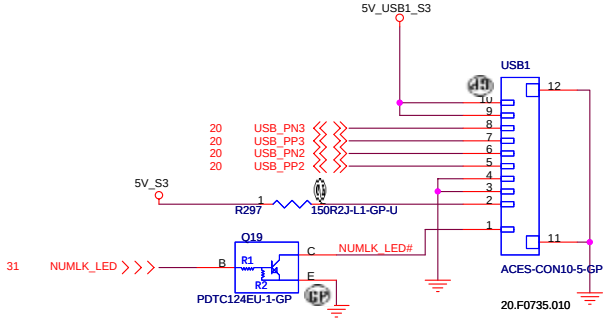
CD-ROM CONNECTOR

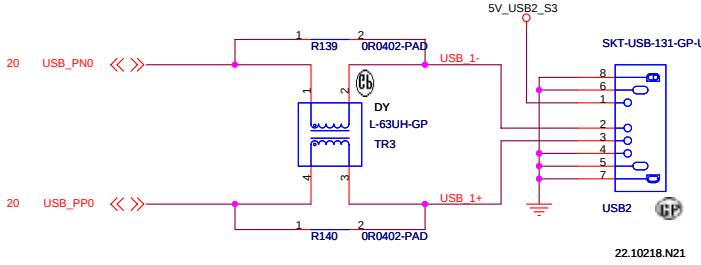


USB PORT









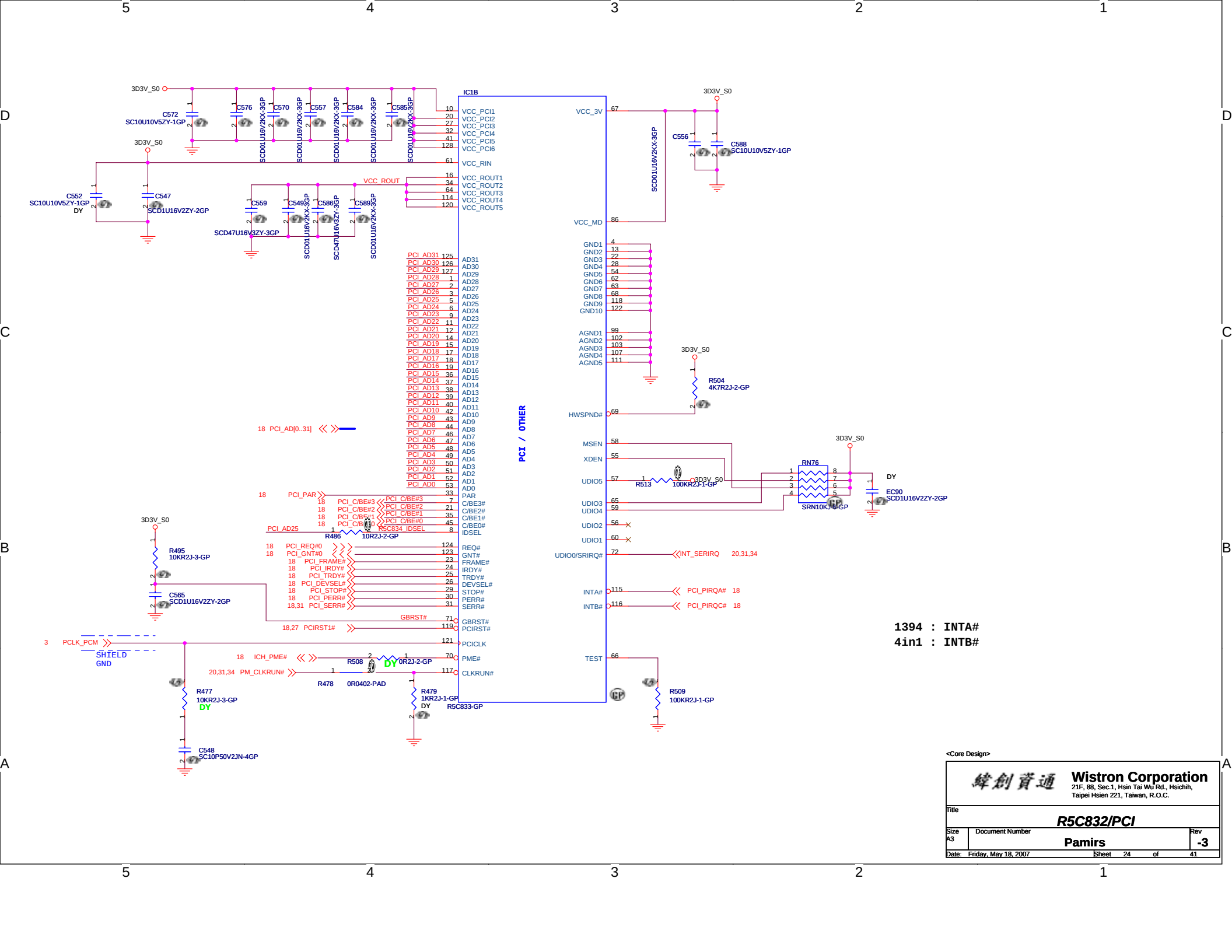
<Core Design>

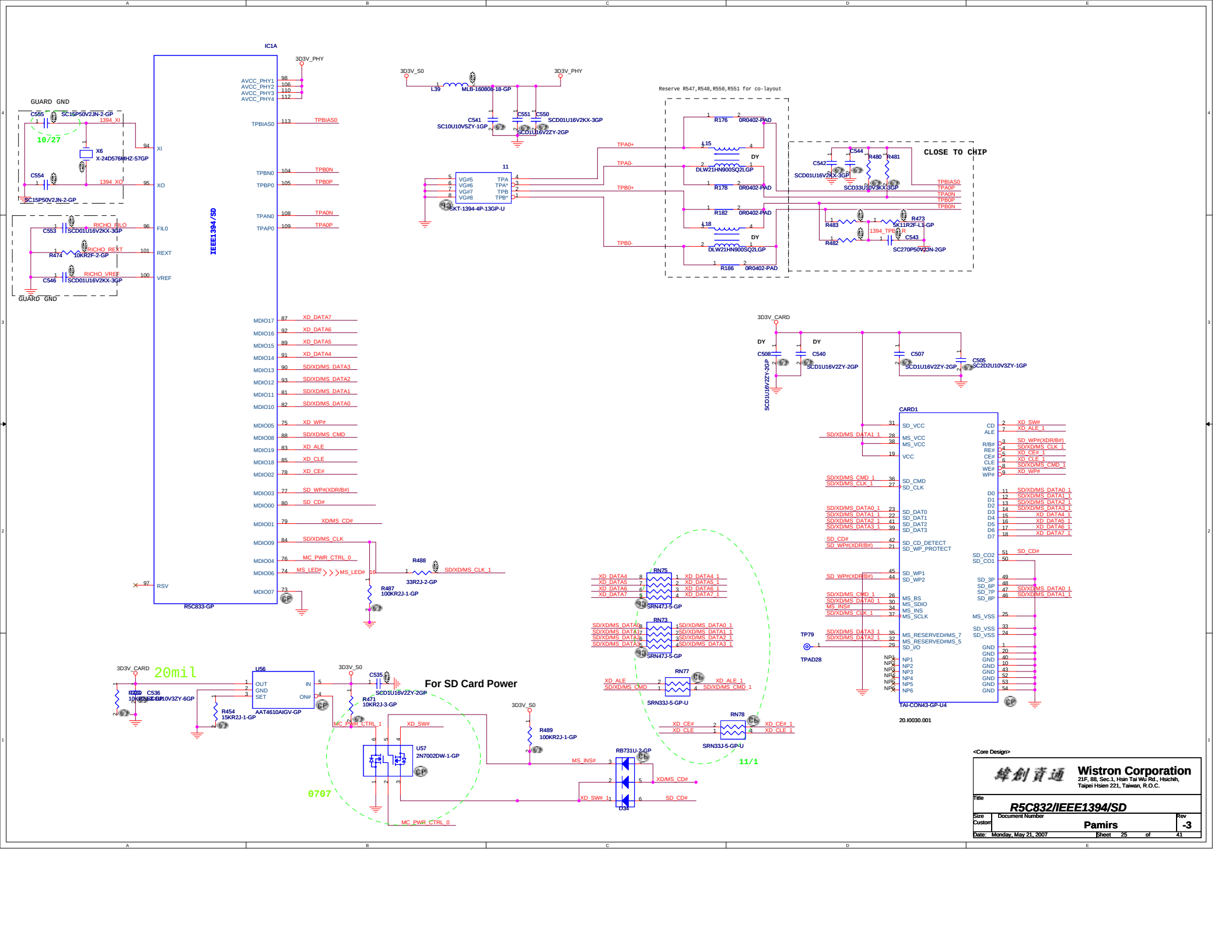
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HD/CDROM/USB**

Size: A3 | Document Number: Pamirs | Rev: -3

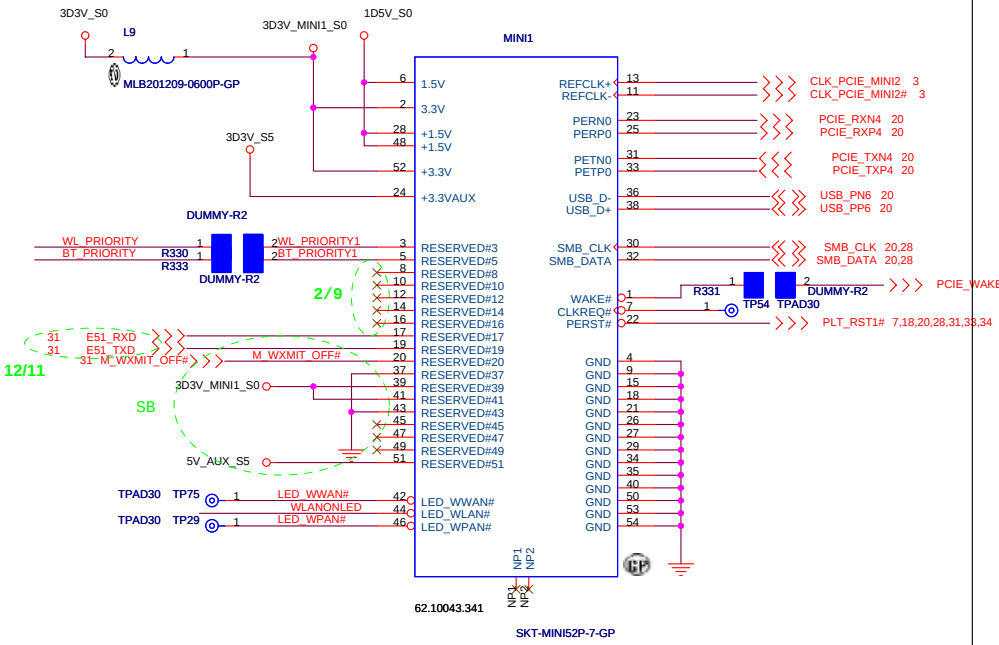
Date: Friday, May 18, 2007 | Sheet 23 of 41

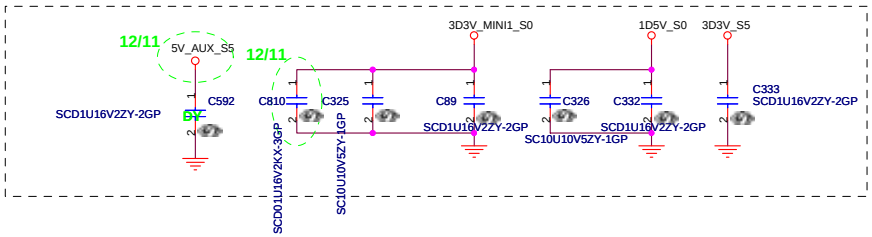

IC1B
PCI / OTHER
R5C833-GP
3D3V_S0
C572
SC10U10V5ZY-1GP
C576
C570
C557
C584
C585
SCD01U16V2KX-3GP
C552
SC10U10V5ZY-1GP
DY
C547
SCD1U16V2ZY-2GP
C559
C549
C586
C589
SCD47U16V3ZY-3GP
SCD47U16V2ZY-3GP
VCC_ROUT
VCC_PCI1
VCC_PCI2
VCC_PCI3
VCC_PCI4
VCC_PCI5
VCC_PCI6
VCC_RIN
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5
VCC_3V
VCC_MD
C556
C588
SC10U10V5ZY-1GP
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
AGND1
AGND2
AGND3
AGND4
AGND5
R504
4K7R2J-2-GP
HWSPND#
MSEN
XDEN
UDIO5
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SRIRQ#
INT_SERIRQ
20,31,34
INTA#
INTB#
PCI_PIRQA#
PCI_PIRQC#
TEST
R513
100KR2J-1-GP
RN76
SRN10KJ-6-GP
EC90
SCD1U16V2ZY-2GP
R509
100KR2J-1-GP
18 PCI_AD[0..31]
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
18 PCI_PAR
PAR
18 PCI_C/BE#3
18 PCI_C/BE#2
18 PCI_C/BE#1
18 PCI_C/BE#0
C/BE3#
C/BE2#
C/BE1#
C/BE0#
PCI_AD25
R5C834_IDSEL
IDSEL
R486
10R2J-2-GP
18 PCI_REQ#0
18 PCI_GNT#0
REQ#
GNT#
18 PCI_FRAME#
18 PCI_IRDY#
18 PCI_TRDY#
18 PCI_DEVSEL#
18 PCI_STOP#
18 PCI_PERR#
18,31 PCI_SERR#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PERR#
SERR#
GBRST#
18,27 PCIRST1#
GBRST#
PCIRST#
3 PCLK_PCM
PCICLK
SHIELD
GND
18 ICH_PME#
R508
DY
0R2J-2-GP
PME#
20,31,34 PM_CLKRUN#
R478
0R0402-PAD
CLKRUN#
R495
10KR2J-3-GP
C565
SCD1U16V2ZY-2GP
R477
10KR2J-3-GP
DY
C548
SC10P50V2JN-4GP
R479
1KR2J-1-GP
DY
1394 : INTA#
4in1 : INTB#
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
R5C832/PCI
Size A3
Document Number
Pamirs
Rev
-3
Date: Friday, May 18, 2007
Sheet 24 of 41


IC1A
R5C833-GP
IEEE1394/SD
3D3V_PHY
AVCC_PHY1
AVCC_PHY2
AVCC_PHY3
AVCC_PHY4
TPBIAS0
TPBN0
TPBP0
TPAN0
TPAP0
XI
XO
FIL0
REXT
VREF
RSV
GUARD GND
C555 SC15P50V2JN-2-GP
1394_XI
10/27
X6
X-24D576MHZ-57GP
C554 SC15P50V2JN-2-GP
1394_XO
C553 SCD01U16V2KX-3GP
RICHO_FILO
R474 10KR2F-2-GP
RICHO_REXT
C546 SCD01U16V2KX-3GP
RICHO_VREF
MDIO17 XD_DATA7
MDIO16 XD_DATA6
MDIO15 XD_DATA5
MDIO14 XD_DATA4
MDIO13 SD/XD/MS_DATA3
MDIO12 SD/XD/MS_DATA2
MDIO11 SD/XD/MS_DATA1
MDIO10 SD/XD/MS_DATA0
MDIO05 XD_WP#
MDIO08 SD/XD/MS_CMD
MDIO19 XD_ALE
MDIO18 XD_CLE
MDIO02 XD_CE#
MDIO03 SD_WP#(XDR/B#)
MDIO00 SD_CD#
MDIO01 XD/MS_CD#
MDIO09 SD/XD/MS_CLK
MDIO04 MC_PWR_CTRL_0
MDIO06 MS_LED#
MDIO07
R488 33R2J-2-GP
SD/XD/MS_CLK_1
R487 100KR2J-1-GP
3D3V_S0
L39 MLB-160808-18-GP
C541 SC10U10V5ZY-1GP
C551 C550
SCD01U16V2KX-3GP
SCD01U16V2ZY-2GP
11
VG#5 VG#6 VG#7 VG#8
TPA TPA* TPB TPB*
SKT-1394-4P-13GP-U
TPA0+
TPA0-
TPB0+
TPB0-
Reserve R547,R548,R550,R551 for co-layout
R176 0R0402-PAD
15
DY
DLW21HN900SQ2LGP
R178 0R0402-PAD
R182 0R0402-PAD
18
DY
DLW21HN900SQ2LGP
R186 0R0402-PAD
CLOSE TO CHIP
C544
C542 SCD01U16V2KX-3GP
R480 R481
SCD33U10V3KX-3GP
TPBIAS0
TPA0P
TPA0N
TPB0P
TPB0N
R483
R482
SK11R2F-L1-GP
1394_TPB0_R
R473
C543 SC270P50V2JN-2GP
3D3V_CARD
DY
C508 SCD1U16V2ZY-2GP
C540 SCD1U16V2ZY-2GP
C507 SCD1U16V2ZY-2GP
C505 SC2D2U10V3ZY-1GP
CARD1
SD_VCC
MS_VCC
MS_VCC
VCC
SD_CMD
SD_CLK
SD_DAT0
SD_DAT1
SD_DAT2
SD_DAT3
SD_CD#
SD_CD_DETECT
SD_WP_PROTECT
SD_WP1
SD_WP2
MS_BS
MS_SDIO
MS_INS
MS_SCLK
MS_RESERVED#MS_7
MS_RESERVED#MS_5
SD_I/O
NP1 NP2 NP3 NP4 NP5 NP6
CD
ALE
R/B#
RE#
CE#
CLE
WE#
WP#
D0 D1 D2 D3 D4 D5 D6 D7
SD_CO2
SD_CO1
SD_3P
SD_6P
SD_7P
SD_8P
MS_VSS
SD_VSS
GND
TAI-CON43-GP-U4
20.I0030.001
TP79
TPAD28
RN75 SRN47J-5-GP
RN73 SRN47J-5-GP
RN77 SRN33J-5-GP-U
RN78 SRN33J-5-GP-U
11/1
3D3V_CARD
20mil
U56
OUT GND SET IN ON#
AAT4610AIGV-GP
C536 SCD1U10V3ZY-6GP
R454 15KR2J-1-GP
3D3V_S0
C535 SCD1U16V2ZY-2GP
For SD Card Power
R471 10KR2J-3-GP
MC_PWR_CTRL_1
XD_SW#
U57 2N7002DW-1-GP
0707
R489 100KR2J-1-GP
MS_INS#
XD/MS_CD#
XD_SW#_1
SD_CD#
MC_PWR_CTRL_0
RB731U-2-GP
D34
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
R5C832/IEEE1394/SD
Size Custom
Document Number
Pamirs
Rev -3
Date: Monday, May 21, 2007
Sheet 25 of 41

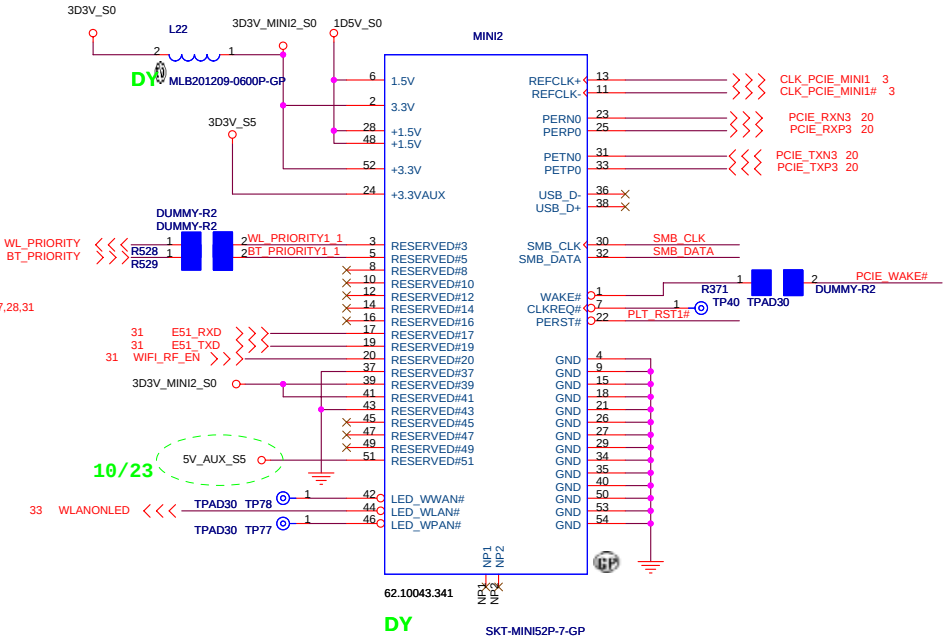
Mini Card Connector

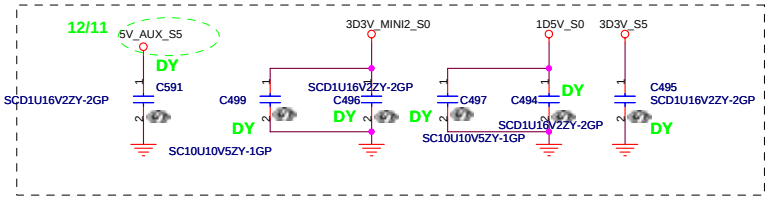
Mini Card Connector 1(WWAN)





Mini Card Connector 2(802.11a/b/g)





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN .

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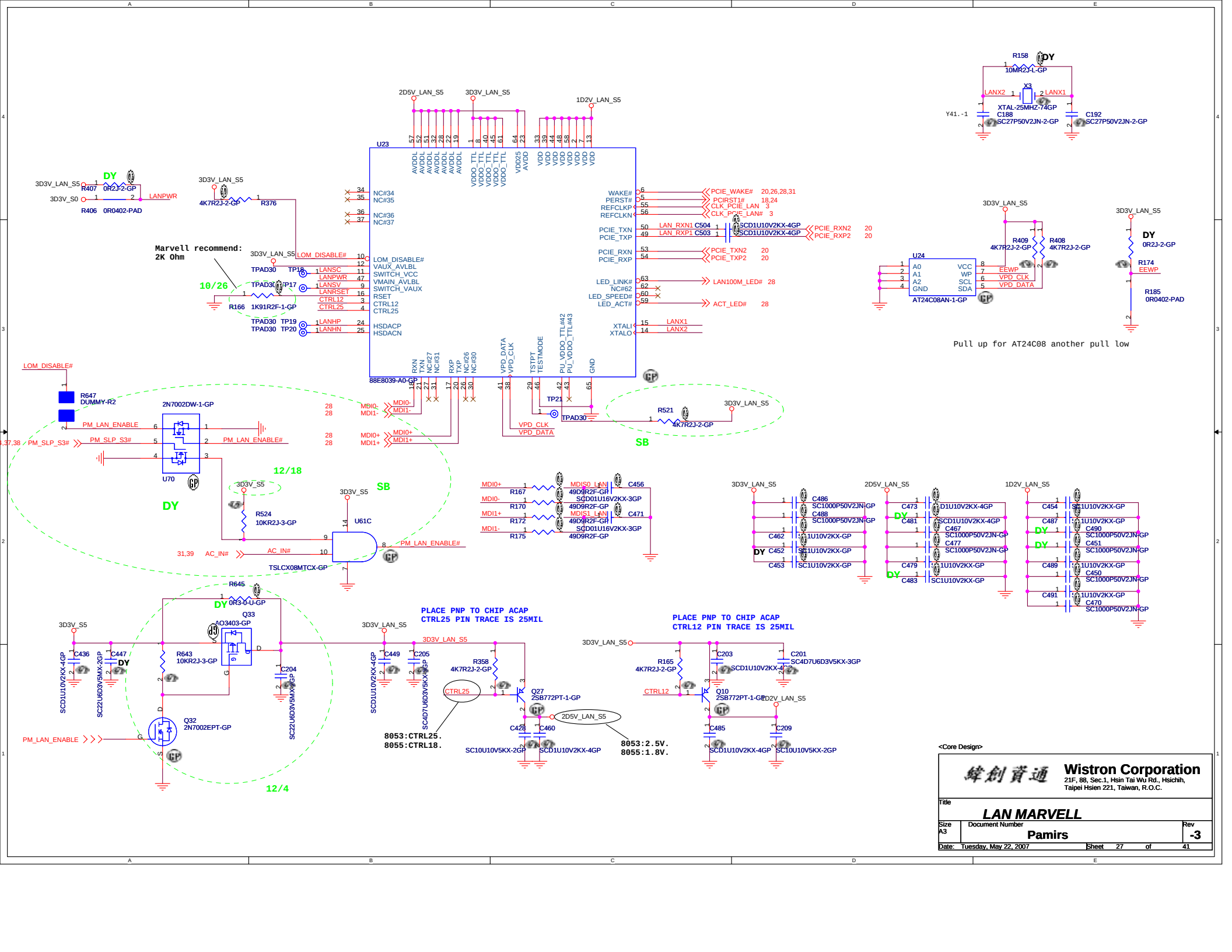
U23
88E8039-A0-GP
Marvell recommend:
2K Ohm
10/26
12/18
12/4
SB
DY
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
8053:CTRL25.
8055:CTRL18.
8053:2.5V.
8055:1.8V.
Pull up for AT24C08 another pull low
U70
U61C
U24
Q33
Q32
Q27
Q10
TSLCX08MTCX-GP
AT24C08AN-1-GP
2N7002DW-1-GP
2N7002EPT-GP
AO3403-GP
2SB772PT-1-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN MARVELL
Size A3
Document Number
Pamirs
Rev
-3
Date: Tuesday, May 22, 2007
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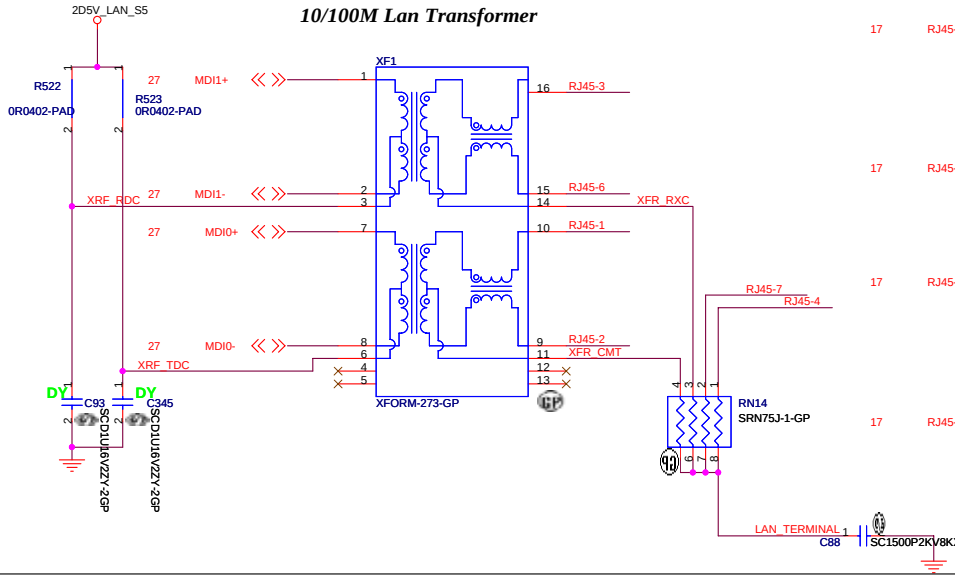
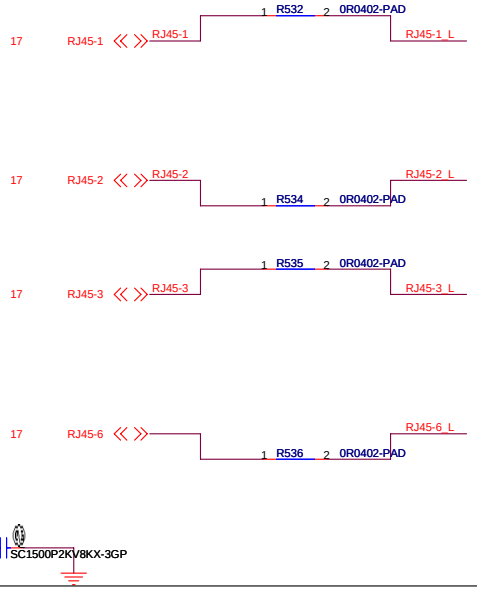
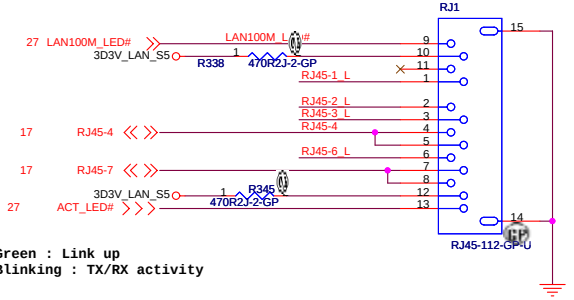




1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

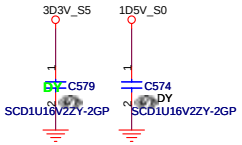
PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW



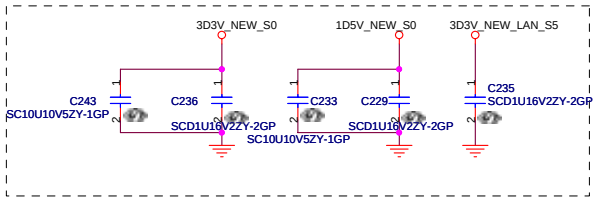
Green : Link up
Blinking : TX/RX activity

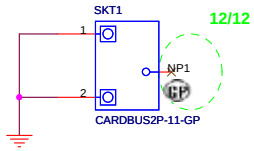
NEWCARD Connector

Place them Near to Chip

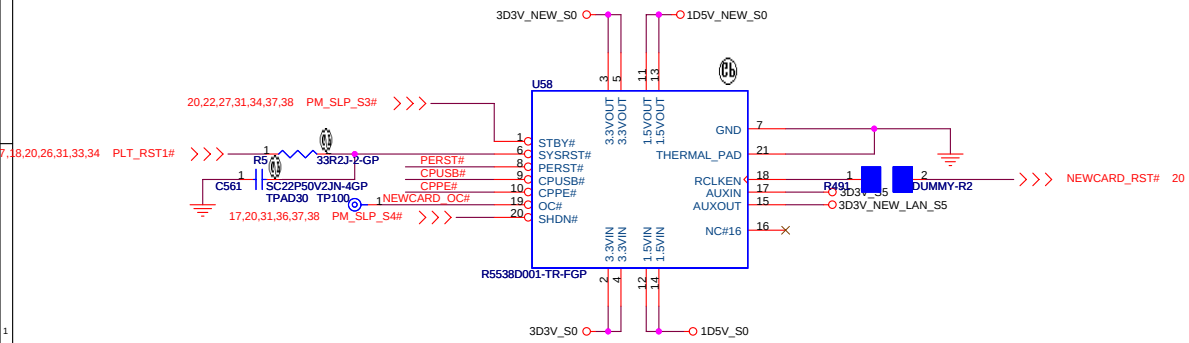


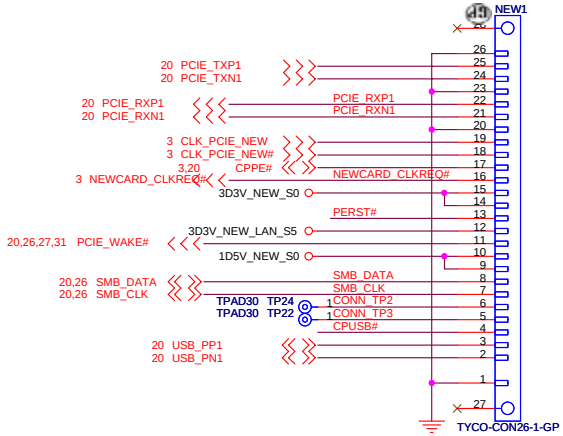
Place them Near to Connector

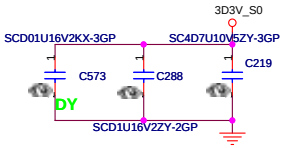




For Newcard socket







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN connector/NEW CARD/SIM

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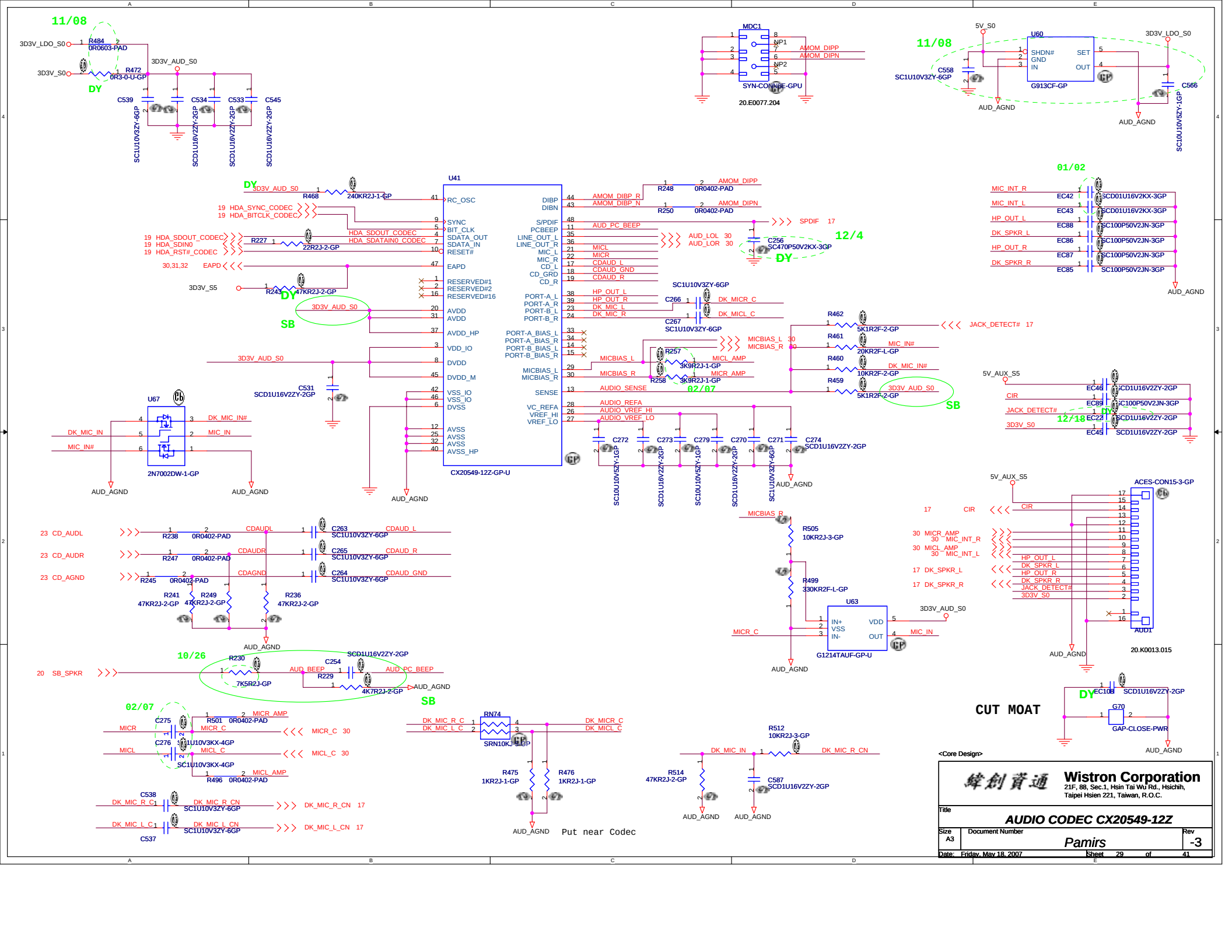
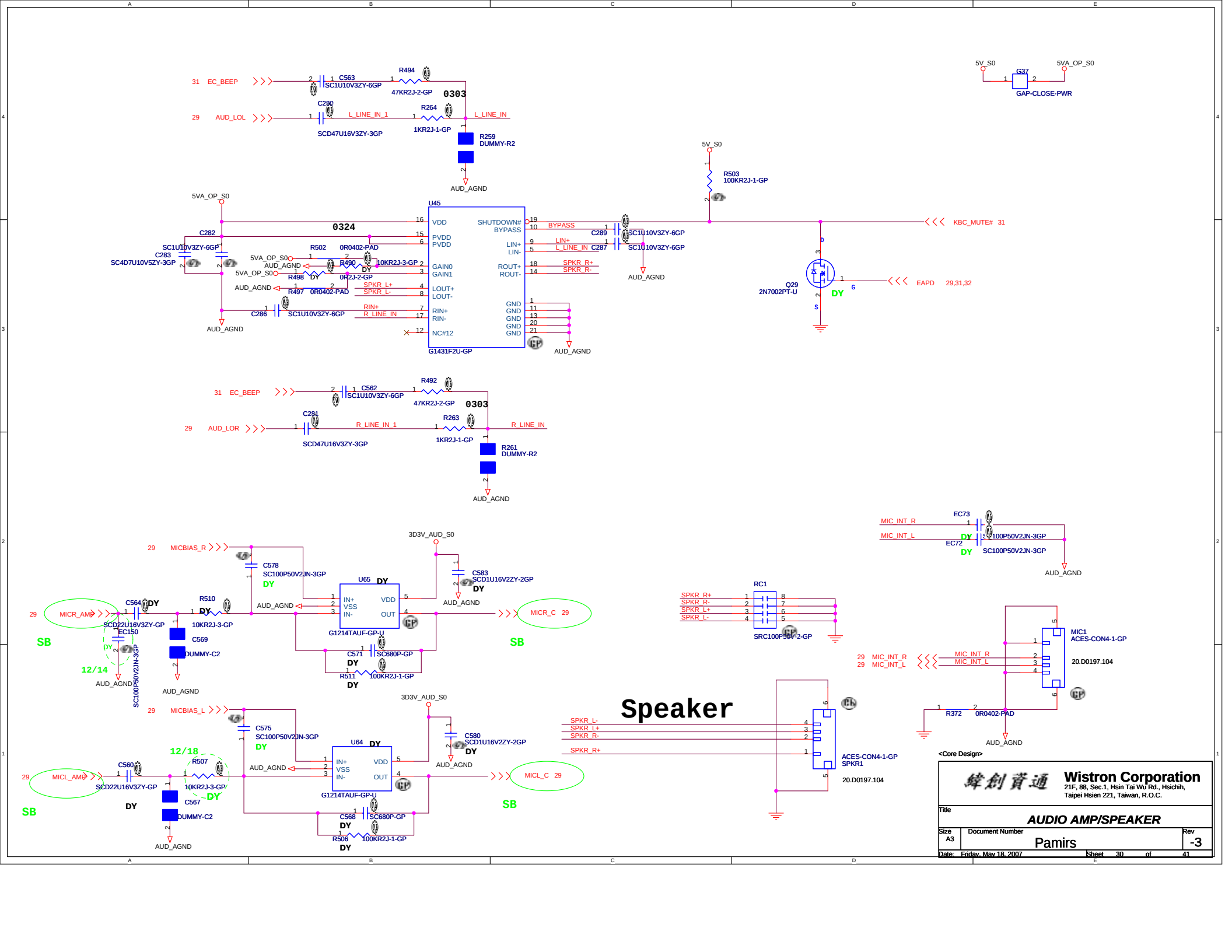
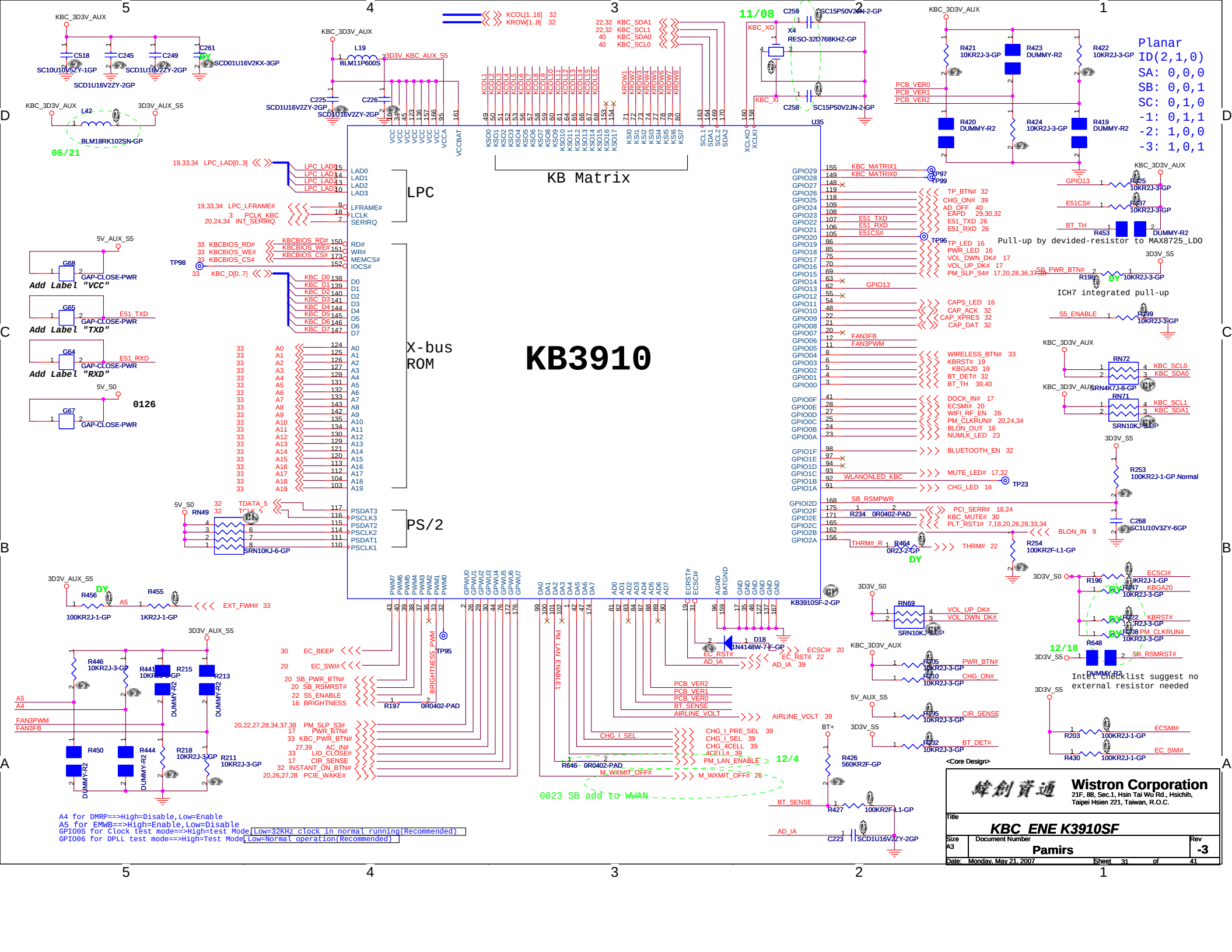
CLOSE TO TRANSFORMER


11/08
3D3V_LDO_S0
R484 0R0603-PAD
3D3V_S0
R472 0R3-0-U-GP
3D3V_AUD_S0
DY
C539 SC1U10V3ZY-6GP
C534 SCD1U16V2ZY-2GP
C533 SCD1U16V2ZY-2GP
C545 SCD1U16V2ZY-2GP
MDC1
NP1
NP2
AMOM_DIPP
AMOM_DIPN
SYN-CONNPE-GPU
20.E0077.204
11/08
5V_S0
U60
SHDN#
GND
IN
SET
OUT
G913CF-GP
3D3V_LDO_S0
C558 SC1U10V3ZY-6GP
C566 SC10U10V5ZY-1GP
AUD_AGND
01/02
MIC_INT_R
MIC_INT_L
HP_OUT_L
DK_SPKR_L
HP_OUT_R
DK_SPKR_R
EC42 SCD01U16V2KX-3GP
EC43 SCD01U16V2KX-3GP
EC88 SC100P50V2JN-3GP
EC86 SC100P50V2JN-3GP
EC87 SC100P50V2JN-3GP
EC85 SC100P50V2JN-3GP
U41
CX20549-12Z-GP-U
RC_OSC
SYNC
BIT_CLK
SDATA_OUT
SDATA_IN
RESET#
EAPD
RESERVED#1
RESERVED#2
RESERVED#16
AVDD
AVDD
AVDD_HP
VDD_IO
DVDD
DVDD_M
VSS_IO
VSS_IO
DVSS
AVSS
AVSS
AVSS
AVSS_HP
DIBP
DIBN
S/PDIF
PCBEEP
LINE_OUT_L
LINE_OUT_R
MIC_L
MIC_R
CD_L
CD_GRD
CD_R
PORT-A_L
PORT-A_R
PORT-B_L
PORT-B_R
PORT-A_BIAS_L
PORT-A_BIAS_R
PORT-B_BIAS_L
PORT-B_BIAS_R
MICBIAS_L
MICBIAS_R
SENSE
VC_REFA
VREF_HI
VREF_LO
DY
3D3V_AUD_S0
R468 240KR2J-1-GP
19 HDA_SYNC_CODEC
19 HDA_BITCLK_CODEC
19 HDA_SDOUT_CODEC
19 HDA_SDIN0
19 HDA_RST#_CODEC
R227 22R2J-2-GP
HDA_SDOUT_CODEC
HDA_SDATAIN0_CODEC
30,31,32 EAPD
3D3V_S5
R243 47KR2J-2-GP
DY
SB
3D3V_AUD_S0
C531 SCD1U16V2ZY-2GP
AUD_AGND
R248 0R0402-PAD
R250 0R0402-PAD
AMOM_DIPP
AMOM_DIPN
SPDIF 17
AUD_PC_BEEP
AUD_LOL 30
AUD_LOR 30
12/4
C256 SC470P50V2KX-3GP
DY
MICL
MICR
CDAUD_L
CDAUD_GND
CDAUD_R
HP_OUT_L
HP_OUT_R
DK_MIC_L
DK_MIC_R
SC1U10V3ZY-6GP
C266 DK_MICR_C
C267 DK_MICL_C
SC1U10V3ZY-6GP
MICBIAS_L 30
MICBIAS_R 30
R257 3K9R2J-1-GP
R258 3K9R2J-1-GP
MICL_AMP
MICR_AMP
02/07
AUDIO_SENSE
AUDIO_REFA
AUDIO_VREF_HI
AUDIO_VREF_LO
C272 SC10U10V5ZY-1GP
C273 SCD1U16V2ZY-2GP
C279 SC10U10V5ZY-1GP
C270 SCD1U16V2ZY-2GP
C271 SC1U10V3ZY-6GP
C274 SCD1U16V2ZY-2GP
AUD_AGND
R462 5K1R2F-2-GP
R461 20KR2F-L-GP
R460 10KR2F-2-GP
R459 5K1R2F-2-GP
JACK_DETECT# 17
MIC_IN# 17
DK_MIC_IN# 17
3D3V_AUD_S0
SB
5V_AUX_S5
CIR
JACK_DETECT#
3D3V_S0
EC46 SCD1U16V2ZY-2GP
EC89 SC100P50V2JN-3GP
EC22 SCD1U16V2ZY-2GP
EC45 SCD1U16V2ZY-2GP
12/18
DY
U67
2N7002DW-1-GP
DK_MIC_IN#
DK_MIC_IN
MIC_IN
MIC_IN#
AUD_AGND
23 CD_AUDL
23 CD_AUDR
23 CD_AGND
R238 0R0402-PAD
R247 0R0402-PAD
R245 0R0402-PAD
CDAUDL
CDAUDR
CDAGND
C263 SC1U10V3ZY-6GP
C265 SC1U10V3ZY-6GP
C264 SC1U10V3ZY-6GP
R241 47KR2J-2-GP
R249 47KR2J-2-GP
R236 47KR2J-2-GP
AUD_AGND
MICBIAS_R
R505 10KR2J-3-GP
R499 330KR2F-L-GP
U63
G1214TAUF-GP-U
IN+
VSS
IN-
VDD
OUT
MIC_IN
MICR_C
3D3V_AUD_S0
AUD_AGND
17 CIR
30 MICR_AMP
30 MICL_AMP
30 MIC_INT_R
30 MIC_INT_L
17 DK_SPKR_L
17 DK_SPKR_R
HP_OUT_L
DK_SPKR_L
HP_OUT_R
DK_SPKR_R
JACK_DETECT#
3D3V_S0
ACES-CON15-3-GP
AUD1
20.K0013.015
AUD_AGND
10/26
20 SB_SPKR
R230 7K5R2J-GP
C254 SCD1U16V2ZY-2GP
R229 4K7R2J-2-GP
AUD_BEEP
AUD_PC_BEEP
AUD_AGND
SB
02/07
MICR
MICL
C275
C276
SC1U10V3KX-4GP
SC1U10V3KX-4GP
R501 0R0402-PAD
R496 0R0402-PAD
MICR_AMP
MICL_AMP
MICR_C 30
MICL_C 30
C538 DK_MIC_R_CN
C537 DK_MIC_L_CN
SC1U10V3ZY-6GP
DK_MIC_R_CN 17
DK_MIC_L_CN 17
DK_MIC_R_C
DK_MIC_L_C
RN74
SRN10KJ-GP
DK_MICR_C
DK_MICL_C
R475 1KR2J-1-GP
R476 1KR2J-1-GP
AUD_AGND
Put near Codec
R512 10KR2J-3-GP
DK_MIC_IN
DK_MIC_R_CN
R514 47KR2J-2-GP
C587 SCD1U16V2ZY-2GP
AUD_AGND
AUD_AGND
CUT MOAT
EC103 SCD1U16V2ZY-2GP
DY
G70
GAP-CLOSE-PWR
AUD_AGND
<Core Design>
蜂創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC CX20549-12Z
Size A3
Document Number
Pamirs
Rev -3
Date: Friday, May 18, 2007
Sheet 29 of 41


31 EC_BEEP
C563
SC1U10V3ZY-6GP
R494
47KR2J-2-GP
0303
29 AUD_LOL
C290
L_LINE_IN_1
R264
1KR2J-1-GP
L_LINE_IN
R259
DUMMY-R2
AUD_AGND
5V_S0
G37
5VA_OP_S0
GAP-CLOSE-PWR
R503
100KR2J-1-GP
5VA_OP_S0
U45
0324
VDD
PVDD
PVDD
GAIN0
GAIN1
LOUT+
LOUT-
RIN+
RIN-
NC#12
SHUTDOWN#
BYPASS
LIN+
LIN-
ROUT+
ROUT-
GND
G1431F2U-GP
C282
SC1U10V3ZY-6GP
C283
SC4D7U10V5ZY-3GP
R502
0R0402-PAD
R490
10KR2J-3-GP
R498
0R2J-2-GP
DY
R497
0R0402-PAD
SPKR_L+
SPKR_L-
C286
SC1U10V3ZY-6GP
RIN+
R_LINE_IN
BYPASS
C289
SC1U10V3ZY-6GP
LIN+
L_LINE_IN
C287
SC1U10V3ZY-6GP
SPKR_R+
SPKR_R-
KBC_MUTE# 31
Q29
2N7002PT-U
EAPD 29,31,32
31 EC_BEEP
C562
SC1U10V3ZY-6GP
R492
47KR2J-2-GP
0303
29 AUD_LOR
C281
R_LINE_IN_1
R263
1KR2J-1-GP
R_LINE_IN
R261
DUMMY-R2
AUD_AGND
MIC_INT_R
MIC_INT_L
EC73
EC72
SC100P50V2JN-3GP
DY
29 MICBIAS_R
C578
SC100P50V2JN-3GP
U65
G1214TAUF-GP-U
3D3V_AUD_S0
C583
SCD1U16V2ZY-2GP
29 MICR_AMP
C564
SCD22U16V3ZY-GP
EC150
SC100P50V2JN-3GP
R510
10KR2J-3-GP
C569
DUMMY-C2
12/14
C571
SC680P-GP
R511
100KR2J-1-GP
MICR_C 29
SB
SPKR_R+
SPKR_R-
SPKR_L+
SPKR_L-
RC1
SRC100P50V-2-GP
MIC1
ACES-CON4-1-GP
20.D0197.104
R372
0R0402-PAD
29 MICBIAS_L
C575
SC100P50V2JN-3GP
U64
G1214TAUF-GP-U
C580
SCD1U16V2ZY-2GP
29 MICL_AMP
C560
SCD22U16V3ZY-GP
R507
10KR2J-3-GP
C567
DUMMY-C2
12/18
C568
SC680P-GP
R506
100KR2J-1-GP
MICL_C 29
Speaker
SPKR_L-
SPKR_L+
SPKR_R-
SPKR_R+
SPKR1
ACES-CON4-1-GP
20.D0197.104
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO AMP/SPEAKER
Size A3
Document Number
Pamirs
Rev -3
Date: Friday, May 18, 2007
Sheet 30 of 41


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
U35
KB3910SF-2-GP
Planar ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
-1: 0,1,1
-2: 1,0,0
-3: 1,0,1
11/08
05/21
0126
12/4
0823 SB add to WWAN
Add Label "VCC"
Add Label "TXD"
Add Label "RXD"
Pull-up by devided-resistor to MAX8725_LDO
ICH7 integrated pull-up
Intel checklist suggest no external resistor needed
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=Test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC_ENE K3910SF
Pamirs
-3
Monday, May 21, 2007
31
41

CAMERA

Blue thumb

Internal KeyBoard Connector

31 KROW[1..8]
31 KCOL[1..16]

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

KB1
ACES-CON24-2-GP
20.K0220.024

TouchPad Connector

TPAD1
FOX-CON4-12-GP

CAM1
ACES-CON5-1GP
20.D0197.105

11/09
12/4
(3.93V)

U71
G913CF-GP
SC10U10V5ZY-1GP

BT1
ACES-CON8-4-GP
20.F0772.008

Close to CN8
0717Change from S5
MAX 150mA

U66
G913CF-GP

CAPACITY BUTTON

CAP1
ACES-CON12-4-GP
20.K0228.012

3/20
2/12

TOUCH-PAD SWITCH

SW1
SW-TACT-68-GP-U

RC6 SRC100P50V-2-GP
RC2 SRC100P50V-2-GP
RC5 SRC100P50V-2-GP
RC7 SRC100P50V-2-GP
RC3 SRC100P50V-2-GP
RC4 SRC100P50V-2-GP
for EMI

Q2
2N7002-11-GP

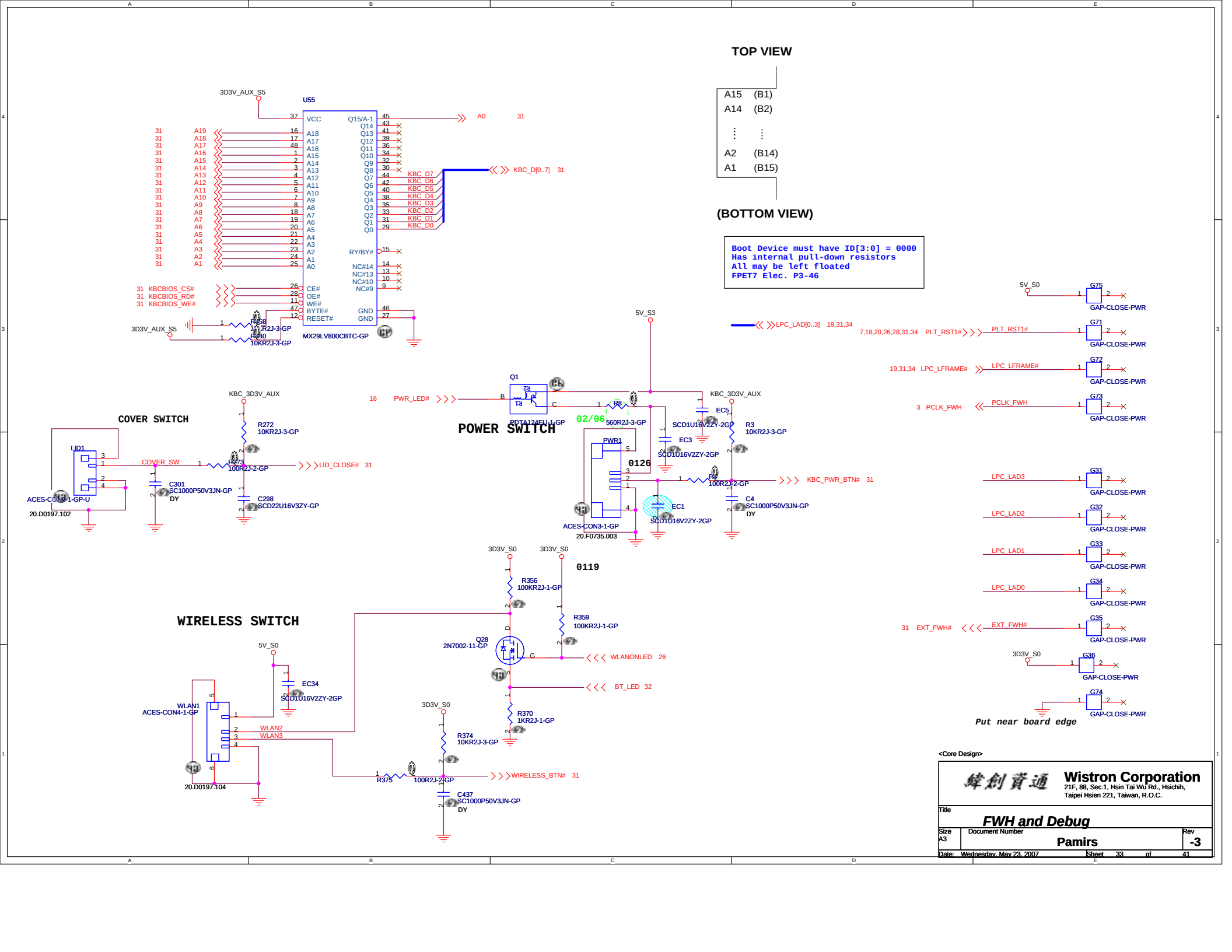
D31 D32 D17 D8 D6 D7 D5
BAV99W-1-GP

TR2 TR4
L-63UH-GP

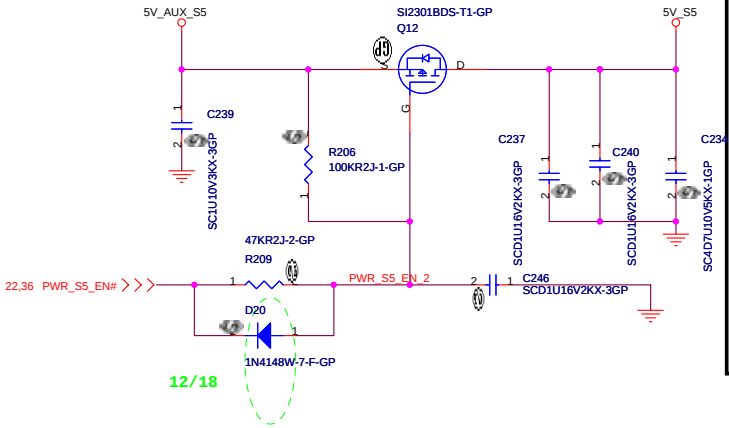
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

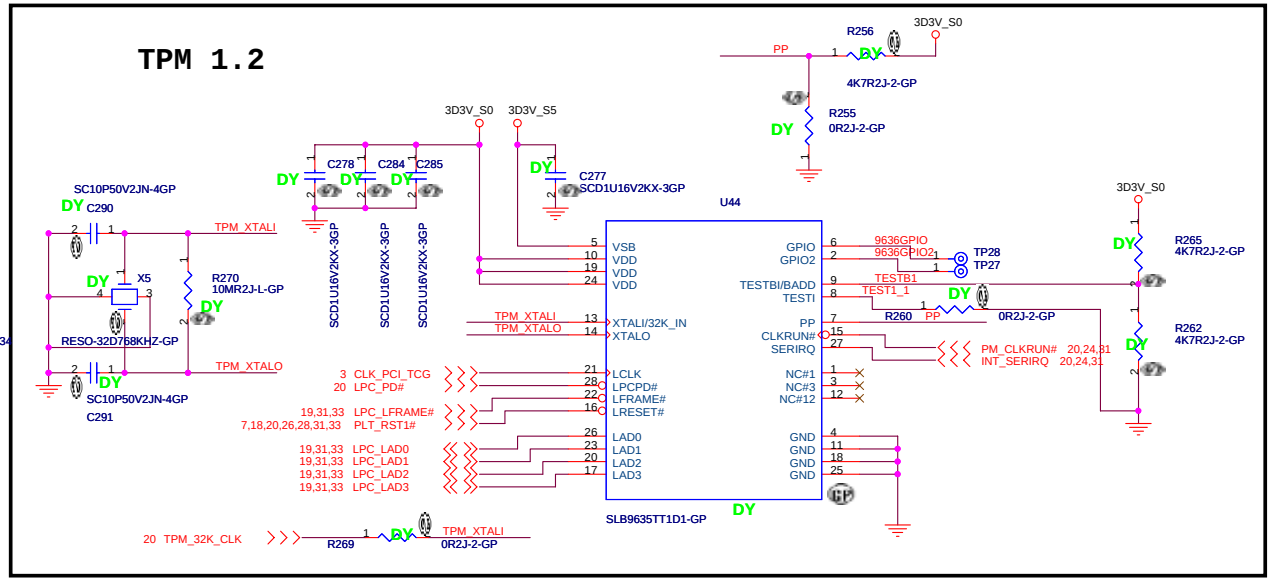
Title: KeyBoard-CONN
Size: A3
Document Number: Pamirs
Rev: -3
Date: Monday, May 21, 2007
Sheet 32 of 41


TOP VIEW
A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)
(BOTTOM VIEW)
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46
U55
MX29LV800CBTC-GP
COVER SWITCH
POWER SWITCH
WIRELESS SWITCH
02/06
0126
0119
Put near board edge
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
FWH and Debug
Size A3
Document Number
Pamirs
Rev -3
Date: Wednesday, May 23, 2007
Sheet 33 of 41

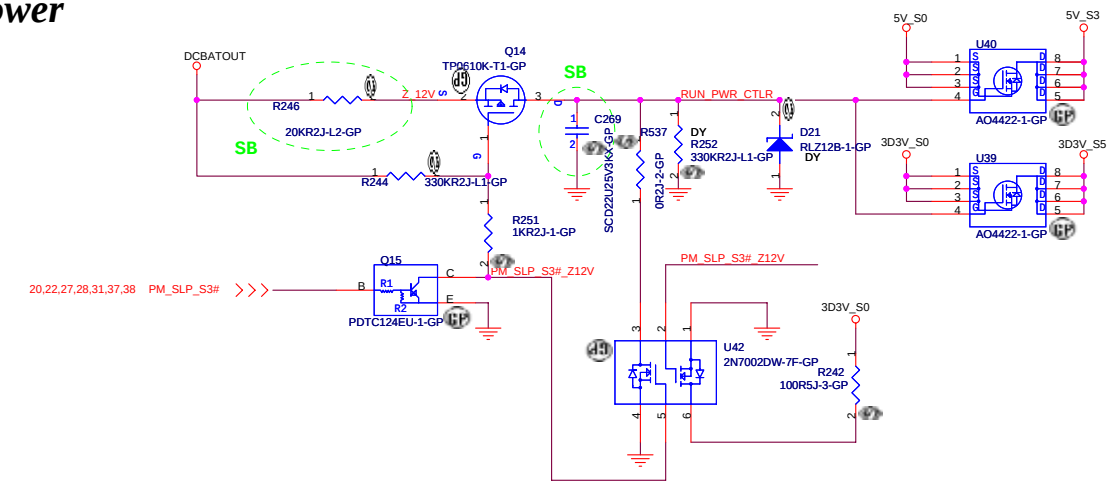
5V_AUX_S5 TO 5V_S5



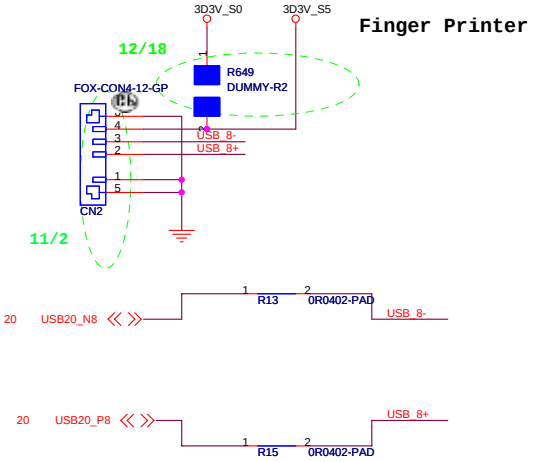
TPM 1.2



Run Power



Finger Printer



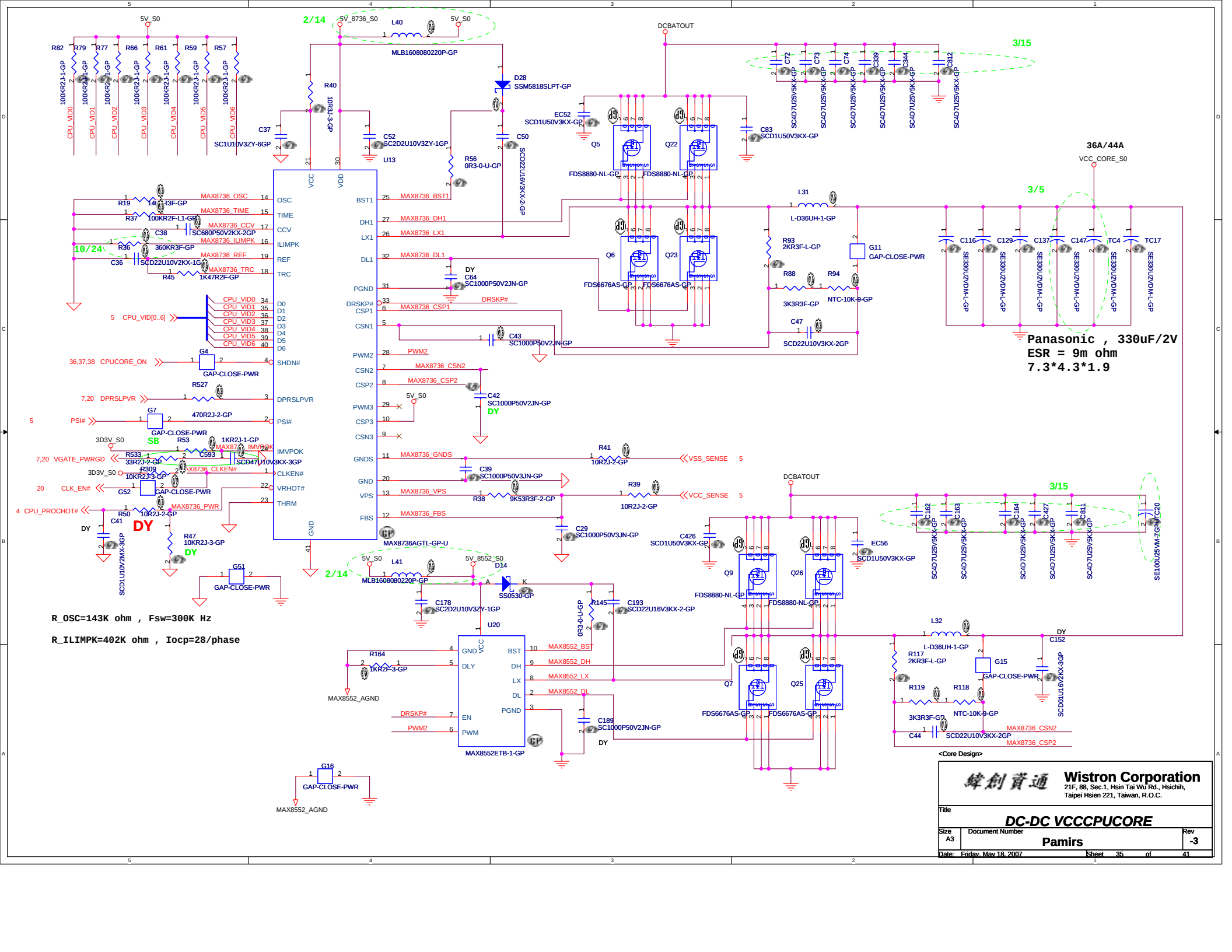
<Core Design>

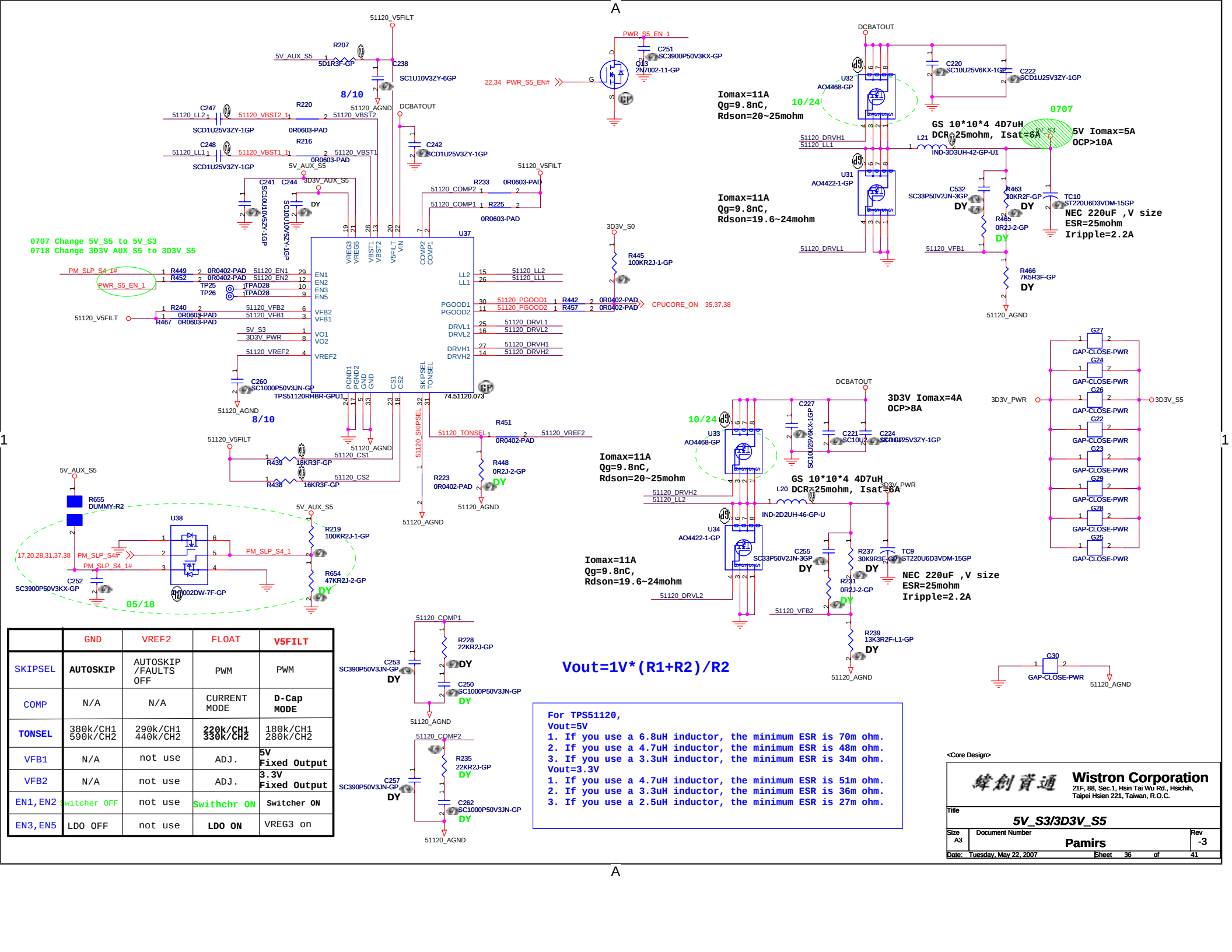
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PWRPLANE&RESETLOGIC**

Size	Document Number	Rev
A3	Pamirs	-3

Date: Monday, May 21, 2007 Sheet 34 of 41


MAX8736AGTL-GP-U
MAX8552ETB-1-GP
Panasonic , 330uF/2V
ESR = 9m ohm
7.3*4.3*1.9
R_OSC=143K ohm , Fsw=300K Hz
R_ILIMPK=402K ohm , Iocp=28/phase
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DC-DC VCCCPUCORE
Pamirs
Size A3
Rev -3
Date: Friday, May 18, 2007
Sheet 35 of 41



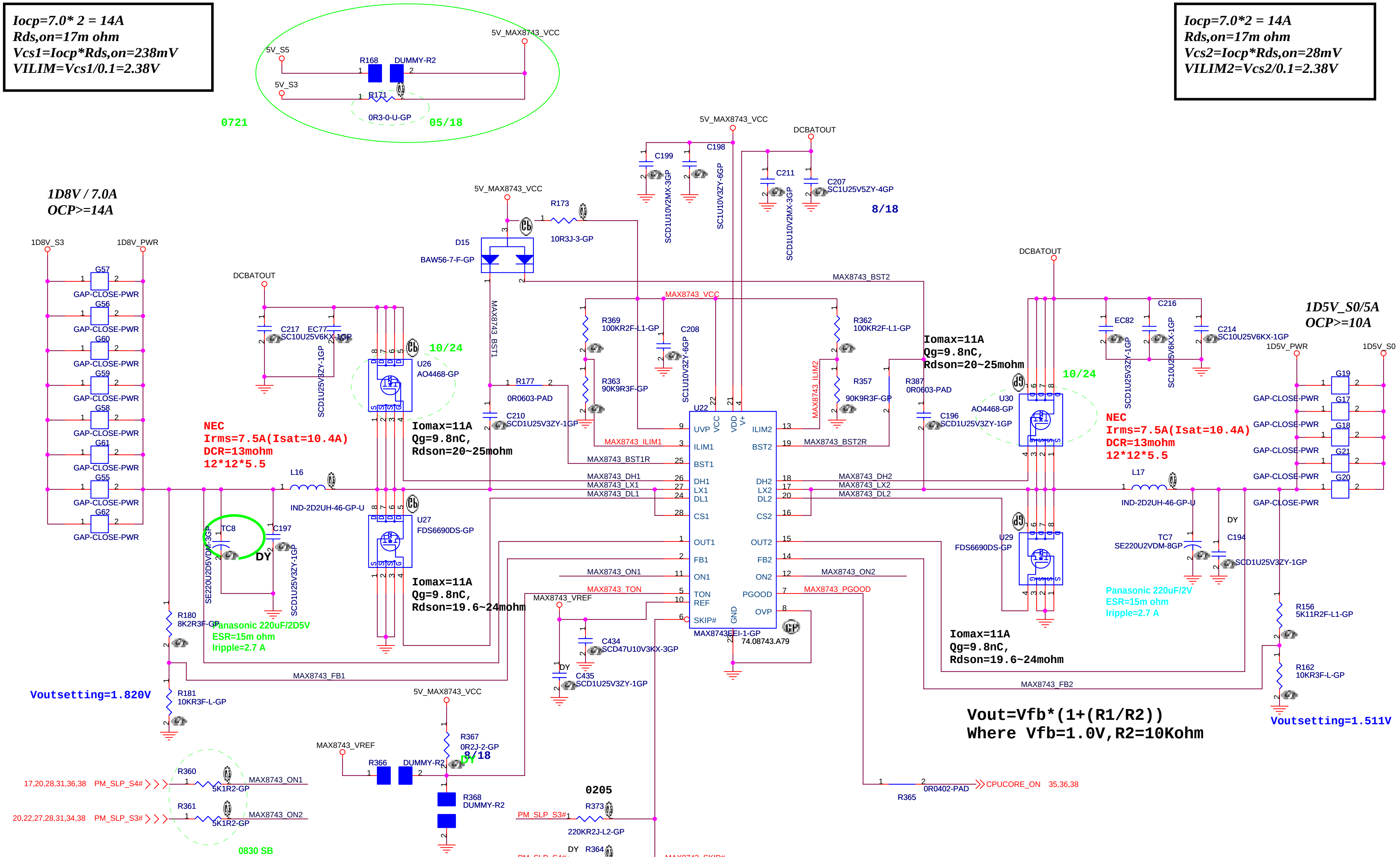
	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **5V_S3/3D3V_S5**

Size: A3 | Document Number: **Pamirs** | Rev: -3

Date: Tuesday, May 22, 2007 | Sheet 36 of 41

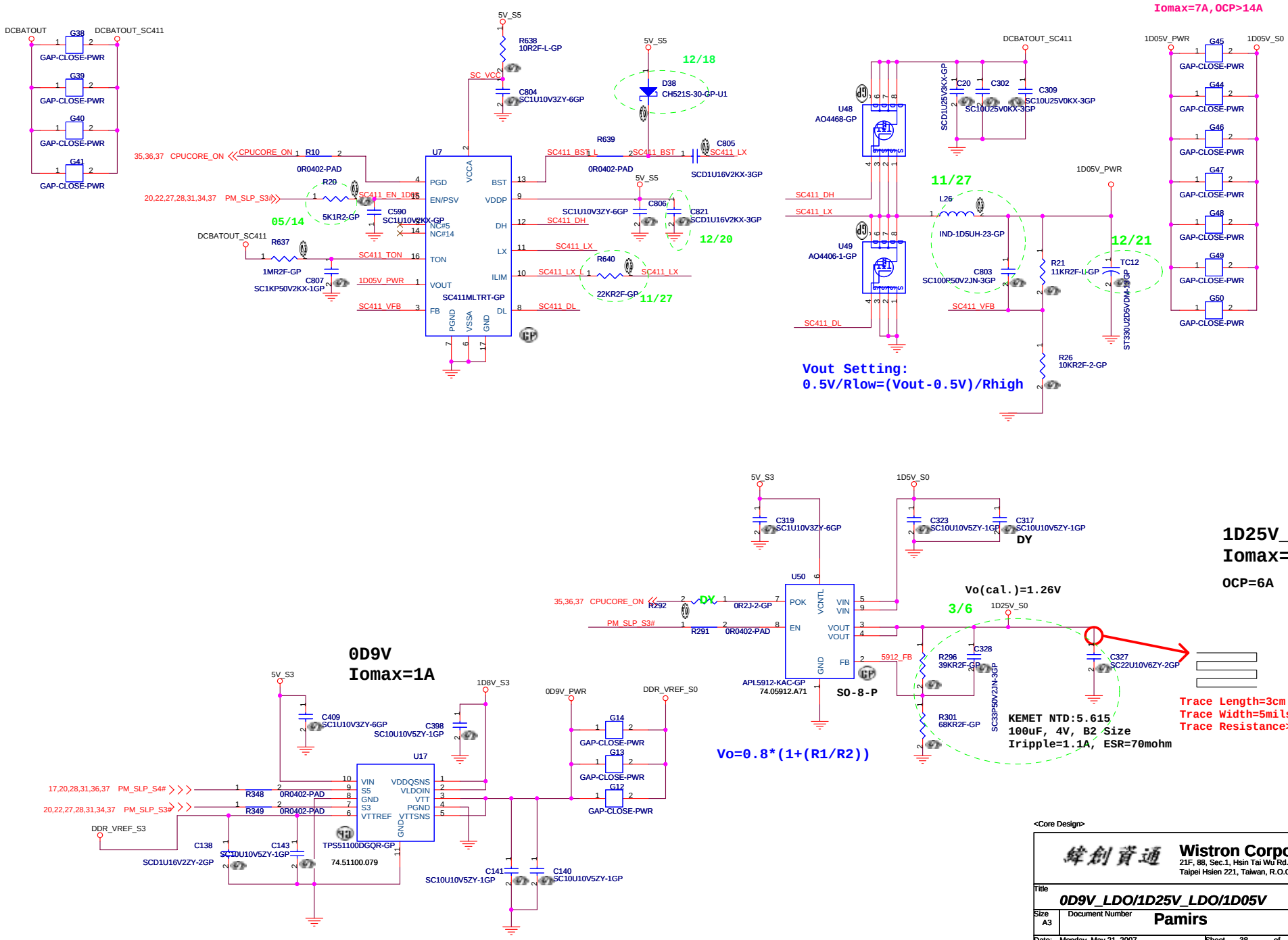

Iocp=7.0* 2 = 14A
Rds,on=17m ohm
Vcs1=Iocp*Rds,on=238mV
VILIM=Vcs1/0.1=2.38V
Iocp=7.0*2 = 14A
Rds,on=17m ohm
Vcs2=Iocp*Rds,on=28mV
VILIM2=Vcs2/0.1=2.38V
5V_S5
5V_S3
5V_MAX8743_VCC
R168
DUMMY-R2
R171
0R3-0-U-GP
0721
05/18
1D8V / 7.0A
OCP>=14A
1D8V_S3
1D8V_PWR
GAP-CLOSE-PWR
DCBATOUT
C217
EC77
SC10U25V6KX-1GP
D15
BAW56-7-F-GP
R173
10R3J-3-GP
C199
C198
SCD1U10V2MX-3GP
SC1U10V3ZY-6GP
C211
C207
SC1U25V5ZY-4GP
SCD1U10V2MX-3GP
8/18
MAX8743_BST2
MAX8743_VCC
R369
100KR2F-L1-GP
C208
R363
90K9R3F-GP
R362
100KR2F-L1-GP
R357
90K9R3F-GP
R387
0R0603-PAD
10/24
U26
AO4468-GP
R177
0R0603-PAD
C210
SCD1U25V3ZY-1GP
C196
SCD1U25V3ZY-1GP
U30
AO4468-GP
Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm
NEC
Irms=7.5A(Isat=10.4A)
DCR=13mohm
12*12*5.5
L16
IND-2D2UH-46-GP-U
L17
IND-2D2UH-46-GP-U
1D5V_S0/5A
OCP>=10A
1D5V_PWR
1D5V_S0
U22
MAX8743EEI-1-GP
74.08743.A79
UVP
ILIM1
BST1
DH1
LX1
DL1
CS1
OUT1
FB1
ON1
TON
REF
SKIP#
VCC
VDD
V+
GND
ILIM2
BST2
DH2
LX2
DL2
CS2
OUT2
FB2
ON2
PGOOD
OVP
U27
FDS6690DS-GP
U29
FDS6690DS-GP
Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm
TC8
C197
SE220U2D5VM-3GP
SCD1U25V3ZY-1GP
DY
Panasonic 220uF/2D5V
ESR=15m ohm
Iripple=2.7 A
TC7
SE220U2VDM-8GP
C194
Panasonic 220uF/2V
ESR=15m ohm
Iripple=2.7 A
MAX8743_VREF
C434
SCD47U10V3KX-3GP
C435
SCD1U25V3ZY-1GP
R180
8K2R3F-GP
R181
10KR3F-L-GP
MAX8743_FB1
MAX8743_FB2
Voutsetting=1.820V
R156
5K11R2F-L1-GP
R162
10KR3F-L-GP
Voutsetting=1.511V
Vout=Vfb*(1+(R1/R2))
Where Vfb=1.0V,R2=10Kohm
R367
0R2J-2-GP
R366
DUMMY-R2
R368
DUMMY-R2
8/18
R360
5K1R2-GP
R361
5K1R2-GP
17,20,28,31,36,38 PM_SLP_S4#
20,22,27,28,31,34,38 PM_SLP_S3#
MAX8743_ON1
MAX8743_ON2
0830 SB
0205
R373
220KR2J-L2-GP
R364
220KR2J-L2-GP
MAX8743_SKIP#
C202
SC1000P50V3JN-GP
R169
0R2J-2-GP
R365
0R0402-PAD
CPUCORE_ON 35,36,38
MAX8743_PGOOD

Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	1D8V_S3/1D5V_S0	
Size A3	Document Number: Pamirs	Rev -3
Date: Monday, May 21, 2007	Sheet 37 of 41	



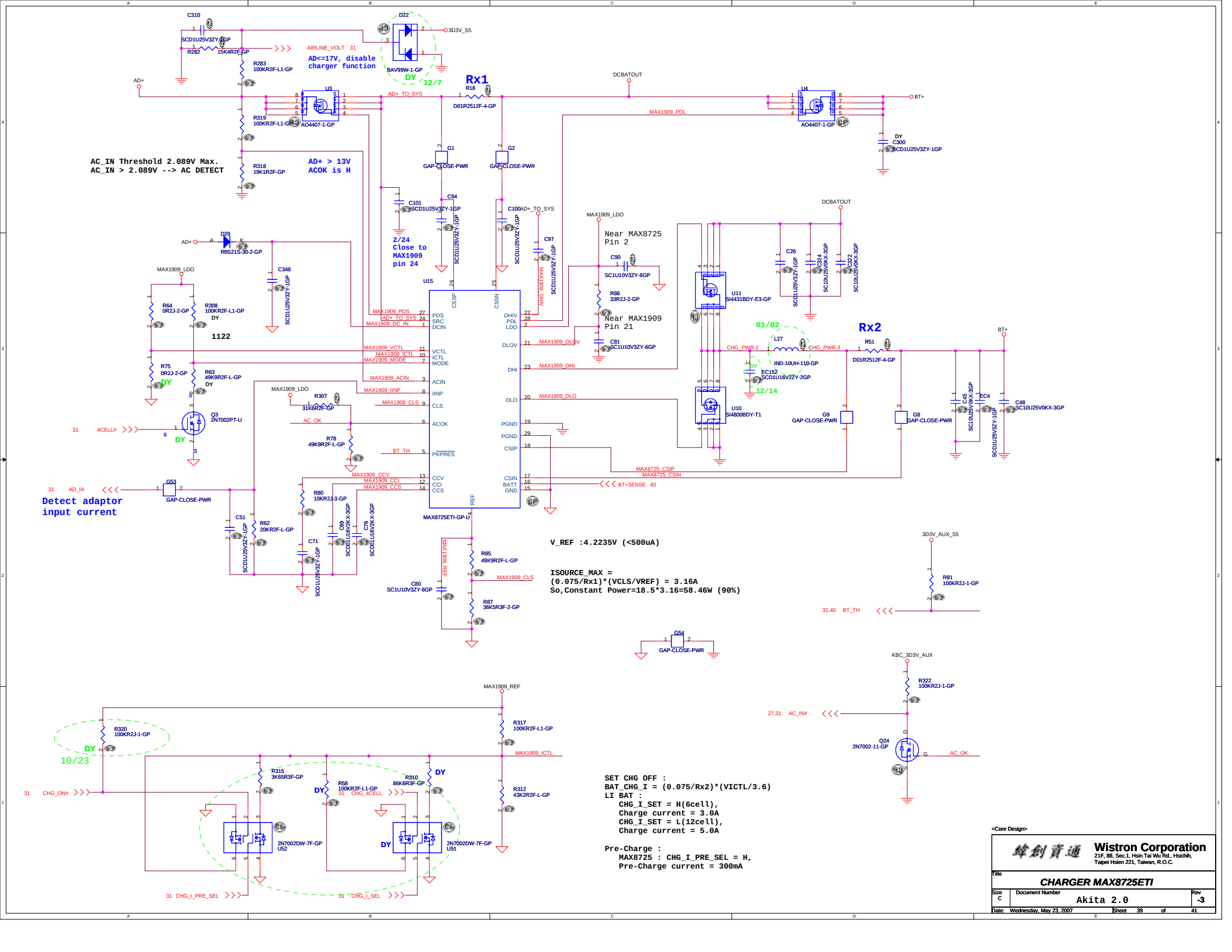
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

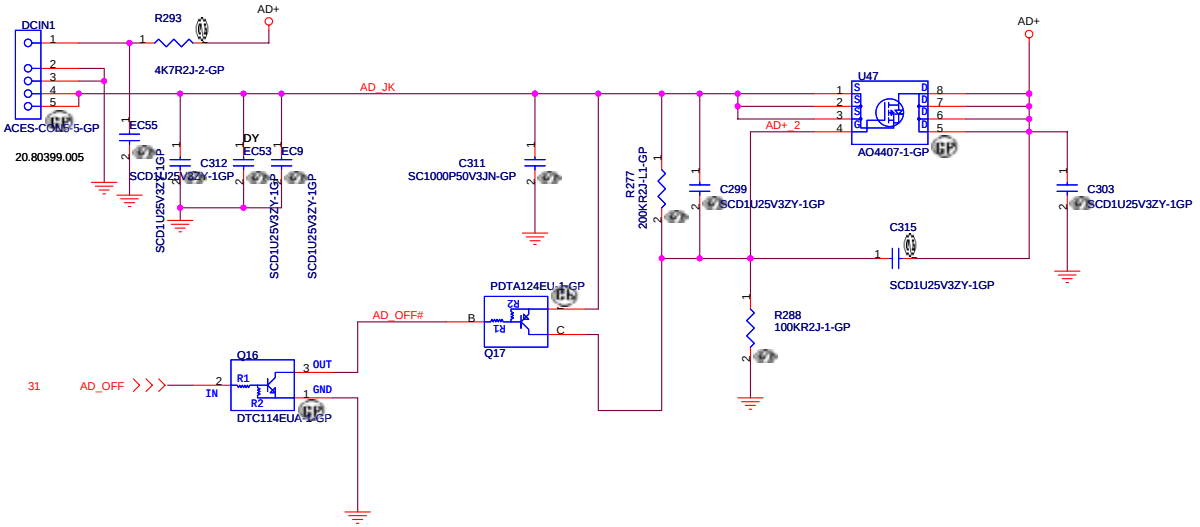
Title: 0D9V_LDO/1D25V_LDO/1D05V

Size	Document Number	Rev
A3	Pamirs	-3

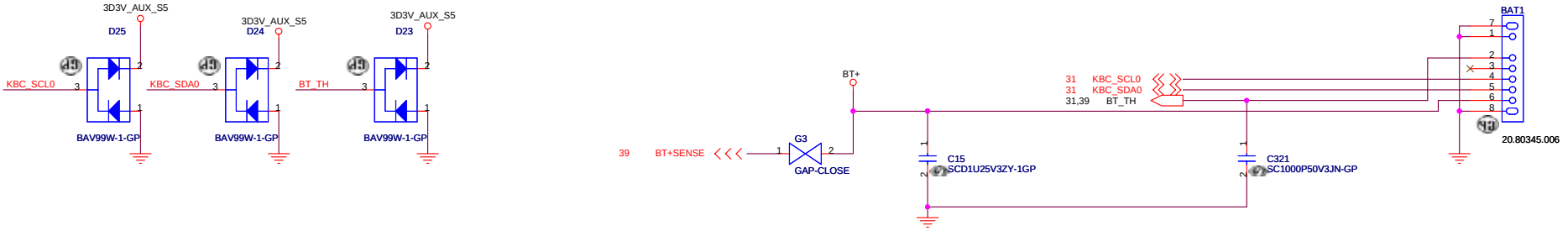
Date: Monday, May 21, 2007 Sheet 38 of 41


AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
AD+ > 13V
ACOK is H
AD<=17V, disable charger function
Rx1
Rx2
Near MAX8725 Pin 2
Near MAX1909 Pin 21
2/24 Close to MAX1909 pin 24
1122
01/02
12/14
12/7
10/23
Detect adaptor input current
V_REF :4.2235V (<500uA)
ISOURCE_MAX =
(0.075/Rx1)*(VCLS/VREF) = 3.16A
So,Constant Power=18.5*3.16=58.46W (90%)
SET CHG OFF :
BAT_CHG_I = (0.075/Rx2)*(VICTL/3.6)
LI BAT :
CHG_I_SET = H(6cell),
Charge current = 3.0A
CHG_I_SET = L(12cell),
Charge current = 5.0A
Pre-Charge :
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 300mA
MAX8725ETI-GP-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8725ETI
Akita 2.0
Wednesday, May 23, 2007

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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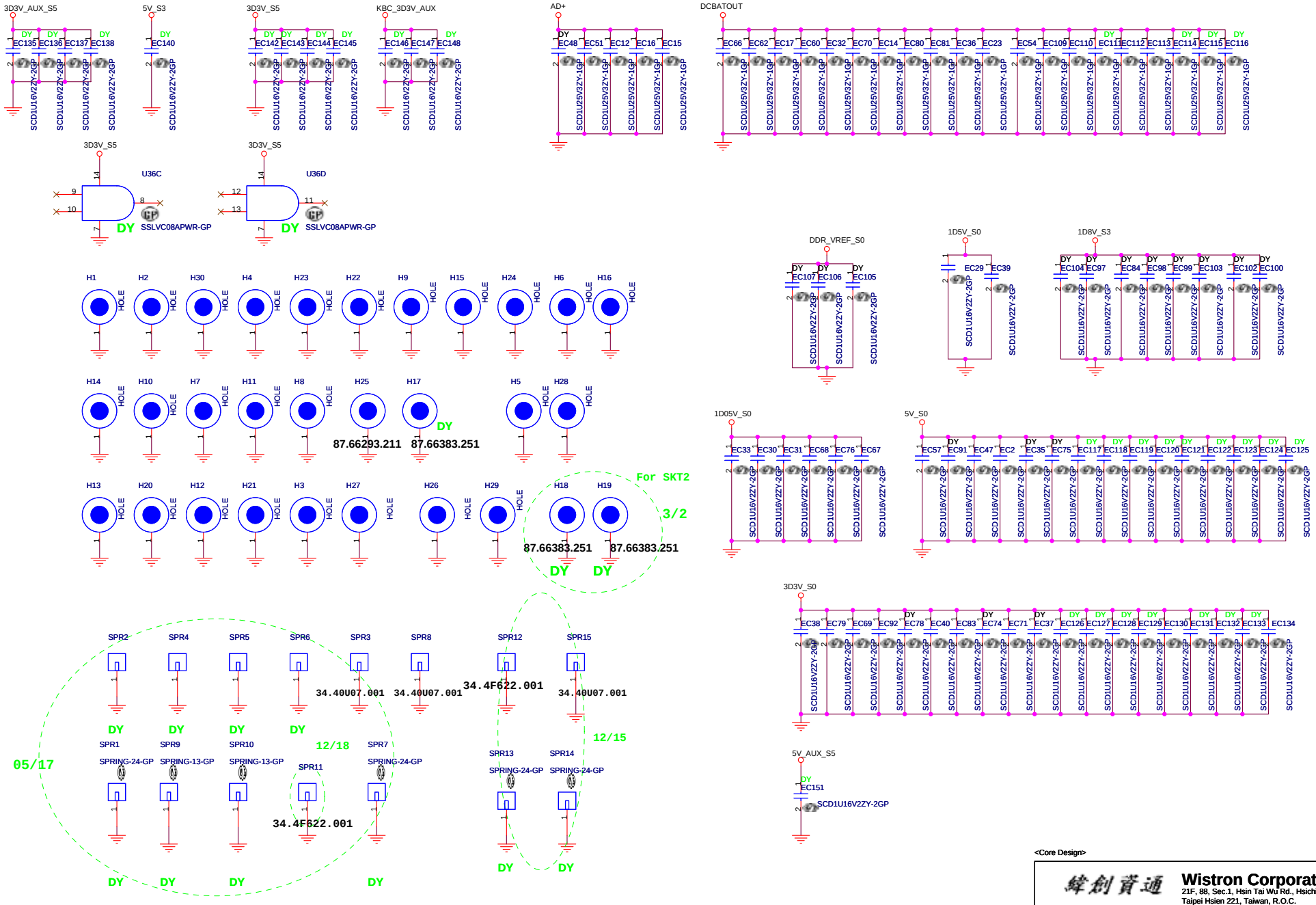

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Title: **MISC**

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