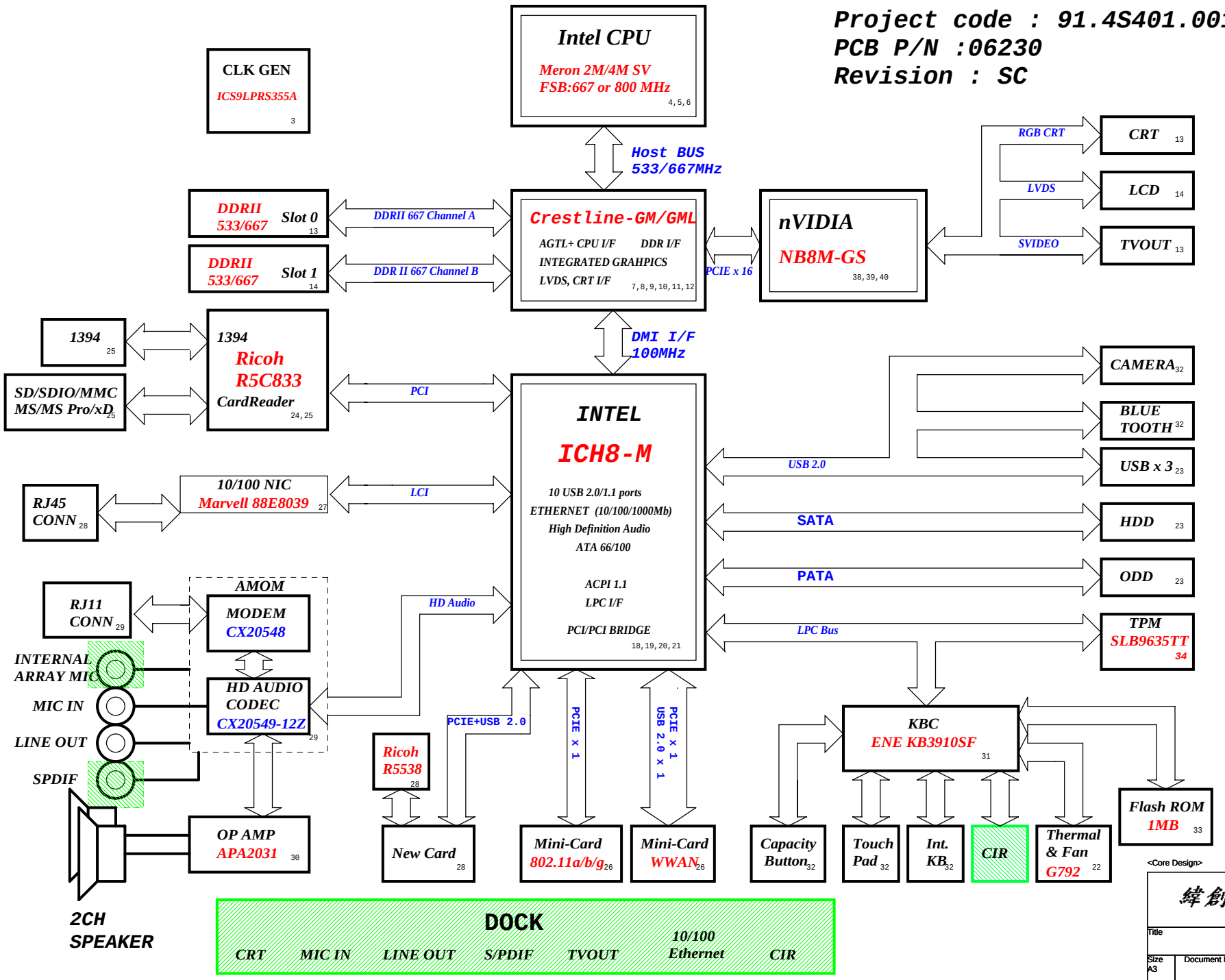
Pamirs-Discrete Block Diagram

Project code : 91.4S401.001
PCB P/N :06230
Revision : SC



SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

SYSTEM DC/DC FAN5234	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0 11A

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8736ETL	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: GND
L6: VCC
L7: Signal 4
L8: Signal 5
L9: GND
L10: Signal 5

<Core Design>

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Title: Block Diagram
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Date: Monday, December 18, 2006 | Sheet 1 of 47

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD/tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3: low = A16 swap override enable; high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN: High=Enable Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP: High=Enable Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR: LOW = Defaule; High=No Reboot

8.2K PULL HIGH

19,21 +RTCVCC → +RTCVCC
4,5,6,7,9,10,11,19,21,37,47 1D05V_S0 → 1D05V_S0
3,7,10,21,38 1D25V_S0 → 1D25V_S0
27 1D2V_LAN_S5 → 1D2V_LAN_S5
28 1D5V_NEW_S0 → 1D5V_NEW_S0
5,10,17,19,20,21,26,28,38,47 1D5V_S0 → 1D5V_S0
7,10,11,13,14,34,37,38 1D8V_S3 → 1D8V_S3
27,28 2D5V_LAN_S5 → 2D5V_LAN_S5
29,30 3D3V_AUD_S0 → 3D3V_AUD_S0
19,31,32,33,36,39,46 3D3V_AUX_S5 → 3D3V_AUX_S5
27,28 3D3V_LAN_S5 → 3D3V_LAN_S5
3,4,7,10,11,13,14,15,16,18,19,20,21,22,23,24,25,26,27,28,29,31,32,33,34,35,36,40,41,42,43,47 3D3V_S0 → 3D3V_S0
17,18,20,21,22,26,27,28,29,31,34,36,39,47 3D3V_S5 → 3D3V_S5
22,26,29,31,34,36 5V_AUX_S5 → 5V_AUX_S5
16,23,32,33,34,36,37,38 5V_S3 → 5V_S3
15,16,17,20,21,22,23,29,30,31,32,33,34,35,47 5V_S0 → 5V_S0
16,21,34,37,40 5V_S5 → 5V_S5
17,39,46,47 AD+ → AD+
16,17,34,35,36,37,39,40,47 DCBATOUT → DCBATOUT
13,14,38 DDR_VREF_S0 → DDR_VREF_S0
7,13,14,38 DDR_VREF_S3 → DDR_VREF_S3
22,31,33,39 KBC_3D3V_AUX → KBC_3D3V_AUX
16 LCDVDD_S0 → LCDVDD_S0
5,6,35 VCC_CORE_S0 → VCC_CORE_S0

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes★ number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reversed	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

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Title: Table of Content

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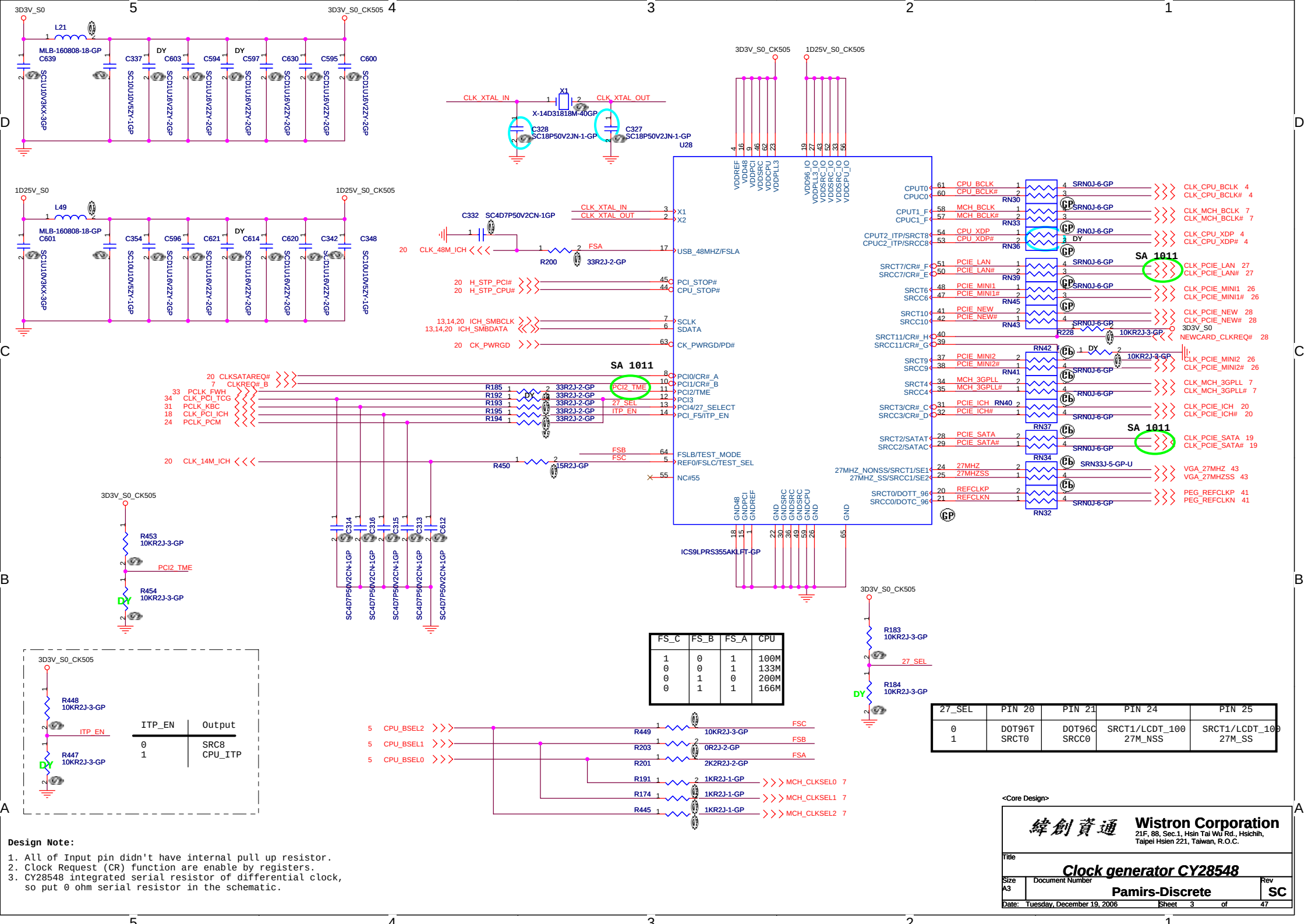
3D3V_S0
3D3V_S0_CK505
1D25V_S0
1D25V_S0_CK505
L21
L49
MLB-160808-18-GP
C639
C601
C337
C603
C594
C597
C630
C595
C600
C354
C596
C621
C614
C620
C342
C348
DY
SC1U10V3KX-3GP
SC10U10V5ZY-1GP
SC1U16V2ZY-2GP
SC10U10V5ZY-1GP
X1
X-14D31818M-40GP
C328
C327
SC18P50V2JN-1-GP
U28
CLK_XTAL_IN
CLK_XTAL_OUT
C332
SC4D7P50V2CN-1GP
CLK_48M_ICH
R200
33R2J-2-GP
FSA
USB_48MHZ/FSLA
H_STP_PCI#
H_STP_CPU#
PCI_STOP#
CPU_STOP#
ICH_SMBCLK
ICH_SMBDATA
SCLK
SDATA
CK_PWRGD
CK_PWRGD/PD#
SA 1011
CLKSATAREQ#
CLKREQ#_B
PCLK_FWH
CLK_PCI_TCG
PCLK_KBC
CLK_PCI_ICH
PCLK_PCM
R185
R192
R193
R195
R194
33R2J-2-GP
PCI2_TME
27_SEL
ITP_EN
PCI0/CR#_A
PCI1/CR#_B
PCI2/TME
PCI3
PCI4/27_SELECT
PCI_F5/ITP_EN
CLK_14M_ICH
R450
15R2J-GP
FSB
FSC
FSLB/TEST_MODE
REF0/FSLC/TEST_SEL
NC#55
ICS9LPRS355AKLFT-GP
R453
10KR2J-3-GP
R454
10KR2J-3-GP
R448
10KR2J-3-GP
R447
10KR2J-3-GP
ITP_EN
R449
R203
R201
R191
R174
R445
10KR2J-3-GP
0R2J-2-GP
2K2R2J-2-GP
1KR2J-1-GP
CPU_BSEL2
CPU_BSEL1
CPU_BSEL0
MCH_CLKSEL0
MCH_CLKSEL1
MCH_CLKSEL2
R183
R184
10KR2J-3-GP
CPU_BCLK
CPU_BCLK#
MCH_BCLK
MCH_BCLK#
CPU_XDP
CPU_XDP#
PCIE_LAN
PCIE_LAN#
PCIE_MINI1
PCIE_MINI1#
PCIE_NEW
PCIE_NEW#
PCIE_MINI2
PCIE_MINI2#
MCH_3GPLL
MCH_3GPLL#
PCIE_ICH
PCIE_ICH#
PCIE_SATA
PCIE_SATA#
27MHZ
27MHZSS
REFCLKP
REFCLKN
SRN0J-6-GP
SRN33J-5-GP-U
RN30
RN33
RN36
RN39
RN45
RN43
RN42
RN41
RN40
RN37
RN34
RN32
R228
10KR2J-3-GP
NEWCARD_CLKREQ#
CLK_CPU_BCLK
CLK_CPU_BCLK#
CLK_MCH_BCLK
CLK_MCH_BCLK#
CLK_CPU_XDP
CLK_CPU_XDP#
CLK_PCIE_LAN
CLK_PCIE_LAN#
CLK_PCIE_MINI1
CLK_PCIE_MINI1#
CLK_PCIE_NEW
CLK_PCIE_NEW#
CLK_PCIE_MINI2
CLK_PCIE_MINI2#
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
CLK_PCIE_ICH
CLK_PCIE_ICH#
CLK_PCIE_SATA
CLK_PCIE_SATA#
VGA_27MHZ
VGA_27MHZSS
PEG_REFCLKP
PEG_REFCLKN
ITP_EN
Output
0
1
SRC8
CPU_ITP
FS_C
FS_B
FS_A
CPU
100M
133M
200M
166M
27_SEL
PIN 20
PIN 21
PIN 24
PIN 25
DOT96T
SRCT0
DOT96C
SRCC0
SRCT1/LCDT_100
27M_NSS
SRCT1/LCDT_100
27M_SS
Design Note:
1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock,
so put 0 ohm serial resistor in the schematic.
<Core Design>
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Title
Clock generator CY28548
Size
A3
Document Number
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Date: Tuesday, December 19, 2006
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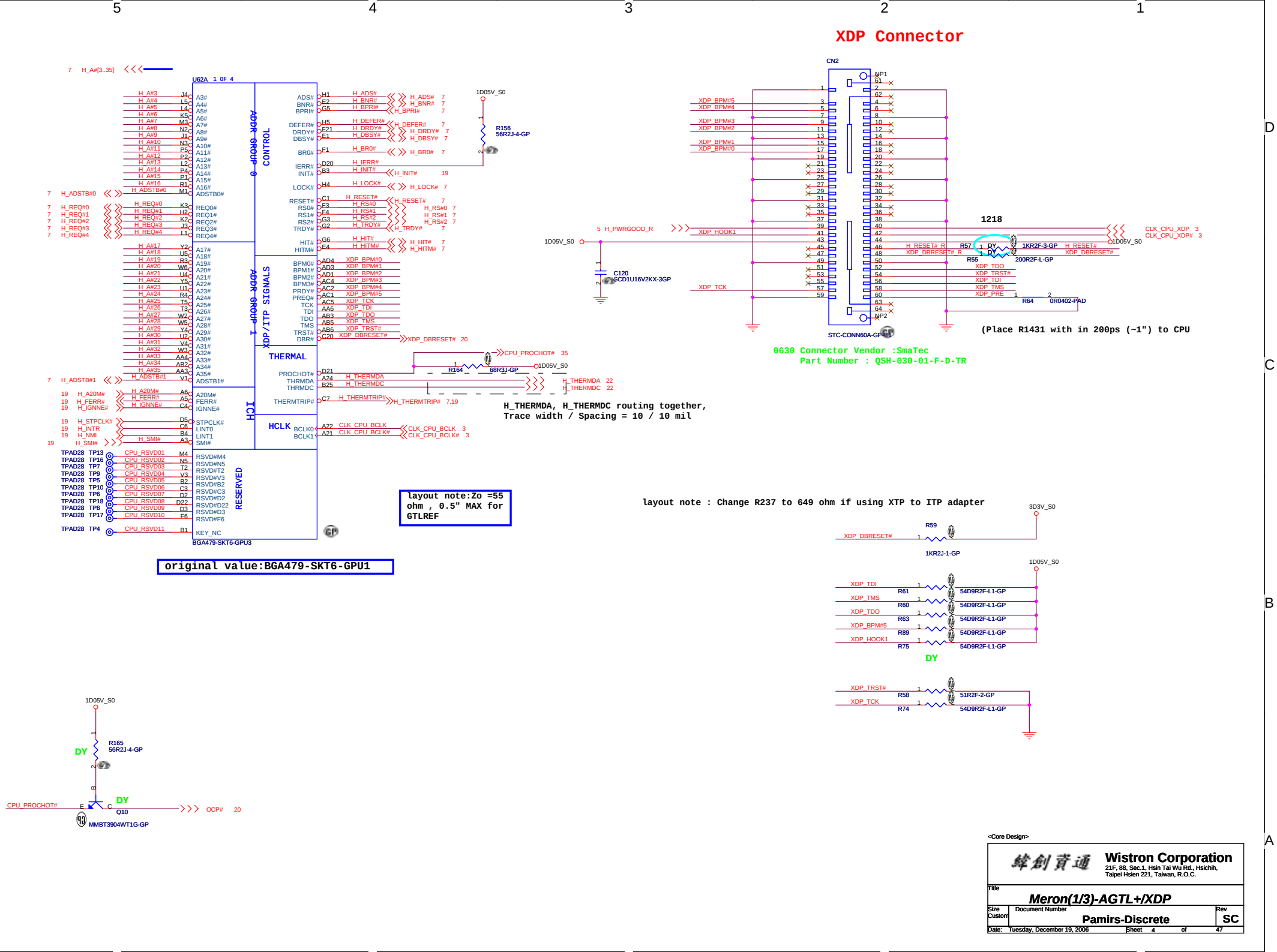
XDP Connector
U62A 1 OF 4
ADDR GROUP 0
CONTROL
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
ICH
HCLK
RESERVED
BGA479-SKT6-GPU3
original value:BGA479-SKT6-GPU1
CN2
STC-CONN60A-GP
0630 Connector Vendor :SmaTec
Part Number : QSH-030-01-F-D-TR
1218
(Place R1431 with in 200ps (~1") to CPU
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil
layout note:Zo =55 ohm , 0.5" MAX for GTLREF
layout note : Change R237 to 649 ohm if using XTP to ITP adapter
MMBT3904WT1G-GP
DY
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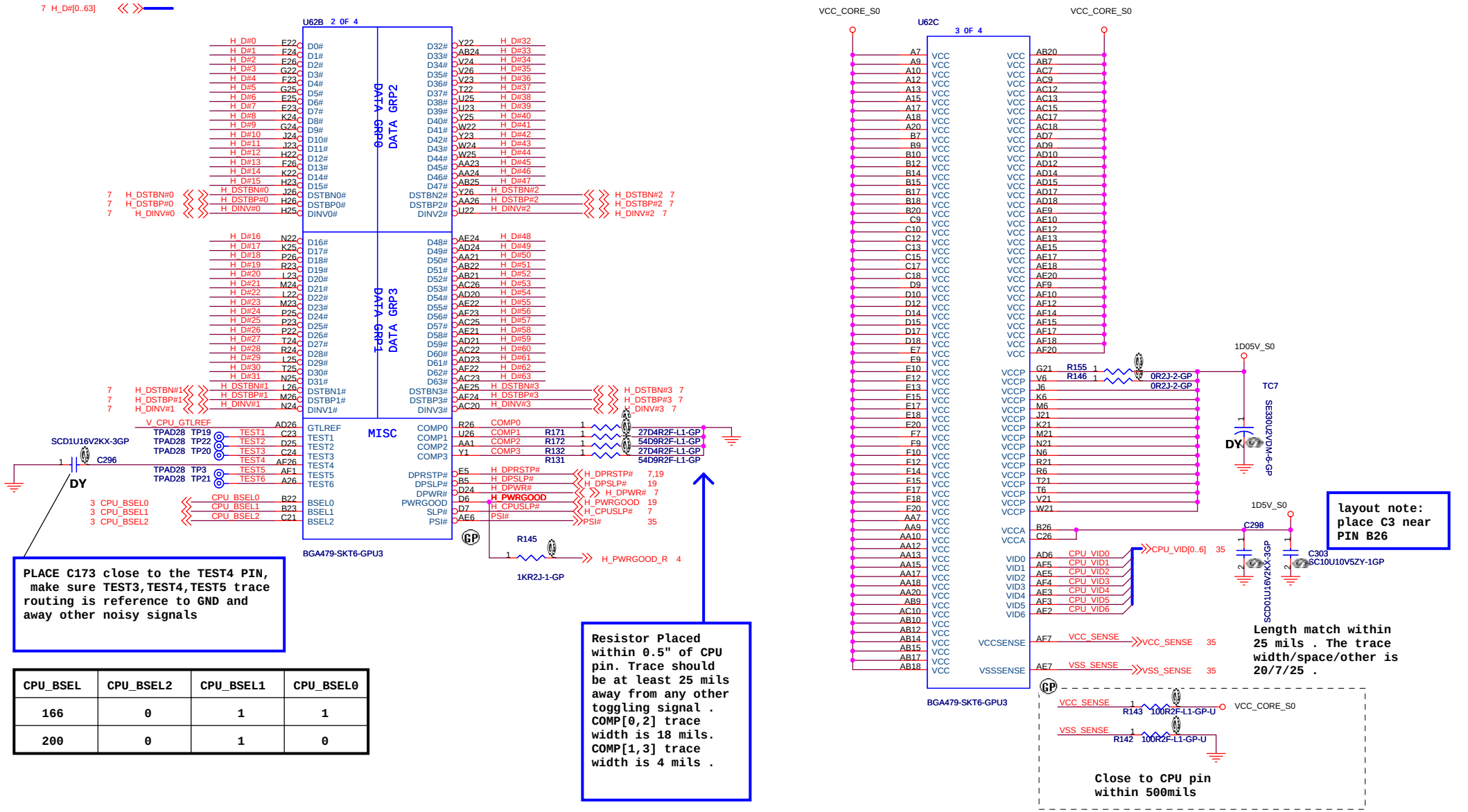
Meron(1/3)-AGTL+/XDP
Pamirs-Discrete
Tuesday, December 19, 2006



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Title: Meron(2/3)-AGTL+/PWR

Size: A3 | Document Number: Pamirs-Discrete | Rev: SC

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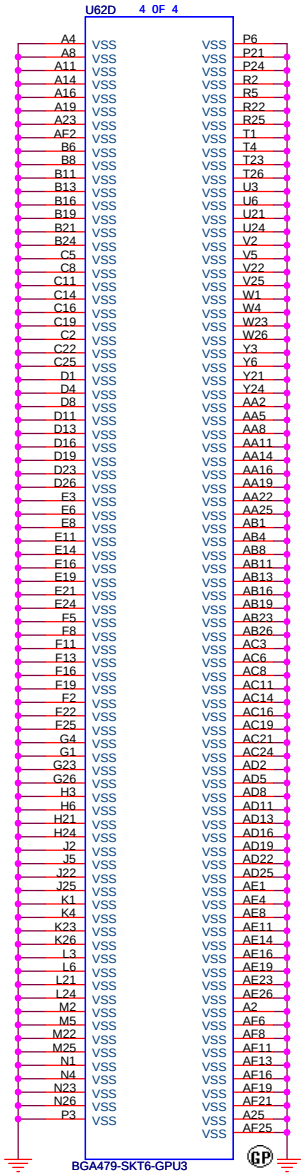
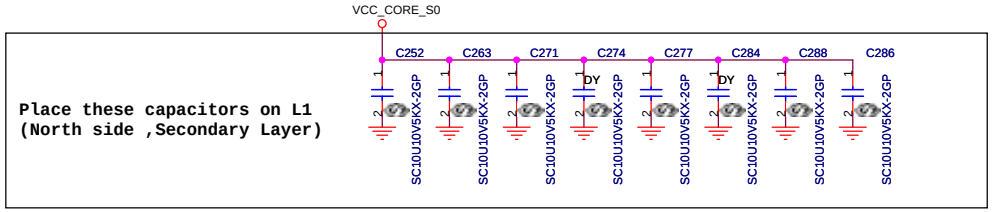
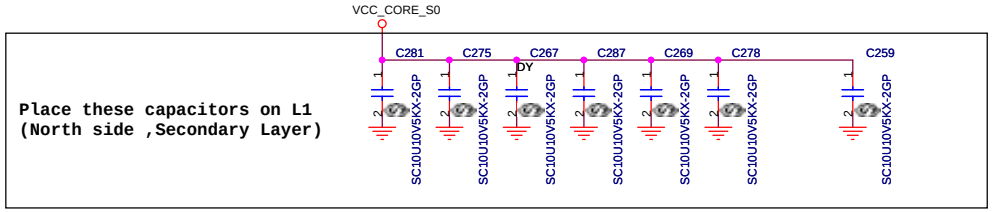
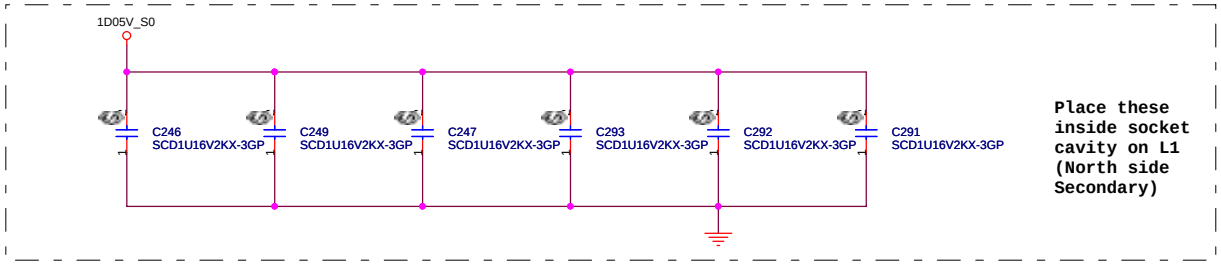






Mid Frequencd Decoupling



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Title: Meron(3/3)-GND&Bypass

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FOR Calero: 80.6 ohm
Crestline: 20 ohm

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

From Astro demo schematic

layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

Layout Note :
Place C151 within 100 mils of NB

Layout Note :
Place C153 near pin B3 of NB

SA 0928

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Title: CRESTLINE(1/6)-AGTL+/DMI/DDR2

Size: Custom | Document Number: Pamirs-Discrete | Rev: SA

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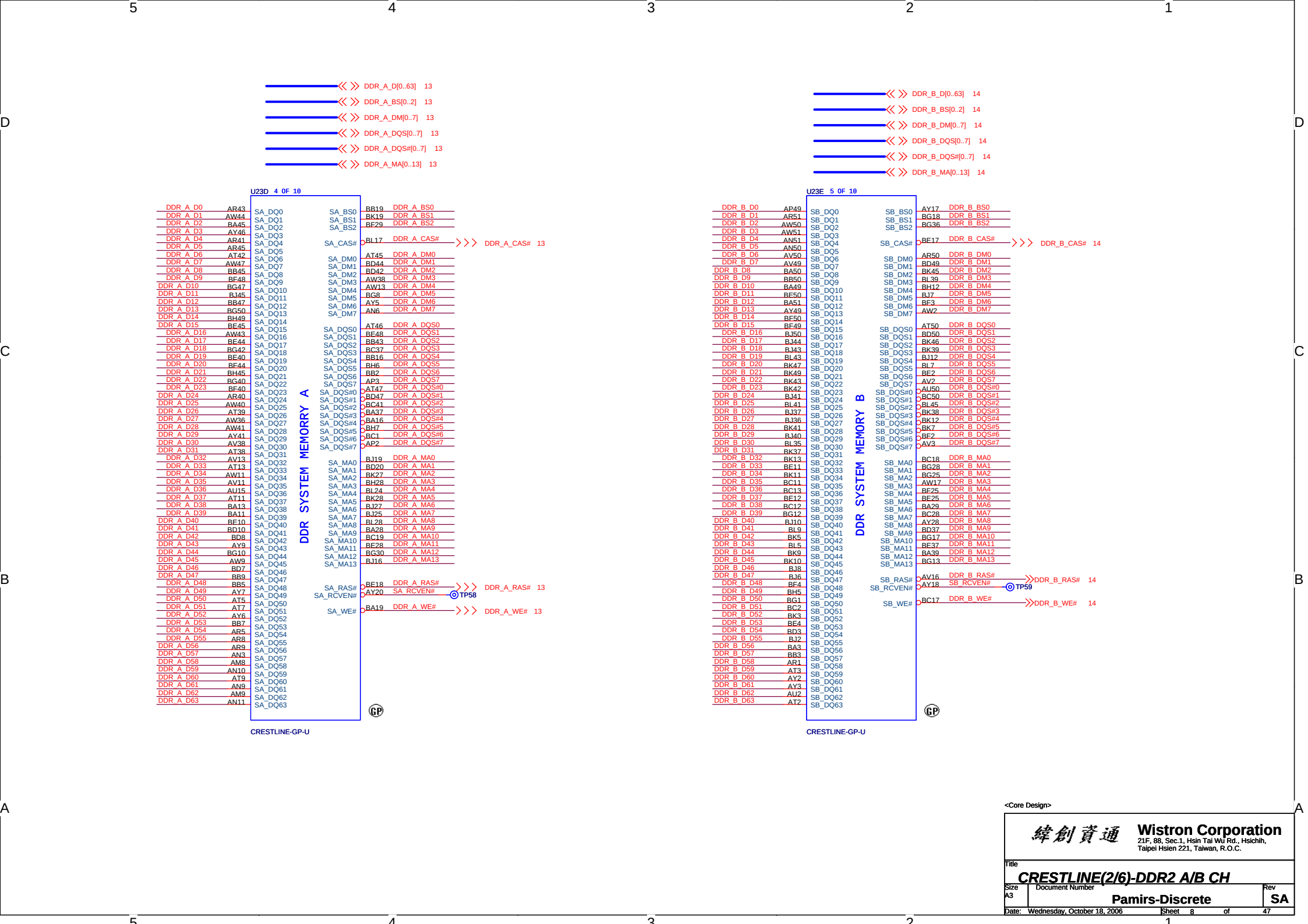

<Core Design>

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Title: CRESTLINE(2/6)-DDR2 A/B CH

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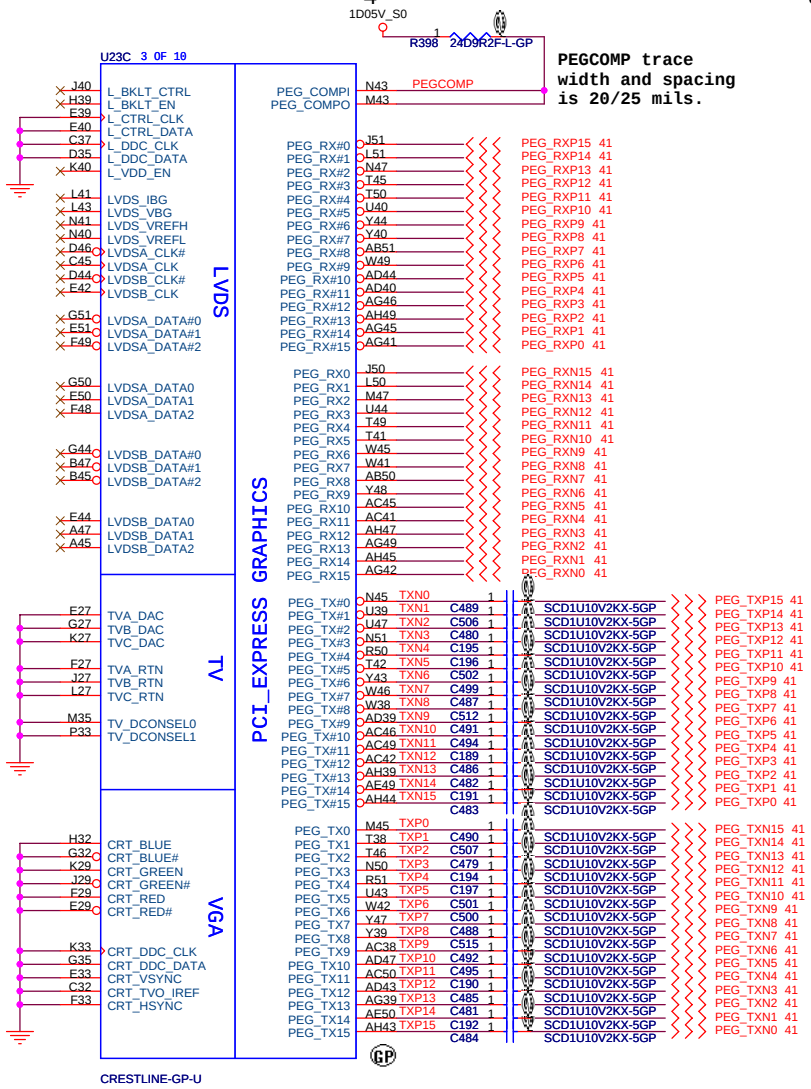

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

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Title: CRESTLINE(3/6)-VGA/LVDS/TV

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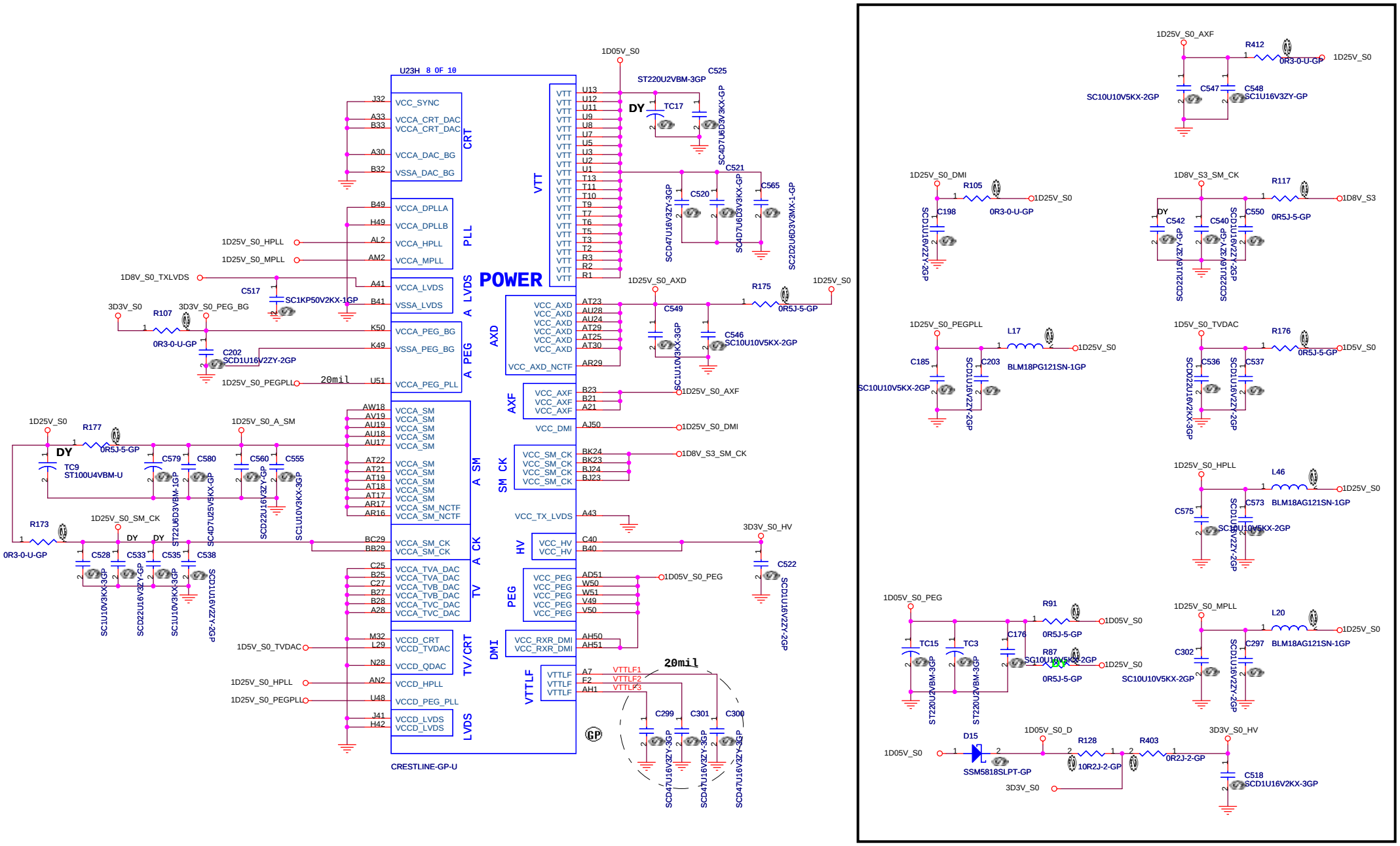

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Title: CRESTLINE(4/6)-PWR

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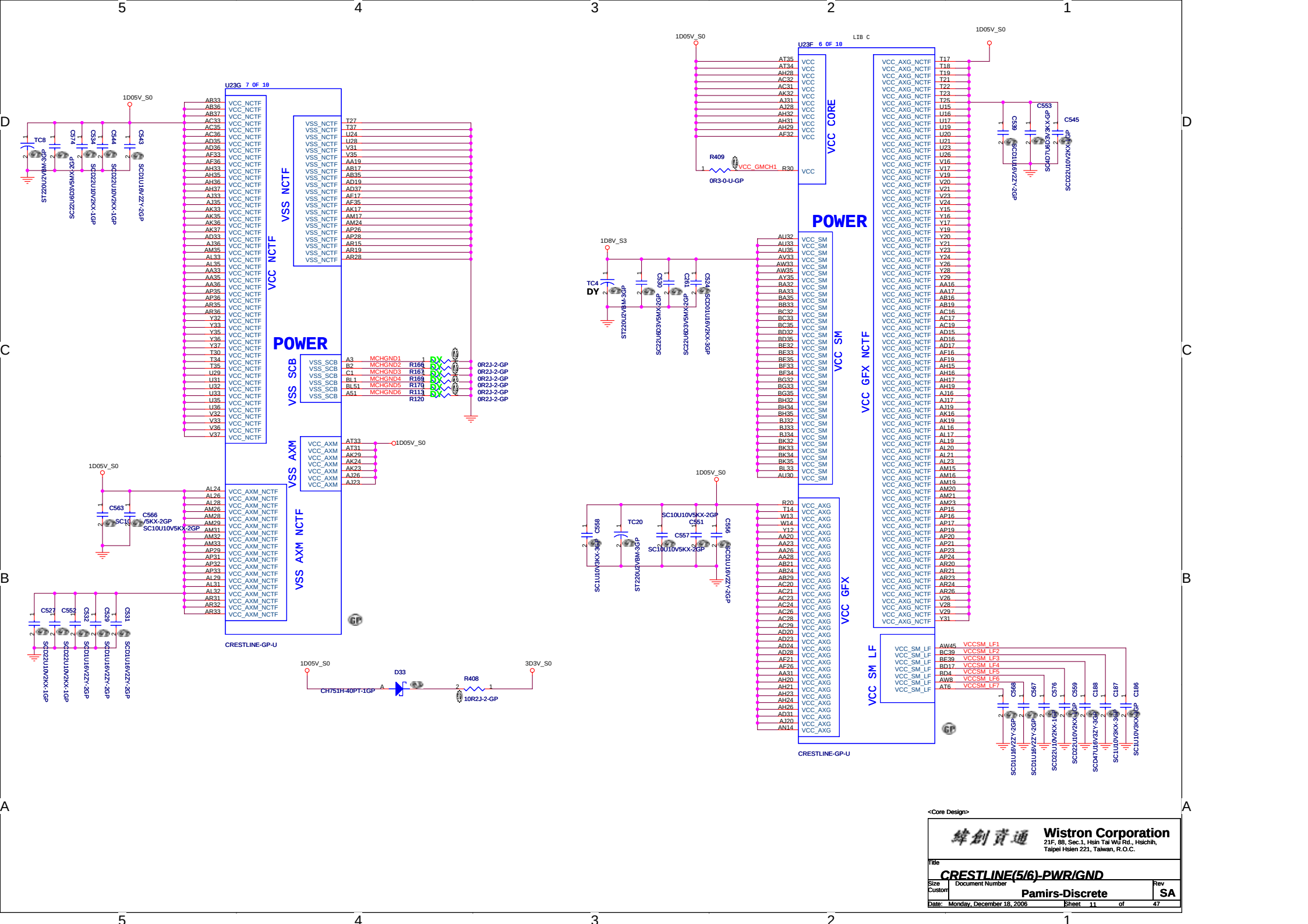
U23G 7 OF 10
U23F 6 OF 10
LIB C
POWER
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
VCC NCTF
VSS NCTF
VSS SCB
VSS AXM
VSS AXM NCTF
1D05V_S0
1D8V_S3
3D3V_S0
R409
0R3-0-U-GP
VCC_GMCH1
D33
CH751H-40PT-1GP
R408
10R2J-2-GP
CRESTLINE-GP-U
<Core Design>
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
CRESTLINE(5/6)-PWR/GND
Size
Custom
Document Number
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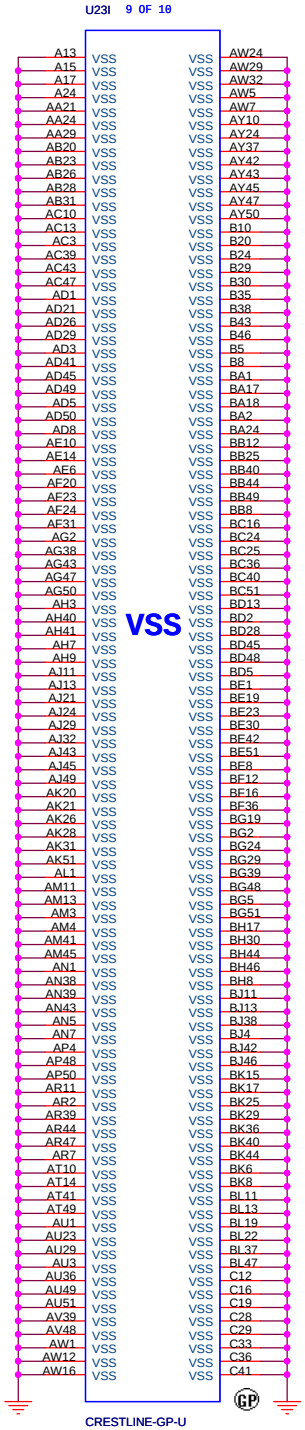

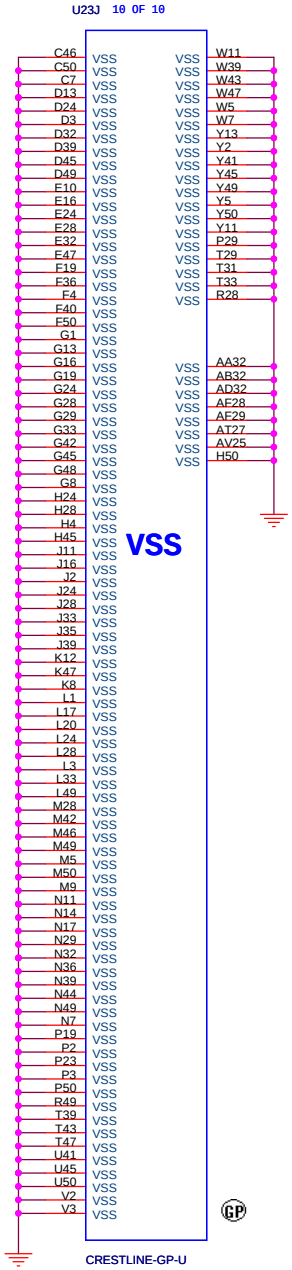

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Title: CRESTLINE(6/6)-PWR/GND

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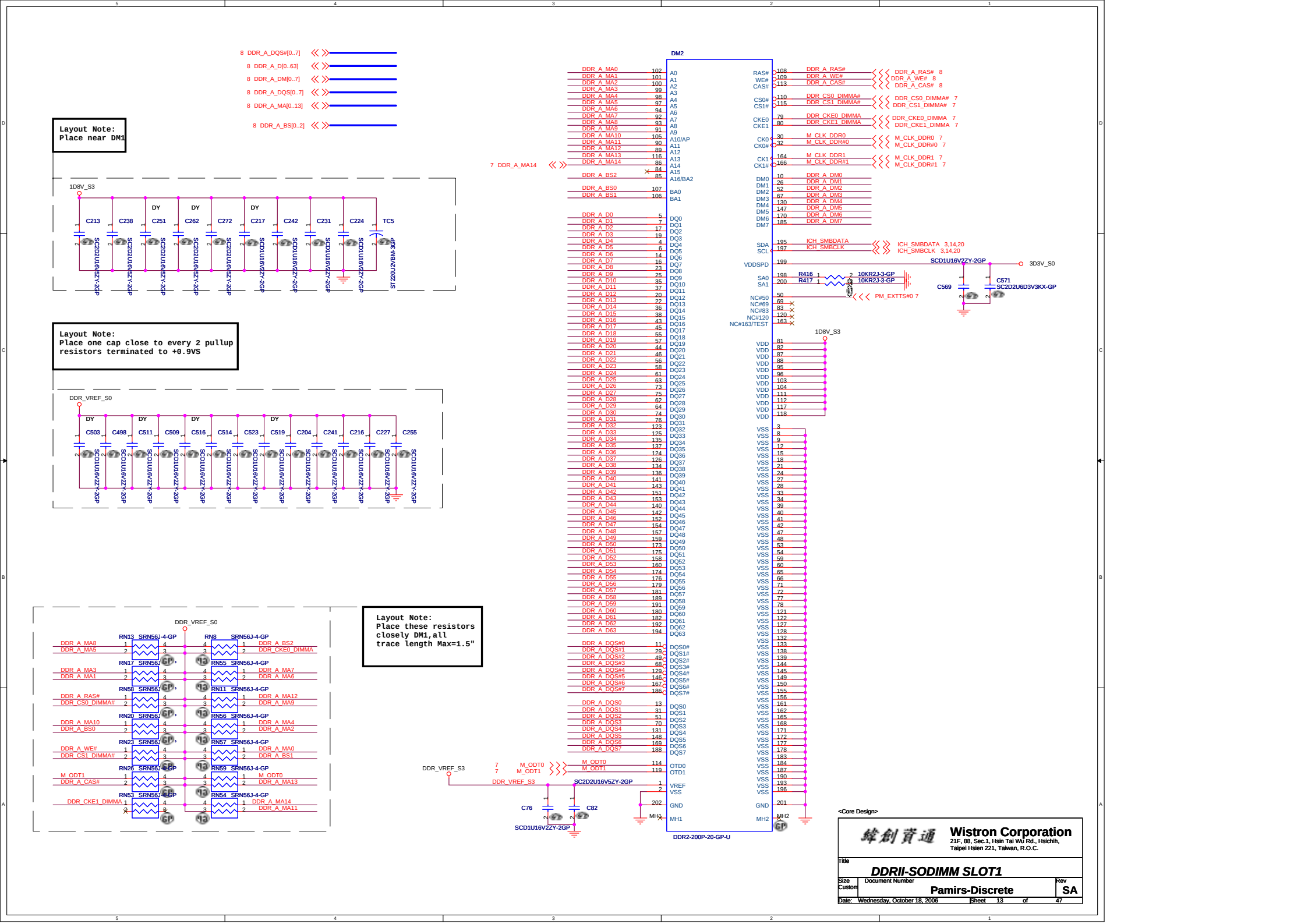
8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..13]
8 DDR_A_BS[0..2]
Layout Note:
Place near DM1
1D8V_S3
C213
C238
C251
C262
C272
C217
C242
C231
C224
TC5
DY
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C503
C498
C511
C509
C516
C514
C523
C519
C204
C241
C216
C227
C255
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
RN13 SRN56J-4-GP
RN8 SRN56J-4-GP
RN17 SRN56J-4-GP
RN55 SRN56J-4-GP
RN58 SRN56J-4-GP
RN11 SRN56J-4-GP
RN20 SRN56J-4-GP
RN56 SRN56J-4-GP
RN23 SRN56J-4-GP
RN57 SRN56J-4-GP
RN26 SRN56J-4-GP
RN59 SRN56J-4-GP
RN53 SRN56J-4-GP
RN54 SRN56J-4-GP
DDR_A_MA8
DDR_A_MA5
DDR_A_MA3
DDR_A_MA1
DDR_A_RAS#
DDR_CS0_DIMMA#
DDR_A_MA10
DDR_A_BS0
DDR_A_WE#
DDR_CS1_DIMMA#
M_ODT1
DDR_A_CAS#
DDR_CKE1_DIMMA
DDR_A_BS2
DDR_CKE0_DIMMA
DDR_A_MA7
DDR_A_MA6
DDR_A_MA12
DDR_A_MA9
DDR_A_MA4
DDR_A_MA2
DDR_A_MA0
DDR_A_BS1
M_ODT0
DDR_A_MA13
DDR_A_MA14
DDR_A_MA11
DM2
DDR_A_MA0
DDR_A_MA1
DDR_A_MA2
DDR_A_MA3
DDR_A_MA4
DDR_A_MA5
DDR_A_MA6
DDR_A_MA7
DDR_A_MA8
DDR_A_MA9
DDR_A_MA10
DDR_A_MA11
DDR_A_MA12
DDR_A_MA13
DDR_A_MA14
DDR_A_BS2
DDR_A_BS0
DDR_A_BS1
DDR_A_D0
DDR_A_D1
DDR_A_D2
DDR_A_D3
DDR_A_D4
DDR_A_D5
DDR_A_D6
DDR_A_D7
DDR_A_D8
DDR_A_D9
DDR_A_D10
DDR_A_D11
DDR_A_D12
DDR_A_D13
DDR_A_D14
DDR_A_D15
DDR_A_D16
DDR_A_D17
DDR_A_D18
DDR_A_D19
DDR_A_D20
DDR_A_D21
DDR_A_D22
DDR_A_D23
DDR_A_D24
DDR_A_D25
DDR_A_D26
DDR_A_D27
DDR_A_D28
DDR_A_D29
DDR_A_D30
DDR_A_D31
DDR_A_D32
DDR_A_D33
DDR_A_D34
DDR_A_D35
DDR_A_D36
DDR_A_D37
DDR_A_D38
DDR_A_D39
DDR_A_D40
DDR_A_D41
DDR_A_D42
DDR_A_D43
DDR_A_D44
DDR_A_D45
DDR_A_D46
DDR_A_D47
DDR_A_D48
DDR_A_D49
DDR_A_D50
DDR_A_D51
DDR_A_D52
DDR_A_D53
DDR_A_D54
DDR_A_D55
DDR_A_D56
DDR_A_D57
DDR_A_D58
DDR_A_D59
DDR_A_D60
DDR_A_D61
DDR_A_D62
DDR_A_D63
DDR_A_DQS#0
DDR_A_DQS#1
DDR_A_DQS#2
DDR_A_DQS#3
DDR_A_DQS#4
DDR_A_DQS#5
DDR_A_DQS#6
DDR_A_DQS#7
DDR_A_DQS0
DDR_A_DQS1
DDR_A_DQS2
DDR_A_DQS3
DDR_A_DQS4
DDR_A_DQS5
DDR_A_DQS6
DDR_A_DQS7
M_ODT0
M_ODT1
DDR_VREF_S3
SC2D2U16V5ZY-2GP
C76
C82
SCD1U16V2ZY-2GP
DDR2-200P-20-GP-U
RAS#
WE#
CAS#
CS0#
CS1#
CKE0
CKE1
CK0
CK0#
CK1
CK1#
DDR_A_RAS#
DDR_A_WE#
DDR_A_CAS#
DDR_CS0_DIMMA#
DDR_CS1_DIMMA#
DDR_CKE0_DIMMA
DDR_CKE1_DIMMA
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
DDR_A_DM0
DDR_A_DM1
DDR_A_DM2
DDR_A_DM3
DDR_A_DM4
DDR_A_DM5
DDR_A_DM6
DDR_A_DM7
SDA
SCL
ICH_SMBDATA
ICH_SMBCLK
ICH_SMBDATA 3,14,20
ICH_SMBCLK 3,14,20
VDDSPD
SA0
SA1
R416
R417
10KR2J-3-GP
PM_EXTTS#0 7
C569
C571
SC2D2U6D3V3KX-GP
3D3V_S0
NC#50
NC#69
NC#83
NC#120
NC#163/TEST
VDD
VSS
GND
MH1
MH2
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT1
Size
Custom
Document Number
Pamirs-Discrete
Rev
SA
Date: Wednesday, October 18, 2006
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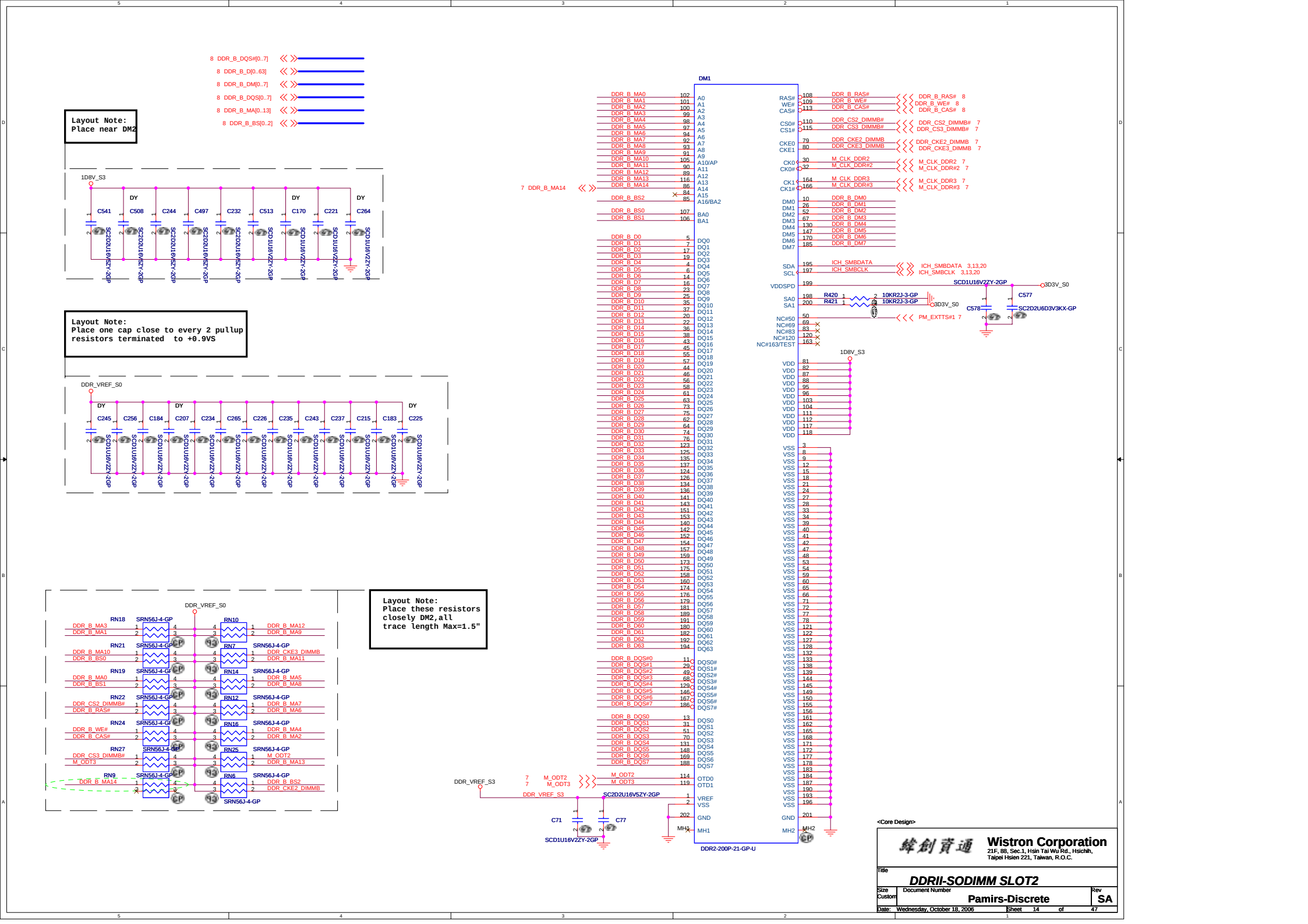
8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]
8 DDR_B_BS[0..2]
Layout Note:
Place near DM2
1D8V_S3
DY
C541 C508 C244 C497 C232 C513 C170 C221 C264
SCD2U16VZY-2GP
SCD1U16VZY-2GP
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C245 C256 C184 C207 C234 C265 C226 C235 C243 C237 C215 C183 C225
SCD1U16V2ZY-2GP
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
RN18 RN21 RN19 RN22 RN24 RN27 RN9 RN10 RN7 RN14 RN12 RN16 RN25 RN6
SRN56J-4-GP
DDR_B_MA3 DDR_B_MA1 DDR_B_MA10 DDR_B_BS0 DDR_B_MA0 DDR_B_BS1 DDR_CS2_DIMMB# DDR_B_RAS# DDR_B_WE# DDR_B_CAS# DDR_CS3_DIMMB# M_ODT3 DDR_B_MA14
DDR_B_MA12 DDR_B_MA9 DDR_CKE3_DIMMB DDR_B_MA11 DDR_B_MA5 DDR_B_MA8 DDR_B_MA7 DDR_B_MA6 DDR_B_MA4 DDR_B_MA2 M_ODT2 DDR_B_MA13 DDR_B_BS2 DDR_CKE2_DIMMB
DM1
DDR2-200P-21-GP-U
DDR_B_MA0 DDR_B_MA1 DDR_B_MA2 DDR_B_MA3 DDR_B_MA4 DDR_B_MA5 DDR_B_MA6 DDR_B_MA7 DDR_B_MA8 DDR_B_MA9 DDR_B_MA10 DDR_B_MA11 DDR_B_MA12 DDR_B_MA13 DDR_B_MA14 DDR_B_BS2 DDR_B_BS0 DDR_B_BS1
DDR_B_D0 DDR_B_D1 DDR_B_D2 DDR_B_D3 DDR_B_D4 DDR_B_D5 DDR_B_D6 DDR_B_D7 DDR_B_D8 DDR_B_D9 DDR_B_D10 DDR_B_D11 DDR_B_D12 DDR_B_D13 DDR_B_D14 DDR_B_D15 DDR_B_D16 DDR_B_D17 DDR_B_D18 DDR_B_D19 DDR_B_D20 DDR_B_D21 DDR_B_D22 DDR_B_D23 DDR_B_D24 DDR_B_D25 DDR_B_D26 DDR_B_D27 DDR_B_D28 DDR_B_D29 DDR_B_D30 DDR_B_D31 DDR_B_D32 DDR_B_D33 DDR_B_D34 DDR_B_D35 DDR_B_D36 DDR_B_D37 DDR_B_D38 DDR_B_D39 DDR_B_D40 DDR_B_D41 DDR_B_D42 DDR_B_D43 DDR_B_D44 DDR_B_D45 DDR_B_D46 DDR_B_D47 DDR_B_D48 DDR_B_D49 DDR_B_D50 DDR_B_D51 DDR_B_D52 DDR_B_D53 DDR_B_D54 DDR_B_D55 DDR_B_D56 DDR_B_D57 DDR_B_D58 DDR_B_D59 DDR_B_D60 DDR_B_D61 DDR_B_D62 DDR_B_D63
DDR_B_DQS#0 DDR_B_DQS#1 DDR_B_DQS#2 DDR_B_DQS#3 DDR_B_DQS#4 DDR_B_DQS#5 DDR_B_DQS#6 DDR_B_DQS#7
DDR_B_DQS0 DDR_B_DQS1 DDR_B_DQS2 DDR_B_DQS3 DDR_B_DQS4 DDR_B_DQS5 DDR_B_DQS6 DDR_B_DQS7
M_ODT2 M_ODT3
DDR_VREF_S3
SC2D2U16V5ZY-2GP
C71 C77
SCD1U16V2ZY-2GP
RAS# WE# CAS#
CS0# CS1#
CKE0 CKE1
CK0 CK0#
CK1 CK1#
DDR_B_RAS# DDR_B_WE# DDR_B_CAS#
DDR_CS2_DIMMB# DDR_CS3_DIMMB#
DDR_CKE2_DIMMB DDR_CKE3_DIMMB
M_CLK_DDR2 M_CLK_DDR#2
M_CLK_DDR3 M_CLK_DDR#3
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
DDR_B_DM0 DDR_B_DM1 DDR_B_DM2 DDR_B_DM3 DDR_B_DM4 DDR_B_DM5 DDR_B_DM6 DDR_B_DM7
SDA SCL
ICH_SMBDATA ICH_SMBCLK
ICH_SMBDATA 3,13,20
ICH_SMBCLK 3,13,20
VDDSPD
SA0 SA1
R420 R421
10KR2J-3-GP
3D3V_S0
SCD1U16V2ZY-2GP
C577 C578
SC2D2U6D3V3KX-GP
PM_EXTTS#1 7
NC#50 NC#69 NC#83 NC#120 NC#163/TEST
1D8V_S3
VDD
VSS
GND
MH1 MH2
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT2
Size Custom
Document Number
Pamirs-Discrete
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SA
Date: Wednesday, October 18, 2006
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CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

42 VGA_RED
42 VGA_GREEN
42 VGA_BLUE

L8 BLM18BB470SN1-GP
L2 BLM18BB470SN1-GP
L1 BLM18BB470SN1-GP

R23 150R2F-1-GP
R20 150R2F-1-GP
R19 150R2F-1-GP

C35 SC10P50V2JN-4GP
C29 SC10P50V2JN-4GP
C22 SC10P50V2JN-4GP
C32 SC10P50V2JN-4GP
C26 SC10P50V2JN-4GP
C21 SC10P50V2JN-4GP

CRT_R → CRT_R 17
CRT_G → CRT_G 17
CRT_B → CRT_B 17

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

5V_CRT_S0 → F1 FUSE-1D1A6V-8GP → 5V_S0
C13 SCD01U16V2KX-3GP
D4 CH751H-40PT-1GP
5V_CRT1_S0
RN1 SRN2K2J-1-GP

CRT1 20.20424.015
CRT_R, CRT_G, CRT_B
DDC_DATA_CON, DDC_CLK_CON
JVGA_HS, JVGA_VS

C15 SC33P50V2JN-3GP DY
C20 SC33P50V2JN-3GP DY
C11 SC22P50V2JN-4GP
C9 SC22P50V2JN-4GP

D11 BAV99W-1-GP
D12 BAV99W-1-GP
DDC_DATA_CON
DDC_CLK_CON

U3 PACDN009MR-GP-U
GMCH_HSYNC
GMCH_VSYNC
CRT_R
CRT_G
CRT_B

5V_S0
C464 SCD1U16V2ZY-2GP
PR_INSERT 17

17,42 GMCH_HSYNC → U6A TSAHCT125PW-GP → HSYNC_5
17,42 GMCH_VSYNC → U6B TSAHCT125PW-GP → VSYNC_5
RN4 SRN33J-5-GP-U → JVGA_HS, JVGA_VS

3D3V_S0
RN2 SRN2K2J-1-GP

U1 2N7002DW-1-GP
42 VGA_DDCDATA ↔ DDC_DATA_CON ↔ DDC_DATA_CON 17
17 DDC_CLK_CON ↔ DDC_CLK_CON ↔ VGA_DDCCLK 42

5V @ ext. CRT side

TV OUT CONN

connector

42 VGA_TV_CRMA → L32 BLM18BB470SN1-GP → TV_CRMA 17
R1 150R2F-1-GP
C432 SC10P50V2JN-4GP
C431 SC10P50V2JN-4GP

42 VGA_TV_COMP → L33 BLM18BB470SN1-GP → TV_COMP 17
R3 150R2F-1-GP
C434 SC10P50V2JN-4GP
C433 SC10P50V2JN-4GP

42 VGA_TV_LUMA → L34 BLM18BB470SN1-GP → TV_LUMA 17
R2 150R2F-1-GP
C438 SC10P50V2JN-4GP
C437 SC10P50V2JN-4GP

Place this 2 resistors close to the TV-out connector

TV1 MINDIN7-16-GP-U
TV_LUMA
TV_CRMA
TV_COMP
LUMA
CRMA
COMP
NC#2
NC#5
GND

D1 BAV99W-1-GP DY
VGA_TV_COMP
C1 SCD1U16V2ZY-2GP DY

D3 BAV99W-1-GP DY
VGA_TV_LUMA
C3 SCD1U16V2ZY-2GP DY

D2 BAV99W-1-GP DY
VGA_TV_CRMA
C2 SCD1U16V2ZY-2GP DY

3D3V_S0

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/TV Connector
Size: A3
Document Number: Pamirs-Discrete
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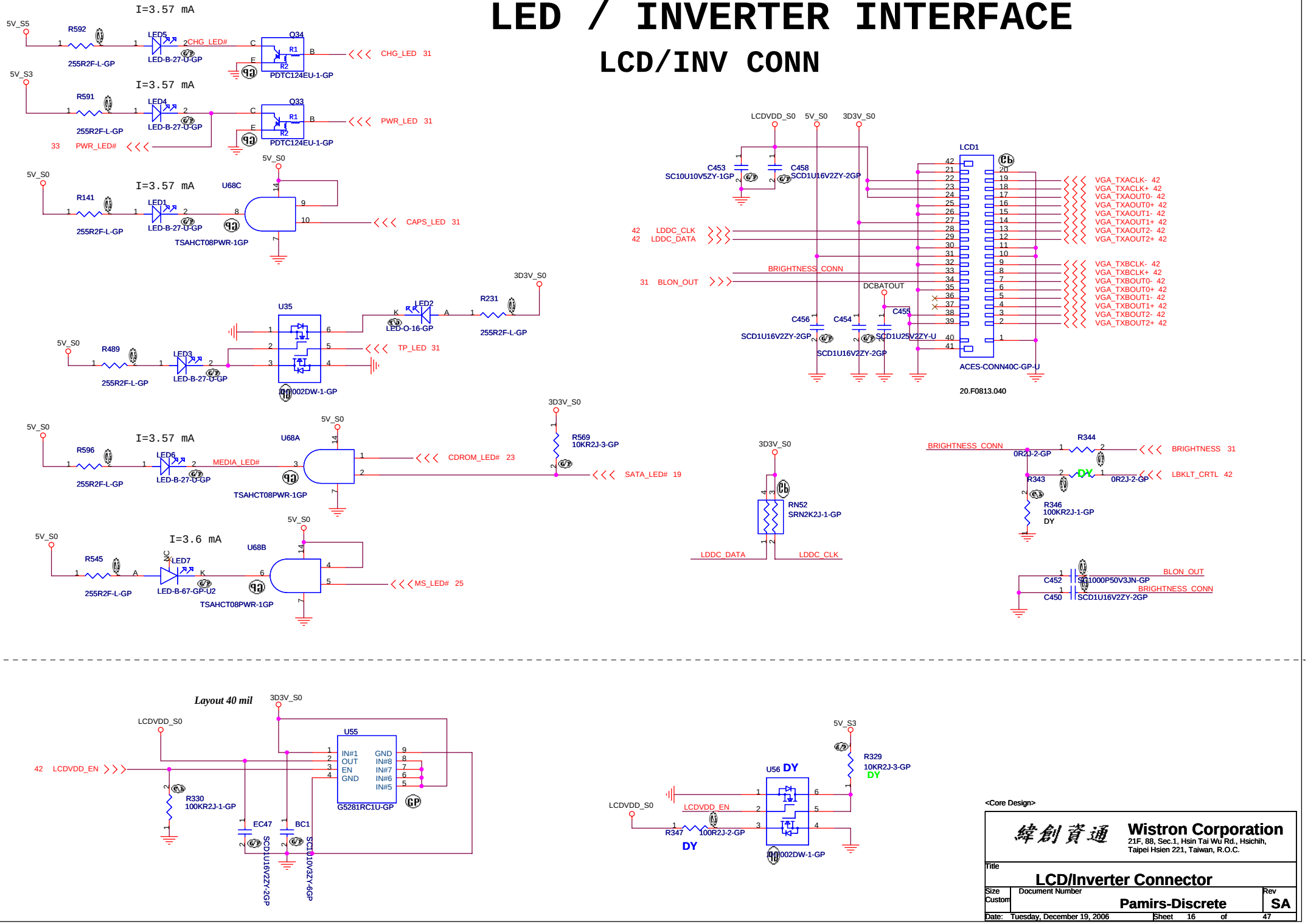
LED / INVERTER INTERFACE

LCD/INV CONN



<Core Design>

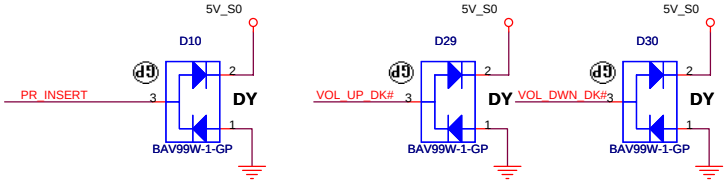
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

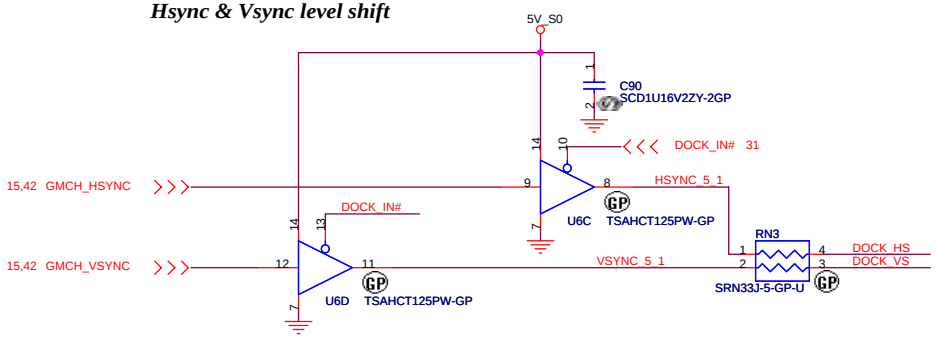
Size	Document Number	Rev
Custom	Pamirs-Discrete	SA

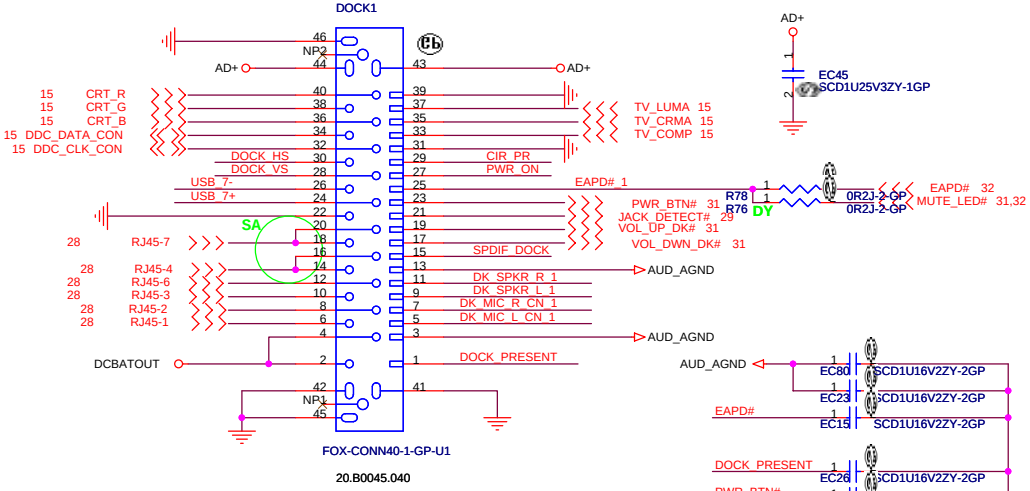
Date: Tuesday, December 19, 2006 Sheet 16 of 47

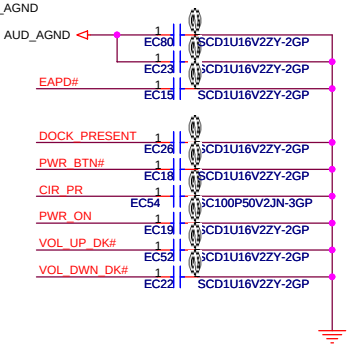
Docking Connector

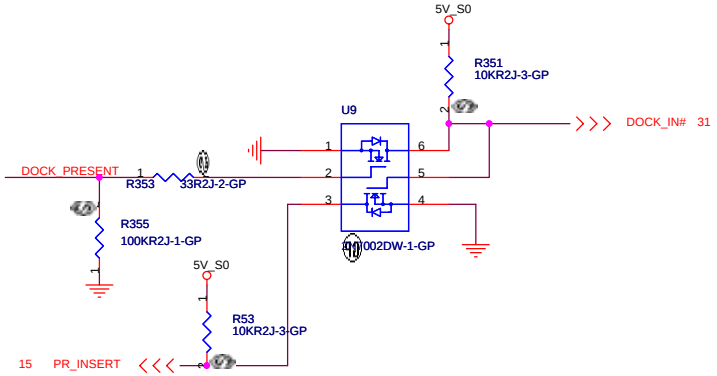


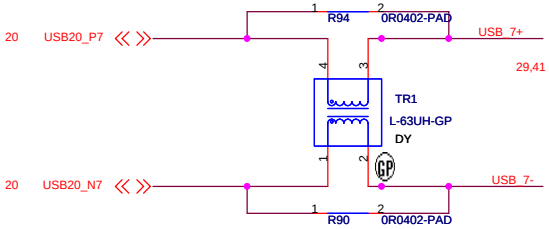
Hsync & Vsync level shift

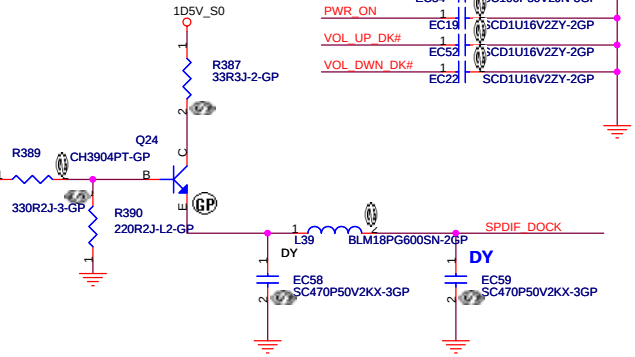


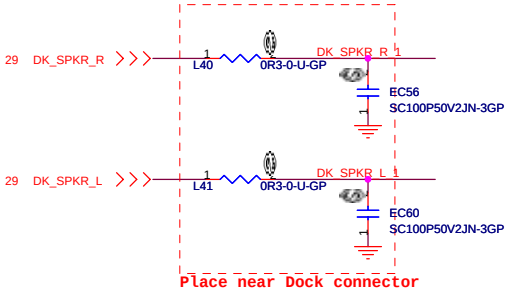


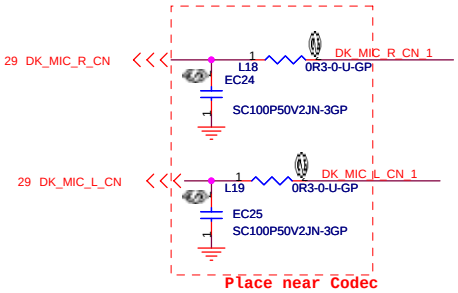


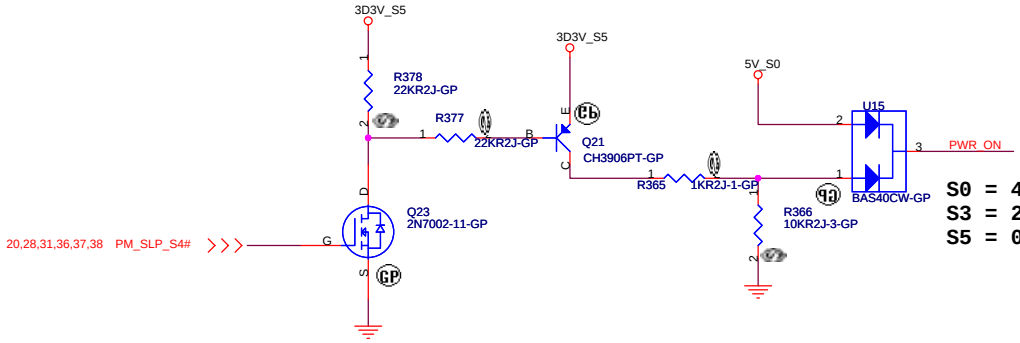












S0 = 4V
S3 = 2.5V
S5 = 0V

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Board to board conn/ Docking***

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A3	Pamirs-Discrete	SA

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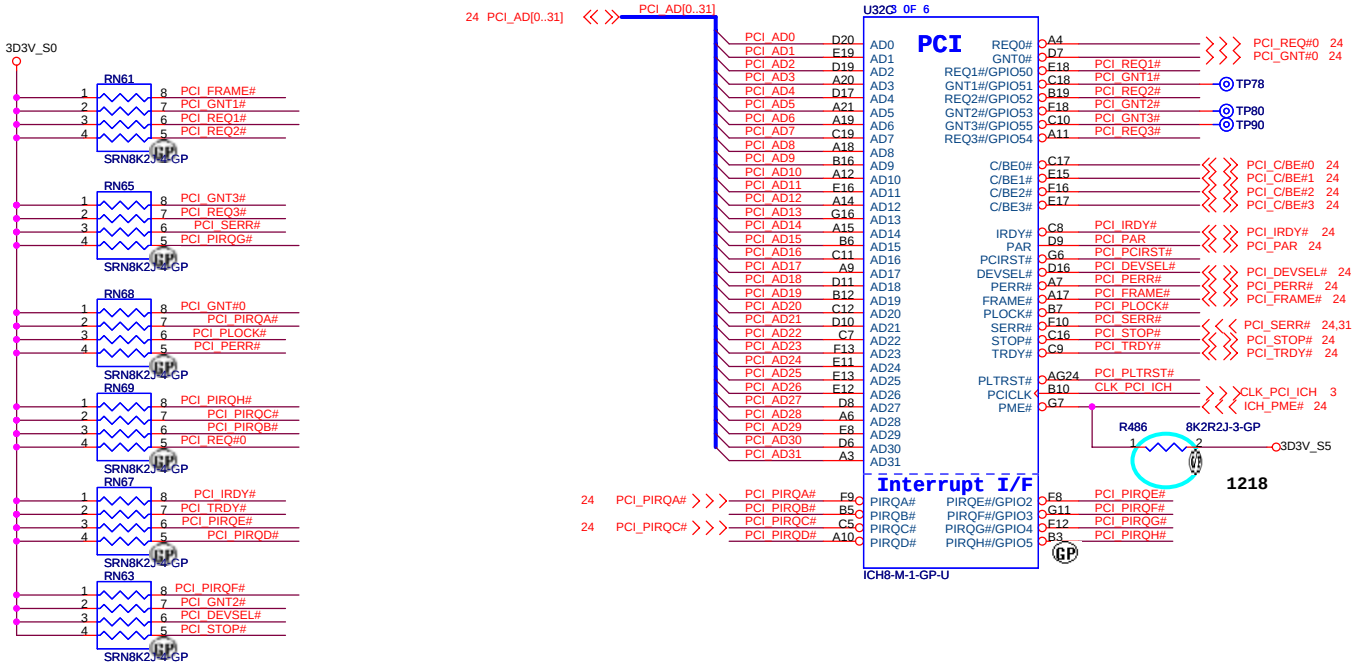
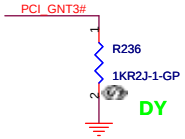
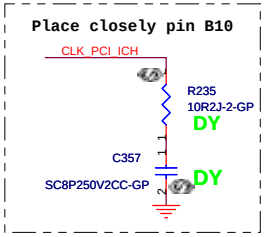
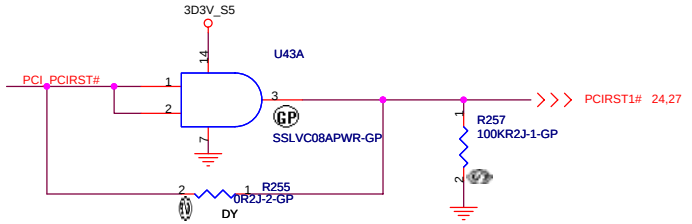


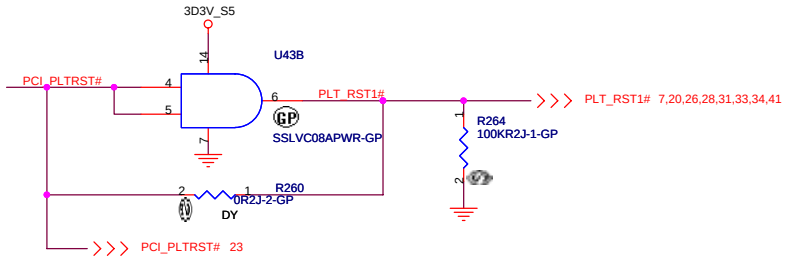


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





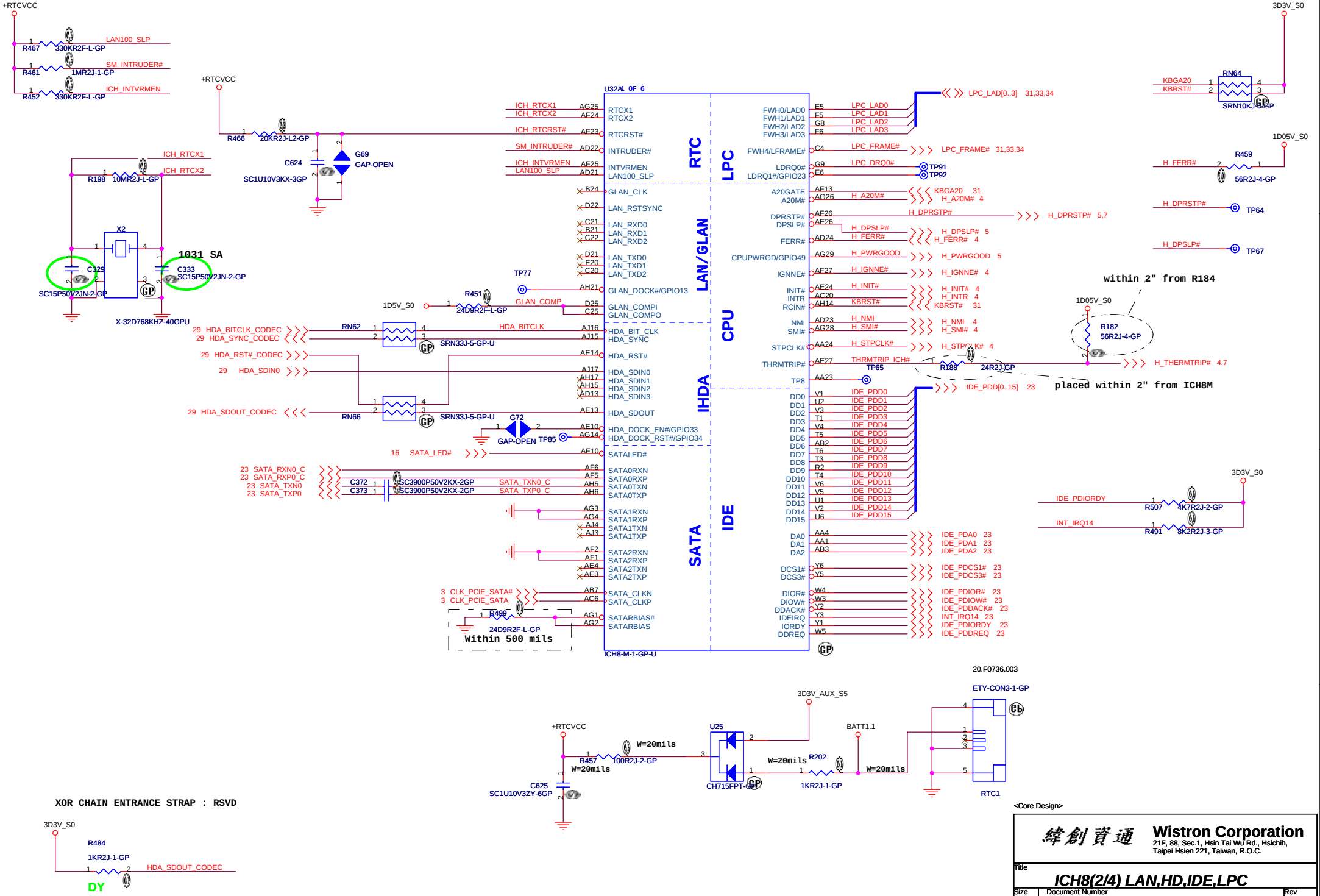
<Core Design>

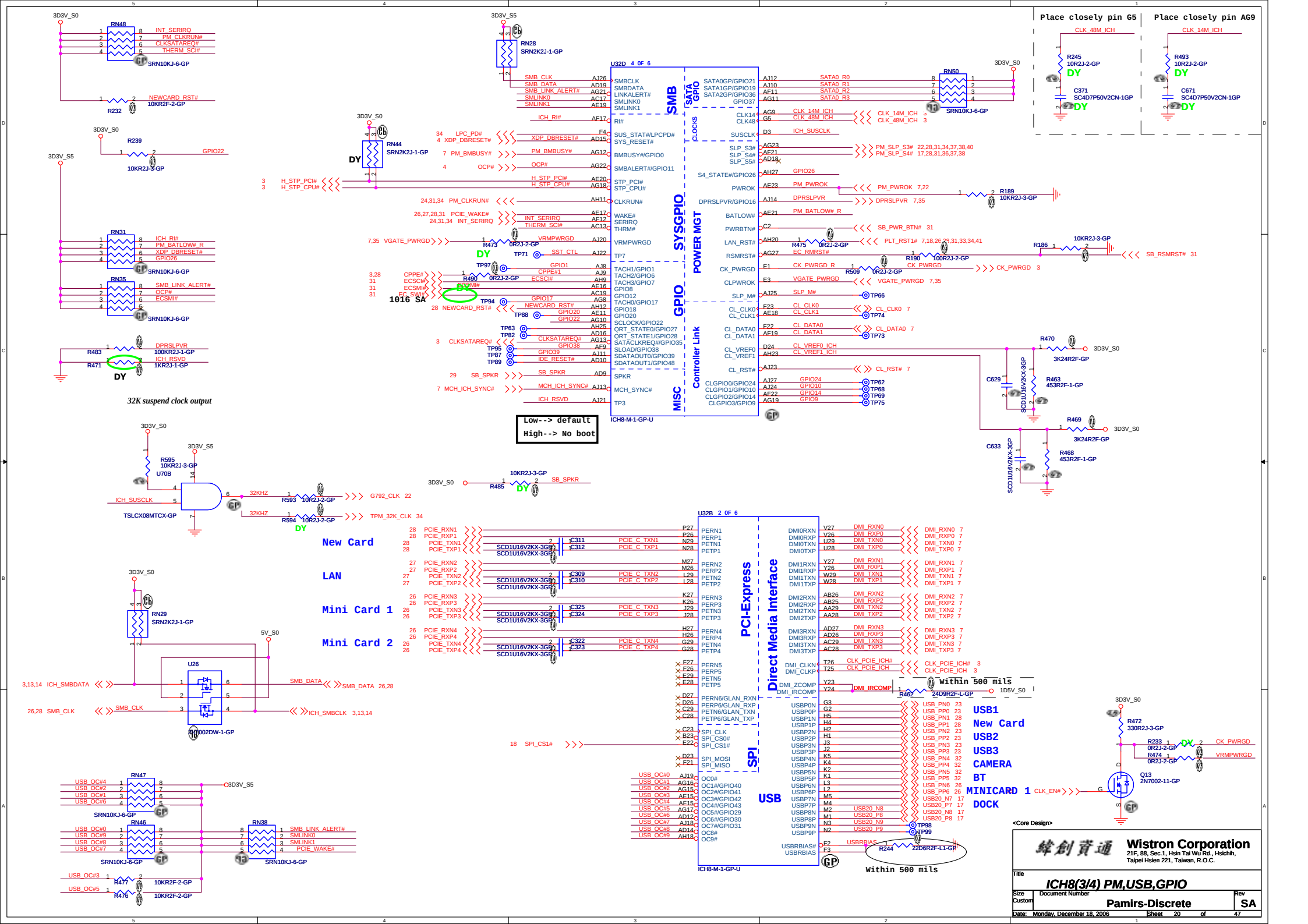
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

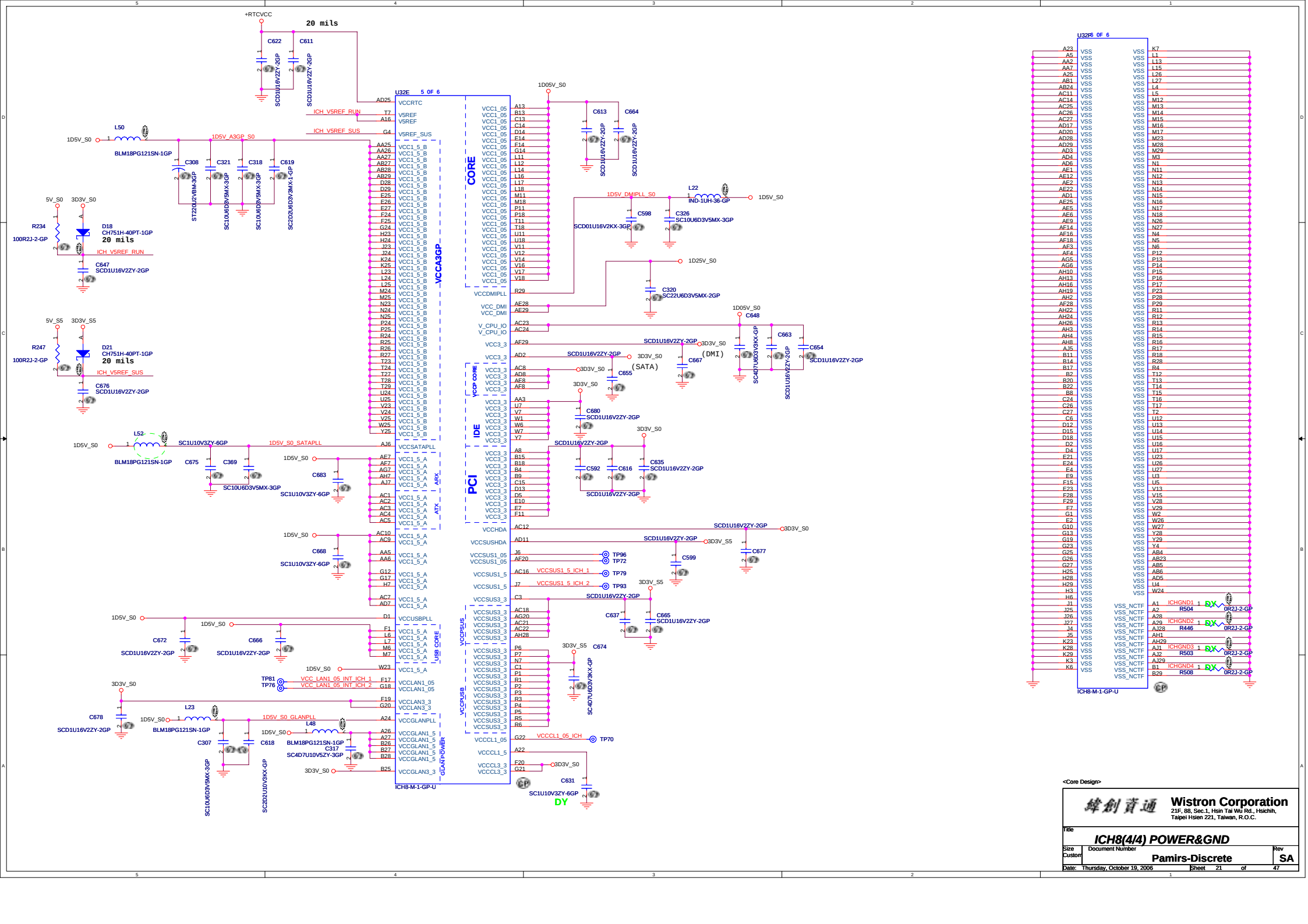
Title: ICH8(1/4)-PCI/INT

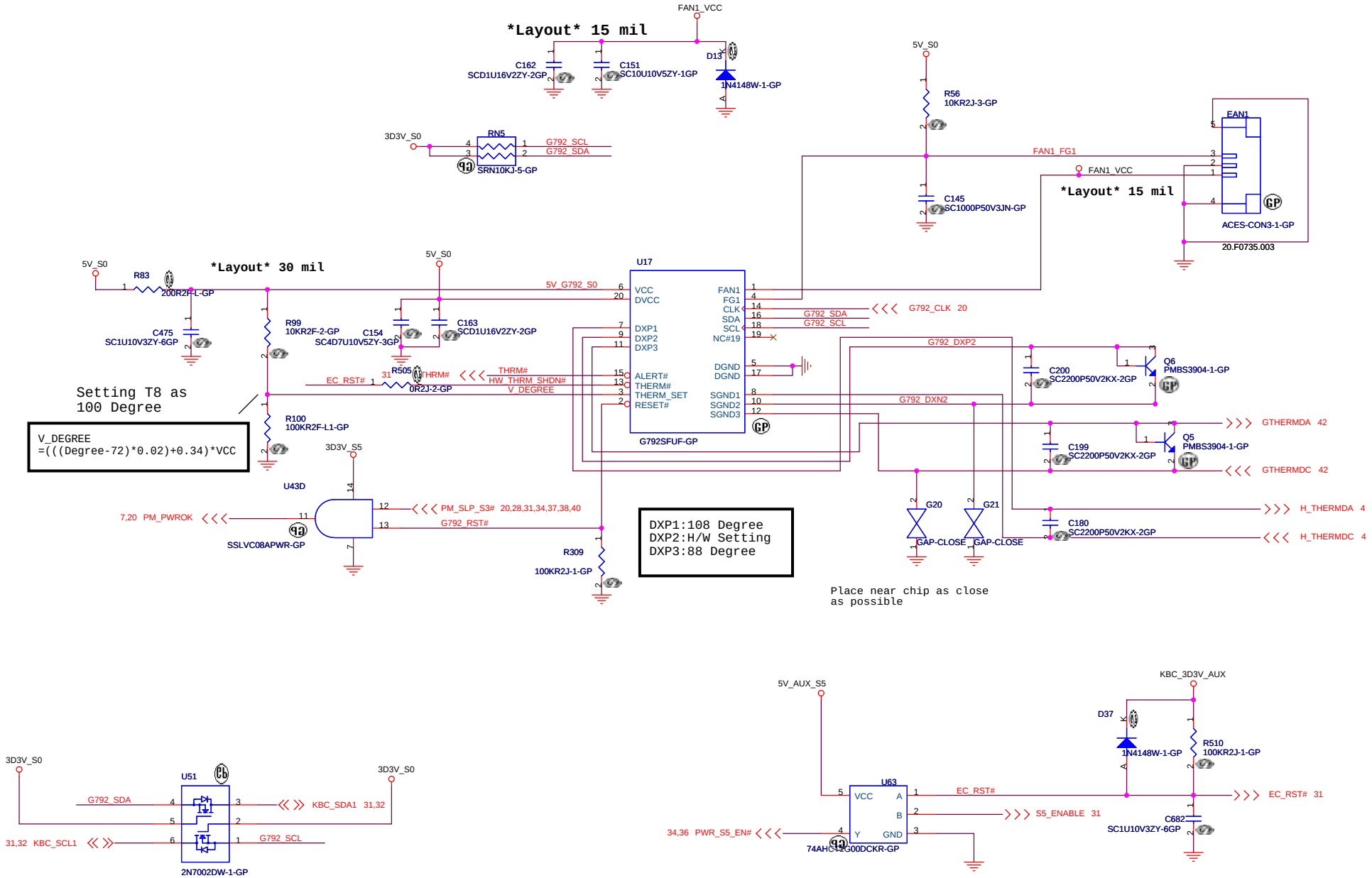
Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Monday, December 18, 2006 Sheet 18 of 47


+RTCVCC
R467 330KR2F-L-GP
LAN100_SLP
R461 1MR2J-1-GP
SM_INTRUDER#
R452 330KR2F-L-GP
ICH_INTVRMEN
R466 20KR2J-L2-GP
C624 SC1U10V3KX-3GP
G69 GAP-OPEN
ICH_RTCX1
ICH_RTCX2
R198 10MR2J-L-GP
X2
X-32D768KHZ-40GPU
C329 SC15P50V2JN-2-GP
C333 SC15P50V2JN-2-GP
1031 SA
U32A1 OF 6
RTC
LPC
LAN/GLAN
CPU
IHDA
IDE
SATA
ICH8-M-1-GP
TP77
R451 24D9R2F-L-GP
GLAN_COMP
1D5V_S0
RN62 SRN33J-5-GP-U
RN66 SRN33J-5-GP-U
HDA_BITCLK_CODEC
HDA_SYNC_CODEC
HDA_RST#_CODEC
HDA_SDIN0
HDA_SDOUT_CODEC
G72 GAP-OPEN
TP85
SATA_LED#
C372 SC3900P50V2KX-2GP
C373 SC3900P50V2KX-2GP
SATA_TXN0_C
SATA_TXP0_C
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0
SATA_TXP0
R499 24D9R2F-L-GP
Within 500 mils
CLK_PCIE_SATA#
CLK_PCIE_SATA
LPC_LAD[0..3] 31,33,34
LPC_FRAME# 31,33,34
LPC_DRQ0#
TP91
TP92
H_A20M# 4
KBGA20 31
H_DPRSTP# 5,7
H_DPSLP# 5
H_FERR# 4
H_PWRGOOD 5
H_IGNNE# 4
H_INIT# 4
H_INTR 4
KBRST# 31
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THERMTRIP# 4,7
TP65
R188 24R2J-GP
within 2" from R184
R182 56R2J-4-GP
placed within 2" from ICH8M
IDE_PDD[0..15] 23
IDE_PDIORDY
R507 4K7R2J-2-GP
INT_IRQ14
R491 8K2R2J-3-GP
IDE_PDA0 23
IDE_PDA1 23
IDE_PDA2 23
IDE_PDCS1# 23
IDE_PDCS3# 23
IDE_PDIOR# 23
IDE_PDIOW# 23
IDE_PDDACK# 23
INT_IRQ14 23
IDE_PDIORDY 23
IDE_PDDREQ 23
3D3V_S0
RN64 SRN10KJ-4-GP
KBGA20
KBRST#
1D05V_S0
R459 56R2J-4-GP
H_FERR#
TP64
TP67
20.F0736.003
ETY-CON3-1-GP
RTC1
3D3V_AUX_S5
U25 CH715FPT-GP
BATT1.1
R457 100R2J-2-GP
W=20mils
R202 1KR2J-1-GP
C625 SC1U10V3ZY-6GP
XOR CHAIN ENTRANCE STRAP : RSVD
R484 1KR2J-1-GP
HDA_SDOUT_CODEC
DY
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(2/4) LAN,HD,IDE,LPC
Size A3
Document Number
Pamirs-Discrete
Rev SA
Date: Wednesday, December 13, 2006
Sheet 19 of 47


Place closely pin G5
Place closely pin AG9
U32D 4 OF 6
ICH8-M-1-GP-U
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
Low--> default
High--> No boot
1016 SA
32K suspend clock output
U32B 2 OF 6
PCI-Express
Direct Media Interface
SPI
USB
New Card
LAN
Mini Card 1
Mini Card 2
USB1
New Card
USB2
USB3
CAMERA
BT
MINICARD 1
DOCK
Within 500 mils
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH8(3/4) PM,USB,GPIO
Pamirs-Discrete
SA
Monday, December 18, 2006
Sheet 20 of 47


+RTCVCC
20 mils
C622
C611
SCD1U16V2ZY-2GP
U32E 5 0F 6
VCCRTC
V5REF
V5REF_SUS
ICH_V5REF_RUN
ICH_V5REF_SUS
L50
BLM18PG121SN-1GP
1D5V_A3GP_S0
C308
C321
C318
C619
ST22UJ2V8M-3GP
SC10U6D3V5MX-3GP
SC22D2U6D3V3MX-1-GP
5V_S0
3D3V_S0
R234
100R2J-2-GP
D18
CH751H-40PT-1GP
C647
5V_S5
3D3V_S5
R247
D21
C676
L52
SC1U10V3ZY-6GP
1D5V_S0_SATAPLL
C675
C369
C683
L23
C678
1D5V_S0_GLANPLL
L48
C307
C618
C317
SC4D7U10V5ZY-3GP
SC2D2U10V3KX-GP
TP81
TP76
VCC_LAN1_05_INT_ICH_1
VCC_LAN1_05_INT_ICH_2
C672
C666
C668
VCCA3GP
VCCSATAPLL
ARX
ATX
USB CORE
VCCLAN1_05
VCCLAN3_3
VCCGLANPLL
VCCGLAN1_5
VCCGLAN3_3
GLAN POWER
ICH8-M-1-GP-U
CORE
IDE
PCI
VCCP CORE
VCCPSUS
VCCPUSB
1D05V_S0
C613
C664
SCD01U16V2KX-3GP
C598
C326
SC10U6D3V5MX-3GP
L22
IND-1UH-38-GP
1D5V_DMIPLL_S0
1D25V_S0
C320
SC22U6D3V5MX-2GP
C648
SC4D7U6D3V3KX-GP
C663
C654
SCD1U16V2ZY-2GP
(DMI)
(SATA)
C667
C655
C680
C592
C616
C635
C599
C677
C637
C665
C674
SC4D7U6D3V3KX-GP
C631
SC1U10V3ZY-6GP
DY
TP96
TP72
TP79
TP93
TP70
VCCSUS1_5_ICH_1
VCCSUS1_5_ICH_2
VCCCL1_05_ICH
3D3V_S5
U32F6 0F 6
ICH8-M-1-GP-U
ICHGND1
ICHGND2
ICHGND3
ICHGND4
R504
R446
R503
R508
0R2J-2-GP
<Core Design>
鋒創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(4/4) POWER&GND
Size
Custom
Document Number
Pamirs-Discrete
Rev
SA
Date: Thursday, October 19, 2006
Sheet 21 of 47



<Core Design>

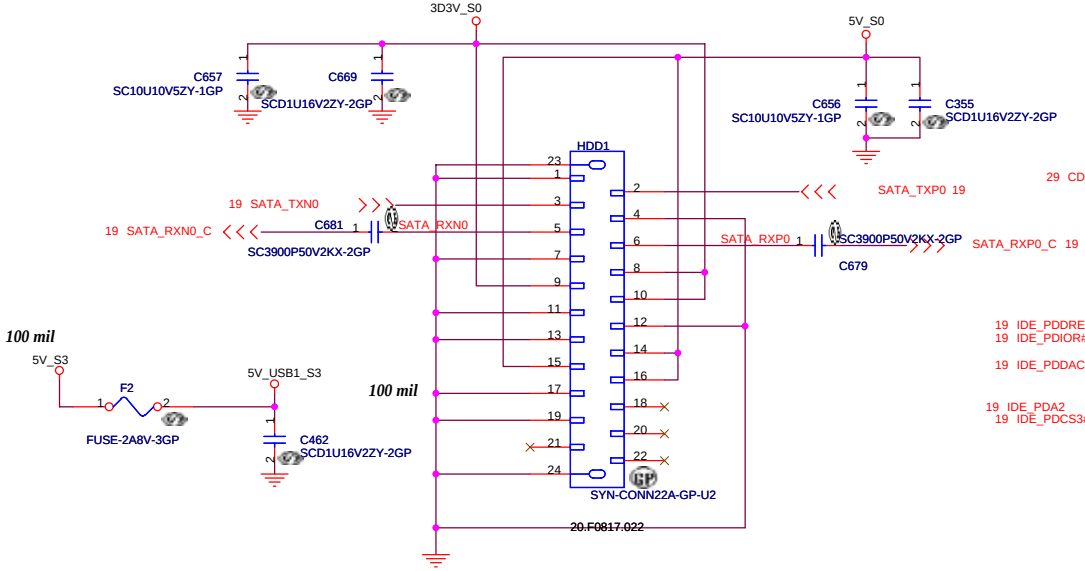
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor G792***

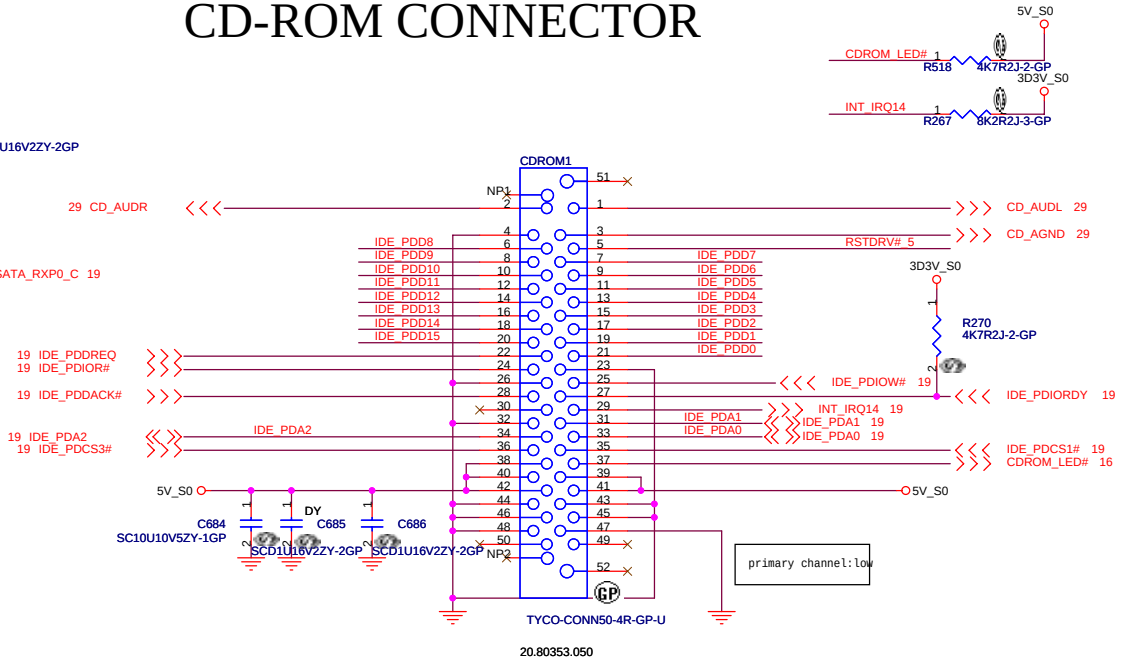
Size	Document Number	Rev
Custom	**Pamirs-Discrete**	**SA**

Date: Monday, October 23, 2006 Sheet 22 of 47

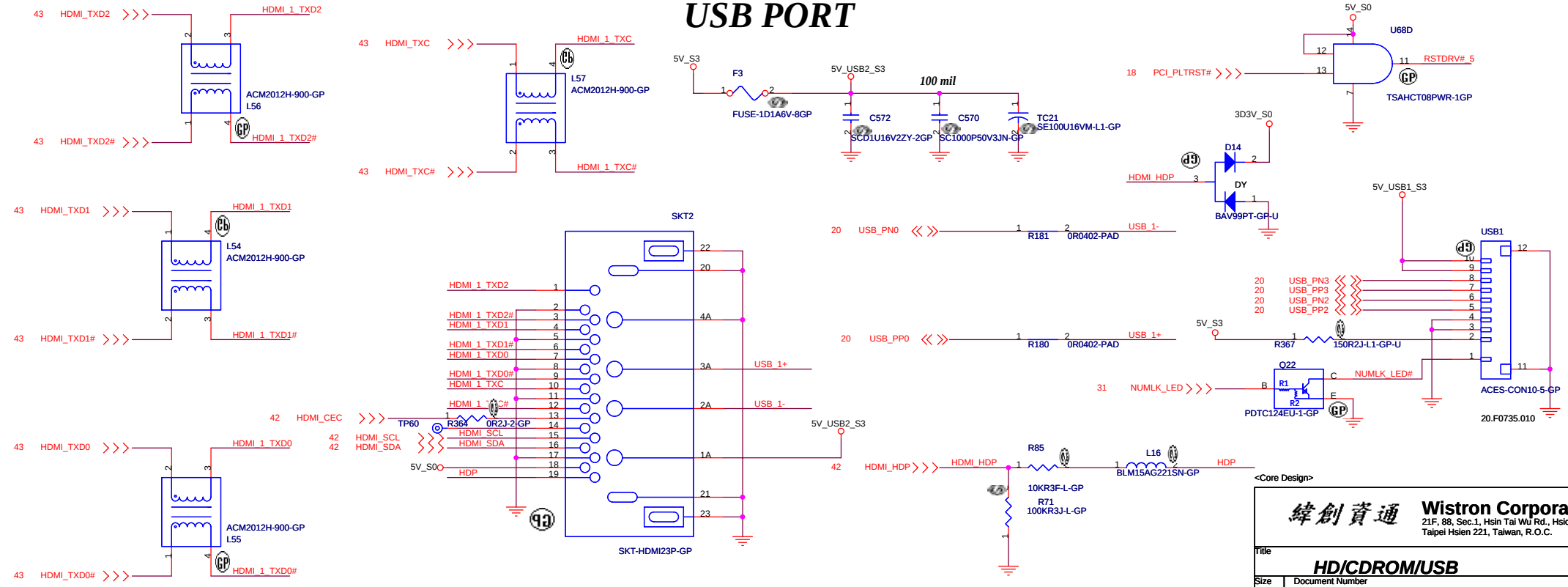
SATA HD Connector



CD-ROM CONNECTOR



USB PORT



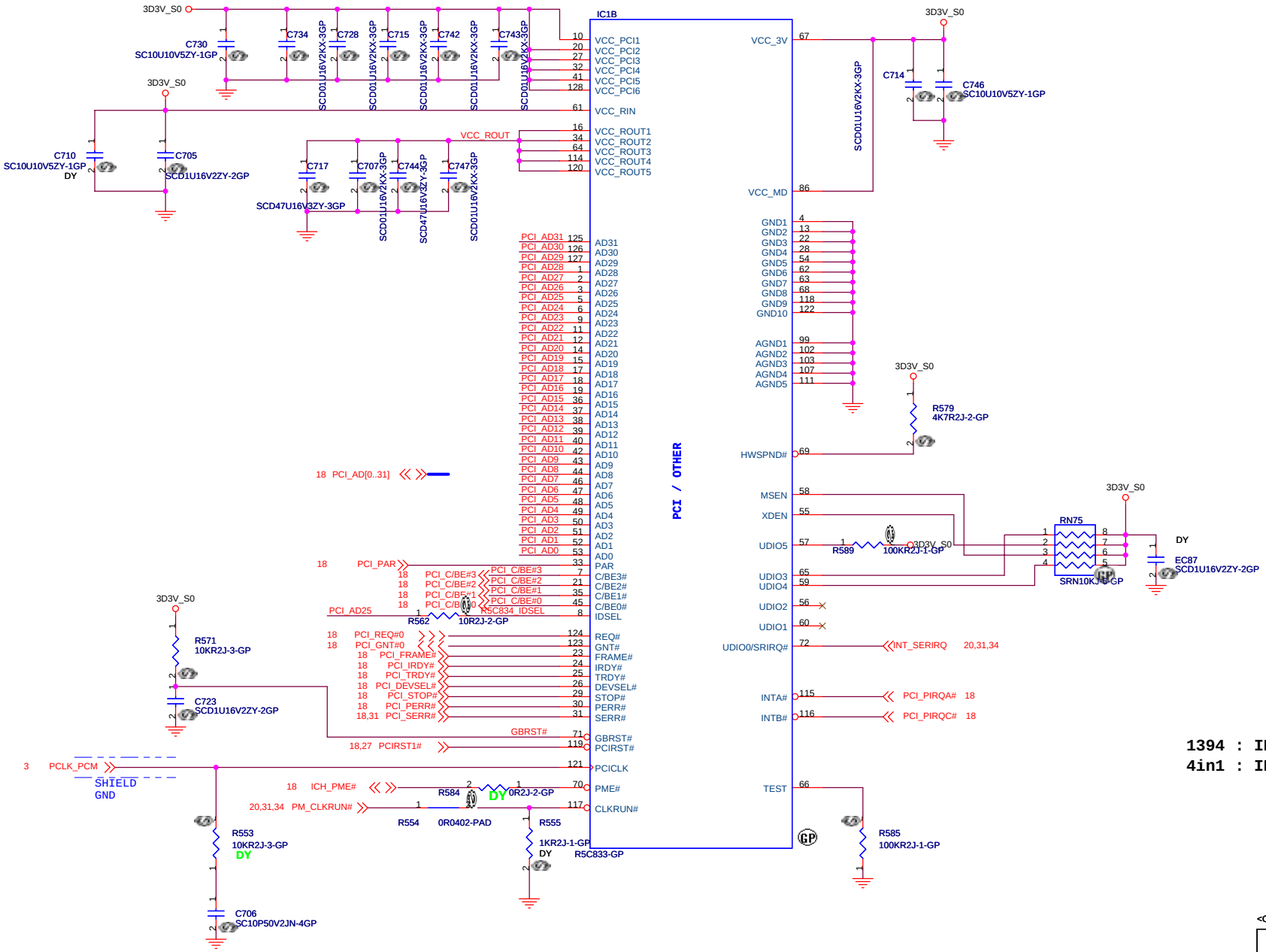
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HD/CDROM/USB**

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Tuesday, December 12, 2006 Sheet 23 of 47



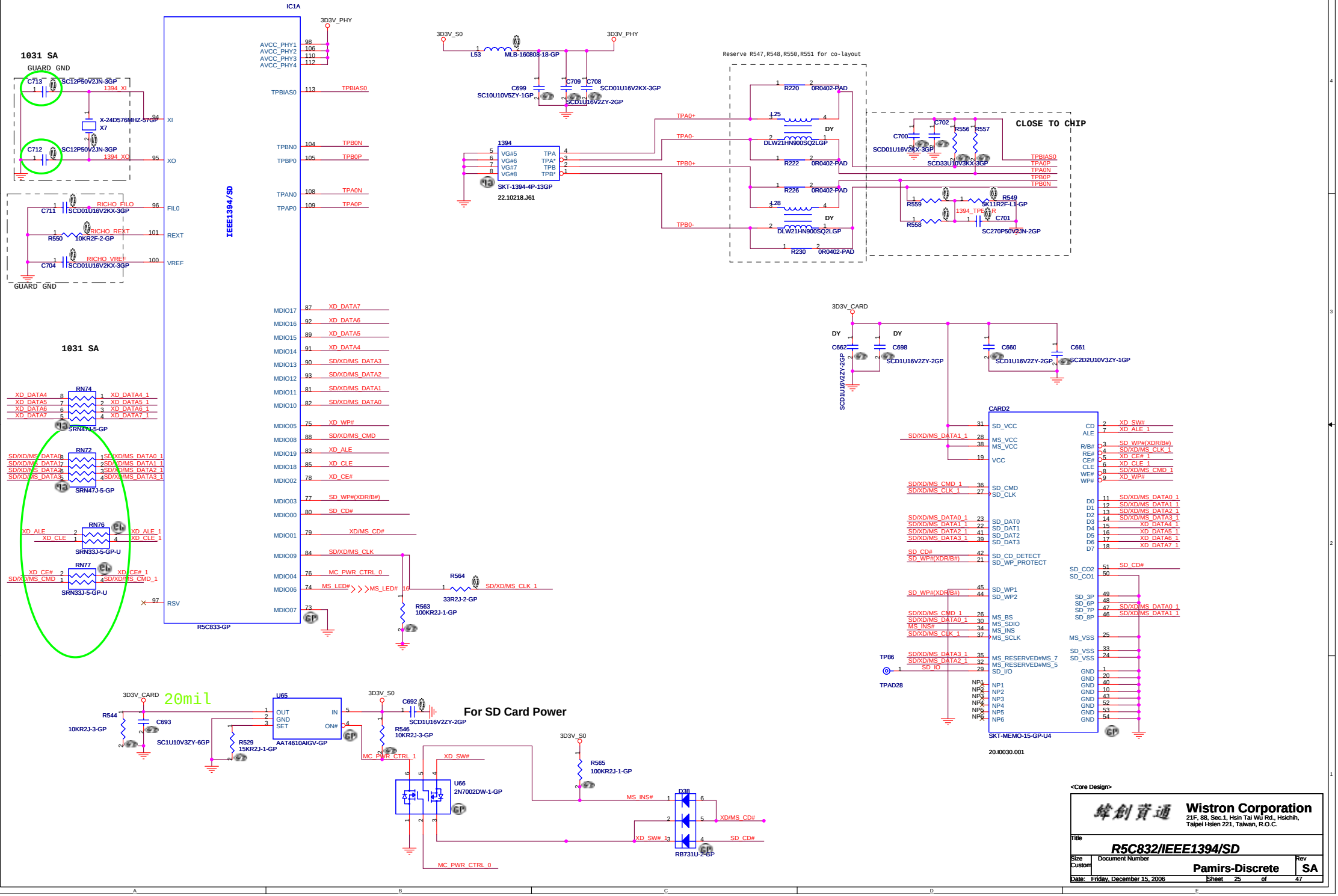
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C832/PCI

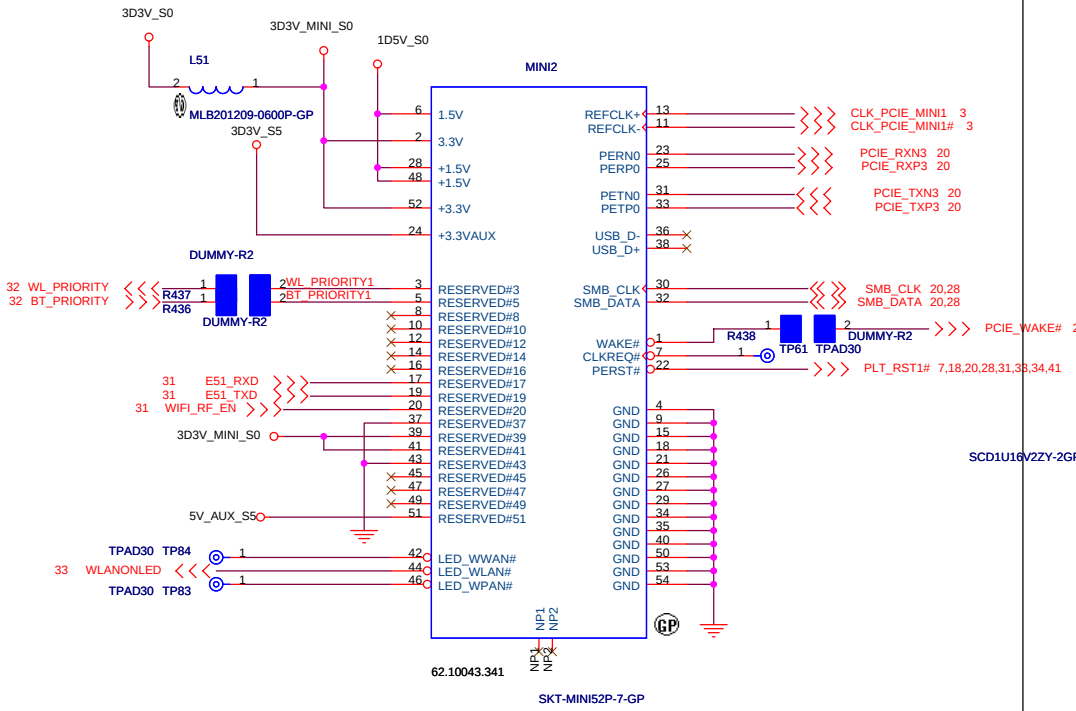
Size	Document Number	Rev
A3	Pamirs-Discrete	SA

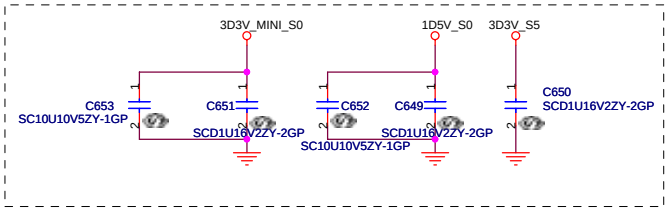
Date: Wednesday, December 06, 2006 Sheet 24 of 47


IC1A
IEEE1394/SD
R5C833-GP
1031 SA
GUARD GND
3D3V_PHY
3D3V_S0
3D3V_CARD
Reserve R547,R548,R550,R551 for co-layout
CLOSE TO CHIP
1394
SKT-1394-4P-13GP
22.10218.J61
DLW21HN900SQ2LGP
SCD01U16V2KX-3GP
SCD1U16V2ZY-2GP
SC12P50V2JN-3GP
X-24D576MHZ-57GP
SC1U10V3ZY-6GP
SCD33U10V3KX-3GP
SC270P50V2JN-2GP
SRN47J-5-GP
SRN33J-5-GP-U
SRN47J-5-GP
CARD2
SKT-MEMO-15-GP-U4
20.I0030.001
AAT4610AIGV-GP
2N7002DW-1-GP
RB731U-2-GP
For SD Card Power
20mil
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
R5C832/IEEE1394/SD
Pamirs-Discrete
Date: Friday, December 15, 2006
Sheet 25 of 47

Mini Card Connector 2

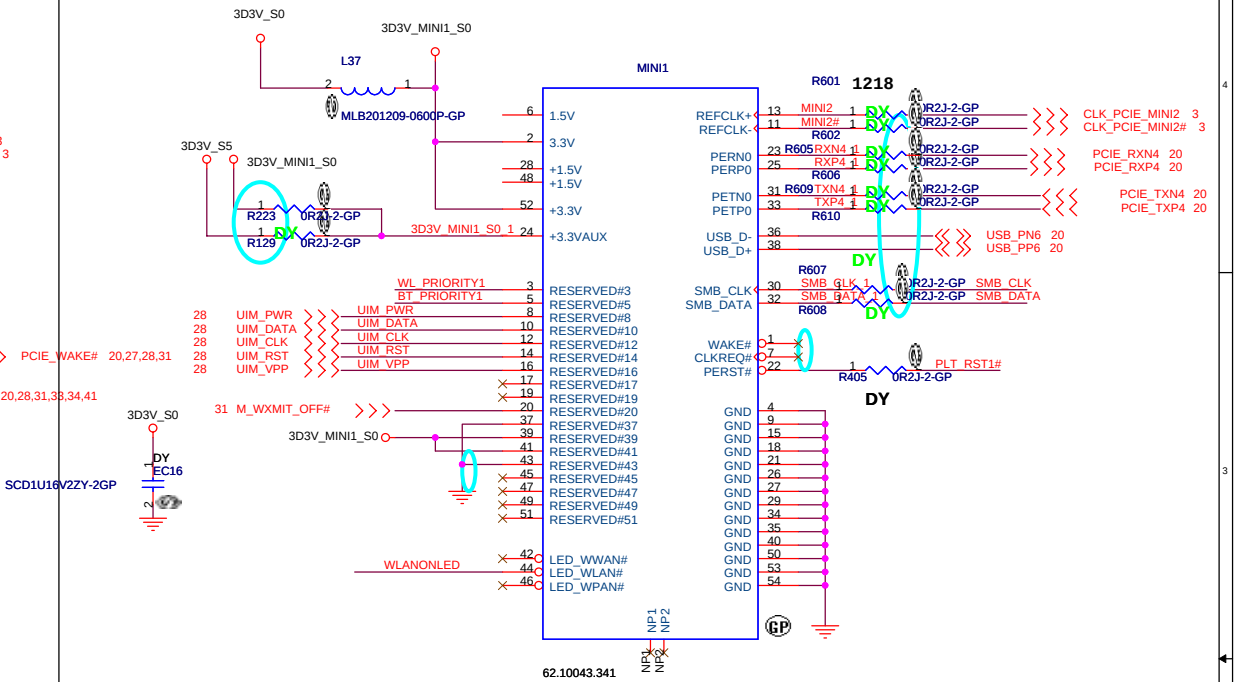
Wireless card

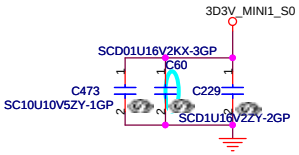




Mini Card Connector 1

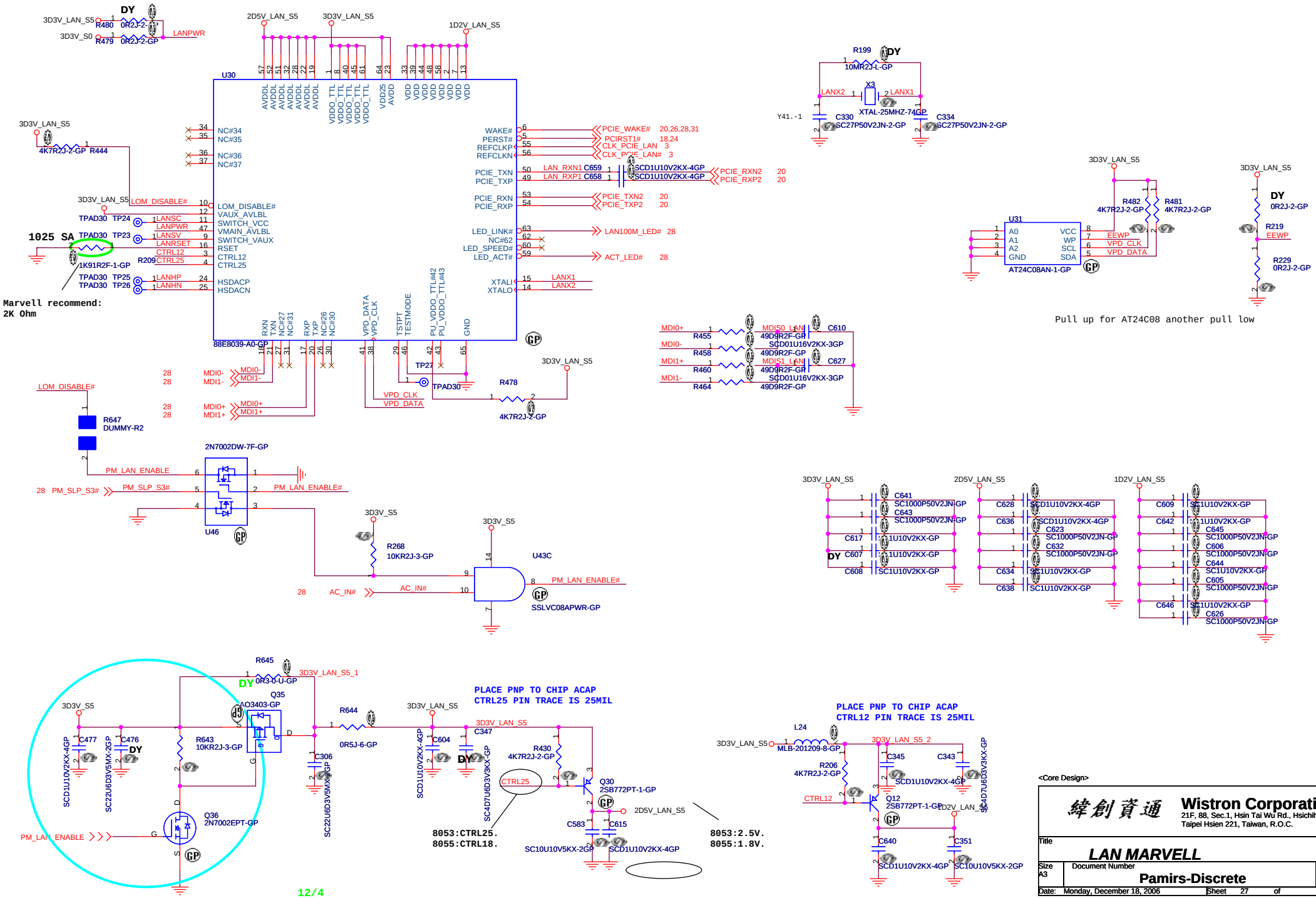
WWAN

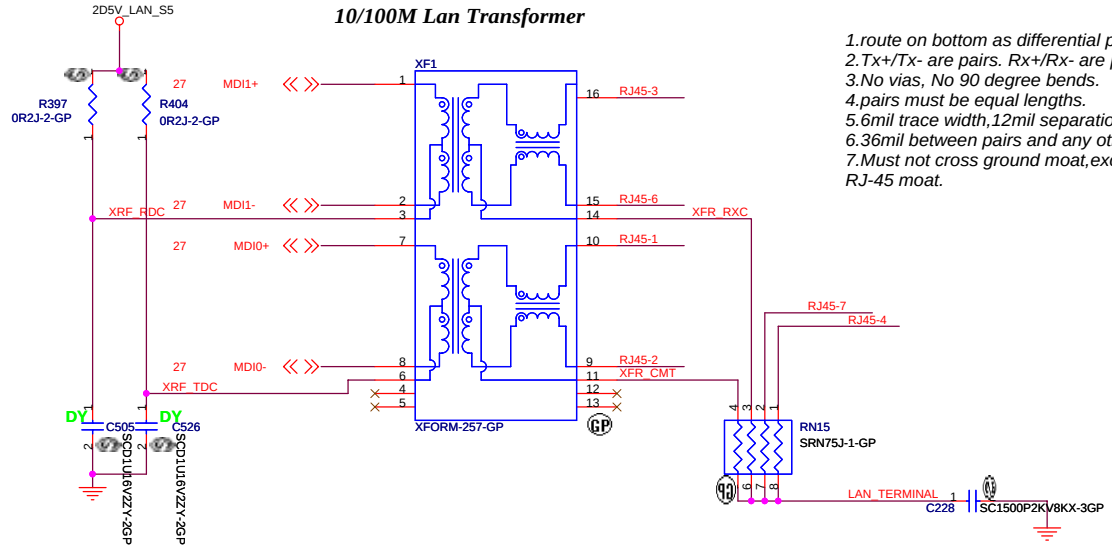




<Core Design>

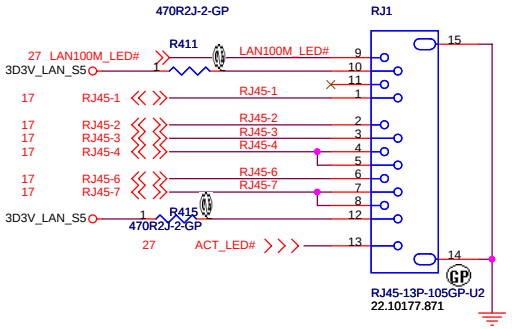
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI CARD CONN .***	
Size A3	Document Number **Pamirs-Discrete**	Rev **SA**
Date: Tuesday, December 19, 2006	Sheet 26 of 47	


U30
88E8039-A0-GP
1025 SA
Marvell recommend:
2K Ohm
U31
AT24C08AN-1-GP
Pull up for AT24C08 another pull low
U46
2N7002DW-7F-GP
U43C
SSLVC08APWR-GP
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
8053:CTRL25.
8055:CTRL18.
8053:2.5V.
8055:1.8V.
12/4
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LAN MARVELL
Pamirs-Discrete
Monday, December 18, 2006



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW

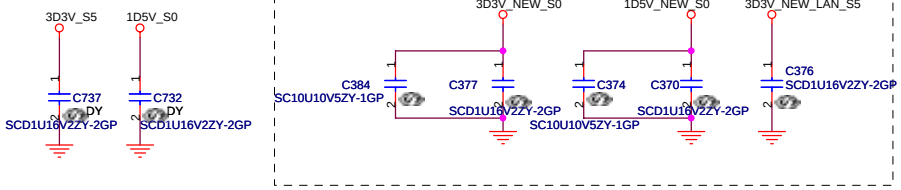


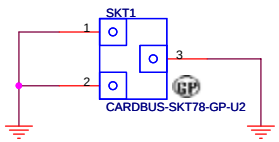
Green : Link up
Blinking : TX/RX activity

NEWCARD Connector

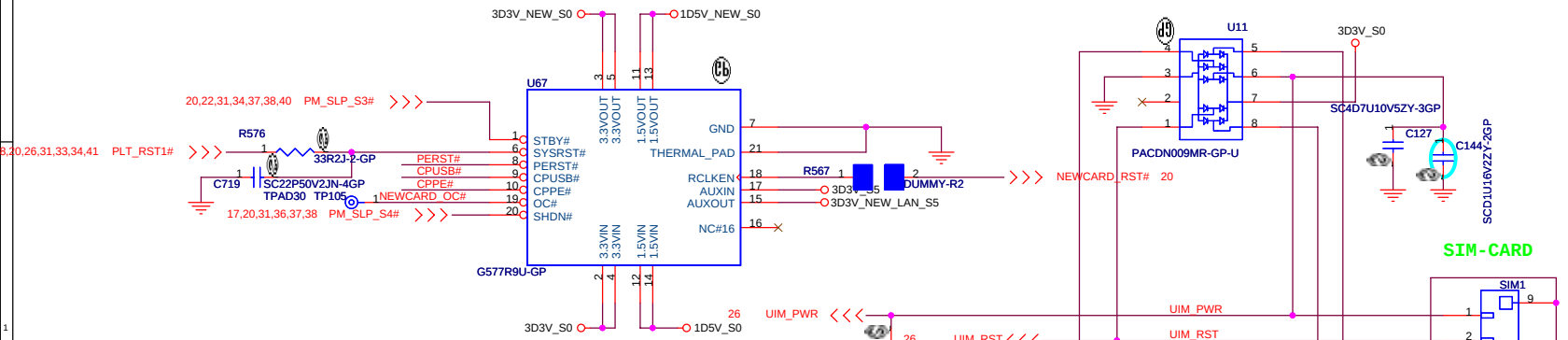
Place them Near to Chip

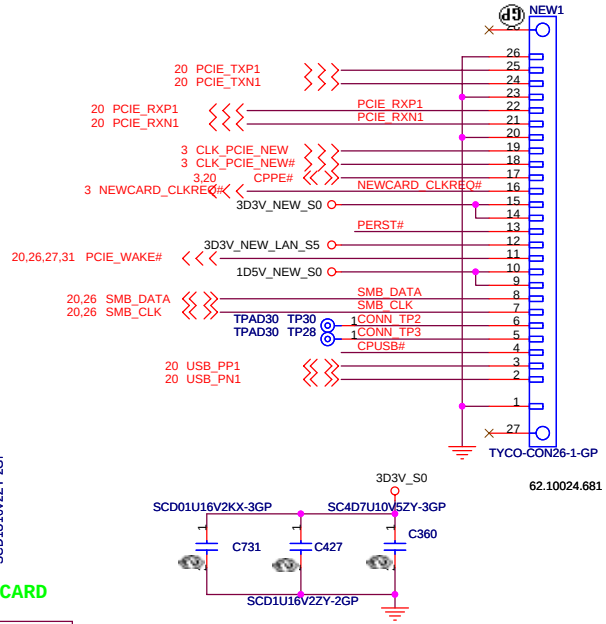
Place them Near to Connector





For Newcard socket





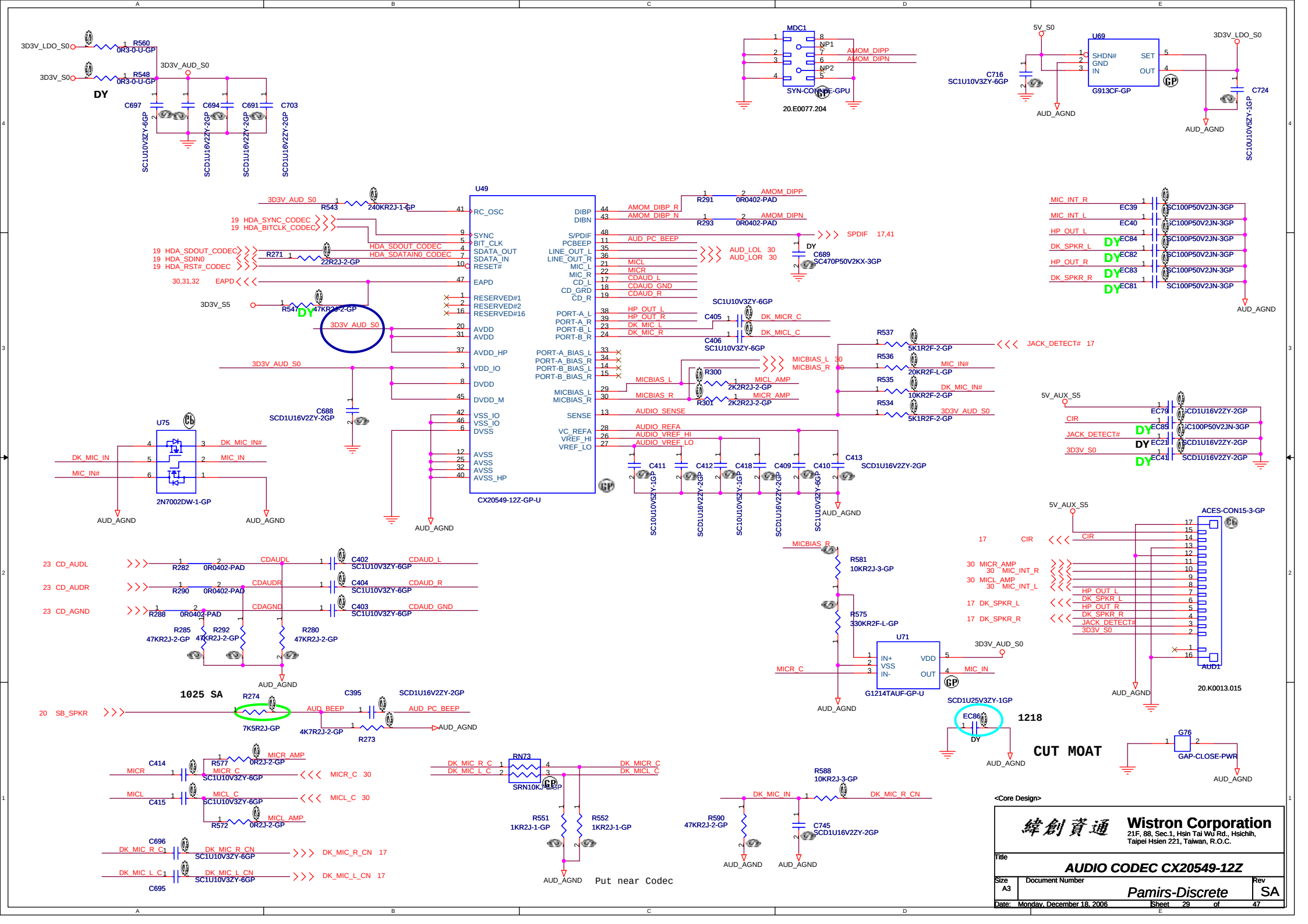
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN connector/NEW CARD/SIM

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Tuesday, December 12, 2006 Sheet 28 of 47


3D3V_LDO_S0
R560 0R3-0-U-GP
3D3V_S0
R548 0R3-0-U-GP
3D3V_AUD_S0
DY
C697 SC1U10V3ZY-6GP
C694 SC1U16V2ZY-2GP
C691 SCD1U16V2ZY-2GP
C703 SCD1U16V2ZY-2GP
MDC1
NP1
NP2
AMOM_DIPP
AMOM_DIPN
SYN-CONDE-GPU
20.E0077.204
5V_S0
U69
SHDN#
GND
IN
SET
OUT
G913CF-GP
C716 SC1U10V3ZY-6GP
C724 SC10U10V5ZY-1GP
AUD_AGND
U49
RC_OSC
SYNC
BIT_CLK
SDATA_OUT
SDATA_IN
RESET#
EAPD
RESERVED#1
RESERVED#2
RESERVED#16
AVDD
AVDD
AVDD_HP
VDD_IO
DVDD
DVDD_M
VSS_IO
VSS_IO
DVSS
AVSS
AVSS
AVSS
AVSS_HP
DIBP
DIBN
S/PDIF
PCBEEP
LINE_OUT_L
LINE_OUT_R
MIC_L
MIC_R
CD_L
CD_GRD
CD_R
PORT-A_L
PORT-A_R
PORT-B_L
PORT-B_R
PORT-A_BIAS_L
PORT-A_BIAS_R
PORT-B_BIAS_L
PORT-B_BIAS_R
MICBIAS_L
MICBIAS_R
SENSE
VC_REFA
VREF_HI
VREF_LO
CX20549-12Z-GP-U
R543 240KR2J-1-GP
R271 22R2J-2-GP
R541 47KR2J-2-GP
C688 SCD1U16V2ZY-2GP
R291 0R0402-PAD
R293 0R0402-PAD
SPDIF 17,41
C689 SC470P50V2KX-3GP
AUD_PC_BEEP
AUD_LOL 30
AUD_LOR 30
C405 SC1U10V3ZY-6GP
C406 SC1U10V3ZY-6GP
DK_MICR_C
DK_MICL_C
R300 2K2R2J-2-GP
R301 2K2R2J-2-GP
MICL_AMP
MICR_AMP
MICBIAS_L 30
MICBIAS_R 30
R537 5K1R2F-2GP
R536 20KR2F-L-GP
R535 10KR2F-2GP
R534 5K1R2F-2GP
JACK_DETECT# 17
MIC_IN#
DK_MIC_IN#
3D3V_AUD_S0
AUDIO_SENSE
AUDIO_REFA
AUDIO_VREF_HI
AUDIO_VREF_LO
C411 SC10U10V5ZY-1GP
C412 SCD1U16V2ZY-2GP
C418 SC10U10V5ZY-1GP
C409 SCD1U16V2ZY-2GP
C410 SC1U10V3ZY-6GP
C413 SCD1U16V2ZY-2GP
MIC_INT_R
MIC_INT_L
HP_OUT_L
DK_SPKR_L
HP_OUT_R
DK_SPKR_R
EC39 SC100P50V2JN-3GP
EC40 SC100P50V2JN-3GP
EC84 SC100P50V2JN-3GP
EC82 SC100P50V2JN-3GP
EC83 SC100P50V2JN-3GP
EC81 SC100P50V2JN-3GP
5V_AUX_S5
CIR
JACK_DETECT#
3D3V_S0
EC79 SCD1U16V2ZY-2GP
EC85 SC100P50V2JN-3GP
EC21 SCD1U16V2ZY-2GP
EC41 SCD1U16V2ZY-2GP
U75
2N7002DW-1-GP
DK_MIC_IN
MIC_IN#
MIC_IN
CD_AUDL
CD_AUDR
CD_AGND
R282 0R0402-PAD
R290 0R0402-PAD
R288 0R0402-PAD
CDAUDL
CDAUDR
CDAGND
C402 SC1U10V3ZY-6GP
C404 SC1U10V3ZY-6GP
C403 SC1U10V3ZY-6GP
CDAUD_L
CDAUD_R
CDAUD_GND
R285 47KR2J-2-GP
R292 47KR2J-2-GP
R280 47KR2J-2-GP
1025 SA
R274 7K5R2J-GP
C395 SCD1U16V2ZY-2GP
SB_SPKR
AUD_BEEP
AUD_PC_BEEP
R273 4K7R2J-2-GP
MICBIAS_R
R581 10KR2J-3-GP
R575 330KR2F-L-GP
U71
IN+
VSS
IN-
VDD
OUT
G1214TAUF-GP-U
MICR_C
MIC_IN
3D3V_AUD_S0
MICR_AMP 30
MICL_AMP 30
MIC_INT_R
MIC_INT_L
ACES-CON15-3-GP
AUD1
20.K0013.015
SCD1U25V3ZY-1GP
EC86
DY
1218
CUT MOAT
G76
GAP-CLOSE-PWR
C414 SC1U10V3ZY-6GP
C415 SC1U10V3ZY-6GP
R577 0R2J-2-GP
R572 0R2J-2-GP
MICR_C 30
MICL_C 30
C696 SC1U10V3ZY-6GP
C695 SC1U10V3ZY-6GP
DK_MIC_R_CN 17
DK_MIC_L_CN 17
RN73 SRN10KJ-6-GP
R551 1KR2J-1-GP
R552 1KR2J-1-GP
Put near Codec
R588 10KR2J-3-GP
R590 47KR2J-2-GP
C745 SCD1U16V2ZY-2GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC CX20549-12Z
Size A3
Document Number
Pamirs-Discrete
Rev SA
Date: Monday, December 18, 2006
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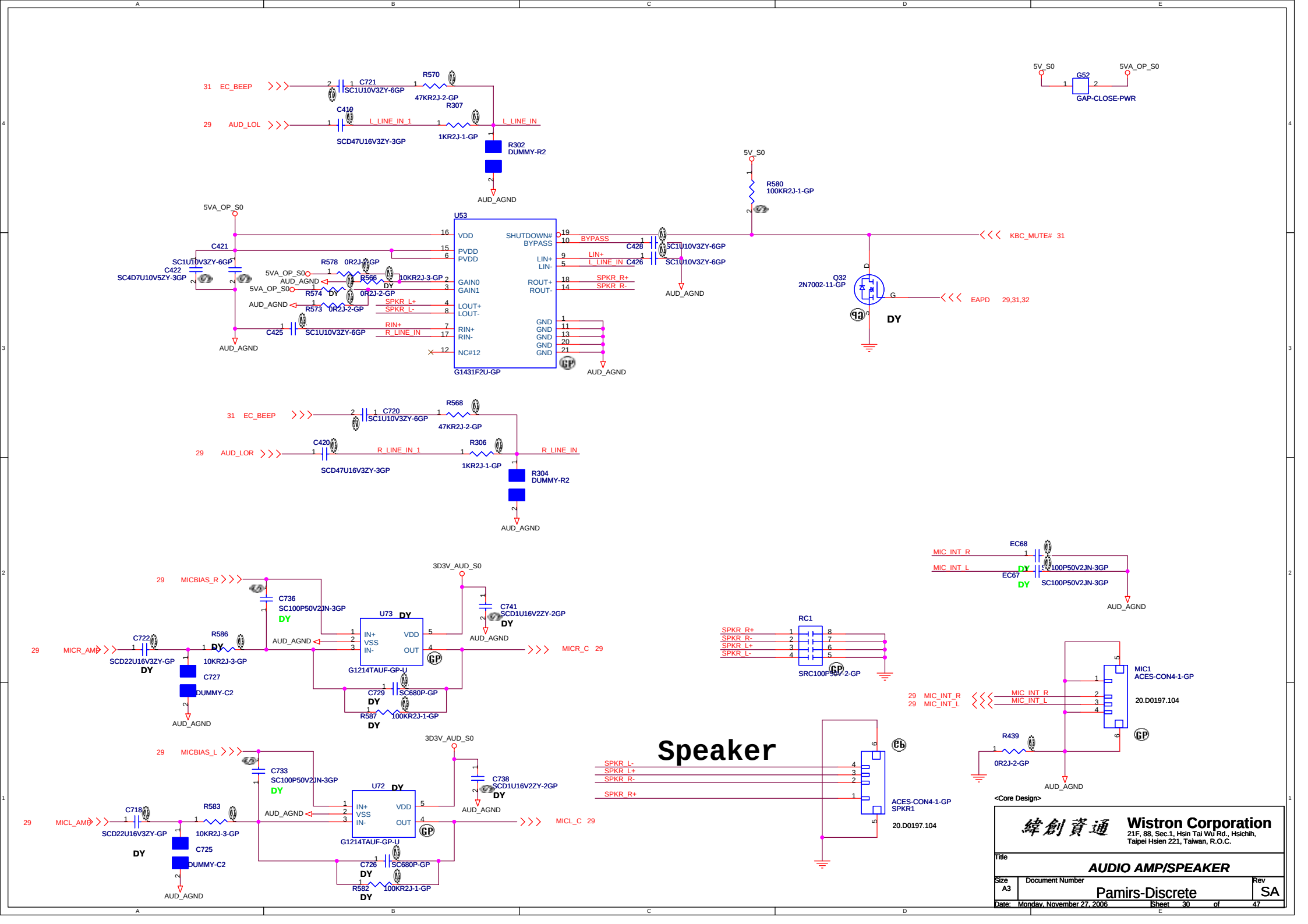
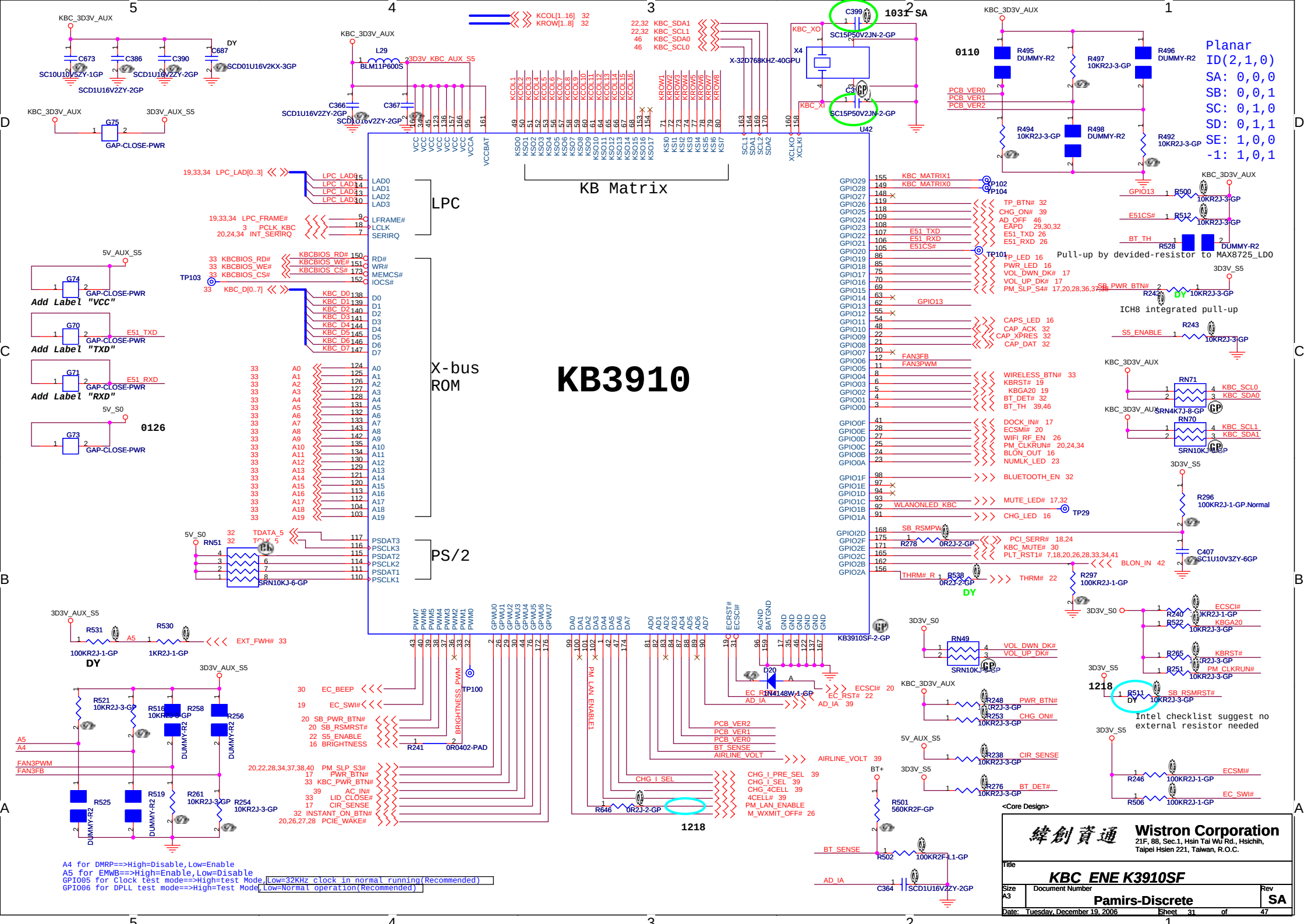

31 EC_BEEP
C721
SC1U10V3ZY-6GP
R570
47KR2J-2-GP
R307
29 AUD_LOL
C419
L_LINE_IN_1
L_LINE_IN
SCD47U16V3ZY-3GP
1KR2J-1-GP
R302
DUMMY-R2
AUD_AGND
5V_S0
5VA_OP_S0
G52
GAP-CLOSE-PWR
R580
100KR2J-1-GP
U53
VDD
PVDD
GAIN0
GAIN1
LOUT+
LOUT-
RIN+
RIN-
NC#12
SHUTDOWN#
BYPASS
LIN+
LIN-
ROUT+
ROUT-
GND
G1431F2U-GP
C421
C422
SC4D7U10V5ZY-3GP
R578
R566
10KR2J-3-GP
R574
R573
0R2J-2-GP
C425
SPKR_L+
SPKR_L-
RIN+
R_LINE_IN
C428
C426
BYPASS
LIN+
L_LINE_IN
SPKR_R+
SPKR_R-
KBC_MUTE# 31
Q32
2N7002-11-GP
EAPD 29,31,32
DY
31 EC_BEEP
C720
R568
47KR2J-2-GP
29 AUD_LOR
C420
R_LINE_IN_1
R_LINE_IN
R306
1KR2J-1-GP
R304
DUMMY-R2
3D3V_AUD_S0
29 MICBIAS_R
C736
SC100P50V2JN-3GP
U73
C741
SCD1U16V2ZY-2GP
29 MICR_AMP
C722
SCD22U16V3ZY-GP
R586
C727
DUMMY-C2
IN+
IN-
VSS
VDD
OUT
G1214TAUF-GP-U
MICR_C 29
C729
SC680P-GP
R587
100KR2J-1-GP
29 MICBIAS_L
C733
U72
C738
29 MICL_AMP
C718
SCD22U16V3ZY-GP
R583
C725
DUMMY-C2
C726
SC680P-GP
R582
100KR2J-1-GP
MICL_C 29
RC1
SPKR_R+
SPKR_R-
SPKR_L+
SPKR_L-
SRC100P50V2-2-GP
EC68
EC67
MIC_INT_R
MIC_INT_L
SC100P50V2JN-3GP
MIC1
ACES-CON4-1-GP
20.D0197.104
R439
0R2J-2-GP
Speaker
SPKR_L-
SPKR_L+
SPKR_R-
SPKR_R+
ACES-CON4-1-GP
SPKR1
20.D0197.104
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO AMP/SPEAKER
Size
A3
Document Number
Pamirs-Discrete
Rev
SA
Date: Monday, November 27, 2006
Sheet 30 of 47


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
Add Label "VCC"
Add Label "TXD"
Add Label "RXD"
Pull-up by devided-resistor to MAX8725_LDO
ICH8 integrated pull-up
Intel checklist suggest no external resistor needed
Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
SE: 1,0,0
-1: 1,0,1
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_ENE K3910SF
Pamirs-Discrete
Tuesday, December 19, 2006
SA

CAMERA

Blue thumb

Internal KeyBoard Connector

31 KROW[1..8]
31 KCOL[1..16]

KB1
ACES-CON24-2-GP
20.K0220.024

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

TouchPad Connector

TPAD1
FOX-CON4-12-GP
SA 1011

TOUCH-PAD SWITCH

SW1
SW-TACT-68-GP-U
62.40009.451

CAPACITY BUTTON

CAP1
ACES-CON12-4-GP
20.K0228.012

BT1
ACES-CON8-4-GP
20.F0772.008

CAM1
ACES-CON5-1GP
20.D0197.105

Close to CN8

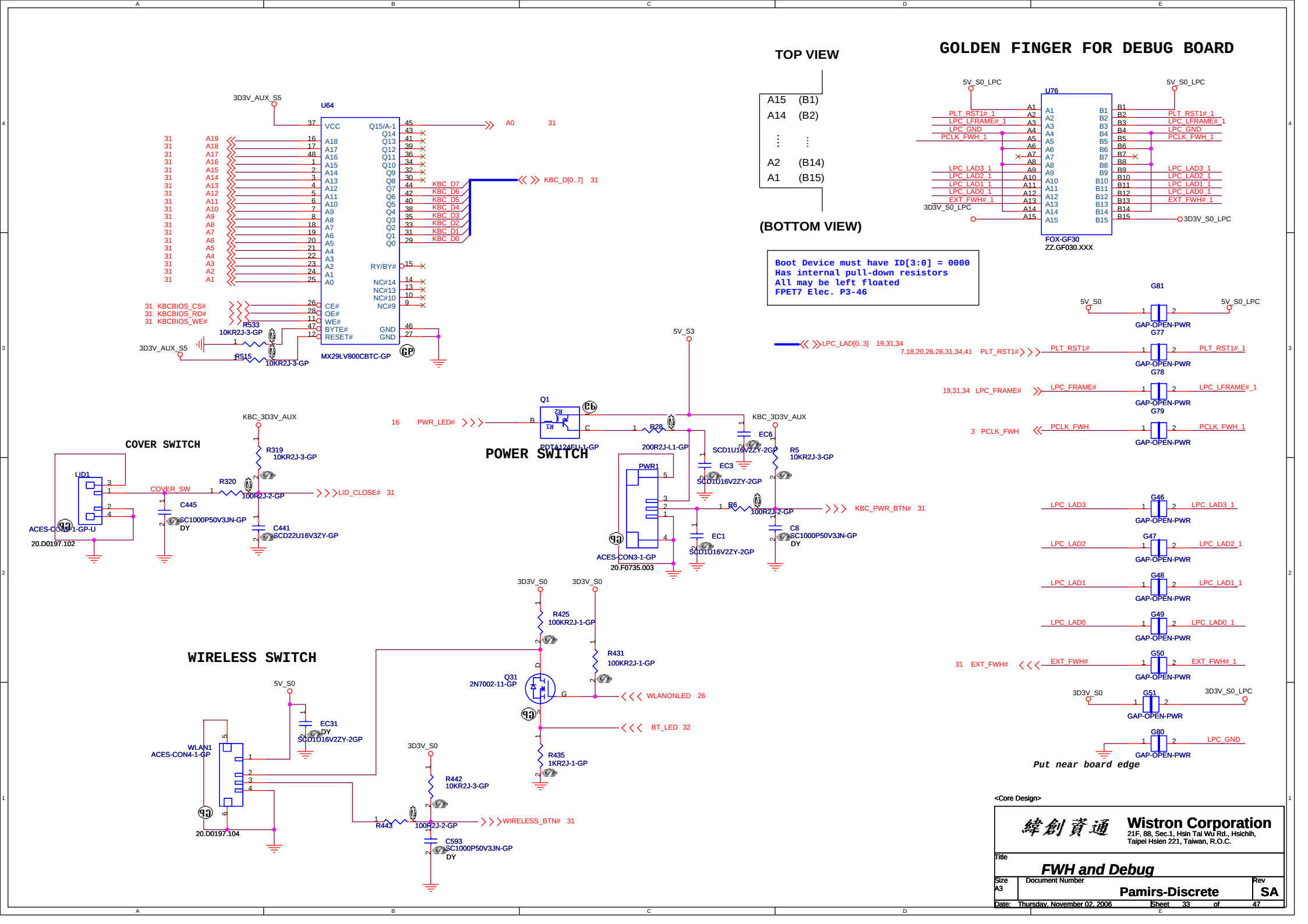
MAX 150mA

for EMI

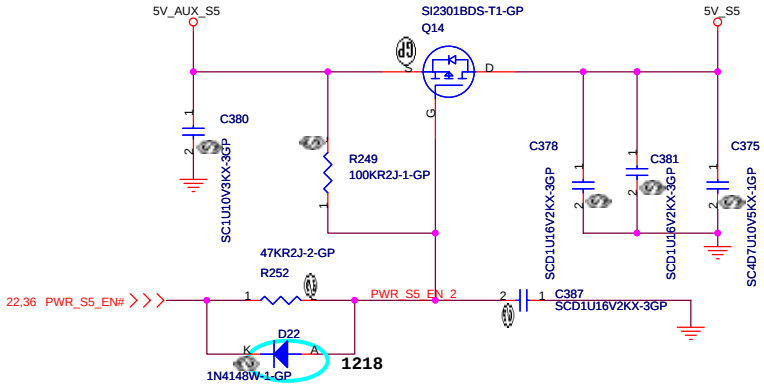
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

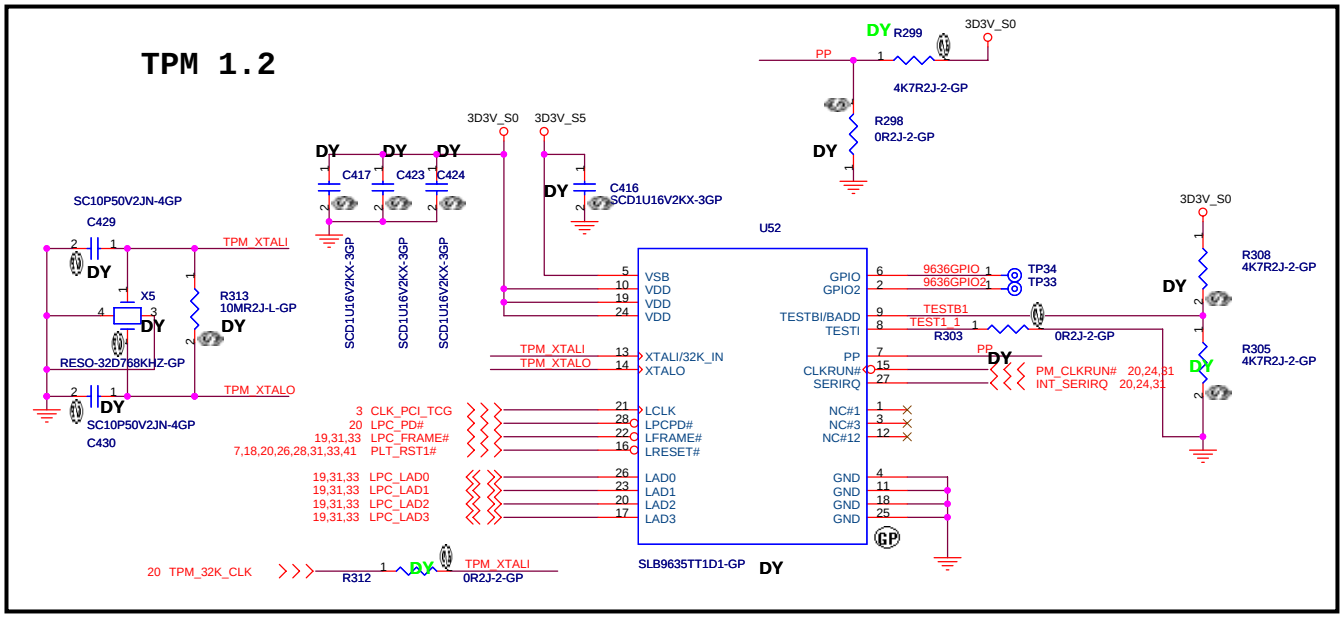
Title: KeyBoard-CONN
Size: A3
Document Number: Pamirs-Discrete
Rev: SA
Date: Monday, December 18, 2006
Sheet 32 of 47


TOP VIEW
A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)
(BOTTOM VIEW)
GOLDEN FINGER FOR DEBUG BOARD
U76
FOX-GF30
ZZ.GF030.XXX
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46
U64
MX29LV800CBTC-GP
COVER SWITCH
POWER SWITCH
WIRELESS SWITCH
Put near board edge
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
FWH and Debug
Pamirs-Discrete
SA
Thursday, November 02, 2006
33
47

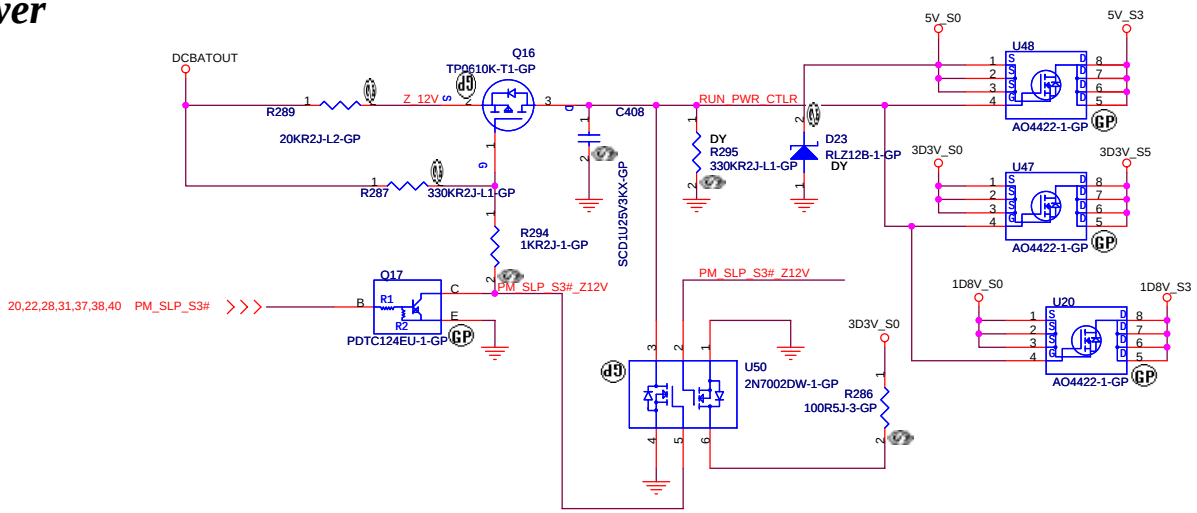
5V_AUX_S5 TO 5V_S5



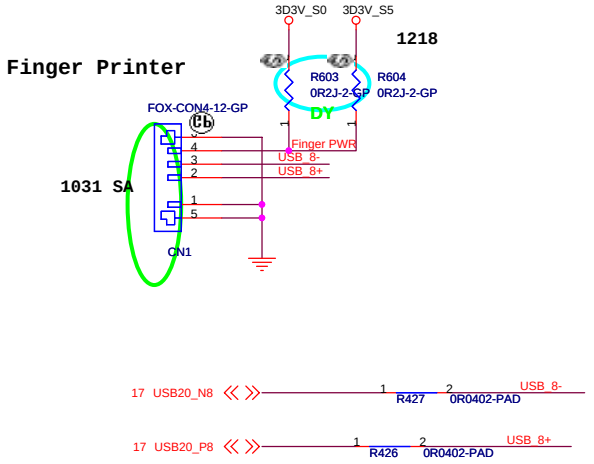
TPM 1.2



Run Power



Finger Printer



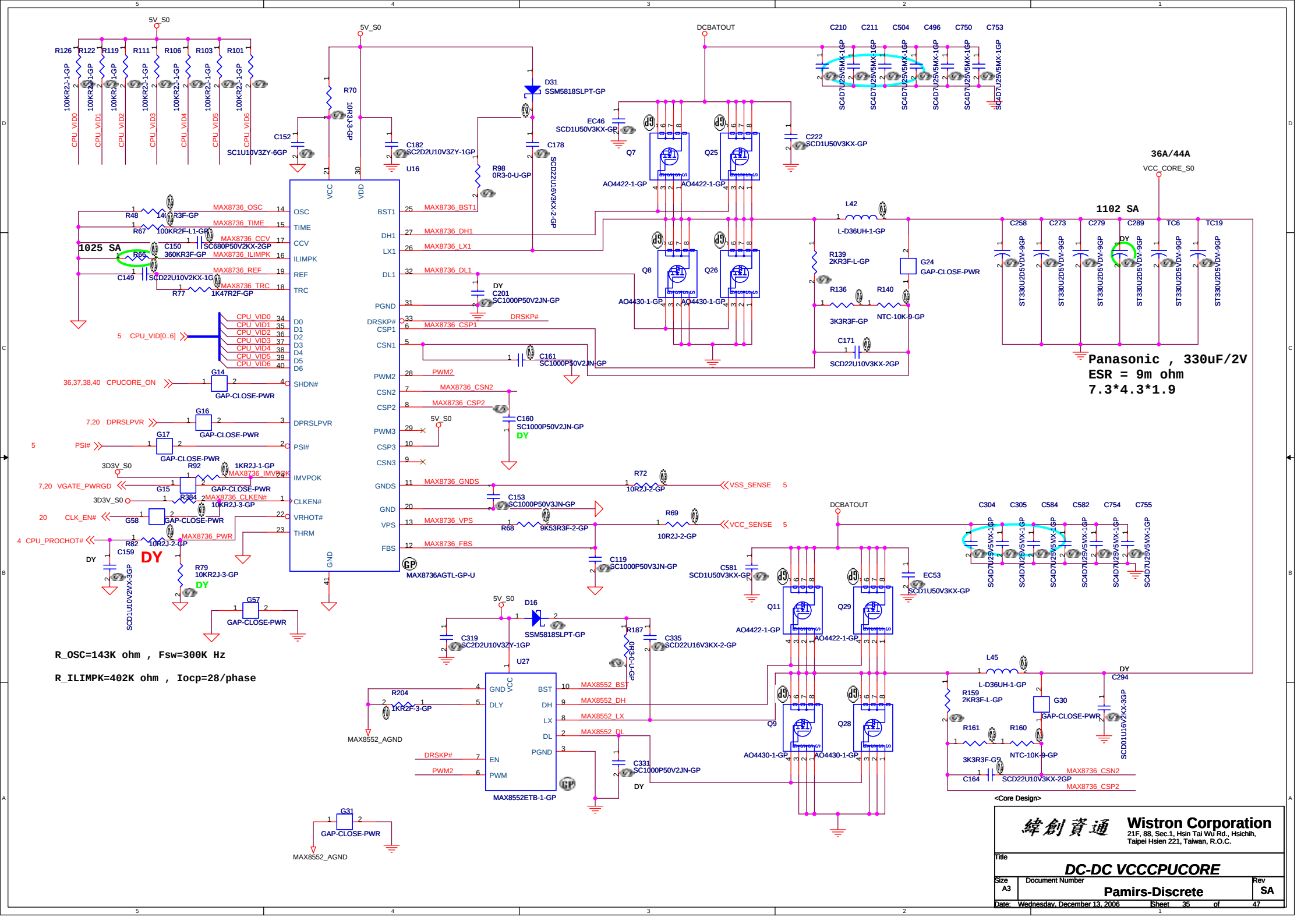
<Core Design>

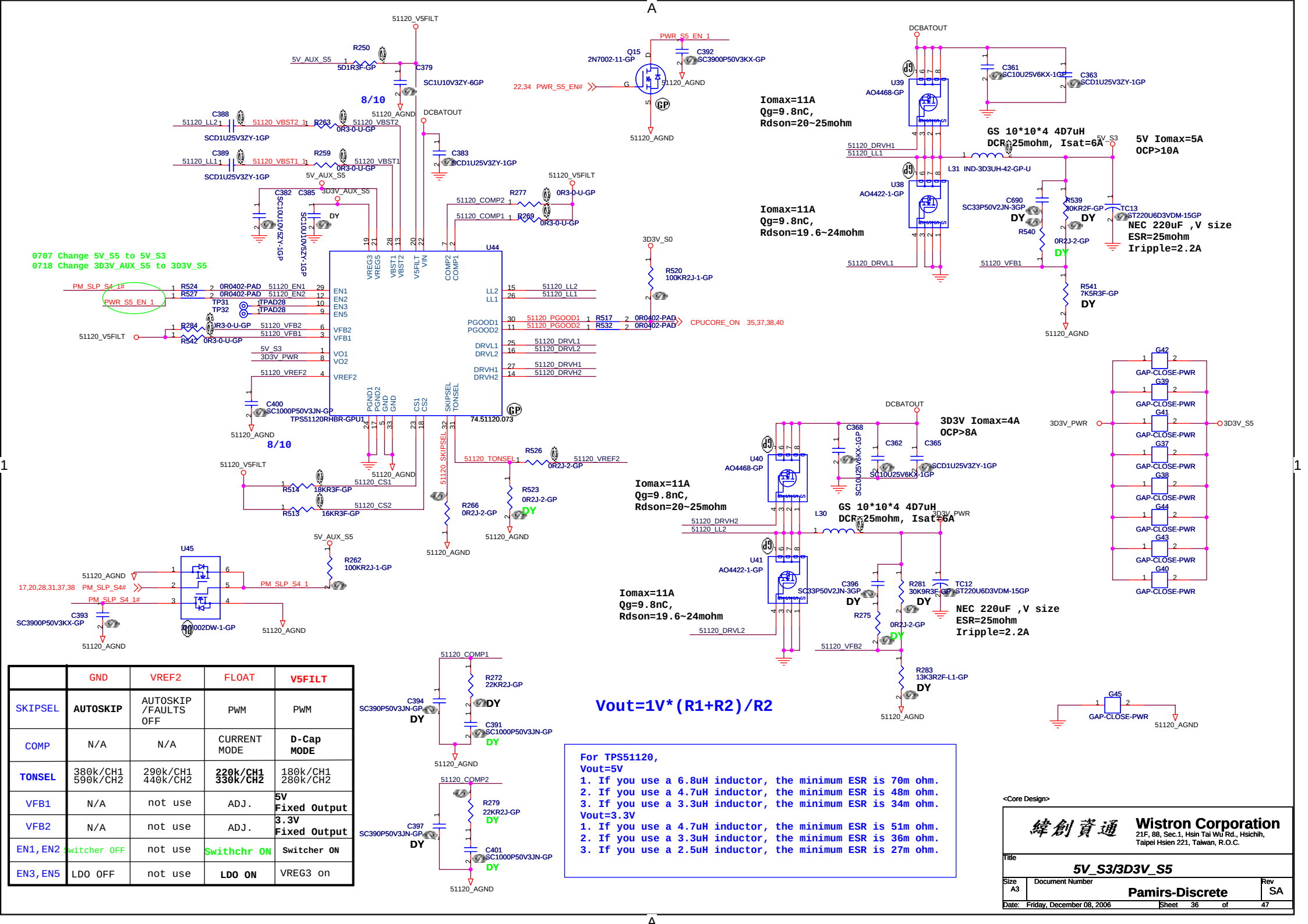
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PWRPLANE&RESETLOGIC***

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Monday, December 18, 2006 Sheet 34 of 47


1025 SA
1102 SA
36A/44A
DY
Panasonic , 330uF/2V
ESR = 9m ohm
7.3*4.3*1.9
R_OSC=143K ohm , Fsw=300K Hz
R_ILIMPK=402K ohm , Iocp=28/phase
MAX8736AGTL-GP-U
MAX8552ETB-1-GP
VCC_CORE_S0
DCBATOUT
5V_S0
3D3V_S0
MAX8552_AGND
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DC-DC VCCCPUCORE
Pamirs-Discrete
SA
Wednesday, December 13, 2006
Sheet 35 of 47



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V_S3/3D3V_S5

Size: A3 | Document Number: Pamirs-Discrete | Rev: SA

Date: Friday, December 08, 2006 | Sheet 36 of 47

Iocp=7.0 2 = 14A*
Rds,on=17m ohm
*Vcs1=Iocp*Rds,on=238mV*
VILIM=Vcs1/0.1=2.38V

*Iocp=7.0*2 = 14A*
Rds,on=17m ohm
*Vcs2=Iocp*Rds,on=28mV*
VILIM2=Vcs2/0.1=2.38V

1D8V / 7.0A
OCP>=14A

1D05V_S0/5A
OCP>=10A

5V_S5 R215 DUMMY-R2 5V_MAX8743_VCC
5V_S3 R217 0R3-0-U-GP

1D8V_S3 1D8V_PWR
G63 G62 G66 G65 G64 G67 G61 G68 GAP-CLOSE-PWR

DCBATOUT
C359 SC10U25V6KX-1GP EC72 SCD1U25V3ZY-1GP
U33 AO4468-GP
U34 AO4712-GP

NEC
Irms=7.5A(Isat=10.4A)
DCR=13mohm
12*12*5.5
1102 SA
L26
EC113 TC11 SE220U2D5VDM-3GP C339 SCD1U25V3ZY-1GP
DY
R224 8K2R3F-GP
Panasonic 220uF/2D5V
ESR=15m ohm
Iripple=2.7 A

Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

Voutsetting=1.820V
R225 9K53R2F-GP

5V_MAX8743_VCC
C341 SCD1U10V2MX-3GP
C340 SC1U10V3ZY-8GP
C353 SCD1U10V2MX-3GP
C349 SC1U25V5ZY-4GP
R218
D17 BAW56-3-GP
MAX8743_BST2
MAX8743_VCC
R429 R212
C350 SC1U10V3ZY-6GP
R221 0R3-0-U-GP
R432 90K9R3F-GP
C352 SCD1U25V3ZY-1GP
R208 90K9R3F-GP
R456 0R3-0-U-GP
C338 SCD1U25V3ZY-1GP
MAX8743_ILIM1
MAX8743_BST1R
MAX8743_DH1
MAX8743_LX1
MAX8743_DL1
MAX8743_ILIM2
MAX8743_BST2R
MAX8743_DH2
MAX8743_LX2
MAX8743_DL2
MAX8743_ON1
MAX8743_TON
MAX8743_VREF
MAX8743_ON2
MAX8743_PGOOD
MAX8743_FB1
MAX8743_FB2
U29
UVP VCC VDD V+ ILIM2 BST2 DH2 LX2 DL2 OUT2 FB2 ON2 PGOOD OVP
ILIM1 BST1 DH1 LX1 DL1 CS1 OUT1 FB1 ON1 TON REF SKIP# GND CS2
MAX8743EEI-1-GP
74.08743.A79

DCBATOUT
U37 AO4468-GP
U36 AO4712-GP
EC77 SCD1U25V3ZY-1GP
C358 SC10U25V6KX-1GP
C356 SC10U25V6KX-1GP
NEC
Irms=7.5A(Isat=10.4A)
DCR=13mohm
12*12*5.5
L27
TC10 SE220U2VDM-8GP
DY C336 SCD1U25V3ZY-1GP
Panasonic 220uF/2V
ESR=15m ohm
Iripple=2.7 A
1D05V_PWR 1D05V_S0
G34 G32 G33 G36 G35 GAP-CLOSE-PWR
10KR2F-2-GP R205
R207 100KR3F-GP
Voutsetting=1.0511V

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

Vout=Vfb*(1+(R1/R2))
Where Vfb=1.0V,R2=10Kohm

C589 SCD47U10V3KX-3GP
C590 DY SCD1U25V3ZY-1GP

17,20,28,31,36,38 PM_SLP_S4# R213 5K1R2-GP MAX8743_ON1
20,22,28,31,34,38,40 PM_SLP_S3# R210 5K1R2-GP MAX8743_ON2
C346 DY SCD1U10V2MX-3GP
C591 DY SCD1U10V2MX-3GP

5V_MAX8743_VCC
R434 DY 0R2J-2-GP
MAX8743_VREF
R433 DUMMY-R2
R440 DUMMY-R2

0205
PM_SLP_S3# R211 220KR2J-L2-GP
PM_SLP_S4# DY R214 220KR2J-L2-GP
MAX8743_SKIP#
C344 SC1000P50V3JN-GP DY
R216 0R2J-2-GP

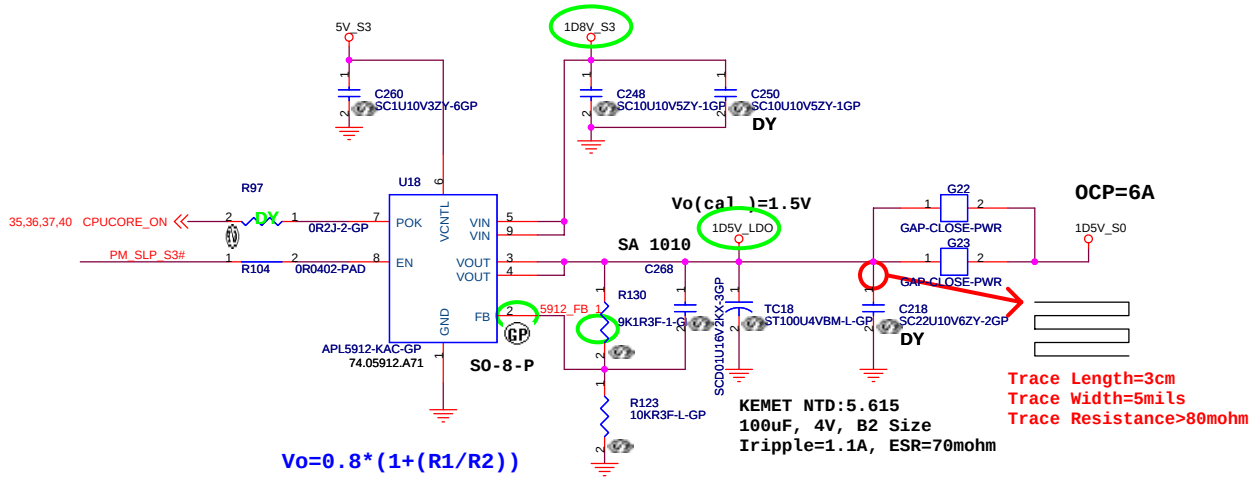
CPUCORE_ON 35,36,38,40
R441 0R0402-PAD

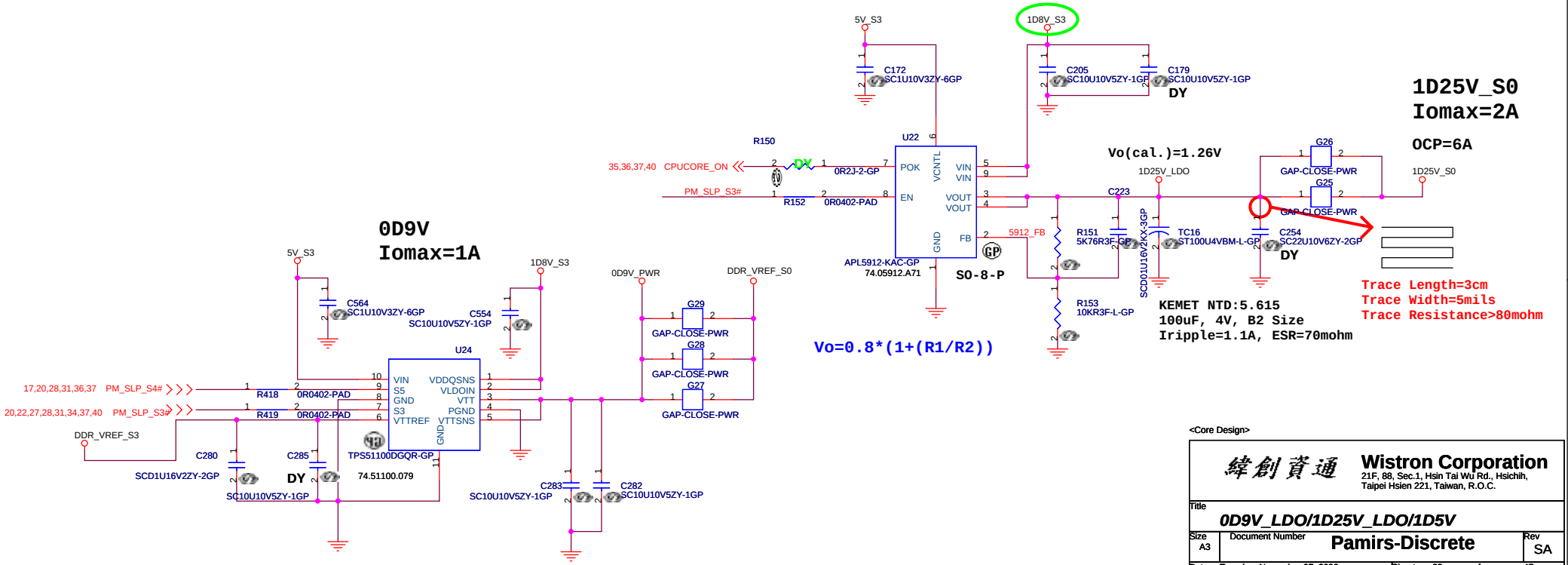
Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *1D8V_S3/1D05V_S0*
Size: A3 | Document Number: **Pamirs-Discrete** | Rev: SA
Date: Monday, December 18, 2006 | Sheet 37 of 47





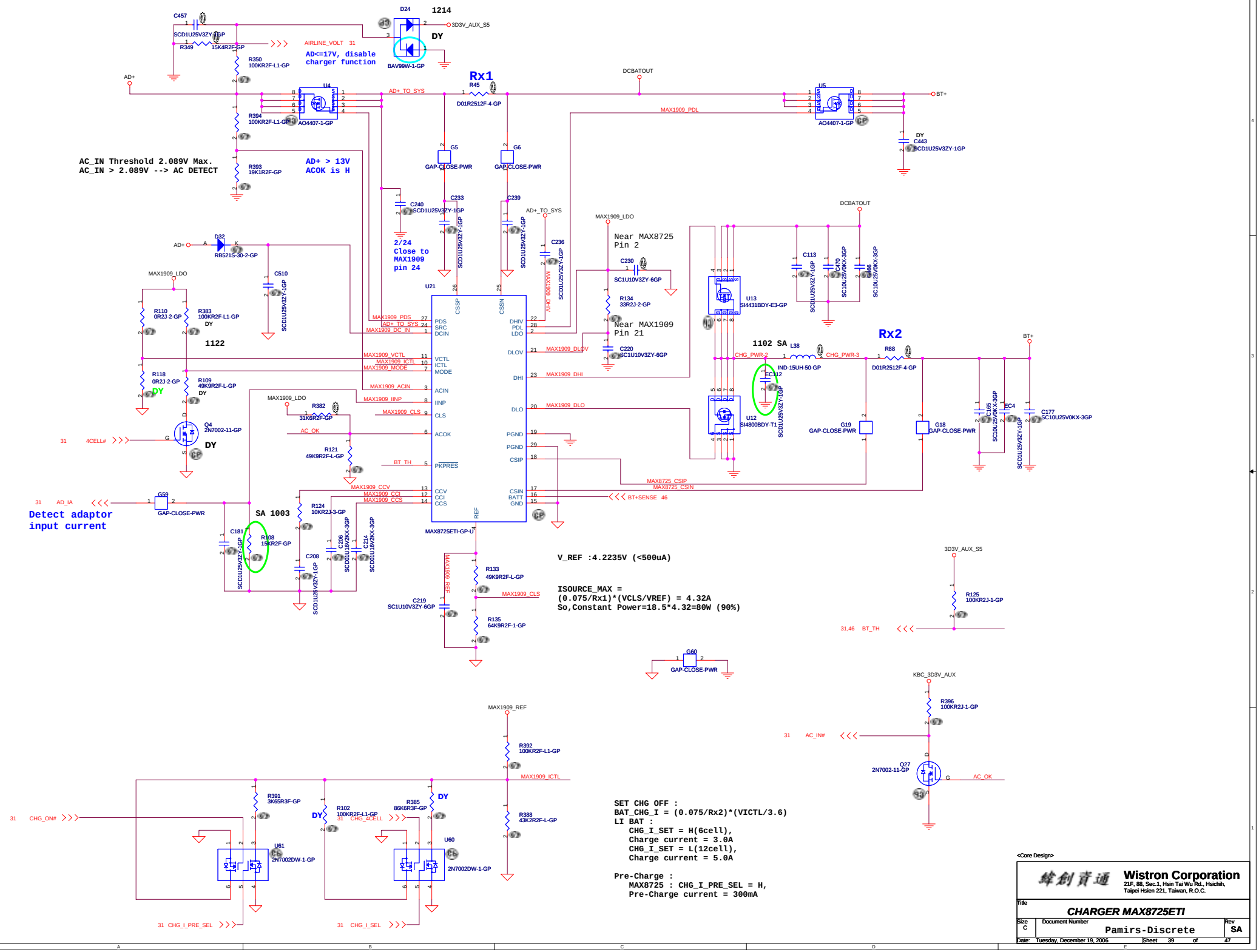
<Core Design>

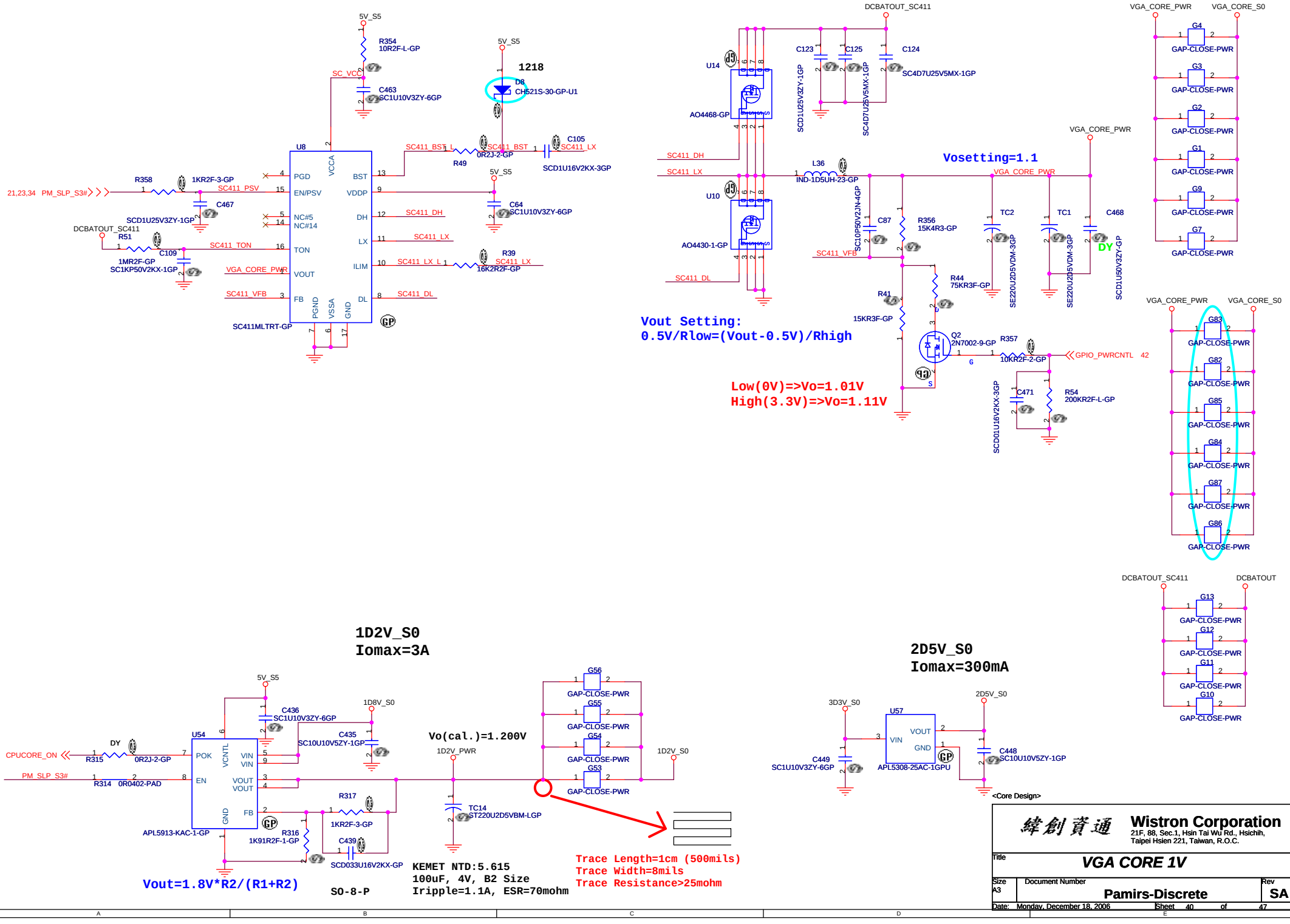
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D9V_LDO/1D25V_LDO/1D5V

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Tuesday, November 07, 2006 Sheet 38 of 47

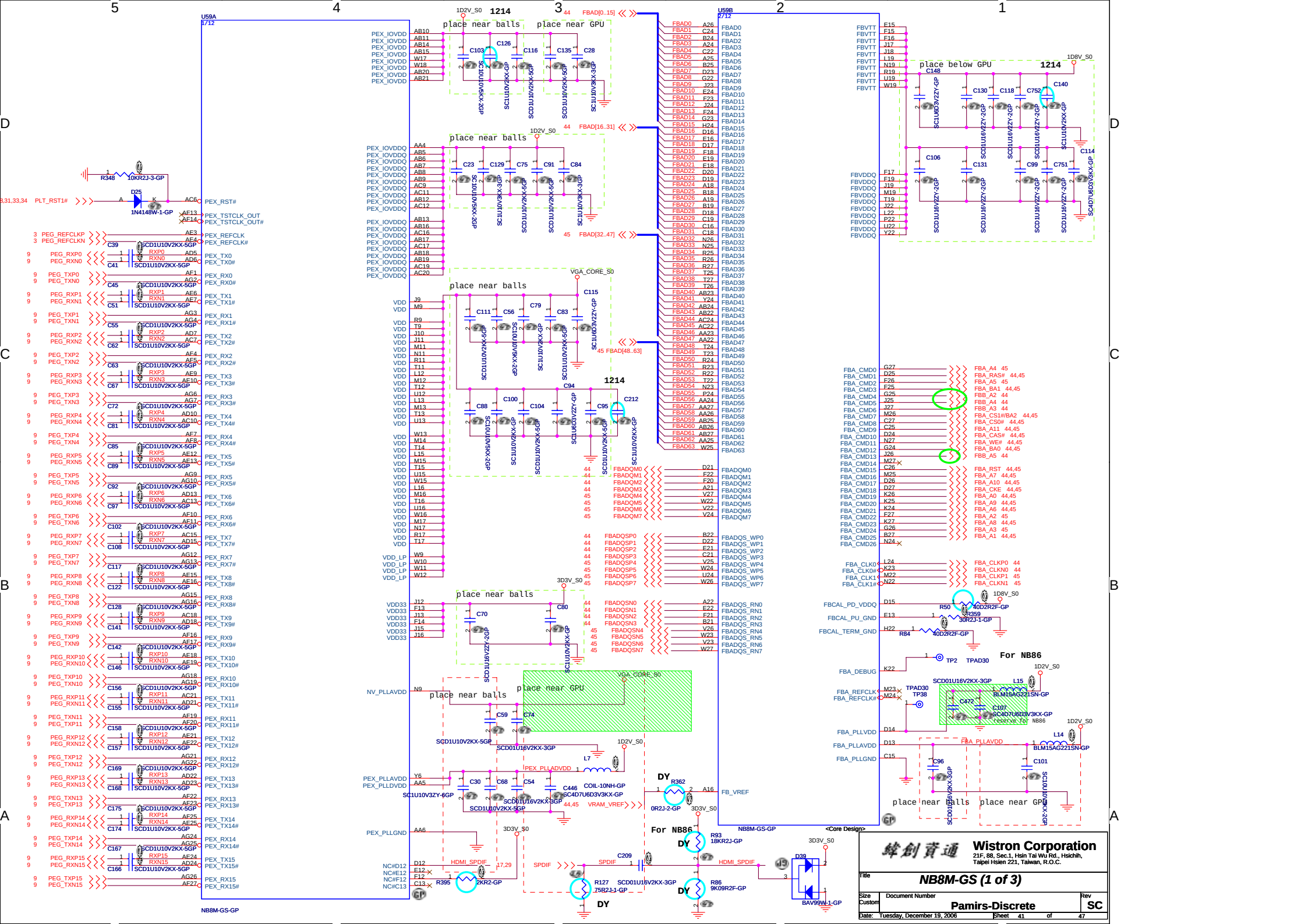

AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
AD+ > 13V
ACOK is H
AD<=17V, disable
charger function
Rx1
Rx2
1214
DY
2/24
Close to
MAX1909
pin 24
Near MAX8725
Pin 2
Near MAX1909
Pin 21
1122
1102 SA
SA 1003
Detect adaptor
input current
V_REF :4.2235V (<500uA)
ISOURCE_MAX =
(0.075/Rx1)*(VCLS/VREF) = 4.32A
So,Constant Power=18.5*4.32=80W (90%)
SET CHG OFF :
BAT_CHG_I = (0.075/Rx2)*(VICTL/3.6)
LI BAT :
CHG_I_SET = H(6cell),
Charge current = 3.0A
CHG_I_SET = L(12cell),
Charge current = 5.0A
Pre-Charge :
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 300mA
MAX8725ETI-GP-U
AO4407-1-GP
D01R2512F-4-GP
IND-15UH-50-GP
SI4431BDY-E3-GP
SI4800BDY-T1
2N7002-11-GP
2N7002DW-1-GP
RB521S-30-2-GP
BAV99W-1-GP
GAP-CLOSE-PWR
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8725ETI
Pamirs-Discrete
Tuesday, December 19, 2006
Sheet 39 of 47

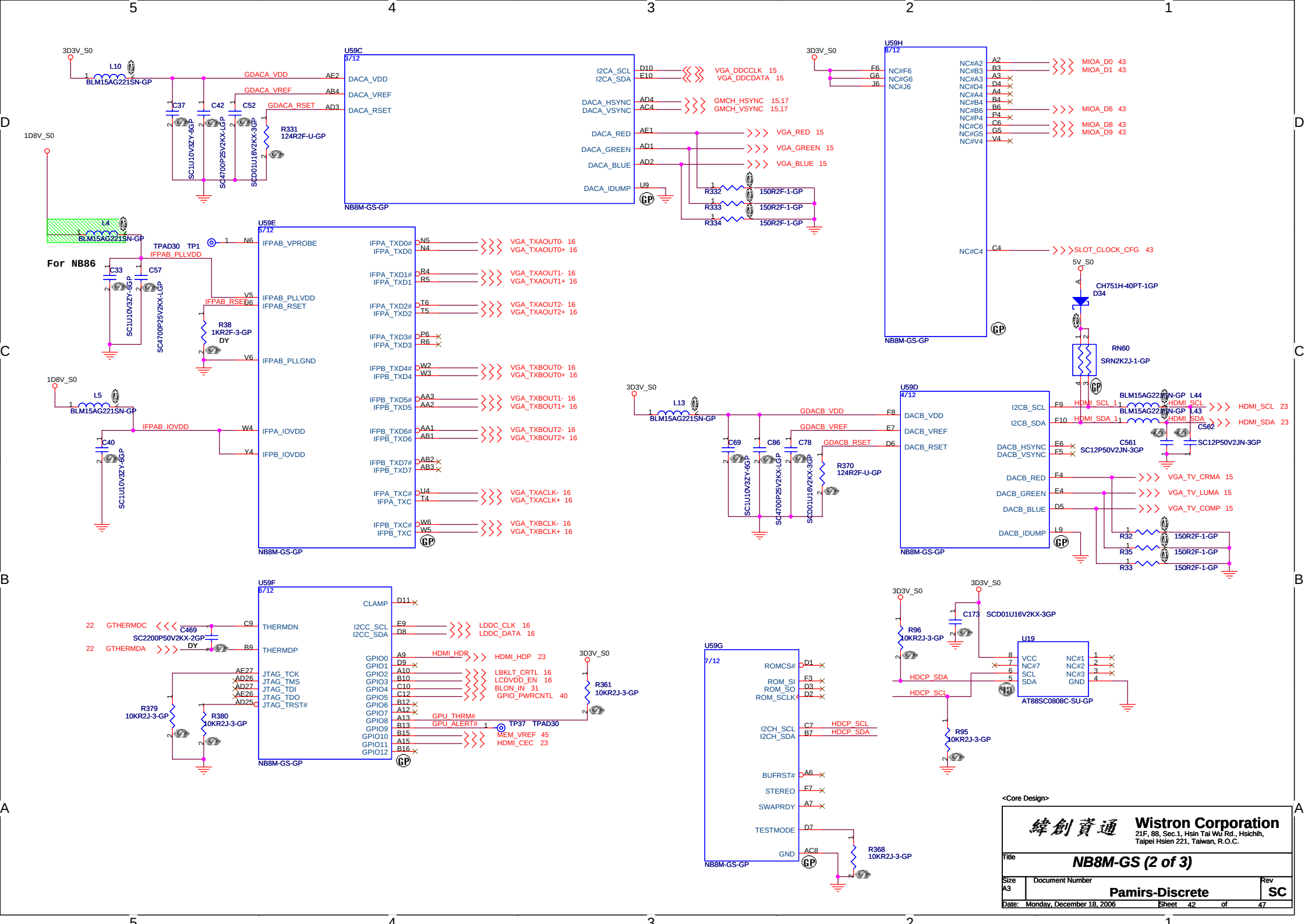


<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**VGA CORE 1V**	
Size A3	Document Number **Pamirs-Discrete**	Rev **SA**
Date: Monday, December 18, 2006	Sheet 40 of 47	


U59A
1/12
U59B
2/12
NB8M-GS-GP
<Core Design>
place near balls
place near GPU
place below GPU
VGA_CORE_S0
1D2V_S0
3D3V_S0
1D8V_S0
For NB86
reserve for NB86
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB8M-GS (1 of 3)
Size
Custom
Document Number
Pamirs-Discrete
Rev
SC
Date: Tuesday, December 19, 2006
Sheet 41 of 47



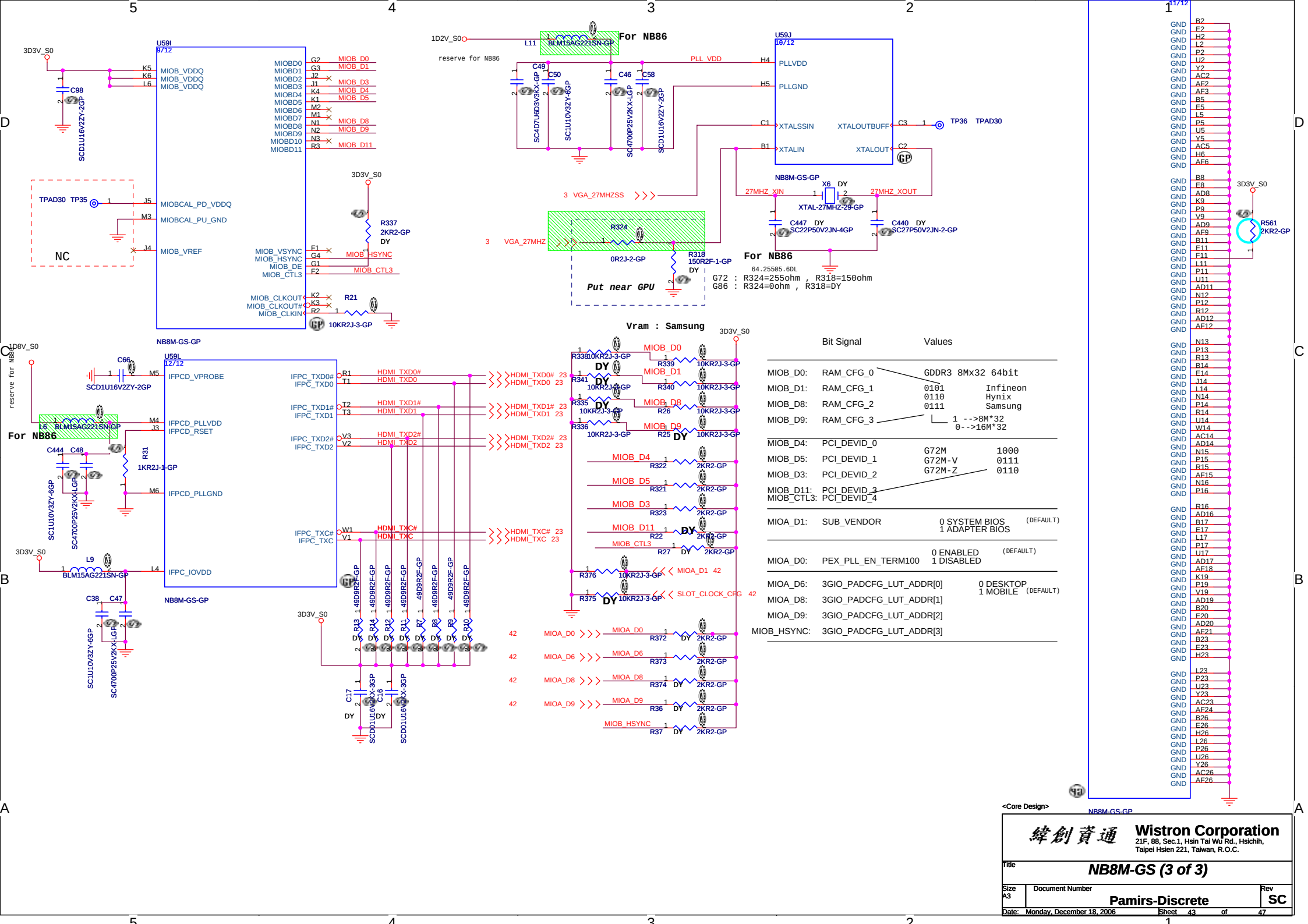
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **NB8M-GS (2 of 3)**

Size	Document Number	Rev
A3	Pamirs-Discrete	SC

Date: Monday, December 18, 2006 Sheet 42 of 47


U59I 9/12
MIOB_VDDQ
MIOB_VDDQ
MIOB_VDDQ
MIOBD0
MIOBD1
MIOBD2
MIOBD3
MIOBD4
MIOBD5
MIOBD6
MIOBD7
MIOBD8
MIOBD9
MIOBD10
MIOBD11
MIOB_D0
MIOB_D1
MIOB_D3
MIOB_D4
MIOB_D5
MIOB_D8
MIOB_D9
MIOB_D11
3D3V_S0
C98
SCD1U16V2ZY-2GP
TPAD30 TP35
NC
MIOBCAL_PD_VDDQ
MIOBCAL_PU_GND
MIOB_VREF
MIOB_VSYNC
MIOB_HSYNC
MIOB_DE
MIOB_CTL3
MIOB_HSYNC
MIOB_CTL3
R337
2KR2-GP
DY
MIOB_CLKOUT
MIOB_CLKOUT#
MIOB_CLKIN
R21
10KR2J-3-GP
1D2V_S0
L11
BLM15AG221SN-GP
For NB86
reserve for NB86
C49
C50
C46
C58
SC4D7U6D3V3KX-GP
SC1U10V3ZY-6GP
SC4700P25V2KX-LGP
SCD1U16V2ZY-2GP
PLL_VDD
U59J 10/12
PLLVDD
PLLGND
XTALSSIN
XTALIN
XTALOUTBUFF
XTALOUT
C1
B1
C3
C2
TP36 TPAD30
3 VGA_27MHZSS
3 VGA_27MHZ
R324
0R2J-2-GP
R318
150R2F-1-GP
DY
Put near GPU
NB8M-GS-GP
27MHZ_XIN
27MHZ_XOUT
X6 DY
XTAL-27MHZ-29-GP
C447 DY
SC22P50V2JN-4GP
C440 DY
SC27P50V2JN-2-GP
For NB86
64.25505.6DL
G72 : R324=255ohm , R318=150ohm
G86 : R324=0ohm , R318=DY
11/12
GND
3D3V_S0
R561
2KR2-GP
Vram : Samsung
R338 10KR2J-3-GP
R339 10KR2J-3-GP
R341 10KR2J-3-GP
R340 10KR2J-3-GP
R335 10KR2J-3-GP
R26 10KR2J-3-GP
R336 10KR2J-3-GP
R25 10KR2J-3-GP
MIOB_D0
MIOB_D1
MIOB_D8
MIOB_D9
MIOB_D4
MIOB_D5
MIOB_D3
MIOB_D11
MIOB_CTL3
R322 2KR2-GP
R321 2KR2-GP
R323 2KR2-GP
R22 2KR2-GP
R27 DY 2KR2-GP
R376 10KR2J-3-GP
R375 10KR2J-3-GP
MIOA_D1 42
SLOT_CLOCK_CFG 42
Bit Signal Values
MIOB_D0: RAM_CFG_0 GDDR3 8Mx32 64bit
MIOB_D1: RAM_CFG_1 0101 Infineon
0110 Hynix
MIOB_D8: RAM_CFG_2 0111 Samsung
MIOB_D9: RAM_CFG_3 1 -->8M*32
0-->16M*32
MIOB_D4: PCI_DEVID_0
MIOB_D5: PCI_DEVID_1 G72M 1000
MIOB_D3: PCI_DEVID_2 G72M-V 0111
MIOB_D11: PCI_DEVID_3 G72M-Z 0110
MIOB_CTL3: PCI_DEVID_4
MIOA_D1: SUB_VENDOR 0 SYSTEM BIOS (DEFAULT)
1 ADAPTER BIOS
MIOA_D0: PEX_PLL_EN_TERM100 0 ENABLED (DEFAULT)
1 DISABLED
MIOA_D6: 3GIO_PADCFG_LUT_ADDR[0] 0 DESKTOP
1 MOBILE (DEFAULT)
MIOA_D8: 3GIO_PADCFG_LUT_ADDR[1]
MIOA_D9: 3GIO_PADCFG_LUT_ADDR[2]
MIOB_HSYNC: 3GIO_PADCFG_LUT_ADDR[3]
U59L 12/12
IFPCD_VPROBE
IFPCD_PLLVDD
IFPCD_RSET
IFPCD_PLLGND
IFPC_IOVDD
SCD1U16V2ZY-2GP
L6 BLM15AG221SN-GP
For NB86
1KR2J-1-GP
C444 C48
C38 C47
L9 BLM15AG221SN-GP
IFPC_TXD0#
IFPC_TXD0
IFPC_TXD1#
IFPC_TXD1
IFPC_TXD2#
IFPC_TXD2
IFPC_TXC#
IFPC_TXC
HDMI_TXD0#
HDMI_TXD0
HDMI_TXD1#
HDMI_TXD1
HDMI_TXD2#
HDMI_TXD2
HDMI_TXC#
HDMI_TXC
HDMI_TXD0# 23
HDMI_TXD0 23
HDMI_TXD1# 23
HDMI_TXD1 23
HDMI_TXD2# 23
HDMI_TXD2 23
HDMI_TXC# 23
HDMI_TXC 23
49D9R2F-GP
R13 R14 R12 R11 R7 R8 R9 R10
C17 C16
SCD01U16V2KX-3GP
MIOA_D0
MIOA_D6
MIOA_D8
MIOA_D9
MIOB_HSYNC
R372 DY 2KR2-GP
R373 2KR2-GP
R374 DY 2KR2-GP
R36 DY 2KR2-GP
R37 DY 2KR2-GP
42
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NB8M-GS-GP
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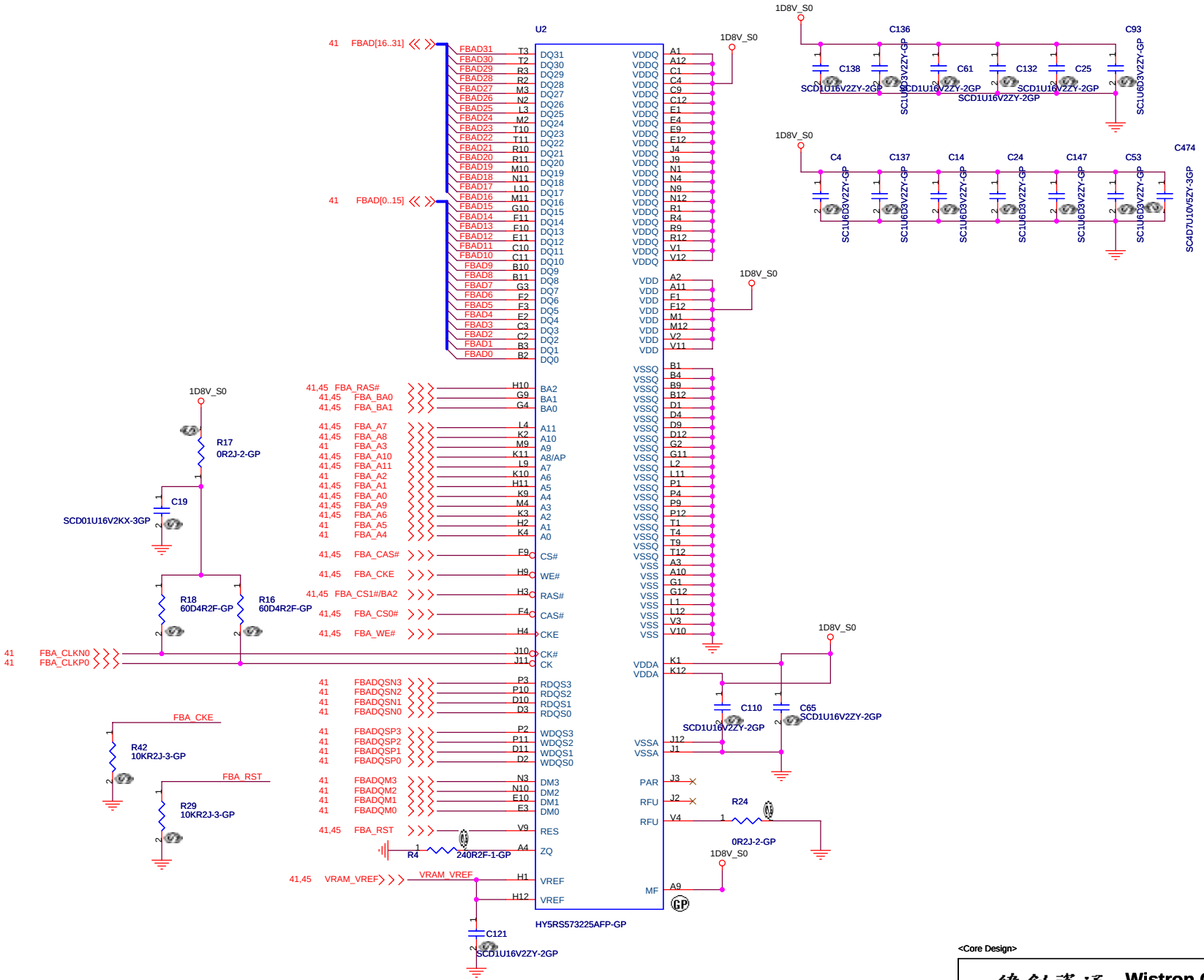
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB8M-GS (3 of 3)
Size A3
Document Number
Pamirs-Discrete
Rev SC
Date: Monday, December 18, 2006
Sheet 43 of 47



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Title: VRAM1

Size: A3 | Document Number: Pamirs-Discrete | Rev: SC

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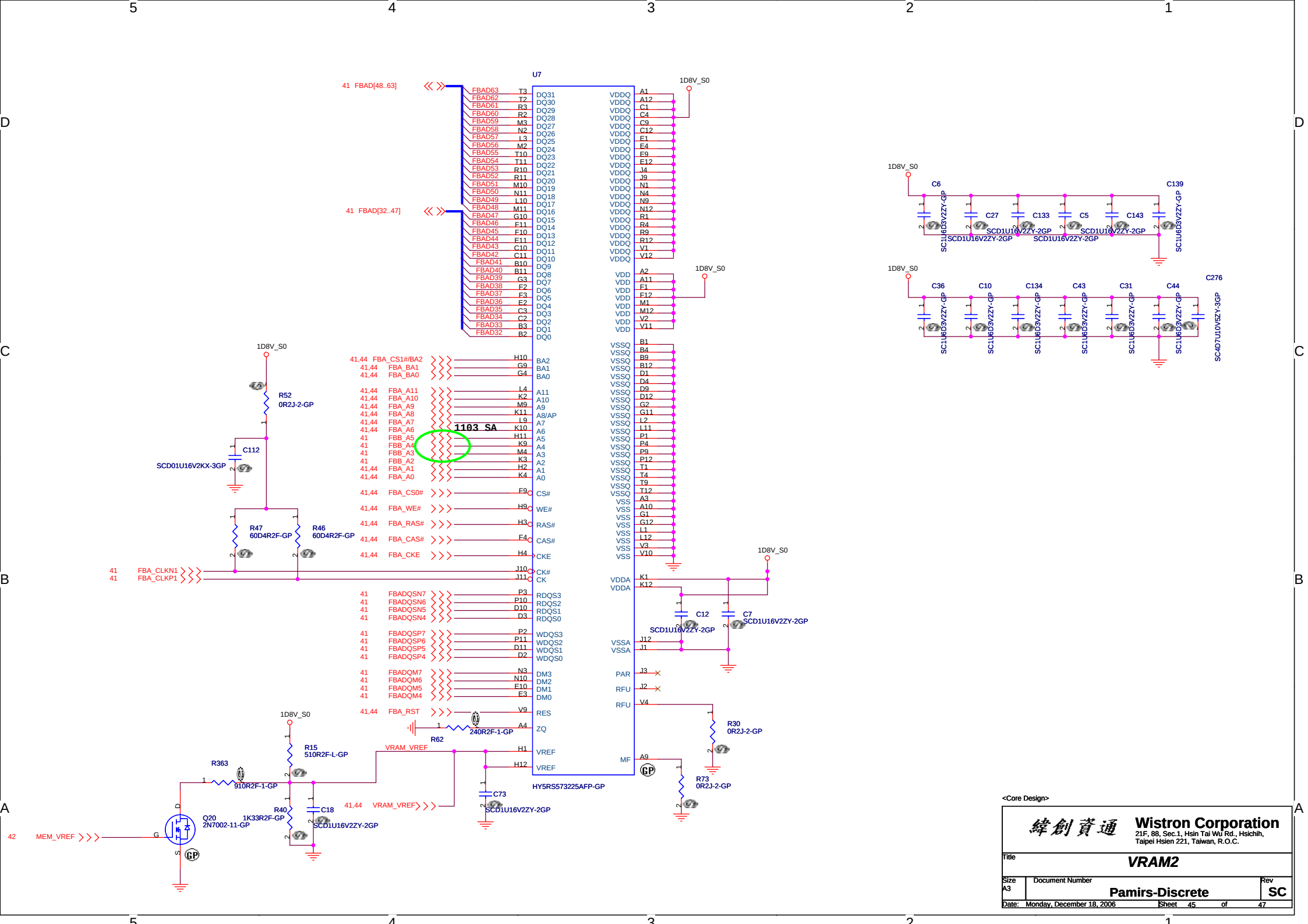
U7
HY5RS573225AFP-GP
1103 SA
1D8V_S0
R52
0R2J-2-GP
C112
SCD01U16V2KX-3GP
R47
60D4R2F-GP
R46
60D4R2F-GP
R62
240R2F-1-GP
R15
510R2F-L-GP
R363
910R2F-1-GP
R40
1K33R2F-GP
C18
SCD1U16V2ZY-2GP
Q20
2N7002-11-GP
C73
SCD1U16V2ZY-2GP
C12
C7
SCD1U16V2ZY-2GP
R30
0R2J-2-GP
R73
0R2J-2-GP
C6
C139
C27
C133
C5
C143
SC1U6D3V2ZY-GP
SCD1U16V2ZY-2GP
C36
C10
C134
C43
C31
C44
C276
SC4D7U10V5ZY-3GP
VRAM_VREF
MEM_VREF
FBA_CLKN1
FBA_CLKP1
FBA_CKE
FBA_CAS#
FBA_RAS#
FBA_WE#
FBA_CS0#
FBA_RST
FBA_CS1#/BA2
FBA_BA1
FBA_BA0
FBA_A11
FBA_A10
FBA_A9
FBA_A8
FBA_A7
FBA_A6
FBB_A5
FBB_A4
FBB_A3
FBB_A2
FBA_A1
FBA_A0
FBADQSN7
FBADQSN6
FBADQSN5
FBADQSN4
FBADQSP7
FBADQSP6
FBADQSP5
FBADQSP4
FBADQM7
FBADQM6
FBADQM5
FBADQM4
FBAD[48..63]
FBAD[32..47]
<Core Design>
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Title
VRAM2
Size
A3
Document Number
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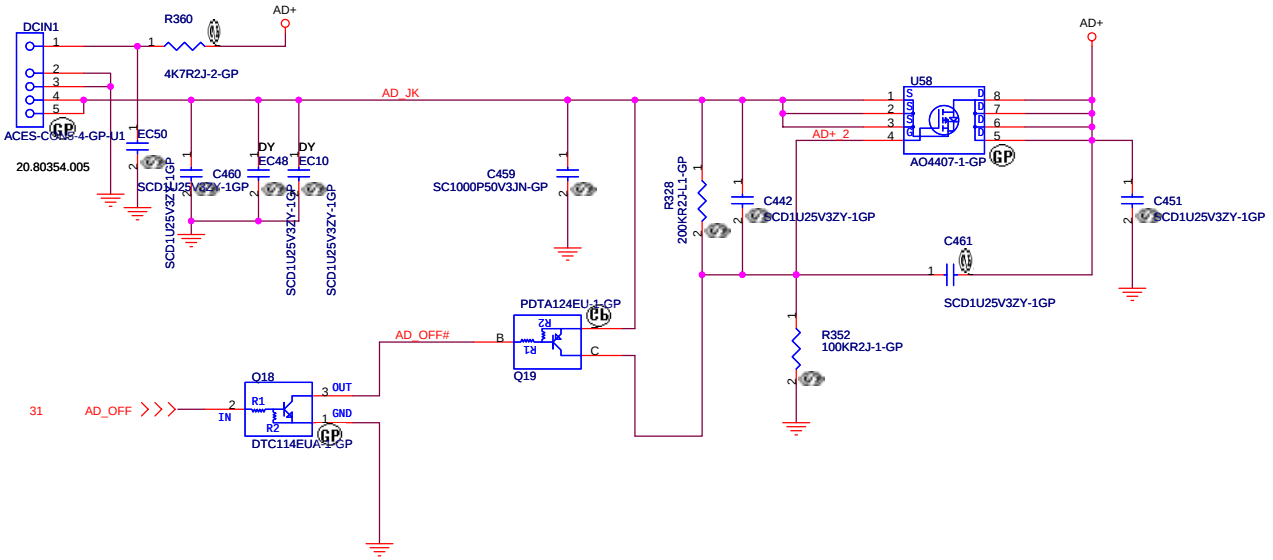
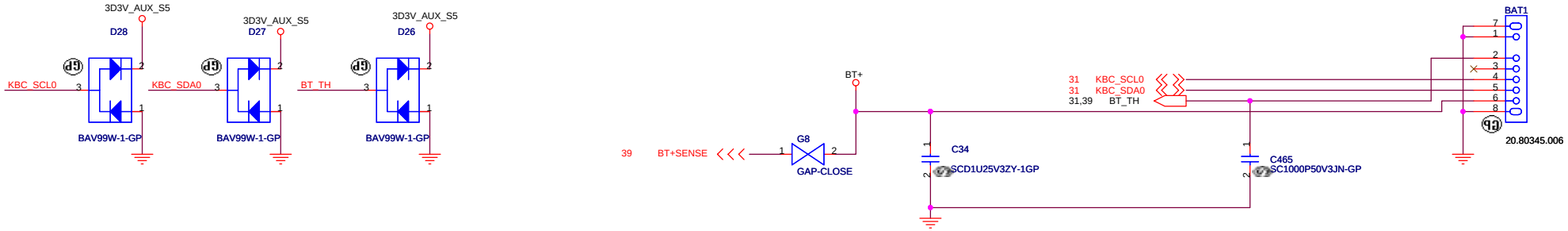
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title: **AD/BATT CONN**

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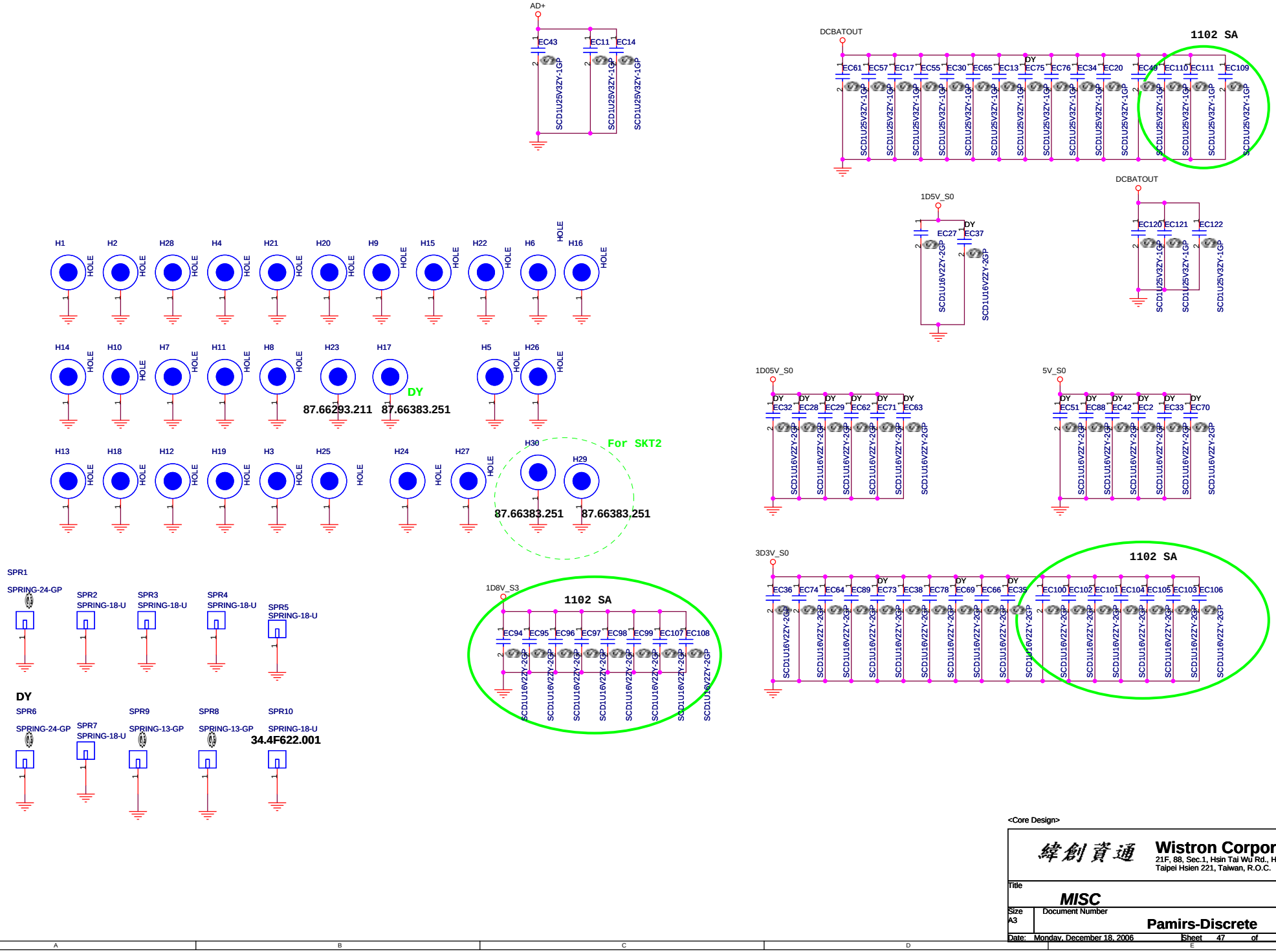

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Title: ***MISC***

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