Leopard2 Block Diagram

Project code: 91.4C701.001
PCB P/N : 48.4C701.011
REVISION : 05202 -1

CLK GEN 3
ICS954206

4,5 Mobile CPU
Dothan

Host BUS
400/533MHz

6,7,8,9,10 Alviso

DMI I/F
100MHz

21,22,23,24 ICH6-M

DDRII*2 11,12

DDR-SDRAM 16,17
HY5DS573222F-28

13,14,15 VGA
ATI M26P

PEG

LVDS → LCD 19

SVIDEO/COMP → TVOUT 18

RGB CRT → CRT

DAUGHTER BOARD

BLUE THUMB

USB 2.0 → USB x 2
USB x 2 35

P EIDE → HDD 26

S EIDE → DVD/ CD-RW 26

PCI EXPRESS/ USB2.0 → EXPRESSCARD 26

LPC Bus

1394 Conn 31

PCMCIA 1 SLOT 29

Power Switch 28
TPS2220A

SD/MS 6 in 1 Card Slost 29

27,28 PCI 7411
CARDBUS
1394
SD/MS/MMC/SM

Mini-PCI 34
802.11a/b/g

RJ45 CONN 31

10/100 RTL8100C 30,31

PCI BUS

RJ11 CONN 31

MODEM 35
MDC Card

AC97-LINK

MIC IN 18

AC'97 CODEC 31
AD1981B

LINE OUT

OP AMP 33
G1420B

DAUGHTER BOARD

Docking 18

KBC 36
NS97551

LPC Debug Conn 38

Power Switch 26
TPS2231

Comsumer IR 35

Touch Pad 37

Int. KB 37

Thermal & Fan 25
G768D

FlashRom 38
4Mb
(512kB)

SYSTEM DC/DC TPS5130 (42)	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 5V_S3 3V_AUX

SYSTEM DC/DC MAX8743 (45)	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_VGA_S0

MAXIM CHARGER MAX8725 (40)	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC MAX1907 (41)	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4
L7: GND
L8: Signal 5

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A3 | Document Number: Leopard2 | Rev: -1
Date: Monday, July 11, 2005 | Sheet 1 of 47

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
5V_S3= 5 Voltage suspend to RAM(S3 state)
5V_S5= 5 Voltage soft off(S5 state)
3D3V_S0= 3.3 Voltage power up on system work(S0 state)
3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
3D3V_S5= 3.3 Voltage soft off(S5 state)
LVDDR_2D8V= 2.8 Voltage power up on system work(S0 state)
1D8V_S3= 1.8 Voltage suspend to RAM(S3 state)
2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S5= 1.5 Voltage soft off(S5 state)
DDR_VREF= 0.9 Voltage power up on system work(S0 state)
1D2V_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
VRAM_VDDQ= 1.8 Voltage power up on system work(S0 state) for VRAM
1D05V_S0= 1.05 Voltage power up on system work(S0 state)
CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0#/GNT0#
Cardbus Controller TI7411	AD22	(CARBUS)P_INTG# (1394)P_INTF# (CARD READER)P_INTG#	REQ1#/GNT1#
LAN	AD23	P_INTE#	REQ2#/GNT2#
Blue Thumb	AD24		

<Core Design>

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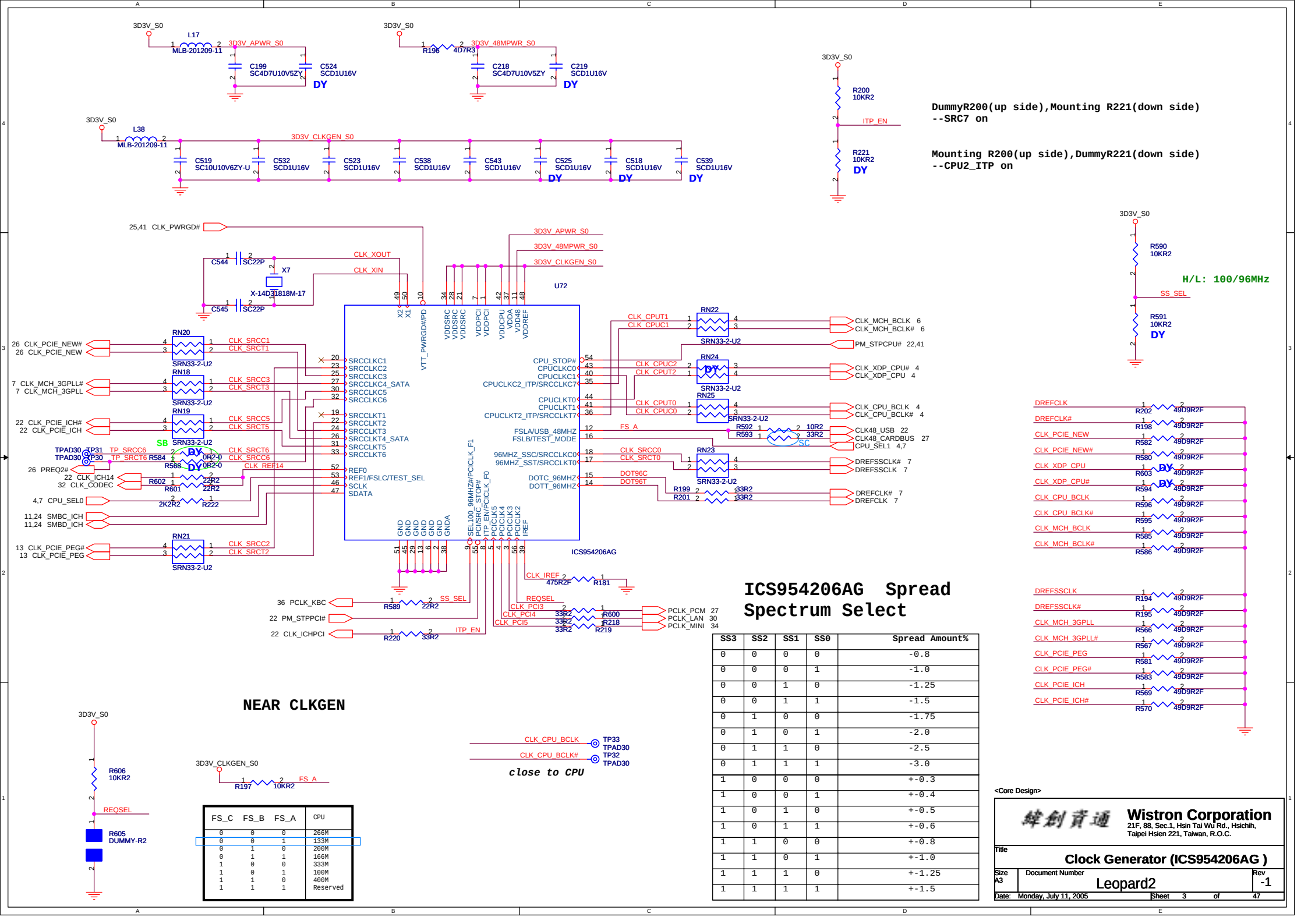
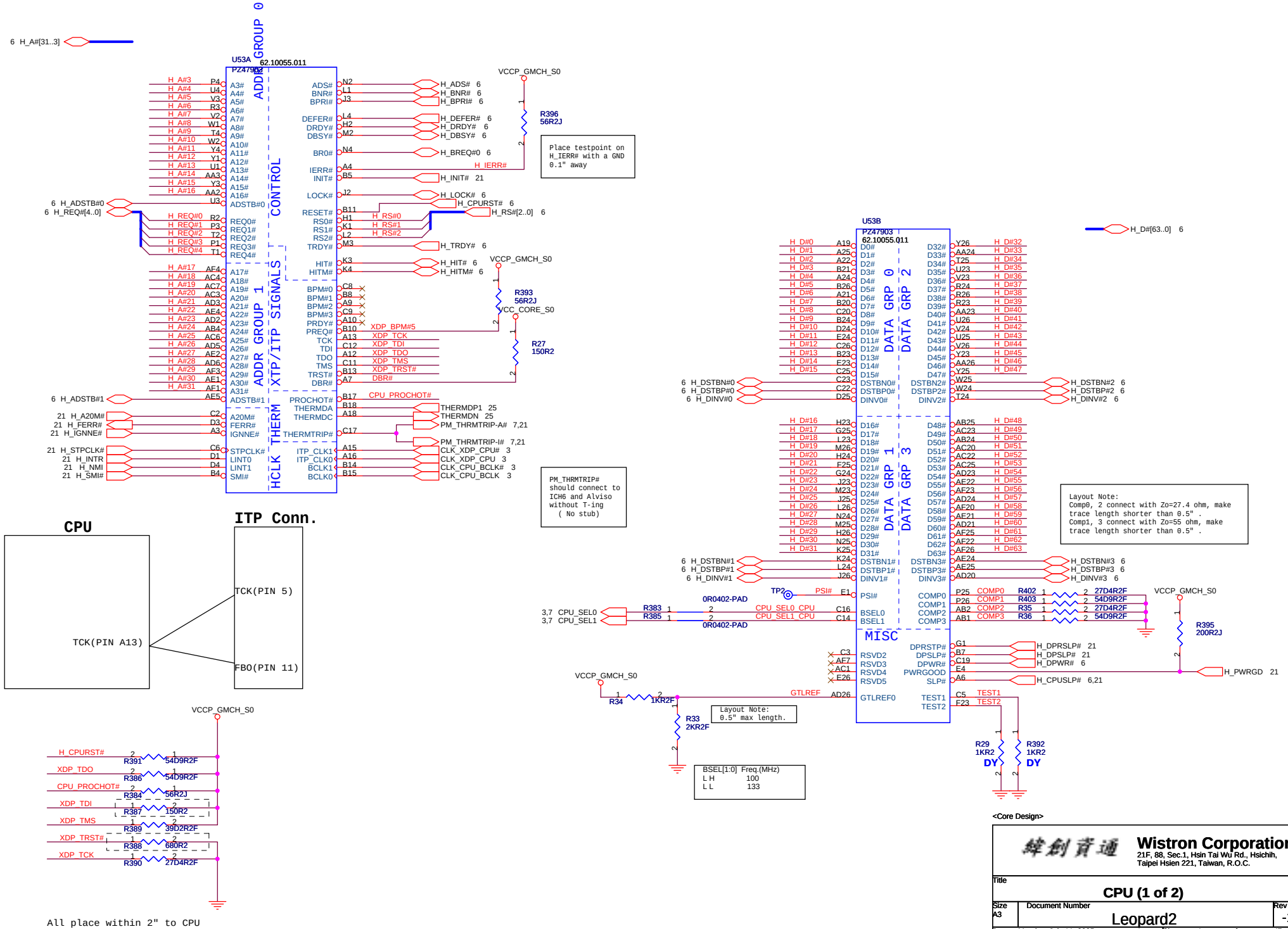
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

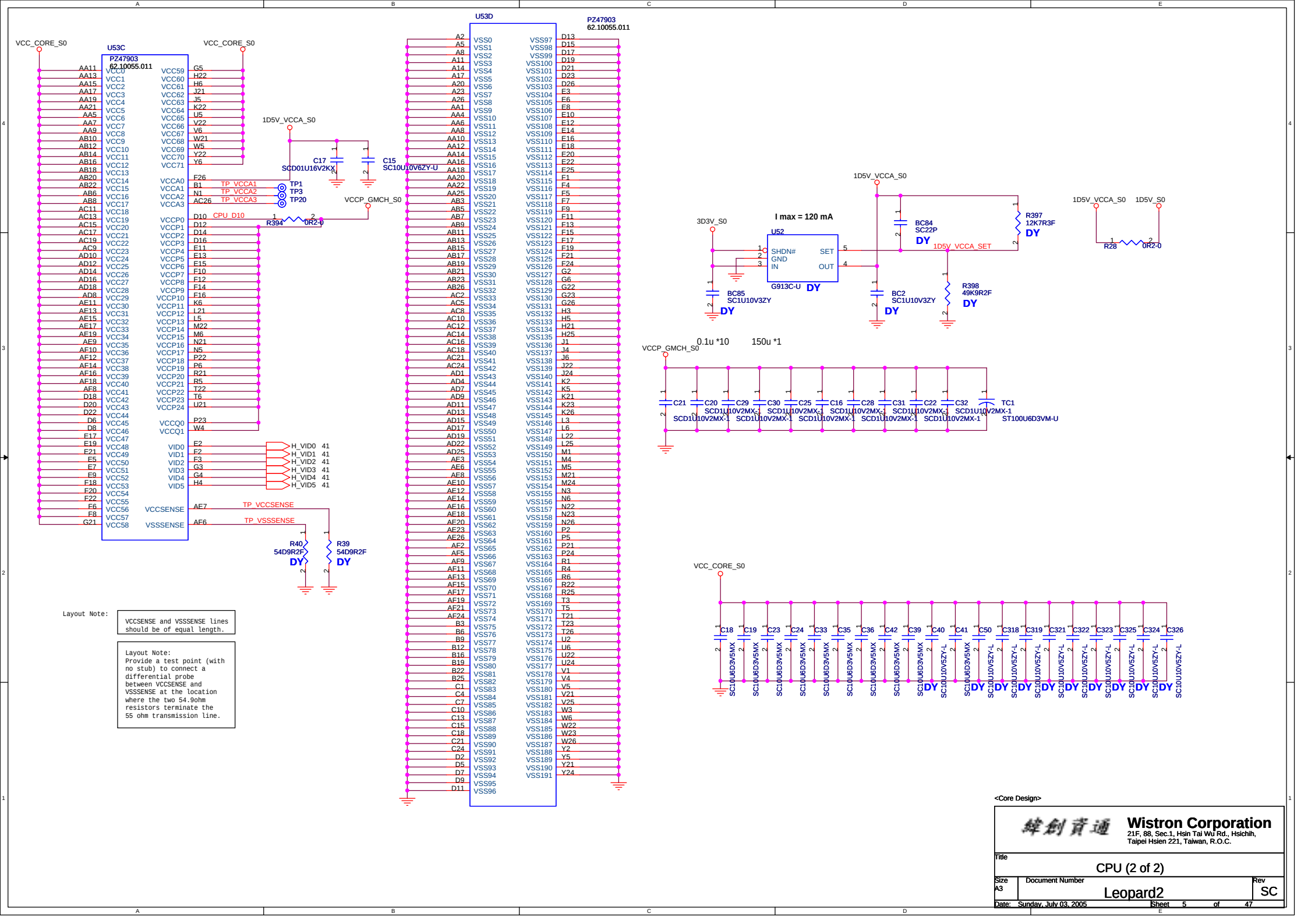
Title: *ITP*

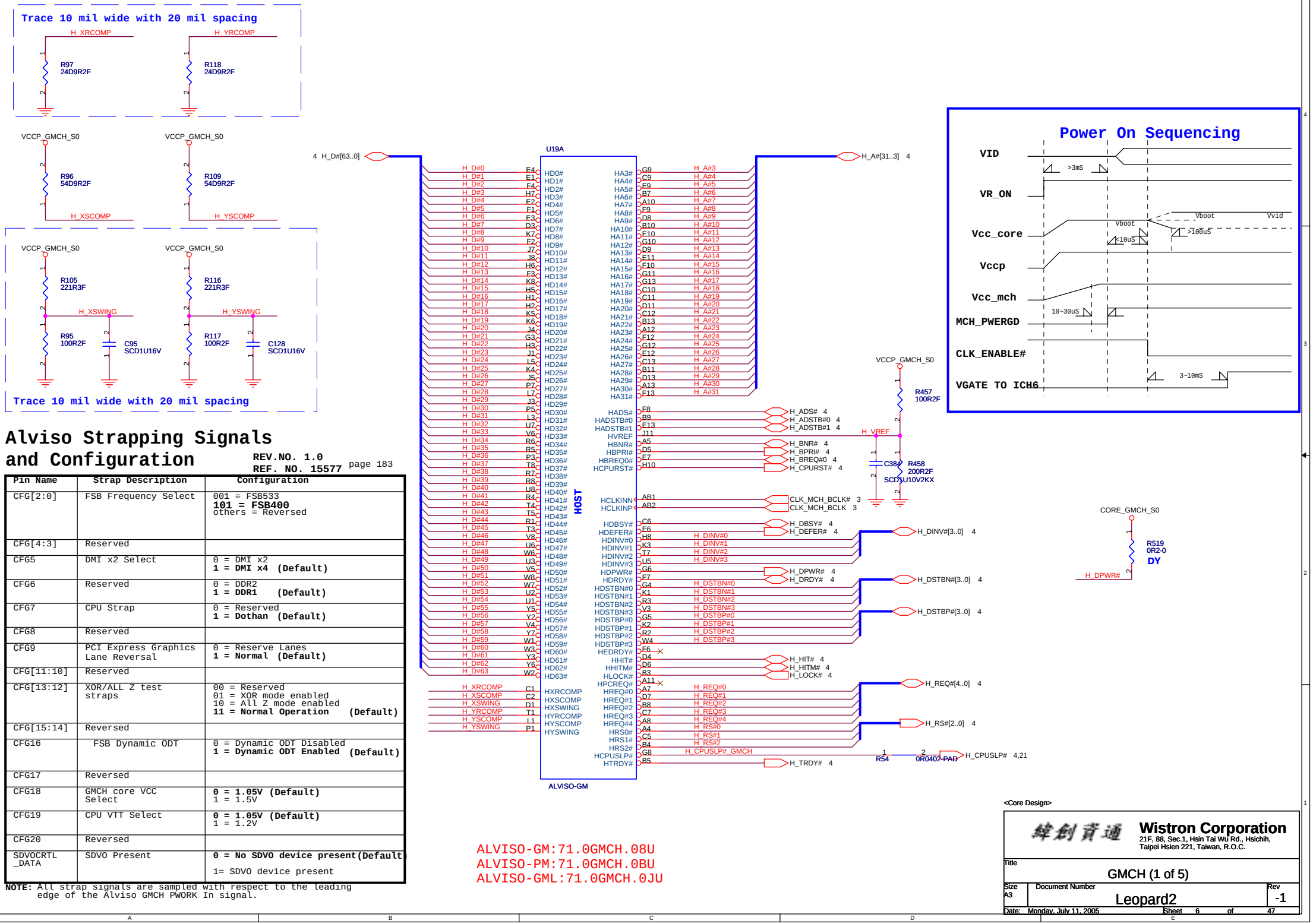
Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Wednesday, July 06, 2005 | Sheet 2 of 47


3D3V_S0
L17
MLB-201209-11
3D3V_APWR_S0
C199
SC4D7U10V5ZY
C524
SCD1U16V
DY
3D3V_48MPWR_S0
R196
4D7R3
C218
C219
L38
MLB-201209-11
3D3V_CLKGEN_S0
C519
SC10U10V6ZY-U
C532
C523
C538
C543
C525
C518
C539
R200
10KR2
ITP_EN
R221
10KR2
DummyR200(up side),Mounting R221(down side)
--SRC7 on
Mounting R200(up side),DummyR221(down side)
--CPU2_ITP on
R590
10KR2
SS_SEL
R591
10KR2
H/L: 100/96MHz
25,41 CLK_PWRGD#
C544
SC22P
X7
X-14D31818M-17
C545
CLK_XOUT
CLK_XIN
U72
VTT_PWRGD#/PD
RN20
RN18
RN19
RN21
SRN33-2-U2
SRCCLKC1
SRCCLKC2
SRCCLKC3
SRCCLKC4_SATA
SRCCLKC5
SRCCLKC6
SRCCLKT1
SRCCLKT2
SRCCLKT3
SRCCLKT4_SATA
SRCCLKT5
SRCCLKT6
REF0
REF1/FSLC/TEST_SEL
SCLK
SDATA
CPU_STOP#
CPUCLKC0
CPUCLKC1
CPUCLKC2_ITP/SRCCLKC7
CPUCLKT0
CPUCLKT1
CPUCLKT2_ITP/SRCCLKT7
FSLA/USB_48MHZ
FSLB/TEST_MODE
96MHZ_SSC/SRCCLKC0
96MHZ_SST/SRCCLKT0
DOTC_96MHZ
DOTT_96MHZ
RN22
RN24
RN25
RN23
CLK_CPUT1
CLK_CPUC1
CLK_CPUC2
CLK_CPUT2
CLK_CPUT0
CLK_CPUC0
CLK_SRCC0
CLK_SRCT0
DOT96C
DOT96T
FS_A
R592
R593
10R2
33R2
R199
R201
33R2
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
PM_STPCPU# 22,41
CLK_XDP_CPU# 4
CLK_XDP_CPU 4
CLK_CPU_BCLK 4
CLK_CPU_BCLK# 4
CLK48_USB 22
CLK48_CARDBUS 27
CPU_SEL1 4,7
DREFSSCLK# 7
DREFSSCLK 7
DREFCLK# 7
DREFCLK 7
26 CLK_PCIE_NEW#
26 CLK_PCIE_NEW
7 CLK_MCH_3GPLL#
7 CLK_MCH_3GPLL
22 CLK_PCIE_ICH#
22 CLK_PCIE_ICH
TPAD30 TP31
TPAD30 TP30
TP_SRCT6
R584
0R2-0
R588
0R2-0
CLK_REF14
26 PREQ2#
22 CLK_ICH14
32 CLK_CODEC
R602
R601
22R2
22R2
4,7 CPU_SEL0
2K2R2
R222
11,24 SMBC_ICH
11,24 SMBD_ICH
13 CLK_PCIE_PEG#
13 CLK_PCIE_PEG
SB
DY
SC
GND
GNDA
SEL100_96MHZ#/PCICLK_F1
PCI/SRC_STOP#
ITP_EN/PCICLK_F0
PCICLK5
PCICLK4
PCICLK3
PCICLK2
IREF
ICS954206AG
CLK_IREF
475R2F
R181
36 PCLK_KBC
R589
22R2
SS_SEL
22 PM_STPPCI#
22 CLK_ICHPCI
R220
33R2
ITP_EN
REQSEL
CLK_PCI3
CLK_PCI4
CLK_PCI5
33R2
33R2
33R2
R600
R218
R219
PCLK_PCM 27
PCLK_LAN 30
PCLK_MINI 34
DREFCLK
DREFCLK#
CLK_PCIE_NEW
CLK_PCIE_NEW#
CLK_XDP_CPU
CLK_XDP_CPU#
CLK_CPU_BCLK
CLK_CPU_BCLK#
CLK_MCH_BCLK
CLK_MCH_BCLK#
R202
R198
R582
R580
R603
R594
R596
R595
R585
R586
49D9R2F
DREFSSCLK
DREFSSCLK#
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
CLK_PCIE_PEG
CLK_PCIE_PEG#
CLK_PCIE_ICH
CLK_PCIE_ICH#
R194
R195
R566
R567
R581
R583
R569
R570
ICS954206AG Spread Spectrum Select
SS3 SS2 SS1 SS0 Spread Amount%
0 0 0 0 -0.8
0 0 0 1 -1.0
0 0 1 0 -1.25
0 0 1 1 -1.5
0 1 0 0 -1.75
0 1 0 1 -2.0
0 1 1 0 -2.5
0 1 1 1 -3.0
1 0 0 0 +-0.3
1 0 0 1 +-0.4
1 0 1 0 +-0.5
1 0 1 1 +-0.6
1 1 0 0 +-0.8
1 1 0 1 +-1.0
1 1 1 0 +-1.25
1 1 1 1 +-1.5
NEAR CLKGEN
3D3V_S0
R606
10KR2
REQSEL
R605
DUMMY-R2
3D3V_CLKGEN_S0
R197
10KR2
FS_A
FS_C FS_B FS_A CPU
0 0 0 266M
0 0 1 133M
0 1 0 200M
0 1 1 166M
1 0 0 333M
1 0 1 100M
1 1 0 400M
1 1 1 Reserved
CLK_CPU_BCLK
CLK_CPU_BCLK#
TP33
TPAD30
TP32
TPAD30
close to CPU
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator (ICS954206AG)
Size A3
Document Number
Leopard2
Rev -1
Date: Monday, July 11, 2005
Sheet 3 of 47


U53A
62.10055.011
PZ47902
ADDR GROUP 0
ADDR GROUP 1
XTP/ITP SIGNALS
CONTROL
HCLK THERM
6 H_A#[31..3]
6 H_ADSTB#0
6 H_REQ#[4..0]
6 H_ADSTB#1
21 H_A20M#
21 H_FERR#
21 H_IGNNE#
21 H_STPCLK#
21 H_INTR
21 H_NMI
21 H_SMI#
H_ADS# 6
H_BNR# 6
H_BPRI# 6
H_DEFER# 6
H_DRDY# 6
H_DBSY# 6
H_BREQ#0 6
H_IERR#
H_INIT# 21
H_LOCK# 6
H_CPURST# 6
H_RS#[2..0] 6
H_TRDY# 6
H_HIT# 6
H_HITM# 6
XDP_BPM#5
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST#
DBR#
CPU_PROCHOT#
THERMDP1 25
THERMDN 25
PM_THRMTRIP-A# 7,21
PM_THRMTRIP-I# 7,21
CLK_XDP_CPU# 3
CLK_XDP_CPU 3
CLK_CPU_BCLK# 3
CLK_CPU_BCLK 3
VCCP_GMCH_S0
VCC_CORE_S0
R396 56R2J
R393 56R2J
R27 150R2
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH6 and Alviso without T-ing (No stub)
CPU
TCK(PIN A13)
ITP Conn.
TCK(PIN 5)
FBO(PIN 11)
H_CPURST#
XDP_TDO
CPU_PROCHOT#
XDP_TDI
XDP_TMS
XDP_TRST#
XDP_TCK
R391 54D9R2F
R386 54D9R2F
R384 56R2J
R387 150R2
R389 39D2R2F
R388 680R2
R390 27D4R2F
All place within 2" to CPU
U53B
PZ47903
62.10055.011
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
H_D#[63..0] 6
6 H_DSTBN#0
6 H_DSTBP#0
6 H_DINV#0
6 H_DSTBN#1
6 H_DSTBP#1
6 H_DINV#1
H_DSTBN#2 6
H_DSTBP#2 6
H_DINV#2 6
H_DSTBN#3 6
H_DSTBP#3 6
H_DINV#3 6
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
TP2
3,7 CPU_SEL0
3,7 CPU_SEL1
R383
R385
0R0402-PAD
CPU_SEL0_CPU
CPU_SEL1_CPU
R402 27D4R2F
R403 54D9R2F
R35 27D4R2F
R36 54D9R2F
R395 200R2J
H_DPRSLP# 21
H_DPSLP# 21
H_DPWR# 6
H_PWRGD 21
H_CPUSLP# 6,21
VCCP_GMCH_S0
R34 1KR2F
R33 2KR2F
GTLREF
Layout Note: 0.5" max length.
BSEL[1:0] Freq.(MHz)
L H 100
L L 133
R29 1KR2 DY
R392 1KR2 DY
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (1 of 2)
Size A3
Document Number
Leopard2
Rev -1
Date: Monday, July 11, 2005
Sheet 4 of 47


U53C
PZ47903
62.10055.011
U53D
PZ47903
62.10055.011
VCC_CORE_S0
1D5V_VCCA_S0
VCCP_GMCH_S0
C17
SCD01U16V2KX
C15
SC10U10V6ZY-U
TP1
TP3
TP20
TP_VCCA1
TP_VCCA2
TP_VCCA3
CPU_D10
R394
0R2-0
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
TP_VCCSENSE
TP_VSSSENSE
R40
54D9R2F
DY
R39
54D9R2F
DY
I max = 120 mA
3D3V_S0
U52
SHDN#
GND
IN
SET
OUT
G913C-U
DY
BC84
SC22P
DY
BC85
SC1U10V3ZY
DY
BC2
SC1U10V3ZY
DY
1D5V_VCCA_SET
R397
12K7R3F
DY
R398
49K9R2F
DY
1D5V_S0
R28
0R2-0
0.1u *10
150u *1
C21
C20
C29
C30
C25
C16
C28
C31
C22
C32
SCD1U10V2MX-1
TC1
ST100U6D3VM-U
C18
C19
C23
C24
C33
C35
C36
C42
C39
C40
C41
C50
C318
C319
C321
C322
C323
C325
C324
C326
SC10U6D3V5MX
SC10U10V5ZY-L
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (2 of 2)
Size
A3
Document Number
Leopard2
Rev
SC
Date: Sunday, July 03, 2005
Sheet 5 of 47



Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 **101 = FSB400** others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	Reserved	0 = DDR2 **1 = DDR1 (Default)**
CFG7	CPU Strap	0 = Reserved **1 = Dothan (Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes **1 = Normal (Default)**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation (Default)**
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Reversed	
CFG18	GMCH core VCC Select	**0 = 1.05V (Default)** 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V (Default)** 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present(Default)** 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

ALVISO-GM:71.0GMCH.08U
ALVISO-PM:71.0GMCH.0BU
ALVISO-GML:71.0GMCH.0JU

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (1 of 5)
Size: A3
Document Number: Leopard2
Rev: -1
Date: Monday, July 11, 2005
Sheet 6 of 47

Alviso will provide SDVO_CTRLCLK
and CTRLDATA pulldowns on-die

U19B

DMI
CFG/RSVD
DDR MUXING
PM
CLK
NC
ALVISO-GM

Note:
CRT_RED,
CRT_GREEN,
CRT_BLUE, are
ground
referenced.

Intel suggest NC Due to votusly DVO

Intel design guide suggest
Ref no.:14511
page 210

Place 150 Ohm termination resistors close to GMCH

Note: Intel design guide
suggest(page 203)
If the LVDS interface is
not implementd, all
signals associated with
the interface can be left
as no connects.

U19G

MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
ALVISO-GM

Layout Note:
Route as short
as possible

DDR_VREF_S3

C154
SCD1U10V2MX-1

FOR DDR2

For Dothan-B

Ref ALVISO EDS-1 Page 115

When Low 2.2K Ohm

When High 1K Ohm

CFG(2..1)	FREQ.(MHz)
10	400
00	533
11	Reserved

CFG2=0(R419):133MHZ
CFG2=1(R420):100MHZ

Strapping

CFG[17:3] have internal pullup resistors.
CFG[19:18] have internal pulldown resistors

<Core Design>

Wistron Corporation
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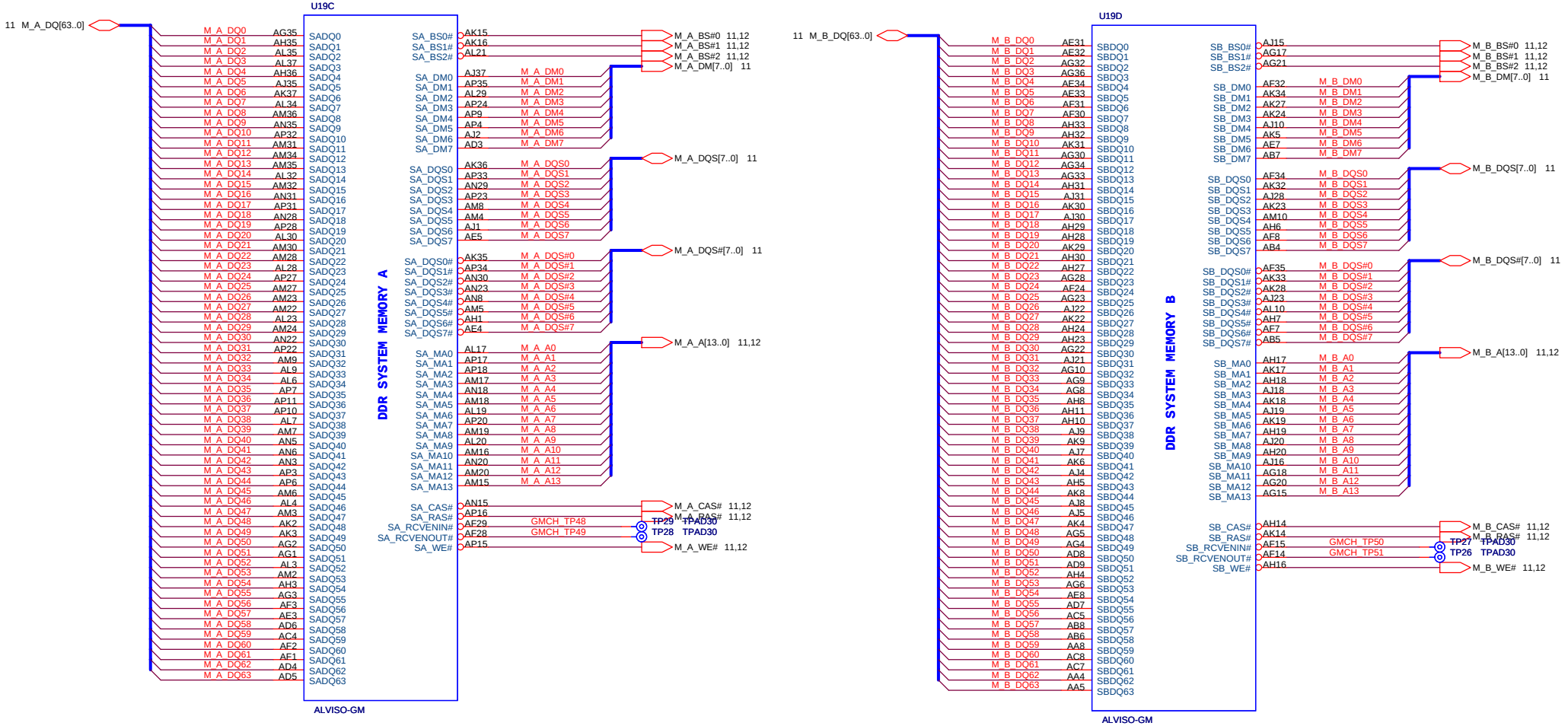
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (2 of 5)

Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 7 of 47



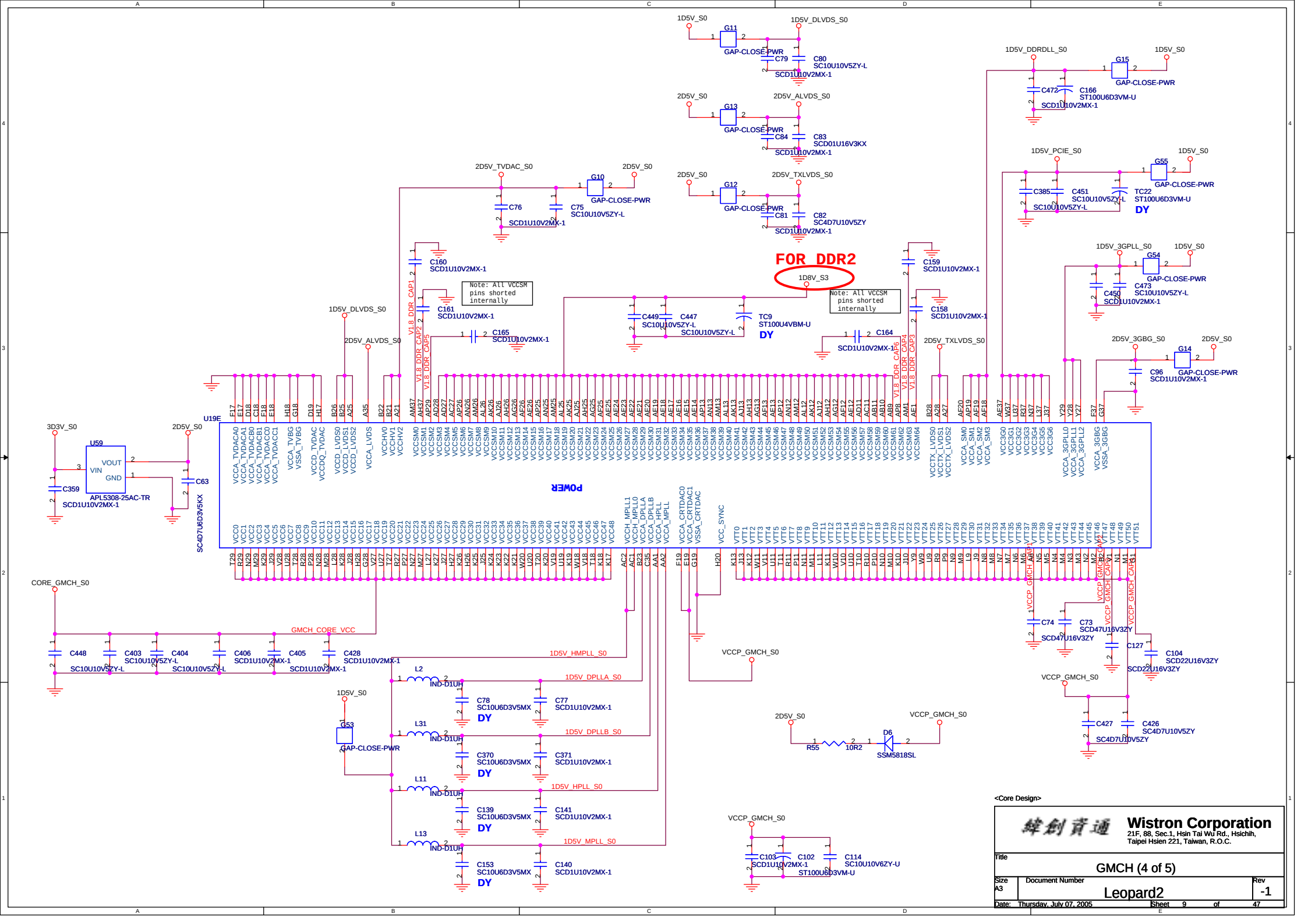
<Core Design>

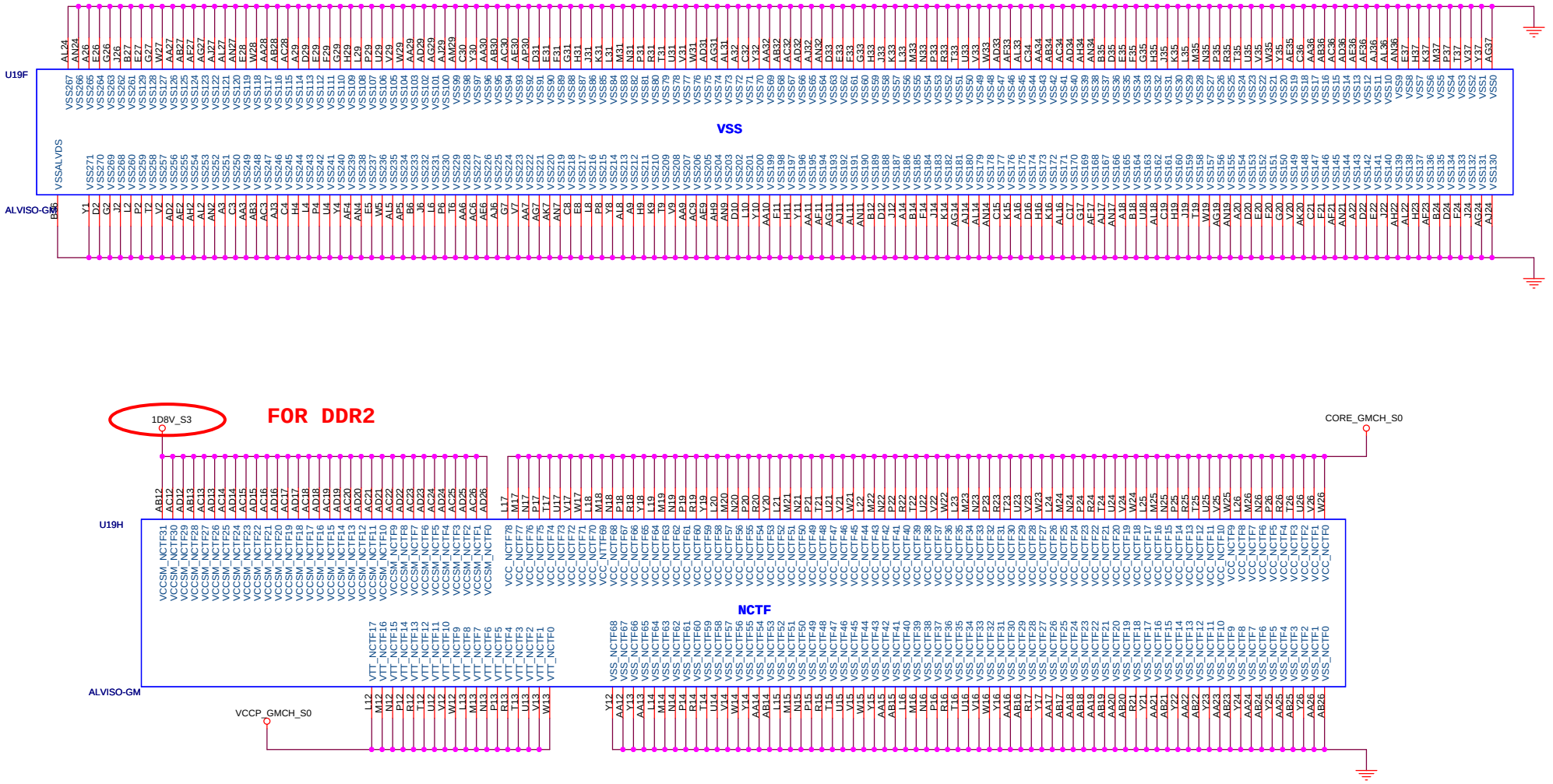
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (3 of 5)

Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 8 of 47


FOR DDR2
POWER
Note: All VCCSM pins shorted internally
Note: All VCCSM pins shorted internally
DY
DY
DY
DY
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (4 of 5)
Size A3
Document Number
Leopard2
Rev -1
Date: Thursday, July 07, 2005
Sheet 9 of 47



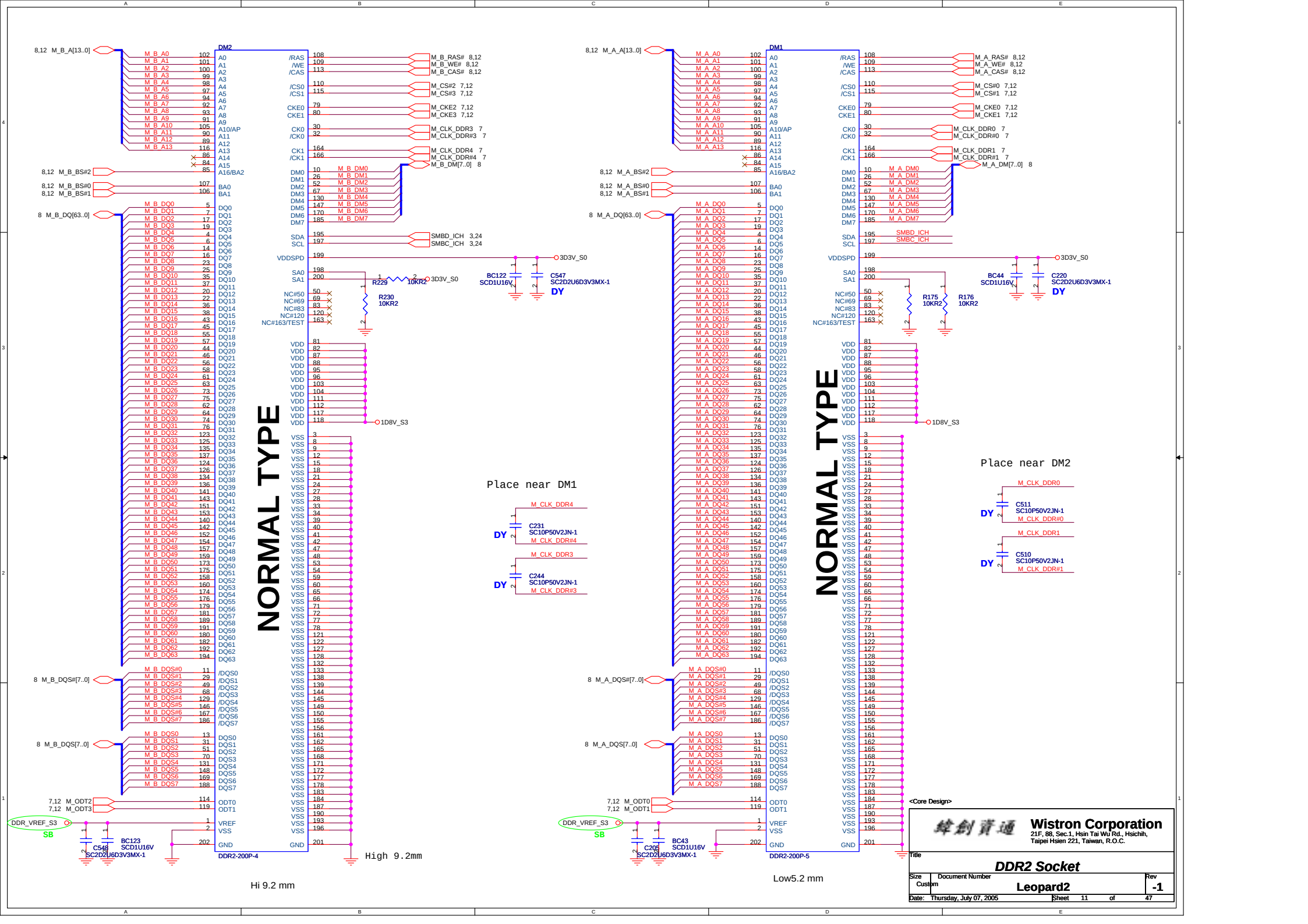
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (5 of 5)

Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Thursday, July 07, 2005 | Sheet 10 of 47



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR2 Socket**

Size	Document Number	Rev
Custom	Leopard2	-1

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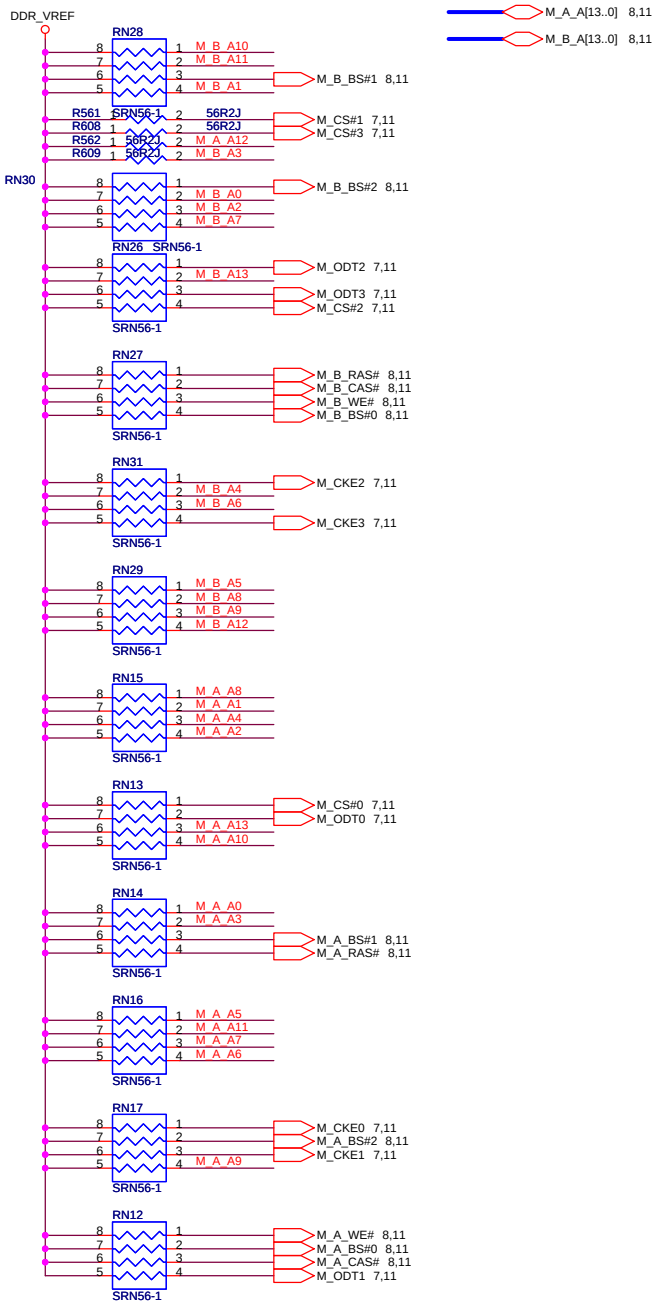
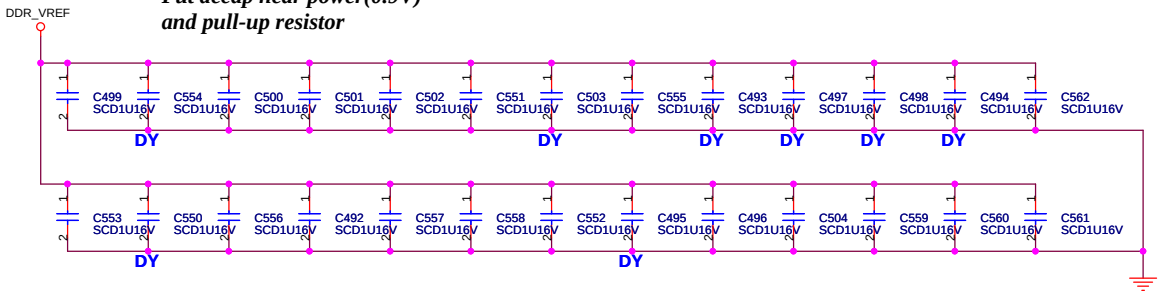
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

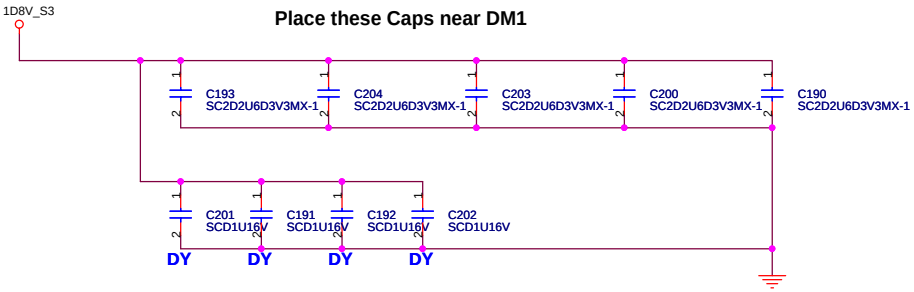


Decoupling Capacitor

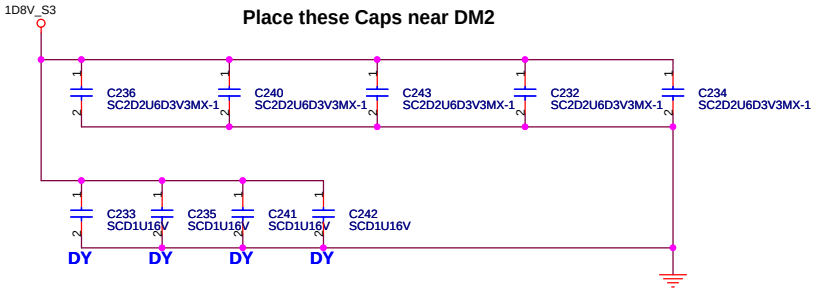
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



<Core Design>

Wistron Corporation
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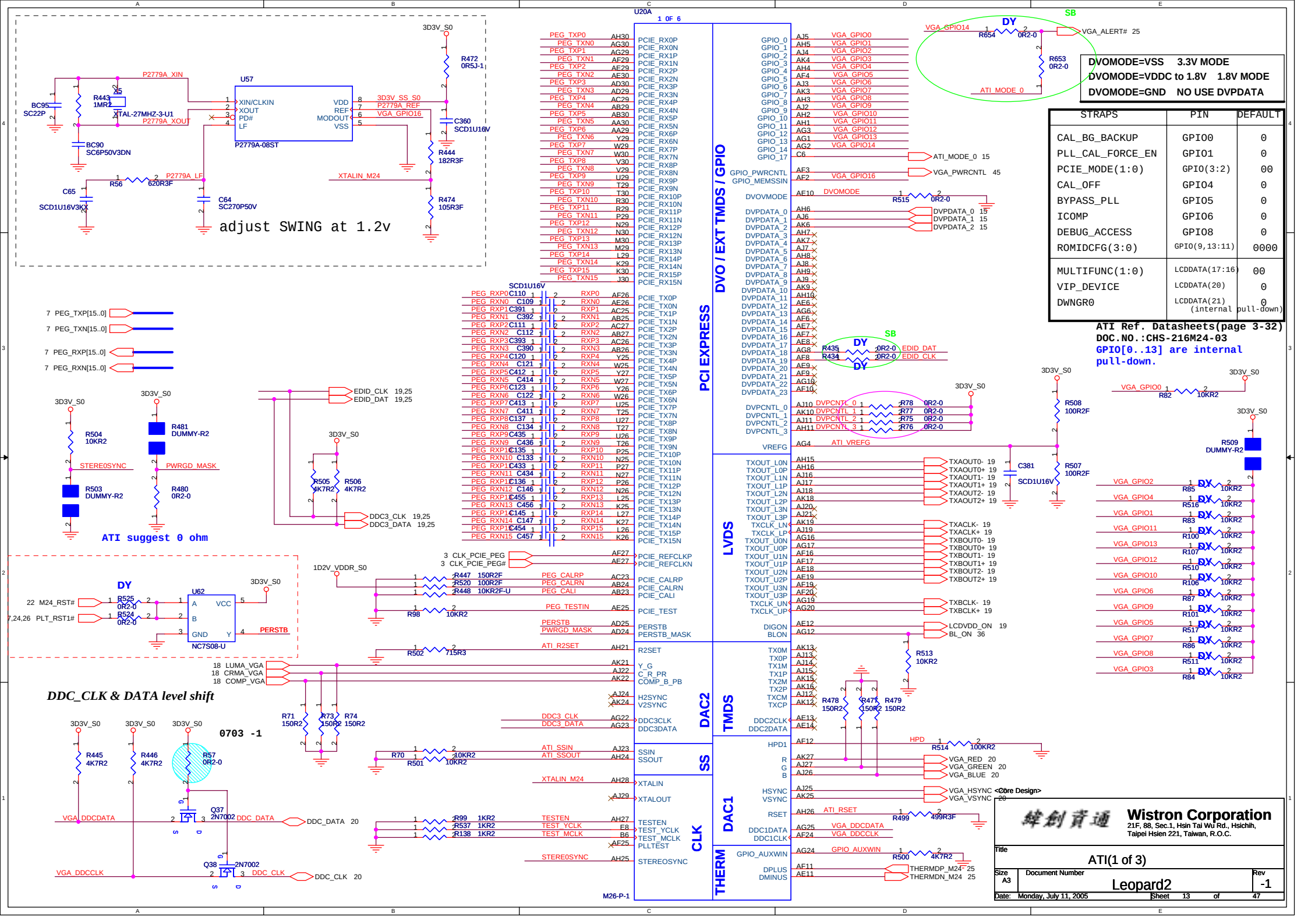
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 Termination Resistor

Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Thursday, July 07, 2005 | Sheet 12 of 47


U20A
1 OF 6
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_CALRP
PCIE_CALRN
PCIE_CALI
PCIE_TEST
PERSTB
PERSTB_MASK
PCI EXPRESS
R2SET
Y_G
C_R_PR
COMP_B_PB
H2SYNC
V2SYNC
DDC3CLK
DDC3DATA
DAC2
SSIN
SSOUT
SS
XTALIN
XTALOUT
TESTEN
TEST_YCLK
TEST_MCLK
PLLTEST
STEREOSYNC
CLK
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13
GPIO_14
GPIO_17
GPIO_PWRCNTL
GPIO_MEMSSIN
DVOVMODE
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCNTL_3
VREFG
DVO / EXT TMDS / GPIO
TXOUT_L0N
TXOUT_L0P
TXOUT_L1N
TXOUT_L1P
TXOUT_L2N
TXOUT_L2P
TXOUT_L3N
TXOUT_L3P
TXCLK_LN
TXCLK_LP
TXOUT_U0N
TXOUT_U0P
TXOUT_U1N
TXOUT_U1P
TXOUT_U2N
TXOUT_U2P
TXOUT_U3N
TXOUT_U3P
TXCLK_UN
TXCLK_UP
DIGON
BLON
LVDS
TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TXCM
TXCP
DDC2CLK
DDC2DATA
TMDS
HPD1
R
G
B
HSYNC
VSYNC
RSET
DDC1DATA
DDC1CLK
DAC1
GPIO_AUXWIN
DPLUS
DMINUS
THERM
M26-P-1
P2779A_XIN
P2779A_XOUT
P2779A_LF
XTALIN_M24
XTAL-27MHZ-3-U1
P2779A-08ST
U57
3D3V_SS_S0
P2779A_REF
VGA_GPIO16
adjust SWING at 1.2v
SCD1U16V
7 PEG_TXP[15..0]
7 PEG_TXN[15..0]
7 PEG_RXP[15..0]
7 PEG_RXN[15..0]
EDID_CLK 19,25
EDID_DAT 19,25
DDC3_CLK 19,25
DDC3_DATA 19,25
ATI suggest 0 ohm
STERE0SYNC
PWRGD_MASK
U62
NC7S08-U
PERSTB
22 M24_RST#
7,24,26 PLT_RST1#
1D2V_VDDR_S0
CLK_PCIE_PEG
CLK_PCIE_PEG#
PEG_CALRP
PEG_CALRN
PEG_CALI
PEG_TESTIN
ATI_R2SET
18 LUMA_VGA
18 CRMA_VGA
18 COMP_VGA
DDC_CLK & DATA level shift
0703 -1
VGA_DDCDATA
VGA_DDCCLK
Q37 2N7002
Q38 2N7002
DDC_DATA
DDC_CLK
DDC_DATA 20
DDC_CLK 20
ATI_SSIN
ATI_SSOUT
TESTEN
TEST_YCLK
TEST_MCLK
VGA_GPIO14
ATI_MODE_0
VGA_ALERT# 25
DVOMODE=VSS 3.3V MODE
DVOMODE=VDDC to 1.8V 1.8V MODE
DVOMODE=GND NO USE DVPDATA
STRAPS | PIN | DEFAULT
CAL_BG_BACKUP | GPIO0 | 0
PLL_CAL_FORCE_EN | GPIO1 | 0
PCIE_MODE(1:0) | GPIO(3:2) | 00
CAL_OFF | GPIO4 | 0
BYPASS_PLL | GPIO5 | 0
ICOMP | GPIO6 | 0
DEBUG_ACCESS | GPIO8 | 0
ROMIDCFG(3:0) | GPIO(9,13:11) | 0000
MULTIFUNC(1:0) | LCDDATA(17:16) | 00
VIP_DEVICE | LCDDATA(20) | 0
DWNGR0 | LCDDATA(21) (internal pull-down) | 0
ATI Ref. Datasheets(page 3-32)
DOC.NO.:CHS-216M24-03
GPIO[0..13] are internal pull-down.
VGA_RED 20
VGA_GREEN 20
VGA_BLUE 20
VGA_HSYNC 20
VGA_VSYNC 20
ATI_RSET
VGA_DDCDATA
VGA_DDCCLK
GPIO_AUXWIN
THERMDP_M24 25
THERMDN_M24 25
LCDVDD_ON 19
BL_ON 36
TXAOUT0- 19
TXAOUT0+ 19
TXAOUT1- 19
TXAOUT1+ 19
TXAOUT2- 19
TXAOUT2+ 19
TXACLK- 19
TXACLK+ 19
TXBOUT0- 19
TXBOUT0+ 19
TXBOUT1- 19
TXBOUT1+ 19
TXBOUT2- 19
TXBOUT2+ 19
TXBCLK- 19
TXBCLK+ 19
EDID_DAT
EDID_CLK
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCNTL_3
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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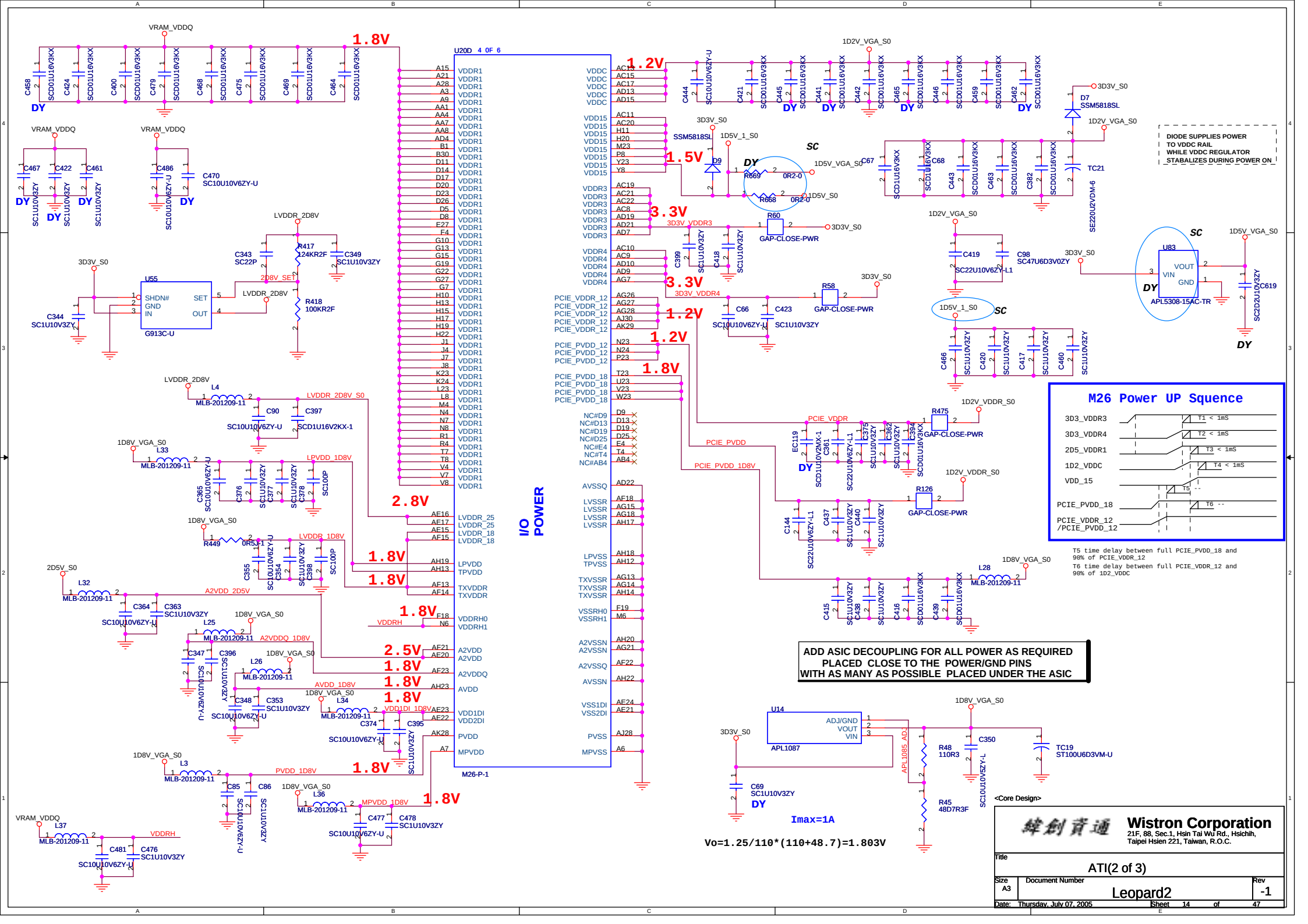
Title
ATI(1 of 3)
Size A3
Document Number
Leopard2
Rev -1
Date: Monday, July 11, 2005
Sheet 13 of 47


U20D 4 OF 6
I/O POWER
M26-P-1
1.8V
1.2V
3.3V
2.8V
2.5V
1D8V_VGA_S0
1D2V_VGA_S0
3D3V_S0
1D5V_1_S0
2D5V_S0
LVDDR_2D8V
VRAM_VDDQ
DY
SC
M26 Power UP Squence
3D3_VDDR3
3D3_VDDR4
2D5_VDDR1
1D2_VDDC
VDD_15
PCIE_PVDD_18
PCIE_VDDR_12 /PCIE_PVDD_12
T1 < 1mS
T2 < 1mS
T3 < 1mS
T4 < 1mS
T5 --
T6 --
T5 time delay between full PCIE_PVDD_18 and 90% of PCIE_VDDR_12
T6 time delay between full PCIE_VDDR_12 and 90% of 1D2_VDDC
DIODE SUPPLIES POWER TO VDDC RAIL WHILE VDDC REGULATOR STABALIZES DURING POWER ON
ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED PLACED CLOSE TO THE POWER/GND PINS WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC
Imax=1A
Vo=1.25/110*(110+48.7)=1.803V
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI(2 of 3)
Size A3
Document Number
Leopard2
Rev -1
Date: Thursday, July 07, 2005
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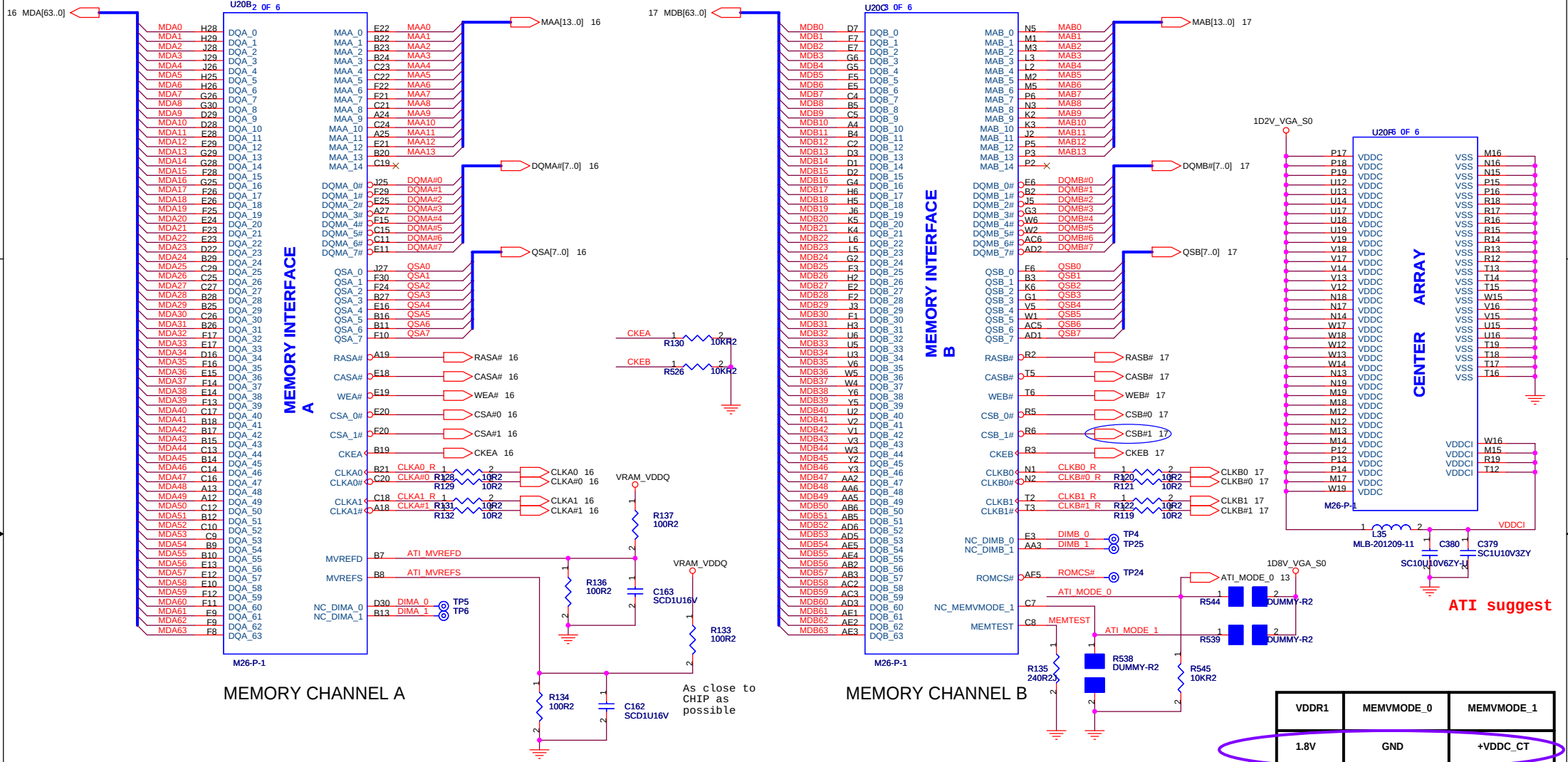

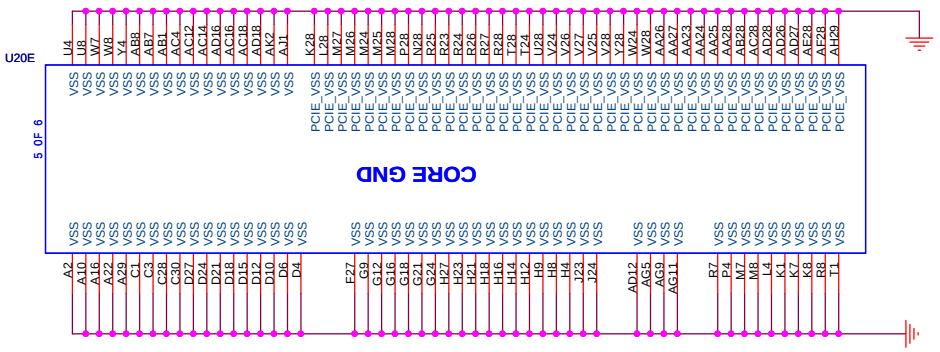

VRAM Selection

Vendor/Size	SETTING DVPDATA_[2:0]
HYNIX/128M	000
SAMSUNG/128M	001
RESERVED	010
RESERVED	011
RESERVED	100
RESERVED	101
RESERVED	110
RESERVED	111

Hynix : HY5DS573222F(P)-28 (8Mx32)

Samsung : K4D553235F-VC2A (8Mx32)

Hynix : 72.55732.B0U

Samsng : 72.45532.M0U

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI(3 of 3)

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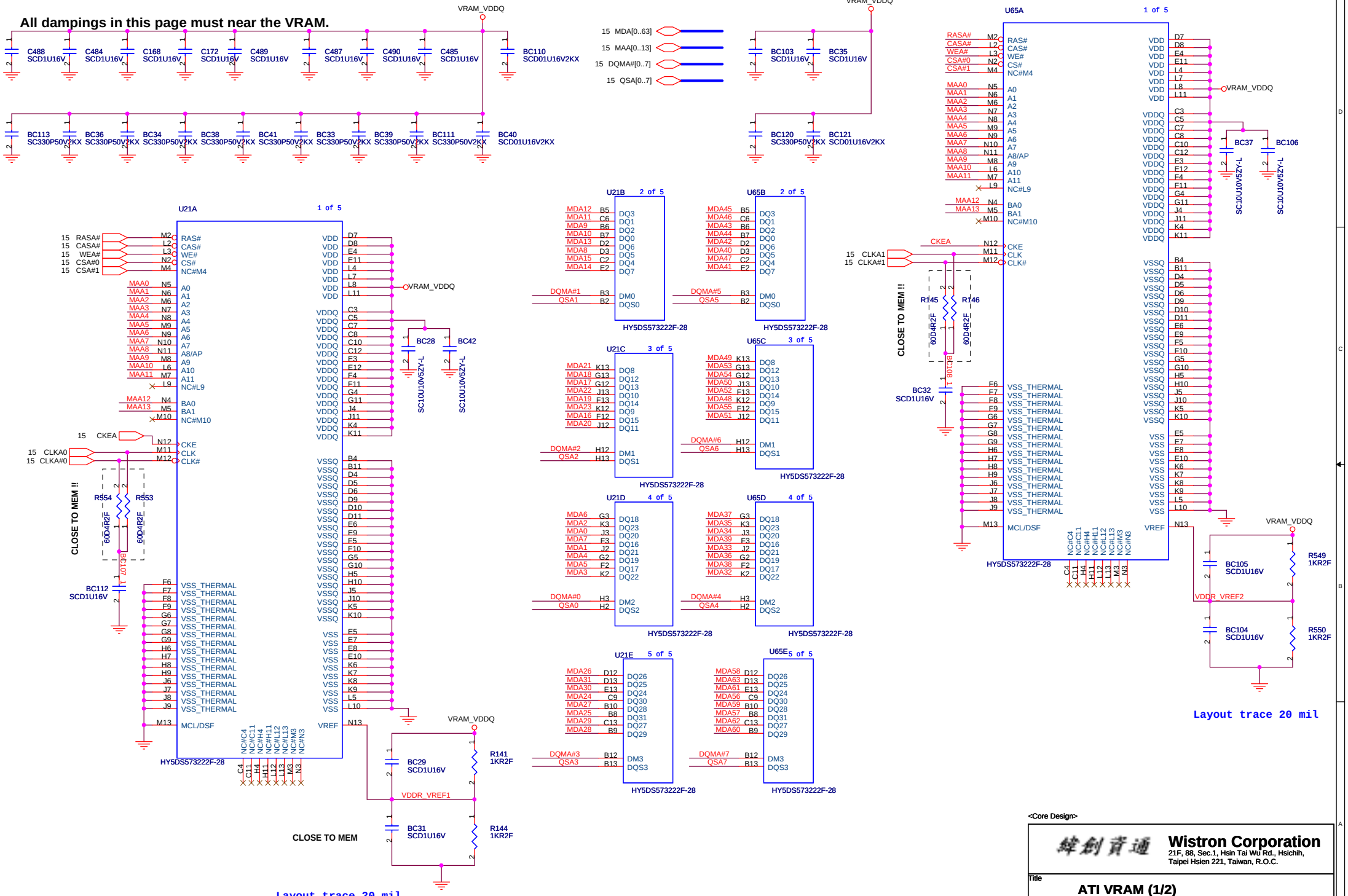
All dampings in this page must near the VRAM.



<Core Design>

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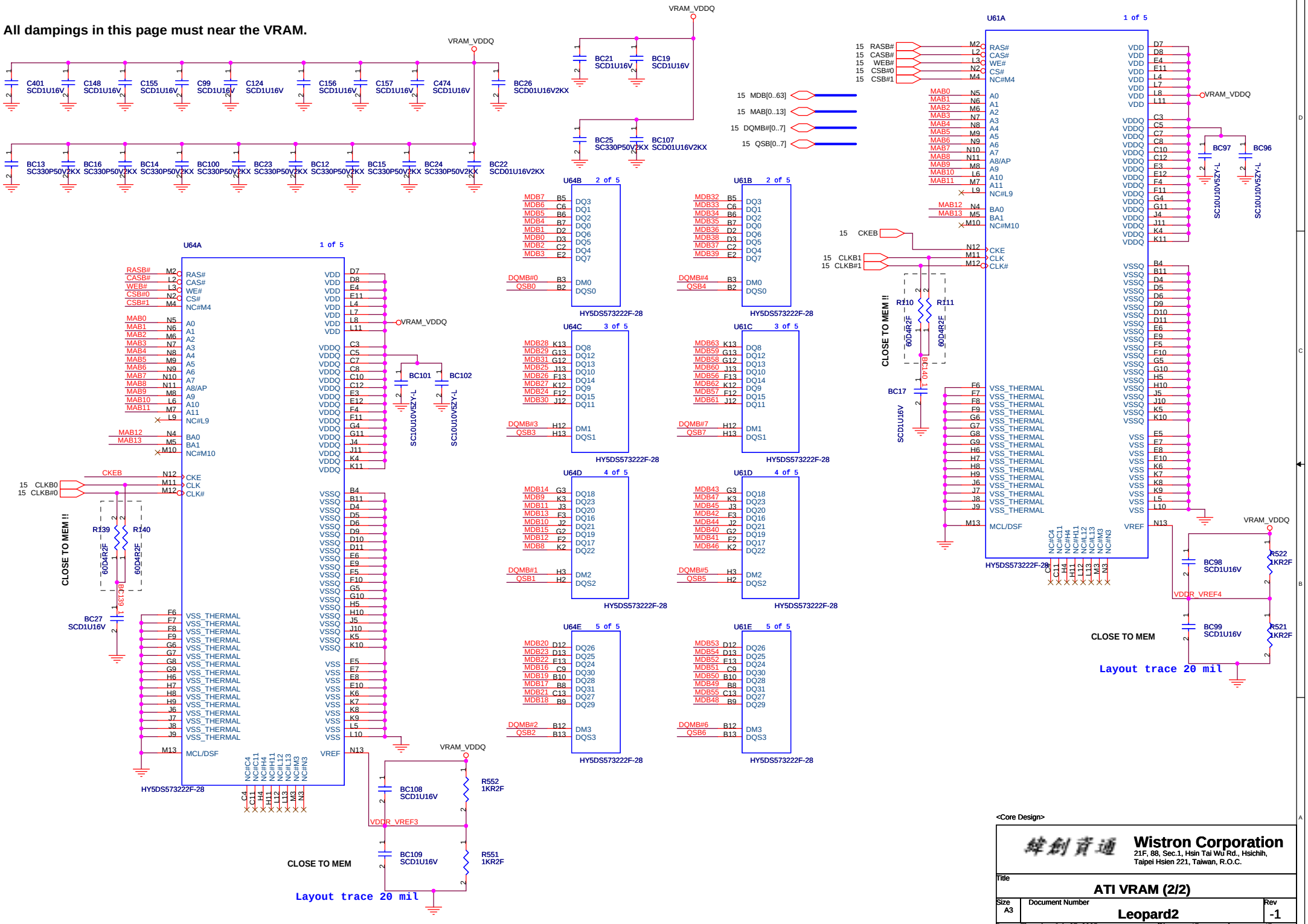
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI VRAM (1/2)

Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Thursday, July 07, 2005 | Sheet 16 of 47

All dampings in this page must near the VRAM.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI VRAM (2/2)**

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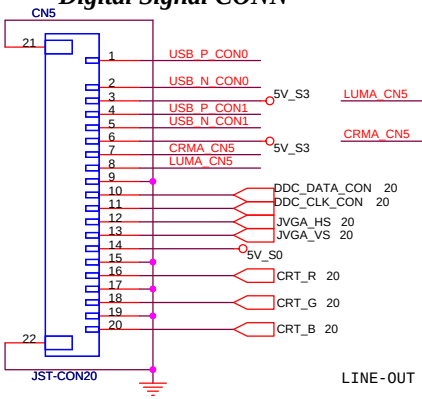
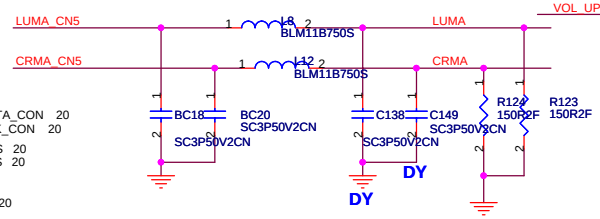
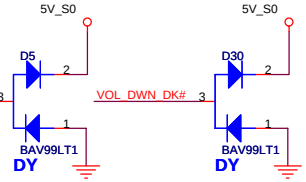
Digital Signal CONN



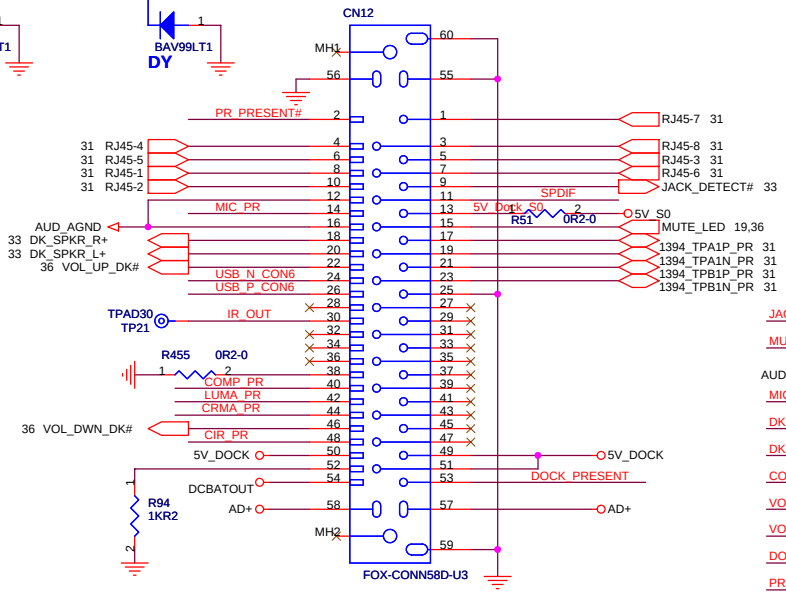
LINE-OUT

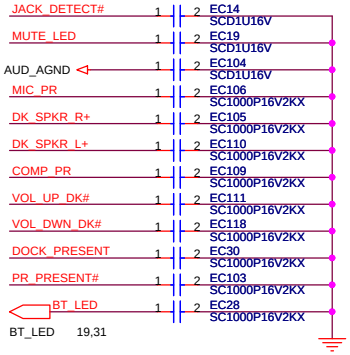


Close to Docking CN

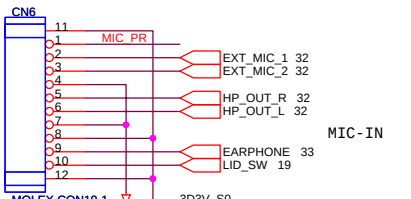


Docking Connector

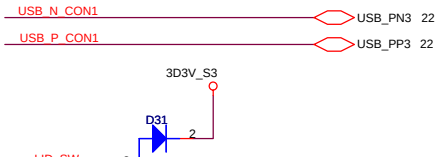


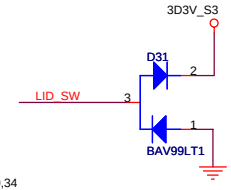


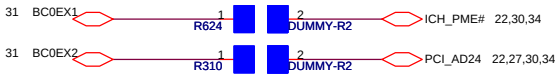
Analog Signal CONN



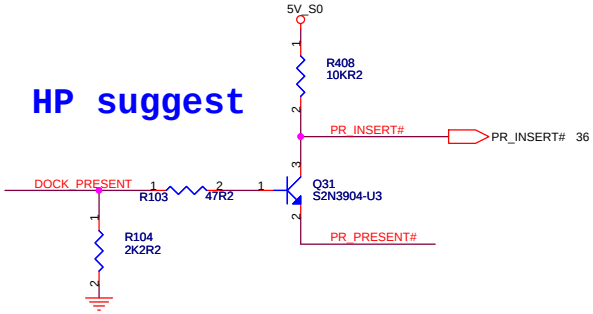
MIC-IN

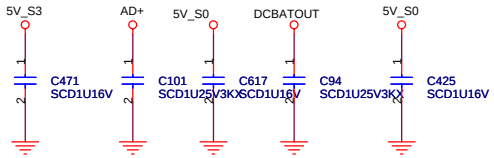


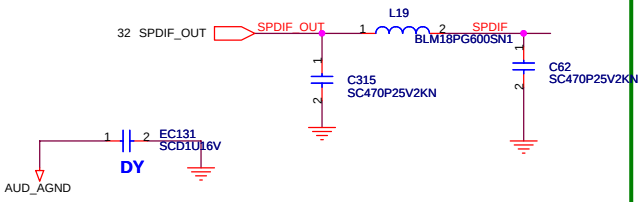


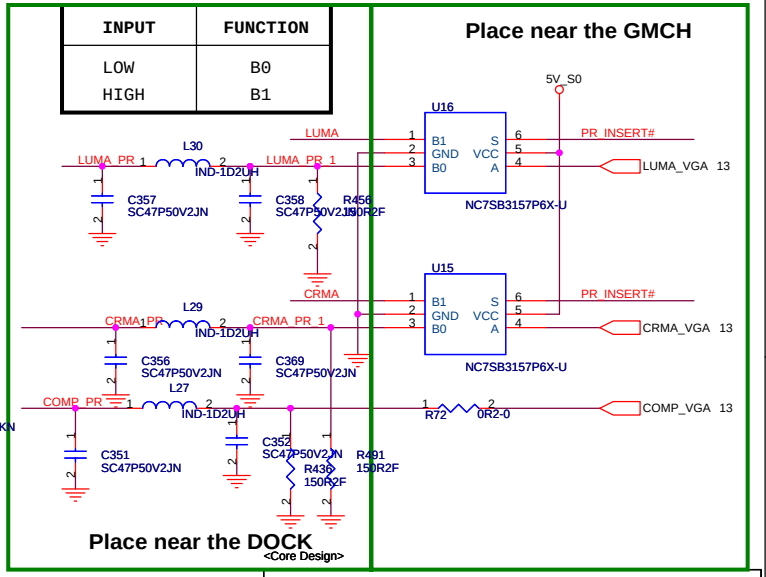


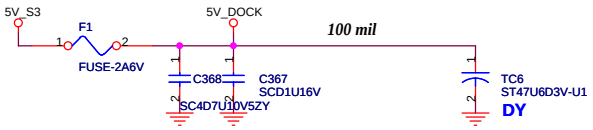
Please close to ICH6

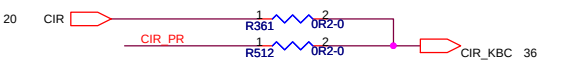












CIR,CIR_PR,CIR_KBC are connect togather. default setting 12/12

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Board to board conn/ Docking
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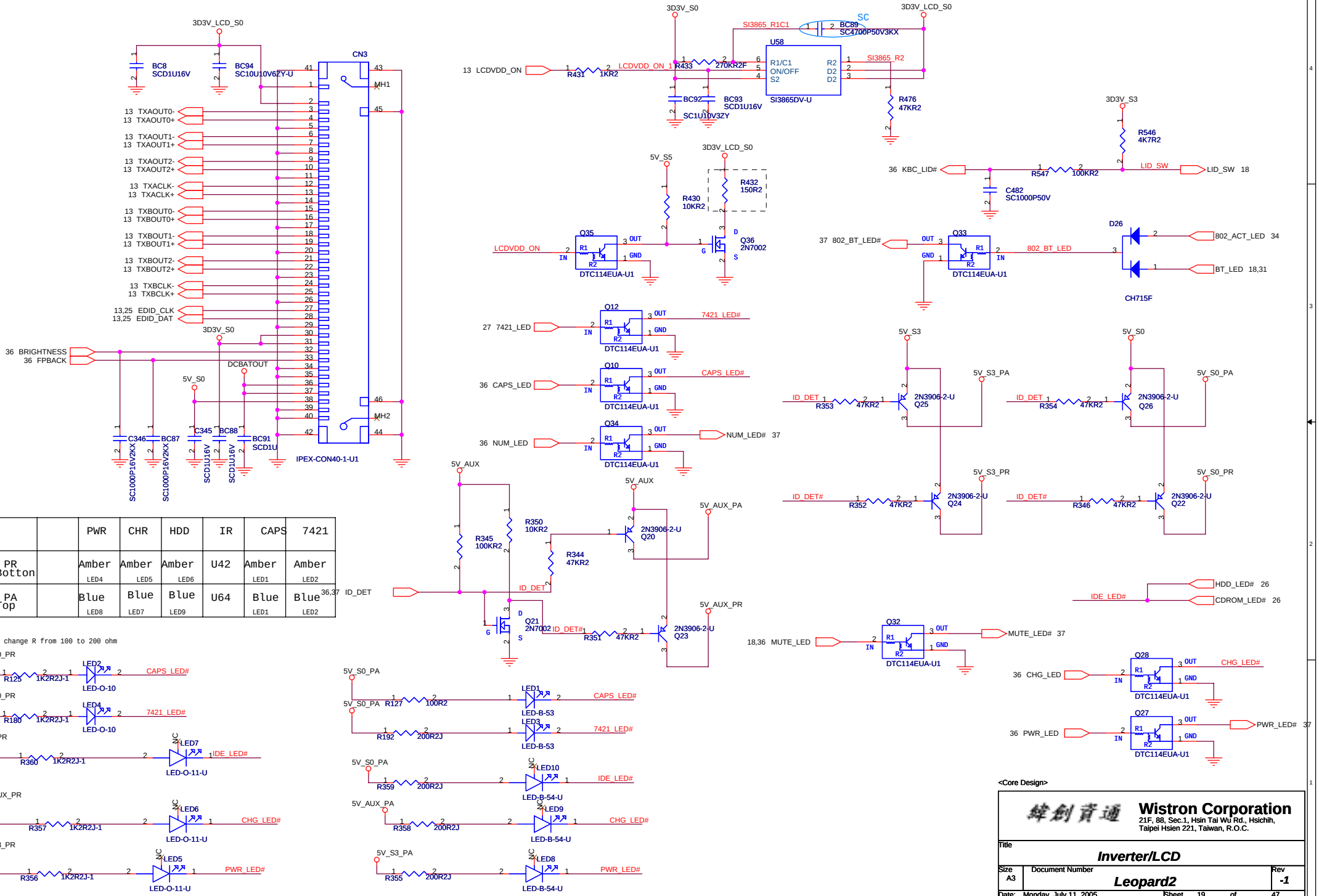
INVERTER/LCD



		PWR	CHR	HDD	IR	CAPS	7421
PR Botton		Amber LED4	Amber LED5	Amber LED6	U42	Amber LED1	Amber LED2
PA Top		Blue LED8	Blue LED7	Blue LED9	U64	Blue LED1	Blue LED2

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	*Inverter/LCD*	
Size A3	Document Number *Leopard2*	Rev *-1*
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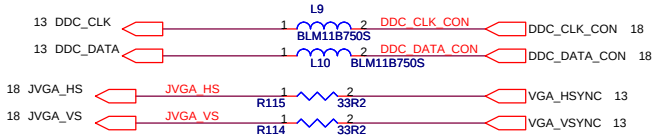
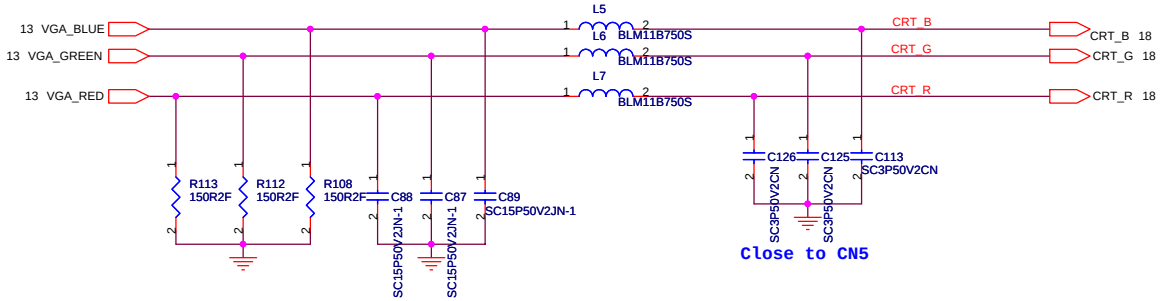
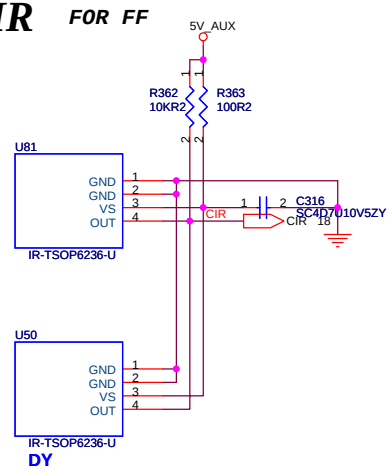
CRT





010804 Modified on Astro ID request

CIR *FOR FF*



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/ CIR

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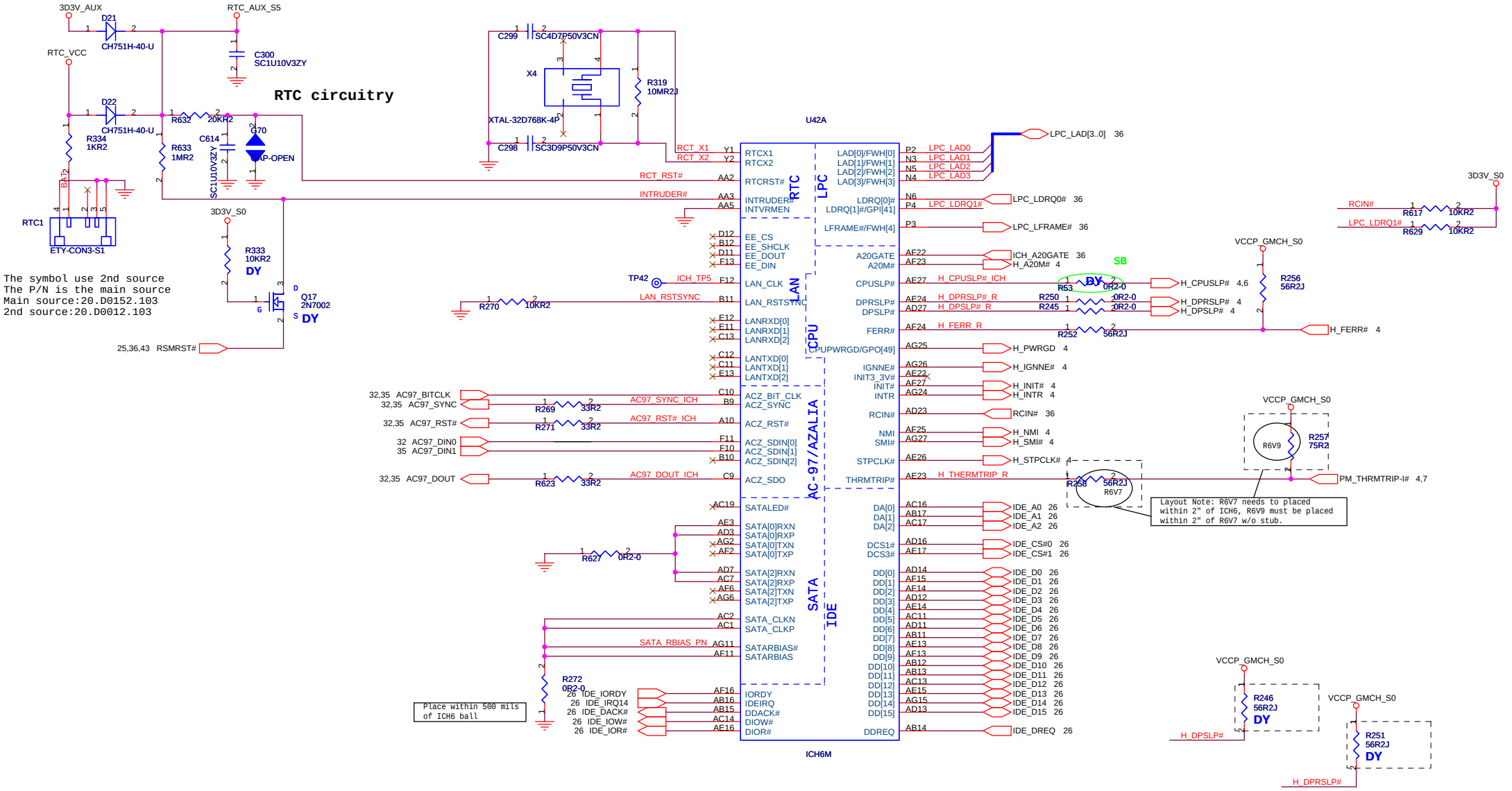
RTC circuitry
The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103
U42A
ICH6M
RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE
Layout Note: R6V7 needs to placed within 2" of ICH6, R6V9 must be placed within 2" of R6V7 w/o stub.
Place within 500 mils of ICH6 ball
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (1 of 4)
Size A3
Document Number
Leopard2
Rev -1
Date: Thursday, July 07, 2005
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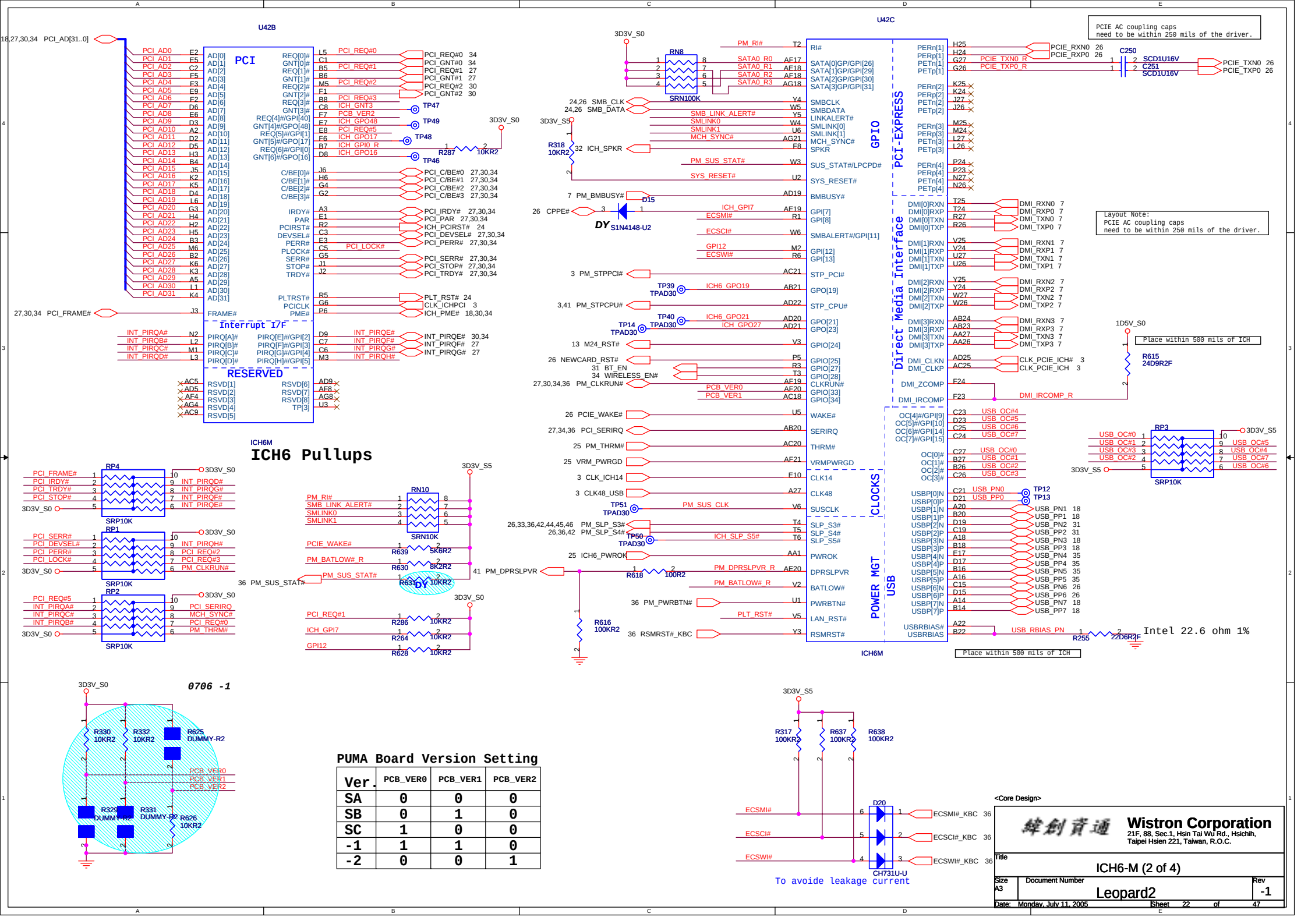
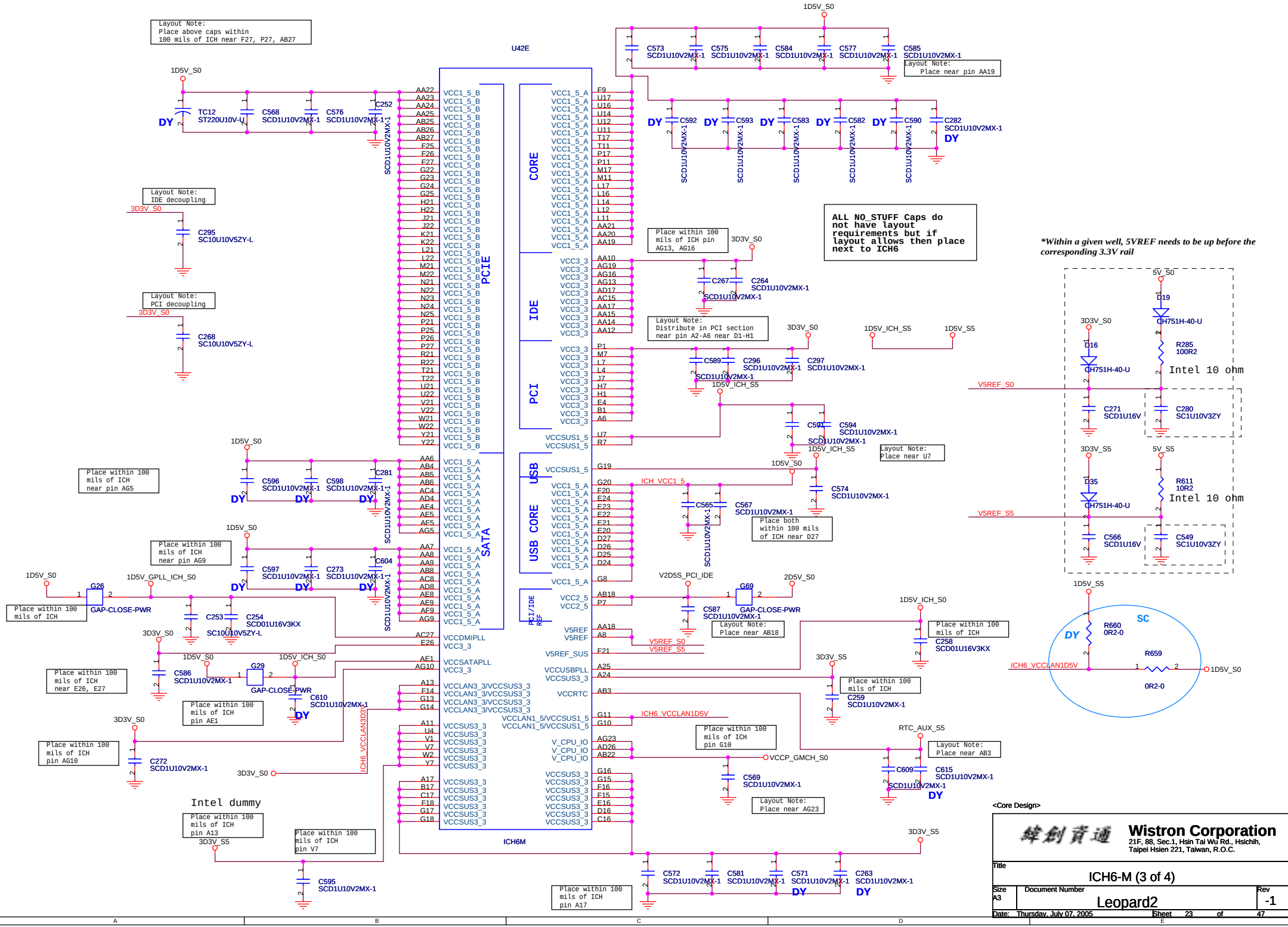

U42B
PCI
Interrupt I/F
RESERVED
U42C
GPIO
PCI-EXPRESS
Direct Media Interface
CLOCKS
POWER MGT
USB
ICH6M
ICH6 Pullups
PCIE AC coupling caps need to be within 250 mils of the driver.
Layout Note: PCIE AC coupling caps need to be within 250 mils of the driver.
Place within 500 mils of ICH
Intel 22.6 ohm 1%
0706 -1
PUMA Board Version Setting
Ver. | PCB_VER0 | PCB_VER1 | PCB_VER2
SA | 0 | 0 | 0
SB | 0 | 1 | 0
SC | 1 | 0 | 0
-1 | 1 | 1 | 0
-2 | 0 | 0 | 1
To avoide leakage current
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH6-M (2 of 4)
Leopard2
Size A3
Rev -1
Date: Monday, July 11, 2005
Sheet 22 of 47


U42E
ICH6M
PCIE
SATA
CORE
IDE
PCI
USB
USB CORE
PCI/IDE REF
Layout Note: Place above caps within 100 mils of ICH near F27, P27, AB27
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Place within 100 mils of ICH near pin AG5
Place within 100 mils of ICH near pin AG9
Place within 100 mils of ICH near E26, E27
Place within 100 mils of ICH pin AE1
Place within 100 mils of ICH pin AG10
Place within 100 mils of ICH pin A13
Place within 100 mils of ICH pin V7
Place within 100 mils of ICH pin A17
Place within 100 mils of ICH pin AG13, AG16
Layout Note: Distribute in PCI section near pin A2-A6 near D1-H1
Layout Note: Place near U7
Place both within 100 mils of ICH near D27
Layout Note: Place near AB18
Place within 100 mils of ICH pin G10
Layout Note: Place near AG23
Layout Note: Place near pin AA19
Layout Note: Place near AB3
ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Intel dummy
Intel 10 ohm
Intel 10 ohm
1D5V_S0
3D3V_S0
3D3V_S5
5V_S0
5V_S5
1D5V_S5
1D5V_ICH_S0
1D5V_ICH_S5
1D5V_GPLL_ICH_S0
2D5V_S0
V2D5S_PCI_IDE
RTC_AUX_S5
V5REF_S0
V5REF_S5
VCCP_GMCH_S0
ICH_VCC1_5
ICH6_VCCLAN1D5V
ICH6_VCCLAN3D3V
GAP-CLOSE-PWR
SCD1U10V2MX-1
SC10U10V5ZY-L
SC1U10V3ZY
SCD01U16V3KX
SCD1U16V
CH751H-40-U
DY
SC
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (3 of 4)
Size A3
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Leopard2
Rev -1
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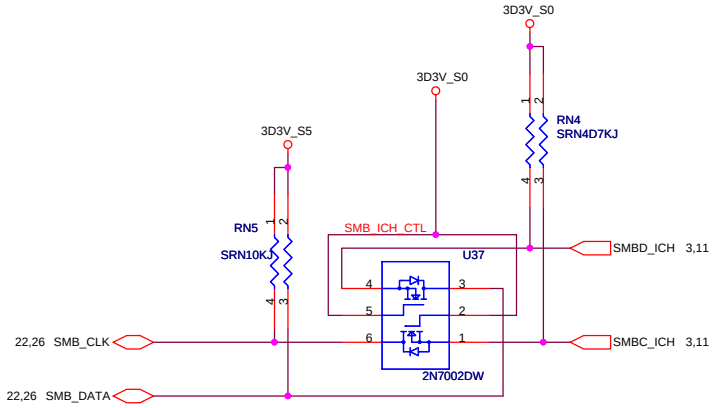
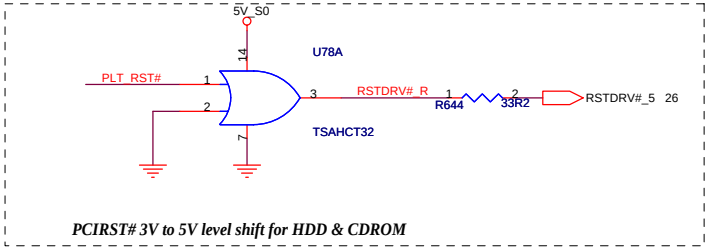
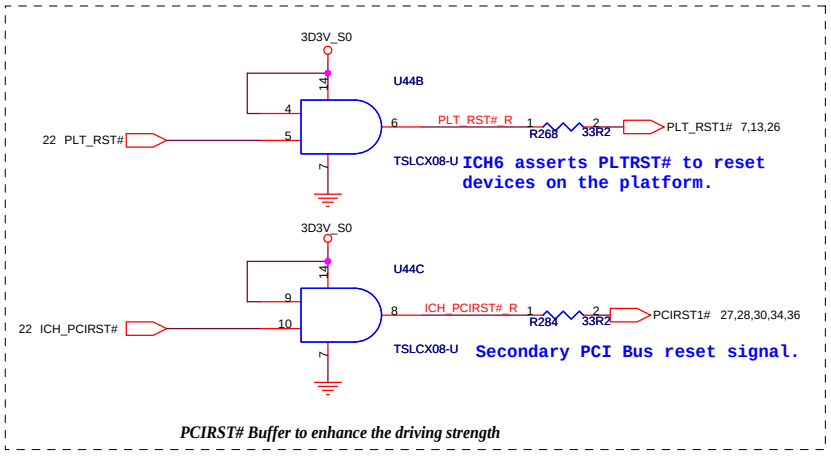
SMBUS(ICH6 ---> SODIMM,CLKGEN)

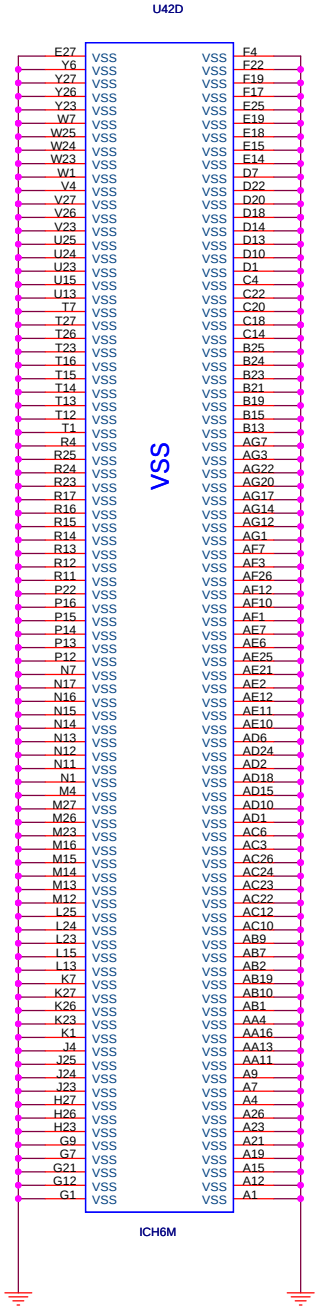




PCIRST# 3V to 5V level shift for HDD & CDROM



PCIRST# Buffer to enhance the driving strength



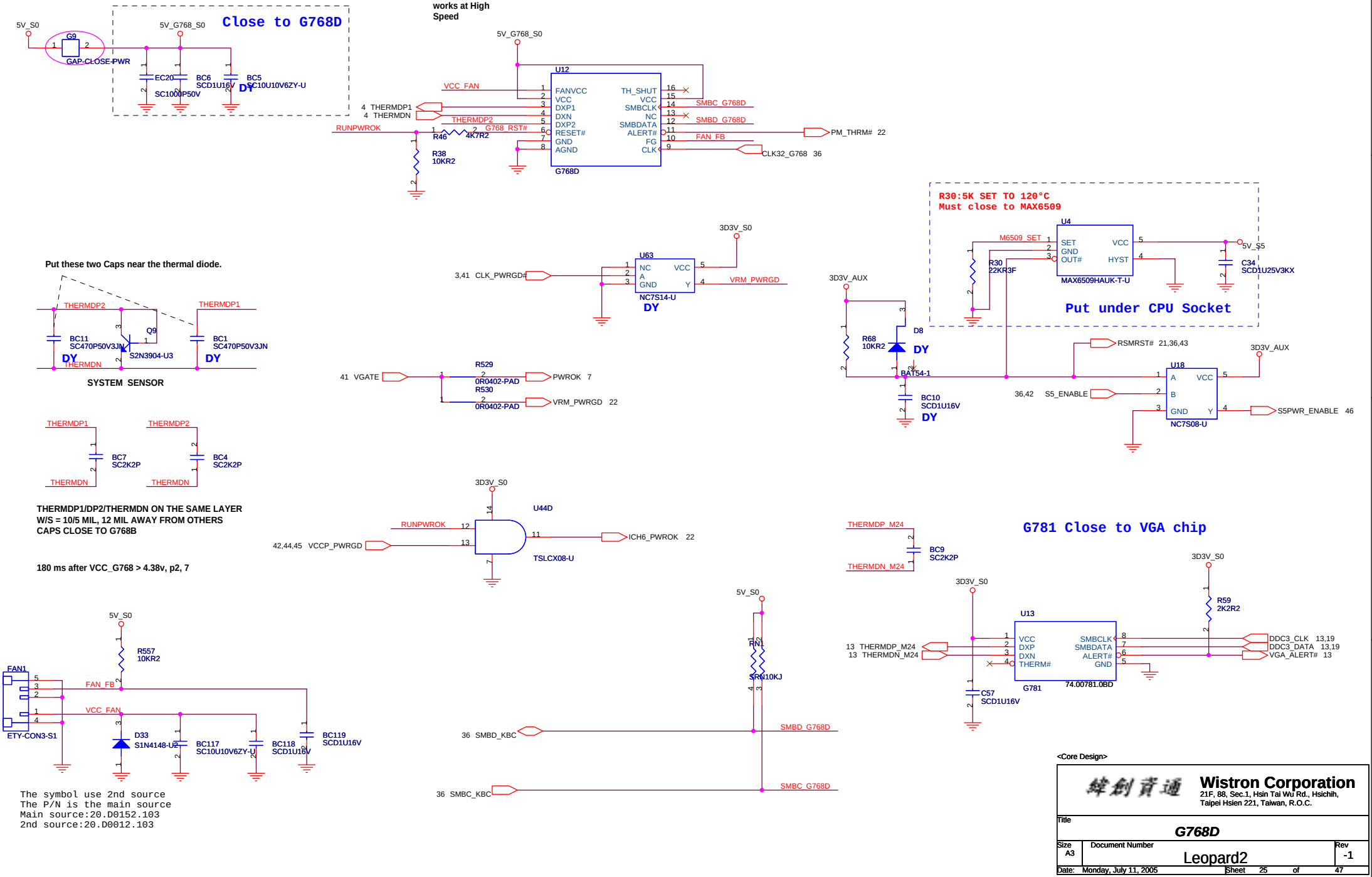
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH6-M (4 of 4)

Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Thursday, July 07, 2005 | Sheet 24 of 47



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G768D

Size	Document Number	Rev
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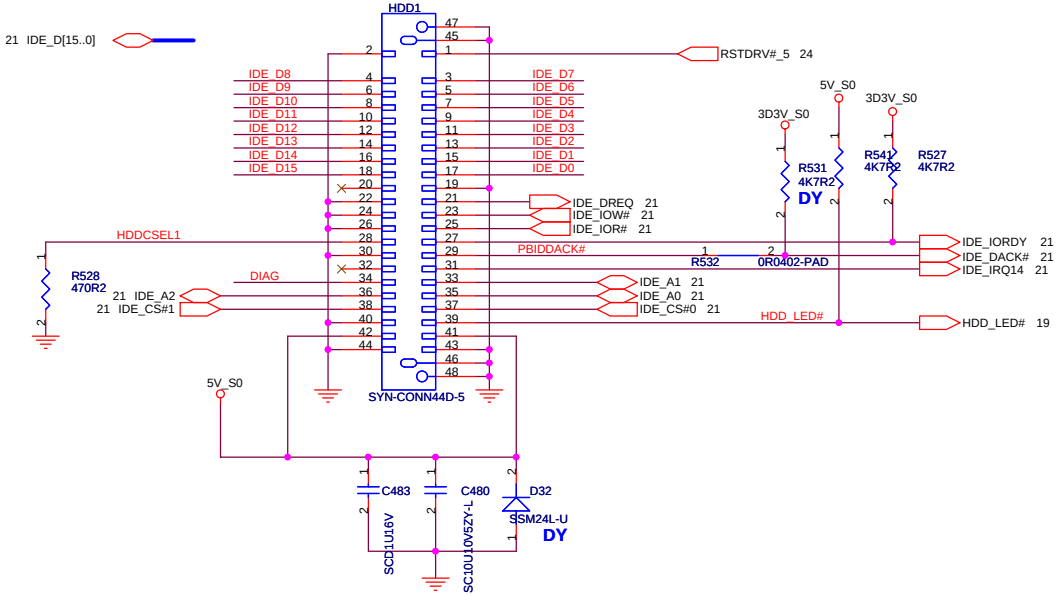
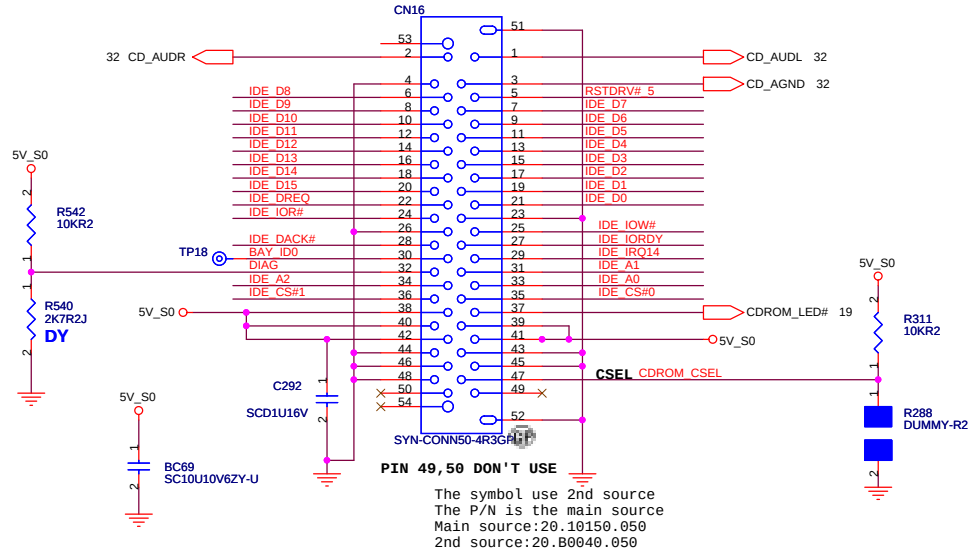
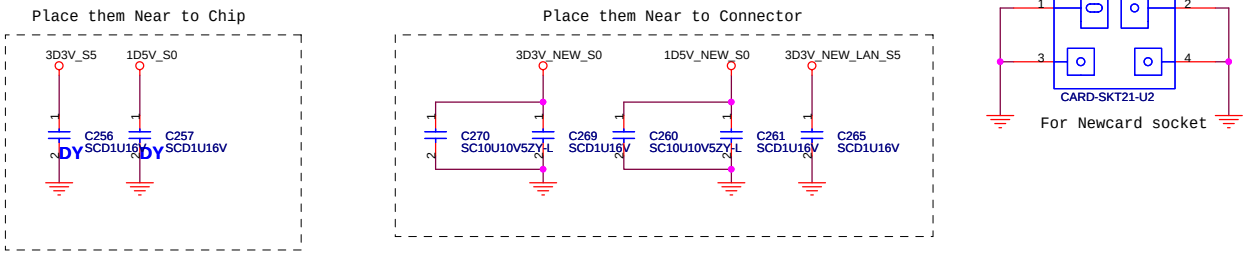
HDD Connector

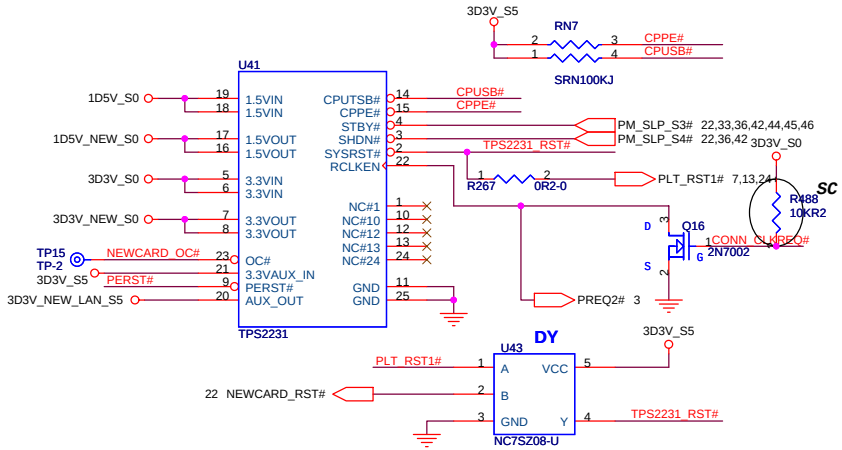


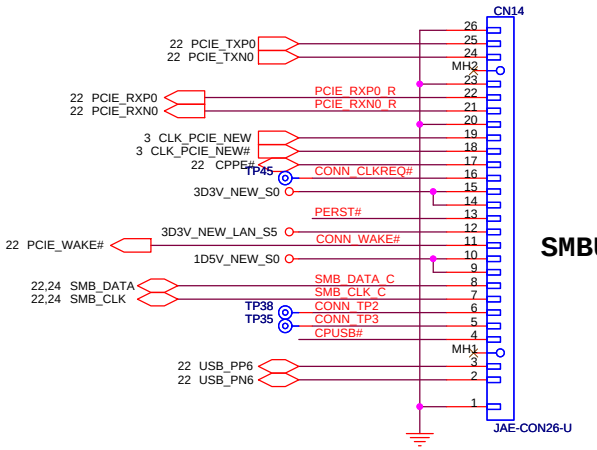
CDROM



NEWCARD Connector







SMBUS(ICH6--NEWCARD,LAN)

<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD / CDROM/NEWCARD		
Size: A3	Document Number: Leopard2	Rev: -1
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INTA# CARBUS 1
INTB# NONE
INTC# 1394
INTD# CARD READER

1 of 4

U47A

PCI7411-1

CARD BUS

1394

SD/SDIO

UNUSED TERMINALS

Bypass/Decupoling Capacitors
Should be places as close to
PCI7421 as possible

* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible

SD
MS/MS_pro

MS/MS_pro
XD

SM

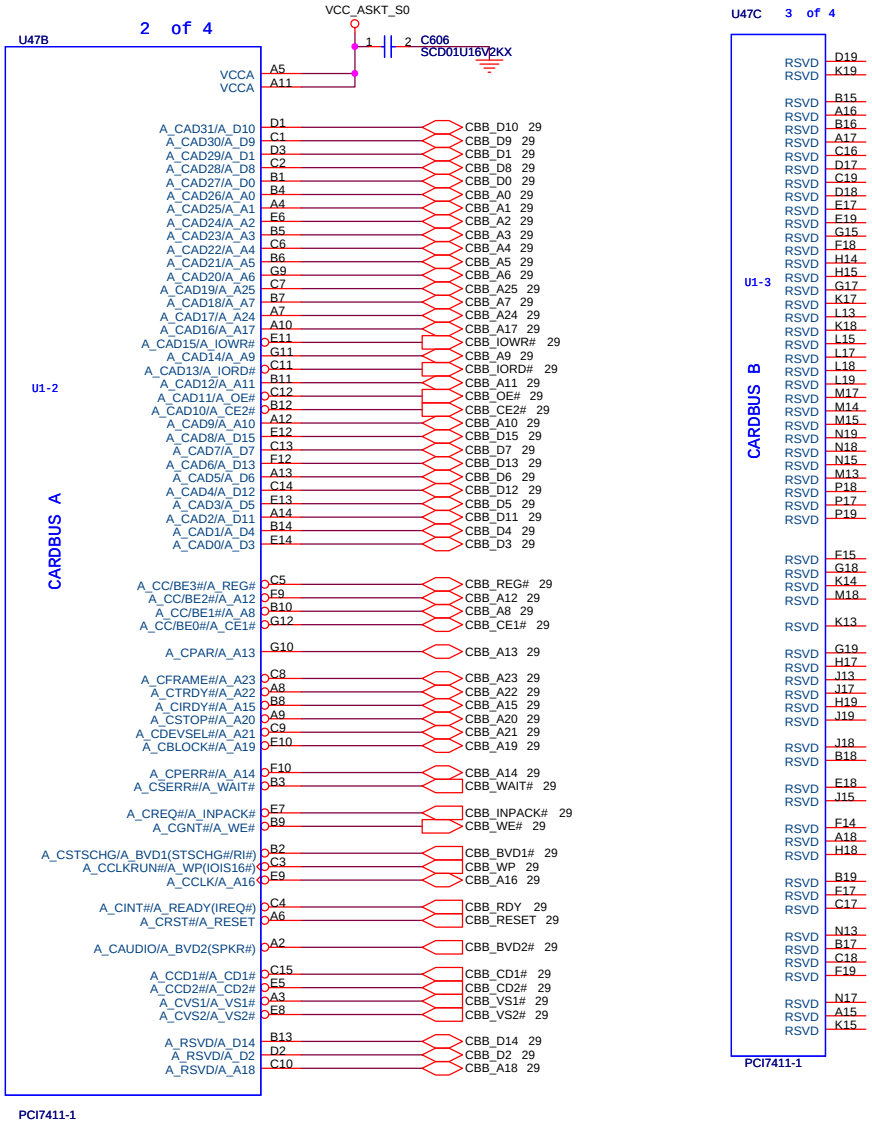
<Core Design>

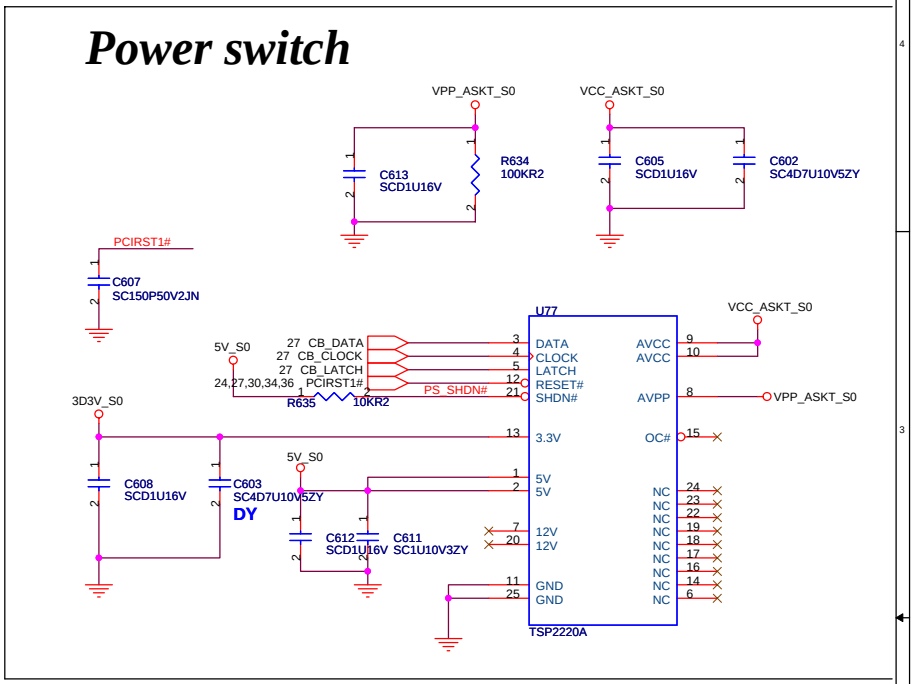
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

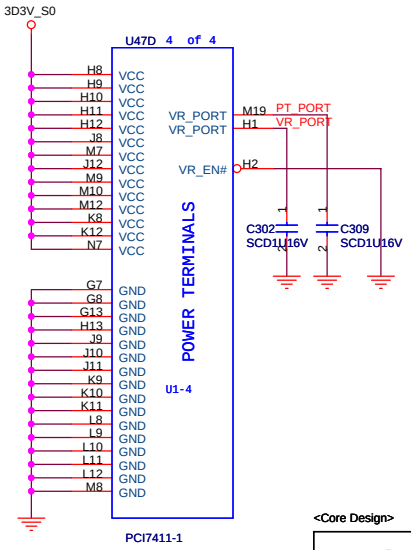
Title: TI SNC1Q21 (1 of 2)

Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Monday, July 11, 2005 | Sheet 27 of 47







<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TI PCI7411 GHK (2 of 2)

Size: A3 | Document Number: Leopard2 | Rev: -1

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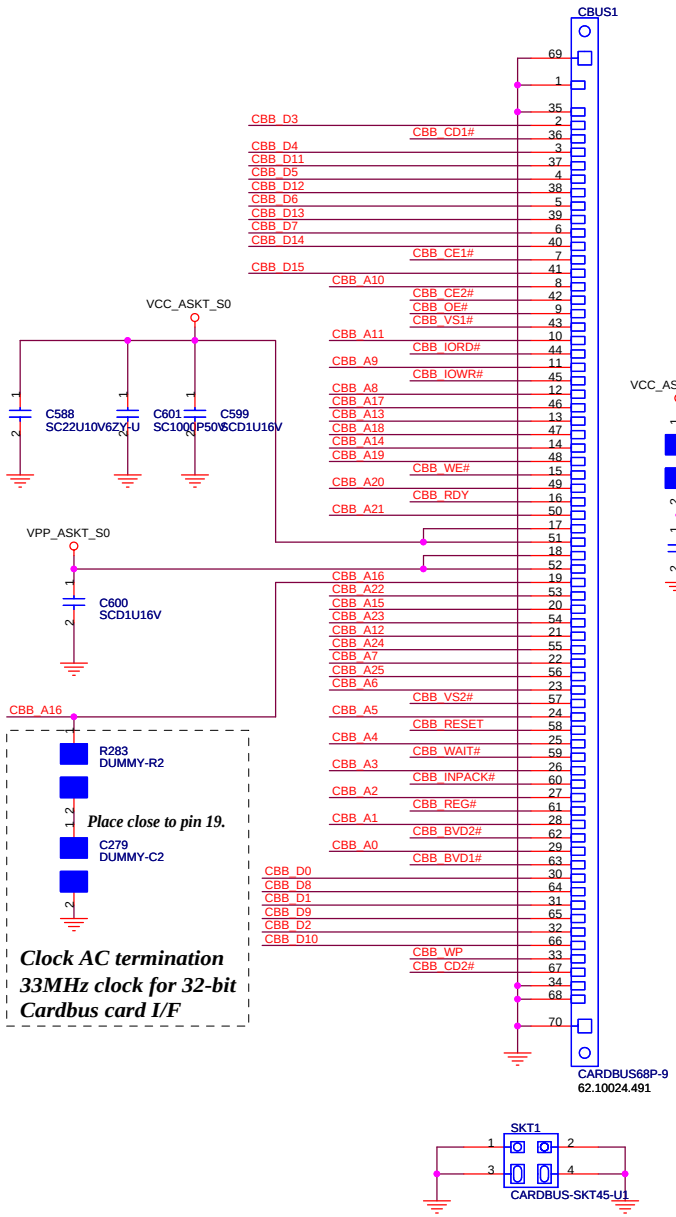
PCMCIA Socket



Cardbus I/F

CBB_D[0..15] 28
CBB_A[0..25] 28
CBB_IORD# 28
CBB_IOWR# 28
CBB_OE# 28
CBB_WE# 28
CBB_REG# 28
CBB_RDY 28
CBB_WP 28
CBB_RESET 28
CBB_WAIT# 28
CBB_INPACK# 28
CBB_CE1# 28
CBB_CE2# 28
CBB_BVD1# 28
CBB_BVD2# 28
CBB_CD1# 28
CBB_CD2# 28
CBB_VS1# 28
CBB_VS2# 28

VCC_ASKT_S0
R301 DUMMY-R2
47K
CBB_RESET
C290 SCD01U16V3KX

3D3V_CR_S0
R577 2K2R2 — SM_RE#
R216 2K2R2 — MS_BS
R558 2K2R2 DY — SM_ALE
R560 2K2R2 DY — SM_CLE
R579 2K2R2 — SM_R/B#
R578 4K7R2 — SD_WP

SKT1
CARDBUS-SKT45-U1

6 in 1 Connector

3D3V_CR_S0
C509 SCD01U16V2KX
C537 SCD01U16V2KX
C517 SCD01U16V2KX
C531 SCD01U16V2KX

SKT2
XD-VCC
S.M-VCC
MS-VCC
SD-VCC
SD-DAT0
SD-DAT1
SD-DAT2
SD-DAT3
MS-DATA0
MS-DATA1
MS-DATA2
MS-DATA3
S.M/XD-D1
S.M/XD-D2
S.M/XD-D3
S.M/XD-D4
S.M/XD-D5
S.M/XD-D6
S.M/XD-D7
S.M-LVD
S.M-CD#
S.M-D0
SM-CD-COM
SM-CD-SW
SM-WP-SW
MS-BS
MS-INS
MS-SCLK
RSV#4
XD-CD
SD-CD-COM
SD-CD-SW
SD-WP-SW
SD-CLK
SD-CMD
S.M#/XD-CLE
S.M#/XD-ALE
S.M#/XD-WE
S.M#/XD-CE
S.M#/XD-RE
S.M#/XD-R/B
S.M/XD-WP-IN
GND
SKT-MEMO-9-U1

MS_SDIO
MS_D1
MS_D2
MS_D3
R214 33R2
R212 33R2
R213 33R2
R193 33R2
SM_D4
SM_D5
SM_D6
SM_D7
SM_CD#
R559 0R2-0
DY
SM_CD#
MS_CLK_R0
MS_BS_1
R604 33R2
MS_CLK
MS_CLK_R
R599 33R2
MS_BS
SM_CLE
SM_ALE
R215 22R2
SM_RE#
SM_R/B#
R588 330R2

3D3V_S0
U34
AAT46101GV-1
OUT
GND
SET
IN
ON#
MC_PWR_CTRL 27
R228 4K7R2
C230 SCD1U16V
R239 15KR2
C239 SC1U10V3ZY

3D3V_S0
U75
NC7SZ66P5X
DY
MS_CLK
MS_CLK_R
A
B
GND
VCC
SE
SD_CD#

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA SLOT/ CARDBUS SKT
Size: A3
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Close to RTL8100C Pin121,Pin122

LAN_X1
LAN_X2
R166 DUMMY-R2
X6 XTAL-25MHZ-43
C186 SC12P50V2JN
C185 SC12P50V2JN

Close to LAN chip

TX+ TX- RX- RX+
R156 49D9R2F
R155 49D9R2F
R153 49D9R2F
R154 49D9R2F
C171 SCD1U16V
C169 SCD1U16V

3D3V_LAN_S5
R174 3K6R3
U27 M93C46-W-3
EECS_3 EESK EEDI EEDO
C225 SCD1U16V

PCI_C/BE#[0..3] 22,27,34
PCI_AD[0..31] 18,22,27,34

AVDD25 VDD25
R152 0R3-U
C176 SCD1U16V

R157 5K6R3F
TP7 TP8 TP9

U24 RTL8100CL-U

1	TX+	31 TX+	
2	TX-	31 TX-	
3	AVDD33	AVDD33	
4	GND		
5	RX+	31 RX+	
6	RX-	31 RX-	
7	AVDD33	AVDD33	
8	CTRL25	CTRL25	
9	NC		
10	NC		
11	NC		
12	AVDD25	AVDD25	
13	NC		
14	NC		
15	NC		
16	NC		
17	GND		
18	NC		
19	NC		
20	AVDD33	AVDD33	
21	GND		
22	NC		
23	ISOLATEB	ISOLATE	
24	NC		
25	INTAB	22,34 INT_PIRQE#	
26	VDD33	3D3V_LAN_S5	
27	PCIRSTB	24,27,28,34,36 PCIRST1#	
28	PCICLK	3 PCLK_LAN	
29	GNTB	22 PCI_GNT#2	
30	REQB	22 PCI_REQ#2	
31	PMEB	18,22,34 ICH_PME#	
32	VDD25	VDD25	
33	PCIAD31	PCI_AD31	
34	PCIAD30	PCI_AD30	
35	GND		
36	PCIAD29	PCI_AD29	
37	PCIAD28	PCI_AD28	
38	GND		
39	PCIAD27	PCI_AD27	
40	PCIAD26	PCI_AD26	
41	PCIAD25	PCI_AD25	
42	PCIAD24	PCI_AD24	
43	CBEB3	PCI_C/BE#3	
44	IDSEL	LAN_IDSEL	
45	NC		
46	PCIAD23	PCI_AD23	
47	NC		
48	PCIAD22	PCI_AD22	
49	PCIAD21	PCI_AD21	
50	GND		
51	PCIAD20	PCI_AD20	
52	VDD25	VDD25	
53	PCIAD19	PCI_AD19	
54	VDD33		
55	PCIAD18	PCI_AD18	
56	PCIAD17	PCI_AD17	
57	PCIAD16	PCI_AD16	
58	CBEB2	PCI_C/BE#2	
59	FRAMEB	PCI_FRAME# 22,27,34	
60	NC		
61	IRDYB	PCI_IRDY# 22,27,34	
62	NC		
63	GND		
64	CLKRUNB	PM_CLKRUN# 22,27,34,36	
65	GND		
66	PERRB	PCI_PERR# 22,27,34	
67	STOPB	PCI_STOP# 22,27,34	
68	DEVSELB	PCI_DEVSEL# 22,27,34	
69	TRDYB	PCI_TRDY# 22,27,34	
70	GND		
71	NC		
72	NC		
73	NC		
74	SERRB	PCI_PAR 22,27,34 / PCI_SERR# 22,27,34	
75	PAR	PCI_PAR	
76	CBEB1	PCI_C/BE#1	
77	VDD25	VDD25	
78	PCIAD15	PCI_AD15	
79	GND		
80	GND		
81	PCIAD14	PCI_AD14	
82	PCIAD13	PCI_AD13	
83	VDD33		
84	PCIAD12	PCI_AD12	
85	PCIAD11	PCI_AD11	
86	PCIAD10	PCI_AD10	
87	NC		
88	PCIAD9	PCI_AD9	
89	PCIAD8	PCI_AD8	
90	GND		
91	CBEB0	PCI_C/BE#0	
92	PCIAD7	PCI_AD7	
93	VDD33		
94	PCIAD6	PCI_AD6	
95	PCIAD5	PCI_AD5	
96	PCIAD4	PCI_AD4	
97	PCIAD3	PCI_AD3	
98	VDD25	VDD25	
99	GND		
100	PCIAD2	PCI_AD2	
101	PCIAD1	PCI_AD1	
102	PCIAD0	PCI_AD0	
103	LANWAKE		
104	EECS	EECS_3	
105	VDD33		
106	EEDO	EEDO	
107	EEDI	EEDI	
108	EESK	EESK	
109	LED2	LAN_LED2	
110	LED1	LAN_LED1	
111	LED0	LAN_LED0	
112	NC		
113	NC		
114	NC		
115	GND		
116	NC		
117	XTAL1	LAN_X1	
118	XTAL2	LAN_X2	
119	NC		
120	NC		
121	NC		
122	NC		
123	GND		
124	GND		
125	NC		
126	NC		
127	RSET		
128	GND		

3D3V_LAN_S5
R165 100R2
PCI_AD23

3D3V_S0
R150 1KR2
R149 15KR2
ISOLATE

3D3V_LAN_S5
C189 C213 C215 C184 C216 C198 C174 SCD1U16V

3D3V_LAN_S5
CTRL25 R151 0R2-0 LAN_PWR_CTRL
CHP69 Q11
G19 GAP-CLOSE-PWR
C167 SC22U10V6ZY-U
VDD25
C173 C188 C214 C217 SCD1U16V

3D3V_LAN_S5
L14 BLM11A601S
AVDD33
C178 C170 C177 C175 SCD1U16V
DY

3D3V_S5 3D3V_LAN_S5
G23 GAP-CLOSE-PWR

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8100C
Size: A3
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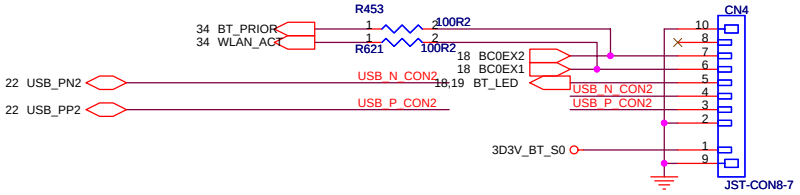
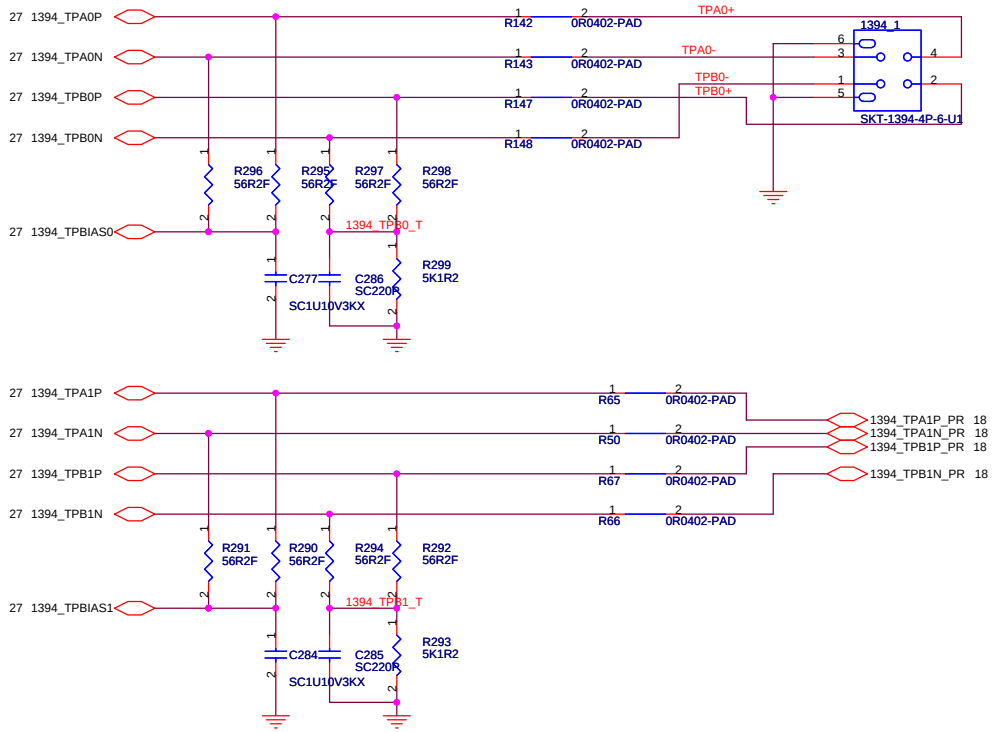
Blue thumb

Place on bottom side
From NEW!
1004-1



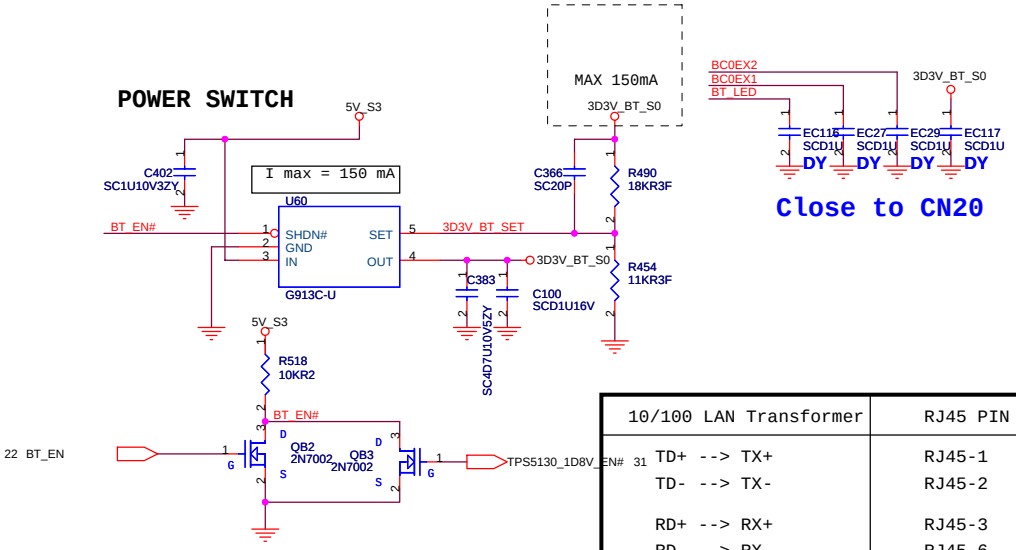
BC0EX2 connect to PCI_AD22 on main board.
BC0EX1 connect to ICH_PME# on main board.

1394 Connector



These components near to chip side.

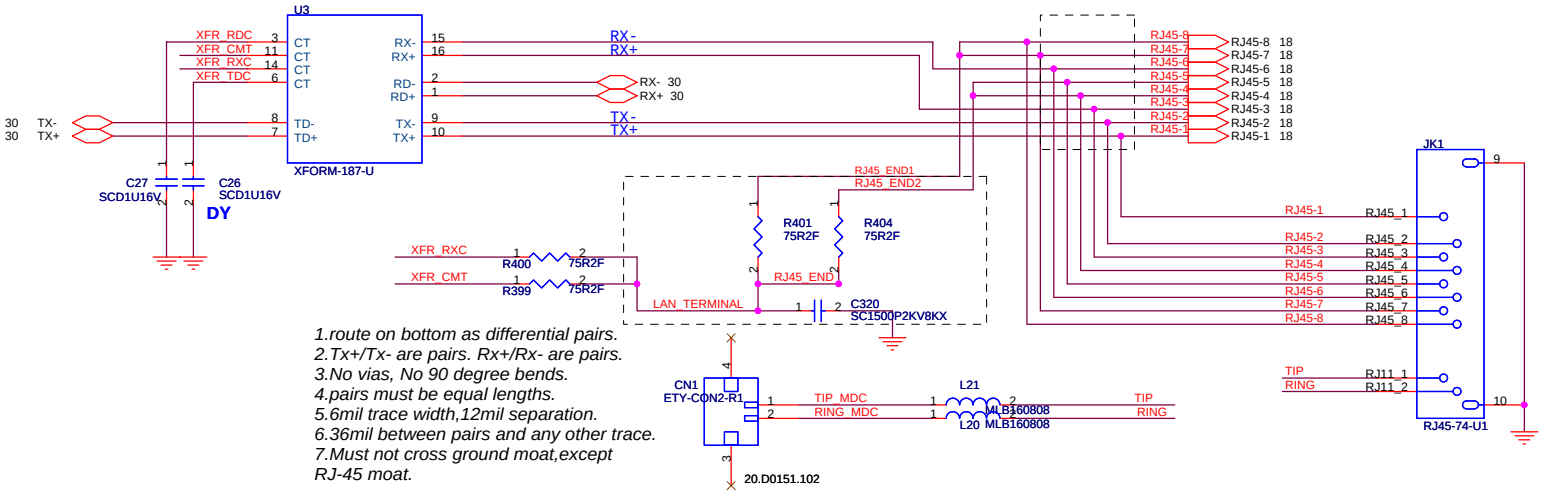
POWER SWITCH



Close to CN20

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

10/100M Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

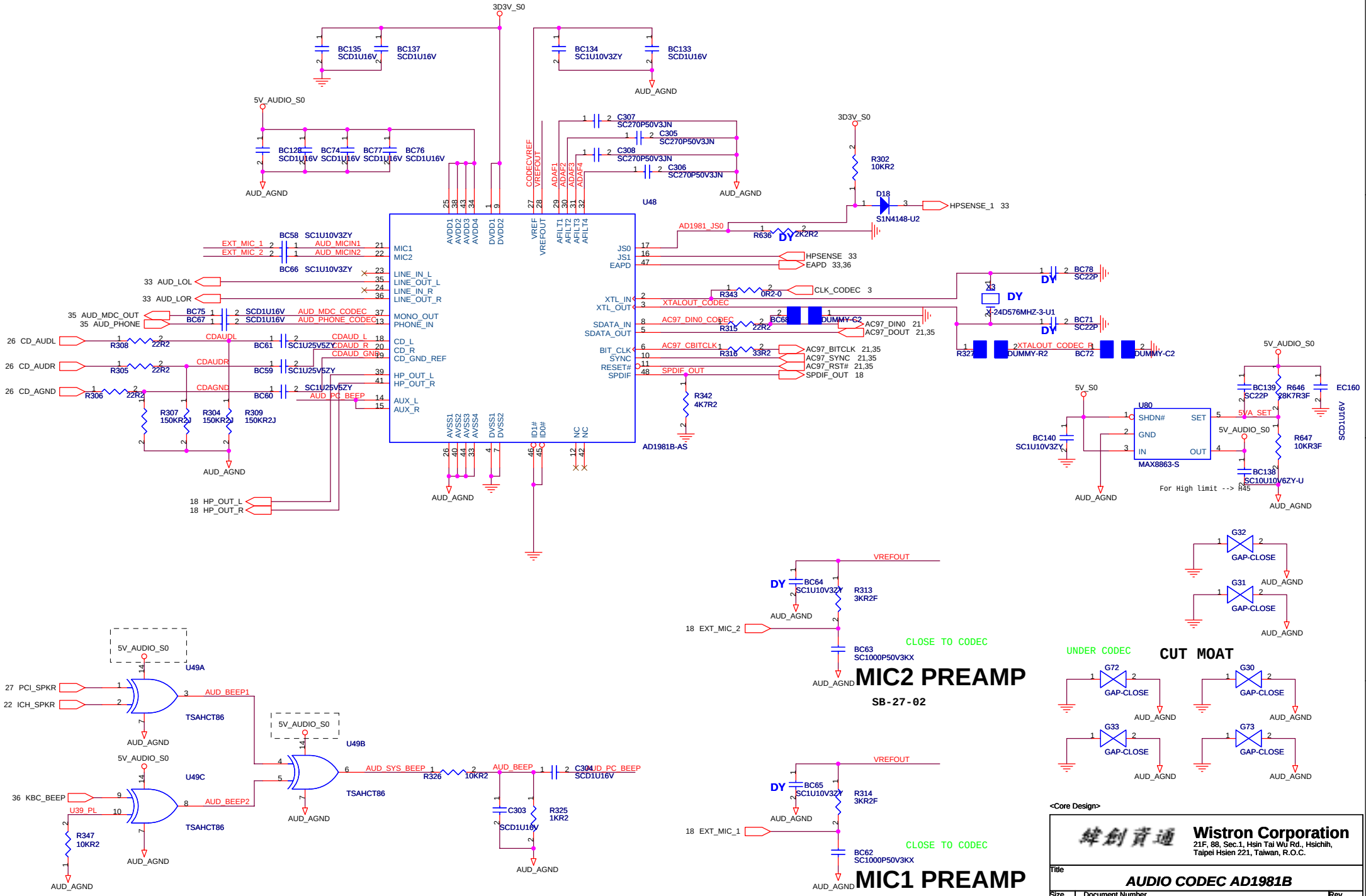
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN / 1394 Connector***

Size	Document Number	Rev
A3	Leopard2	-1

Date: Monday, July 11, 2005 Sheet 31 of 47



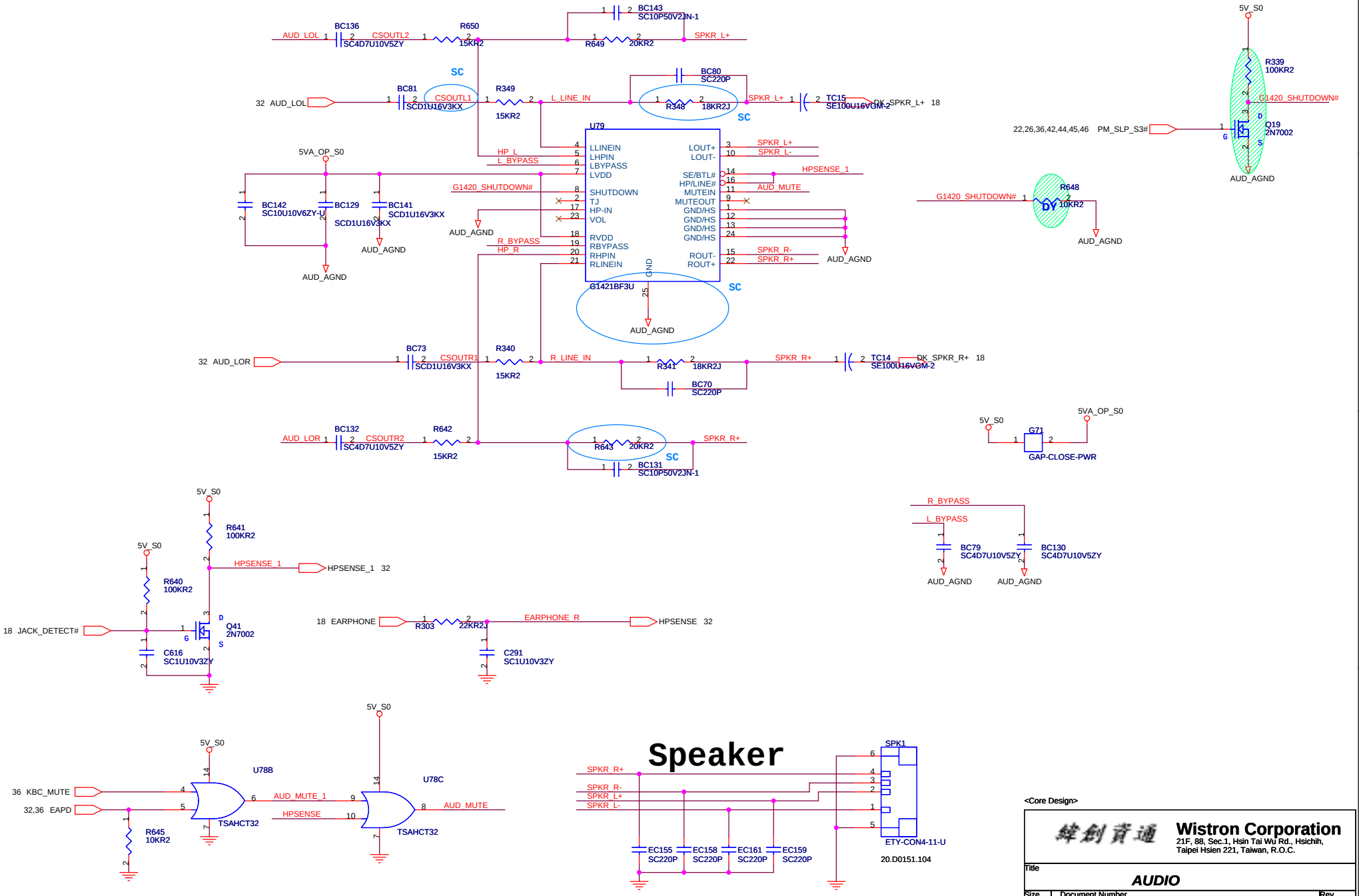
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC AD1981B

Size	Document Number	Rev
A3	Leopard2	-1

Date: Monday, July 11, 2005 Sheet 32 of 47



<Core Design>

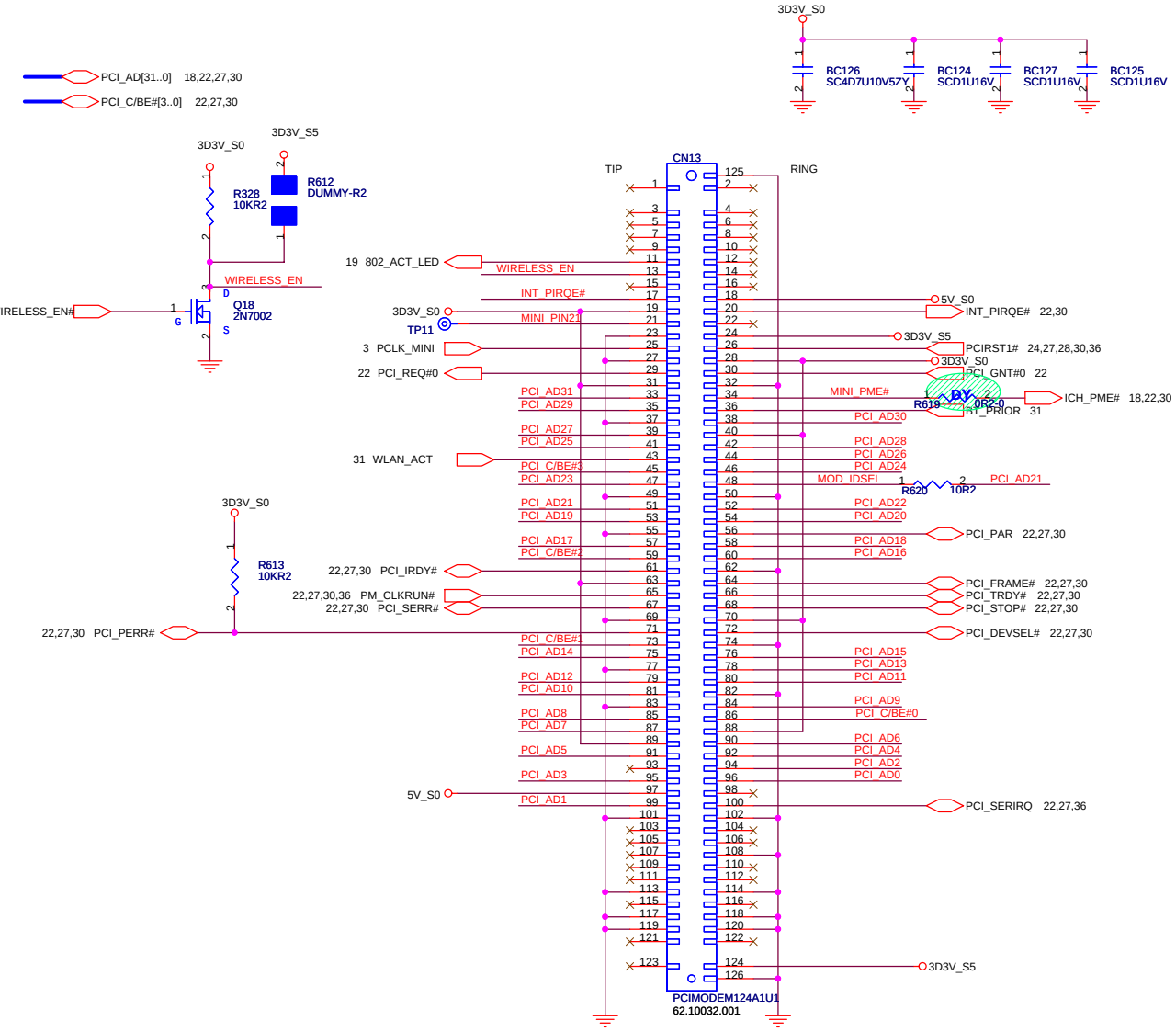
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO**

Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 33 of 47

MINI-PCI



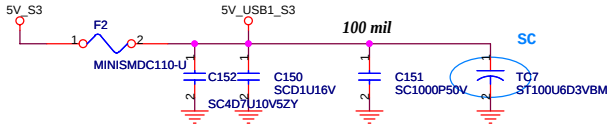
The symbol use 2nd source
The P/N is the main source
Main source:62.10032.001
2nd source:62.10032.031

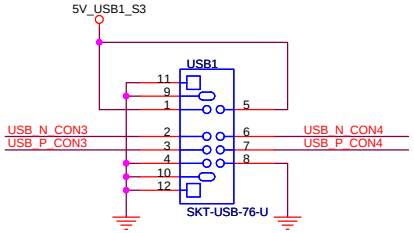
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

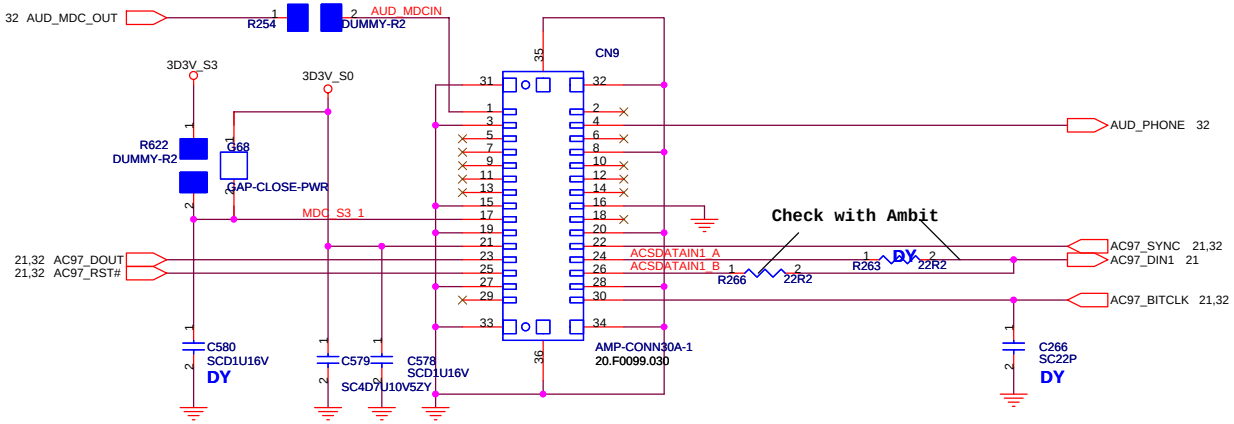
Title	MINI-PCI	
Size A3	Document Number Leopard2	Rev -1
Date: Thursday, July 07, 2005	Sheet 34 of 47	

USB POWER





MDC Connector



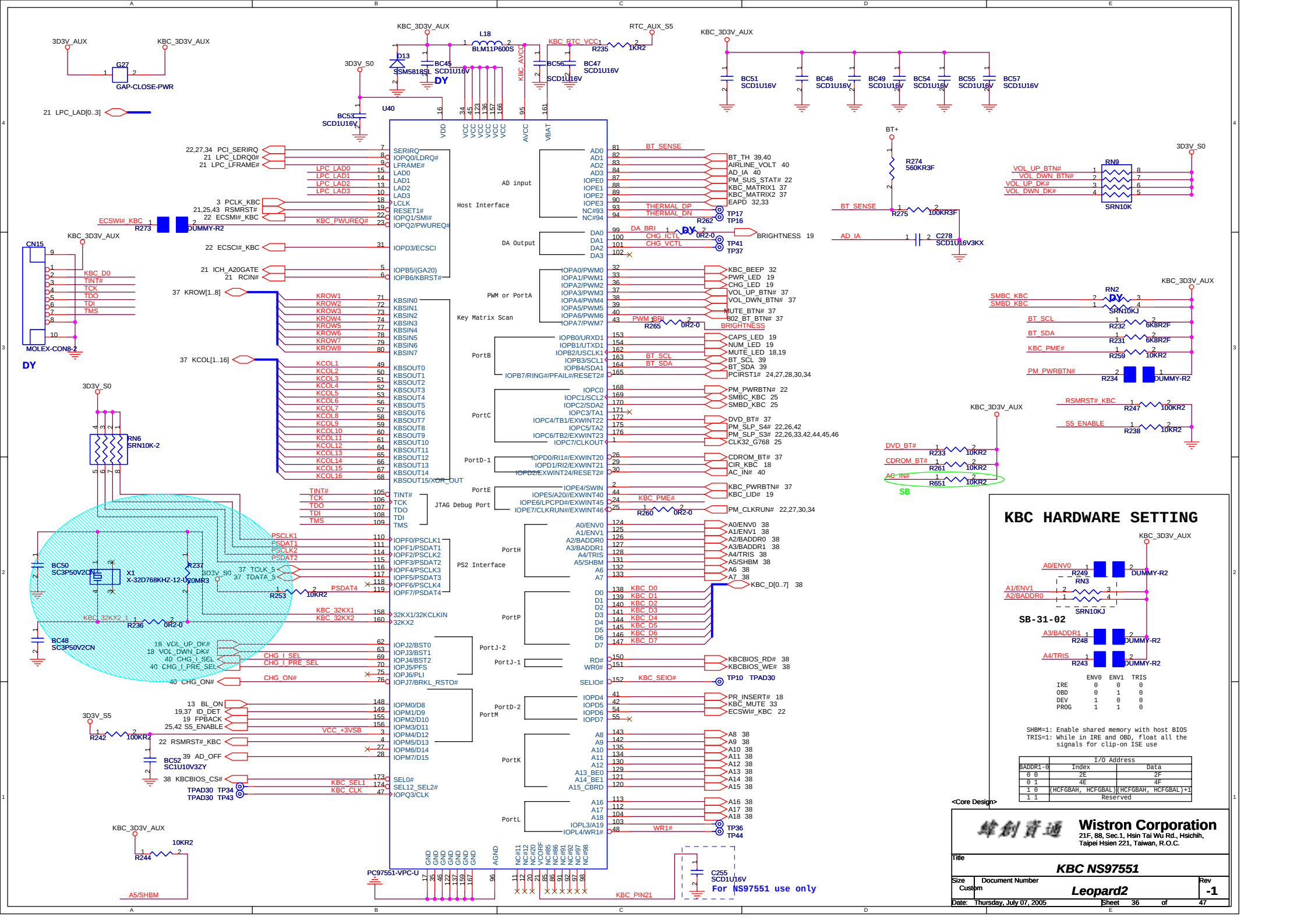
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB / MDC CONN.***

Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 35 of 47


KBC HARDWARE SETTING
SB-31-02
ENV0 ENV1 TRIS
IRE 0 0 0
OBD 0 1 0
DEV 1 0 0
PROG 1 1 0
SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use
I/O Address
BADDR1-0 Index Data
0 0 2E 2F
0 1 4E 4F
1 0 (HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1
1 1 Reserved
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC NS97551
Size Custom
Document Number Leopard2
Rev -1
Date: Thursday, July 07, 2005
Sheet 36 of 47
U40
PC97551-VPC-U
Host Interface
AD input
DA Output
PWM or PortA
Key Matrix Scan
PortB
PortC
PortD-1
PortE
JTAG Debug Port
PS2 Interface
PortH
PortP
PortJ-2
PortJ-1
PortD-2
PortM
PortK
PortL
For NS97551 use only
DY
SB

INTERNAL KEYBOARD CONNECTOR

KROW[1..8] 36

KCOL[1..16] 36

CN8

ETY-CON24-1
20.K0170.001

3D3V_S0

R406 10KR2

802_BT_BTN#

3D3V_S0

R415 10KR2

MUTE_BTN#

KBC_3D3V_AUX

R278 10KR2 DY

R277 10KR2 DY

R279 10KR2

R276 10KR2

KBC_MATRIX2 36

KBC_MATRIX1 36

the matrix table for PCB

KBC_MATRIX2,KBC_MATRIX1

	PA	PR
Discrete	00	01
UMA	10	11

3D3V_S0

D28

VOL_UP_BTN# 3

BAV99LT1 DY

3D3V_S0

D29

VOL_DWN_BTN# 3

BAV99LT1 DY

LAUNCH Board

POWER BUTTON

3D3V_AUX

R407 10KR2

36 KBC_PWRBTN#

R416 470R2

PWRBTN#

BC86 SCD1U16V

36 DVD_BT#

36 CDROM_BT#

DVD_BT#

CDROM_BT#

EC101 SC1000P16V2KX

EC100 SC1000P16V2KX

5V_S3

CN2

C335 SCD1U10V2MX-1

C336 SCD1U10V2MX-1

5V_S0

19 PWR_LED#
19 MUTE_LED#
19 802_BT_LED#
36 VOL_UP_BTN#
36 VOL_DWN_BTN#
36 802_BT_BTN#
19,36 ID_DET
19 NUM_LED#
36 MUTE_BTN#

JST-CON20

VOL_DWN_BTN#
VOL_UP_BTN#
802_BT_LED#
MUTE_LED#
PWR_LED#
NUM_LED#

EC99 EC94 EC95 EC96 EC97 EC98

SC1000P16V2KX

TouchPad Connector

5V_S3

R555 10KR2

R556 10KR2

36 TDATA_5

36 TCLK_5

CN7

BC115 BC116 BC30 BC114

DY SC47P50V2JN

DY SC47P50V2JN

DY SC1U10V3Z7Y

DY SCD1U16V

ETY-CON8-5

KCOL9 KCOL8 KCOL5 KCOL3

RC2 SRC100P50V-U

KROW1 KCOL2 KCOL6 KROW4

RC4 SRC100P50V-U

KCOL14 KCOL13 KCOL4 KCOL7

RC3 SRC100P50V-U

KCOL16 KCOL11 KCOL12 KCOL15

RC1 SRC100P50V-U

for EMI

for EMI

KROW3 KCOL1 KROW6 KROW5

RC5 SRC100P50V-U

KCOL10 KROW7 KROW8 KROW2

RC6 SRC100P50V-U

for EMI

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KEYBOARD/TOUCH PAD/Launch key

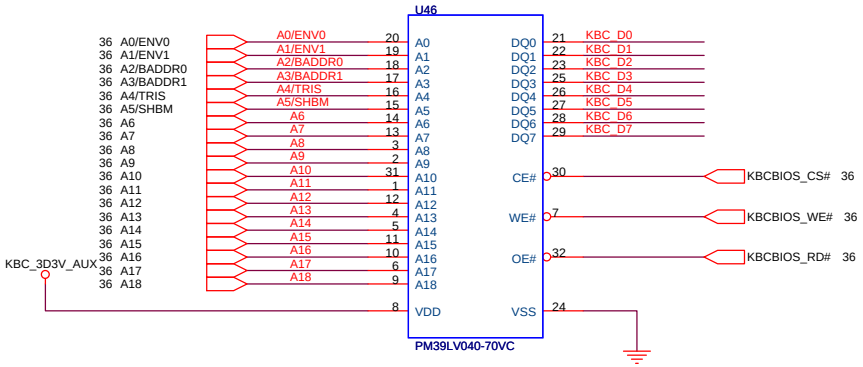
Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Thursday, July 07, 2005 | Sheet 37 of 47

KBC_D[0..7] 36

FLASH ROM

512KB Flash



<Core Design>

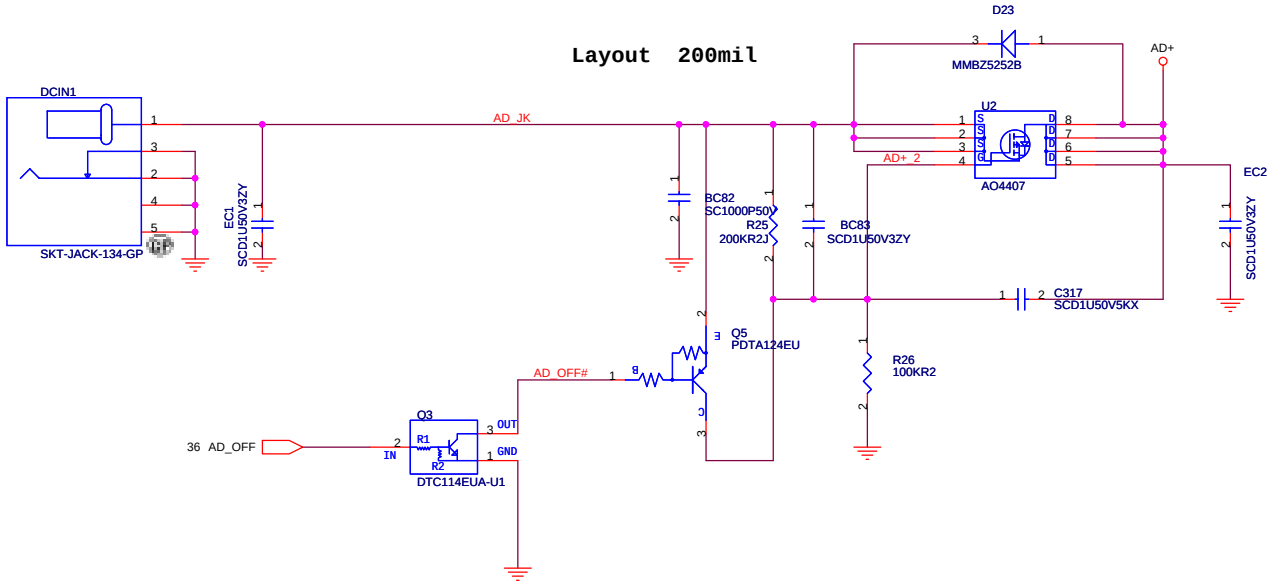
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

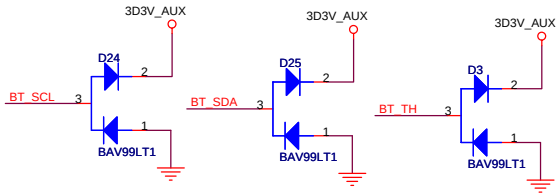
Title: BIOS/GF

Size: A3 | Document Number: Leopard2 | Rev: -1

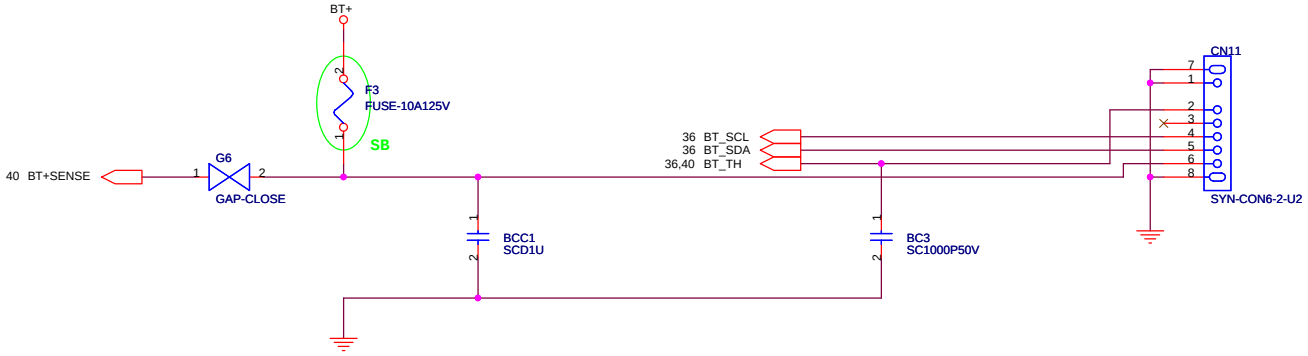
Date: Thursday, July 07, 2005 | Sheet 38 of 47

Adaptor in to generate DCBATOUT



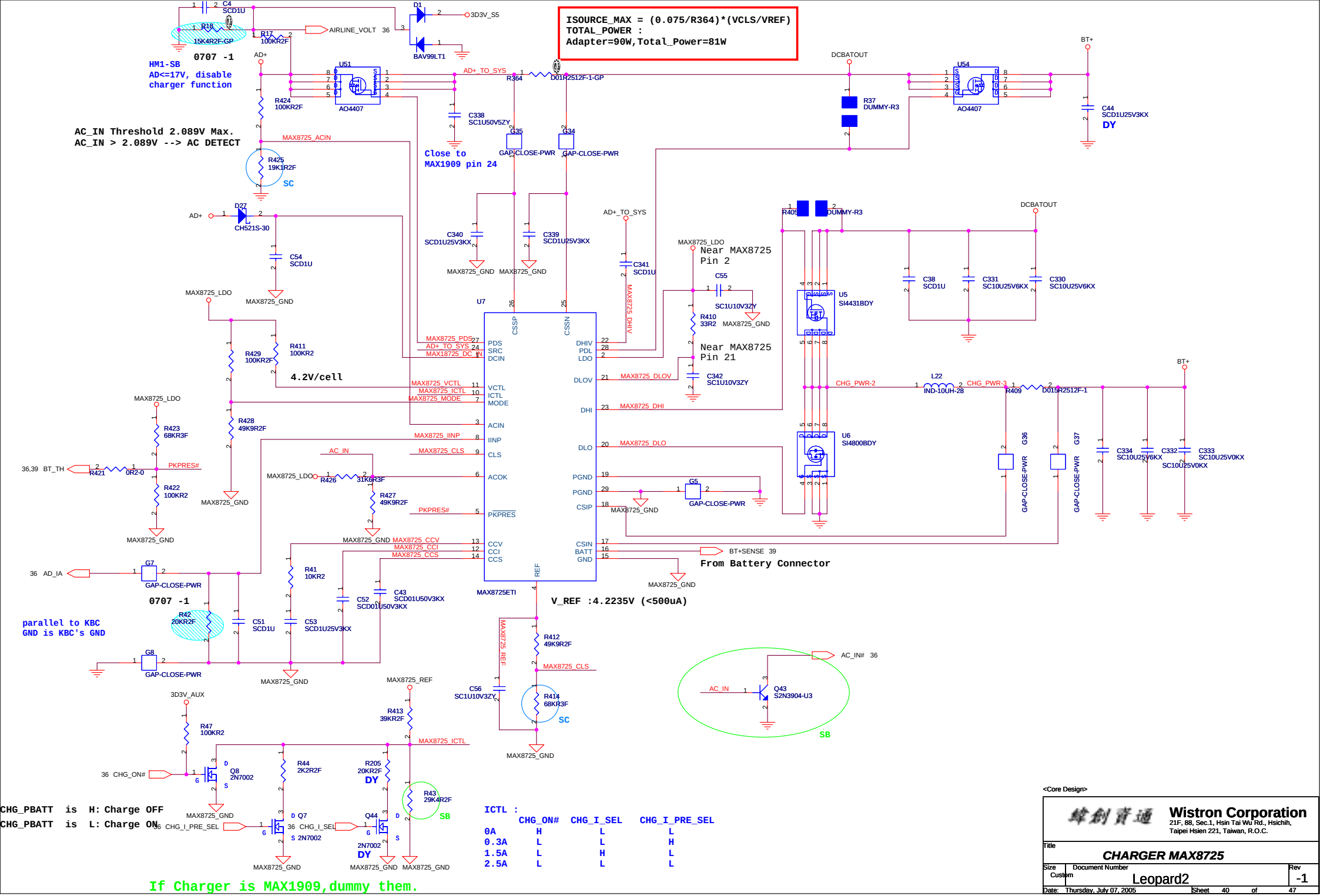


BATTERY CONNECTOR

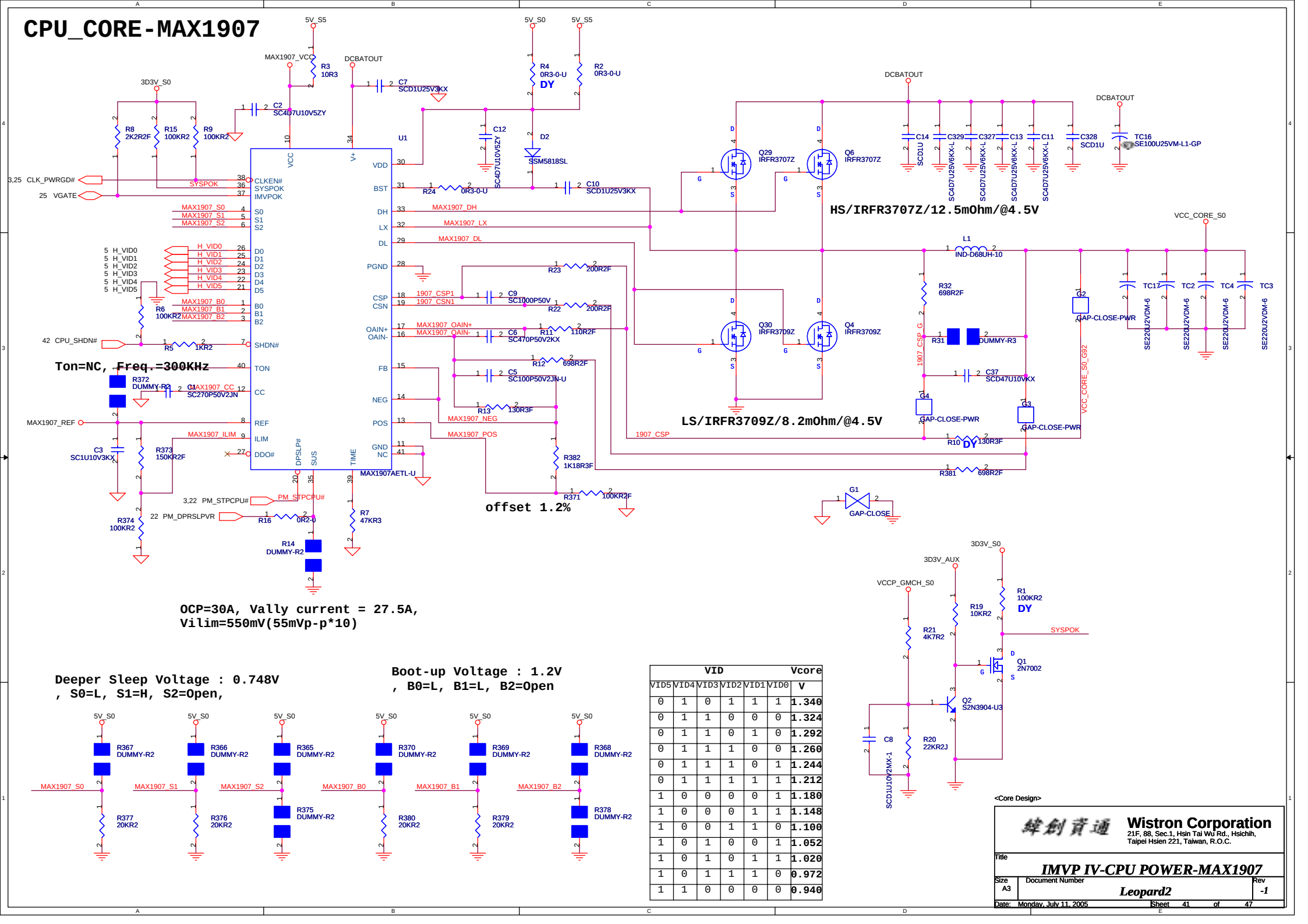


<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Adaptor/ Bettery conn.***
Size A3 / Document Number	Leopard2 / Rev -1
Date: Thursday, July 07, 2005	Sheet 39 of 47


ISOURCE_MAX = (0.075/R364)*(VCLS/VREF)
TOTAL_POWER :
Adapter=90W,Total_Power=81W
HM1-SB
AD<=17V, disable charger function
0707 -1
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
Close to MAX1909 pin 24
4.2V/cell
Near MAX8725 Pin 2
Near MAX8725 Pin 21
From Battery Connector
V_REF :4.2235V (<500uA)
parallel to KBC
GND is KBC's GND
MAX8725ETI
SC
SB
DY
CHG_PBATT is H: Charge OFF
CHG_PBATT is L: Charge ON
If Charger is MAX1909,dummy them.
ICTL :
CHG_ON# CHG_I_SEL CHG_I_PRE_SEL
0A H L L
0.3A L L H
1.5A L H L
2.5A L L L
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8725
Size Custom
Document Number Leopard2
Rev -1
Date: Thursday, July 07, 2005
Sheet 40 of 47

CPU_CORE-MAX1907



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IMVP IV-CPU POWER-MAX1907

Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Monday, July 11, 2005 | Sheet 41 of 47

TI TPS5130 for 1D8V, 3D3V, 5V

(1D8V=>CH1 , 3D3V=>CH2 , 5V =>CH3)

For 3.3V
SETTING=3.349V

For 5V
SETTING=5.0915V

For 1.8V
SETTING=1.82V

close to IC

Vo=(R1*0.85)/R2+0.85

T(soft)=1.736ms

0703 -1

1D8V_OCP
SC
DCBATOUT
OCP
8.2A=>R186=13K
close to IC

3D3V_OCP
SC
DCBATOUT
OCP
5.82A=>R182=10K
close to IC

5V_OCP
SC
DCBATOUT
OCP
8.88A=>R207=15K
close to IC

TPS5130

TPS5130PT-U

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

HW Thermal Throttling

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

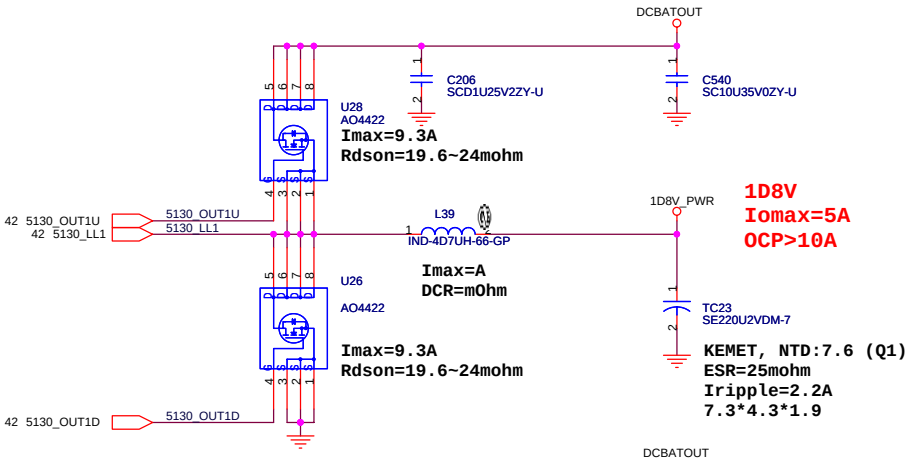
Title: TPS5130 (3D3V/5V/1D8V)

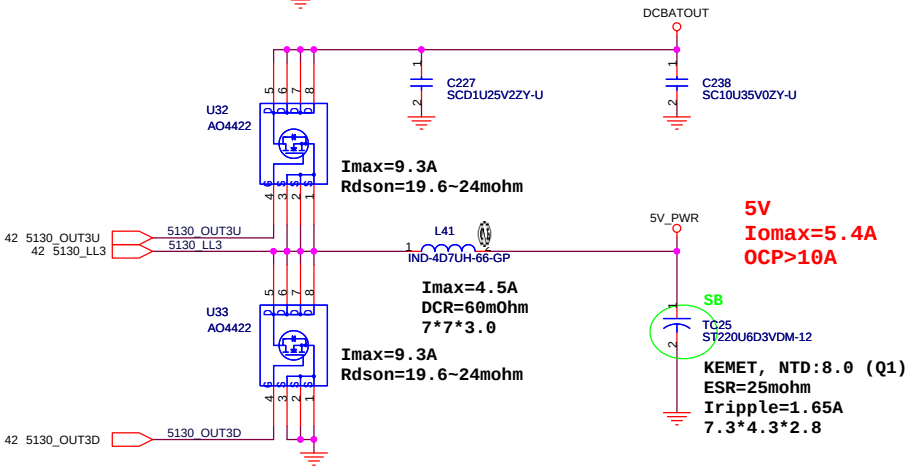
Size: A3 | Document Number: Leopard2 | Rev: -1

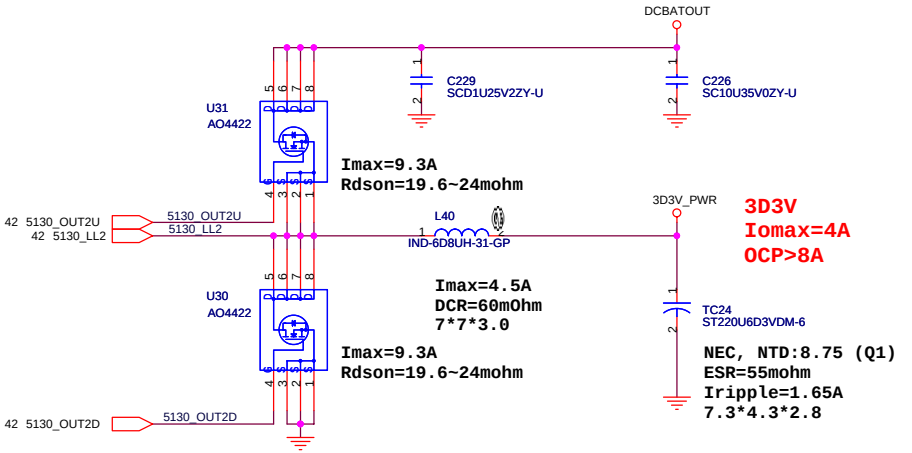
Date: Thursday, July 07, 2005 | Sheet 42 of 47

TI TPS5130 for 1D2V, 5V, 3D3V

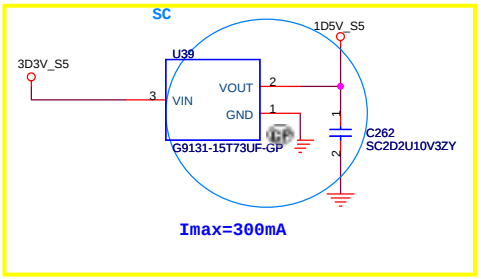
(1D2V=>CH1 , 5V=>CH2 , 3D3V =>CH3)

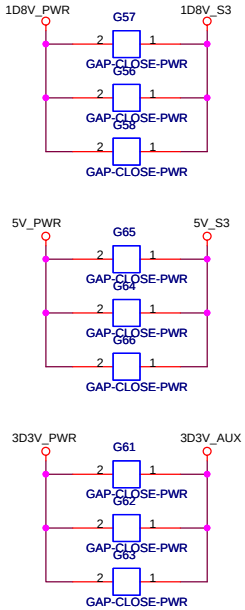


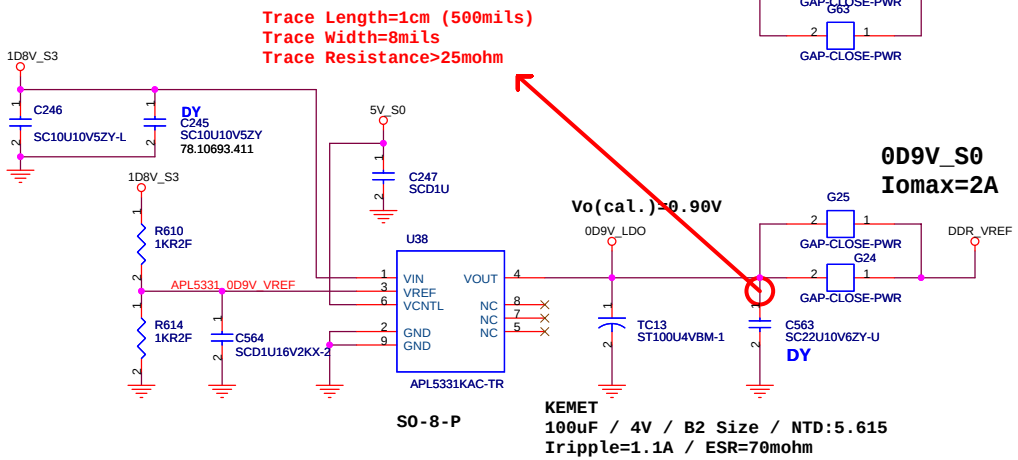




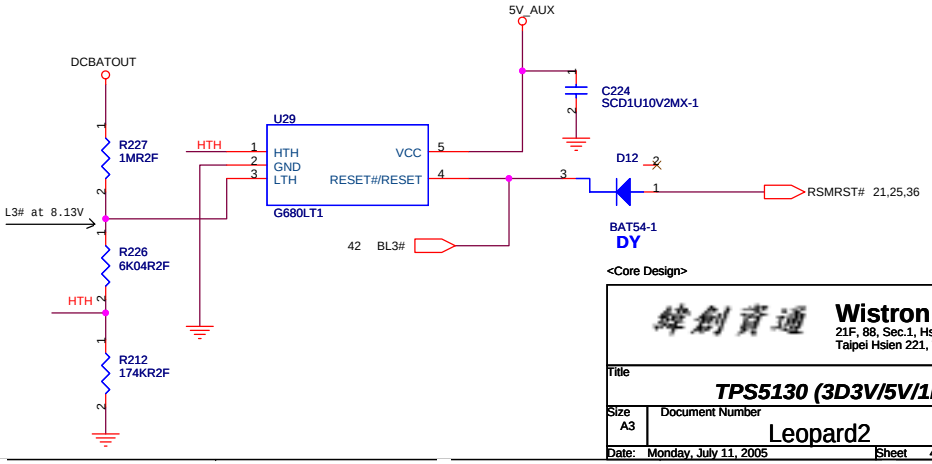
1.5V_S5 (For ICH6)







L3# circuit



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

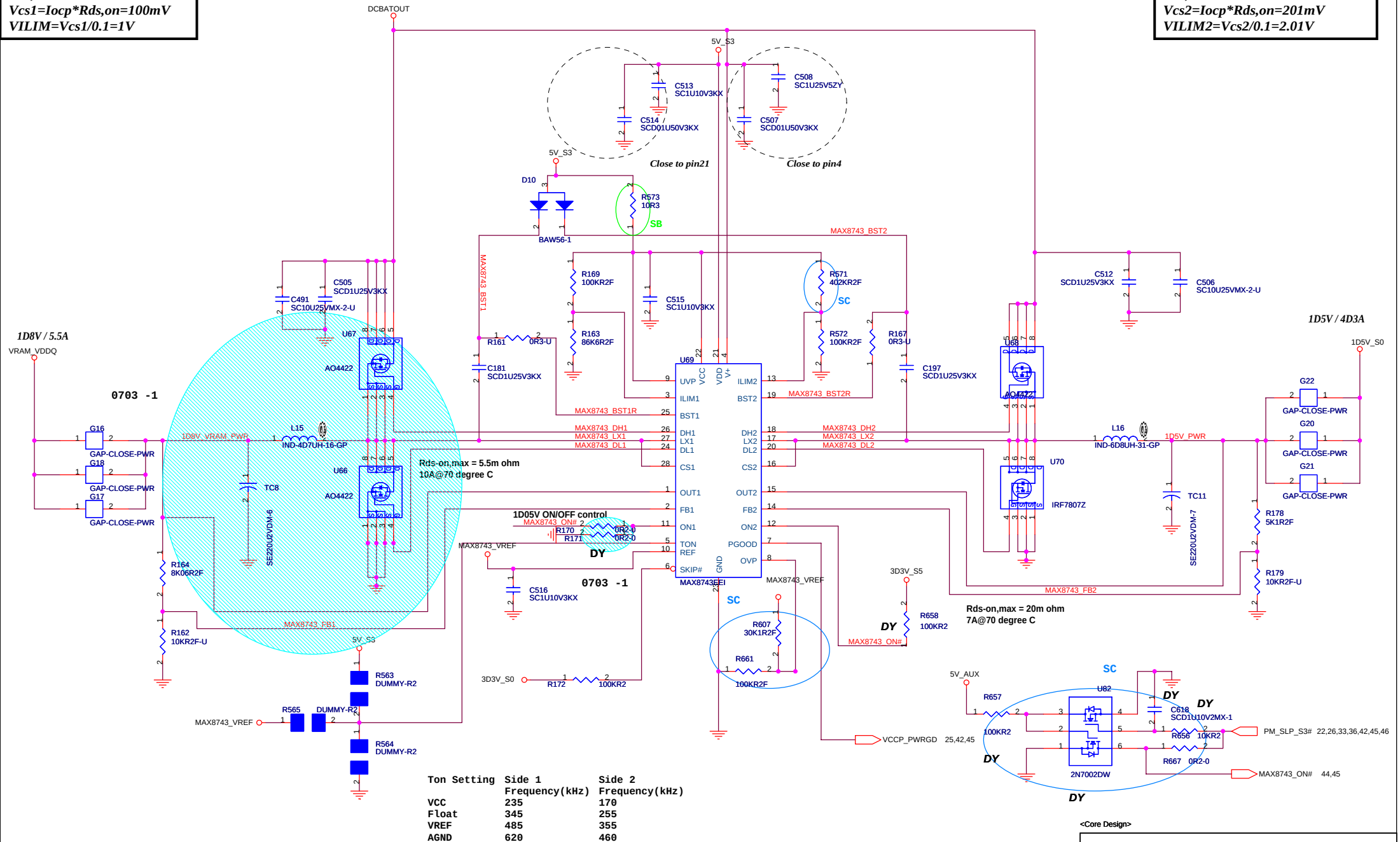
Title: *TPS5130 (3D3V/5V/1D8V/0D9V)*

Size	Document Number	Rev
A3	Leopard2	-1

Date: Monday, July 11, 2005 Sheet 43 of 47

*Iocp=7.8 * 1.7 = 13.3A*
*Rds,on=5.5*1.375=7.563m ohm*
*Vcs1=Iocp*Rds,on=100mV*
VILIM=Vcs1/0.1=1V

*Iocp=4.3 * 1.7 = 7.3A*
*Rds,on=20*1.375=27.5m ohm*
*Vcs2=Iocp*Rds,on=201mV*
VILIM2=Vcs2/0.1=2.01V



Ton Setting	Side 1 Frequency(kHz)	Side 2 Frequency(kHz)
VCC	235	170
Float	345	255
VREF	485	355
AGND	620	460

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

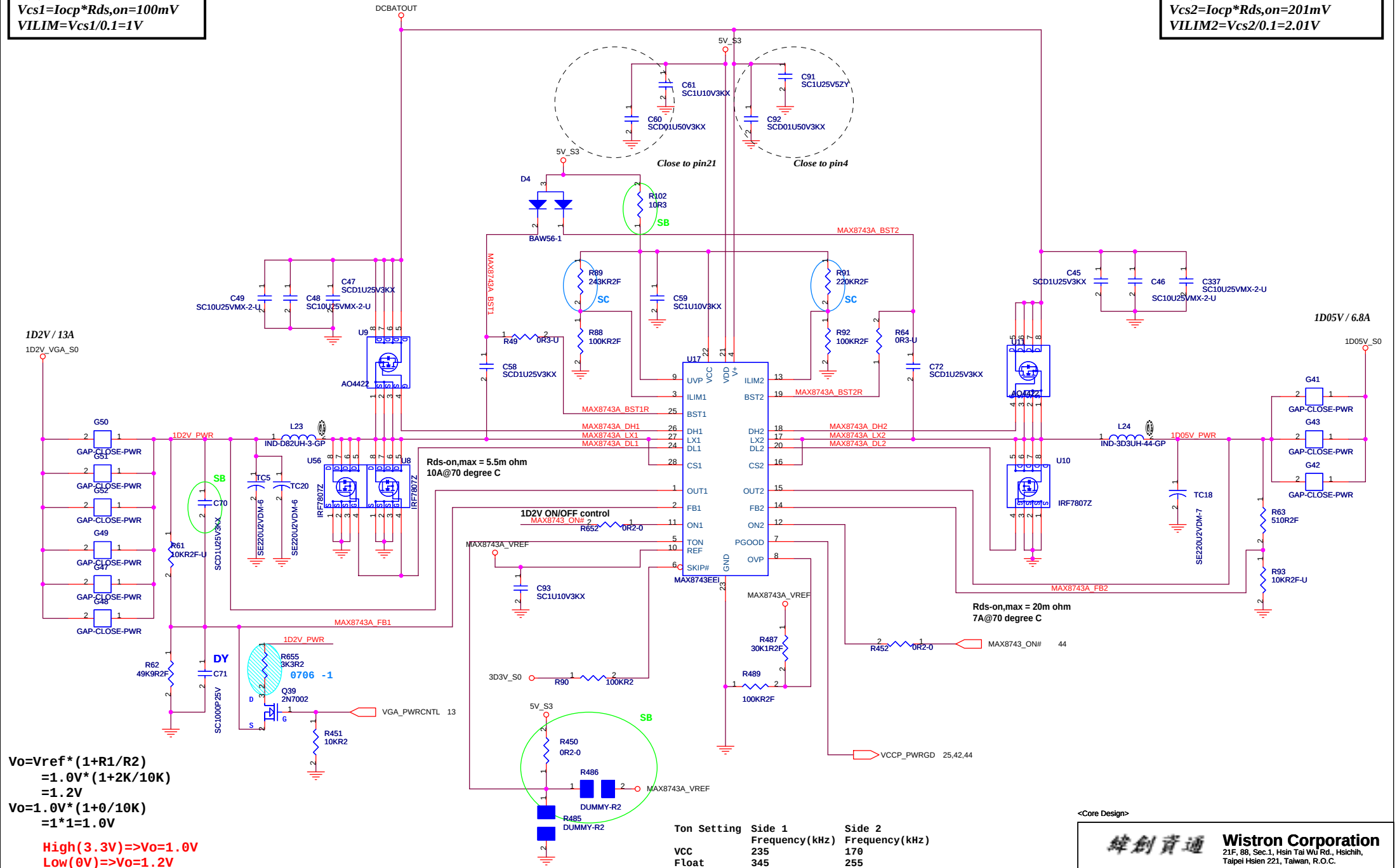
Title: *MAX8743 (1D8V_S0/1D5V_S0)*

Size	Document Number	Rev
A3	Leopard2	-1

Date: Monday, July 11, 2005 Sheet 44 of 47

*Iocp=7.8 * 1.7 = 13.3A*
*Rds,on=5.5*1.375=7.563m ohm*
*Vcs1=Iocp*Rds,on=100mV*
VILIM=Vcs1/0.1=1V

*Iocp=4.3 * 1.7 = 7.3A*
*Rds,on=20*1.375=27.5m ohm*
*Vcs2=Iocp*Rds,on=201mV*
VILIM2=Vcs2/0.1=2.01V



Vo=Vref*(1+R1/R2)
=1.0V*(1+2K/10K)
=1.2V
Vo=1.0V*(1+0/10K)
=1*1=1.0V

High(3.3V)=>Vo=1.0V
Low(0V)=>Vo=1.2V

M24/M26 POWER PLAY (VGA_PWRCNTL)
high (3.3V) = set lower core voltage (VDDC = 1.0V)
low (0V) = set higher core voltage (VDDC = 1.2V)

Ton Setting	Side 1 Frequency(kHz)	Side 2 Frequency(kHz)
VCC	235	170
Float	345	255
VREF	485	355
AGND	620	460

<Core Design>

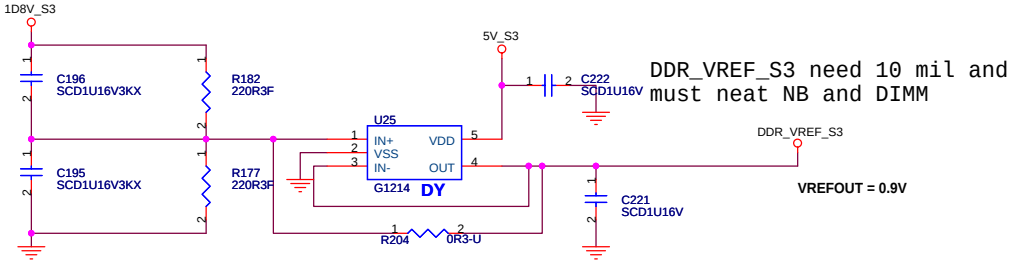
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *MAX8743 (1D2V_VGA_S0/1D05V)*

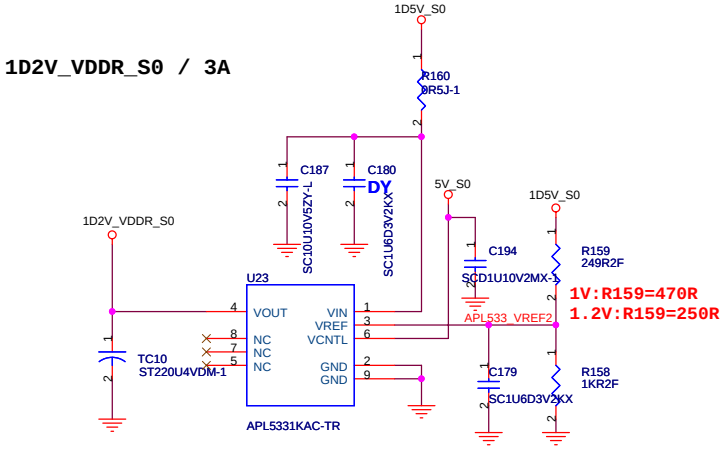
Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 45 of 47

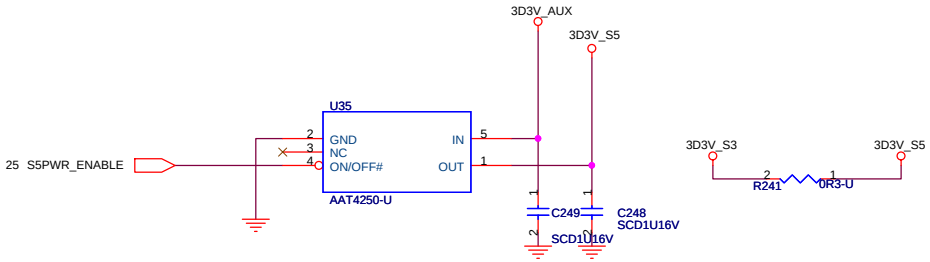
FOR GMCH Power



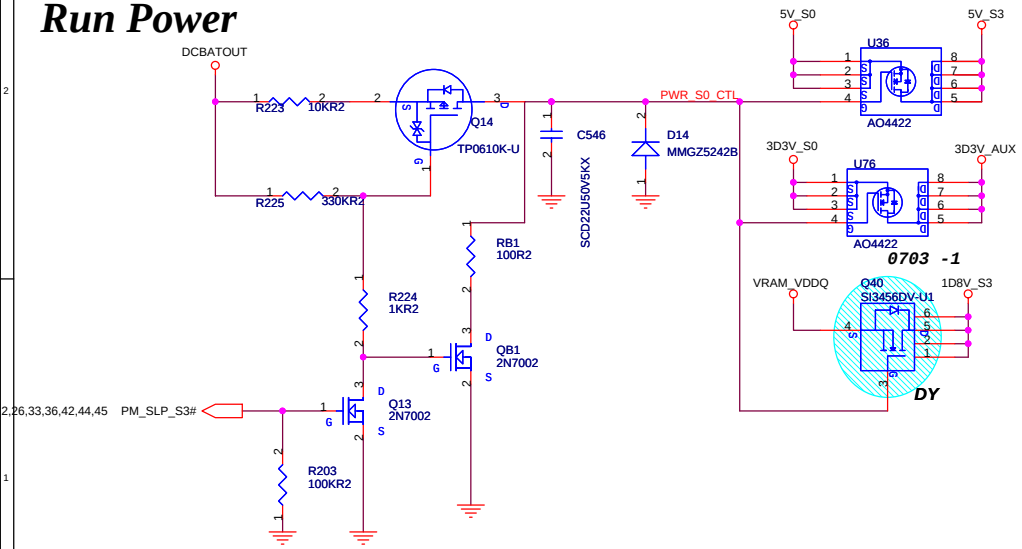
FOR DDR2 Power

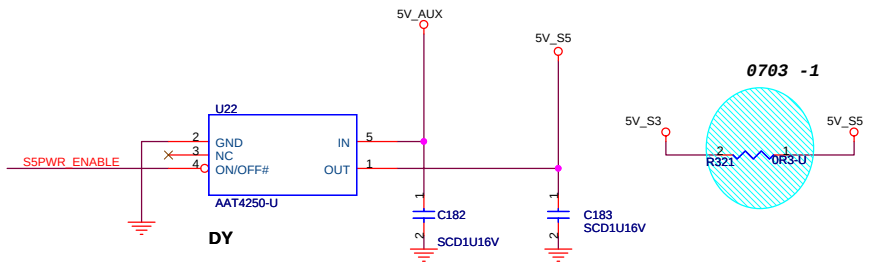


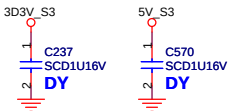
Suspend Power



Run Power







<Core Design>

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Title	PWRPLANE&RESETLOGIC	
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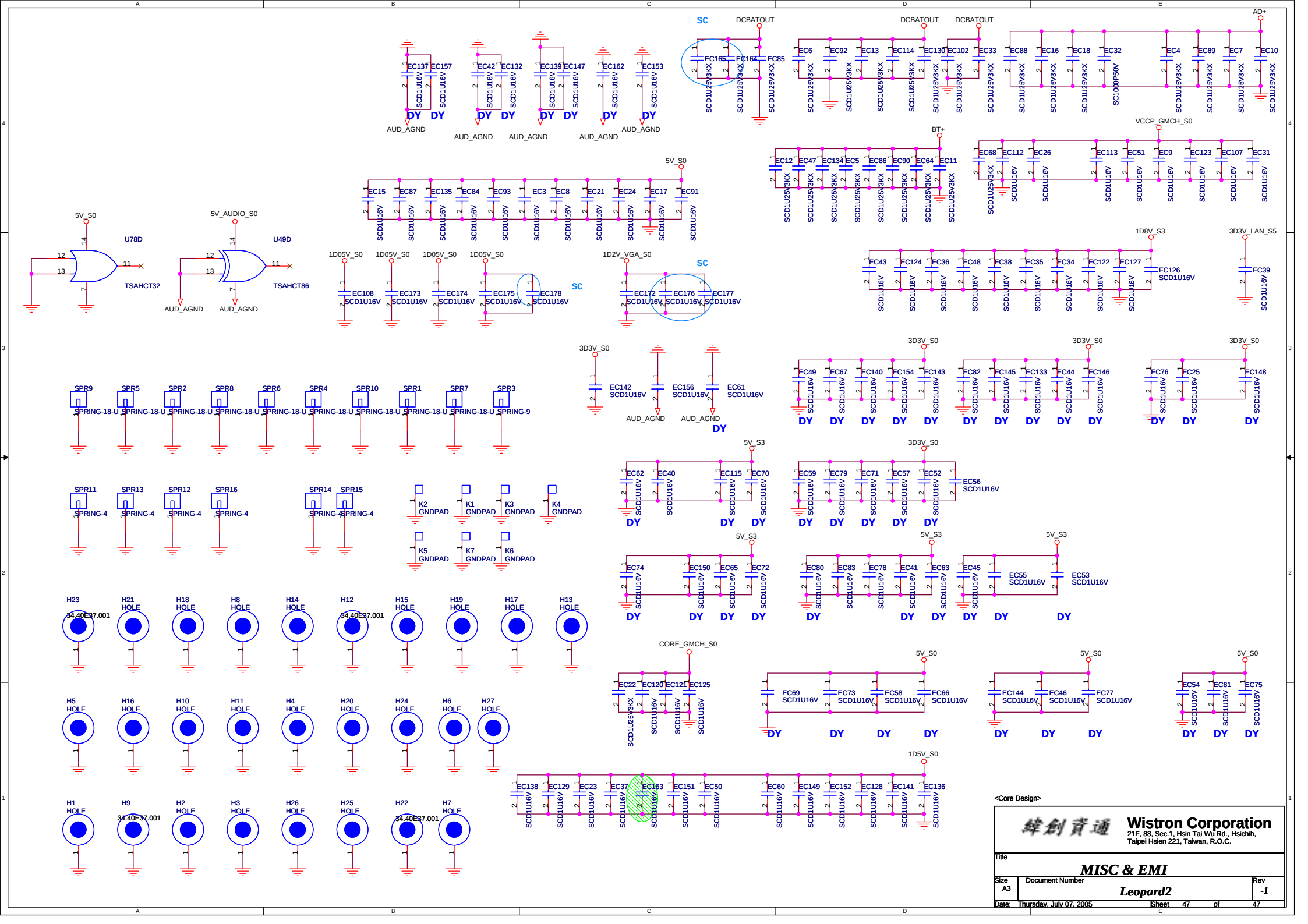

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