AT3U BLOCK DIAGRAM

01

04-- 0402 footprint
06-- 0603 footprint
08-- 0805 footprint
12-- 1206 footprint
F-- 1% tolerance

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

CPU Merom
478P (uPGA)/35W
PAG 3,4

CPU THERMAL SENSOR
PAG 11

14.318MHz

CLOCK GEN
ICS9LPRS355AGLFT
64pinsTSSOP
PAG 2

CLK_CPU_BCLK,CLK_CPU_BCLK#
CLK_MCH_BCLK,CLK_MCH_BCLK#
DREFCLK,DREFCLK#
DREFSSCLK,DREFSSCLK#

NORTH BRIDGE
Crestline
PAG 5,6,7,8,9,10,11

DDRII-SODIMM1
PAG 12,13
DDRII 533,667 MHz

DDRII-SODIMM2
PAG 12,13
DDRII 533,667 MHz

TV_OUT
CRT_OUT
LVDS(2 Channel)

CRT/S-VIDEO
PAG 18

Panel Connector
PAG 19

Cable Docking
PAG 31
- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

NBSRCCLK, NBSRCCLK#

DMI LINK

SOUTH BRIDGE
ICH-8M
PAG 14,15,16,17

USB2.0
5 0 3 4,6,7

Bluetooth PAG 27

USB2.0 I/O Ports X1 PAG 24

Camera X1 PAG 24

Mini PCI-E Card x1
Express Card x1
Cable Docking x1 PAG 31

PCI BUS / 33MHz

PCI-E

Azalia

SATA2
SATA - HDD1 PAG 24

SATA0
SATA - HDD2 PAG 27

PATA (66/100/133)
PATA- CD-ROM PAG 24

LPC

Mini PCI-E Card
PCI Express Mini Card (Wireless LAN)
PAG 30

LAN
Realtek PCIE-LAN RTL8101 (10/100)
PAG 25,26

Express Card 34
(NEW CARD)
PAG 27

RICOH
RICOH 832
PAG 20,21

Realtek
ALC 268
PAG 22

Two-element microphone PAG 28

Audio Jacks (Phone/ MIC) PAG 22

RJ45 PAG 25

IEEE1394 CONN PAG 21

Memory CardReader PAG 20

ENE KBC
KB3926QF A2
PAG 32

Keyboard Touch Pad PAG 28

CIR PAG 22

Capacitive Sense SW PAG 28

AUDIO Amplifier PAG 23

Jack to Speaker PAG 28

FAN PAG 31

SPI PAG 32

SYSTEM CHARGER(MAX8724) PAG 33

SYSTEM POWER MAX8778 PAG 34

VCCP +1.5V AND GMCH 1.05V(MAX8717) PAG 35

CPU CORE MAX8771 PAG 36

DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAG 37

DISCHARGE/3VS/5VS/LANVCC PAG 38

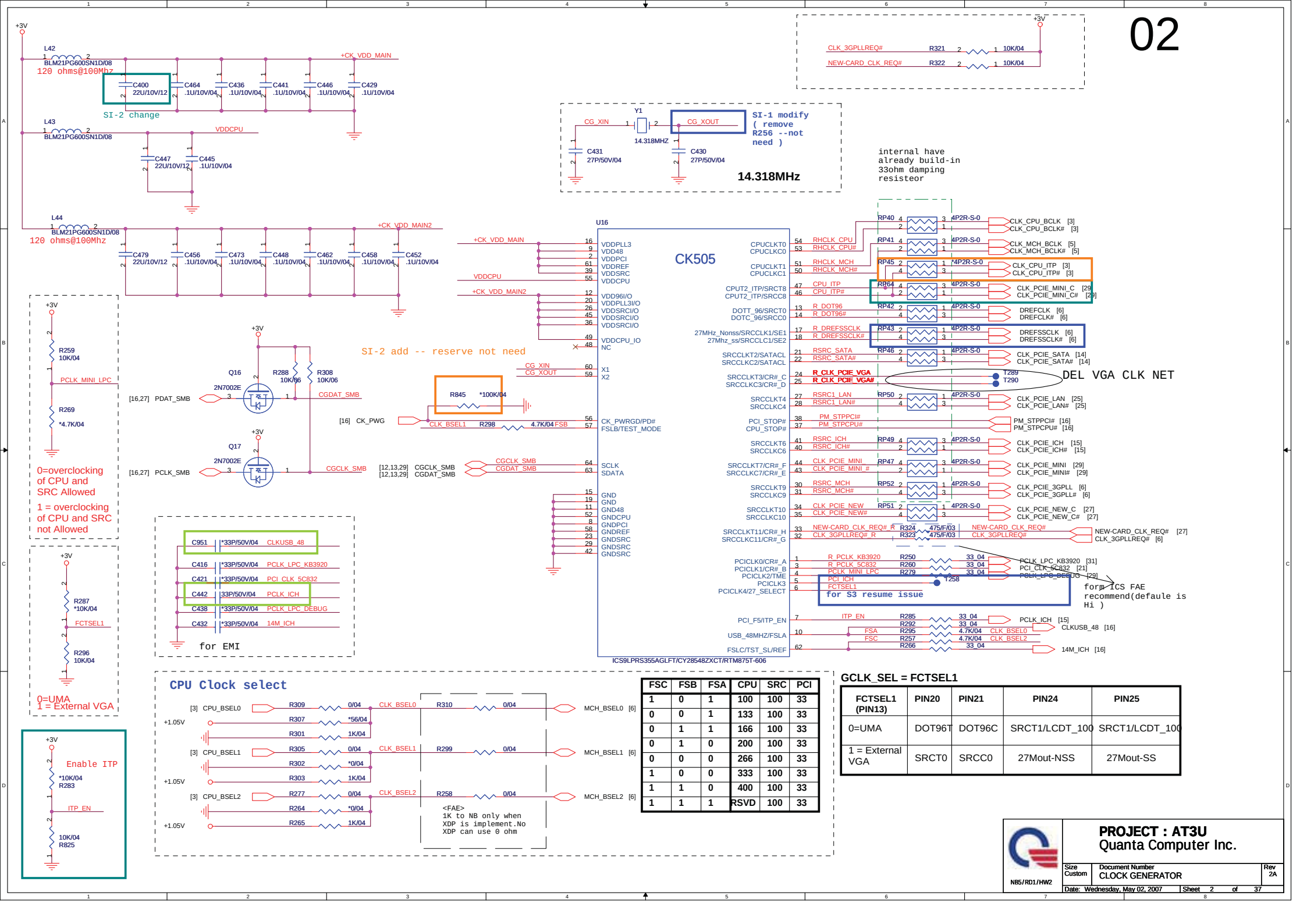
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	2A

NB5/RD1/HW2

Date: Monday, April 30, 2007 Sheet 1 of 37



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

GCLK_SEL = FCTSEL1

FCTSEL1 (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	2A

NB5/RD1/HW2

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for power noise

Layout Note: Place voltage divider within 0.5" of GTLREF pin

SI-2 modified for fix run TAT hang

modified --remove R72

modified resevved for power noise

Note: H_DPRSTP need to daisy chain from ICH8 to IMVP6 to CPU.

Reserved for EMI.

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.

Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.

Populate ITP700Flex for bringup

ITP debug signals

Layout Note: Place R8 close ITP.

Layout Note: Place R4,R361,R346 & R7 close to CPU.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

Note: Populate R5, R8, C372 & R430 when ITP connector is populated.

PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	2A
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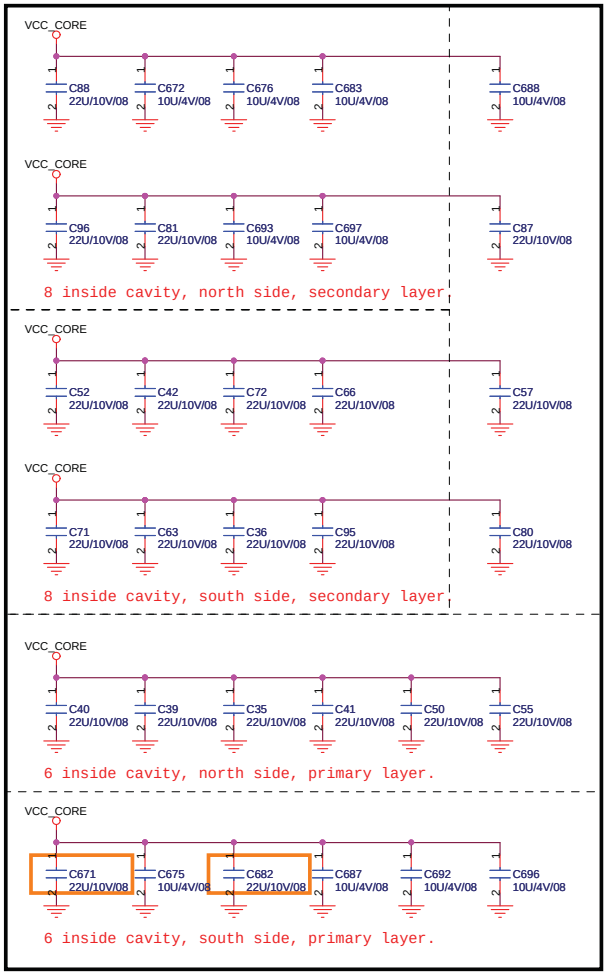
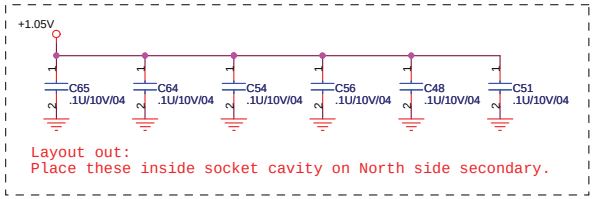
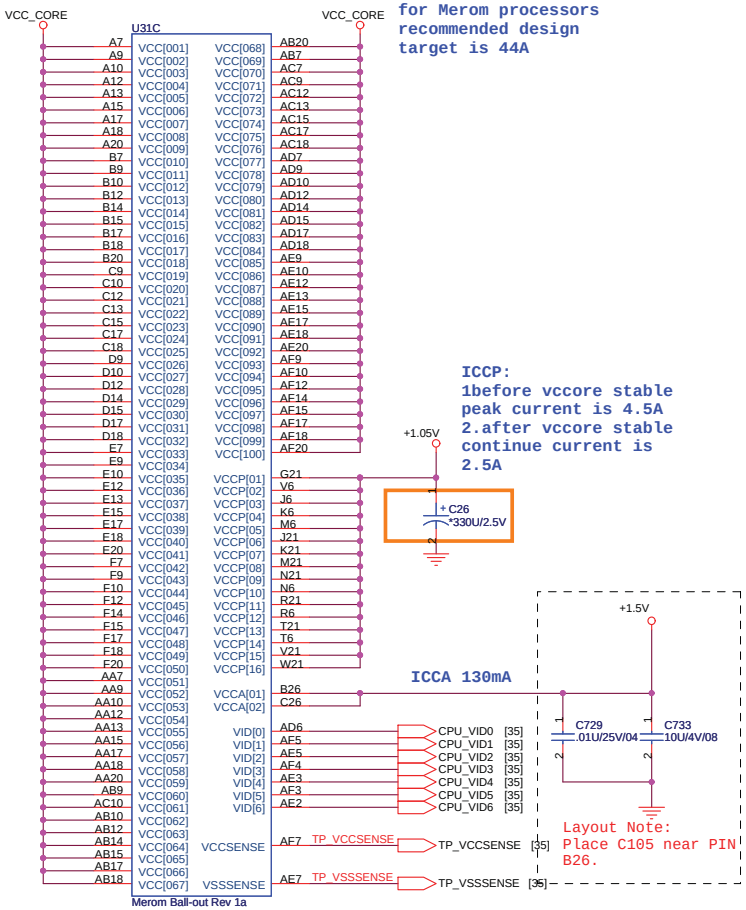
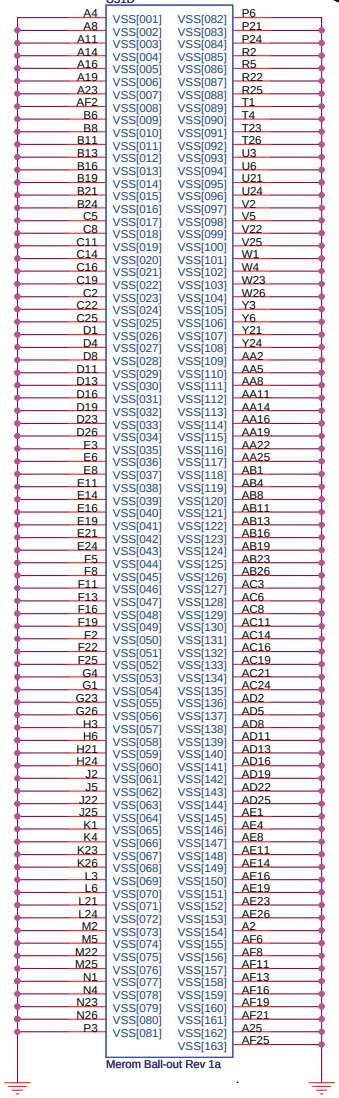
NB5/RD1/HW2









PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Merom Processor (POWER)	2A

NB5/RD1/HW2

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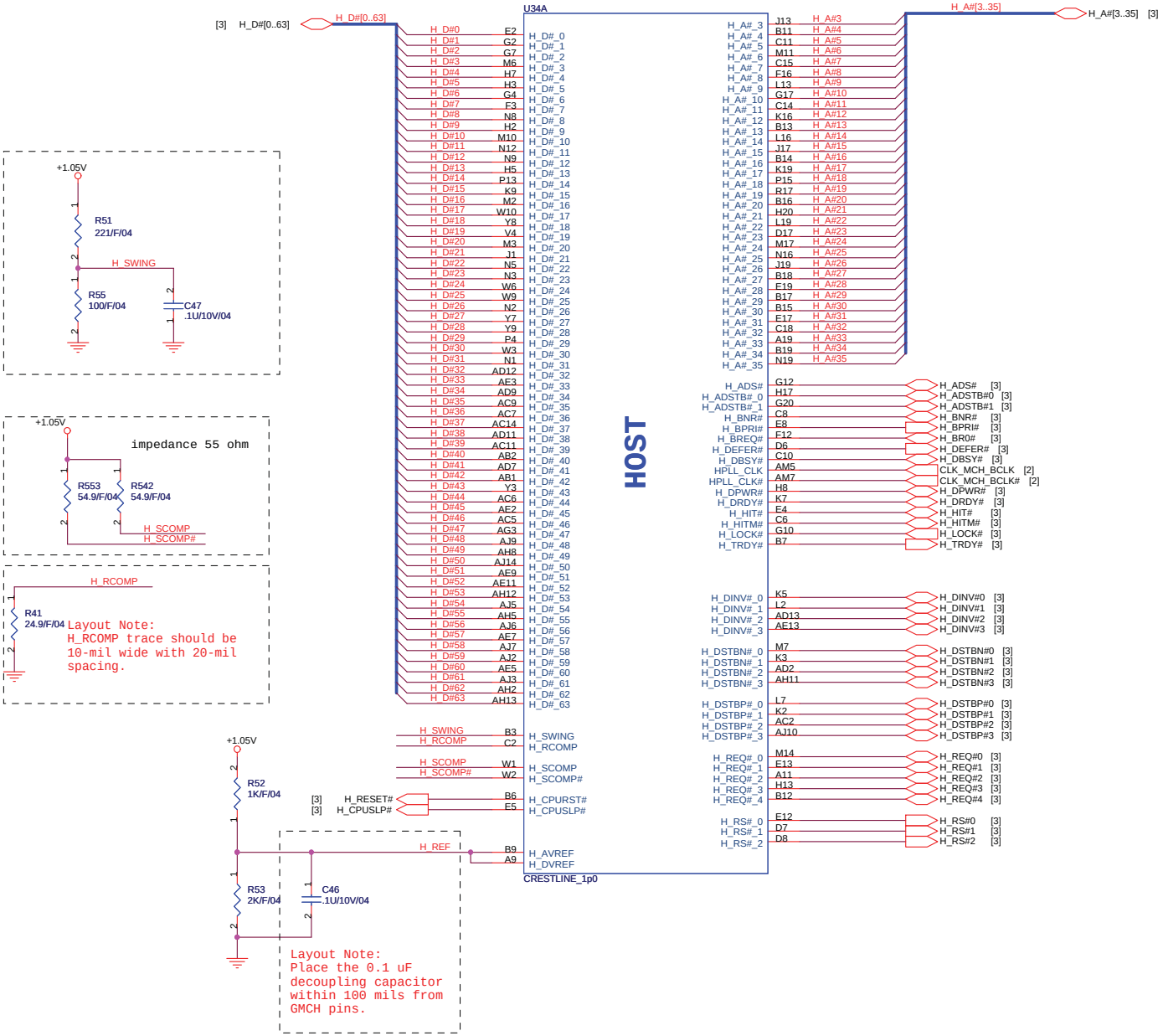
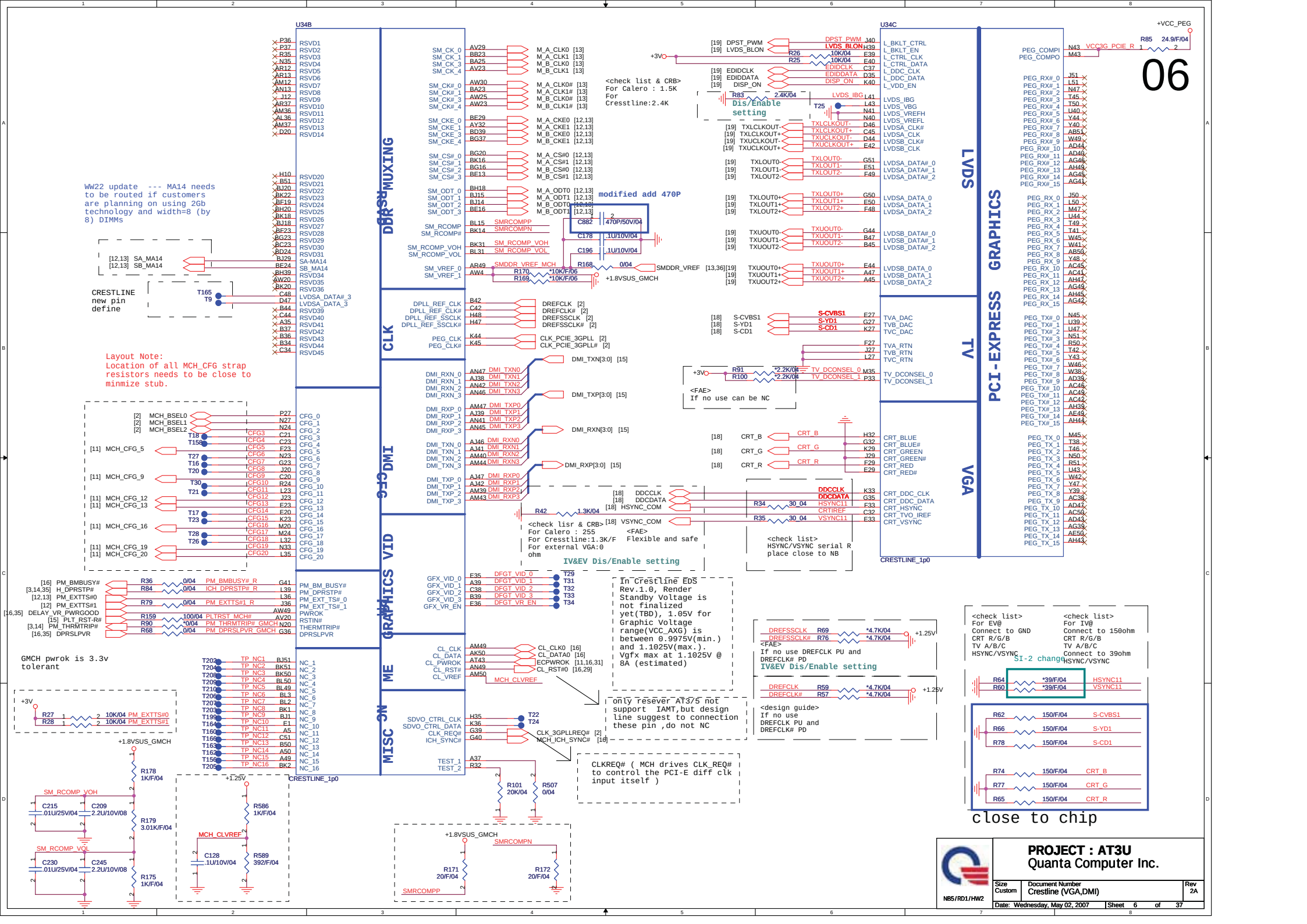


PROJECT : AT3U	
Quanta Computer Inc.	
Size: Custom	Document Number: Crestline (HOST)
Rev: 2A	
NB5/RD1/HW2	
Date: Wednesday, May 02, 2007	Sheet 5 of 37


U34B
DDR MUXING
CLK
DMI CFG
GRAPHICS VID
MISC
NC
U34C
LVDS
TV
PCI-EXPRESS GRAPHICS
VGA
CRESTLINE_1p0
CRESTLINE_1p0
WW22 update --- MA14 needs to be routed if customers are planning on using 2Gb technology and width=8 (by 8) DIMMs
CRESTLINE new pin define
Layout Note: Location of all MCH_CFG strap resistors needs to be close to minmize stub.
modified add 470P
Dis/Enable setting
IV&EV Dis/Enable setting
GMCH pwrok is 3.3v tolerant
In Crestline EDS Rev.1.0, Render Standby Voltage is not finalized yet(TBD), 1.05V for Graphic Voltage range(VCC_AXG) is between 0.9975V(min.) and 1.1025V(max.). Vgfx max at 1.1025V @ 8A (estimated)
only resever AT3/5 not support IAMT,but design line suggest to connection these pin ,do not NC
CLKREQ# (MCH drives CLK_REQ# to control the PCI-E diff clk input itself)
SI-2 change
close to chip
06
PROJECT : AT3U
Quanta Computer Inc.
N85/RD1/HW2
Crestline (VGA,DMI)
Wednesday, May 02, 2007
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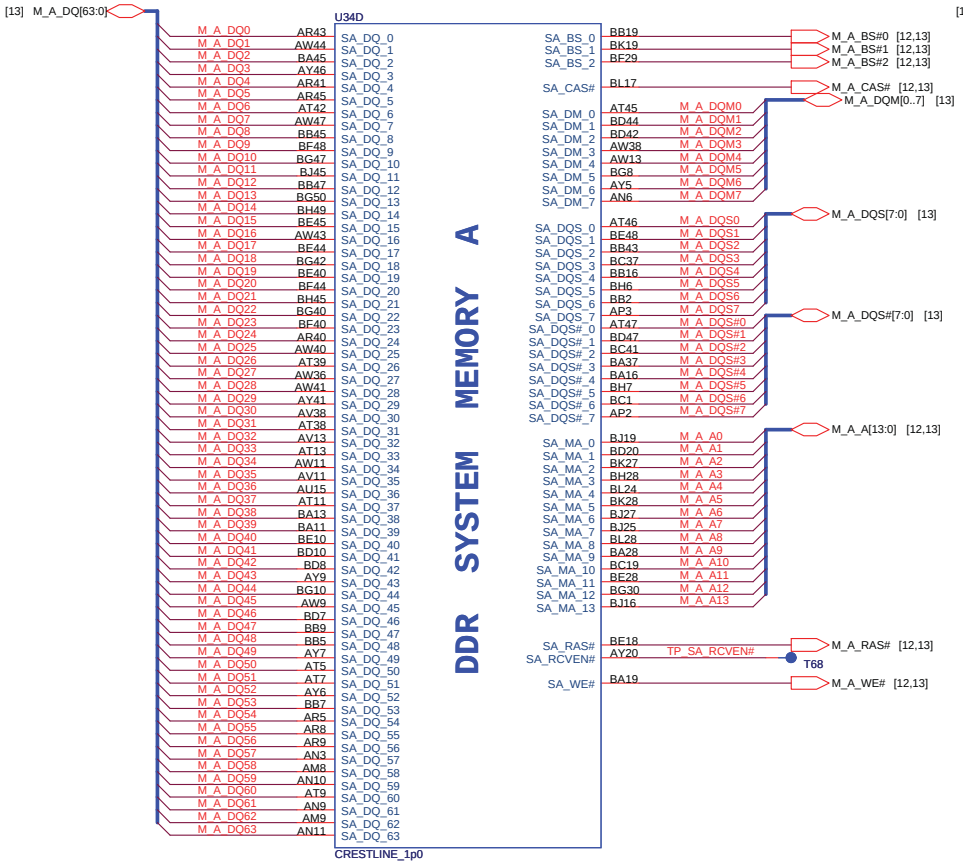

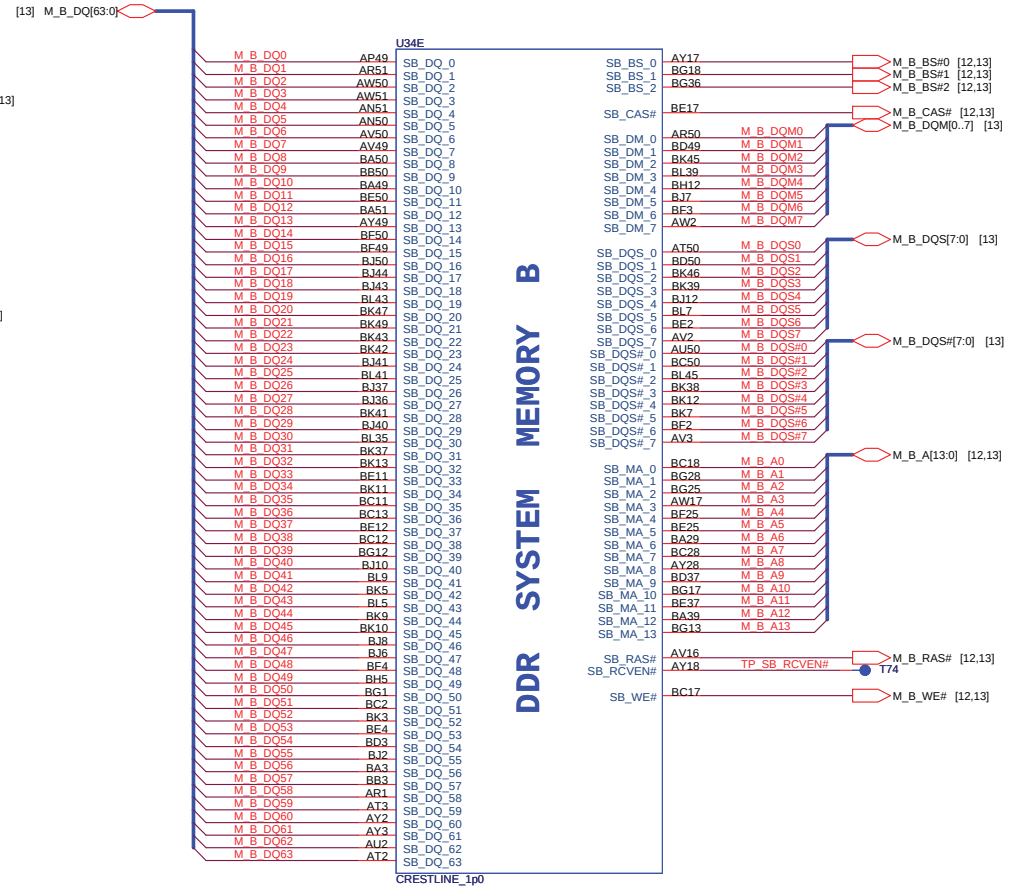

PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (DDR)	2A

NB5/RD1/HW2

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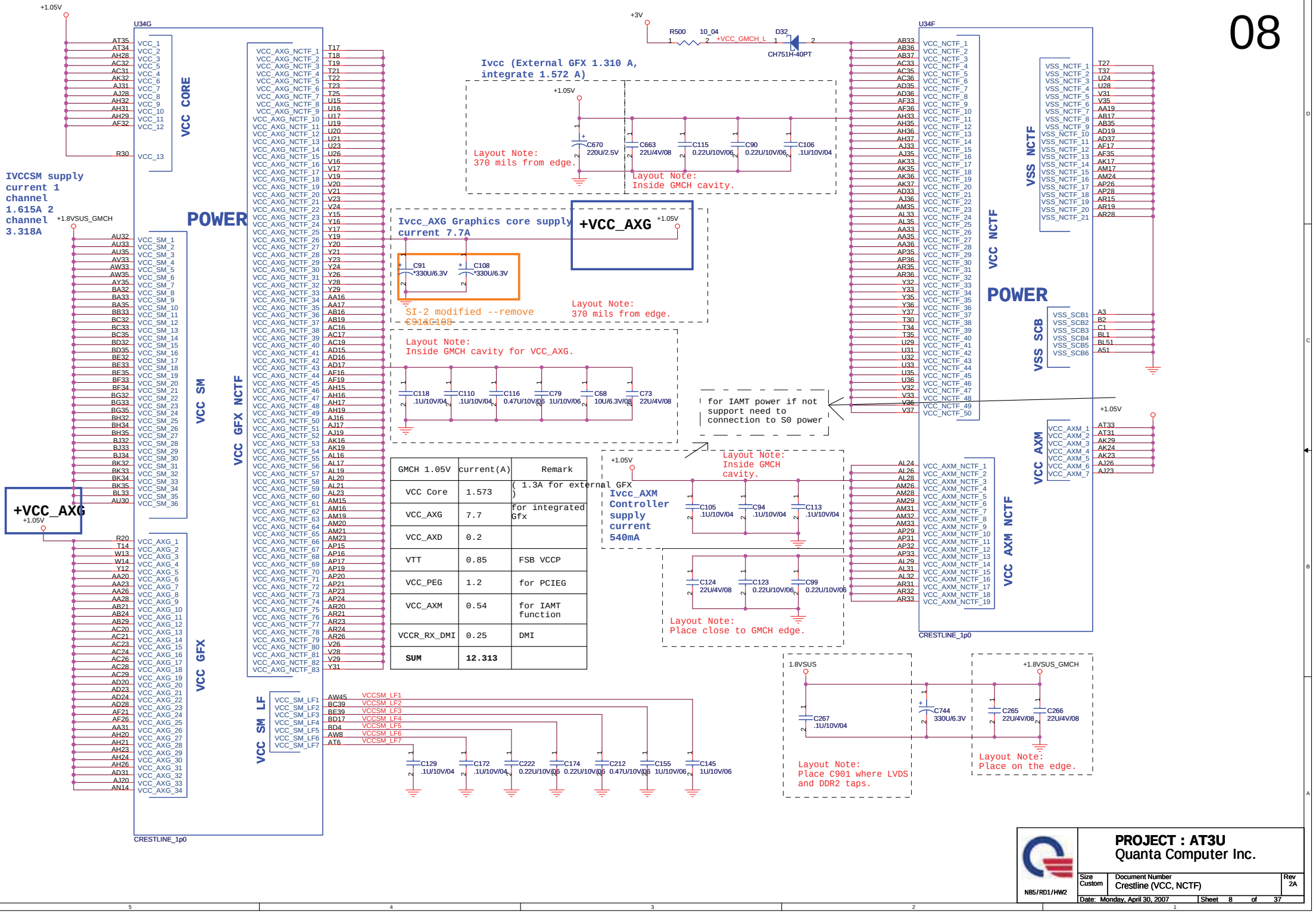


GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

NB5/RD1/HW2	**PROJECT : AT3U** Quanta Computer Inc.		
	Size: Custom	Document Number: Crestline (VCC, NCTF)	Rev: 2A
	Date: Monday, April 30, 2007	Sheet 8 of 37	

CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

9

IV&EV Dis/Enable setting

<FAE>
INT VGA disable
VCCSYNC connect
to GND

FB_180ohm+-25%
_100mHz_1500mA
_0.09ohm DC

FB_120ohm+-25%_100mHz
_200mA_0.2ohm DC

10uH+-20%_100mA

0.1Caps should be placed 200 mils with in its pins.

SI-1 modify
(NET name
wrong)

POWER

Ivcc_VTT FSB supply current 0.85A

Place on the edge.

Reserved L81 pad for inductor.

Place caps close to VCC_AXD.

Ivcc_DMI supply current 100mA

Place caps close to VCC_AXF

Ivcca_PEG_BG supply current 100mA

Ivcc_PEG supply current 1.2A

SI-1 modified change

Ivcc_RX_DMI supply current 250mA

1uH+-20%_300mA

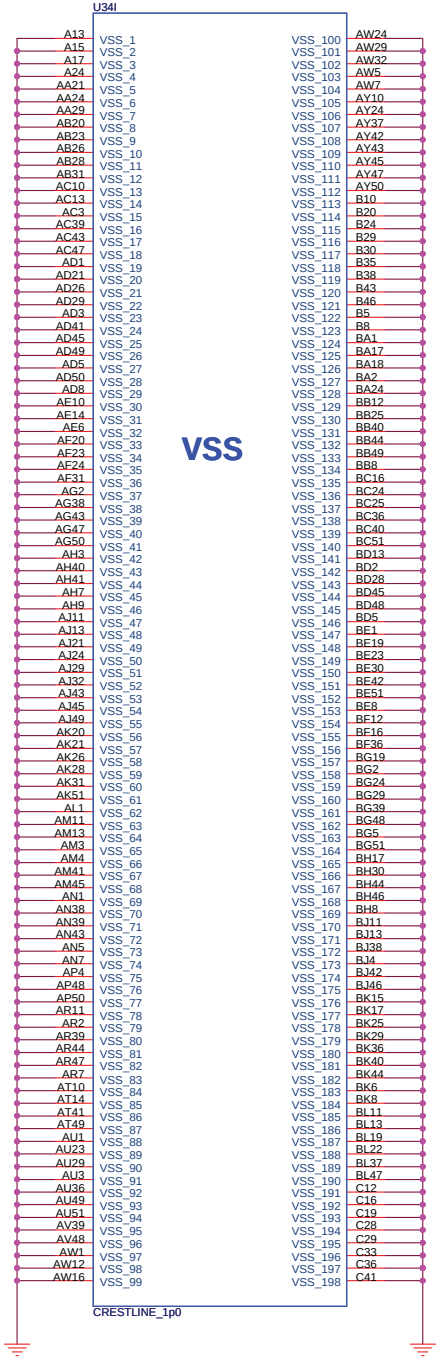
FB_220ohm+-25%_100MHz
_2A_0.1ohm DC

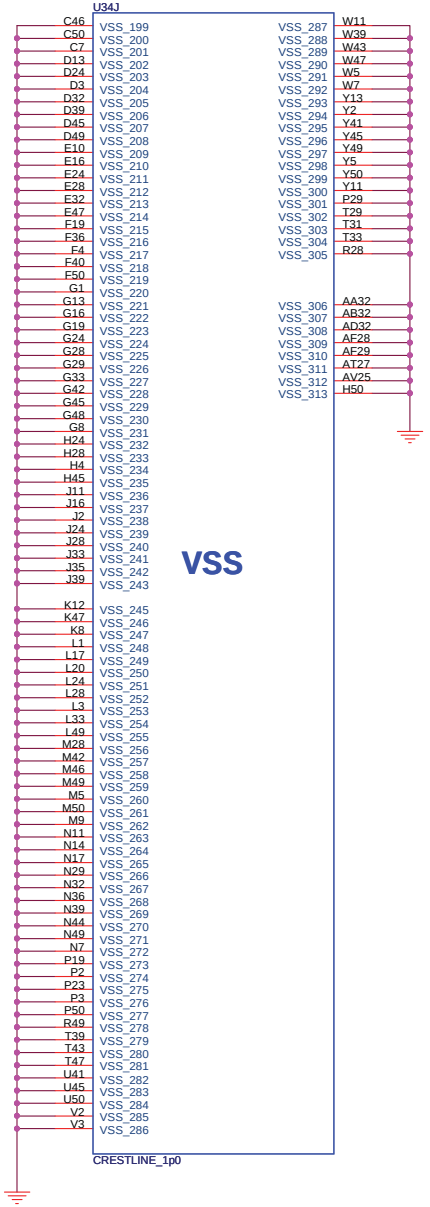
22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.

+3V_VCC_HV

40 mil wide

CRESTLINE_1p0





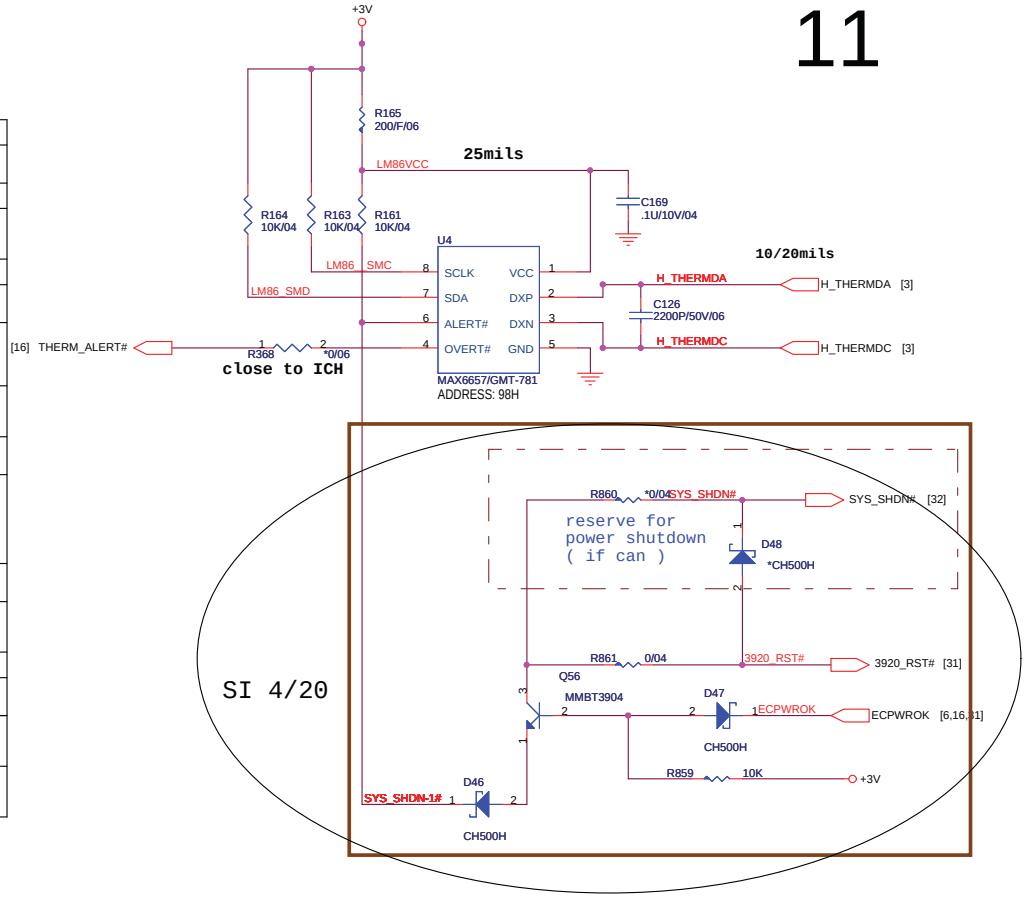
PROJECT : AT3U	
Quanta Computer Inc.	
Size: Custom	Document Number: Crestline (VSS)
Rev: 2A	
NB5/RD1/HW2	
Date: Monday, April 30, 2007	Sheet 10 of 37

Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

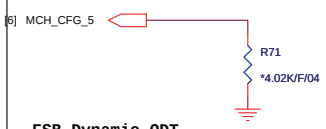
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port



DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)

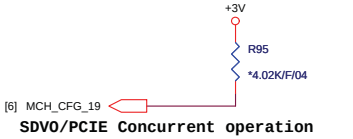


FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)

DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

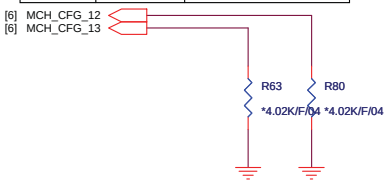


SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port

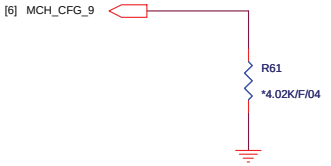
XOR /ALLz /Clock Un-gating

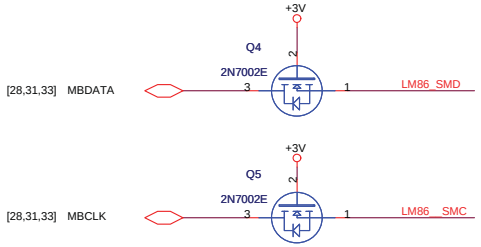
MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)





SDVO Present

Strap define at External DVI control page

PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- GMCH STRAP-3(6 of 6)	2A

NB5/RD1/HW2

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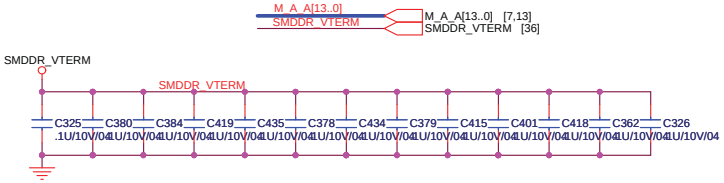
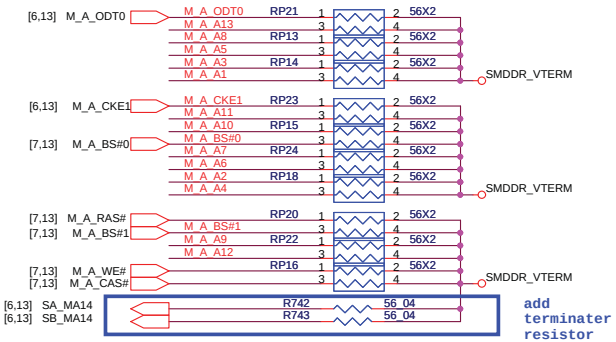
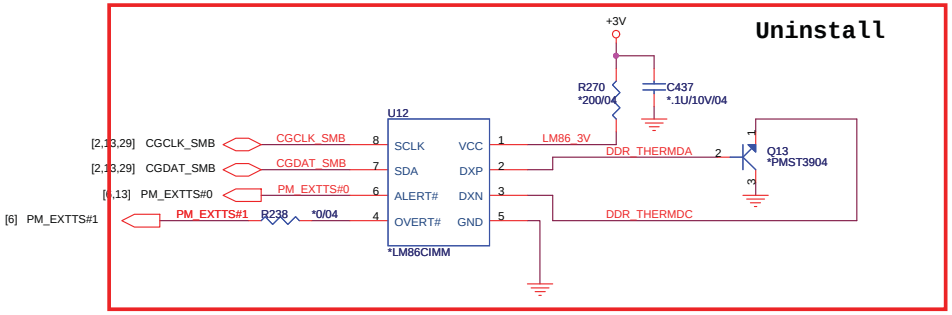
DDRII DUAL CHANNEL A,B.

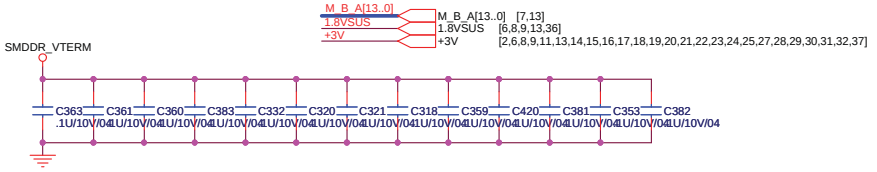
DDRII A CHANNEL



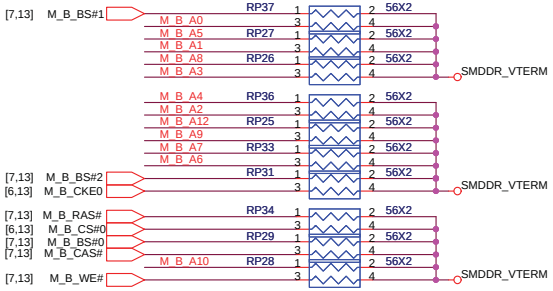


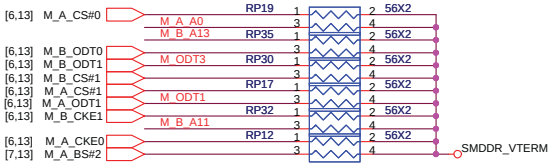


DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM





PROJECT : AT3U Quanta Computer Inc.		
NB5/RD1/HW2	Size: Custom Document Number: DDRII RES.ARRAY	Rev: 2A
	Date: Wednesday, May 02, 2007	Sheet 12 of 37

CGCLK_SMB
CGDAT_SMB
M_A_CKE[0..1]
M_A_CS#[0..1]
M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_CLK0
M_A_CLK0#
M_A_CLK1
M_A_CLK1#
M_A_BS#[0..2]
M_A_ODT[0..1]
M_A_DQM[0..7]
M_A_DQ[0..63]
M_A_DQS[0..7]
M_A_DQS#[0..7]
M_A_A[13..0]
M_B_CKE[0..1]
M_B_CS#[0..1]
M_B_RAS#
M_B_CAS#
M_B_WE#
M_B_CLK0
M_B_CLK0#
M_B_CLK1
M_B_CLK1#
M_B_BS#[0..2]
M_B_ODT[0..1]
M_B_DQM[0..7]
M_B_DQ[0..63]
M_B_DQS[0..7]
M_B_DQS#[0..7]
M_B_A[13..0]
+3V
1.8VSUS

CKEA 0,1

H 9.2

FOX=AS0A426-M2S-TR
CN26A

CKEB 0,1

H 5.2

FOX=AS0A426-MAS-TR
CN24A

PC2100 DDR2 SDRAM SO-DIMM (200P)

SMbus address A4

SMbus address A0

FOX=AS0A426-M2S-TR
CN26B

FOX=AS0A426-MAS-TR
CN24B

C771 470P/50V/04
R226 0/06
R227 *10K/F/06
R603 *10K/F/06

Place these Caps near So-Dimm1.

C773 2.2U/6.3V/06
C775 2.2U/6.3V/06
C785 2.2U/6.3V/06
C444 .1U/10V/04
C764 2.2U/6.3V/06
C770 .1U/10V/04
C788 .1U/10V/04
C439 .1U/10V/04
C433 .1U/10V/04
C769 .1U/10V/04
C767 .1U/10V/04
C772 .1U/10V/04
C768 2.2U/6.3V/06
C317 2.2U/6.3V/06
C316 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.

Place these Caps near So-Dimm2.

C774 2.2U/6.3V/06
C786 2.2U/6.3V/06
C784 2.2U/6.3V/06
C759 .1U/10V/04
C760 .1U/10V/04
C776 .1U/10V/04
C789 .1U/10V/04
C787 .1U/10V/04
C443 .1U/10V/04
C765 .1U/10V/04
C766 .1U/10V/04
C371 .1U/10V/04
C373 2.2U/6.3V/06
C372 2.2U/6.3V/06
C385 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm2

No Vias Between the Trace of PIN to CAP.

NB5/RD1/HW2

PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII SO-DIMM(200P)	2A

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RTC

Place near to Mini-door

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF

VCCRTC
3VPCU
D41 SDM10K45
D42 SDM10K45
C804 1U/16V/06
R638 20K/06
R635 1K/06
R637 1M/F/06
C811 1U/16V/06
G2 *SHORT_PAD1
C820 15P/50V/04
C817 15P/50V/04
Y6 32.768KHZ
R663 10M/06
CLK_32KX1
CLK_32KX2
RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
LAN100_SLP
CN30 CWY020-B0G1Z
change to battery conn

5VPCU
20MIL 20MIL
R625 *1.2K/06
R628 *1K/06
Q42 *MMBT3904
R626 *4.7K/06
R629 *15K/06
add RTC Bat rechargeable circuit

U42A

RTCX1 AG25
RTCX2 AF24
RTCRST# AF23
INTRUDER# AD22
INTVRMEN AE25
LAN100_SLP AD21

RTC

LAN_JCLK T234 B24 GLAN_CLK
LAN_RSTSYNC T102 D22 LAN_RSTSYNC
LAN_RXD0 T104 C21 LAN_RXD0
LAN_RXD1 T233 B21 LAN_RXD1
LAN_RXD2 T226 C22 LAN_RXD2
LAN_TXD0 T105 D21 LAN_TXD0
LAN_TXD1 T112 E20 LAN_TXD1
LAN_TXD2 T99 C20 LAN_TXD2
AH21 GLAN_DOCK#/GPIO13
R334 24.9/F/04 +1.5V_PCIE
GLAN_COMP_SB C25 GLAN_COMPI
GLAN_COMPO

LAN / GLAN

ACZ_BCLK AJ16 HDA_BIT_CLK
ACZ_SYNC AJ15 HDA_SYNC
ACZ_RST# AE14 HDA_RST#
[22] ACZ_SDIN0 ACZ_SDIN0 AJ17 HDA_SDIN0
ACZ_SDIN1 AH17 HDA_SDIN1
T255 ACZ_SDIN2 AH15 HDA_SDIN2
T132 ACZ_SDIN3 AD13 HDA_SDIN3
ACZ_SDOUT AE13 HDA_SDOUT
[25] LAN_DISABLE# AE10 HDA_DOCK_EN#/GPIO33
+3V R691 10K/06 T143 AG14 HDA_DOCK_RST#/GPIO34
[28] SATA_LED# SATA_LED# AF10 SATALED#

IHDA

[27] SATA_RXN2 C576 3900P/25V/04 SATA_RXN2_C AF6 SATA0RXN
[27] SATA_RXP2 C577 3900P/25V/04 SATA_RXP2_C AF5 SATA0RXP
[27] SATA_TXN2 C587 3900P/25V/04 SATA_TXN2_C AH5 SATA0TXN
[27] SATA_TXP2 C590 3900P/25V/04 SATA_TXP2_C AH6 SATA0TXP
CKL:1n ~ 20nF
T244 AG3 SATA1RXN
T243 AG4 SATA1RXP
T135 AJ4 SATA1TXN
T136 AJ3 SATA1TXP
[24] SATA_RXN0 C597 3900P/25V/04 SATA_RXN0_C AF2 SATA2RXN
[24] SATA_RXP0 C600 3900P/25V/04 SATA_RXP0_C AF1 SATA2RXP
[24] SATA_TXN0 C606 3900P/25V/04 SATA_TXN0_C AE4 SATA2TXN
[24] SATA_TXP0 C609 3900P/25V/04 SATA_TXP0_C AE3 SATA2TXP
CKL:1n ~ 20nF
[2] CLK_PCIE_SATA# AB7 SATA_CLKN
[2] CLK_PCIE_SATA AC6 SATA_CLKP
R655 24.9/F/06 SATA_BIAS AG1 SATARBIAS#
AG2 SATARBIAS

SATA

Place within 500 mils of ICH7
25mils/15mils

ICH8M REV 1.0

LPC

FWH0/LAD0 E5 LAD0 [29,31]
FWH1/LAD1 F5 LAD1 [29,31]
FWH2/LAD2 G8 LAD2 [29,31]
FWH3/LAD3 F6 LAD3 [29,31]
FWH4/LFRAME# C4 LFRAME# [29,31]
LDRQ0# G9 LDRQ#0 T116
LDRQ1#/GPIO23 E6 LDRQ#1 T230

LAN / GLAN

A20GATE AF13 GATEA20 GATEA20 [31]
A20M# AG26 H_A20M# [3]
DPRSTP# AF26 H_DPRSTP#_R R439 0/06 H_DPRSTP# [3,6,35]
DPSLP# AE26 H_DPSLP#_R R415 0/06 H_DPSLP# [3]
FERR# AD24 H_FERR# [3]
CPUPWRGD/GPIO49 AG29 R432 0/06 H_PWRGD [3]
IGNNE# AF27 H_IGNNE# [3]
INIT# AE24 H_INIT# [3]
INTR AC20 H_INTR [3]
RCIN# AH14 RCIN# RCIN# [31]
NMI AD23 H_NMI [3]
SMI# AG28 H_SMI#_R R425 0/06 H_SMI# [3]
STPCLK# AA24 H_STPCLK# [3]
THRMTRIP# AE27 H_THERMTRIP_R R406 24.9/F/06 PM_THRMTRIP# [3,6]
TP8 AA23 T127 PDD[15:0] [24]

CPU

IDE

DD0 V1 PDD0
DD1 U2 PDD1
DD2 V3 PDD2
DD3 T1 PDD3
DD4 V4 PDD4
DD5 T5 PDD5
DD6 AB2 PDD6
DD7 T6 PDD7
DD8 T3 PDD8
DD9 R2 PDD9
DD10 T4 PDD10
DD11 V6 PDD11
DD12 V5 PDD12
DD13 U1 PDD13
DD14 V2 PDD14
DD15 U6 PDD15
PDA[2:0] [24]
DA0 AA4 PDA0
DA1 AA1 PDA1
DA2 AB3 PDA2
DCS1# Y6 PDCS1# [24]
DCS3# Y5 PDCS3# [24]
DIOR# W4 PDIOR# [24]
DIOW# W3 PDIOW# [24]
DDACK# Y2 PDDACK# [24]
IDEIRQ Y3 IRQ14 IRQ14 [24]
IORDY Y1 PDIORDY PDIORDY [24]
DDREQ W5 PDDREQ [24]

+3V R447 10K/06 R648 10K/06
RCIN# GATEA20
+1.05V R409 *56/F/06 R449 *56/F/06
+1.05V R442 56/F/06
for fix ESD issue
+1.05V R849 56_04
Should be 2" close ICH7
C560 *SFI0603-050E101NP/06

ACZ_SDOUT R654 33_04 ACZ_SDOUT_AUDIO [22] C814 *10P/50V/04
ACZ_SYNC R649 33_04 ACZ_SYNC_AUDIO [22] C816 *10P/50V/04
ACZ_BCLK R653 33_04 BIT_CLK_AUDIO [22] C813 *10P/50V/04
ACZ_RST# R646 33_04 ACZ_RST#_AUDIO [22]

intel check list define to stuff 33ohm

SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

VCCRTC
R443 332K/F/06
ICH_INTVRMEN
R417 *0

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

VCCRTC
R444 332K/F/06
LAN100_SLP
R414 *0

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

+3V
R644 *1K/06
ACZ_SDOUT
ICH_TP3 [16]
R428 *1K

NB5/RD1/HW2	PROJECT : AT3U Quanta Computer Inc.	
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MINI CARD PCI-E

EXPRESS CARD (NEW CARD)

support RBSON card

PCIE-LAN

U42D

PCI-Express Direct Media Interface

SPI

USB

ICH8M REV 1.0

15/15mils

R379 24.9/F/06

Place within 500 mils of ICH7

USB Connector

USB Connector

FINGERPRINT

Carama USB

Docking

BLUETOOTH

WWAN

NEW CARD

USB Connector

USB Connector

swaped for fix dash issue

25mils/15mils

Place within 500 mils of ICH8

R632 22.6/F/06

RP61 8.2KX8

RP62 8.2KX8

RP63 8.2KX8

RP53 10P8R-10K

CHECK LIST suggest pull up 10k

A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

GNT3# R332 *1K

ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R337 *1K

GNT0# R331 *1K

U42B

PCI

Interrupt I/F

ICH8M REV 1.0

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

U41 TC7SH08FU

C792 0.1U/16V/06

Don't connect to PCI device / Express card

PCLK_ICH R328 *0 C484 *33P/50V

for EMI request

PROJECT : AT3U
Quanta Computer Inc.

NB5/RD1/HW2

Size: Custom | Document Number: ICH7-M M PCI E(2/4) | Rev: 2A

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fix re-boot fail

R833 2K/F/04

[35] VR_PWRGD_CK410#

U26 NL17SZ14DFT2G

C608 1U/16V/04

VR_PWRGD_CK410

R809 100K/04

these pin if unused require 8.2k to 10k pull-up to +3v

SI-1 add

U42C ICH8M REV 1.0

SMB: PCLK_SMB R816 0/04, PDAT_SMB R817 0/04, SMB_LINK_ALERT# R621 10K/06, SMLINK0 R619 10K/06, SMLINK1 R618 10K/06

SATA GPIO: SATA0GP/GPIO21 BOARD_ID1, SATA1GP/GPIO19 BOARD_ID0, SATA2GP/GPIO36 BOARD_ID3, SATA3GP/GPIO37 BOARD_ID4

Clocks: CLK14 14M_ICH, CLK48 CLKUSB_48, SUSCLK T108

SYS GPIO: RI# R624 8.2K/06, SYS_RST#-1 R615 10K/06, SMB_ALERT# R273 10K/06, KBSMI# R281 10K/06, SWI# R280 10K/06, CLKRUN# R433 8.2K/06, SERIRQ R656 8.2K/06, SCI# R662 10K/06, PM_RSMRST# R658 10K/06

14M_ICH R856 *33/04, CLKUSB_48 R857 33_04, C953 10P/04, C952 *10P/04

SYS_RST# R614 0/04, SYS_RST#-1

SLP_S3# R616 100/F/06, SLP_S4# R326 100/F/06, SUSB# [31], SUSC# [31]

100ohm to 499 ohm check list -- series 500ohm to IMVP6+

PWROK ICH_PWROK, DPRSLPVR-ICH R620 499/F DPRSLPVR, DPRSLPVR [6,35]

BATLOW# PM_BATLOW# R642 0/04, DNBSWON# [31]

PWRBTN# C819 *1U/16V/04, R665 *100/F/06

LAN_RST# PLTRST_LAN# R666 100/F/06, LAN_REST [25,31], PLTRST# [15,24,25,27,29,31]

RSMRST# PM_RSMRST# R659 100/F/06 RSMRST#, RSMRST# [31]

LAN_RST pin : 1.if used pci LAN please tie to PLTRST# 2.if used PHY LAN please tie to RSMRST#

CK_PWRGD R623 0/04, CK_PWG [2]

CLPWROK R622 0/04, ECPWROK [6,11,31]

SLP_M# SUSM# T251

CL_CLK0 F23, CL_CLK1 E18, CL_DATA0 F22, CL_DATA1 AF19, CL_VREF0 D24, CL_VREF1 AH23, CL_RST# AJ23

CL_CLK0 [6], ICH_CL_CLK1 [29], CL_DATA0 [6], ICH_CL_DATA1 [29], CL_VREF0_SB, CL_VREF1_SB, CL_RST#0 [6,29]

MEM_LED/GPIO24 AJ27, ME_EC_ALERT/GPIO10 AJ24, EC_ME_ALERT/GPIO14 AF22, WOL_EN/GPIO9 AG19

ME_SMC_ALERT# R284 0/04, BT_OFF# [27], T250, T141, T144

R819 10K/04 3VSUS

ADD (ww36 request)

Controller Link 1 VREF for IAMT support only: R631 3.24K/F/06, R633 453/F/04, C798 1U/10V/04

Controller Link 0 VREF for IAMT support only: R338 3.24K/F/06, R344 453/F/04, C511 1U/10V/04

GPIO: TACH1/GPIO1, TACH2/GPIO6, TACH3/GPIO7, GPIO8, GPIO12, TACH0/GPIO17, GPIO18, GPIO20, SCLOCK/GPIO22, QRT_STATE0/GPIO27, QRT_STATE1/GPIO28, SATACLKREQ#/GPIO35, SLOAD/GPIO38, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48

Power MGT: VRMPWRGD, TP7

MISC: SPKR, MCH_SYNC#, TP3

R768 10K/04, R769 10K/04, R770 10K/04

R427 0/04, R435 *10K, MCH_ICH_SYNC#_R, ICH_TP3

R450 *10K/F/06, R315 *10K/F/06

R402 0/06, R436 0/06, PM_STPPCI_ICH#, PM_STPCPU_ICH#

R364 8.2K/06

R405 0/04, R386 0/04, R611 0/04

R687 0/04, R671 0/04, R420 0/04

LCD_BK, BOARD_ID2

3/22

No Reboot strap

HDA_SPKR	Low = Default High = No Reboot

ACZ_SPKR R411 *10K

SI-2 Change

CRB STUFF 2K%1

R657 2K/F/04, C818 .047U/10V/04

[6,35] DELAY_VR_PWRGOOD, ECPWROK, R661 100K/06

U43 TC7SH08FU

ICH_PWROK, R667 10K/06

Board ID	15 " AT3U 965GM DUAL HDD (0:0:1:1:1) BOARD ID 7	
ID0	R692 Stuff	R693 not Stuff
ID1	R688 Stuff	R448 not Stuff
ID2	R690 Stuff	R689 not Stuff
ID3	R760 Stuff	R660 not Stuff
ID4	R761 Stuff	R652 not Stuff

R660 *10K/06, R652 *10K/06, R692 10K/06, R688 10K/06, R690 10K/06

R760 10K/06, R761 10K/06, R693 *10K/06, R448 *10K/06, R689 *10K/06

PROJECT : AT3U
Quanta Computer Inc.

NB5/RD1/HW2

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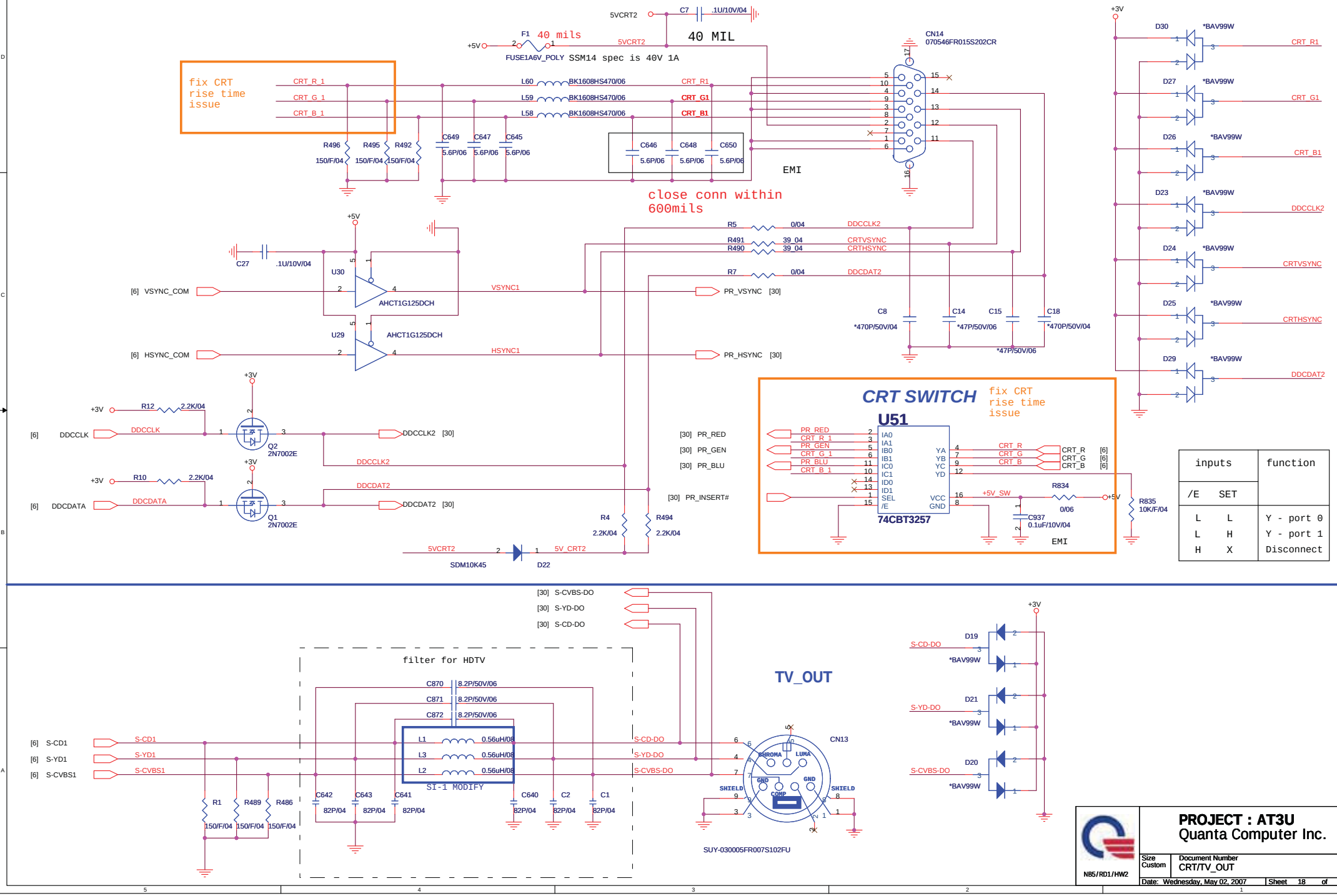
1.5V_A 1.5A
1.5V_B 675mA
VCC1.05 1.13A

V5REF 1mA
V5REF_SUS 1mA
VCCSATAPLL 47mA
VCCUSBPLL 10mA
VCCGLAN3.3 1mA
VCCGLLAN_PLL --23mA
VCCGLAN1.5 80mA
VCCGLAN3.3 18mA
VCCDMIPLL 23mA
VCC_DMI 50mA
VCPU_IO 1mA
VCC3.3 278mA
VCCHDA 32mA
VCC_SUSHDA 32mA
VCC_SUS3.3 177mA
VCCL3.3 18mA - 64mA (S3)

U42E — ICH8M REV 1.0
U42F — ICH8M REV 1.0

CRT PORT



PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/TV_OUT	2A

NB5/RD1/HW2

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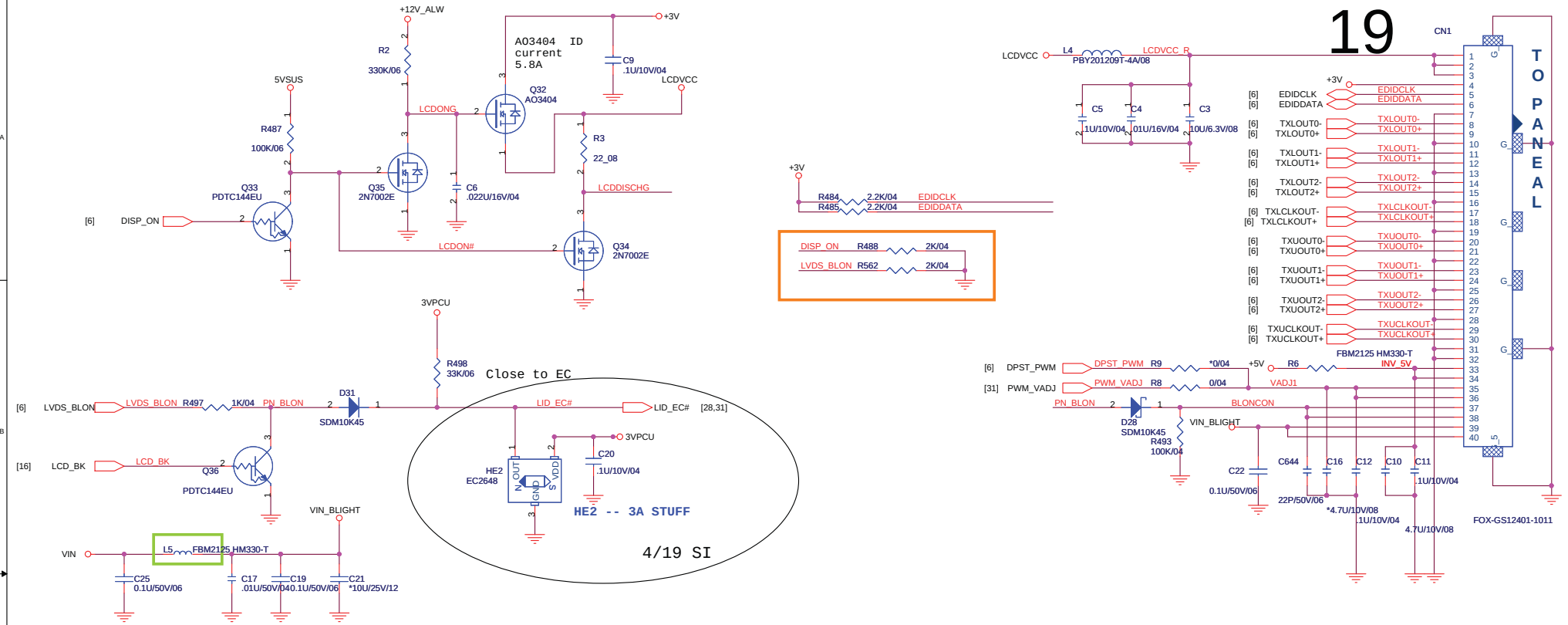
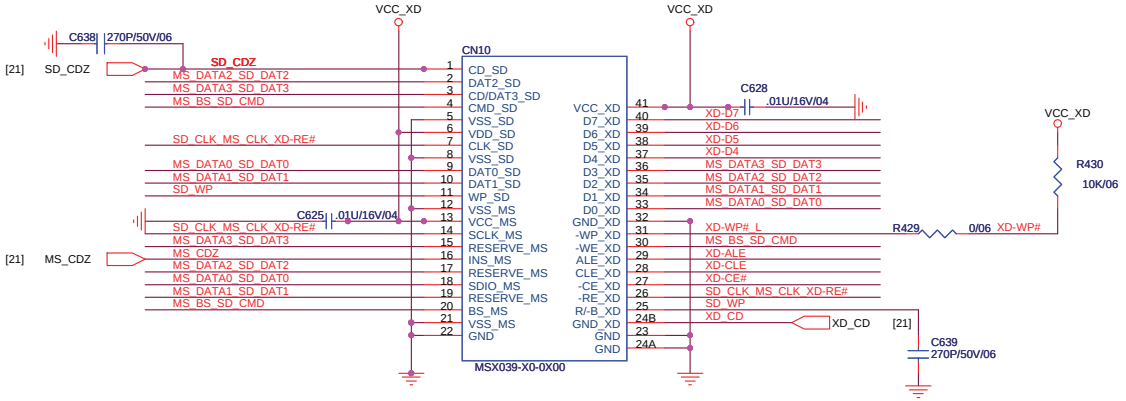

+12V_ALW
R2
330K/06
AO3404 ID current 5.8A
+3V
C9
.1U/10V/04
LCDVCC
5VSUS
Q32
AO3404
LCDONG
R487
100K/06
R3
22_08
LCDDISCHG
Q33
PDTC144EU
[6] DISP_ON
Q35
2N7002E
C6
.022U/16V/04
LCDON#
Q34
2N7002E
3VPCU
R498
33K/06
Close to EC
[6] LVDS_BLON
LVDS_BLON R497
1K/04
PN_BLON
D31
SDM10K45
LID_EC#
LID_EC# [28,31]
[16] LCD_BK
LCD_BK
Q36
PDTC144EU
HE2
EC2648
C20
.1U/10V/04
HE2 -- 3A STUFF
4/19 SI
VIN_BLIGHT
VIN
L5 FBM2125 HM330-T
C25
0.1U/50V/06
C17
.01U/50V/04
C19
0.1U/50V/06
C21
*10U/25V/12

+3V
R484 2.2K/04 EDIDCLK
R485 2.2K/04 EDIDDATA
DISP_ON R488 2K/04
LVDS_BLON R562 2K/04

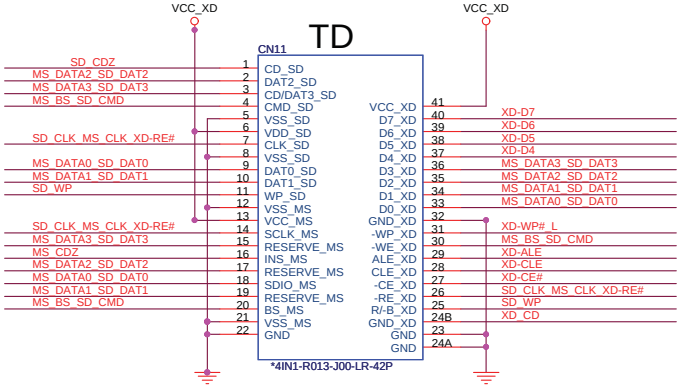
CN1
LCDVCC
L4 PBY201209T-4A/08
LCDVCC_R
C5 1U/10V/04
C4 .01U/16V/04
C3 10U/6.3V/08
+3V
[6] EDIDCLK
[6] EDIDDATA
TXLOUT0-
TXLOUT0+
TXLOUT1-
TXLOUT1+
TXLOUT2-
TXLOUT2+
TXLCLKOUT-
TXLCLKOUT+
TXUOUT0-
TXUOUT0+
TXUOUT1-
TXUOUT1+
TXUOUT2-
TXUOUT2+
TXUCLKOUT-
TXUCLKOUT+
FBM2125 HM330-T
TO PANEAL
[6] DPST_PWM
DPST_PWM R9 *0/04
+5V
R6
INV_5V
[31] PWM_VADJ
PWM_VADJ R8 0/04
VADJ1
PN_BLON
D28 SDM10K45
R493 100K/04
BLONCON
VIN_BLIGHT
C22 0.1U/50V/06
C644 22P/50V/06
C16 *4.7U/10V/08
C12 .1U/10V/04
C10 4.7U/10V/08
C11 1U/10V/04
FOX-GS12401-1011

5 IN1 CARD READER

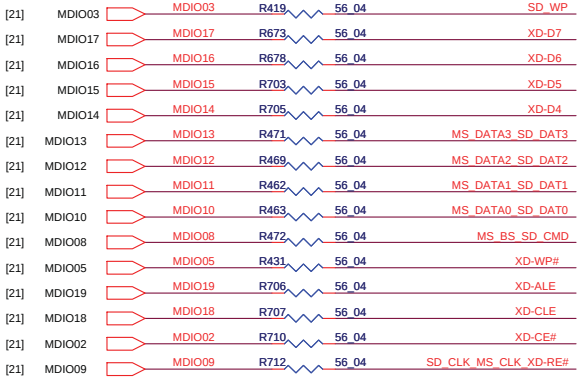
XD,MMC/SD,MS/MSP

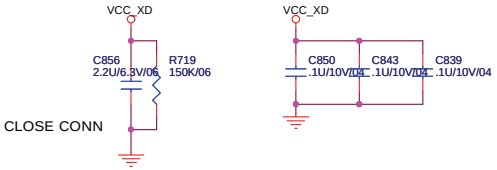


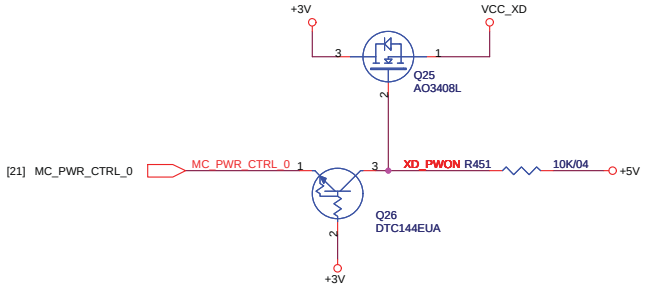
TD



bom create 2'nd source

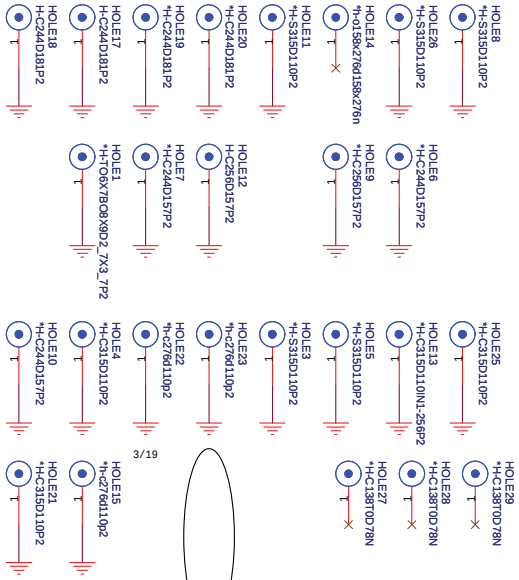






20

SCREW HOLE

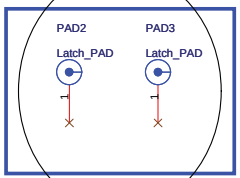


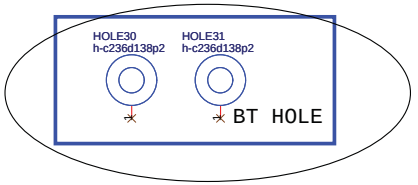
3/19

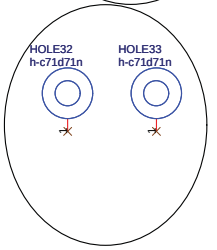
SI 4/20 del hole16

SI 4/30 del PAD1,9,10,13,16

BT PAD







NB5/RD1/HW2	**PROJECT : AT3U** Quanta Computer Inc.	
	Size: Custom — Document Number: CARD READER/HOLE	Rev: 1A
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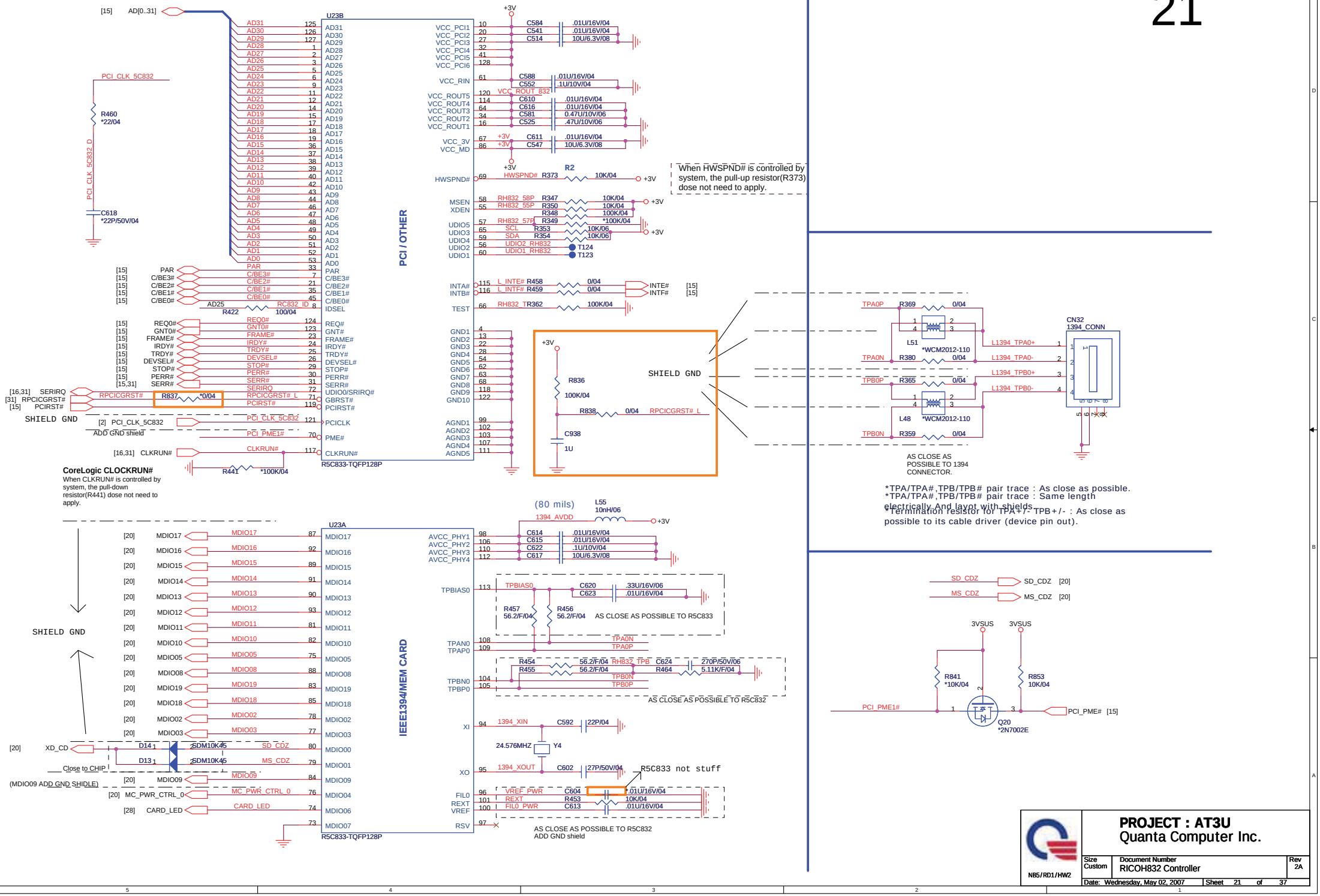
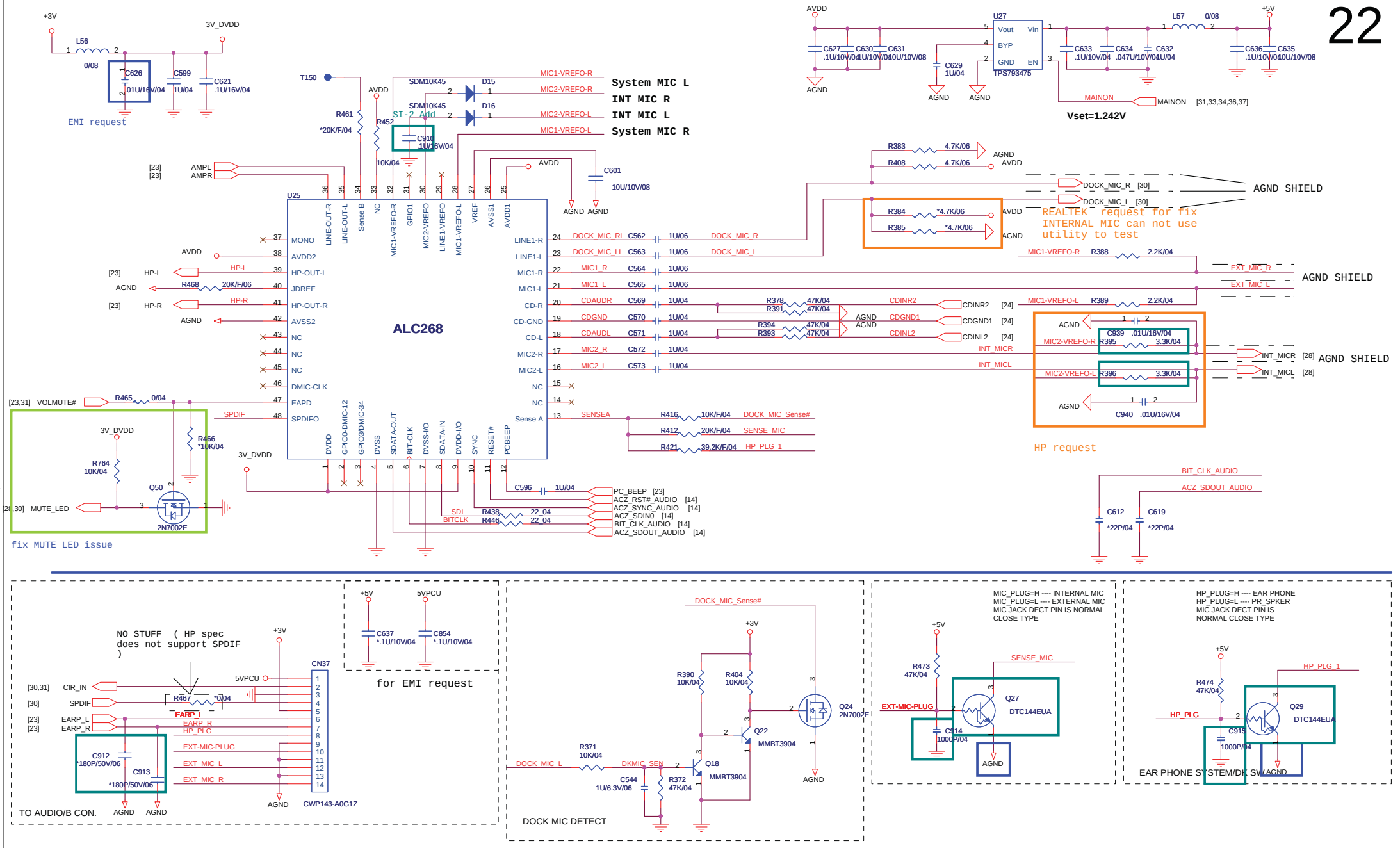

U23B
PCI / OTHER
R5C833-TQFP128P
U23A
IEEE1394/MEM CARD
R5C833-TQFP128P
SHIELD GND
When HWSPND# is controlled by system, the pull-up resistor(R373) dose not need to apply.
CoreLogic CLOCKRUN#
When CLKRUN# is controlled by system, the pull-down resistor(R441) dose not need to apply.
AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.
*TPA/TPA#,TPB/TPB# pair trace : As close as possible.
*TPA/TPA#,TPB/TPB# pair trace : Same length electrically And layot with shields.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).
AS CLOSE AS POSSIBLE TO R5C833
AS CLOSE AS POSSIBLE TO R5C832
ADD GND shield
R5C833 not stuff
Close to CHIP
(MDIO09 ADD GND SHIDLE)
PROJECT : AT3U
Quanta Computer Inc.
NB5/RD1/HW2
RICOH832 Controller
Rev 2A
Date: Wednesday, May 02, 2007
Sheet 21 of 37



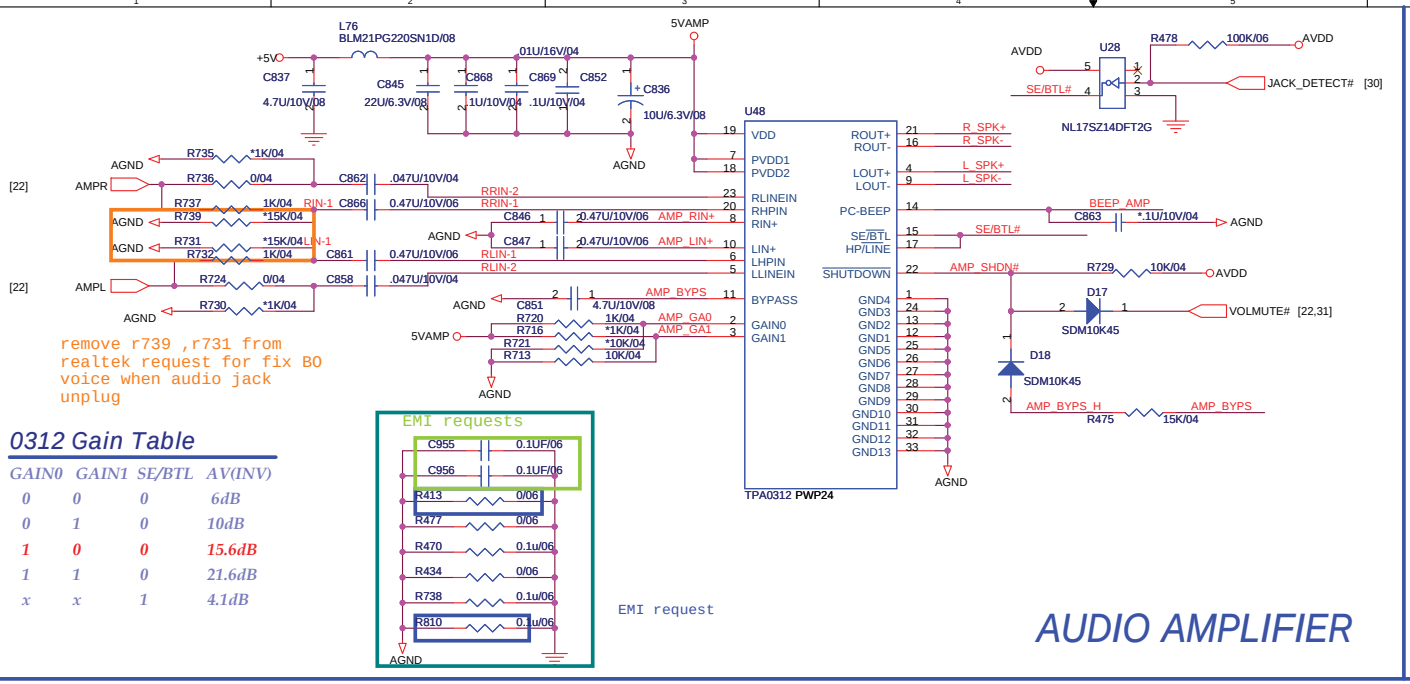
PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia CONEXANT20549-12	2A

NB5/RD1/HW2

Date: Wednesday, May 02, 2007 Sheet 22 of 37

AUDIO AMPLIFIER

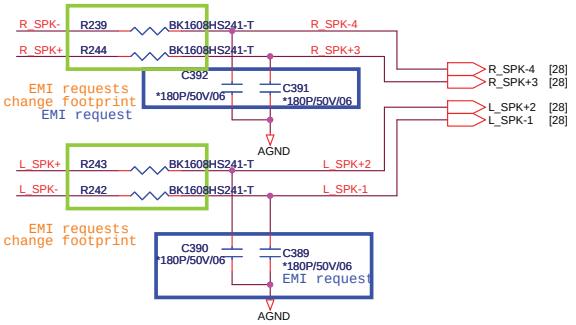


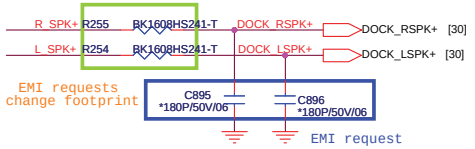
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	**0**	**0**	**15.6dB**
1	1	0	21.6dB
x	x	1	4.1dB

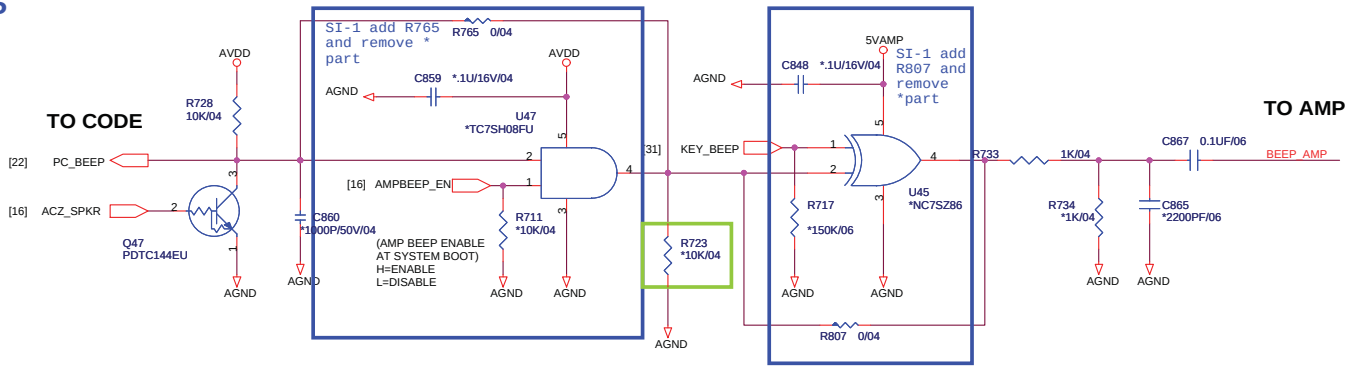
EMI request

INT. SPEAKER

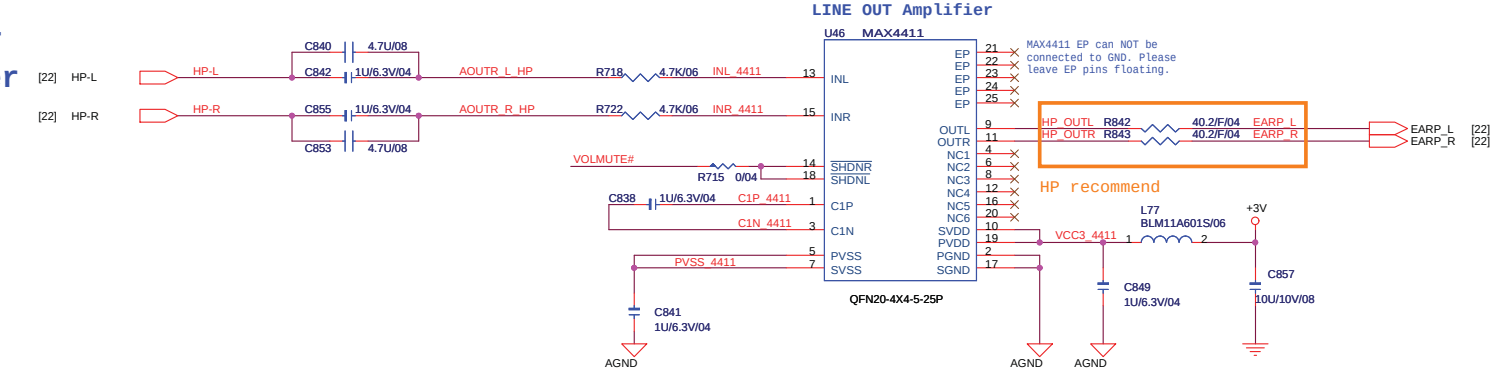




PCSPK BEEP

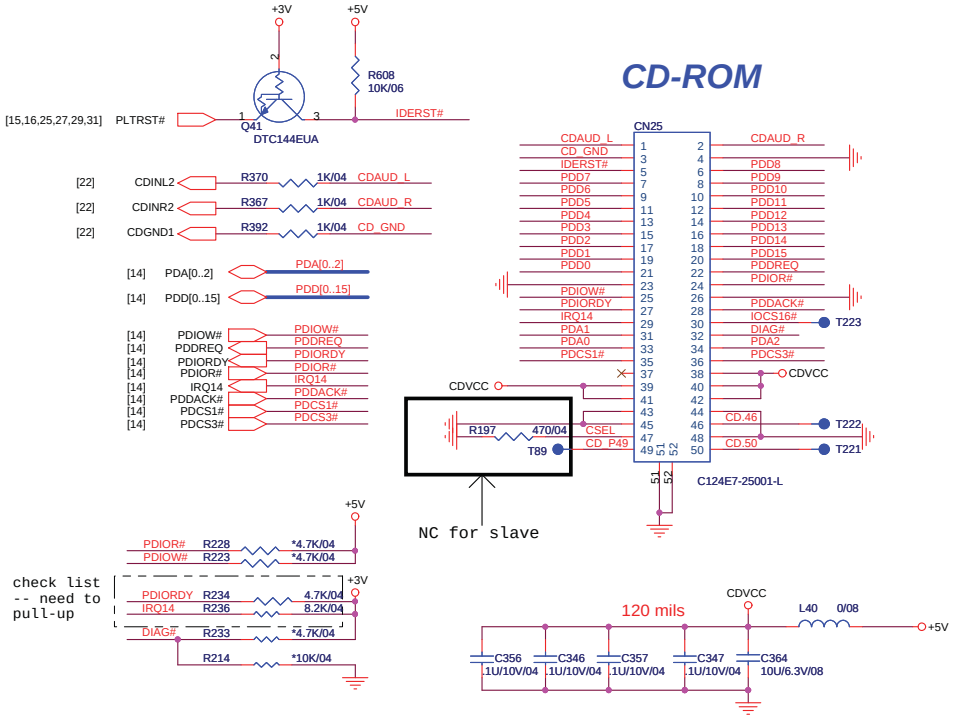


LINE OUT Amplifier

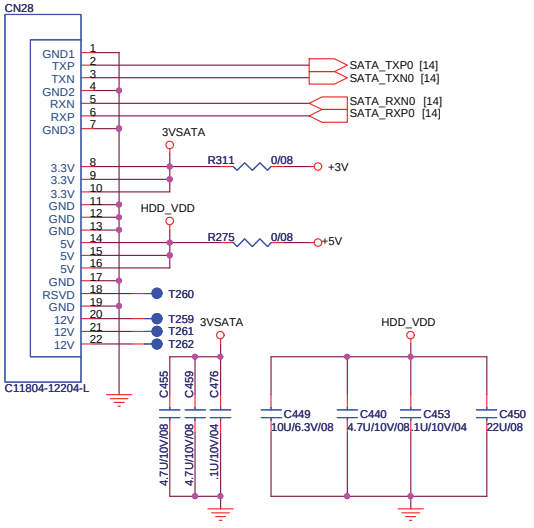


PROJECT : AT3U
Quanta Computer Inc.
Size: Custom
Document Number: JACK/AMP_TAP0312
Rev: 2A
N85/RD1/HW2
Date: Wednesday, May 02, 2007
Sheet 23 of 37

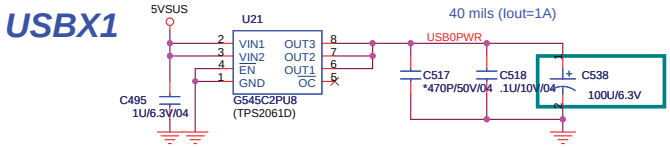
CD-ROM



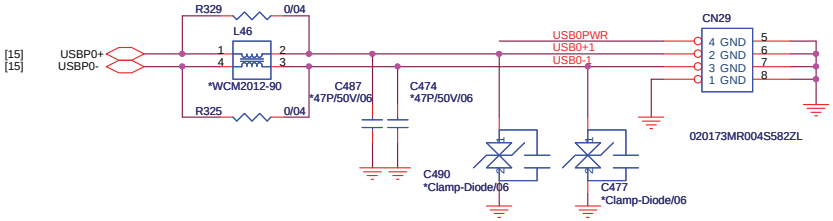
SATA_2 CONNECTOR



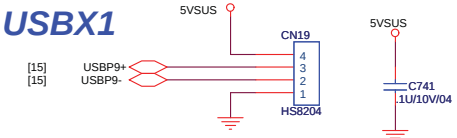
USBX1



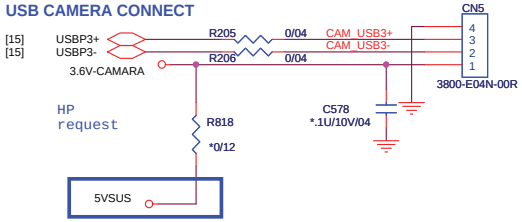
USB 0

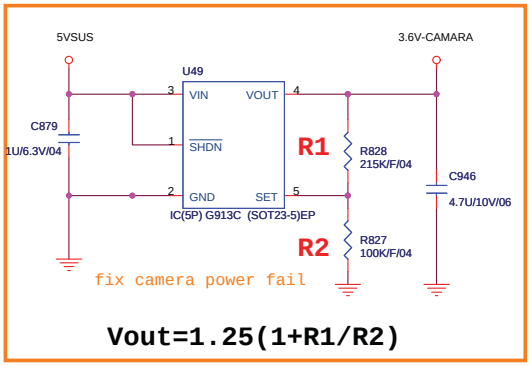


USBX1



USB CAMERA CONNECT





NB5/RD1/HW2	PROJECT : AT3U Quanta Computer Inc.	
Size: Custom	Document Number: SATA HDD/CD-ROM/USBX2	Rev: 2A
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E : Stuffed for 8101E(10/100)

fix 10/100 LAN LED issue

R345 0/04

R21 value should be 2.49K (1%) for 8111B/8111C application. R21 should be 2.0K(1%) for 8101E application

SI 4/20

U19 RTL8111B/8111C/8101E

for 93C56 used. NC if 93C46 is used.

U22 93C46-3GR

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

BLOCK A is only for RTL8101E application.

Block A

RJ45

Remove R70 for 8111B and 8111C

U14 NS892405

SI 4/20

NS892405:10/100

close U6

PROJECT : AT3U	
Quanta Computer Inc.	
Size: Custom	Document Number: RTL8101E
Rev: 2A	
NB5/RD1/HW2	Date: Wednesday, May 02, 2007
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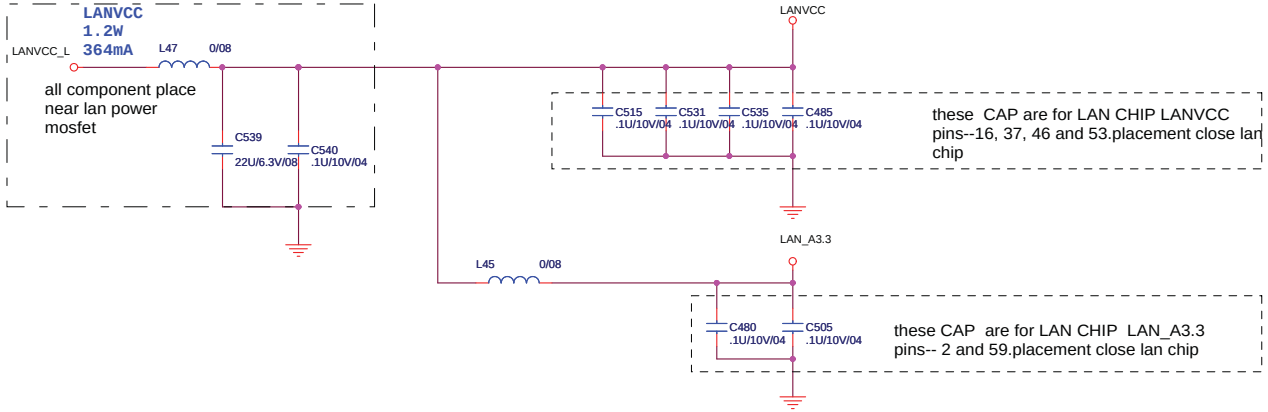
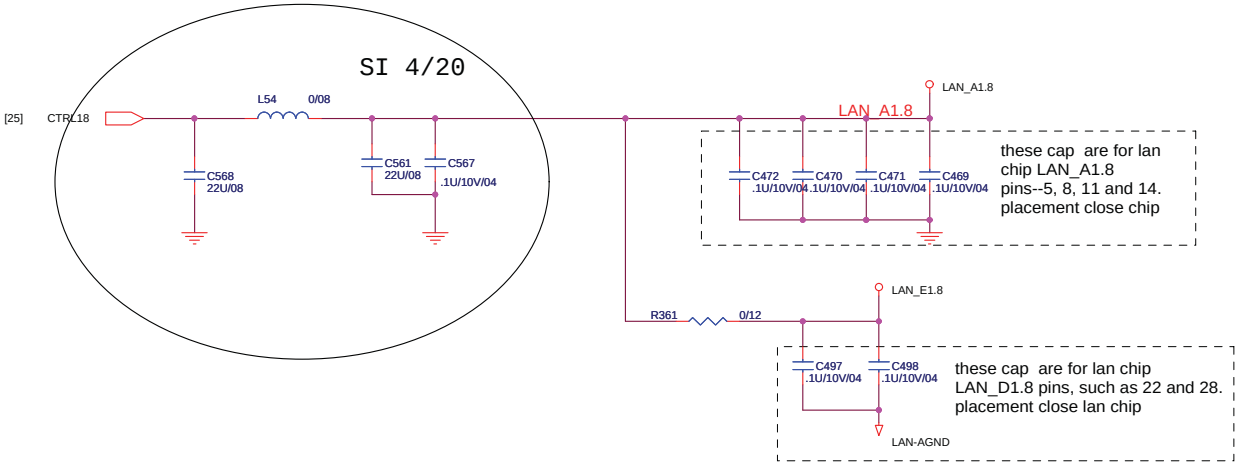
E : Stuffed for 8101E(10/100)

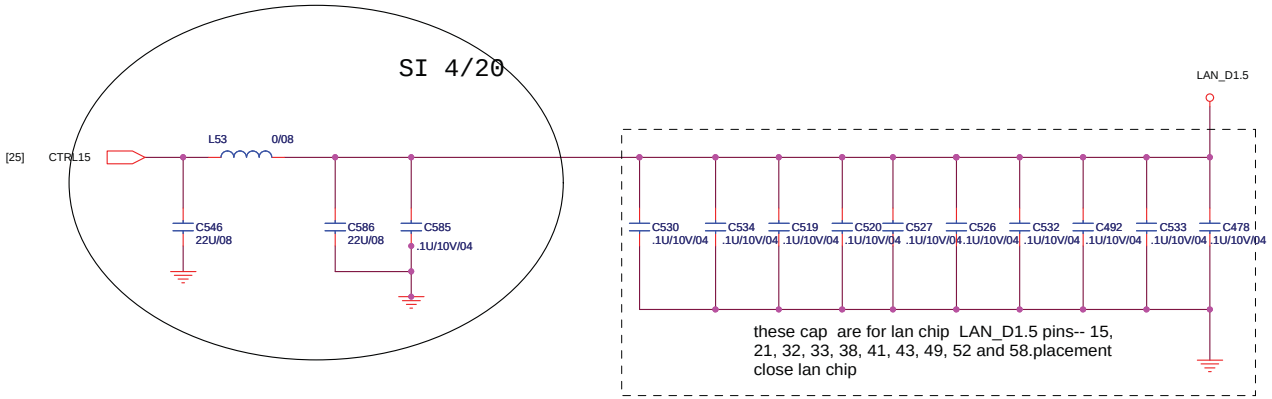




Power domain chart

	RTL8111B / RTL8101E	
LANVCC	*3.3V*	
LAN_D1.8	*1.8V*	
LAN_A1.8	*1.8V*	
LAN_D1.5	*1.5V*	

	Q19	Q21
RTL8111B	*Need*	*Need*
RTL8101E	*N/A*	*N/A*



NB5/RD1/HW2

PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN POWER	2A

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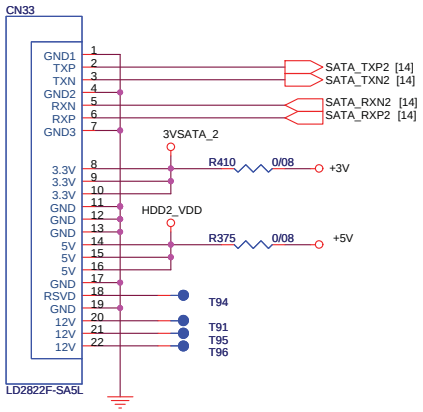
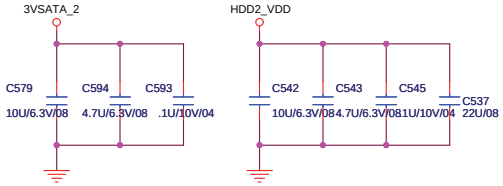
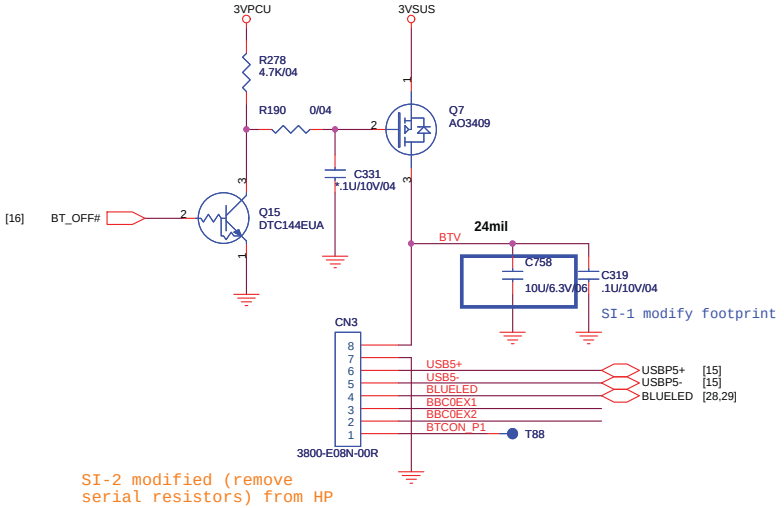
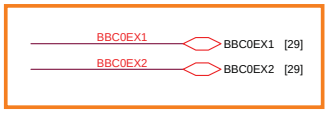
SATA_1 CONNECTOR





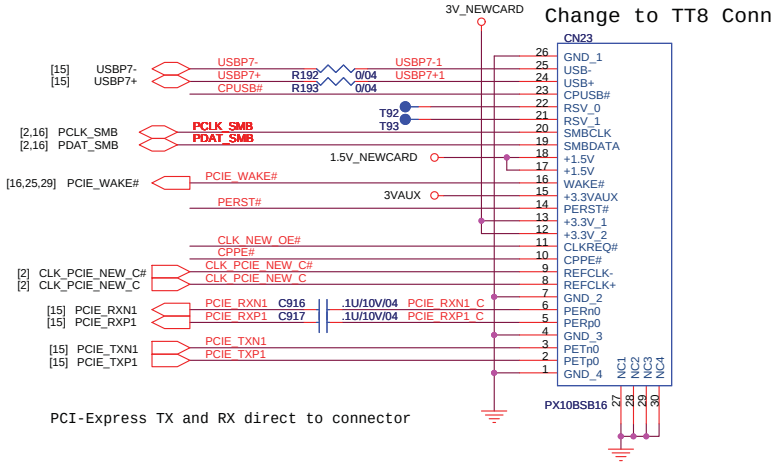
BLUETOOTH



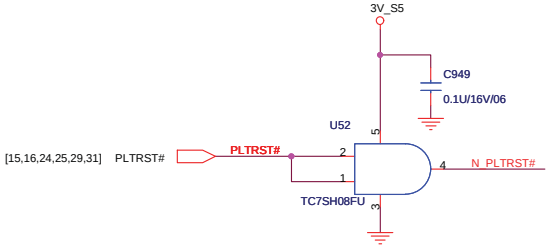


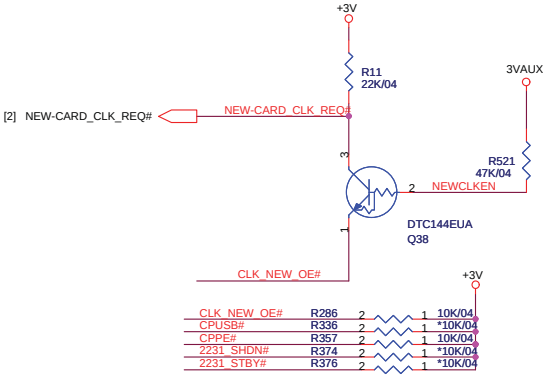
NEWCARD

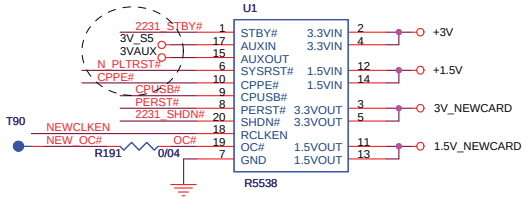
Change to TT8 Conn

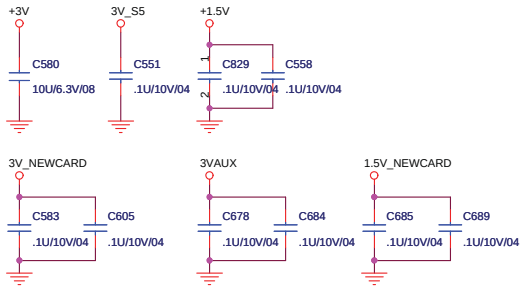


PCI-Express TX and RX direct to connector









PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD/BT	2A

NB5/RD1/HW2

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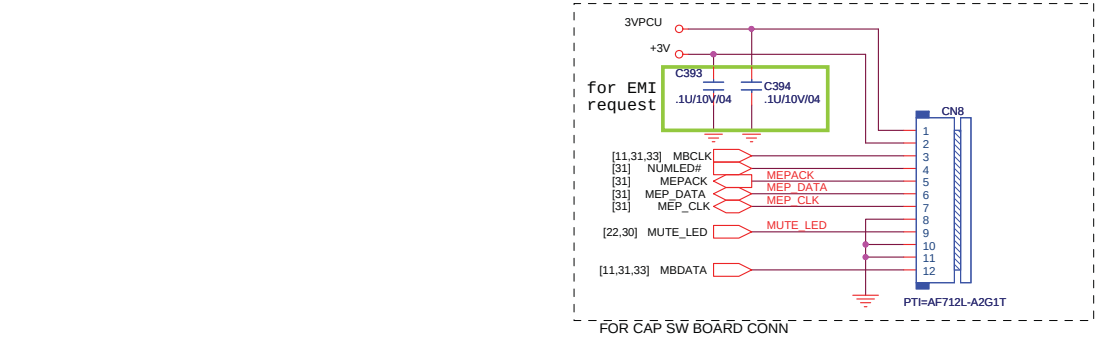
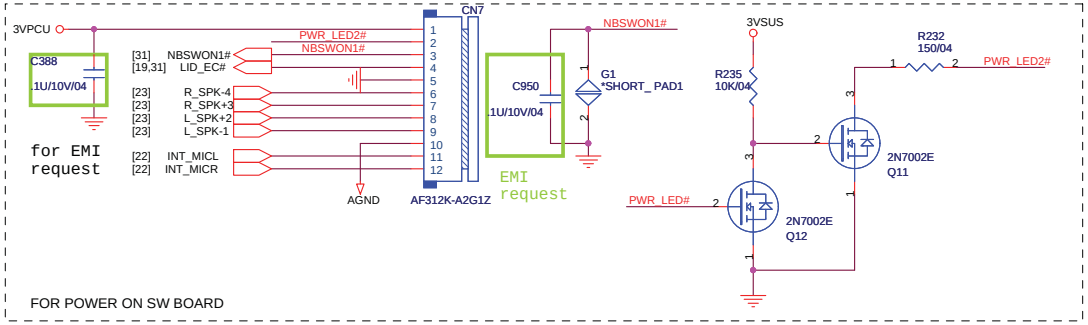
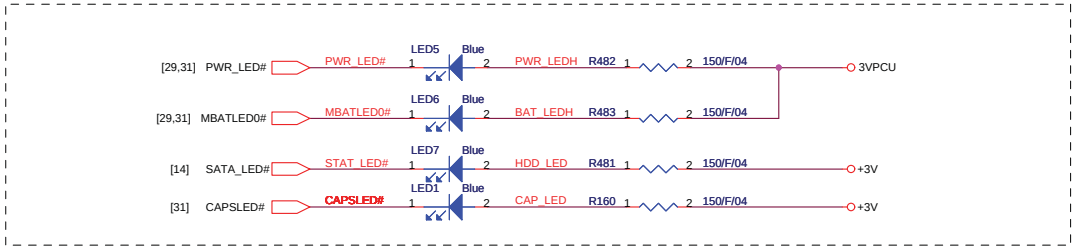
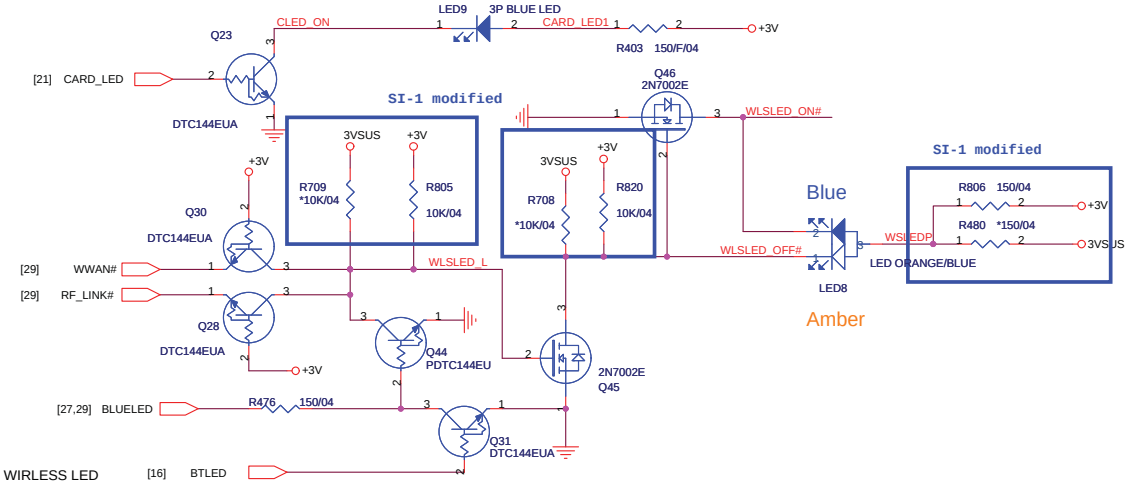
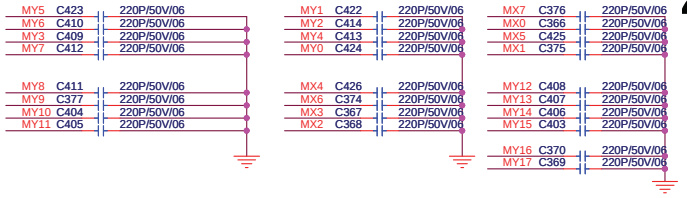


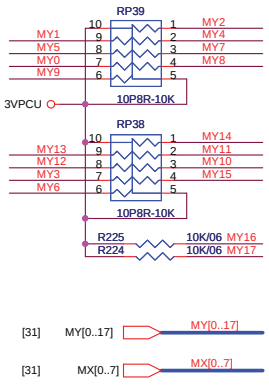


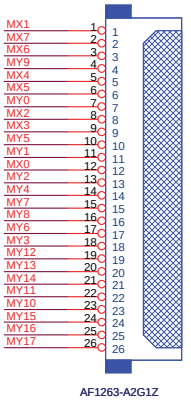


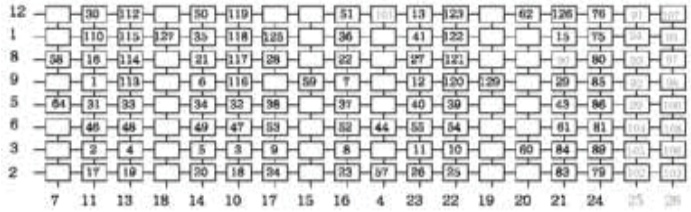




KEYBOARD PULL-UP

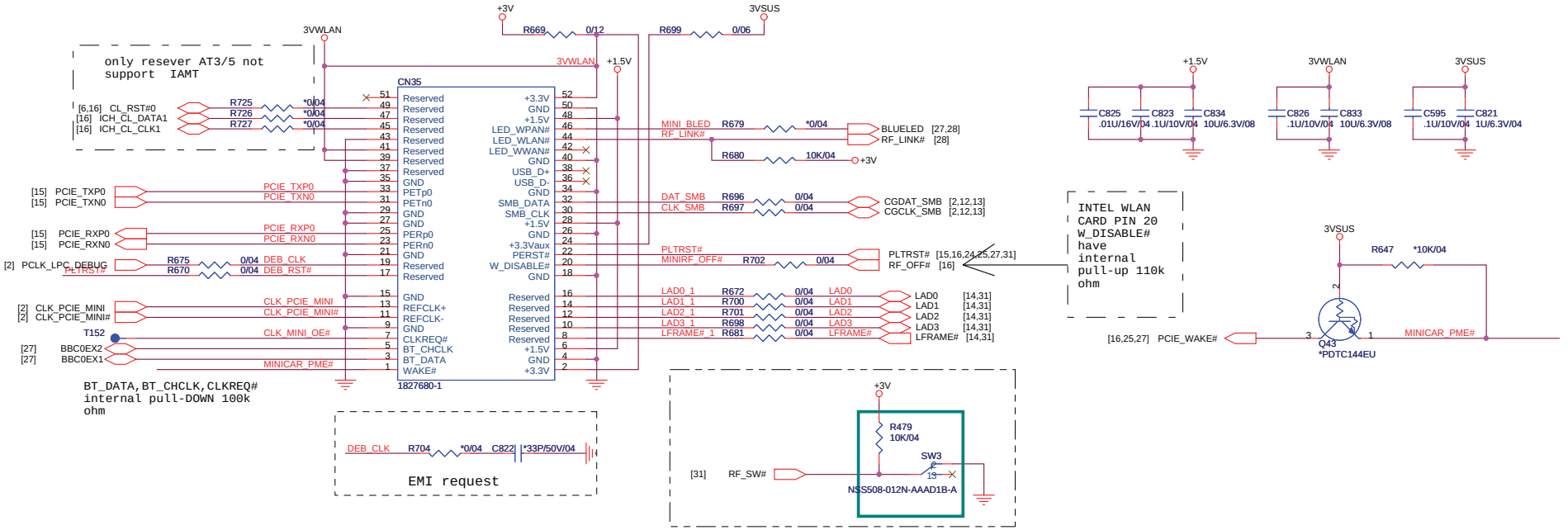






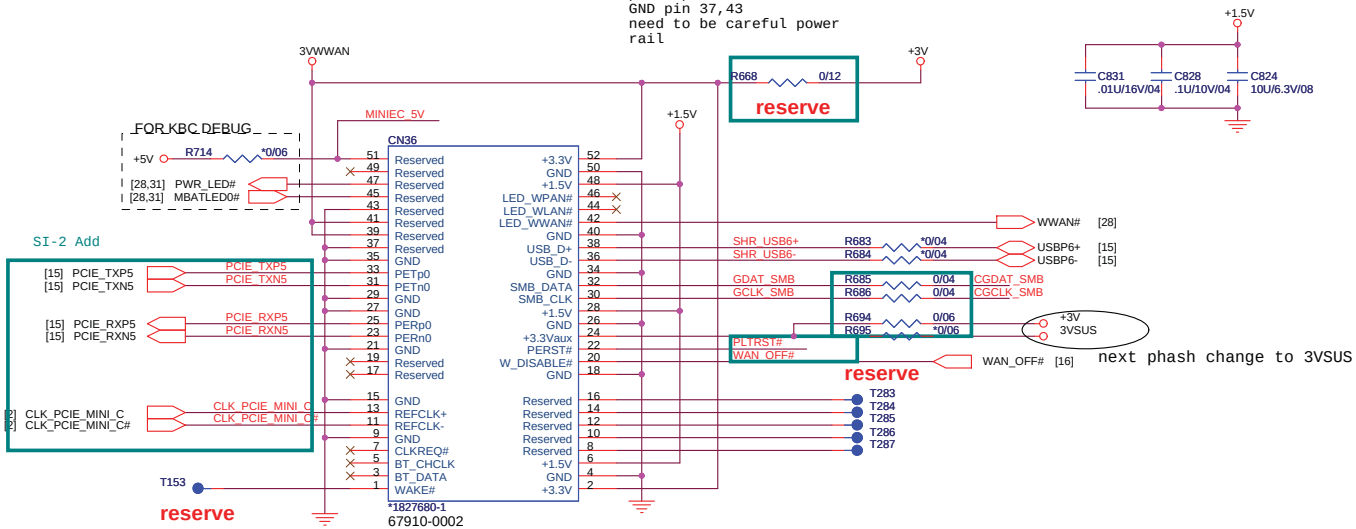
NB5/RD1/HW2	PROJECT : AT3U Quanta Computer Inc.	
	Size: Custom Document Number: LED/KEYBOARD/SW	Rev: 2A
	Date: Wednesday, May 02, 2007	Sheet 28 of 37

Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2

WWAN -- have 2.8A 7W power consumption
power pin 24.39.41
GND pin 37,43
need to be careful power rail



NB5/RD1/HW2	PROJECT : AT3U Quanta Computer Inc.	
	Size: Custom Document Number: MINI CARD X2	Rev: 2A
	Date: Wednesday, May 02, 2007	Sheet 29 of 37

CABLE DOCK

support 6A 200mils
CX000480005

support docking
SPIDF

+1.5V
R522 33_04
C883 .1U/10V/04
SPDDK_V
Q37 MMBT3904
[22] SPDIF
R531 510/F/04
SPDIF_DK
R525 510/F/04
C681 68P/50V/04
L68 0/06
SPD_DK
SPDIF_DOCK

DOCK_VA
L61 FBMJ3216HS480NT/12
[33] DOCK_VA
VA_P
C658 0.1U/50V/06
C651 0.1U/50V/06

SI change EMI request
EMI request

CN18
VA_P
PR_GEN
PR_RED
DDCDAT2
PR_BLU
PR_HSYNC
DDCCLK2
PR_VSYNC
R45 BK1608LL680/06
R38 BK1608LL680/06
R54 BK1608LL680/06
R811 0/06
R812 0/06
CRT_GDK
CRT_RDK
CRT_BDK
PR_HSYNC_D
PR_VSYNC_D
USB4-1
USB4+1
S-YD-DO-PR R510 0/04
S-CD-DO-PR R516 0/04
S-CVBS-DO-PR R518 0/04
S-YD-DO [18]
S-CD-DO [18]
S-CVBS-DO [18]
CIR_IN [22,31]
PWR_ON
MUTE_LED [22,28]
SLP_BTN# [31]
JACK_DETECT# [23]
VOLME_UP# [31]
VOLME_DN# [31]
SPDIF_DOCK
RSPK_DK C60 100U/6.3V
LSPK_DK C75 100U/6.3V
AGND
DOCK_RSPK+ [23]
DOCK_LSPK+ [23]
DOCK_MIC_R [22]
DOCK_MIC_L [22]
DOCK_PRESENT
+LAN_MX1_PR
-LAN_MX1_PR
+LAN_MX0_PR
-LAN_MX0_PR
VIN
C894 0.1U/50V/06
VDD
VSS
QL1122L-H212AR-7F

R528 0/04
USBP4-
USBP4+
L67 *CMM211T-900M-S
R526 0/04
C892 *47P/50V/06
C893 *47P/50V/06

+3V
3VPCU
R844 100K/04
R548 *100K/04
PR_INSERT#
PR_INSERT# [18]
docking
insert is HI
voltage
DOCK_PRESENT
R579
DKPR#
1K/04
Q40 2N7002E
R573 2K/F/06

D33
D34
1N4148
+5V
5VSUS
R520 10K/04
DK_PWRON
PWR_ON
R527 15K/04
S0: 4V
S3: 2.5V
S4/S5:
0V
*Check voltage on DB

DOCK_MIC_R
DOCK_MIC_L
RSPK_DK
LSPK_DK
JACK_DETECT#
VOLME_DN#
CIR_IN
C673 *120P/50V/04
C677 *120P/50V/04
C674 270P/25V/04
C897 180P/50V/04
C898 180P/50V/04
C902 180P/50V/04
C903 180P/50V/04
EMI request

PR_GEN
PR_RED
PR_BLU
CRT_GDK
CRT_RDK
CRT_BDK
C918 5.6P/06
C919 5.6P/06
C920 5.6P/06
C941 5.6P/06
C942 5.6P/06
C943 5.6P/06
fix docking R.G.B
signals measure fail
R56 150/F/04
R30 150/F/04
R39 150/F/04

S-YD-DO-PR
S-CD-DO-PR
S-CVBS-DO-PR
R519 *150/F/04
R517 *150/F/04
R506 *150/F/04

FAN

CPU FAN
20 mil
D39 *SSM34PT L-F
L73 0/08
[31]
5VFAN1
FAN1ON
CN22
PTI=CWP043-A0G1T
+5V
C749 2.2U/6.3V/06
C748 1U/10V/04
R594 4.7K/06
FAN1SIG
FAN1SIG [31]

FAN1 PWM CONNECTOR

N85/RD1/HW2	PROJECT : AT3U Quanta Computer Inc.	
	Size: Custom Document Number: CABLE DOCKING/FAN	Rev: 2A
	Date: Wednesday, May 02, 2007	Sheet 30 of 37

STRAP PIN

MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode

DEL R209,R210,R218,R219,R220

MY2 R208 *10K/04

MY3 R212 *0/04

All hardware straps default internal pull-up, so don't need pull-UP outside. A TEST need try --andrew ????

SELECT KBC TPYE

PIN NAME	USE KBC3920	USE KBC3926
MY2	R208	REMOVE R208
BIOS_A0	REMOVE R808	R808

SI 4/30

remove R245 and add R241

SLPBTN# R241 0/04

NBSWON1# R245 *0/04 SLP_BTN# [30]

SCI1# D9 1N4148 SCI# [16]

PM_BATLOW1# D11 1N4148 PM_BATLOW# [16]

DNBSWON1# D10 1N4148 DNBSWON# [16]

KBSMI#1 D7 1N4148 KBSMI# [16]

SWI#1 D8 1SS355 SWI# [16]

[11] 3920_RST#

3VPCU R221 470K/04 3920_RST# C365 1U/6.3V/04

U50

KB3926

SERIRQ LFRAME# LAD0 LAD1 LAD2 LAD3 PCLK_LPC_KB3920 PLTRST# CLKRUN# SCI1# GATEA20 RCIN#

MX0–MX7 KSI0–KSI7

MY0–MY17 KSO0–KSO17

MEP_CLK MEP_DATA MEPACK ACIN TPCLK TPDATA

BIOS_RD# BIOS_WR# BIOS_CS# SERR# ECPWROK VOLME_UP# VOLME_DN# BIOS_D2–BIOS_D5 SIM_DETECT RF_SW#

BIOS_A0 SUSON MAINON LAN_POWER S5_ON BIOS_A5–BIOS_A11

VCC1–VCC6 AVCC

C451 C395 C463 C465 C396 C454 C402 .1U/10V/04 10U/6.3V/08

AD0/GPI38 AD1/GPI39 AD2/GPI3A AD3/GPI3B TEMP_MBAT MBATV AD_AIR SYS_I

CC-SET CELL_SLT DA_VADJ D/C#

PWM_VADJ KEY_BEEP (1KHz)

FAN1ON FAN2ON FANSIG CIR_IN

MBCLK MBDATA

T303 T304

SUSB# HWPG PM_BATLOW1# SUSC# LAN_REST SWI#1 NBSWON1# BL/C# MBATLED0# PWR_LED# KBSMI#1 VRON NUMLED#

SLPBTN# RPCICGRST# DNBSWON#1 ALERT CAPSLED# TP_LED1# TP_LED2# RSMRST# VOLMUTE# SPI_CLK LID_EC#

T307 T308 T309 T310 T311 T312

XCLKO CRY2 C489 18P/04

XCLKI CRY1 Y2 32.768KHZ C488 18P/04

GND1–GND5 AGND

T263 V18R

+3V R274 *10K/04 HWPG

3VPCU R204 100K/04 CIR_IN; R222 10K/04 NBSWON1#; R215 10K/04 VOLME_UP#; R207 10K/04 VOLME_DN#; R297 10K/04 SLPBTN#; R248 4.7K/04 MBCLK; R261 4.7K/04 MBDATA; R247 *8.2K/04 PM_BATLOW#; R262 10K/04 MEP_CLK; R276 10K/04 MEP_DATA

ICH8 has internal pull-up

+3V R289 *470K/04 LAD0; R294 *470K/04 LAD1; R300 *470K/04 LAD2; R304 *470K/04 LAD3; R306 *470K/04 LFRAME#

SI-1 ADD

PV-2 Add

3VPCU C954 1U/10V/04

R346 10K/04

BIOS_CS# SPI_CLK R813 33_0/4 BIOS_WR# R814 0/04 BIOS_RD# R815 0/04

U17 CE# SCK SI SO WP# VSS HOLD# VDD

SPI_3P SPI_7P

MX25L8005

R314 10K/04

1M byte SPI BIOS

(Amber) LED3 R609 150/04 R610 150/04 TPLD1 TPLD2 TP_LED1# TP_LED2# +3V

(Blue) LED BLUE/AMBER

TOUCH PAD CONNECTOR

25 mils

5VSUS L30 BK1608HS800-T/06 5VTP C330 1U/10V/04

TPCLK L28 SBK160808T-221/06 TPCLK-1

TPDATA L31 SBK160808T-221/06 TPDATA-1

C323 *10P/50V/04 C327 *10P/50V/04

CN4 AF1043-A2G1Z

PCLK_LPC_KB3920 R249 *0/04 C428 *33P/50V/04

for EMI request

5VSUS R290 4.7K/04 TPCLK; R291 4.7K/04 TPDATA

SW1 MY7 MX4 NTC031-AA1G-A160T

NB5/RD1/HW2

PROJECT : AT3U
Quanta Computer Inc.

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Custom	KB3920/ROM/TP	2A

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DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

5 Volt +/- 5%
Countinue current:8A
Peak current:11A
OCP minimum 13A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

Place these CAPs close to FETs

Place these CAPs close to FETs

Rds(on) 13m ohm

Rds(on) 15m ohm

SI-1 MODIFY

PROJECT : AT3U	
Quanta Computer Inc.	
Size: Custom	Document Number: 3v/5v
Rev: 2A	
Date: Wednesday, May 02, 2007	Sheet 32 of 37
N85/RD1/HW2	

C30: Add PD22 for 12cell battery issue

TOP DC_JACK
65W/90W

SI-2 modify

SI-1-2 Add

SI power

SI-2 ADD

SI-2 MODIFY

Setting the Vin min to 8V

Iinput=Vcls/Vref * 0.075/RS1
Vref=4.096V,RS1=10m-ohm

ADP TYPE	VALUE	P/N
65W	39.2K/F	CS33922FB15
90W	20K/F	CS32002FB29

CELL_SLT = 1 -- 3 S
CELL_SLT = 0 -- 4 S

Battery Low = 8V

BL/C#	D/C#	M/A#	Status
0	0	0	Chareg A batt
0	0	1	Charge M batt
0	1	0	Discharge A batt
0	1	1	Discharge M batt
1	0	0	Free Dicharge
1	0	1	Free Dicharge
1	1	0	Free Dicharge
1	1	1	Free Dicharge

PROJECT : AT3U
Quanta Computer Inc.

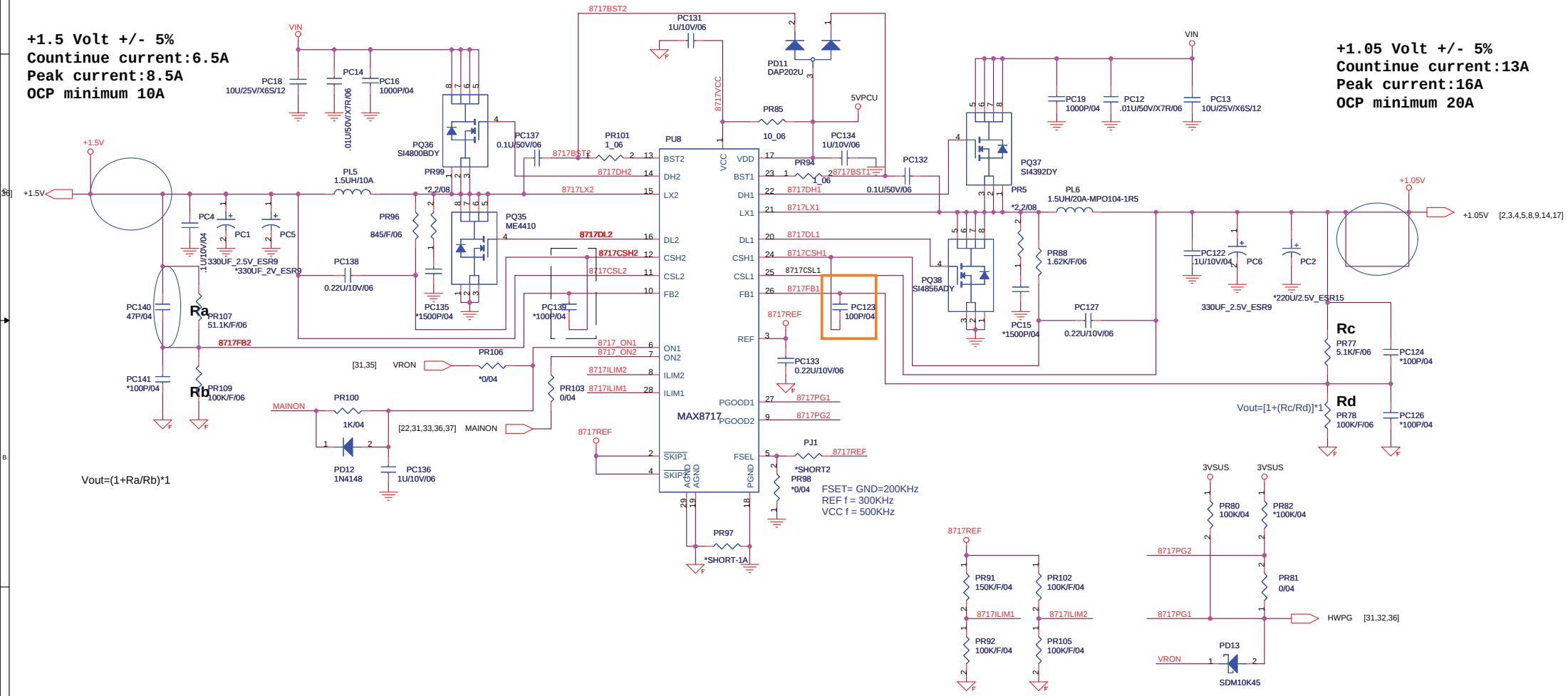
NB5/RD1/HW2

Size: Custom | Document Number: SYSTEM CHARGER(MAX8724) | Rev: 2A

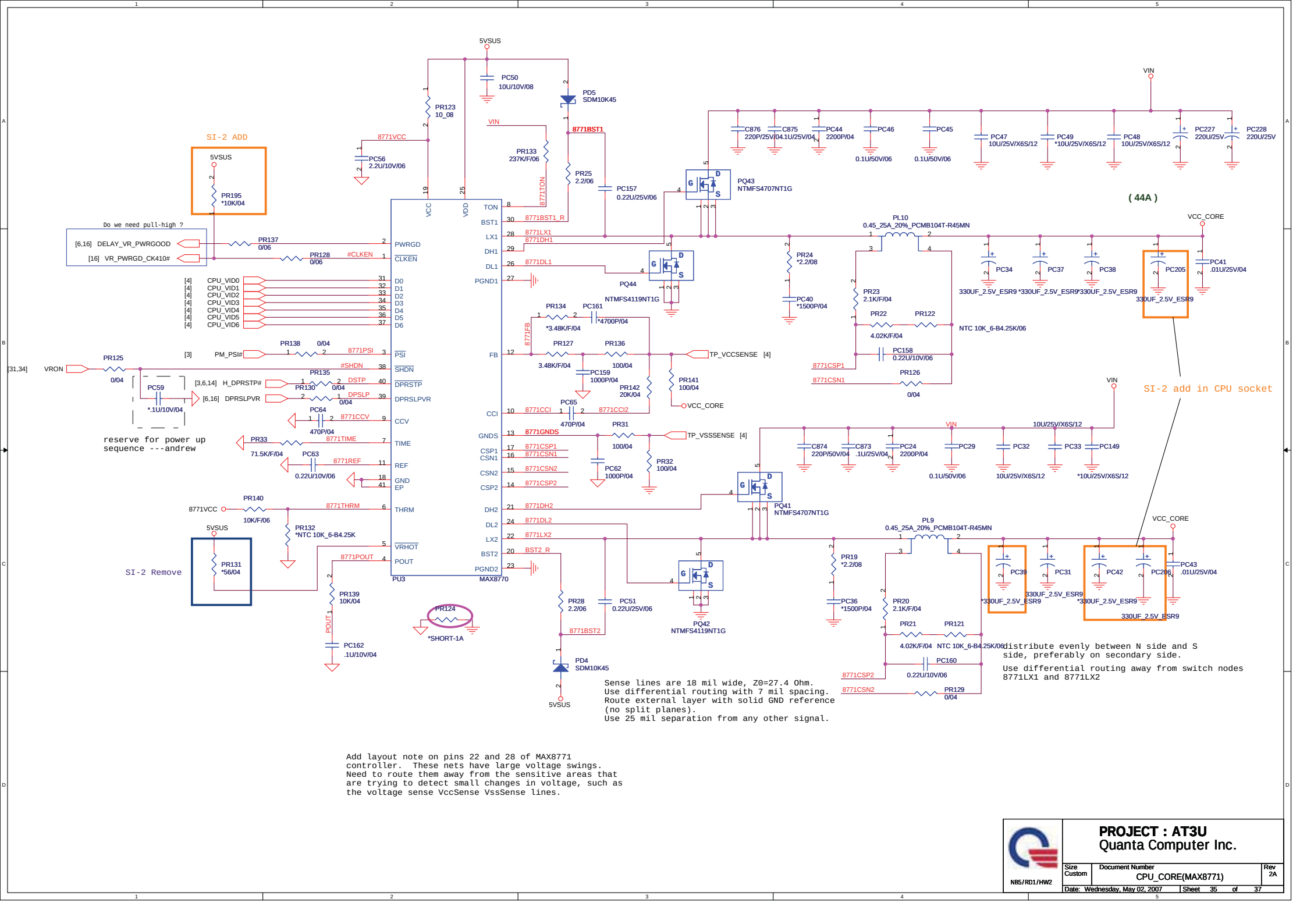
Date: Wednesday, May 02, 2007 | Sheet 33 of 37

+1.5 Volt +/- 5%
Countinue current:6.5A
Peak current:8.5A
OCP minimum 10A

+1.05 Volt +/- 5%
Countinue current:13A
Peak current:16A
OCP minimum 20A



PROJECT : AT3U	
Quanta Computer Inc.	
NB5/RD1/HW2	
Size: Custom	Document Number: +-1.5V &VCCP+1.05V(MAX8743)
Rev: 2A	
Date: Wednesday, May 02, 2007	Sheet 34 of 37


5VSUS
PC50
10U/10V/08
PD5
SDM10K45
PR123
10_08
8771VCC
PC56
2.2U/10V/06
VIN
PR133
237K/F/06
8771TON
8771BST1
PR25
2.2/06
PC157
0.22U/25V/06
SI-2 ADD
PR195
*10K/04
Do we need pull-high ?
[6,16] DELAY_VR_PWRGOOD
[16] VR_PWRGD_CK410#
PR137
0/06
PR128
0/06
#CLKEN
PWRGD
CLKEN
[4] CPU_VID0
[4] CPU_VID1
[4] CPU_VID2
[4] CPU_VID3
[4] CPU_VID4
[4] CPU_VID5
[4] CPU_VID6
D0
D1
D2
D3
D4
D5
D6
[3] PM_PSI#
PR138
0/04
8771PSI
PSI
[31,34] VRON
PR125
0/04
#SHDN
SHDN
PR135
PC59
*.1U/10V/04
[3,6,14] H_DPRSTP#
PR130
0/04
DSTP
DPRSTP
[6,16] DPRSLPVR
DPSLP
0/04
DPRSLPVR
PC64
470P/04
8771CCV
CCV
reserve for power up
sequence ---andrew
PR33
71.5K/F/04
8771TIME
TIME
PC63
0.22U/10V/06
8771REF
REF
GND
EP
PR140
10K/F/06
8771VCC
8771THRM
THRM
PR132
*NTC 10K_6-B4.25K
5VSUS
SI-2 Remove
PR131
*56/04
VRHOT
POUT
8771POUT
PR139
10K/04
POUT1
PC162
.1U/10V/04
PR124
*SHORT-1A
VCC
VDD
TON
BST1
LX1
DH1
DL1
PGND1
FB
CCI
GNDS
CSP1
CSN1
CSN2
CSP2
DH2
DL2
LX2
BST2
PGND2
PU3
MAX8770
8771BST1_R
8771LX1
8771DH1
8771DL1
PQ44
NTMFS4119NT1G
PR134
*3.48K/F/04
PC161
*4700P/04
8771FB
PR127
3.48K/F/04
PR136
100/04
PC159
1000P/04
PR142
20K/04
PR141
100/04
TP_VCCSENSE [4]
VCC_CORE
PC65
470P/04
8771CCI
8771CCI2
8771GNDS
PR31
100/04
TP_VSSSENSE [4]
PR32
100/04
PC62
1000P/04
8771CSP1
8771CSN1
8771CSN2
8771CSP2
8771DH2
8771DL2
8771LX2
BST2_R
PR28
2.2/06
PC51
0.22U/25V/06
8771BST2
PD4
SDM10K45
5VSUS
PQ42
NTMFS4119NT1G
PQ43
NTMFS4707NT1G
PQ41
NTMFS4707NT1G
C876
220P/25V/04
C875
.1U/25V/04
PC44
2200P/04
PC46
0.1U/50V/06
PC45
0.1U/50V/06
PC47
10U/25V/X6S/12
PC49
*10U/25V/X6S/12
PC48
10U/25V/X6S/12
PC227
220U/25V
PC228
220U/25V
(44A)
PL10
0.45_25A_20%_PCMB104T-R45MN
PR24
*2.2/08
PC40
*1500P/04
PR23
2.1K/F/04
PR22
4.02K/F/04
PR122
NTC 10K_6-B4.25K/06
PC158
0.22U/10V/06
PR126
0/04
8771CSP1
8771CSN1
VCC_CORE
PC34
330UF_2.5V_ESR9
PC37
*330UF_2.5V_ESR9
PC38
*330UF_2.5V_ESR9
PC205
330UF_2.5V_ESR9
PC41
.01U/25V/04
SI-2 add in CPU socket
C874
220P/50V/04
C873
.1U/25V/04
PC24
2200P/04
PC29
0.1U/50V/06
PC32
10U/25V/X6S/12
PC33
10U/25V/X6S/12
PC149
*10U/25V/X6S/12
PL9
0.45_25A_20%_PCMB104T-R45MN
PR19
*2.2/08
PC36
*1500P/04
PR20
2.1K/F/04
PR21
4.02K/F/04
PR121
NTC 10K_6-B4.25K/06
PC160
0.22U/10V/06
PR129
0/04
8771CSP2
8771CSN2
PC39
*330UF_2.5V_ESR9
PC31
330UF_2.5V_ESR9
PC42
*330UF_2.5V_ESR9
PC206
330UF_2.5V_ESR9
PC43
.01U/25V/04
distribute evenly between N side and S
side, preferably on secondary side.
Use differential routing away from switch nodes
8771LX1 and 8771LX2
Sense lines are 18 mil wide, Z0=27.4 Ohm.
Use differential routing with 7 mil spacing.
Route external layer with solid GND reference
(no split planes).
Use 25 mil separation from any other signal.
Add layout note on pins 22 and 28 of MAX8771
controller. These nets have large voltage swings.
Need to route them away from the sensitive areas that
are trying to detect small changes in voltage, such as
the voltage sense VccSense VssSense lines.
PROJECT : AT3U
Quanta Computer Inc.
Size
Custom
Document Number
CPU_CORE(MAX8771)
Rev
2A
NB5/RD1/HW2
Date: Wednesday, May 02, 2007
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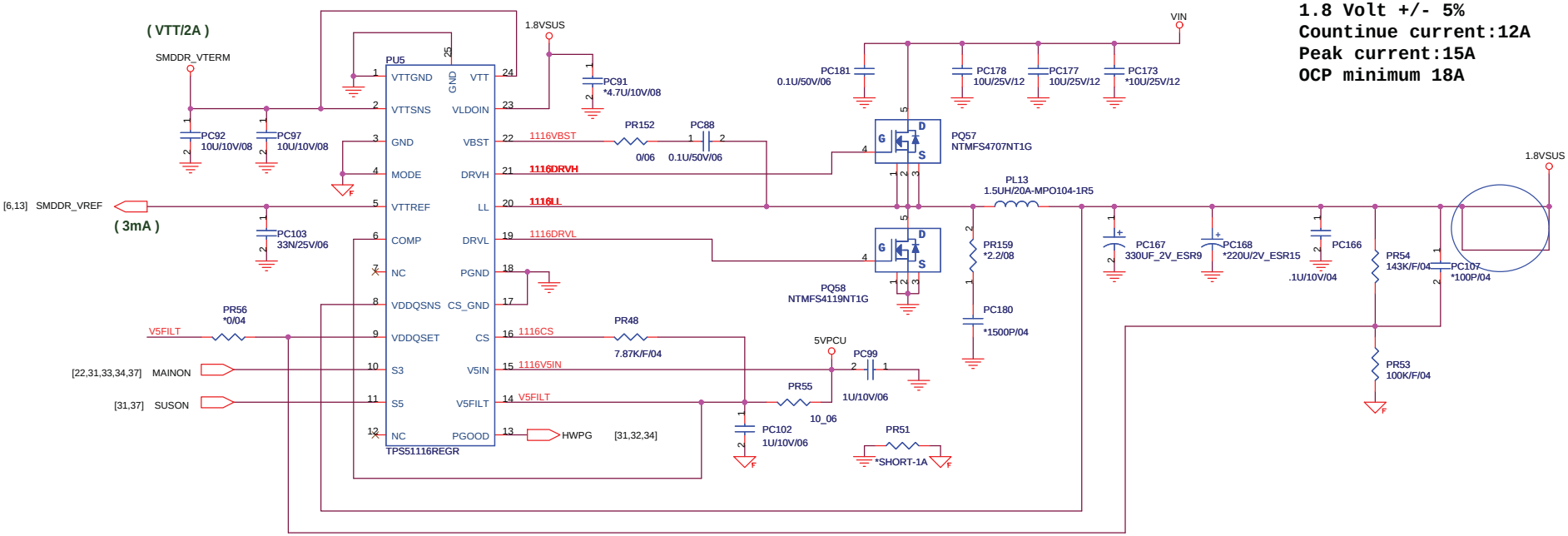
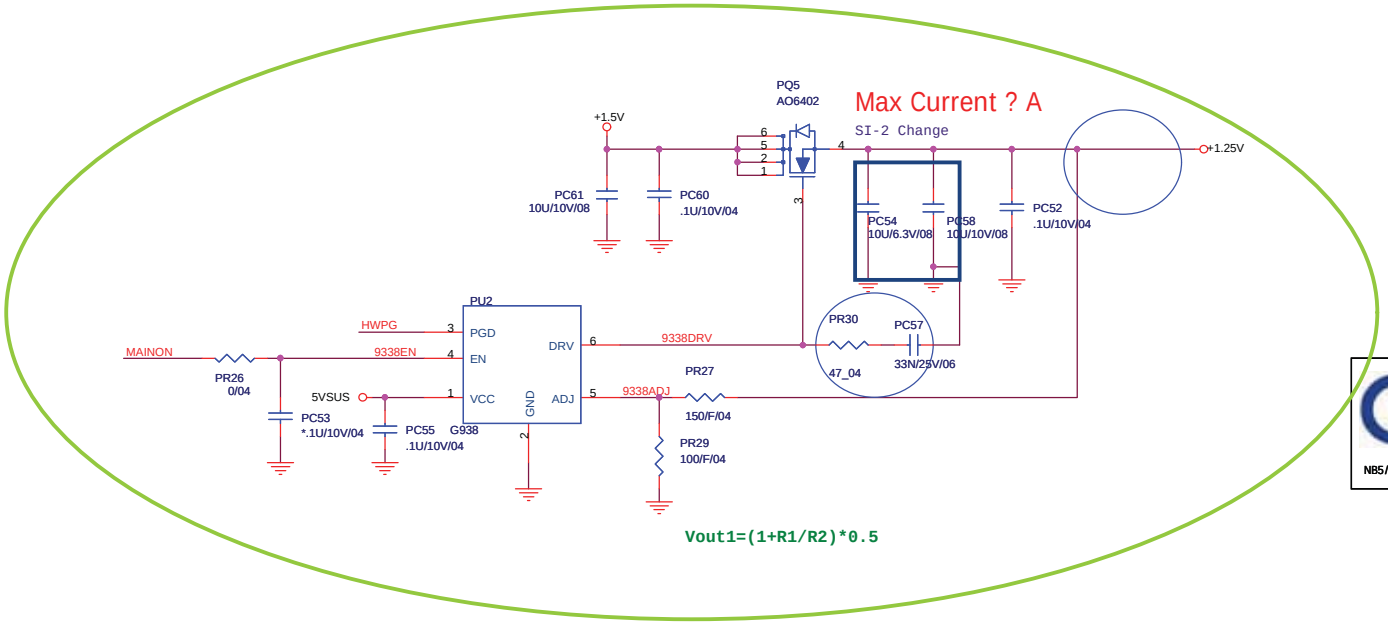
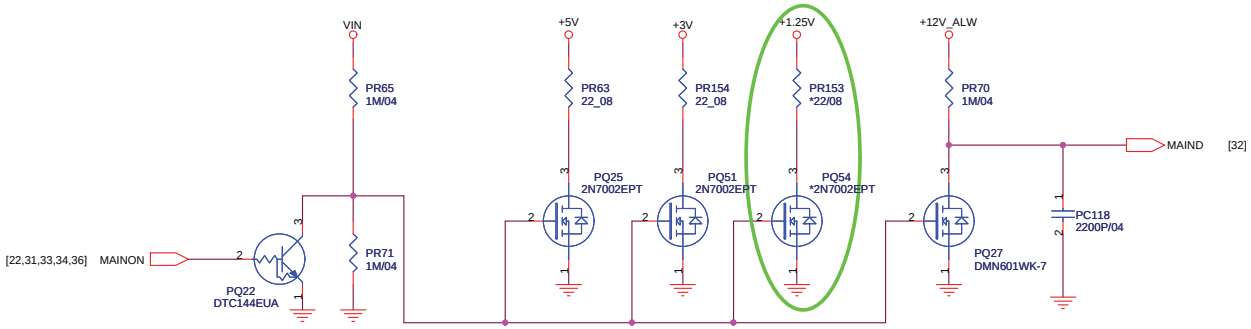


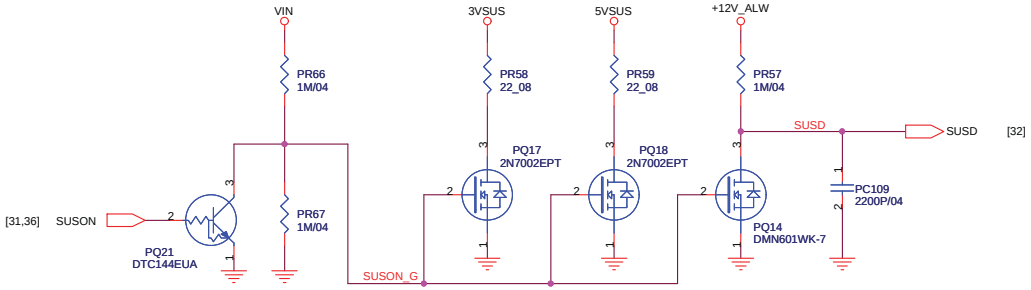


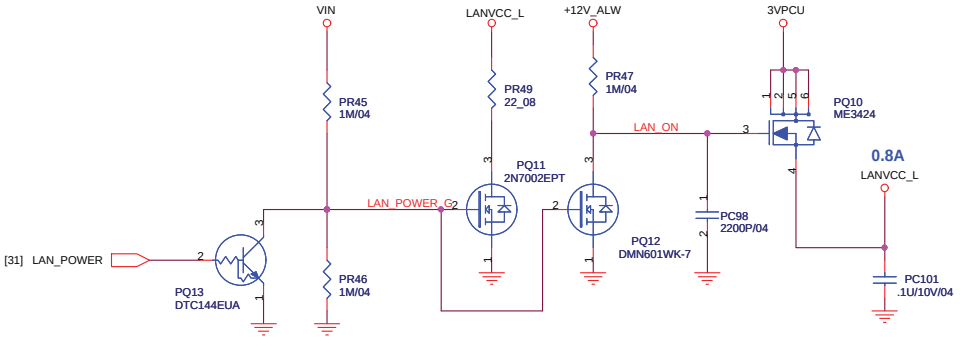
NB5/RD1/HW2

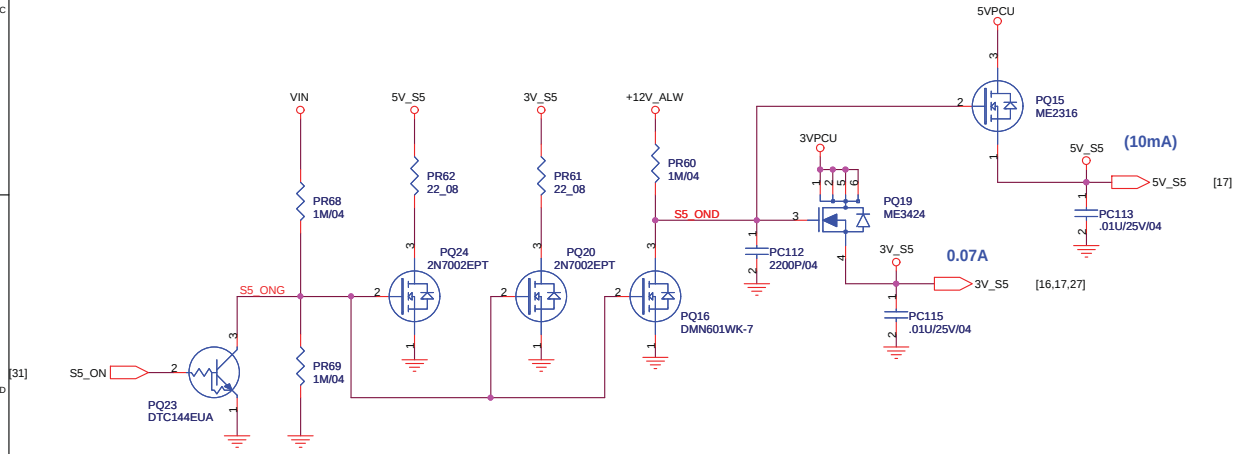
PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII 1.8VSUS/SMDDR_VTERM	2A
Date: Wednesday, May 02, 2007	Sheet 36 of 37	









PROJECT : AT3U
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE	2A
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