# R33 INTEL UMA/DISCRETE SYSTEM DIAGRAM 01

+3V/+5V S5 PG.35
+1.05V_VTT PG.38
CPU Core PG.40~41
DDR3 PG.37
VCCSA PG.36
Charge PG.34
Dis-Charge PG.39
+VGACORE PG.42
+1.0V_VGA PG.43

SODIMM1 Max. 4GB PG.12 — DDR3 Channel A
SODIMM2 Max. 4GB PG.13 — DDR3 Channel B

**INTEL IVY**
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.2~5

PCI-E x8

**AMD Thames XT**
29mm X 29mm
TDP 25W
PG.14~20

DDR3 900MHz
**VRAM** 128Mx16x8,128bit PG.21~22

FDI DMI

**INTEL PCH Panther Point**
PG.6~11

HDMI PG.25
CRT PG.24
LVDS PG.23

HDD PG.32 — SATA0
ODD PG.32 — SATA1

DP Port B
CRT
LVDS

PCI-E x 1 — LANE2 / LANE1
LAN RTL8105EH 10/100 PG.29
WLAN BT COMBO PG.33 — USB 2.0 PORT10

PCI-E x 1 — LANE3
Accelerometer PG.33 — SMBUS
Card Reader RTS5229 PG.26

KBC EnE KB3930QF A2 PG.30 — LPC
KB PG.31 | TP PG.31 | ROM PG.30 | FAN PG.32

USB 3.0
USB3.0 Ports X2 PG.28 — PORT1,2
Webcam PG.23 — PORT4
USB 2.0 — PORT0,1
USB2.0 Ports PG.28

AUDIO CODEC
IDT 92HD87
ICT PG.27

Speaker PG.27
HP/MIC PG.28
Analog MIC PG.28

**Stackup**
TOP
GND
IN1
IN2
VCC
BOT

NB5

PROJECT : R33
Quanta Computer Inc.

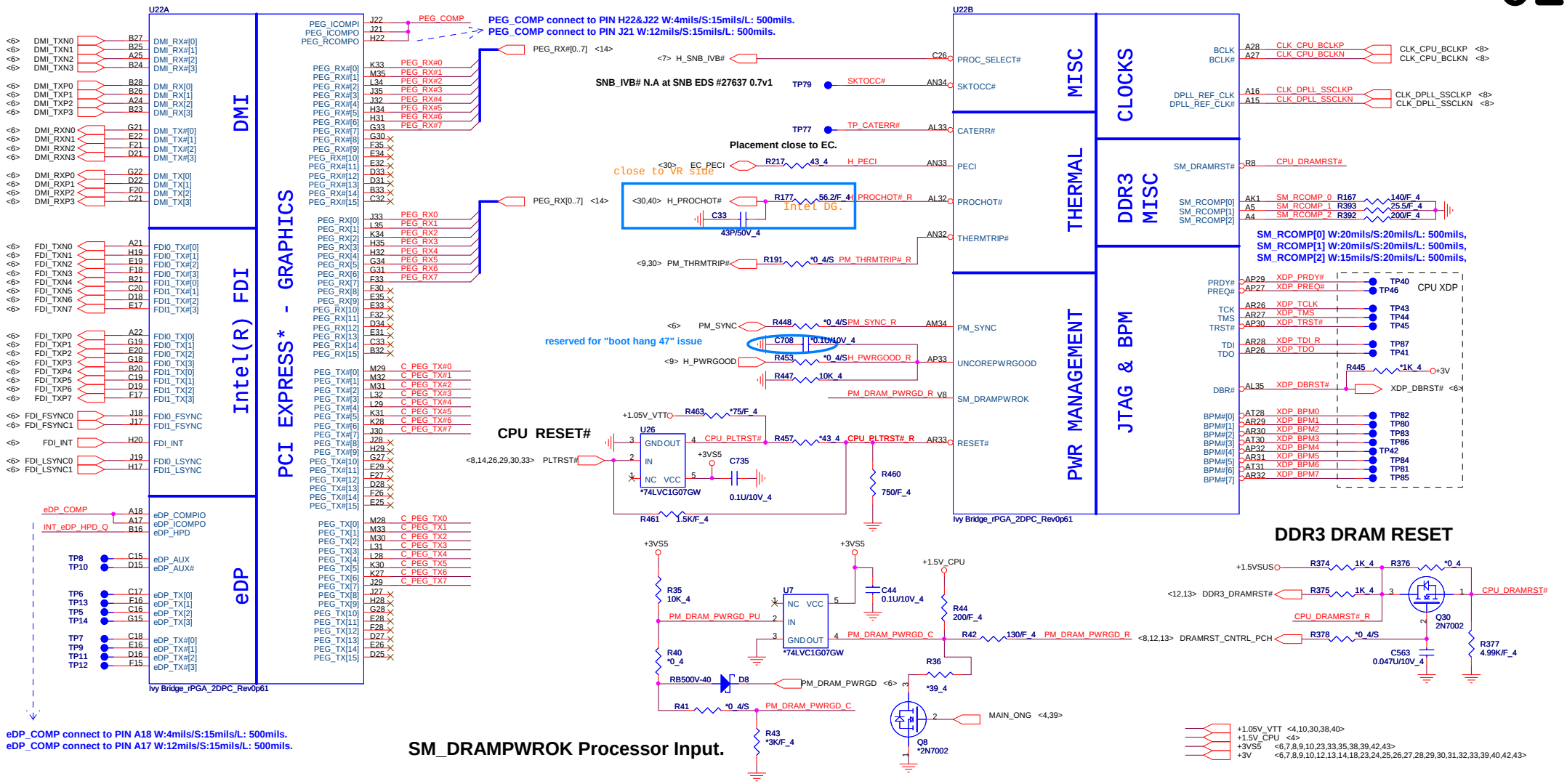
| Size | Document Number | Rev |
|---|---|---|
| Custom | BLOCK DIAGRAM | 1A |

Date: Wednesday, September 07, 2011 Sheet 1 of 43

# Ivy Bridge Processor (DMI,PEG,FDI)

# Ivy Bridge Processor (CLK,MISC,JTAG)

02

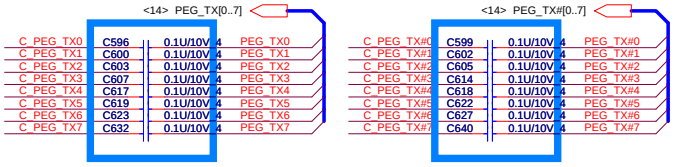



## FDI disable (DIS only stuff)

DEL

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

## PEG x16 disable (UMA only remove)

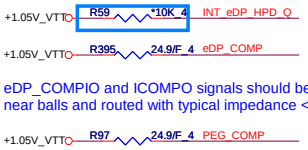



0.22uF AC coupling Caps for PCIE GEN1/2/3

0.22uF AC coupling Caps for PCIE GEN1/2/3

## DP & PEG Compensation

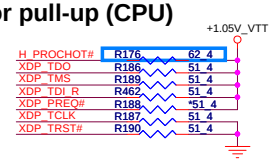
check




eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

## Processor pull-up (CPU)




NB5

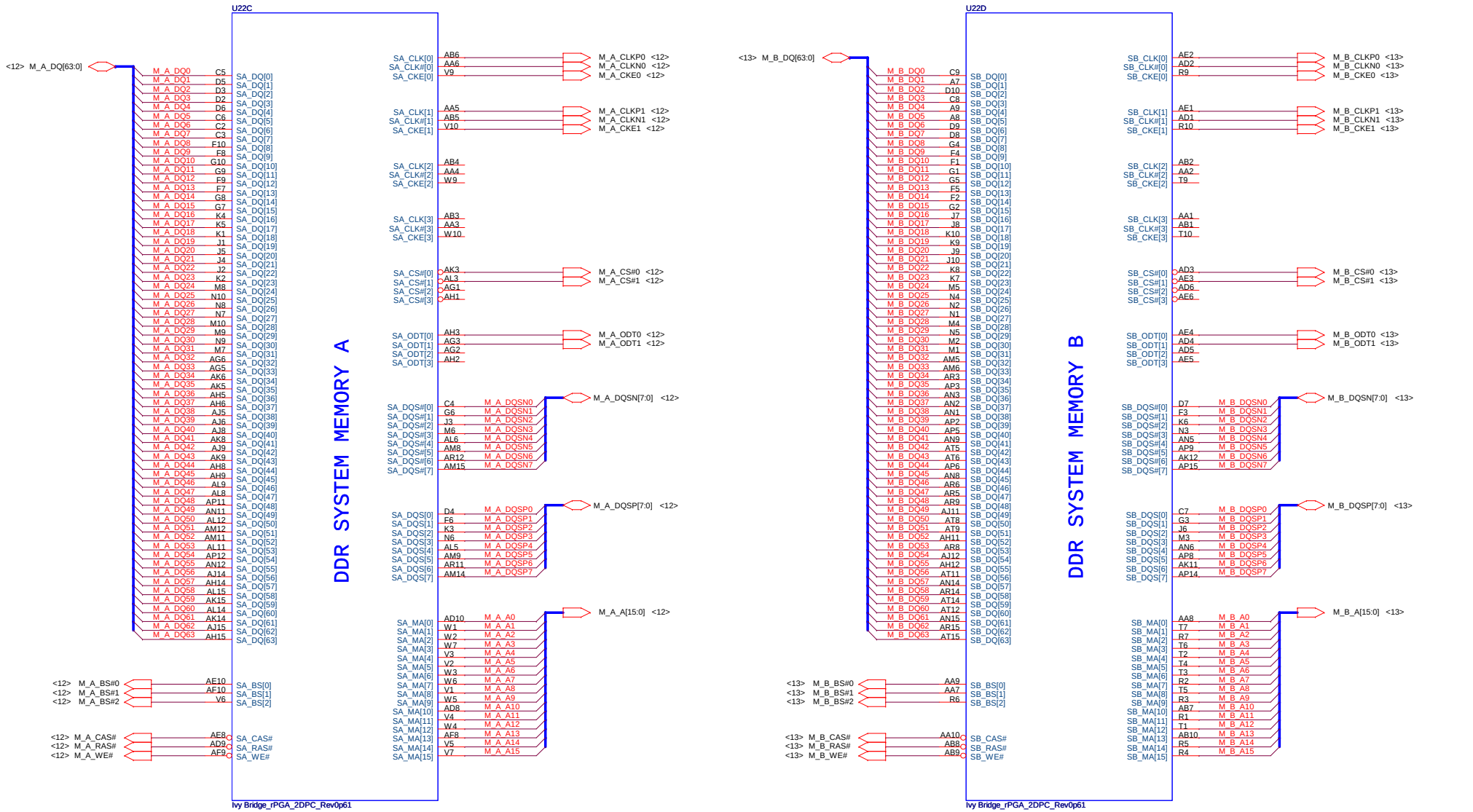
**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | SNB 1/4 (PCIE&DMI&FDI) | 1A |

Date: Wednesday, August 31, 2011 Sheet 2 of 43

# Ivy Bridge Processor (DDR3)






**PROJECT : R33**
Quanta Computer Inc.

NB5

| Size | Document Number | Rev |
|---|---|---|
| Custom | SNB 2/4 (DDR3 I/F) | 1A |

Date: Wednesday, August 31, 2011 | Sheet 3 of 43

# Ivy Bridge Processor (POWER)

04

## POWER

U22F

SNB: 55A
IVY: 55A

+VCC_CORE

C638 22U/6.3VS_8 C682 10U/6.3VS_6 C637 22U/6.3VS_8
C80 22U/6.3VS_8 C67 22U/6.3VS_8 C193 22U/6.3VS_8
C664 22U/6.3VS_8 C196 22U/6.3VS_8 C272 22U/6.3VS_8
C699 22U/6.3VS_8 C53 22U/6.3VS_8 C639 22U/6.3VS_8
C199 22U/6.3VS_8 C691 *10U/6.3V_6S C58 22U/6.3VS_8
C160 22U/6.3VS_8 C277 22U/6.3VS_8 C303 22U/6.3VS_8
C248 22U/6.3VS_8 C233 22U/6.3VS_8 C179 22U/6.3VS_8
C684 *22U/6.3VS_8 C222 *22U/6.3VS_8 C576 22U/6.3VS_8
C192 22U/6.3VS_8 C678 10U/6.3VS_6 C253 22U/6.3VS_8
C573 22U/6.3VS_8 C572 22U/6.3VS_8 C695 *10U/6.3V_6S

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

CORE SUPPLY

Ivy Bridge_rPGA_2DPC_Rev0p61

### PEG AND DDR

SNB: 8.5A
IVY: 8.5A

+1.05V_VTT

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

C165 22U/6.3VS_8 C156 22U/6.3VS_8 C626 22U/6.3VS_8
C271 22U/6.3VS_8 C207 22U/6.3VS_8 C184 22U/6.3VS_8
C155 *22U/6.3VS_8 C227 22U/6.3VS_8 C666 22U/6.3VS_8
C677 *22U/6.3VS_8 C218 *22U/6.3VS_8 C88 *22U/6.3VS_8
5/14 modify
C635 22U/6.3VS_8 C94 *22U/6.3VS_8 C302 *22U/6.3VS_8
C188 *22U/6.3VS_8 C652 22U/6.3VS_8 C247 *22U/6.3VS_8
C657 *22U/6.3VS_8 C645 22U/6.3VS_8 C168 22U/6.3VS_8

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

### SVID

+1.05V_VTT

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

### SENSE LINES

VCC_SENSE AJ35 VSS_SENSE AJ34
R157 100_4 +VCC_CORE
VCC_SENSE <40>
VSS_SENSE <40>
R160 100_4

VCCIO_SENSE B10 VSS_SENSE_VCCIO A10
VCCP_SENSE VCCP_SENSE <38>
VSSP_SENSE VSSP_SENSE <38>

Trace Route to Power IC area.

+1.05V_VTT
VCCP_SENSE R394 10/F_4
VSSP_SENSE R390 10/F_4

+1.5V <10,12,33>
+1.8V <7,10,38,43>
+VCCSA <36>
+1.5VSUS <2,10,12,13,37,43>
+1.5V_CPU <2>
+VCC_GFX <41>
+1.05V_VTT <2,10,30,38,40>
+VCC_CORE <41>

## POWER

U22G

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

+VCC_GFX SNB: 21.5A

C669 22U/6.3V_8 C273 22U/6.3V_8
C305 22U/6.3V_8 C324 22U/6.3V_8
C304 22U/6.3V_8 C670 22U/6.3V_8
C325 22U/6.3V_8 C249 22U/6.3V_8
C668 22U/6.3V_8 C250 22U/6.3V_8
C274 22U/6.3V_8 C671 22U/6.3V_8

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

GRAPHICS

### 1.8V RAIL

+1.8V SNB: 1.5A

C55 10U/6.3V_8 C51 1U/6.3V_4 C50 1U/6.3V_4 C65 *330u_2.5V_3528

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

Ivy Bridge_rPGA_2DPC_Rev0p61

### SENSE LINES

VAXG_SENSE AK35
VSSAXG_SENSE AK34
R162 100/F_4 +VCC_GFX
VCC_AXG_SENSE <40>
VSS_AXG_SENSE <40>
R166 100/F_4

### VREF

+VDDR_REF_CPU
CAD Note: +VDDR_REF_CPU should have 10 mil trace width

SM_VREF AL1
R192 100K_4
Q18 2N7002
DDR_VTTREF <12,13,37>
MAIND MAIND <39>

SA_DIMM_VREFDQ B4
SB_DIMM_VREFDQ D1
SMDDR_VREF_DQ0_M3 <12>
SMDDR_VREF_DQ1_M3 <13>
R391 *1K_4 R386 *1K_4

### DDR3 -1.5V RAILS

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

SNB: 5A +1.5V_CPU

C320 10U/6.3V_6 C226 10U/6.3V_8 C310 10U/6.3V_6 C275 10U/6.3V_6
C209 10U/6.3V_6 C341 10U/6.3V_6 C737 *330U_2.5V_5.0x5.9_ESR10m

330uF x1, 10uF_8 x6 Socket BOT edge.

### SA RAIL

SNB: 6A +VCCSA

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

C625 10U/6.3V_8 C579 10U/6.3V_8 C630 10U/6.3V_8 C571 *10U/6.3V_8

330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.

### MISC

VCCSA_SENSE H23 VCCUSA_SENSE_R R85 *0_4/S VCCUSA_SENSE <36>
VCCSA_VID[0] C22 VCCSA_SEL0 R71 10K_4 VCCSA_SEL0 <36>
VCCSA_VID[1] C24 VCCSA_SEL R73 10K_4 VCCSA_SEL <36>
VCCIO_SEL A19 VTTVID1 R389 0_4 H_VTTVID1 <38>

+1.5V_CPU R50 *0_8/S +1.5V
40mile routing

Layout note: need routing together and ALERT need between CLK and DATA.

### SVID CLK

H_CPU_SVIDCLK VR_SVID_CLK <40>

### SVID DATA

+1.05V_VTT +1.05V_VTT
Place PU resistor close to CPU
R172 130/F_4
R175 *130/F_4
Place PU resistor close to VR
H_CPU_SVIDDAT VR_SVID_DATA <40>

Place PU resistor close to CPU

### SVID ALERT

C352 0.1U/10V_4
+1.05V_VTT R170 75/F_4
H_CPU_SVIDALRT# R171 43_4 VR_SVID_ALERT# <40>

### CPU VDDQ

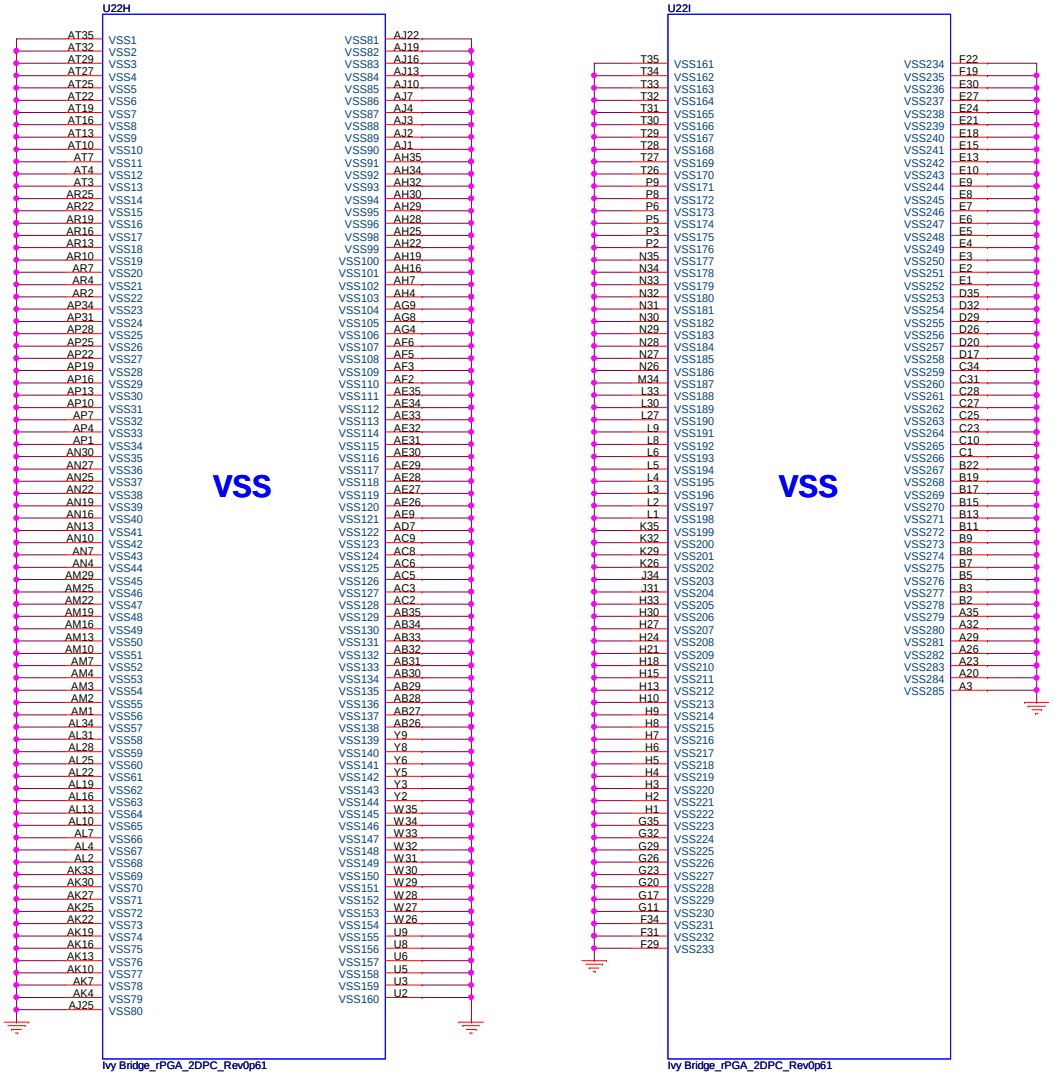
+1.5VSUS +1.5V_CPU +1.5VSUS
Q10 AON7410
R229 220_8
MAIND
C582 0.1U/10V_4
C580 0.1U/10V_4
C574 0.1U/10V_4
C577 0.1U/10V_4
Placement close to CPU.
C54 *470P/50V_4
Q22 2N7002
MAIN_ONG <2,39>

NB5

PROJECT : R33
Quanta Computer Inc.

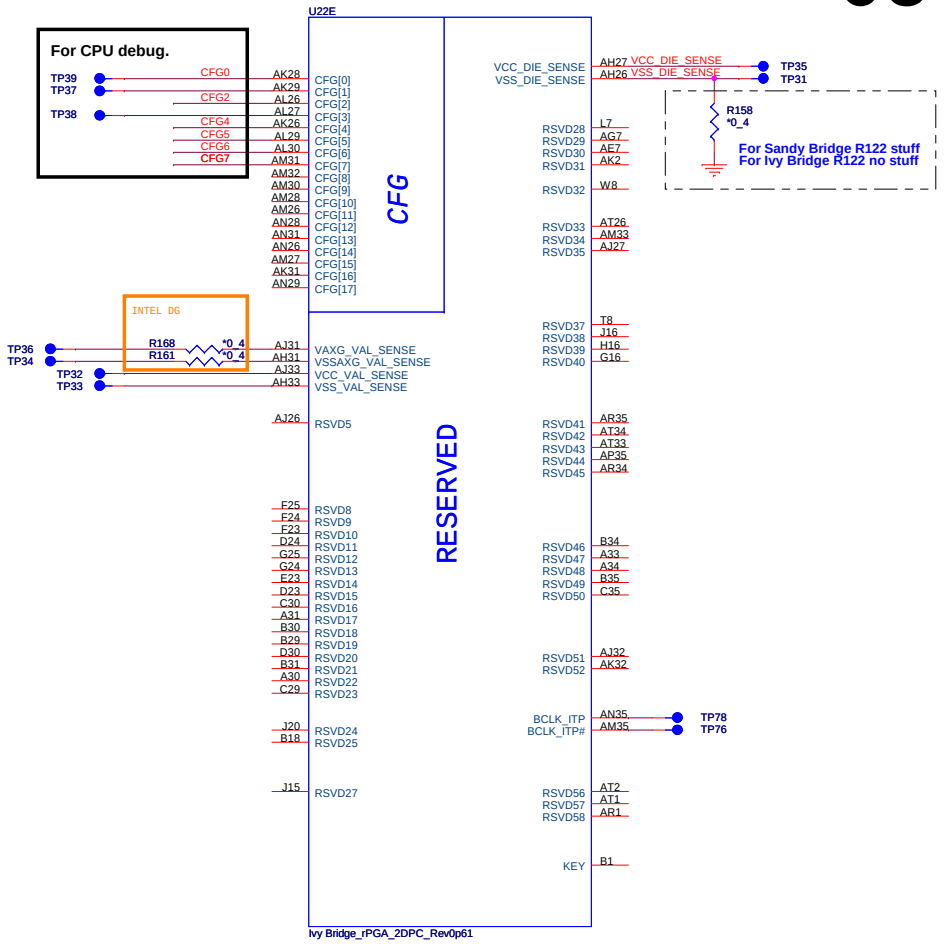
| Size | Document Number | Rev |
|---|---|---|
| Custom | SNB 3/4 (POWER) | 1A |
| Date: Wednesday, August 31, 2011 | Sheet 4 of 43 | |

# Ivy Bridge Processor (GND)




# Ivy Bridge Processor (RESERVED, CFG)





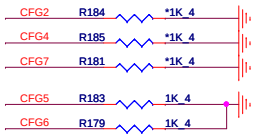

## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

| | 1 | 0 |
|---|---|---|
| CFG2<br>(PEG Static Lane Reversal) | Normal Operation | Lane Reversed |
| CFG4<br>(DP Presence Strap) | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP |
| CFG7<br>(PEG Defer Training) | PEG train immediately following xxRESETB de assertion | PEG wait for BIOS training |

**CFG[6:5] (PCIE Port Bifurcation Straps)**

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled




NB5

**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | SNB 4/4 (GND) | 1A |

Date: Wednesday, August 31, 2011 Sheet 5 of 43

# Cougar Point/Panther Point (DMI,FDI,PM)

# Cougar Point/Panther Point (LVDS,DDI)

06

U32C

U32D

PD Res place close to PCH

PCH to Res routeing 37.5 ohm Impedance.

Res to connector filter routeing 50ohm Impedance.

Reserve from EMI request

Reserve for power on sequence

## PCH Pull-high/low(CLG)

## INT HDMI disable (DIS only remove)

INT HDMI Detect Function

## System PWR_OK(CLG)

## DPWROK FOR DSW

Remove DSW power rail

On Die DSW VR Enable

High = Enable (Default)
Low = Disable

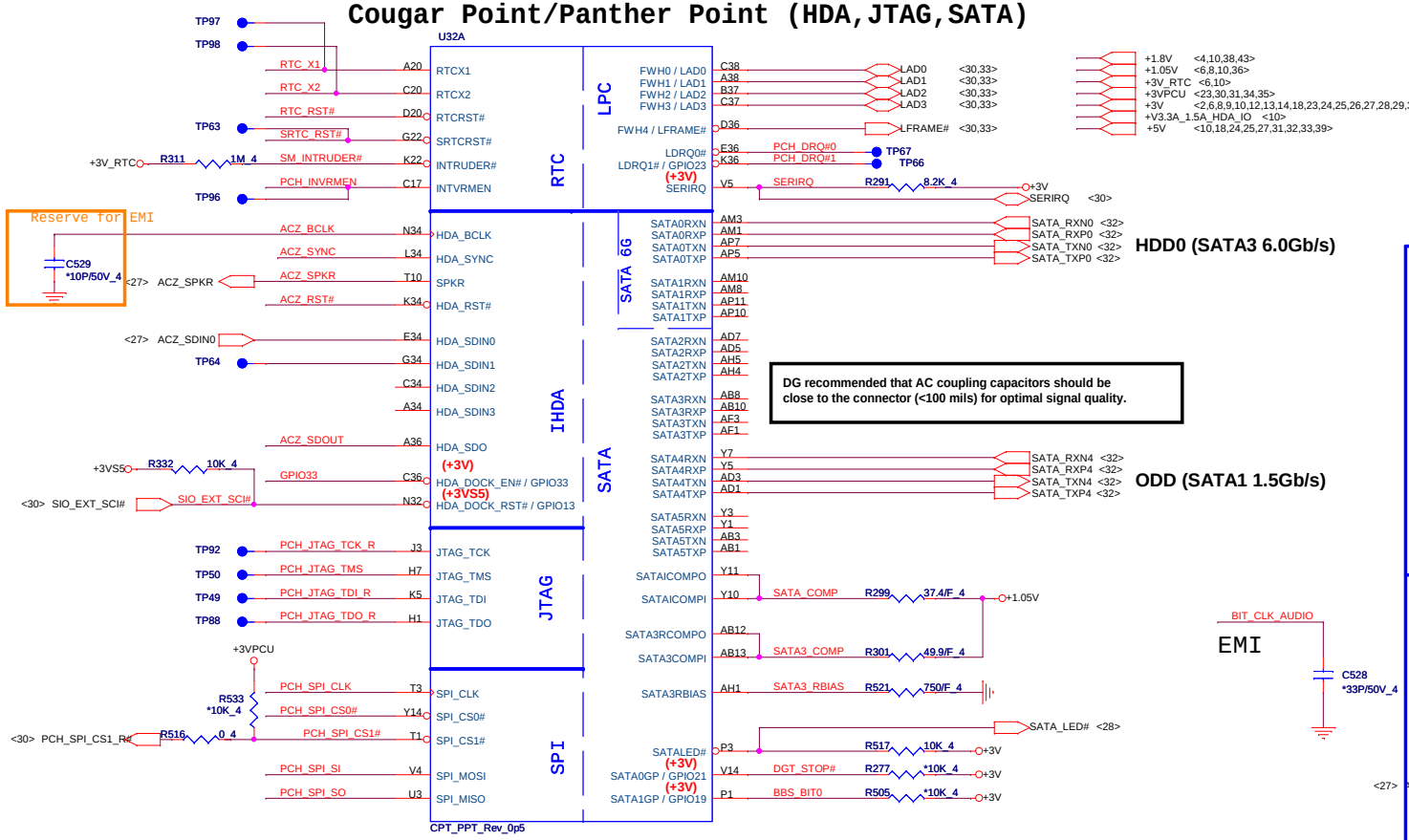
PROJECT : R33
Quanta Computer Inc.

NB5

Size: Custom | Document Number: PCH 1/6 (DMI/FDI/VIDEO) | Rev: 1A

Date: Wednesday, August 31, 2011 | Sheet 6 of 43

# Cougar Point/Panther Point (HDA,JTAG,SATA)




HDD0 (SATA3 6.0Gb/s)

ODD (SATA1 1.5Gb/s)

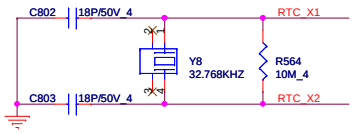
DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

EMI

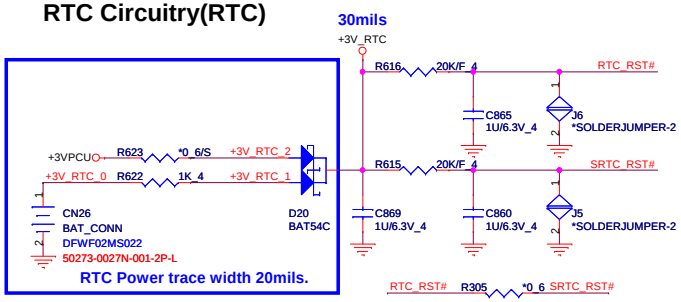
## PCH Strap Table

| Pin Name | Strap description | Sampled | Configuration | Circuit |
|---|---|---|---|---|
| SPKR (Different from Calpella) | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode | ACZ_SPKR R500 *1K_4 +3V |
| GNT3# / GPIO55 | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K) | +3V R584 *1K_4 R595 10K_4 PCI_GNT3# <8> |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up | PCH_INVRMEN R563 330K_4 +3V_RTC |
| HDA_DOCK_EN#/GPIO33 | Flash Descriptor Security Only for Interposer | PWROK | 0 = Override<br>1 = Default (weak pull-up 20K) | GPIO33 R572 0_4 BIOS_WP# |
| GNT1# / GPIO51 | Boot BIOS Selection 1 [bit-1] | PWROK | GNT1# 1 0 / GNT0# 1 0 / Boot Location SPI LPC | [Need external pull-down for LPC BIOS]<br>Default weak pull-up on GNT0/1# |
| GPIO19 (Different from Calpella) | Boot BIOS Selection 0 [bit-0] | PWROK | | R534 *1K_4 BBS_BIT0<br>R585 *1K_4 BBS_BIT1 <8> |
| GNT2# / GPIO53 | ESI strap (Server only) | PWROK | Should not be pull-down (weak pull-up 20K) | USE GPIO PIN |
| NV_ALE | Intel Anti-Theft HDD protection Only for Interposer | PWROK | 0 = Disable (Internal pull-down 20kohm) | +1.8V R547 *1K_4 NV_ALE <8> |
| NV_CLE | DMI Termination voltage | PWROK | weak pull-down 20kohm | +1.8V R526 2.2K_4 R546 1K_4 NV_CLE <9> H_SNB_IVB# <2> sandy/Ivy bridge |
| HDA_SYNC | On-Die PLL VR Voltage Select | RSMRST | 0 = Support by 1.8V (weak pull-down)<br>1 = Support by 1.5V | +3VS5 R334 1K_4 ACZ_SYNC |
| HDA_SDO | Flash Descriptor Security | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Overridden | GPIO33_E ACZ_SDOUT R573 *1K_4 +V3.3A_1.5A_HDA_IO |
| GPIO8 | Integrated Clock Chip Enable | RSMRST# | Should be pull-down (weak pull-up 20K) | |
| GPIO28 (Different from Calpella) | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable<br>1 = Enable (Default) | R492 *1K_4 PLL_ODVR_EN <9> |
| SPI_MOSI | iTPM function Disable | APWROK | 0 = Default (weak pull-down 20K)<br>1 = Enable | PCH_SPI_SI R292 1K_4 +3V |

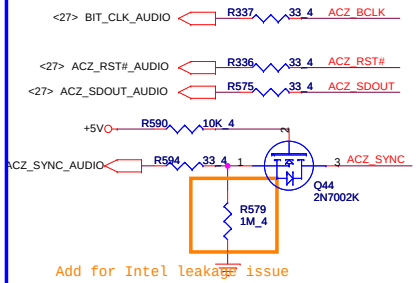
## RTC Clock 32.768KHz



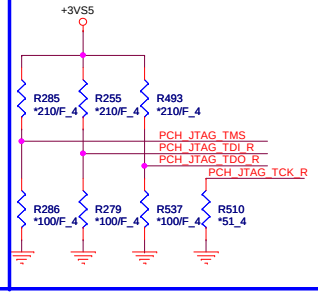

## RTC Circuitry(RTC)



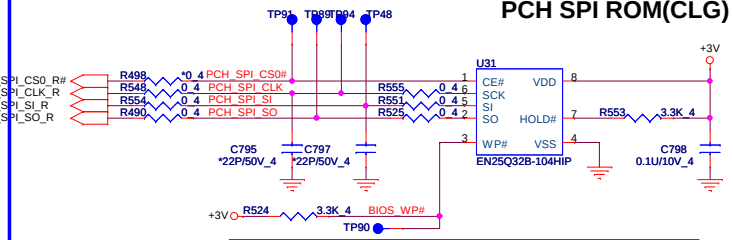

## HDA Bus(CLG)




## PCH JTAG Debug(CLG)




## PCH SPI ROM(CLG)




| Vender | Size | P/N |
|---|---|---|
| EON | 4MB | AKE39ZN0Q02 (EN25Q32B-104HIP) |
| Max | 4MB | AKE39FP0Z02 (MX25L3206EM2I-12G) |
| Socket | | DFHS08FS023 |

NB5

**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 2/6 (SATA/HDA/SPI) | 1A |

Date: Wednesday, August 31, 2011 | Sheet 7 of 43

07

# Cougar Point/Panther Point (PCI,USB,NVRAM)

# Cougar Point/Panther Point(PCI-E,SMBUS,CLK)

08

## PCI/USBOC# Pull-up(CLG)

## USB3.0

## EMI

change 25M to small size

## RF

## PLTRST#(CLG)

## SMBus/Pull-up(CLG)

## CLK_REQ/Strap Pin(CLG)

## PCIE Clock

## SMBus/Pull-up(CLG)

**MPC Switch Control**

| MPC_PWR_CTRL# | Low = MPC ON<br>High = MPC OFF (Default) |
|---|---|

Remove Ra, Rb for UMA &
SG. 27MHz support DIS only.

Remove for UMA only.

CLOCK TERMINATION for FCIM

SG : Rb ; UMA : Ra

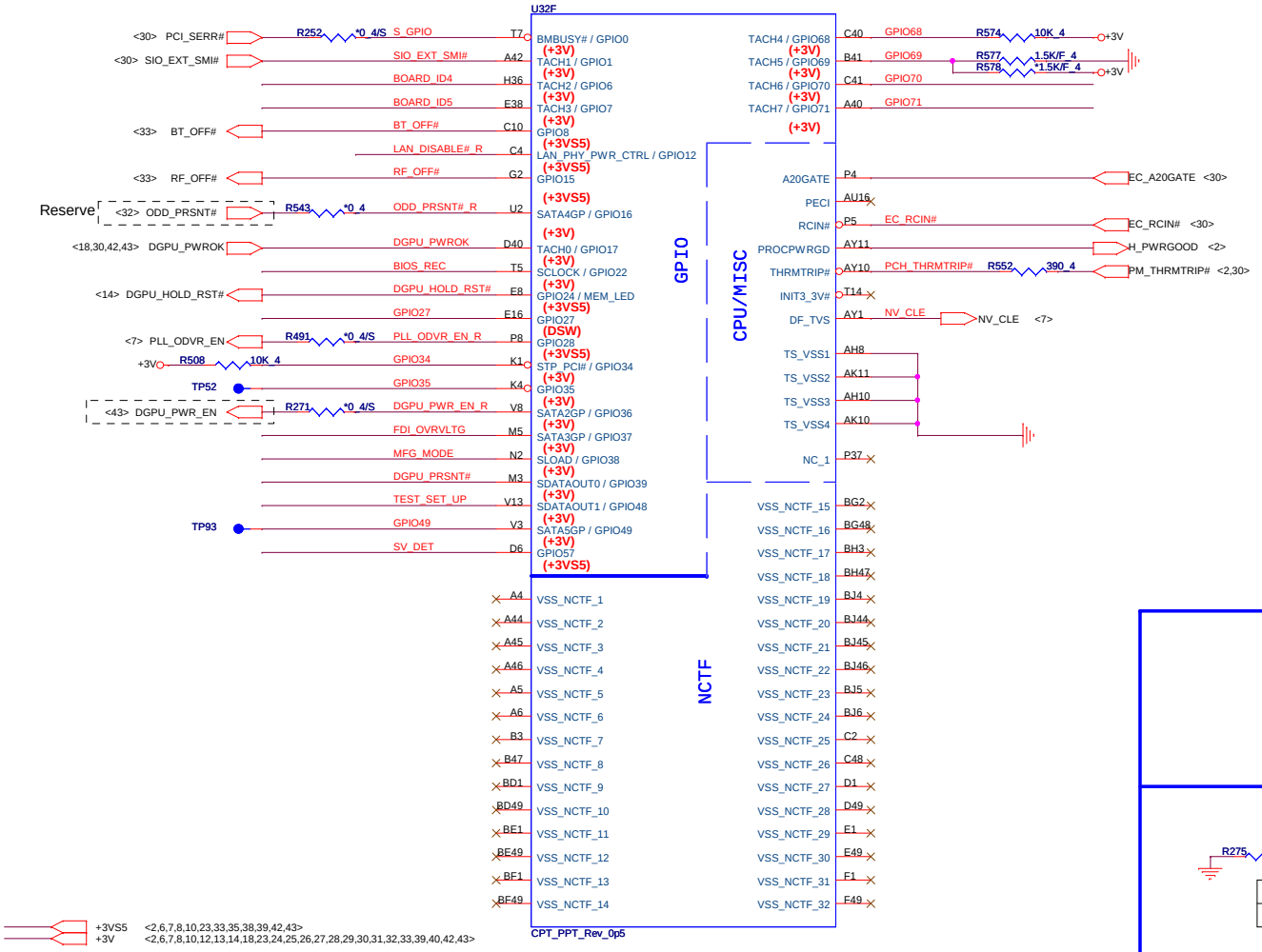
**PROJECT : R33**
**Quanta Computer Inc.**

NB5

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 3/6 (PCIE/USB/CLK) | 1A |

Date: Wednesday, August 31, 2011 | Sheet 8 of 43

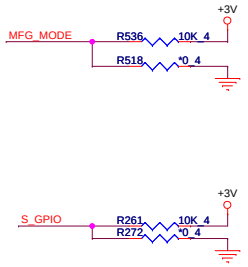
# Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



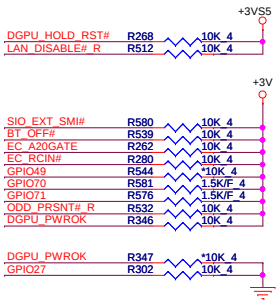

# Clock Gen Power OK (CLG)

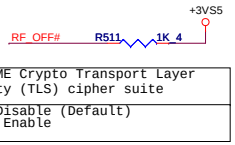
# 09

## MFG-TEST

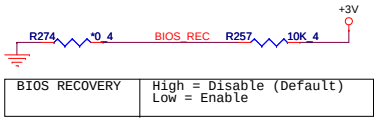



## GPIO Pull-up/Pull-down(CLG)

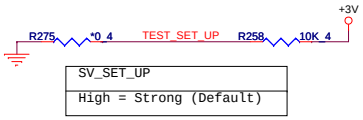


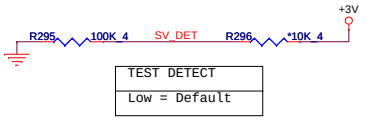

| Intel ME Crypto Transport Layer Security (TLS) cipher suite |
|---|
| Low = Disable (Default)<br>High = Enable |




| BIOS RECOVERY | High = Disable (Default)<br>Low = Enable |
|---|---|

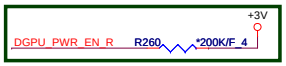



| SV_SET_UP |
|---|
| High = Strong (Default) |




| TEST DETECT |
|---|
| Low = Default |

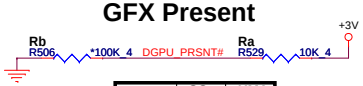
9/3 SI for H/W.




| DMI TERMINATION VOLTAGE OVERRIDE | Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT) |
|---|---|


| FDI TERMINATION VOLTAGE OVERRIDE | LOW - Tx, Rx terminated to same voltage |
|---|---|

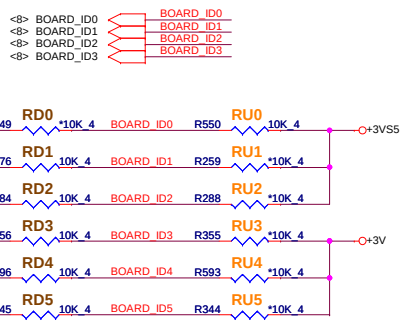
## GFX Present




| | SG | UMA |
|---|---|---|
| Stuff | Ra | Rb |
| NC | Rb | Ra |

## BOARD ID SETTING

| Model | BOARD_ID5 | BOARD_ID4 | BOARD_ID3 | BOARD_ID2 | BOARD_ID1 | BOARD_ID0 |
|---|---|---|---|---|---|---|
| R33 UMA | 0 | 0 | 0 | 0 | 0 | 0 |
| R33 DIS | 0 | 0 | 0 | 0 | 0 | 1 |
| | 0 | 0 | 0 | 0 | 1 | 1 |
| | 0 | 0 | 0 | 1 | 1 | 1 |
| | 0 | 0 | 0 | 0 | 0 | 0 |




NB5

**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 4/6 (GPIO/MISC) | 1A |

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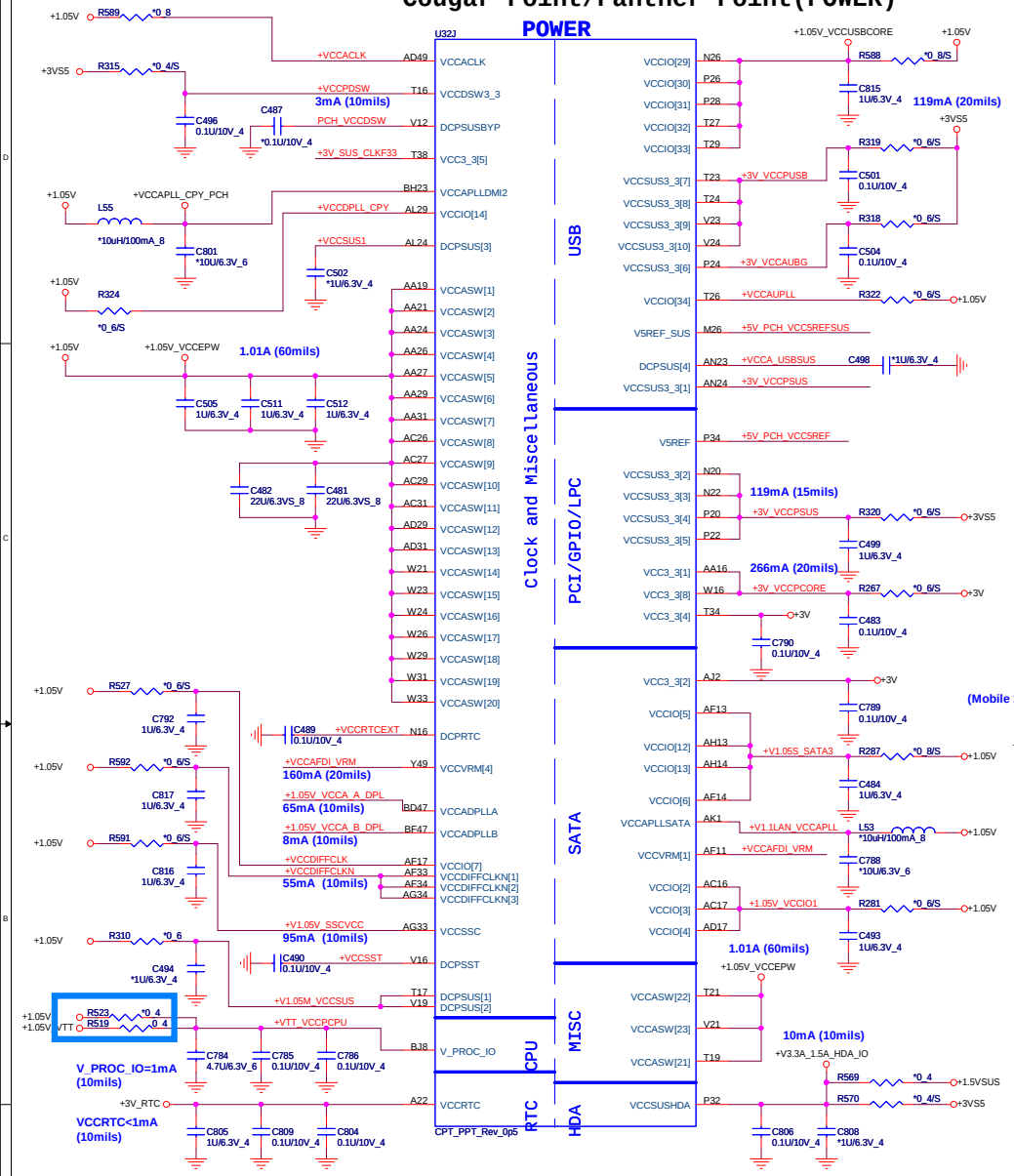
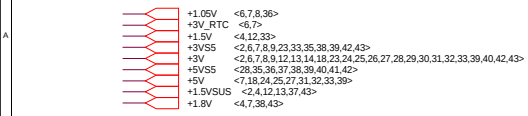
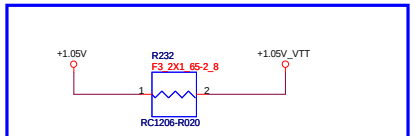
# Cougar Point/Panther Point(POWER)

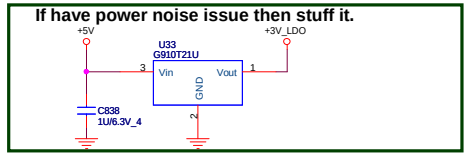



# COUGAR POINT/Panther Point (POWER)



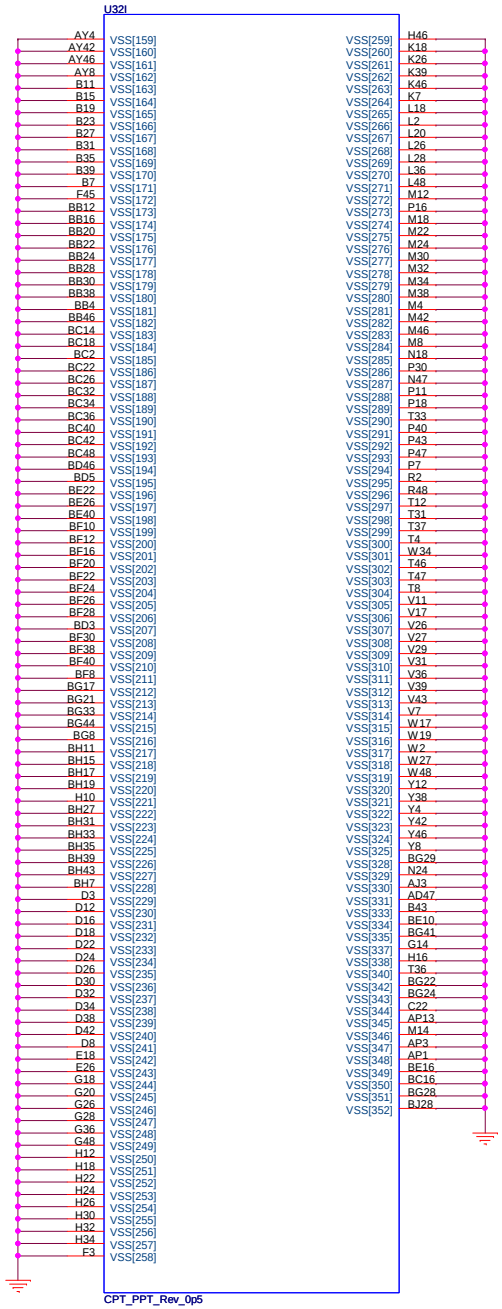



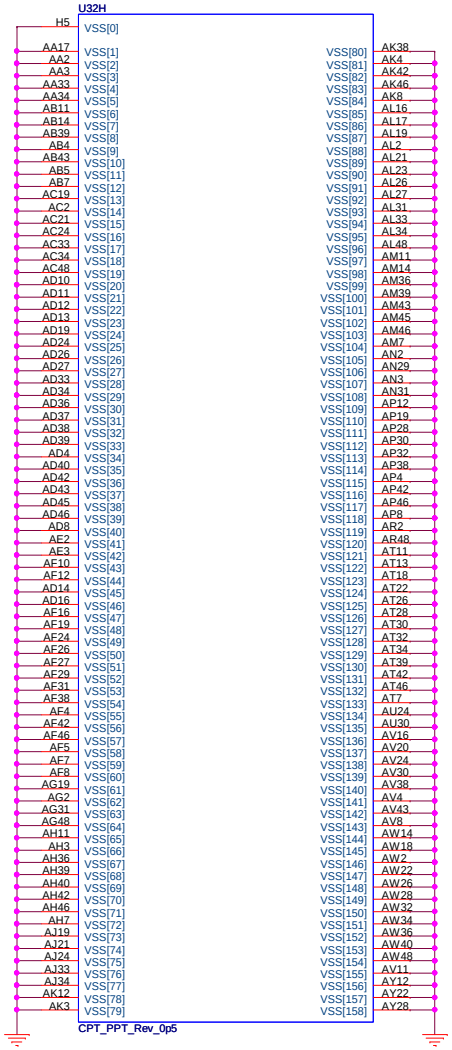

| | |
|---|---|
| PROJECT : R33 | |
| Quanta Computer Inc. | |
| NB5 | |
| Size: Custom | Document Number: PCH 5/6 (POWER) |
| Rev: 1A | |
| Date: Wednesday, August 31, 2011 | Sheet 10 of 43 |

10

# Cougar Point/Panther Point (GND)




# Cougar Point/Panther Point (GND)

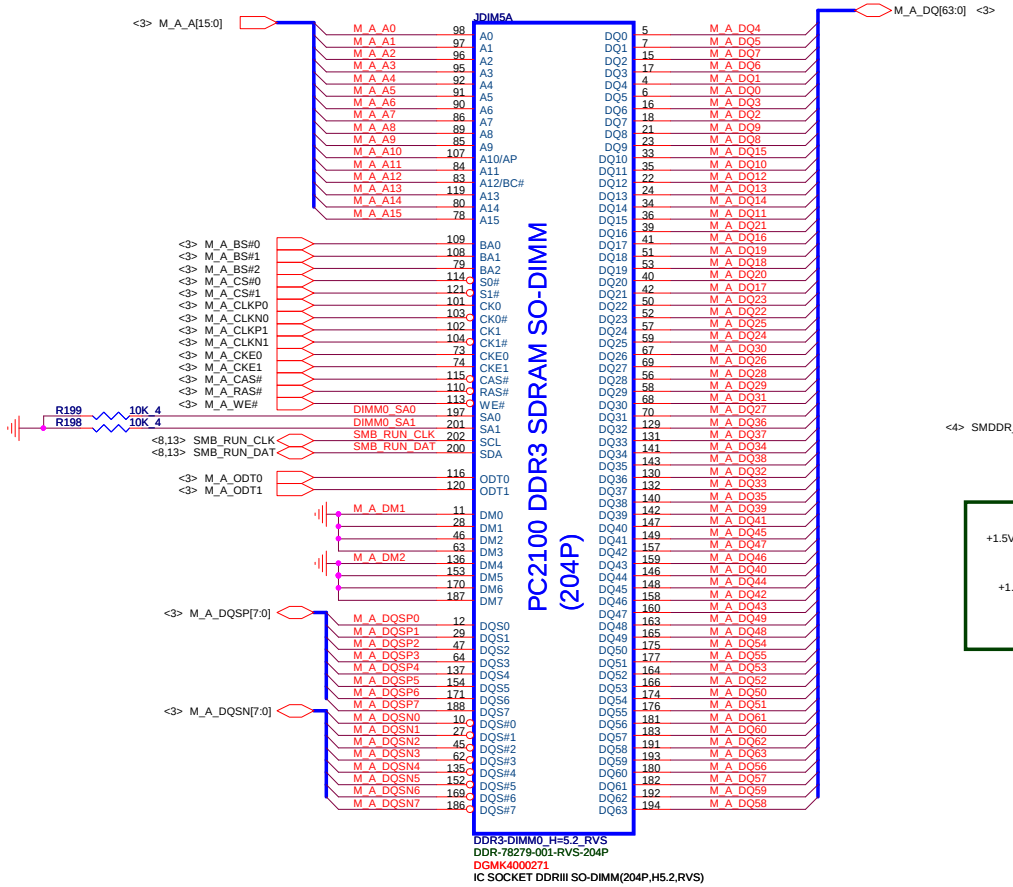


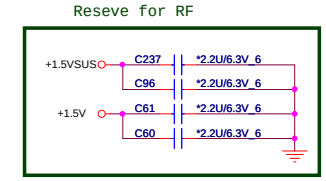

NB5

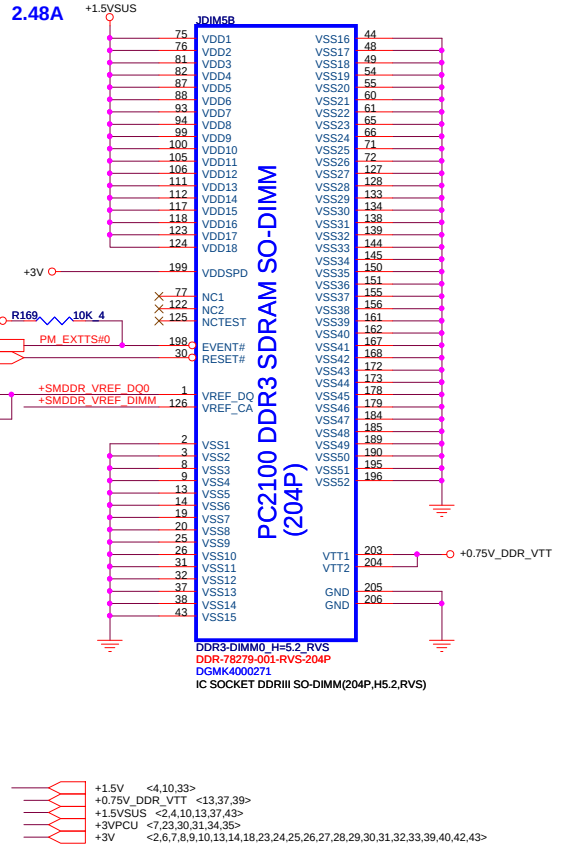
**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 6/6 (GND) | 1A |

Date: Wednesday, August 31, 2011 | Sheet 11 of 43



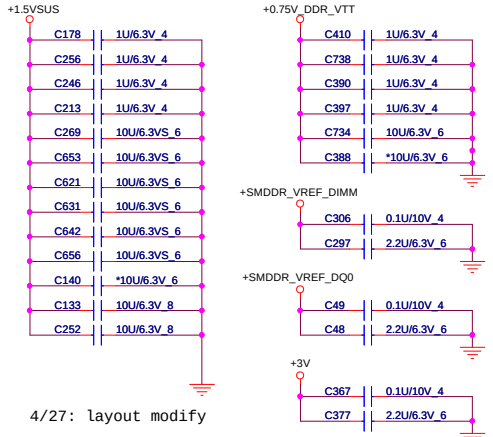



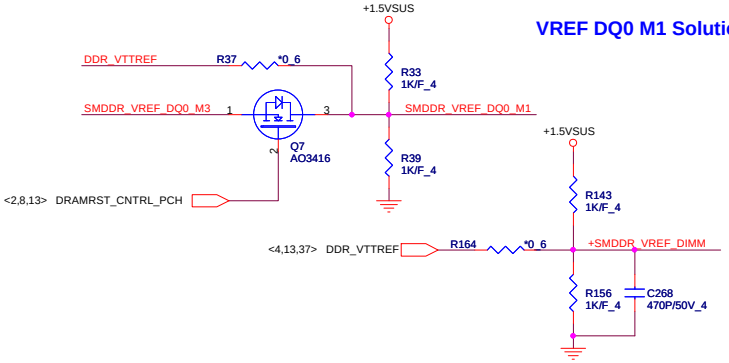

## VREF DQ0 M2 Solution

del M2 solution

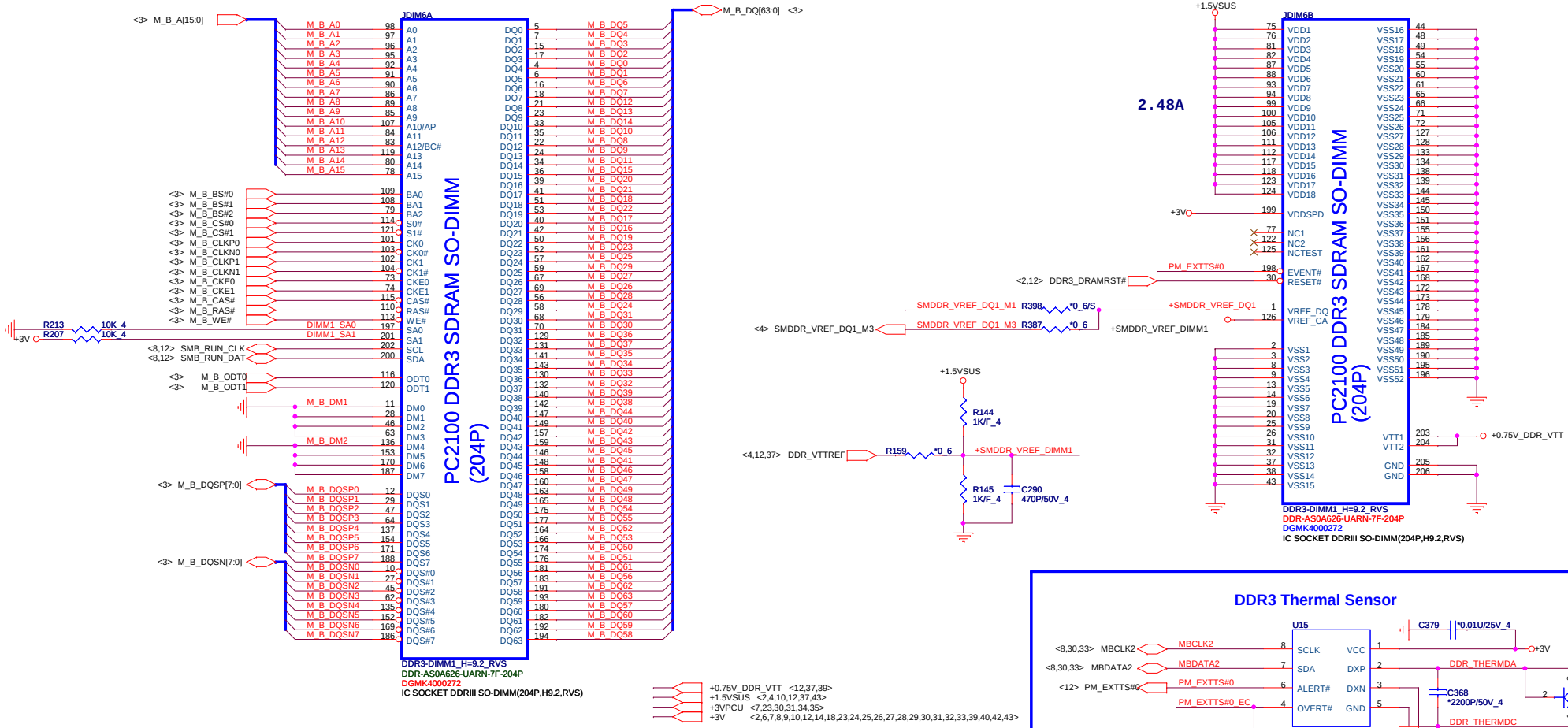
## Place these Caps near So-Dimm0.




## VREF DQ0 M1 Solution



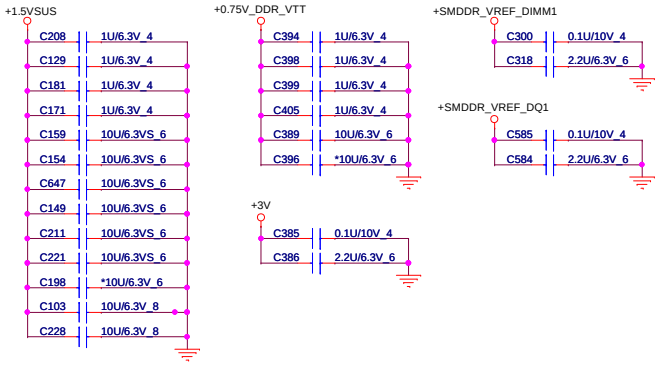
| | | |
|---|---|---|
| NB5 | PROJECT : R33<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: DDR3 DIMM0-RVS (5.2H) | Rev: 1A |
| Date: Wednesday, August 31, 2011 | Sheet 12 of 43 | |



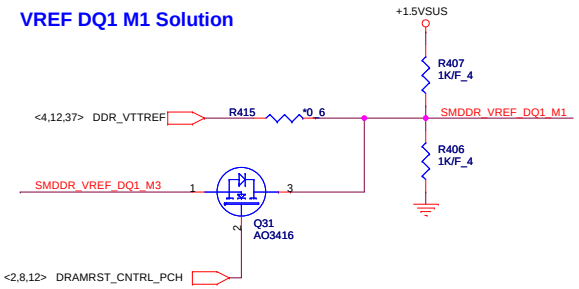

## DDR3 Thermal Sensor




## Place these Caps near So-Dimm1.




## VREF DQ1 M1 Solution

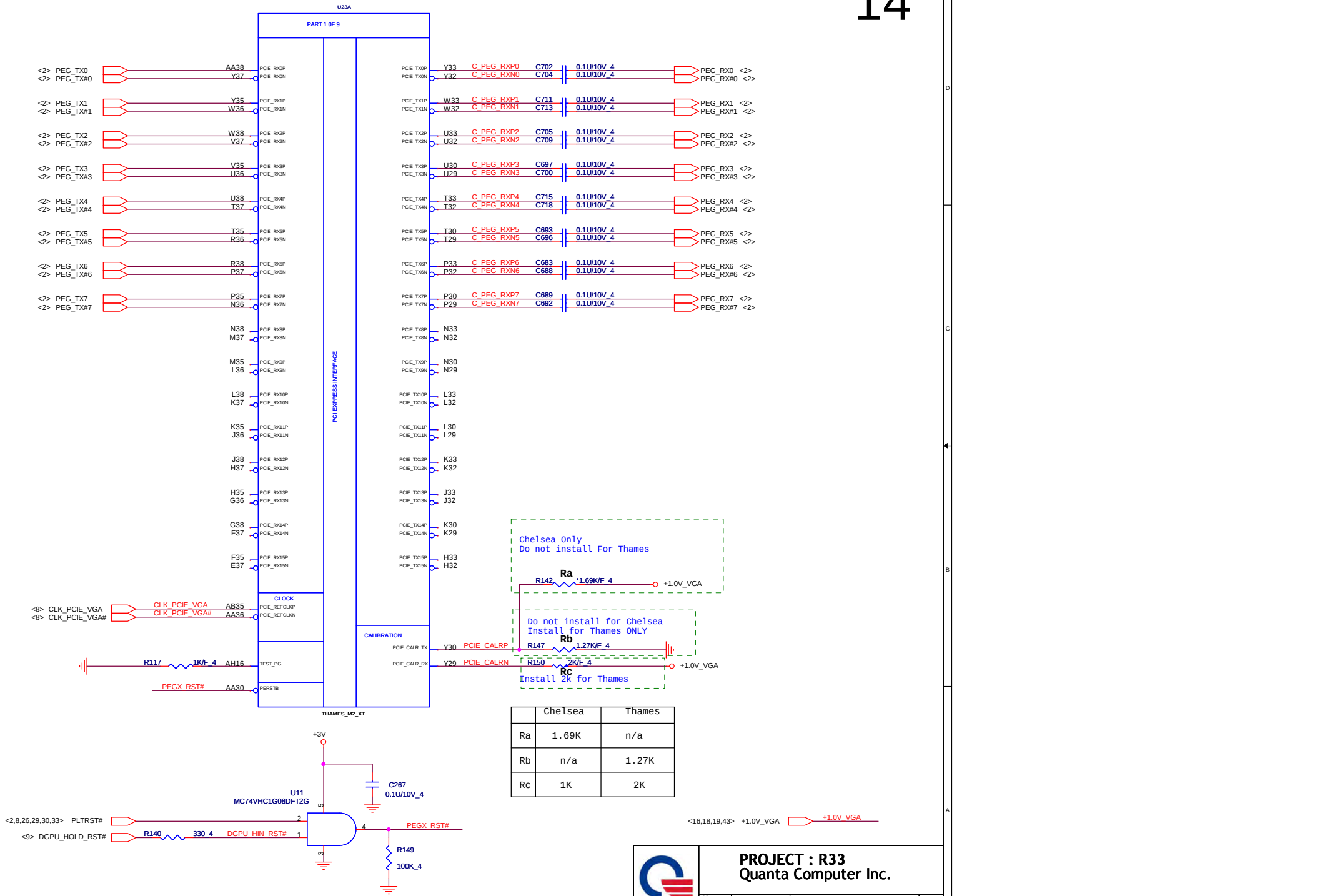



del M2 solution

NB5

**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DDR3 DIMM1-RVS (9.2H) | 1A |
| Date: Wednesday, August 31, 2011 | Sheet 13 of 43 | |




| | Chelsea | Thames |
|---|---|---|
| Ra | 1.69K | n/a |
| Rb | n/a | 1.27K |
| Rc | 1K | 2K |

NB5

**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | THAMES_PCIE_Interface | 1A |

Date: Wednesday, August 31, 2011 Sheet 14 of 43

| MEM_ID[3:0] | Vendor | Type | Vendor P/N |
|---|---|---|---|
| 0000 | Hynix- D (VEGA) | 64Mx16 *8, 900Mhz | H5TQ1663DFR-11C |
| 0001 | Micron- G die | 64Mx16 *8, 900Mhz | MT41J64M16JT-107G:G |
| 0010 | Samsung- G die | 64Mx16 *8, 900Mhz | K4W1G1646G-BC11 |
| 0011 | Hynix- B (VEGA) | 128Mx16 *8, 900Mhz | H5TQ2663BFR-11C |
| 0100 | Micron- D die | 128Mx16 *8, 900Mhz | MT41J128M16HA-107G:D |
| 0101 | Samsung- C die | 128Mx16 *8, 900Mhz | K4W2G1646C-HC11 |
| 0110 | Hynix- B (VEGA) | 128Mx16 *4, 900Mhz | H5TQ2663BFR-11C |
| 0111 | Micron- D die | 128Mx16 *4, 900Mhz | MT41J128M16HA-107G:D |
| 1000 | Samsung- C die | 128Mx16 *4, 900Mhz | K4W2G1646C-HC11 |
| 1001 | | | |
| 1010 | | | |
| 1011 | | | |
| 1100 | | | |
| 1101 | | | |
| 1110 | | | |
| 1111 | | | |

GPIO16 GPIO20 GPIO15

| Thames XT | PWRCNTL2 | PWRCNTL1 | PWRCNTL0 | V-CORE |
|---|---|---|---|---|
| L | 0 | 0 | 0 | 1.0V |
| M | 0 | 0 | 1 | 0.9V |
| H | 0 | 1 | 0 | 0.875V |
| | 0 | 1 | 1 | 0.85V |
| | 1 | 0 | 0 | 0.8V |
| | 1 | 0 | 1 | 0.75V |

Memory ID

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

A 3-k external pull up (3.3 V) is required if an external BIOS ROM chip is used.

Thames INSTALL, do not install for Chelsea
PS_0 should be tied to GND on Thames

PS_1,PS_2, PS_3 are NC on Thames
Do not install for Thames

Reserve for Power Play

1.8V(8mA TSVDD)

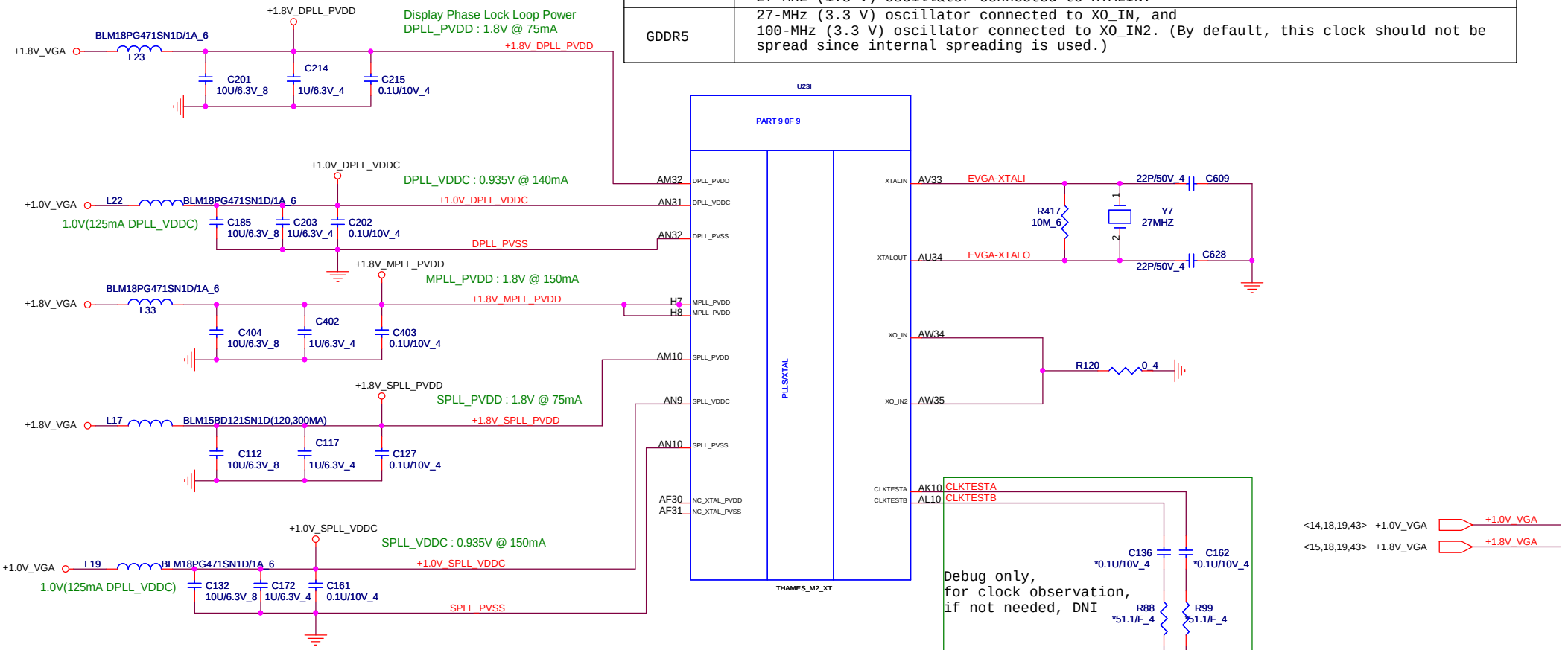
PROJECT : R33
Quanta Computer Inc.

NB5

Size: Custom | Document Number: THAMES_Main & GND | Rev: 1A

Date: Wednesday, August 31, 2011 | Sheet 15 of 43

| Memory Type | |
|---|---|
| DDR3 | 27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or<br>27-MHz (1.8 V) oscillator connected to XTALIN. |
| GDDR5 | 27-MHz (3.3 V) oscillator connected to XO_IN, and<br>100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.) |

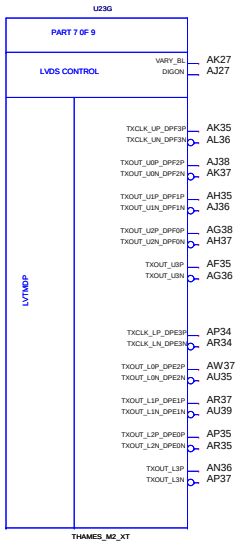


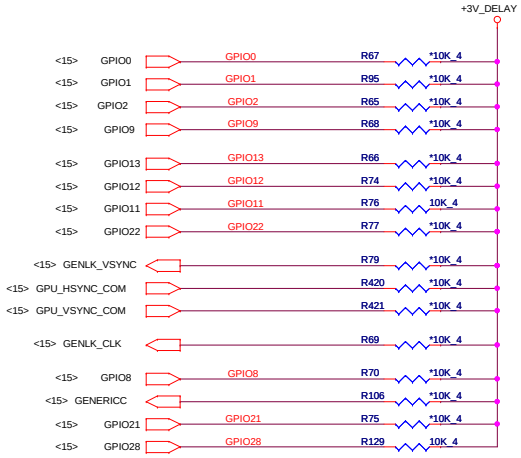

NB5

**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | THAMES_XTAL | 1A |

Date: Wednesday, August 31, 2011 Sheet 16 of 43



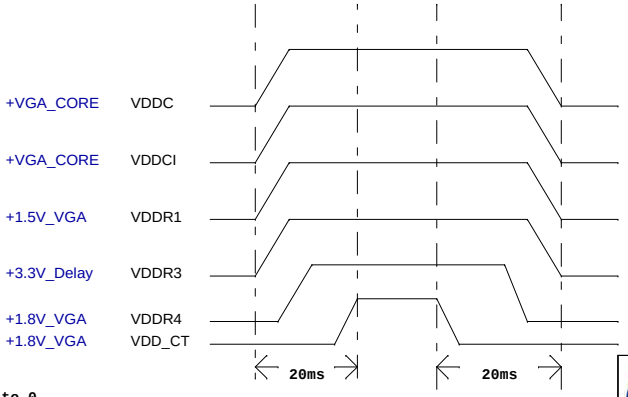

| CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS<br>ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,<br>THEY MUST NOT CONFLICT DURING RESET | | | | |
|---|---|---|---|---|
| STRAPS | MLPS | GPIO PIN | DESCRIPTION OF DEFAULT SETTINGS | Default Setting |
| MLPS_DISABLE | NA | GPIO_28_FDO | Enable MLPS, NA for Thames/Whistler/Seymour<br>0: Enable MLPS, disable GPIO PINSTRAP<br>1: Disable MLPS, enable GPIO PINSTRAP | X |
| TX_PWRS_ENB | PS_1[4] | GPIO0 | Transmitter Power Savings Enable<br>0: 50% Tx output swing<br>1: Full Tx output swing | X |
| TX_DEEMPH_EN | PS_1[5] | GPIO1 | PCIE Transmitter De-emphasis Enable<br>0: Tx de-emphasis disabled<br>1: Tx de-emphasis enabled | X |
| BIF_GEN3_EN_A | PS_1[1] | GPIO2 | PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour)<br>0: GEN3 not supported at power-on<br>1: GEN3 supported at power-on | 1 |
| BIF_VGA DIS | PS_2[4] | GPIO9 | VGA Control<br>0: VGA controller capacity enabled<br>1: VGA controller capacity disabled (for multi-GPU) | 0 |
| ROMIDCFG[2:0] | PS_0[3..1] | GPIO[13:11] | Serial ROM type or Memory Aperture Size Select<br><br>If GPIO22 = 0, defines memory aperture size<br>If GPIO22 = 1, defines ROM type<br>100 - 512Kbit M25P05A (ST)<br>101 - 1Mbit M25P10A (ST)<br>101 - 2Mbit M25P20 (ST)<br>101 - 4Mbit M25P40 (ST)<br>101 - 8Mbit M25P80 (ST)<br>100 - 512Kbit Pm25LV512 (Chingis)<br>101 - 1Mbit Pm25LV010 (Chingis) | XXX |
| BIOS_ROM_EN | PS_2[3] | GPIO22 | Enable external BIOS ROM device<br>0: Disabled<br>1: Enabled | X |
| AUD[1]<br>AUD[0] | NA<br>NA | HSYNC<br>VSYNC | 00 - No audio function<br>01 - Audio for DP only<br>10 - Audio for DP and HDMI if dongle is detected<br>11 - Audio for both DP and HDMI<br>HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature. | XX |
| CEC_DIS | PS_0[4] | GENLK_VSYNC | Enable CEC function. Reserved for Thames/Whistler/Seymour<br>0: Disabled<br>1: Enabled | X |
| | | | NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR<br>IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET | |
| RESERVED<br>RESERVED<br>RESERVED<br>RESERVED | PS_1[3]<br>PS_1[2]<br>NA<br>NA | GENLK_CLK<br>GPIO8<br>GPIO21<br>GENERICC | Reserved<br>Reserved<br>Reserved<br>Reserved (for Thames/Whistler/Seymour only) | 0<br>0<br>0<br>0 |
| AUD_PORT_CONN_PINSTRAP[2]<br>AUD_PORT_CONN_PINSTRAP[1]<br>AUD_PORT_CONN_PINSTRAP[0] | PS_3[5]<br>PS_3[4]<br>PS_0[5] | NA<br>NA<br>NA | STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS<br>111 = 0 usable endpoints<br>110 = 1 usable endpoints<br>101 = 2 usable endpoints<br>100 = 3 usable endpoints<br>011 = 4 usable endpoints<br>010 = 5 usable endpoints<br>001 = 6 usable endpoints<br>000 = all endpoints are usable | XXX |

## Memory Aperture size

| GPIO9 BIOSROM | | GPIO13 ROMIDCFG2 | GPIO12 ROMIDCFG1 | GPIO11 ROMIDCFG0 |
|---|---|---|---|---|
| 0 | 128M | 0 | 0 | 0 |
| 0 | 256M | 0 | 0 | 1 |
| 0 | 64M | 0 | 1 | 0 |
| 0 | 32M | 0 | 1 | 1 |
| 0 | 512M | 1 | 0 | 0 |
| 0 | 1G | 1 | 0 | 1 |
| 0 | 2G | 1 | 1 | 0 |
| 0 | 4G | 1 | 1 | 1 |

**It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.**

## Power Up/Down Sequence

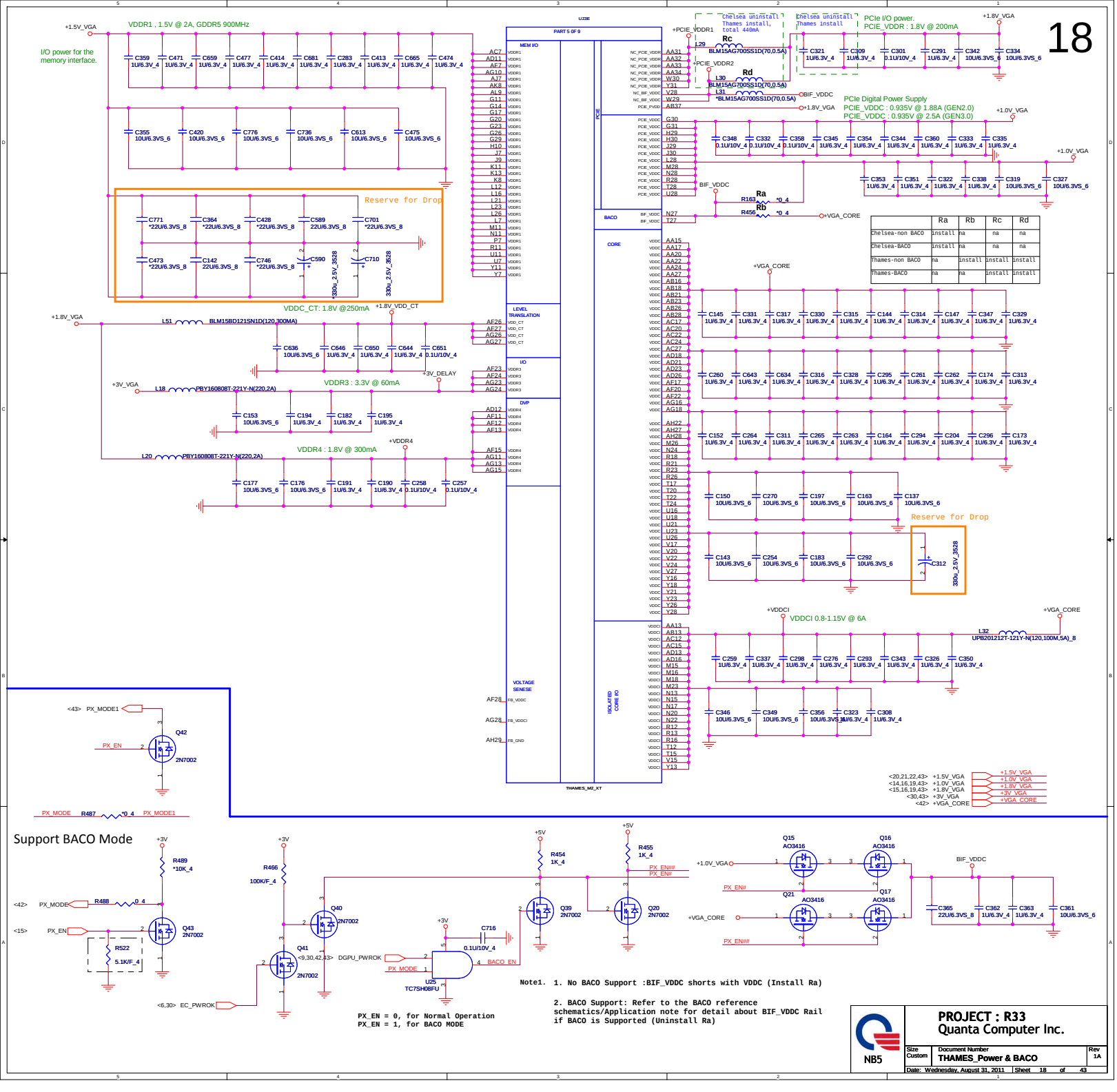



NB5

**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | THAMES_LVDS / STRAP | 1A |

Date: Wednesday, August 31, 2011 Sheet 17 of 43

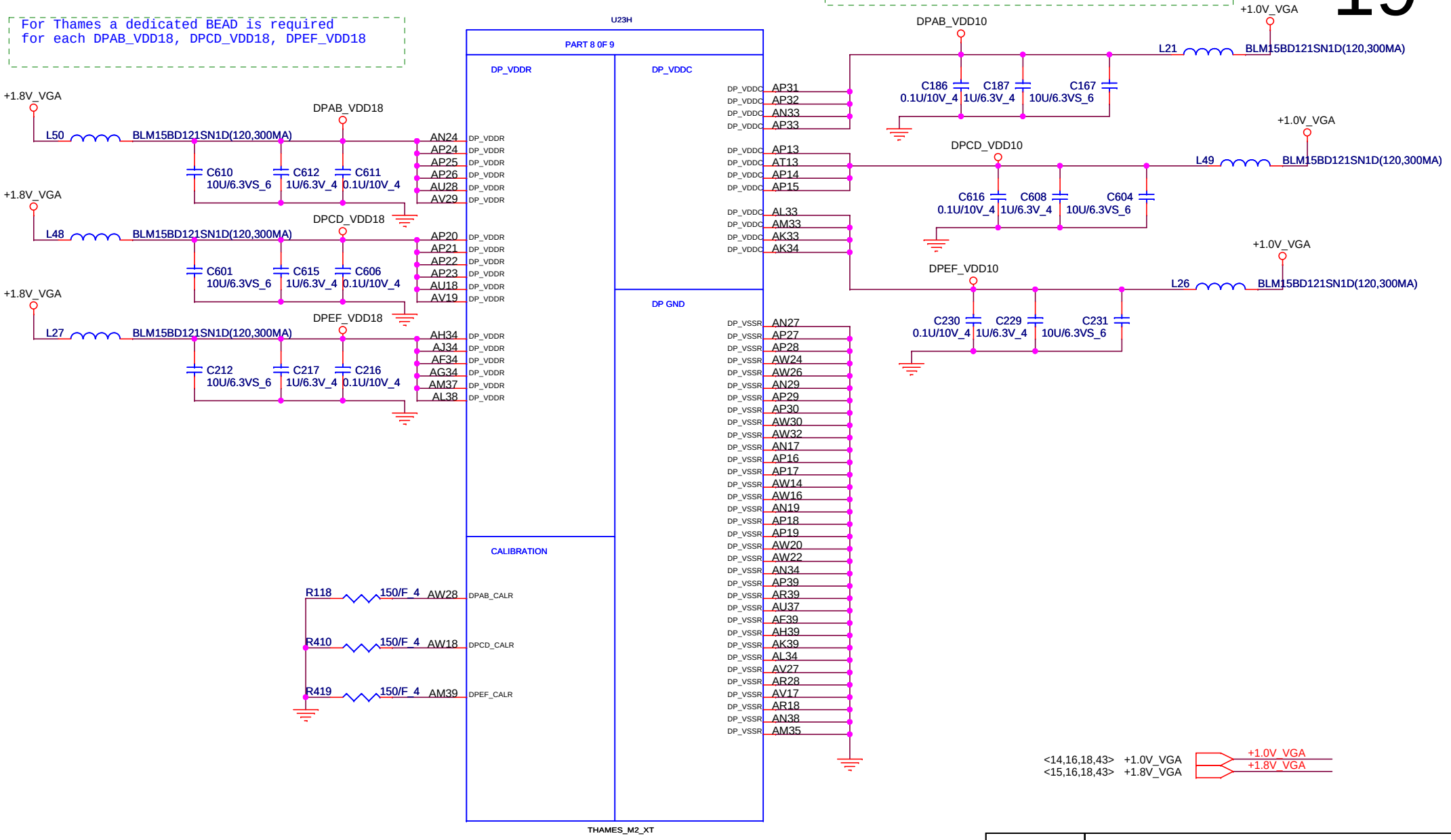



| | Ra | Rb | Rc | Rd |
|---|---|---|---|---|
| Chelsea-non BACO | install | na | na | na |
| Chelsea-BACO | install | na | na | na |
| Thames-non BACO | na | install | install | install |
| Thames-BACO | na | na | install | install |

PROJECT : R33
Quanta Computer Inc.
NB5
Size: Custom | Document Number: THAMES_Power & BACO | Rev: 1A
Date: Wednesday, August 31, 2011 | Sheet 18 of 43

For Thames a dedicated BEAD is required
for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

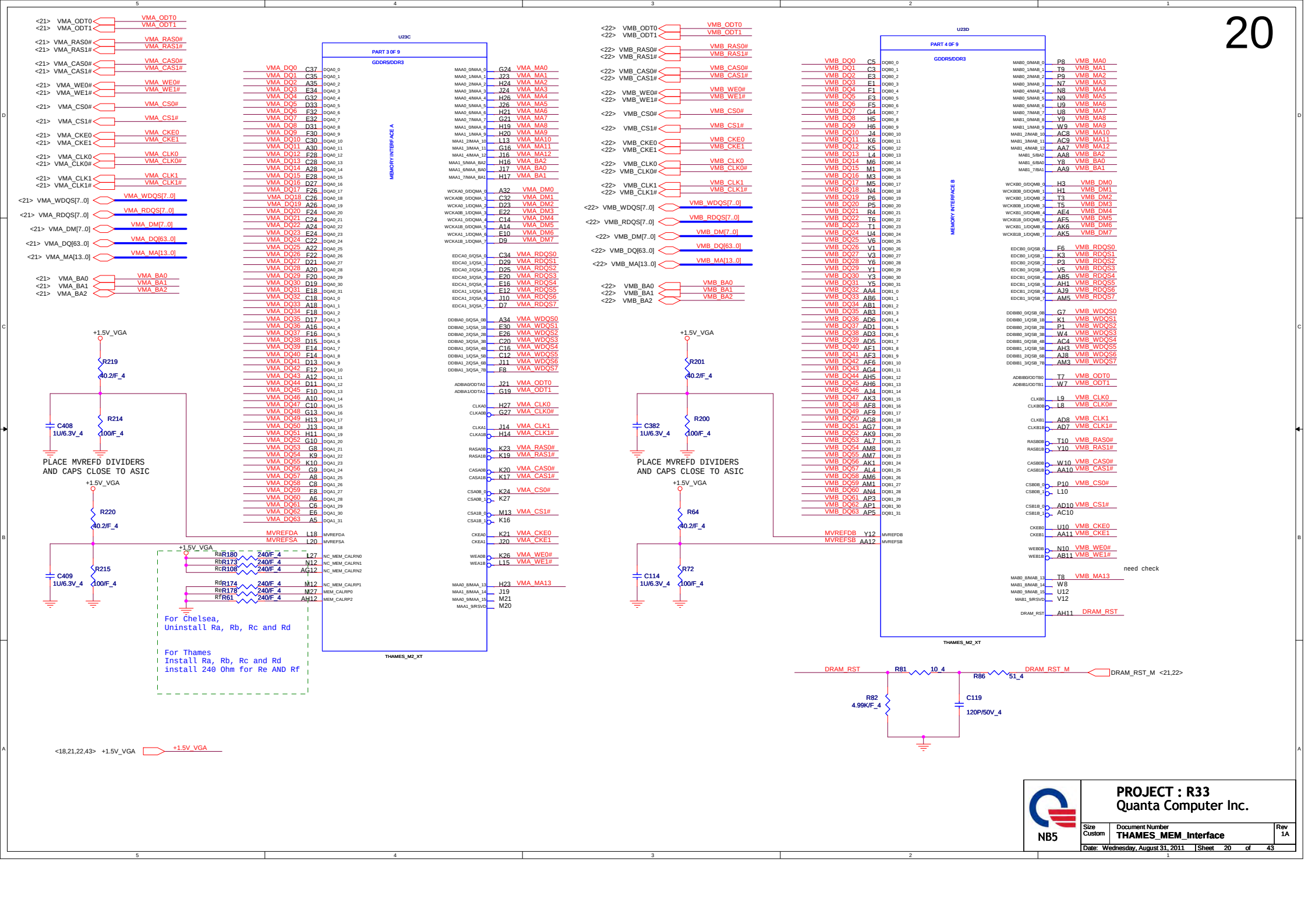
For Thames a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10




NB5

**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | **THAMES_DP Powers** | 1A |
| Date: Wednesday, August 31, 2011 | Sheet 19 of 43 | |




| | |
|---|---|
| NB5 | PROJECT : R33<br>Quanta Computer Inc. |
| Size: Custom | Document Number: THAMES_MEM_Interface |
| Rev: 1A | |
| Date: Wednesday, August 31, 2011 | Sheet 20 of 43 |

# CHANNEL A: 256MB/512MB DDR3



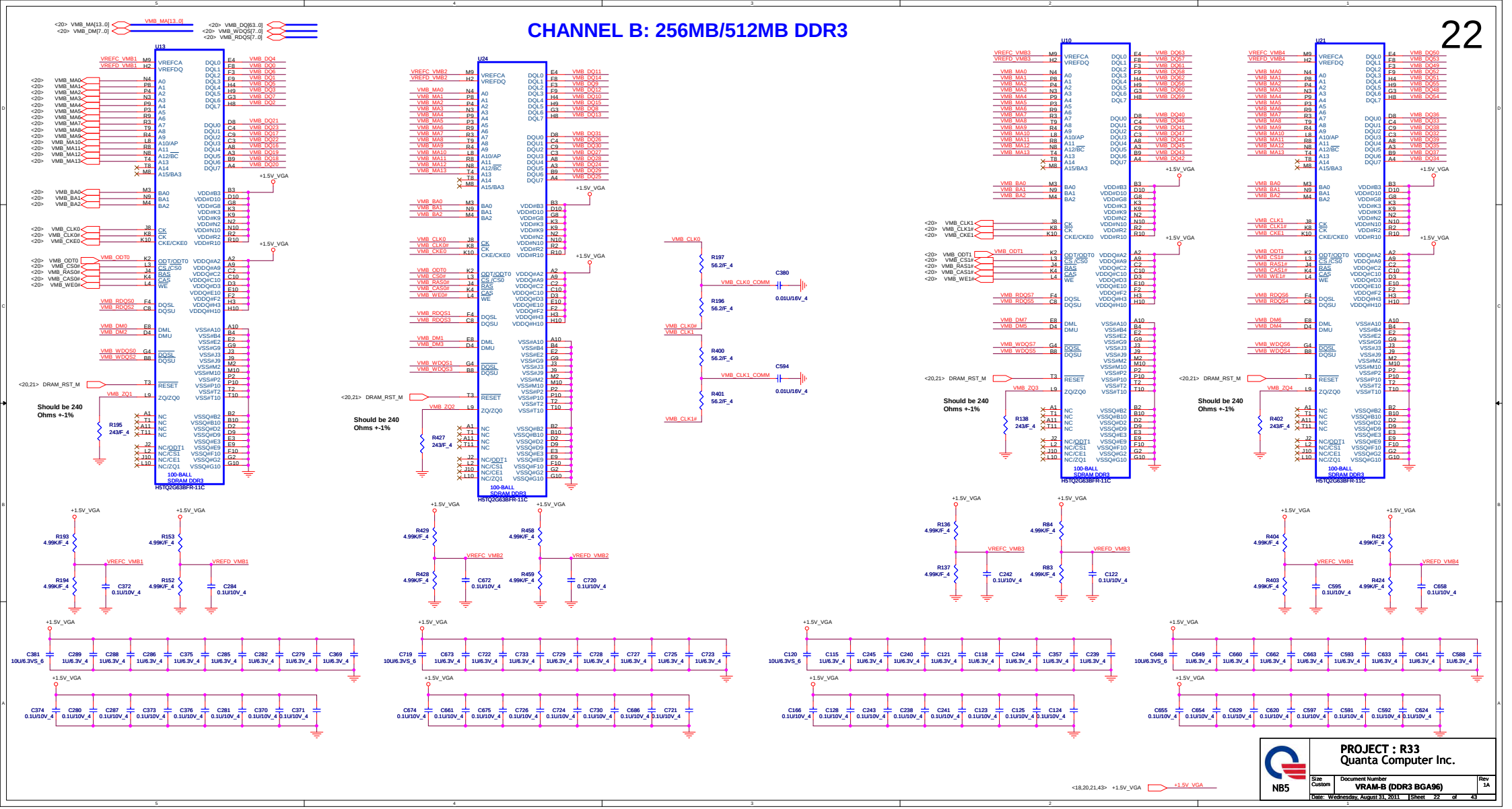
| Vendor | QCI PN | B/S PN |
|---|---|---|
| Hynix D(Vega) | AKD5LZWTW02 | AKD5LZWTW08 |
| Micron G die | AKD5EGSTL00 | AKD5LZSTL10 |
| SAMSUNG G die | AKD5EGGT500 | AKD5EGGT502 |
| Hynix B(Vega) | AKD5MGWTW00 | AKD5MGWTW07 |
| SAMSUNG C die | AKD5MGWT500 | AKD5MGWT508 |

Should be 240 Ohms +-1%

100-BALL SDRAM DDR3 H5TQ2G63BFR-11C

# CHANNEL B: 256MB/512MB DDR3



























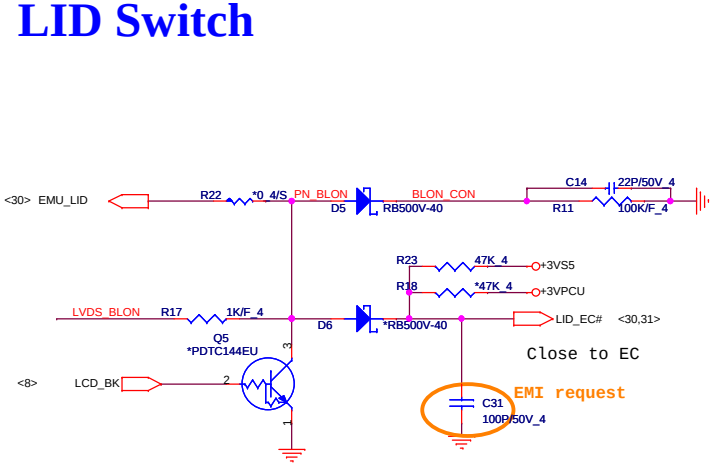


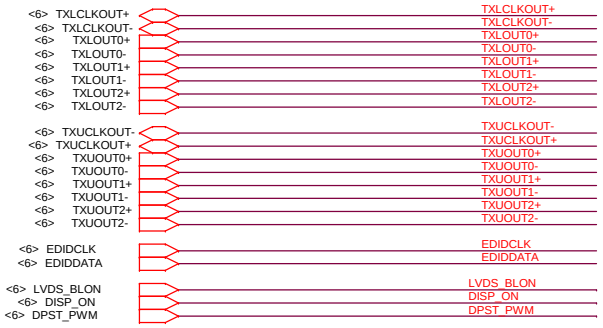


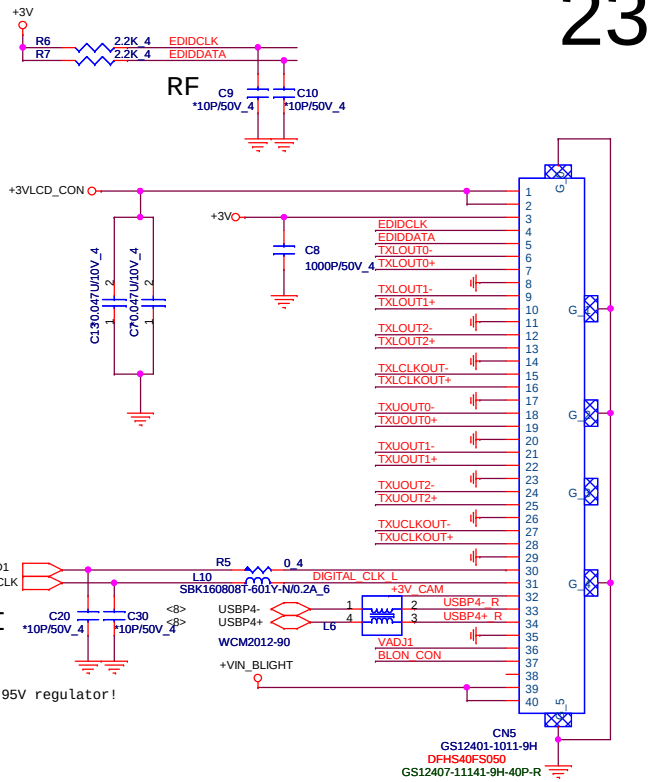

<18,20,21,43> +1.5V_VGA

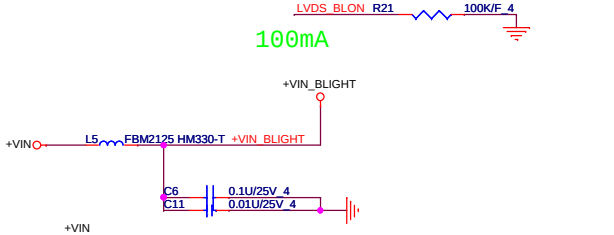
# LID Switch

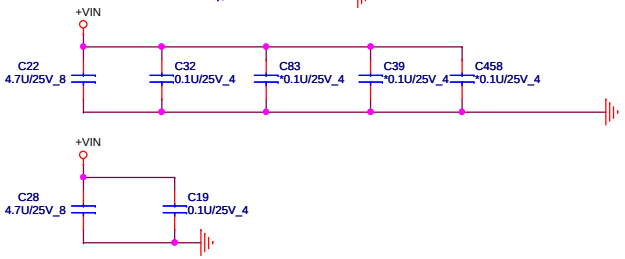


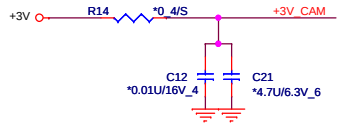






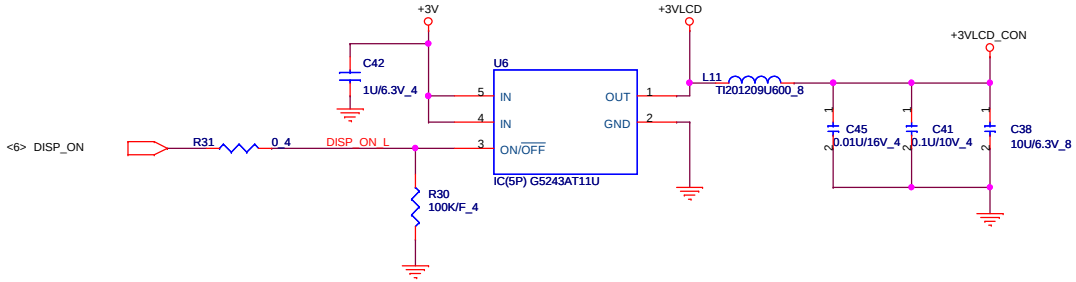
Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

follow L6 location

USBP4- R8 *0_4 USBP4-_R

USBP4+ R9 *0_4 USBP4+_R




<2,6,7,8,9,10,12,13,14,18,24,25,26,27,28,29,30,31,32,33,39,40,42,43> +3V
<7,30,31,34,35> +3VPCU
<7,10,18,24,25,27,31,32,33,39> +5V
<32,34,39,43> +12VALW
<34,35,36,37,38,39,41,42,43> +VIN

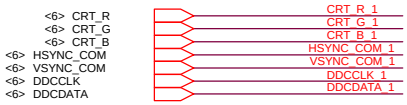
NB5

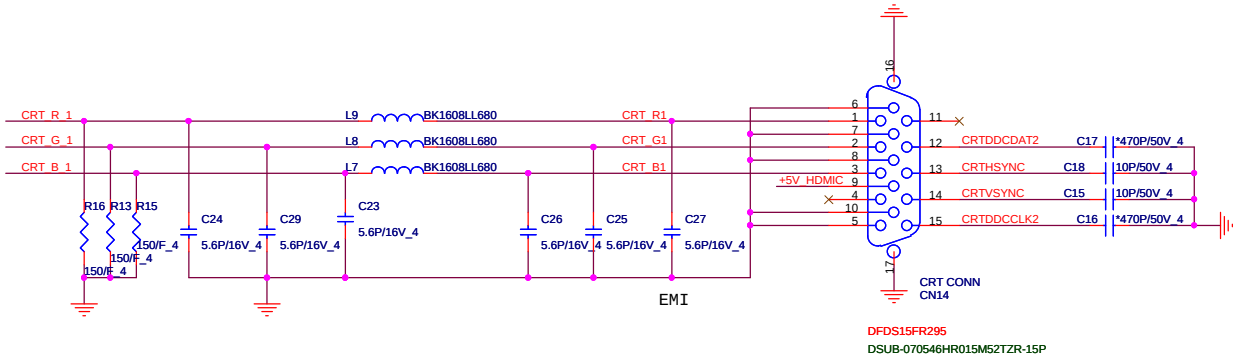
**PROJECT : R33**
Quanta Computer Inc.

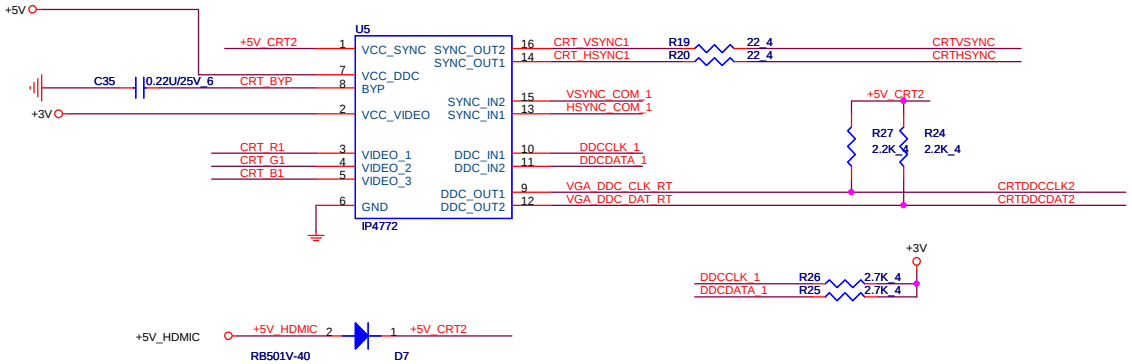
| Size | Document Number | Rev |
|---|---|---|
| Custom | LCD CONN/LID/CAM | 1A |

Date: Wednesday, August 31, 2011 Sheet 23 of 43

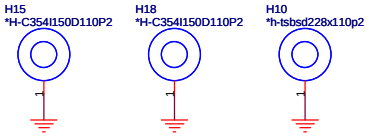
# CRT PORT

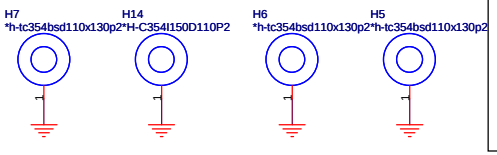


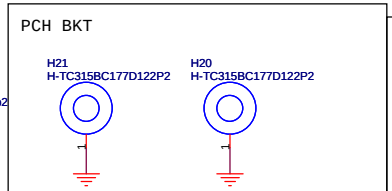



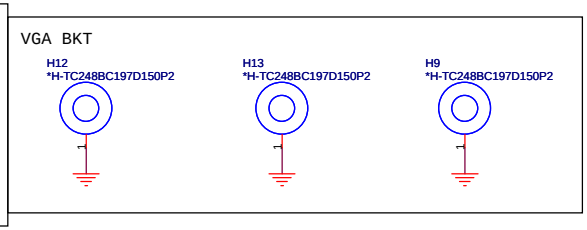



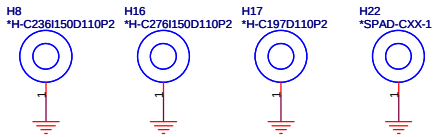

# HOLE

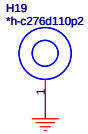


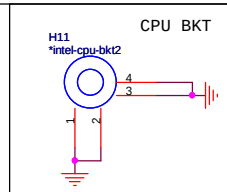




NB5

**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | CRT,Hole | 1A |

Date: Wednesday, August 24, 2011 | Sheet 24 of 43

EMI request

+3V

C586
0.1U/10V_4

EMI request

+5V_HDMIC

C164
0.1U/10V_4

Add for EMI

+5V_HDMIC

C101
220P/50V_4

close to HDMI conn

<6> IN_CLK#
<6> IN_CLK
<6> IN_D0#
<6> IN_D0
<6> IN_D1#
<6> IN_D1
<6> IN_D2#
<6> IN_D2

IN_CLK# C141 0.1U/10V_4 C_TXC_HDMI-
IN_CLK C148 0.1U/10V_4 C_TXC_HDMI+
IN_D0# C180 0.1U/10V_4 C_TX0_HDMI-
IN_D0 C189 0.1U/10V_4 C_TX0_HDMI+
IN_D1# C157 0.1U/10V_4 C_TX1_HDMI-
IN_D1 C169 0.1U/10V_4 C_TX1_HDMI+
IN_D2# C200 0.1U/10V_4 C_TX2_HDMI-
IN_D2 C210 0.1U/10V_4 C_TX2_HDMI+

<6> SDVO_CLK
<6> SDVO_DATA

SDVO_CLK HDMI_SCL_R
SDVO_DATA HDMI_SDA_R

<6> HDMI_HPD_CON

HDMI_HPD_CON HDMI_HPD_3V

DISCRETE HDMI I2C SELECT
Close to HDMI Connector

+3V
R418 2.2K_4
HDMI_SCL_R
HDMI_SCLK
Q36 2N7002
R408 2.2K_4
HDMI_SDA_R
HDMI_SDATA
Q35 2N7002

reserve for Intel DG

+3V
R38 *1M_4
HDMI_HPD_3V
HDMI_HPD
Q9 *2N7002

+5V
R132 *0_4/S
Q13 2N7002K
R139 100K_4
C255 0.1U/10V_4

R127 680_4/F C_TX2_HDMI+
R123 680_4/F C_TX2_HDMI-
R109 680_4/F C_TX1_HDMI+
R105 680_4/F C_TX1_HDMI-
R119 680_4/F C_TX0_HDMI+
R115 680_4/F C_TX0_HDMI-
R102 680_4/F C_TXC_HDMI+
R94 680_4/F C_TXC_HDMI-

+3V
Q6 MMBT3904-7-F
HDMI_DET_R
R32 200K/F_4
HDMI_HPD
HDMI_HPD_3V
R34 10K/F_4
R399 *200K/F_4

EMI request

C_TX2_HDMI+ R126 150/F_4 C_TX2_HDMI-
C_TX1_HDMI+ R107 150/F_4 C_TX1_HDMI-
C_TX0_HDMI+ R116 150/F_4 C_TX0_HDMI-

C_TXC_HDMI+ R98 150/F_4 C_TXC_HDMI-

reserved for EMI

C131 *10P/50V_4
HDMI_SDATA
C135 *10P/50V_4
HDMI_SCLK

C_TX2_HDMI+
C_TX2_HDMI-
C_TX1_HDMI+
C_TX1_HDMI-
C_TX0_HDMI+
C_TX0_HDMI-
C_TXC_HDMI+
C_TXC_HDMI-

CN19
D2+
D2-
D1+
D1-
D0+
D0-
CK+
CK-
SHELL1
SHELL2
SHELL2
SHELL2
D2 Shield
D1 Shield
D0 Shield
CK Shield
GND
DDC CLK CE Remote
DDC DATA
NC
+5V
HP DET
HDMI CONN

HDMI_SCLK
HDMI_SDATA
1A
+5V_HDMIC
FUSE1.1A8V_POLY
F5
HDMI_HPD
HDMI_HPD_L
*0_6/S
L47
C598 220P/50V_4
VC5 *AVLCSS_4
DFHD19MR191
hdmi-2he1608-000111f-19p-ldv

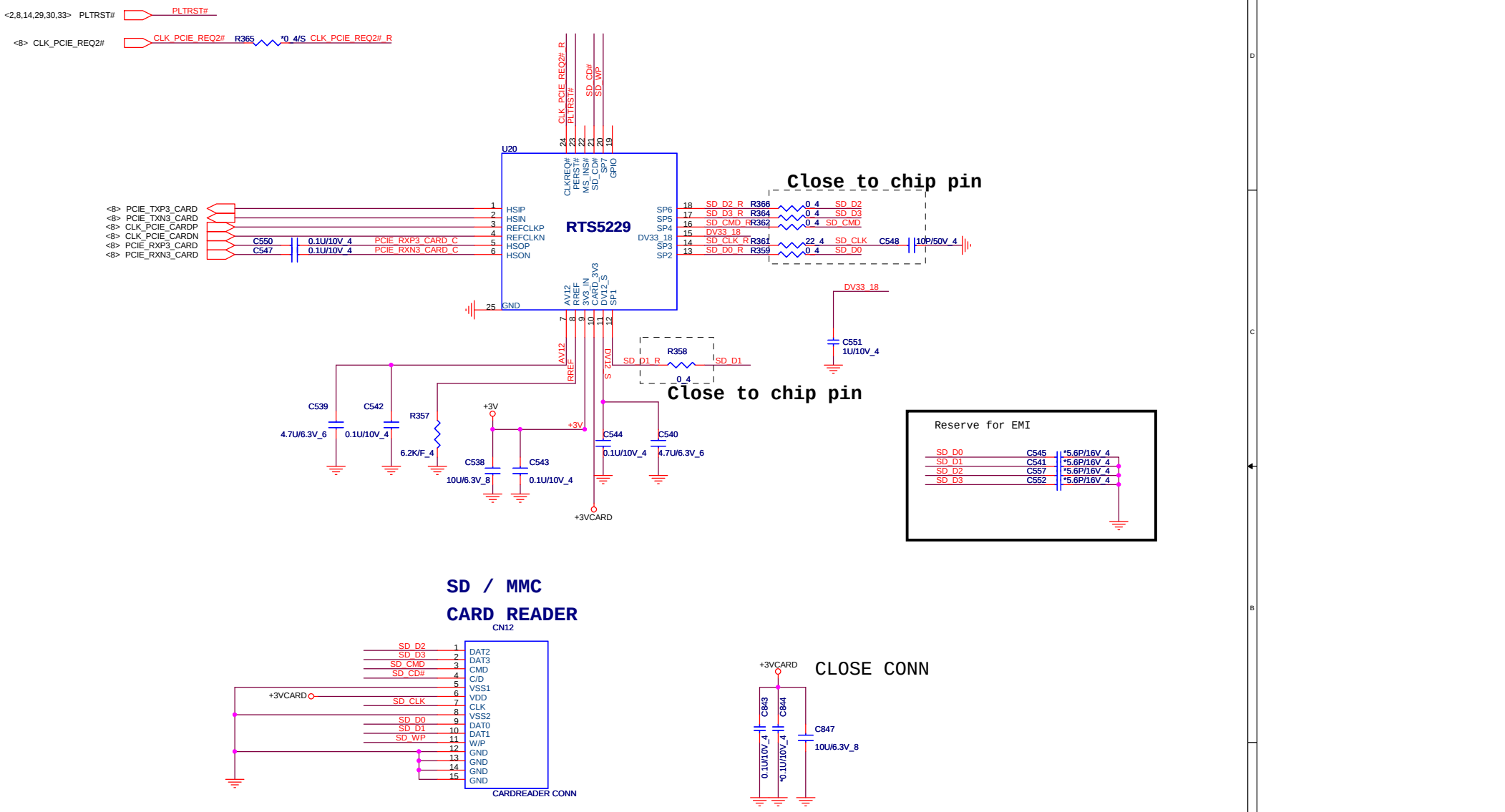
+5V_HDMIC
+5V_HDMIC
D10 RB501V-40
D9 RB501V-40
R90 2.2K_4
R87 2.2K_4
HDMI_SCLK
HDMI_SDATA

NB5

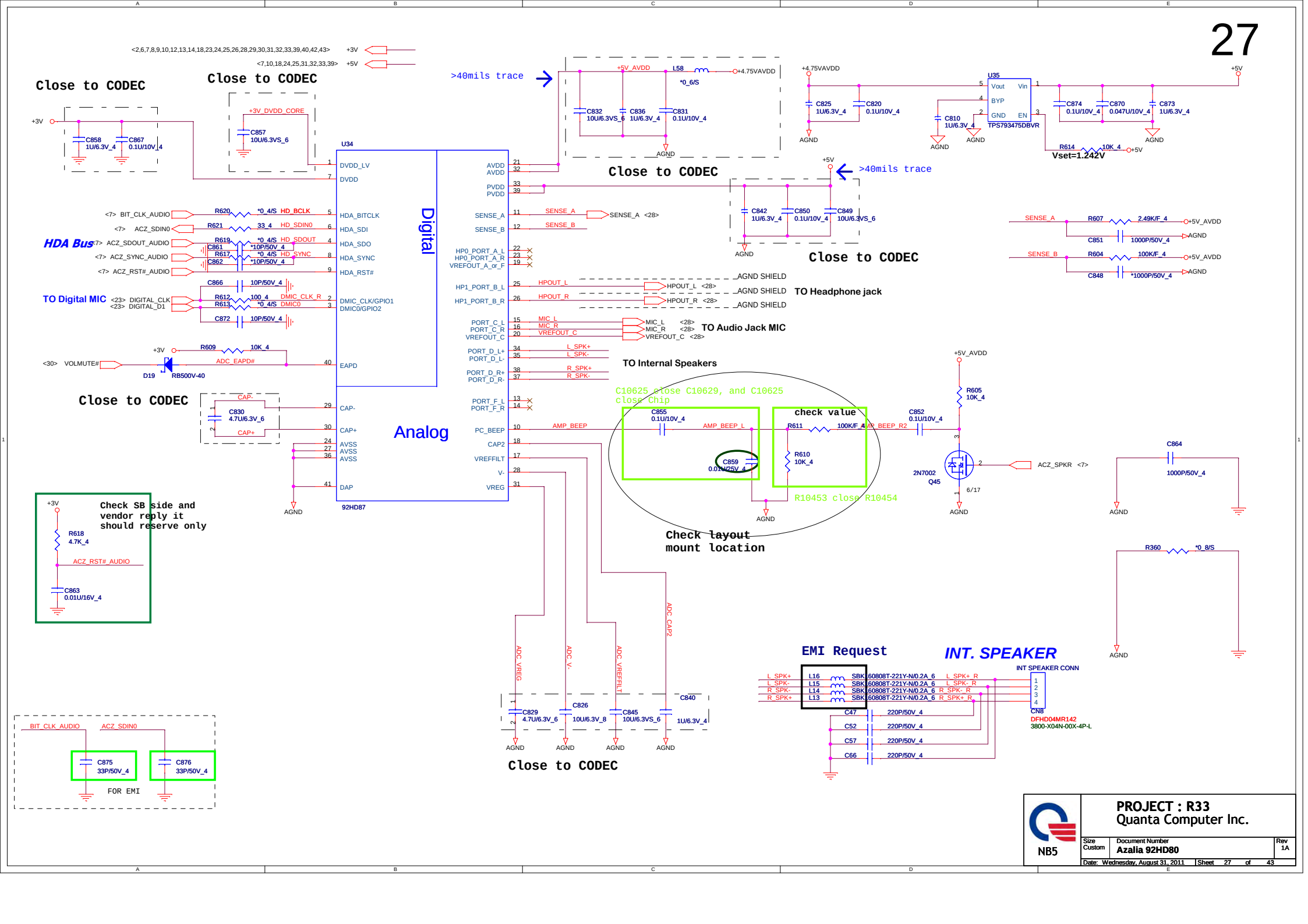
PROJECT : R33
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | HDMI CONN | 1A |

Date: Wednesday, August 24, 2011 Sheet 25 of 43




| | | |
|---|---|---|
| NB5 | PROJECT : R33<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: RTS5229 & CR SOCKET | Rev: 1A |
| Date: Thursday, August 25, 2011 | Sheet 26 of 43 | |


Close to CODEC
Close to CODEC
>40mils trace
Close to CODEC
>40mils trace
Close to CODEC
Close to CODEC
Close to CODEC
HDA Bus
TO Digital MIC
TO Headphone jack
TO Audio Jack MIC
TO Internal Speakers
Digital
Analog
U34
92HD87
U35
TPS793475DBVR
Vset=1.242V
C10625 close C10629, and C10625 close Chip
check value
R10453 close R10454
Check layout mount location
Check SB side and vendor reply it should reserve only
EMI Request
INT. SPEAKER
INT SPEAKER CONN
CN8
DFHD04MR142
3800-X04N-00X-4P-L
FOR EMI
NB5
PROJECT : R33
Quanta Computer Inc.
Azalia 92HD80
Wednesday, August 31, 2011

# USB3.0 X 2/USB2.0 COMBO

28

## USB 3.0

EMI request

1A

C739 1000P/50V_4

CN21 USB3.0 CONN

+5V_USBP0

USBP0- C C407 *Clamp-Diode

USBP0+ C C412 *Clamp-Diode

USB30_TX1- C C401 *Clamp-Diode

USB30_TX1+ C C383 *Clamp-Diode

USB30_RX1- C C422 *Clamp-Diode

USB30_RX1+ C C419 *Clamp-Diode

<8> USBP0-
<8> USBP0+

R218 0_4 L36 *WCM2012-90 R221 0_4

R227 0_4 L38 *WCM2012-90 R225 0_4

<8> USB30_RX1-
<8> USB30_RX1+

R208 0_4 L35 *WCM2012-90 R203 0_4

<8> USB30_TX1-
<8> USB30_TX1+

C395 0.1U/10V_4
C387 0.1U/10V_4

USB30_TX1- R
USB30_TX1+ R

USBP0- C
USBP0+ C

USB30_RX1- C
USB30_RX1+ C

USB30_TX1- C
USB30_TX1+ C

## USB 3.0

EMI request

1A

C765 1000P/50V_4

CN22 USB3.0 CONN

+5V_USBP0

USBP1- C C465 *Clamp-Diode

USBP1+ C C476 *Clamp-Diode

USB30_TX2- C C457 *Clamp-Diode

USB30_TX2+ C C447 *Clamp-Diode

USB30_RX2- C C479 *Clamp-Diode

USB30_RX2+ C C478 *Clamp-Diode

<8> USBP1-
<8> USBP1+

R244 0_4 L41 *WCM2012-90 R245 0_4

R249 0_4 L42 *WCM2012-90 R247 0_4

<8> USB30_RX2-
<8> USB30_RX2+

R243 0_4 L40 *WCM2012-90 R242 0_4

<8> USB30_TX2-
<8> USB30_TX2+

C455 0.1U/10V_4
C451 0.1U/10V_4

USB30_TX2- R
USB30_TX2+ R

USBP1- C
USBP1+ C

USB30_RX2- C
USB30_RX2+ C

USB30_TX2- C
USB30_TX2+ C

## USB3.0 X 2/USB2.0 COMBO

U30 G547N2P81U

80 mils (Iout=2A)

+5VS5

+5V_USBP0

VIN1 VIN2 EN GND
OUT3 OUT2 OUT1 OC

<30> USBPW_ON#

C793 1U/6.3V_4

C741 470P/50V_4
C740 0.1U/10V_4
C791 470P/50V_4
C787 0.1U/10V_4
C782 100U/25V

## Right SIDE USBX1

USBP9- R29 *0_4 USBP9- R

USBP9+ R28 *0_4 USBP9+ R

C43 0.1U/10V_4 +5VS5

<8> USBP9-
<8> USBP9+

L12 WCM2012-90

USBPW_ON#
USBP9- R
USBP9+ R

<7> SATA_LED#
<30> PWRLED_RIGHT

SATA_LED#
C37 1000P/50V_4
PWRLED_RIGHT
C36 1000P/50V_4

<8> ACC_LED#

+3V

CN6 USB CONN

EMI request

USBPW_ON# C40 220P/50V_4

## Line out

AGND SHIELD
AGND SHIELD
AGND SHIELD

<27> HPOUT_L
<27> HPOUT_R

HPOUT_L
HPOUT_R

R327 16/F_4 HPOUT_L1
R313 16/F_4 HPOUT_R1

BLM18BD601SN1D L46
BLM18BD601SN1D L45

R317 *20K/F_4
R333 *20K/F_4
C507 1000P/50V_4
C522 1000P/50V_4

AGND

HPOUT_L2
HPOUT_R2

VC11 *AVLC5S_4
VC9 *AVLC5S_4
C526 0.1U/10V_4
C518 0.1U/10V_4

AGND

CN24

HP-JACK-BLACK
Normal Open

SENSE_PHONE

VC10 *AVLC5S_4 AGND

SENSE_PHONE R312 20K/F_4 SENSE_A

SENSE_A <27>

SENSE_MIC R283 10K/F_4 SENSE_A

VC6 *AVLC5S_4 AGND

## MIC

<27> VREFOUT_C

C486 1U/6.3V_4 AGND

VREFOUT_C R297 3.9K/F_4

R300 3.9K/F_4

<27> MIC_L
<27> MIC_R

MIC_L C799 2.2U/6.3V_6
MIC_R C794 2.2U/6.3V_6

MIC_L1
MIC_R1

BLM18BD601SN1D L44
BLM18BD601SN1D L43

MIC_IN_L
MIC_IN_R

C485 220P/50V_4
C491 220P/50V_4

AGND

VC7 *AVLC5S_4
VC8 *AVLC5S_4

AGND

CN23

HP-JACK-BLACK
Normal Open

SENSE_MIC

COMPONENT CHOICES:
The selection of ferrite beads can have a large effect on THD+N, causing failures versus the WLP requirements.
At this time, IDT has verified three ferrite beads that will meet the WLP performance requirements:
Murata: BLM18BD601SN1
TDK: MMZ1608Y601BTA
Taiyo Yuden: LF BK 1608HM601-T

NB5

**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | USB/BT/Audio JacK | 1A |

Date: Monday, August 29, 2011 | Sheet 28 of 43

For EMI 0 ~ 22 ohm

R54 10_4 LAN_XTAL1 XTAL1

Y5 25MHz XTAL2

C70 33P/50V_4

C71 33P/50V_4

+3VLANVCC

C79 0.1U/10V_4

C76 0.1U/10V_4

C97 0.1U/10V_4

+3V_LAN

C85 0.1U/10V_4

GND VIA x 9 Pcs

+1.05V_LAN

R55 2.49K/F_4 LANRSET

+3V_LAN

LAN_TX#

LAN_GPIOS R56 1K/F_4 +3V_LAN

LAN_GLINK100#

U9 RTL8105E

GND AVDD33 AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 AVDD33 DVDD10(NC) LED0 DVDD33 GPO/SMBALERT LED1/EESK

MDI0+ MDI0- MDI1+ MDI1-

MDIP0 MDIN0 AVDD10 MDIP1 MDIN1 AVDD10(NC) MDIP2(NC) MDIN2(NC) AVDD10(NC) MDIP3(NC) MDIN3(NC) AVDD33(NC)

REGOUT VDDREG VDDREG ENSWREG EEDI LED3/EEDO EECS DVDD10 LANWAKEB DVDD33 ISOLATEB PERSTB

LAN_GLINK10# R57 10K/F_4

LAN_ECS_SCL R58 10K/F_4

PCIE_WAKE# +1.05V_LAN

PCIE_WAKE# <6,33>

+3V_LAN

ISOLATEB

PLTRST# <2,8,14,26,30,33>

DVDD10 SMBCLK(NC) SMBDATA(NC) CLKREQB HSIP HSIN REFCLK_P REFCLK_N EVDD10 HSOP HSON GND

+1.05V_LAN

LAN_CLKRQ

EVDD10

PCIE_RXN2_LAN_L C107 0.1U/10V_4 PCIE_RXN2_LAN <8>

PCIE_RXP2_LAN_L C110 0.1U/10V_4 PCIE_RXP2_LAN <8>

<8> PCIE_CLKREQ_LAN# PCIE_CLKREQ_LAN# R63 *0_4/S

<8> PCIE_TXP2_LAN PCIE_TXP2_LAN

<8> PCIE_TXN2_LAN PCIE_TXN2_LAN

<8> CLK_PCIE_LANP CLK_PCIE_LANP

<8> CLK_PCIE_LANN CLK_PCIE_LANN

+3V

R62 1K_4

ISOLATEB

R60 15K/F_4

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs ( excluding PCIE_WAKE# pin )

U8 NS681684

LAN_MX0+ LAN_MX0- LAN_MCT1 LAN_MX1+ LAN_MX1- LAN_MCT0

TD+ TD- CT RD+ RD- CT

TX+ CMT TX- RX- CT RX+

MDI0+ V_DAC2 MDI0- MDI1- V_DAC1 MDI1+

75_4 R51 C64 0.01U/100V_0603

75_4 R53 C77 0.01U/100V_0603

C46 10P/3KV_1808

C72 0.01U/25V_4

+1.05V_LAN

C106 0.1U/10V_4 C78 0.1U/10V_4 C105 0.1U/10V_4

EVDD10

C90 1U/6.3V_4 C98 0.1U/10V_4

+1.05V_LAN

C93 0.1U/10V_4 C92 0.1U/10V_4 C109 0.1U/10V_4 C108 0.1U/10V_4

LAN_GLINK100# LAN_GLED#

LAN_TX# LAN_YLED#

C234 *1000P/50V_4 C366 *1000P/50V_4

Link

RJ45

+3V_LAN R444 330_4 C707 1000P/50V_4

CN20

LAN_YLED LAN_YLED#

LED_AMBER_P LED_AMBER_N

LAN_MX1- LAN_MX0- LAN_MX1+ LAN_MX0+

RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+

FOR EMI

GND1 GND

R452 0_4

R422 0_4

+3V_LAN R425 330_4

LAN_GLED LAN_GLED#

LED_WHITE_P LED_WHITE_N

C667 1000P/50V_4

C690 1000P/50V_4

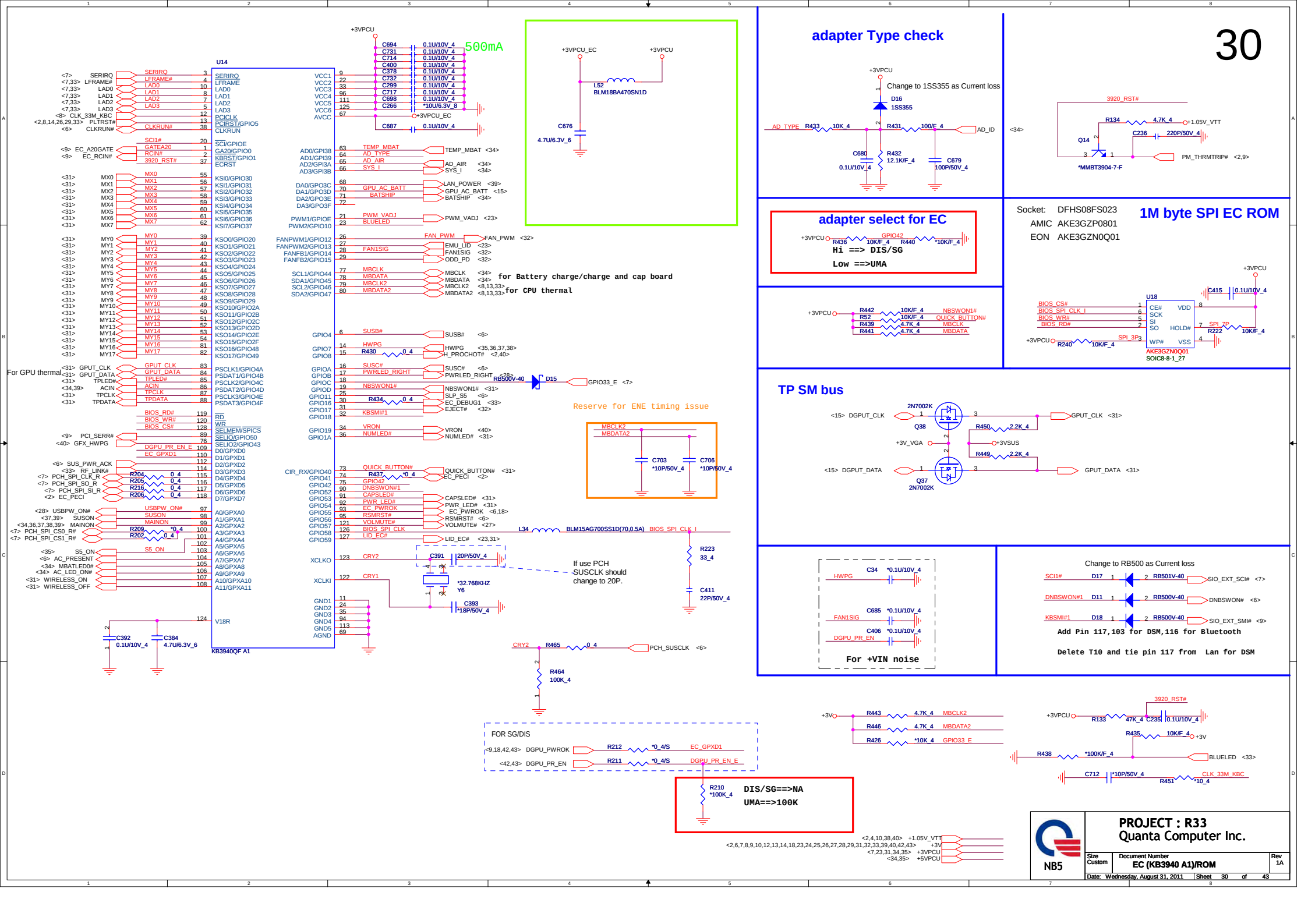
RJ45_CONN

NB5

PROJECT : R33
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | RTL 8105E/RJ45 | 1A |

Date: Wednesday, August 24, 2011 Sheet 29 of 43


30
adapter Type check
Change to 1SS355 as Current loss
D16
1SS355
AD_TYPE R433 10K_4
R431 100/F_4
AD_ID
C680 0.1U/10V_4
R432 12.1K/F_4
C679 100P/50V_4
3920_RST#
R134 4.7K_4
+1.05V_VTT
C236 220P/50V_4
Q14
PM_THRMTRIP# <2,9>
*MMBT3904-7-F
adapter select for EC
+3VPCU
R436 10K/F_4
GPIO42
R440 *10K/F_4
Hi ==> DIS/SG
Low ==>UMA
Socket: DFHS08FS023
AMIC AKE3GZP0801
EON AKE3GZN0Q01
1M byte SPI EC ROM
U18
BIOS_CS#
BIOS_SPI_CLK_I
BIOS_WR#
BIOS_RD#
CE# VDD
SCK
SI
SO HOLD#
WP# VSS
C415 0.1U/10V_4
SPI_ZP
R222 10K/F_4
SPI_3P
R240 10K/F_4
AKE3GZN0Q01
SOIC8-8-1_27
R442 10K/F_4 NBSWON1#
R52 10K/F_4 QUICK_BUTTON#
R439 4.7K_4 MBCLK
R441 4.7K_4 MBDATA
TP SM bus
2N7002K
Q38
Q37
R450 2.2K_4
R449 2.2K_4
+3V_VGA
+3VSUS
<15> DGPUT_CLK
<15> DGPUT_DATA
GPUT_CLK <31>
GPUT_DATA <31>
U14
KB3940QF A1
SERIRQ
LFRAME
LAD0
LAD1
LAD2
LAD3
PCICLK
PCIRST/GPIO5
CLKRUN
SCI/GPIOE
GA20/GPIO0
KBRST/GPIO1
ECRST
KSI0/GPIO30
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34
KSI5/GPIO35
KSI6/GPIO36
KSI7/GPIO37
KSO0/GPIO20
KSO1/GPIO21
KSO2/GPIO22
KSO3/GPIO23
KSO4/GPIO24
KSO5/GPIO25
KSO6/GPIO26
KSO7/GPIO27
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B
KSO12/GPIO2C
KSO13/GPIO2D
KSO14/GPIO2E
KSO15/GPIO2F
KSO16/GPIO48
KSO17/GPIO49
PSCLK1/GPIO4A
PSDAT1/GPIO4B
PSCLK2/GPIO4C
PSDAT2/GPIO4D
PSCLK3/GPIO4E
PSDAT3/GPIO4F
RD
WR
SELMEM/SPICS
SELIO/GPIO50
SELIO2/GPIO43
D0/GPXD0
D1/GPXD1
D2/GPXD2
D3/GPXD3
D4/GPXD4
D5/GPXD5
D6/GPXD6
D7/GPXD7
A0/GPXA0
A1/GPXA1
A2/GPXA2
A3/GPXA3
A4/GPXA4
A5/GPXA5
A6/GPXA6
A7/GPXA7
A8/GPXA8
A9/GPXA9
A10/GPXA10
A11/GPXA11
V18R
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
AVCC
GND1
GND2
GND3
GND4
GND5
AGND
C694 0.1U/10V_4
C731 0.1U/10V_4
C714 0.1U/10V_4
C400 0.1U/10V_4
C378 0.1U/10V_4
C732 0.1U/10V_4
C299 0.1U/10V_4
C717 0.1U/10V_4
C698 0.1U/10V_4
C266 *10U/6.3V_8
C687 0.1U/10V_4
500mA
+3VPCU_EC
+3VPCU
L52
BLM18BA470SN1D
C676
4.7U/6.3V_6
C392 0.1U/10V_4
C384 4.7U/6.3V_6
TEMP_MBAT <34>
AD_TYPE
AD_AIR <34>
SYS_I <34>
GPU_AC_BATT <15>
BATSHIP <34>
PWM_VADJ <23>
BLUELED
FAN_PWM <32>
EMU_LID <23>
FAN1SIG <32>
ODD_PD <32>
MBCLK <34>
MBDATA <34>
MBCLK2 <8,13,33>
MBDATA2 <8,13,33>
for Battery charge/charge and cap board
for CPU thermal
SUSB# <6>
HWPG <35,36,37,38>
H_PROCHOT# <2,40>
SUSC# <6>
PWRLED_RIGHT <28>
RB500V-40
D15
GPIO33_E <7>
NBSWON1# <31>
SLP_S5 <6>
EC_DEBUG1 <33>
EJECT# <32>
KBSMI#1
VRON <40>
NUMLED# <31>
Reserve for ENE timing issue
MBCLK2
MBDATA2
C703 *10P/50V_4
C706 *10P/50V_4
QUICK_BUTTON# <31>
EC_PECI <2>
CAPSLED# <31>
PWR_LED# <31>
EC_PWROK <6,18>
RSMRST# <6>
VOLMUTE# <27>
LID_EC# <23,31>
BIOS_SPI_CLK_I
L34 BLM15AG700SS1D(70,0.5A)
R223 33_4
C411 22P/50V_4
CRY2
CRY1
C391 20P/50V_4
*32.768KHZ
Y6
C393 *18P/50V_4
If use PCH SUSCLK should change to 20P.
R465 0_4
PCH_SUSCLK <6>
R464 100K_4
For GPU thermal
For +VIN noise
C34 *0.1U/10V_4
C685 *0.1U/10V_4
C406 *0.1U/10V_4
Change to RB500 as Current loss
D17 RB501V-40
D11 RB500V-40
D18 RB500V-40
SIO_EXT_SCI# <7>
DNBSWON# <6>
SIO_EXT_SMI# <9>
Add Pin 117,103 for DSM,116 for Bluetooth
Delete T10 and tie pin 117 from Lan for DSM
FOR SG/DIS
DGPU_PWROK
DGPU_PR_EN
R212 *0_4/S EC_GPXD1
R211 *0_4/S DGPU_PR_EN_E
R210 *100K_4
DIS/SG==>NA
UMA==>100K
R443 4.7K_4 MBCLK2
R446 4.7K_4 MBDATA2
R426 *10K_4 GIO33_E
R133 47K_4 C235 0.1U/10V_4
R435 10K/F_4
R438 *100K/F_4
C712 *10P/50V_4
R451 *10_4
CLK_33M_KBC
<2,4,10,38,40> +1.05V_VTT
<2,6,7,8,9,10,12,13,14,18,23,24,25,26,27,28,29,31,32,33,39,40,42,43> +3V
<7,23,31,34,35> +3VPCU
<34,35> +5VPCU
NB5
PROJECT : R33
Quanta Computer Inc.
Size Custom
Document Number EC (KB3940 A1)/ROM
Rev 1A
Date: Wednesday, August 31, 2011
Sheet 30 of 43

# KEYBOARD Con.

SI un-install

KEYBOARD PULL-UP

EC KB3930 has included K/B pull-up resistor and function

9/15 SI for H/W.

DFFC32FR025
bl135h-32rla-tand-32p-l-smt
*KB CONN

# KEYBOARD Con.
# Co-layout for 17" only

KB CONN

# POWER BOTTON CONNECT

100mA

1. +3VPCU(LIDSWITCH PWR)
2. QUICK_BUTTON
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

PWR BTN CONN
DFFC06MR001
88513-0601-6P-L-SMT

# TOUCH PAD Con.

change to +3VSUS
close conn

25 mils

TOUCH PAD CONN
DFFC08FR026
50503-0080n-001-8p-l

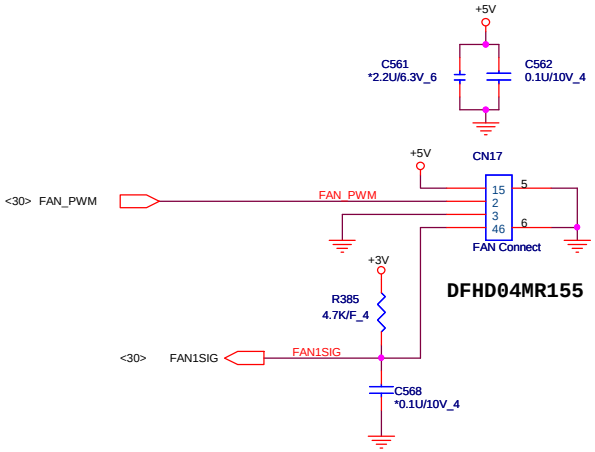
NB5

**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | LED/KB/SW/TP | 1A |

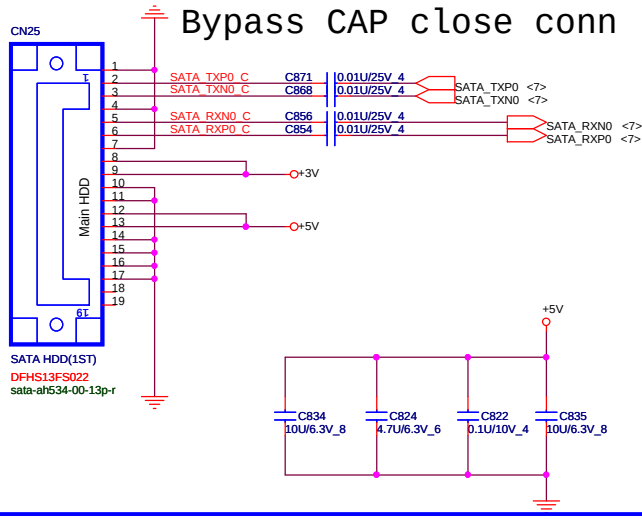
Date: Wednesday, August 24, 2011 | Sheet 31 of 43

# CPU FAN

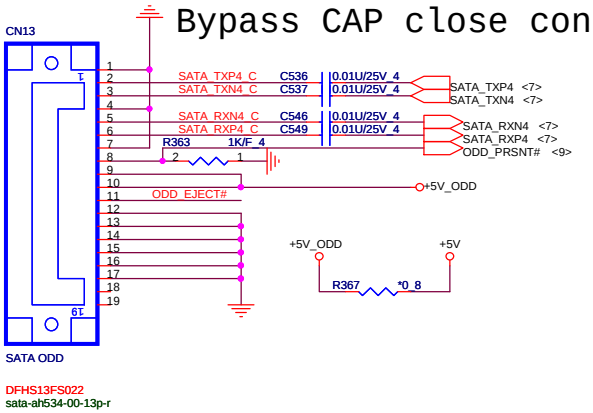


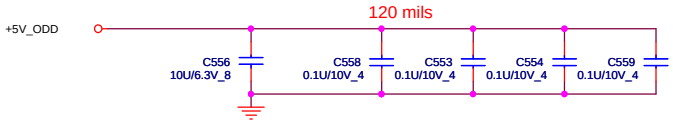

# SATA HDD CONNECTOR



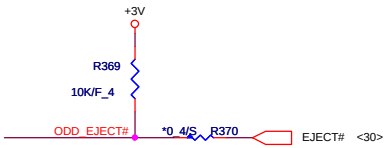



# SATA ODD CONNECTOR

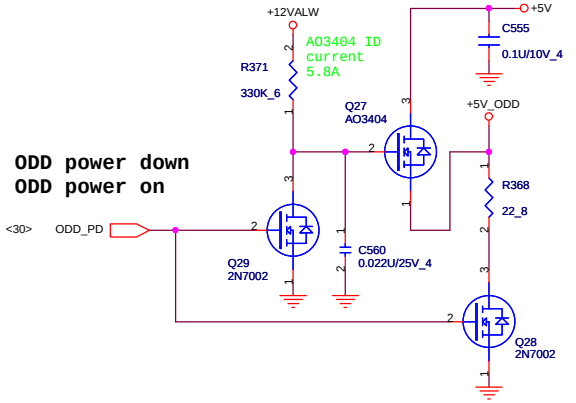



follow INTEL DG change eject PU to +3V.

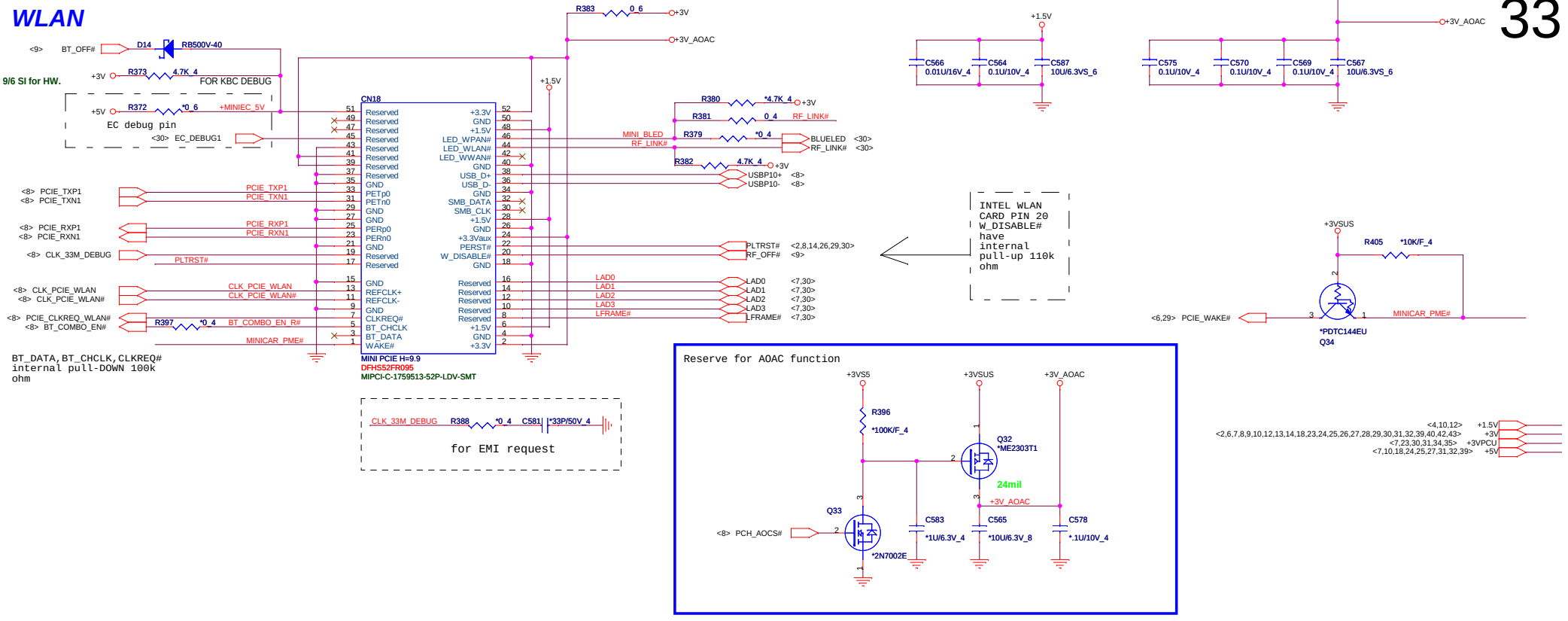



High : ODD power down
Low : ODD power on

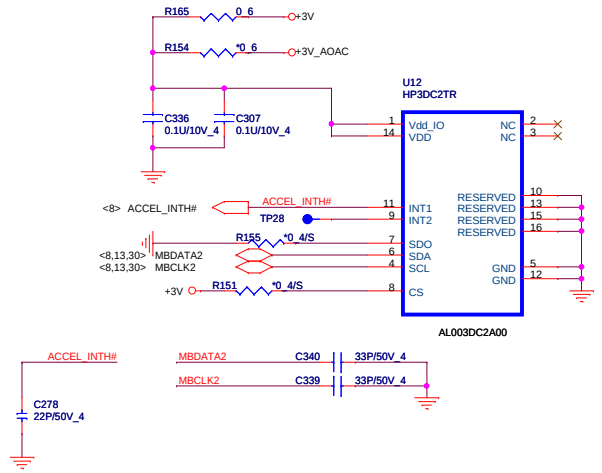



| | | |
|---|---|---|
| NB5 | PROJECT : R33<br>Quanta Computer Inc. | |
| | Size: Custom<br>Document Number: HDD/ODD/FAN | Rev: 1A |
| | Date: Thursday, August 25, 2011 | Sheet 32 of 43 |

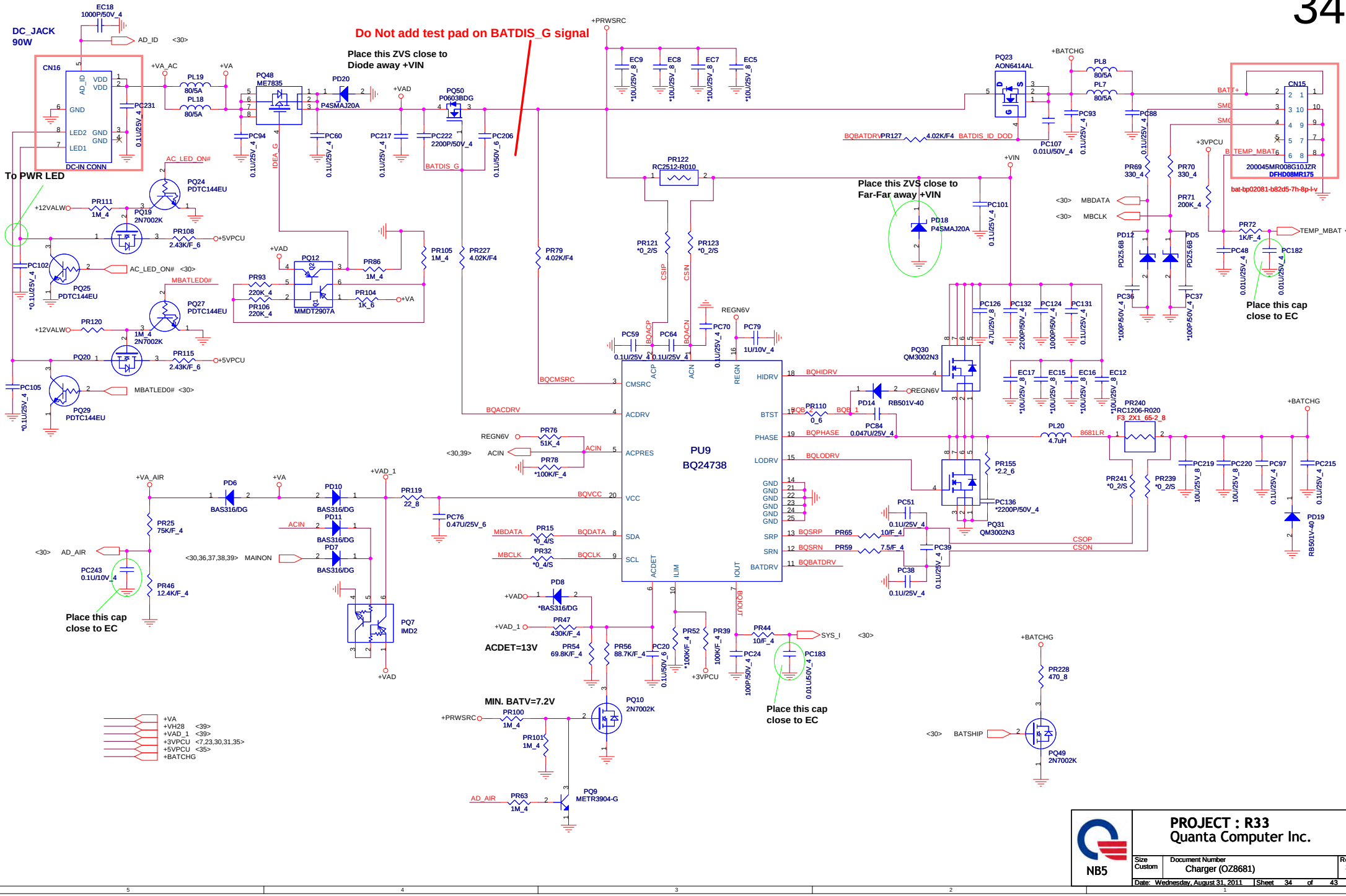
# Mini PCI-E Card 1
## WLAN




# Accelerometer Sensor




| | | | |
|---|---|---|---|
| NB5 | PROJECT : R33<br>Quanta Computer Inc. | | |
| | Size: Custom | Document Number: MINI PCIE CONN & G-sensor | Rev: 1A |
| | Date: Wednesday, August 31, 2011 | Sheet 33 of 43 | |


DC_JACK
90W
CN16
DC-IN CONN
To PWR LED
Do Not add test pad on BATDIS_G signal
Place this ZVS close to
Diode away +VIN
Place this ZVS close to
Far-Far away +VIN
Place this cap
close to EC
Place this cap
close to EC
Place this cap
close to EC
PU9
BQ24738
ACDET=13V
MIN. BATV=7.2V
+PRWSRC
+VIN
+BATCHG
+VA
+VAD
+3VPCU
+5VPCU
+12VALW
REGN6V
SYS_I
BATSHIP
CN15
200045MR008G10JZR
DFHD08MR175
bat-bp02081-b82d5-7h-8p-l-v
PROJECT : R33
Quanta Computer Inc.
NB5
Size Custom
Document Number
Charger (OZ8681)
Rev 1A
Date: Wednesday, August 31, 2011
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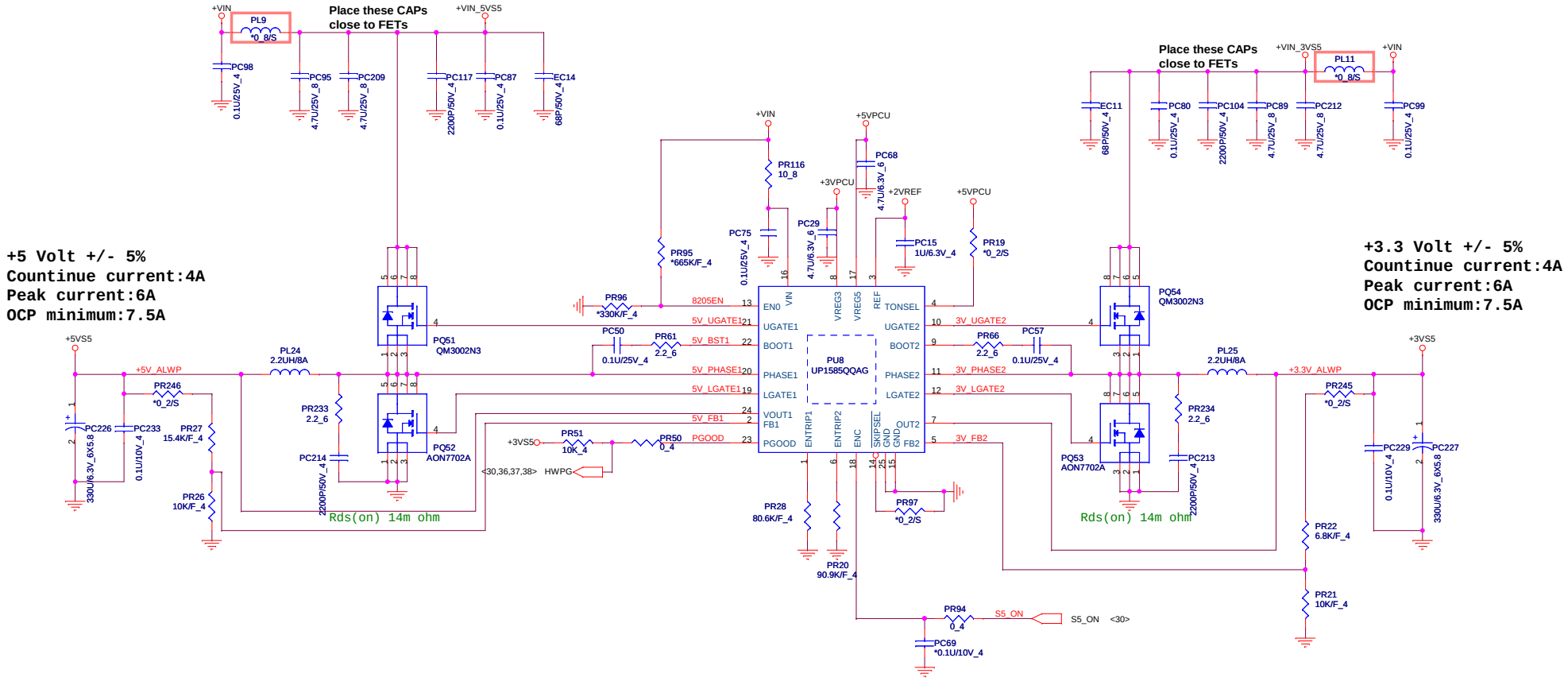
+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A
Place these CAPs close to FETs
Place these CAPs close to FETs
PU8 UP1585QQAG
PQ51 QM3002N3
PQ52 AON7702A
PQ53 AON7702A
PQ54 QM3002N3
Rds(on) 14m ohm
Rds(on) 14m ohm
+VIN
+VIN_5VS5
+VIN_3VS5
+5VS5
+3VS5
+5VPCU
+3VPCU
+2VREF
+5V_ALWP
+3.3V_ALWP
8205EN
5V_UGATE1
5V_BST1
5V_PHASE1
5V_LGATE1
5V_FB1
PGOOD
3V_UGATE2
3V_PHASE2
3V_LGATE2
3V_FB2
S5_ON
<30,36,37,38> HWPG
PL9 *0_8/S
PL11 *0_8/S
PL24 2.2UH/8A
PL25 2.2UH/8A
PR116 10_8
PR95 *665K/F_4
PR96 *330K/F_4
PR97 *0_2/S
PR19 *0_2/S
PR28 80.6K/F_4
PR20 90.9K/F_4
PR94 0_4
PR22 6.8K/F_4
PR21 10K/F_4
PR246 *0_2/S
PR245 *0_2/S
PR233 2.2_6
PR234 2.2_6
PR27 15.4K/F_4
PR26 10K/F_4
PR51 10K_4
PR50 0_4
PR61 2.2_6
PR66 2.2_6
PC50 0.1U/25V_4
PC57 0.1U/25V_4
PC214 2200P/50V_4
PC213 2200P/50V_4
PC69 *0.1U/10V_4
PC68 4.7U/6.3V_6
PC29 4.7U/6.3V_6
PC75 0.1U/25V_4
PC15 1U/6.3V_4
PC98 0.1U/25V_4
PC95 4.7U/25V_8
PC209 4.7U/25V_8
PC117 2200P/50V_4
PC87 0.1U/25V_4
EC14 68P/50V_4
EC11 68P/50V_4
PC80 0.1U/25V_4
PC104 2200P/50V_4
PC89 4.7U/25V_8
PC212 4.7U/25V_8
PC99 0.1U/25V_4
PC226 330U/6.3V_6X5.8
PC233 0.1U/10V_4
PC229 0.1U/10V_4
PC227 330U/6.3V_6X5.8
NB5
PROJECT : R33
Quanta Computer Inc.
Size Custom
Document Number 3/5VPCU(RT8223P)
Rev 1A
Date: Monday, August 29, 2011
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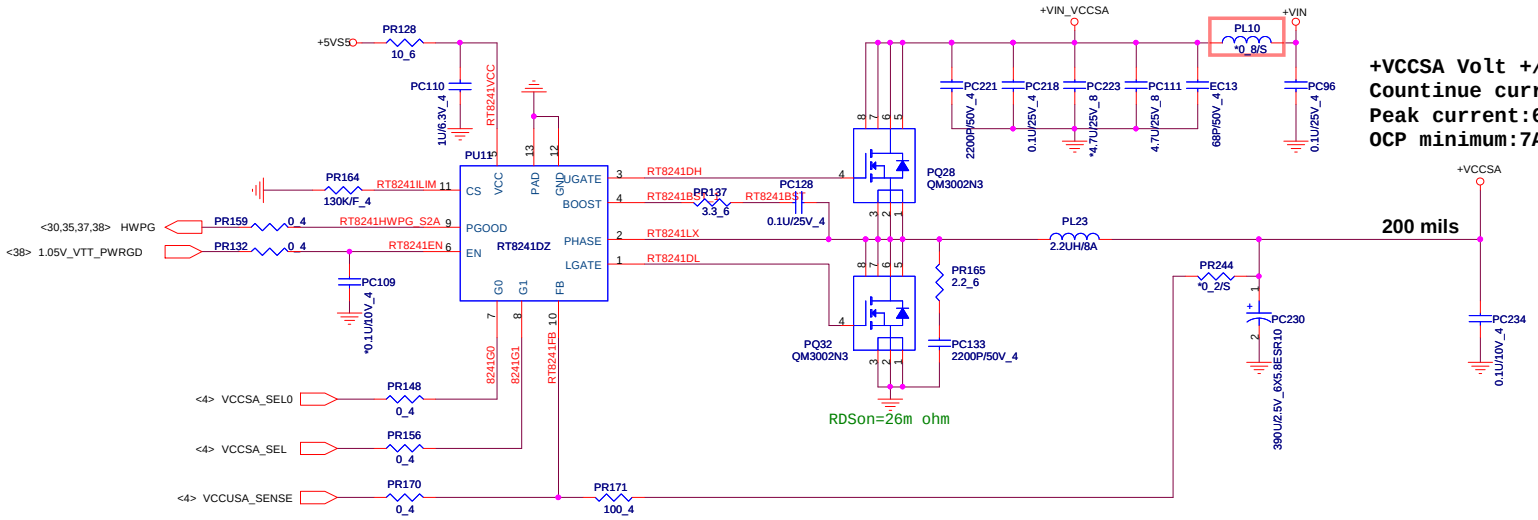
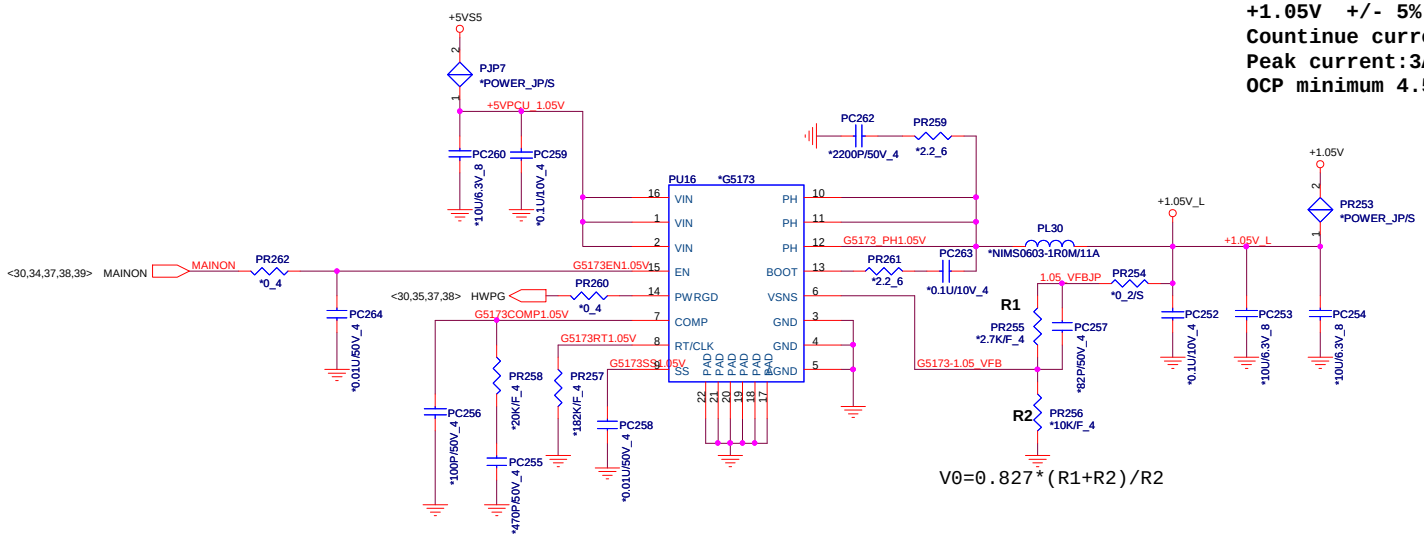
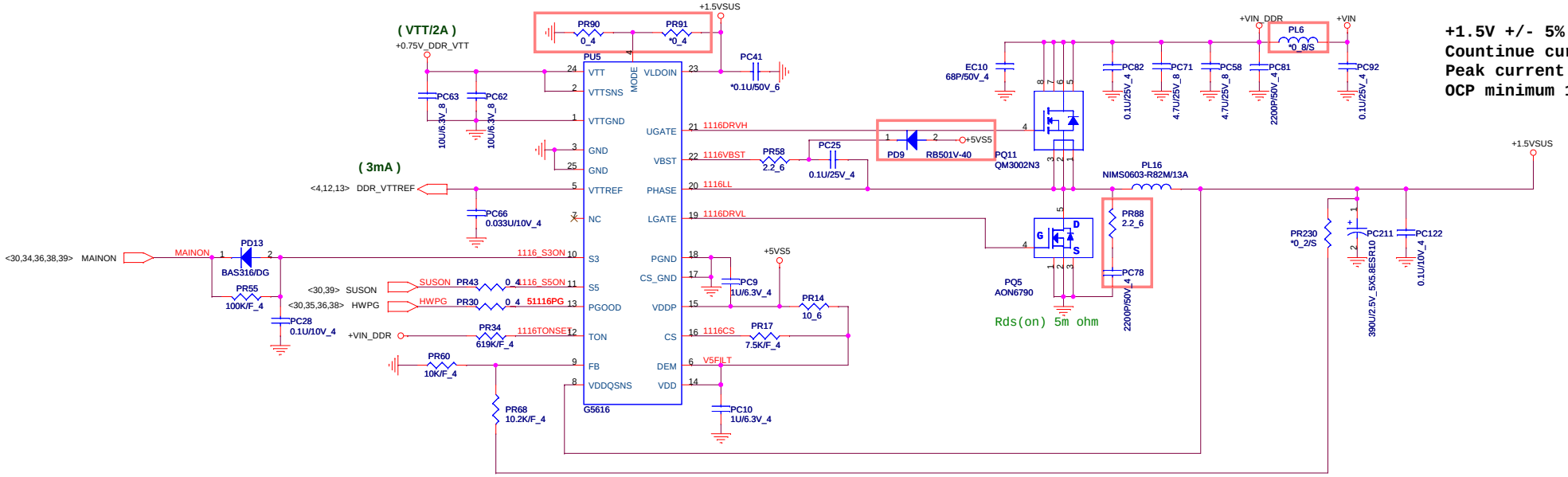



**CPU system agent**
**voltage slew rate of 0.5 -10 mV/µs**

| H_FC_C22<br>VID0 | VCCSA_SEL<br>VID1 | Vout |
|---|---|---|
| 0 | 0 | 0.9V |
| 0 | 1 | 0.80V (SV-RT8241DZGQW)<br>0.85V (LV-RT8241EZGQW) |
| 1 | 0 | 0.725V |
| 1 | 1 | 0.675V |




| | | |
|---|---|---|
| NB5 | PROJECT : R33<br>Quanta Computer Inc. | |
| | Size: Custom<br>Document Number: VCCSA (RT8241EZ) | Rev: 1A |
| | Date: Monday, August 29, 2011 | Sheet 36 of 43 |




**+1.5V +/- 5%**
**Countinue current:10A**
**Peak current:12A**
**OCP minimum 15A**

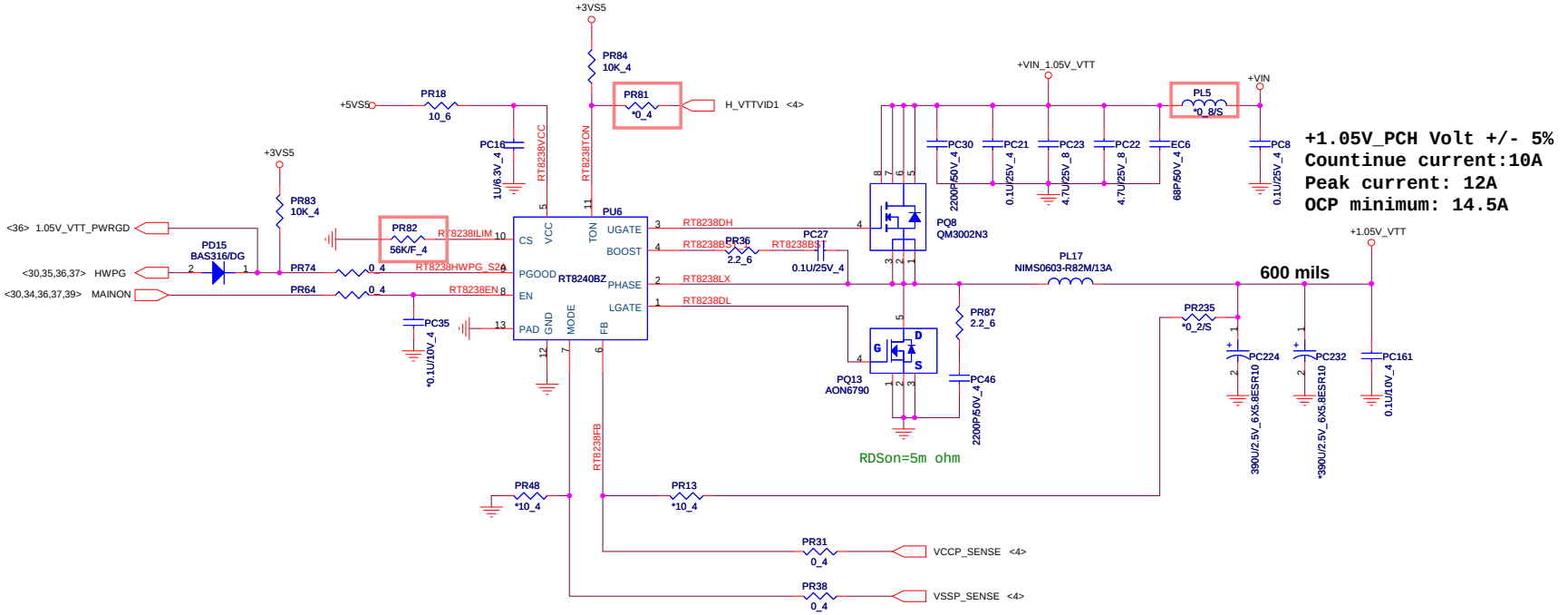
**PROJECT : R33**
Quanta Computer Inc.

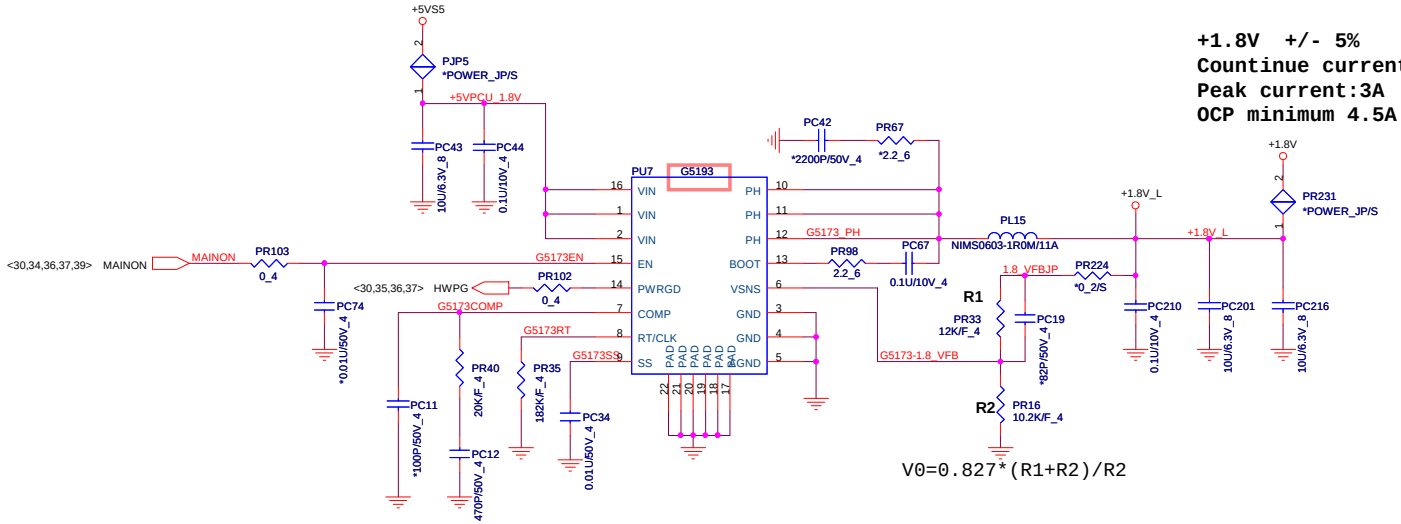
| Size | Document Number | Rev |
|---|---|---|
| Custom | DDRIII(RT8207LGQW) | 1A |
| Date: Wednesday, August 31, 2011 | Sheet 37 of 43 | |

NB5

# 1.05V_VTT



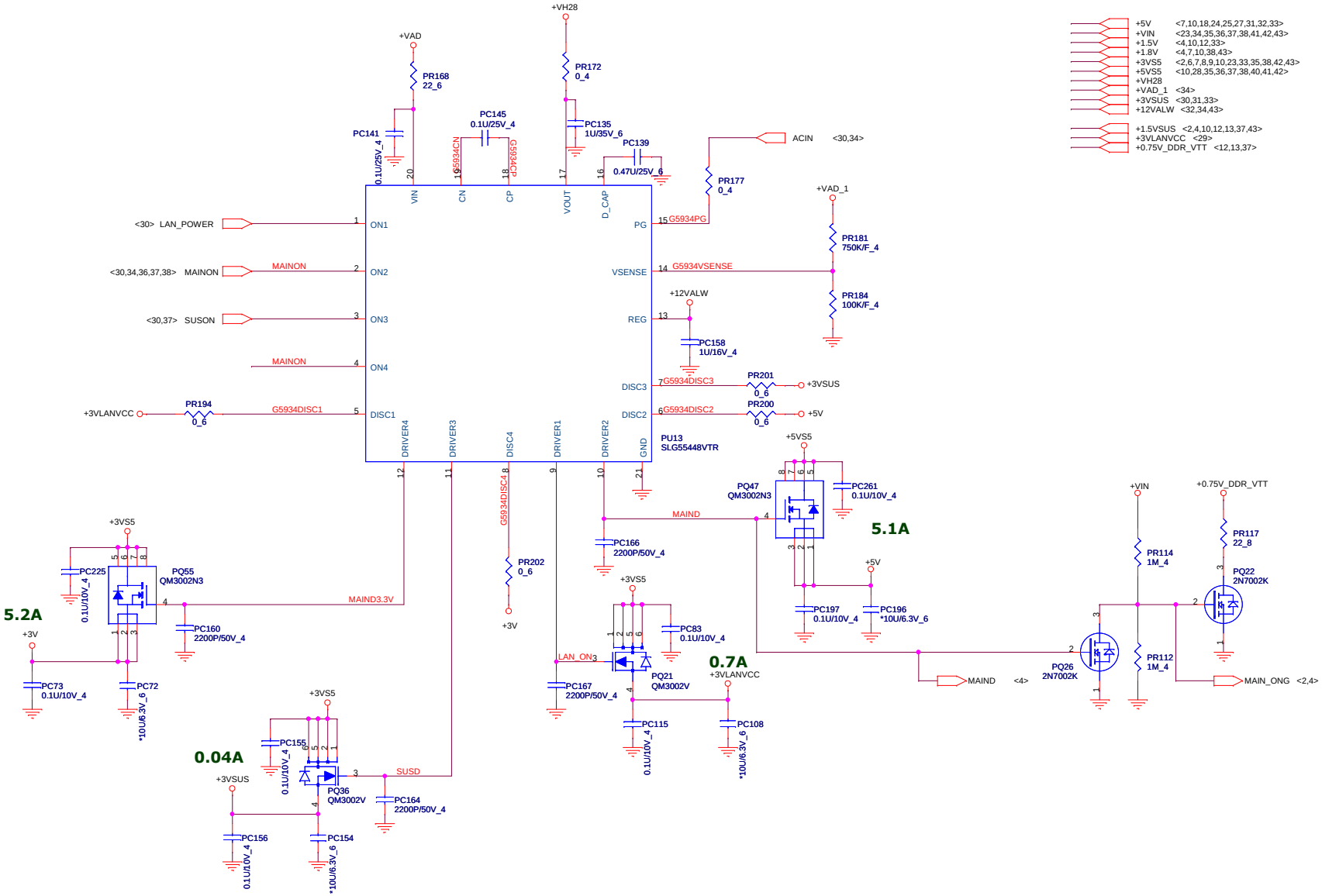



NB5

**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | 1.0V(RT8228BZ)/1.8V(G5173) | 1A |
| Date: Wednesday, August 31, 2011 | Sheet 38 of 43 | |




+5V <7,10,18,24,25,27,31,32,33>
+VIN <23,34,35,36,37,38,41,42,43>
+1.5V <4,10,12,33>
+1.8V <4,7,10,38,43>
+3VS5 <2,6,7,8,9,10,23,33,35,38,42,43>
+5VS5 <10,28,35,36,37,38,40,41,42>
+VH28
+VAD_1 <34>
+3VSUS <30,31,33>
+12VALW <32,34,43>

+1.5VSUS <2,4,10,12,13,37,43>
+3VLANVCC <29>
+0.75V_DDR_VTT <12,13,37>

NB5

**PROJECT : R33**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Dis-charge IC (G5934) | 1A |

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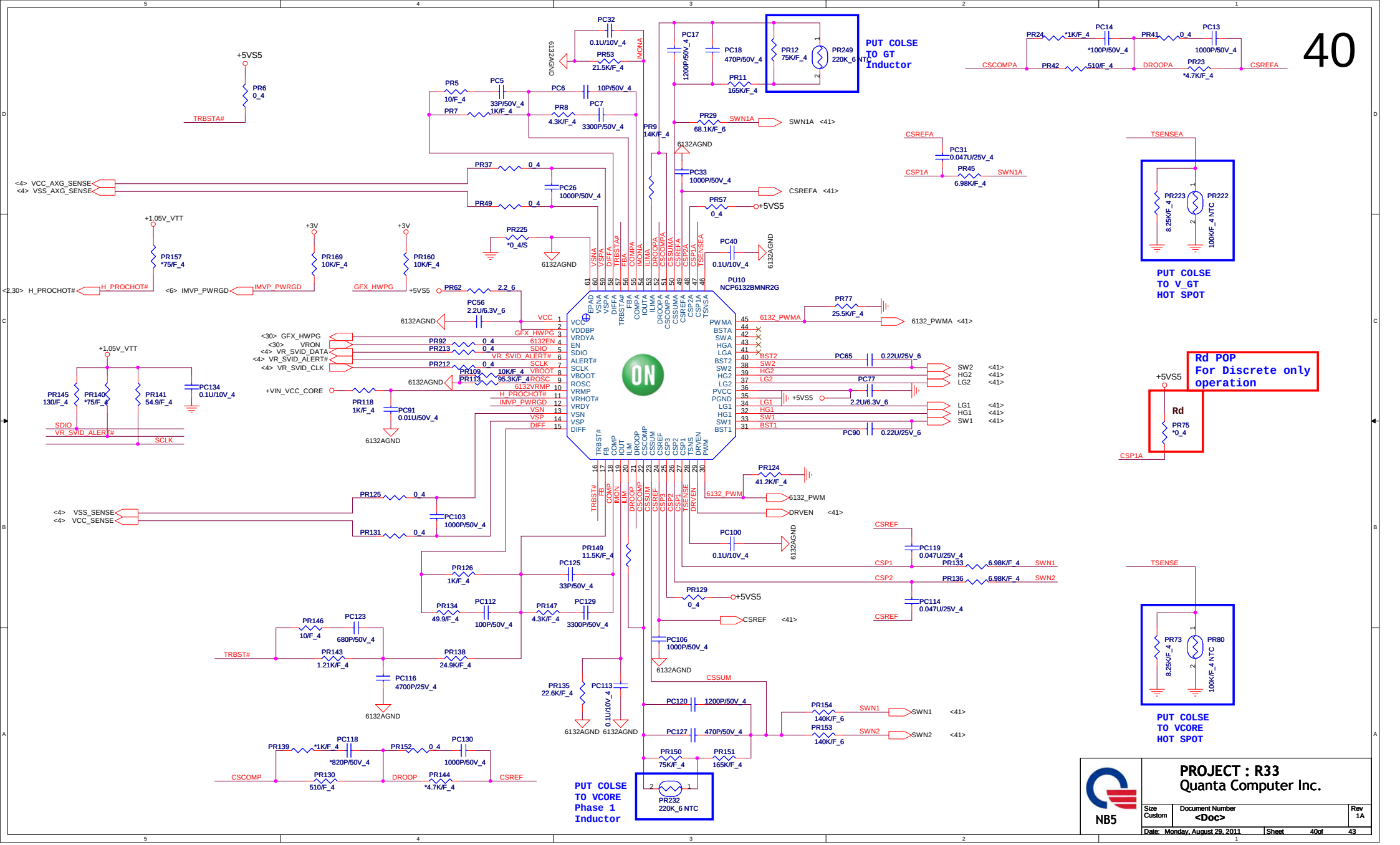
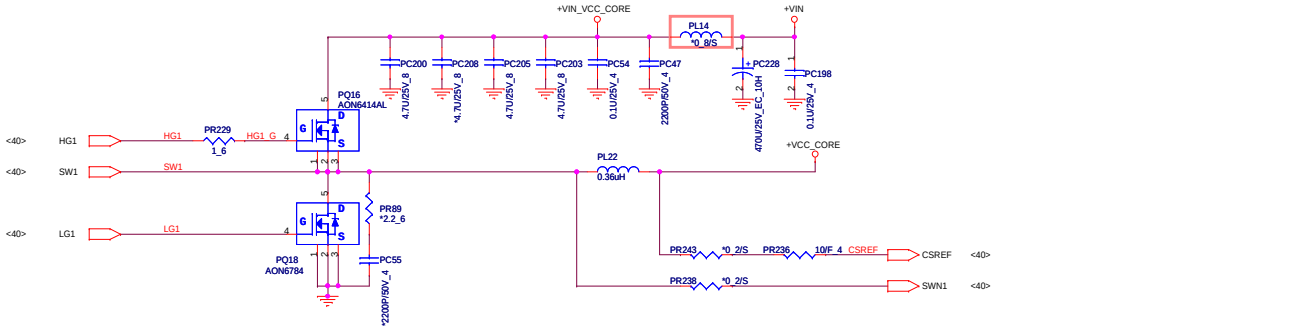
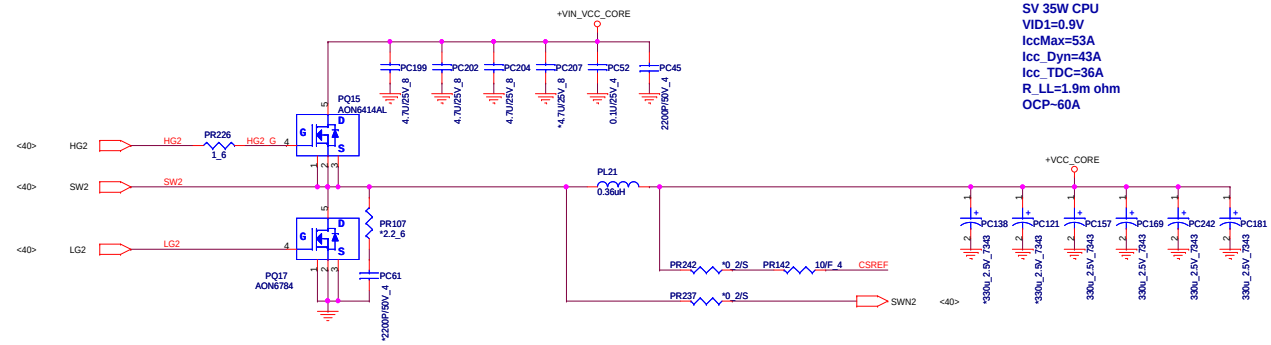
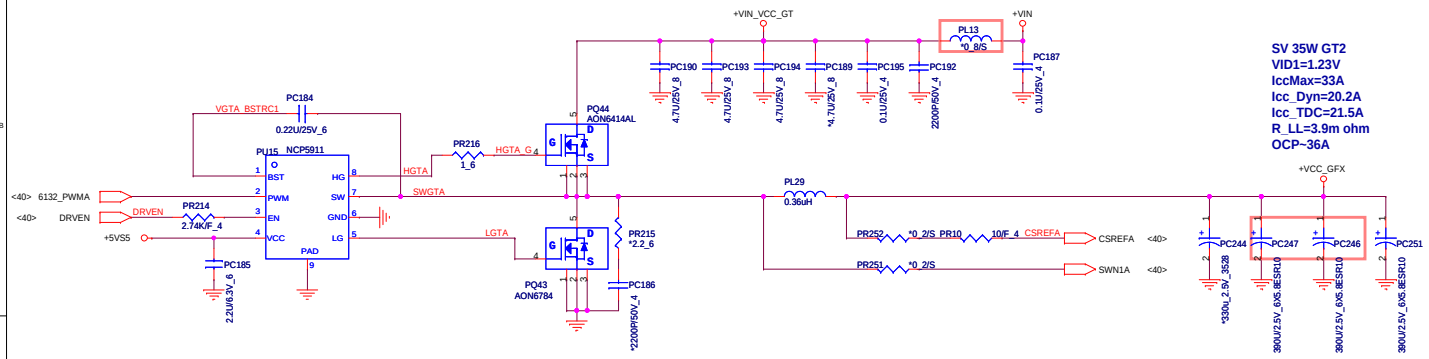

40
PUT COLSE TO GT Inductor
PUT COLSE TO V_GT HOT SPOT
PUT COLSE TO VCORE HOT SPOT
PUT COLSE TO VCORE Phase 1 Inductor
Rd POP For Discrete only operation
PU10 NCP6132BMNR2G
PROJECT : R33
Quanta Computer Inc.
NB5
Size Custom
Document Number <Doc>
Rev 1A
Date: Monday, August 29, 2011
Sheet 40of 43




**SV 35W CPU**
**VID1=0.9V**
**IccMax=53A**
**Icc_Dyn=43A**
**Icc_TDC=36A**
**R_LL=1.9m ohm**
**OCP~60A**




**SV 35W GT2**
**VID1=1.23V**
**IccMax=33A**
**Icc_Dyn=20.2A**
**Icc_TDC=21.5A**
**R_LL=3.9m ohm**
**OCP~36A**

| | | |
|---|---|---|
| NB5 | PROJECT : R33<br>Quanta Computer Inc. | |
| Size C | Document Number <Doc> | Rev 1A |
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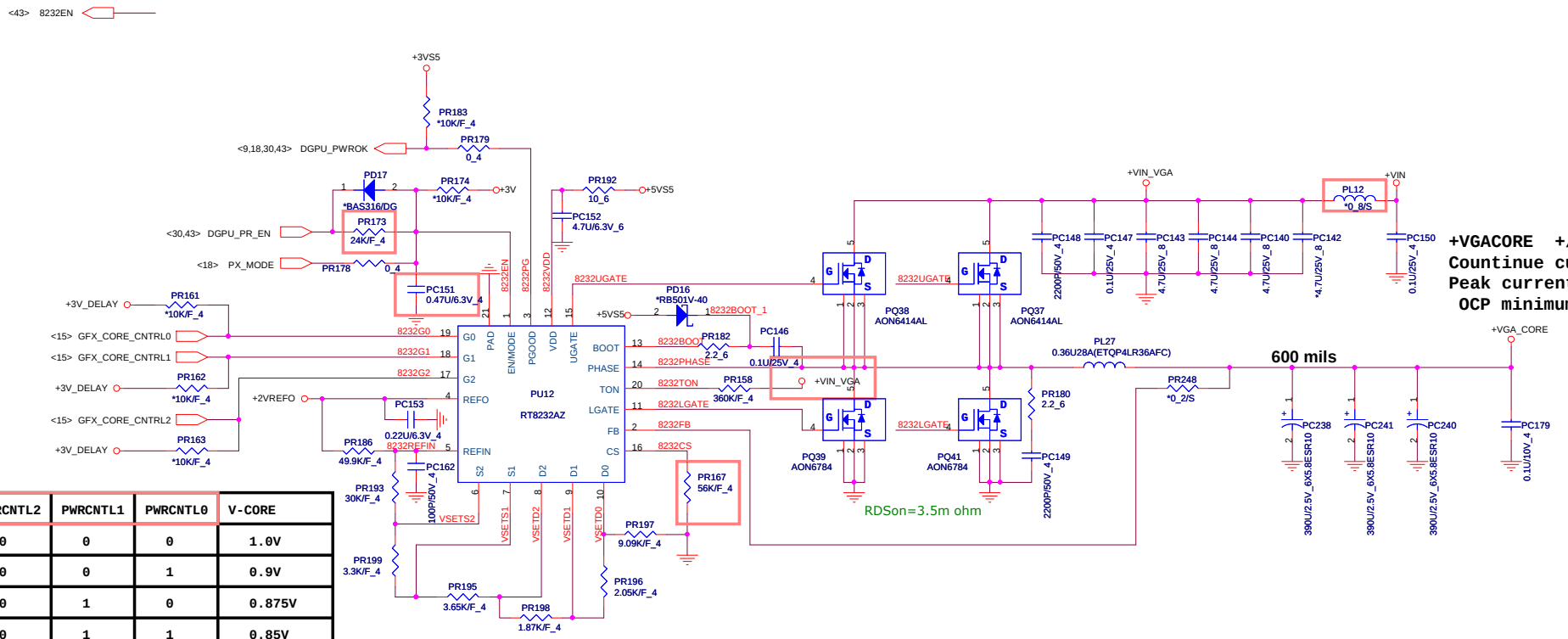
# VGA Core






| thames xt | PWRCNTL2 | PWRCNTL1 | PWRCNTL0 | V-CORE |
|---|---|---|---|---|
| L | 0 | 0 | 0 | 1.0V |
| M | 0 | 0 | 1 | 0.9V |
| H | 0 | 1 | 0 | 0.875V |
| | 0 | 1 | 1 | 0.85V |
| | 1 | 0 | 0 | 0.8V |
| | 1 | 0 | 1 | 0.75V |

| | | | |
|---|---|---|---|
| NB5 | PROJECT : R33<br>Quanta Computer Inc. | | |
| | Size: Custom | Document Number: +VGACORE (RT8208/1.8V) | Rev: 1A |
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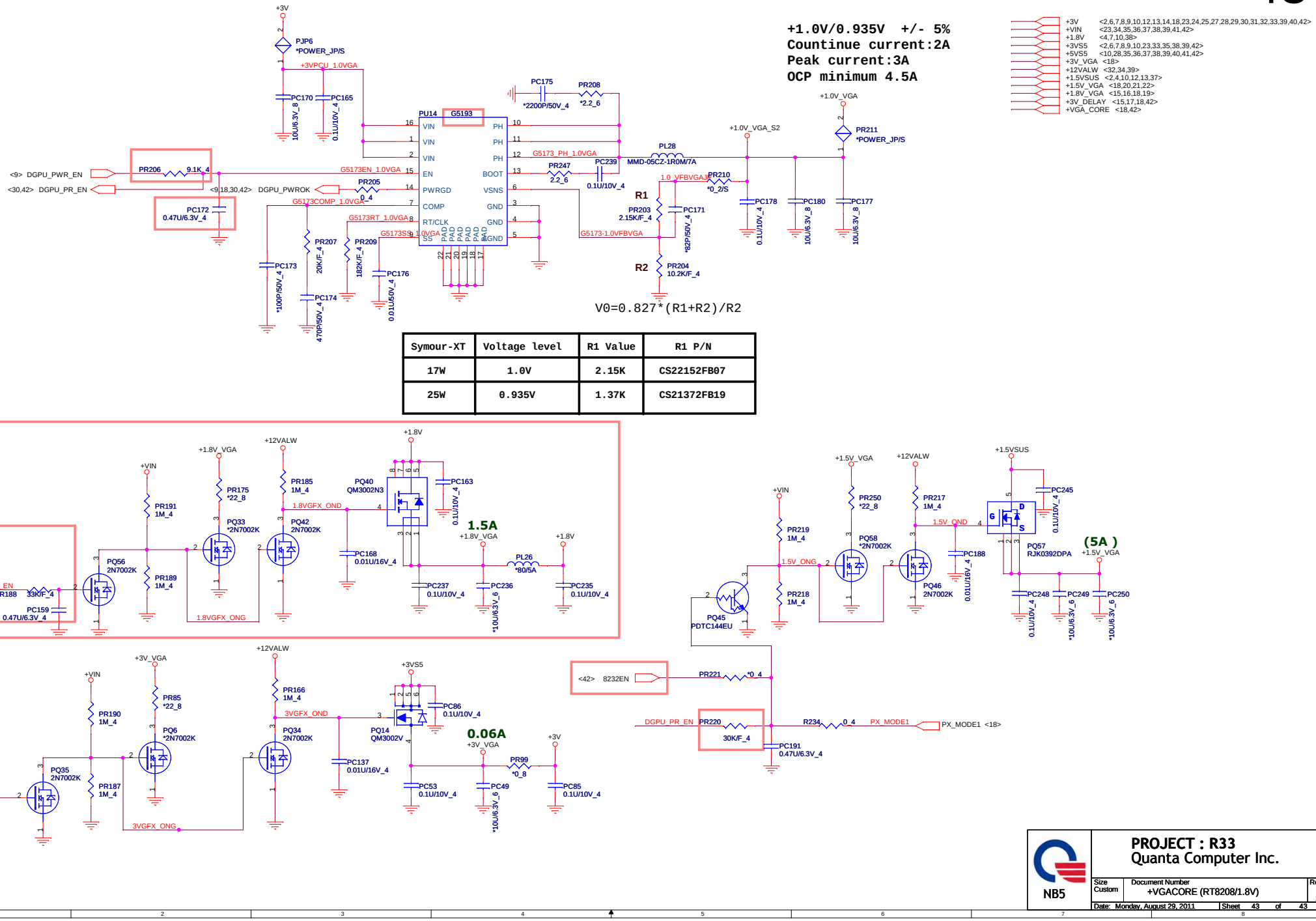


| Symour-XT | Voltage level | R1 Value | R1 P/N |
|---|---|---|---|
| 17W | 1.0V | 2.15K | CS22152FB07 |
| 25W | 0.935V | 1.37K | CS21372FB19 |













NB5

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