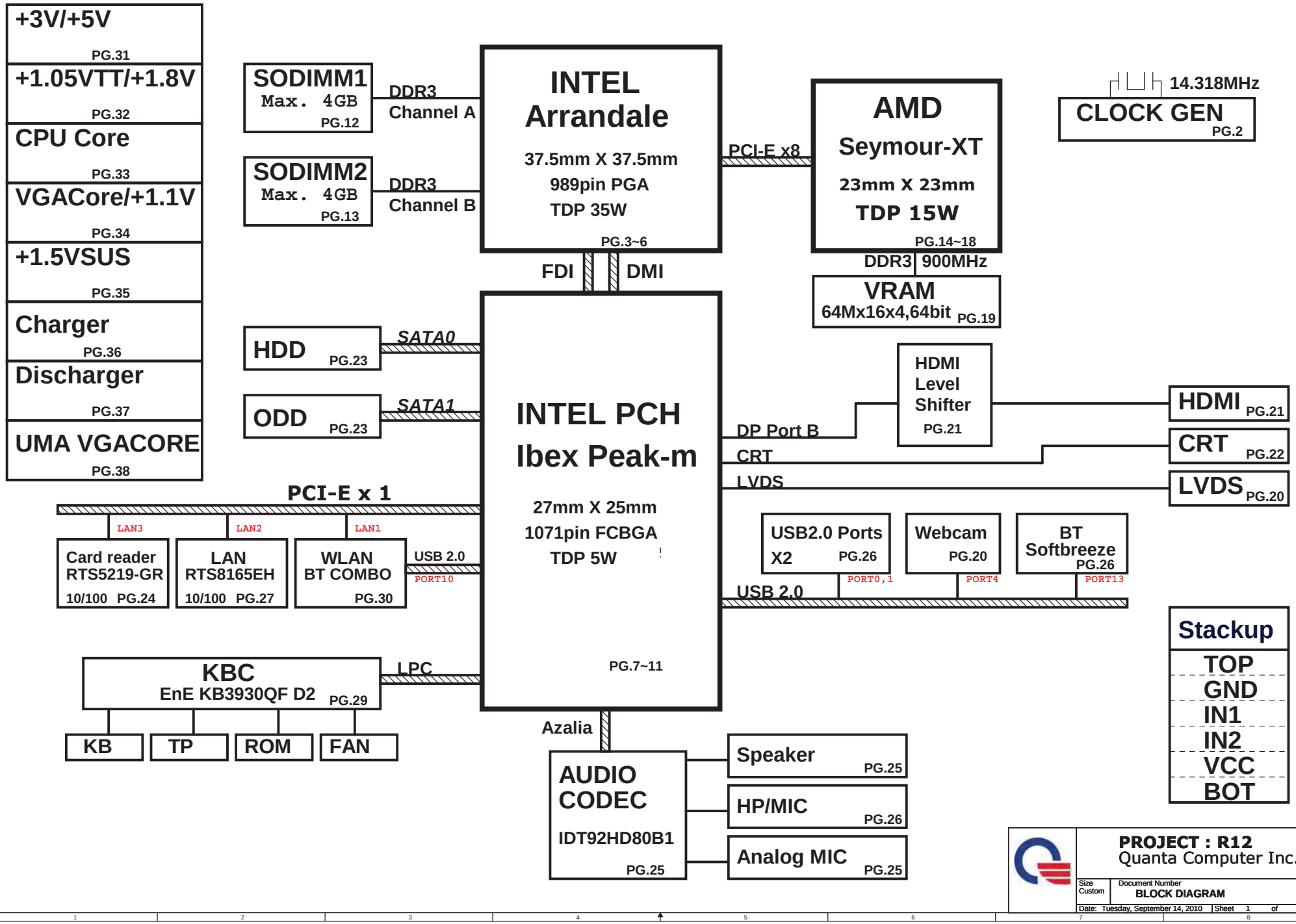
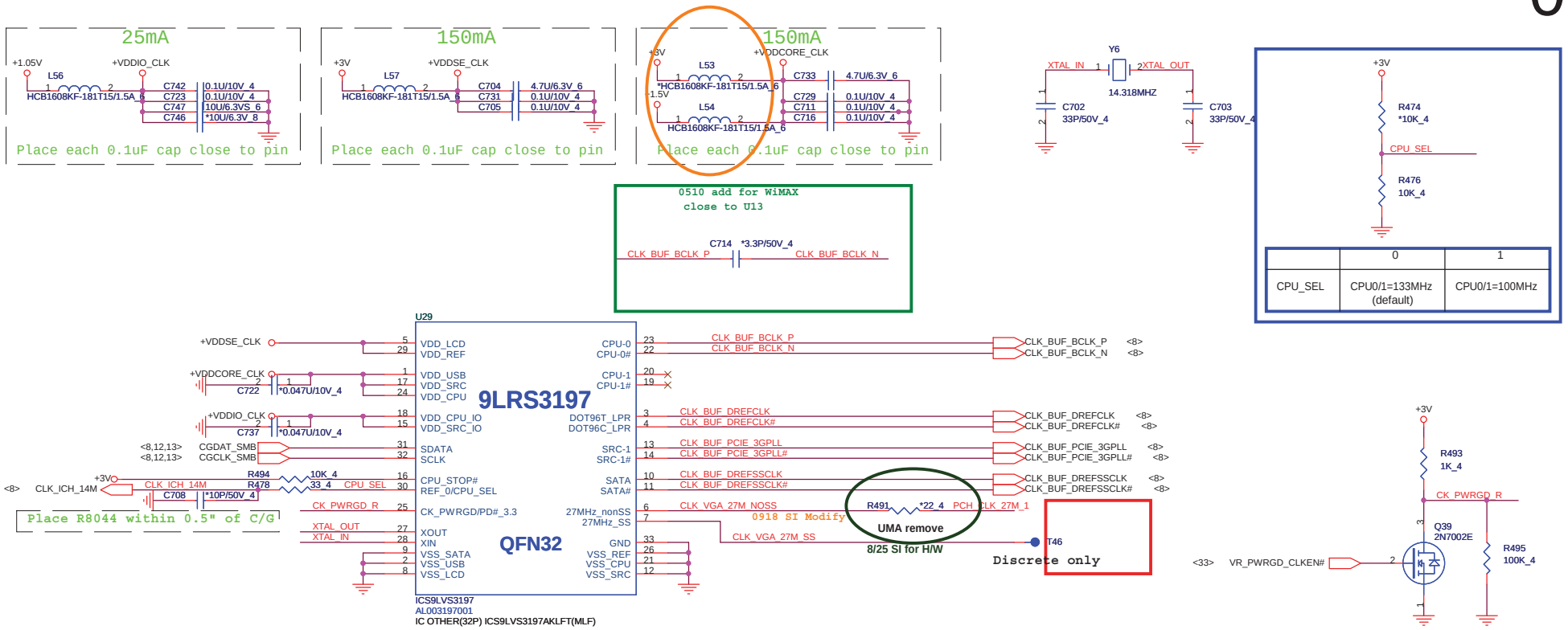
R12 INTEL UMA/DISCRETE SYSTEM DIAGRAM



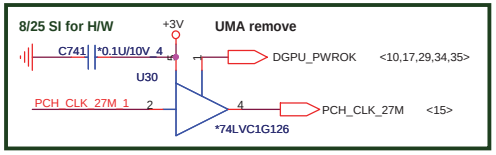
PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Tuesday, September 14, 2010 | Sheet 1 of 39



Vender	Part	Part Number	Part Description
ICS	ICS9LVS3197	AL003197000	IC OTHER(32P) ICS9LVS3197AKLFT(MLF)
Realtek	RTM890N-632	AL000890000	IC OTHER(32P) RTM890N-632-GRT(QFN)
Silego	SLG8LV595VTR	AL000595000	IC OTHER(32P)SLG8LV595VTR(QFN)



+1.05V <7,8,9,11,39>
+1.5V <5,30>
+3V <3,7,8,9,10,11,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36>

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Gen(9LRS3197)	1A

Date: Sunday, September 19, 2010 | Sheet 2 of 39

	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

03

U15A

DMI

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

2.7GT/s data rate

IC,AUB_CFD_rPGA,R1P0

U15B

MISC

THERMAL

CLOCKS

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

UMA remove

for S3 power reduction

SI modify

Use a voltage divider with VDDQ (1.5 V) rail ON in S3) and resistor combination of 1.5K ±1% (to VDDQ)/750±1% (to GND) to convert to processor VTT level.

JTAG MAPPING

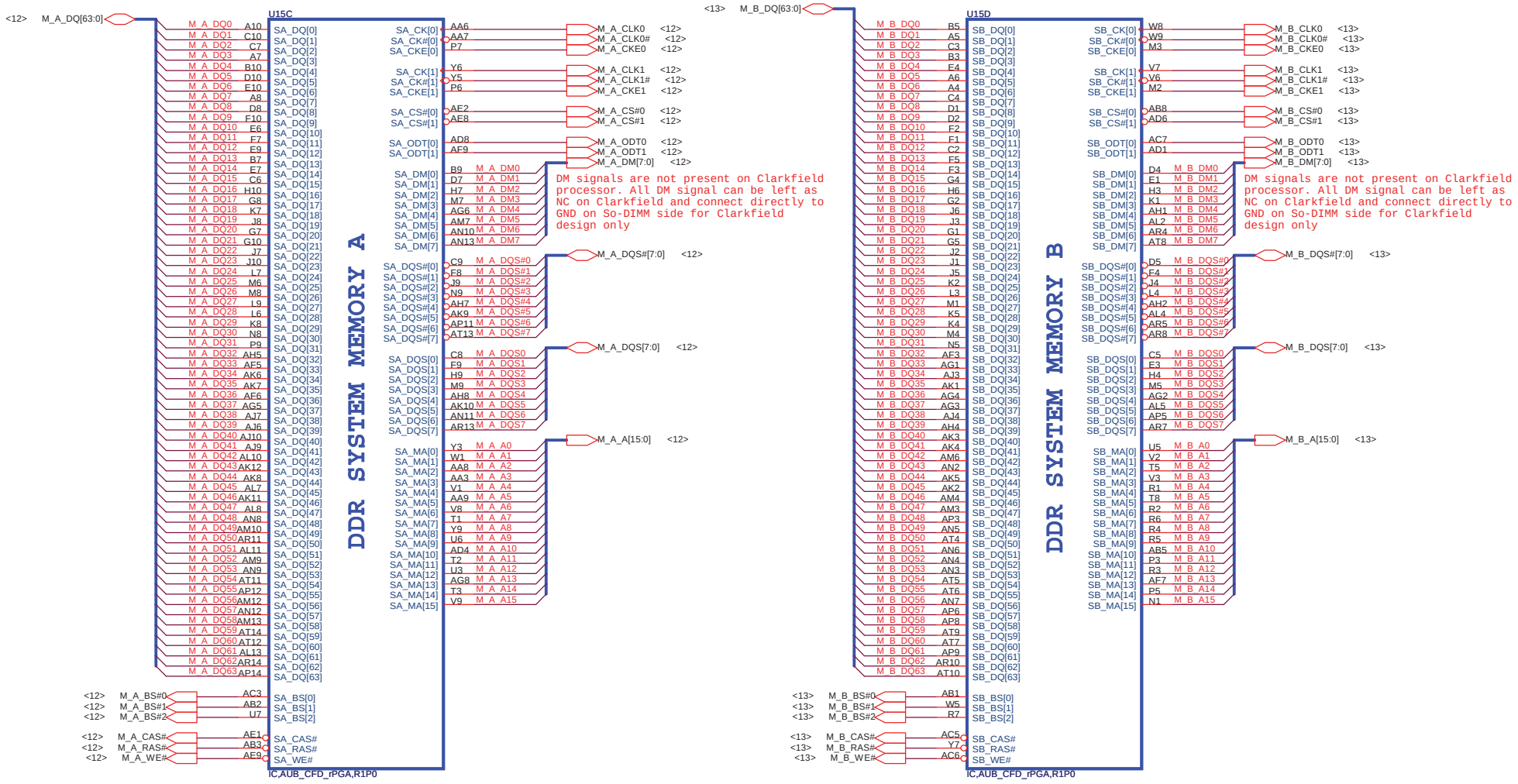
Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 1/4(HOST&PEX)	1A

Date: Sunday, September 19, 2010 Sheet 3 of 39

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



18A

	DIS	UMA
Rc	NA	4.7K
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA

U15F

POWER

CPU CORE SUPPLY

1.1V RAIL POWER

CPU VIDS

SENSE LINES

IC,AUB_CFD_rPGA,R1P0

8/25 SI for H/W.

UMA only

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

	DIS	UMA
Ra	0 ohm	NA

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

U15G

POWER

GRAPHICS

SENSE LINES

GRAPHICS VIDs

DDR3 - 1.5V RAILS

PDI

PEG & DMI

1.1V

1.8V

2A

for S3 power reduction

SI modify

AON7410

Q33

Q34 2N7002E

40mile routing

0510 add for WiMAX

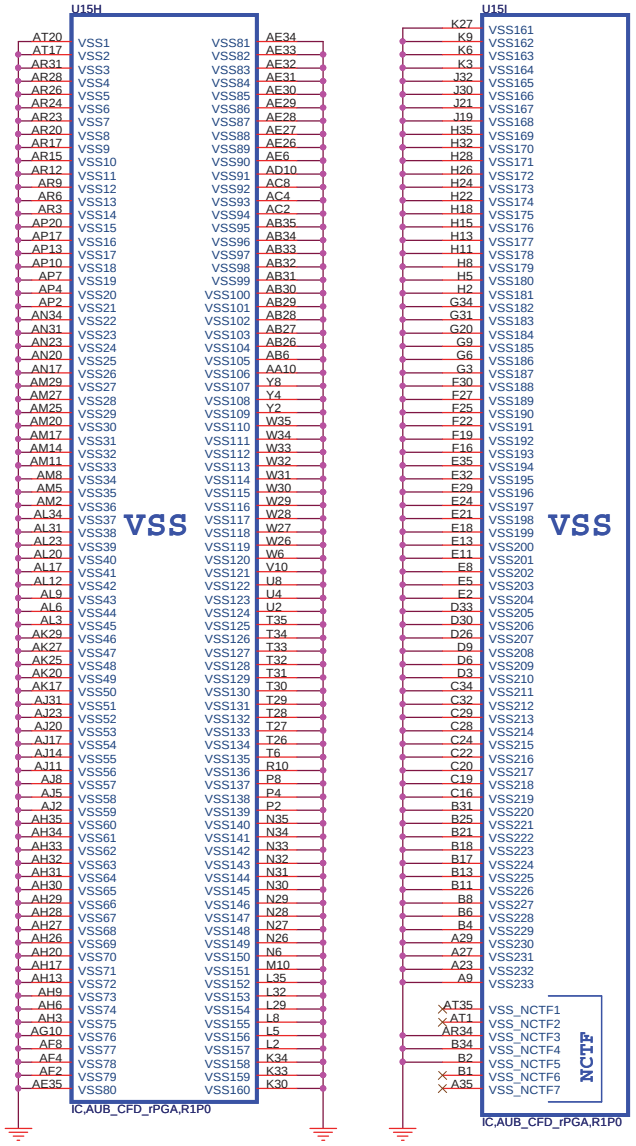
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

PROJECT : R12
Quanta Computer Inc.

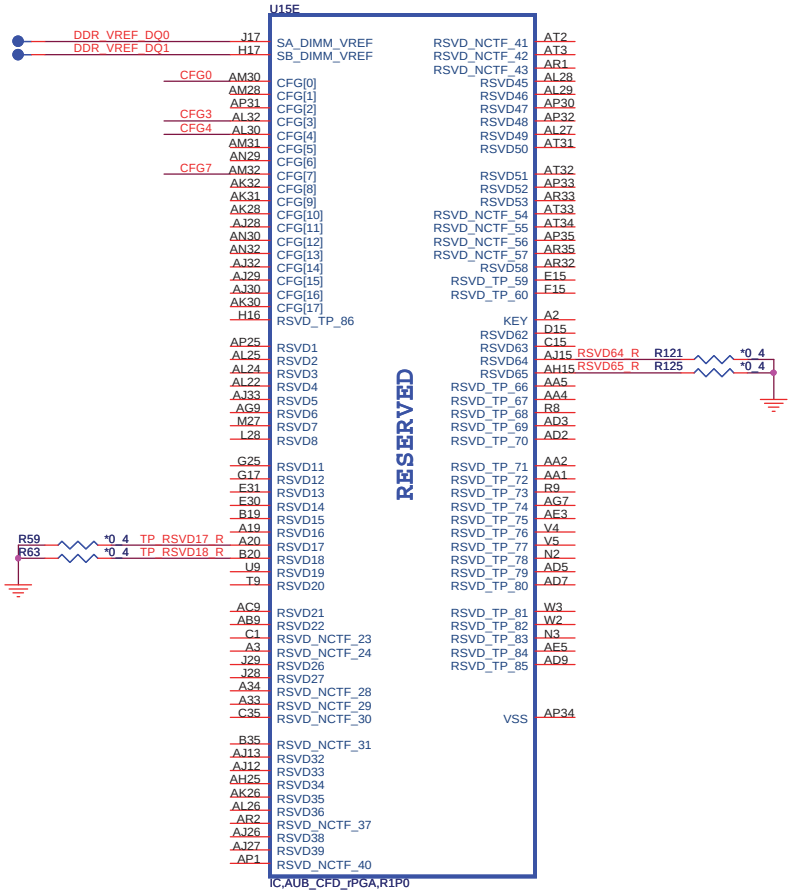
Size	Document Number	Rev
Custom	PROCESSER 3/4(POWER)	1A

Date: Sunday, September 19, 2010 | Sheet 5 of 39

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



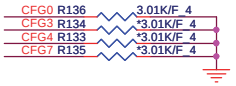
AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

For Discrete only



CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 4/4 (GND)	1A
Date: Sunday, September 19, 2010	Sheet 6 of 39	

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U24A

Ibex-M 1 OF 10

RTC
RTCX1 B13
RTCX2 D13
RTCRST# C14
SRTCRST# D17
INTRUDER# A16
INTVRMEN A14

LPC
FWH0 / LAD0 D33
FWH1 / LAD1 B33
FWH2 / LAD2 C32
FWH3 / LAD3 A32
FWH4 / LFRAME# C34
LDRQ0# A34
(+3V) LDRQ1# / GPIO23 F34
SERIRQ AB9

IHDA
HDA_BCLK A30
HDA_SYNC D29
SPKR P1
HDA_RST# C30
HDA_SDIN0 G30
HDA_SDIN1 F30
HDA_SDIN2 E32
HDA_SDIN3 F32
HDA_SDO B29
HDA_DOCK_EN# / GPIO33 (+3V) H32
HDA_DOCK_RST# / GPIO13 (+3V_S5) J30

JTAG
JTAG_TCK M3
JTAG_TMS K3
JTAG_TDI K1
JTAG_TDO J2
TRST# J4

SPI
SPI_CLK BA2
SPI_CS0# AV3
SPI_CS1# AY3
SPI_MOSI AY1
SPI_MISO AV1

SATA
SATA0RXN AK7
SATA0RXP AK6
SATA0TXN AK11
SATA0TXP AK9
SATA1RXN AH6
SATA1RXP AH5
SATA1TXN AH9
SATA1TXP AH8
SATA2RXN AF11
SATA2RXP AF9
SATA2TXN AF7
SATA2TXP AF6
SATA3RXN AH3
SATA3RXP AH1
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN AD9
SATA4RXP AD8
SATA4TXN AD6
SATA4TXP AD5
SATA5RXN AD3
SATA5RXP AD1
SATA5TXN AB3
SATA5TXP AB1
SATAICOMPO AF16
SATAICOMPI AF15
SATALED# T3
(+3V) SATA0GP / GPIO21
(+3V_S5) SATA1GP / GPIO19 Y9 V1

HDD
SATA_RXN0 SATA_RXP0 SATA_TXN0 SATA_TXP0
ODD
SATA_RXN4 SATA_RXP4 SATA_TXN4 SATA_TXP4

IbexPeak-M_Rev1_0

C663 18P/50V_4
Y4 32.768KHZ
R444 10M_4
C665 18P/50V_4
RTC_X1
RTC_X2
+RTC_CELL
R445 330K_6 PCH_INVRMEN
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
<10,25> ACZ_SPKR
<25> ACZ_SDIN0
ACZ_SDOUT
<10,29> GPIO33_E
R249 *0_4 PCH_GPIO33_R
TP12 PCH_JTAG_TCK
TP10 PCH_JTAG_TMS
TP9 PCH_JTAG_TDI
TP8 PCH_JTAG_TDO
TP1 PCH_JTAG_RST#
must add test point.
SPI_CLK_R
SPI_CS0#_R
TP13 SPI_CS1#
SPI_SI_R
SPI_SO
R230 10K_4 +3V SERIRQ <29>
LAD0 LAD1 LAD2 LAD3 LFRAME# <29,30>
SATA_RXN0 <23> SATA_RXP0 <23> SATA_TXN0 <23> SATA_TXP0 <23>
SATA_RXN4 <23> SATA_RXP4 <23> SATA_TXN4 <23> SATA_TXP4 <23>
SATA_COMP R237 37.4/F_4 +1.05V
SATA_LED# <28>
SATA_DET0#
SATA_DET1#
R409 *0_4 ODD_PRSNT# <23>

IBEX PEAK-M (LVDS,DDI)

UMA CRT,LVDS&HDMI signals

U24D

Ibex-M 4 OF 10

LVDS--A
L_BKLTEN T48
L_VDD_EN T47
L_BKLTCTL Y48
L_DDC_CLK AB48
L_DDC_DATA Y45
L_CTRL_CLK AB46
L_CTRL_DATA V48
LVD_IBG AB39
LVD_VBG AP41
LVD_VREFH AT43
LVD_VREFL AT42
LVDSA_CLK# AV53
LVDSA_CLK AV51
LVDSA_DATA#0 BB47
LVDSA_DATA#1 BA52
LVDSA_DATA#2 AY48
LVDSA_DATA#3 AV47
LVDSA_DATA0 BB48
LVDSA_DATA1 BA50
LVDSA_DATA2 AY49
LVDSA_DATA3 AV48

LVDS--B
LVDSB_CLK# AP48
LVDSB_CLK AP47
LVDSB_DATA#0 AY53
LVDSB_DATA#1 AT49
LVDSB_DATA#2 AU52
LVDSB_DATA#3 AT53
LVDSB_DATA0 AY51
LVDSB_DATA1 AT48
LVDSB_DATA2 AU50
LVDSB_DATA3 AT51

CRT
CRT_BLUE AA52
CRT_GREEN AB53
CRT_RED AD53
CRT_DDC_CLK V51
CRT_DDC_DATA V53
CRT_HSYNC Y53
CRT_VSYNC Y51
DAC_IREF AD48
CRT_IRTN AB51

SDVO
SDVO_TVCLKINN BJ46
SDVO_TVCLKINP BG46
SDVO_STALLN BJ48
SDVO_STALLP BG48
SDVO_INTN BF45
SDVO_INTP BH45
SDVO_CTRLCLK T51 DPB_CTRL_CLK
SDVO_CTRLDATA T53 DPB_CTRL_DATA

Digital Display Interface

DISPLAY PORT B
DDPB_AUXN BG44
DDPB_AUXP BJ44
DDPB_HPD AU38 DPB_HPD_Q
DDPB_0N BD42 DPB_LANE0_N
DDPB_0P BC42 DPB_LANE0_P
DDPB_1N BJ42 DPB_LANE1_N
DDPB_1P BG42 DPB_LANE1_P
DDPB_2N BB40 DPB_LANE2_N
DDPB_2P BA40 DPB_LANE2_P
DDPB_3N AW38 DPB_LANE3_N
DDPB_3P BA38 DPB_LANE3_P

DISPLAY PORT C
DDPC_CTRLCLK Y49
DDPC_CTRLDATA AB49
DDPC_AUXN BE44
DDPC_AUXP BD44
DDPC_HPD AV40
DDPC_0N BE40
DDPC_0P BD40
DDPC_1N BF41
DDPC_1P BH41
DDPC_2N BD38
DDPC_2P BC38
DDPC_3N BB36
DDPC_3P BA36

DISPLAY PORT D
DDPD_CTRLCLK U50
DDPD_CTRLDATA U52
DDPD_AUXN BC46
DDPD_AUXP BD46
DDPD_HPD AT38
DDPD_0N BJ40
DDPD_0P BG40
DDPD_1N BJ38
DDPD_1P BG38
DDPD_2N BF37
DDPD_2P BH37
DDPD_3N BE36
DDPD_3P BD36

TP16
TP15

HDD0 (SATA3 6.0Gb/s)
<20> LVDS_BLON
<20> DISP_ON
<20> DPST_PWM
<20> EDIDCLK
<20> EDIDDATA
R266 10K_4 L_CTRL_CLK
R269 10K_4 L_CTRL_DATA
+3V
R259 2.37K/F_4 LVDS_IBG
LVDS_VBG
TP7
<20> TXLCLKOUT-
<20> TXLCLKOUT+
<20> TXLOUT0-
<20> TXLOUT1-
<20> TXLOUT2-
<20> TXLOUT0+
<20> TXLOUT1+
<20> TXLOUT2+
<20> TXUCLKOUT-
<20> TXUCLKOUT+
<20> TXUOUT0-
<20> TXUOUT1-
<20> TXUOUT2-
<20> TXUOUT0+
<20> TXUOUT1+
<20> TXUOUT2+
<22> CRT_B
<22> CRT_G
<22> CRT_R
R455 150/F_4
R457 150/F_4
R456 150/F_4
<22> DDCCLK
<22> DDCDATA
<22> HSYNC_COM
<22> VSYNC_COM
R272 1K/F_4 DAC_IREF

IbexPeak-M_Rev1_0

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

+3V
R411 10K_4 SATA_LED#
R223 10K_4 SATA_DET0#
R410 10K_4 SATA_DET1#
R251 *10K_4 GPIO33_E

R433 51_4 PCH_JTAG_TCK

+3VS5
For ES1 ONLY.NI for ES2.
R415 200_4
R413 200_4
R416 200_4
R193 20K/F_4
PCH_JTAG_RST#
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TMS
For ES1 ONLY.NI for ES2.
R414 100_4
R412 100_4
R436 100_4
R197 10K_4

Part
Part Number
Part Description

UMA HDMI signals

DPB_CTRL_CLK R459 0_4 SDVO_CLK <21>
DPB_CTRL_DATA R458 0_4 SDVO_DATA <21>
DPB_LANE0_N C474 0.1U/10V_4 IN_D2# <21>
DPB_LANE0_P C478 0.1U/10V_4 IN_D2 <21>
DPB_LANE1_N C471 0.1U/10V_4 IN_D1# <21>
DPB_LANE1_P C472 0.1U/10V_4 IN_D1 <21>
DPB_LANE2_N C480 0.1U/10V_4 IN_D0# <21>
DPB_LANE2_P C482 0.1U/10V_4 IN_D0 <21>
DPB_LANE3_N C465 0.1U/10V_4 IN_CLK# <21>
DPB_LANE3_P C467 0.1U/10V_4 IN_CLK <21>

+3V
Q18 *2N7002K
DPB_HPD_Q
HDMI_HPD_CON <21>
R287 100K_4
R286 0_4

For AUDIO

<25> ACZ_RST#_AUDIO R452 33_4 ACZ_RST#
<25> ACZ_SDOUT_AUDIO R450 33_4 ACZ_SDOUT
C666 *10P/50V_4
<25> ACZ_SYNC_AUDIO R451 33_4 ACZ_SYNC
C667 *10P/50V_4
<25> BIT_CLK_AUDIO R453 33_4 ACZ_BCLK
C464 *10P/50V_4

For MDC

RTC

1mA

+RTC_CELL
+3VPCU
RB500V-40 CR1
+3VRTC_2
RB500V-40 CR2
C438 1U/6.3V_4
R242 20K/F_4 RTC_RST#
C428 1U/6.3V_4
R241 20K/F_4 SRTC_RST#
C429 1U/6.3V_4
R243 1M_4 SM_INTRUDER#
CN24
R254 1K_4 +3VRTC_1
BAT_CONN
DFWF02MS032
50273-0027N-001-2P-L
8/25 SI for M/E.

4M byte SPI ROM

+3V
U22
VDD CE# SCK SI HOLD# SO VSS WP#
SPI_HOLD# R422 10K_4
C659 0.1U/10V_4
SPI_CS0#_R
SPI_CLK_R
SPI_SI_R
SPI_SO
SPI_WP# R440 10K_4 +3V
W25Q32BVSSIG
AKE391P0N00
IC FLASH(8P) W25Q32BVSSIG(SOIC)

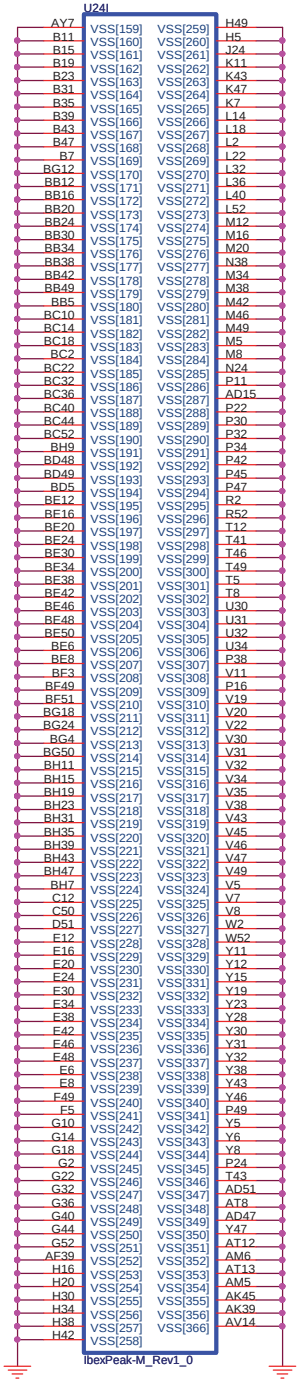
<2,8,9,11,39> +1.05V
<2,3,8,9,10,11,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36> +3V
<20,28,29,31,37> +3VPCU

Vender
Socket DG008000031
EON - EN25F32-100HIP
AKE39FN0Q00 IC FLASH(8P) EN25F32-100HIP (SOIC)
WINBOND - W25Q32BVSSIG
AKE391P0N00 IC FLASH(8P) W25Q32BVSSIG(SOIC)

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/5 (SATA,HDA,LPC)	1A
Date: Sunday, September 19, 2010	Sheet 7 of 39	

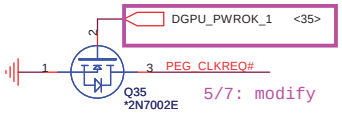
IBEX PEAK-M (GND)

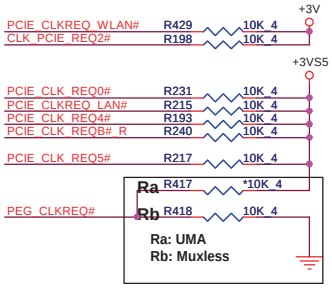


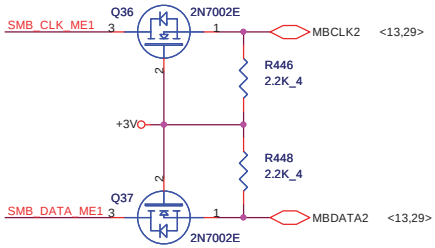
IBEX PEAK-M (PCI-E,SMBUS,CLK)

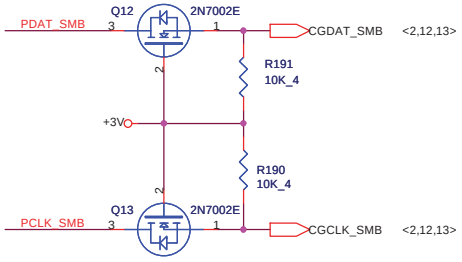
08

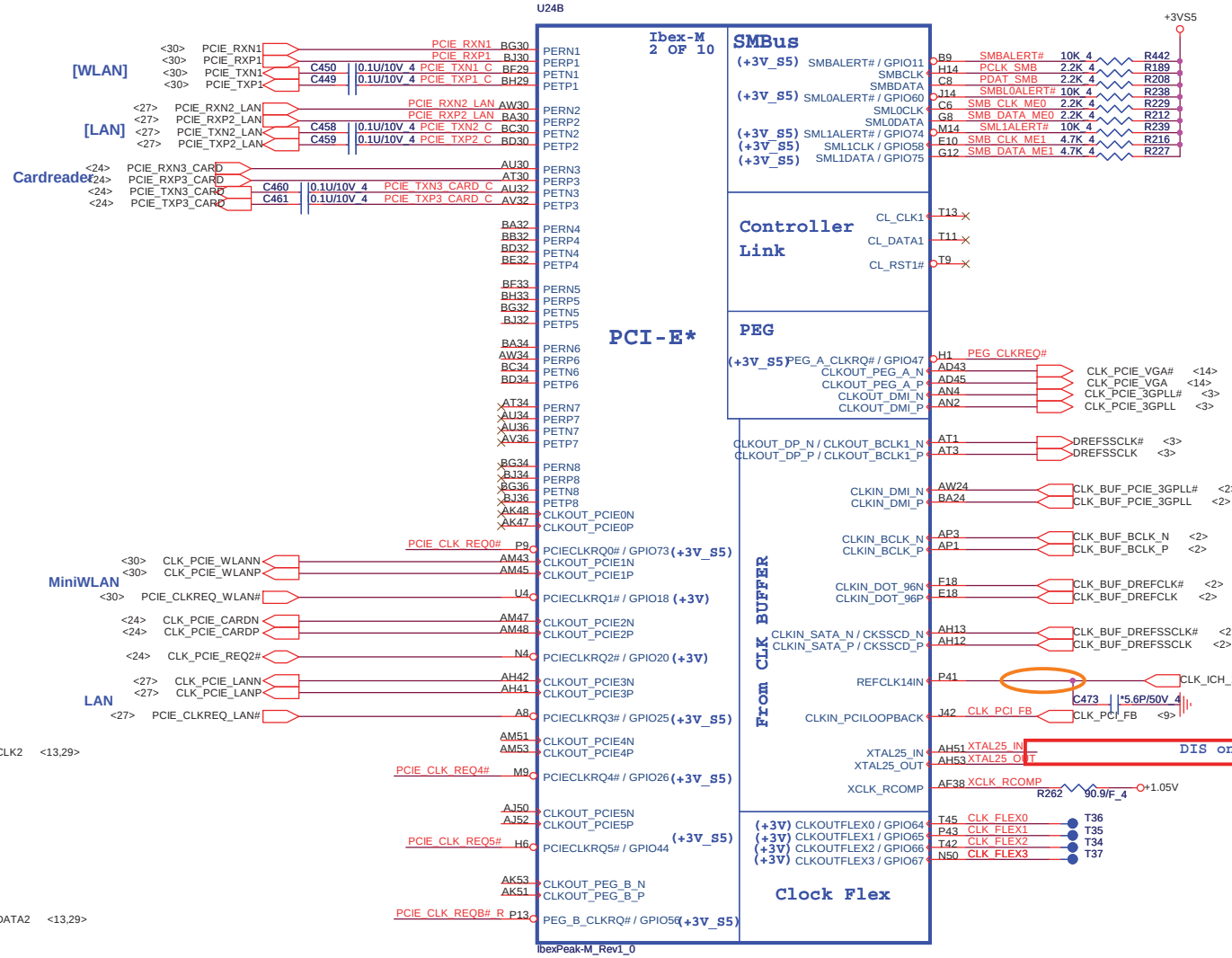
PEG Clock detect (SG only)

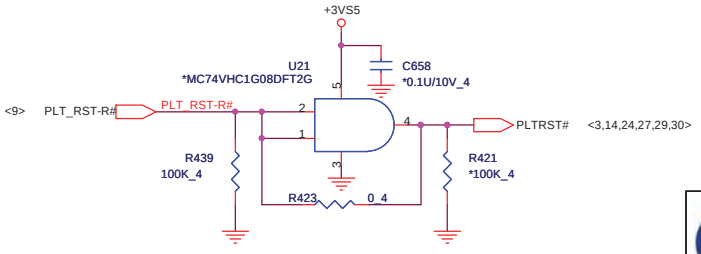


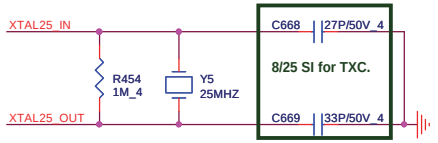










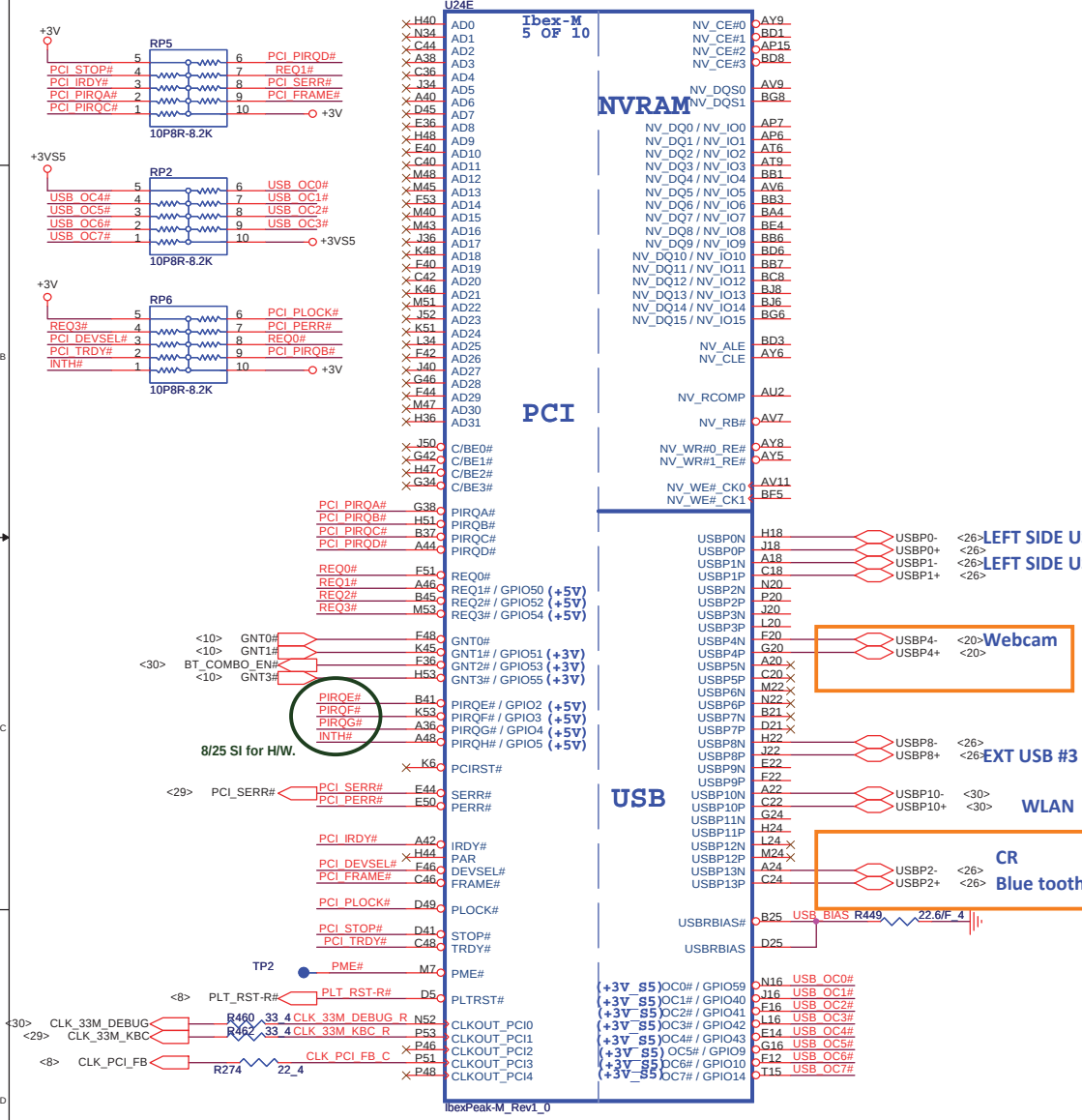


PROJECT : R12
Quanta Computer Inc.

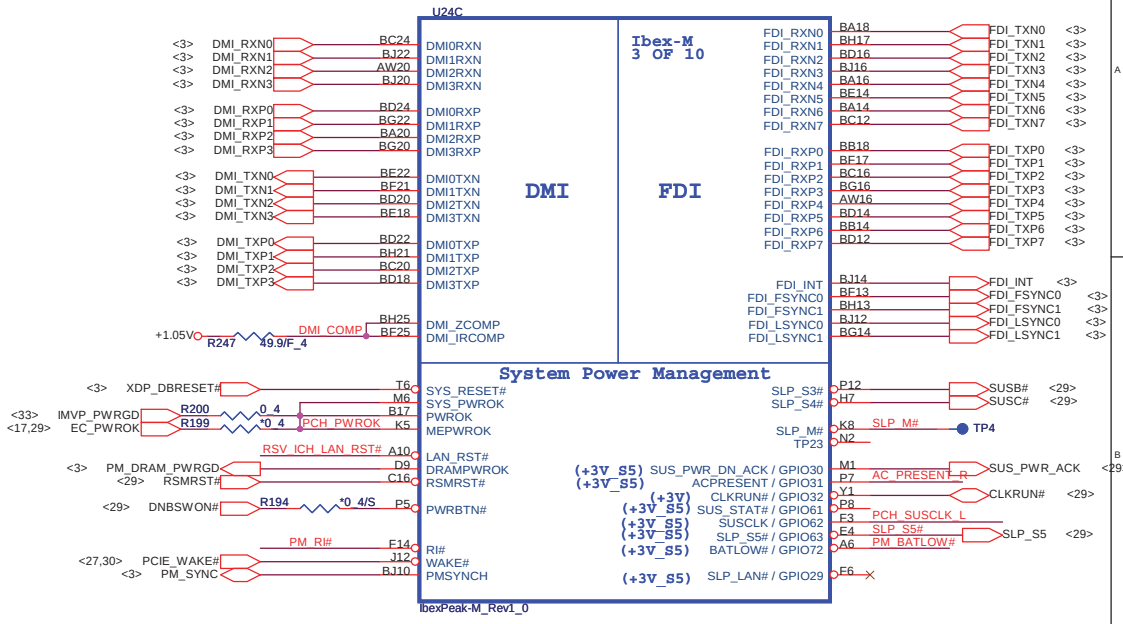
Size	Document Number	Rev
Custom	PCH 2/5 (PCIE, SMBUS, CK)	1A

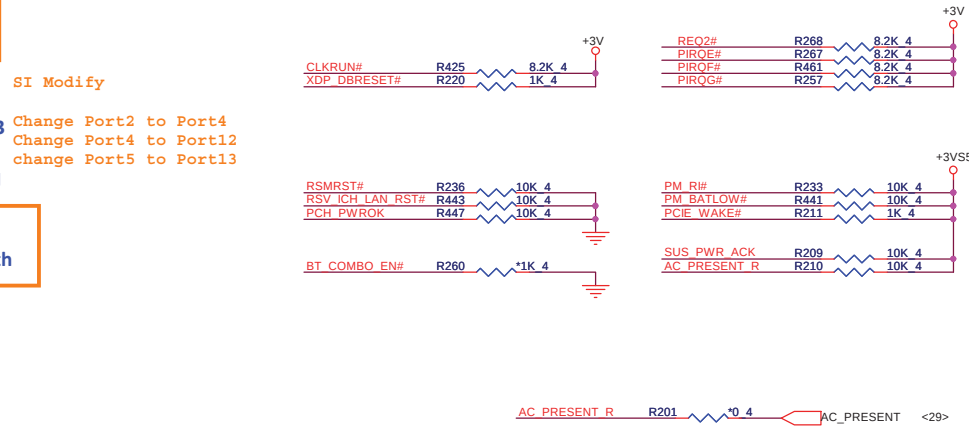
Date: Sunday, September 19, 2010 Sheet 8 of 39

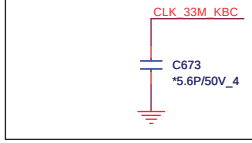
IBEX PEAK-M (PCI,USB,NVRAM)

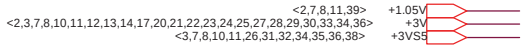


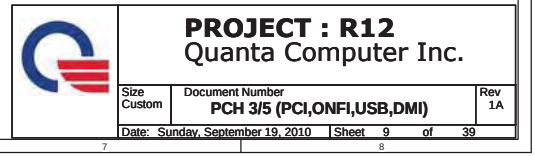
IBEX PEAK-M (DMI,FDI,GPIO)



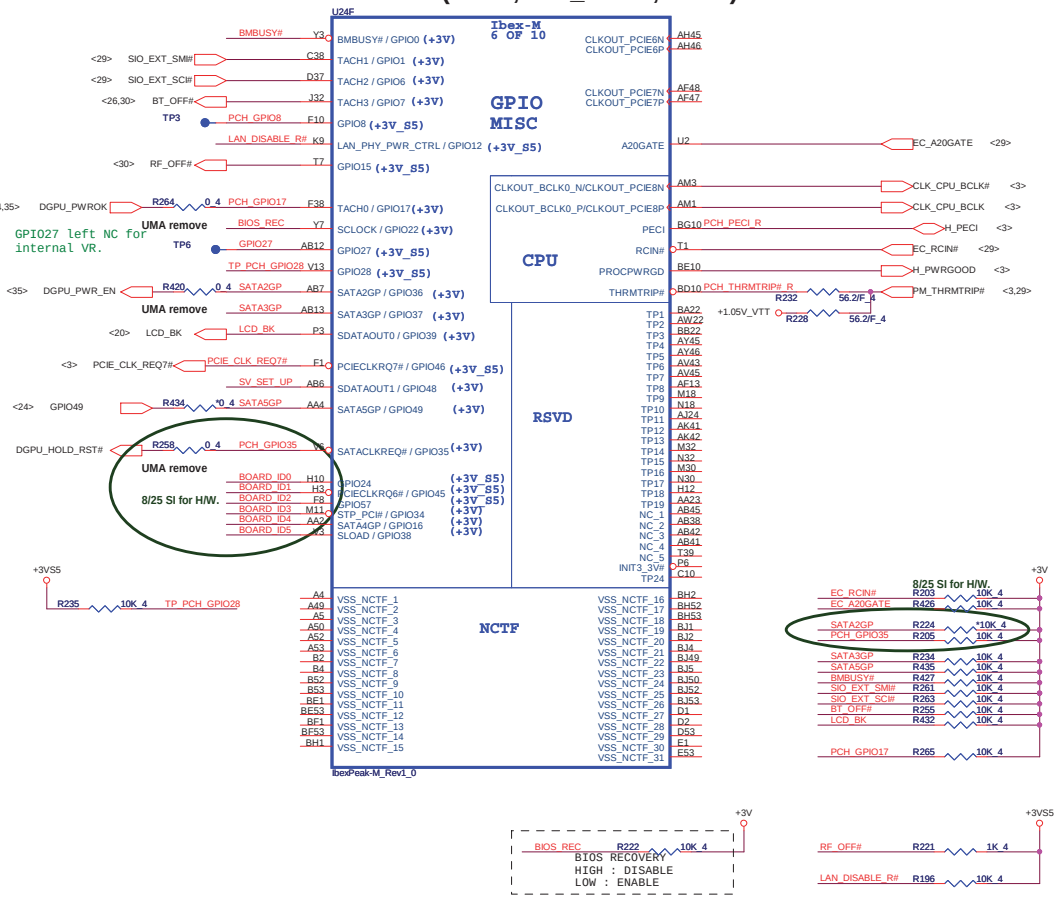




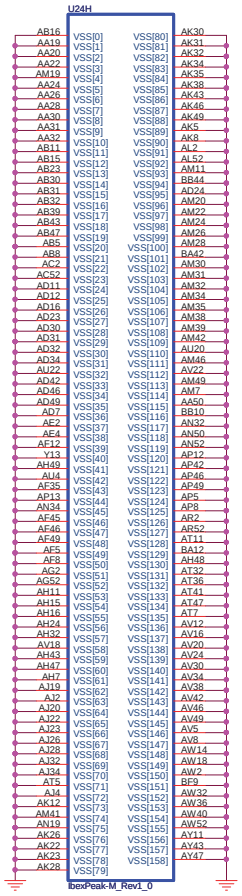


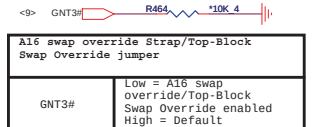


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)





A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

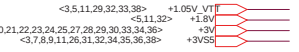
SV_SET_UP	1-X High = Strong (Default)

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

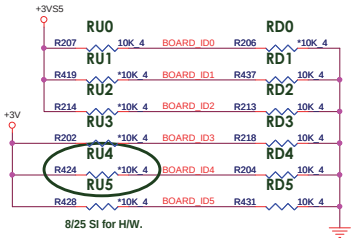
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap



R12 MB P/N	ID0	ID1	ID2	ID3	ID4	ID5
UMA						
31R12MB0000 (PIM) 31R12MB0010 (PDT)	0 0	0 0	0 0	0 0	0 0	0 0
Seymour XT Hynix 512						
31R12MB0020 (PIM) 31R12MB0030 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0
Samsung 512						
31R12MB0040 (PIM) 31R12MB0050 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0
Hynix 1G						
31R12MB0060 (PIM) 31R12MB0070 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0
Samsung 1G						
31R12MB0080 (PIM) 31R12MB0090 (PDT)	1 1	0 0	0 0	0 0	0 0	0 0

Board ID	ID0 GPIO24	ID1 GPIO45	ID2 GPIO57	ID3 GPIO34	ID4 GPIO35	ID5 GPIO38
UMA/DIS	0=UMA 1=Dis.					
Reserve		0=No 1=Yes				
Reserve			0=No 1=Yes			
Reserve				0=No 1=Yes		
Reserve					0=No 1=Yes	
Reserve						0=No 1=Yes



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/5 (GPIO & Strap)	1A

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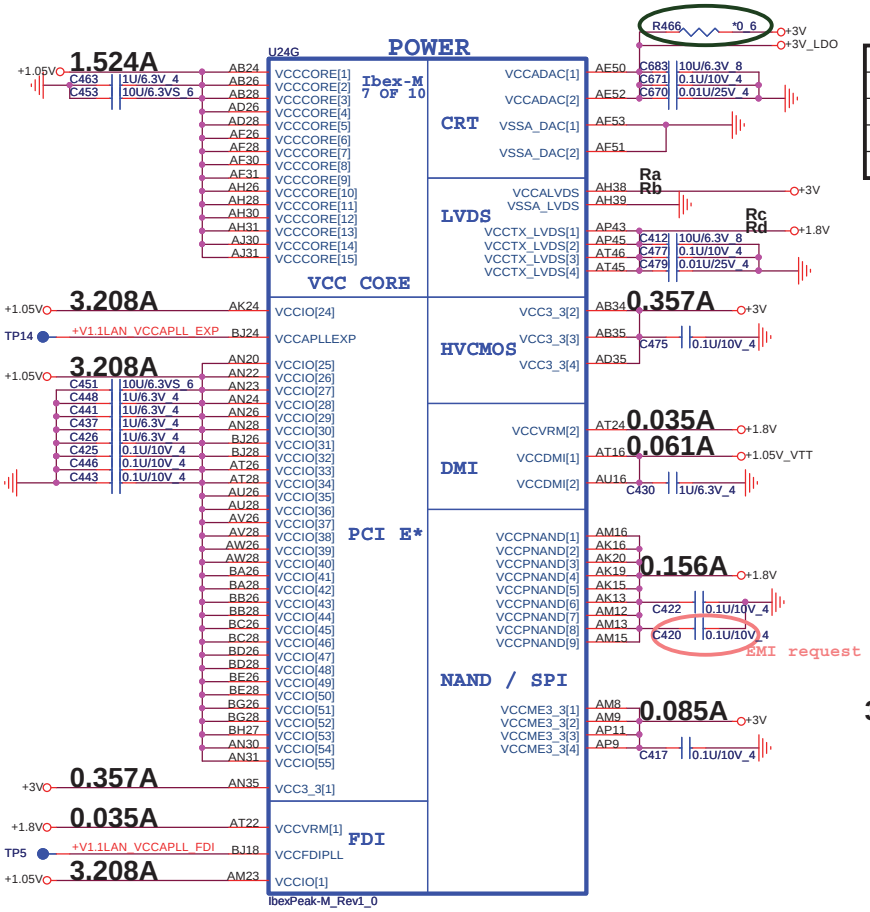
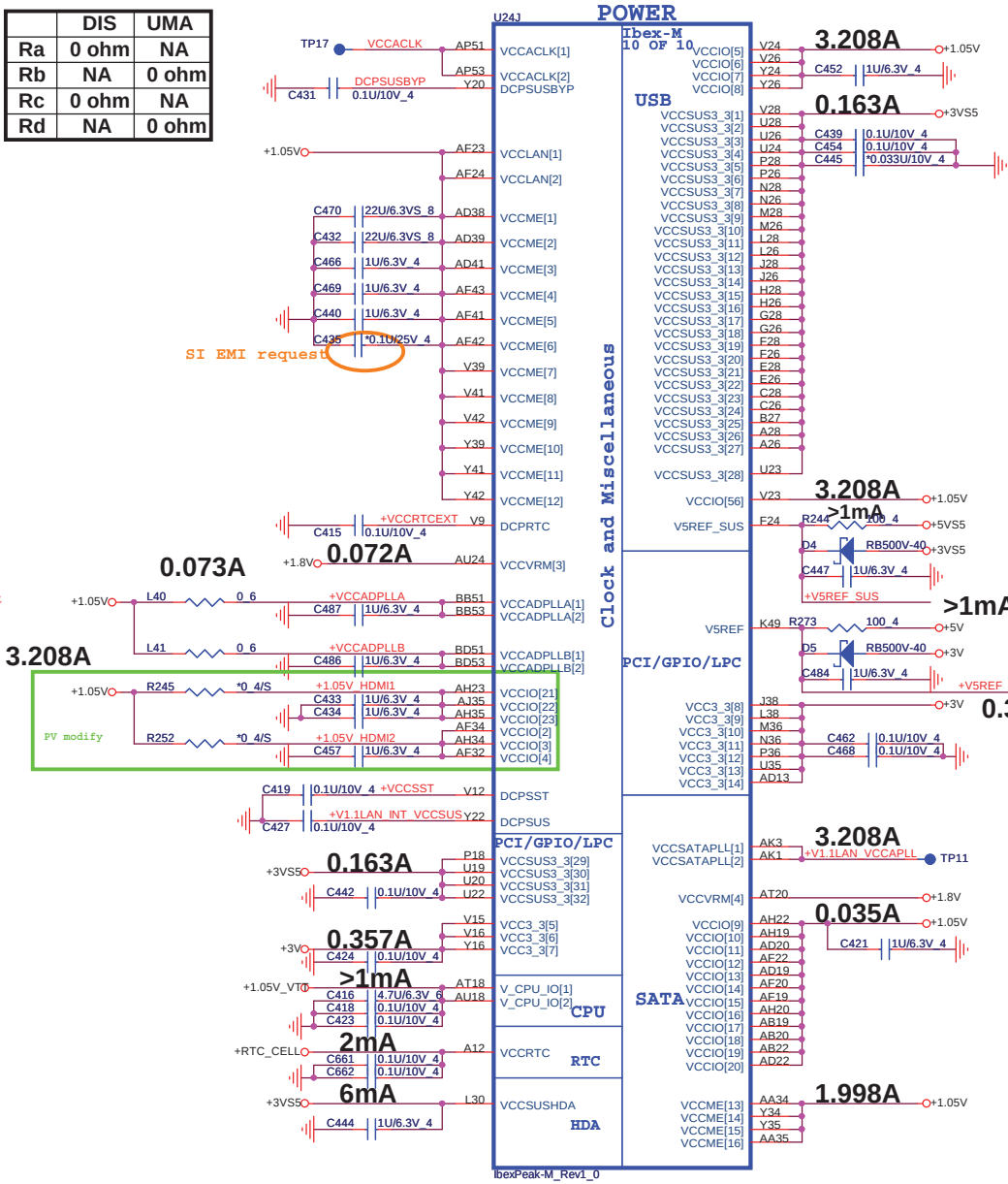
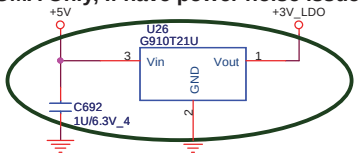
8/25 SI modify
Uninstall on UMA
Install on DIS

	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm





UMA Only, If have power noise issue then stuff it.



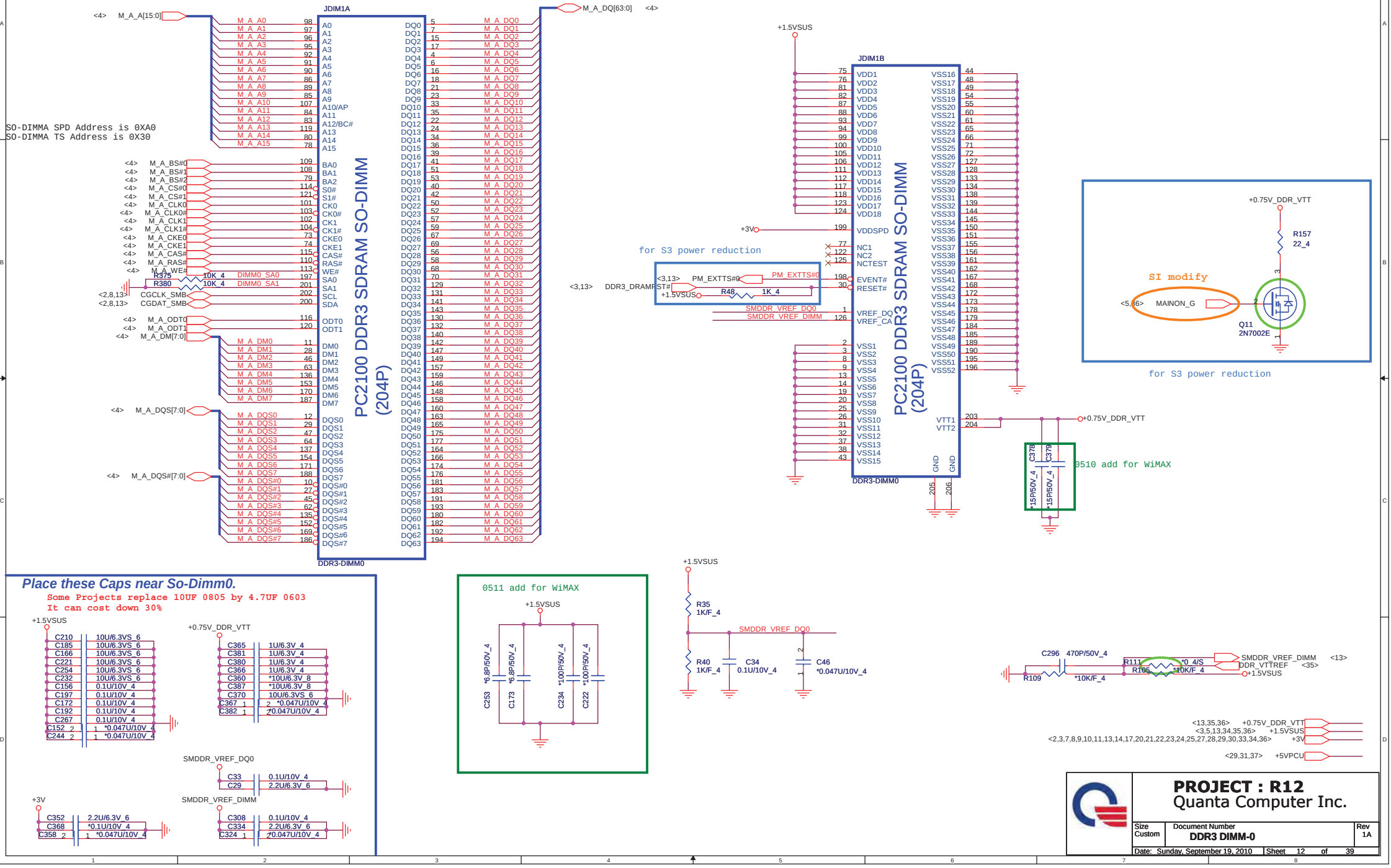
8/25 SI modify
Install LDO when UMA

<2,7,8,9,39> +1.05V
<3,5,10,29,32,33,38> +1.05V_VTT
<5,32> +1.8V
<2,3,7,8,9,10,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36> +3V
<3,7,8,9,10,26,31,32,34,35,36,38> +3VS5
<17,21,22,23,25,28,30,36> +5V
<20,26,31,32,33,34,35,36,38,39> +5VS5

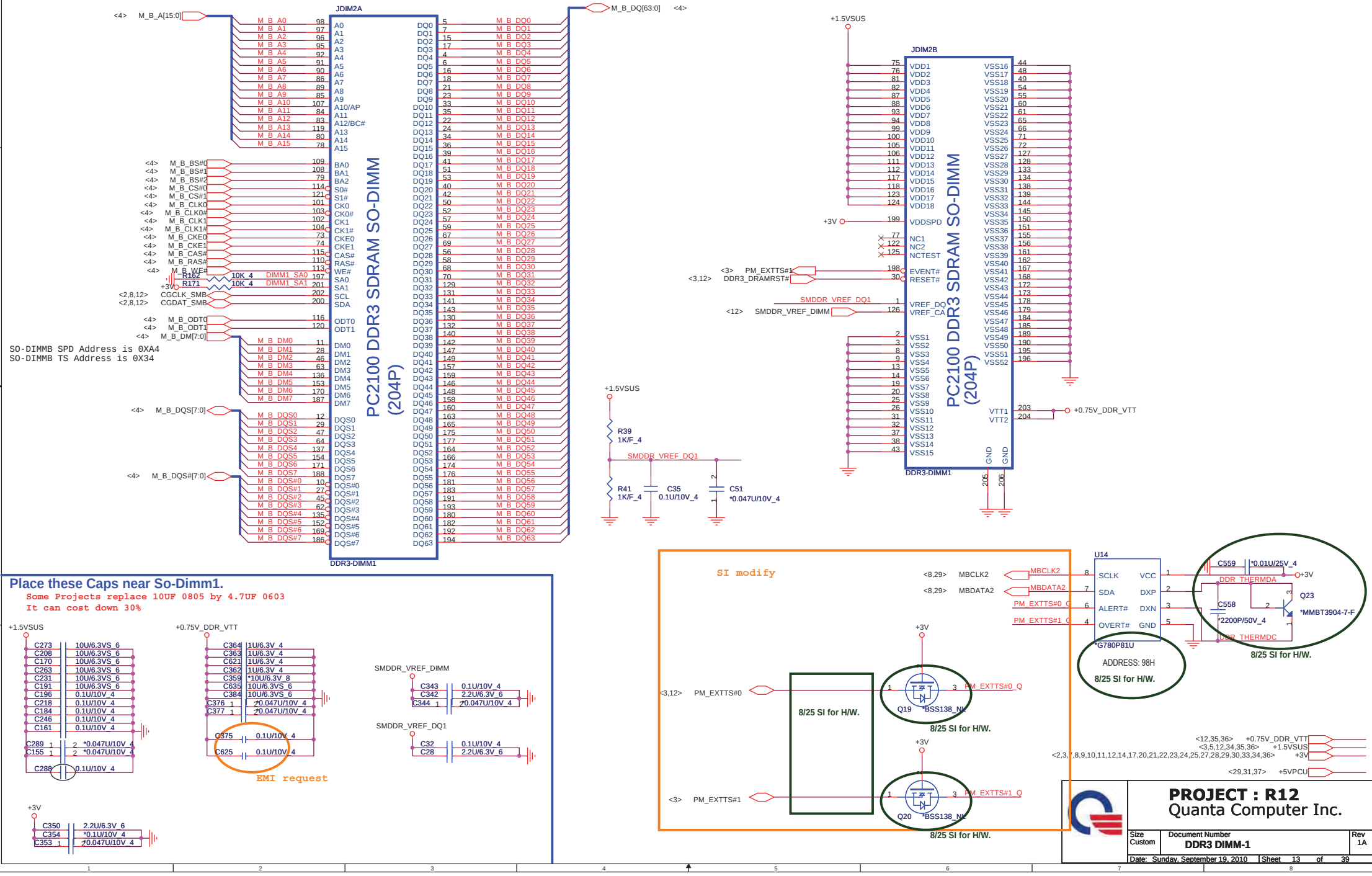
PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	1A

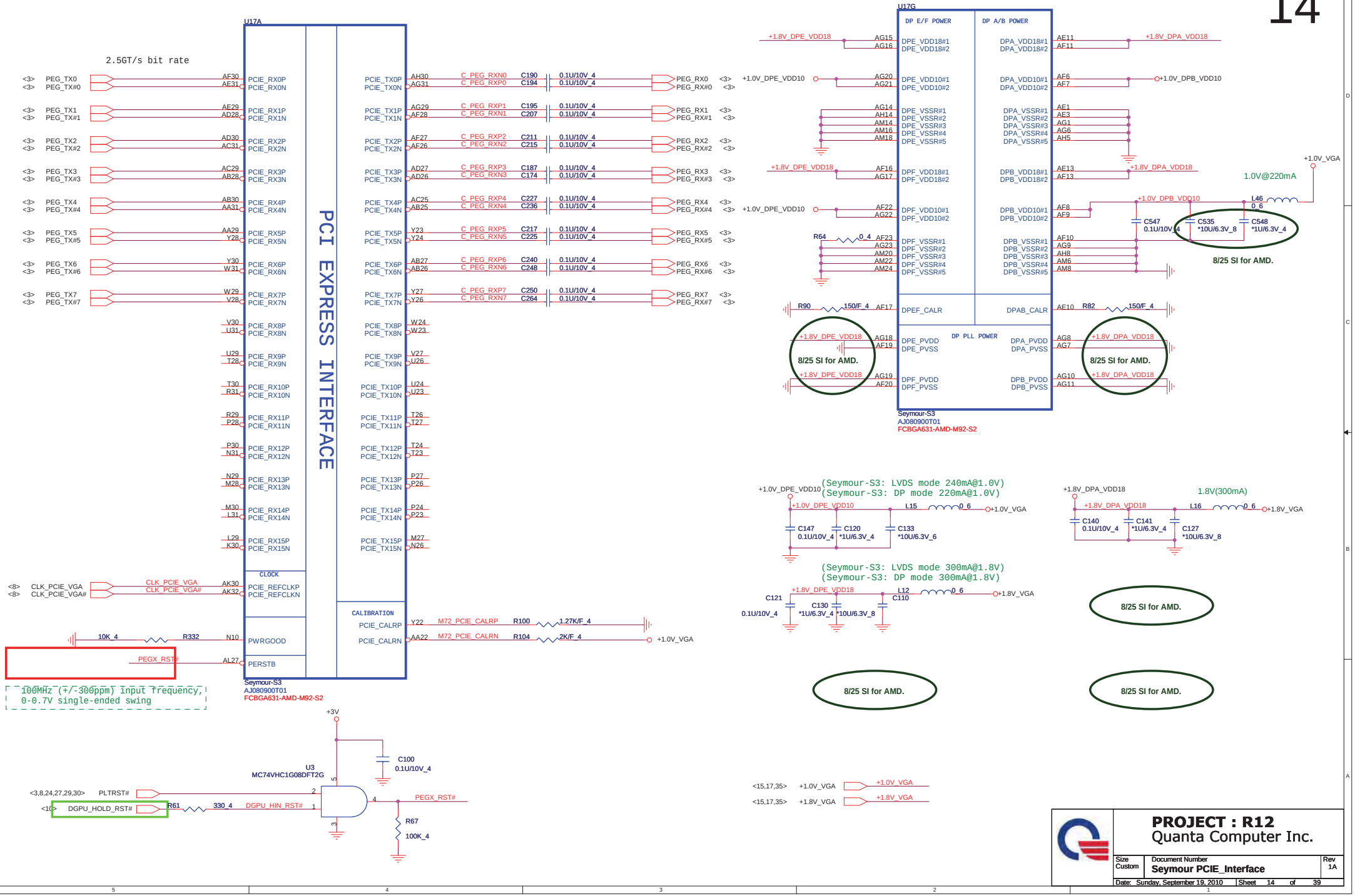
Date: Sunday, September 19, 2010 | Sheet 11 of 39



PROJECT : R12 Quanta Computer Inc.			
Size: Custom	Document Number: DDR3 DIMM-0		Rev: 1A
Date: Sunday, September 19, 2010	Sheet 12 of 39		



PROJECT : R12			
Quanta Computer Inc.			
Size: Custom	Document Number: DDR3 DIMM-1		Rev: 1A
Date: Sunday, September 19, 2010	Sheet 13 of 39		


U17A
PCI EXPRESS INTERFACE
2.5GT/s bit rate
PEG_TX0 PEG_TX#0 PEG_TX1 PEG_TX#1 PEG_TX2 PEG_TX#2 PEG_TX3 PEG_TX#3 PEG_TX4 PEG_TX#4 PEG_TX5 PEG_TX#5 PEG_TX6 PEG_TX#6 PEG_TX7 PEG_TX#7
PCIE_RX0P PCIE_RX0N PCIE_RX1P PCIE_RX1N PCIE_RX2P PCIE_RX2N PCIE_RX3P PCIE_RX3N PCIE_RX4P PCIE_RX4N PCIE_RX5P PCIE_RX5N PCIE_RX6P PCIE_RX6N PCIE_RX7P PCIE_RX7N PCIE_RX8P PCIE_RX8N PCIE_RX9P PCIE_RX9N PCIE_RX10P PCIE_RX10N PCIE_RX11P PCIE_RX11N PCIE_RX12P PCIE_RX12N PCIE_RX13P PCIE_RX13N PCIE_RX14P PCIE_RX14N PCIE_RX15P PCIE_RX15N
PCIE_TX0P PCIE_TX0N PCIE_TX1P PCIE_TX1N PCIE_TX2P PCIE_TX2N PCIE_TX3P PCIE_TX3N PCIE_TX4P PCIE_TX4N PCIE_TX5P PCIE_TX5N PCIE_TX6P PCIE_TX6N PCIE_TX7P PCIE_TX7N PCIE_TX8P PCIE_TX8N PCIE_TX9P PCIE_TX9N PCIE_TX10P PCIE_TX10N PCIE_TX11P PCIE_TX11N PCIE_TX12P PCIE_TX12N PCIE_TX13P PCIE_TX13N PCIE_TX14P PCIE_TX14N PCIE_TX15P PCIE_TX15N
C_PEG_RXN0 C_PEG_RXP0 C_PEG_RXN1 C_PEG_RXP1 C_PEG_RXN2 C_PEG_RXP2 C_PEG_RXN3 C_PEG_RXP3 C_PEG_RXN4 C_PEG_RXP4 C_PEG_RXN5 C_PEG_RXP5 C_PEG_RXN6 C_PEG_RXP6 C_PEG_RXN7 C_PEG_RXP7
C190 C194 C195 C207 C211 C215 C187 C174 C227 C236 C217 C225 C240 C248 C250 C264
0.1U/10V_4
PEG_RX0 PEG_RX#0 PEG_RX1 PEG_RX#1 PEG_RX2 PEG_RX#2 PEG_RX3 PEG_RX#3 PEG_RX4 PEG_RX#4 PEG_RX5 PEG_RX#5 PEG_RX6 PEG_RX#6 PEG_RX7 PEG_RX#7
CLOCK
CLK_PCIE_VGA CLK_PCIE_VGA#
PCIE_REFCLKP PCIE_REFCLKN
PWRGOOD PERSTB
10K_4 R332 PEGX_RST#
100MHz (+/-300ppm) input frequency, 0-0.7V single-ended swing
CALIBRATION
PCIE_CALRP PCIE_CALRN
M72_PCIE_CALRP M72_PCIE_CALRN
R100 1.27K/F_4 R104 2K/F_4
+1.0V_VGA
Seymour-S3
AJ080900T01
FCBGA631-AMD-M92-S2
U17G
DP E/F POWER
DP A/B POWER
+1.8V_DPE_VDD18 +1.0V_DPE_VDD10
DPE_VDD18#1 DPE_VDD18#2 DPE_VDD10#1 DPE_VDD10#2 DPE_VSSR#1 DPE_VSSR#2 DPE_VSSR#3 DPE_VSSR#4 DPE_VSSR#5
DPA_VDD18#1 DPA_VDD18#2 DPA_VDD10#1 DPA_VDD10#2 DPA_VSSR#1 DPA_VSSR#2 DPA_VSSR#3 DPA_VSSR#4 DPA_VSSR#5
+1.8V_DPA_VDD18 +1.0V_DPB_VDD10
DPB_VDD18#1 DPB_VDD18#2 DPB_VDD10#1 DPB_VDD10#2 DPB_VSSR#1 DPB_VSSR#2 DPB_VSSR#3 DPB_VSSR#4 DPB_VSSR#5
DPEF_CALR DPAB_CALR R90 150/F_4 R82 150/F_4
DP PLL POWER
DPE_PVDD DPE_PVSS DPA_PVDD DPA_PVSS DPF_PVDD DPF_PVSS DPB_PVDD DPB_PVSS
8/25 SI for AMD.
1.0V@220mA
+1.0V_VGA
L46 0_6
C547 0.1U/10V_4 C535 *10U/6.3V_8 C548 *1U/6.3V_4
R64 0_4
Seymour-S3
AJ080900T01
FCBGA631-AMD-M92-S2
(Seymour-S3: LVDS mode 240mA@1.0V)
(Seymour-S3: DP mode 220mA@1.0V)
L15 0_6
C147 0.1U/10V_4 C120 *1U/6.3V_4 C133 *10U/6.3V_6
1.8V(300mA)
L16 0_6
C140 0.1U/10V_4 C141 *1U/6.3V_4 C127 *10U/6.3V_8
(Seymour-S3: LVDS mode 300mA@1.8V)
(Seymour-S3: DP mode 300mA@1.8V)
L12 0_6
C121 0.1U/10V_4 C130 *1U/6.3V_4 C110 *10U/6.3V_8
8/25 SI for AMD.
U3
MC74VHC1G08DFT2G
C100 0.1U/10V_4
<3,8,24,27,29,30> PLTRST#
<10> DGPU_HOLD_RST#
R61 330_4 DGPU_HIN_RST#
PEGX_RST#
R67 100K_4
<15,17,35> +1.0V_VGA
<15,17,35> +1.8V_VGA
PROJECT : R12
Quanta Computer Inc.
Size Custom
Document Number
Seymour PCIE_Interface
Rev 1A
Date: Sunday, September 19, 2010
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MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung- E die	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix- Vega die	64*16-800MHZ	H5TQ1G63DFR-12C
0010	Hynix- Vega die	128*16-800MHZ	H5TQ2G63BFR-12C
0011	Samsung- C die	128*16-800MHZ	K4W2G1646C-HC12
0100	Micron	128*16-800MHZ	MT41J128M16HA-125:D
0101	Reserved		
0110	Hynix- Vega die	64*16-900MHZ	H5TQ1G63DFR-11C
0111	Samsung- B die	64*16-900MHZ	K4W1G1646E-HC11
1000	Samsung- G die	64*16-900MHZ	K4W1G1646G-BC11
1001	Reserved		
1010	Hynix- Vega die	128*16-900MHZ	H5TQ2G63BFR-11C
1011	Samsung- C die	128*16-900MHZ	K4W2G1646C-HC11
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111			

GPIO15 GPIO20

Seymour	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	0.95V
H	1	0	1.12V (Default)
TBD	1	1	NA

Access to SCL and SDA is mandatory on BACO designs for debug purposes

GPIO22(ROMCS#) PD without external VBIOS ROM

If no contact this pin to LVDS need pull low

Seymour uninstall Ra to meet AF24 N/C

8/25 SI for H/W.

DAC2 is NC on Seymour

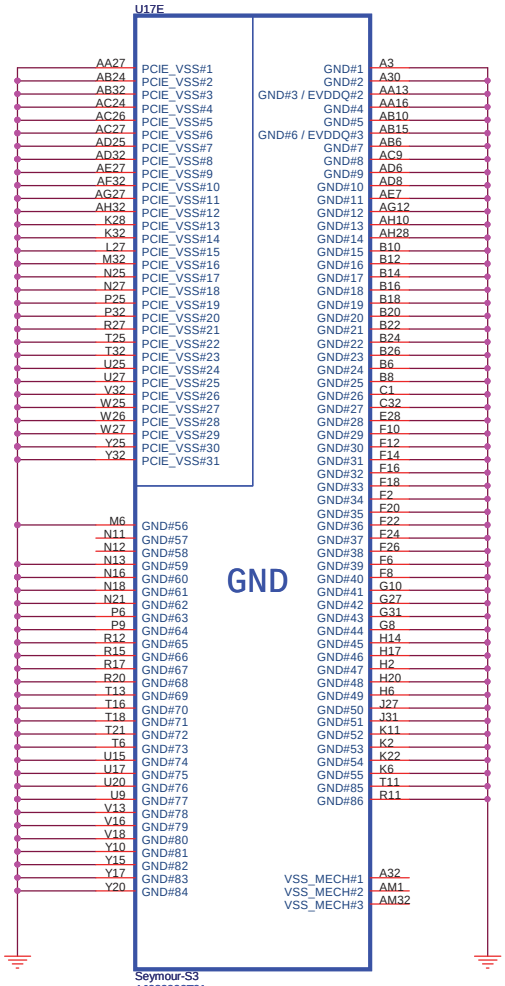
Seymour-S3--NC ROBSON--install

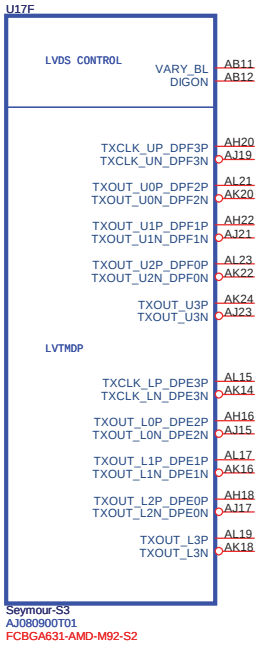
Reserve for DB debug only

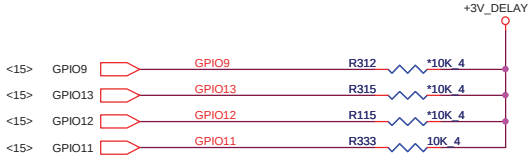
Robson-- Install Seymour- NC BACO mode -- install

For Int Clk 27Mhz

8/25 SI for H/W.







CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

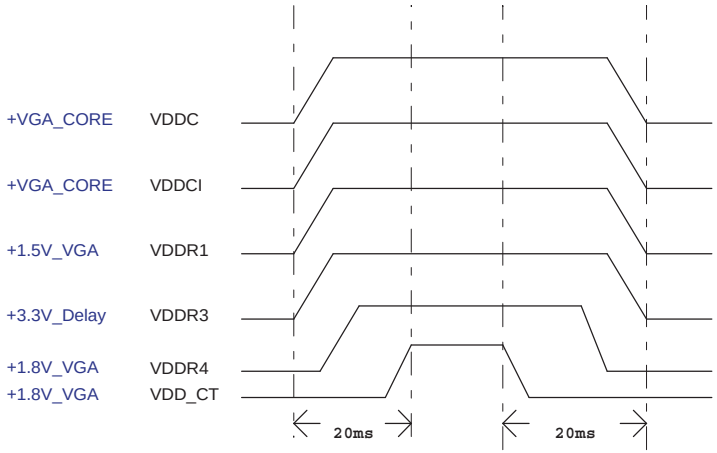
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

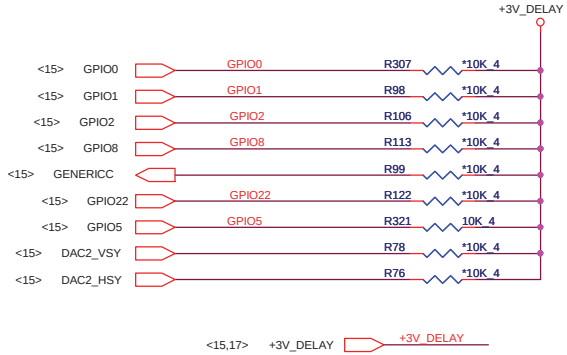
Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour GND / LVDS/ Straps	1A
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PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

+1.5V_VGA

1.5V (DDR3, MVDDQ = 1.5V@2.0A)

C404 1U/6.3V_4 C327 1U/6.3V_4 C330 1U/6.3V_4 C331 1U/6.3V_4 C336 1U/6.3V_4

C645 10U/6.3VS_6 C624 10U/6.3VS_6 C395 10U/6.3VS_6

U17D

MEM I/O

VDDR1#1 H13
VDDR1#2 H16
VDDR1#3 H19
VDDR1#4 J10
VDDR1#5 J23
VDDR1#6 J24
VDDR1#7 J9
VDDR1#8 K10
VDDR1#9 K23
VDDR1#10 K24
VDDR1#11 K9
VDDR1#12 L11
VDDR1#13 L12
VDDR1#14 L13
VDDR1#15 L20
VDDR1#16 L21
VDDR1#17 L22

PCIE

PCIE_VDDR#1 AB23
PCIE_VDDR#2 AC23
PCIE_VDDR#3 AD24
PCIE_VDDR#4 AE24
PCIE_VDDR#5 AE25
PCIE_VDDR#6 AE26
PCIE_VDDR#7 AF25
PCIE_VDDR#8 AG26

+1.8V_PCIE_VDDR

1.8V(500mA)

PBY160808T-221Y-N/2A_6 L18 +1.8V_VGA

C242 0.1U/10V_4 C150 0.1U/10V_4 C154 1U/6.3V_4 C136 1U/6.3V_4 C135 1U/6.3V_4 C230 1U/6.3V_4 C137 1U/6.3V_4 C162 10U/6.3VS_6

PCIE_VDDC#1 L23
PCIE_VDDC#2 L24
PCIE_VDDC#3 L25
PCIE_VDDC#4 L26
PCIE_VDDC#5 M22
PCIE_VDDC#6 N22
PCIE_VDDC#7 N23
PCIE_VDDC#8 N24
PCIE_VDDC#9 R22
PCIE_VDDC#10 T22
PCIE_VDDC#11 U22
PCIE_VDDC#12 V22

+1.0V_VGA

+1.0V_PCIE_VDDC

1.0V(2.0A)

+1.0V_PCIE_VDDC

0_8 L26

C304 1U/6.3V_4 C280 1U/6.3V_4 C269 1U/6.3V_4 C294 1U/6.3V_4 C260 1U/6.3V_4 C299 1U/6.3V_4 C319 1U/6.3V_4 C307 10U/6.3VS_6

1.8V(110mA VDD_CT)

+1.8V_VGA L22 PBY160808T-121Y-N/2.5A_6 +1.8V_VDD_CT

C163 10U/6.3VS_6 C167 1U/6.3V_4 C241 1U/6.3V_4 C168 1U/6.3V_4 C249 0.1U/10V_4

LEVEL TRANSLATION

VDD_CT#1 AA20
VDD_CT#2 AA21
VDD_CT#3 AB20
VDD_CT#4 AB21

Gated 3.3V 60mA by VDDC

+3V_VGA L19 0_6 +3V_DELAY +3V_DELAY

C228 1U/6.3V_4 C226 1U/6.3V_4 C279 1U/6.3V_4 C243 10U/6.3VS_6

VDD_R3 --IO power for 3.3 V pins (e.g. GPIO's). 3.3 V ± 5%

Seymour-S3 I/O

VDDR3#1 AA17
VDDR3#2 AA18
VDDR3#3 AB17
VDDR3#4 AB18

+VDDR4

+1.8V_VGA L23 PBY160808T-121Y-N/2.5A_6 +VDDR4

1.8V(170mA VDDR4)

C209 10U/6.3VS_6 C212 1U/6.3V_4 C256 0.1U/10V_4 T14

VDDR4#1 / VDDR5 V12
VDDR4#2 Y12
VDDR4#3 / VDDR5 U12

NC#1 / VDDR4 AA11
DVCLK / VDDR4 Y11

NC#3 / VDDR5 V11
NC / VDDR5 U11

VDDC+VDDCI

0.85~1.1V(15A peak)(Ripple < 87.2mV)

+VGA_CORE

CORE POWER

VDDC#1 AA15
VDDC#2 N15
VDDC#3 N17
VDDC#4 R13
VDDC#5 R16
VDDC#6 R18
VDDC#7 Y21
VDDC#8 T12
VDDC#9 T15
VDDC#10 T17
VDDC#11 T20
VDDC#12 U13
VDDC#13 U16
VDDC#14 U18
VDDC#15 V21
VDDC#16 V15
VDDC#17 V17
VDDC#18 V20
VDDC#20 Y13
VDDC#21 Y16
VDDC#22 Y18
VDDC#23 /BIF_VDDC R21
VDDC#19/BIF_VDDC U21

C86 1U/6.3V_4 C92 1U/6.3V_4 C293 1U/6.3V_4 C276 1U/6.3V_4 C91 1U/6.3V_4 C268 1U/6.3V_4 C277 1U/6.3V_4 C519 10U/6.3VS_6

C85 1U/6.3V_4 C323 2.2U/6.3V_4 C262 1U/6.3V_4 C305 10U/6.3V_8 C272 1U/6.3V_4 C257 1U/6.3V_4 C258 1U/6.3V_4

C259 1U/6.3V_4 C286 2.2U/6.3V_4 C275 1U/6.3V_4 C87 1U/6.3V_4 C79 1U/6.3V_4 C247 1U/6.3V_4

C81 10U/6.3VS_6 C88 10U/6.3VS_6 C83 10U/6.3VS_6 C521 10U/6.3VS_6 C520 10U/6.3VS_6 C82 10U/6.3VS_6

1.8V(75mA MPV18)

+1.8V_VGA L50 BLM18PG471SN1D/1A_6 MPV18

C600 1U/6.3V_4 C602 0.1U/10V_4

MEM CLK

VDDRHA L17
VSSRHA L16

1.8V(40mA PCIE_PVDD)

+1.8V_PCIE_VDDR

8/25 SI for SMT.

PLL

PCIE_PVDD AM30

1.8V(90mA SPV18)

+1.8V_VGA L27 PBY160808T-121Y-N/2.5A_6 SPV18

C317 1U/6.3V_4 C295 0.1U/10V_4

MPV18 L8

SPV18 H7

1.0V_VGA(100mA SPV10)

+1.0V_VGA L29 BLM18PG471SN1D/1A_6 +1.0V_VGA_SPV10

C337 10U/6.3VS_6 C332 0.1U/10V_4 C328 1U/6.3V_4

SPV10 H8
SPVSS J7

ISOLATED CORE I/O

VDDCI#1 M13
VDDCI#2 M15
VDDCI#3 M16
VDDCI#4 M17
VDDCI#5 M18
VDDCI#6 M20
VDDCI#7 M21
VDDCI#8 N20

Note1.

BIF_VDDC R112 0_4 +VGA_CORE

Ra

0.95V~1.1V(2A VDDCI)

+VDDCI 0_8 L24 +VGA_CORE

C329 1U/6.3V_4 C313 1U/6.3V_4 C306 1U/6.3V_4 C265 10U/6.3VS_6 C266 10U/6.3VS_6 C315 10U/6.3VS_6

BACK BIAS

BBP#1 M11
BBP#2 M12

<11,21,22,23,25,28,30,36> +5V
<2,3,7,8,9,10,11,12,13,14,20,21,22,23,24,25,27,28,29,30,33,34,36> +3V
<14,15,35> +1.0V_VGA
<34> +3V_VGA
<34> +VGA_CORE

+5V +3V +1.0V_VGA +3V_VGA +VGA_CORE

Seymour-S3
AJ080900T01
FCBGA631-AMD-M92-S2

Support BACO Mode

+3V R330 *10K_4 not stuff

<34> PX_MODE R334 *0_4

<18> PX_EN

R94 *5.1K_4

Q31 *2N7002E

8/25 SI for AMD.

<34> PX_MODE1

PX_EN Q41 *2N7002E

8/25 SI for AMD.

<9,29> EC_PWROK

Q29 *2N7002E

R500 PX_MODE PX_MODE1 *0_4

<2,10,29,34,35> DGPU_PWROK

R323 *100K_4 Q25 *2N7002E

+3V C592 *0.1U/10V_4

PX_MODE U18 *TC7SH08FU BACO_EN

+5V R337 *1K_4 R336 *1K_4

PX_EN## PX_EN#

Q28 *2N7002E Q30 *2N7002E

+1.0V_VGA Q10 *AO3416 Q27 *AO3416

PX_EN# Q9 *AO3416 Q26 *AO3416

+VGA_CORE PX_EN##

BIF_VDDC

C325 *22U/6.3VS_8 C287 *10U/6.3VS_6 C297 *10U/6.3VS_6 C270 *2.2U/6.3V_4 C271 *2.2U/6.3V_4

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

Note1.

1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour_Power_and_NC	1A

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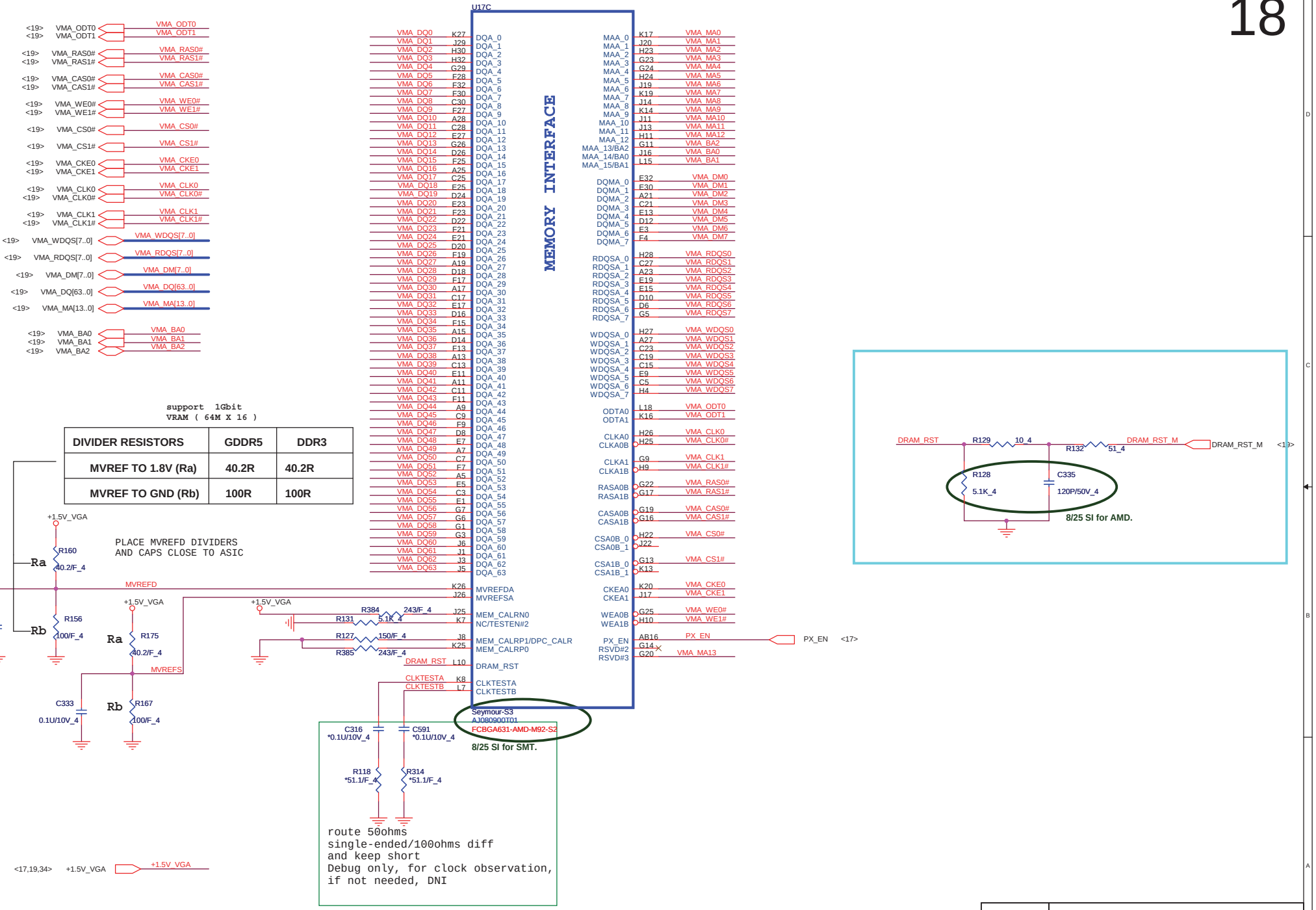
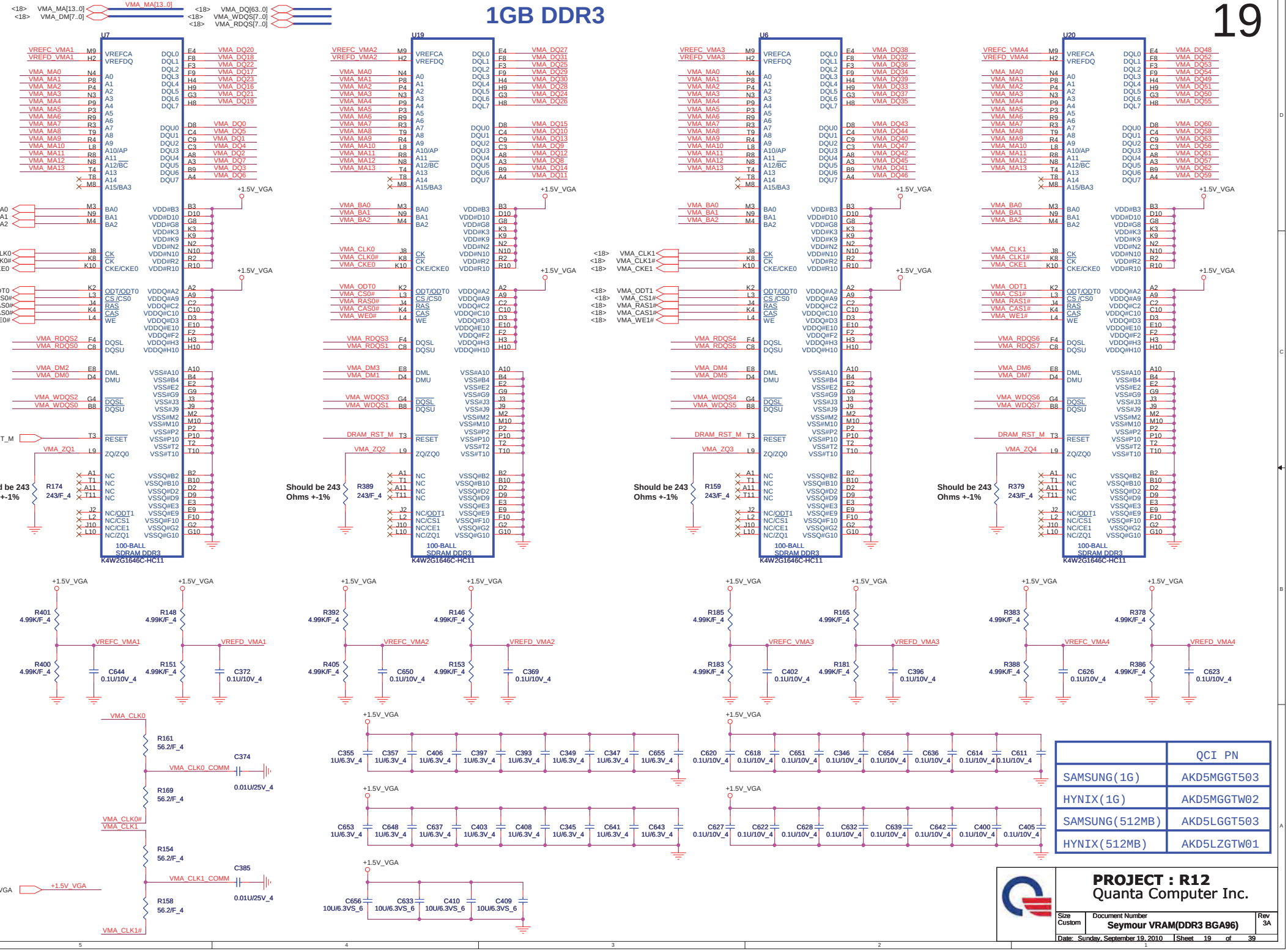

U17C
MEMORY INTERFACE
VMA_ODT0
VMA_ODT1
VMA_RAS0#
VMA_RAS1#
VMA_CAS0#
VMA_CAS1#
VMA_WE0#
VMA_WE1#
VMA_CS0#
VMA_CS1#
VMA_CKE0
VMA_CKE1
VMA_CLK0
VMA_CLK0#
VMA_CLK1
VMA_CLK1#
VMA_WDQS[7..0]
VMA_RDQS[7..0]
VMA_DM[7..0]
VMA_DQ[63..0]
VMA_MA[13..0]
VMA_BA0
VMA_BA1
VMA_BA2
support 1Gbit
VRAM (64M X 16)
DIVIDER RESISTORS
GDDR5
DDR3
MVREF TO 1.8V (Ra)
40.2R
40.2R
MVREF TO GND (Rb)
100R
100R
PLACE MVREFD DIVIDERS
AND CAPS CLOSE TO ASIC
+1.5V_VGA
R160
Ra
40.2/F_4
MVREFD
C326
0.1U/10V_4
R156
Rb
100/F_4
R175
MVREFS
C333
R167
R384
243/F_4
R131
5.1K_4
R127
150/F_4
R385
DRAM_RST
CLKTESTA
CLKTESTB
C316
*0.1U/10V_4
C591
R118
*51.1/F_4
R314
route 50ohms
single-ended/100ohms diff
and keep short
Debug only, for clock observation,
if not needed, DNI
Seymour-S3
AJ080900T01
FCBGA631-AMD-M92-S2
8/25 SI for SMT.
PX_EN
VMA_MA13
DRAM_RST
R129
10_4
R132
51_4
DRAM_RST_M
R128
5.1K_4
C335
120P/50V_4
8/25 SI for AMD.

1GB DDR3



	QCI PN
SAMSUNG(1G)	AKD5MGGT503
HYNIX(1G)	AKD5MGGTW02
SAMSUNG(512MB)	AKD5LGGT503
HYNIX(512MB)	AKD5LZGTW01

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour VRAM(DDR3 BGA96)	3A

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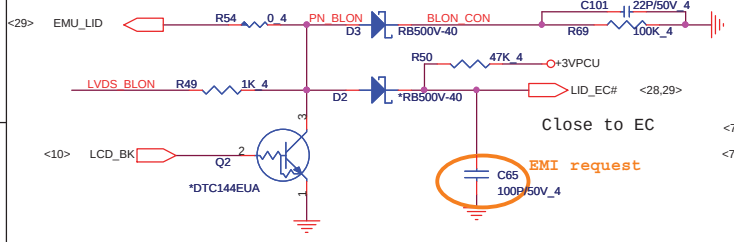
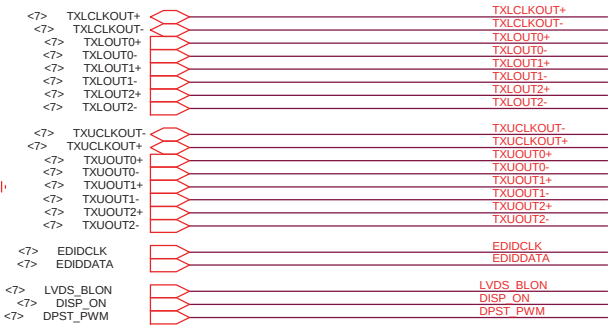
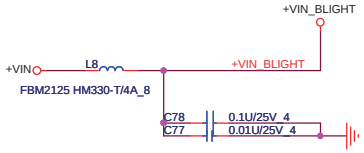
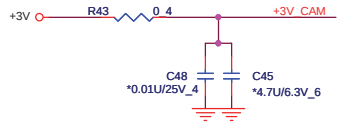
LID Switch





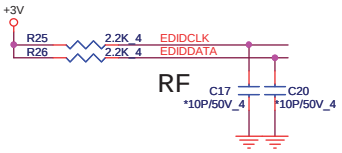


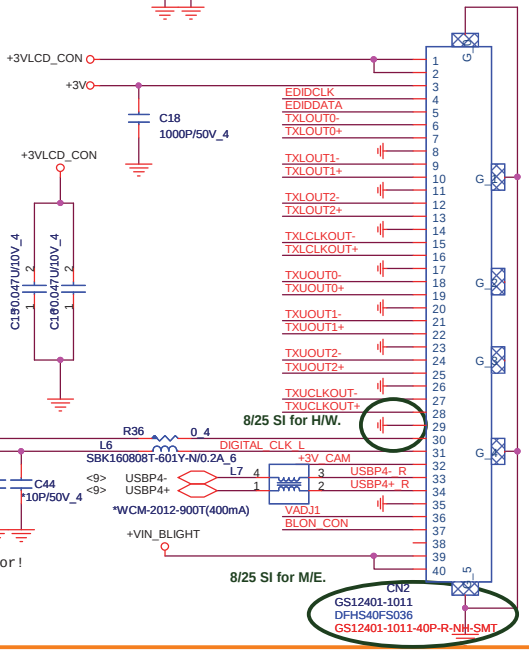


Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

follow L4 location

USBP4- R44 0_4 USBP4- R
USBP4+ R46 0_4 USBP4+ R



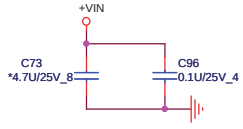


EMI

SI modify

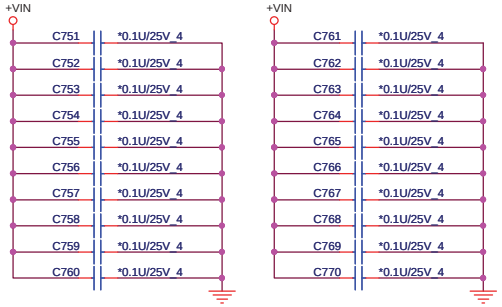
1A

EMI & RF



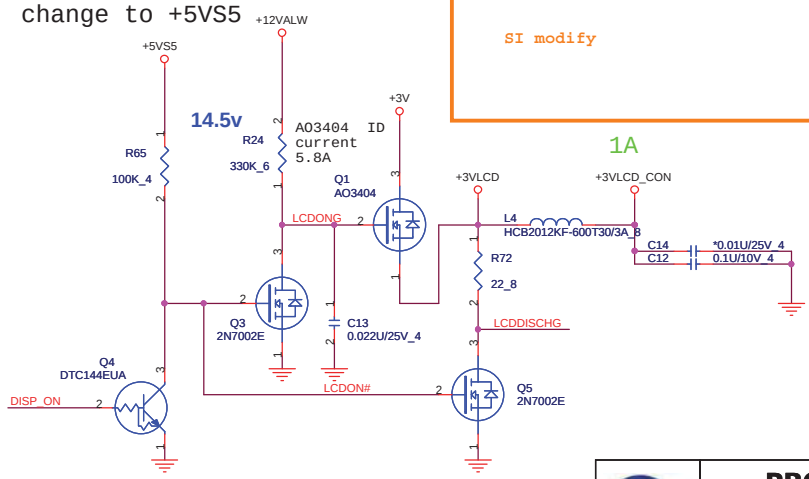
8/25 SI for H/W.

Coupling CAP.



8/25 SI for H/W.

change to +5VS5



<7,28,29,31,37> +3VPCU
<2,3,7,8,9,10,11,12,13,14,17,21,22,23,24,25,27,28,29,30,33,34,36> +3V
<23,34,36,37> +12VALW
<31,32,33,34,35,36,37,38,39> +VIN

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A

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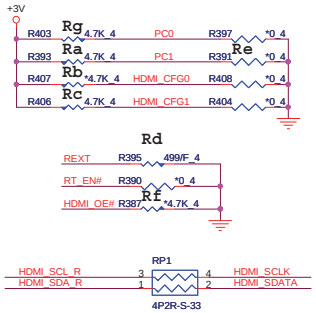
For UMA HDMI function

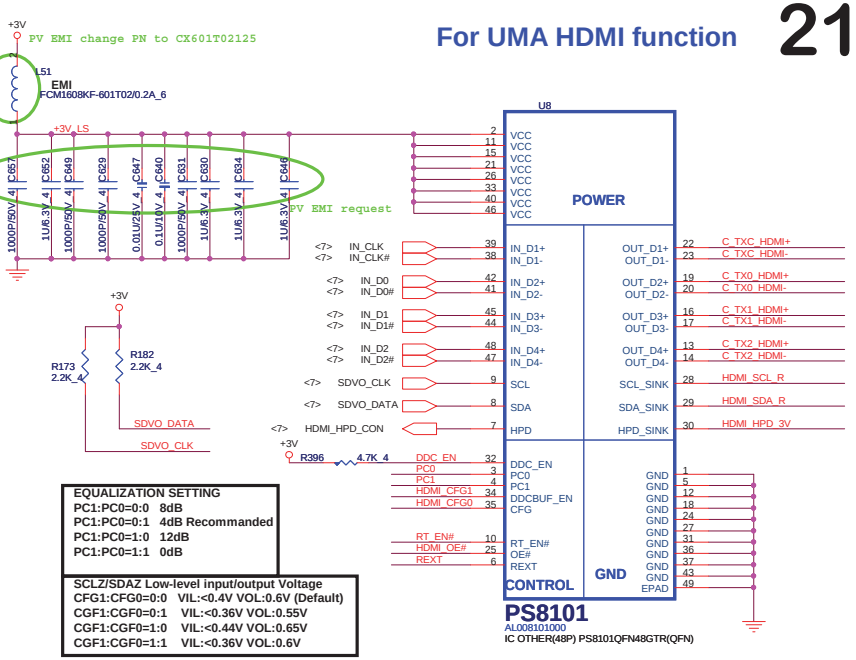
Signals		PDT	PIM	CHR
PC1	Ra	4.7K	4.7K	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	4.7K	1.2K
PC1	Re	NC	NC	4.7K
HDMI_OE#	Rf	NC	NC	4.7K
PC0	Rg	4.7K	4.7K	4.7K



Vender	Part	Part Number	Part Description
PDT	PS8101	AL008101000	IC OTHER(48P) PS8101QFN48GTR(QFN)
PIM	PI3VDP411LSRZBE	ALP411LS004	IC OTHER(48P) PI3VDP411LSRZBE(TQFN)
CHR	CH7318C	AL007318002	IC OTHER(48P) CH7318C-BF-TR(QFN)

9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

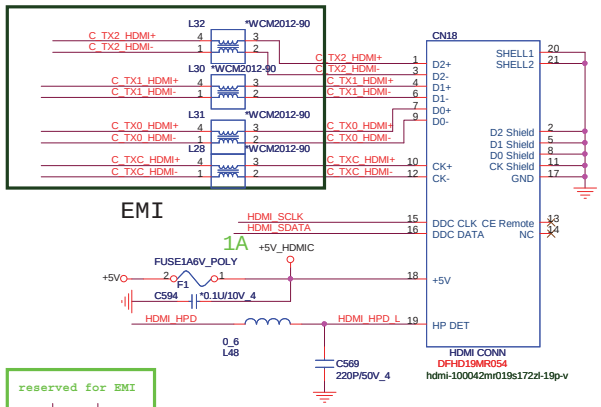
CHR : need Na R1182, add R1027 for capella

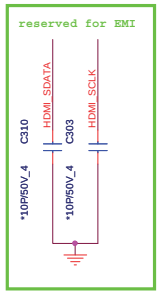


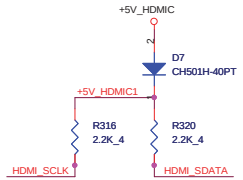
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

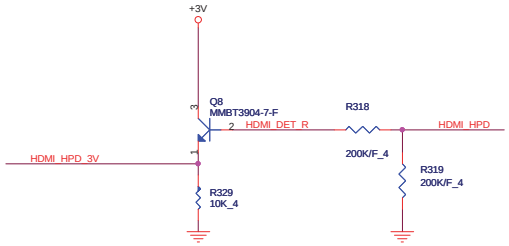
SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

8/25 SI for EMI reserve.









PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI CONN	1A

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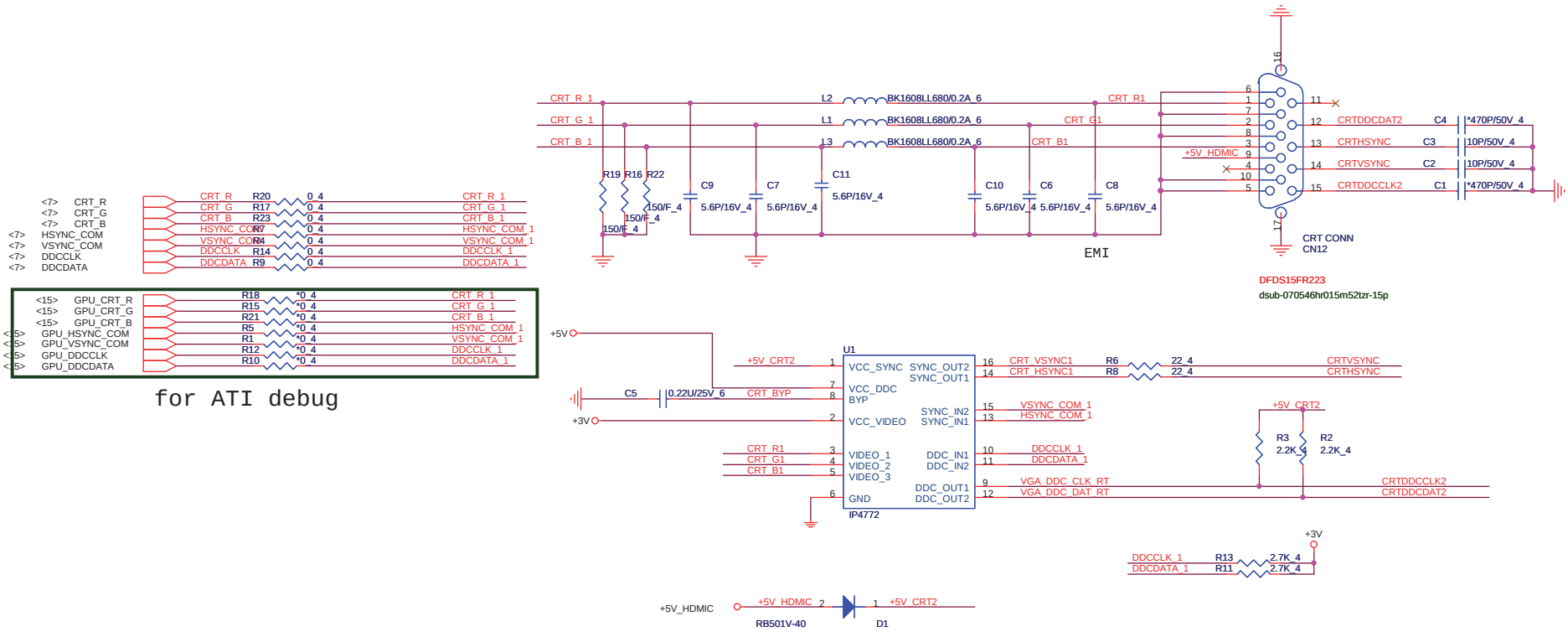
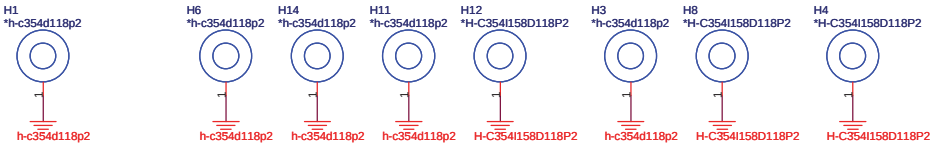
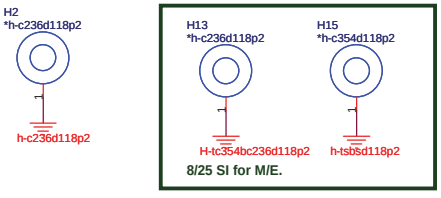
CRT PORT

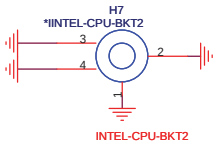


HOLE

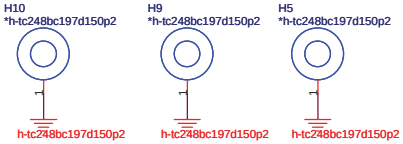




CPU



VGA



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT,Hole	1A

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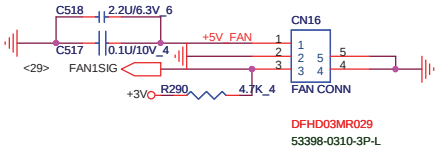
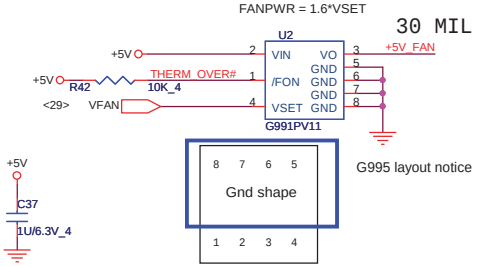
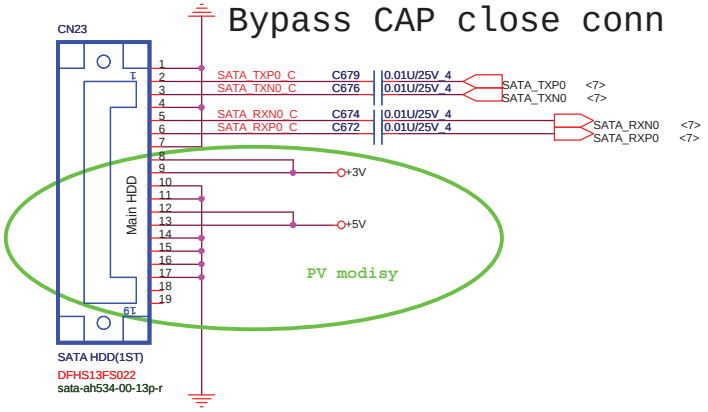
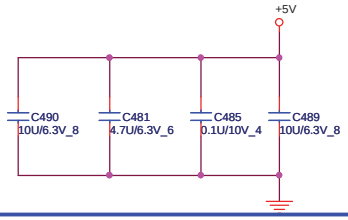
CPU FAN



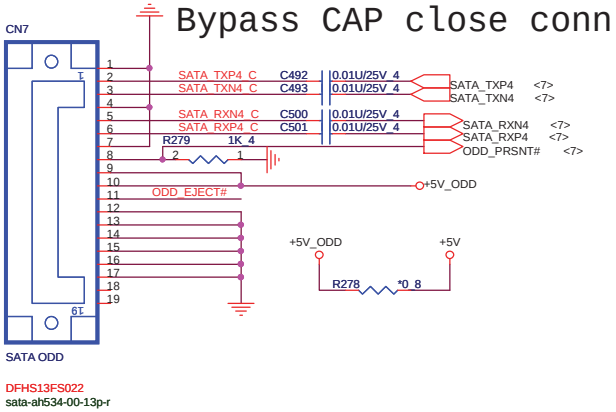


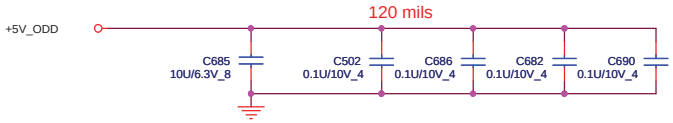
SATA HDD CONNECTOR



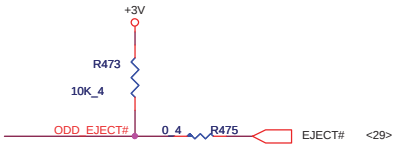


SATA ODD CONNECTOR

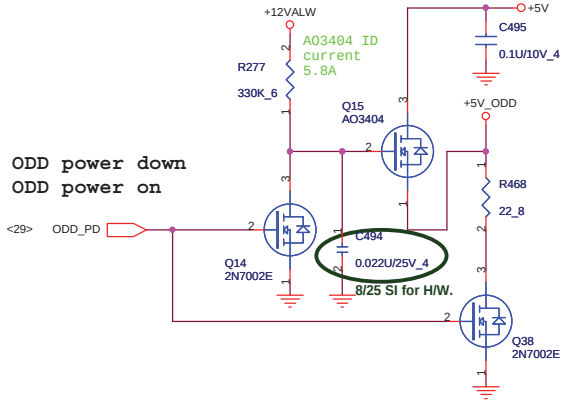




follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A

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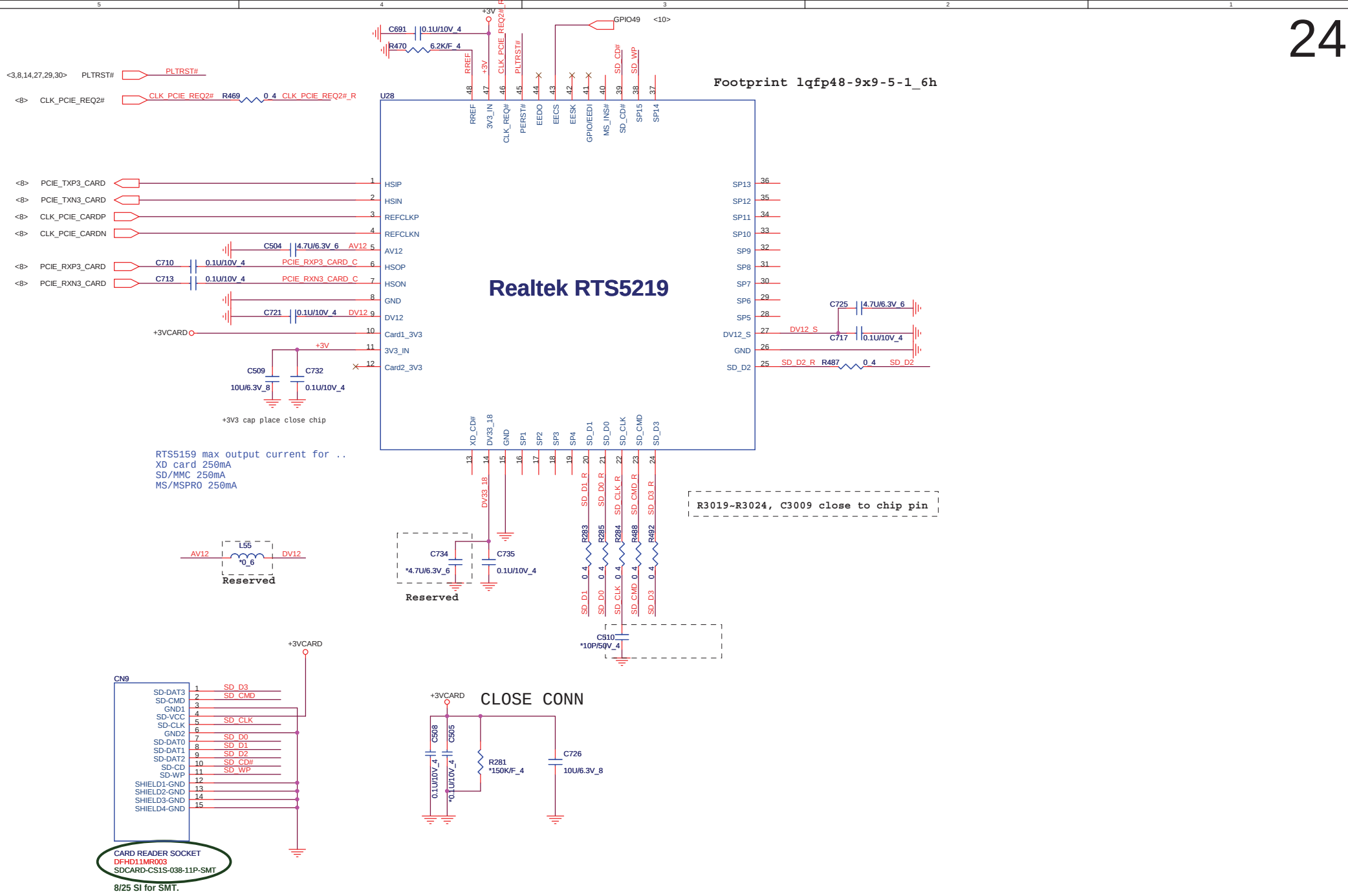
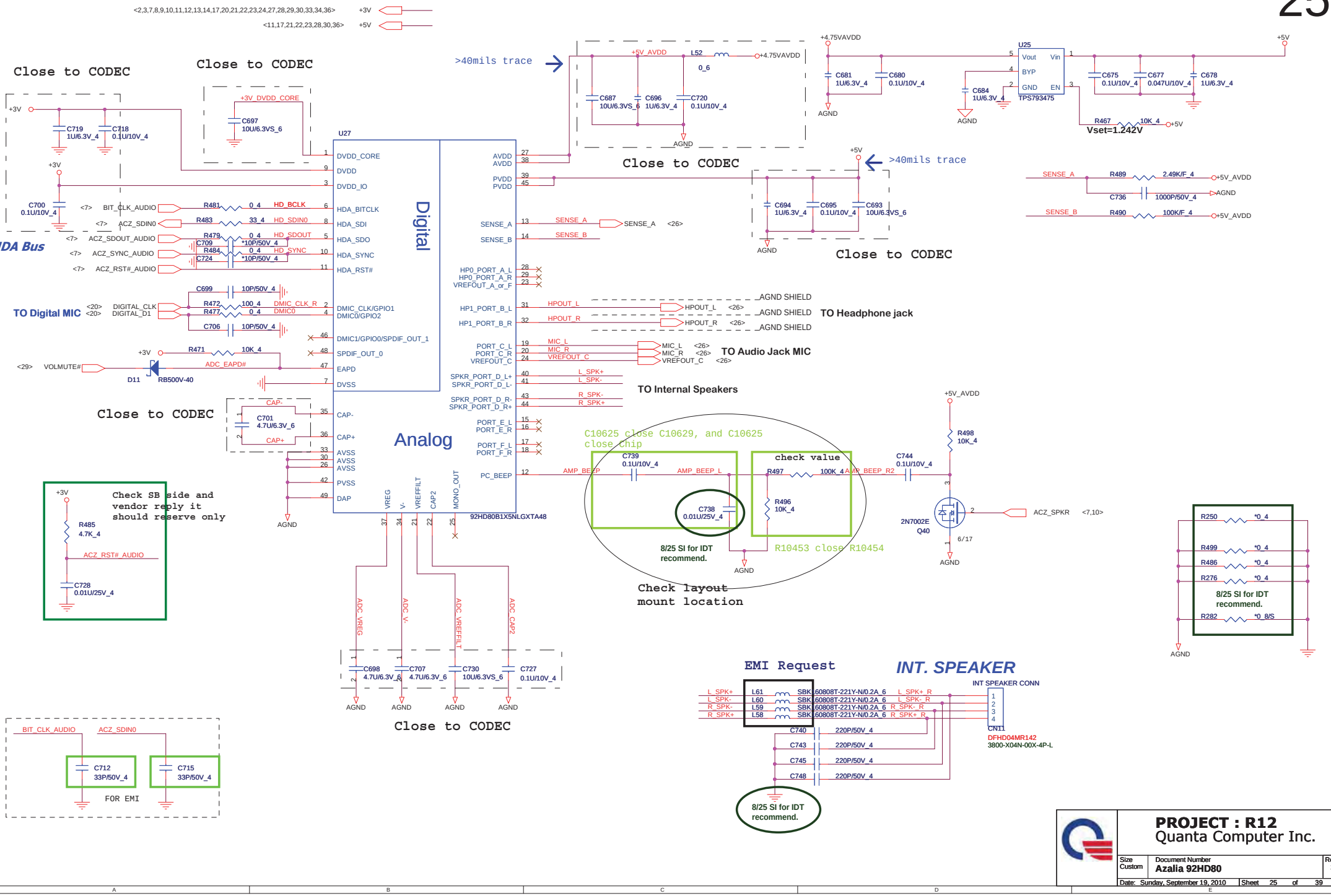


Quanta Computer Inc.	PROJECT : R12	
Size: Custom	Document Number: RTS5219 & CR SOCKET &HOLE	Rev: 1A
Date: Sunday, September 19, 2010	Sheet 24 of 39	


Close to CODEC
Close to CODEC
>40mils trace
Close to CODEC
>40mils trace
Close to CODEC
HDA Bus
TO Digital MIC
TO Headphone jack
TO Audio Jack MIC
TO Internal Speakers
Close to CODEC
Digital
Analog
92HD80B1X5NLGXTA48
C10625 close C10629, and C10625 close Chip
check value
R10453 close R10454
8/25 SI for IDT recommend.
Check layout mount location
Check SB side and vendor reply it should reserve only
Close to CODEC
EMI Request
INT. SPEAKER
FOR EMI
Vset=1.242V
TPS793475
2N7002E
Q40
DFHD04MR142
3800-X04N-00X-4P-L
PROJECT : R12
Quanta Computer Inc.
Azalia 92HD80
Date: Sunday, September 19, 2010
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BLUETOOTH

EMI request

BLUELED C496 *1000P/50V_4

300mA

change to +3VS5

+3VS5 R280 4.7K_4

+3VS5 Q16 ME2303T1

24mil 300mA

+3VPCU_BT

Q17 DTC144EUA

<10,30> BT_OFF#

C503 *0.01U/25V_4

C498 0.1U/10V_4

C499 *10U/6.3V_8

CN8

C497 *1000P/50V_4

BTCON_P1 T38

BLUELED <29,30>

USBP2- <9>

USBP2+ <9>

+3VPCU_BT

BLUE TOOTH CONN

87213-0600-6P-L

DFHD06MR058

LEFT SIDE USBX2

change to AL000547005

2A 2A

change to +5VS5

+5VS5 U23 80 mils (Iout=2A) +5V_USBP0

VIN1 VIN2 EN GND OUT3 OUT2 OUT1 OC

G547E2P81U

<29> USBPW_ON#

C664 1U/6.3V_4

C348 470P/50V_4

C351 0.1U/10V_4

C414 470P/50V_4

C413 0.1U/10V_4

C660 100U/25V

8/25 SI for H/W.

change to ELEC CAP

C356 *0.1U/10V_4

1A

R149 *0_4 L33 R152 *0_4 WCM2012-90

+5V_USBP0

USBP0- R

USBP0+ R

<9> USBP0-

<9> USBP0+

CN19

1 GND 2 GND 3 GND 4 GND

USB CONN

DFHD04MR133

usb-020173mr004s53qzl-4p-r-v

8/25 SI for EMI.

C411 *0.1U/10V_4

1A

R225 *0_4 L36 R226 *0_4 WCM2012-90

+5V_USBP0

USBP1- R

USBP1+ R

<9> USBP1-

<9> USBP1+

CN20

1 GND 2 GND 3 GND 4 GND

USB CONN

DFHD04MR133

usb-020173mr004s53qzl-4p-r-v

8/25 SI for EMI.

Right SIDE USBX1

+5VS5 C27 0.1U/10V_4

<29> USBPW_ON#

R502 *0_4 L5 WCM2012-90 R503 *0_4

<9> USBP8-

<9> USBP8+

USBP8- R

USBP8+ R

CN1

USB board

DFFC06MR001

88513-0601-6P-L-SMT

8/25 SI for EMI.

EMI request

USBPW_ON# C19 220P/50_4

Line out

SENSE_PHONE R465 20K/F_4 SENSE_A SENSE_A <25>

SENSE_MIC R256 10K/F_4 SENSE_A

AGND SHIELD

AGND SHIELD

AGND SHIELD

<25> HPOUT_L HPOUT_L R482 16/F_4 HPOUT_L1 L39 SBK160808T-301Y-N/0.2A_6 HPOUT_L2

<25> HPOUT_R HPOUT_R R480 16/F_4 HPOUT_R1 L42 SBK160808T-301Y-N/0.2A_6 HPOUT_R2

R275 20K/F_4

R270 20K/F_4

C491 1000P/50V_4

C476 1000P/50V_4

AGND

C483 0.1U/10V_4 C488 0.1U/10V_4

AGND

CN22

DFTJ06FR335

audio-311105-2-6p

AEC_311105-2

Normal Open

AGND

SENSE_PHONE

MIC

<25> VREFOUT_C VREFOUT_C C455 1U/6.3V_4 AGND

R248 3.9K/F_4

R246 3.9K/F_4

<25> MIC_L MIC_L C688 2.2U/6.3V_6 MIC_L1 L37 SBK160808T-301Y-N/0.2A_6 MIC_IN_L

<25> MIC_R MIC_R C689 2.2U/6.3V_6 MIC_R1 L38 SBK160808T-301Y-N/0.2A_6 MIC_IN_R

C456 220P/50V_4

C436 220P/50V_4

AGND

CN21

DFTJ06FR335

audio-311105-2-6p

AGND

AEC_311105-2

Normal Open

AGND

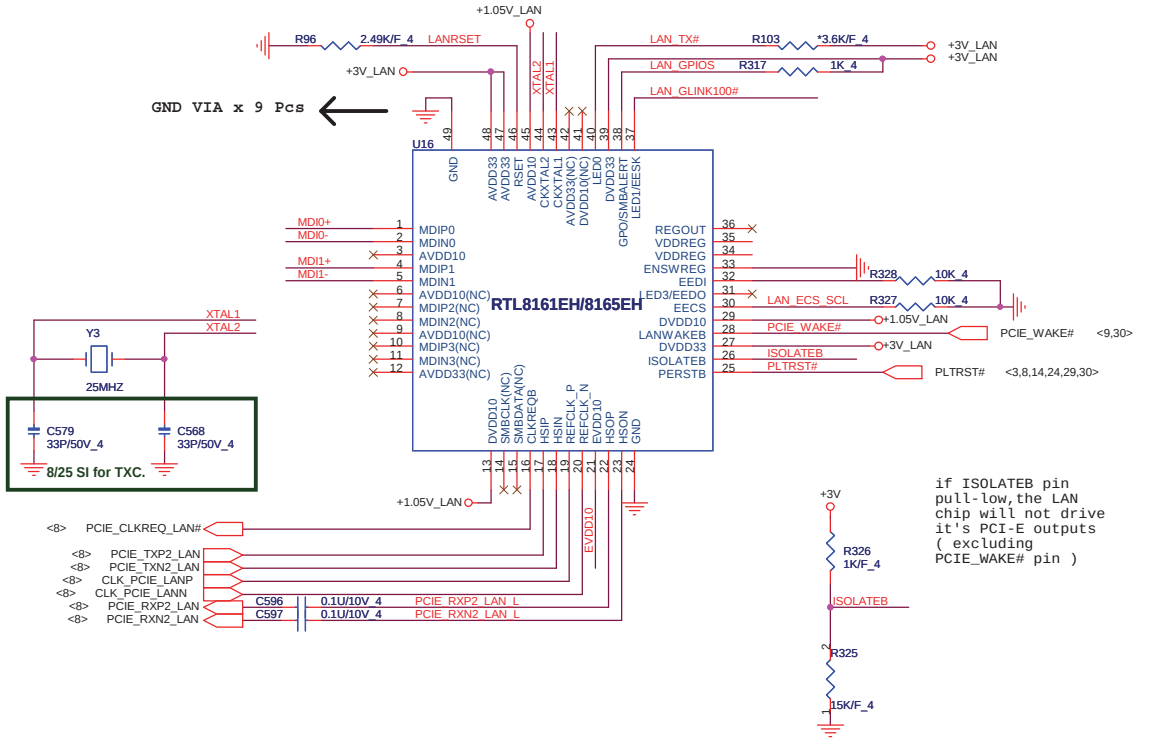
SENSE_MIC

PROJECT : R12

Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB/BT/Audio JacK	1A

Date: Sunday, September 19, 2010 | Sheet 26 of 39

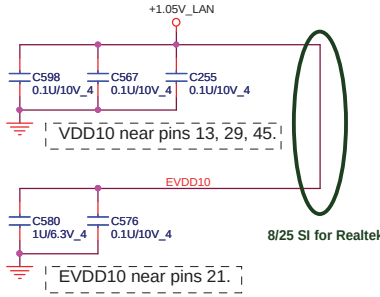


if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

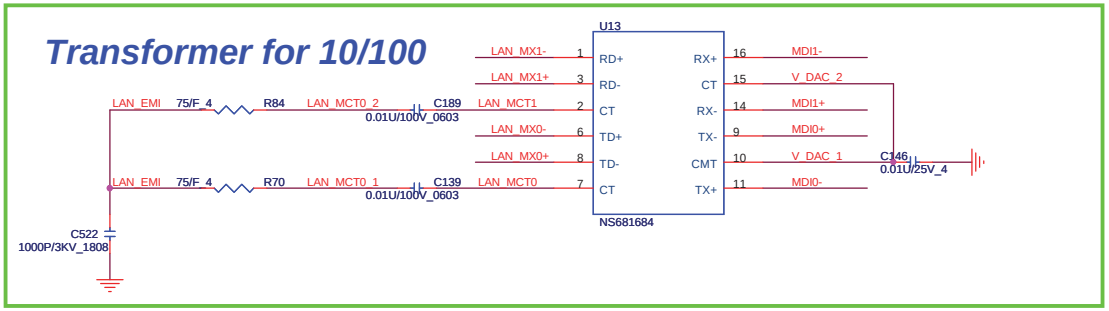
IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M) CV-4707MZ00

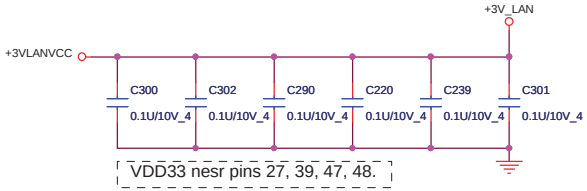
Power trace Layout 寬度> 60mil

>60mil

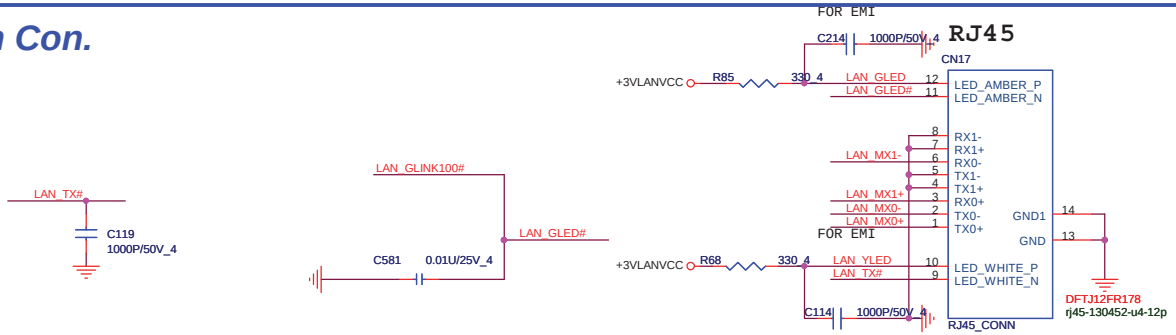


Transformer for 10/100





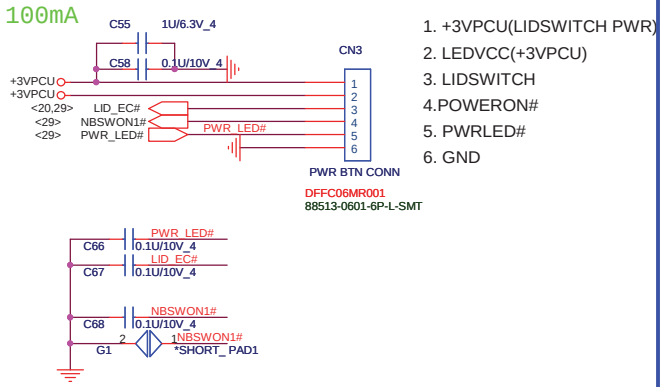
Lan Con.



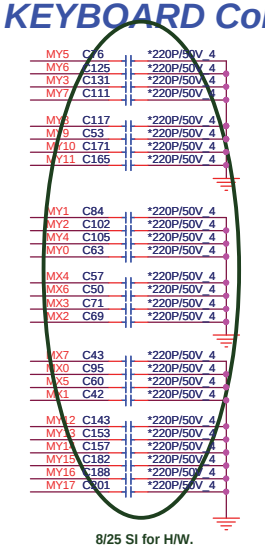
PROJECT : R12
Quanta Computer Inc.

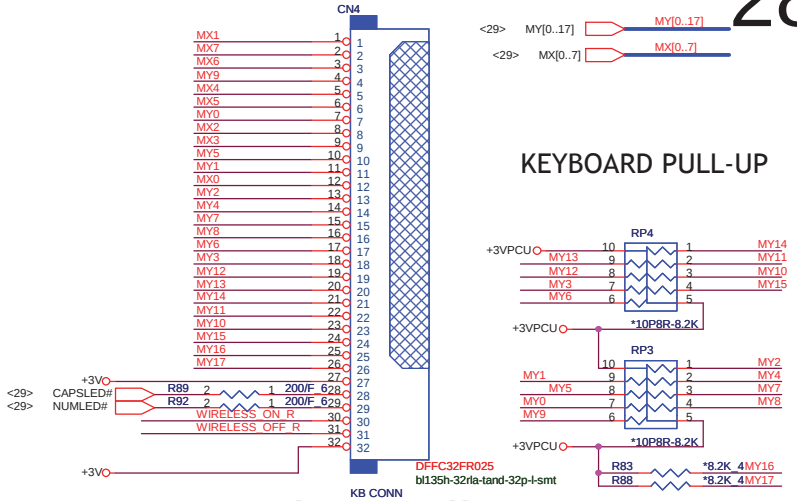
Size	Document Number	Rev
Custom	RTL8165EH	1A
Date: Sunday, September 19, 2010	Sheet 27 of 39	

POWER BOTTON CONNECT



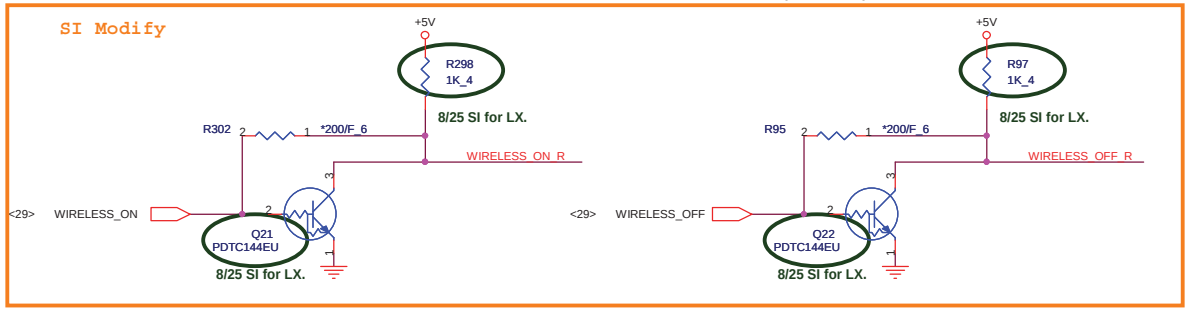
KEYBOARD Con.



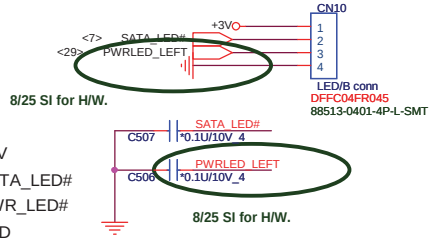


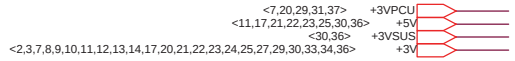
KEYBOARD PULL-UP

EC KB3930 has included K/B pull-up resistor and function

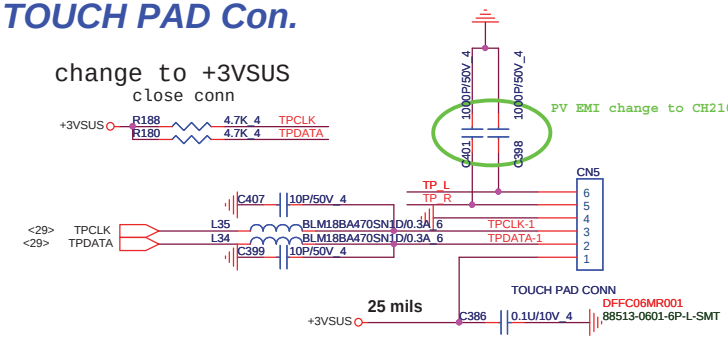


LED Con.

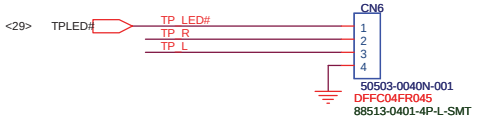




TOUCH PAD Con.



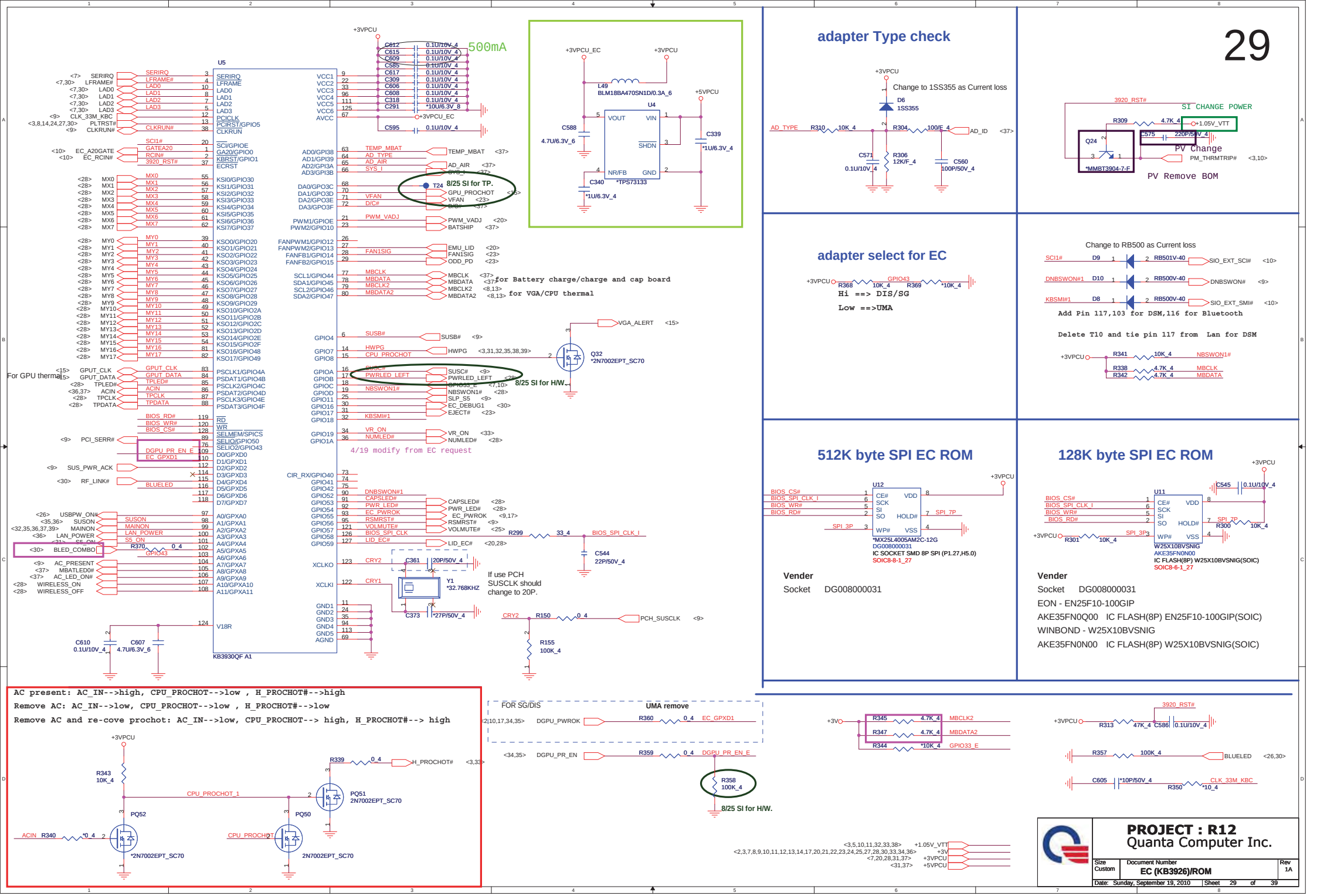
To TOUCH PAD SW board



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A

Date: Sunday, September 19, 2010 | Sheet 28 of 39



adapter Type check

Change to 1SS355 as Current loss

adapter select for EC

Hi ==> DIS/SG

Low ==>UMA

Change to RB500 as Current loss

Add Pin 117,103 for DSM,116 for Bluetooth

Delete T10 and tie pin 117 from Lan for DSM

512K byte SPI EC ROM

*MX25L4005AM2C-12G
DG008000031
IC SOCKET SMD 8P SPI (P1.27,H5.0)
SOIC8-8-1_27

Vender

Socket DG008000031

128K byte SPI EC ROM

W25X10BVSNIG
AKE35FN0N00
IC FLASH(8P) W25X10BVSNIG(SOIC)
SOIC8-6-1_27

Vender

Socket DG008000031

EON - EN25F10-100GIP

AKE35FN0Q00 IC FLASH(8P) EN25F10-100GIP(SOIC)

WINBOND - W25X10BVSNIG

AKE35FN0N00 IC FLASH(8P) W25X10BVSNIG(SOIC)

29

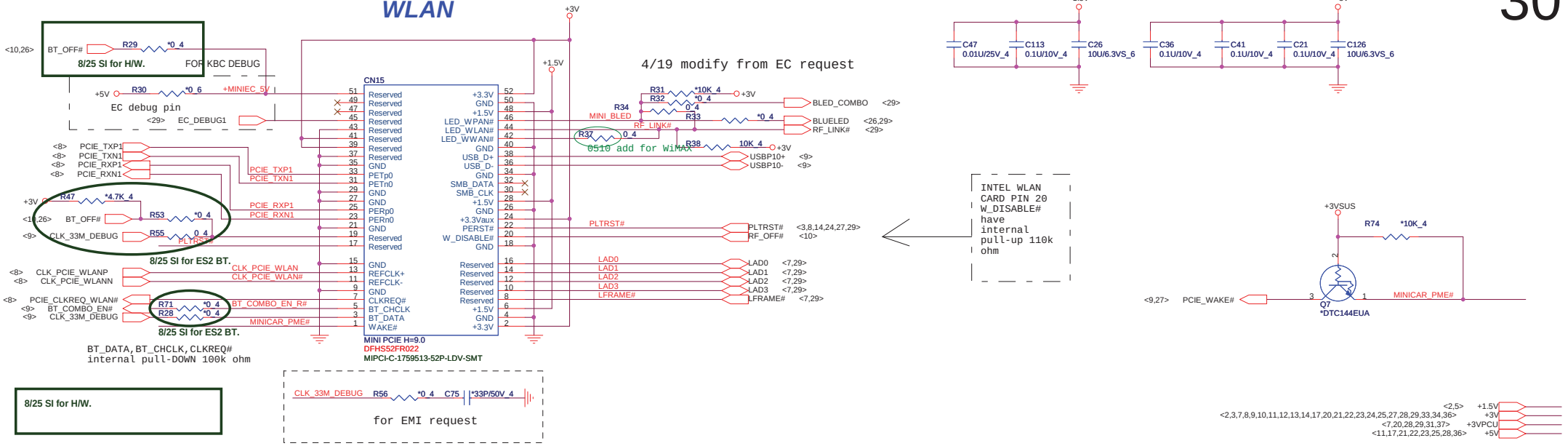
PV Change

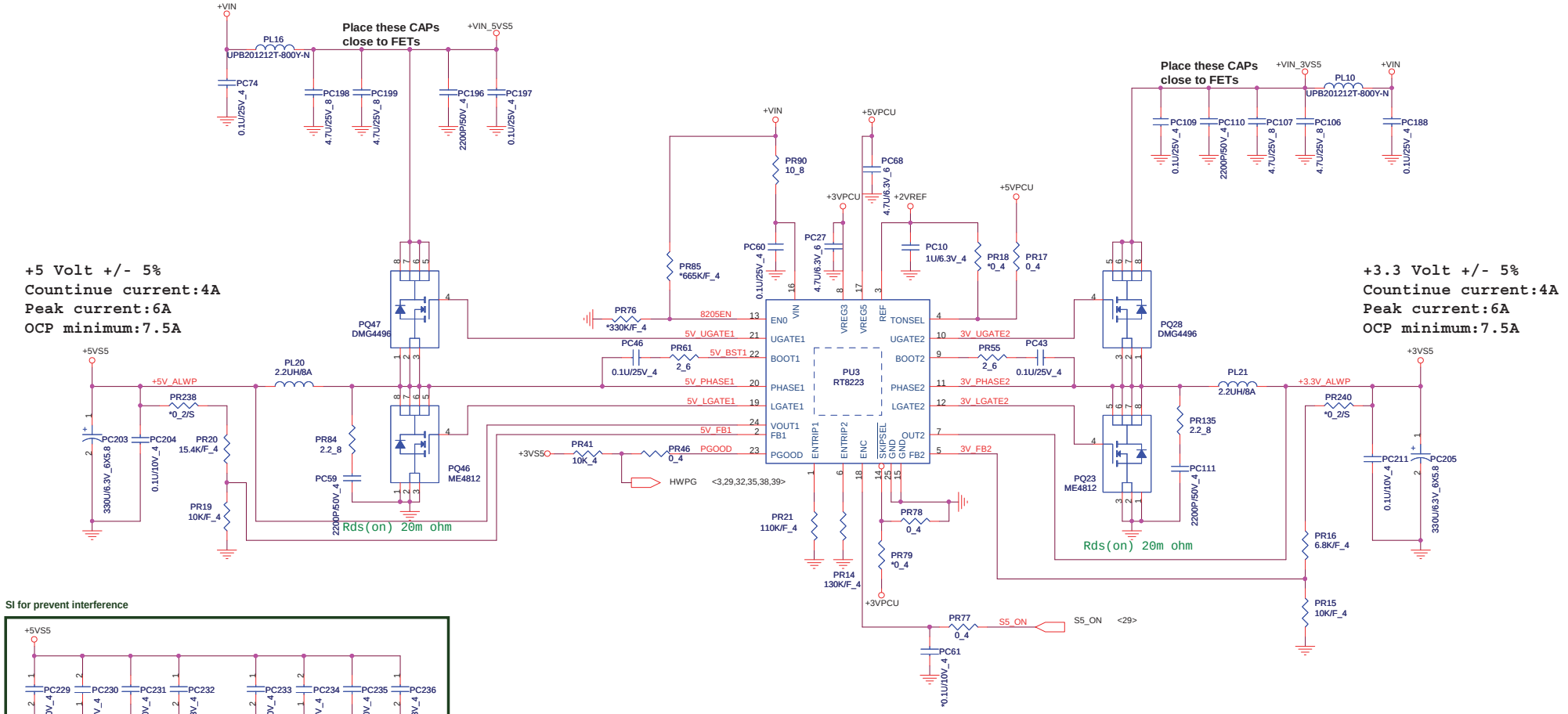
PV Remove BOM

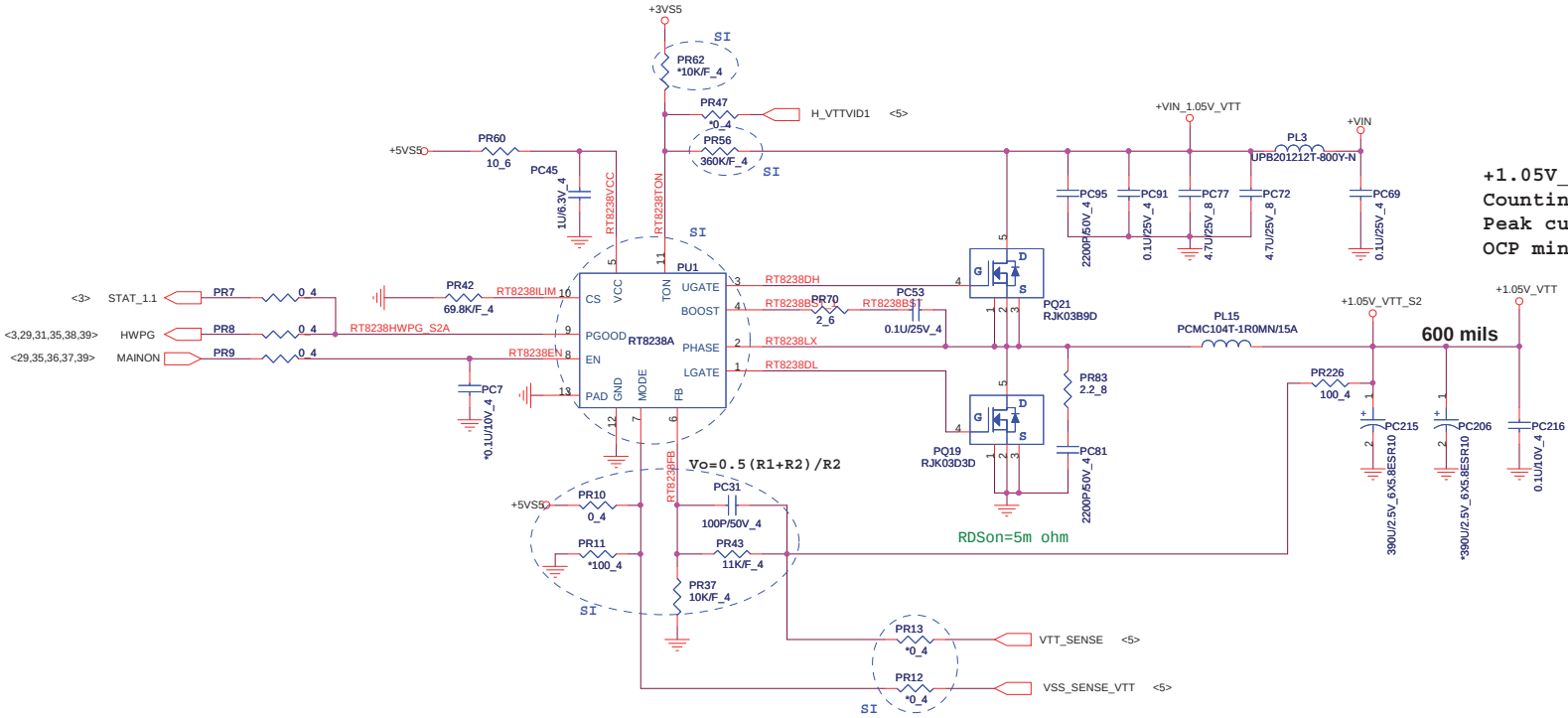
PROJECT :	R12
Quanta Computer Inc.	
Size: Custom	Document Number: EC (KB3926)/ROM
Rev: 1A	
Date: Sunday, September 19, 2010	Sheet 29 of 39

Mini PCI-E Card 1

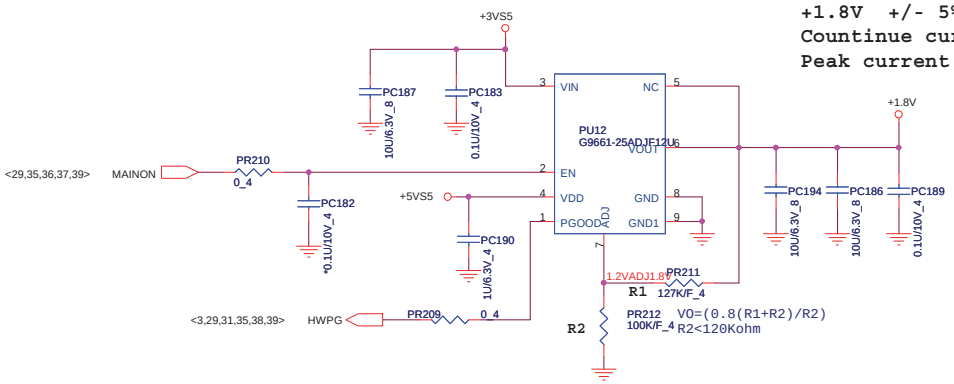
WLAN




+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A
Place these CAPs close to FETs
Place these CAPs close to FETs
PU3 RT8223
PQ47 DMG4496
PQ46 ME4812
PQ28 DMG4496
PQ23 ME4812
Rds(on) 20m ohm
Rds(on) 20m ohm
HWPG
S5_ON
SI for prevent interference



+1.05V_VTT Volt +/- 5%
Countinue current:10A
Peak current: 16A
OCP minimum: 18A



+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1V VTT / PCH	1A

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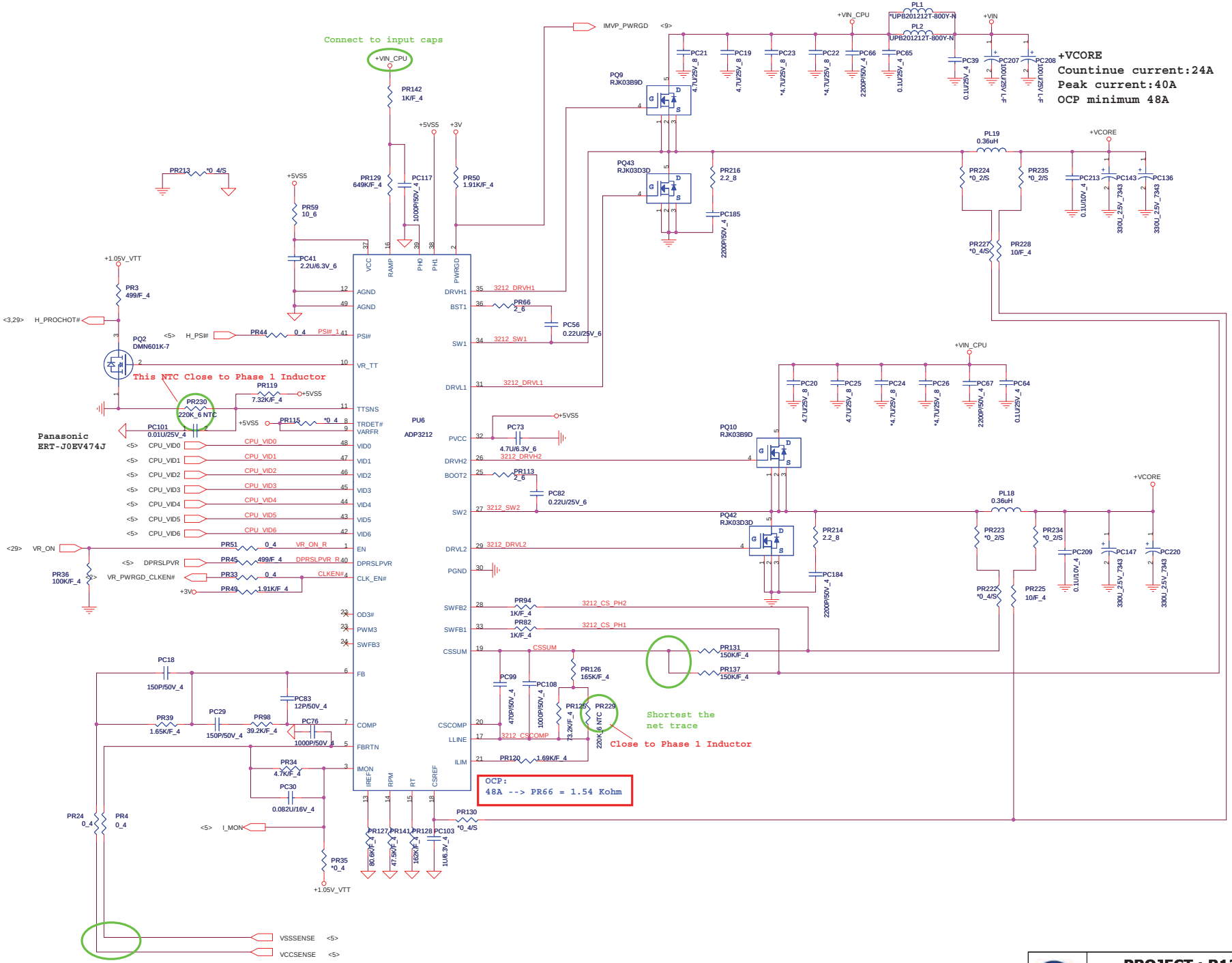

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core (ADP3212)	1A

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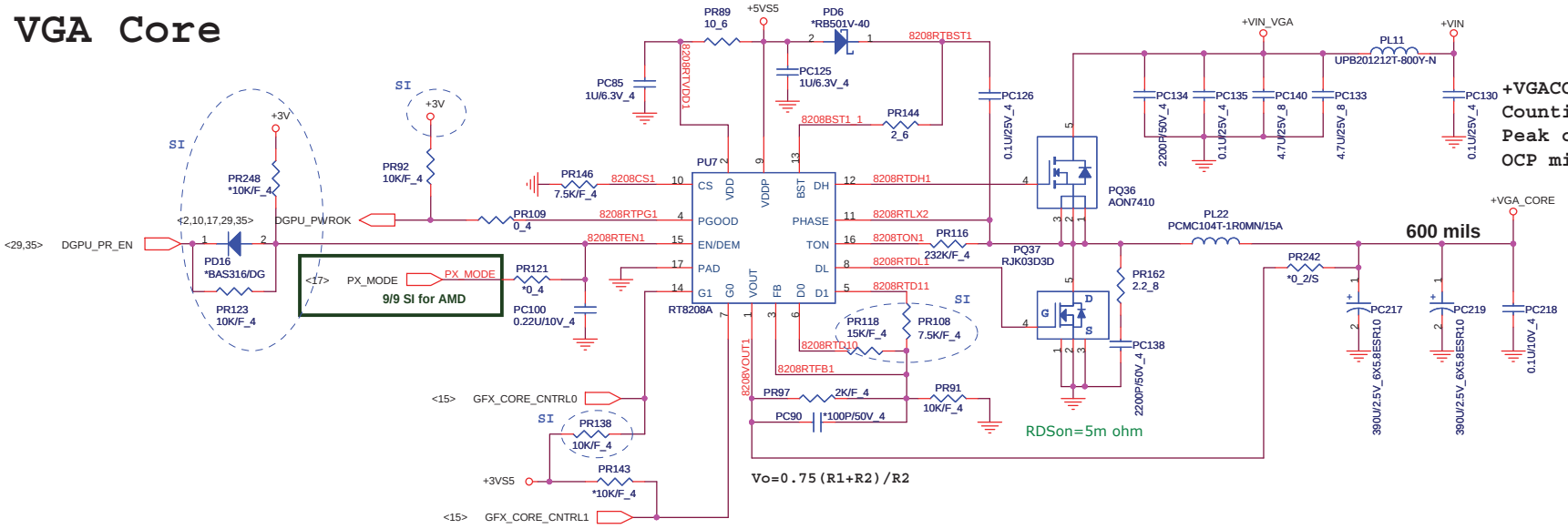
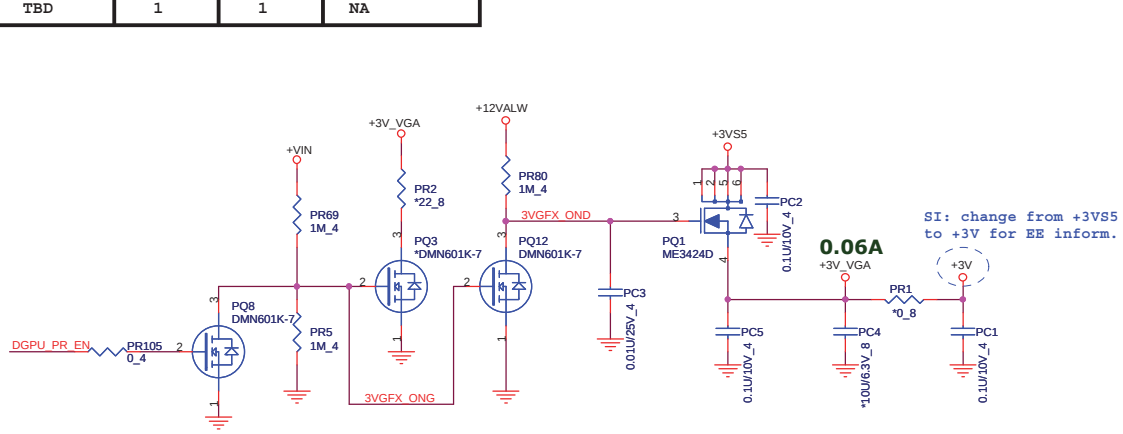
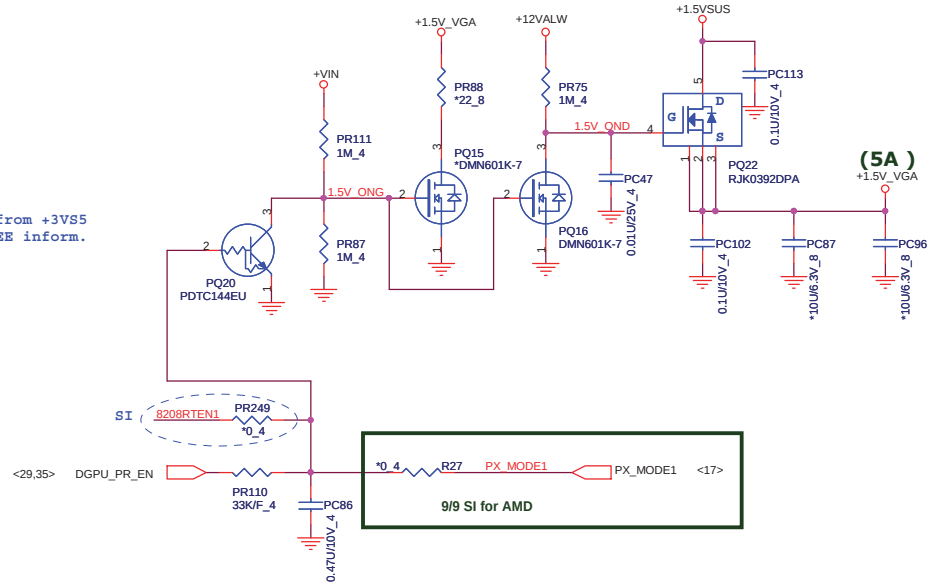
VGA Core



Seymour-XT	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA

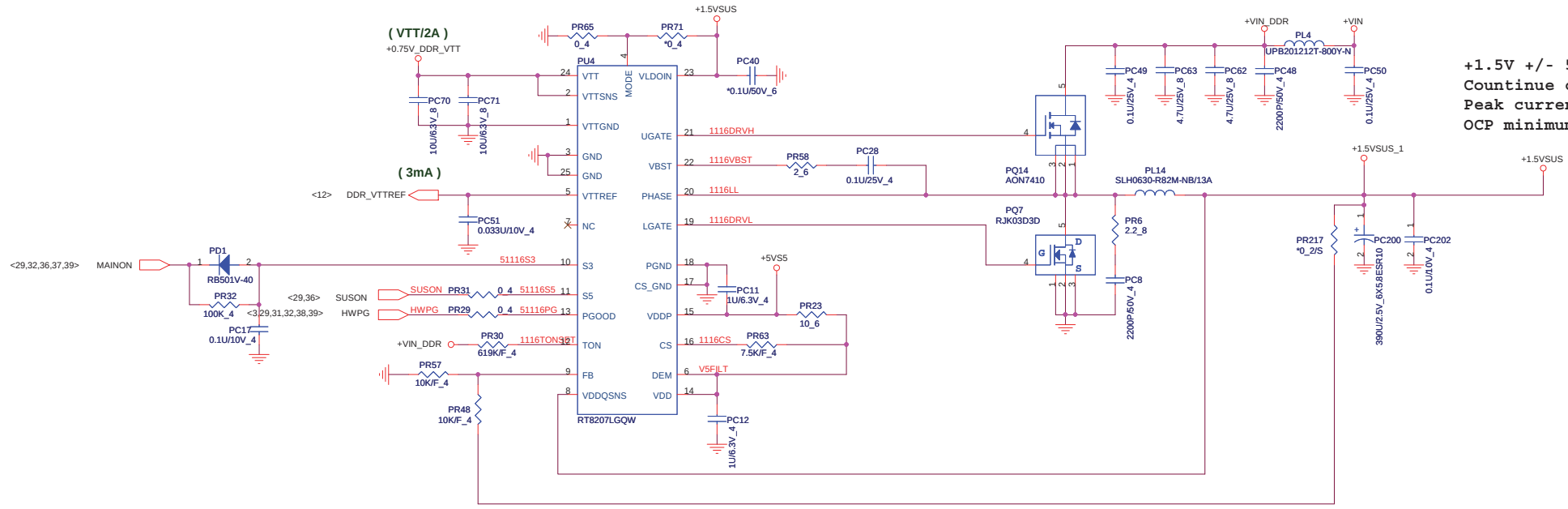




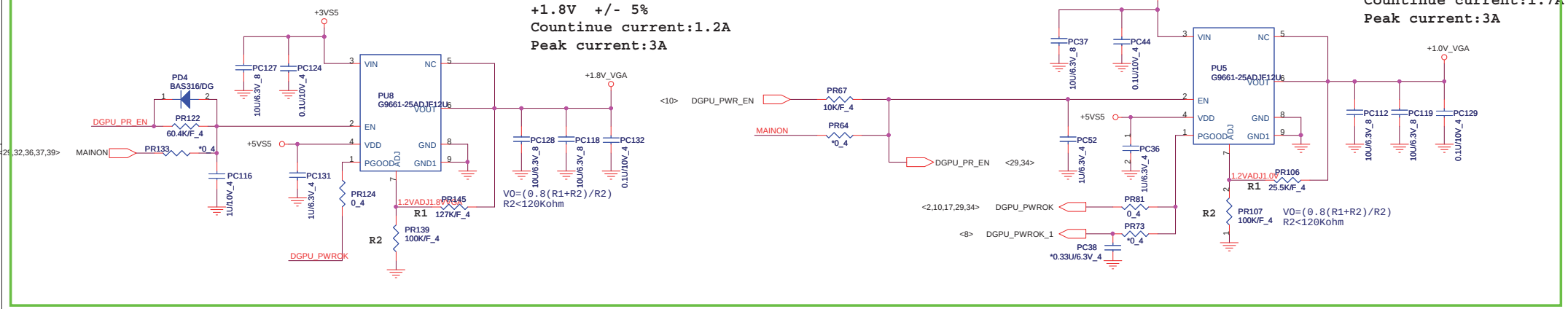
PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A

Date: Saturday, September 18, 2010 | Sheet 34 of 39



SG & Discrete Only



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A

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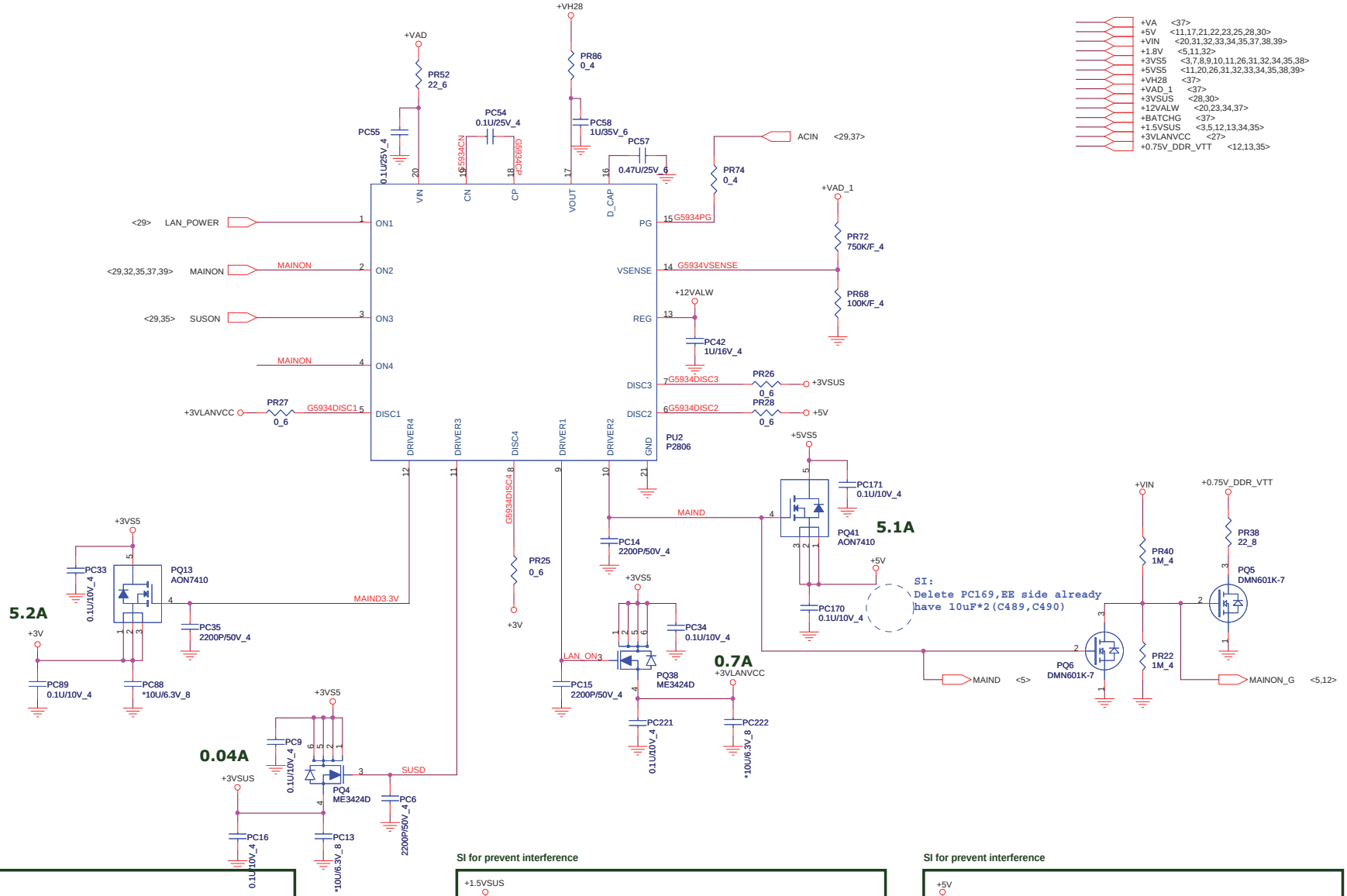
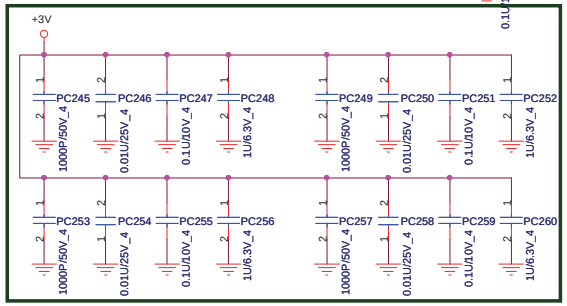
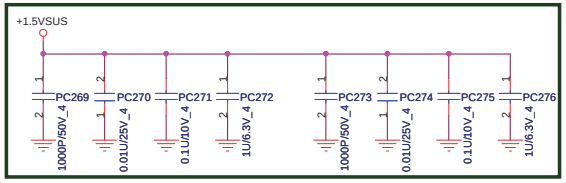
+VA <37>
+5V <11,17,21,22,23,25,28,30>
+VIN <20,31,32,33,34,35,37,38,39>
+1.8V <5,11,32>
+3VS5 <3,7,8,9,10,11,26,31,32,34,35,38>
+5VS5 <11,20,26,31,32,33,34,35,38,39>
+VH28 <37>
+VAD_1 <37>
+3VSUS <28,30>
+12VALW <20,23,34,37>
+BATCHG <37>
+1.5VSUS <3,5,12,13,34,35>
+3VLANVCC <27>
+0.75V_DDR_VTT <12,13,35>



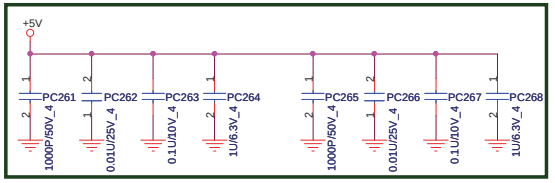
SI for prevent interference



SI for prevent interference



SI for prevent interference



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	1A

Date: Sunday, September 19, 2010 Sheet 36 of 39

DC_JACK
90W

SI:
M/E modify.

Do Not add test pad on BATDIS_G signal

To PWR LED

Place this ZVS close to Diode away +VIN

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this cap close to EC

Place this cap close to EC

PU9
OZ8681

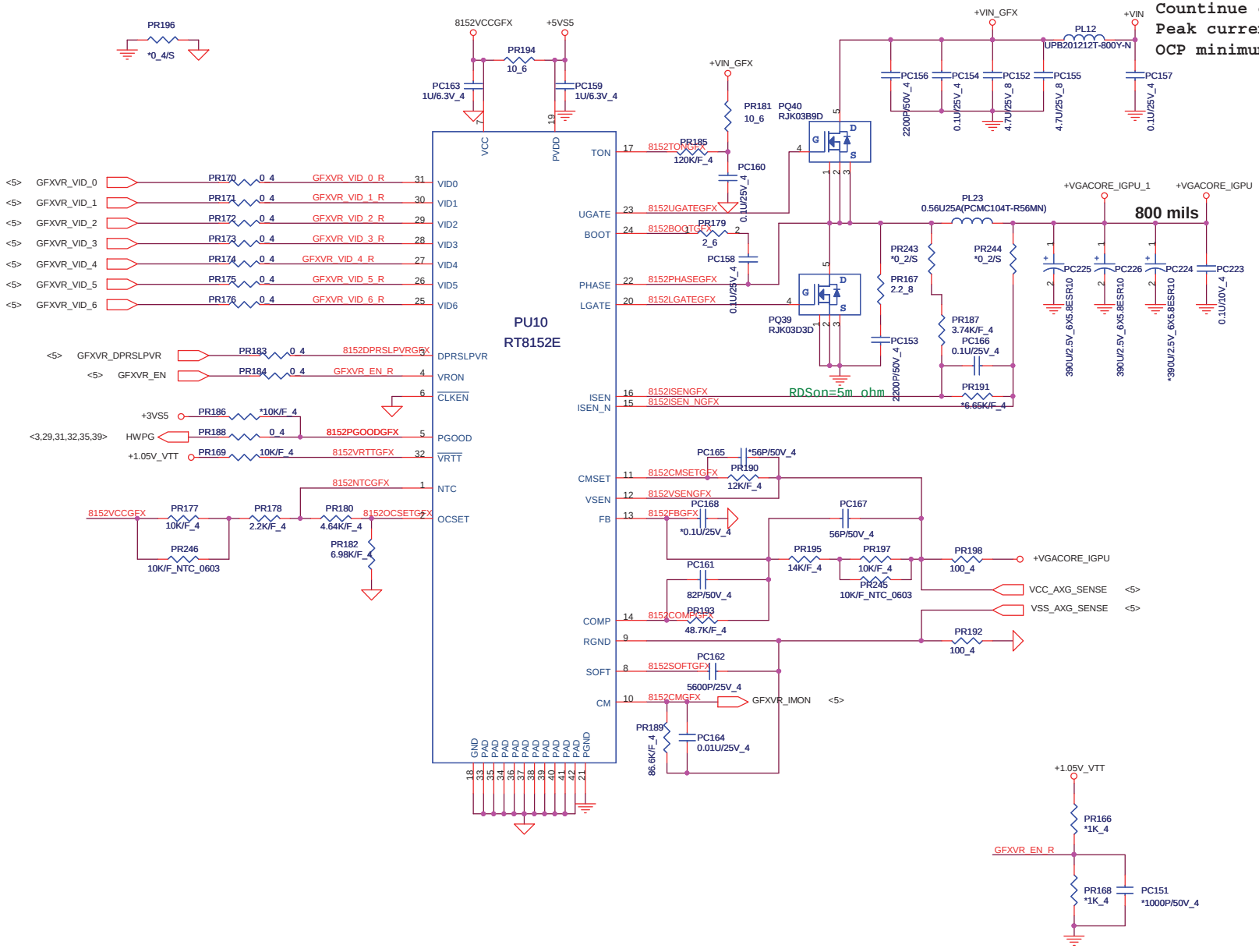
+VA	
+VH28	<36>
+VAD_1	<36>
+3VPCU	<7,20,28,29,31>
+5VPCU	<29,31>
+BATCHG	

PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (OZ8681)	1A

Date: Sunday, September 19, 2010 Sheet 37 of 39

+VGA_UMA +/- 5%
Countinue current:12A
Peak current:18A
OCP minimum 22A



PROJECT : R12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	UMA GPU CORE (RT8152C)	1A

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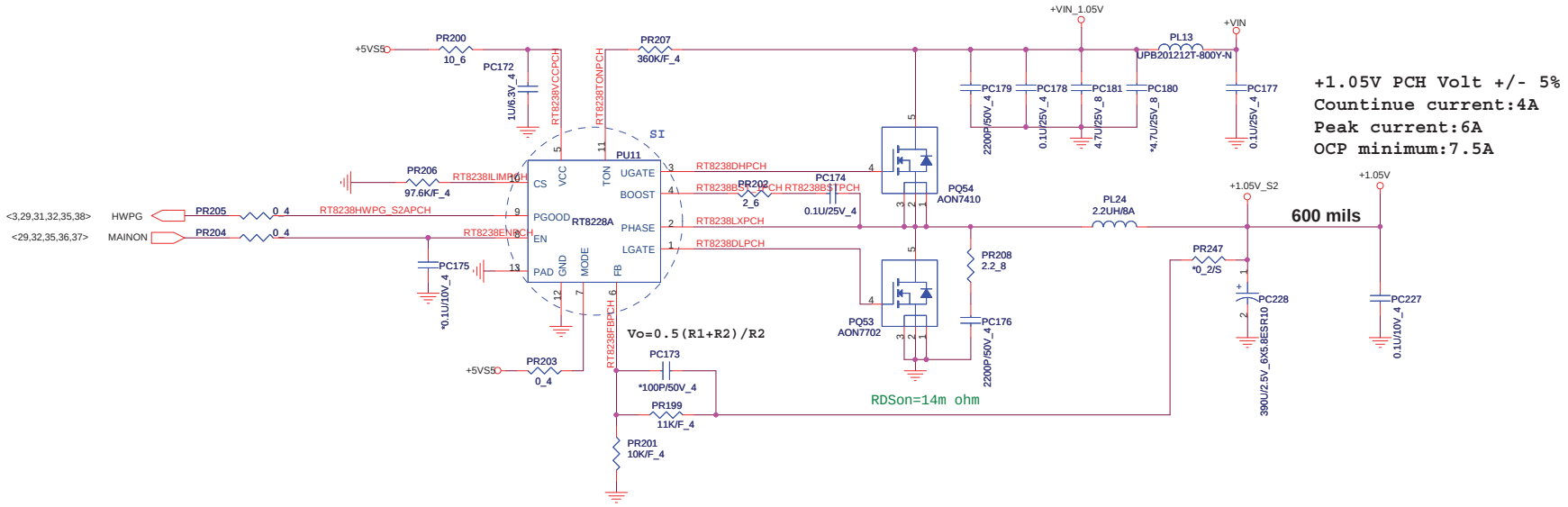

PROJECT : R12 Quanta Computer Inc.			
Size: Custom	Document Number: +1.05V (RT8238A)		Rev: 1A
Date: Sunday, September 19, 2010	Sheet 39 of 39		