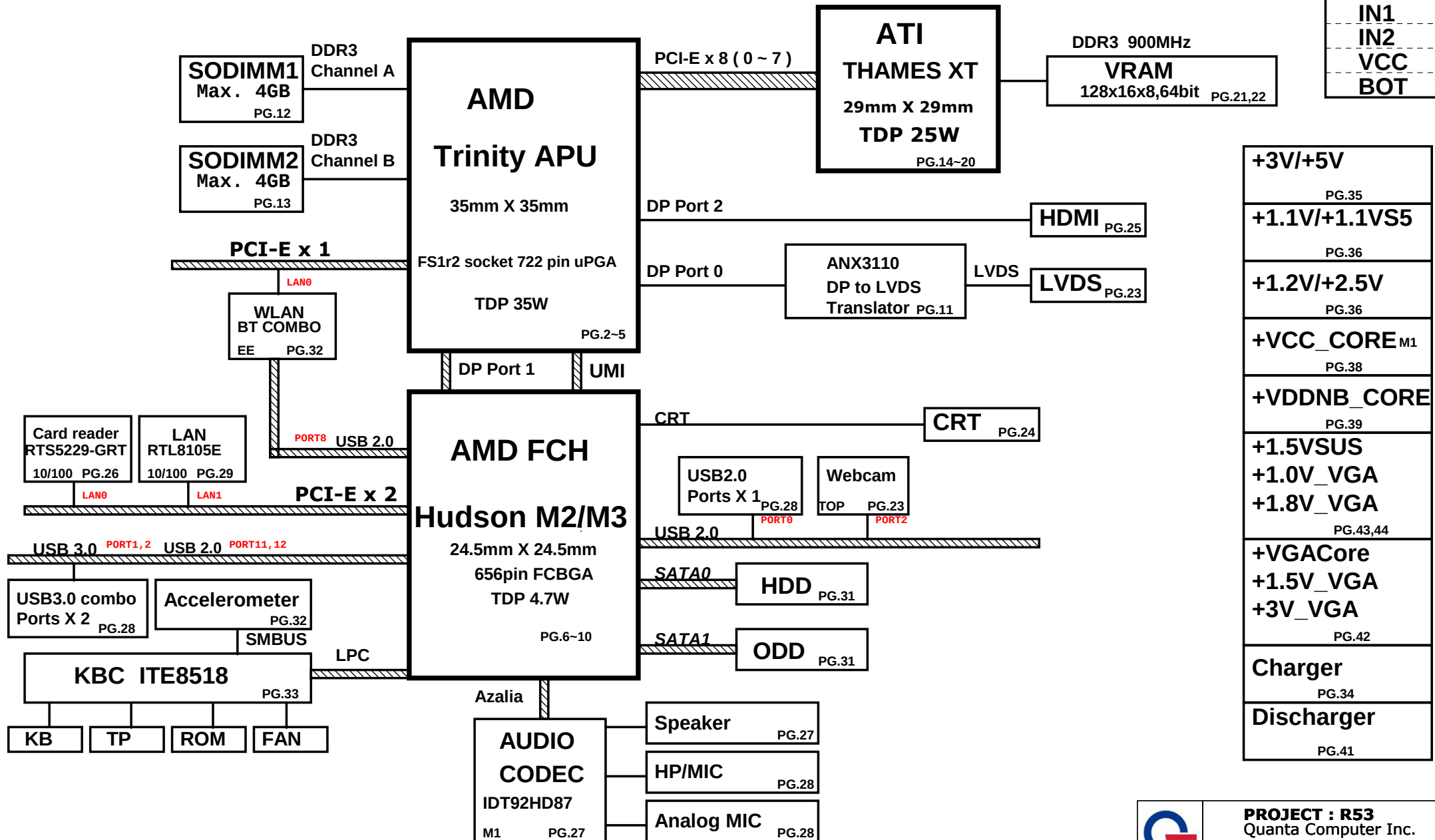


R53 AMD Comal UMA/Muxless SYSTEM DIAGRAM

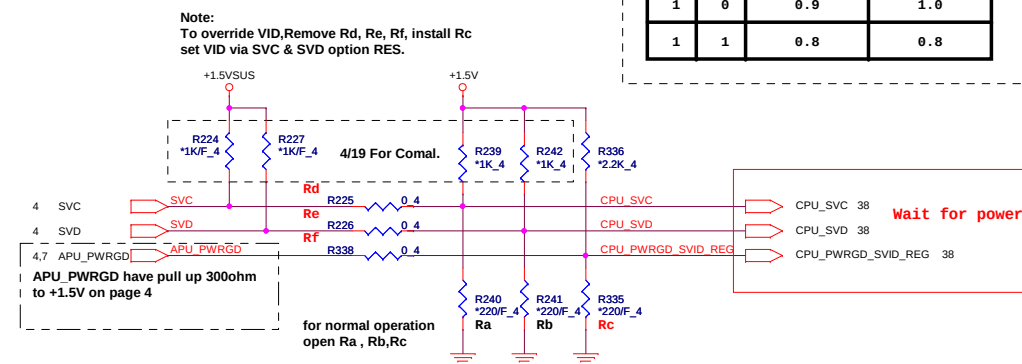
Stackup

TOP
GND
IN1
IN2
VCC
BOT



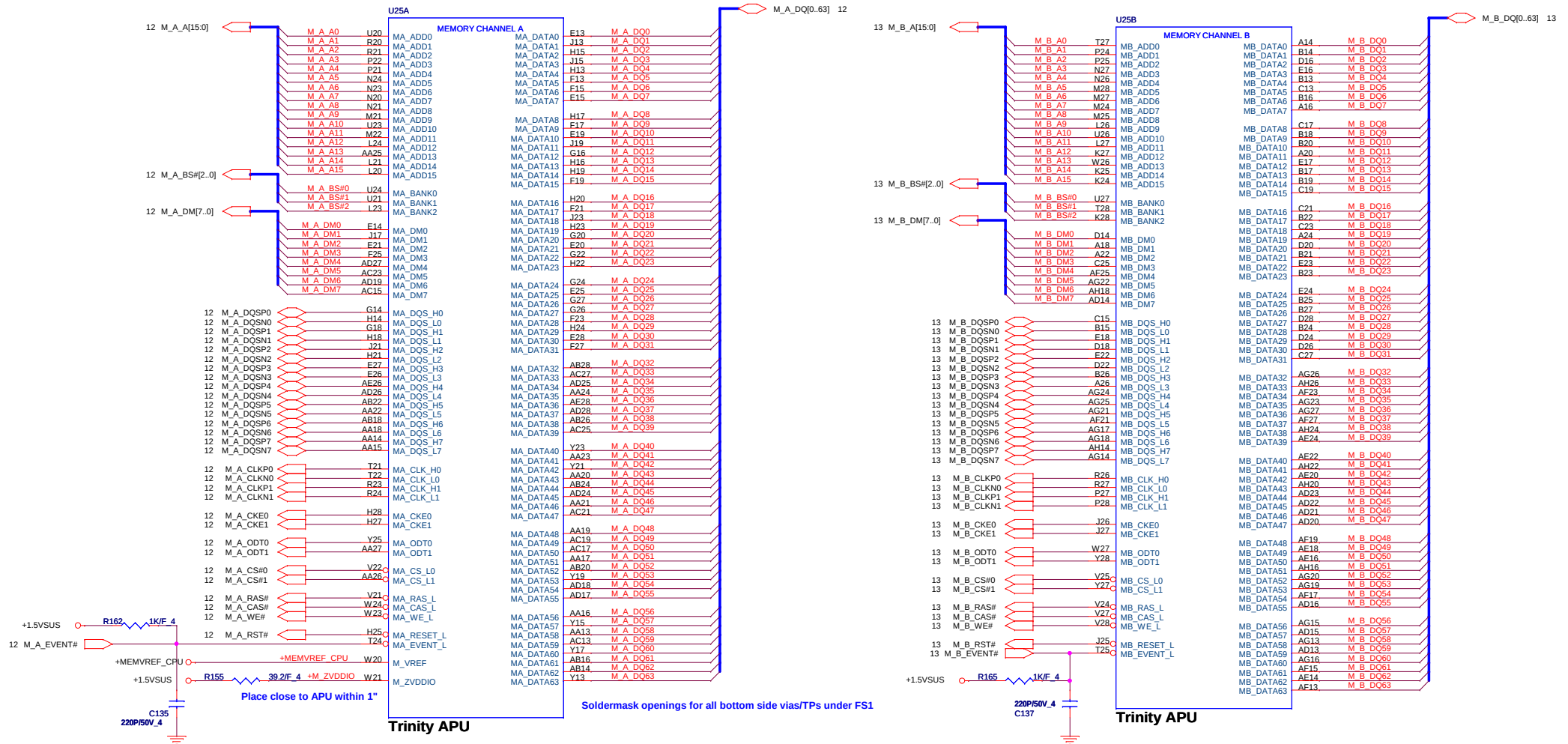


		BOOT VOLTAGE	
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8



PROJECT : R53
Quanta Computer Inc.

Size Custom	Document Number Llano PCIE/UMI/GPP	Rev 1A
Date: Monday, November 14, 2011		Sheet 2 of 44

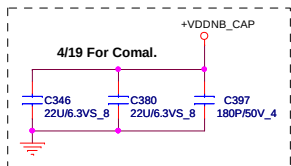
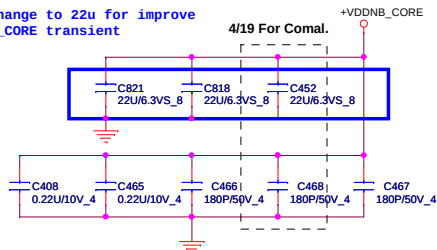


APU POWER TABLE

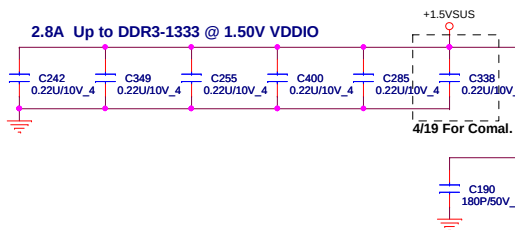
PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

SI , change to 22u for improve
+VDDNB_CORE transient

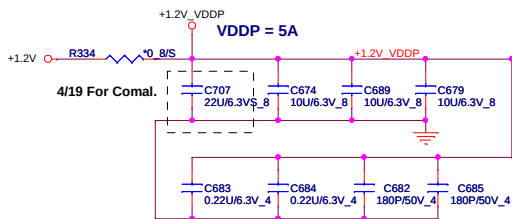
4/19 For Comal.



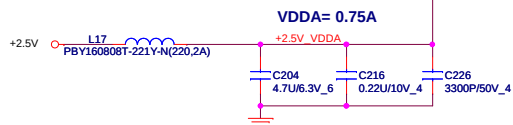
2.8A Up to DDR3-1333 @ 1.50V VDDIO



VDDP = 5A



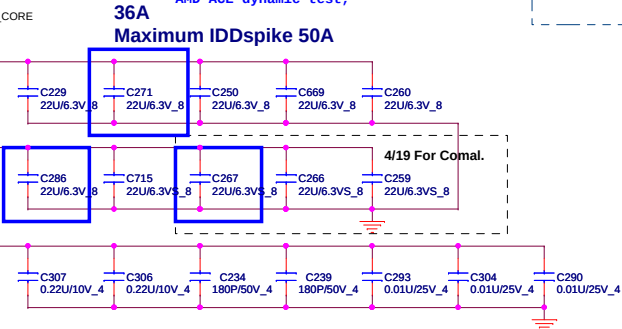
VDDA= 0.75A



Trinity APU

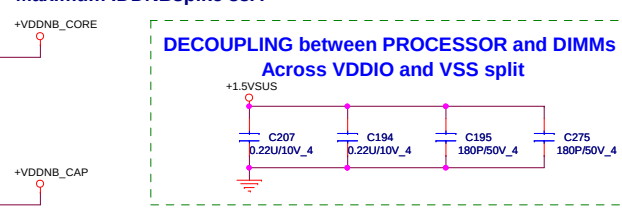
36A

Maximum IDDspike 50A

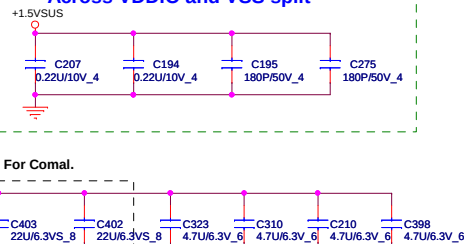


25A

Maximum IDDNBSpike 33A

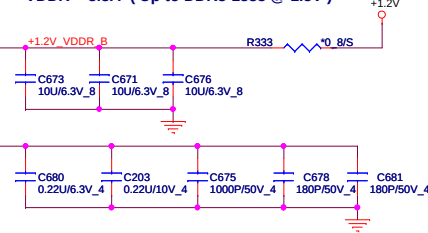


DECOUPLING between PROCESSOR and DIMMs
Across VDDIO and VSS split

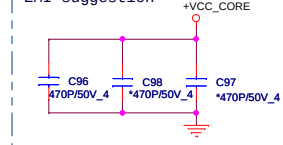


If the VSS plane is cut to create a VDDIO plane,
ceramic capacitors are connected across
the VDDIO and VSS plane split as follows

VDDR = 3.3A (Up to DDR3-1333 @ 1.5V)



EMI suggestion



Trinity APU

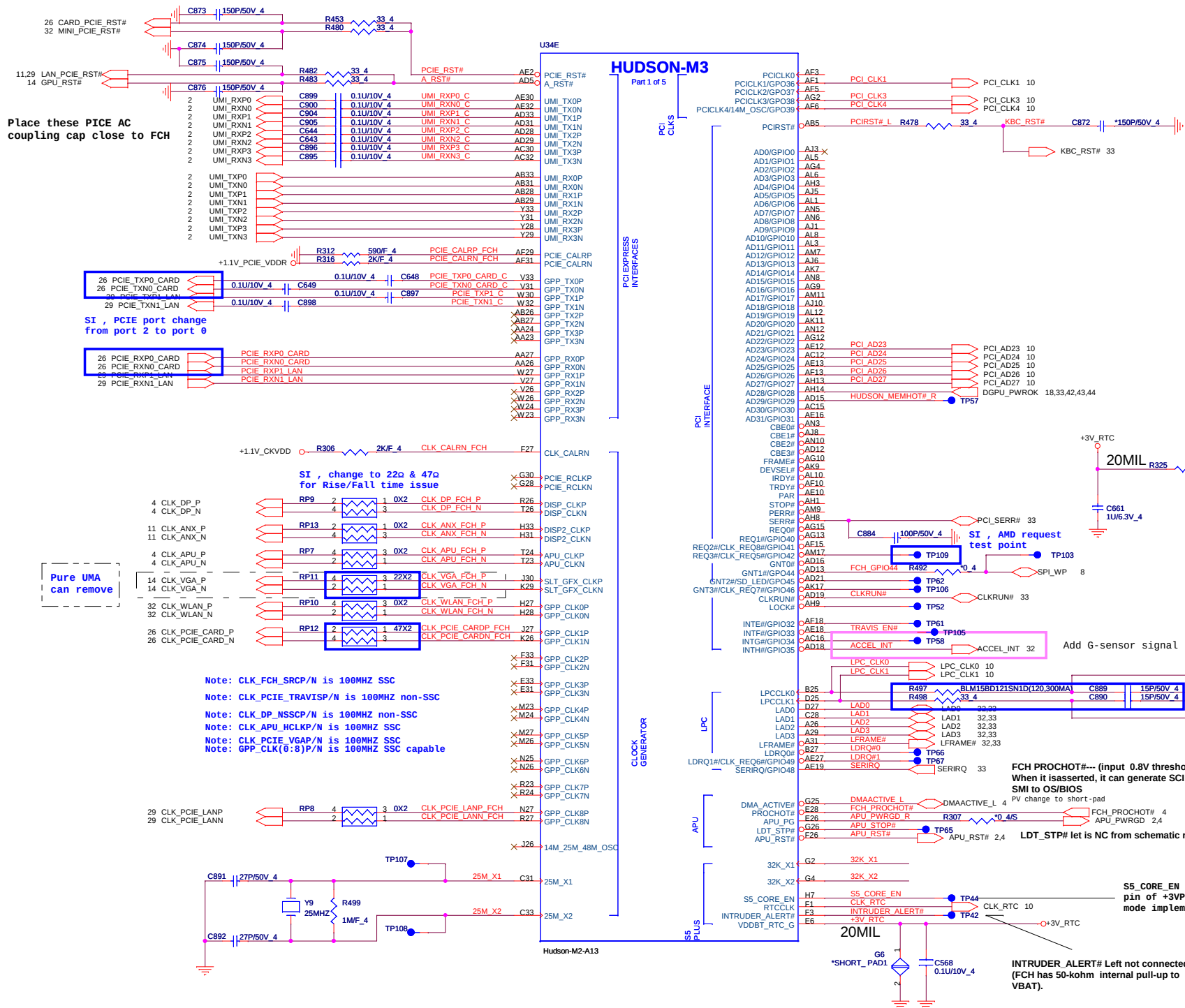


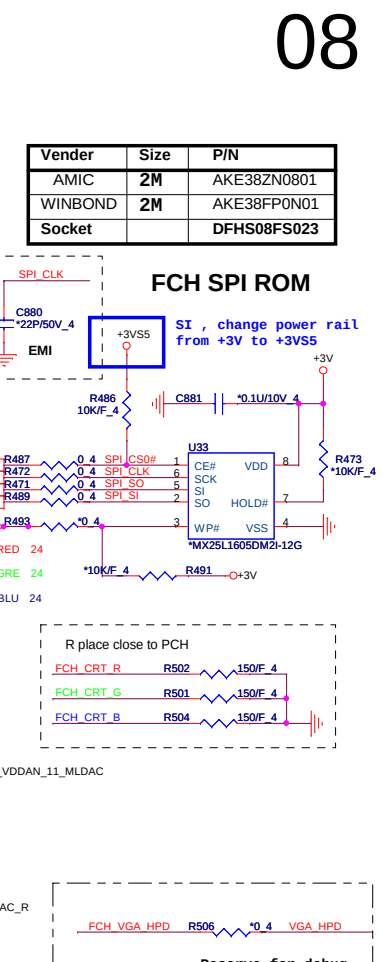
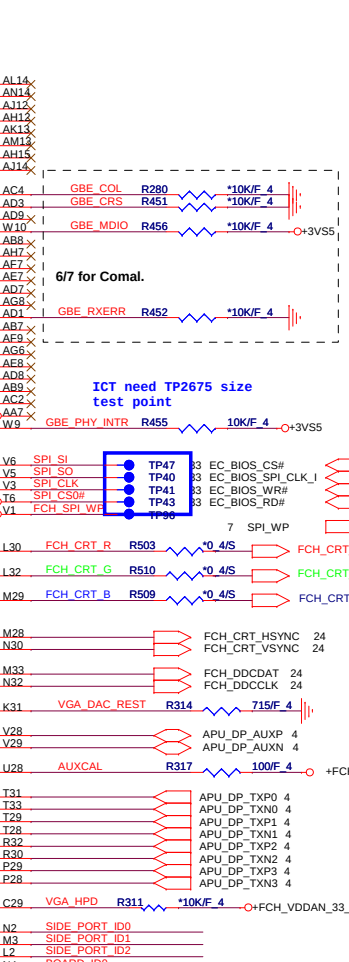
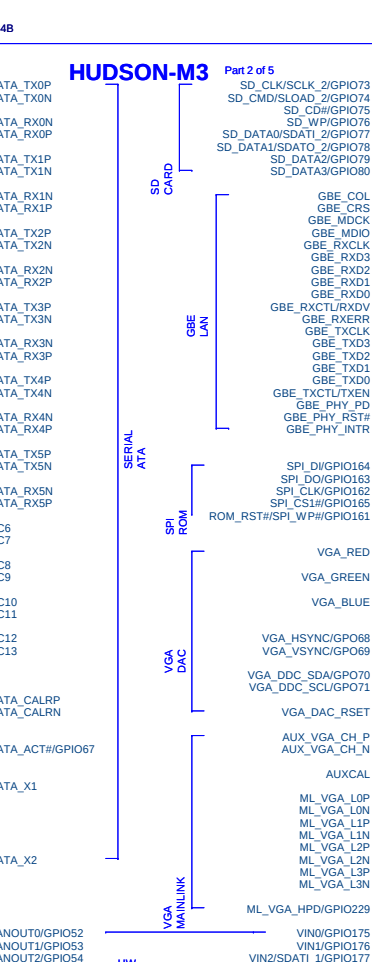
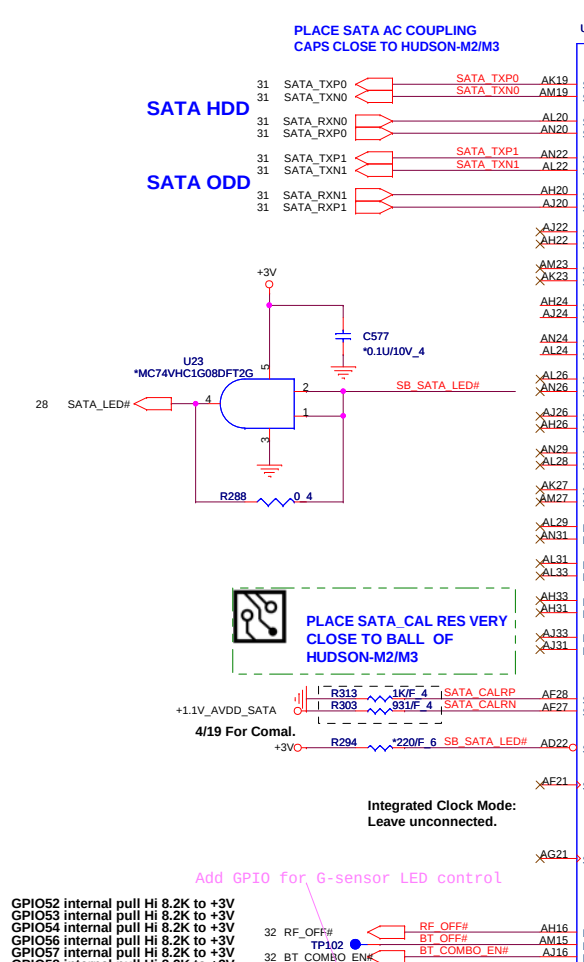
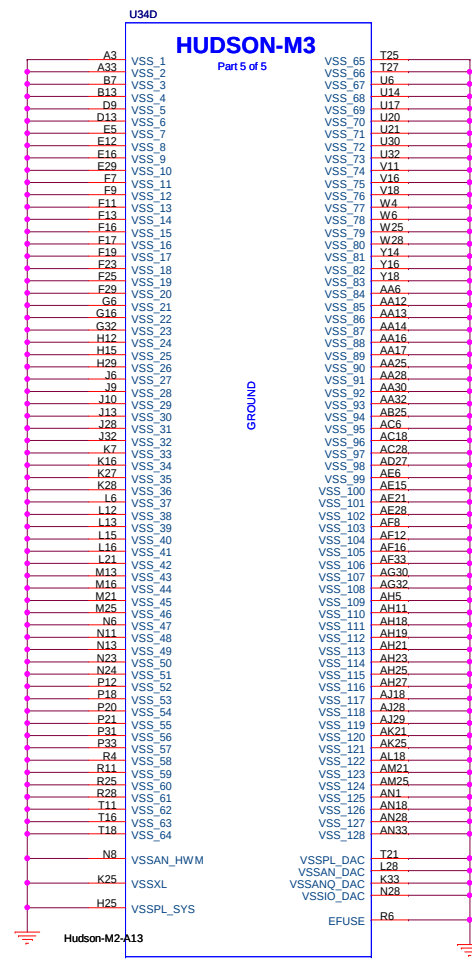
PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Llano POWER/GND	1A
Date: Friday, November 11, 2011	Sheet 5 of 44	

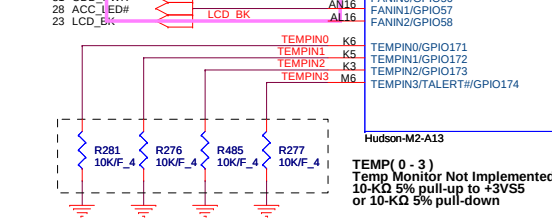


Place these PICE AC
coupling cap close to FCH

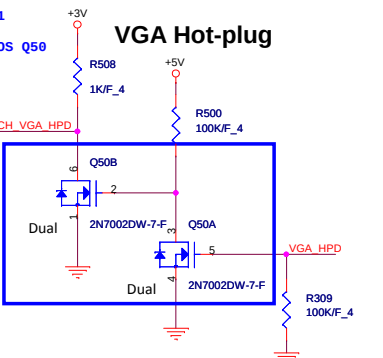
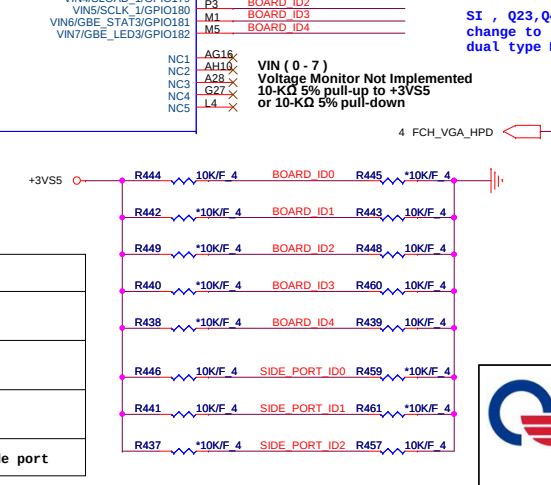




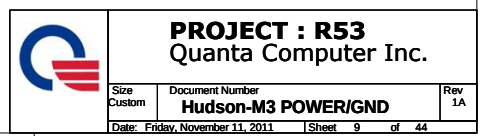
ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	0	1			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12



SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

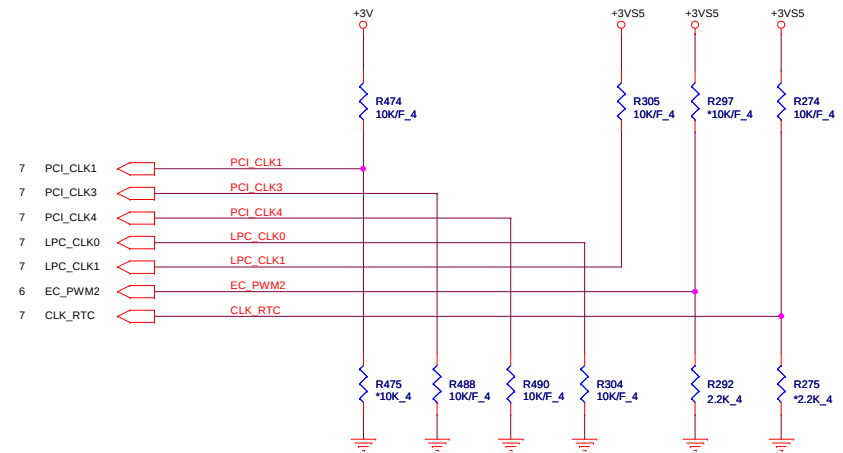


SI2 , remove discharge circuit
SI , reserve for leakage issue



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE DISABLED DEFAULT

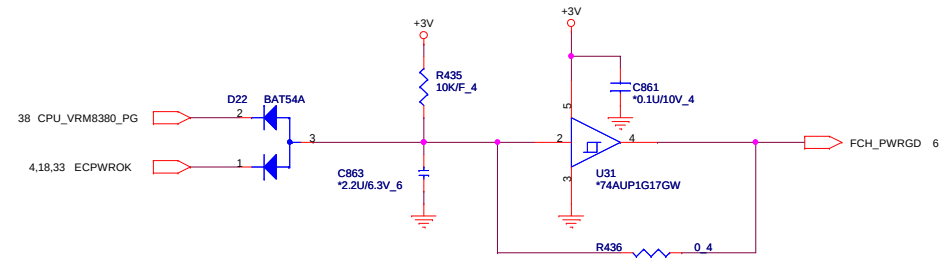
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]

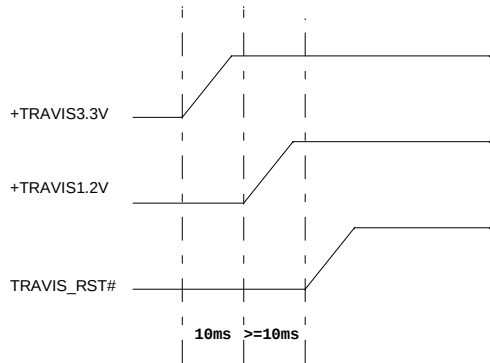


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD

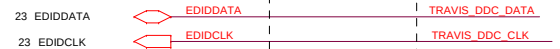
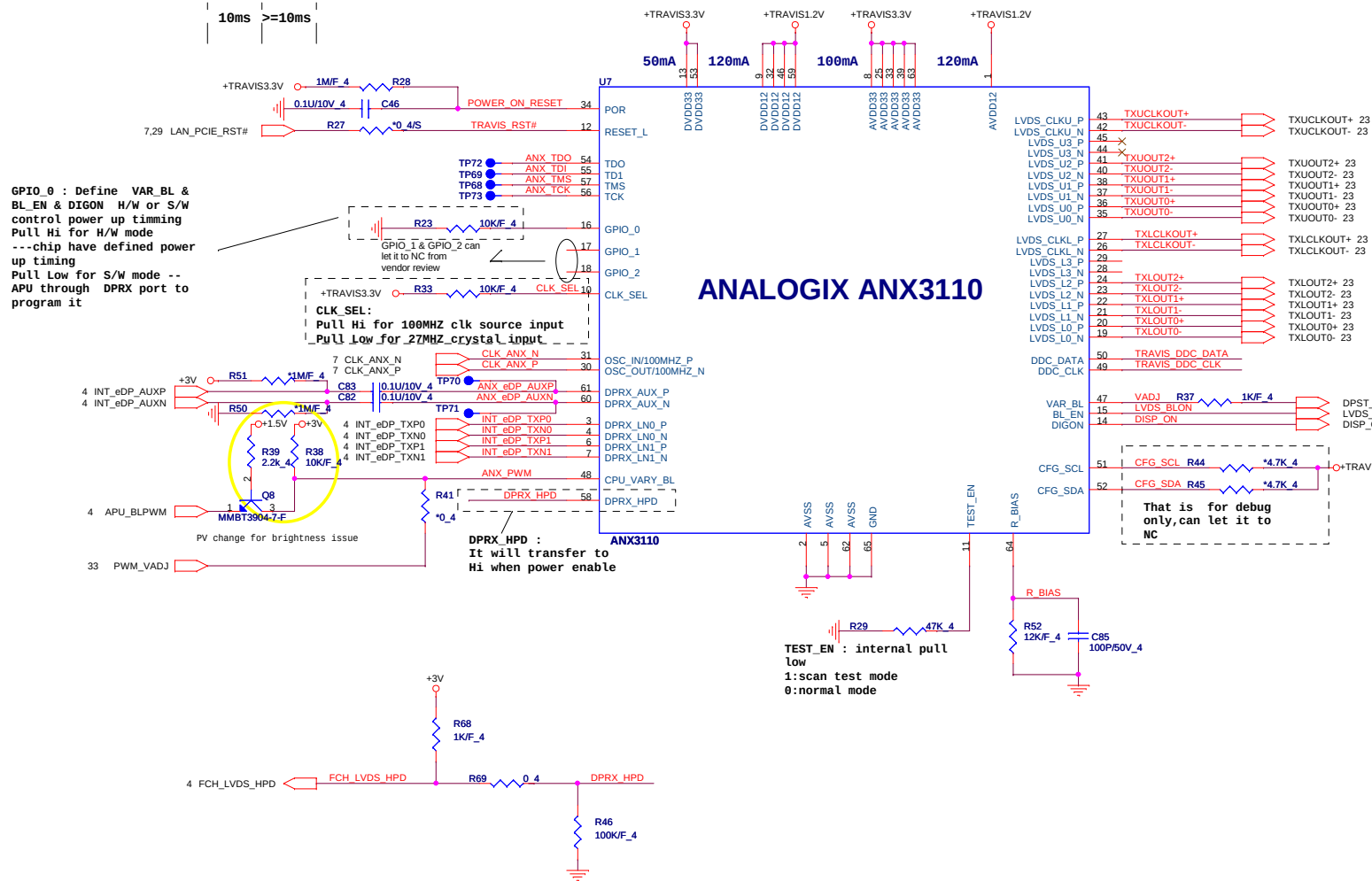


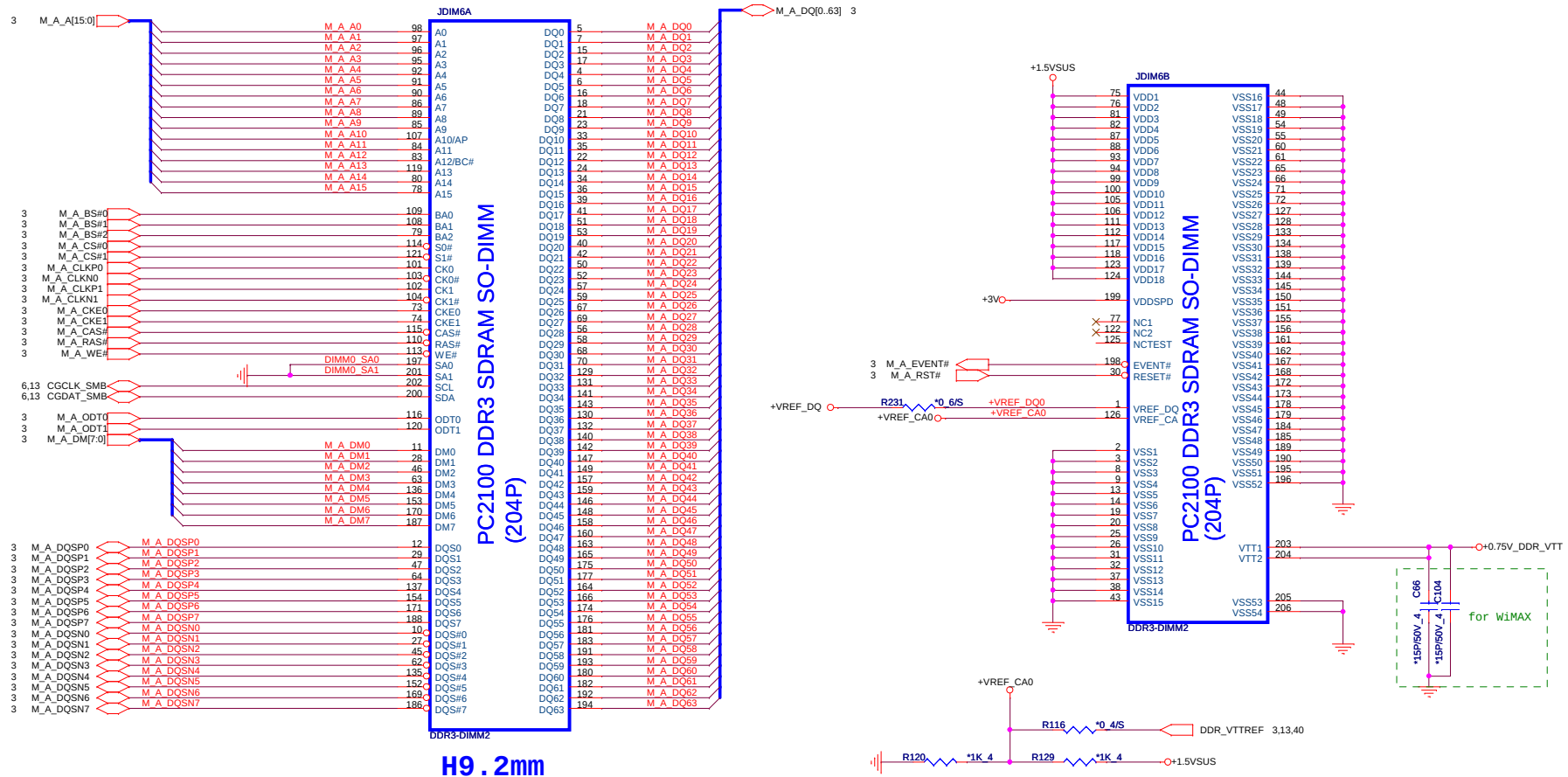
ANX3110 Power Up Sequence

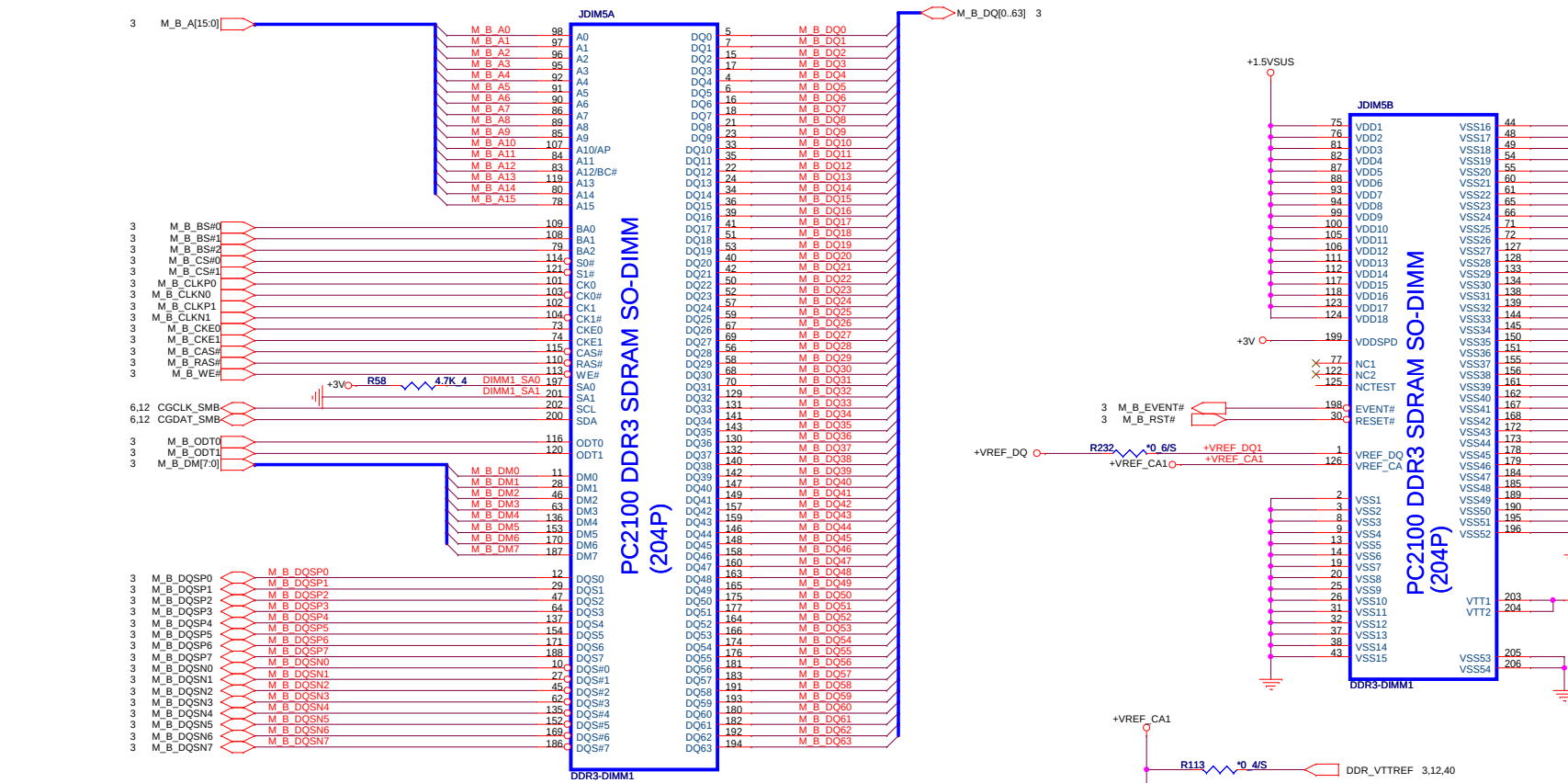


11

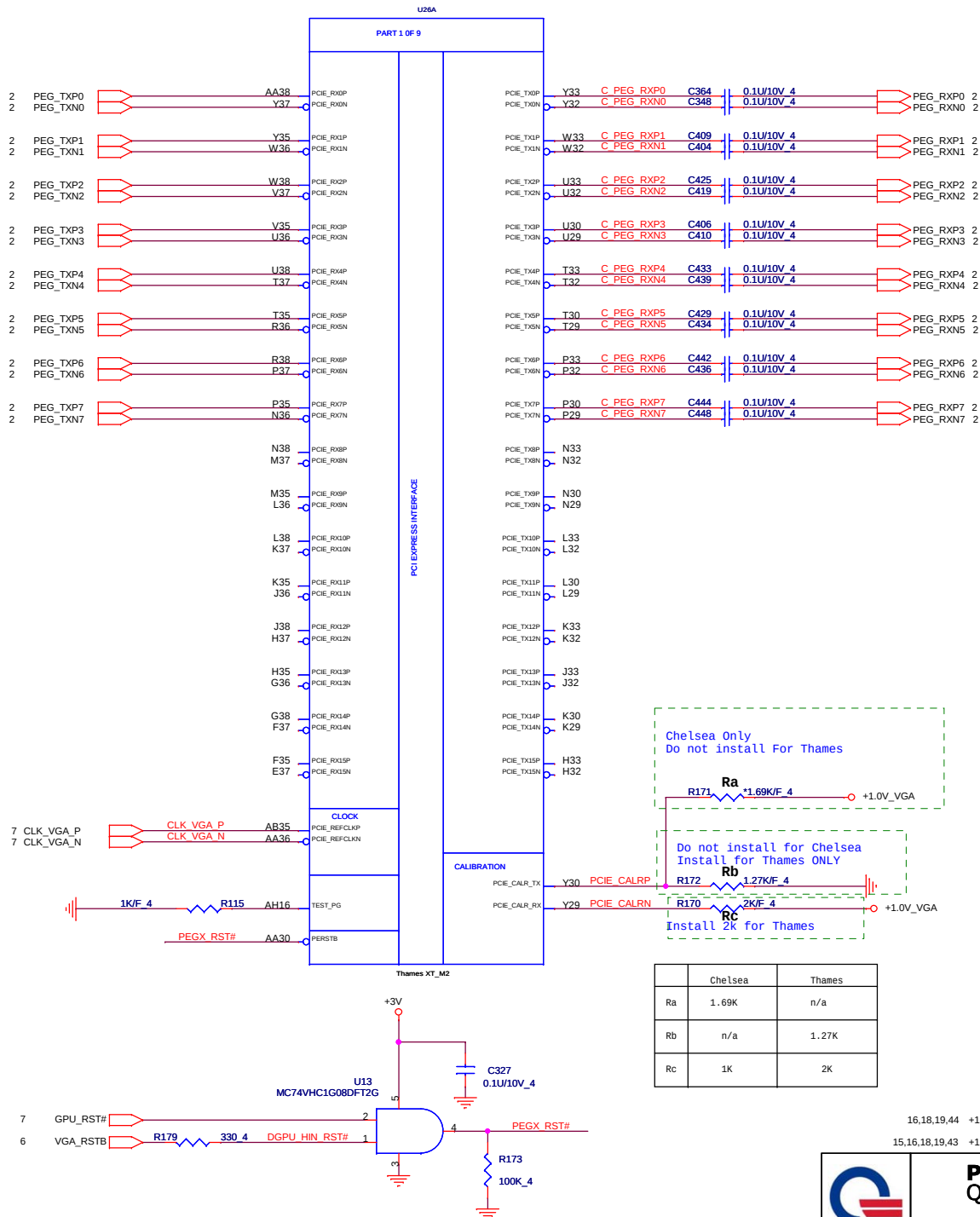
GPI0_0 : Define VAR_BL & BL_EN & DIGON H/W or S/W control power up timing Pull Hi for H/W mode ---chip have defined power up timing Pull Low for S/W mode -- APU through DPRX port to program it







12.40 +0.75V_DDR_VTT
2.3,4,5,12,40,41,44 +1.5V_SVS
2.4,6,8,9,10,11,12,14,18,23,24,25,26,27,28,29,30,31,32,33,41,42,44 +3V



16,18,19,44 +1.0V_VGA

15,16,18,19,43 +1.8V_VGA

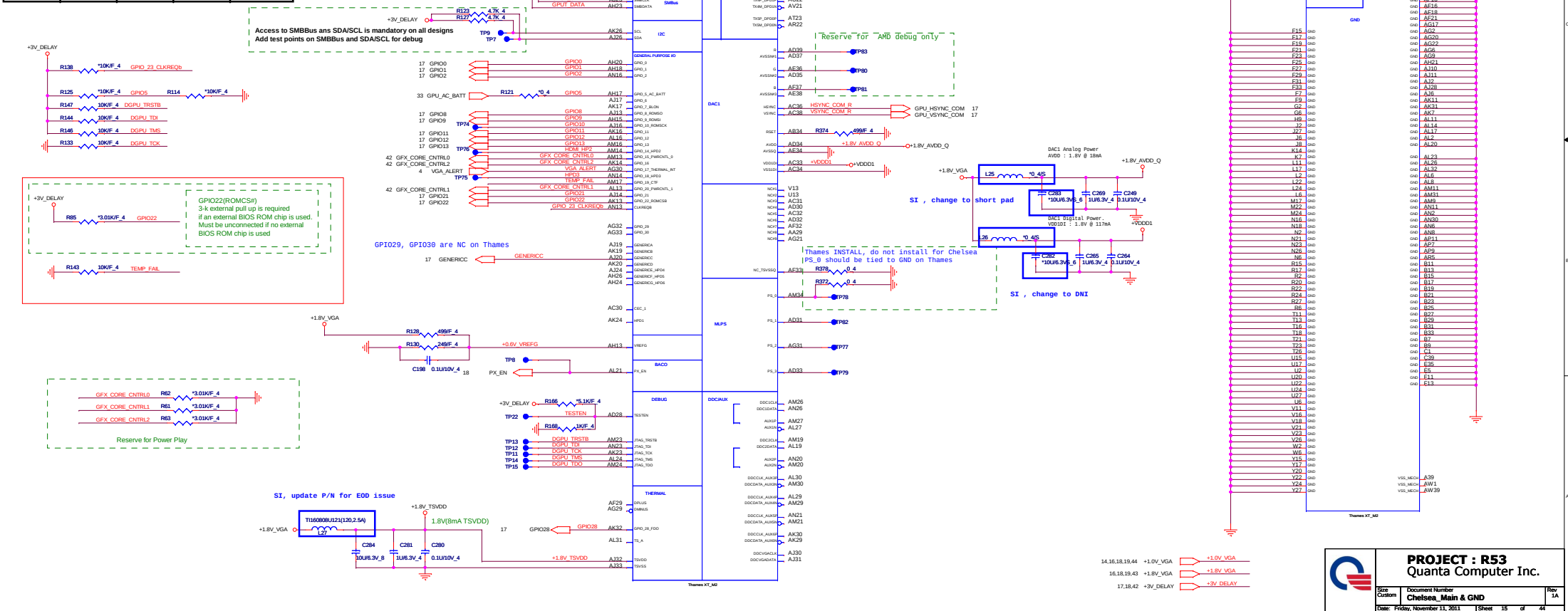


PROJECT : R53
Quanta Computer Inc.

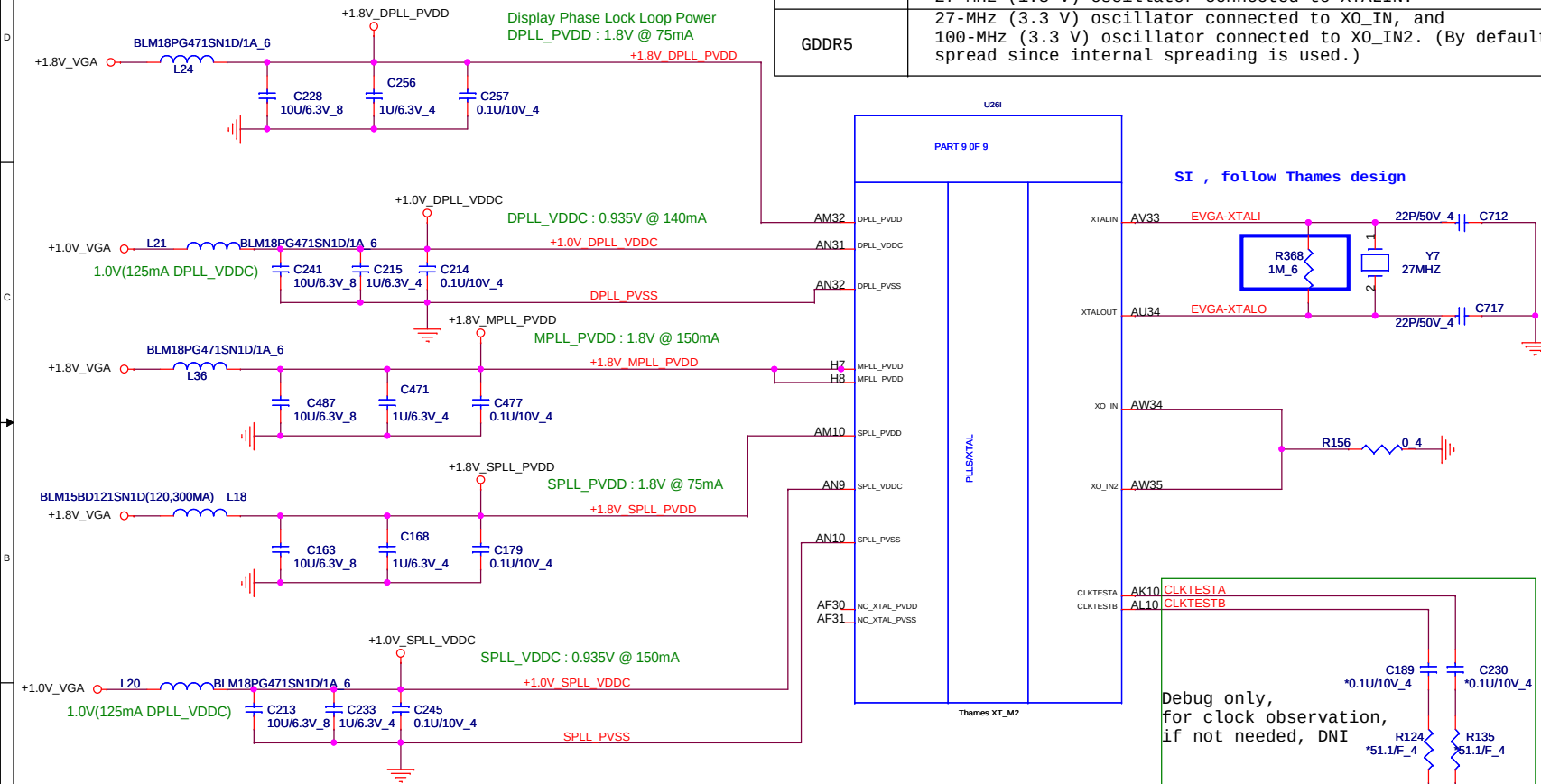
Size Custom	Document Number Chelsea_PCIE_Interface	Rev 1A
Date: Monday, November 14, 2011 Sheet 14 of 44		

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix- D die	64Mx16 *8, 900MHz	H5TQ16630FR-11C
0001	Micron- G die	64Mx16 *8, 900MHz	MT41J64M15JT-1076:G
0010	Samsung- G die	64Mx16 *8, 900MHz	K4W16646E-BC11
0011	Hynix- D die	128Mx16 *8, 900MHz	H5TQ26630FR-11C
0100	Micron- D die	128Mx16 *8, 900MHz	MT41J128M16HA-1076:D
0101	Samsung- C die	128Mx16 *8, 900MHz	K4W261646C-HC11
0110			
0111			
1000			
1001			
1010			
1011			
1100			
1101			
1110			
1111			

	GPIO16	GPIO20	GPIO15	
Thames-XT	PWRCNTL 2	PWRCNTL 1	PWRCNTL 0	VGA CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V



Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to X0_IN, and 100-MHz (3.3 V) oscillator connected to X0_IN2. (By default, this clock should not be spread since internal spreading is used.)



SI , follow Thames design

Debug only,
for clock observation,
if not needed, DNI

route 50ohms
single-ended/
100ohms diff and keep short

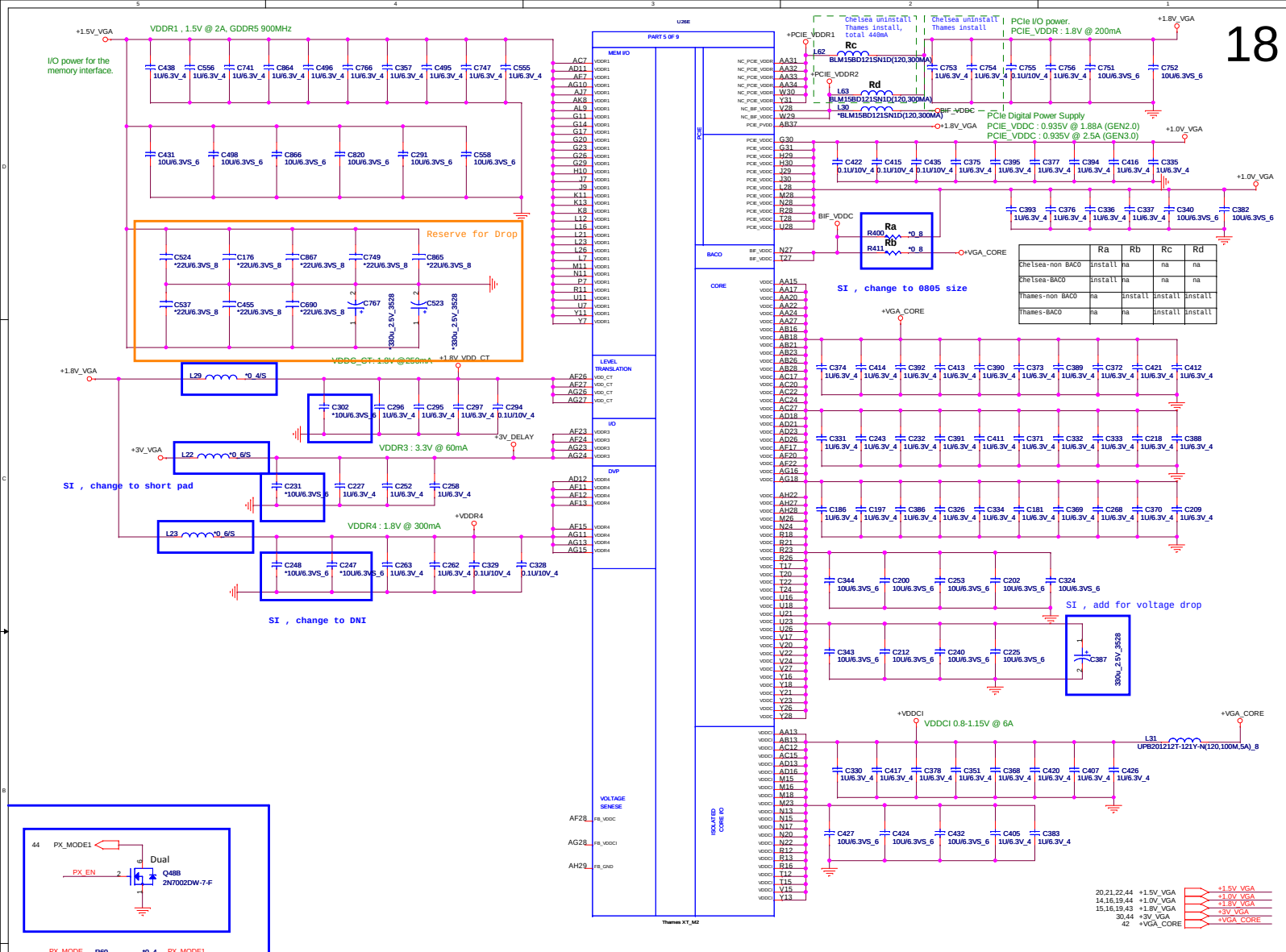
14,18,19,44 +1.0V_VGA
15,18,19,43 +1.8V_VGA



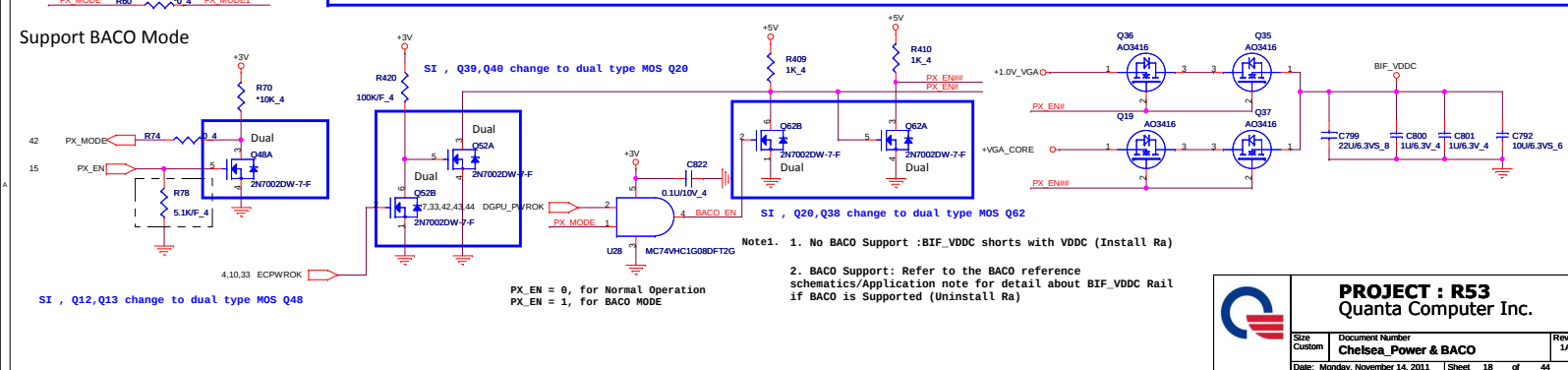
PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea XTAL	1A
Date:	Monday, November 14, 2011	Sheet 16 of 44

Size Custom	Document Number Chelsea_LVDS / STRAP	F
Date: Friday, November 11, 2011	Sheet 17 of 44	

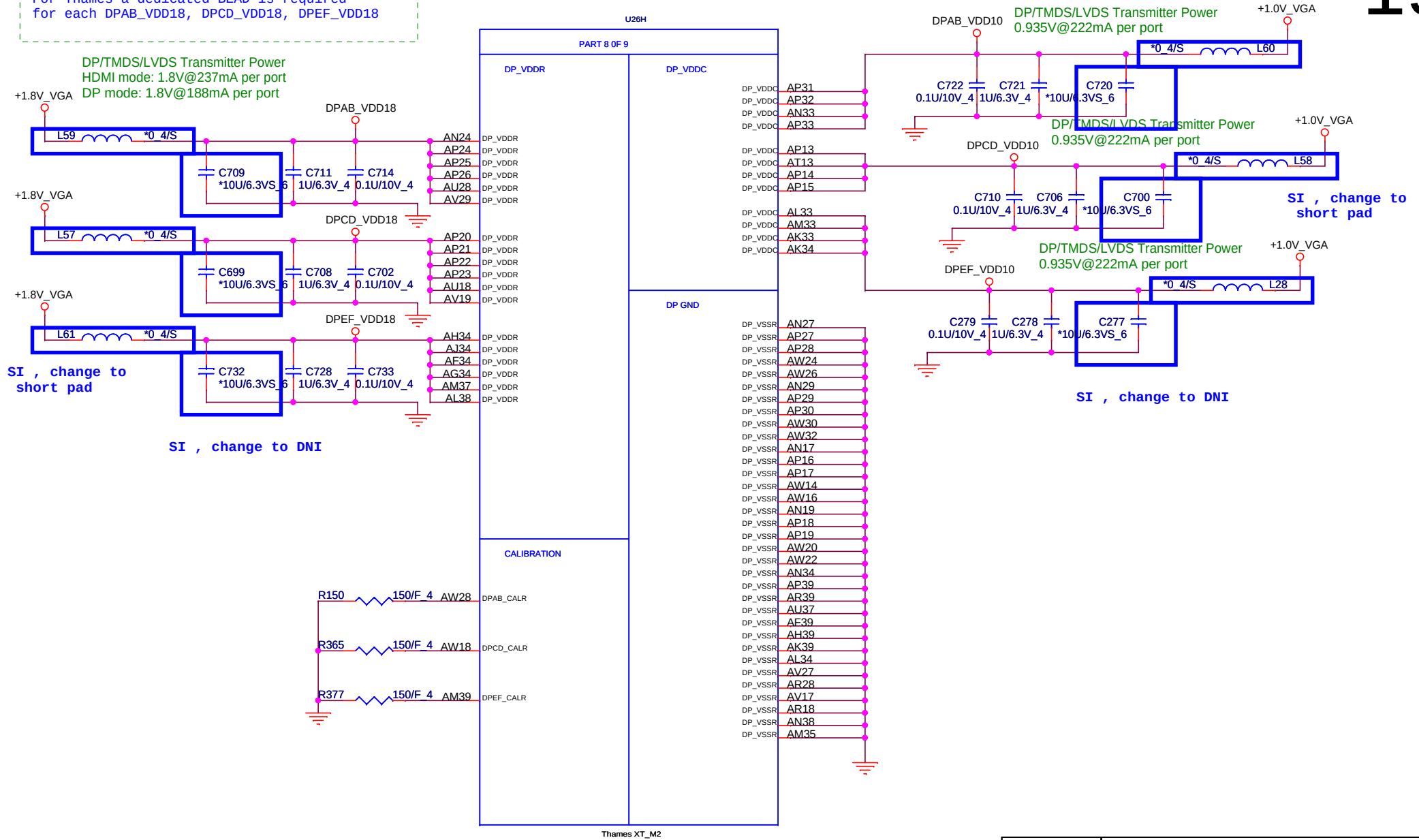


Support BACO Mode



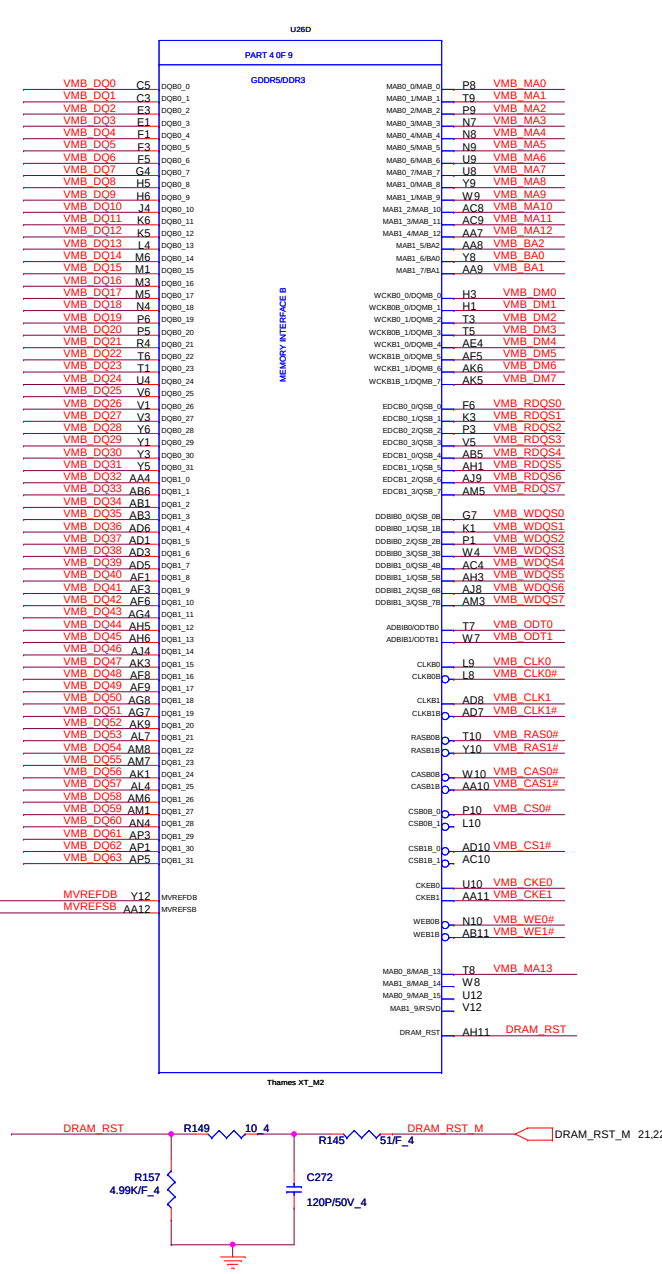
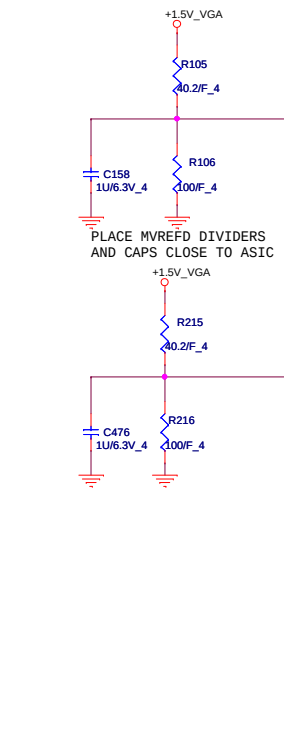
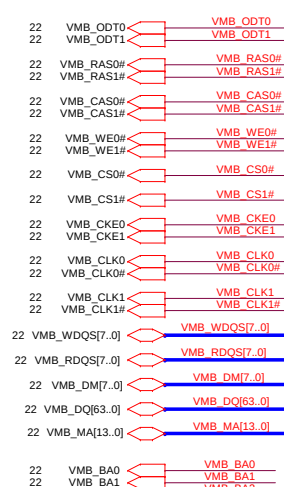
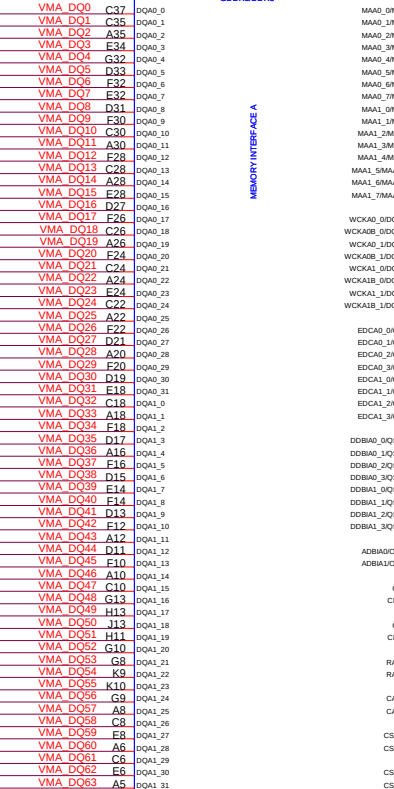
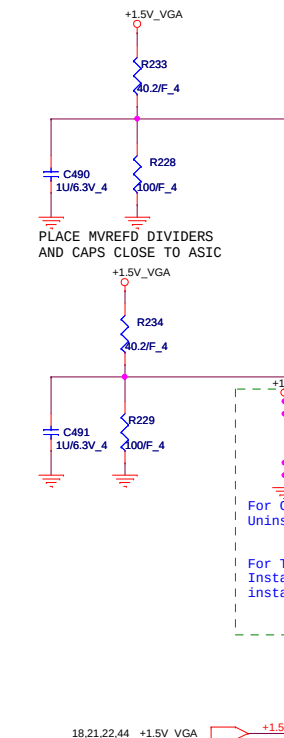
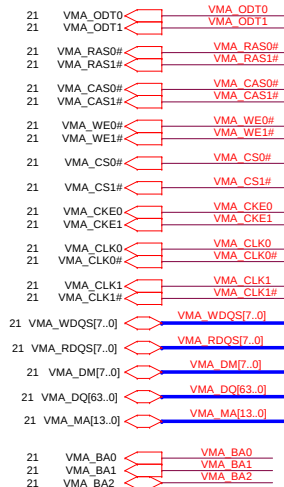
For Thames a dedicated BEAD is required for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

For Thames a dedicated BEAD is required for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10



PROJECT : R53
Quanta Computer Inc.

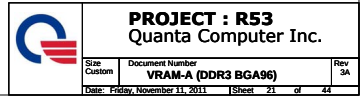
Size Custom	Document Number Chelsea_DP Powers	Rev 1A
Date: Monday, November 14, 2011	Sheet 19 of 44	

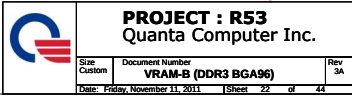


PROJECT : R53

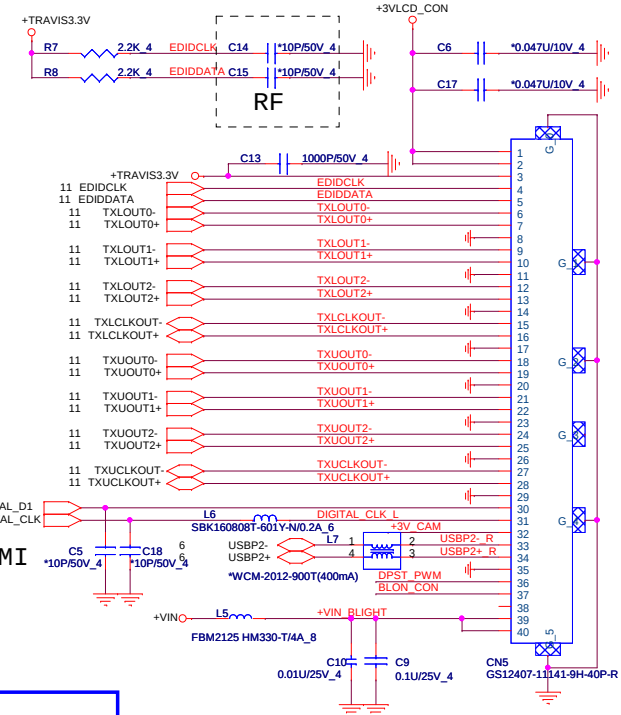
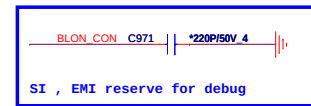
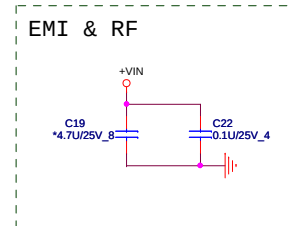
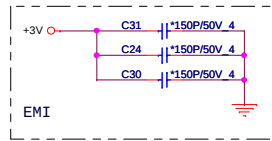
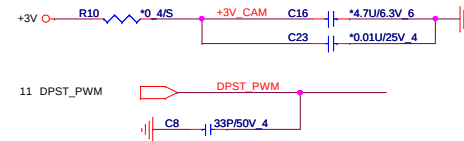
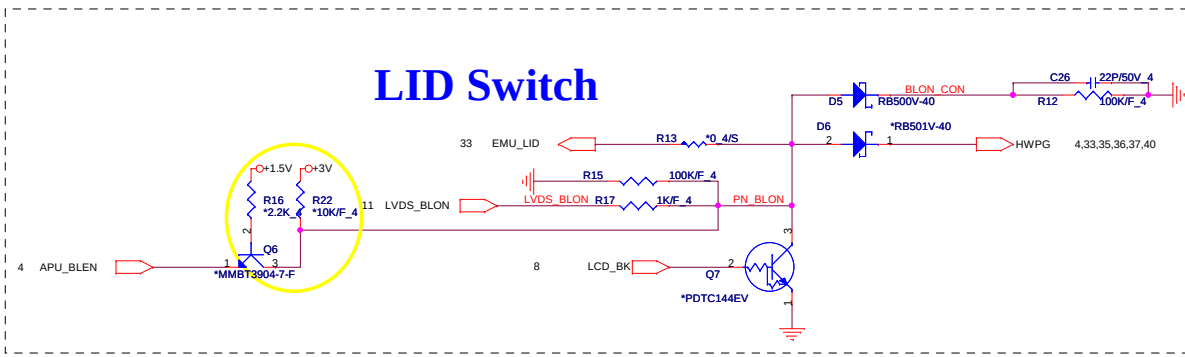
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea_MEM_Interface	1A
Date: Friday, November 11, 2011	Sheet 20 of 44	

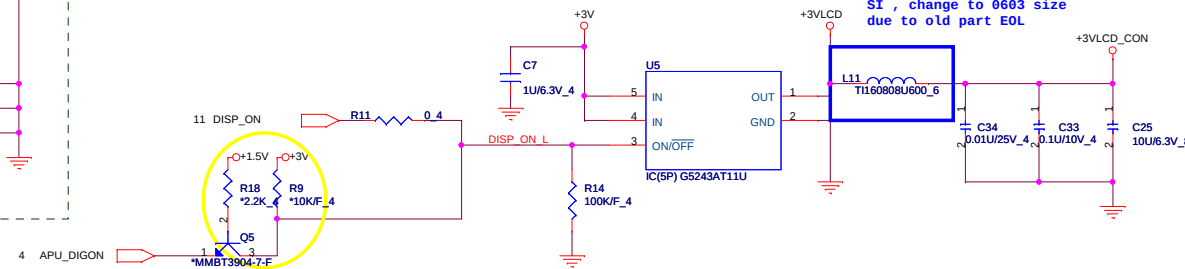
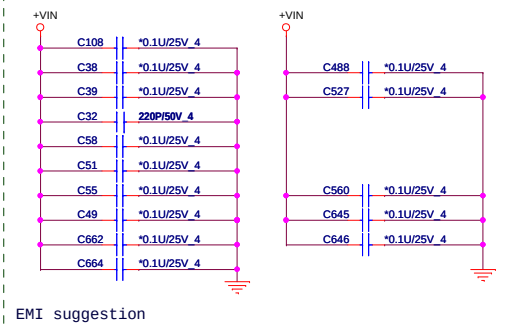


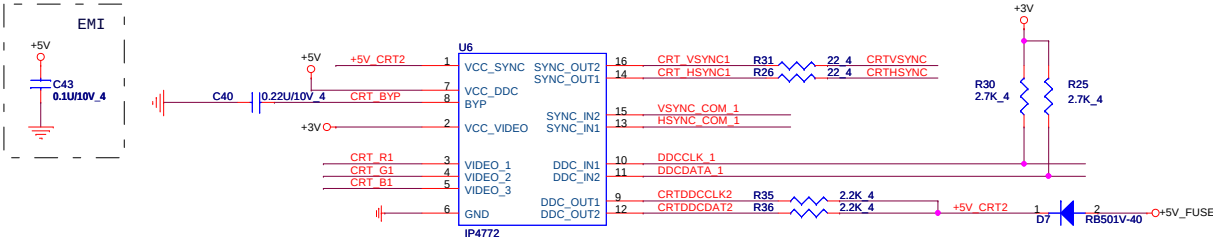
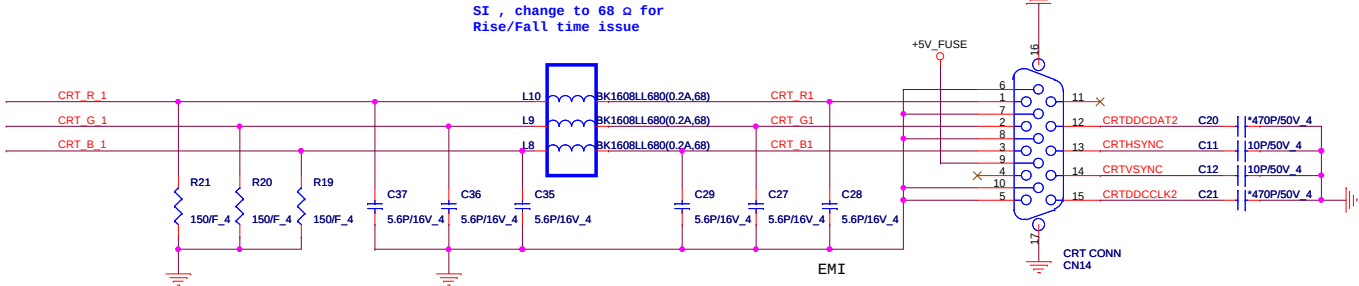
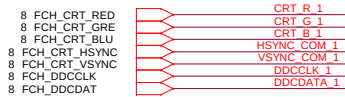


LID Switch



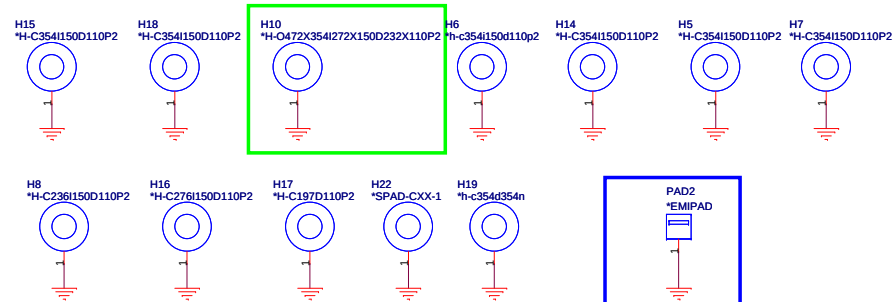
Coupling CAP.





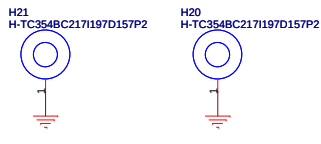
HOLE

SI2 , update footprint

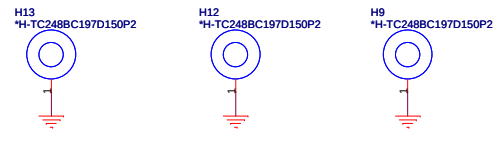


SI , add for EMI

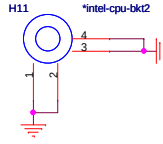
FCH NUT

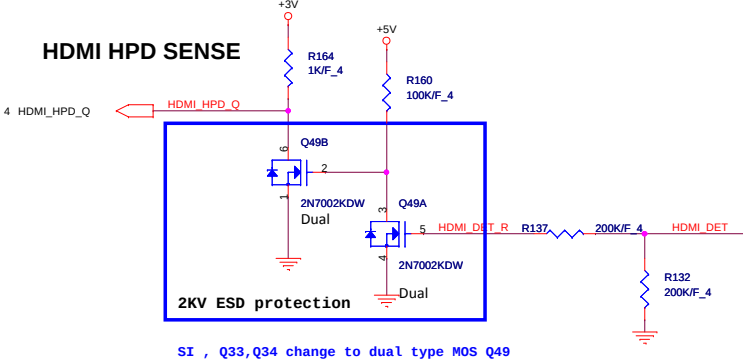
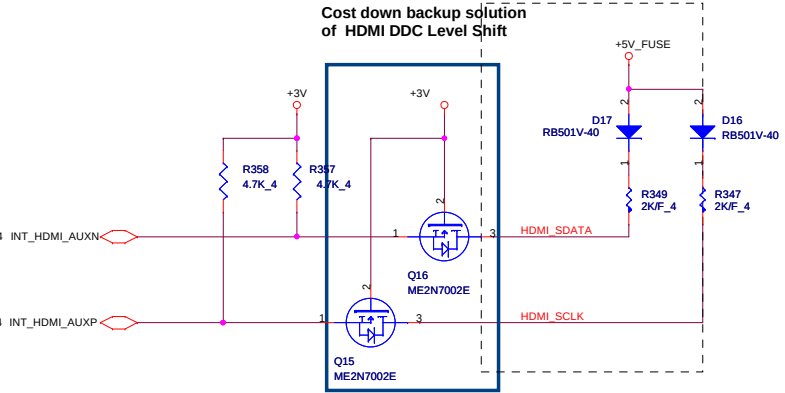
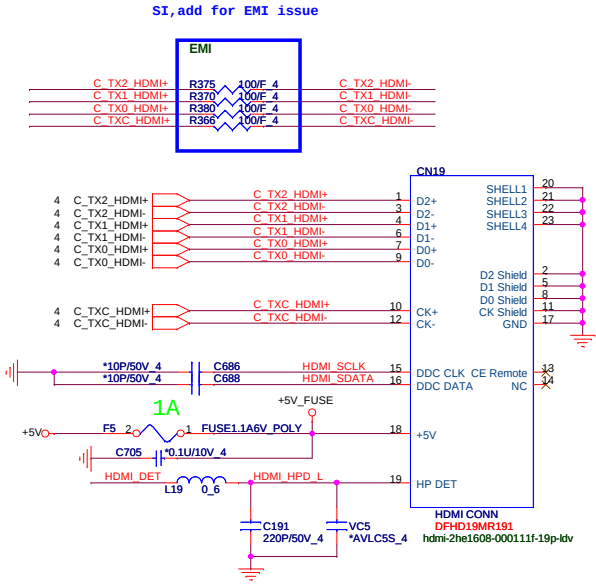
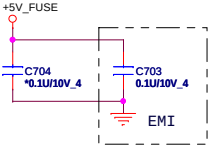
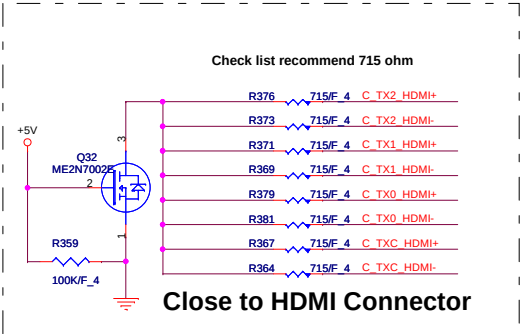


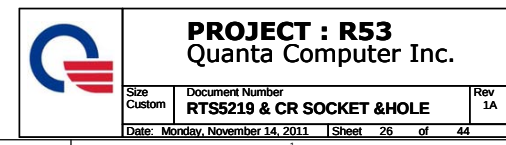
VGA BKT



APU BKT

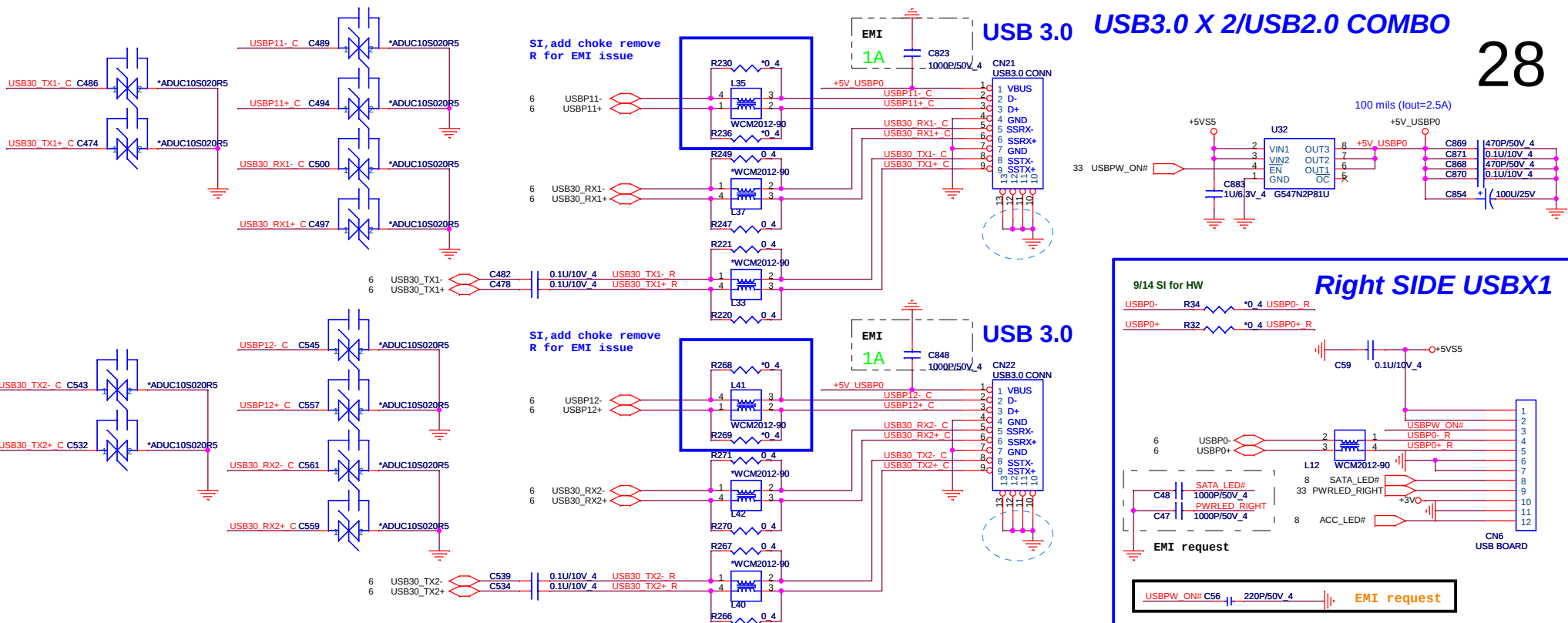




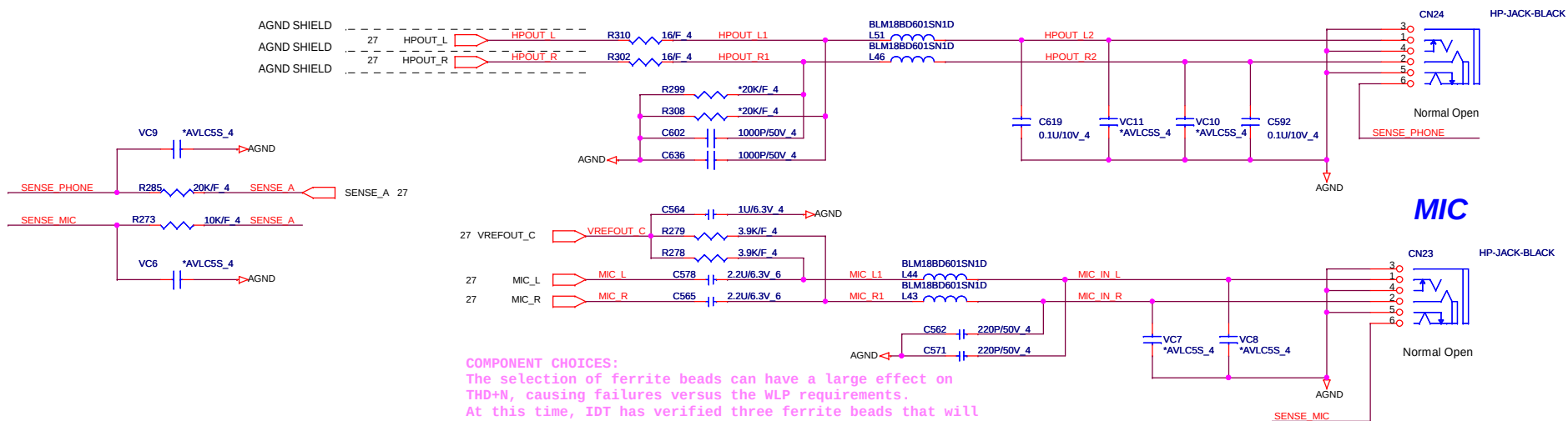




USB 3.0 USB3.0 X 2/USB2.0 COMBO



Line out



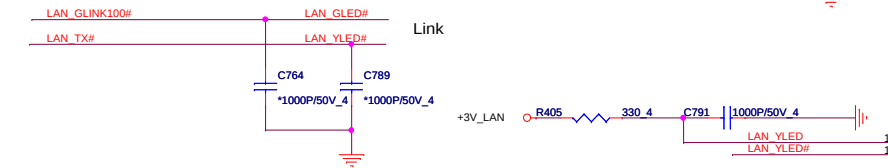
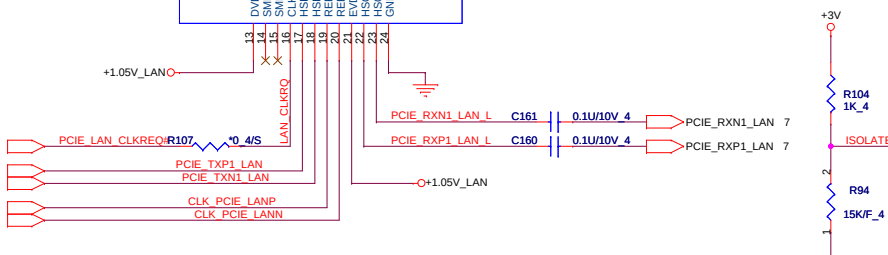
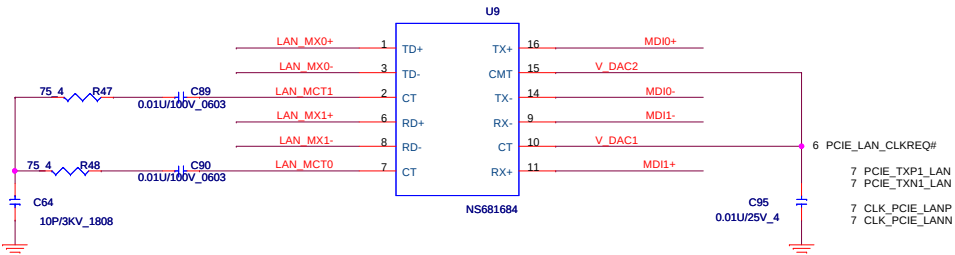
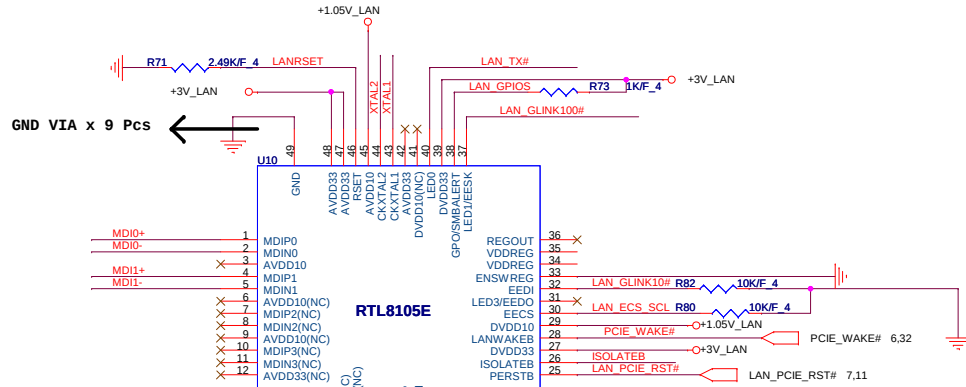
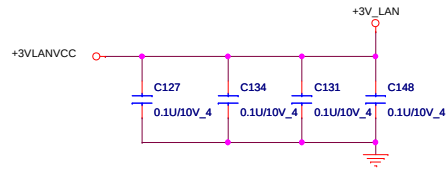
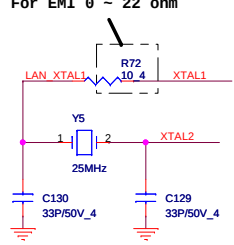
COMPONENT CHOICES:
 The selection of ferrite beads can have a large effect on THD+N, causing failures versus the WLP requirements.
 At this time, IDT has verified three ferrite beads that will meet the WLP performance requirements:
 Murata: BLM188D601SN1D
 TDK: MMZ1608Y601BTA
 Taiyo Yuden: LF BK 1608HM601-T



PROJECT : R53
 Quanta Computer Inc.

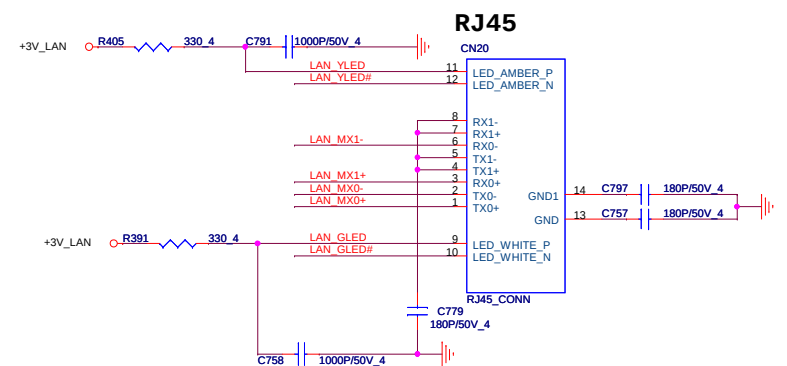
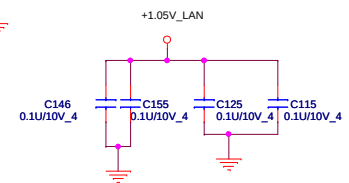
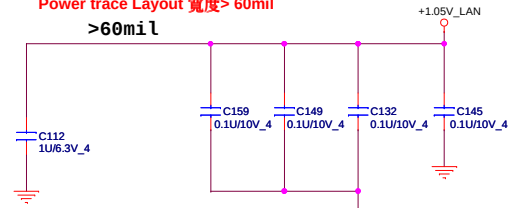
Size	Document Number	Rev
Custom	USB/BT/Audio Jack	1A
Date:	Monday, November 14, 2011	Sheet 28 of 44

For EMI $\theta \sim 22 \text{ ohm}$

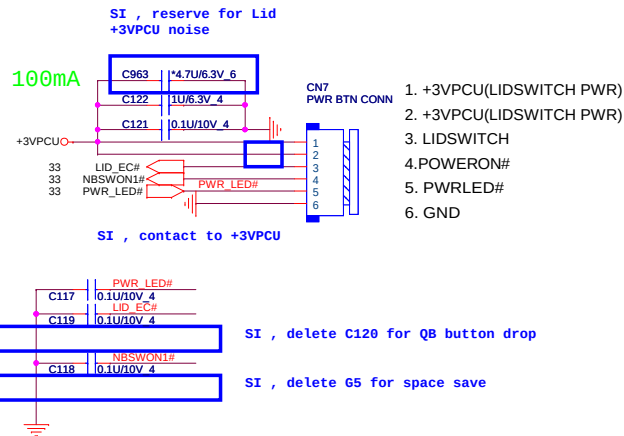


IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M)
CV-4787MZ00

Power trace Layout 寬度 > 60mil
>60mil

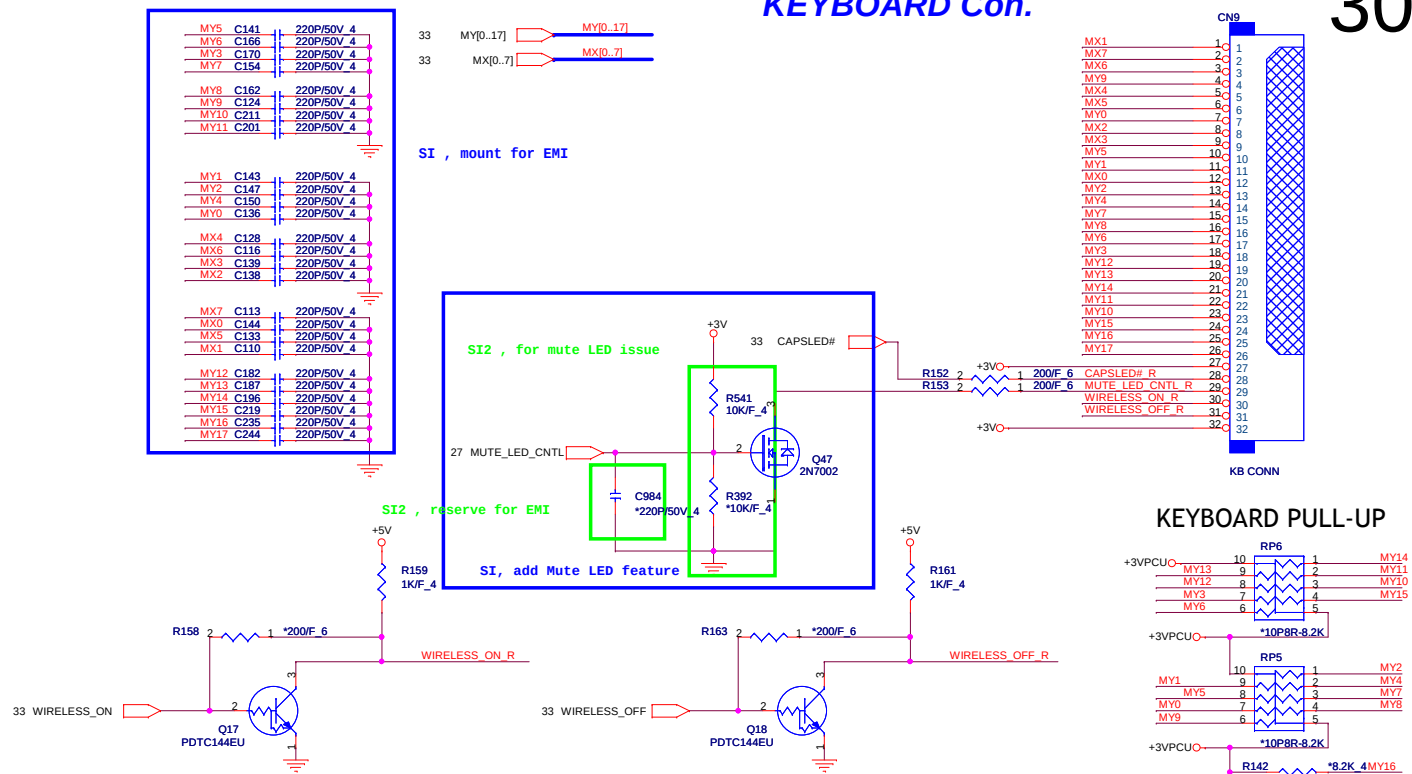


POWER BOTTON CONNECT

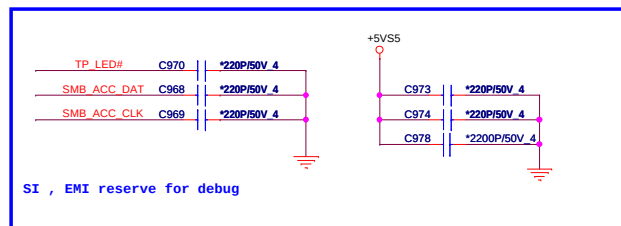


KEYBOARD Con.

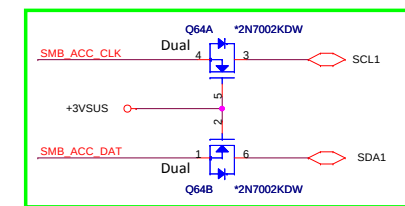
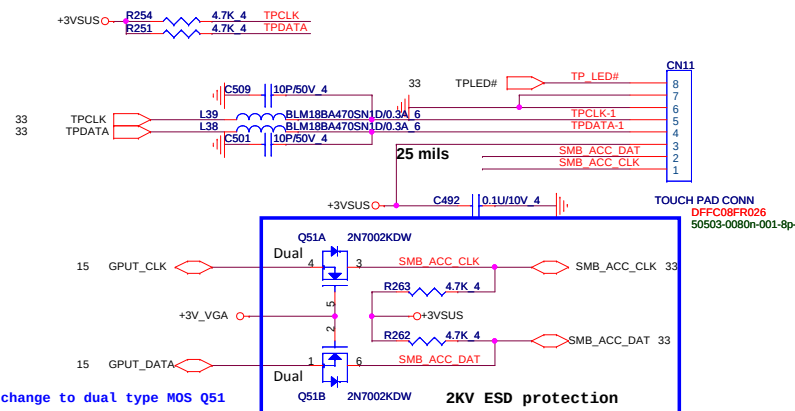
30



TOUCH PAD Con.



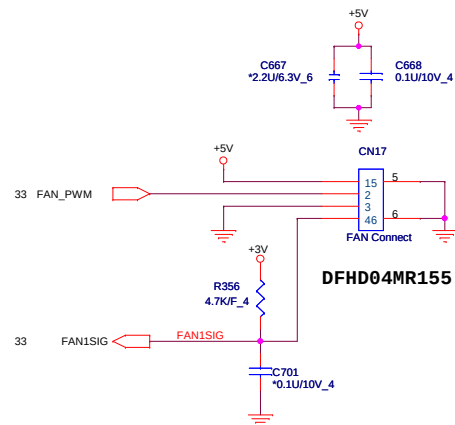
change to +3VSUS
close conn



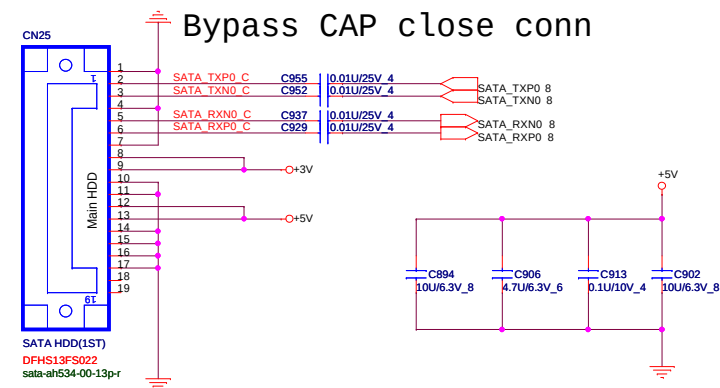
SI2 , HP request Image sensor
SMBUS reserve to FCH

SI , Q21,Q22 change to dual type MOS Q51

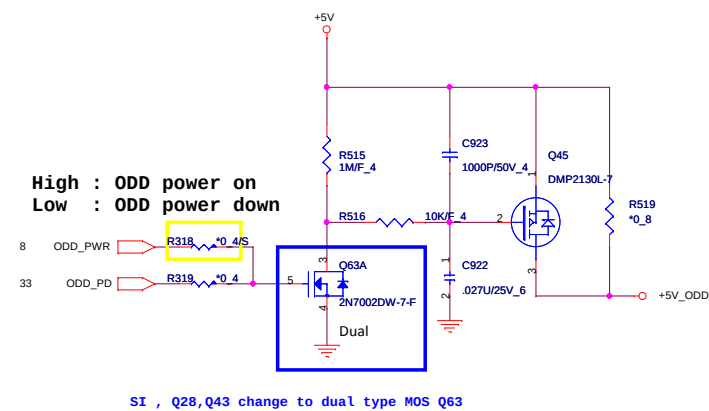
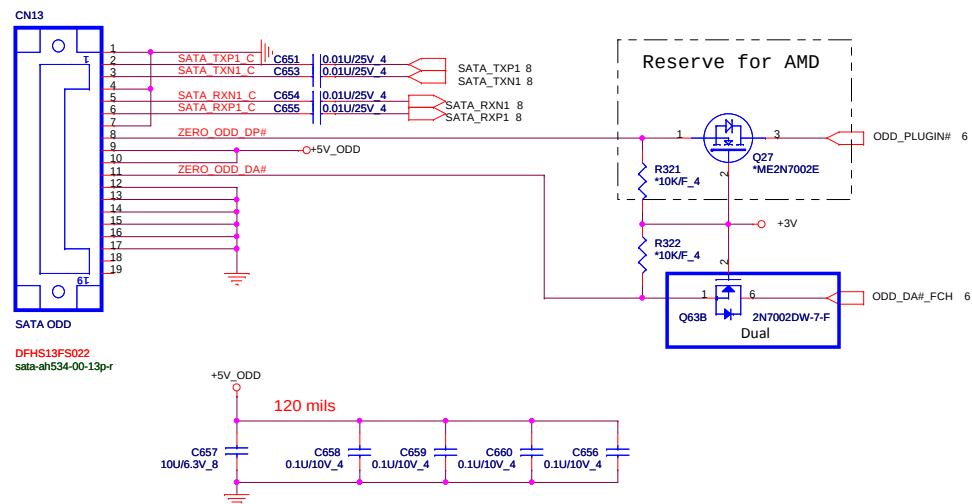
CPU FAN



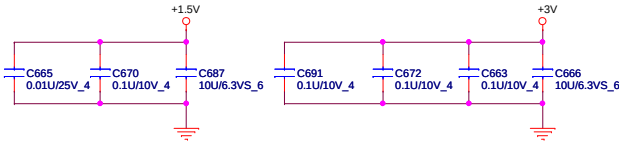
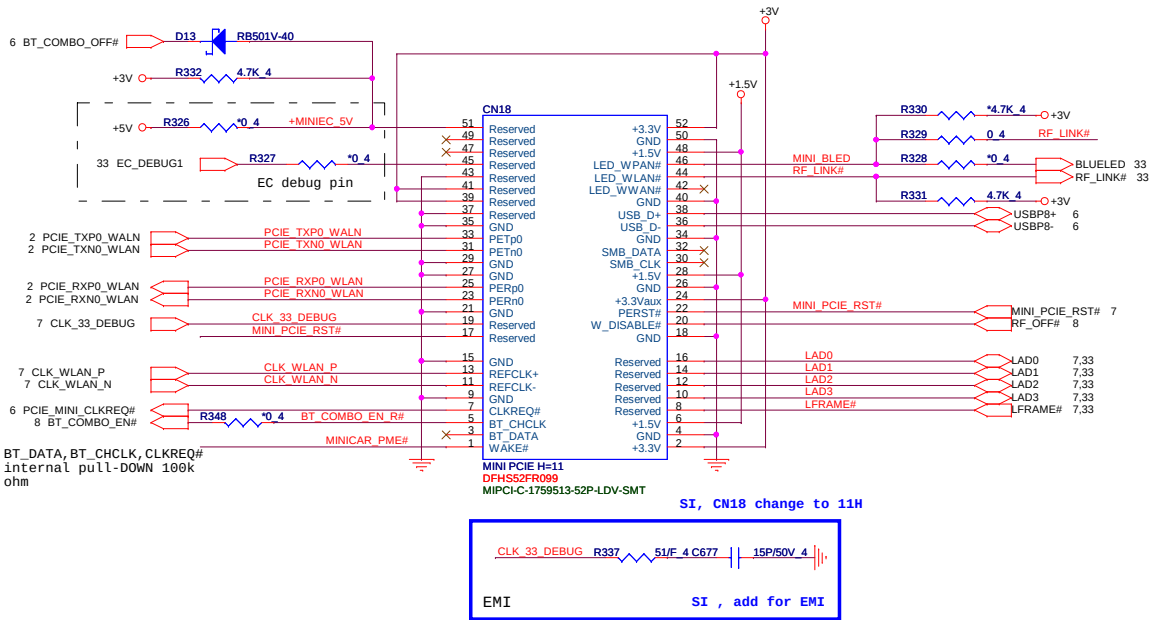
SATA HDD CONNECTOR



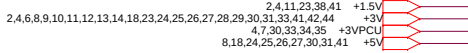
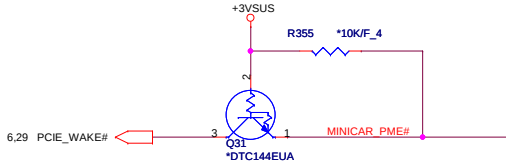
SATA ODD CONNECTOR SATA ODD



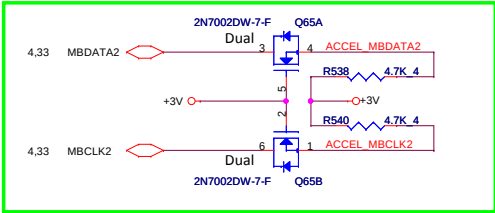
Mini PCI-E Card 1 WLAN



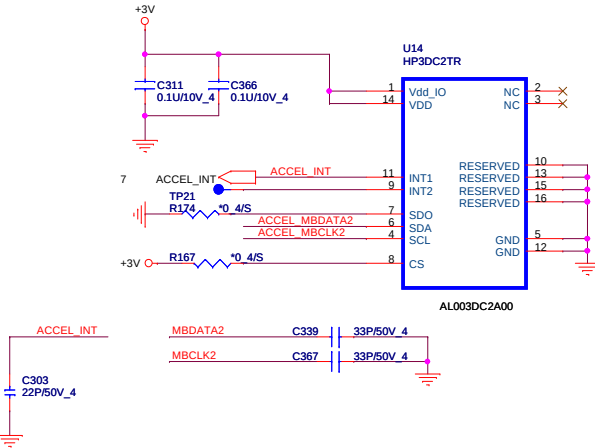
INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm



Accelerometer Sensor

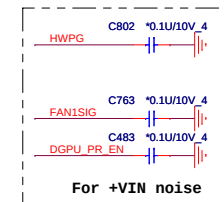
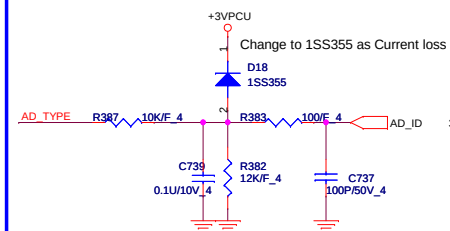
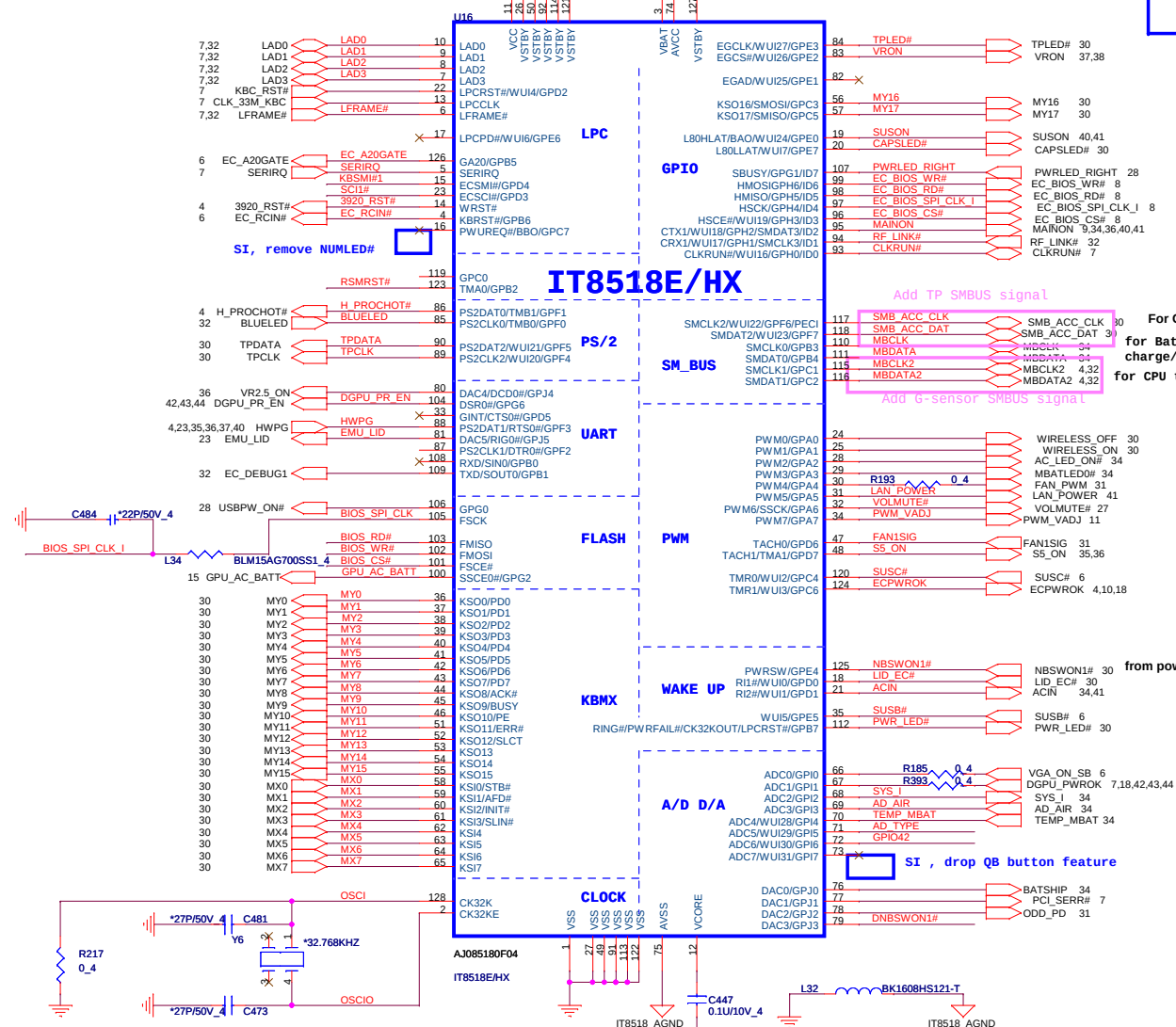


SI2 , add for avoid leakage from SUS power



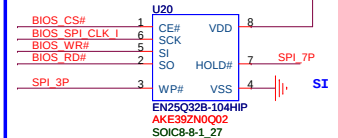
Smart adapter Type check

**ITE pin 100 , 104 , 106 default
can not pull up to +3VPCU it
will cause chip into test mode**

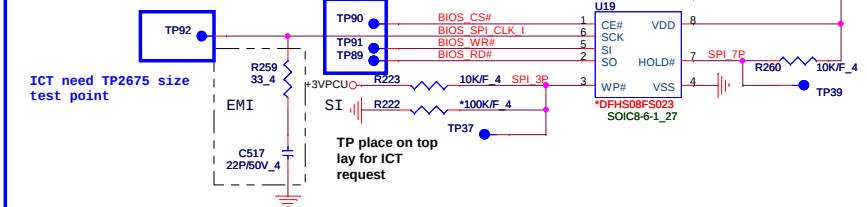


Vender	Size	P/N
AMIC	4M	AKE39F-0800
EON	4M	AKE39ZN0Q02
Socket		DFHS08FS023

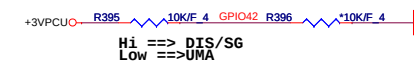
4M SPI EC ROM



128K byte SPI EC ROM



Adapter select

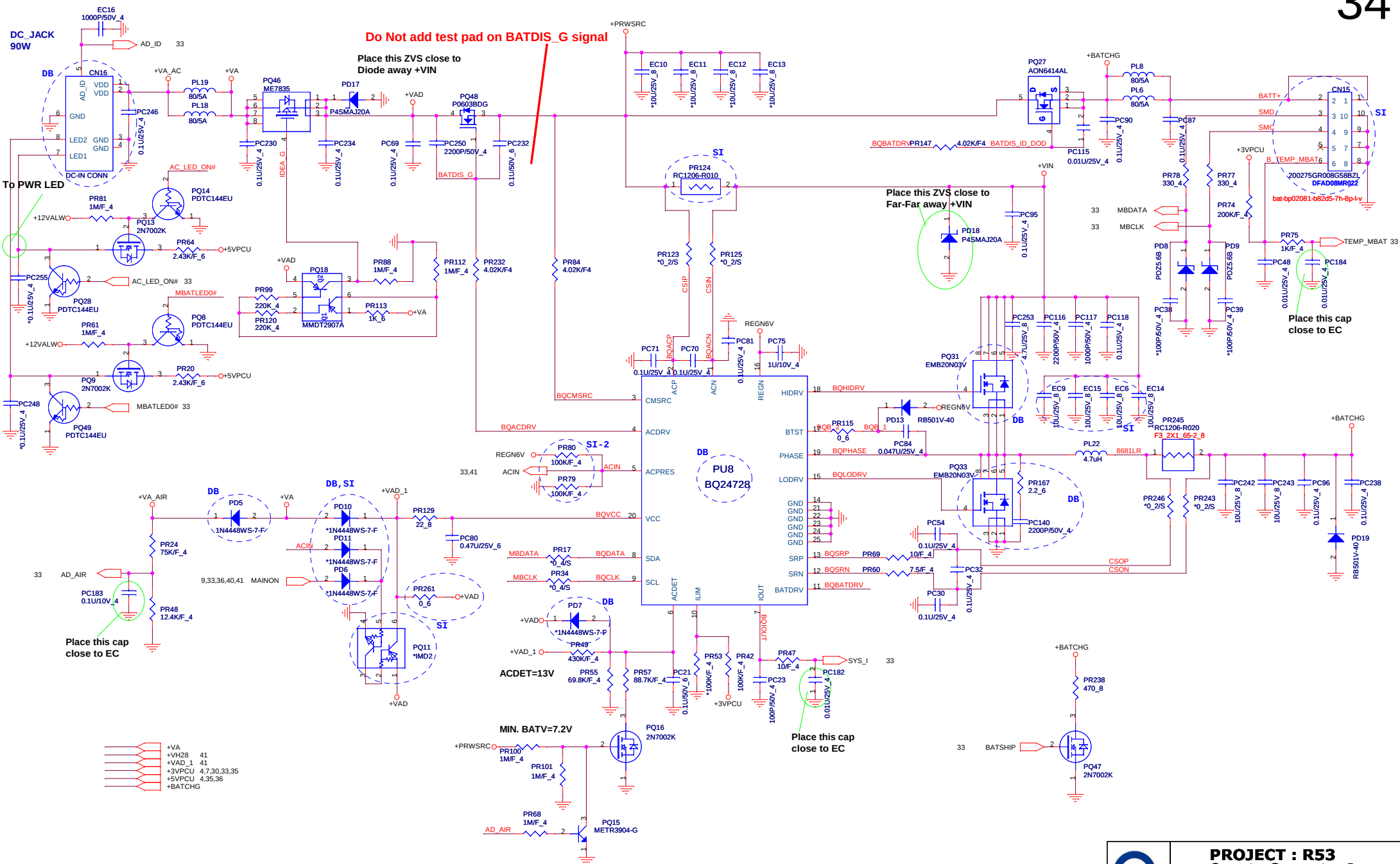


Platform model	GPI042	adapter
SG/DIS	High	90W
UMA	Low	65W



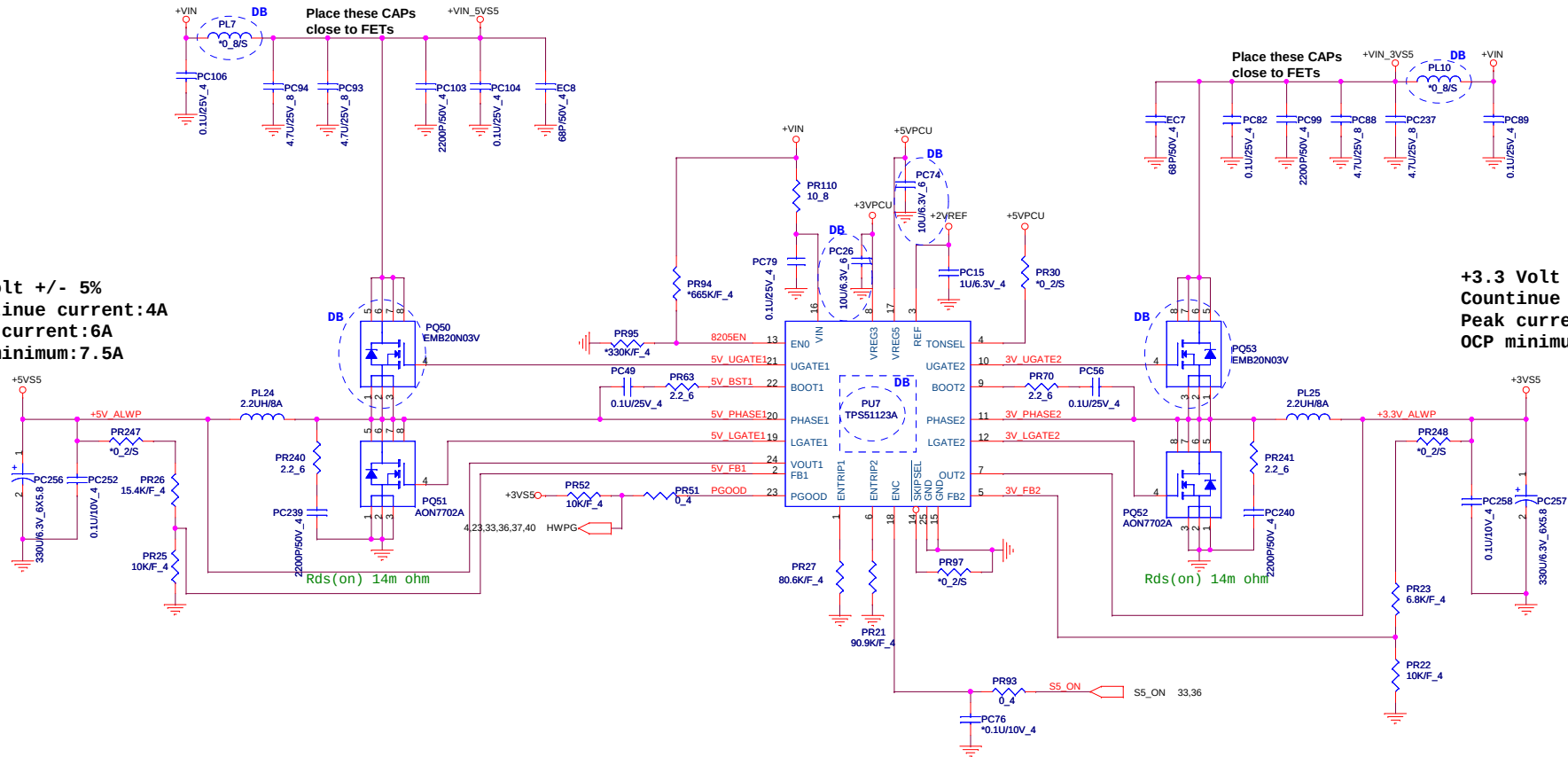
PROJECT : R53
Quanta Computer Inc.

Size Custom	Document Number EC (KB3926)/ROM	Rev 1A
Date: Friday, November 11, 2011		Sheet 33 of 44



+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

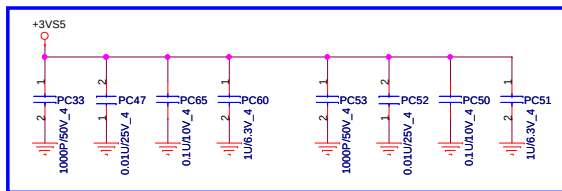
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

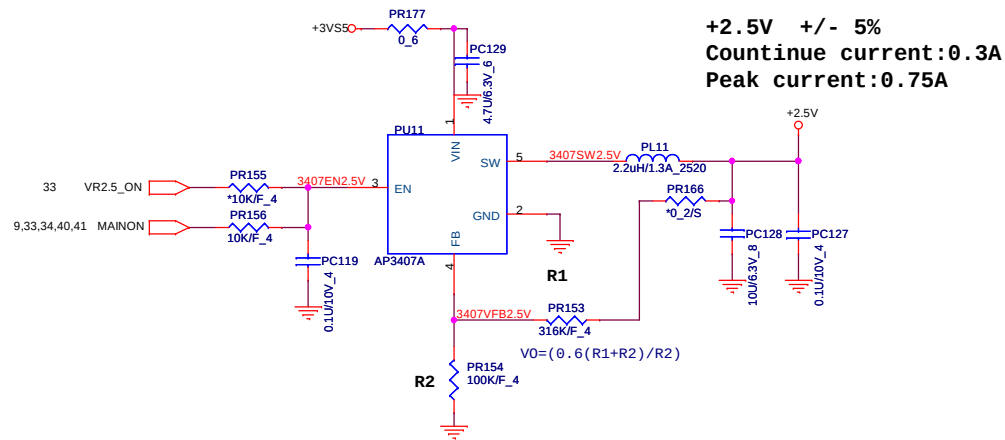
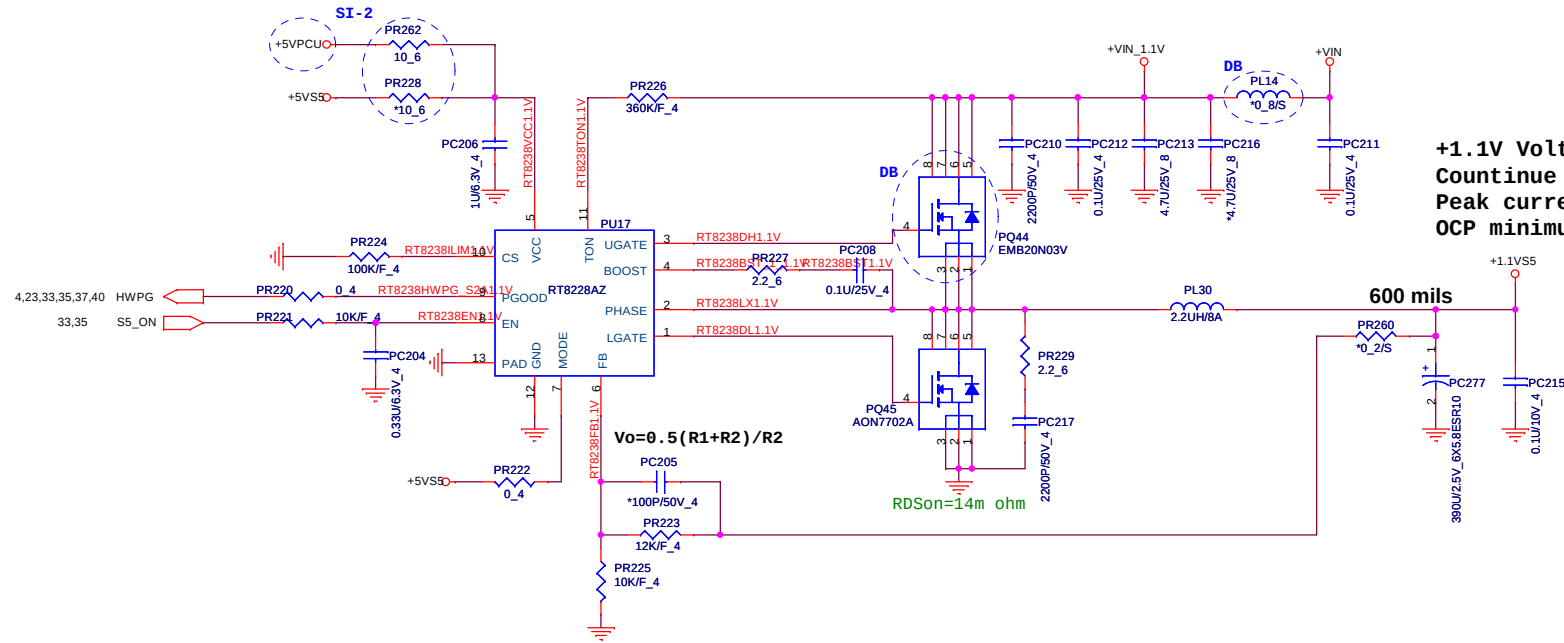


Place these CAPs close to FETs

Place these CAPs close to FETs

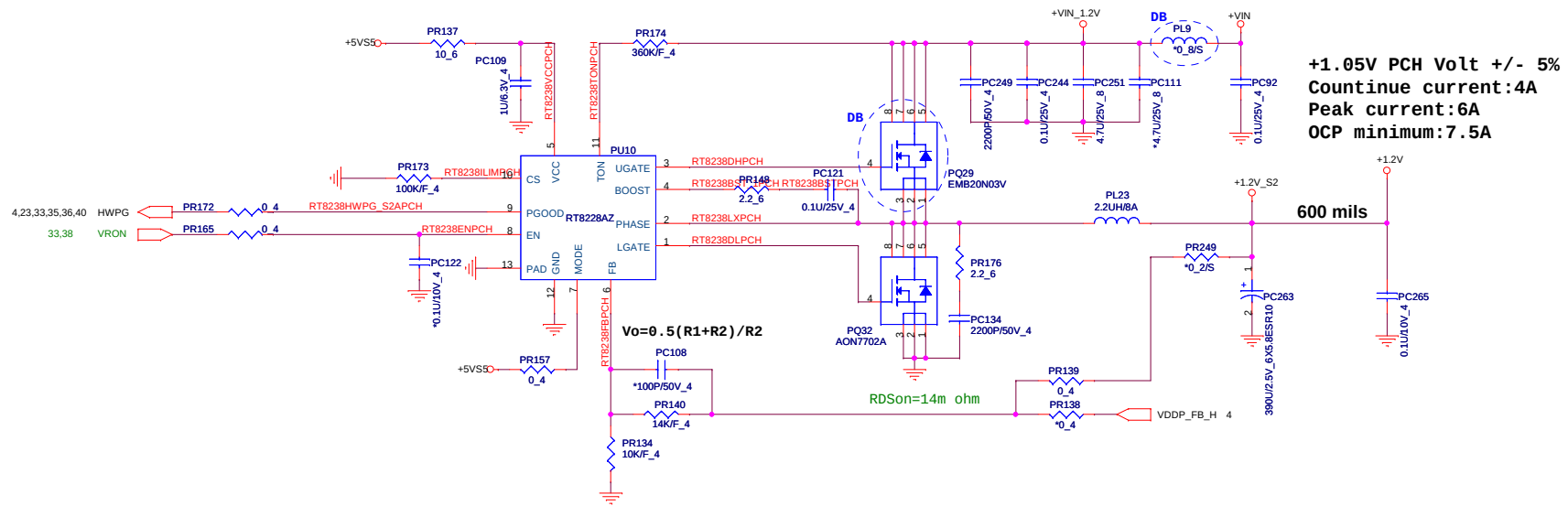
DB for prevent interference

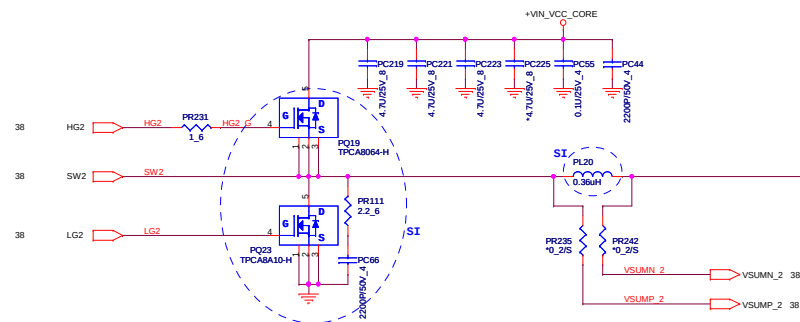
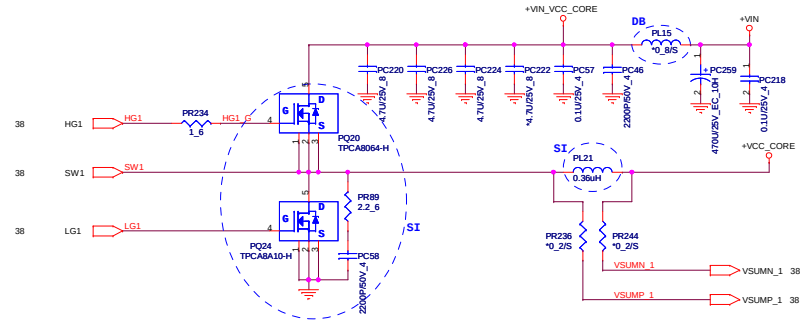




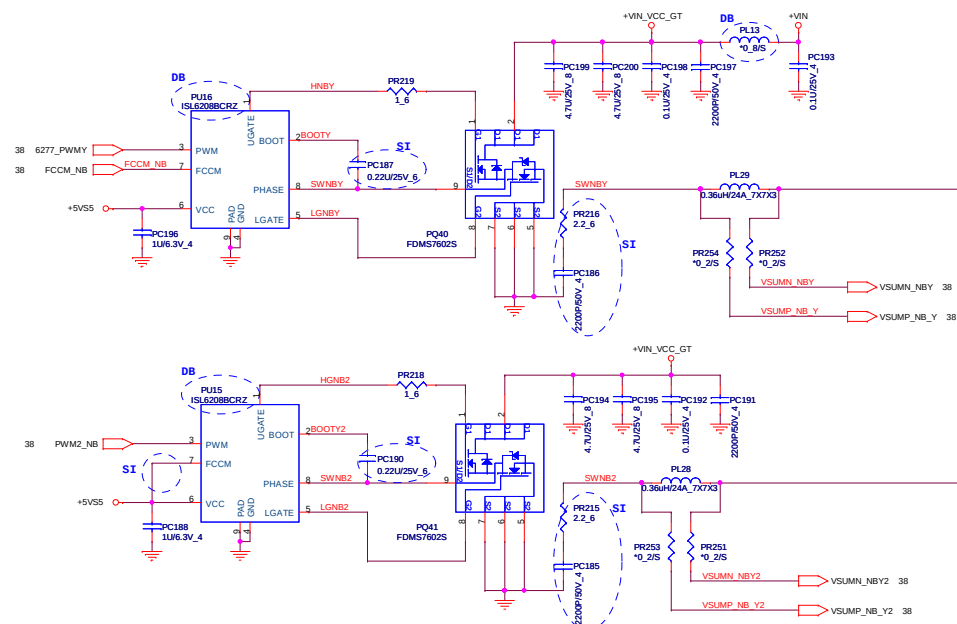
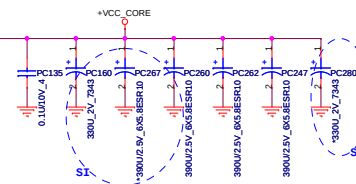
PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1VSS (RT8228)/2.5V	1A
Date:	Friday, November 11, 2011	Sheet 36 of 44

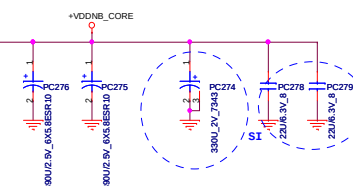


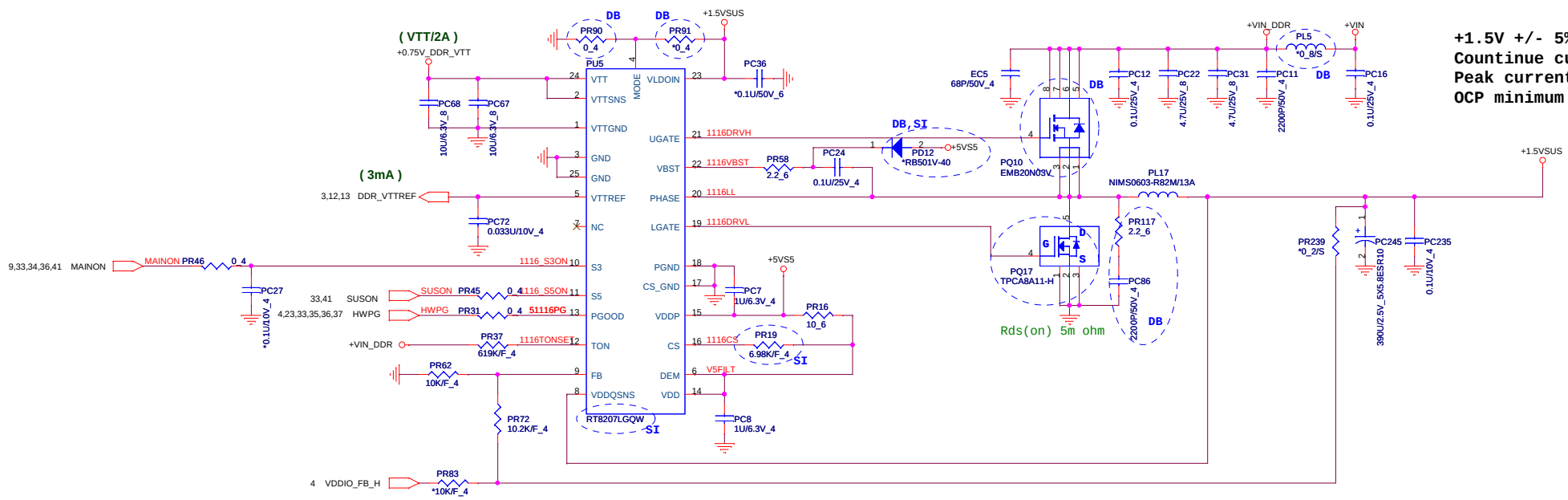


CPU CORE Volt
Continue current:36A
Peak current:50A
OCP minimum:60A

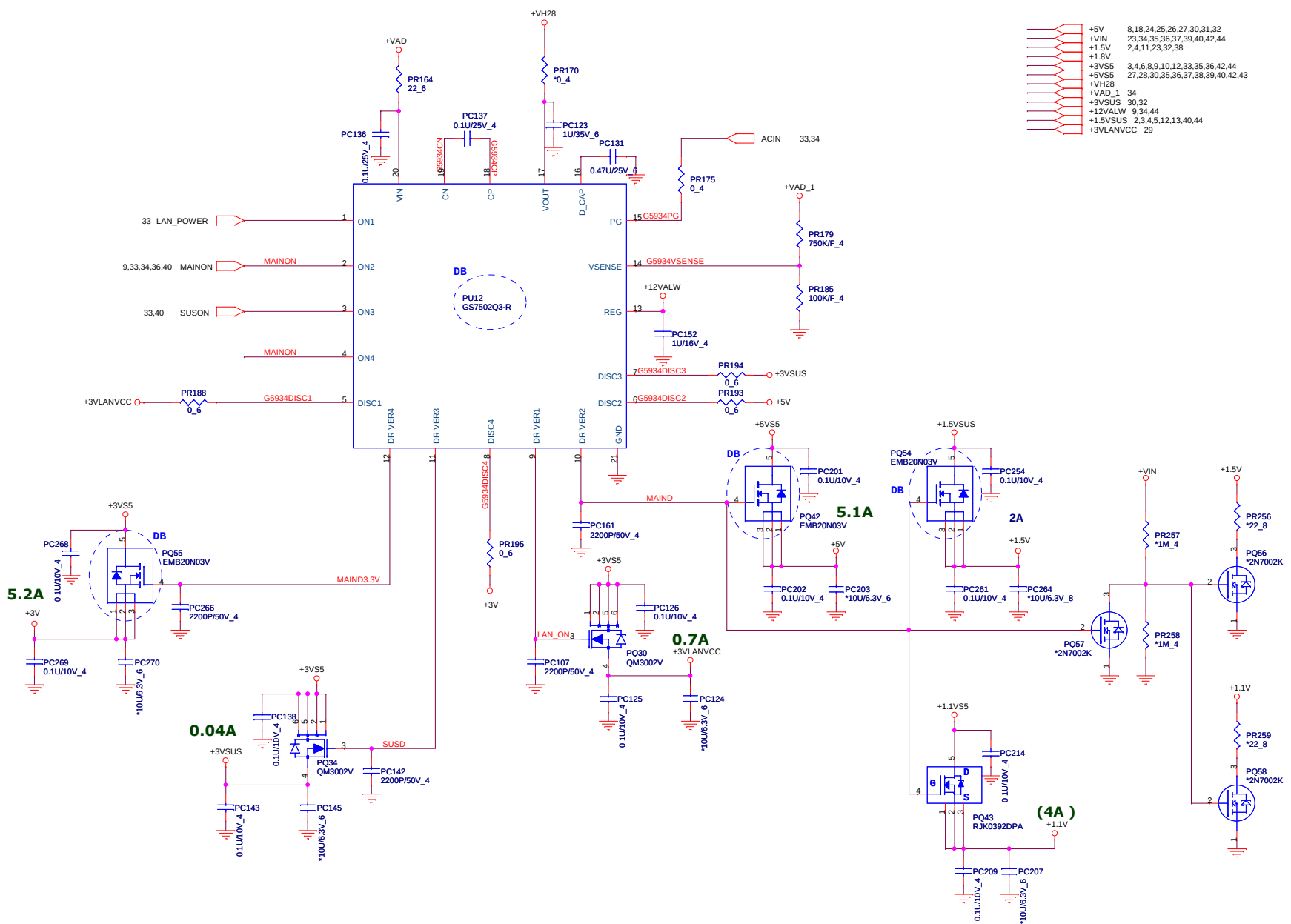


VDDNB Volt
Continue current:25A
Peak current:33A
OCP minimum:40A

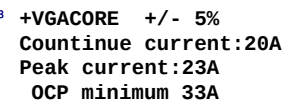




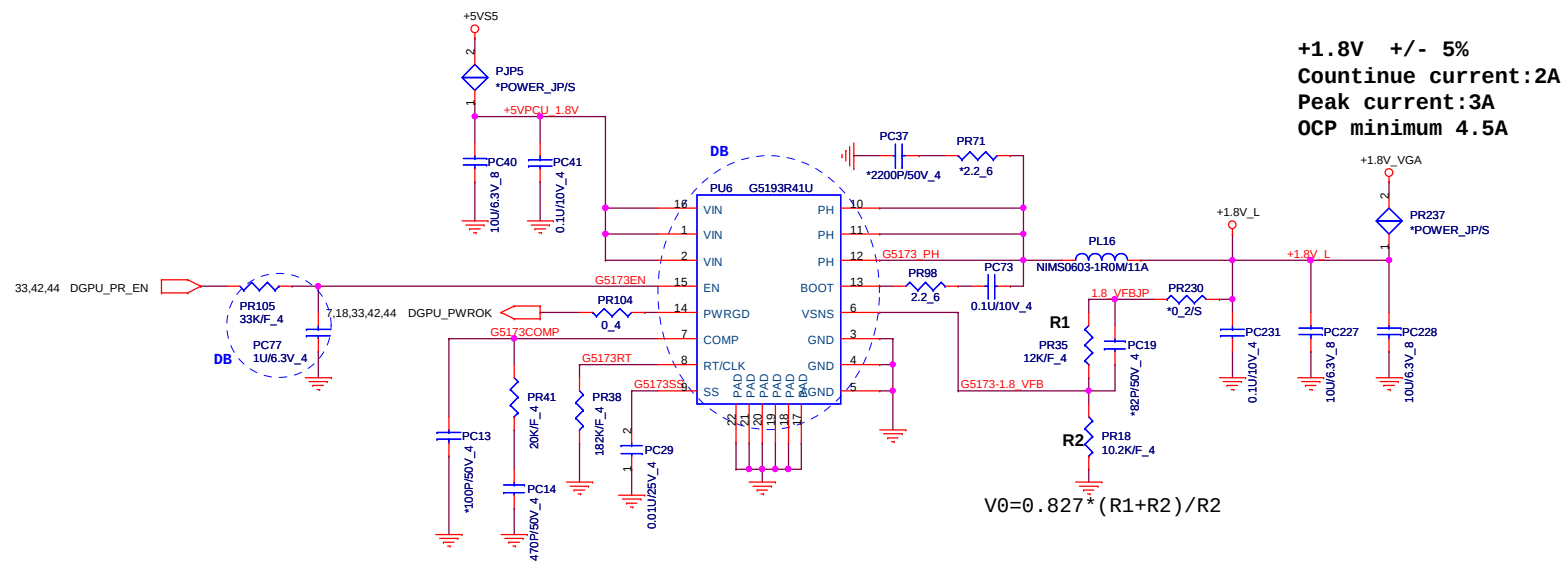
+1.5V +/- 5%
Continue current:10A
Peak current:12A
OCP minimum 15A



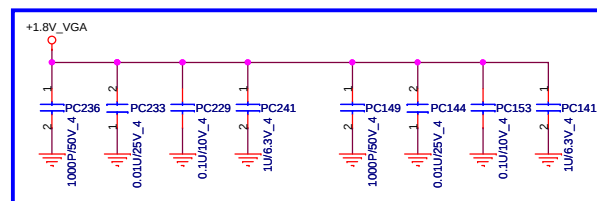
+5V	8,18,24,25,26,27,30,31,32
+VIN	23,34,35,36,37,39,40,42,44
+1.5V	2,4,11,23,32,38
+1.8V	
+3VS5	3,4,6,8,9,10,12,33,35,36,42,44
+5VS5	27,28,30,35,36,37,38,39,40,42,43
+VH28	
+VAD_1	34
+3VSUS	30,32
+12VALW	9,34,44
+1.5VSUS	2,3,4,5,12,13,40,44
+3VLNVCC	29



Symour-XT	PWRCNTL2 (GPIO16)	PWRCNTL1 (GPIO20)	PWRCNTL0 (GPIO15)	V-CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V



DB for prevent interference

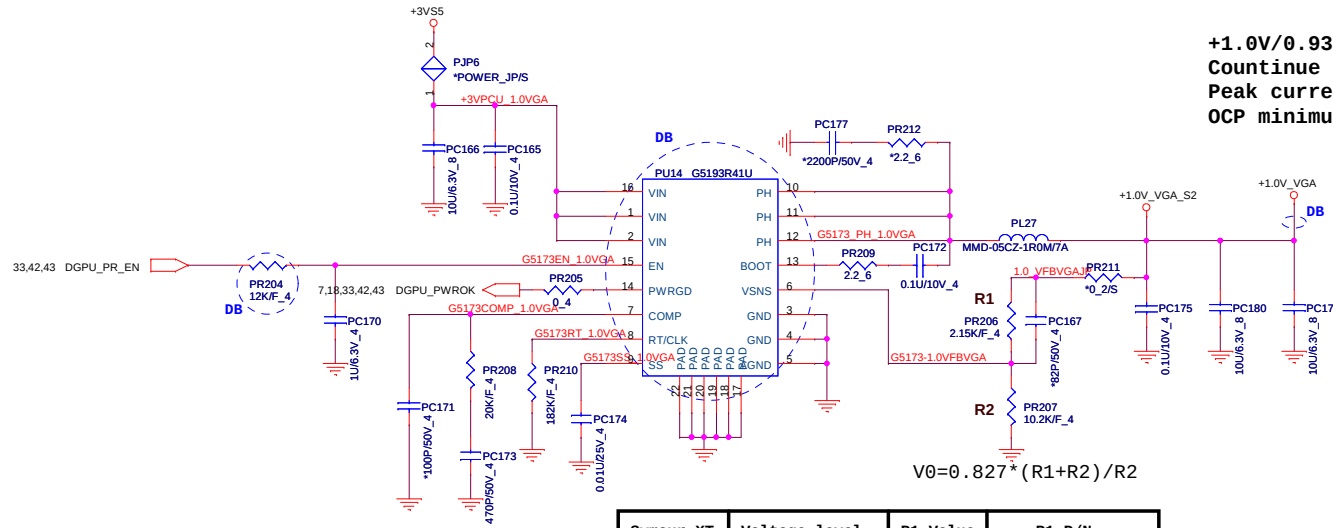


PROJECT : R53
Quanta Computer Inc.

Size Custom	Document Number +1.8V_VGA (G5193)	Rev 1A
Date: Friday, November 11, 2011	Sheet 43 of 44	

+1.0V/0.935V +/- 5%
Countinue current:2A
Peak current:3A
OCp minimum 4.5A

+3V	2,4,6,8,9,10,11,12,13,14,18,23,24,25,26,27,28,29,30,31,32,33,41,42
+VIN	23,34,35,36,37,39,40,41,42
+3VS5	3,4,6,8,9,10,12,33,35,36,41,42
+5VS5	27,28,30,35,36,37,38,39,40,41,42,43
+3V_VGA	18,30
+12VALW	9,34,41
+1.5VSUS	2,3,4,5,12,13,40,41
+1.5V_VGA	18,20,21,22



Symour-XT	Voltage level	R1 Value	R1 P/N
17W	1.0V	2.15K	CS22152FB07
25W	0.935V	1.37K	CS21372FB19

