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QCL51 Schematics Document

AMD Comal Platform

AMD Trinity APU / Hudson FCH / ATI Chelsea Pro M2

Muxless/UMA / PX 4.0 / PX 5.0

2011-10-26

LA-8712P REV: 0.1

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Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title: Cover Page	
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				Date: Monday, November 28, 2011	Sheet 1 of 56	

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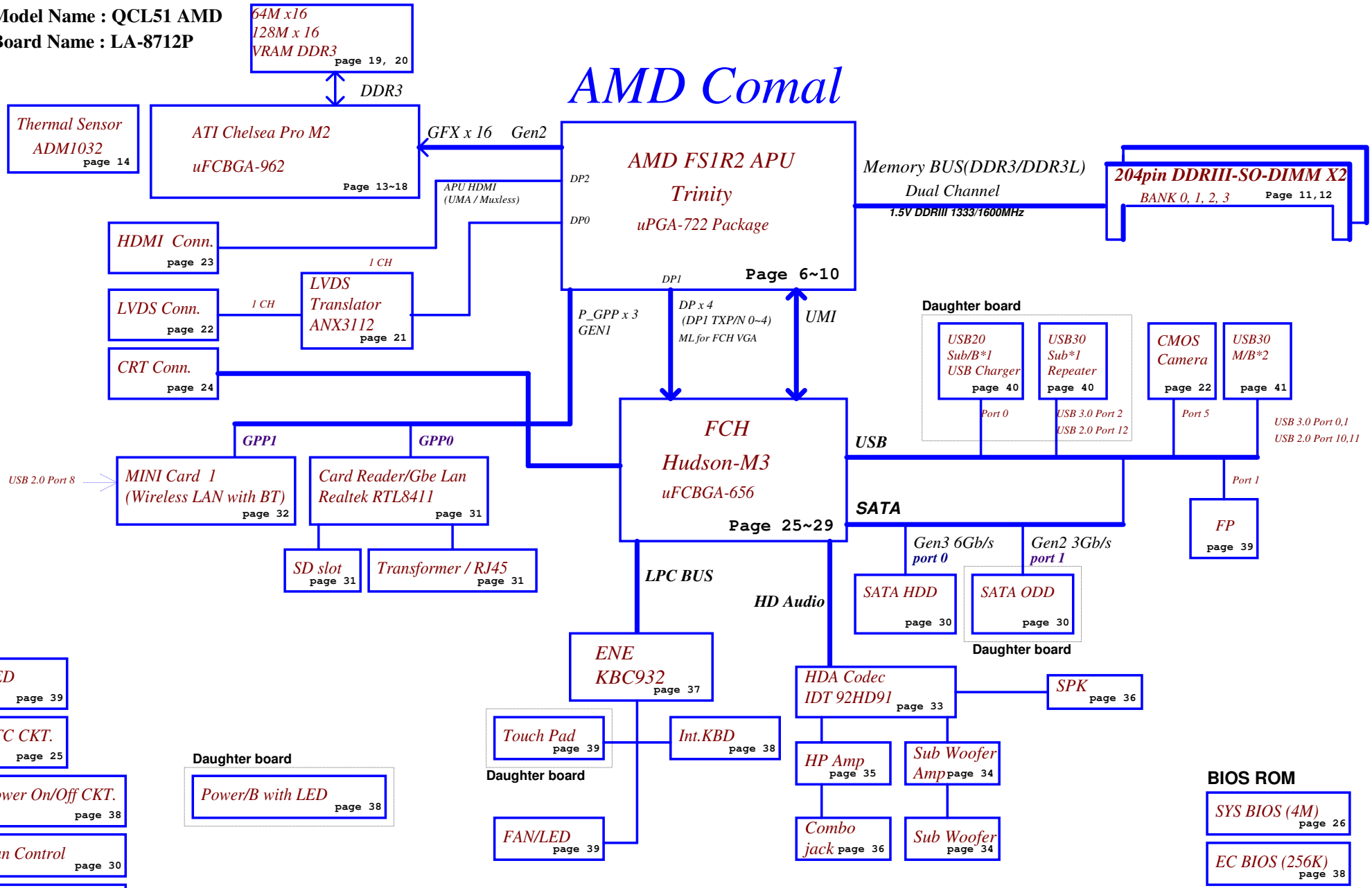
Model Name : QCL51 AMD
Board Name : LA-8712P



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title	Block Diagrams		
Size B	Document Number QCL51 LA-8712P		Rev 0.1
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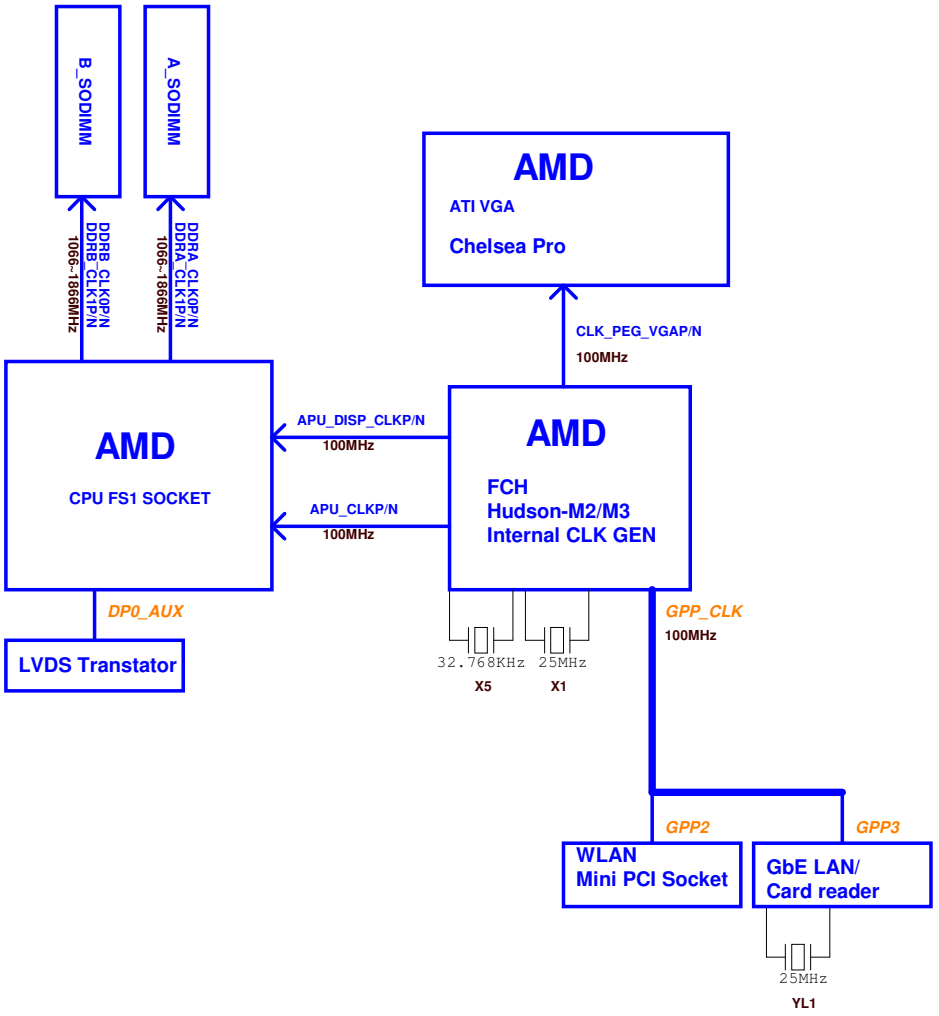
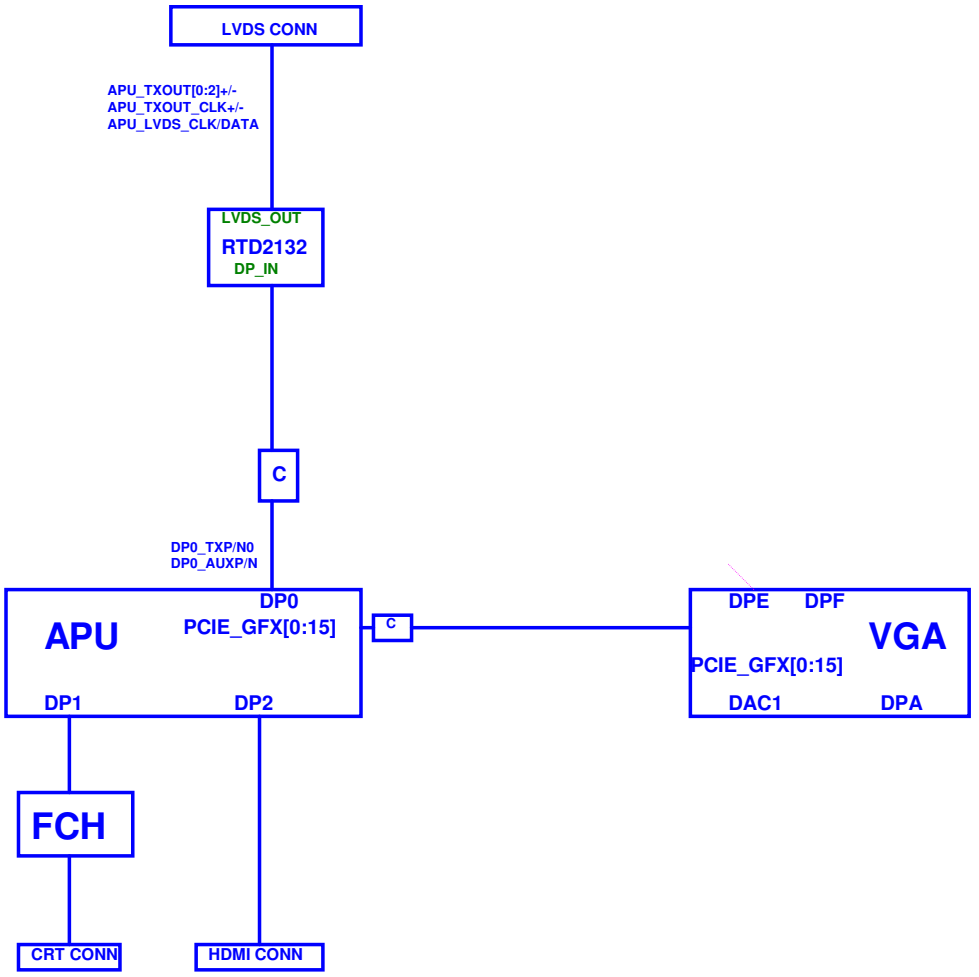
CLOCK DISTRIBUTION



DISPLAY OUTPUT



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Issued Date	2011/07/08	Deciphered Date 2015/07/08	Title: CLOCK / DISPLAY DISTRIBUTION
			Size: Custom; Document Number: QCL51 LA-8712P; Rev: 0.1
			Date: Monday, November 28, 2011; Sheet 3 of 56

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+0.935VGS	0.935V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5V_PCIE	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_VDD_3V3	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

ZZZ1

PCB
Part Number = DA80000SH00
PCB 0OH LA-8712P REV0 M/B

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rb	100K +/- 5%

Board ID	Ra / Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	DB
1	
2	
3	
4	
5	
6	
7	

BOM Option Table

BOM Structure	Description
PX@	PX function

BOM Config

UMA	PX
	V

x = 1 is read cmd, x= 0 is writee cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (GPU)	1001 101X b	9AH
SB-TSI (APU)	1001 100X b	98H
LVDS TR	1010 100X b	A8H
VGA Internal Thermal	1000 001X b	82H

FCH (S0) SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1010 000X b	A0
DDR DIMM2	1010 001X b	A2
Amplifier		

FCH (S0~S5) SM Bus 1 address

Device	Address	HEX
Touch pad		

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Title	Notes List		
Size B	Document Number QCL51 LA-8712P		Rev 0.1
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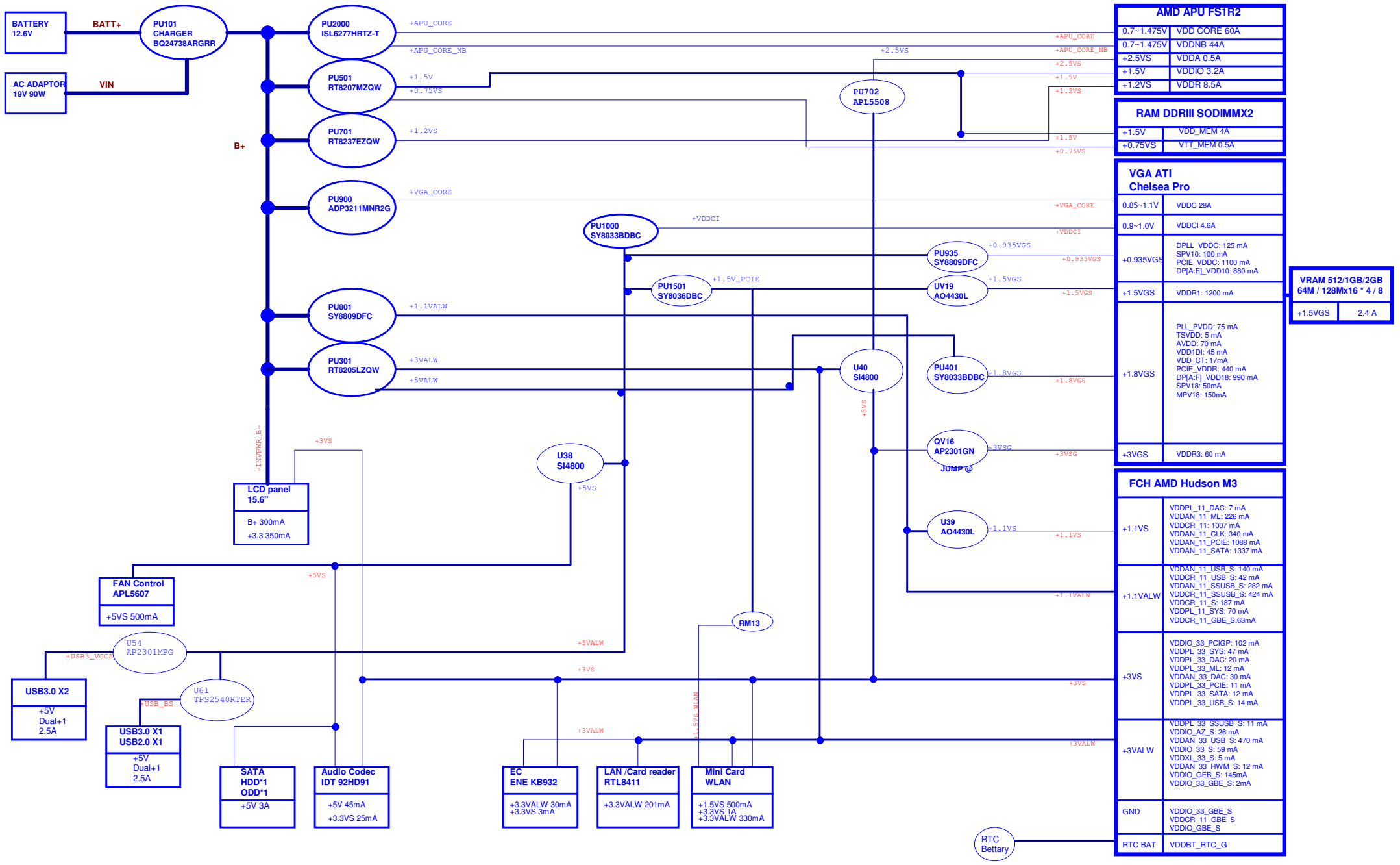

Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Title: POWER DELIVERY CHART

Size	Document Number	Rev
Custom	QCL51 LA-8712P	0.1

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13 PCIE_GTX_C_FRX_P[0..15]
13 PCIE_GTX_C_FRX_N[0..15]

PCIE_FTX_C_GRX_P[0..15] 13
PCIE_FTX_C_GRX_N[0..15] 13

GPU

GLAN/Card reader
WLAN

UMI

JCPU1A

PCI EXPRESS

PCIE_GTX_C_FRX_P0	AB8	P_GFX_RXP0	P_GFX_TXP0	AB2	PCIE_FTX_GRX_P0	C917	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P0								
PCIE_GTX_C_FRX_N0	AB7	P_GFX_RXN0	P_GFX_TXN0	AB1	PCIE_FTX_GRX_N0	C918	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N0								
PCIE_GTX_C_FRX_P1	AA9	P_GFX_RXP1	P_GFX_TXP1	AA3	PCIE_FTX_GRX_P1	C919	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P1								
PCIE_GTX_C_FRX_N1	AA8	P_GFX_RXN1	P_GFX_TXN1	AA2	PCIE_FTX_GRX_N1	C920	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N1								
PCIE_GTX_C_FRX_P2	AA5	P_GFX_RXP2	P_GFX_TXP2	Y5	PCIE_FTX_GRX_P2	C921	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P2								
PCIE_GTX_C_FRX_N2	AA6	P_GFX_RXN2	P_GFX_TXN2	Y4	PCIE_FTX_GRX_N2	C922	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N2								
PCIE_GTX_C_FRX_P3	Y8	P_GFX_RXP3	P_GFX_TXP3	Y2	PCIE_FTX_GRX_P3	C923	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P3								
PCIE_GTX_C_FRX_N3	Y7	P_GFX_RXN3	P_GFX_TXN3	Y1	PCIE_FTX_GRX_N3	C924	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N3								
PCIE_GTX_C_FRX_P4	W9	P_GFX_RXP4	P_GFX_TXP4	W3	PCIE_FTX_GRX_P4	C925	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P4								
PCIE_GTX_C_FRX_N4	W8	P_GFX_RXN4	P_GFX_TXN4	W2	PCIE_FTX_GRX_N4	C926	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N4								
PCIE_GTX_C_FRX_P5	W5	P_GFX_RXP5	P_GFX_TXP5	V5	PCIE_FTX_GRX_P5	C927	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P5								
PCIE_GTX_C_FRX_N5	W6	P_GFX_RXN5	P_GFX_TXN5	V4	PCIE_FTX_GRX_N5	C928	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N5								
PCIE_GTX_C_FRX_P6	V8	P_GFX_RXP6	P_GFX_TXP6	V2	PCIE_FTX_GRX_P6	C929	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P6								
PCIE_GTX_C_FRX_N6	V7	P_GFX_RXN6	P_GFX_TXN6	V1	PCIE_FTX_GRX_N6	C930	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N6								
PCIE_GTX_C_FRX_P7	U9	P_GFX_RXP7	P_GFX_TXP7	U3	PCIE_FTX_GRX_P7	C931	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P7								
PCIE_GTX_C_FRX_N7	U8	P_GFX_RXN7	P_GFX_TXN7	U2	PCIE_FTX_GRX_N7	C932	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N7								
PCIE_GTX_C_FRX_P8	U5	P_GFX_RXP8	P_GFX_TXP8	T5	PCIE_FTX_GRX_P8	C933	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P8								
PCIE_GTX_C_FRX_N8	U6	P_GFX_RXN8	P_GFX_TXN8	T4	PCIE_FTX_GRX_N8	C934	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N8								
PCIE_GTX_C_FRX_P9	T8	P_GFX_RXP9	P_GFX_TXP9	T2	PCIE_FTX_GRX_P9	C936	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P9								
PCIE_GTX_C_FRX_N9	T7	P_GFX_RXN9	P_GFX_TXN9	T1	PCIE_FTX_GRX_N9	C937	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N9								
PCIE_GTX_C_FRX_P10	R9	P_GFX_RXP10	P_GFX_TXP10	R3	PCIE_FTX_GRX_P10	C938	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P10								
PCIE_GTX_C_FRX_N10	R8	P_GFX_RXN10	P_GFX_TXN10	R2	PCIE_FTX_GRX_N10	C939	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N10								
PCIE_GTX_C_FRX_P11	R5	P_GFX_RXP11	P_GFX_TXP11	P5	PCIE_FTX_GRX_P11	C940	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P11								
PCIE_GTX_C_FRX_N11	R6	P_GFX_RXN11	P_GFX_TXN11	P4	PCIE_FTX_GRX_N11	C941	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N11								
PCIE_GTX_C_FRX_P12	P8	P_GFX_RXP12	P_GFX_TXP12	P2	PCIE_FTX_GRX_P12	C942	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P12								
PCIE_GTX_C_FRX_N12	P7	P_GFX_RXN12	P_GFX_TXN12	P1	PCIE_FTX_GRX_N12	C943	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N12								
PCIE_GTX_C_FRX_P13	N9	P_GFX_RXP13	P_GFX_TXP13	N3	PCIE_FTX_GRX_P13	C944	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P13								
PCIE_GTX_C_FRX_N13	N8	P_GFX_RXN13	P_GFX_TXN13	N2	PCIE_FTX_GRX_N13	C945	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N13								
PCIE_GTX_C_FRX_P14	N5	P_GFX_RXP14	P_GFX_TXP14	M5	PCIE_FTX_GRX_P14	C946	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P14								
PCIE_GTX_C_FRX_N14	N6	P_GFX_RXN14	P_GFX_TXN14	M4	PCIE_FTX_GRX_N14	C947	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N14								
PCIE_GTX_C_FRX_P15	M8	P_GFX_RXP15	P_GFX_TXP15	M2	PCIE_FTX_GRX_P15	C948	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_P15								
PCIE_GTX_C_FRX_N15	M7	P_GFX_RXN15	P_GFX_TXN15	M1	PCIE_FTX_GRX_N15	C949	PX@	1	2	.1U_0402_16V7K	PCIE_FTX_C_GRX_N15								

GRAPHICS

	AE5	P_GPP_RXP0	P_GPP_TXP0	AD5	PCIE_FTX_DRX_P0	C950	1	2	.1U_0402_16V7K										
	AE6	P_GPP_RXN0	P_GPP_TXN0	AD4	PCIE_FTX_DRX_N0	C951	1	2	.1U_0402_16V7K										
	AD8	P_GPP_RXP1	P_GPP_TXP1	AD2	PCIE_FTX_DRX_P1	C952	1	2	.1U_0402_16V7K										
	AD7	P_GPP_RXN1	P_GPP_TXN1	AD1	PCIE_FTX_DRX_N1	C953	1	2	.1U_0402_16V7K										
	AC9	P_GPP_RXP2	P_GPP_TXP2	AC3															
	AC8	P_GPP_RXN2	P_GPP_TXN2	AC2															
	AC5	P_GPP_RXP3	P_GPP_TXP3	AB5															
	AC6	P_GPP_RXN3	P_GPP_TXN3	AB4															

GPP

	AG8	P_UMI_RXP0	P_UMI_TXP0	AG2	UMI_FTX_MRX_P0	C956	1	2	.1U_0402_16V7K										
	AG9	P_UMI_RXN0	P_UMI_TXN0	AG3	UMI_FTX_MRX_N0	C957	1	2	.1U_0402_16V7K										
	AG6	P_UMI_RXP1	P_UMI_TXP1	AF4	UMI_FTX_MRX_P1	C958	1	2	.1U_0402_16V7K										
	AG5	P_UMI_RXN1	P_UMI_TXN1	AF5	UMI_FTX_MRX_N1	C959	1	2	.1U_0402_16V7K										
	AF7	P_UMI_RXP2	P_UMI_TXP2	AF1	UMI_FTX_MRX_P2	C960	1	2	.1U_0402_16V7K										
	AF8	P_UMI_RXN2	P_UMI_TXN2	AF2	UMI_FTX_MRX_N2	C961	1	2	.1U_0402_16V7K										
	AE8	P_UMI_RXP3	P_UMI_TXP3	AE2	UMI_FTX_MRX_P3	C962	1	2	.1U_0402_16V7K										
	AE9	P_UMI_RXN3	P_UMI_TXN3	AE3	UMI_FTX_MRX_N3	C963	1	2	.1U_0402_16V7K										

UMI

31	PCIE_DTX_C_FRX_P0											PCIE_FTX_C_DRX_P0	31						
31	PCIE_DTX_C_FRX_N0											PCIE_FTX_C_DRX_N0	31						
32	PCIE_DTX_C_FRX_P1											PCIE_FTX_C_DRX_P1	32						
32	PCIE_DTX_C_FRX_N1											PCIE_FTX_C_DRX_N1	32						

25	UMI_MTX_C_FRX_P0											UMI_FTX_C_MRX_P0	25						
25	UMI_MTX_C_FRX_N0											UMI_FTX_C_MRX_N0	25						
25	UMI_MTX_C_FRX_P1											UMI_FTX_C_MRX_P1	25						
25	UMI_MTX_C_FRX_N1											UMI_FTX_C_MRX_N1	25						
25	UMI_MTX_C_FRX_P2											UMI_FTX_C_MRX_P2	25						
25	UMI_MTX_C_FRX_N2											UMI_FTX_C_MRX_N2	25						
25	UMI_MTX_C_FRX_P3											UMI_FTX_C_MRX_P3	25						
25	UMI_MTX_C_FRX_N3											UMI_FTX_C_MRX_N3	25						

+1.2VS 1 R539 2 196_0402_1%

P_ZVDDP AG11

P_ZVDDP

P_ZVSS

AH11 P_ZVSS 1 R540 2 196_0402_1%

LOTES_ACA-ZIF-109-P12-A_FS1R2
CONN@

P_ZVDDP W/S=8/12 mil, <3000mil

P_ZVSS W/S=8/12 mil, <3000mil

GPU

GLAN/Card reader
WLAN

UMI

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: AMD FS1R2 PCIE / GFX / UMI

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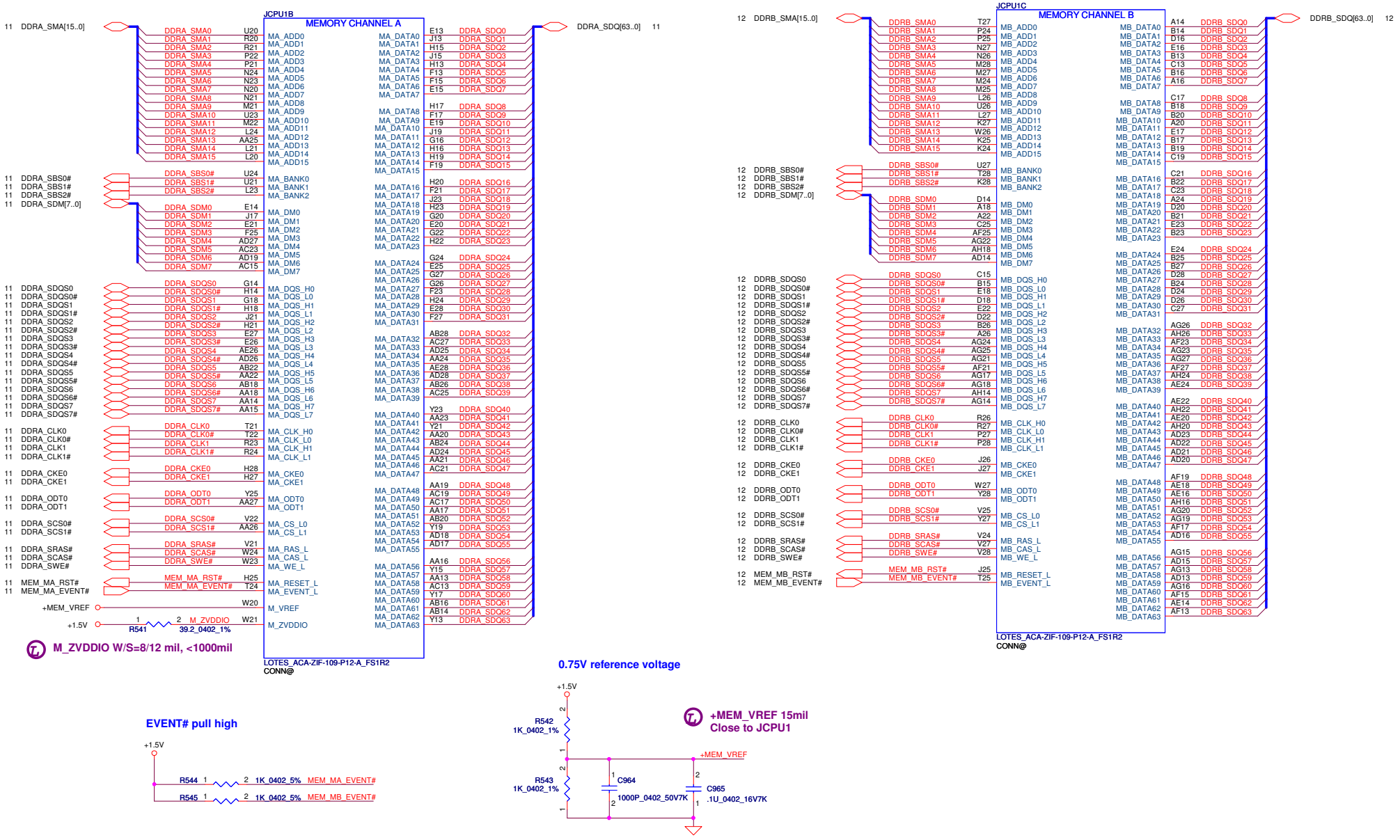

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Issued Date	2011/07/08	Deciphered Date 2015/07/08	Title: AMD FS1 DDRIII I/F

Size: B/5 Custom	Document Number: QCL51 LA-8712P		Rev: 0.1
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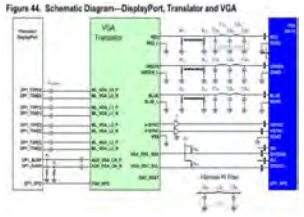

Close to APU (JCPU1)

Place near APU

JCPU1D

ANALOG/DISPLAY/MISC

To LVDS Translator

Del DP0_TXP1/N1

To FCH VGA ML

To HDMI

To LVDS Translator

To FCH

To HDMI

LVDS/eDP
CRT
HDMI

LA-8124 no use this DP_ENBKL.

Del DP_ENVDD

VDDIO level
Need Level shift

DP_AUX_ZVSS W/S=8/12 mil, <3000mil

11/14 Reserve

Allow_STOP leakage issue

For ESD request close APU side

100MHz

100MHz NSS

SVI 2.0 (0 ohm at Power Side)

SB-TSI (S5 Domain)

Internal PU when no use HDT

11/15 RF

TEST35 change to PU for HDMI can not output 20110126

11/14 Change net name

Close to Header

10/27 300 ohm??

Route as differential with APU_VDD_RUN_FB_L

LOTES_ACA-ZIF-109-P12-A_FS1R2 CONN@

CPU TSI interface level shift

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

When APU High -> MOS OFF (Vgs < 0.4V)
APU Low -> MOS ON (Vgs > 1.3V)

Vg = 1.607 V

BSH111_SOT23-3

Asserted as an input to force processor into HTC-active state

MMBT3904_SOT23-3

THERMTRIP shutdown temperature: 115 degree

Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately

HDT Debug conn

11/10 del debug connector

Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: AMD FS1 Display / MISC / HDT

Size: Custom | Document Number: QCL51 LA-8712P | Rev: 0.1

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Power Name	Consumption
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	37A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.75A

+CPU_CORE-->+APU_CORE

On power team page

On power team page

+CPU_CORE Decoupling

330uF x 4 @ x1
22uF x 10
0.22uF x2
0.01uF x3
180pF x2 @ x1

+CPU_CORE_NB Decoupling

330uF x2
22uF x2 @ x2
10uF x1
0.22uF x2
180pF x3

+1.5V / VDDIO Decoupling

330uF x1
22uF x4
4.7uF x4
0.22uF x6
180pF x1 @x1

Decoupling between CPU and DIMMs across VDDIO and VSS split

VDDR Decoupling
Close JCPU1.AG10,AH8,AH9,AH10

10uF x3
0.22uF x2
1000pF x1
180pF x2

VDDP Decoupling
Close JCPU1.AH3~7

22uF x1
10uF x3
0.22uF x2
1000pF @x1
180pF x2
220uF x1

VDDA Decoupling

47uF x1
0.22uF x1
3300pF x1
180pF x1

+CPU_CORE_NB-->+APU_CORE_NB

Northbridge Power Pins for Remote Decoupling

VDDIO: 3200mA

VDDR: 3500mA

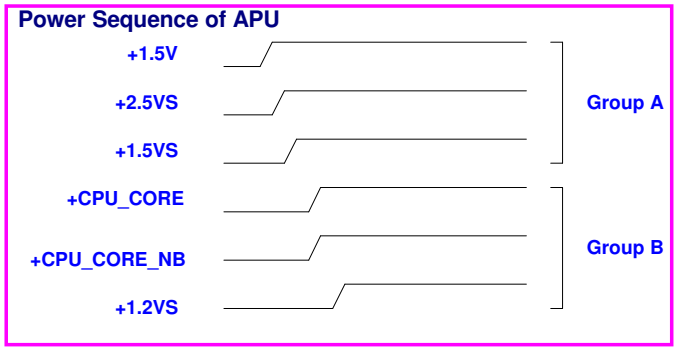
VDDP: 5000mA

VDDA: 750mA

FBMA-L11-201209-221LMA30T_0805

LOTES_ACA-ZIF-109-P12-A_FS1R2 CONN@

Power Sequence of APU



Decoupling Caps.

Pop / @	330uF	220uF	47uF	22uF	10uF	4.7uF	0.22uF	0.01uF	3300pF	1nF	180pF
Pumori 2.0			0	19/11	7	5	17	3	1	1 / 1	13/3
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16

Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: AMD FS1R2 PWR / GND

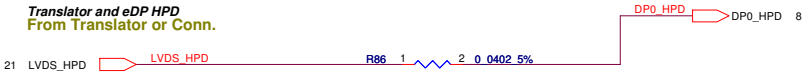
Size: Custom | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 9 of 56

HPD

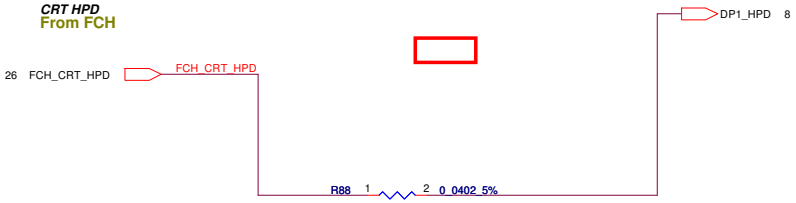
Del reserved NMOS

Translator and eDP HPD
From Translator or Conn.



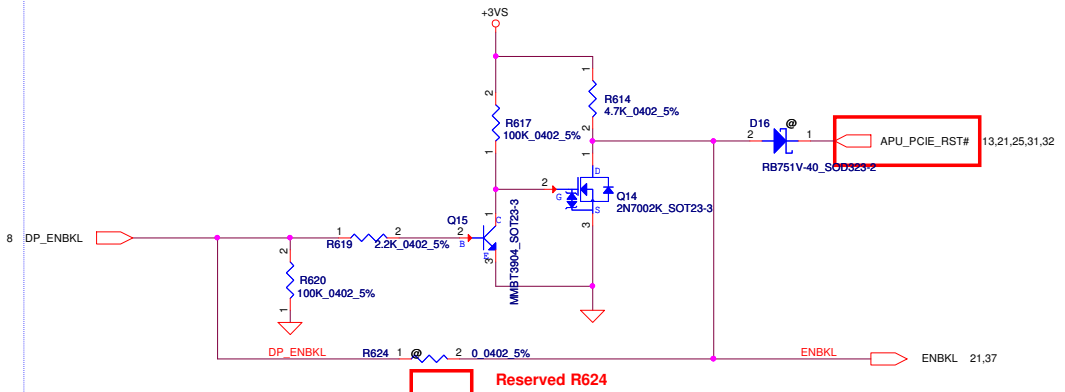
Del reserved NMOS

CRT HPD
From FCH



Panel ENBKL

LA-8124 no use this DP_ENBKL.



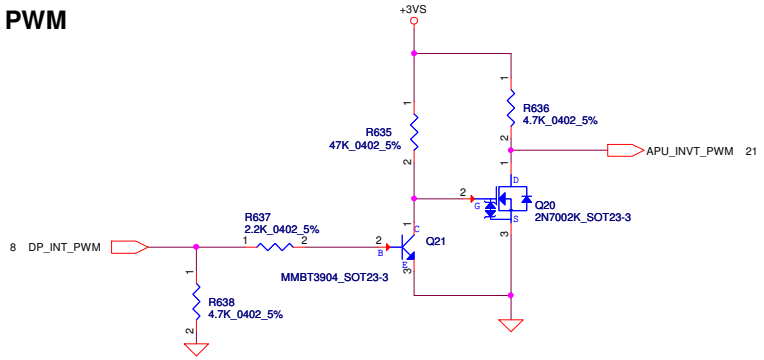
Reserved R624

Del VGA_ENBKL

eDP Panel ENVDD

Del eDP panel control

Panel PWM

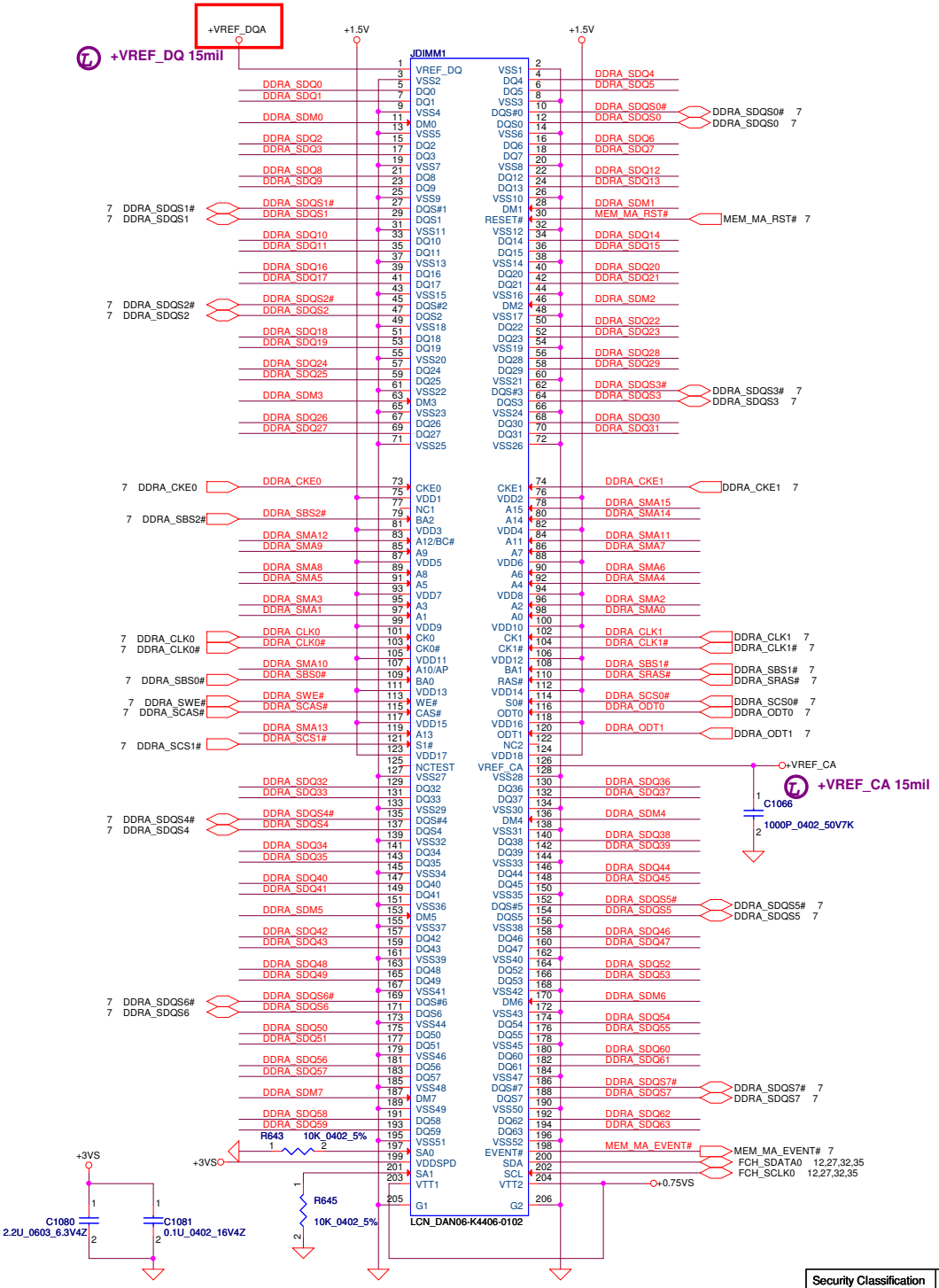


Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Title: AMD FS1R2 Singal Level Shifter

Size: Custom | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 10 of 56



DIMM_A REV H:4mm

<Address: 00>

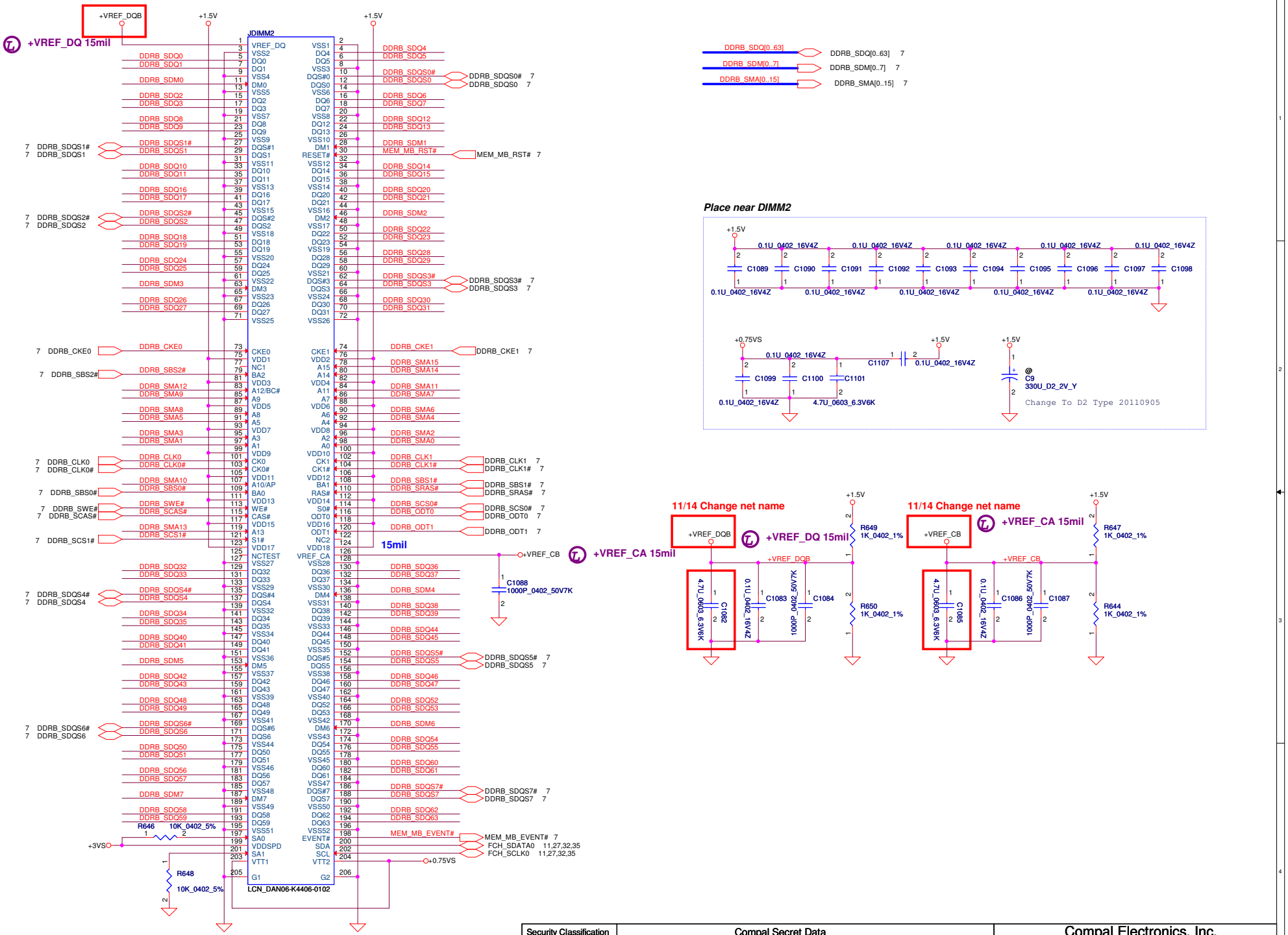
Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 1

Size: Custom | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 11 of 56



DIMM_B REV H:8mm

<Address: 01>

Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

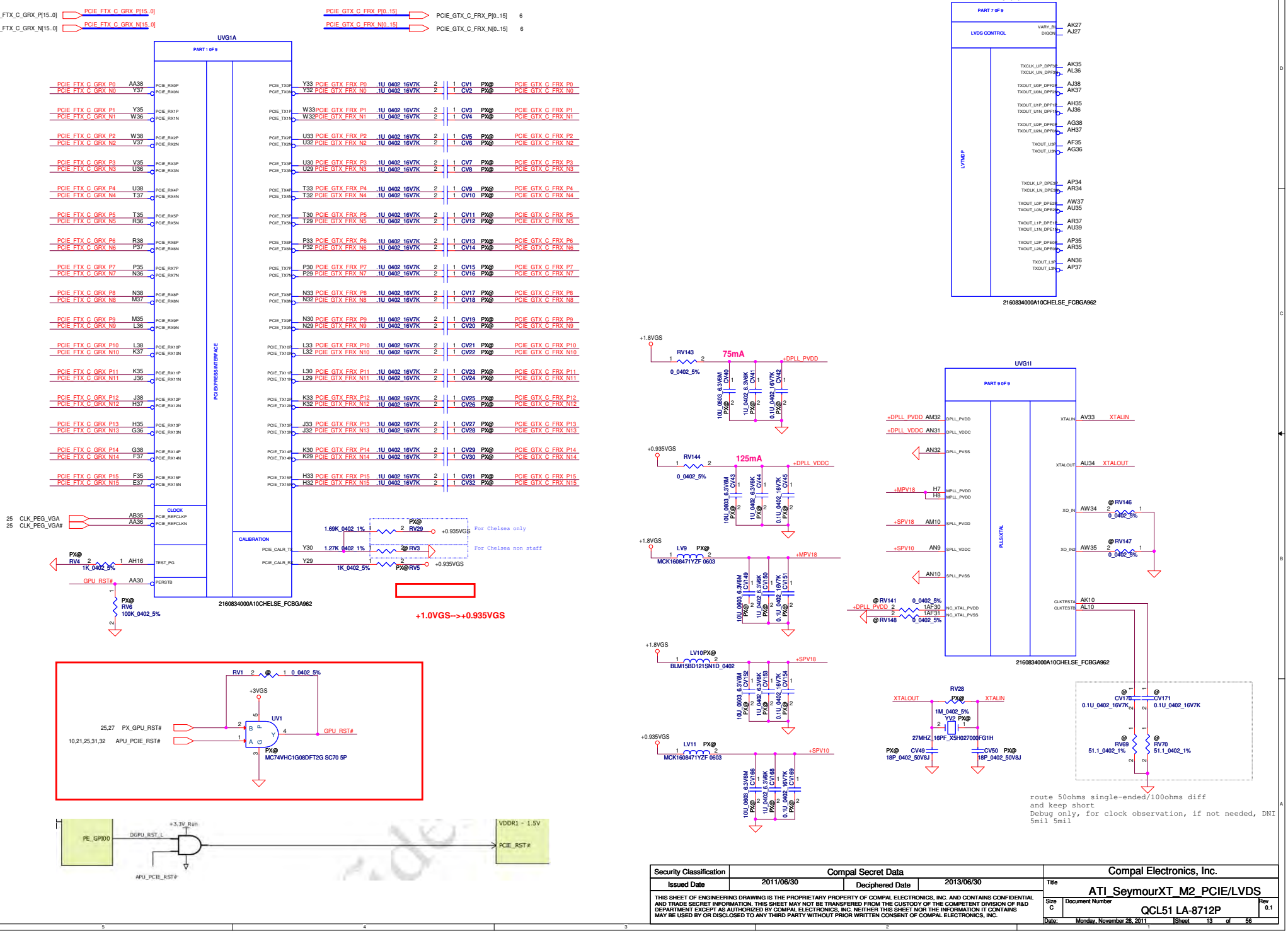
Compal Electronics, Inc.

Title: DDRIII SO-DIMM 2

Size: Custom | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 12 of 56

LVDS Interface



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Title	ATI_SeymourXT_M2_PCIE/LVDS		
Size C	Document Number QCL51 LA-8712P		Rev 0.1
Date: Monday, November 28, 2011	Sheet 13 of 56		

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS <all internal PD>	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE TRANSMITTER Power Saving Enable 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	Internal use only.This Pad has an internal PD and Must be 0V at reset. The pad may be left unconnected.	0
RSVD	H2SYNC		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT GPIO13,12,11(config 2,1,0): internal PD. a)If BIOS_ROM_EN=1,the config[2:0] defines the ROM type. b)If BIOS_ROM_EN=0,the config[2:0] defines the primary aperture size.	XXX Memory apertures config[3:0] 128MB 000 256MB 001 64MB 010
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

STRAPS

Update net name

RV9 SMT-->@

VRAM ID

Internal VGA Thermal Sensor

Use Internal Thermal Sensor

External VGA Thermal Sensor: No stuff

Base on AMD Check list
GPIO_23_CLKREQB should be reserve

11/15 AMD suggest

11/16 add

(1.8V@20mA TSVDD)

(1.8V@65mA AVDD)

(1.8V@100mA VDD1DI)

For Chelsea non staff

2160834000A10CHELSE_FCBGA962

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Main_MSIC

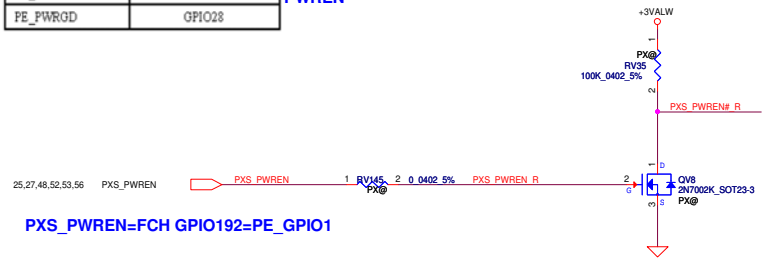
Size: C | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 14 of 56

Name	FCH Pin Assignments
	Hudson-2 / Hudson-3
PE_GPIO0	GPIO191
PE_GPIO1	GPIO192
PE_PWRGD	GPIO28

GPU_Reset

PWREN

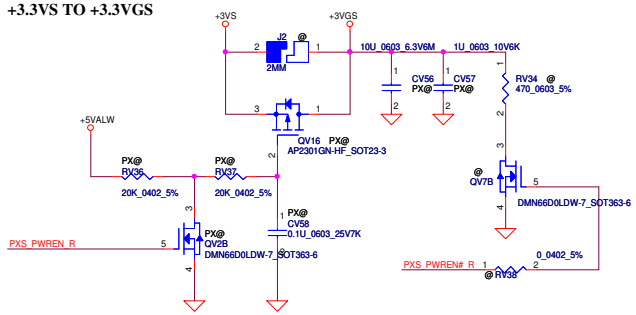


PXS_PWREN=FCH GPIO192=PE_GPIO1

Del +1.8VGS DC DC

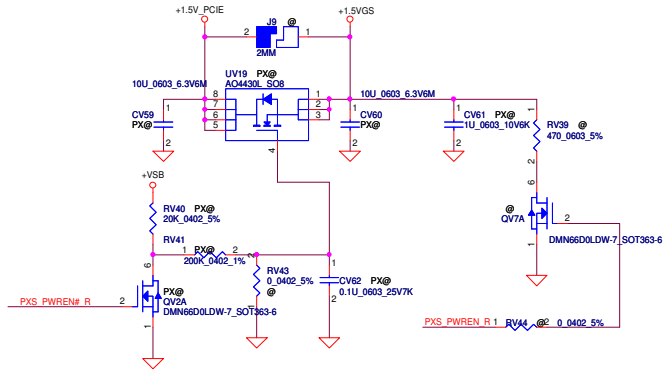
11/10 follow Lotus

+3.3VS TO +3.3VGS



+1.5V_PCIE TO +1.5VGS

Add +1.5VGS DC DC

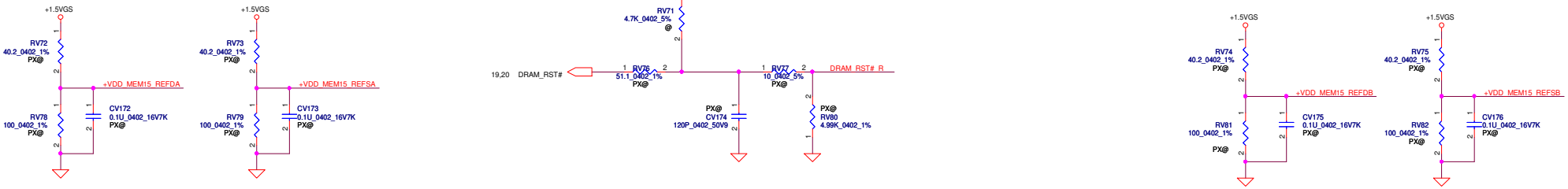


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Title	ATI_SeymourXT_M2_BACO POWER		
Size C	Document Number QCL51 LA-8712P		Rev 0.1
Date: Monday, November 28, 2011	Sheet 15 of 56		

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
128M16 (2G) H5TQ2G63DFR-11C Hynix 2GB PN:SA00003YO70	RV56 1	RV58 0	RV61 0
128M16 (2G) K4W2G1646C-HC11 Samsung 2GB PN:SA000047Q00	RV56 0	RV57 1	RV61 0
64M16 (1G) H5TQ1G63DFR-11C Hynix 1GB PN:SA000041S20	RV59 1	RV58 0	RV60 1
64M16 (1G) K4W1G1646G-BC11 Samsung 1GB PN:SA00004GS20	RV59 0	RV57 1	RV60 1

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2



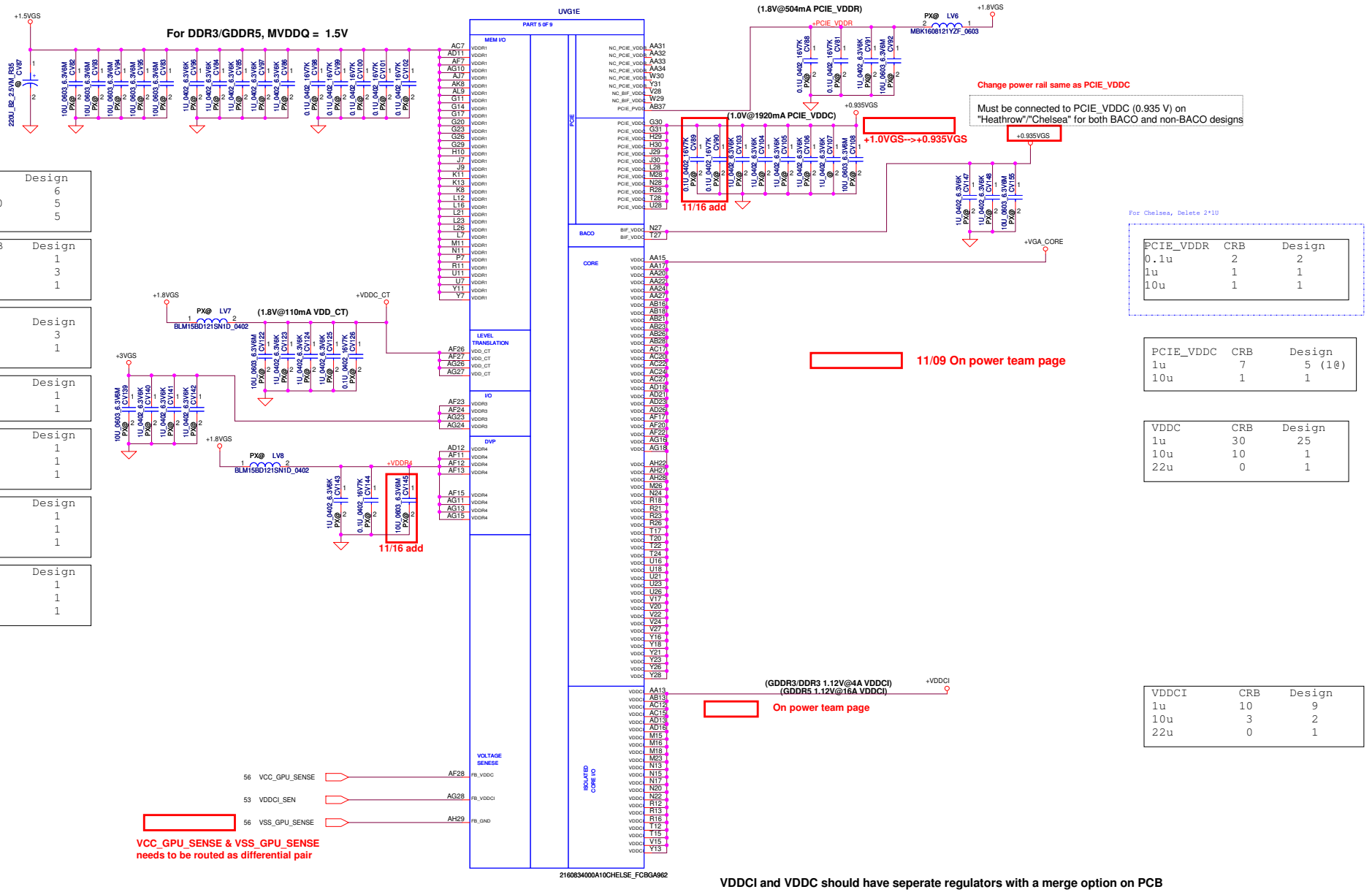
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_MEM IF

Size	Document Number	Rev
C	QCL51 LA-8712P	0.1

Date: Monday, November 28, 2011 Sheet 16 of 56



VDDR1	CRB	Design
0.1u	6	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

For Chelsea, Delete 2*1U

PCIE_VDDR	CRB	Design
0.1u	2	2
1u	1	1
10u	1	1

PCIE_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

VDDC	CRB	Design
1u	30	25
10u	10	1
22u	0	1

VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

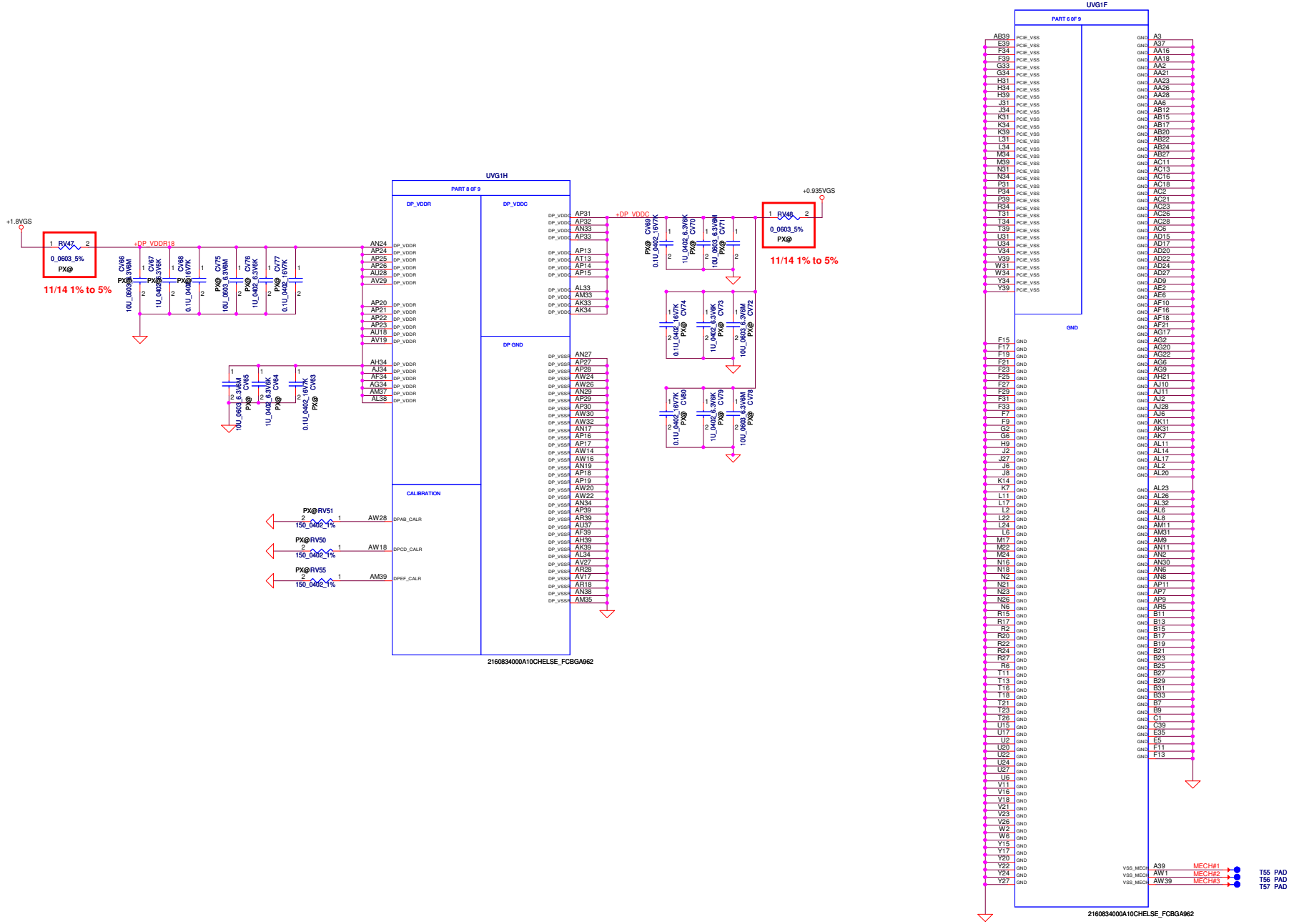
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

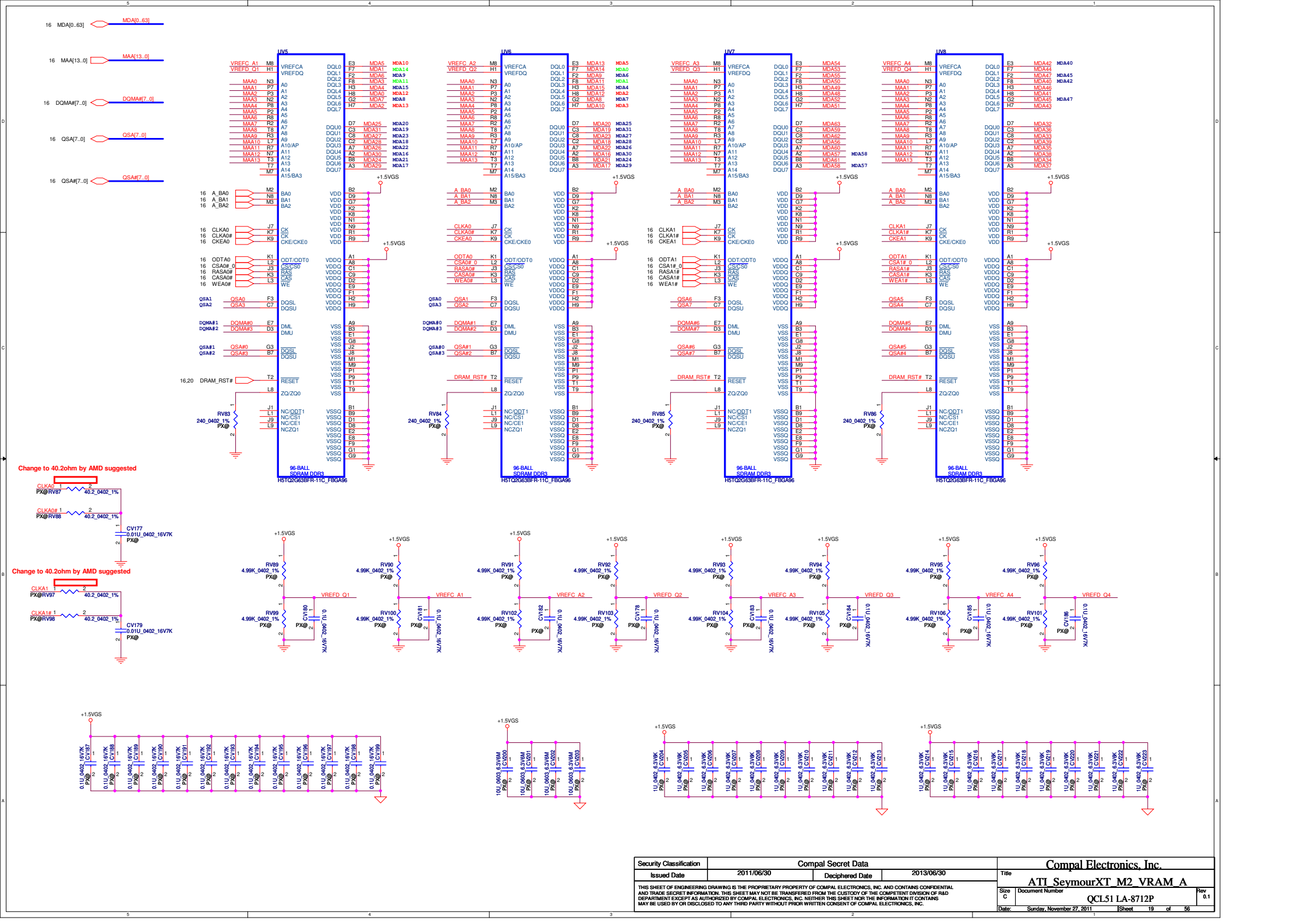
Title: ATI_SeymourXT_M2_Power

Size	Document Number	Rev
C	QCL51 LA-8712P	0.1

Date: Monday, November 28, 2011 Sheet 17 of 56



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/30	Deciphered Date	2013/06/30
Title	ATI_SetmourXT_M2_PWR_GND		
Size C	Document Number QCL51 LA-8712P		Rev 0.1
Date: Monday, November 28, 2011	Sheet 18 of 56		



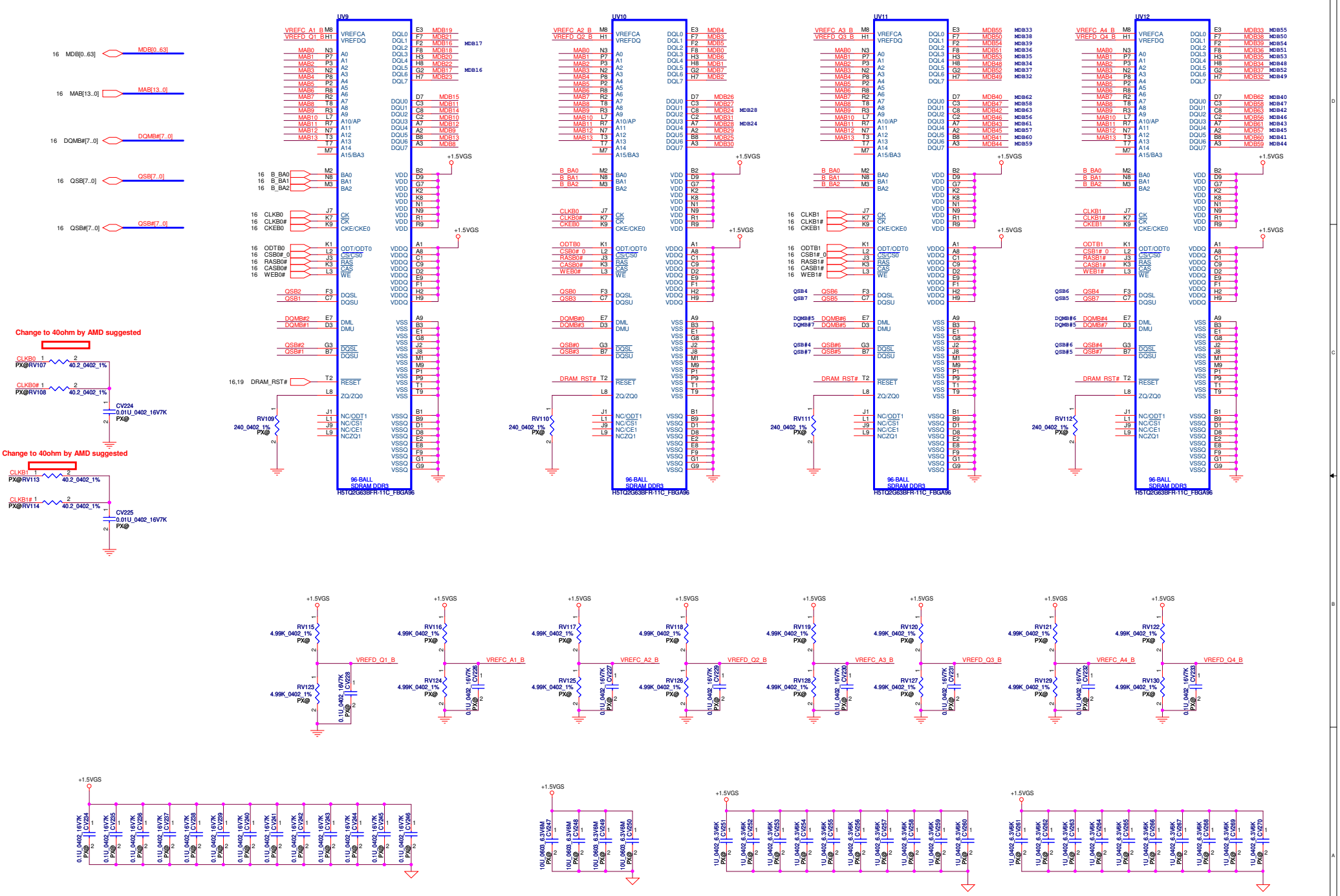
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_A

Size	Document Number	Rev
C	QCL51 LA-8712P	0.1

Date: Sunday, November 27, 2011 | Sheet 19 of 56



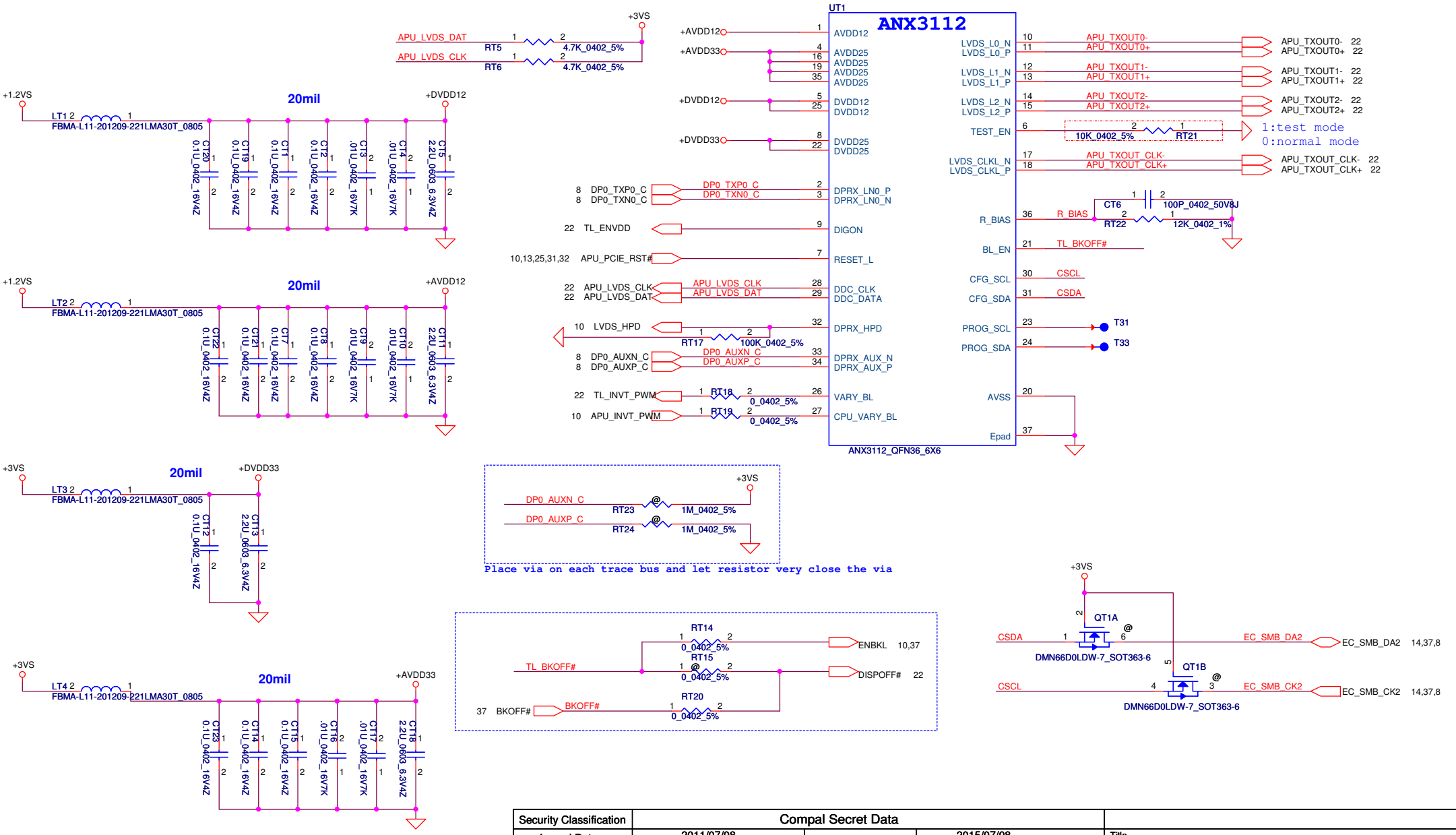
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_B

Size	Document Number	Rev
C	QCL51 LA-8712P	0.1

Date: Sunday, November 27, 2011 | Sheet 20 of 56



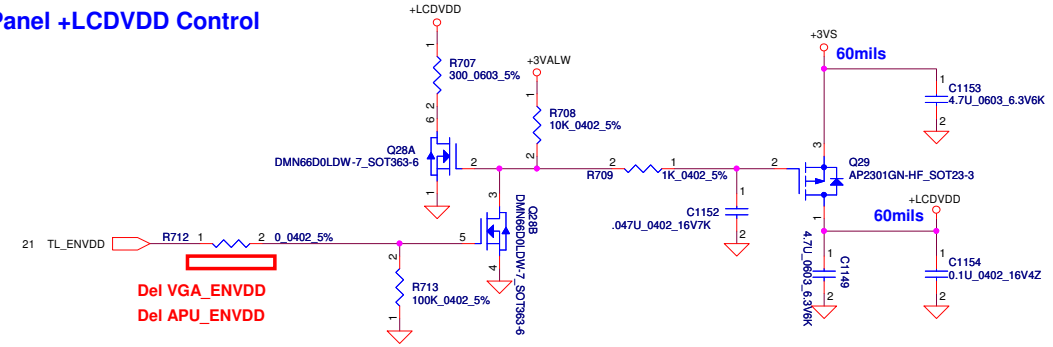
Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

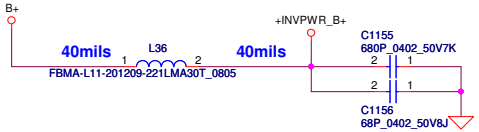
Title: *LVDS Translator - ANX3112X*

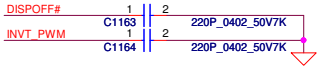
Size: B | Document Number: *QCL51 LA-8712P* | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 21 of 56

Panel +LCDVDD Control



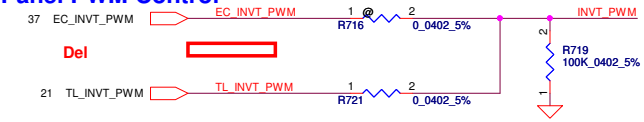


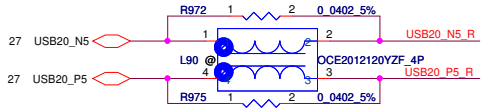


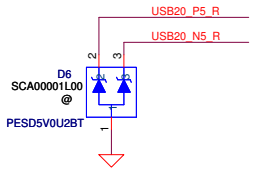
Panel Backlight Control

Modify and change to page 21

Panel PWM Control

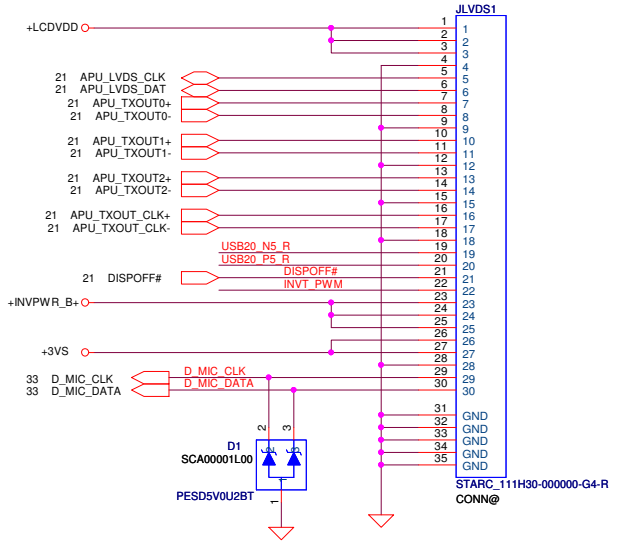






<Translator LVDS Output>

LVDS Connector



no updated.

11/10 follow QCL50

Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

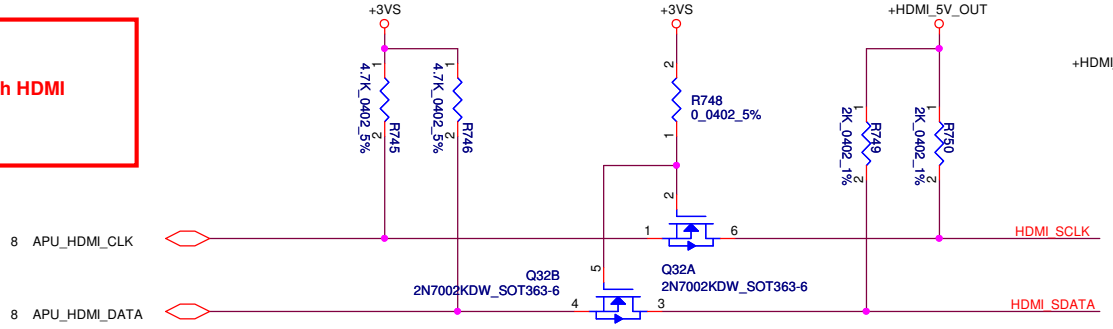
Compal Electronics, Inc.

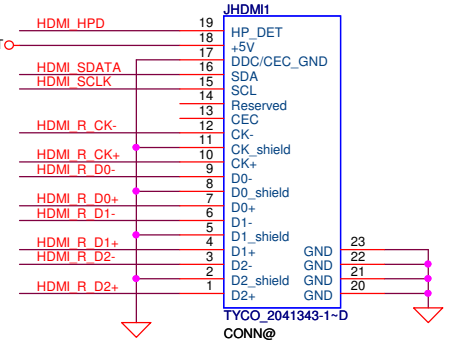
Title: LVDS/eDP Connector

Size	Document Number	Rev
Custom	QCL51 LA-8712P	0.1

Date: Monday, November 28, 2011 Sheet 22 of 56

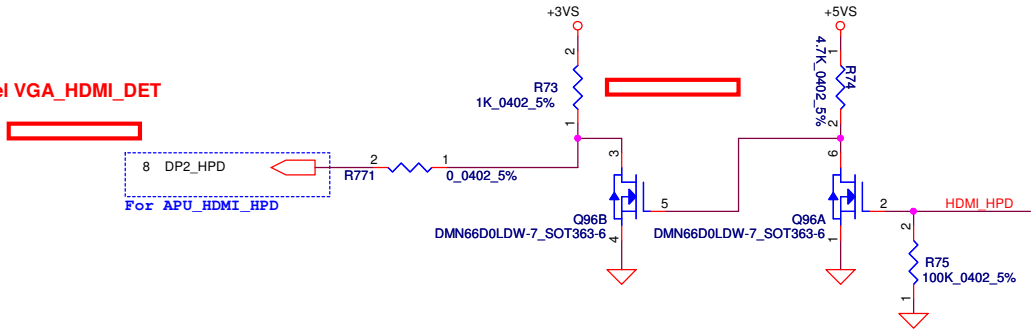
Combine with HDMI

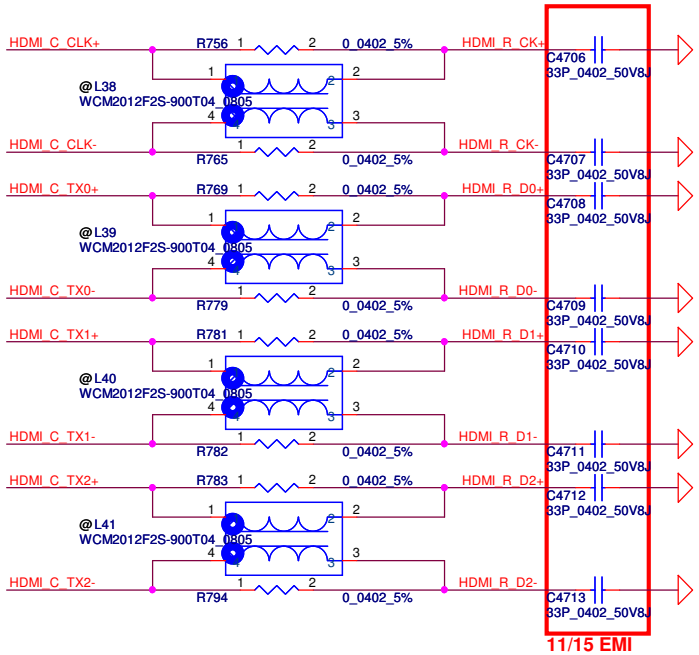




11/05 update footprint.

Del VGA_HDMI_DET



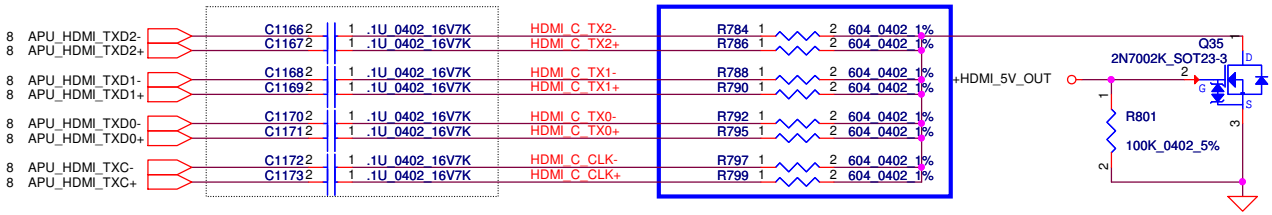


11/15 EMI
Near connector

Close to HDMI conn

10/27 change to 604 ohm.

From APU



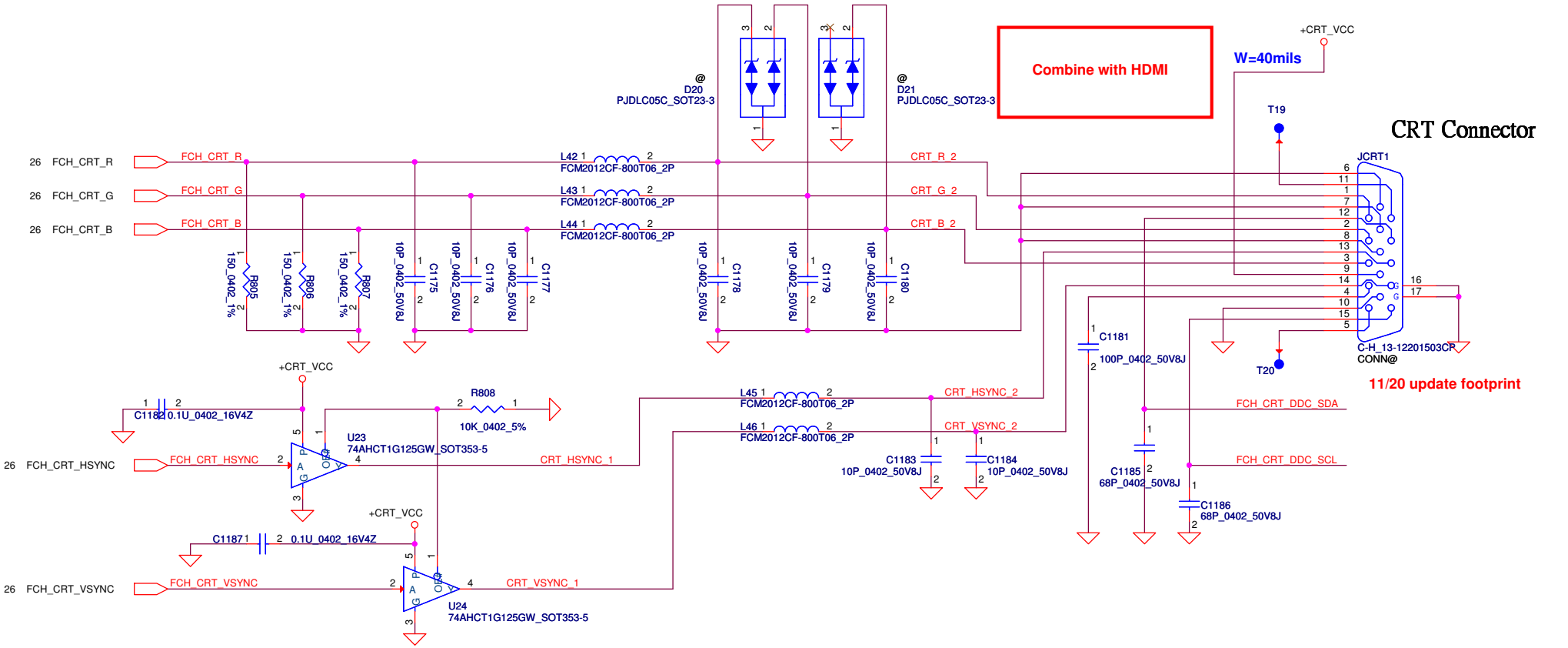
Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: HDMI Connector

Size: B | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 23 of 56



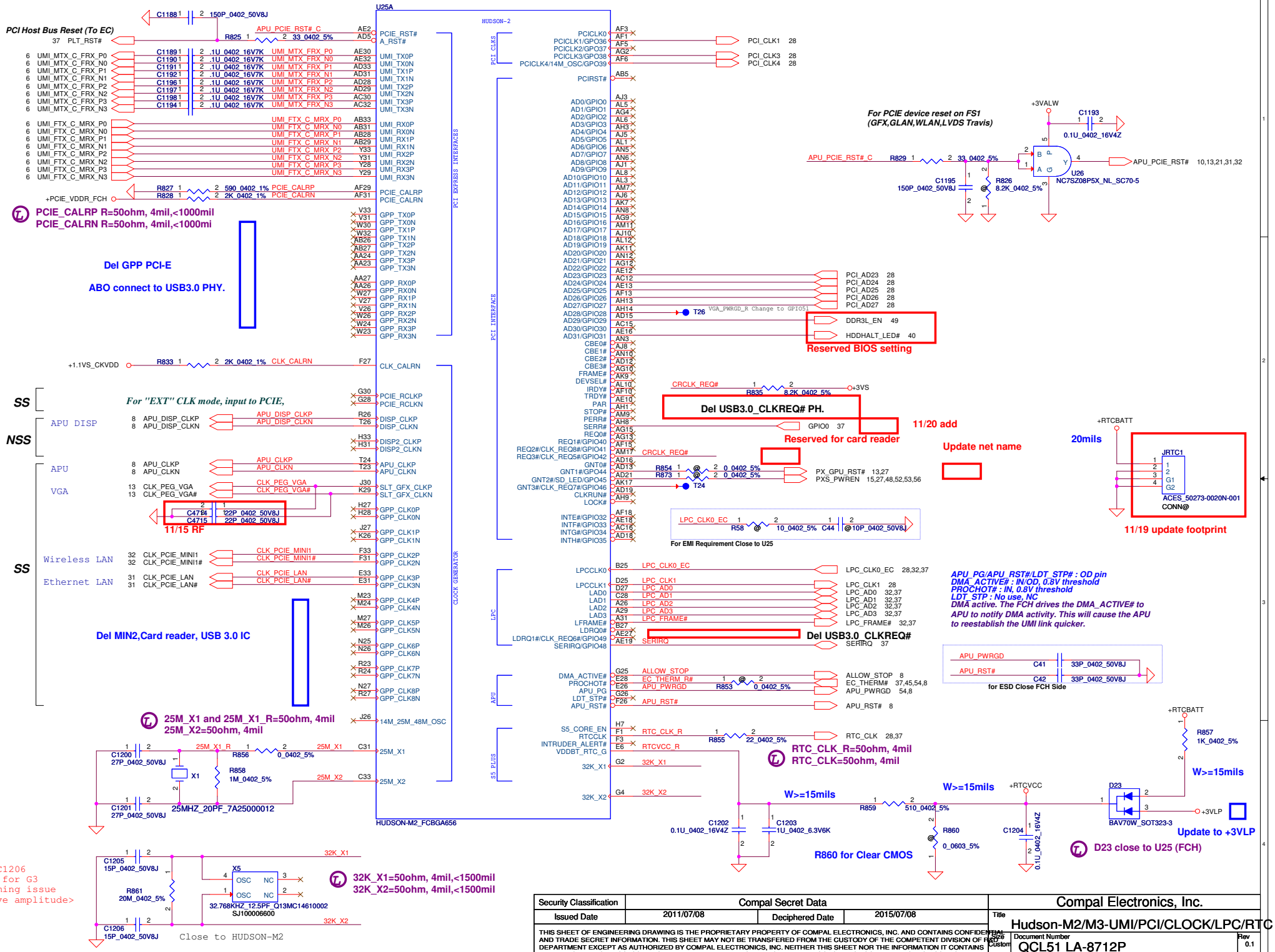
Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 24 of 56



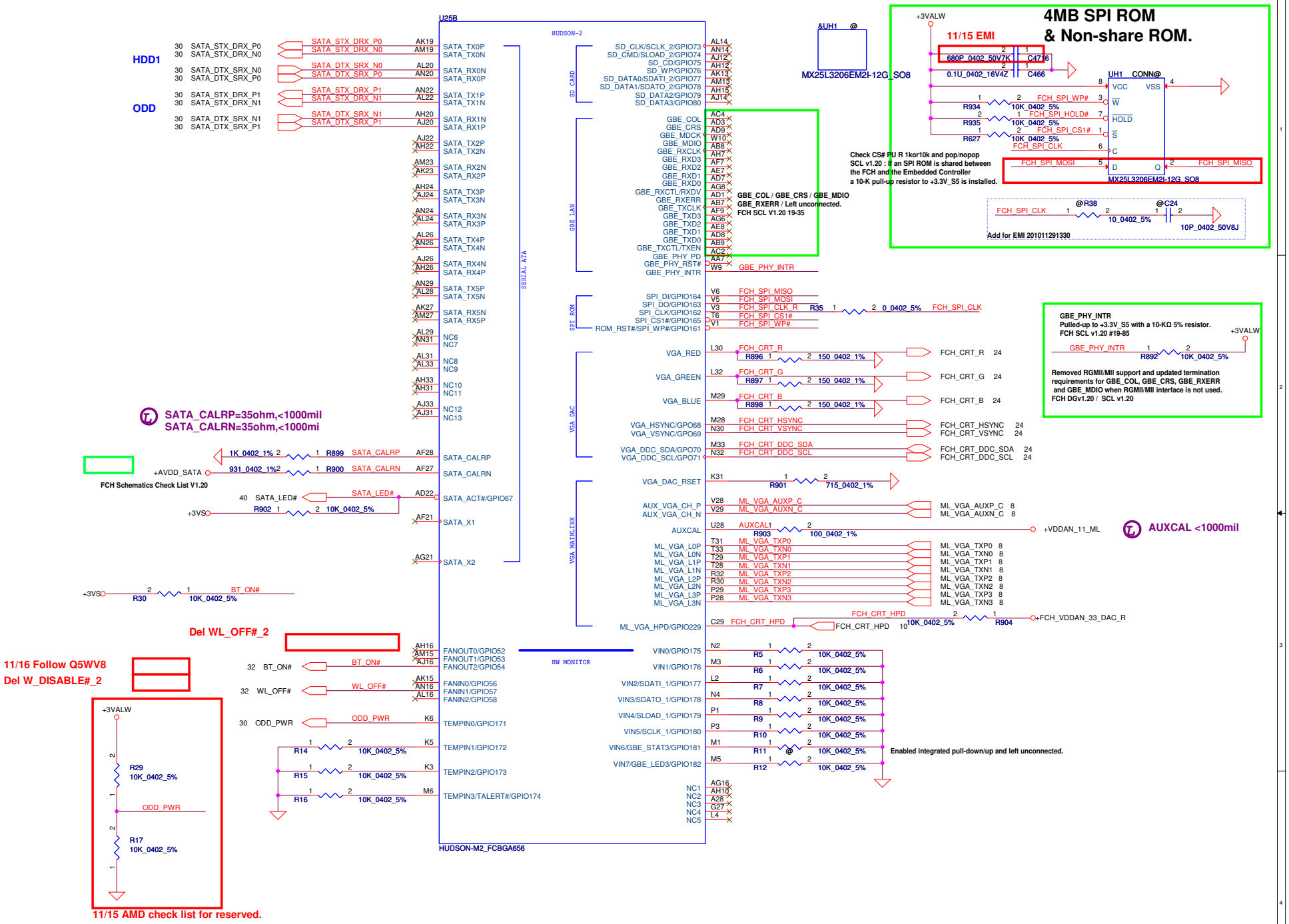
Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC

Size	Document Number	Rev
B25 Custom	QCL51 LA-8712P	0.1

Date: Monday, November 28, 2011 | Sheet 25 of 56



Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.			
Title	Hudson-M2/M3-SATA/GBE/HWM		
Size: B/5 Custom	Document Number: QCL51 LA-8712P		Rev: 0.1
Date: Monday, November 28, 2011	Sheet 26 of 56		

FCH_PCIE_RST# IS FOR PCIE DEVICES ON Hudson-M2/M3

Del FCH_PCIE_RST#

THERMTRIP:
Need level shift from +3VALW to +1.5V
Note: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.

SM bus 0-->S0 PWR domain
SM bus 1-->S5 PWR domain

FCH GEVENT (S5 domain) with isolation circuit to avoid leakage

Del Card det

Del MINI2_CLKREQ#

PC_BEEP use.

11/08 Reserved BIOS setting

11/15 ESD

Del SIMB output

33ohm termination resistor at CODEC side

Add USB_OC0#

Change GPIO fellow Pumori

Del FCH_GPIO187

Update net name

For FCH internal debug use

Del MINI2_CLKREQ# PH.

11/15 RF

Del FCH_GPIO187 R57 R55

DIS is High
DIS is High

Project SKU ID		
GPIO189 (use VGA)	L(NO) R44	H(YES) R43
GPIO190 (use PX)	L(NO) R46	H(YES) R45
GPIO188	TBD	TBD
GPIO187 (Reserved)		

U25D HUDSON-2

USB 2.0 port(Right-1)
USB 2.0 port(Left-2)
USB 2.0 port(Left-1)
Del USB port 9
Mini1-WLAN
Del USB port 7
Camera
USB port3-->USB port0
FP
USB 2.0 port(Right-2)

USBSS_CALRP=35ohm,<1000mil
USBSS_CALRN=35ohm,<1000mi

USB 3.0 port(Right-1)
USB 3.0 port(Left-2)
USB 3.0 port(Left-1)

For PCIE device reset on FS1 (GFX,GLAN,WLAN,LVDS Travis)

HUDSON-M2_FCBGA656

Hudson-M2/M3 OHCI CTL DEV 20, Fn 5 <Disable CTL>
Hudson-M2 EHCI CTL DEV 22, Fn 2 <Disable CTL of M2>
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0
Hudson-M2/M3 EHCI CTL DEV 19, Fn 2
Hudson-M2/M3 EHCI CTL DEV 18, Fn 2 <Support Wakeup>
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0

Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: Hudson-M2/M3-ACPI/USB/EC

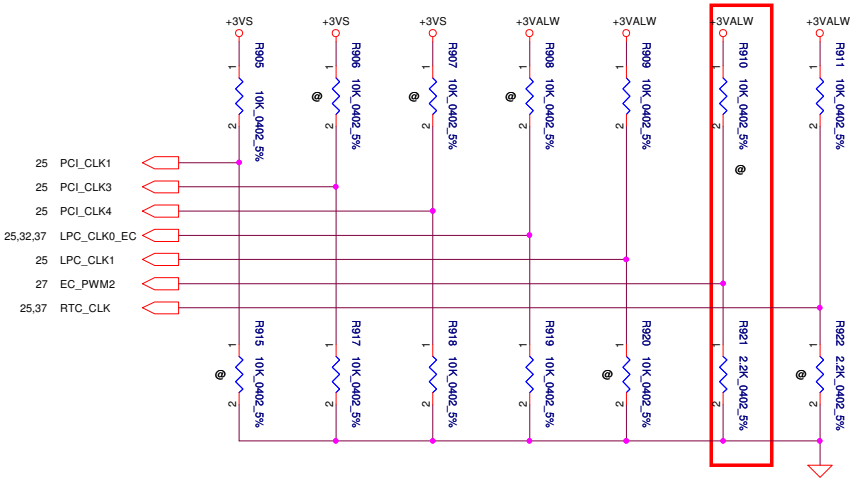
Size	Document Number	Rev
C	QCL51 LA-8712P	0.1

Date: Monday, November 28, 2011 Sheet 27 of 56

Change to SPI

STRAP PINS

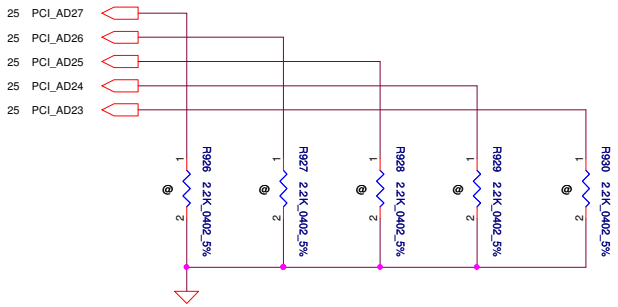
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM	S5 PLUS MODE ENABLED

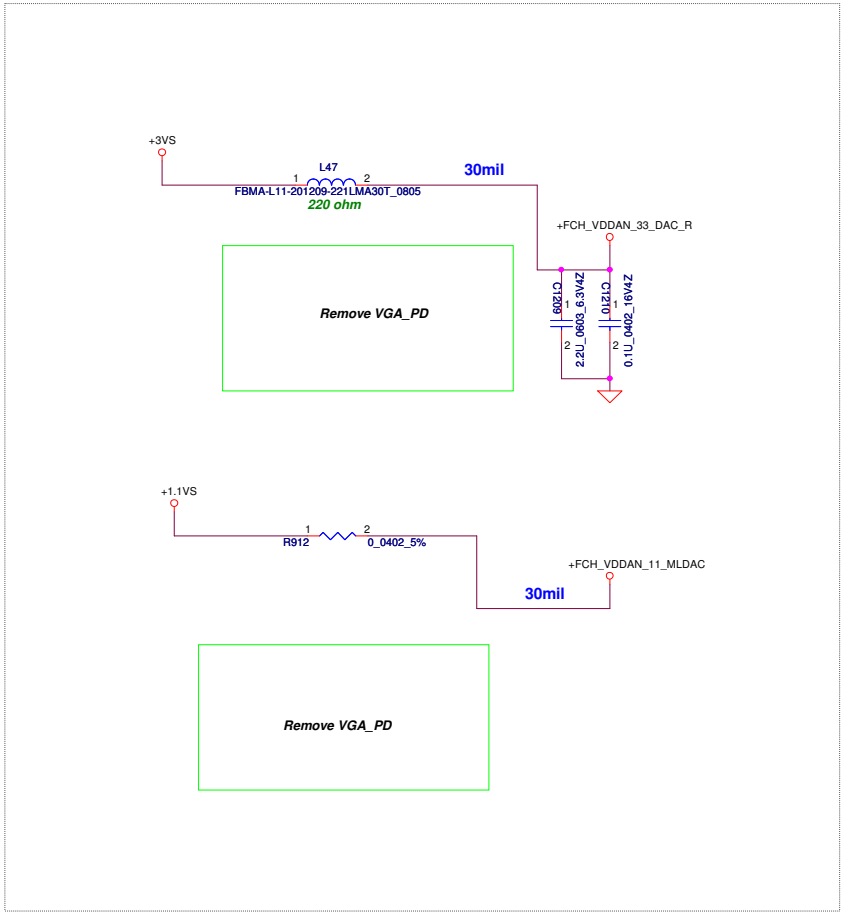


DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23
No external R	USE PCI PLL DEFAULT	Normal REFCLK termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	Inverted REFCLK termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





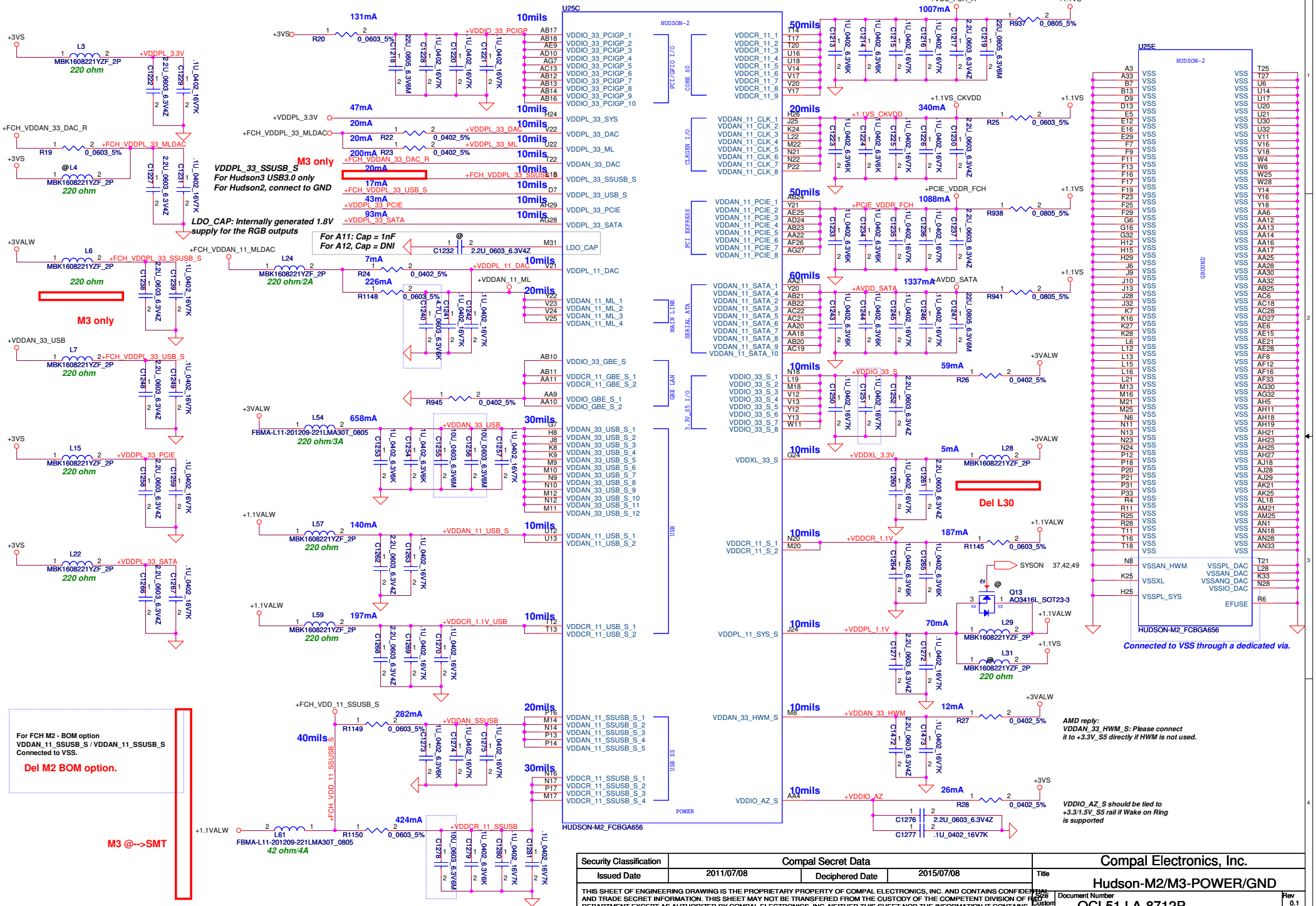
Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: Hudson-M2/M3-STRAP

Size: B (5/25 Custom) | Document Number: QCL51 LA-8712P | Rev: 0.1

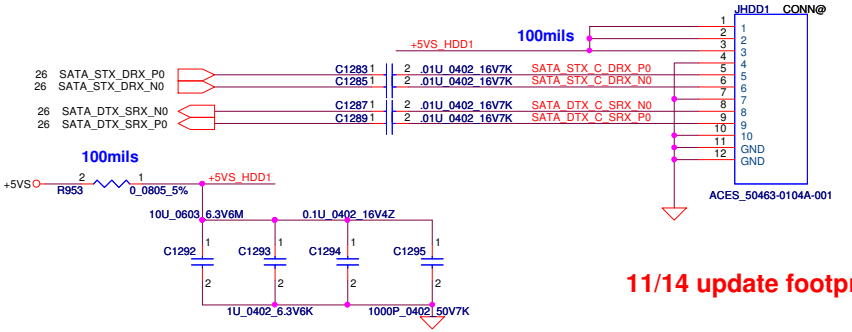
Date: Monday, November 28, 2011 | Sheet 28 of 56



Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

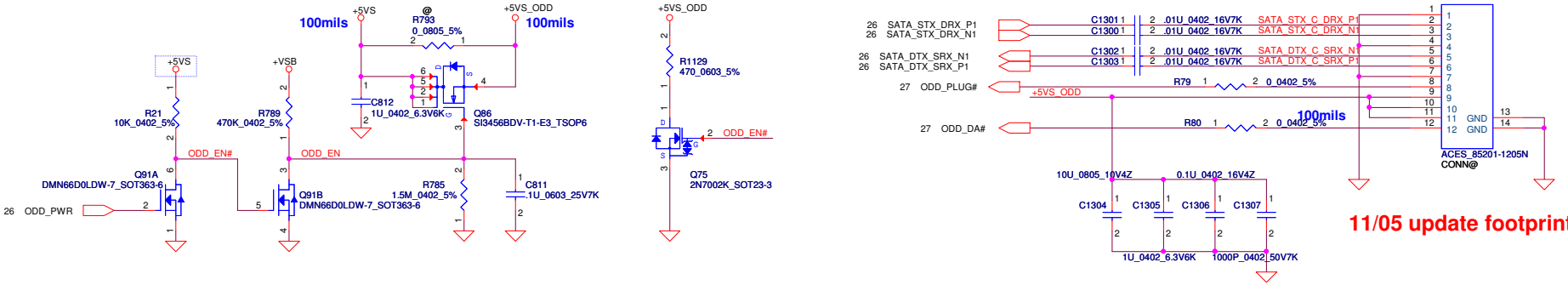
Compal Electronics, Inc.			
Title	Hudson-M2/M3-POWER/GND		
Size: B, Custom	Document Number: QCL51 LA-8712P		Rev: 0.1
Date: Monday, November 28, 2011	Sheet 29 of 56		

SATA HDD1 Conn.



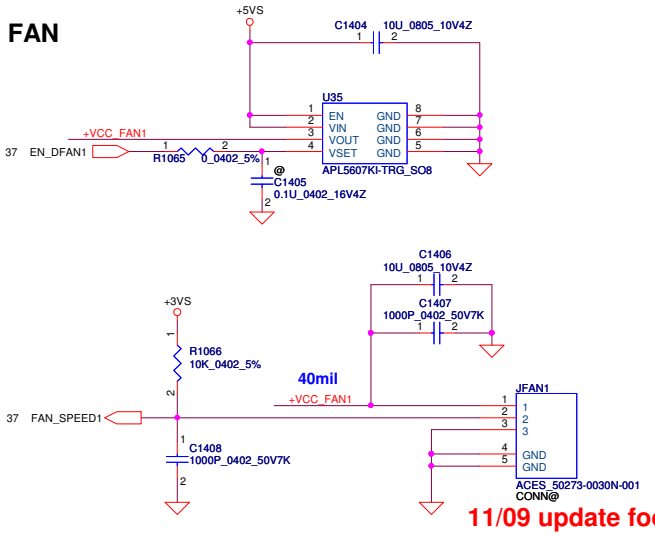
11/14 update footprint

ODD conn



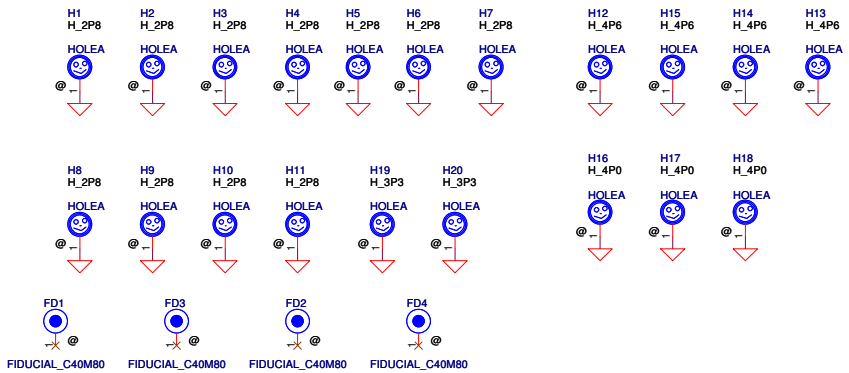
11/05 update footprint

FAN



11/09 update footprint to VT.

Screw Hole



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/08	Deciphered Date 2015/07/08	Title HDD/ODD/FAN/SCREW
Size B	Document Number QCL51 LA-8712P		Rev 0.1
Date: Monday, November 28, 2011	Sheet 30 of 56		

W=60mils

W=60mils

1.5A

These caps close to U1: Pin 11,12,39,58,63,64

Modify by Project

11/05 update footprint

11/22 NPTH

Need to check RL6,RL7,RL8 Option

Change net name from PLT_RST# to APU_PCIE_RST#

PN : SA00005B400

Follow QCL50

EMI-ESD

Modify by Project

Check power rail

11/15 Update footprint

11/16 Update footprint for DB

VDD33/18 for SD UHS Mode Power

Switching Regulator Circuit

11/15 EMI

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

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Compal Electronics, Inc.

Title: LAN&CardReader Realtek RTL8411

Size: Document Number: QCL51 LA-8712P

Rev: 0.1

Date: Monday, November 28, 2011

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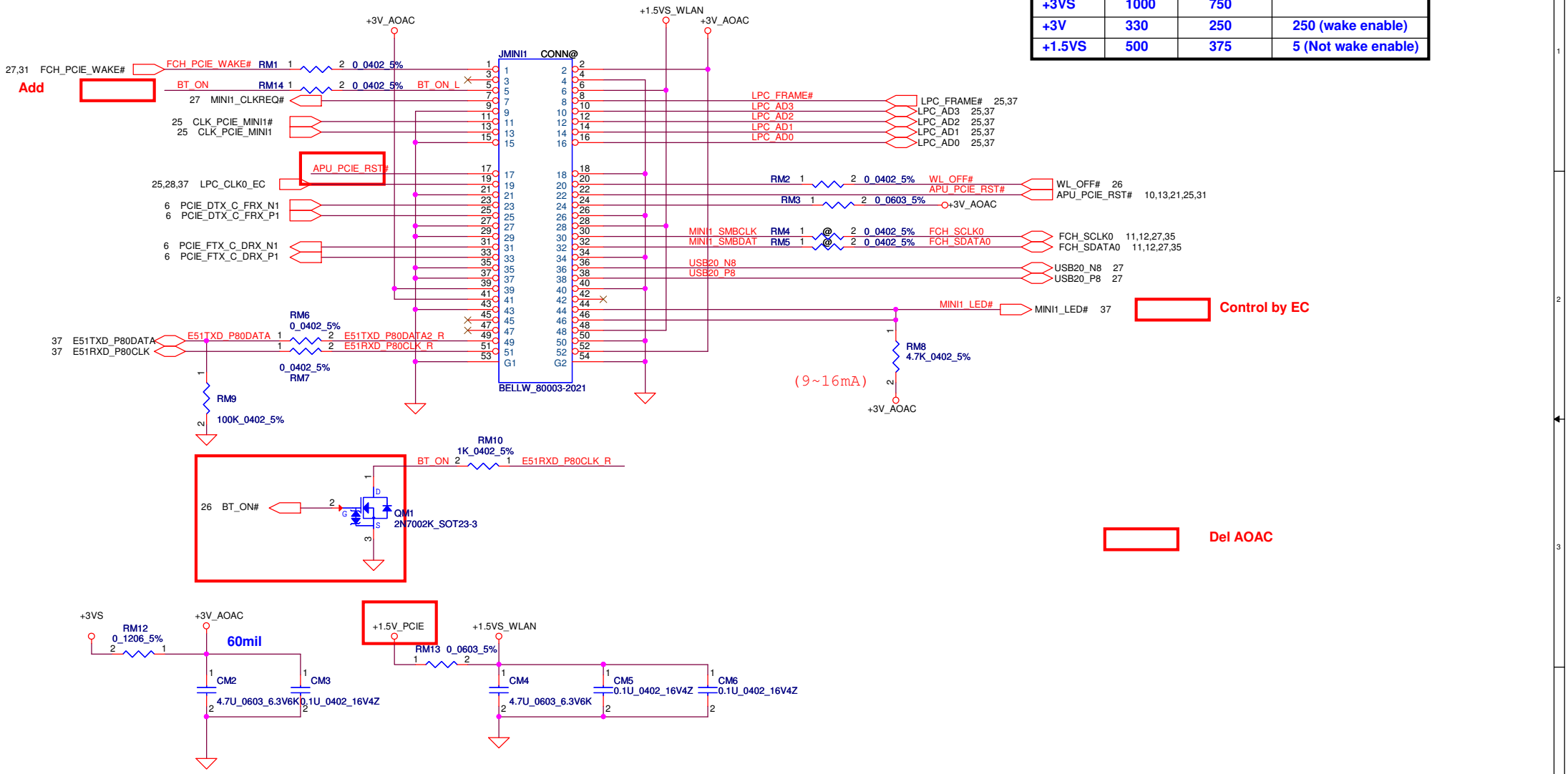
WLAN

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: MINI1 CARD (WLAN) / MINI2 CARD (Option)

Size	Document Number	Rev
B	QCL51 LA-8712P	0.1

Date: Monday, November 28, 2011 Sheet 32 of 56

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

RA2 0805-->0603

Place AVDD ,PVDD,and DVDD cap close to Codec (UA5)

11/15 EMI near UA5

11/16 vendor review

Place C208 close to Codec

CA8,CA10 near UA5 PIN45
CA9,CA21 near UA5 PIN39

C209,C210,CA87,CA89 close to Codec (UA5)

PLACE CLOSE TO UA5 PIN 13

If Sense_A total length is greater than 6 inches, chagne C12 to 0.1uF

If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

PLACE CLOSE TO UA5 PIN 14

External MIC
Combo jack
Headphone

SPK

11/15 modified

Del AOAC

Close to Audio Codec (UA5)

Need confirmed.

11/15 EMI

RA53 need under or near UA5

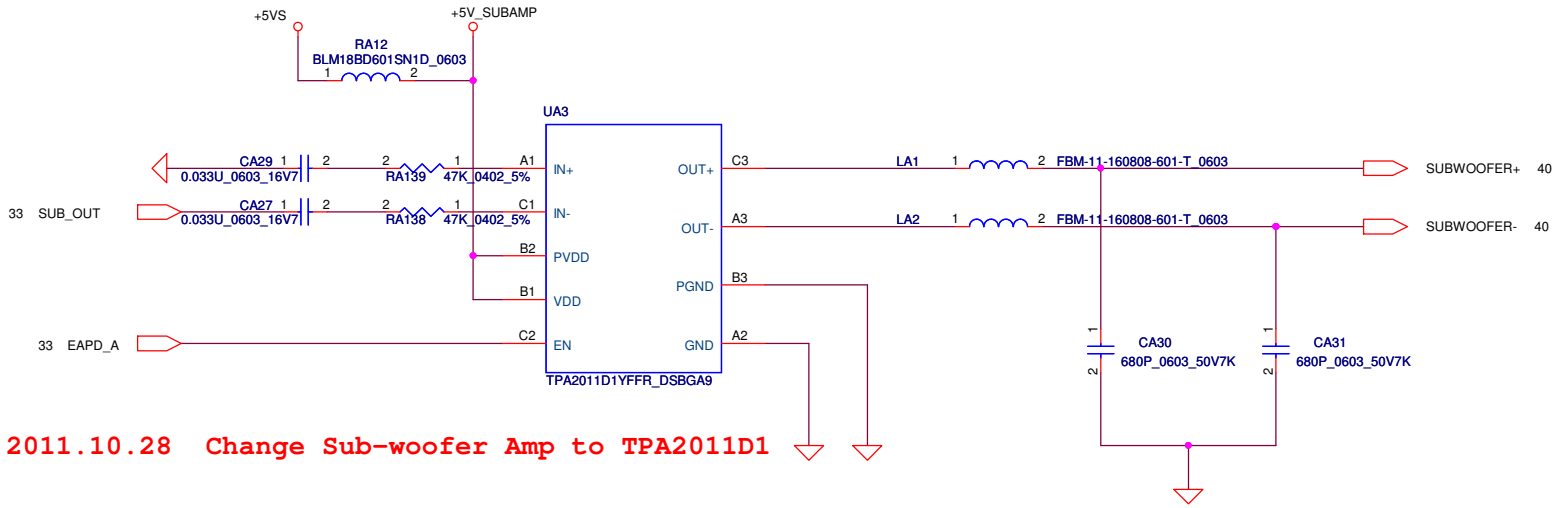
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: Audio IDT 92HD91

Size: Custom | Document Number: LA-8551P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 33 of 56



2011.10.28 Change Sub-woofer Amp to TPA2011D1

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

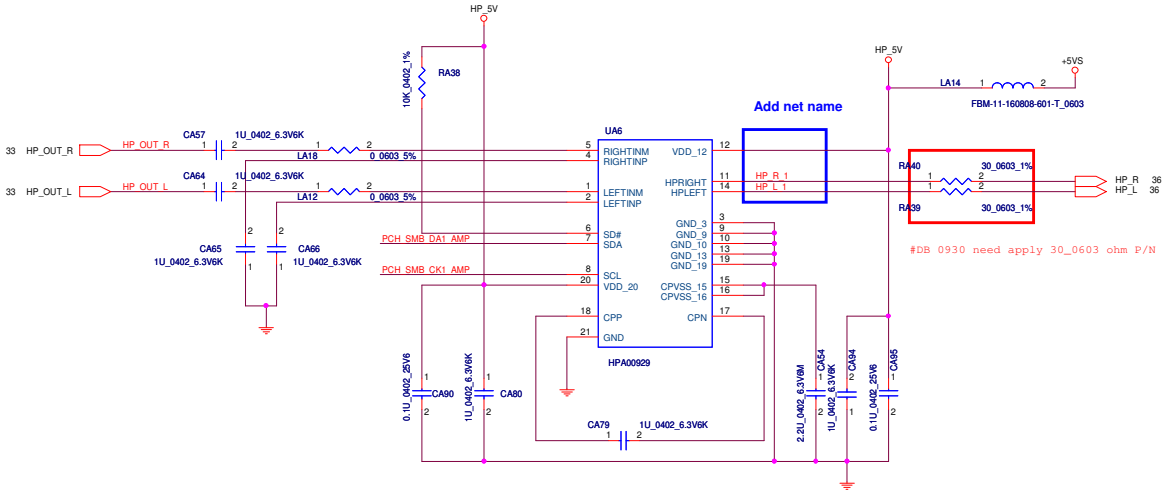
Compal Electronics, Inc.

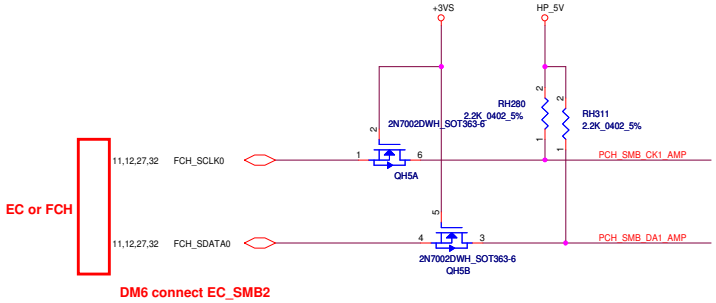
Title: Audio Woofer Amplifier

Size: B | Document Number: LA-8551P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 34 of 56

Headphone amplifier





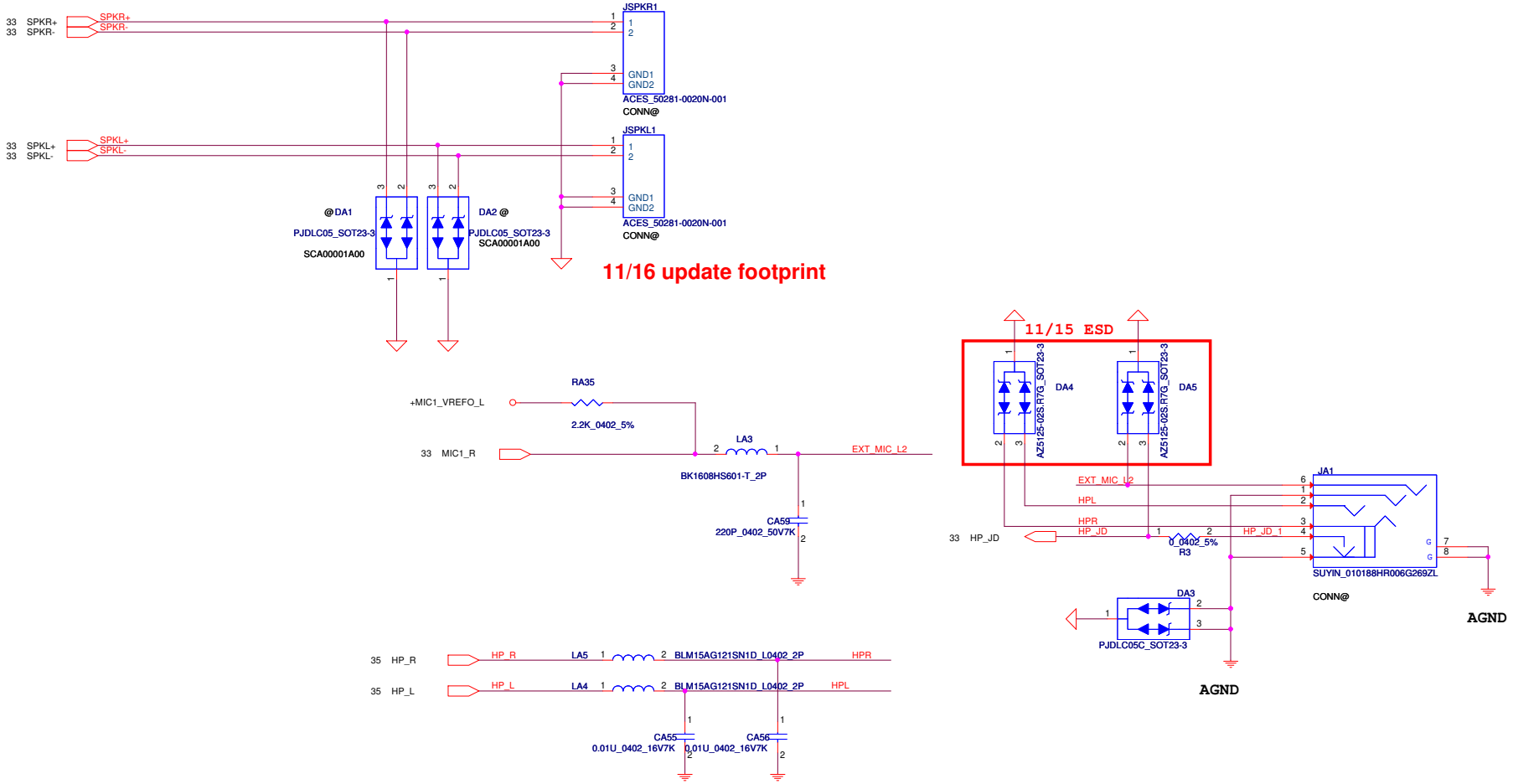
Compal Electronics, Inc.

Title: Audio SPK/HP Amplifier

Size	Document Number	Rev
Custom	LA-8551P	0.1

Date: Monday, November 28, 2011 Sheet 35 of 56

SPK conn



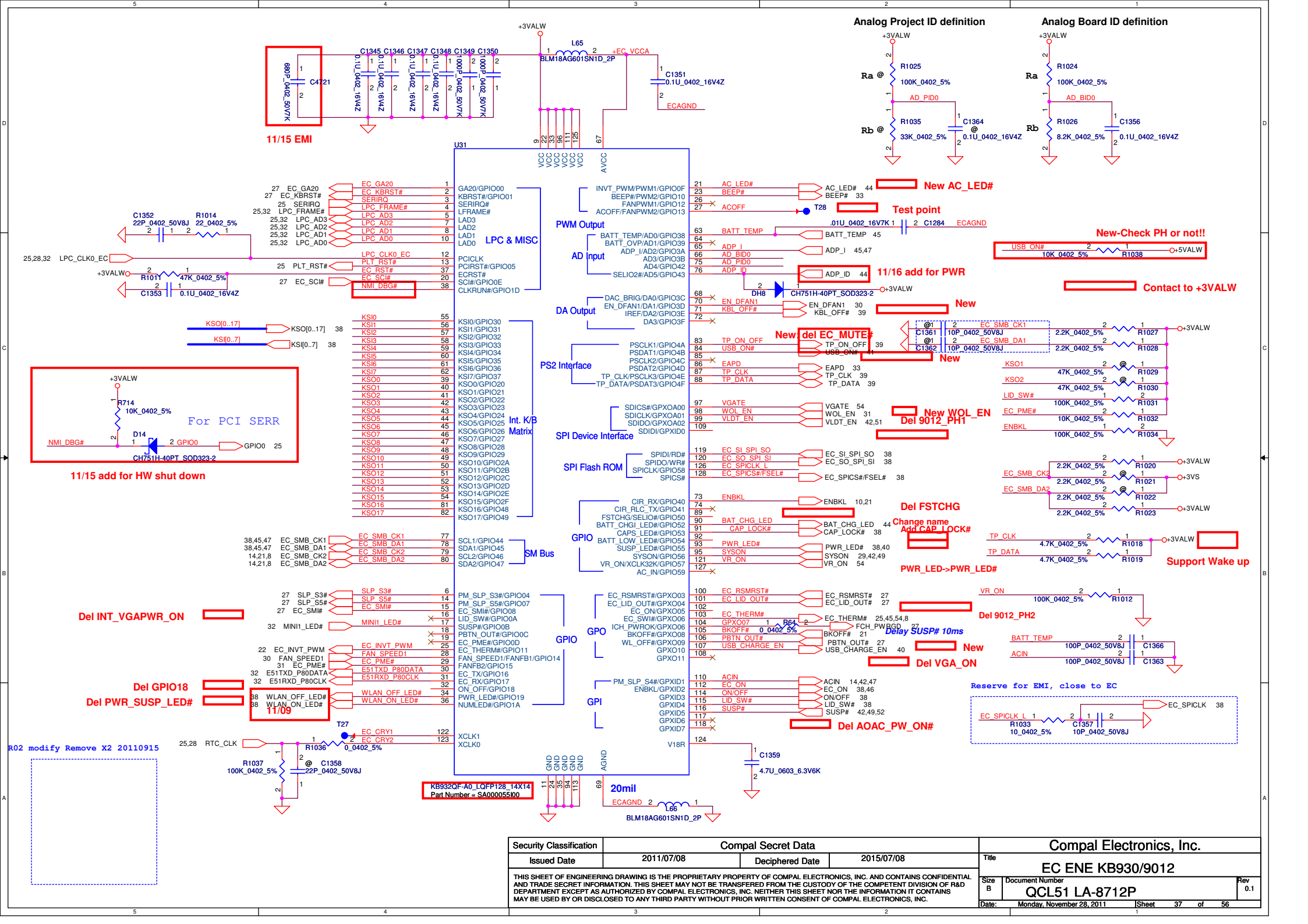
Security Classification	Compal Secret Data		
Issued Date	2009/04/07	Deciphered Date	2012/10/21

Compal Electronics, Inc.

Title: Audio SPK Conn/Jack/MIC

Size	Document Number	Rev
Custom	QCL51 LA-8712P	0.1

Date: Monday, November 28, 2011 Sheet 36 of 56



Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: EC ENE KB930/9012

Size: B | Document Number: QCL51 LA-8712P | Rev: 0.1

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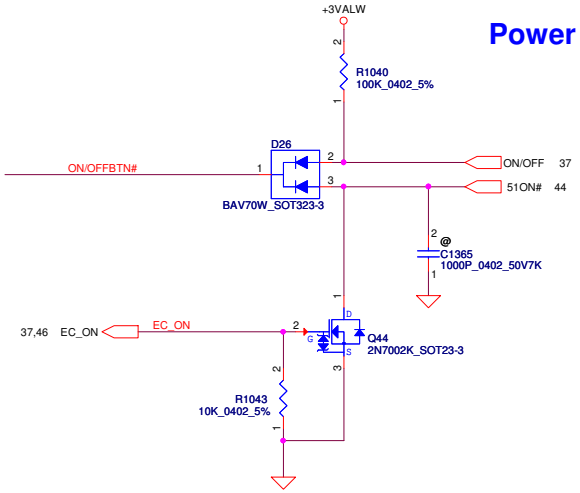
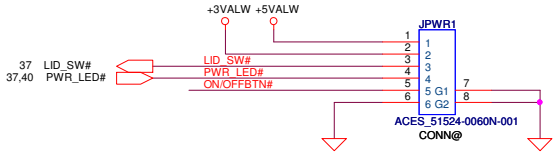
Power Button



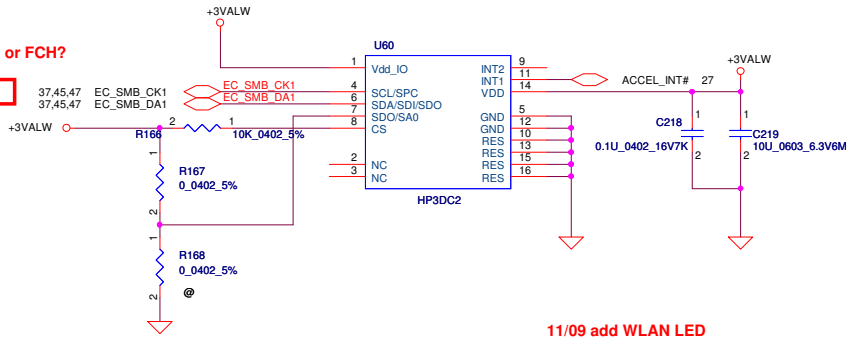
POWER/B



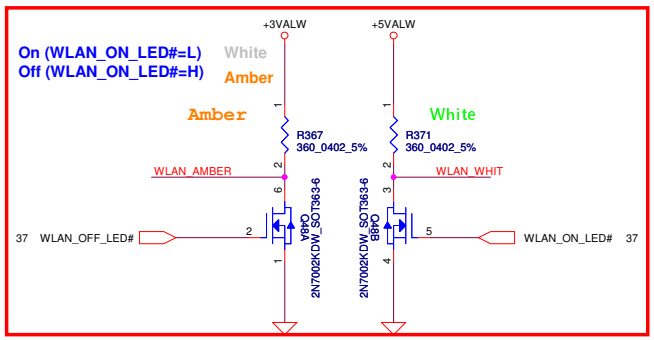
11/05 update footprint

ACCELEROMETER

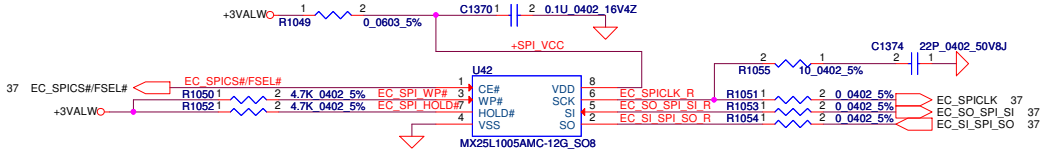
EC or FCH?



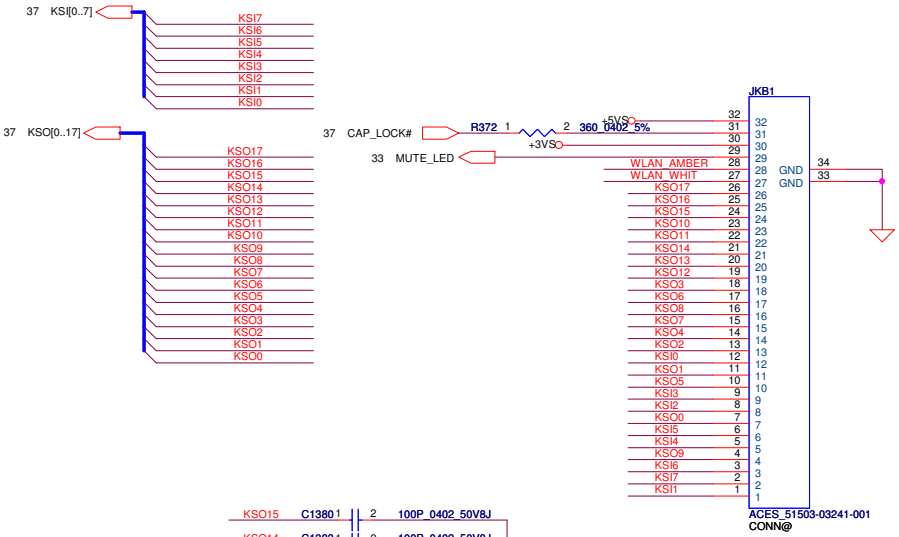
11/09 add WLAN LED



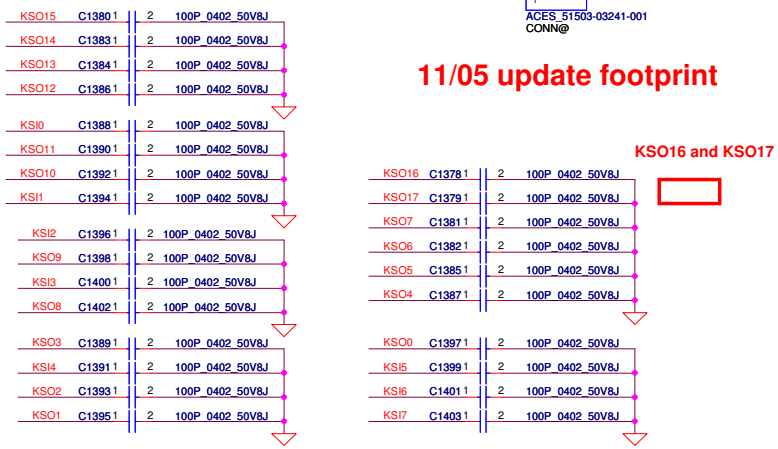
EC BIOS ROM



KB conn



11/05 update footprint

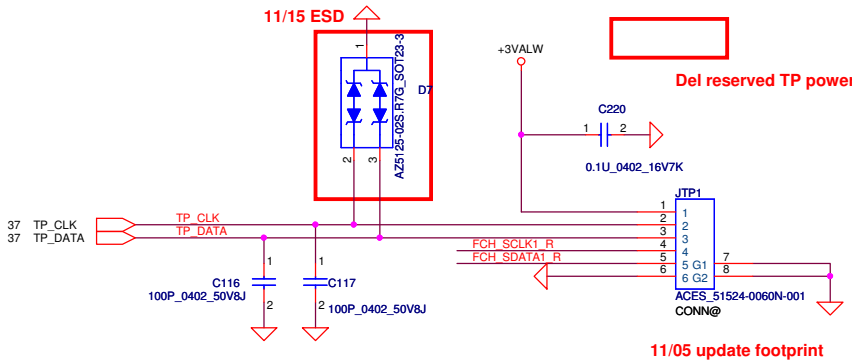


KSO16 and KSO17

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Title	BIOS, I/O Port & K/B CONN/TP CONN/PBTN		
Size B	Document Number QCL51 LA-8712P		Rev 0.1
Date: Monday, November 28, 2011	Sheet 38 of 56		

TP Conn

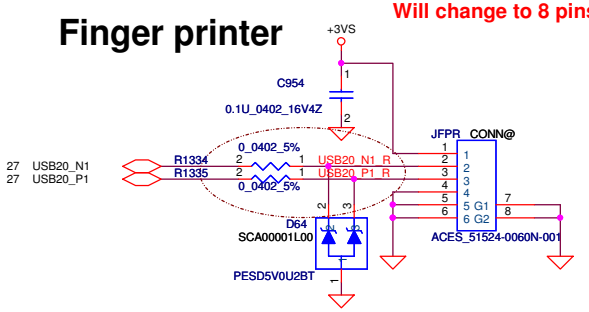


FCH use SMBus 1??

For multi-touch function

Finger printer

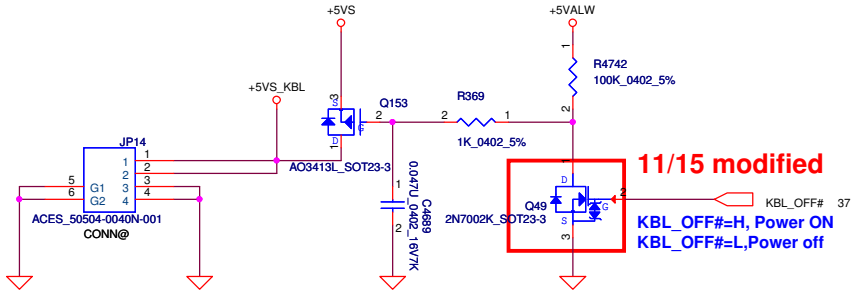
Will change to 8 pins



WLAN ON/OFF LED

11/09 Change to KB connector

Keyboard backlight Conn

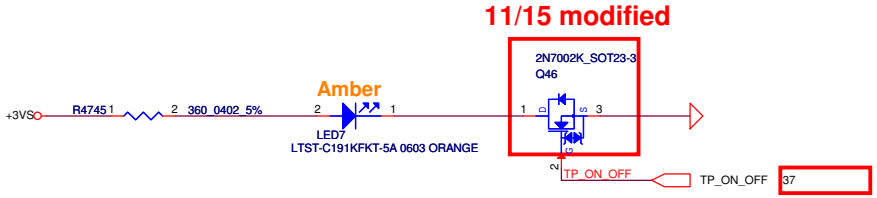


11/05 update footprint

AOAC power control

Del AOAC

T/P On/Off LED



Mute On/Off LED

11/09 Change to KB connector

Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size: Custom | Document Number: QCL51 LA-8712P | Rev: 0.1

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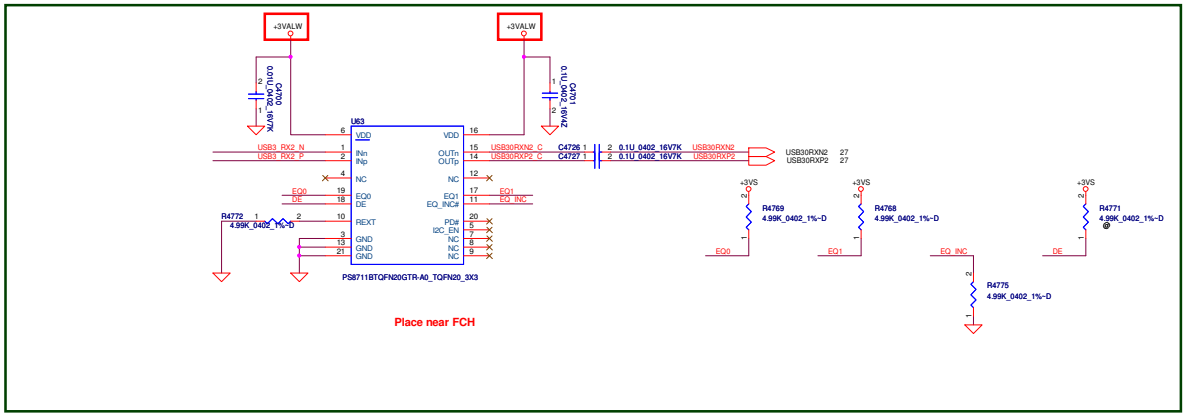
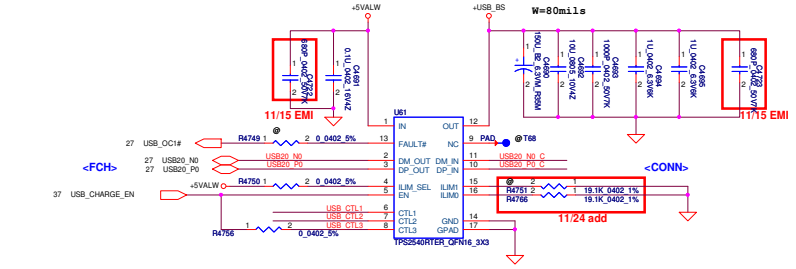
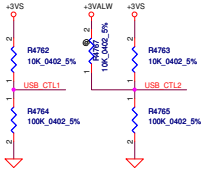
11/24 move to sub board

USB3.0 Repeater



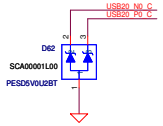
USB Charger

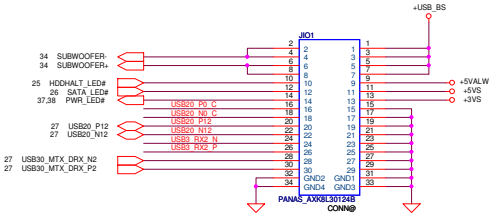




State	S0				S3, S4, S5			
Mode	CDP				DCP			
Control pin	CTL1	CTL2	CTL3	ILIM_SEL	CTL1	CTL2	CTL3	ILIM_SEL
	1	1	1	1	0	0	1	1

11/10 del chock



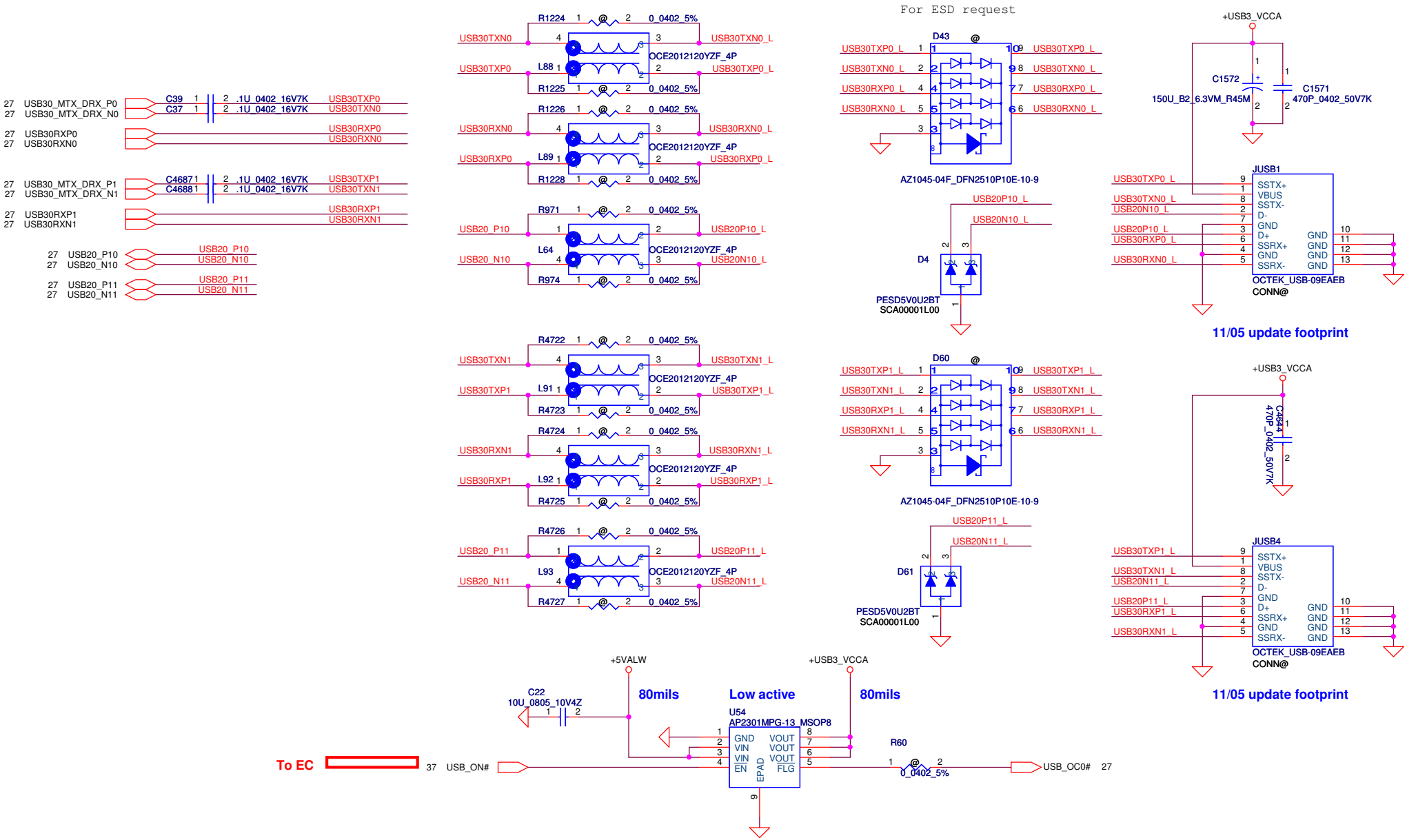


11/16 update footprint

11/24 change pin definition

Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.	
Title	Gsensor/ Sub USB
Size: Custom	Document Number: QCL51 LA-8712P
Rev	0.1
Date: Monday, November 28, 2011	Sheet 40 of 56



Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

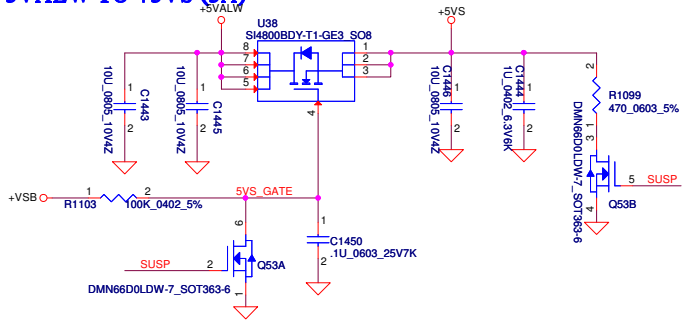
Compal Electronics, Inc.

Title: USB2.0 / USB3.0 / BT

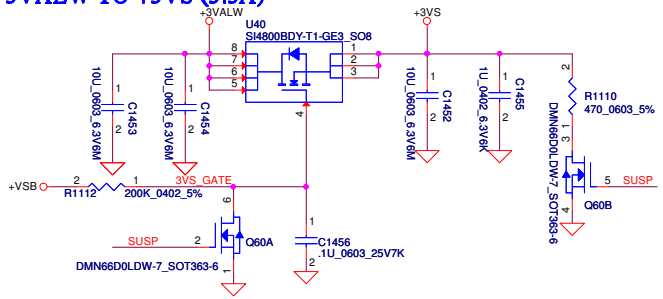
Size	Document Number	Rev
B	QCL51 LA-8712P	0.1

Date: Monday, November 28, 2011 Sheet 41 of 56

+5VALW TO +5VS (5A)



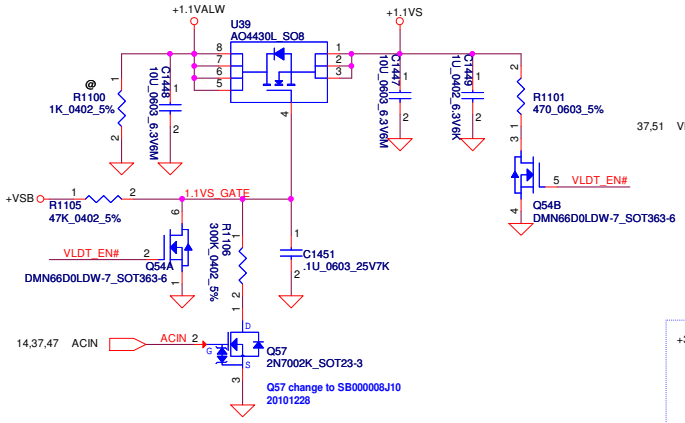
+3VALW TO +3VS (3.3A)

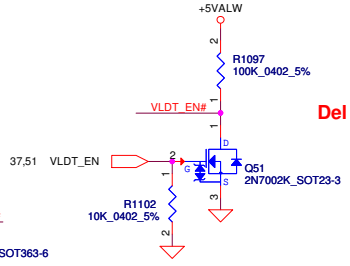


+1.5V TO +1.5VS (1.5A)

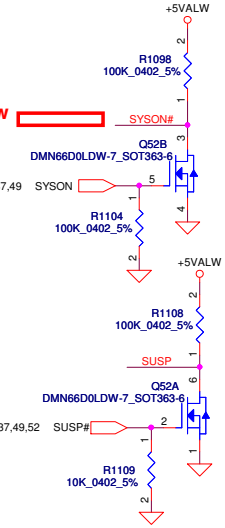
Del +1.5V to +1.5VS

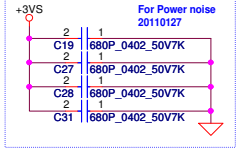
+1.1VALW TO +1.1VS (1.1A)





Del arrow



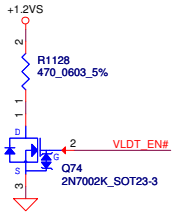


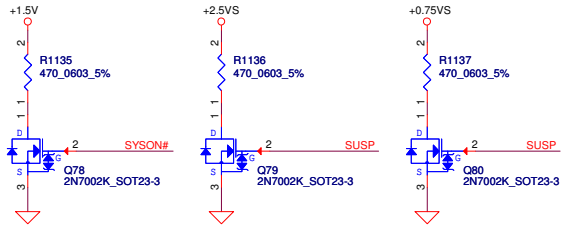
VGA Power

+1.5V to +1.5VSG (1.5A)

Del +1.5VSG and reserved on GPU

Del +3VSG and reserved on GPU





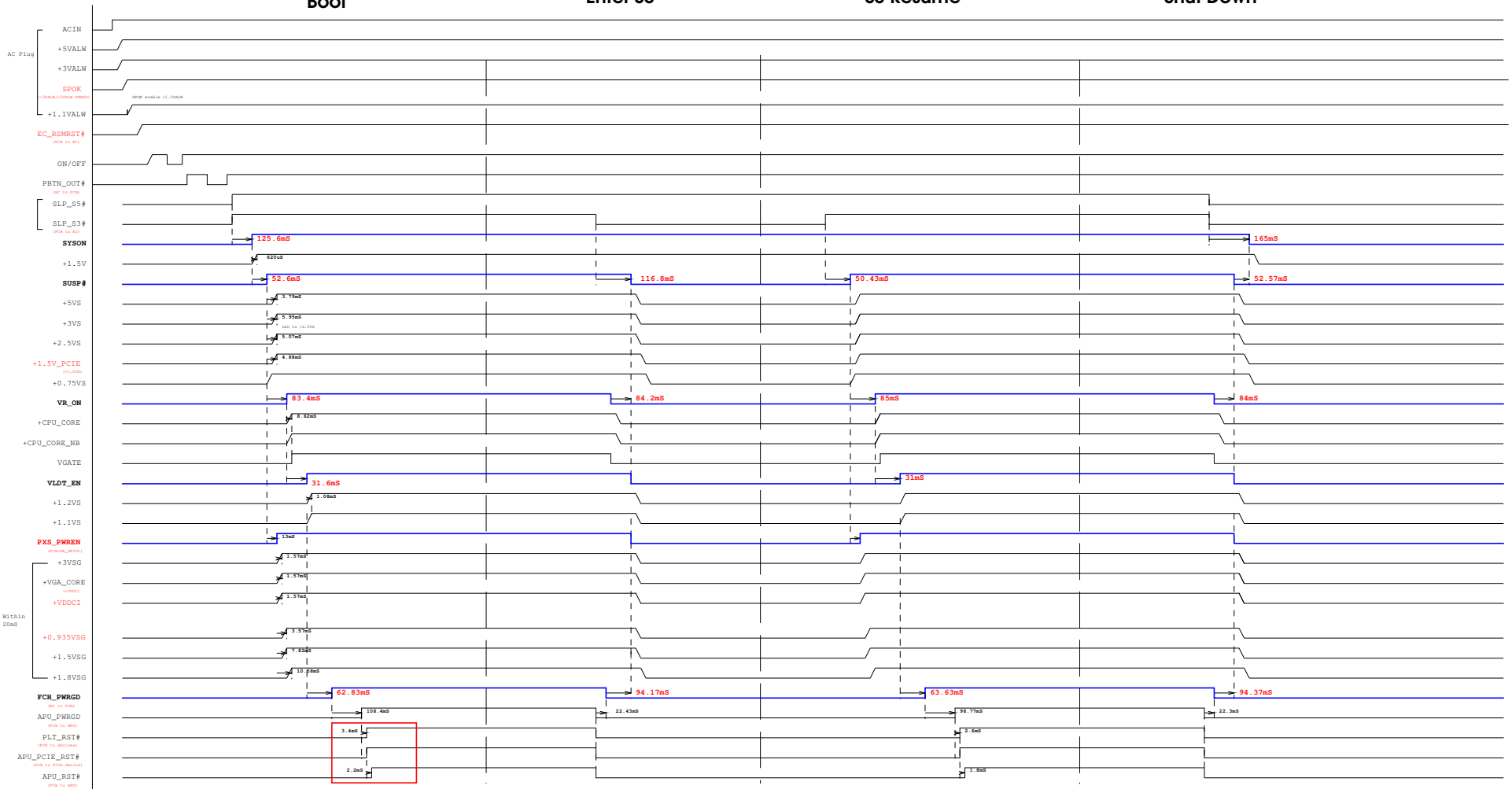
Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

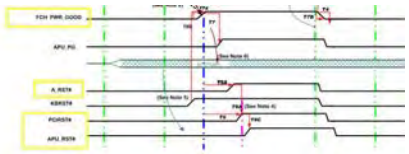
Compal Electronics, Inc.

Title: DC Interface

Size: B | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 42 of 56





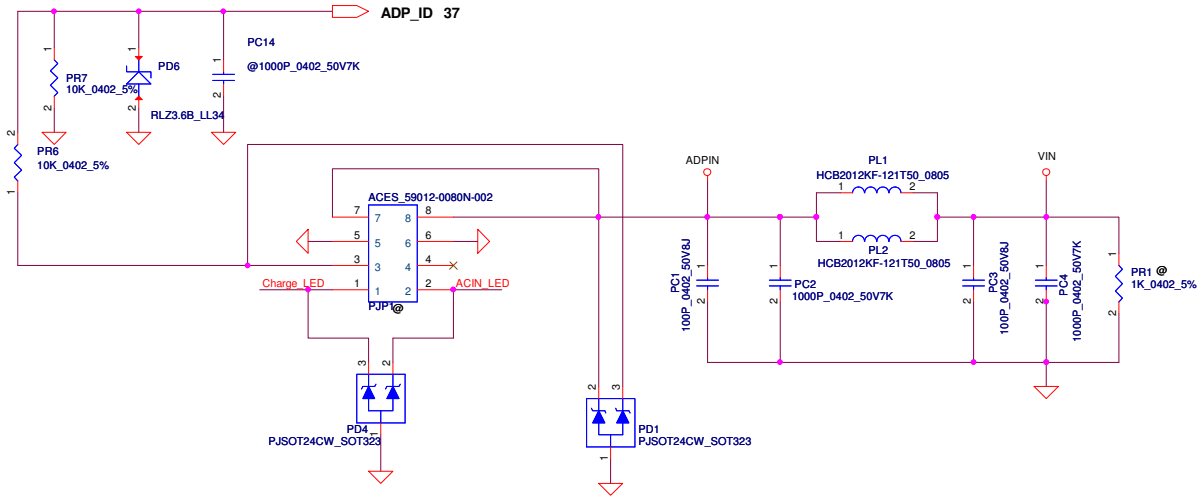
Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

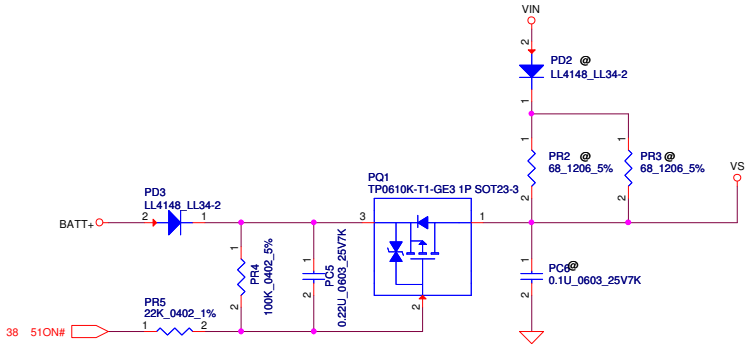
Title: DC Interface

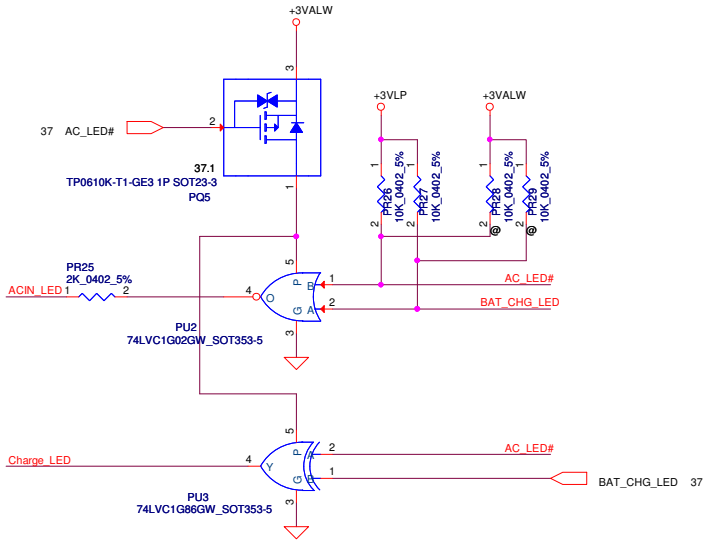
Size: Custom | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 43 of 56



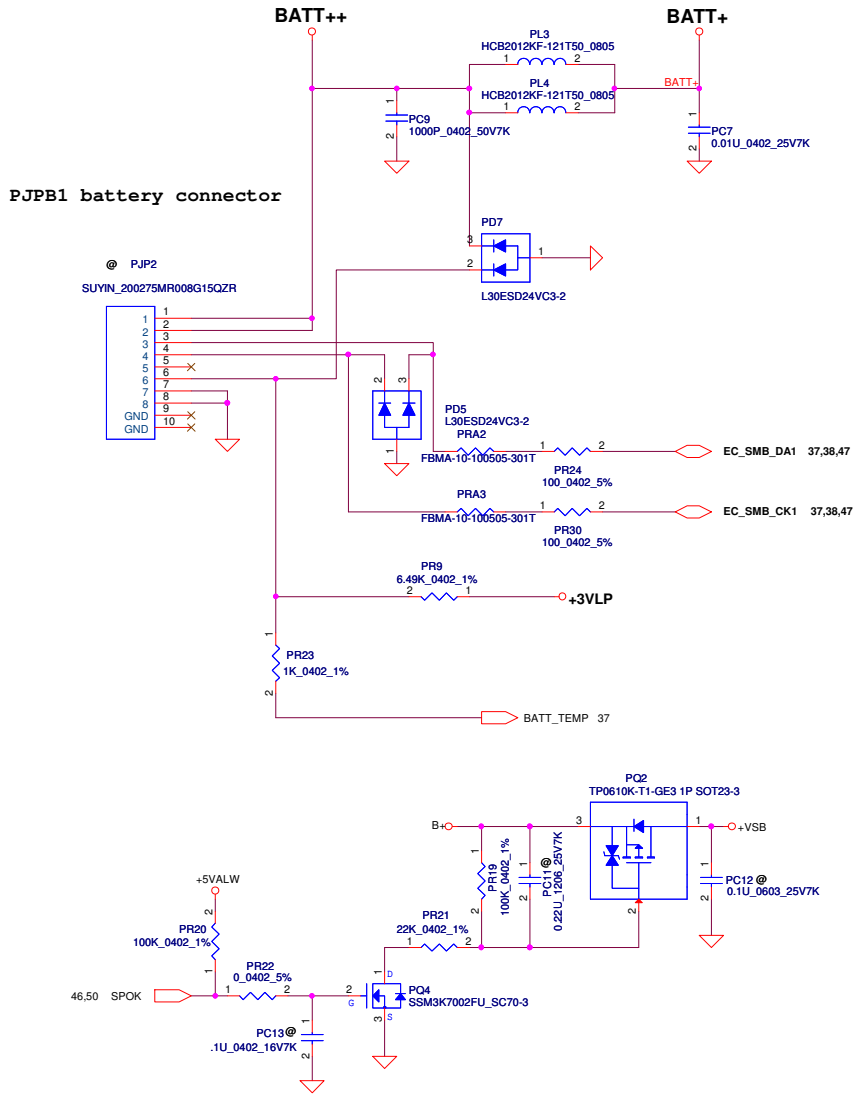
ESD diode : SCA00001G00





Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title: PWR- DCIN / Vin Detector			
Size: Custom	Document Number: QCL51 LA-8712P		Rev: 0.1
Date: Monday, November 28, 2011	Sheet 44 of 56		

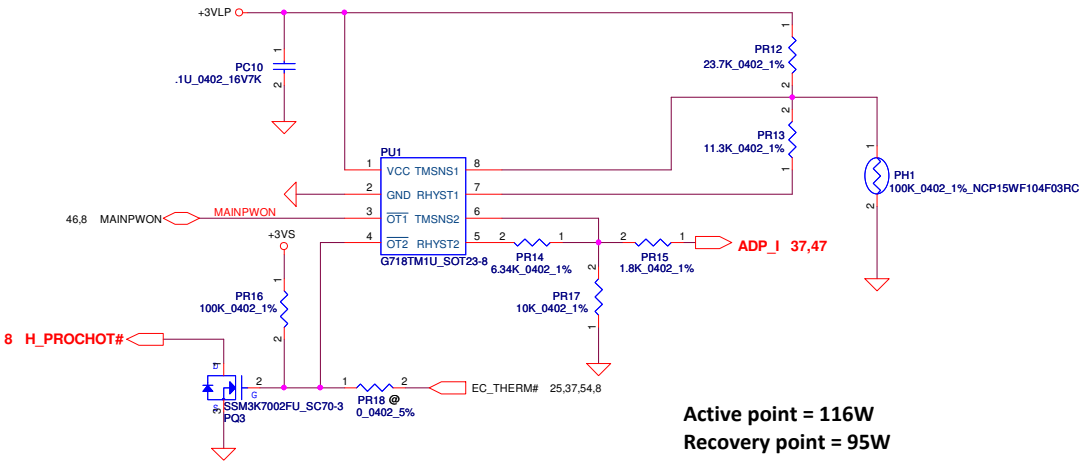


For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 56 +-3 degree C

Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)

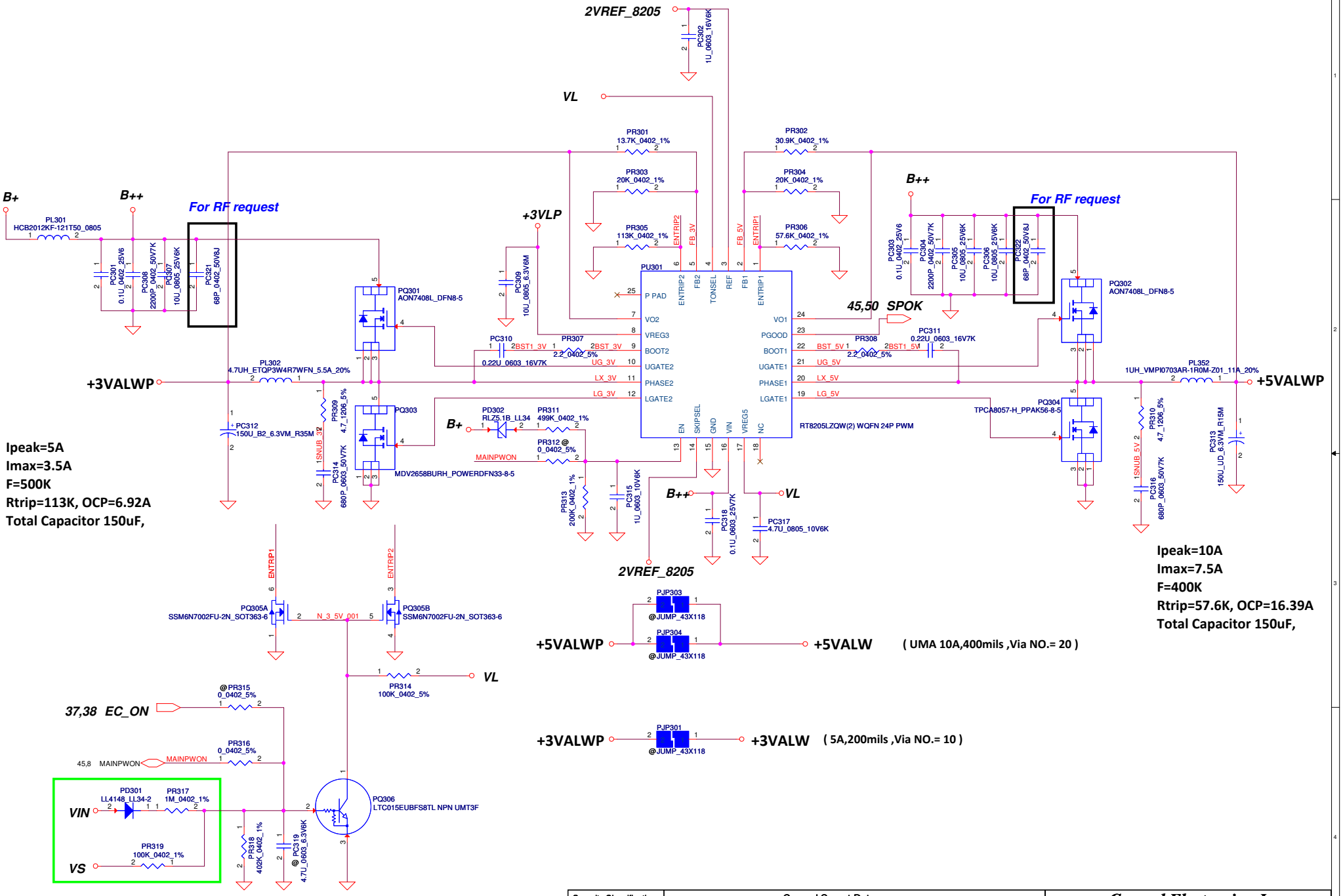
Rtmh at 90C = 7.8K, Rtml at 56C = 26.1K
Rset = 3 * 7.8K = 23.4K ==> 23.7K
Rhyst = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K ==> 11.3K



Active point = 116W
Recovery point = 95W

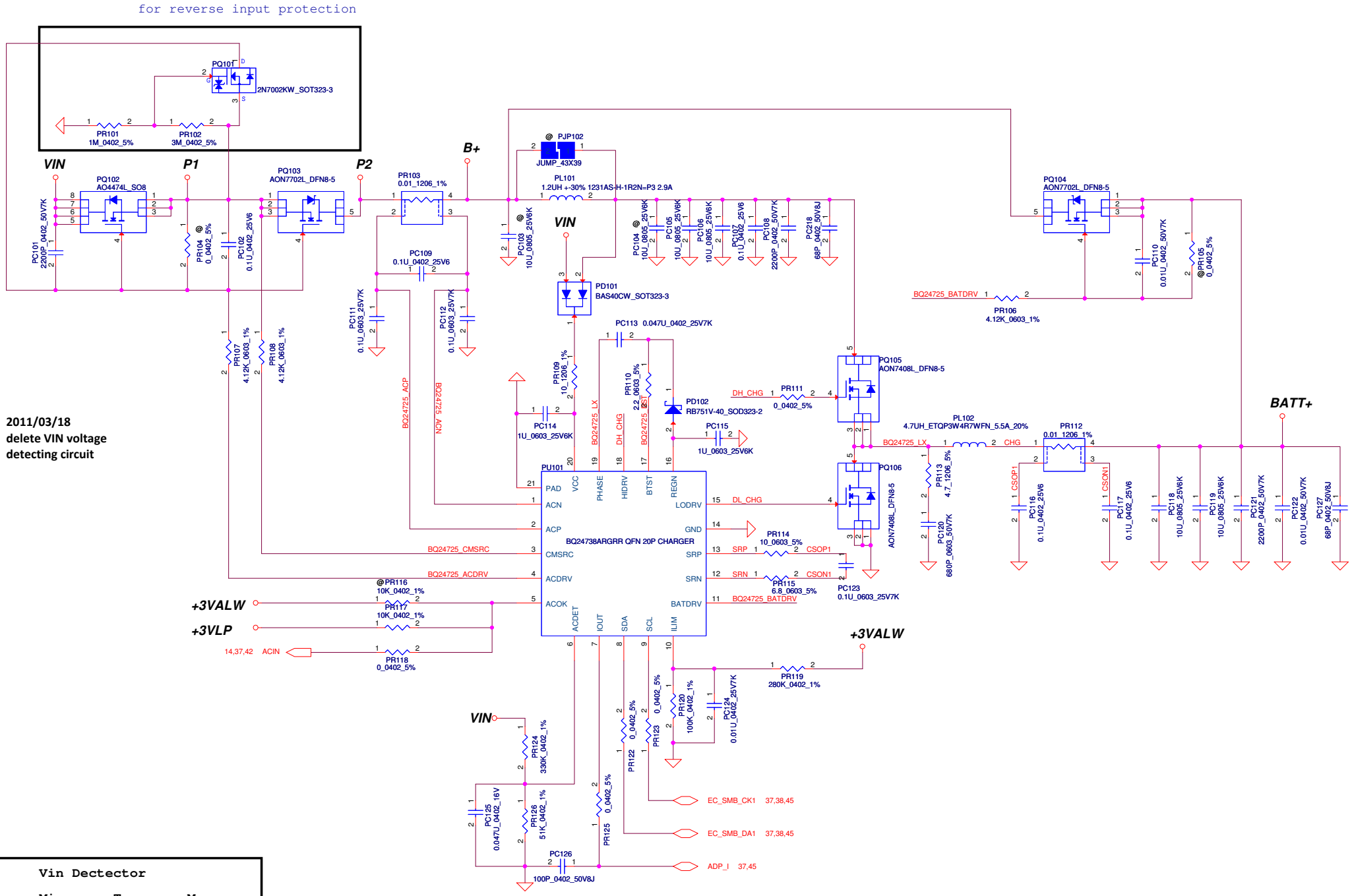
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title	PWR- BATTERY CONN		
Size: Custom	Document Number: QCL51 LA-8712P		Rev: 0.1
Date: Monday, November 28, 2011	Sheet 45 of 56		



Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title: PWR- 3VALWP/5VALWP			
Size: Custom	Document Number: QCL51 LA-8712P		Rev: 0.1
Date: Monday, November 28, 2011	Sheet 46 of 56		


for reverse input protection
PQ101
2N7002KW_SOT323-3
PR101
1M_0402_5%
PR102
3M_0402_5%
VIN
P1
P2
B+
PQ102
AO4474L_SO8
PQ103
AON7702L_DFN8-5
PR103
0.01_1206_1%
@ PJP102
JUMP_43X39
PL101
1.2UH +-30% 1231AS-H-1R2N=P3 2.9A
PC101
2200P_0402_50V7K
PR104 @
0_0402_5%
PC102
0.1U_0402_25V6
PC103 @
10U_0805_25V6K
PC104 @
10U_0805_25V6K
PC105
10U_0805_25V6K
PC106
10U_0805_25V6K
PC107
0.1U_0402_25V6
PC108
2200P_0402_50V7K
PC218
68P_0402_50V8J
PC109
0.1U_0402_25V6
PD101
BAS40CW_SOT323-3
PC111
0.1U_0603_25V7K
PC112
0.1U_0603_25V7K
PR107
4.12K_0603_1%
PR108
4.12K_0603_1%
PC113 0.047U_0402_25V7K
PR109
10_1206_1%
PR110
2.2_0603_5%
PD102
RB751V-40_SOD323-2
PC114
1U_0603_25V6K
PC115
1U_0603_25V6K
PU101
BQ24738ARGRR QFN 20P CHARGER
PAD
VCC
PHASE
HIDRV
BTST
REGN
ACN
LODRV
ACP
GND
CMSRC
SRP
ACDRV
SRN
ACOK
BATDRV
ACDET
IOUT
SDA
SCL
ILIM
BQ24725_ACP
BQ24725_ACN
BQ24725_LX
DH_CHG
BQ24725_BST
BQ24725_CMSRC
BQ24725_ACDRV
BQ24725_BATDRV
DL_CHG
SRP
SRN
CSOP1
CSON1
PQ104
AON7702L_DFN8-5
BQ24725_BATDRV
PR106
4.12K_0603_1%
PQ105
AON7408L_DFN8-5
DH_CHG
PR111
0_0402_5%
PQ106
AON7408L_DFN8-5
PL102
4.7UH_ETQP3W4R7WFN_5.5A_20%
BQ24725_LX
CHG
PR112
0.01_1206_1%
BATT+
PR113
4.7_1206_5%
PC120
680P_0603_50V7K
PC116
0.1U_0402_25V6
PC117
0.1U_0402_25V6
PC118
10U_0805_25V6K
PC119
10U_0805_25V6K
PC121
2200P_0402_50V7K
PC122
0.01U_0402_50V7K
PC127
68P_0402_50V8J
PR114
10_0603_5%
PR115
6.8_0603_5%
PC123
0.1U_0603_25V7K
@PR116
10K_0402_1%
PR117
10K_0402_1%
+3VALW
+3VLP
14,37,42 ACIN
PR118
0_0402_5%
PR119
280K_0402_1%
PR120
100K_0402_1%
PC124
0.01U_0402_25V7K
PR122
0_0402_5%
PR123
0_0402_5%
PR124
330K_0402_1%
PC125
0.047U_0402_16V
PR126
51K_0402_1%
PR125
0_0402_5%
PC126
100P_0402_50V8J
EC_SMB_CK1 37,38,45
EC_SMB_DA1 37,38,45
ADP_I 37,45
2011/03/18
delete VIN voltage
detecting circuit
Vin Dectector
Min. Typ Max.
H-->L 17.33V
L-->H 16.98V
ILIM and external DPM
4.36A
Security Classification
Compal Secret Data
Issued Date
2011/10/03
Deciphered Date
2014/12/31
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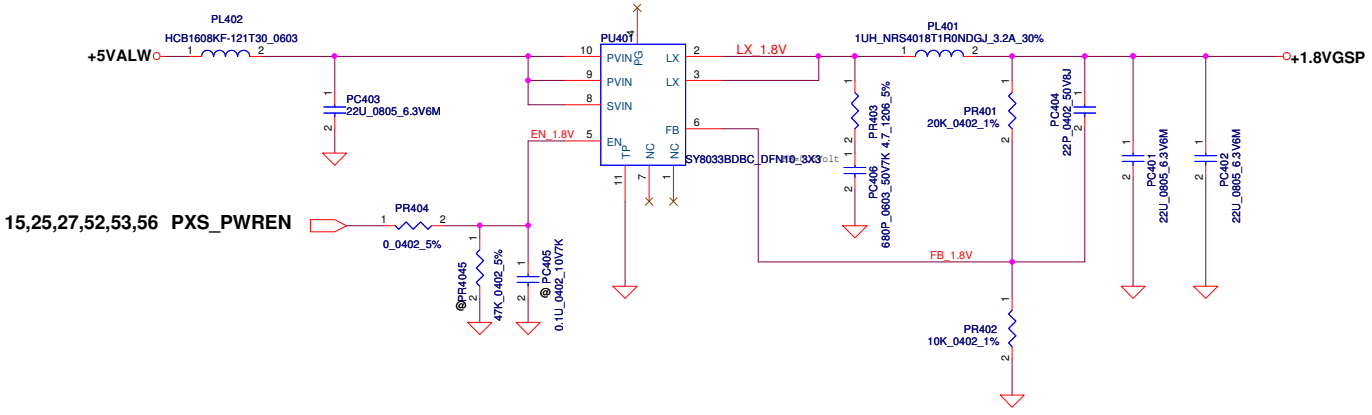
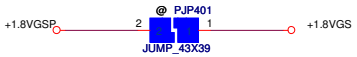
Compal Electronics, Inc.
Title
PWR- CHARGER
Size
Document Number
LA-8712P
Rev
0.1
Date: Monday, November 28, 2011
Sheet 47 of 56

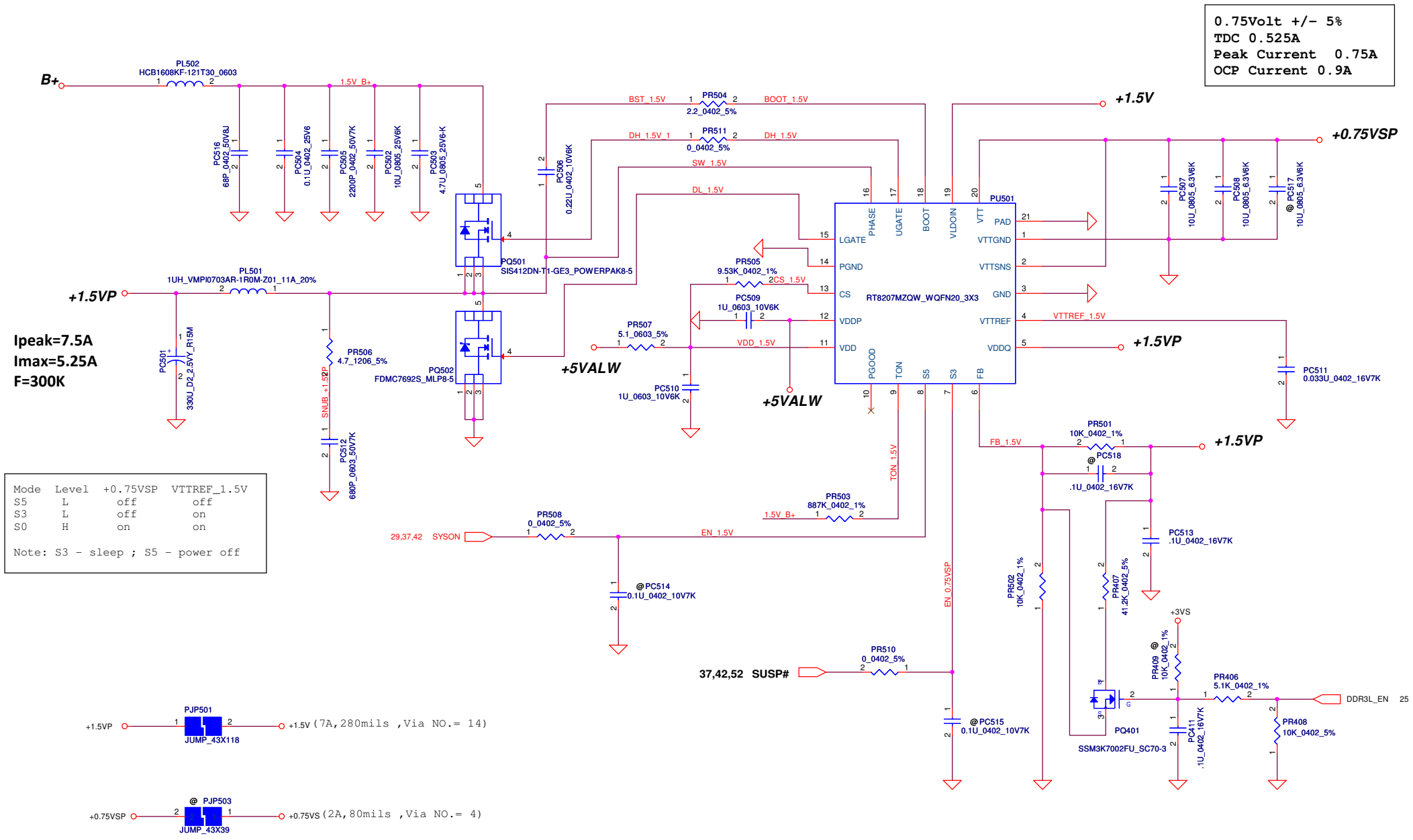
1.8VGSP
Peak Current 1.4A
OCP current 3A





(4A,240mils ,Via NO.= 8)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/29	Deciphered Date	Title: +1.8VP
Size: B	Document Number: LA-8712P		Rev: 0.1
Date: Monday, November 28, 2011	Sheet 48 of 56		



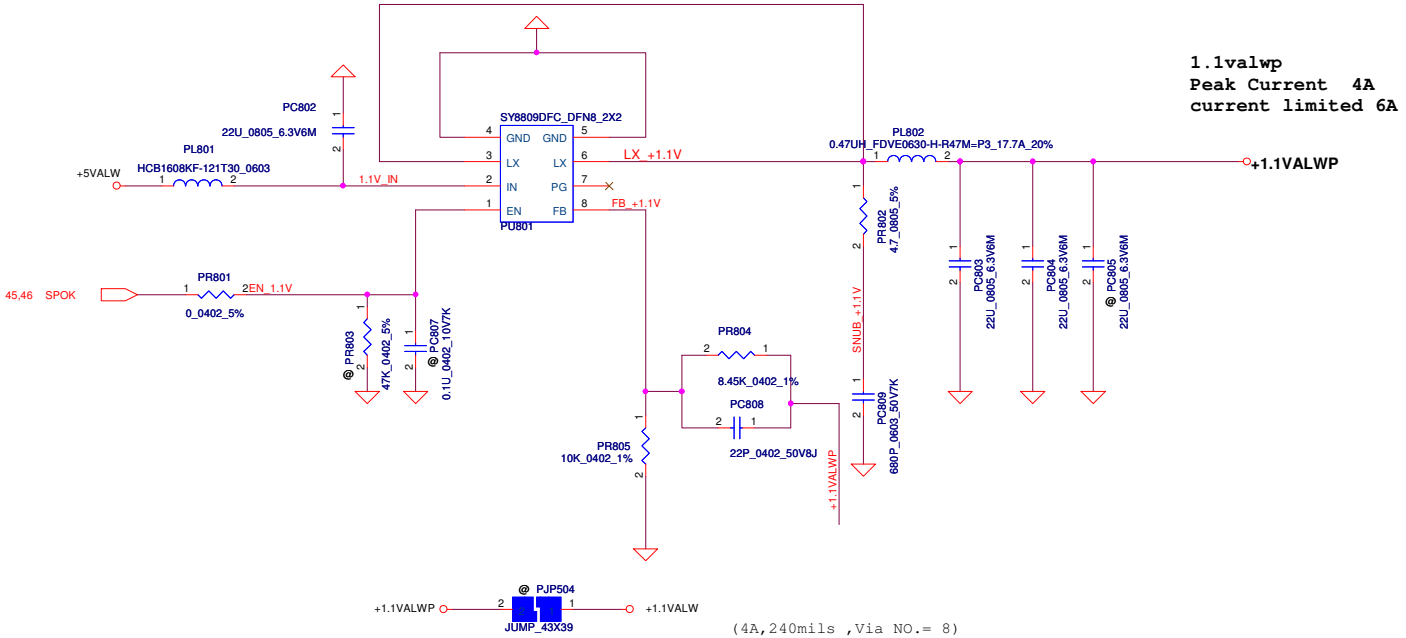
Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: PWR-1.5VP / +0.75VSP

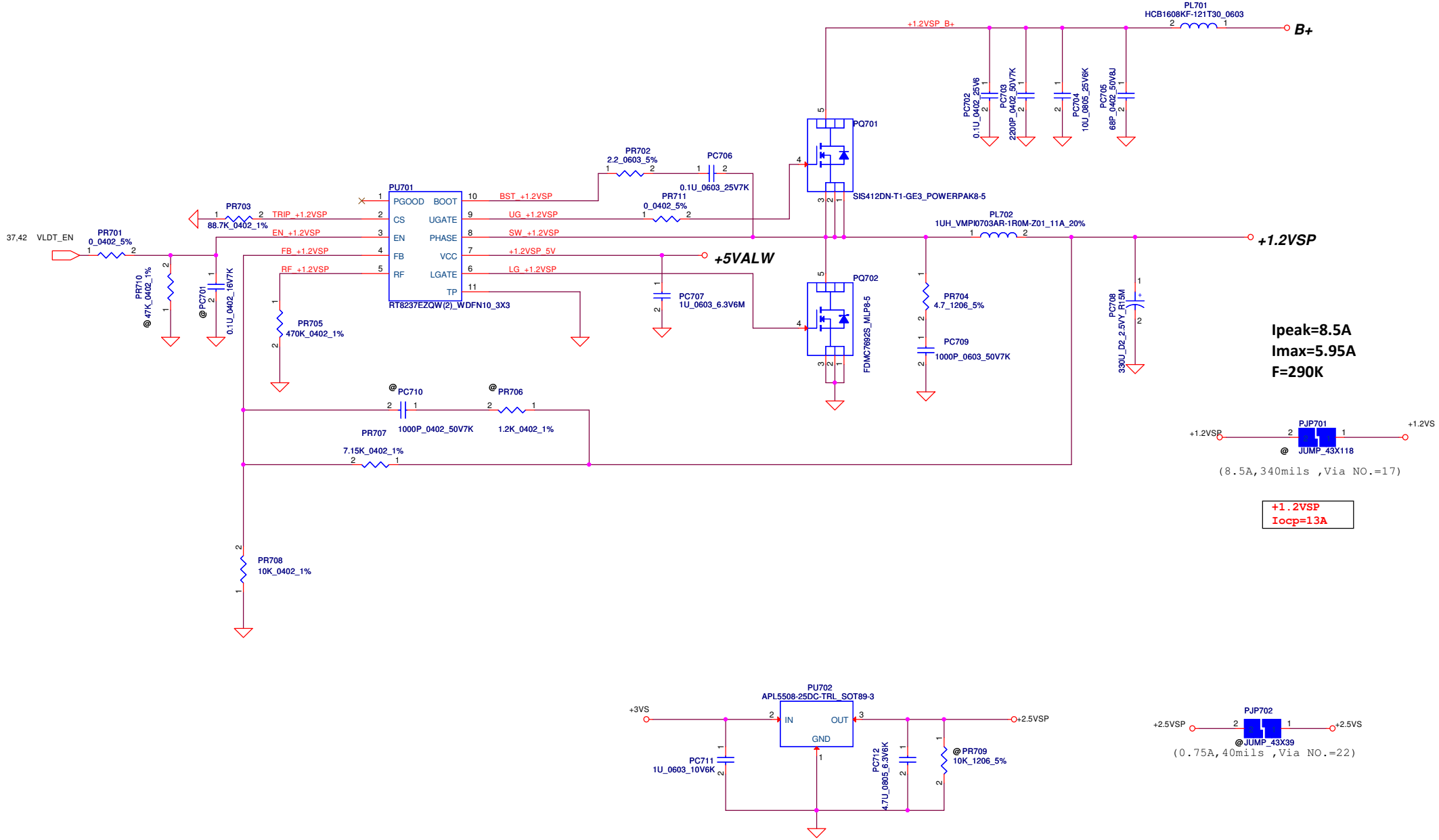
Size	Document Number	Rev
Custom	LA-8712P	0.1

Date: Monday, November 28, 2011 Sheet 49 of 56



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/29	Deciphered Date	Title: +1.1VALWP

Size: B	Document Number: LA-8712P		Rev: 0.1
Date: Monday, November 28, 2011	Sheet 50 of 56		



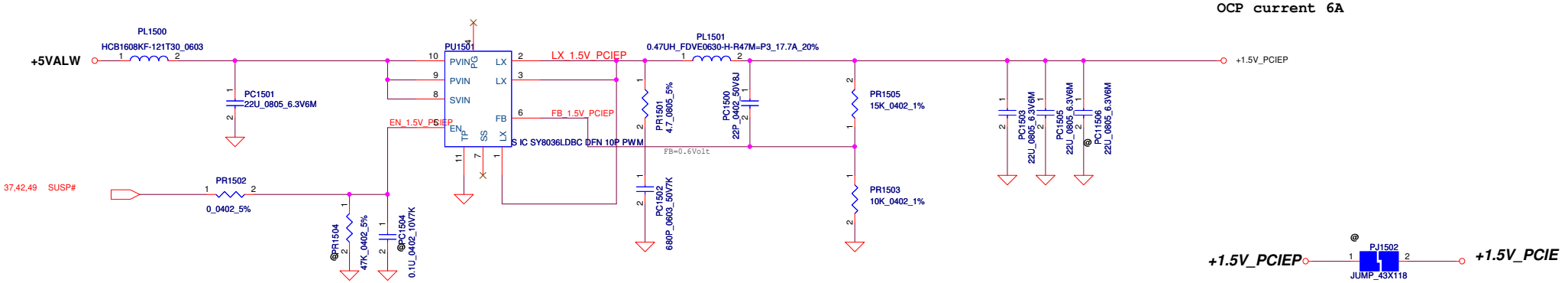
Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	

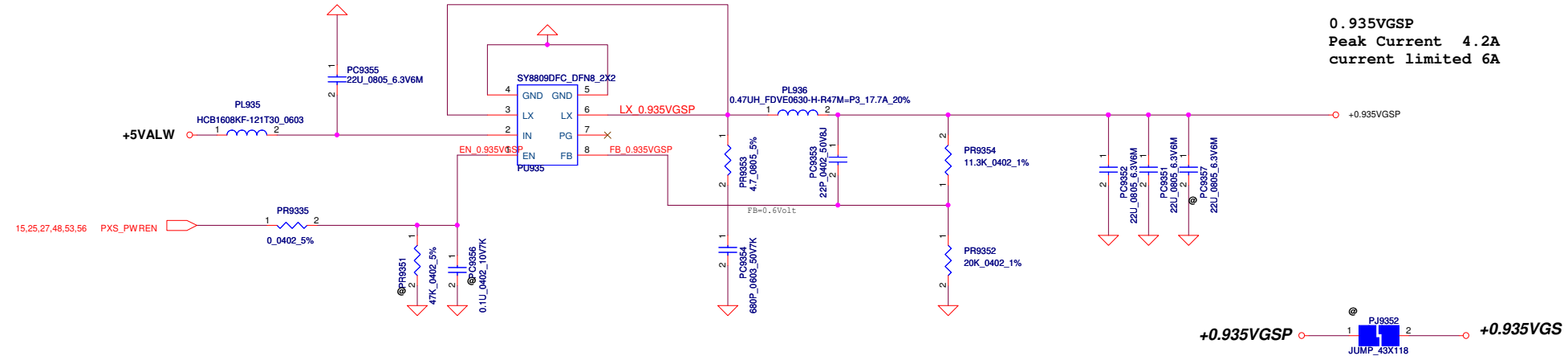
Compal Electronics, Inc.

Title: +1.2VSP/+2.5VSP

Size	Document Number	Rev
	LA-8712P	0.1

Date: Monday, November 28, 2011 | Sheet 51 of 56





Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Compal Electronics, Inc.

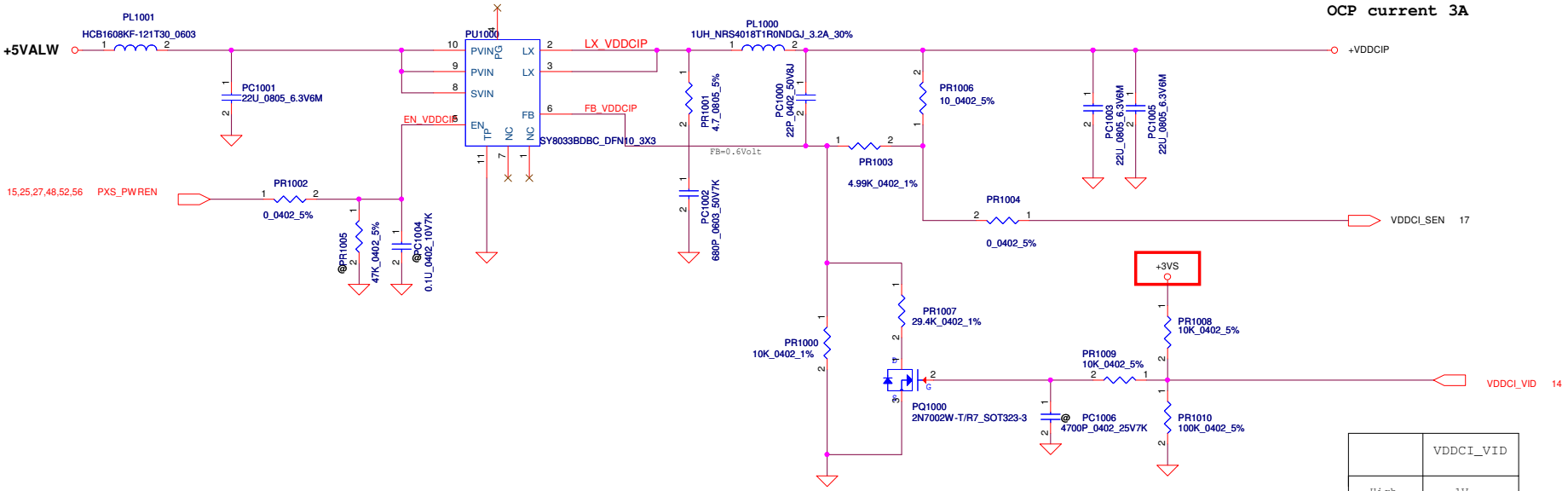
Title: +1.5VPCIE/0.935V

Size | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 52 of 56

+VDDCI
TDC 2.2A

OCP current 3A



	VDDCI_VID
High	1V
Low	0.9V

+VDDCIP @ PJ1001 +VDDCI

JUMP_43X39

(2.2A,100mils ,Via NO.= 5)

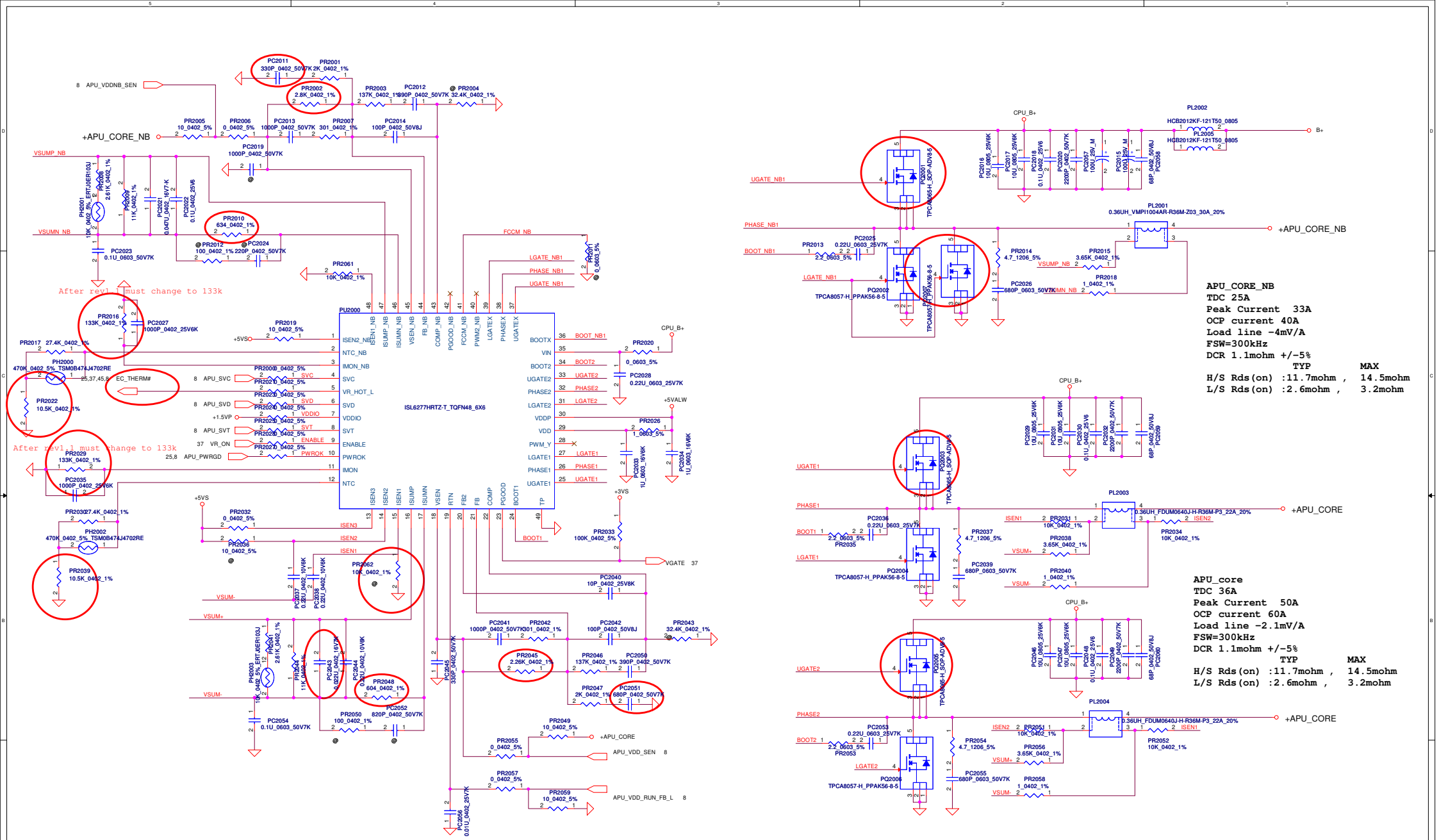
Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Compal Electronics, Inc.

Title: +VDDCIP

Size | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 53 of 56



Security Classification	Compal Secret Data		
Issued Date	2011/04/18	Deciphered Date	2015/07/08

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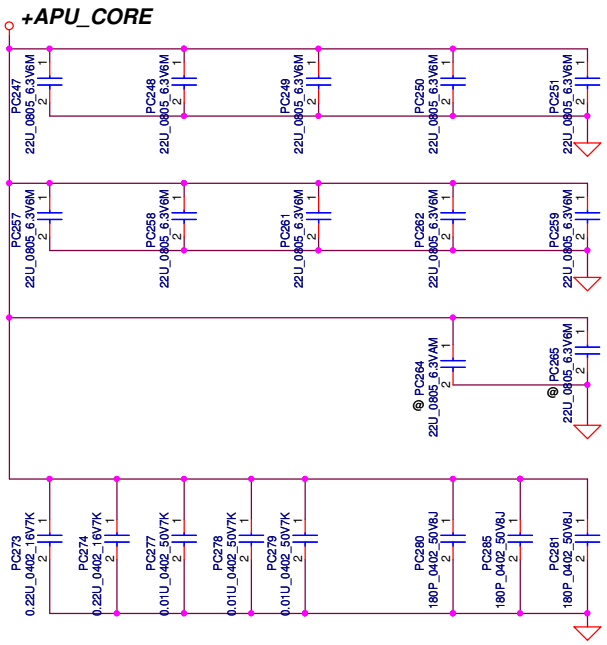
Compal Electronics, Inc.

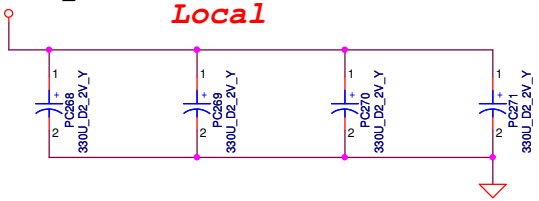
Title: **CPU_COREP**

Size	Document Number	Rev
Custom		0.1

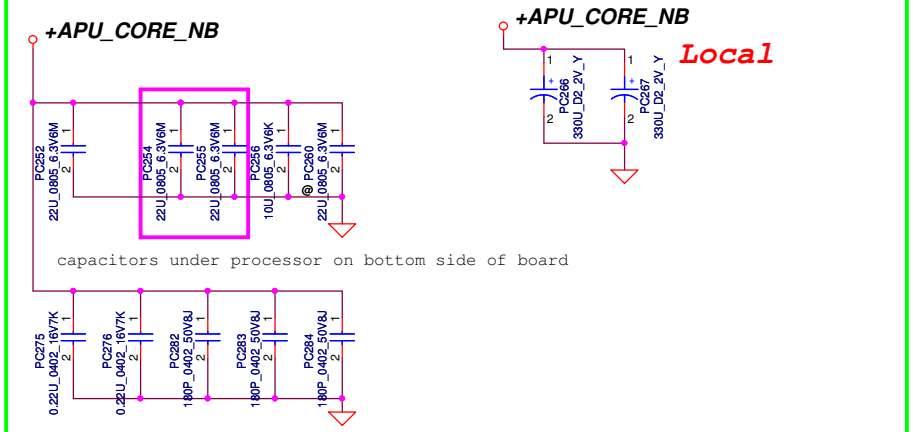
Date: Monday, November 28, 2011 Sheet 54 of 56

+APU_CORE

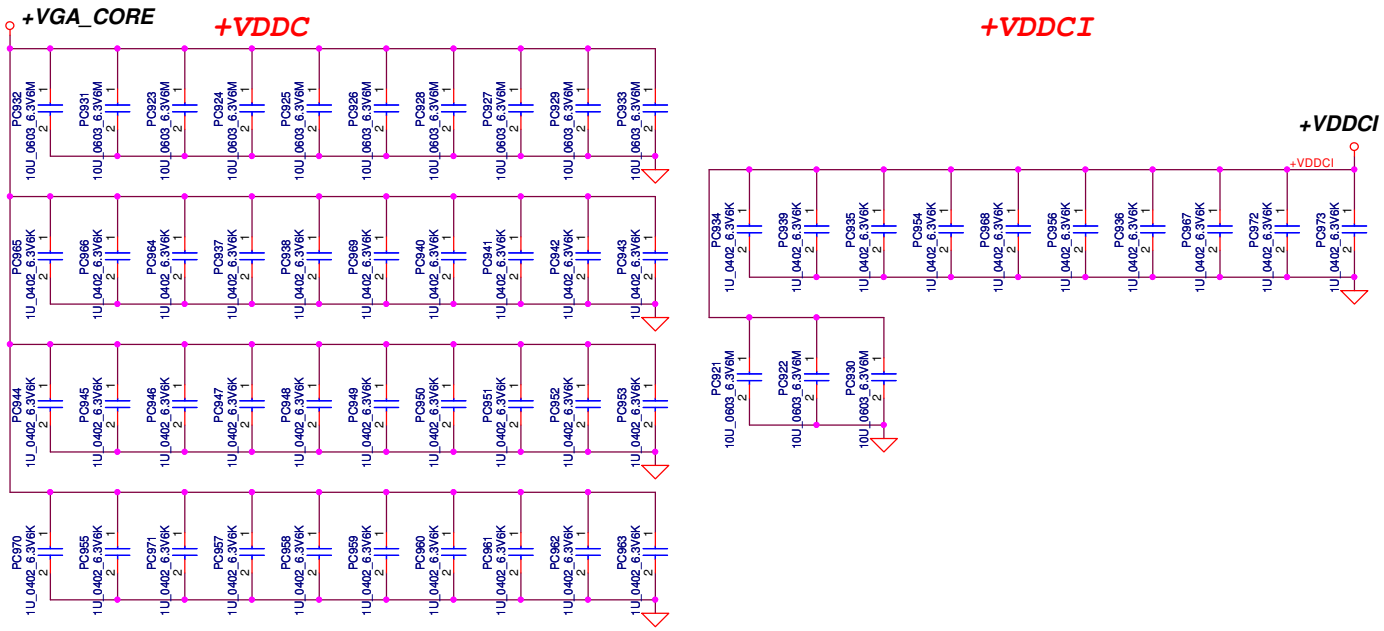




+APU_CORE_NB

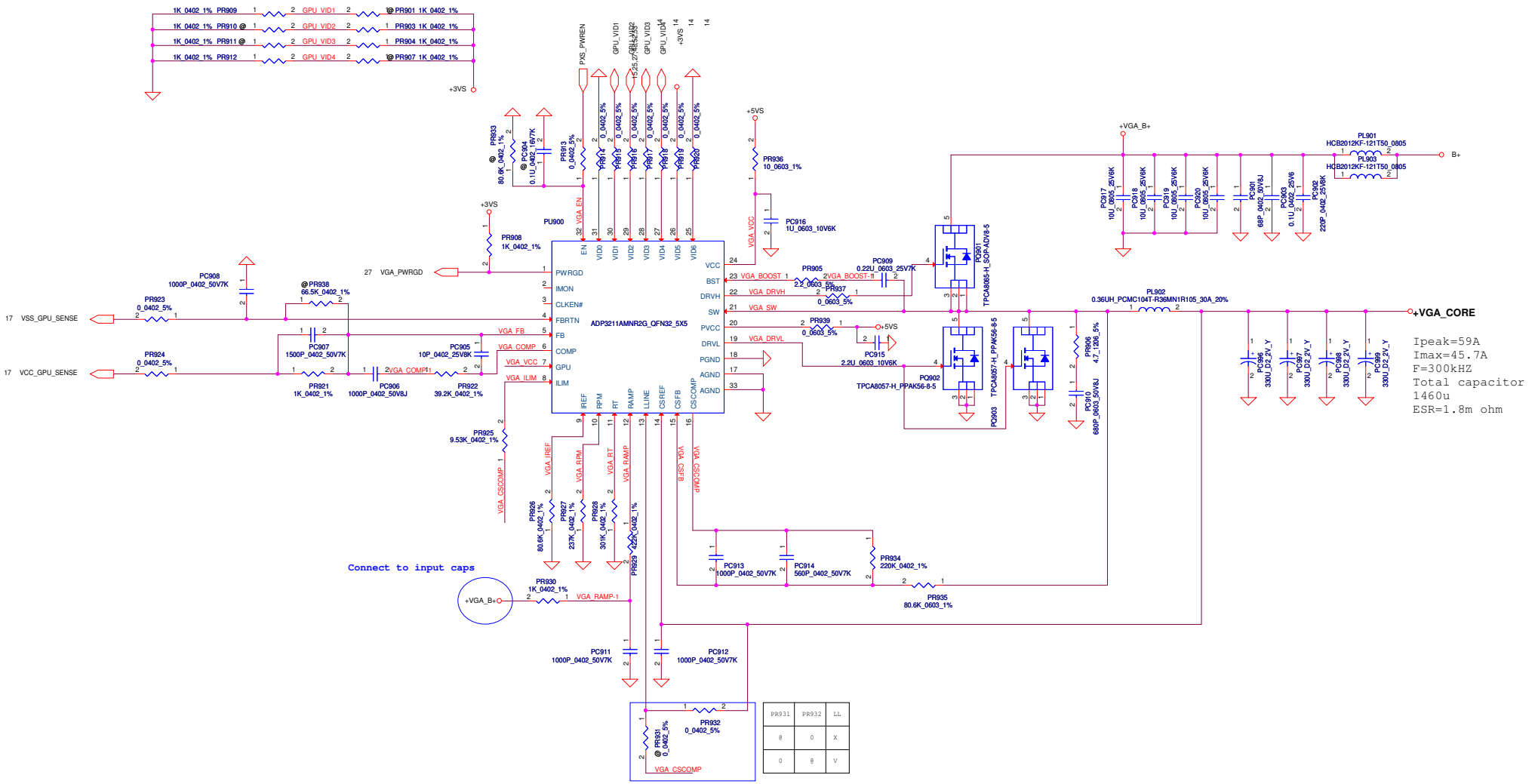


+VGA_CORE



Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	

Compal Electronics, Inc.			
Title: PROCESSOR DECOUPLING			
Size: A3	Document Number: LA-8712P		Rev: 0.1
Date: Monday, November 28, 2011		Sheet 55 of 56	



Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.

Title: **+VGA_COREP**

Size	Document Number	Rev
	LA-8712P	0.1

Date: Monday, November 28, 2011 | Sheet 56 of 56