R62 INTEL CHIEF RIVER SYSTEM DIAGRAM

01

+3V/+5V S5 PG.35
+1.05V PG.36
CPU Core PG.40~41
DDR3 PG.37
Charge PG.34
Dis-Charge PG.39
+VGACORE PG.42
+VCCSA PG.38
+1.0V/+1.8/ +3 VGA PG.43

SODIMM1 Max. 4GB PG.12 — DDR3 Channel A
SODIMM2 Max. 4GB PG.13 — DDR3 Channel B

INTEL IVY
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.2~5

PCI-E x8 — AMD Mars / SUN XT 29mm X 29mm TDP 35W / 25W PG.14~20
DDR3 900MHz — VRAM 128Mx16x8,128bit PG.21~22
EDP

FDI DMI

HDD PG.32 — SATA0
ODD PG.32 — SATA1

INTEL PCH
Panther Point
Power : 3.5 Watt
Package : FCBG989
Size : 25 x 25 (mm)
PG.6~11

LVDS PG.24 — LVDS
DP Port B PG.25 — HDMI
CRT PG.23 — CRT

PCI-E x 1 — LANE2 / LANE1
LAN RTL8166 10/100 PG.29
WLAN BT COMBO PG.33 — USB 2.0 PORT10

USB 3.0 — USB3.0 Ports X2 PG.28 — Webcam PG.24
USB 2.0 — PORT1,2 / PORT4 / PORT0,1
USB2.0 Ports PG.28

PCI-E x 1 — LANE3
Accelerometer PG.33 — SMBUS
Card Reader RTS5239 PG.26

KBC EnE KB3940QF A1 PG.30 — LPC
KB PG.31
TP PG.31
ROM PG.30
FAN PG.31

AUDIO CODEC ALC 3227 PG.27
Speaker PG.27
HP/MIC PG.28
Analog MIC PG.28

Stackup
TOP
GND
IN1
IN2
VCC
BOT

NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Monday, October 22, 2012 Sheet 1 of 43

Ivy Bridge Processor (DMI,PEG,FDI)

Ivy Bridge Processor (CLK,MISC,JTAG)

02

U22A

DMI

Intel(R) FDI

PCI EXPRESS* - GRAPHICS

eDP

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

Ivy Bridge_rPGA_2DPC_Rev0p61

U22B

MISC

CLOCKS

DDR3 MISC

THERMAL

PWR MANAGEMENT

JTAG & BPM

SNB_IVB# N.A at SNB EDS #27637 0.7v1

close to VR side

CPU RESET#

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

CPU XDP

Ivy Bridge_rPGA_2DPC_Rev0p61

SM_DRAMPWROK Processor Input.

DDR3 DRAM RESET

PEG x8 disable (UMA only remove)

0.22uF AC coupling Caps for PCIE GEN1/2/3

0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

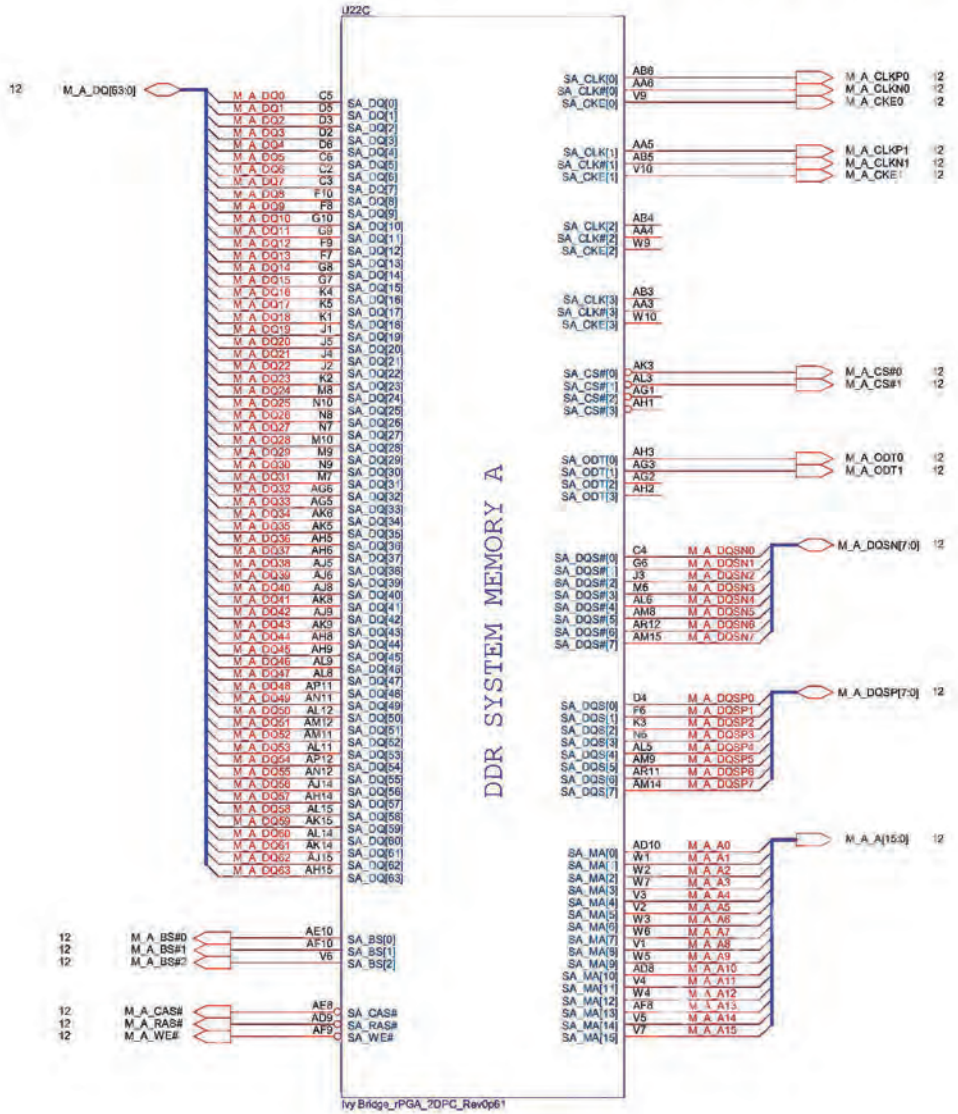
PROJECT : R62
Quanta Computer Inc.

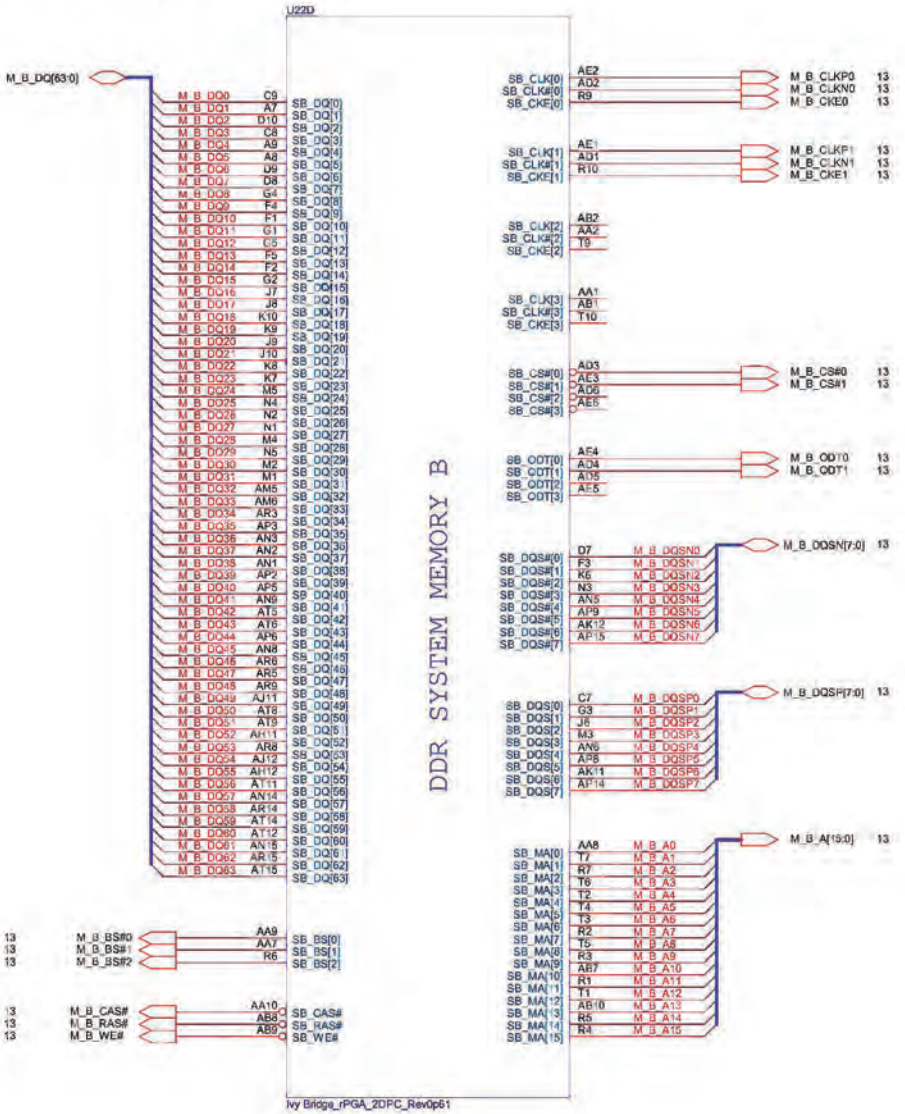
NB5

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	1A

Date: Monday, October 22, 2012 Sheet 2 of 43

Ivy Bridge Processor (DDR3)





NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	1A

Date: Monday, October 22, 2012 Sheet 3 of 43

Ivy Bridge Processor (POWER)

04

POWER

U22F

SNB: 55A
IVY: 55A

+VCC_CORE

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

SNB: 8.5A
IVY: 8.5A

+1.05V_VTT

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

VIDALERT# H_CPU_SVIDALRT#
VIDSCLK H_CPU_SVIDCLK
VIDSOUT H_CPU_SVIDDAT

VCC_SENSE
VSS_SENSE
VCCIO_SENSE
VSS_SENSE_VCCIO

Trace Route to Power IC area.

Ivy Bridge_rPGA_2DPC_Rev0p61

+1.5V	10,12,27,33
+1.8V	7,10,37,43
+VCCSA	38
+1.5VSUS	2,12,13,37,43
+1.5V_CPU	2
+VCC_GFX	41
+1.05V_VTT	2,6,7,8,9,10,25,30,36,40
+VCC_CORE	41

POWER

U22G

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

+VCC_GFX SNB: 21.5A

+1.8V SNB: 1.5A

330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

GRAPHICS

1.8V RAIL

SENSE LINES

VAXG_SENSE
VSSAXG_SENSE

VREF

SM_VREF
SA_DIMM_VREFDQ
SB_DIMM_VREFDQ

DDR3 -1.5V RAILS

SNB: 5A

330uF x1, 10uF_8 x6 Socket BOT edge.

SA RAIL

SNB: 6A

330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.

MISC

VCCSA_SENSE
VCCSA_VID[0]
VCCSA_VID[1]
VCCIO_SEL

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

+VDDR_REF_CPU

DDR_VTTREF 12,13,37

MAIND 39

SMDDR_VREF_DQ2M3
SMDDR_VREF_DQ1M3

+1.5V_CPU

+VCCSA

VCCUSA_SENSE 38
VCCSA_SEL0 38
VCCSA_SEL 38
H_VTTVID1 36

Ivy Bridge_rPGA_2DPC_Rev0p61

+1.5V_CPU R752 *0_8/S +1.5V
40mile routing

Layout note: need routing together and ALERT need between CLK and DATA.

SVID CLK

H_CPU_SVIDCLK → VR_SVID_CLK 40

SVID DATA

+1.05V_VTT
Place PU resistor close to CPU
R754 130/F_4
H_CPU_SVIDDAT → VR_SVID_DATA 40

Place PU resistor close to CPU

SVID ALERT

C352 0.1U/10V_4
+1.05V_VTT R756 75/F_4
H_CPU_SVIDALRT# R757 43_4 → VR_SVID_ALERT# 40

+1.5VSUS
+1.5V_CPU
Q10 QM3002N3
R753 220_8
MAIND
C54 *470P/50V_4
Q22 2N7002
MAIN_ONG 2,39
Placement close to CPU.

CPU VDDQ

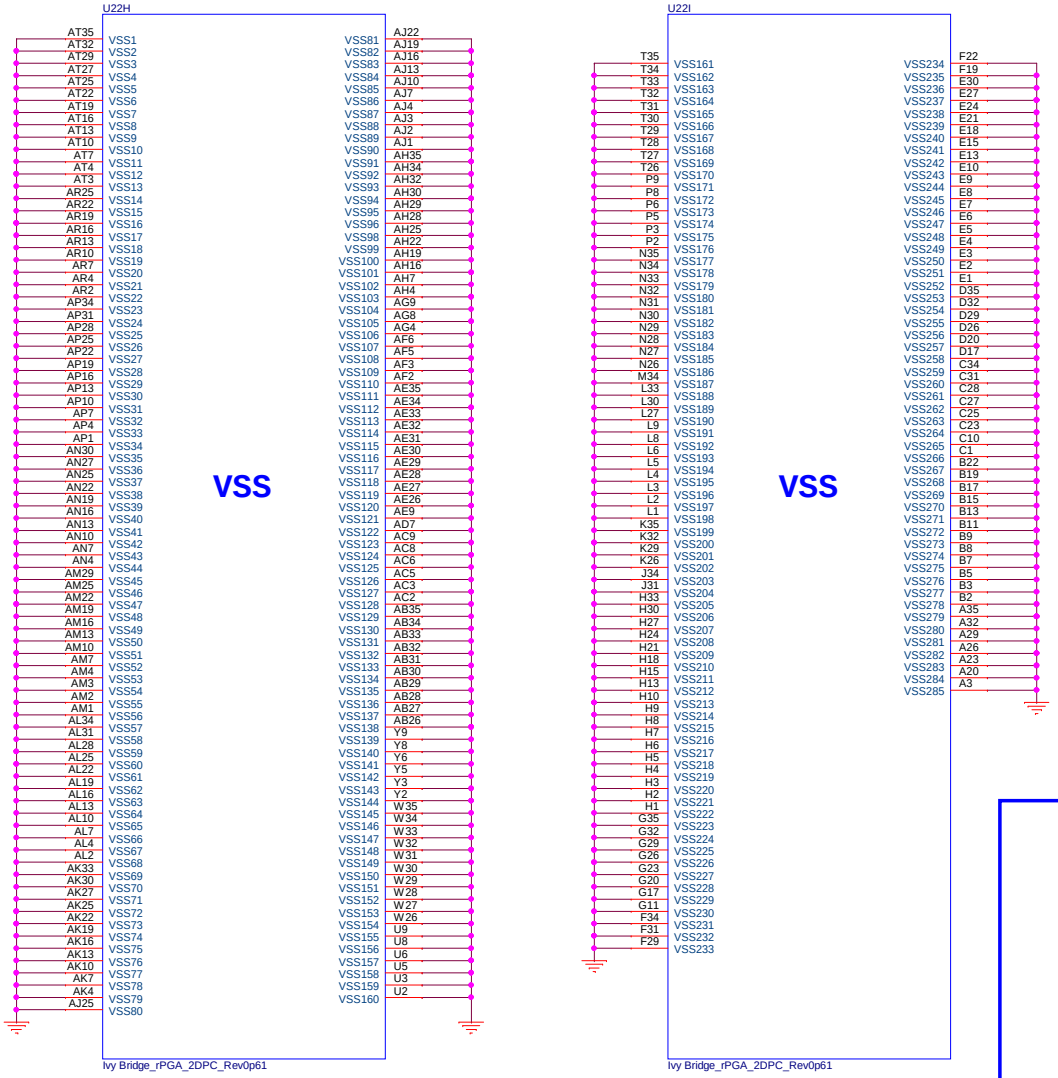
NB5

PROJECT : R62
Quanta Computer Inc.

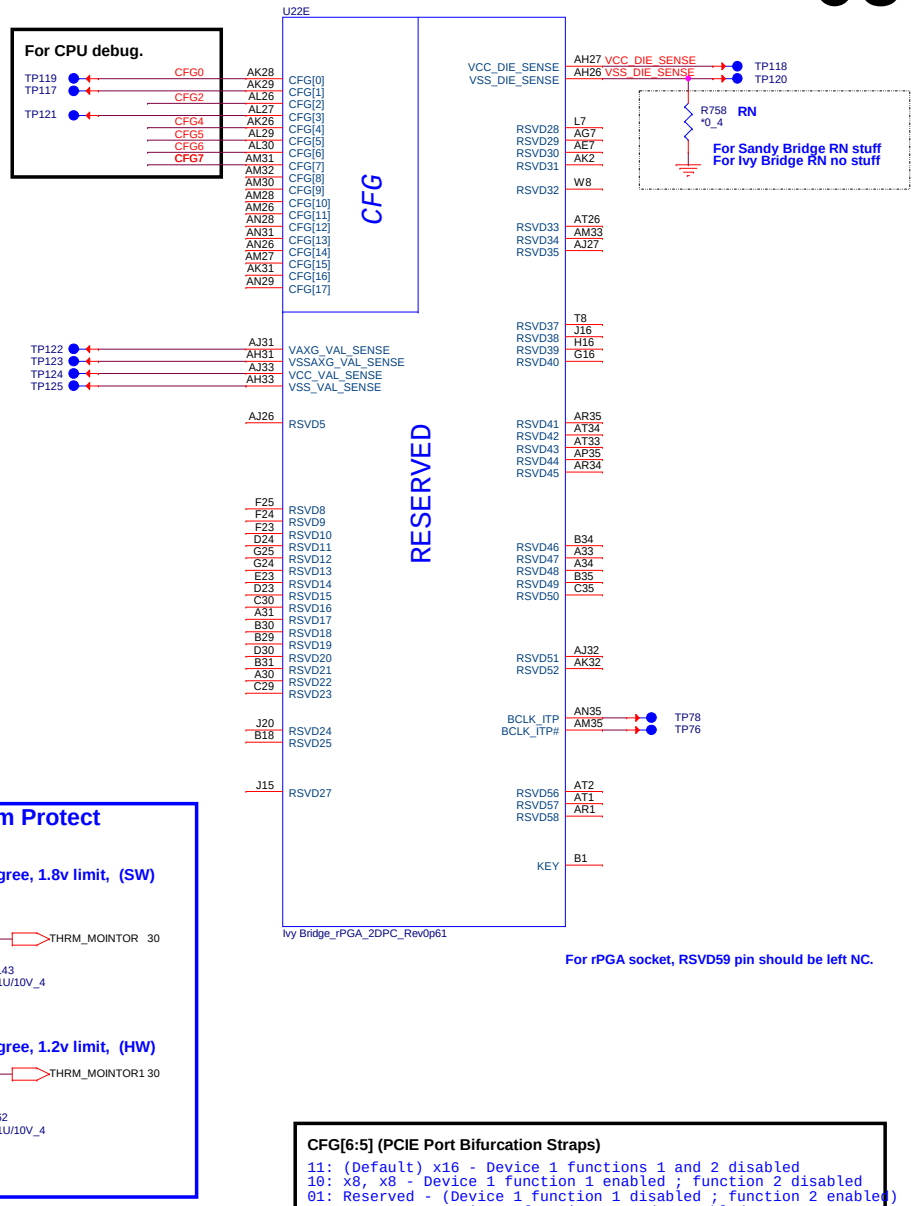
Size	Document Number	Rev
Custom	SNB 3/4 (POWER)	1A

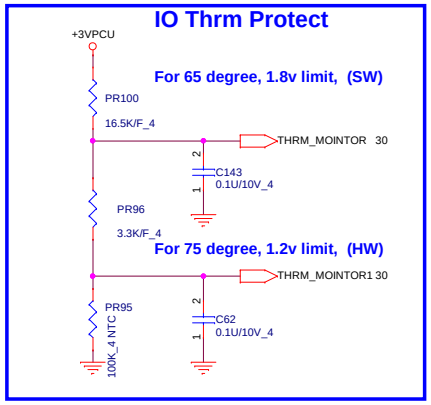
Date: Monday, October 22, 2012 Sheet 4 of 43

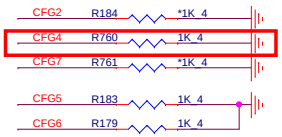
Ivy Bridge Processor (GND)



Ivy Bridge Processor (RESERVED, CFG)







Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : R62
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	SNB 4/4 (GND)	1A

Date: Monday, October 22, 2012 Sheet 5 of 43

05

Cougar Point/Panther Point (DMI,FDI,PM)

Cougar Point/Panther Point (LVDS,DDI)

06

U32C

U32D

DMI

FDI

System Power Management

LVDS

Digital Display Interface

INT. HDMI

CRT

CPT_PPT_Rev_0p5

for DS3

PCH to Res routeing 37.5 ohm Impedance.
Res to connector filter routeing 50ohm Impedance. PD Res place close to PCH

Reserve from EMI request

Reserve for power on sequence

+3V_DEEP_SUS 7,8,9,10,39
+3V_RTC 7,10,25
+1.05V 2,4,7,8,9,10,25,30,36,40
+3VPCU 5,7,25,30,31,33,34,35
+3VS5 7,9,10,33,35,36,39,43
+3V 2,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42
+5V 7,10,23,25,27,31,32,33,39

PCH Pull-high/low(CLG)

for DS3

SI reserve

INT HDMI disable (DIS only remove)

INT HDMI Detect Function

System PWR_OK(CLG)

On Die DSW VR Enable

High = Enable (Default)
Low = Disable

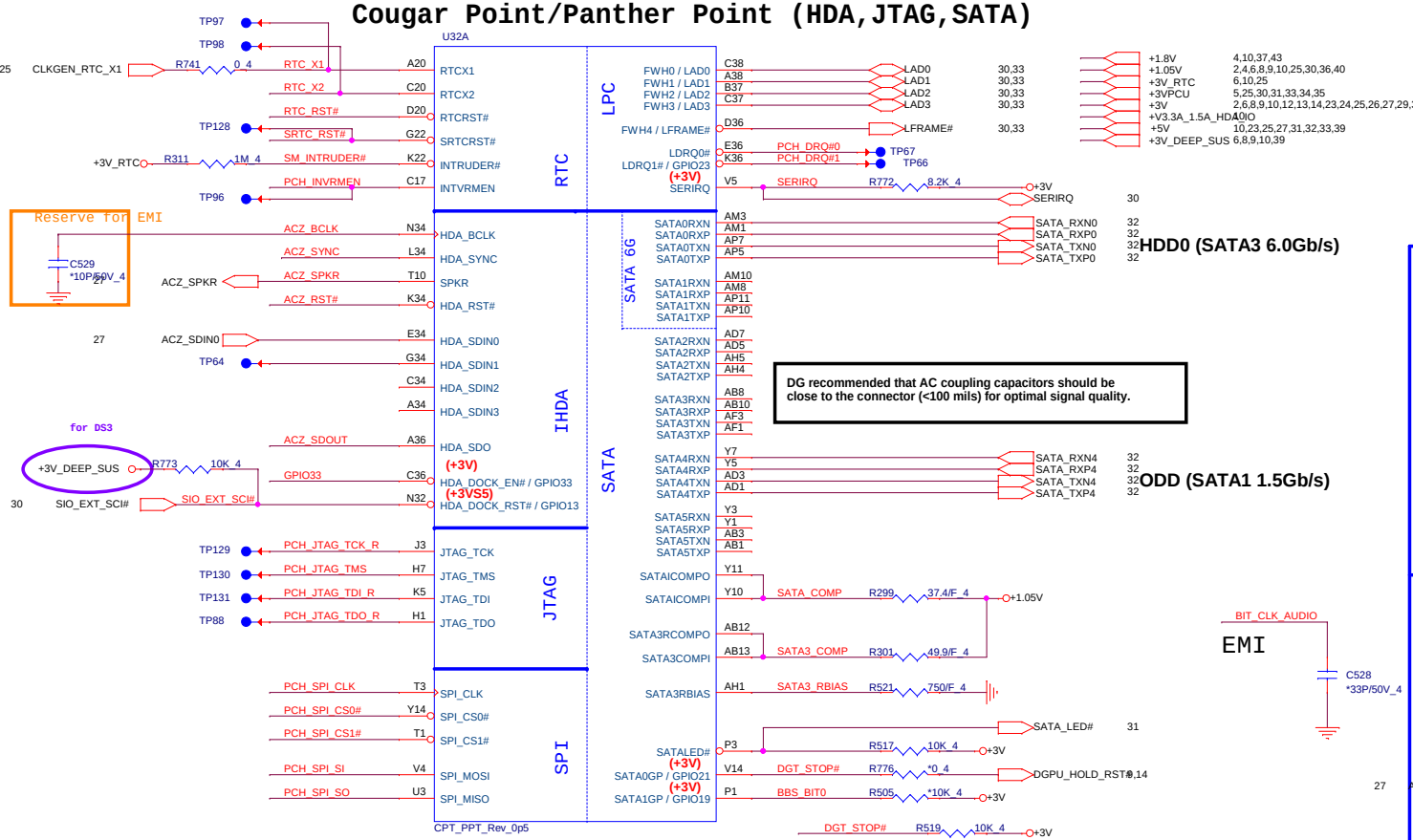
NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A

Date: Monday, October 22, 2012 Sheet 6 of 43

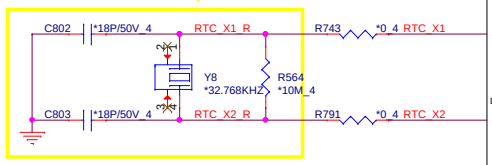
Cougar Point/Panther Point (HDA,JTAG,SATA)



07

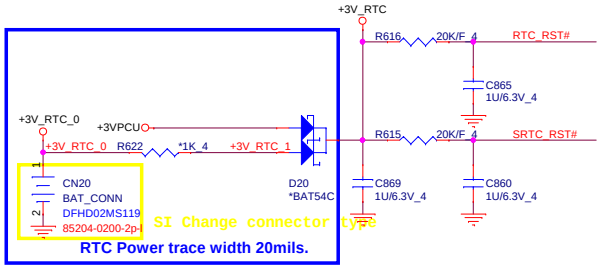
RTC Clock 32.768KHz

SI DEL reserve parts

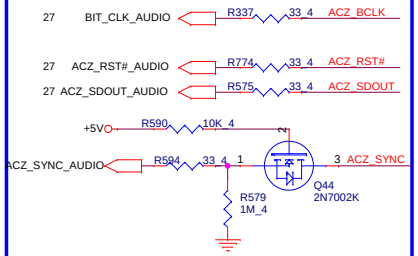


RTC Circuitry(RTC)

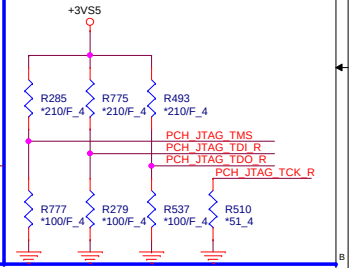
30mils



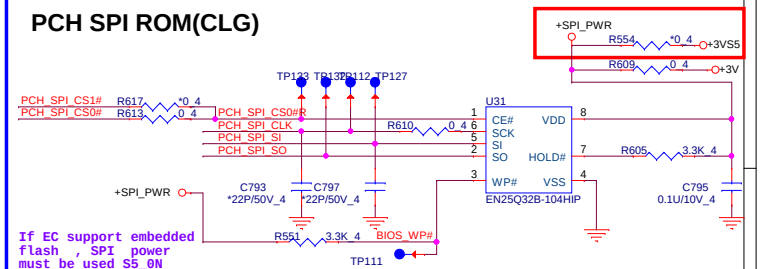
HDA Bus(CLG)



PCH JTAG Debug(CLG)



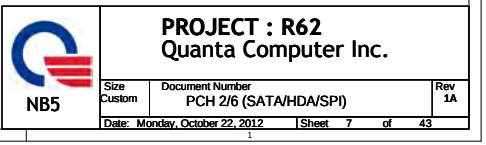
PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39ZN0Q02 (EN25Q32B-104HIP)
PMC	4MB	AKE39ZN0500 (PM25LQ032C-BCE)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R595 10K_4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R563 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R572 0_4 BIOS_WP#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 1 SPI; 1 0 LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		R782 *1K_4 BBS_BIT0 R585 *1K_4 BBS_BIT1 8
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R783 *1K_4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R526 2.2K_4 R546 1K_4 NV_CLE 9 H_SNB_IVB# 2 Sandy/Ivy bridge
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+V3.3A_1.5A_HDA_IO R784 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Overridden	GPIO33_E ACZ_SDOUT R673 *1K_4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	



Cougar Point/Panther Point (PCI,USB,NVRAM)

Cougar Point/Panther Point(PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

USB3.0

USB2.0

USB2.0/USB3.0 COMBO 1st

USB2.0/USB3.0 COMBO 2nd

WLAN

LAN

Cardreader

Webcam

Right_USB

WLAN

EMI

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

PCIE Clock

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

SG : Rb ; UMA : Ra

CLOCK TERMINATION for FCIM

PLTRST#(CLG)

SMBus/Pull-up(CLG)

Remove for UMA only.

PROJECT :	R62
Quanta Computer Inc.	
Size: Custom	Document Number: PCH 3/6 (PCIE/USB/CLK)
Rev: 1A	
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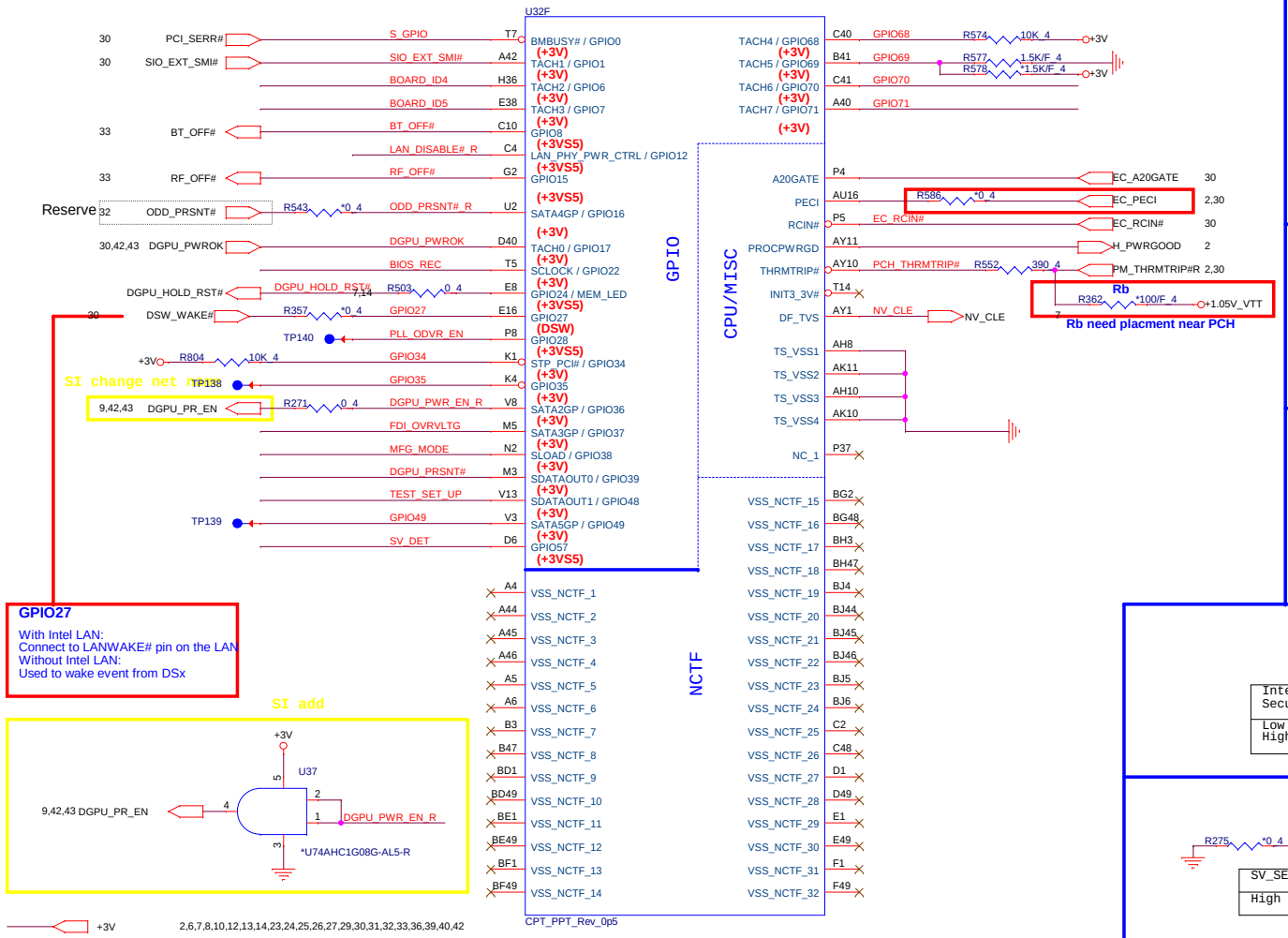
NB5

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



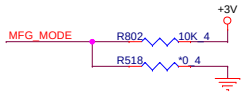
GPIO27

With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx

SI add

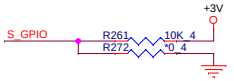
+3V 2,6,7,8,10,12,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42

MFG-TEST

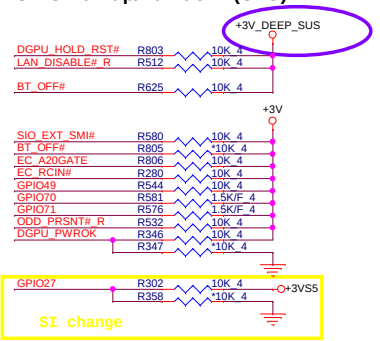


Swap GPIO

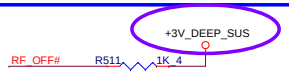
0 = SGPIO
1 = Default



GPIO Pull-up/Pull-down(CLG) for DS3

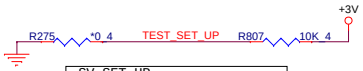


for DS3



Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default) High = Enable

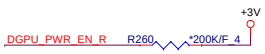
BIOS RECOVERY	High = Disable (Default) Low = Enable



SV_SET_UP
High = Strong (Default)

TEST DETECT
Low = Default

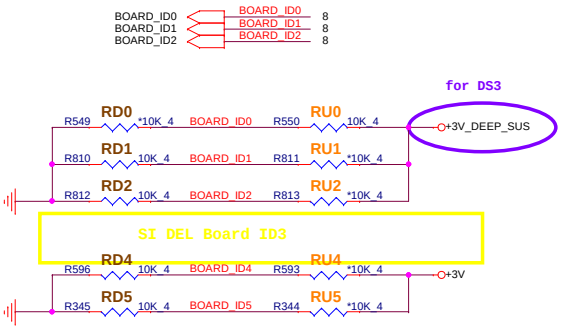
for DS3



BOARD ID SETTING

BOARD_ID1
For Stage Use

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
DB R62 UMA				0	0	0
DB R62 DIS				0	0	1
				0	1	1
				1	1	1
				0	0	0



GFX Present

	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

PROJECT : R62
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A

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Cougar Point/Panther Point(POWER)

COUGAR POINT/Panther Point (POWER)

POWER

U32J

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

POWER

U32G

VCC CORE | VCCIO | CRT | LVDS | HVCMOS | DMI | DFT / SPI | FDI

PCH DS3 PWR

PCH DS3 PWR

If have power noise issue then stuff it.

If EC support embedded flash , SPI power must be used S5_0N power rail for EC load code.

SI add C1107 for 3D mark Screen garbage issue.

+3V_DEEP_SUS	6,7,8,9,39
+1.05V	2,4,6,7,8,9,25,30,36,40
+3V_RTC	6,7,25
+1.5V	4,12,27,33
+3VS5	6,7,9,33,35,36,39,43
+3V	2,6,7,8,9,12,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42
+5VS5	28,29,33,35,36,37,38,39,40,41,42,43
+5V	7,23,25,27,31,32,33,39
+1.8V	4,7,37,43

NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	1A

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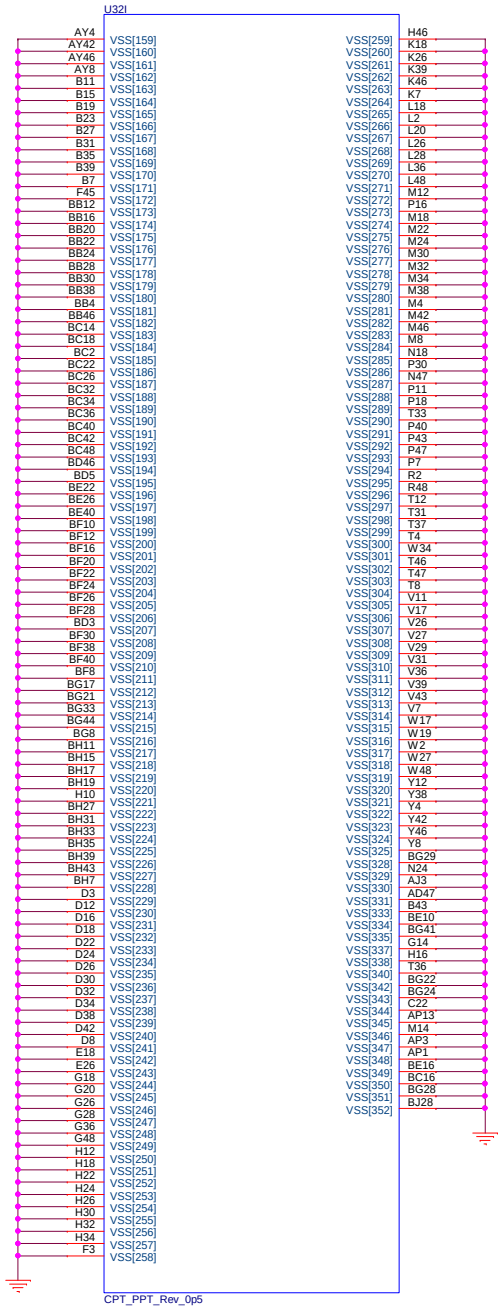
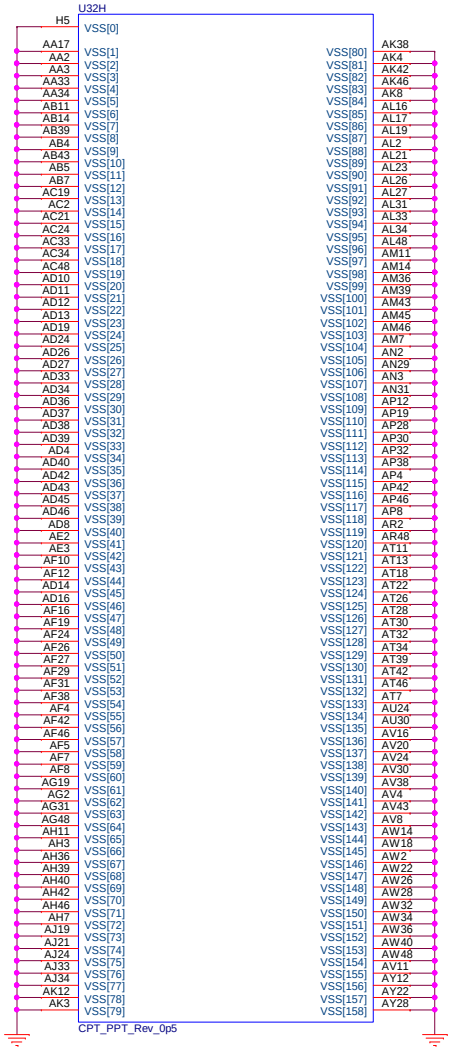
Cougar Point/Panther Point (GND)



Cougar Point/Panther Point (GND)



NB5

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Quanta Computer Inc.

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Custom	PCH 6/6 (GND)	1A

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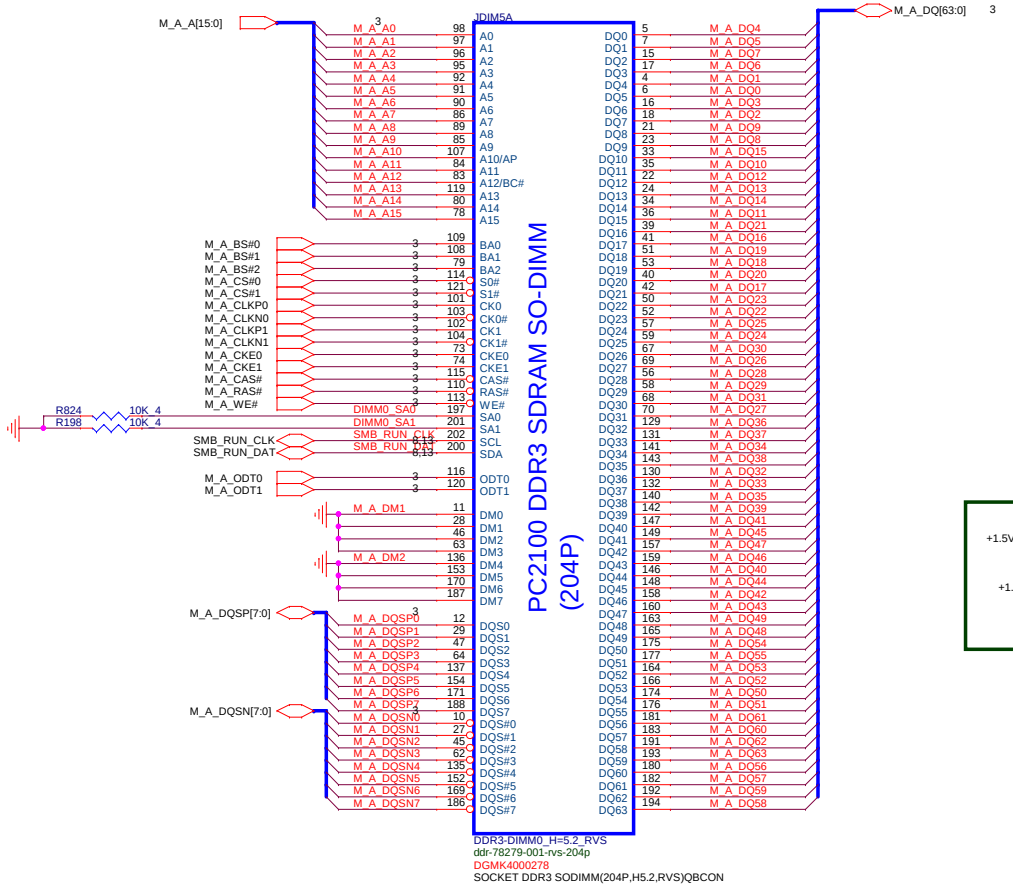
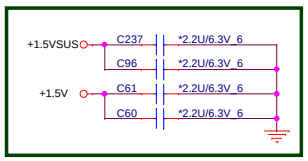
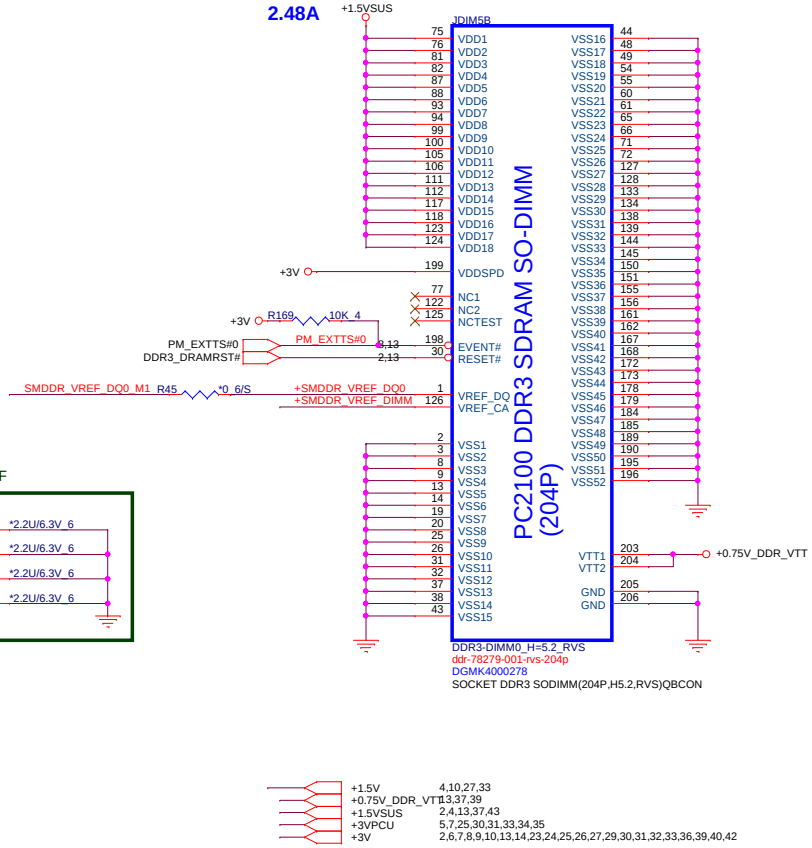


Reseve for RF

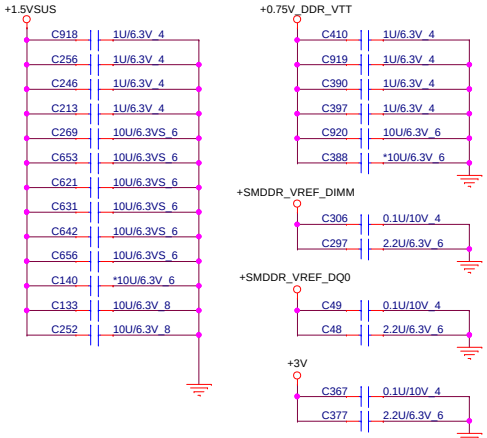


2.48A

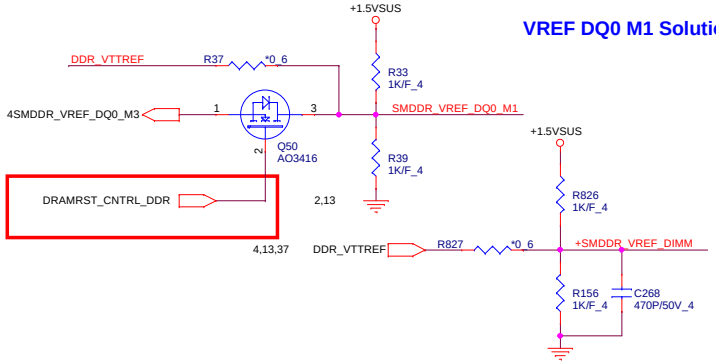


+1.5V	4,10,27,33
+0.75V_DDR_VTT	13,37,39
+1.5VSUS	2,4,13,37,43
+3VPCU	5,7,25,30,31,33,34,35
+3V	2,6,7,8,9,10,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42

Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution



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Custom	DDR3 DIMM0-RVS (5.2H)	1A
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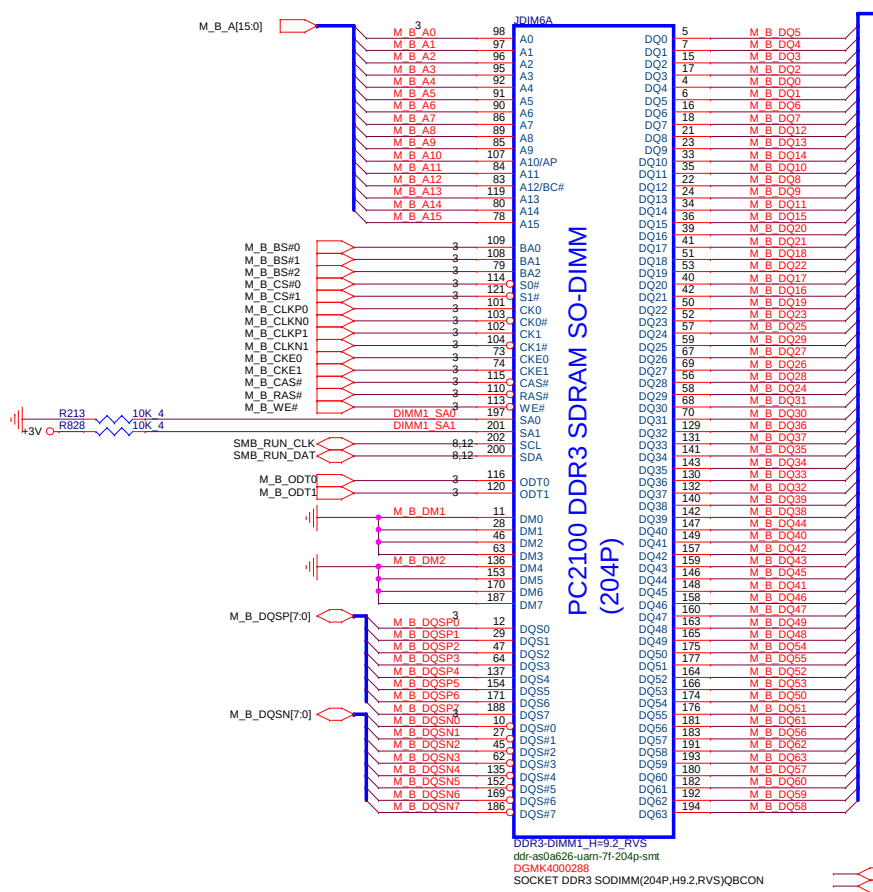
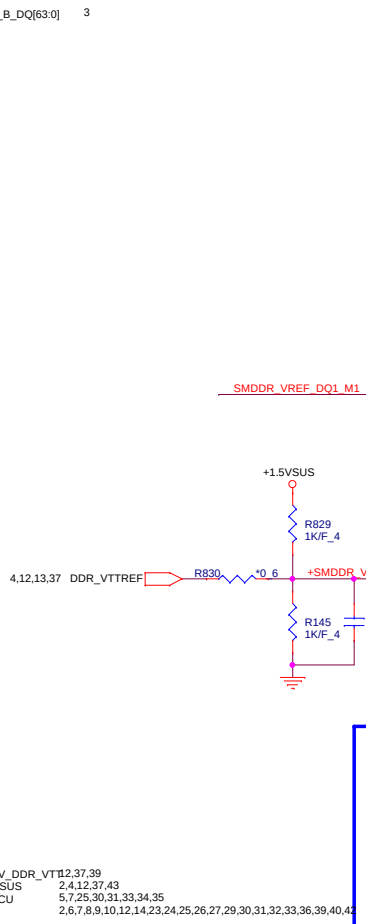
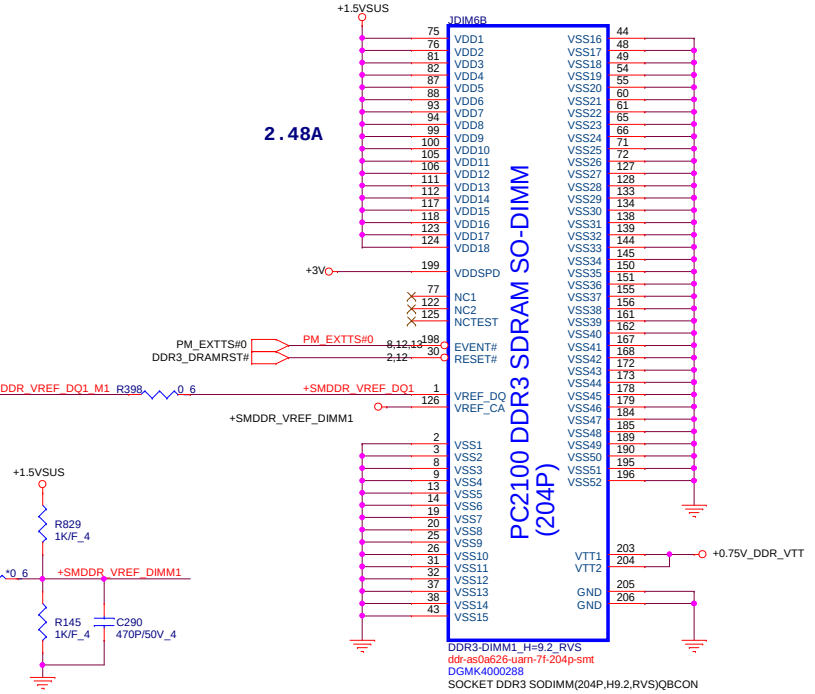
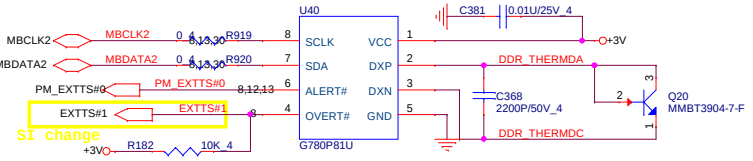




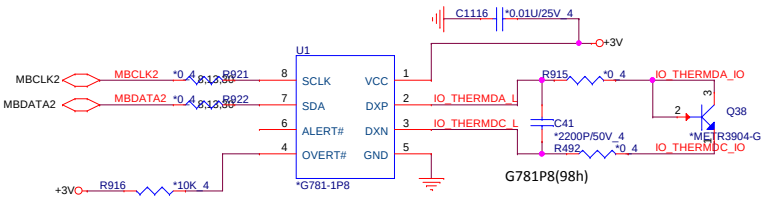


DDR3 Thermal Sensor

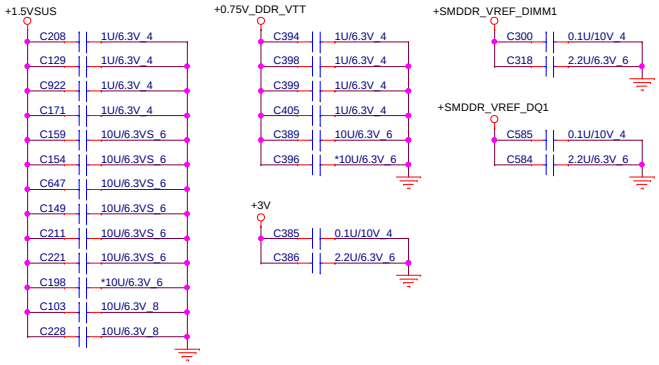


SI Add

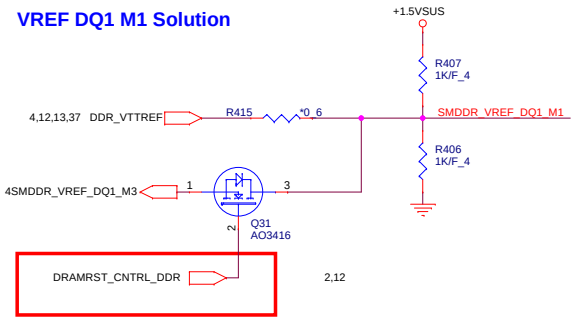
Local Thermal Sensor



Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



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Custom	DDR3 DIMM1-RVS (9.2H)	1A
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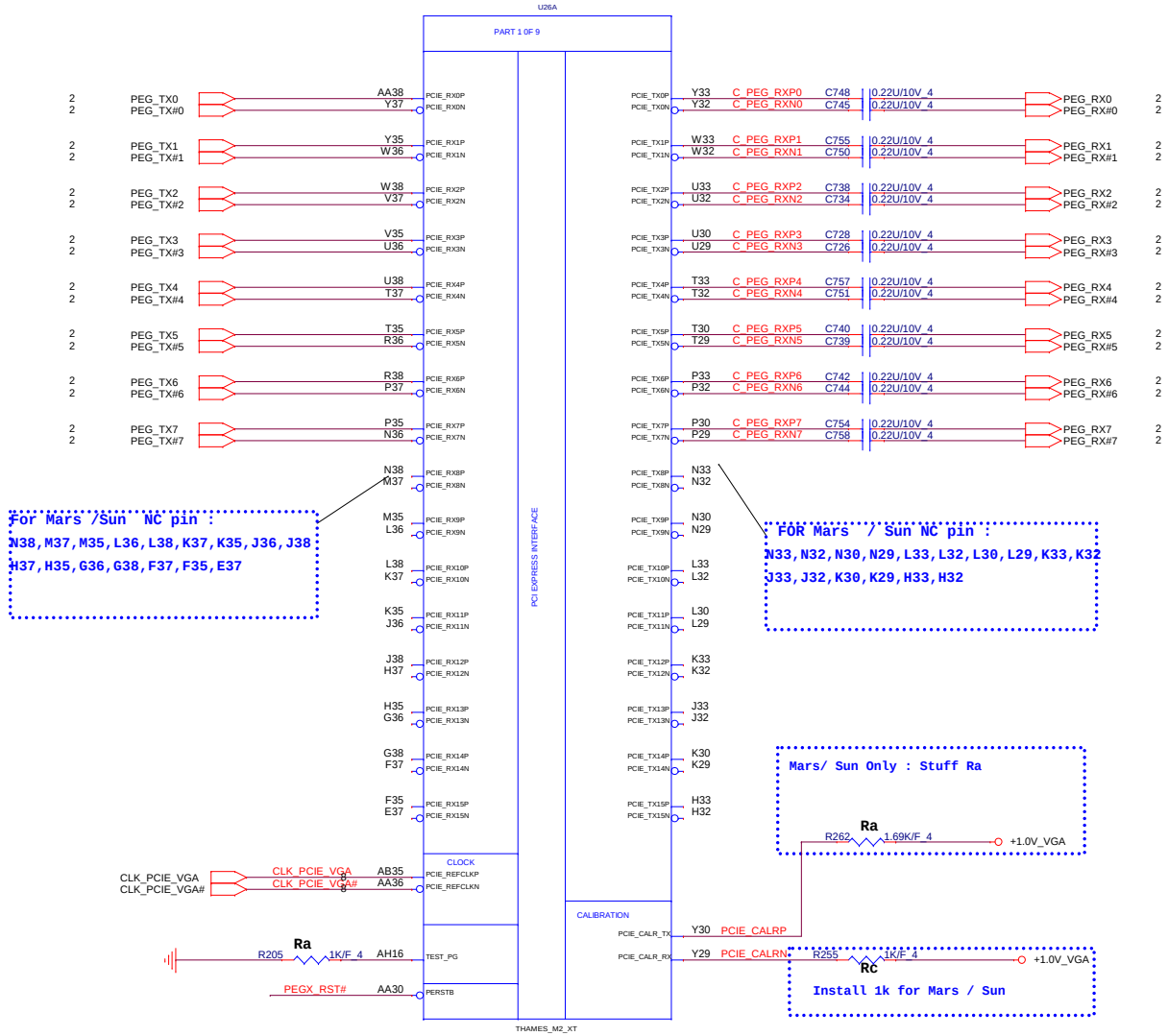

2,6,7,8,9,10,12,16,18,19,43 +1.0V_VGA

+3V
+1.0V_VGA

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Custom	THAMES_PCIE_Interface	1A

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For Mars / Sun : AR1/AW8/AR3/AR8/AU8: NC pin

For Sun only : AD20 /AC20 /AJ21 /AK21: NC pin

For Mars / Sun : DP A to D Port: all NC pin

For Sun only :
AP10 /AV11 /AT11 /AR12 /AW12 / AU12 /AP12 : NC pin

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

SI add

SI DEL revrse R749,R755,R759

SI DEL revrse R778,R781

FOR MARS: AD37/ AE38 / AD35 AVSSN to GND
FOR SUN : AD37/ AE38 / AD35 NC pin

FOR SUN NC PIN : AD34/ AE34 / AC33 / AC34 / AD39 / AE36
AF37/ AC36 / AC38 / AB34 /

FOR SUN GPIO NC PIN : AJ19/ AK19 / AK24 / AM14 / AN14 / AJ24/ AH26 / AH24 / AJ20
AK20/ AH18 / AN16 / AK17 / AK16 / AL16/ AM16

Mars: stuff
For Sun Nc: R167, R141, C923

SI change to SUN setting

A 3-k external pull up (3.3 V) is required if an external BIOS ROM chip is used.

Thermal Solution(Close to GPU)

SI add

Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Reserve for Power Play

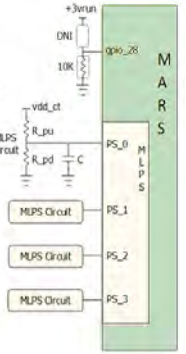
For Mars: Stuff Ra, Rc=> VDDC 1.1V

For Mars / Sun:NC pin
AL30, AM30, AL29, AM29, AN21, AM21, AK30, AK29

For Sun Only :NC pin
AL27, AM27, AN20, AN26, AM26, AL19, ,
AM19, AJ30, AJ31

MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance



Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

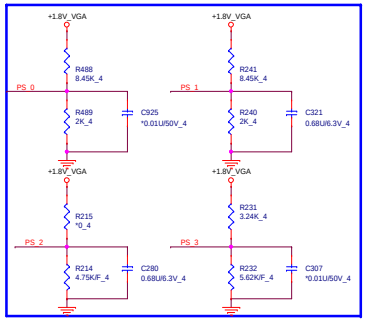
R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

BIT5 => BIT1

PS0	=>	11001
PS1	=>	00001
PS2	=>	00000
PS3	=>	11000

VENDOR	R231	R232
HYNIX 2G	NA	4.75K
MICRON 2G	8.45K	2K
SAM 2G	4.53K	2K
HYNIX 1G	6.98K	4.99K
MICRON 1G	4.53K	4.99K
SAM 1G	3.24K	5.62K



PS3 BIT3=>BIT1	ID	Memory Type	Configuration	PN	Channel Size
000	0	Hynix	H5TC4G63AFR-11C	256Mx16 *4 pces	AKD5PGWTW08 IC SDRAM(96P)H5TC4G63AFR-11C	2G
001	1	Micron	MT41J256M16HA-093G:E	256Mx16 *4 pces	AKD5PZSTL01 IC SDRAM(96P)MT41J256M16HA-093G:E	2G
010	2	Samsung	K4W4G1646B-HC1A	256Mx16 *4 pces	AKD5PZDT501 IC SDRAM(96P)K4W4G1646B-HC1A	2G
011	3	Hynix	H5TC2G63FFR-11C	128Mx16 *4 pces	AKD5MZDTW03 IC SDRAM(96P)H5TC2G63FFR-11C	1G
100	4	Micron	MT41J128M16JT-093G:E	128Mx16 *4 pces		1G
101	5	Samsung	K4W2G1646E-BC1A	128Mx16 *4 pces	AKD5MGGT535 IC SDRAM(96P)K4W2G1646E-BC1A	1G

14,16,18,19,42 1.0V_VGA +1.0V_VGA
16,18,19,25,42 1.8V_VGA +1.8V_VGA
17,18 +3V_DELAY +3V_DELAY

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Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

Fo Mars/ Sun
Change La, Lb
Bead to 0 ohm

La

+1.8V_VGA — L23 0_6 — +1.8V_DPLL_PVDD

Display Phase Lock Loop Power
DPLL_PVDD : 1.8V @ 75mA

C259 10U/6.3V_8 | C264 1U/6.3V_4 | C265 0.1U/10V_4

+1.8V_DPLL_PVDD → AM32 DPLL_PVDD

Lb

+1.0V_VGA — L21 0_6 — +1.0V_DPLL_VDDC

DPLL_VDDC : 0.935V @ 140mA

1.0V(125mA DPLL_VDDC)

C928 10U/6.3V_8 | C929 1U/6.3V_4 | C267 0.1U/10V_4

+1.0V_DPLL_VDDC → AN31 DPLL_VDDC

DPLL_PVSS → AN32 DPLL_PVSS

+1.8V_MPLL_PVDD

MPLL_PVDD : 1.8V @ 150mA

+1.8V_VGA — HCB1608KF-471T10 L35 — +1.8V_MPLL_PVDD → H7 H8 MPLL_PVDD

C441 10U/6.3V_8 | C437 1U/6.3V_4 | C438 0.1U/10V_4

AM10 SPLL_PVDD

+1.8V_SPLL_PVDD

SPLL_PVDD : 1.8V @ 75mA

+1.8V_VGA — L16 TB160808U121N005 — +1.8V_SPLL_PVDD

C167 10U/6.3V_8 | C176 1U/6.3V_4 | C191 0.1U/10V_4

AN9 SPLL_VDDC

AN10 SPLL_PVSS

+1.0V_SPLL_VDDC

SPLL_VDDC : 0.935V @ 150mA

+1.0V_VGA — L19 HCB1608KF-471T10 — +1.0V_SPLL_VDDC

1.0V(125mA DPLL_VDDC)

C181 10U/6.3V_8 | C932 1U/6.3V_4 | C216 0.1U/10V_4

SPLL_PVSS

AF30 NC_XTAL_PVDD
AF31 NC_XTAL_PVSS

DPEF_VDD18

R212 Ra *0_4
R249 Rb *0_4

SI change to DP_VDDR

reserve Ra, Rb for future ASIC

U26I

PART 9 0F 9

PLLS/XTAL

THAMES_M2_XT

SI 27MHz change to XTALIN

R742 0_4 VGA_XTAL27_IN 25

XTALIN AV33 — R818 *0_4 — EVGA-XTALI — *22P/50V_4 C244

R207 *10M_6 | Y2 *7A27000010

XTALOUT AU34 — R819 *0_4 — EVGA-XTALO — *22P/50V_4 C245

SI DEL reserve parts

XO_IN AW34 — TP148

XO_IN2 AW35 — R487 *0_4

CLKTESTA AK10 CLKTESTA
CLKTESTB AL10 CLKTESTB

Debug only,
for clock observation,
if not needed, DNI

C930 *0.1U/10V_4 | C931 *0.1U/10V_4

R171 *51.1/F_4 | R181 *51.1/F_4

route 50ohms
single-ended/
100ohms diff and keep short

14,18,19,43 +1.0V_VGA → +1.0V_VGA

15,18,19,25,42 +1.8V_VGA → +1.8V_VGA

U26F

PART 6 0F 9

PCIE_VSS: AB39 E39 F34 F39 G33 G34 H31 H34 H39 J31 J34 K31 K34 K39 L31 L34 M34 M39 N31 N34 P31 P34 P39 R34 T31 T34 T39 U31 U34 V34 V39 W31 W34 Y34 Y39

GND: F15 F17 F19 F21 F23 F25 F27 F29 F31 F33 F7 F9 G2 G6 H9 J2 J27 J6 J8 K14 K7 L11 L17 L2 L22 L24 L6 M17 M22 M24 N16 N18 N2 N21 N23 N26 N6 R15 R17 R2 R20 R22 R24 R27 R6 T11 T13 T16 T18 T21 T23 T26 U15 U17 U2 U20 U22 U24 U27 U6 V11 V16 V18 V21 V23 V26 W2 W6 Y15 Y17 Y20 Y22 Y24 Y27

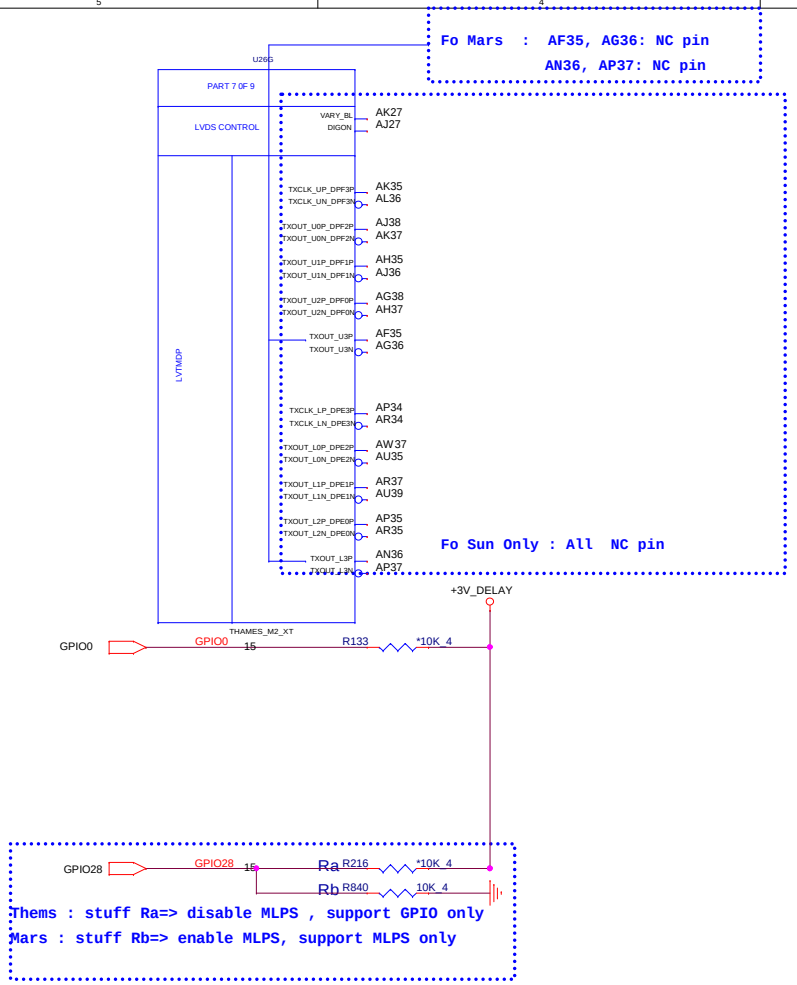
GND: A3 A37 AA16 AA18 AA2 AA21 AA23 AA26 AA28 AA6 AB12 AB15 AB17 AB20 AB22 AB24 AB27 AC11 AC13 AC16 AC18 AC2 AC21 AC23 AC26 AC28 AC6 AD15 AD17 AD20 AD22 AD24 AD27 AD9 AE2 AE6 AF10 AF16 AF18 AF21 AG17 AG2 AG20 AG22 AG6 AG9 AH21 AJ10 AJ11 AJ2 AJ28 AJ6 AK11 AK31 AK7 AL11 AL14 AL17 AL2 AL20

AG22 is nc pin

GND: AL23 AL26 AL32 AL6 AL8 AM11 AM31 AM9 AN11 AN2 AN30 AN6 AN8 AP11 AP7 AP9 AR5 B11 B13 B15 B17 B19 B21 B23 B25 B27 B29 B31 B33 B7 B9 C1 C39 E35 E5 F11 F13

VSS_MECH: A39 AW1 AW39

THAMES_M2_XT



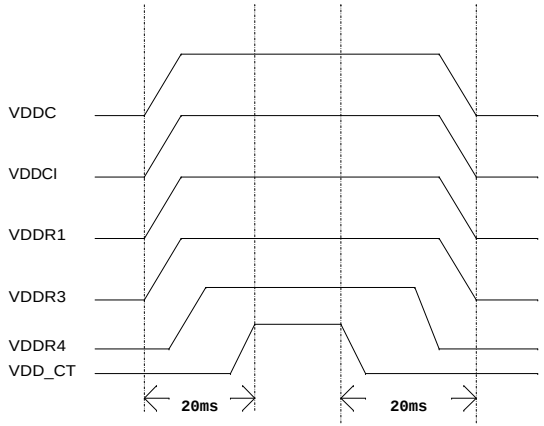
CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0	
0	128M	0	0	0	+VGA_CORE
0	256M	0	0	1	+VGA_CORE
0	64M	0	1	0	+1.5V_VGA
0	32M	0	1	1	+3.3V_Delay
0	512M	1	0	0	+1.8V_VGA
0	1G	1	0	1	+1.8V_VGA
0	2G	1	1	0	
0	4G	1	1	1	

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

Power Up/Down Sequence



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Custom	THAMES_LVDS / STRAP	1A
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+1.5V_VGA

VDDR1 , 1.5V @ 2A, GDDR5 900MHz

I/O power for the memory interface.

C933 1U/6.3V_4 C934 1U/6.3V_4 C719 1U/6.3V_4 C468 1U/6.3V_4 C935 1U/6.3V_4 C764 1U/6.3V_4 C335 1U/6.3V_4 C936 1U/6.3V_4 C725 1U/6.3V_4 C470 1U/6.3V_4

C401 10U/6.3VS_6 C479 10U/6.3VS_6 C942 10U/6.3VS_6 C943 10U/6.3VS_6 C689 10U/6.3VS_6 C944 10U/6.3VS_6

Reserve for Drop

C826 *22U/6.3VS_8 C254 *22U/6.3VS_8 C453 *22U/6.3VS_8 C178 22U/6.3VS_8 C449 *22U/6.3VS_8

C457 *22U/6.3VS_8 C205 22U/6.3VS_8 C785 *22U/6.3VS_8 C609 *330u_2.5V_3528 C710 *330u_2.5V_3528

AC7 AD11 AF7 AG10 AJ7 AK8 AL9 G11 G14 G17 G20 G23 G26 G29 H10 J7 J9 K11 K13 K8 L12 L16 L21 L23 L26 L7 M11 N11 P7 R11 U11 U7 Y11 Y7 — VDDR1

VDDC_CT: 1.8V @250mA

+1.8V_VDD_CT

+1.8V_VGA

L49 0_6

C672 *10U/6.3VS_6 C660 1U/6.3V_4 C661 1U/6.3V_4 C655 1U/6.3V_4 C654 0.1U/10V_4

AF26 AF27 AG26 AG27 — VDD_CT

VDDR3 : 3.3V @ 60mA

+3V_DELAY

+3V_VGA

L17 0_6

C676 *10U/6.3VS_6 C673 1U/6.3V_4 C240 1U/6.3V_4 C674 1U/6.3V_4

AF23 AF24 AG23 AG24 — VDDR3

VDDR4 : 1.8V @ 300mA

+VDDR4

L18 *0_6

C214 *10U/6.3VS_6 C223 *10U/6.3VS_6 C241 *1U/6.3V_4 C232 *1U/6.3V_4 C311 *0.1U/10V_4 C955 *0.1U/10V_4

AD12 AF11 AF12 AF13 — VDDR4

AF15 AG11 AG13 AG15 — VDDR4

For Mars: stuff

For Sun: NC L18, C214, C223,C241, C232, C311, C955

SI DEL parts for SUN setting

U26E

PART 5 OF 9

MEM I/O — LEVEL TRANSLATION — I/O — DVP — VOLTAGE SENSE — PCIE — BACO — CORE — ISOLATED CORE I/O

THAMES_M2_XT

NC_PCIE_VDDR AA31 AA32 AA33 AA34 W30 Y31 V28 W29 AB37

C961 0.1U/10V_4 C376 1U/6.3V_4 C362 10U/6.3VS_6

PCIe Digital Power Supply
PCIE_VDDC : 0.935V @ 1.88A (GEN2.0)
PCIE_VDDC : 0.935V @ 2.5A (GEN3.0)

+1.0V_VGA

G30 G31 H29 H30 J29 J30 L28 M28 N28 R28 T28 U28 — PCIE_VDDC

C939 0.1U/10V_4 C373 0.1U/10V_4 C940 0.1U/10V_4 C366 1U/6.3V_4 C393 1U/6.3V_4 C379 1U/6.3V_4 C941 1U/6.3V_4 C374 1U/6.3V_4 C363 1U/6.3V_4

C378 1U/6.3V_4 C945 1U/6.3V_4 C364 1U/6.3V_4 C380 1U/6.3V_4 C361 10U/6.3VS_6 C360 10U/6.3VS_6

BIF_VDDC

R267 Ra 0_8

R290 Rb *0_8

N27 T27 — BIF_VDDC

+VGA_CORE

	Ra	Rb	Rc	Rd
Chelsea-non BACO	install	na	na	na
Chelsea-BACO	install	na	na	na
Thames-non BACO	na	install	install	install
Thames-BACO	na	na	install	install

AA15 AA17 AA20 AA22 AA24 AA27 AB16 AB18 AB21 AB23 AB26 AB28 AC17 AC20 AC22 AC24 AC27 AD18 AD21 AD23 AD26 AF17 AF20 AF22 AG16 AG18 AH22 AH27 AH28 M26 N24 R18 R21 R23 R26 T17 T20 T22 T24 U16 U18 U21 U23 U26 V17 V20 V22 V24 V27 Y16 Y18 Y21 Y23 Y26 Y28 — VDDC

C946 1U/6.3V_4 C372 1U/6.3V_4 C356 1U/6.3V_4 C371 1U/6.3V_4 C354 1U/6.3V_4 C210 1U/6.3V_4 C353 1U/6.3V_4 C219 1U/6.3V_4 C384 1U/6.3V_4 C370 1U/6.3V_4

C313 1U/6.3V_4 C947 1U/6.3V_4 C948 1U/6.3V_4 C355 1U/6.3V_4 C369 1U/6.3V_4 C949 1U/6.3V_4 C314 1U/6.3V_4 C315 1U/6.3V_4 C180 1U/6.3V_4 C950 1U/6.3V_4

C951 1U/6.3V_4 C317 1U/6.3V_4 C350 1U/6.3V_4 C952 1U/6.3V_4 C316 1U/6.3V_4 C953 1U/6.3V_4 C340 1U/6.3V_4 C239 1U/6.3V_4 C342 1U/6.3V_4 C954 1U/6.3V_4

C217 10U/6.3VS_6 C956 10U/6.3VS_6 C224 10U/6.3VS_6 C203 10U/6.3VS_6 C957 10U/6.3VS_6

C242 10U/6.3VS_6 C309 10U/6.3VS_6 C234 10U/6.3VS_6 C338 10U/6.3VS_6

C351 330u_2.5V_3528

BIF_VDDC

C403 22U/6.3VS_8 C959 1U/6.3V_4 C404 1U/6.3V_4 C391 10U/6.3VS_6

20,21,22,43 +1.5V_VGA
14,16,19,43 +1.0V_VGA
15,16,19,25,43 +1.8V_VGA
43 +3V_VGA
33,42,43 +VGA_CORE

+1.5V_VGA +1.0V_VGA +1.8V_VGA +3V_VGA +VGA_CORE

+VDDCI

VDDCI 0.8-1.15V @ 6A

+VGA_CORE

AA13 AB13 AC12 AC15 AD13 AD16 M15 M16 M18 M23 N13 N15 N17 N20 N22 R12 R13 R16 T12 T15 V15 Y13 — VDDCI

C312 1U/6.3V_4 C375 1U/6.3V_4 C343 1U/6.3V_4 C331 1U/6.3V_4 C339 1U/6.3V_4 C382 1U/6.3V_4 C958 1U/6.3V_4 C387 1U/6.3V_4

C383 10U/6.3VS_6 C960 10U/6.3VS_6 C395 10U/6.3VS_6 C365 1U/6.3V_4 C348 1U/6.3V_4

Route as differential pair and connect to the VSEN and RTN pins of the VR through a decoupling and termination circuit.

VGPU_CORE_SENSE — AF28 — FB_VDDC

TP33 — AG28 — FB_VDDCI

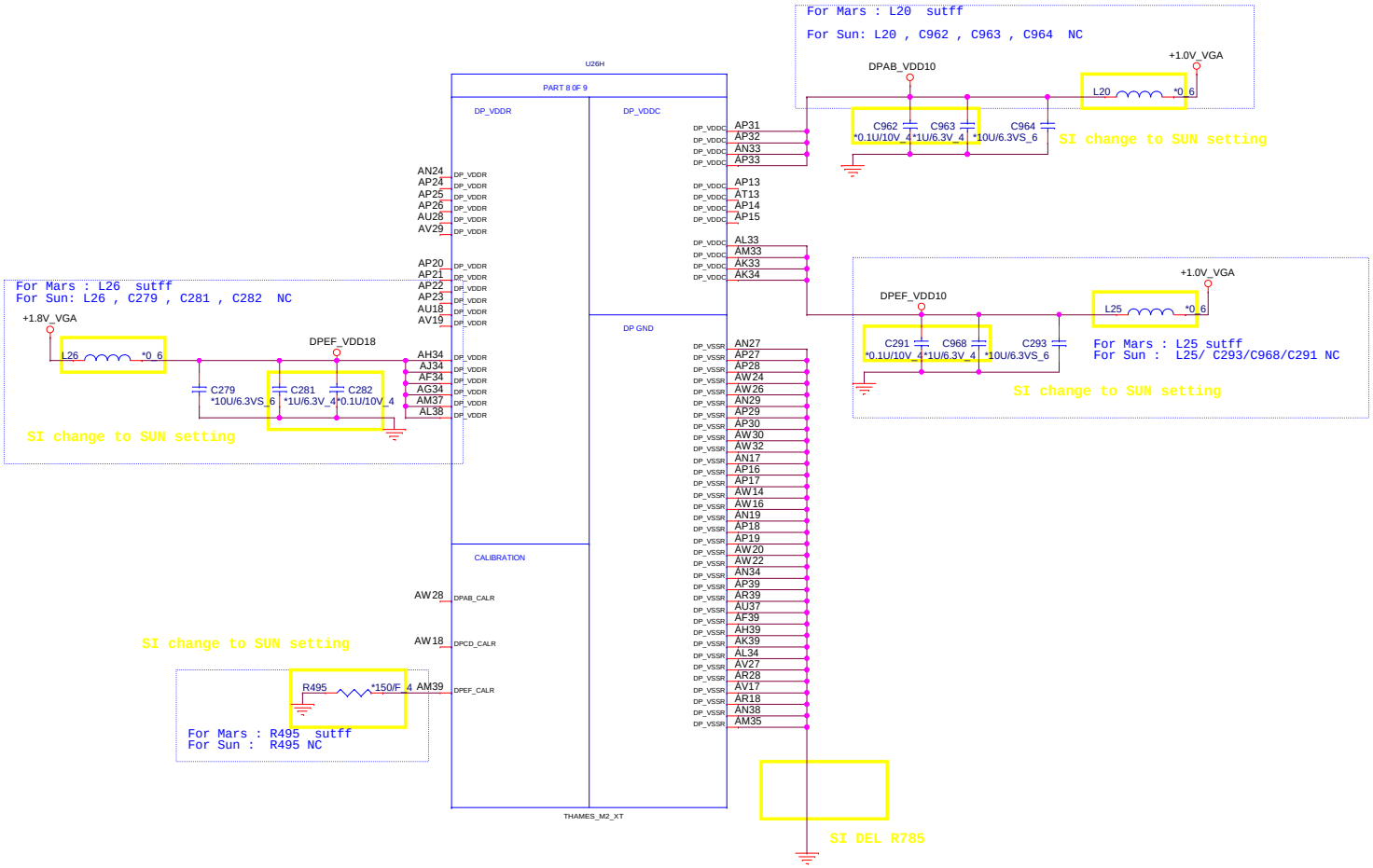
VSS_GPU_SENSE — AH29 — FB_GND

NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_Power & BACO	1A

Date: Monday, October 22, 2012 Sheet 18 of 43



14,16,18,43 +1.0V_VGA
15,16,18,25,48 +1.8V_VGA

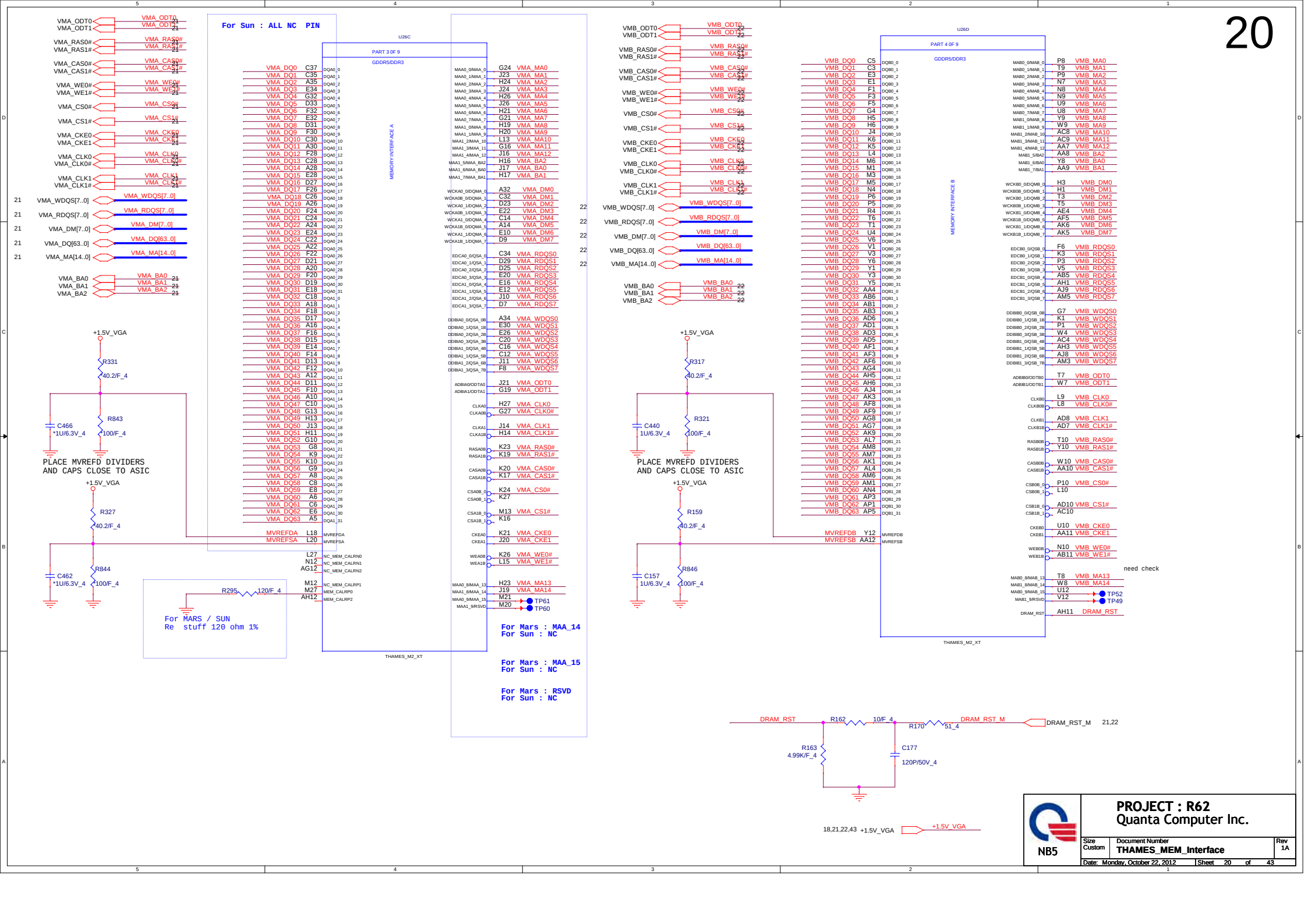
+1.0V_VGA
+1.8V_VGA

NB5

PROJECT : R62
Quanta Computer Inc.

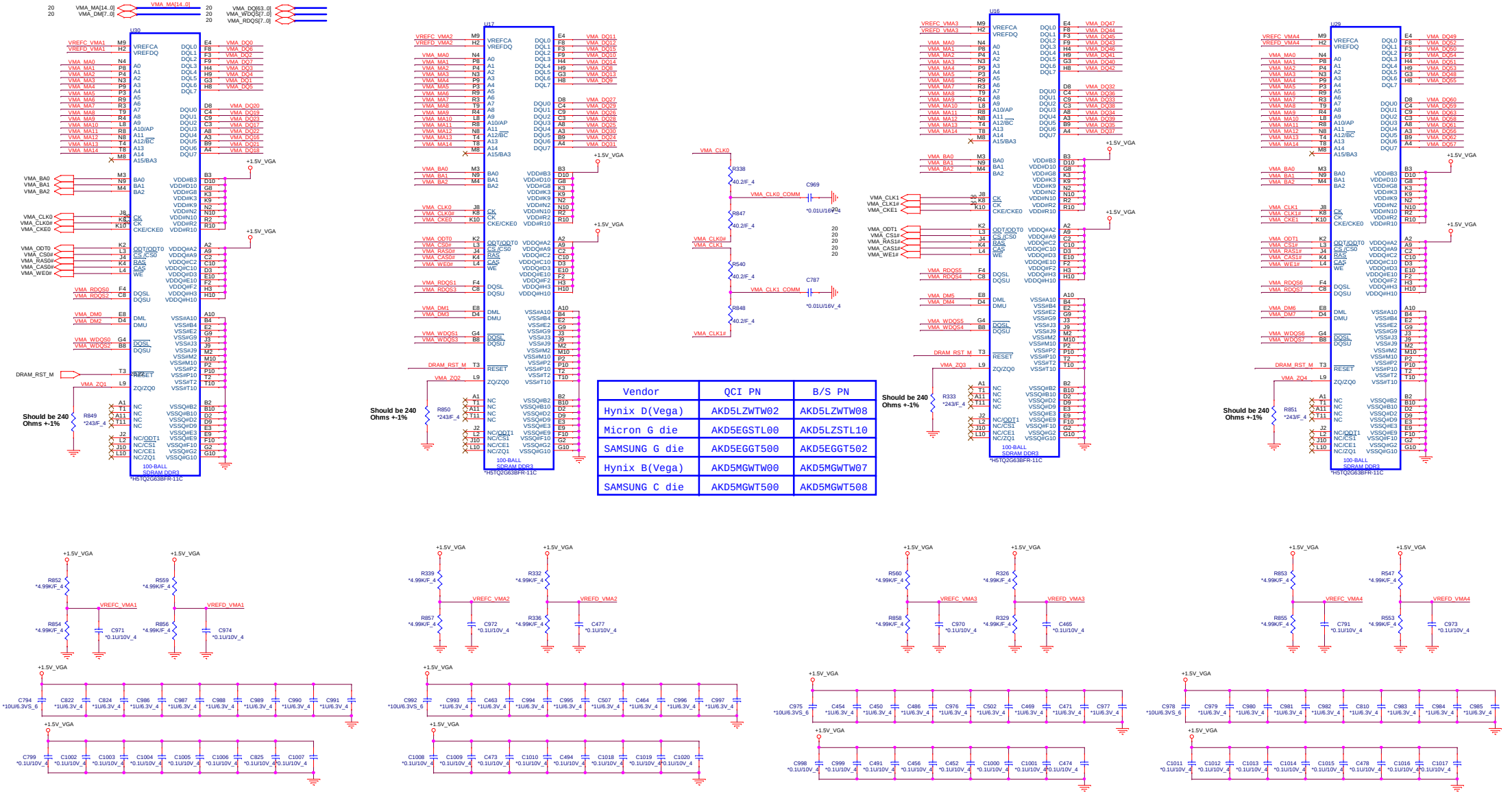
Size	Document Number	Rev
Custom	THAMES_DP Powers	1A

Date: Monday, October 22, 2012 Sheet 19 of 43



PROJECT : R62	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: THAMES_MEM_Interface
Rev: 1A	
Date: Monday, October 22, 2012	Sheet 20 of 43

CHANNEL A: 256MB/512MB DDR3



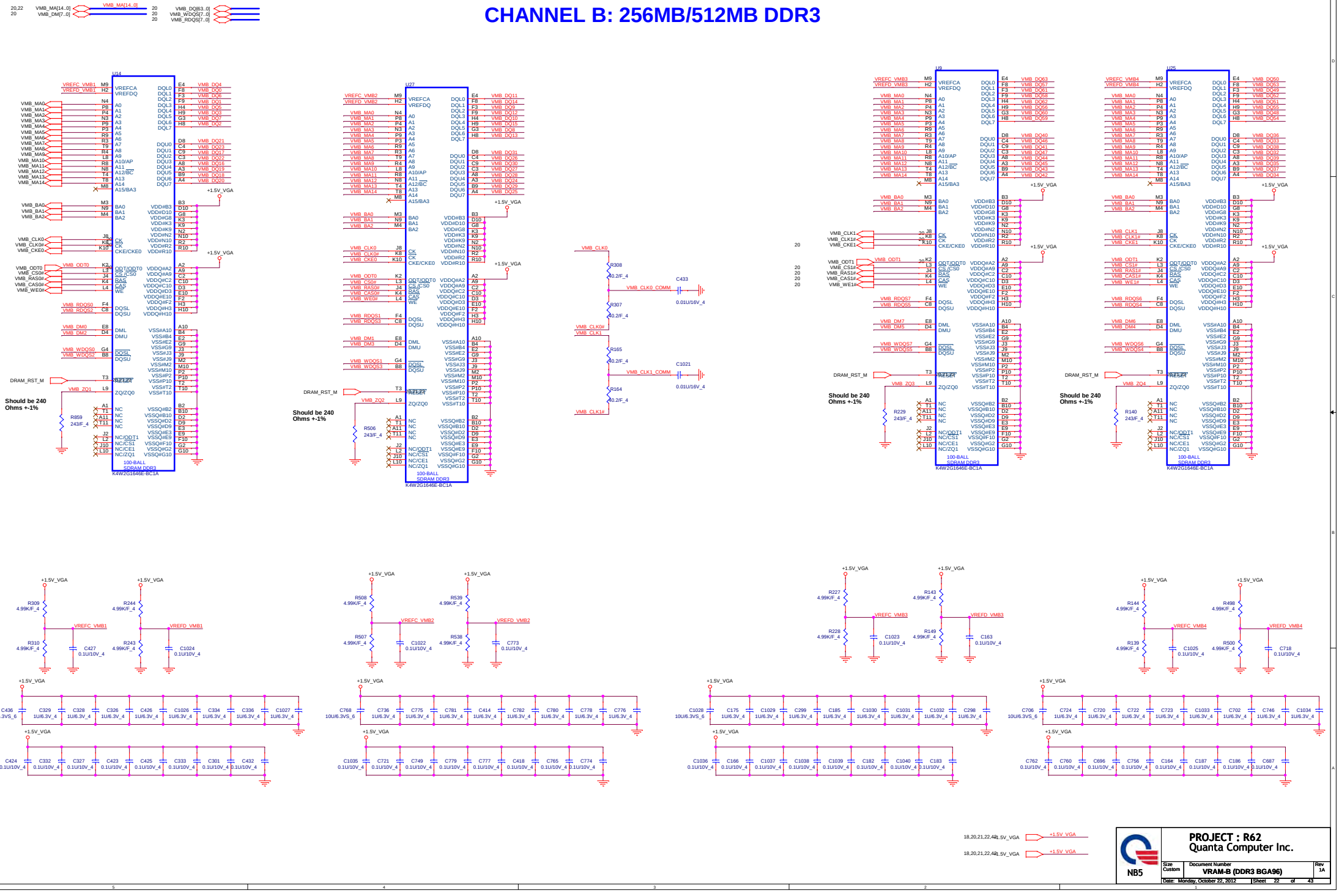
Vendor	QCI PN	B/S PN
Hynix D(Vega)	AKD5LZWTW02	AKD5LZWTW08
Micron G die	AKD5EGSTL00	AKD5LZSTL10
SAMSUNG G die	AKD5EGGT500	AKD5EGGT502
Hynix B(Vega)	AKD5MGWTW00	AKD5MGWTW07
SAMSUNG C die	AKD5MGWT500	AKD5MGWT508

18,20,22,43 +1.5V_VGA +1.5V_VGA

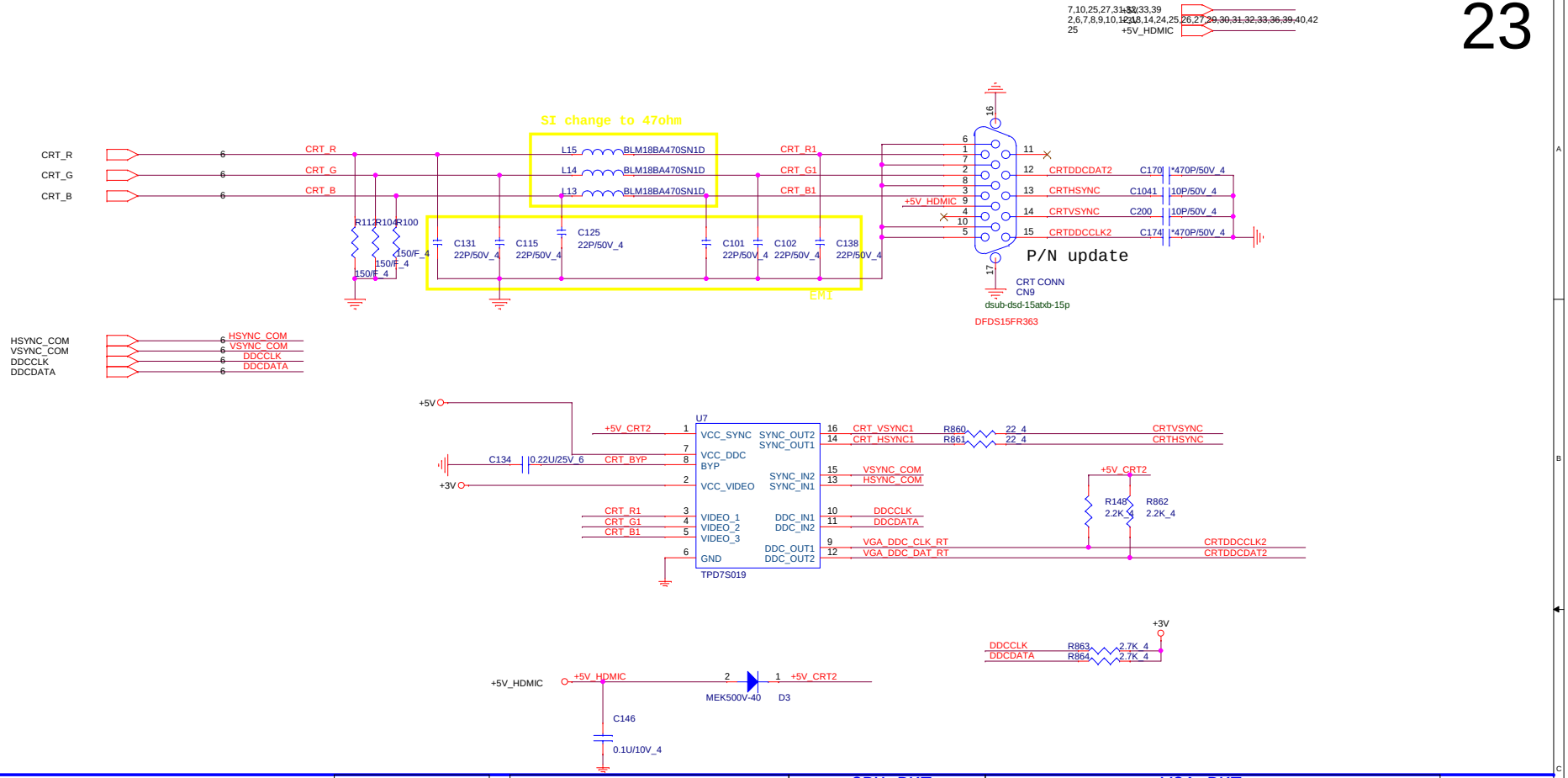
NB5	Size: Custom	Document Number: VRAM-A (DDR3 BGA96)		Rev: 3A
	Date: Monday, October 22, 2012	Sheet 21 of 43		

PROJECT : R62
Quanta Computer Inc.

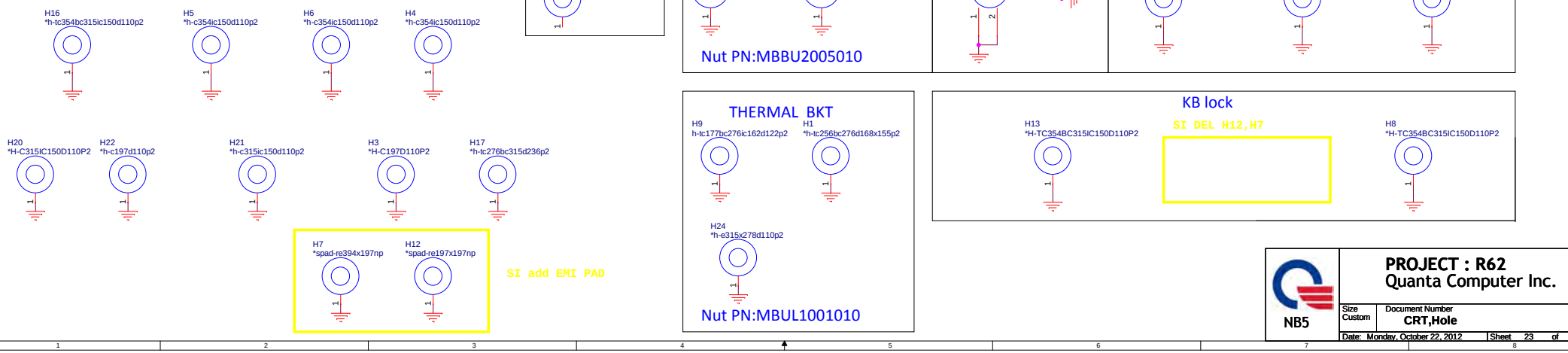
CHANNEL B: 256MB/512MB DDR3



CRT PORT

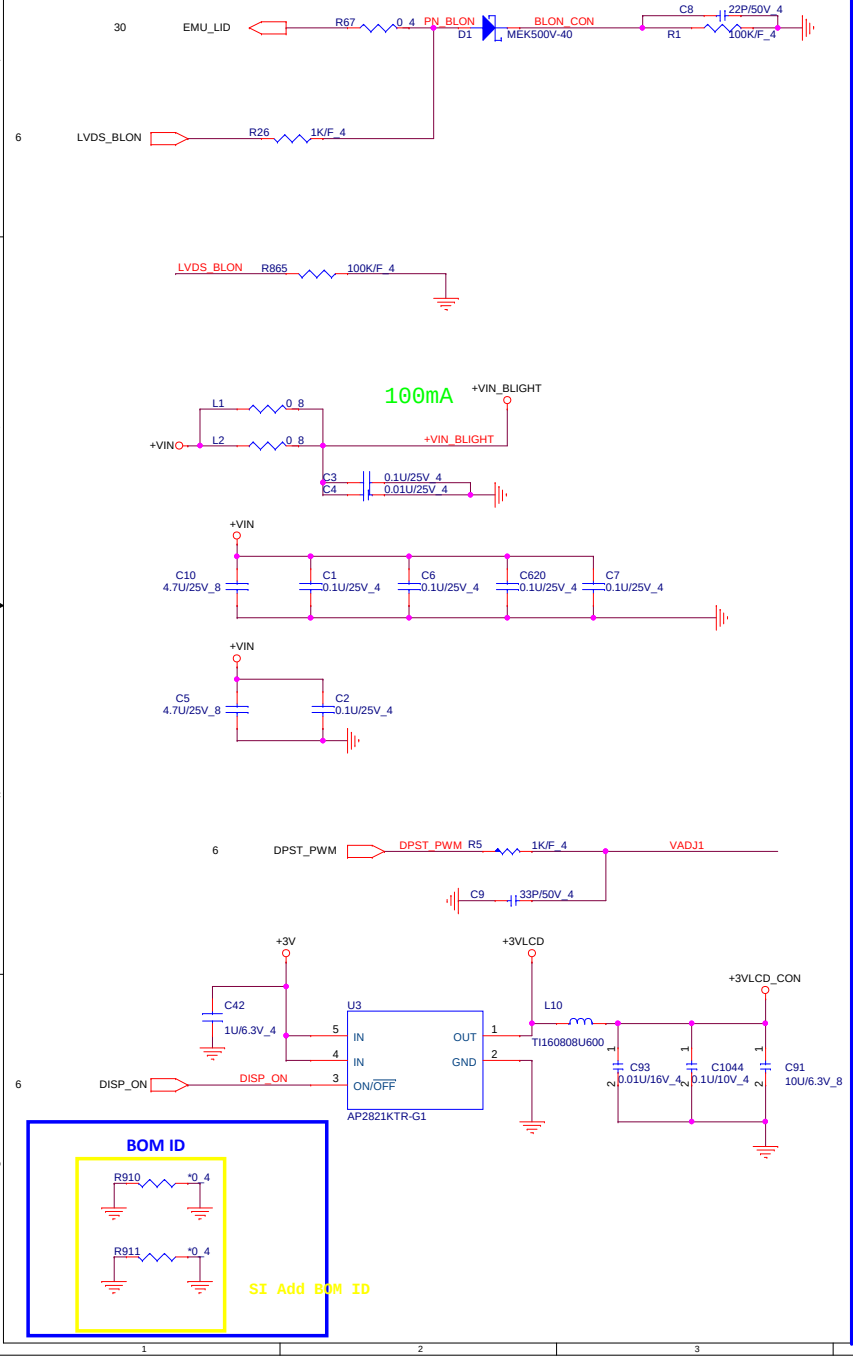


HOLE



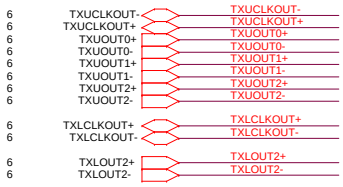
NB5	PROJECT : R62 Quanta Computer Inc.	
Size: Custom	Document Number: CRT,Hole	Rev: 1A
Date: Monday, October 22, 2012	Sheet 23 of 43	

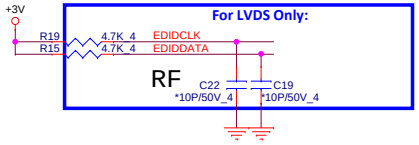
LID Switch

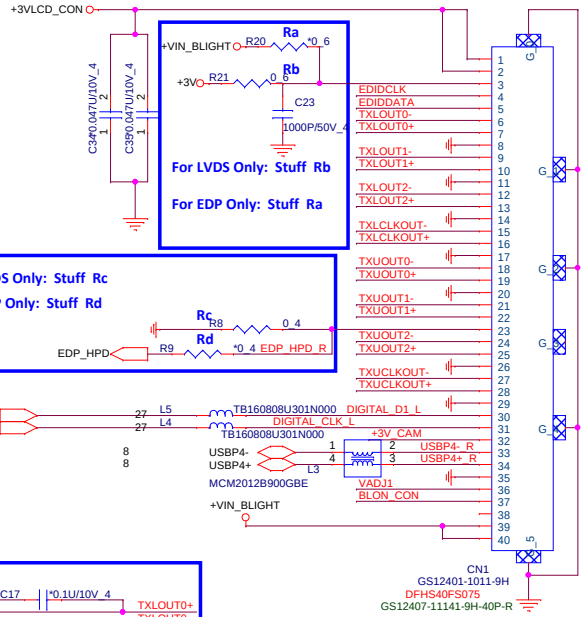


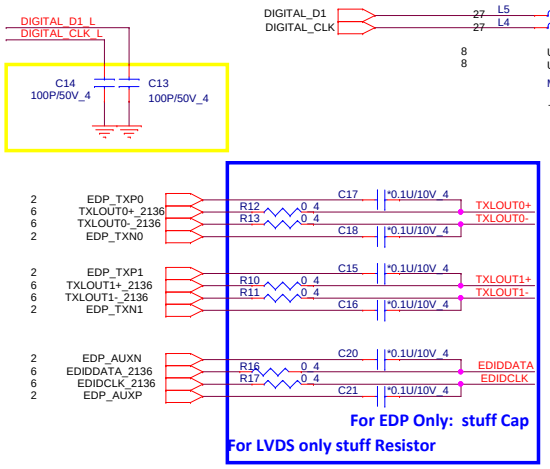
BOM ID

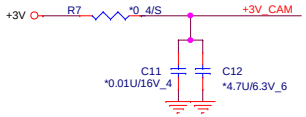
SI Add BOM ID

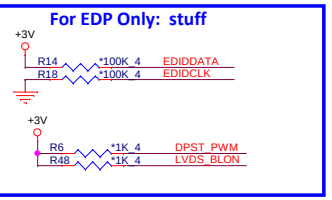


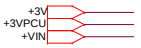












2,6,7,8,9,10,12,13,14,23,25,26,27,29,30,31,32,33,36,3
5,7,25,30,31,33,34,35
33,34,35,36,37,39,41,42,43

NB5

PROJECT : R62
Quanta Computer Inc.

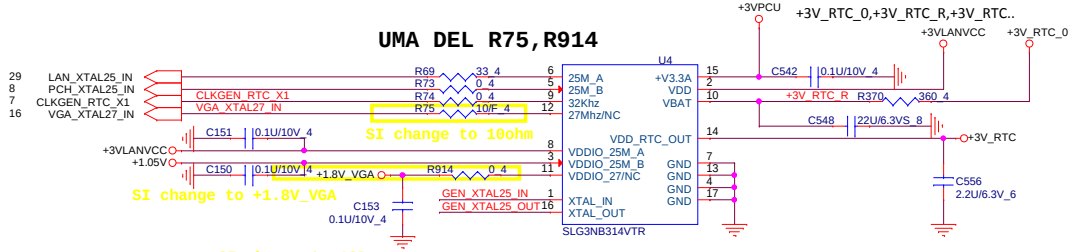
Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A

Date: Monday, October 22, 2012 Sheet 24 of 43

Green CLK Circuitry

20mils width(min)
+3V_RTC_0,+3V_RTC_R,+3V_RTC..

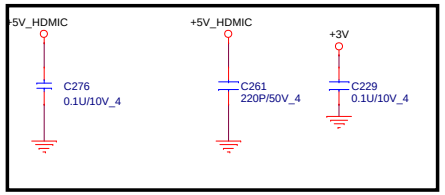
UMA DEL R75,R914



	U4 P/N
UMA	AL3NB244000
DIS	AL000314000

5,7,30,31,33,34,35 +3VPCU
29,39 +3VLANVCC
7 +3V_RTC_0
6,7,10 +3V_RTC
2,4,6,7,8,9,10,39,40,41 +3V
18,43 +3V_VGA

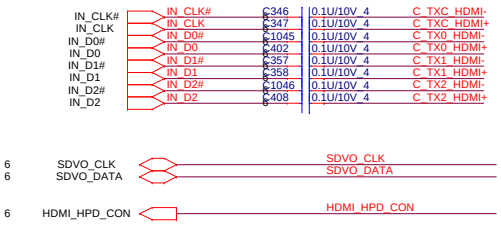
EMI request



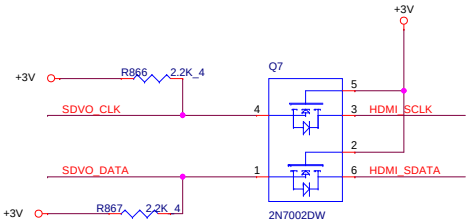
7,10,23,27,31,32,33,36 +3V
23 +5V_HDMIC
2,6,7,8,9,10,12,13,14,24,26,27,29,30,31,32,33,36,39,40,42

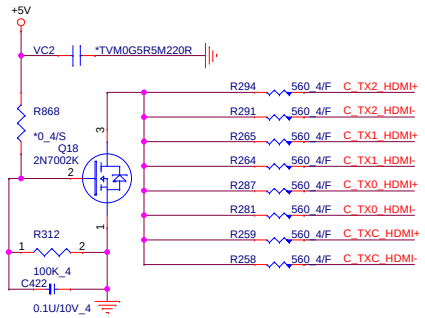
EMI request

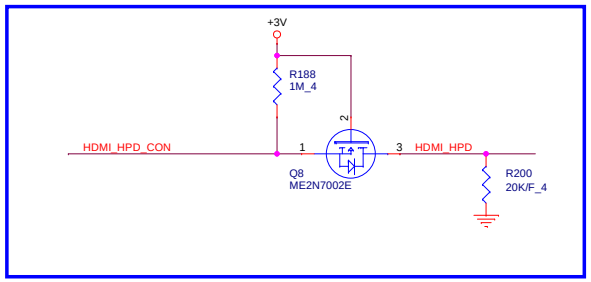
close to HDMI conn

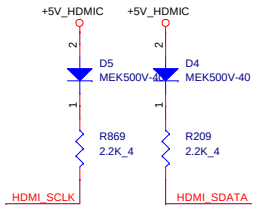


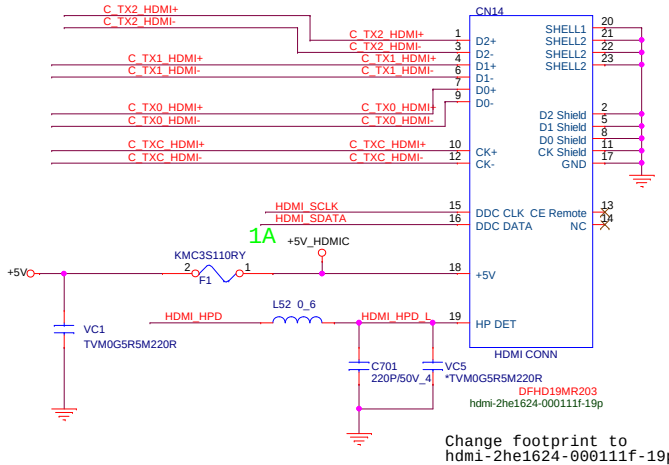
Close to HDMI Connector











Change footprint to
hdmi-2he1624-000111f-19p

PROJECT : R62
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	HDMI CONN	1A
Date: Monday, October 22, 2012	Sheet 25 of 43	

8 CLK_PCIE_REQ2# CLK_PCIE_REQ2# R446 *0_4/S CLK_PCIE_REQ2#_R

Share Pin

SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS

R449 10K_4 +3V

2,8,14,29,30,33 PLTRST# R870 0_4 CLK_PCIE_REQ2#_R

SD_CD# SD_WP RTS5227_GPIO

U38

CLKREQ# PERST# MS_INS# SD_CW SP7 GPIO

Close to chip pin

8 PCIE_TXP3_CARD
8 PCIE_TXN3_CARD
8 CLK_PCIE_CARDP
8 CLK_PCIE_CARDN
8 PCIE_RXP3_CARD
8 PCIE_RXN3_CARD

C598 0.1U/10V_4 PCIE_RXP3_CARD_C
C597 0.1U/10V_4 PCIE_RXN3_CARD_C

1 HSIP
2 HSIN
3 REFCLKP
4 REFCLKN
5 HSOP
6 HSON
25 GND

RTS5239

DV33_18 SP3 SP2

Close to chip pin

18 SP6 SD_D2_R R871 0_4 SD_D2
17 SP5 SD_D3_R R443 0_4 SD_D3
16 SP4 SD_CMD_R R442 0_4 SD_CMD
15 DV33_18
14 SP3 SD_CLK_R R441 22_4 SD_CLK
13 SP2 SD_D0_R R438 0_4 SD_D0

1U/10V_4 C1047
C1048 5.6P/16V_4

Please add 9 GND VIAs connection with thermal PAD

AV12 RREF 3V3IN 3V3AD_3V3 DV12S SP1

RTS5239

7 8 9 10 11 12

RTS5227_AV12 RTS5227_DV12S

SD_D1_R R437 0_4 SD_D1

4.7U/6.3V_6 C633
0.1U/10V_4 C590

R435 6.2K/F_4 RTS5227_RREF
C589 *100P/50V_4

R435 need colse to Chip

+3V

C591 0.1U/10V_4
C588 4.7U/6.3V_6

C587 10U/6.3V_8
C593 0.1U/10V_4

+3VCARD

Reserve for EMI

SD_D0	C1069	*5.6P/16V_4
SD_D1	C612	*5.6P/16V_4
SD_D2	C611	*5.6P/16V_4
SD_D3	C1068	*5.6P/16V_4

Close to U38

SD / MMC CARD READER

CN8

SD_D3 1 DAT3
SD_CMD 2 CMD
3 VSS1
+3VCARD 4 VDD
SD_CLK 5 CLK
6 VSS2
SD_D0 7 DAT0
SD_D1 8 DAT1
SD_D2 9 DAT2
SD_WP 10 W/P
SD_CD# 11 C/D
12 GND
13 GND
14 GND
15 GND

CARDREADER CONN
P/N update

+3VCARD

C854 0.1U/10V_4
C866 *0.1U/10V_4
C844 10U/6.3V_8

CLOSE CONN

Reserve for EMI

SD_D0	C1049	*5.6P/16V_4
SD_D1	C586	*5.6P/16V_4
SD_D2	C610	*5.6P/16V_4
SD_D3	C1050	*5.6P/16V_4
SD_CLK	C1100	*5.6P/16V_4

Close to CN8

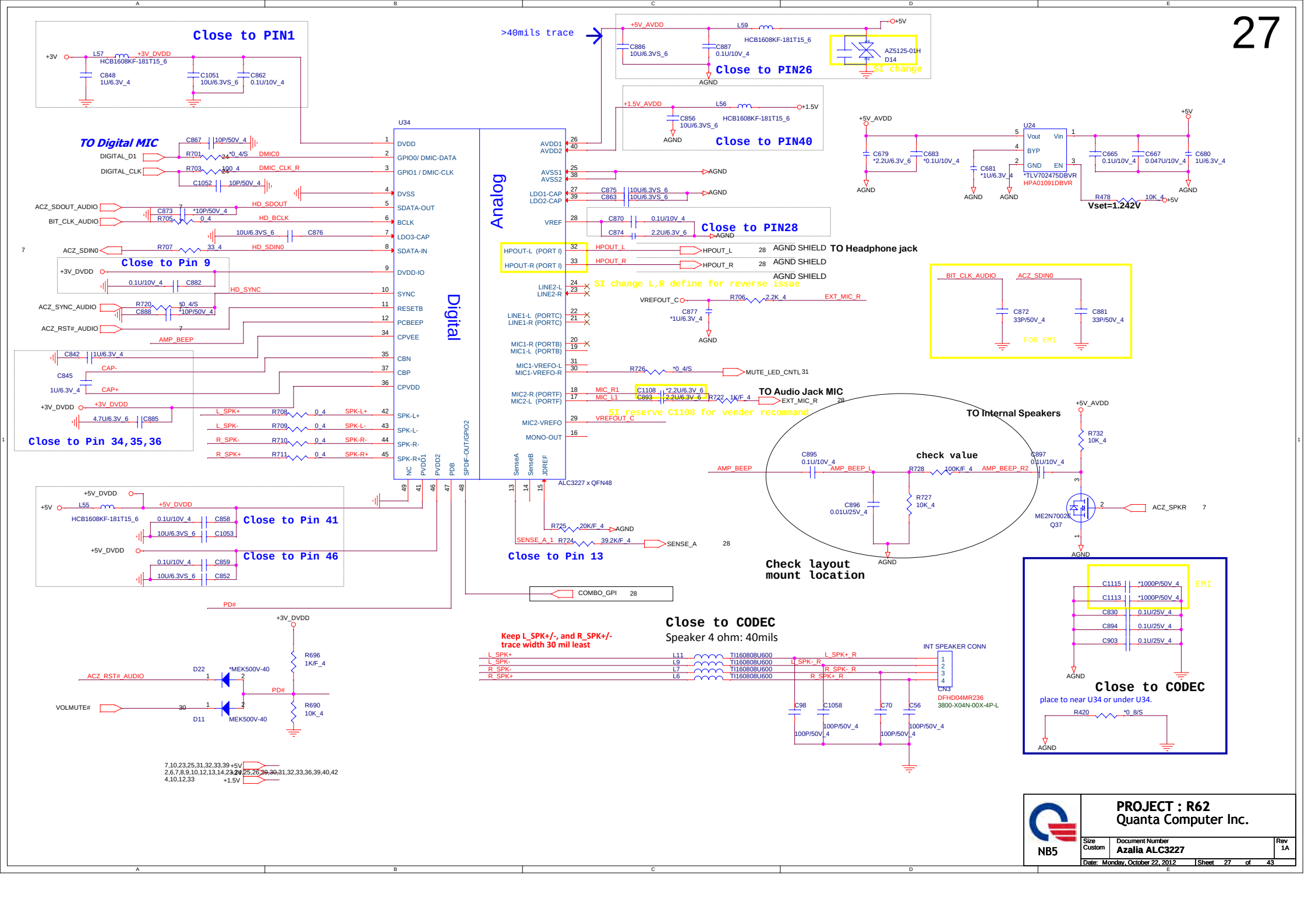
2,6,7,8,9,10,12,13,14,23,24,25,27,29,30,31,32,33,36,39,40,42

PROJECT : R62
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	RTS5229 & CR SOCKET	1A

Date: Monday, October 22, 2012 Sheet 26 of 43


Close to PIN1
>40mils trace
Close to PIN26
SI change
Close to PIN40
TO Digital MIC
Close to Pin 9
Close to Pin 34,35,36
Close to PIN28
TO Headphone jack
AGND SHIELD
SI change L,R define for reverse issue
TO Audio Jack MIC
SI reserve C1108 for vender recommand
TO Internal Speakers
check value
Check layout
mount location
Close to Pin 41
Close to Pin 46
Close to Pin 13
Close to CODEC
Speaker 4 ohm: 40mils
Keep L_SPK+/-, and R_SPK+/-
trace width 30 mil least
Close to CODEC
place to near U34 or under U34.
Vset=1.242V
U34
Analog
Digital
ALC3227 x QFN48
INT SPEAKER CONN
CN3
DFHD04MR236
3800-X04N-00X-4P-L
ME2N7002E
Q37
MEK500V-40
*TLV702475DBVR
HPA01091DBVR
PROJECT : R62
Quanta Computer Inc.
NB5
Size Custom
Document Number
Azalia ALC3227
Rev 1A
Date: Monday, October 22, 2012
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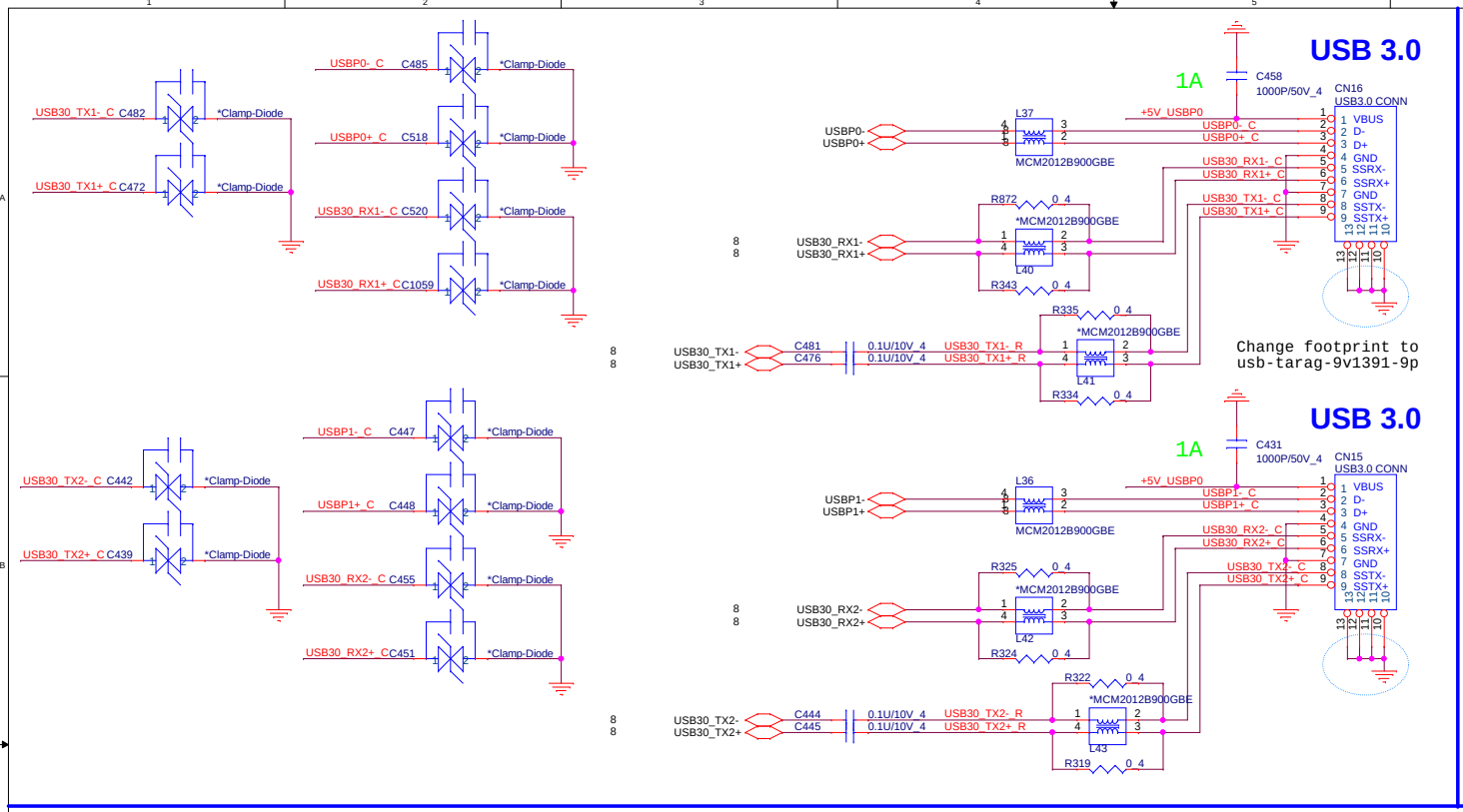
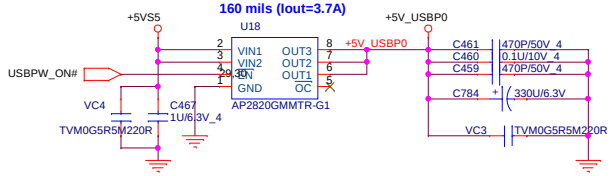
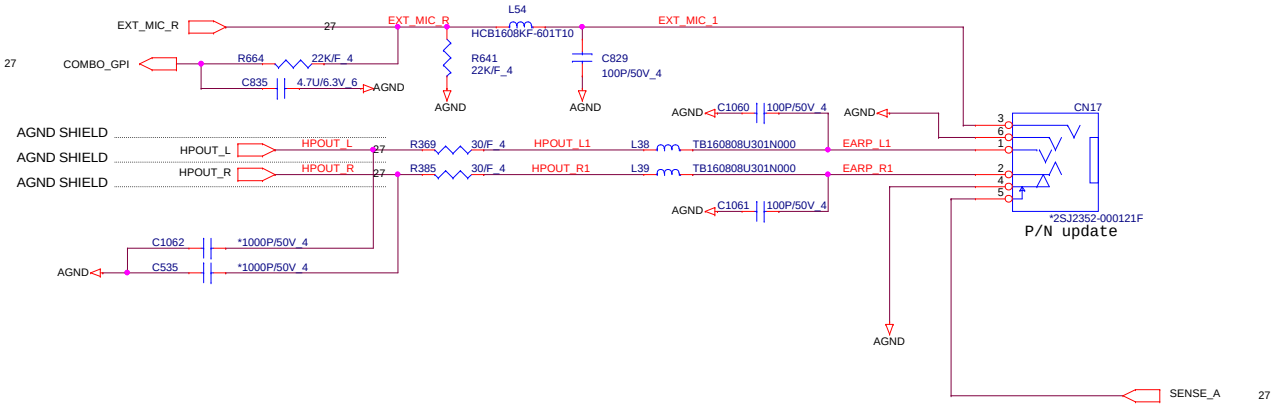


USB3.0 X 2/USB2.0 COMBO



COMBO JACK



10,29,33,35,36,37,38,39,40,41,42,43
2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42
25,29,39 +3VLANVCC

NB5	PROJECT : R62 Quanta Computer Inc.		
	Size: Custom	Document Number: USB/BT/Audio JacK	Rev: 1A
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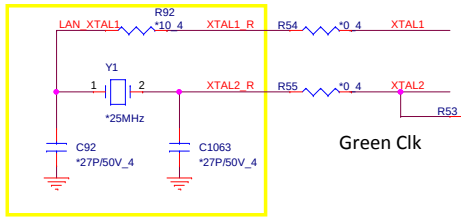
SI DEL reserve parts

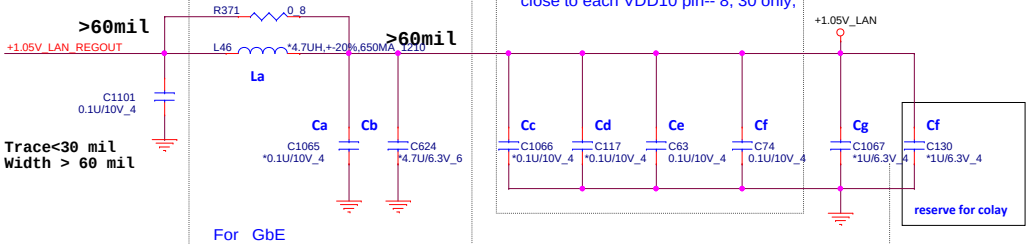


Green Clk

For GbE
* Place Cc,Cd,Ce,Cf close to each VDD10 pin-- 3, 22, 8 , 30

For 10/100 NA Ce,Cf
* Place Ce , Cf close to each VDD10 pin-- 8, 30 only,

Power trace Layout 寬度> 60mil



For GbE
Stuff La, Ca ,Cb

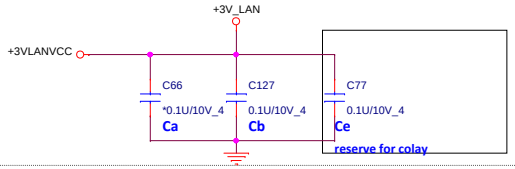
For 10/100
NA: La, Ca ,Cb

For GbE
* Place Cf close to each VDD10 pin-- 22 (reserve)

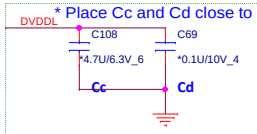
For 10/100
* Place Cg close to each VDD10 pin-- 30 (reserve)

For 10/100
* Stuff Ca and Ce only, close to each VDD33 pin-- 23, 32

For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



* Place Cc and Cd close to each VDD33 pin-- 23

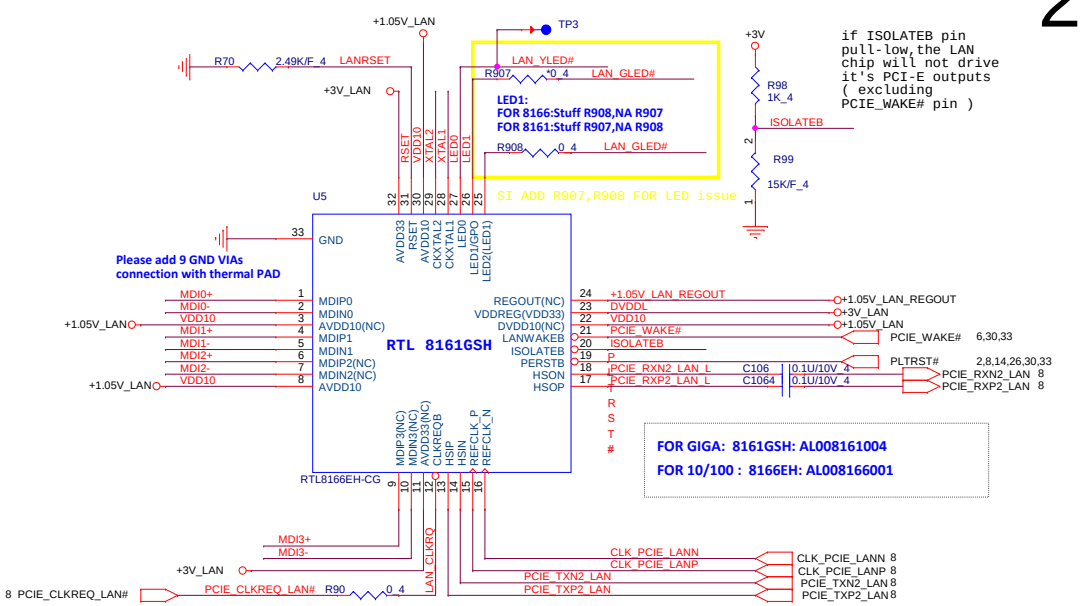


For GIGA
Stuff Cc ,Cd

For 10/100
NA: Cc, Cd

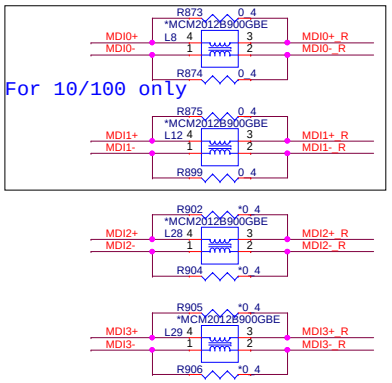
Remove For Not Using SWR mode

2,6,7,8,9,10,12,18,14,23,24,25,26,27,30,31,32,33,36,39,40,42
25,39 +3VLANVCC

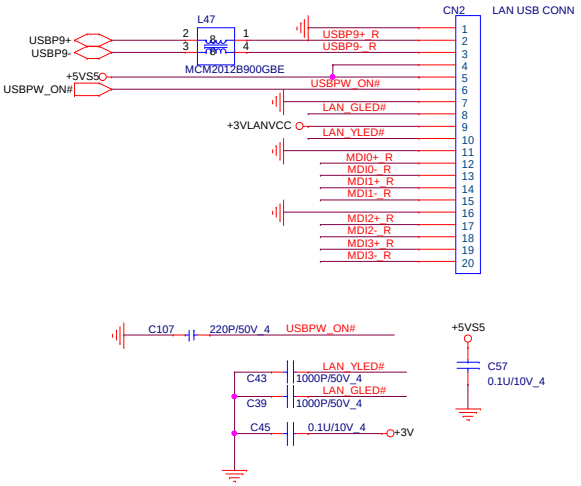


FOR GIGA: 8161GSH: AL008161004
FOR 10/100 : 8166EH: AL008166001

Right SIDE USBX1 and LAN CONN

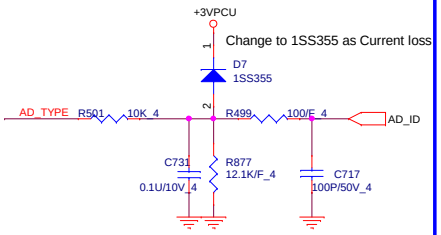


28,30

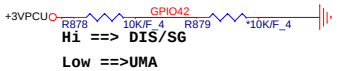


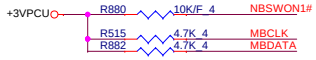
NB5	PROJECT : R62 Quanta Computer Inc.		
	Size: Custom	Document Number: RTL 8105E/RJ45	Rev: 1A
	Date: Monday, October 22, 2012	Sheet 29 of 43	

adapter Type check

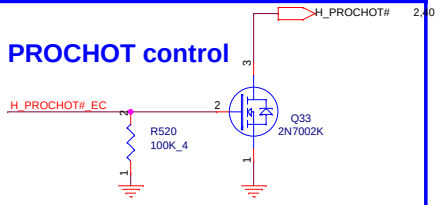


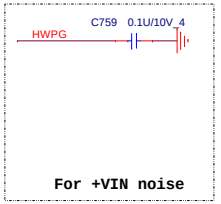
adapter select for EC

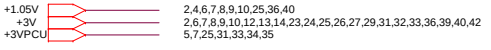


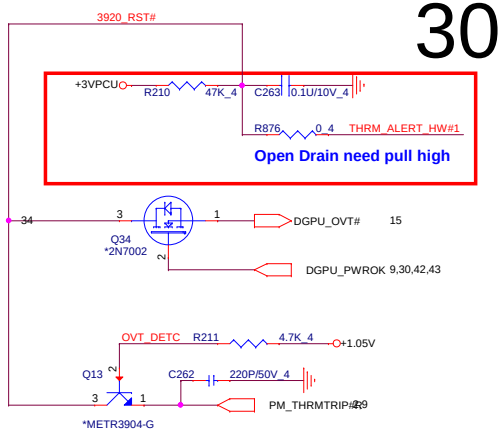


PROCHOT control

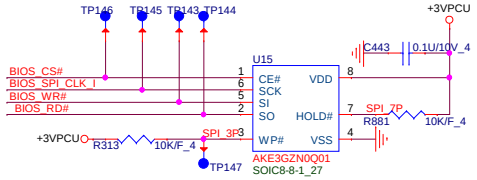




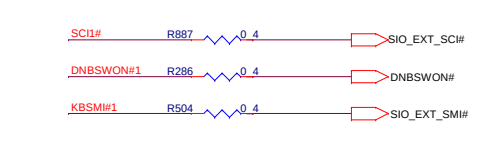


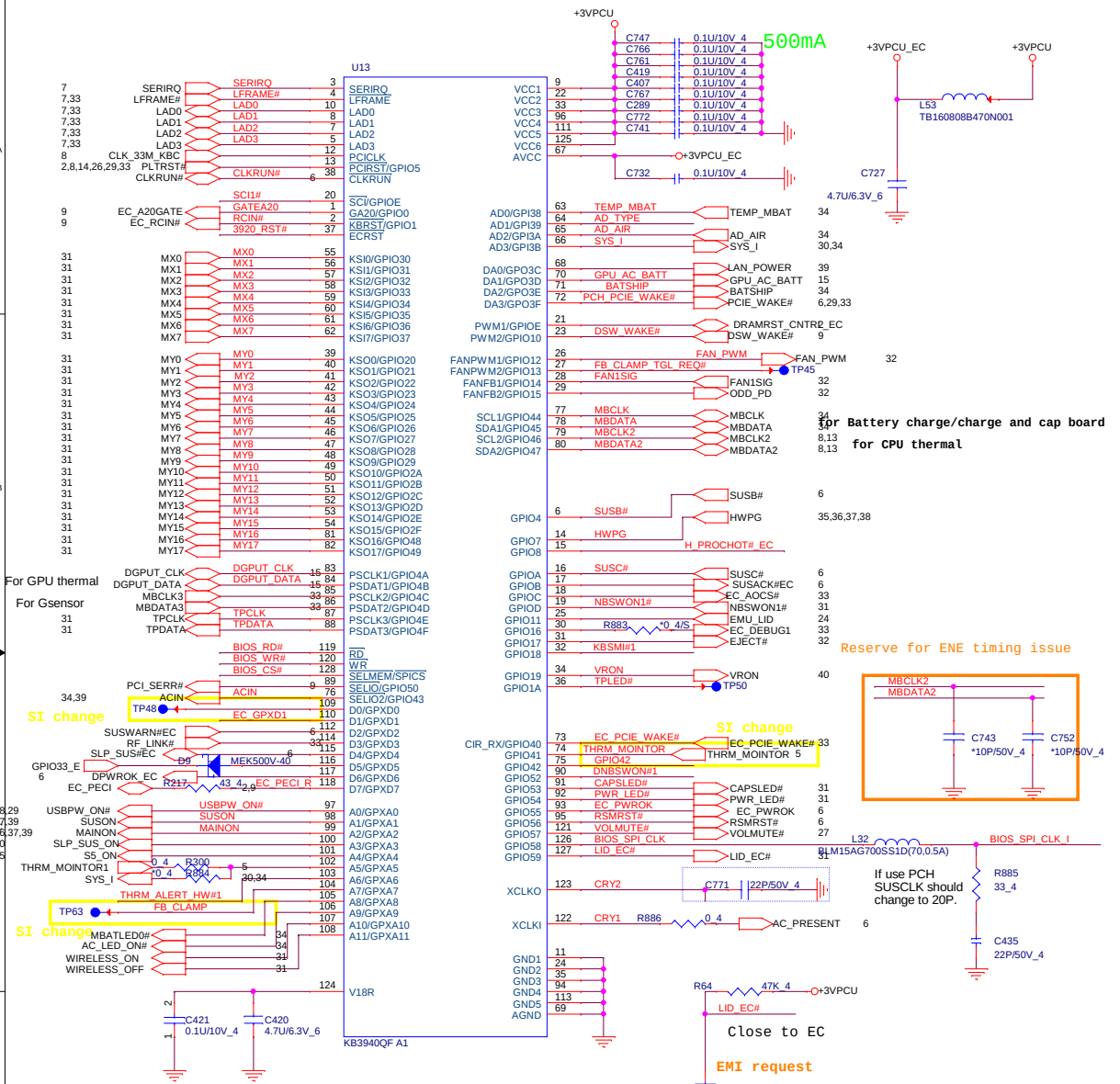


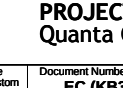
1M byte SPI EC ROM



Vender	Size	P/N
EON	1MB	AKE3GZN0Q01 (EN25Q80A-100HIP)
GigaDevice	1MB	AKE3GGN0Q00 (GD25Q80BSIGR)
AMIC	1MB	AKE3GZP0801 (A25L080M-F)
Socket		DFHS08FS023







PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC (KB3940 A1)/ROM	1A

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KEYBOARD Con.

30 MY[0..17] MY[0..17]
30 MX[0..7] MX[0..7]

KB CONN 50698-03201-001-32p-l
DFFC32FR035

MX1 MX7 MX6 MY9 MX4 MX5 MY0 MX2 MX3 MY5 MY1 MX0 MY2 MY4 MY7 MY8 MY6 MY3 MY12 MY13 MY14 MY11 MY10 MY15 MY16 MY17 → CN6

P/N update

SATA_LED

C902 *AVLC 5S
SATA_LED# → SATA_LED#
ACC_LED# → R733 200/F_6
SATA_R_LED1 R734 39_6 +3V
LED2 LED 3P WHITE/AMBER (Amber)
C899 *AVLC 5S

KEYBOARD PULL-UP

RP2: +3VPCU, MY6, MY3, MY12, MY13 → MY15, MY10, MY11, MY14 *10P8R-8.2K
RP1: +3VPCU, MY9, MY0, MY5, MY1 → MY8, MY7, MY4, MY2 *10P8R-8.2K
R173 *8.2K_4 MY16
R176 *8.2K_4 MY17

MY5 C109 *220P/50V_4
MY6 C142 *220P/50V_4
MY3 C145 *220P/50V_4
MY7 C1070 *220P/50V_4
MY8 C141 *220P/50V_4
MY9 C76 *220P/50V_4
MY10 C173 *220P/50V_4
MY11 C169 *220P/50V_4
MY1 C128 *220P/50V_4
MY2 C136 *220P/50V_4
MY4 C139 *220P/50V_4
MY0 C1071 *220P/50V_4
MX4 C82 *220P/50V_4
MX6 C73 *220P/50V_4
MX3 C104 *220P/50V_4
MX2 C97 *220P/50V_4
MX7 C1072 *220P/50V_4
MX0 C1073 *220P/50V_4
MX5 C90 *220P/50V_4
MX1 C1074 *220P/50V_4
MY12 C1075 *220P/50V_4
MY13 C152 *220P/50V_4
MY14 C1076 *220P/50V_4
MY15 C190 *220P/50V_4
MY16 C201 *220P/50V_4
MY17 C206 *220P/50V_4

CAPSLED# R185 R191 200/F_6 +3V
CAPSLED#_R MUTE_LED_CNTL_R WIRELESS_ON_R WIRELESS_OFF_R

MUTE_LED_CNTL → Q6 2N7002K R147 10K/F_4

SI, add Mute LED feature

EC KB3930 has included K/B pull-up resistor and function

WIRELESS_ON → R195 *200/F_6 → Q52 DRC5144E0L; R196 1K/F_4 +5V; R218 *200/F_6 +3V; WIRELESS_ON_R
WIRELESS_OFF → R208 *200/F_6 → Q9 DRC5144E0L; R199 1K/F_4 +5V; WIRELESS_OFF_R

PWR_LED

+3VPCU → R440 360_4 → LED1 3P WHITE LED → C601 *AVLC 5S → DEEP_PWRLED#
C1077 SATA_LED# 1000P/50V_4
C604 DEEP_PWRLED# 1000P/50V_4

POWER BOTTON CONNECT

100mA
C116 *4.7U/6.3V_6
C114 1U/10V_4
C113 0.1U/10V_4
+3VPCU
30 LID_EC#
30 NBSWON1#
PWR_LED# R116 *0_4 30,31
DEEP_PWRLED# R117 0_4
PWR_LED1#
CN4 → PWR BTN CONN
DFFC06MR001
88513-0601-6P-L-SMT

1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

C110 PWR_LED# *0.1U/10V_4
C112 LID_EC# 0.1U/10V_4
C111 NBSWON1# 0.1U/10V_4

+3VPCU R120 10K/F_4
Q5 DRC5144E0L
PWR_LED# 30,31
C135 0.1U/10V_4
DEEP_PWRLED# → for EC into Deep Sleep in S3 Mode

TOUCH PAD Con.

+3VSUS R890 4.7K_4 TP_SMB_CLK
R323 4.7K_4 TP_SMB_DATA

change to +3VSUS
close conn

+3VSUS R891 4.7K_4 TPCLK
R892 4.7K_4 TPDATA

TPCLK C429 10P/50V_4 L34 TB160808B470N001 TPCLK-1
TPDATA L33 TB160808B470N001 TPDATA-1 C428 10P/50V_4
TP_SMB_DATA
TP_SMB_CLK
CN7 → TOUCH PAD CONN
DFFC06MR001
88513-0601-6P-L-SMT

25 mils

C880 *10P/50V_4
C878 *10P/50V_4
+3VSUS C430 0.1U/10V_4

Change footprint to 88513-0601-6P-L-SMT

+3VSUS
Q19 *2N7002DW
TP_SMB_CLK → SMB_PCH_CLK 8
TP_SMB_DATA → SMB_PCH_DAT 8

PV , HP request Image sensor
SMBUS reserve to PCH

+3VPCU 5,7,25,30,33,34,
+5V 7,10,23,25,27,32
+3VSUS 39
+3V 2,6,7,8,9,10,12,1
27,29,30,32,33,36,39,40,42

NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A

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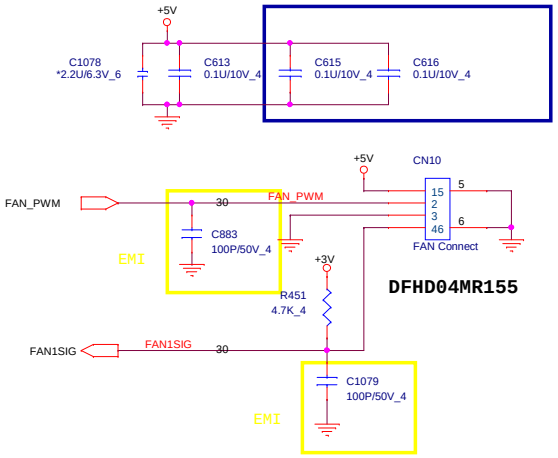
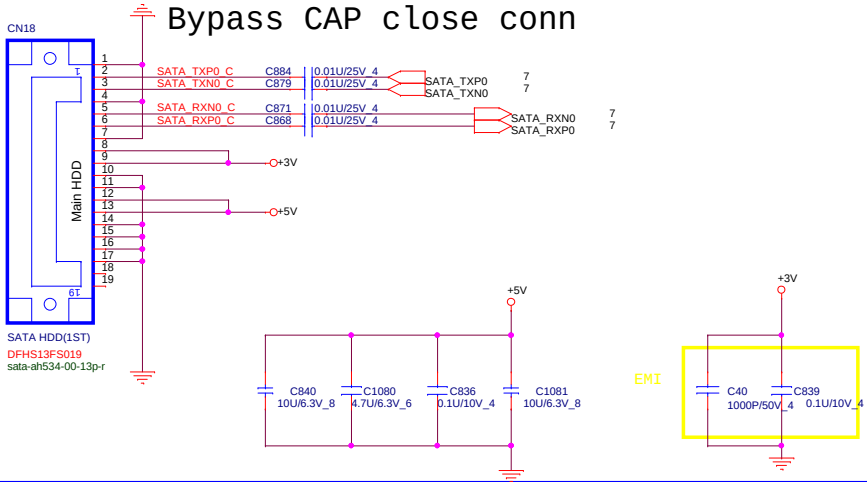
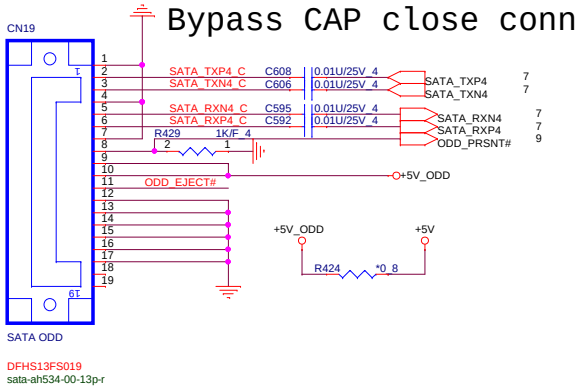
CPU FAN

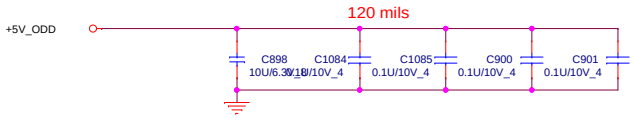


SATA HDD CONNECTOR

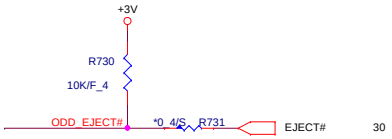


SATA ODD CONNECTOR

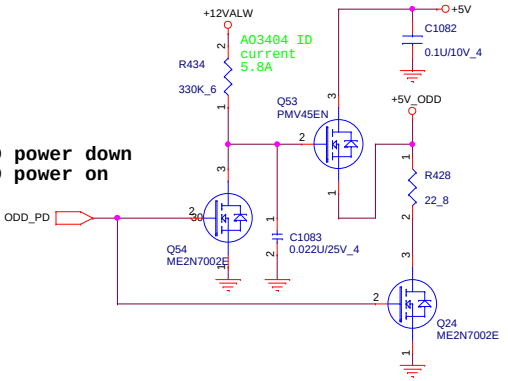




follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on



+3V	2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,33,36,39,40,42
+3VPCU	5,7,25,30,31,33,34,35
+5V	7,10,23,25,27,31,33,39
+12VALW	34,39,43

NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A

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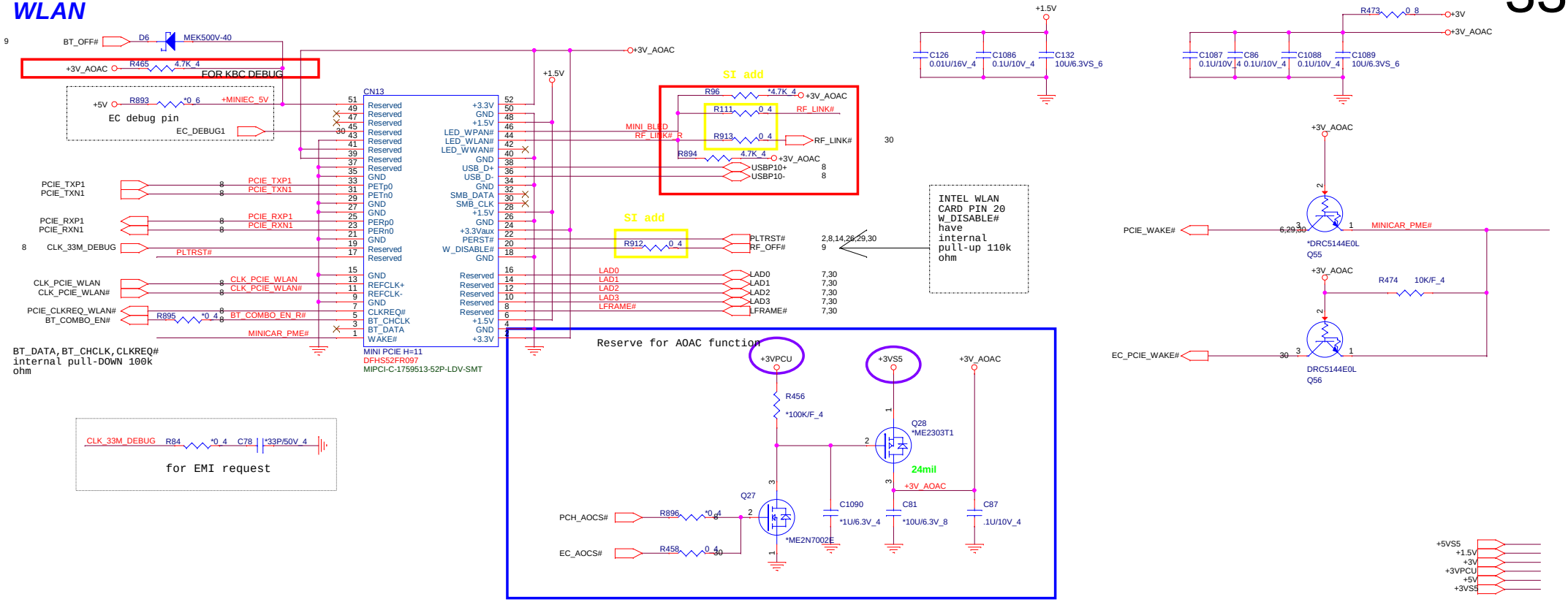
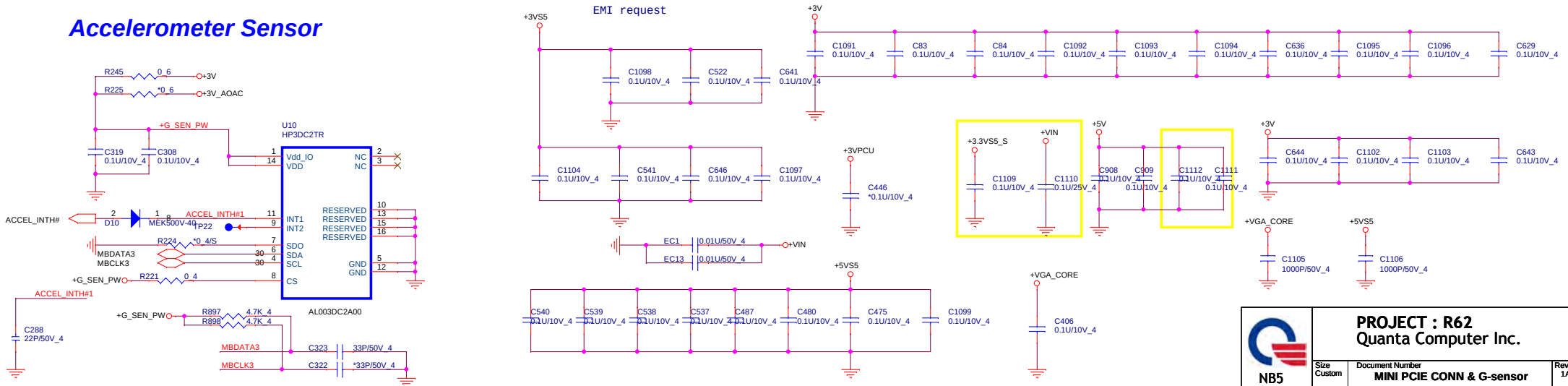
Mini PCI-E Card 1
WLAN



Accelerometer Sensor



NB5	PROJECT : R62 Quanta Computer Inc.
Size: Custom	Document Number: MINI PCIE CONN & G-sensor
Rev: 1A	
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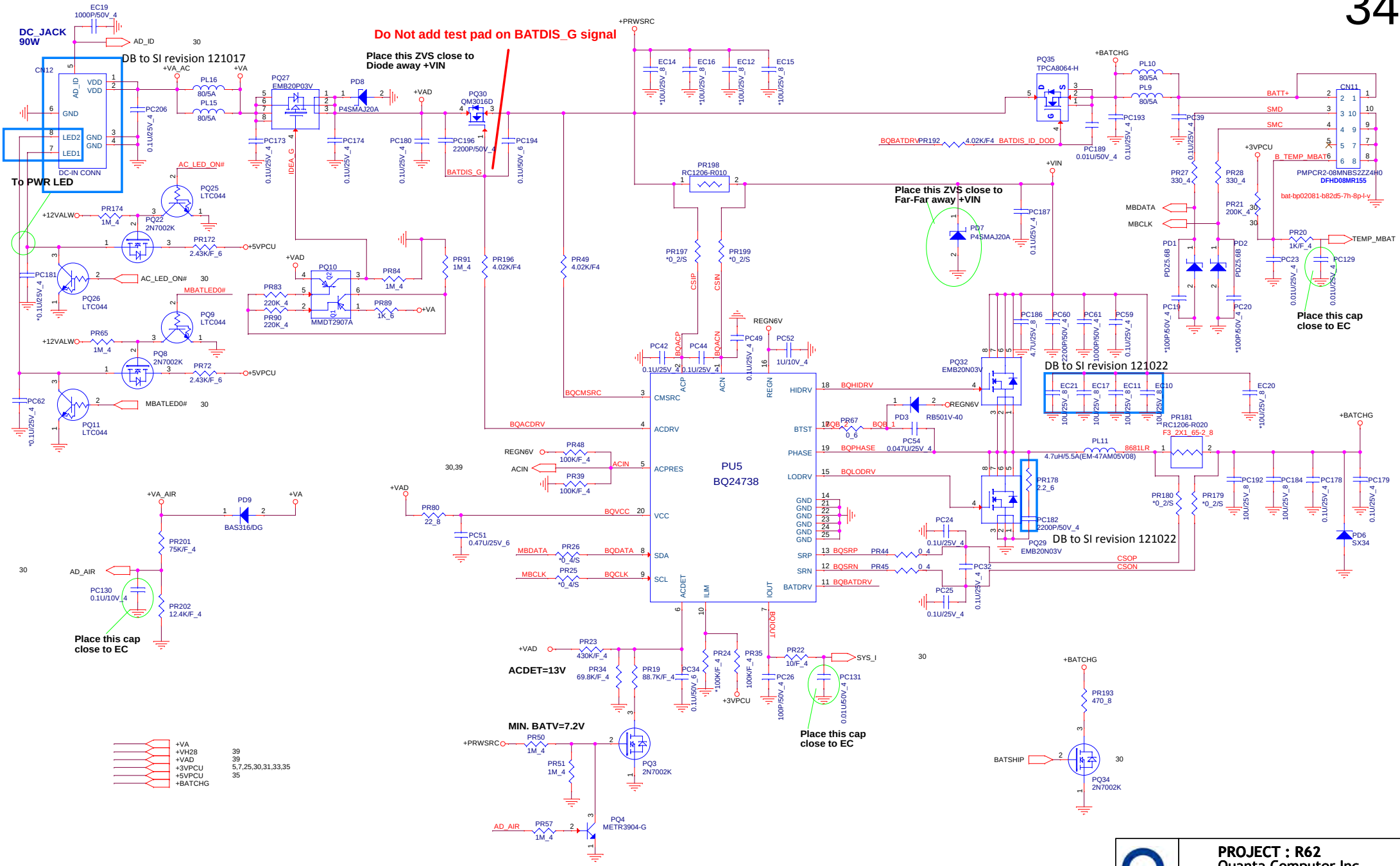
DC_JACK 90W
DB to SI revision 121017
To PWR LED
Do Not add test pad on BATDIS_G signal
Place this ZVS close to Diode away +VIN
Place this ZVS close to Far-Far away +VIN
Place this cap close to EC
DB to SI revision 121022
PU5
BQ24738
ACDET=13V
MIN. BATV=7.2V
+VA
+VH28 39
+VAD 39
+3VPCU 5,7,25,30,31,33,35
+5VPCU 35
+BATCHG
NB5
PROJECT : R62
Quanta Computer Inc.
Size Custom
Document Number Charger (OZ8681)
Rev 1A
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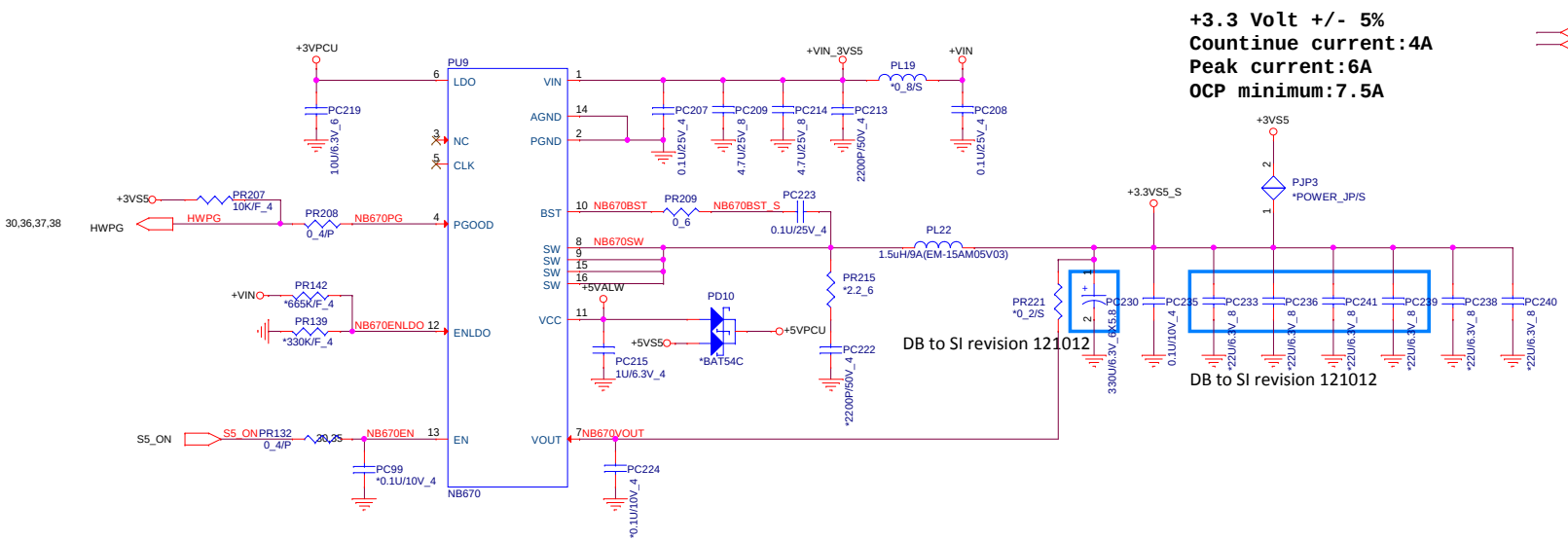
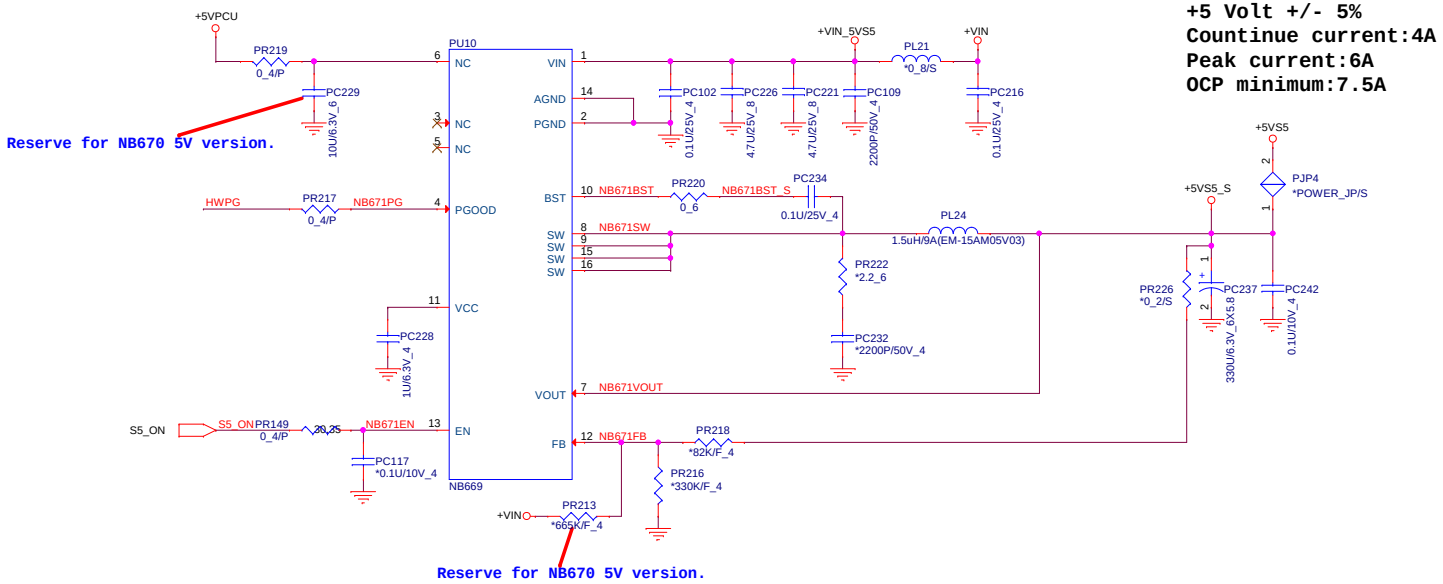
DC/DC +3VS5/+5VS5





NB5	PROJECT : R62 Quanta Computer Inc.		
	Size: Custom	Document Number: 3/5VPCU(RT8243A)	Rev: 1A
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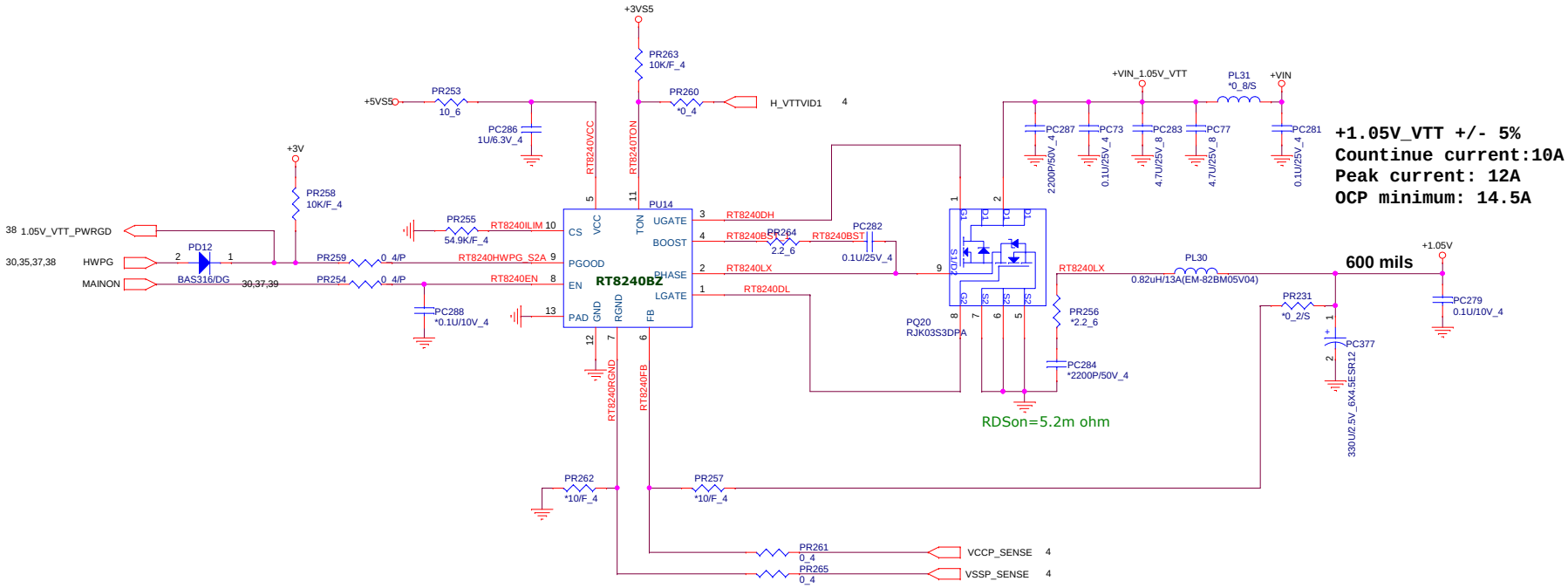

+1.05V 2,4,6,7,8,9,10,25,30,40

NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.05V(RT8228BZ)	1A

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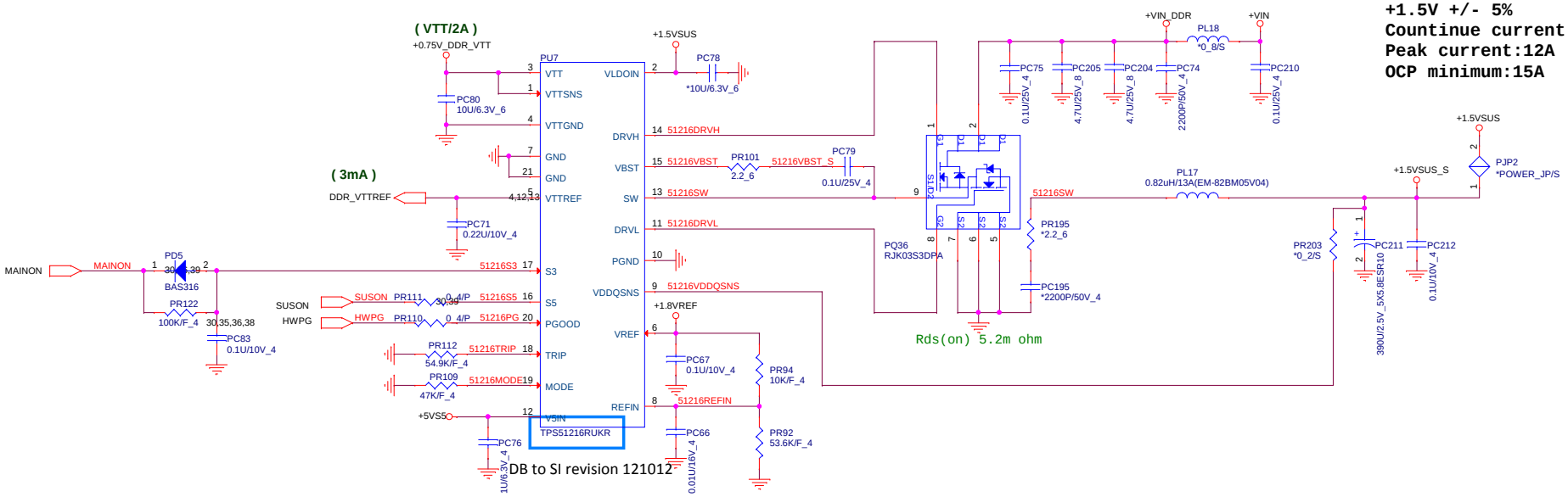
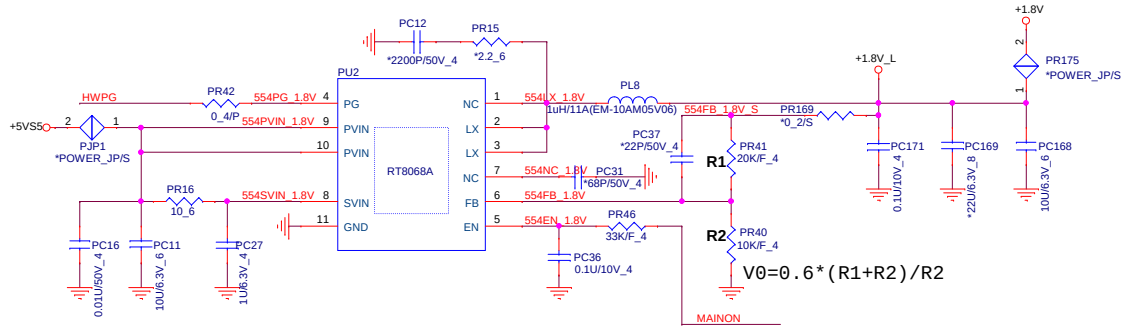
+1.5VSUS 2,4,12,13,43

+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCP minimum:15A



1.8V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A



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Quanta Computer Inc.

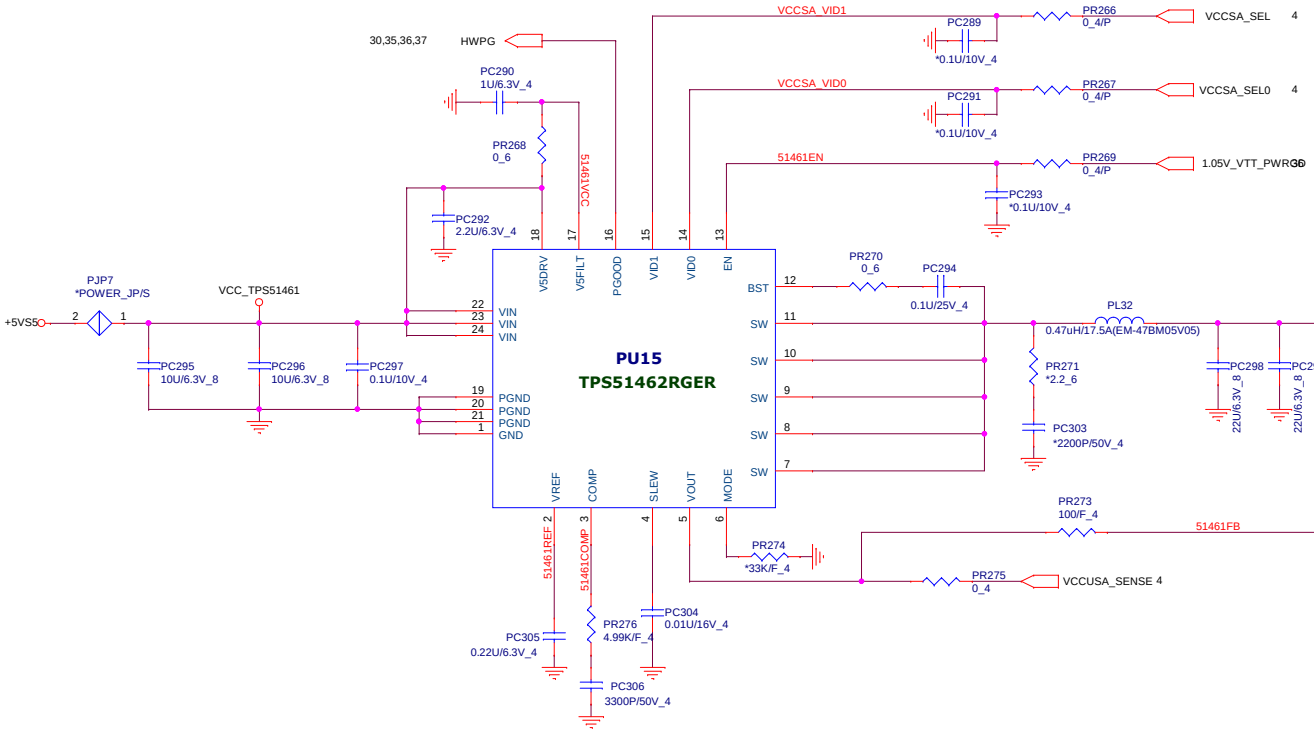
NB5

Size	Document Number	Rev
Custom	DDR3L(APW8819)	1A
Date: Monday, October 22, 2012	Sheet 37 of 43	

TPS51462RGER/AL051462000

For CPU SV system agent voltage slew rate of 0.5 -10 mV/µs

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



+VCCSA Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7A

NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3L(APW8819)	1A
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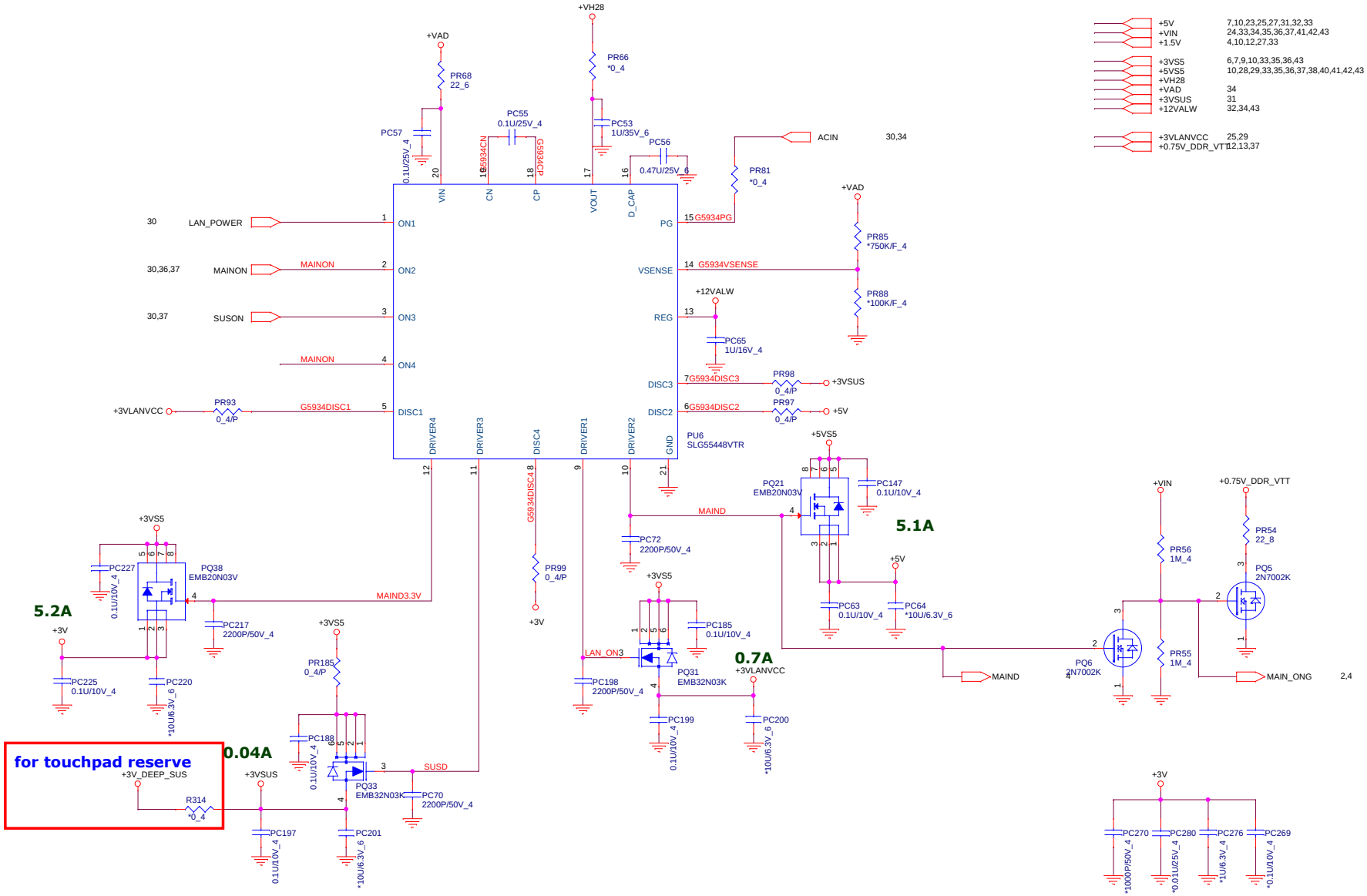

PROJECT : R62		
Quanta Computer Inc.		
NB5	Size: Custom	Document Number: Dis-charge IC (G5934)
	Rev: 1A	
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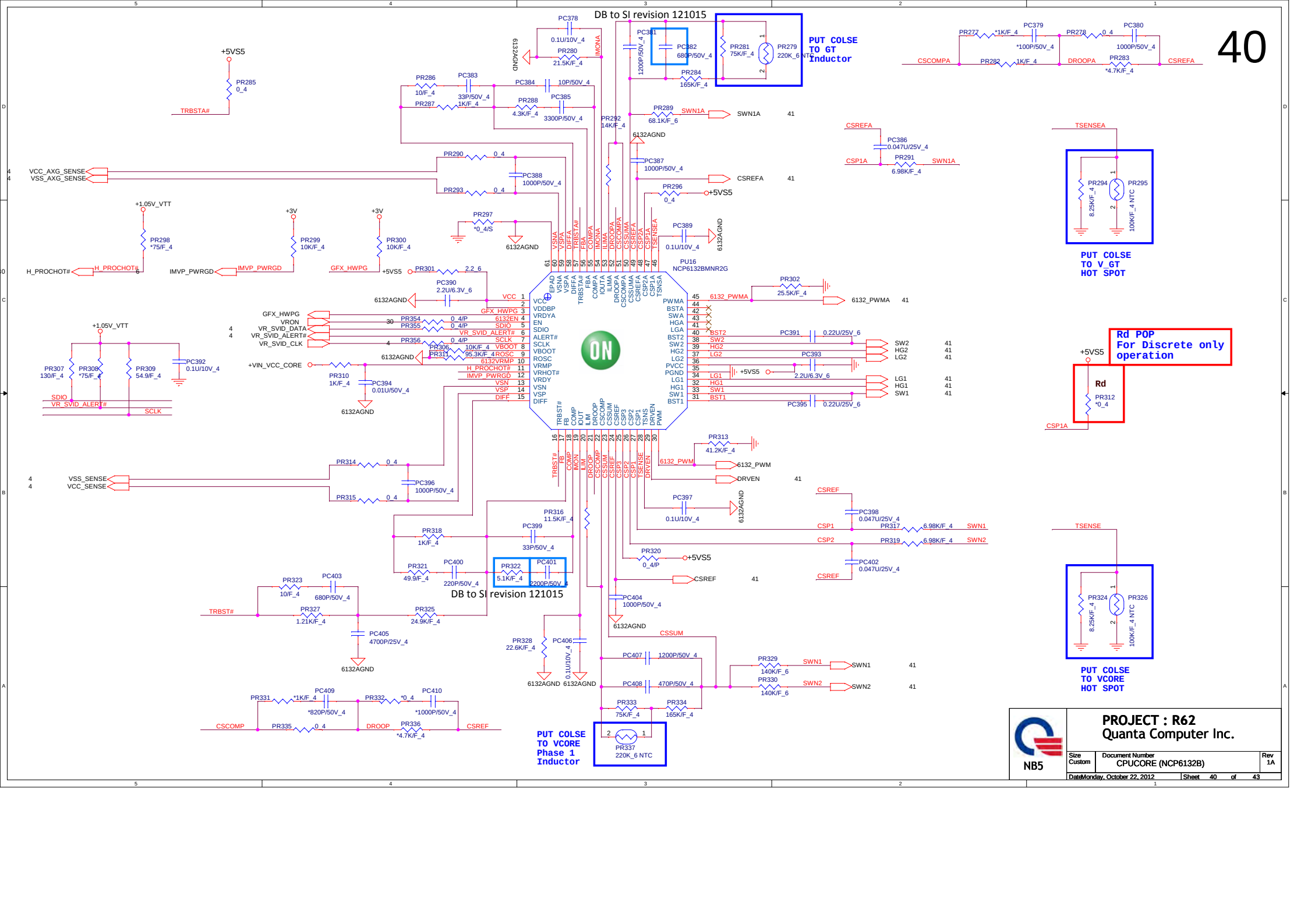
DB to SI revision 121015
PUT COLSE TO GT Inductor
PUT COLSE TO V_GT HOT SPOT
Rd POP For Discrete only operation
PUT COLSE TO VCORE HOT SPOT
PUT COLSE TO VCORE Phase 1 Inductor
PU16 NCP6132BMNR2G
DB to SI revision 121015
40
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NB5
CPUCORE (NCP6132B)
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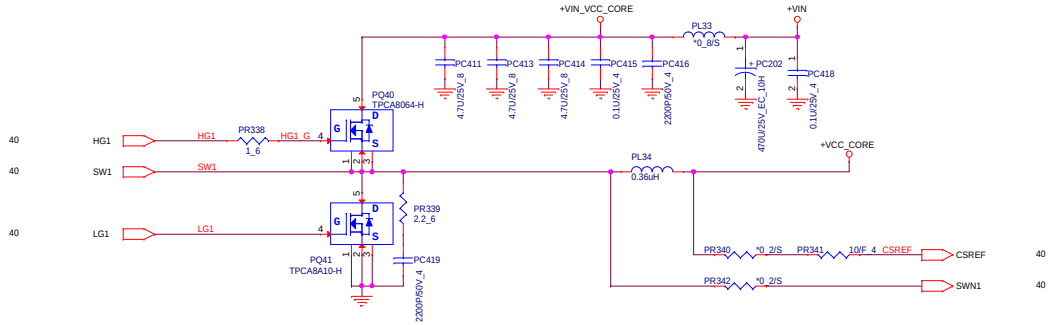
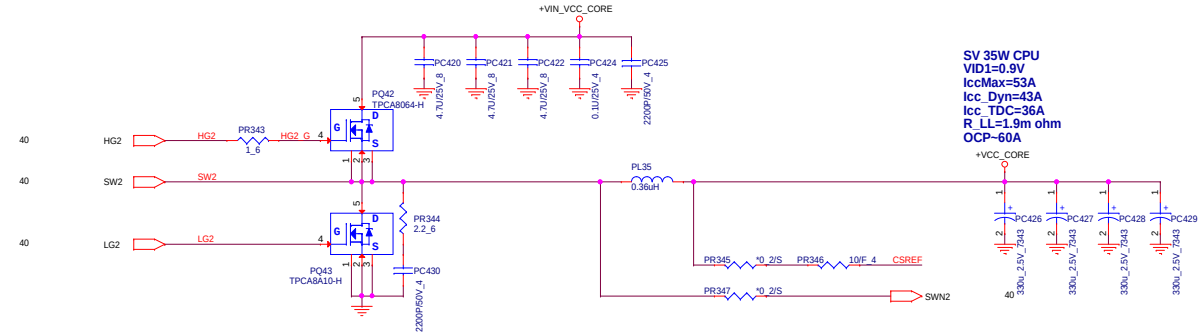
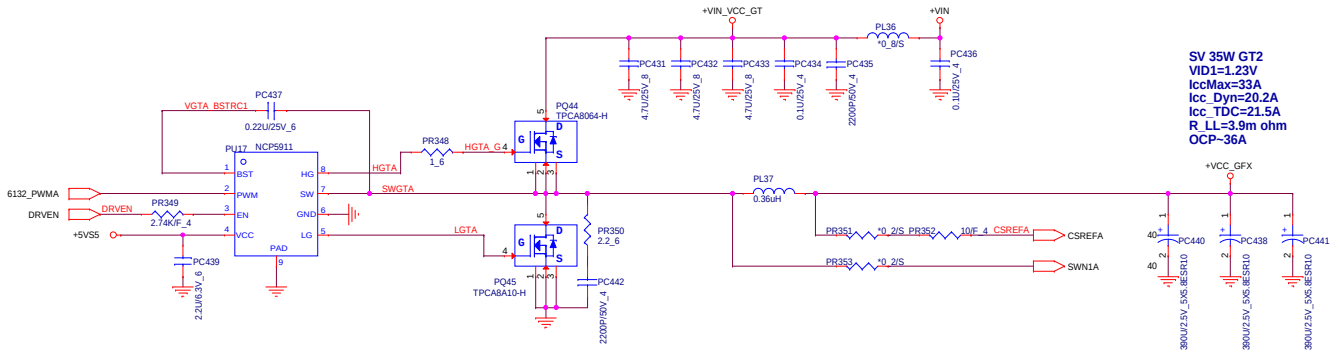




SV 35W CPU
VID1=0.9V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~60A



SV 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~36A

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VGA Core

GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

+VGA_CORE 18,33,43

42

Mars (25W)

+VGA_CORE
Countinue current: 25A
Peak current: 30A
OCP minimum: 33A
L-L: 0mV/A

DCR_1.4m ohm

DB to SI revision 121018

DB to SI revision 121015

DB to SI revision 121022

DCR_1.4m ohm

DB to SI revision 121022

DB to SI modify on 1008

DB to SI revision 121012

DB to SI revision 121015

This NTC Close to Phase 1 MOSFET

Close to Phase 1 Inductor

Shortest the net trace

PU8
NCP3218G

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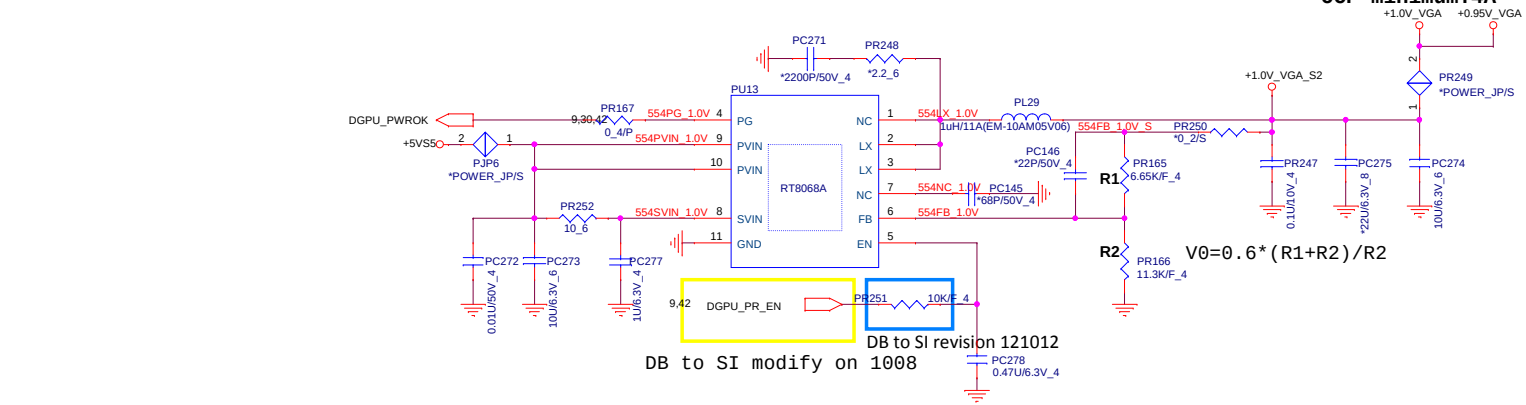
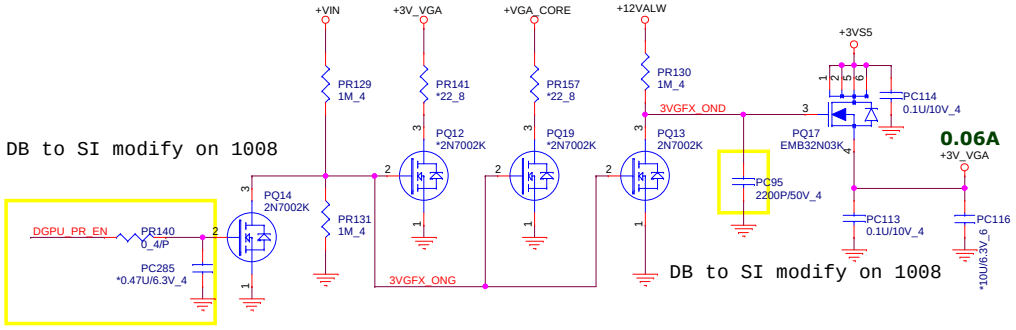
R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V

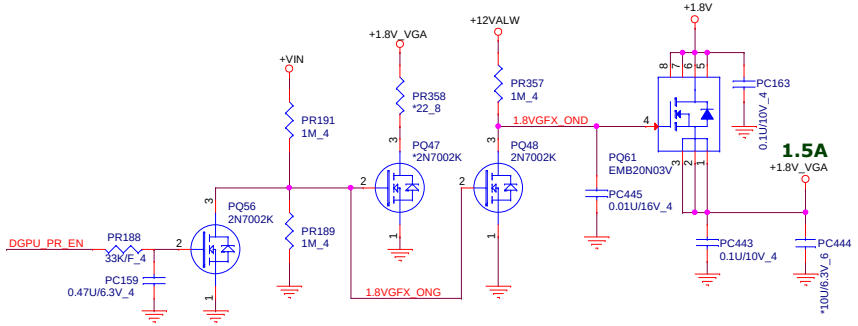
+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A

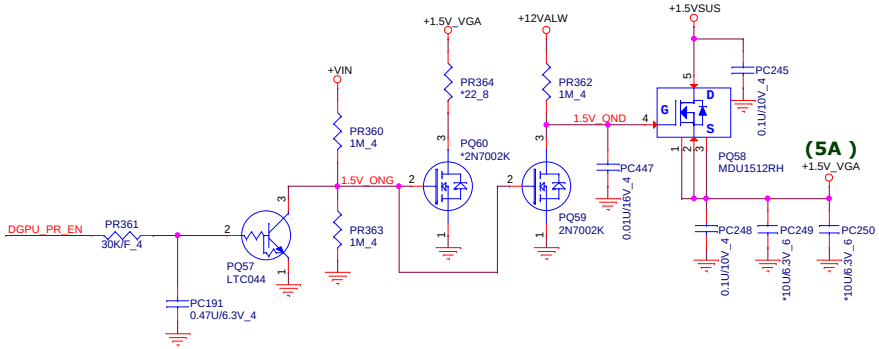


DB to SI modify on 1008



DB to SI modify on 1008





+1.8V_VGA 15,16,18,19,25
+1.0V_VGA 14,16,18,19
+3V_VGA 18

NB5

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