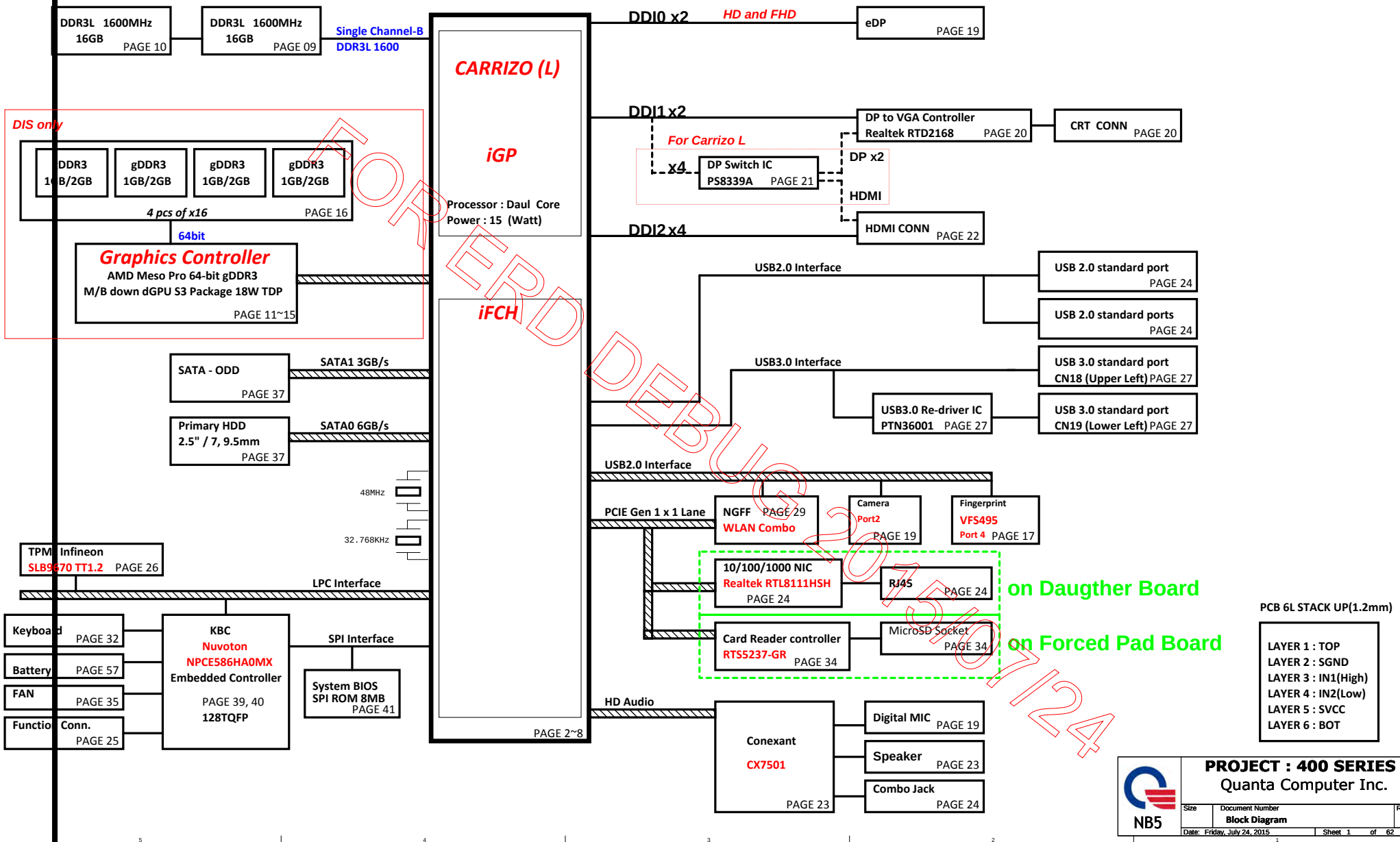
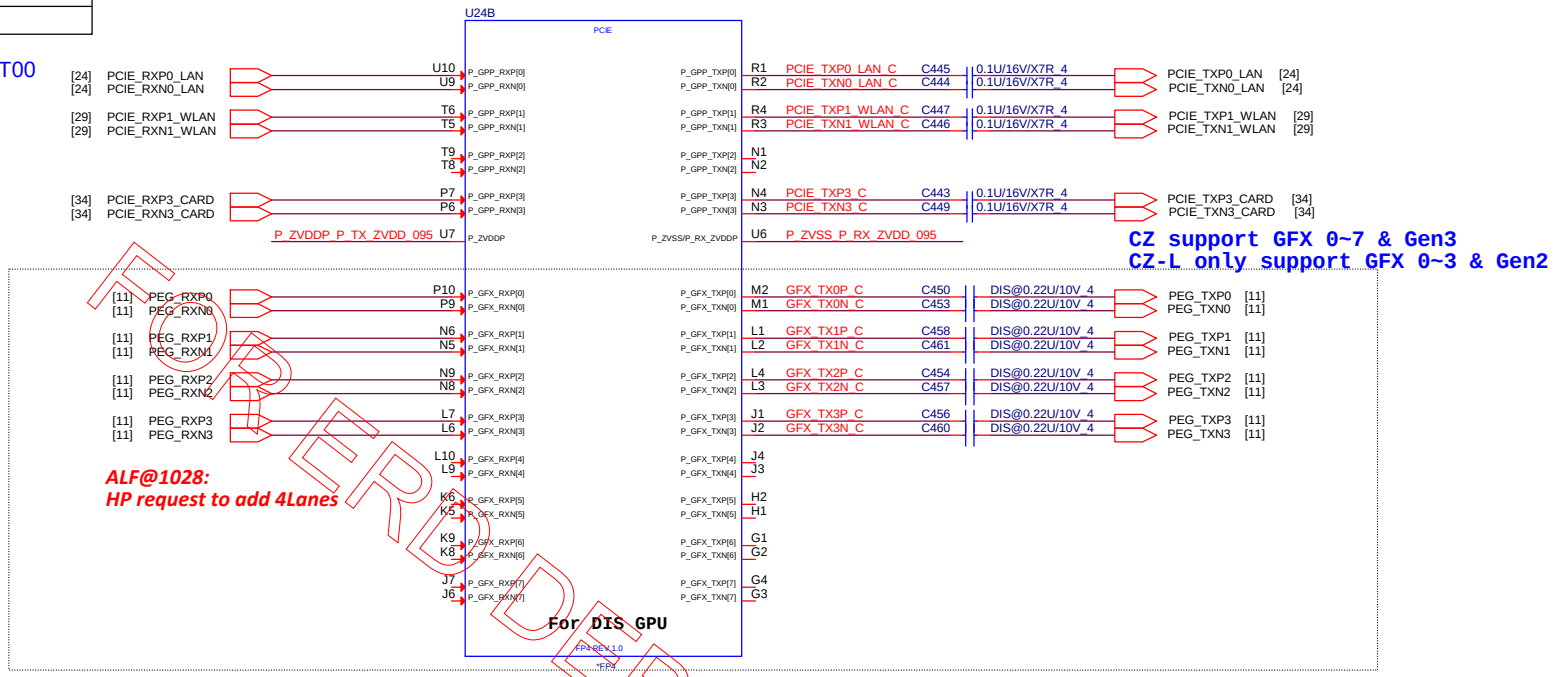
400 series Palazzo / X73A (UMA/DIS) Schematics

01

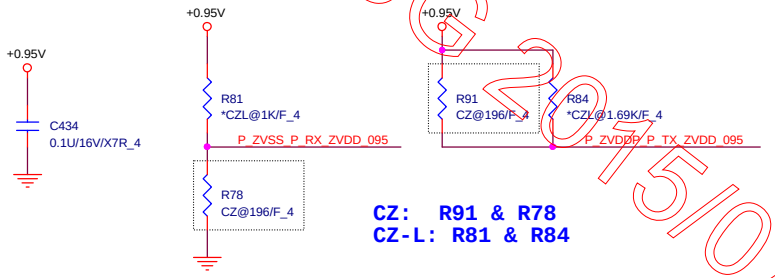


	QBCON	TOPBSQ
Carrizo	AJ1802CUT01	AJ1802CUT02

Carrizo DB phase use AJ1802CUT00



Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4103K1B08



NB5

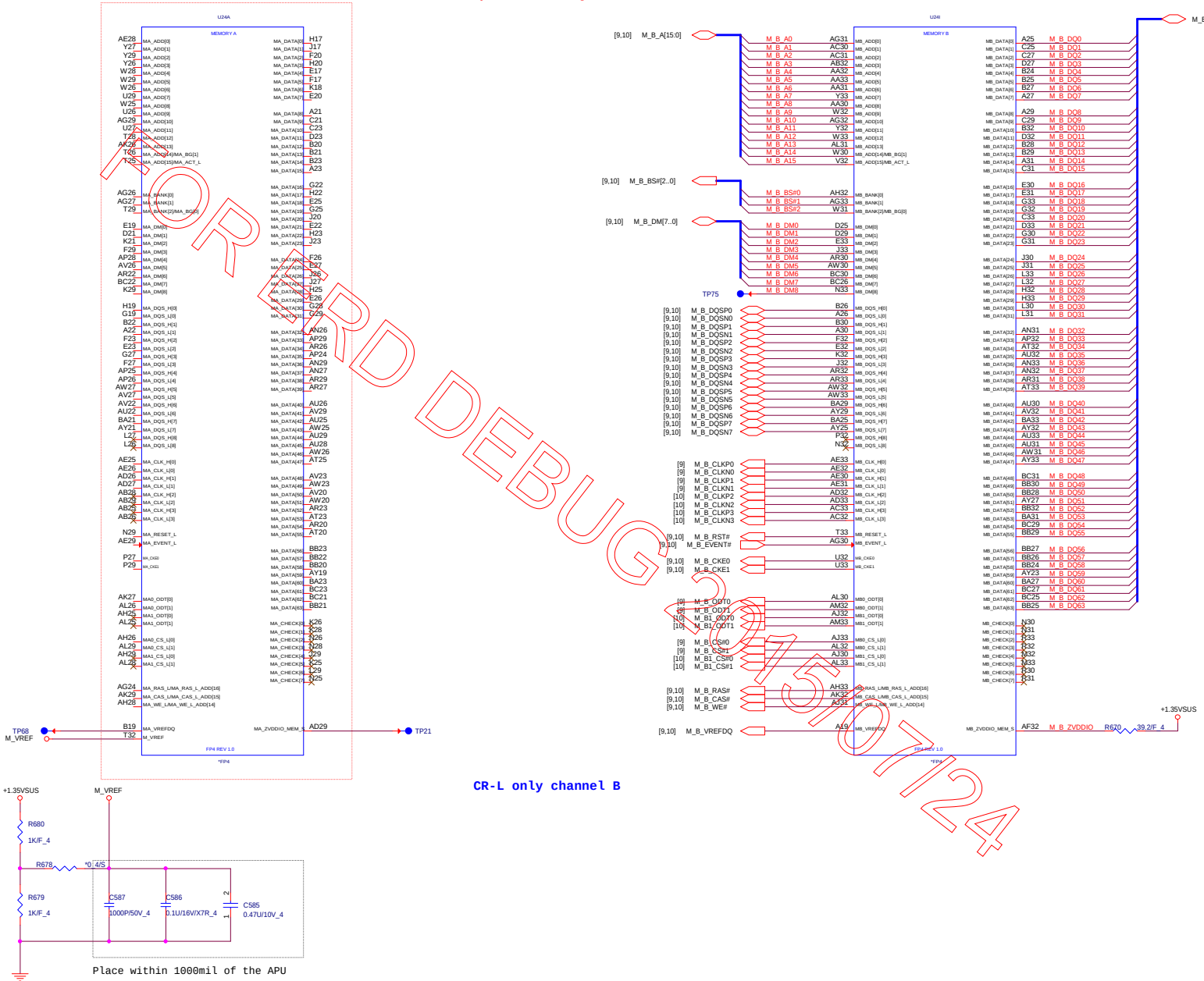
PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
	Carrizo 1/7 (PCIE)	1A

Date: Friday, July 24, 2015 | Sheet 2 of 62

Ronny@1013:
2 So-Dimm per Channel (B)

1013@RNY: Also need to check AMD whether it can float ot not?
1102@RNY: AMD recommend reserve test point at VREFDQ/ZVDDIO_MEM_S



NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
	Size:	Document Number: Carrizo 2/7 (MEM) Rev: 1A
	Date: Friday, July 24, 2015	Sheet 8 of 62

+1.8V
R198 301/F_4 APU_RST#
R242 301/F_4 APU_PWROK

CZ18V_CZL30V
R181 1K/F_4 APU_PROCHOT#
R523 1K/F_4 APU_ALERT#
R549 1K/F_4 APU_SIC
R548 1K/F_4 APU_SID

+3V CZ18V_CZL30V
R169 R2 *CZL@0_4
+1.8V
R176 R1 CZ@0_4

CZ: R1
CZ-L: R2

1016: Alfred
Swap the DDI Port frm DDI2 to DDI1.
CZ only

HDMI
[21] IN_D2 / [21] IN_D2#
[21] IN_D1 / [21] IN_D1#
[21] IN_D0 / [21] IN_D0#
[21] IN_CLK / [21] IN_CLK#

DP Switch or
DP to VGA Chip

eDP
[21] DDI1_TX0_P / [21] DDI1_TX0_N
[21] DDI1_TX1_P / [21] DDI1_TX1_N
[21] DDI1_TX2_P / [21] DDI1_TX2_N
[21] DDI1_TX3_P / [21] DDI1_TX3_N
[19] INT_eDP_TXP0 / [19] INT_eDP_TXN0
[19] INT_eDP_TXP1 / [19] INT_eDP_TXN1

U24C
DISPLAYSVID2/3T AGITEST

DP_ZVSS A9 — DP_ZVSS R458 2K/F_4
DP_AUX_ZVSS B9 — DP_AUX_ZVSS R451 150/F_4
DP_BLON G5 — APU_LVDS_BLON [19]
DP_DIGON G6 — APU_DISP_ON [19]
DP_VARY_BL F11 — APU_DPST_PWM [19]

CZ only
DP2_AUXP H9 — IN_DDC_SCL [21]
DP2_AUXN G9 — IN_DDC_SDA [21]
DP2_HPD E9 — IN_HPD [21]
DP1_AUXP F7 — INT_DDI1_AUXP [21]
DP1_AUXN E7 — INT_DDI1_AUXN [21]
DP1_HPD F5 — DDI1_HPD_CON [21]
DP0_AUXP F8 — INT_eDP_AUXP [19]
DP0_AUXN E8 — INT_eDP_AUXN [19]
DP0_HPD G8 — EDP_HPD [19]

RSVD_1 K24 CORETYPE — TP34
TEMPIN0 E15 APU_TEMPIN0 — TP17
TEMPIN1 E14 APU_TEMPIN1 — TP16
TEMPIN2 E12 APU_TEMPIN2 — TP64
TEMPINRETURN F14 APU_TEMPRETURN — R508 *0_4/S
TEST410 AK24 APU_TEST410
TEST411 AL24 APU_TEST411 — TP22
TEST4 P24 APU_THERMDA — TP23
TEST5 N24 APU_THERMDC — TP20
TEST6 AN24 APU_TEST6 — TP19
TEST9 AB8 APU_TEST9 — TP31
TEST10 Y9 APU_TEST10
TEST14 B10 APU_TEST14 — TP15 R446 *1K/F_4 — TP14
TEST15 D11 APU_TEST15
TEST16 A10 APU_TEST16 — TP24 R452 *1K/F_4
TEST17 C11 APU_TEST17 R493 *1K/F_4
TEST11 B11 APU_TEST11 R482 *1K/F_4
TEST18 A14 APU_TEST18 R279 1K/F_4
TEST19 B14 APU_TEST19 R243 1K/F_4

TEST28_H A13 APU_TEST28_H — TP66
TEST28_L B13 APU_TEST28_L — TP65 R700 *1K/F_4 — +1.8V
TEST31 P26 APU_TEST31 R693 *1K/F_4 — CZ18V_CZL30V
DP_STEREOSYNC/TEST36 E11 DP_STEREOSYNC R159 1K/F_4 — +1.8V
TEST37 A17 APU_TEST37 R158 *1K/F_4
R531 *1K/F_4
R530 *1K/F_4

VDDCR_GFX_SENSE H11 VDDCR_GFX_SENSE R494 CZ@0_4
VDDCR_NB_SENSE J12 VDDCR_NB_SENSE R481 *0_4/S
VDDCR_CPU_SENSE G12 VDDCR_CPU_SENSE R471 *0_4/S
VDDP_SENSE AY18 VDDP_SENSE — TP27
VSS_SENSE H12 VSS_SENSE R487 CZ@0_4
R478 *0_4/S

DIFFERENTIAL ROUTING
GFX_FB_H [50] / APU_VDDNB_FB_H [48] / APU_VDD_FB_H [48]
GFX_FB_L [50] / APU_VDD_VDDNB_FB_L [48]

SVT C15 SVT0
SVC D17 SVC0
SVD D19 SVD0
GFX_SVT_R B15 SVT1
GFX_SVC_R B16 SVC1
GFX_SVD_R A18 SVD1
APU_SIC B18 SIC
APU_SID C17 SID
APU_RST# D15 RESET_L
APU_PWROK C19 PWROK
APU_PROCHOT# A15 PROCHOT_L
APU_ALERT# B17 ALERT_L
APU_TDI H15 TDI
APU_TDO H14 TDO
APU_TCK D13 TCK
APU_TMS G15 TMS
APU_TRSTN J14 TRST_L
APU_DBRDY C13 DBRDY
APU_DBREQ# A11 DBREQ_L

FP4 REV 1.0
*FP4

CZ: Ra+LS / 1.8V interface (level-shifter)
CZ-L: Rb / 3.3V interface

RNY@1122
Move LS to LCD side and follow CRB

CZ: LS, CZ18V_CZL30V=1.8V
CZ-L: LS, CZ18V_CZL30V=3.3V

+1.8V
LS
[12,20,36,39] KBC_SMCLK — KBC_SMCLK — APU_SIC
[12,20,36,39] KBC_SMDATA — KBC_SMDATA — APU_SID
Q26
DMN5L06DWK/50V_0.302A
+1.8V

APU_PROCHOT# Signal Level:
CZ: +1.8V
CZ-L: +3.3V

[39] KBC_PROCHOT — KBC_PROCHOT
[43,48,50] APU_PROCHOT# — APU_PROCHOT#
[40] OCP_PWM_OUT
Q53
2N7002DW

+1.8V
R710 2.2K_4
APU_PROCHOT#
PJA138K
Q49
2 KBC_PROCHOT
2N7002K
Q54
FAN_FULL_SPEED# [35,36]

Thermal Sensor

ALF@1025:
CZ & CZ-L for LS

TP25
[48,50] APU_PG — R255 *0_4/S

APU_RST#
APU_PWROK
C251 *150P/50V_4
C294 *150P/50V_4

VDDCR_CPU_SENSE — TP46
VDDCR_NB_SENSE — TP12
VDDCR_GFX_SENSE — TP62

DP_STEREOSYNC: HDMI enable pin.

CZ: R494, R487 Stuff
CZ-L: R494, R487 No Stuff

APU Serial VID

ALF@1030:
Needs confirm with AMD

+1.8V
Place near APU within 500mil
[48] APU_SVT — R597 *0_4/S — SVT
[48] APU_SVC — R575 36/F_4 — SVC
[48] APU_SVD — R582 36/F_4 — SVD
R566 *1K/F_4
R576 *1K/F_4
R513 *1K/F_4

PV, 0414, change SVID R to 0 ohm
PV, 0420, change SVID R to 36 ohm

GFX Serial VID

ALF@1030:
Needs confirm with AMD

+1.8V
Place near APU within 500mil
[50] GFX_SVT — R512 CZ@0_4 — GFX_SVT_R
[50] GFX_SVC — R535 CZ@0_4 — GFX_SVC_R
[50] GFX_SVD — R544 CZ@0_4 — GFX_SVD_R
R545 *CZ@1K/F_4
R536 CZ@1K/F_4
R518 *CZ@1K/F_4

12/9: confirm AMD PAE Scoop no need setting

VFIX MODE — VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

IO Thermal Protect

ALF@1031:
Del NTC Circuit

HDT+ Connector for Debug only
Can remove on MP

+3V
C331 0.1U/16V/X7R_4
U12 TC7SH08FU
CPU_LDT_RST_HTPA# — APU_RST#

J1 HDT CONN 88511-2001-20p-l
INT TP35
APU_TEST18
APU_TEST19
APU_RST_L_BUF
CPU_LDT_RST_HTPA#
APU_DBREQ#
APU_DBRDY
APU_TCK
APU_TMS
APU_TDI
APU_TRST#
APU_TDO
APU_PWROK_BUF

+3V +1.8V
R295 0_4
R290 *0_4
C327 0.1U/16V/X7R_4
R288 1K/F_4
R284 1K/F_4
+1.8V
U11 74LVC2G07GW
APU_RST# — APU_RST_L_BUF
APU_PWROK — APU_PWROK_BUF

Close to HDT & No remove.
+1.8V
APU_TDI R409 1K/F_4
APU_TCK R407 1K/F_4
APU_TMS R410 1K/F_4
APU_TRST# R408 1K/F_4
APU_DBREQ# R400 1K/F_4

NB5
PROJECT : 400 SERIES
Quanta Computer Inc.
Size | Document Number: Carrizo 3/7 (DIS/MISC) | Rev 1A
Date: Friday, July 24, 2015 | Sheet of 62

	PLT_ID1	PLT_ID2	PLT_ID3
	EGPIO95	EGPIO96	EGPIO101
Palazzo 15"	0	1	0

	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
BOARD REVISION	EGPIO97	EGPIO98	EGPIO99	EGPIO100	
DB0	0	0	0	0	
DB1	0	0	0	1	
DB2	0	0	1	0	
	0	0	1	1	
SI1	0	1	0	0	
SIB	0	1	0	1	
SI2	0	1	1	0	
	0	1	1	1	
PV1	1	0	0	0	
	1	0	0	1	
	1	0	1	0	
	1	0	1	1	
MV1	1	1	0	0	Default
	1	1	0	1	
	1	1	1	0	
	1	1	1	1	

VBIOS_ID	VBIOS_ID1	VBIOS_ID2
	AGPIO6	AGPIO24
Discrete VRAM Group #1	0	0
Discrete VRAM Group #2	0	1
Discrete VRAM Group #3	1	0
UMA	1	1

ALF@1110:
HP confirmed the 00 for DIS, 11 for UMA, need to set in BOM

Default

ALF@1110:
HP confirmed Okay!!

ALF@1105:
Changed the "ODD_PWR" to EGPIO93

RNY@1108: Changed LANLINK# to PU

ALF@1107:
Changed WOL_EN and PD

Only CZ Stuff if no used

SYS_RST# internal 10K pull up

PV, 0415, reserve NMI_SMI_DBG# PU resistor

to DDR3 SMBUS

Only CZ Stuff

ALF@1119:
Reserved the CLKREQG# for dGPU

PV, 0420, change NMI_SMI_DBG# from AGPIO86 to AGPIO17, and delete CR_PWREN#

Power Domain
CZ CZ-L

to TP SMBUS

PCIE_WAKE# PU & LAN use 0 ohm to open.

PV, 0420, delete CR_PWREN# pull-up resistor

ALF@1109:
HP request to add the Card Reader weak feature

SI, 0117, fine tune GPU sequence

for GPIO145~148
CZ pop those resistor
CZ-L can NC them

1029@RNY: Add PU for LAN CLKREQ#

ALF@1031:
Following AMD Leading to add LS

SI, 0117, fine tune GPU sequence

SI, 0201, reserved for fine tune GPU sequence

PV, 0414, change ACCEL_INTH GPIO pin and Pull-up power rail

Only CZ-L Stuff if no used

SI, 0201, fine tune GPU sequence

To Azalia

PV, 0414, pull-down 1K for AZ timing issue

Follow AMD checklist 53537_1_03 suggestion to stuff R118/R120/R122

TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled

ALF@1030:
For dGPU VGA REQ

Pure UMA can remove

From dGPU PG Ready (As default)

ALF@1030:
For dGPU Power Enable Sequence & GPIOs

SI, 0117, fine tune GPU sequence

PROJECT	400 SERIES
Quanta Computer Inc.	
NB5	
Size	
Document Number	Carrizo 4/7 (GPIO/AZ/UARTH)
Rev	1A
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Only CZ Stuff if no used

1029@RNY: DEVSLP0 is used, PU no need

R179 *10K/F_4 DEVSLP0
R182 10K/F_4 CAMERA_ON
R489 *10K/F_4 SPI_TPM_CS#
R455 10K/F_4 EGPIO119

ALF@1109:
HP request to add Card Reader weak feature

U23 *MC74VHC1G08DFT2G

[34] LED_3S_SATA#

R522 *0_4/S

C492 *0.1U/16V/X7R_4

HDD
ODD

[37] SATA_TXP0 / [37] SATA_TXN0
[37] SATA_RXN0 / [37] SATA_RXP0
[37] SATA_TXP1 / [37] SATA_TXN1
[37] SATA_RXN1 / [37] SATA_RXP1

R427 1K/F_4 SATA_CALRN
R434 1K/F_4 SATA_CALRP
[37] DEVSLP0
[19] CAMERA_ON
SB_SATA_LED#

PV, 0414, change AGPIO90 to CAMERA_ON

Integrated Clock Mode:
Leave unconnected.

TP37 TP38

SI, 0203, change cap to fine tune XTAL

C74 4.7P/50V_4
Y1 48MHZ +-10PPM
C67 4.7P/50V_4
R83 1M/F_4
48M_X1 48M_X2

[11] CLK_GFX_P / [11] CLK_GFX_N
[24] CLK_PCIE_LANP / [24] CLK_PCIE_LANN
[29] CLK_WLAN_P / [29] CLK_WLAN_N
[34] CLK_PCIE_CARDP / [34] CLK_PCIE_CARDN

RP1 33_4P2R_4
RP4 0_4P2R_4
RP2 47_4P2R_4
RP3 0.4P2R_4

PV, 0414, change RP1 to 33ohm, RP2 to 47ohm for CZ

BC10 X25M_48M_OSC

C485 *10P/50V_4
C473 *10P/50V_4

SI, 0203, EMI solution

R496 BLM15BB470SN1D(47,300mA)
R486 56_4

[29,39] CLK_R3S_KBC
[38] CLK_R3S_DEBUG

PV, 0414, change CLK_R3S_DEBUG R to 56ohm for CZ

[29,38,39] LAD0
[29,38,39] LAD1
[29,38,39] LAD2
[29,38,39] LAD3
[29,38,39] LFRAME#
[38,39] PCI_3S_SERIRQ
[39] PCI_3S_CLKRUN#

R156 10K/F_4

1029@RNY: follow Leading NC
PV, 0415, follow AMD DG to PD LPC_PD_L, no used

R480 4.7K_4 PCI_3S_CLKRUN#
R514 10K/F_4 SB_SATA_LED#
R597 10K/F_4 PCI_3S_SERIRQ
R488 *150/F_4 PCI_3S_CLKRUN#

[41] SPI_CS0#
[41] SPI_CLK
[41] SPI_SO
[41] SPI_SI
[26] SPI_TPM_CS#
[41] SPI_WP

C467 *15P/50V_4

PV, 0421, TP42 change to 2075 for layout

ALF@1103:
HP request to add SPI_WP to SPI

U24E

Camera USB
DB right side USB2.0 port
DB right side USB2.0 port

ALF@1029:
Del the USB2.0 for Touch Screen

WLAN Min-Card
Finger Printer
left side USB Combo 3.0/2.0.
left side USB Combo 3.0/2.0.

CZ: Maximum 8 devices (Ex: 8 USB2.0 –OR-- 4 USB2.0 + 4 USB3.0 external, etc…)

CZ-L: Maximum 8 devices (Ex: 8 USB2.0 –OR-- 6 USB2.0 + 2 USB3.0 external, etc…)

+0.95V_DEEP_SUS
R73 *0_4/S
R74 *0_4
+0.95V

Support S3~S5 wake up
No support S3~S5 wake up

Left side USB Combo 3.0/2.0.
Left side USB Combo 3.0/2.0.

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

LPC_CLK0
LPC_CLK1
LFRAME#
[5] AGPIO3
[5,40] RTC_CLK
[5] AGPIO11
[5] SYS_RST#

1024@Ronny: AGPIO11 STRAP?

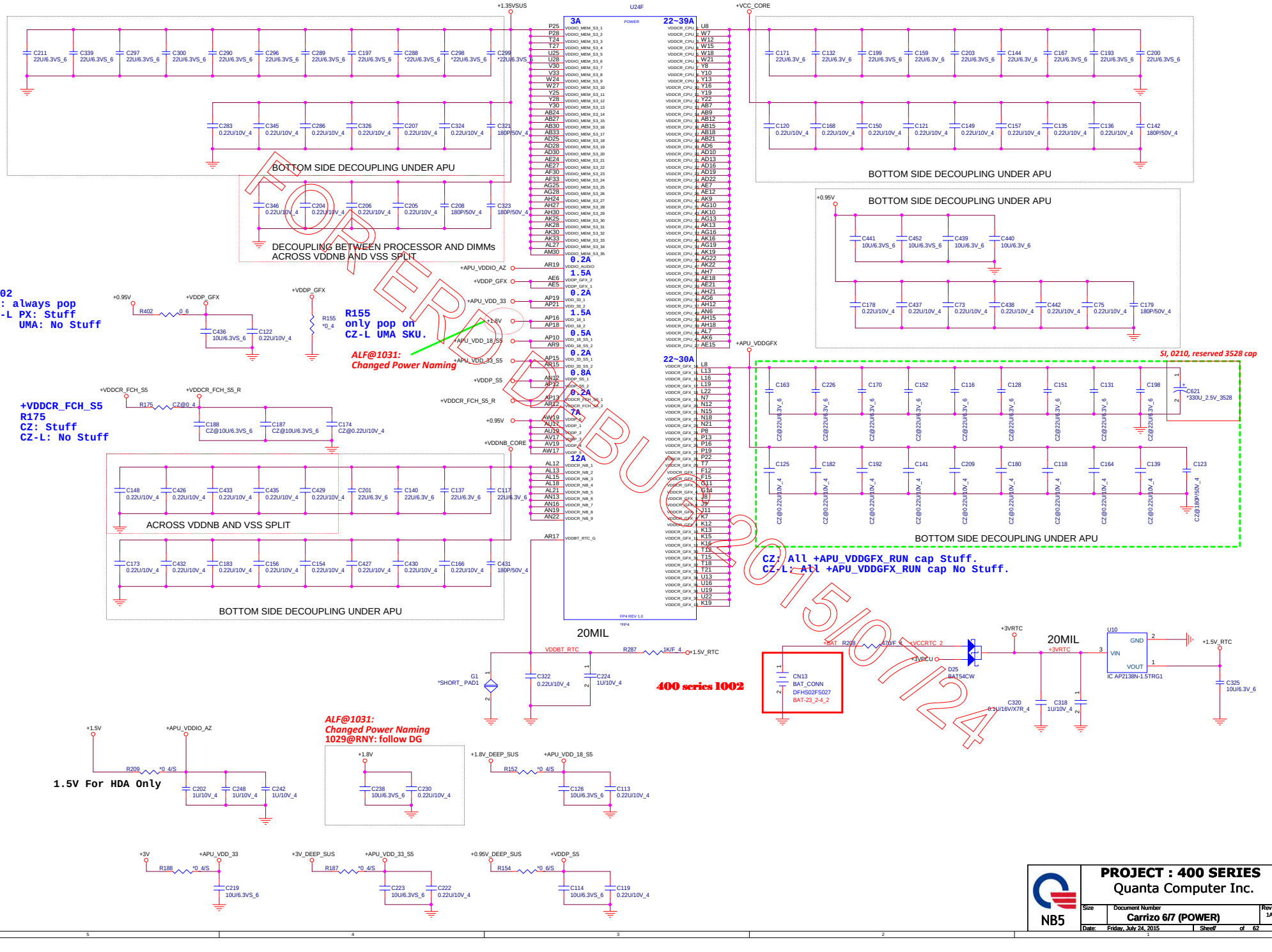
CZ: pop R445
CZ-L:pop R457

Follow FAE comment: R659 change to 2K, R401 to 10k, R142 is NC

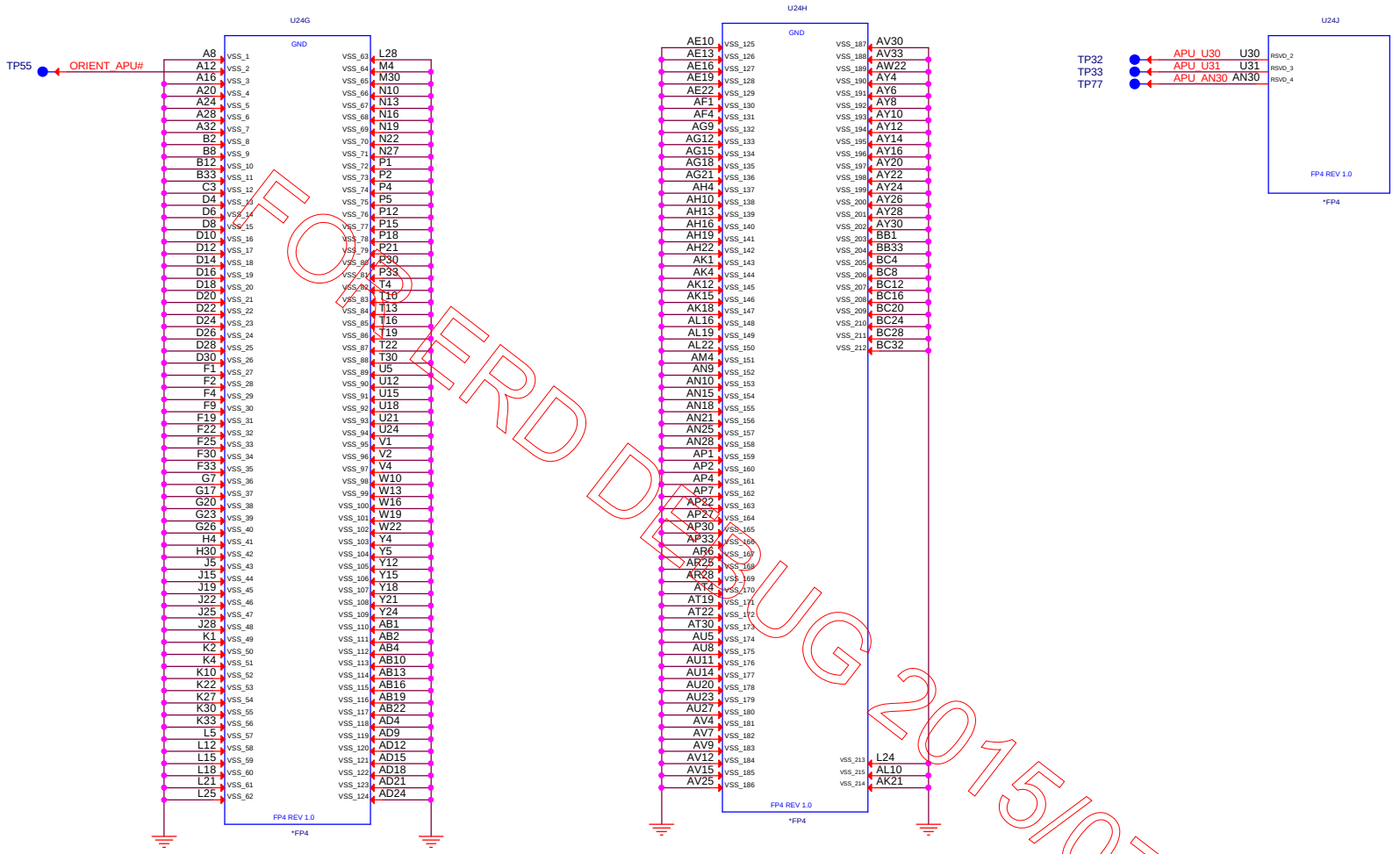
REQUIRED STRAPS

	LPC_CLK0	LPC_CLK1	LFRAME#	AGPIO3 Int Pull-Up		RTC_CLK Int Pull-Up	AGPIO11 BLINK Int Pull-Up	SYS_RST# Int Pull-Up
				CZ-L	CZ			
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM	Enhanced reset logic (for quicker S5 resume) DEFAULT	Coin battery is on board. DEFAULT	LDT_RST#/LDT_PWRGD output to APU DEFAULT	normal reset mode DEFAULT
PULL LOW	BOOT FAIL TIMER DISABLED DEFAULT	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC ROM	3.3V SPI ROM DEFAULT	Default to traditional reset logic	Coin battery is not on board.	LDT_RST#/LDT_PWRGD output to Pads	short reset mode

PROJECT : 400 SERIES
Quanta Computer Inc.
NB5
Size | Document Number: Carrizo 5/7 (SATA/USB/SPI) | Rev: 1A
Date: Friday, July 24, 2015 | Sheet 6 of 62



NB5	PROJECT : 400 SERIES Quanta Computer Inc.		
	Size	Document Number Carrizo 6/7 (POWER)	Rev 1A
	Date: Friday, July 24, 2015	Sheet 7 of 62	

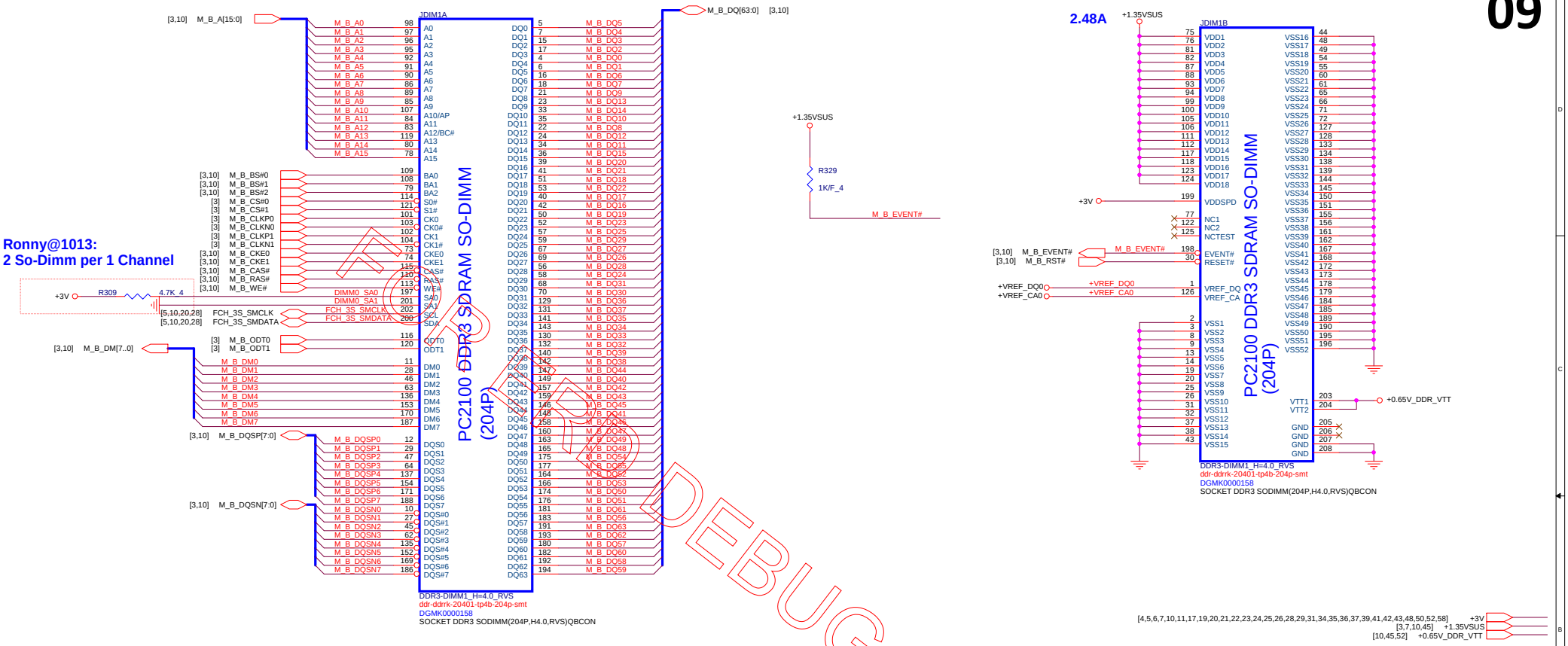


NB5

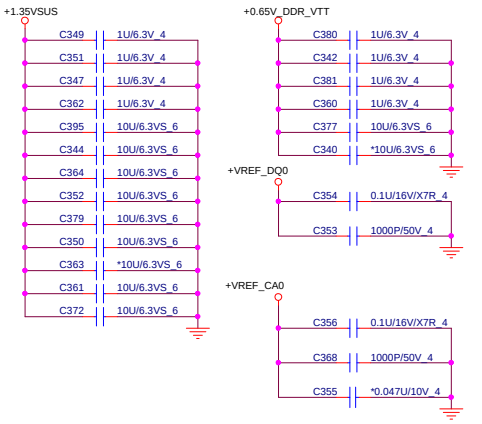
PROJECT : 400 SERIES
Quanta Computer Inc.

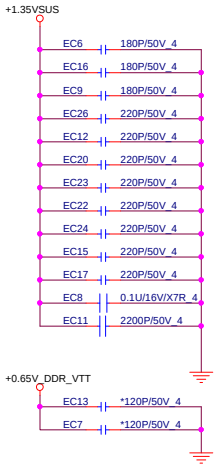
Size	Document Number	Rev
	Carrzio 7/7 (GND)	1A
Date: Friday, July 24, 2015	Sheet 8 of 62	

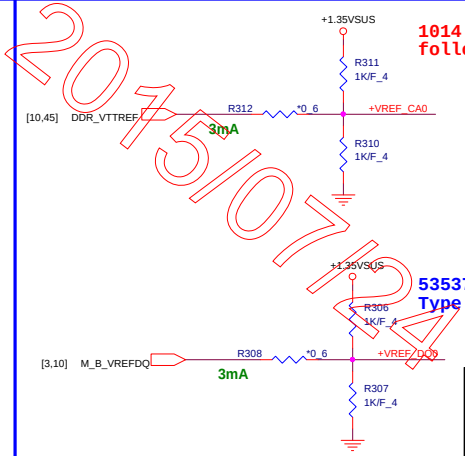
Ronny@1013:
2 So-Dimm per 1 Channel



Place these Caps near So-Dimm0.





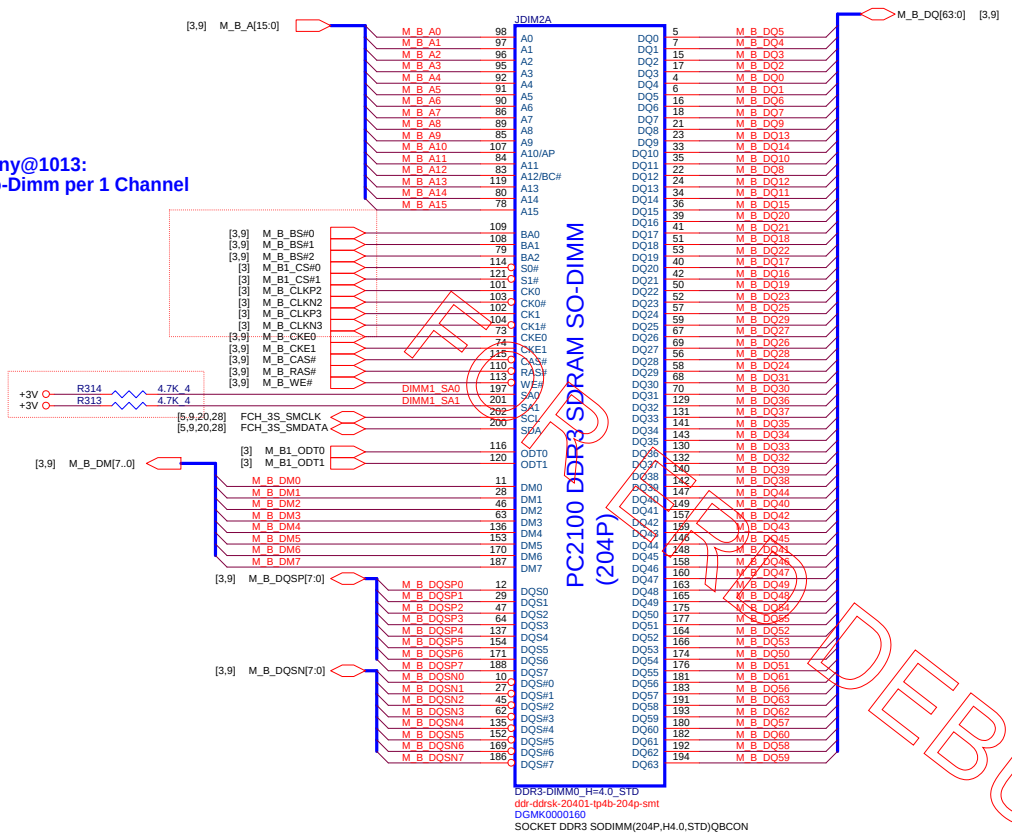


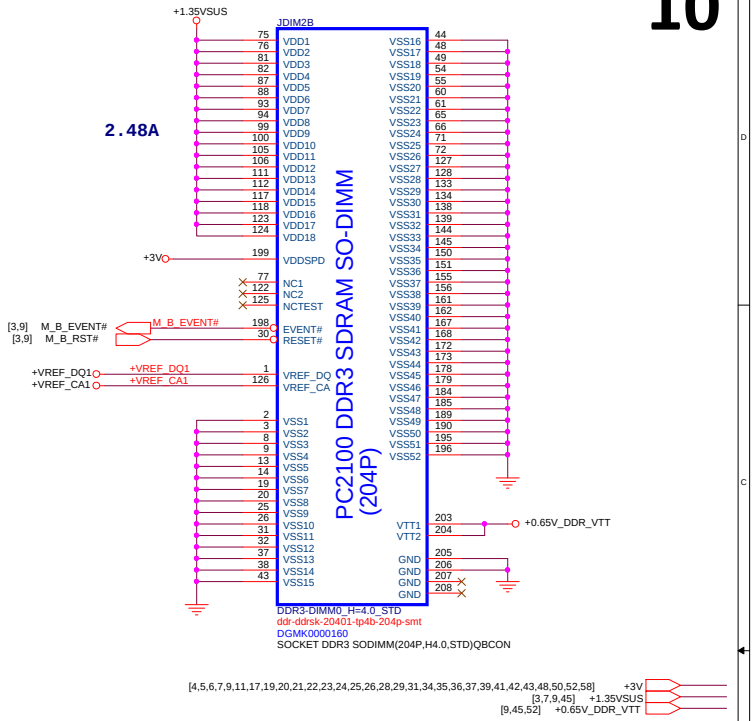
1014: Ronny
follow DG use voltage divider

53537_105 change:
Type 1: and Type 2: from 1K/2 voltage

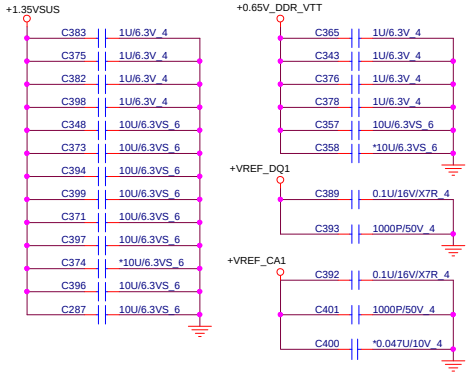
NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
Size: Custom	Document Number: System Memory 1/2 (4H)	Rev: 1A
Date: Friday, July 24, 2015	Sheet 9 of 62	

Ronny@1013:
2 So-Dimm per 1 Channel

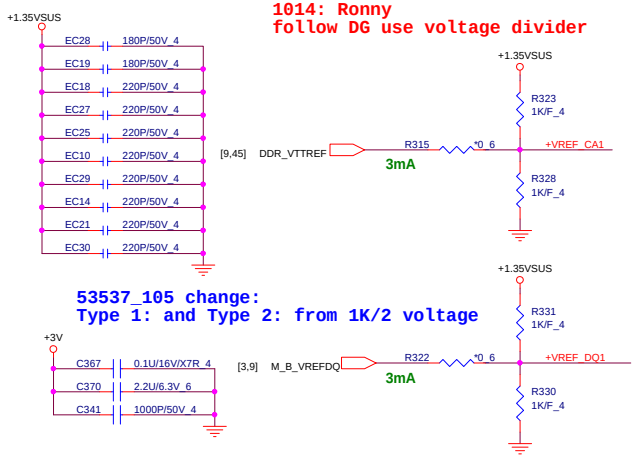




Place these Caps near So-Dimm1.



1014: Ronny
follow DG use voltage divider

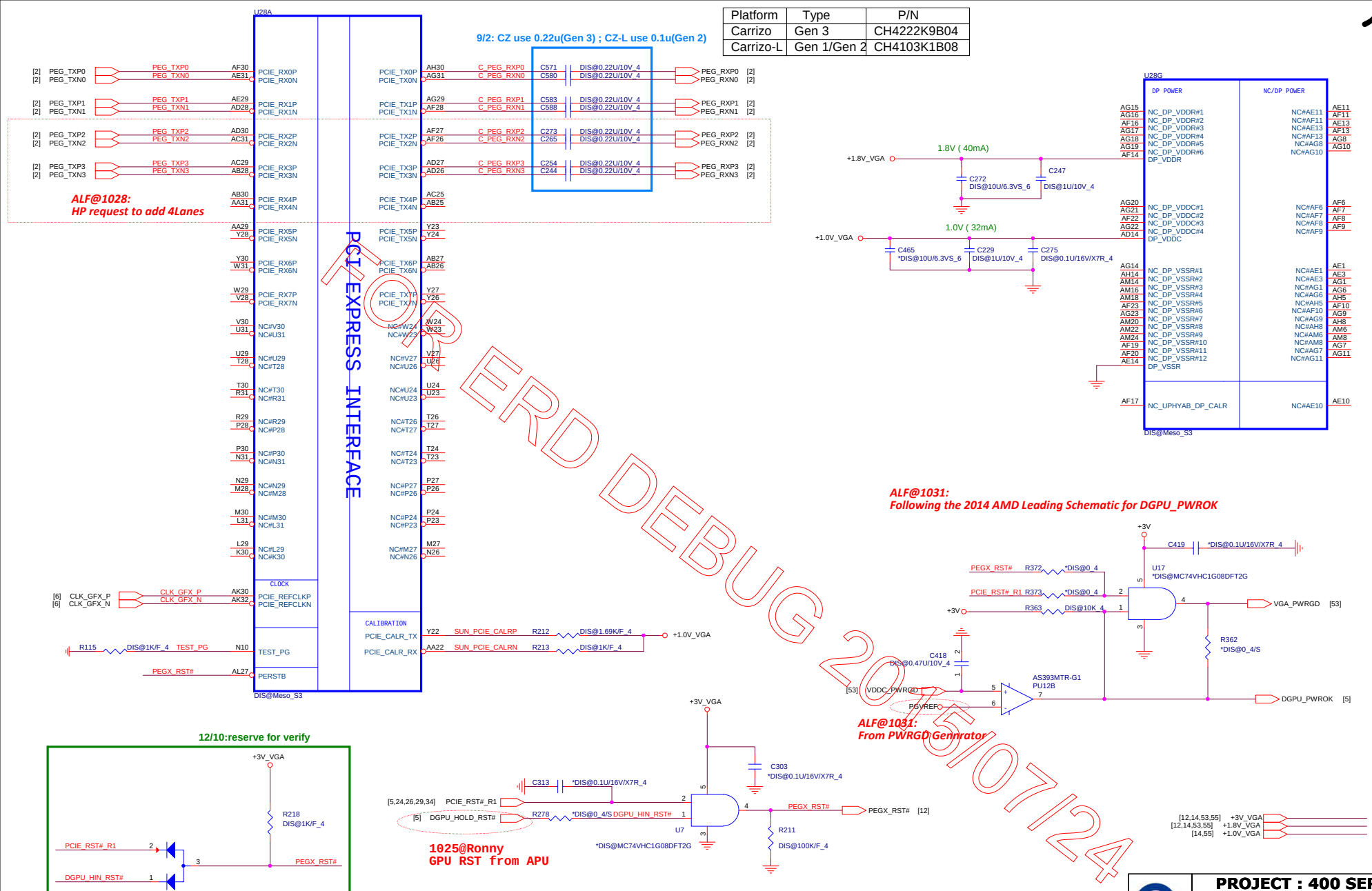


DDR3 Thermal Sensor

1028: Ronny
delete DDR thermail IC, please refer to Page41

NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
	Size: Custom Document Number: System Memory 2/2 (4H)	Rev: 1A
	Date: Friday, July 24, 2015	Sheet 10 of 62

Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4103K1B08



PROJECT :	400 SERIES
Quanta Computer Inc.	
Size	Document Number: TOPAZ S3 PCIE/DP power
Rev	1A
NB5	Monday, July 27, 2015
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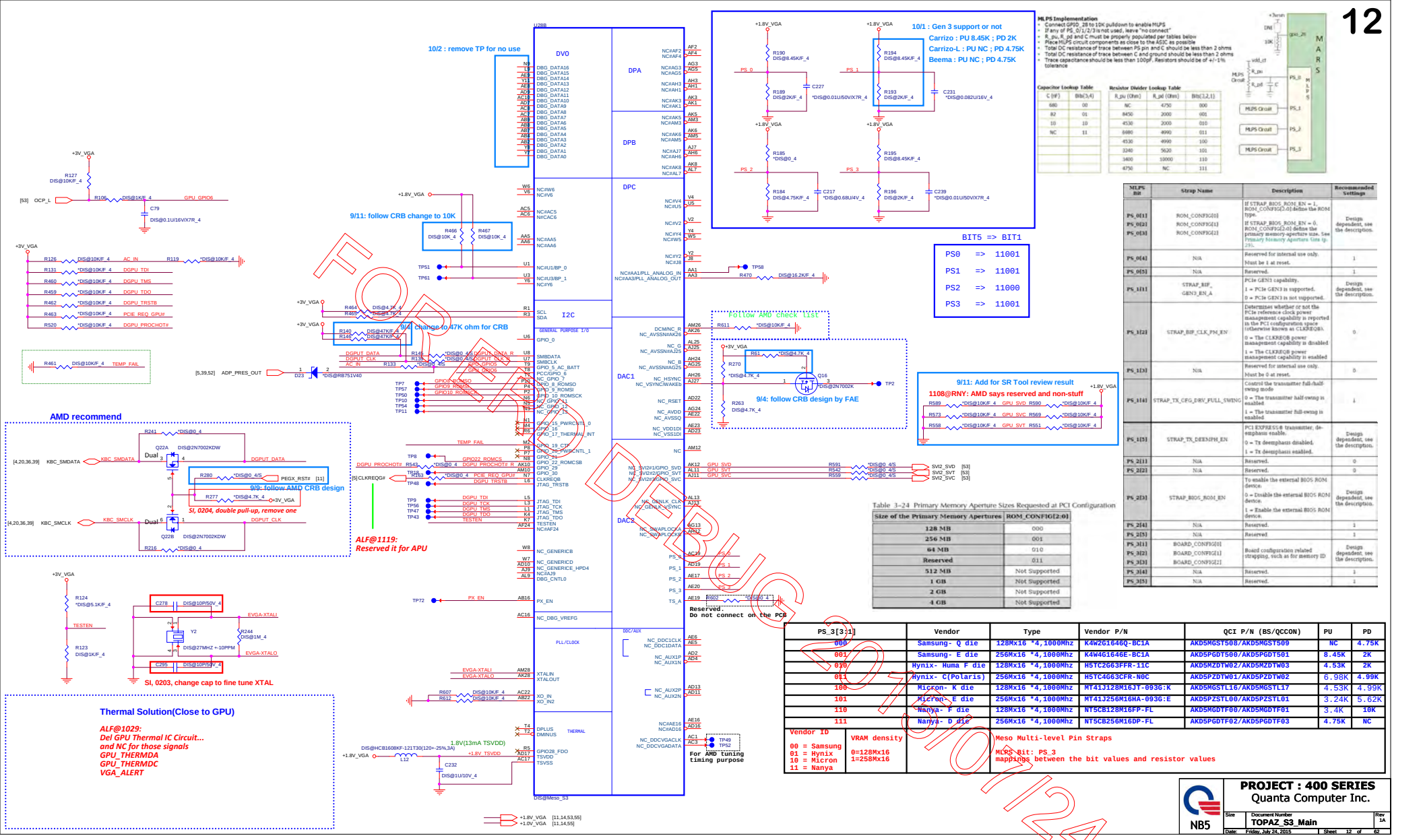

MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(3,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(12,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory aperture size. See Primary Memory Aperture Size (p. 29).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[4]	N/A	Reserved.	1
PS_2[5]	N/A	Reserved.	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[4]	N/A	Reserved.	1
PS_3[5]	N/A	Reserved.	1

Table 3-24 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

PS_3[3:1]	Vendor	Type	Vendor P/N	QCI P/N (BS/QCCON)	PU	PD
000	Samsung- Q die	128Mx16 *4,1000Mhz	K4W2G1646Q-BC1A	AKD5MGST508/AKD5MGST509	NC	4.75K
001	Samsung- E die	256Mx16 *4,1000Mhz	K4W4G1646E-BC1A	AKD5PGDT500/AKD5PGDT501	8.45K	2K
010	Hynix- Huma F die	128Mx16 *4,1000Mhz	H5TC2G63FFR-11C	AKD5MZDTW02/AKD5MZDTW03	4.53K	2K
011	Hynix- C(Polaris)	256Mx16 *4,1000Mhz	H5TC4G63CFR-N0C	AKD5PZDTW01/AKD5PZDTW02	6.98K	4.99K
100	Micron- K die	128Mx16 *4,1000Mhz	MT41J128M16JT-093G:K	AKD5MGSTL16/AKD5MGSTL17	4.53K	4.99K
101	Micron- E die	256Mx16 *4,1000Mhz	MT41J256M16HA-093G:E	AKD5PZSTL00/AKD5PZSTL01	3.24K	5.62K
110	Nanya- F die	128Mx16 *4,1000Mhz	NT5CB128M16FP-FL	AKD5MGDTF00/AKD5MGDTF01	3.4K	10K
111	Nanya- D die	256Mx16 *4,1000Mhz	NT5CB256M16DP-FL	AKD5PGDTF02/AKD5PGDTF03	4.75K	NC

Vendor ID

00 = Samsung
01 = Hynix
10 = Micron
11 = Nanya

VRAM density

0=128Mx16
1=258Mx16

Meso Multi-level Pin Straps

MLPS Bit: PS_3
mappings between the bit values and resistor values

PROJECT : 400 SERIES	
Quanta Computer Inc.	
NB5	Size: — Document Number: TOPAZ_S3_Main Rev: 1A
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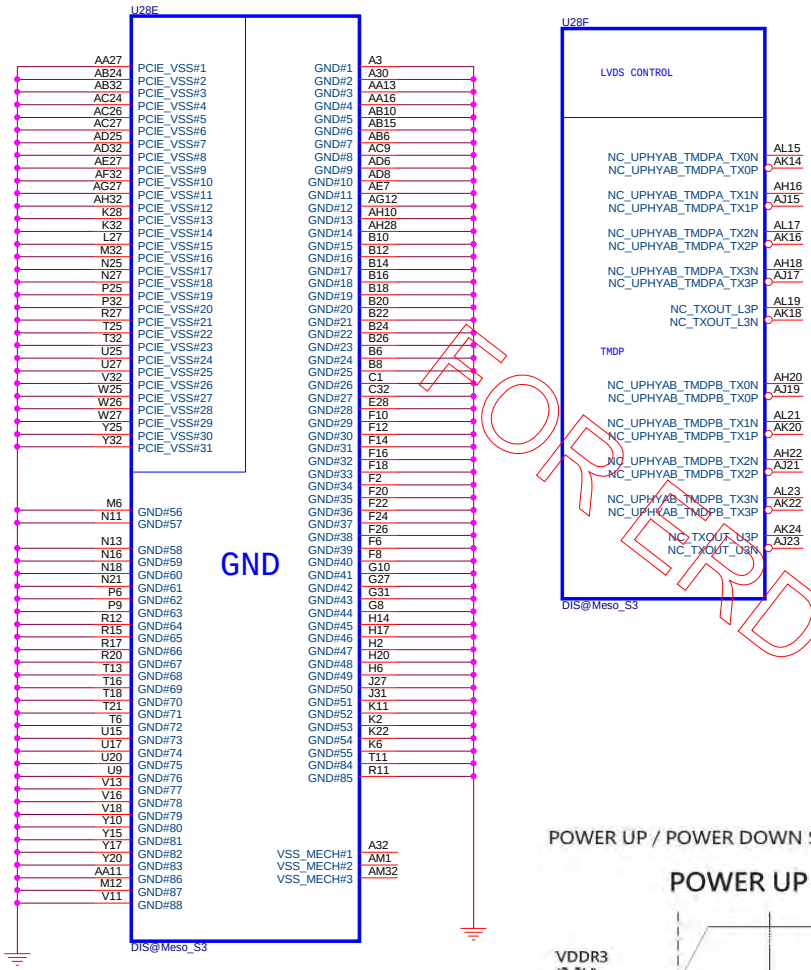


CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

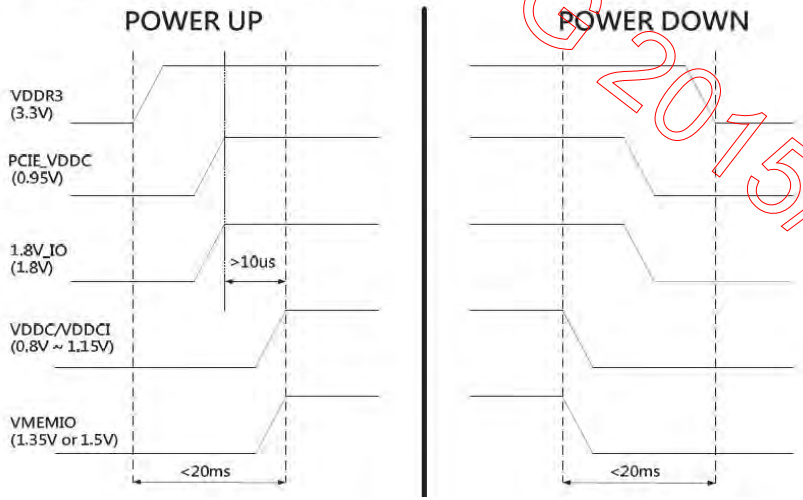
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

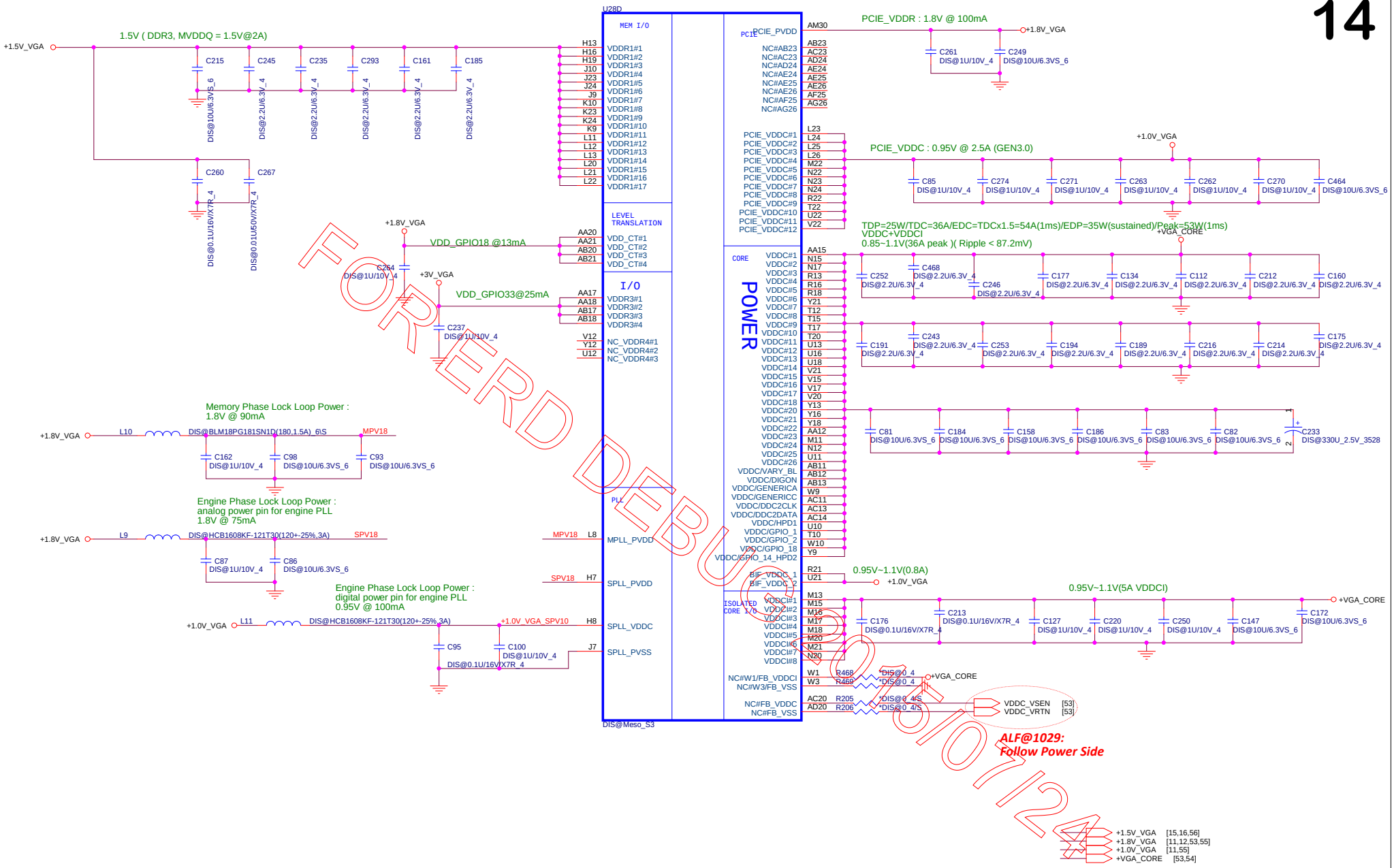
POWER UP / POWER DOWN SEQUENCE



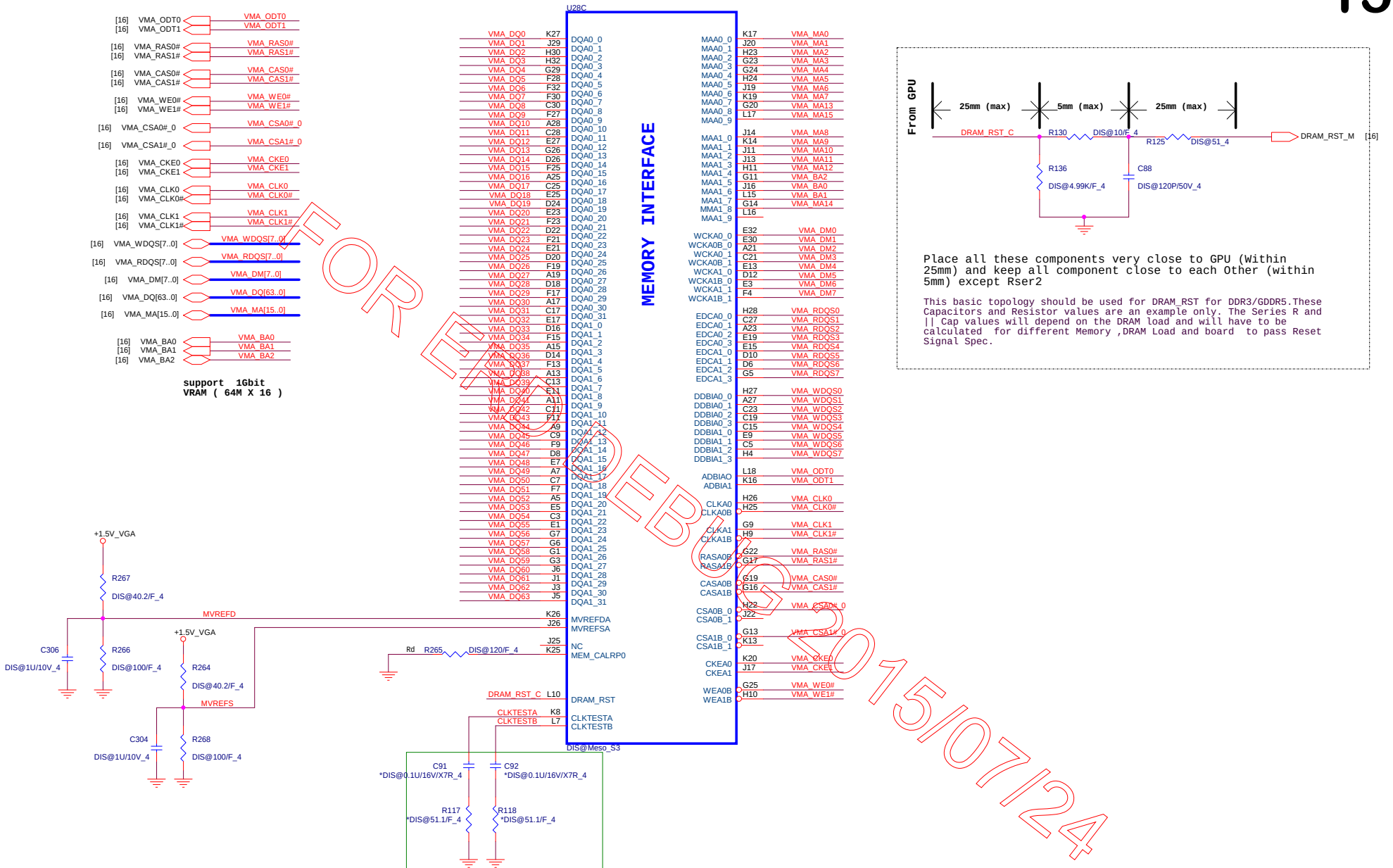
NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
	TOPAZ_S3_GND/LVDS/Strap	1A
Date: Friday, July 24, 2015	Sheet 13 of 62	



NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
Size	Document Number TOPAZ S3 Power	Rev 1A
Date: Friday, July 24, 2015	Sheet 14 of 62	



NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
Size	Document Number TPOAZ_S3_MEM_Interface	Rev 1A
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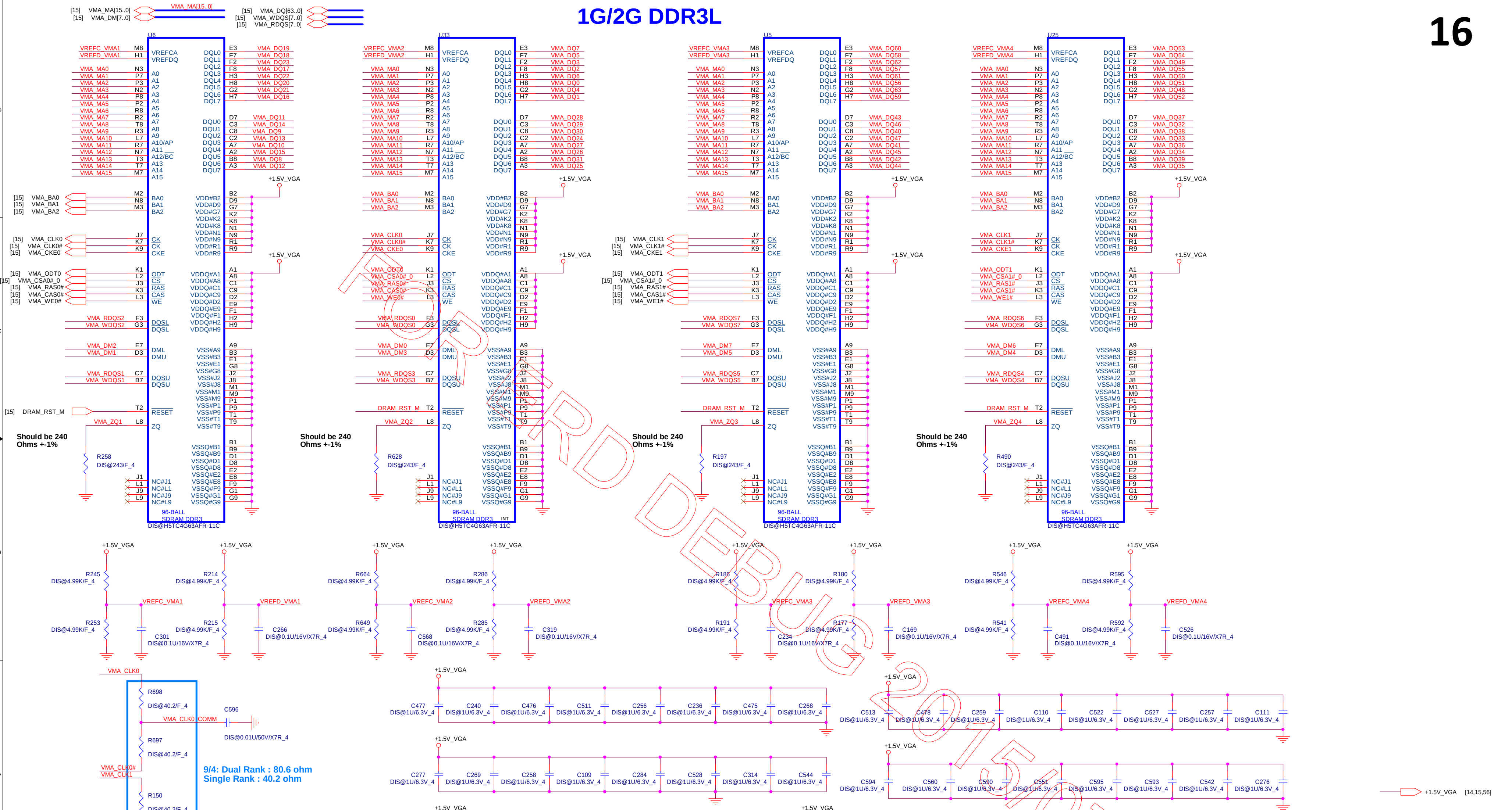
1G/2G DDR3L



PROJECT : 400 SERIES
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Sun S3 VRAM(DDR3 BGA96P)	1A

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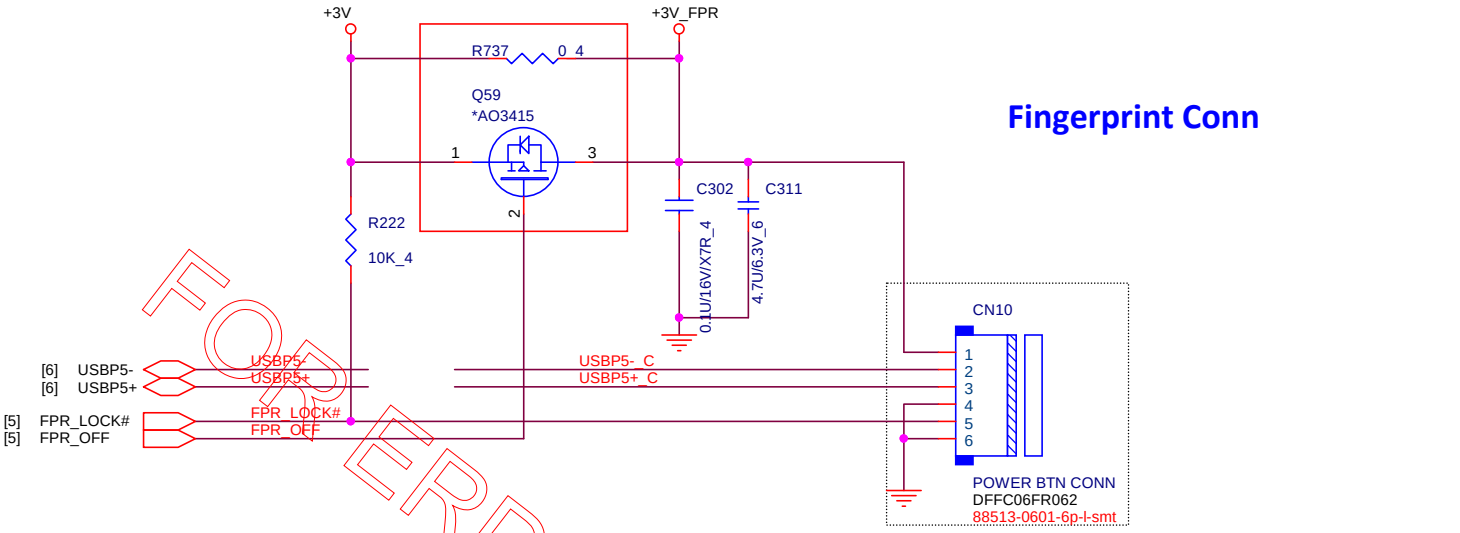
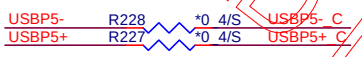
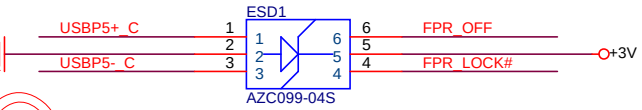
PV, 0415, follow leading project to add MOSFET for FPR_OFF

Fingerprint Conn



1105@Ronny: need to change PN and FP





NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**Finger Printer**	1A
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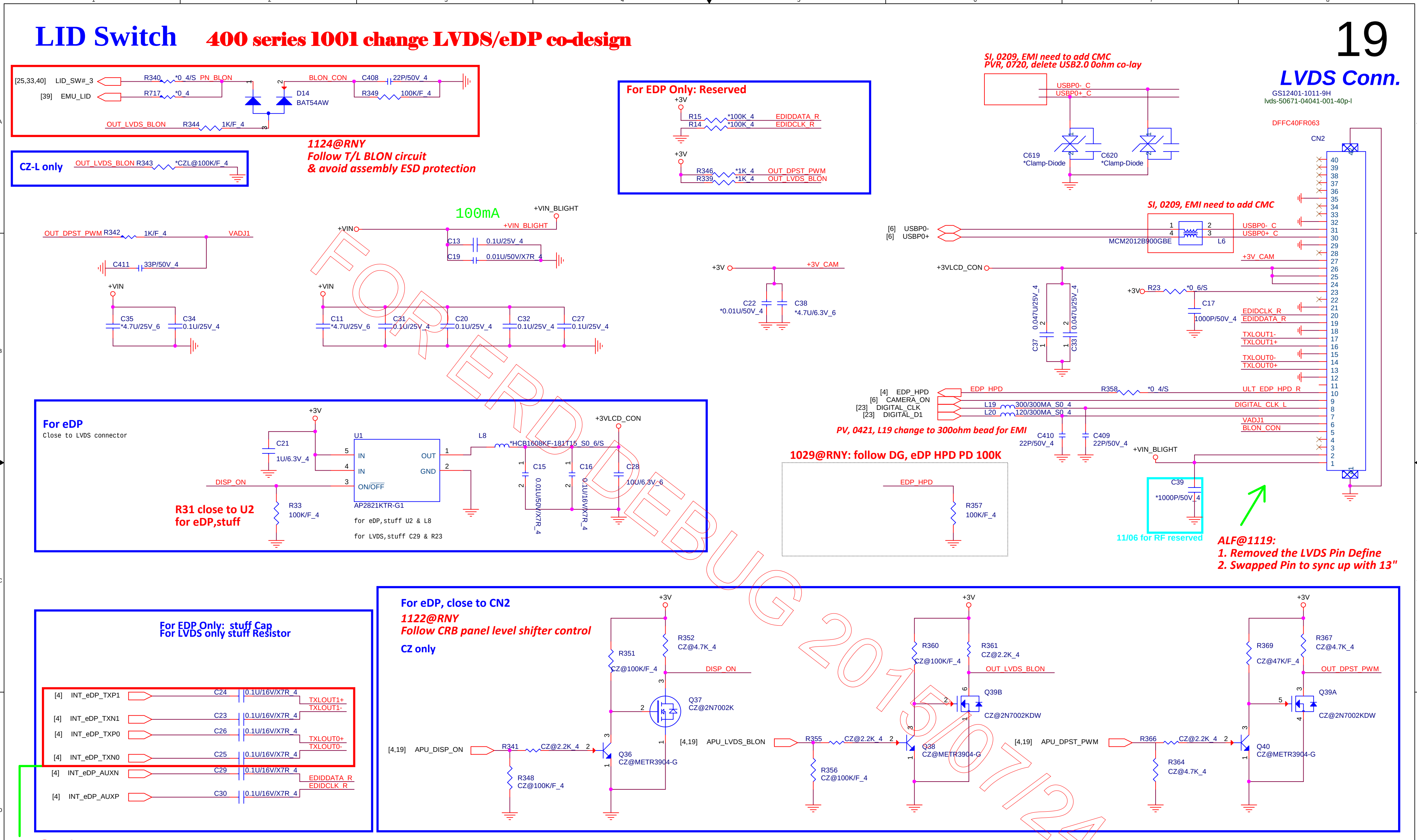
400 series 0930 Delete DP DemultiPlexter due to not support docking

400 series 1001 change to LVDS/eDP co-design

ALF@1119:
HP confirmed to remove the eDP to LVDS convertor.

[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,35,36,37,39,41,42,43,48,50,52,58] +3V



PROJECT : 400 SERIES
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM/D-MIC	1A

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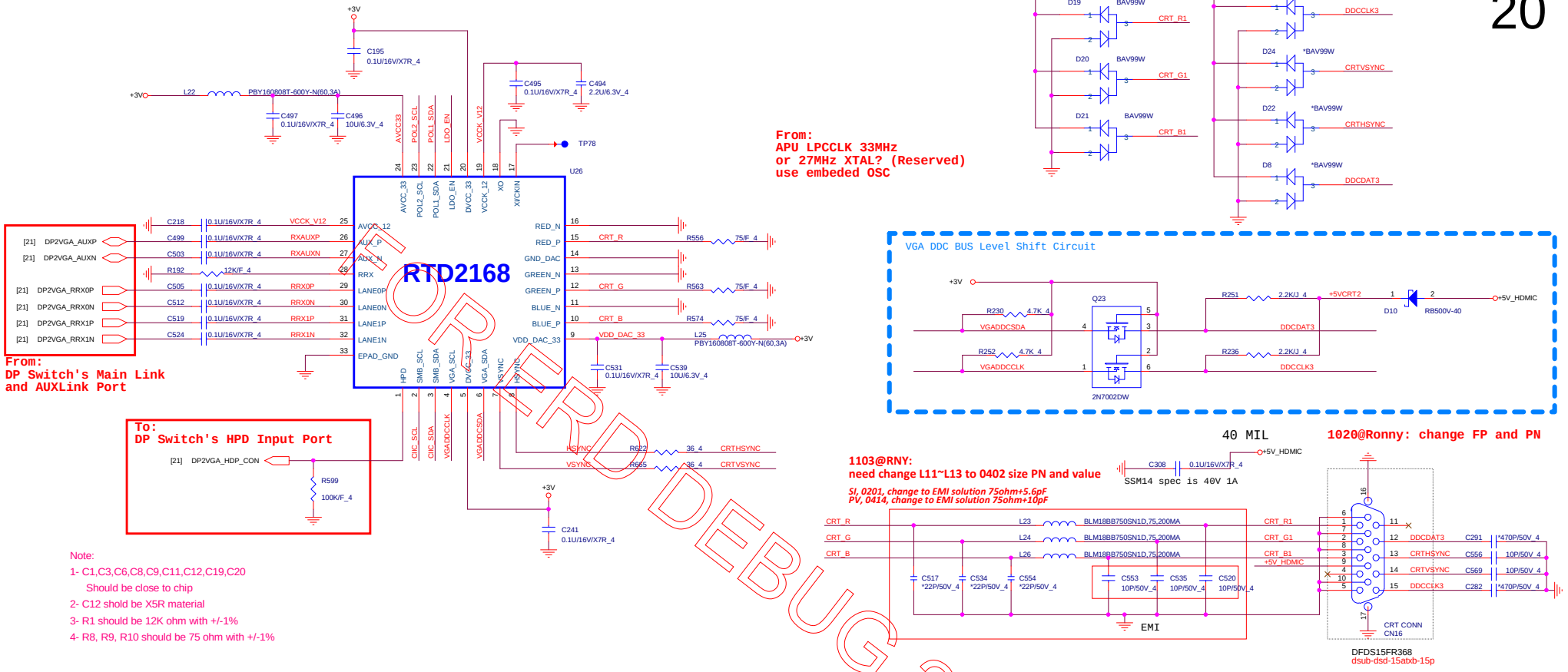


Note:
1- C1,C3,C6,C8,C9,C11,C12,C19,C20
Should be close to chip
2- C12 shold be X5R material
3- R1 should be 12K ohm with +/-1%
4- R8, R9, R10 should be 75 ohm with +/-1%

Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

1031@RNY: defualt use internal ROM
RTD2168 Supports three operation mode for system design.
Reserve 4.7K resistor pull high/low for mode selection

ROM ONLY Mode : PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high

EEPROM MODE

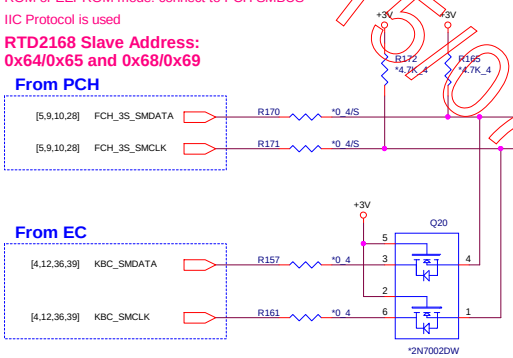
In EEPROM mode,an additional EEPROM is needed.
EEPROM should configure with following conditions.

1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

CIIC_SCL, CIIC_SDA Connection

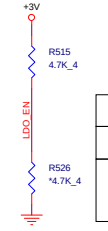
EP mode: Pin2, Pin3 connect to EC SMBUS
ROM or EEPROM mode: connect to PCH SMBUS
IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69



Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO



LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

NB5	PROJECT : 400 SERIES Quanta Computer Inc.		
	Size: Custom	Document Number: DP to VGA	Rev: 1A
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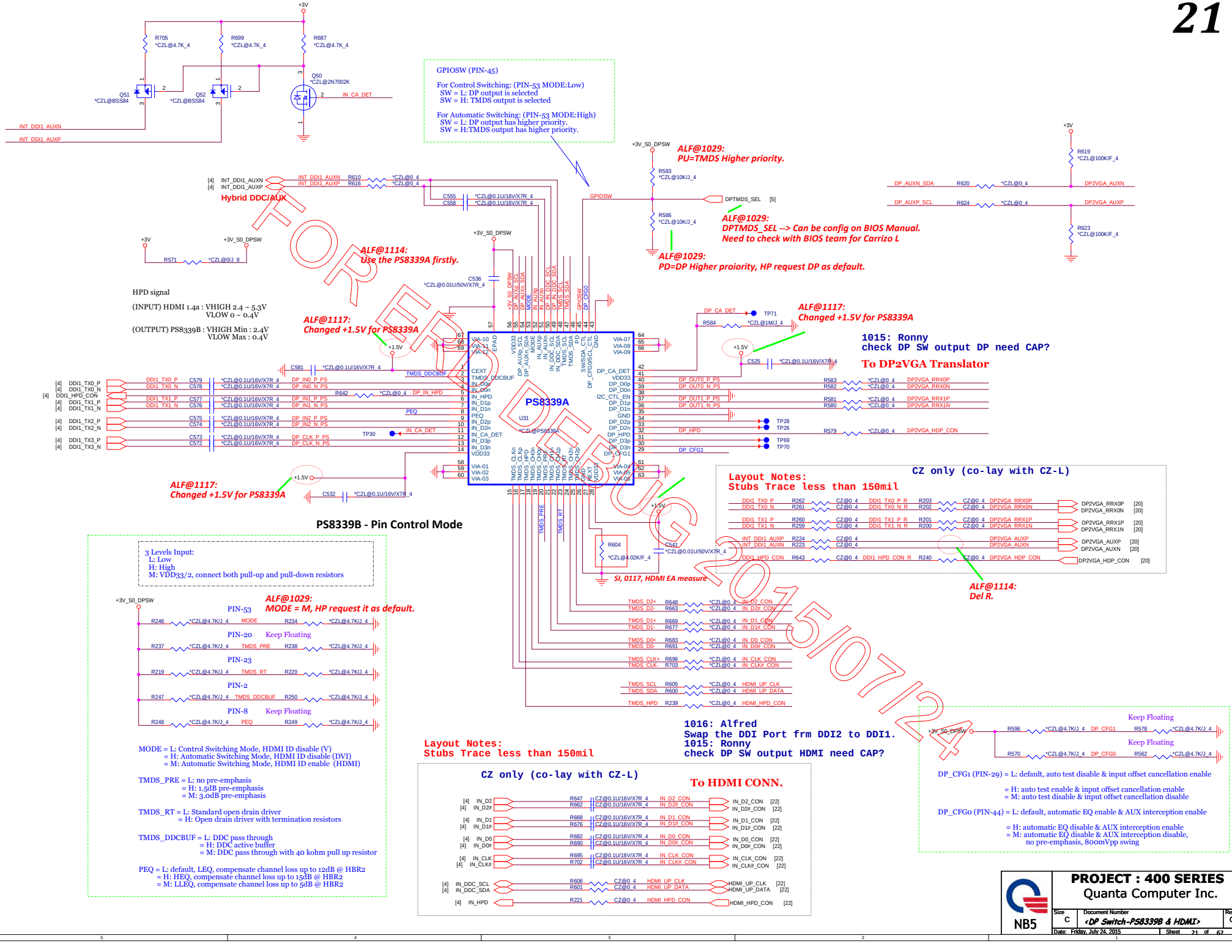
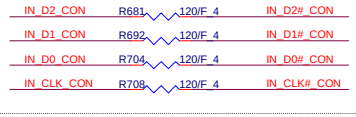
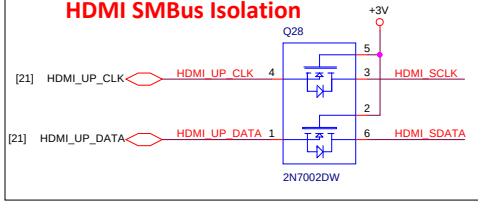
July 24, 2014



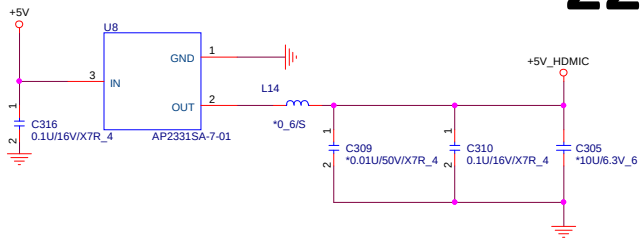
EMI Solution



HDMI SMBus Isolation

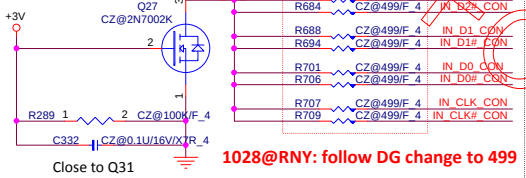


1105@RNY: follow AMD leading



CZ only, DP switch contain below circuit

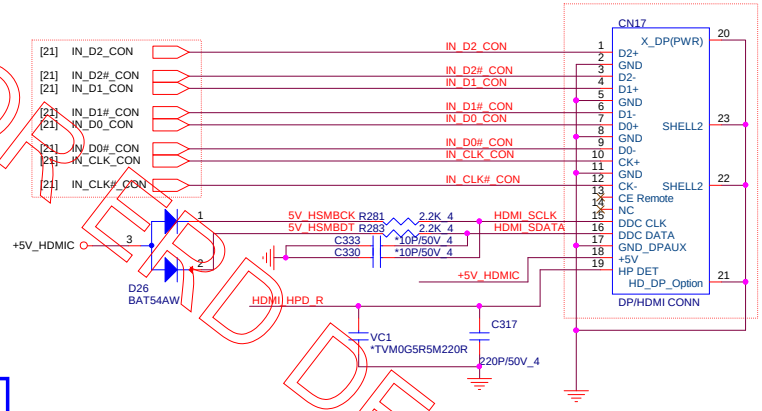
Close to HDMI connector

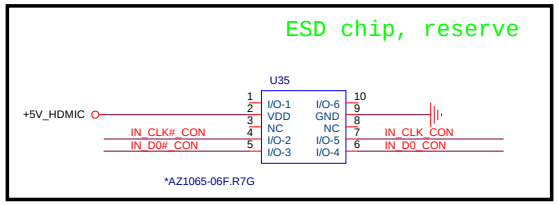


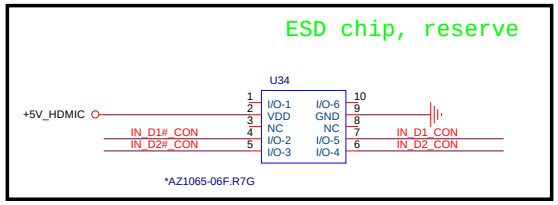
1028@RNY: follow DG change to 499

1014@Ronny : remove re-driver IC
1015@Ronny: Add DP Switch
1016@Alfred: Changed the DDI1 to DDI2

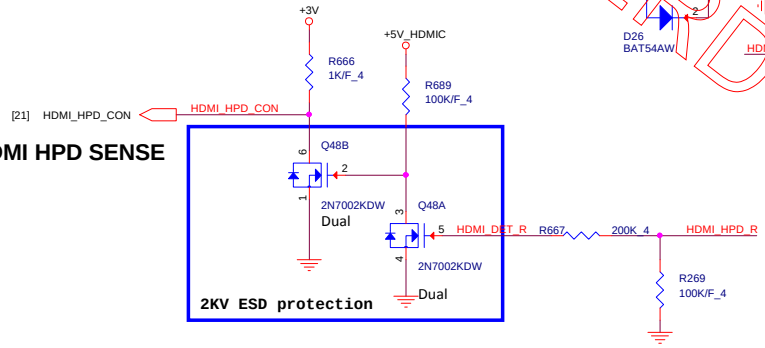
1028@Ronny : change FP only need confirm PN then change PN







HDMI HPD SENSE



1028@RNY: follow X21 HPD circuit

NB5	**PROJECT : 400 SERIES** Quanta Computer Inc.	
Size: Custom	Document Number: **HDMI CONNECTOR**	Rev: 1A
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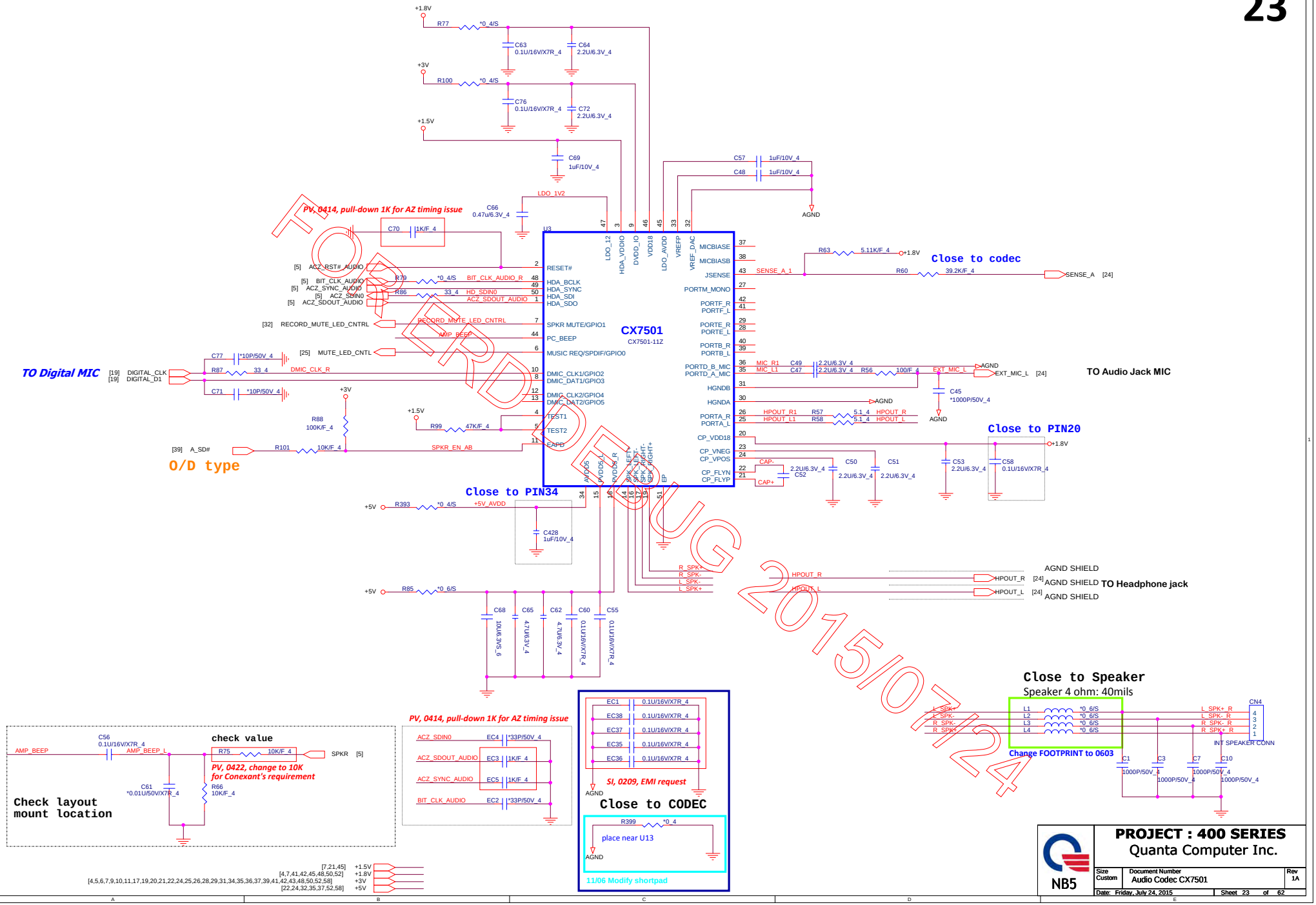
Audio Codec



NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
Size: Custom	Document Number: Audio Codec CX7501	Rev: 1A
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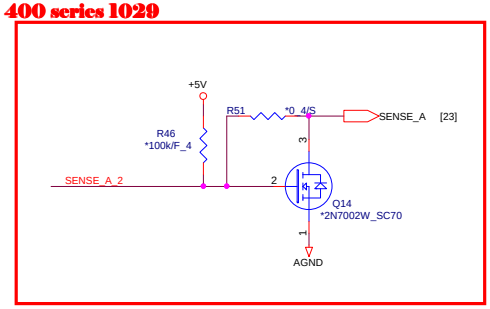
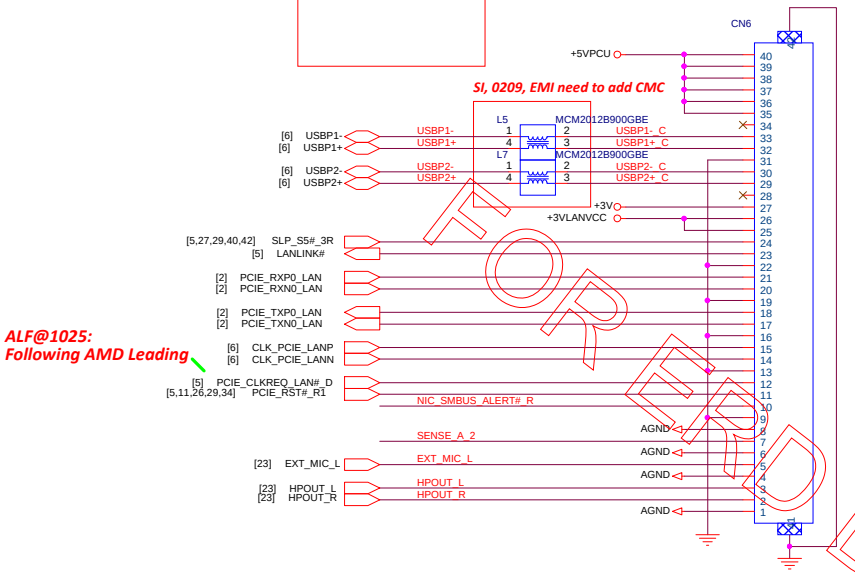
USB2.0 x2/LAN/Headphone_Mic Combo Jack Daugther Board Connector

PVR, 0720, delete USB 0 ohm co-lay

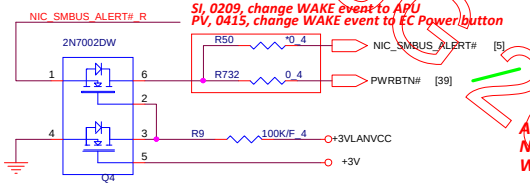
400 series 1029



SI, 0209, EMI need to add CMC



ALF@1025:
Following AMD Leading



SI, 0209, change WAKE event to APU
PV, 0415, change WAKE event to EC Power button

ALF@1031:
HP requested LAN PCIE wake to PWRBTN#

ALF@1031:
Needs to add 1 Pin for LAN Link to FCH.
Waiting for discussing with internal team

NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
Size: Custom	Document Number: Audio/USB BOARD	Rev: 1A
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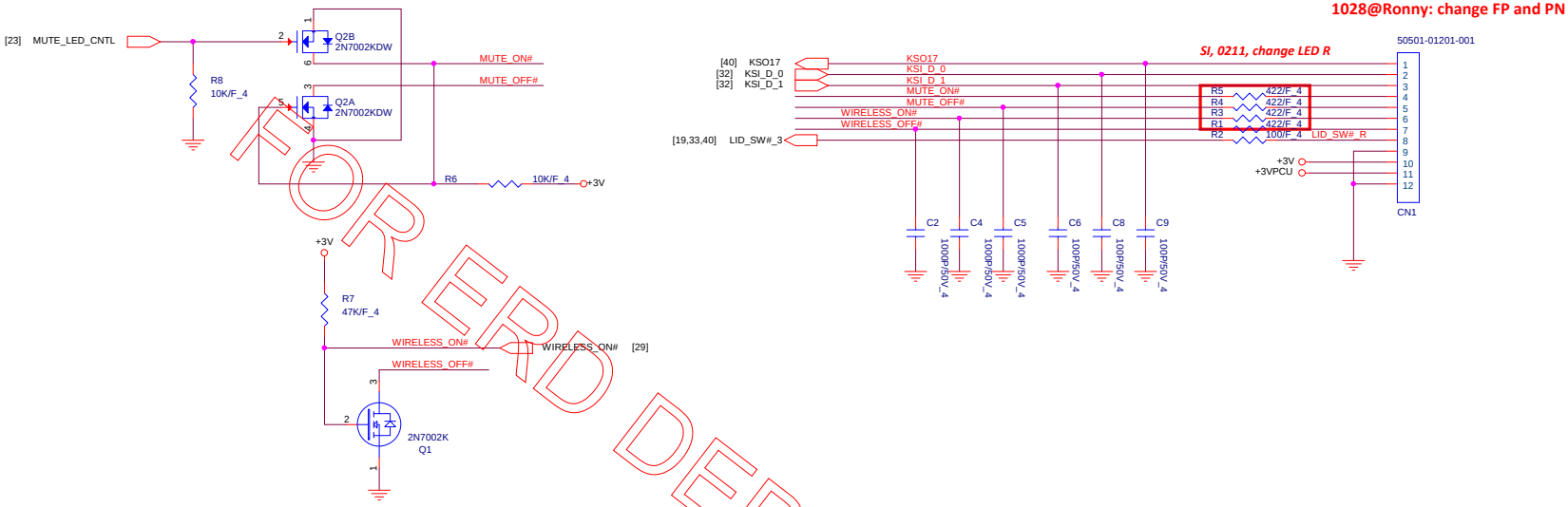

NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
Size: Custom	Document Number: Function Conn./LED	Rev: 1A
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TPM (1.2 or 2.0)

ALF@1031:
Changed Power Nameing
1023@Ronny: follow Leading platform

1023@Ronny: follow Leading platform

ALF@1031:
Changed Power Nameing

SI, 0117, unstuff for double PU

ALF@1106:
When CZ, Stuff Q1

ALF@1106:
When CZ-L, Stuff R1

ALF@1118:
Following AMD Leading DB1.

ALF@1119:
Updated the QCI P/N

PV, 0415, update TPM PN with 06.40 FW

Need apply PN

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Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: TPM SLB9665_QFN
Rev: 1A	
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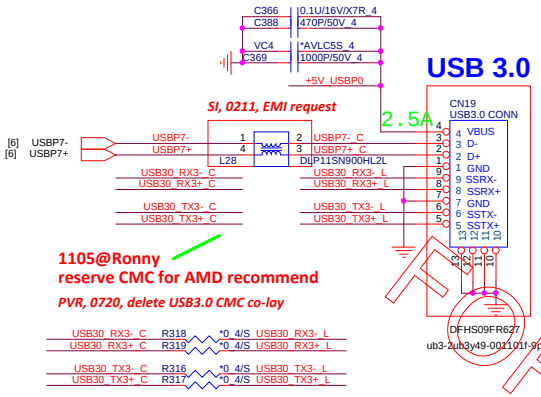
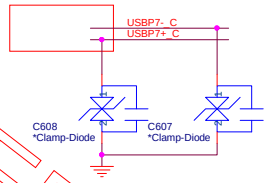
USB 2.0/3.0 Combo

USB 3.0 (Lower Left)

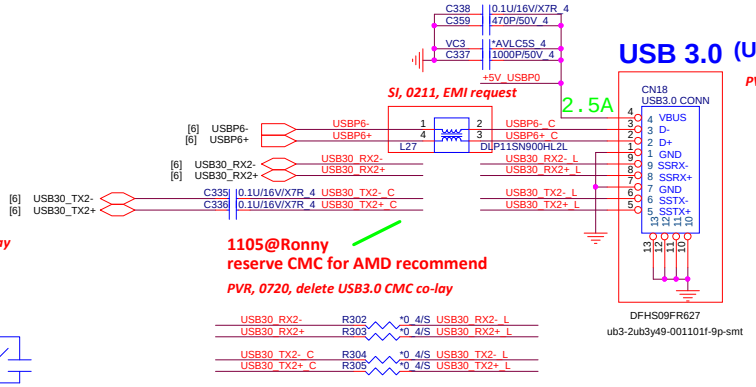


PV, 0416, change FP for SMT

SI, 0211, EMI request
PVR, 0720, delete USB2.0 0ohm co-lay

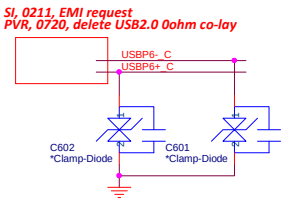


USB 3.0 (Upper Left)

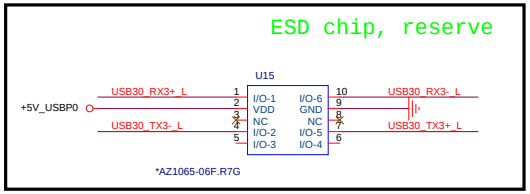


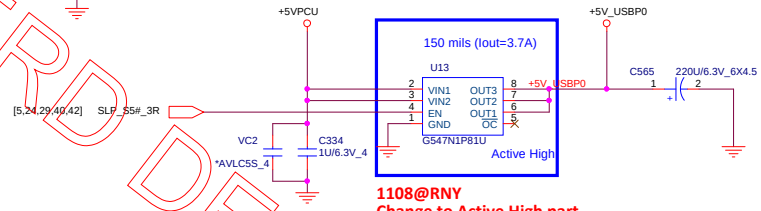
PV, 0416, change FP for SMT

SI, 0211, EMI request
PVR, 0720, delete USB2.0 0ohm co-lay



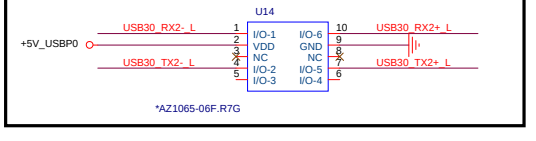
ESD chip, reserve





1108@RNY
Change to Active High part

ESD chip, reserve



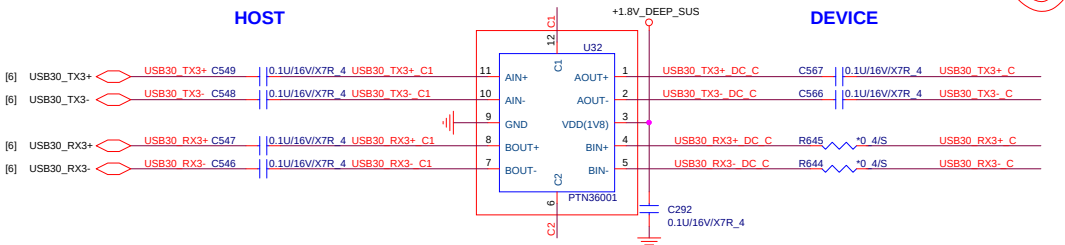
USB3.0

USB3.0 Re-driver IC

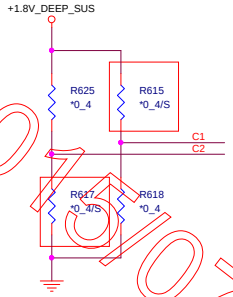
1016: Alfred
Added USB3.0 Re-driver for Lower Left.

USB3.0 re-driver IC

1121@RNY
Change USB3.0 redriver to NXP solution



PV, 0420, change to new Rev. re-driver IC PN



SI, 0203, fine tune re-driver setting

Table 4. C1 pin controls long/medium/short traces

State	Channel type	Pin C1 state	Channel B	Channel A	
			EQ[1]	DE[2]	OS[3]
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

Table 5. C2 pin controls long/medium/short traces

State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ[1]	DE[2]	OS[3]
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

USB3.0 bypass 0 ohm

1112@ALF
Deleted the bypass way, due to the space limitation.

Layout Notes:
Stubs Trace less than 150mil

[24,31,34,43,44,45,46,47,48,50,52,53,55,56,58] +5VPCU
[7,25,32,33,35,36,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU
[7,42,46,52,61] +1.8V_DEEP_SUS

NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

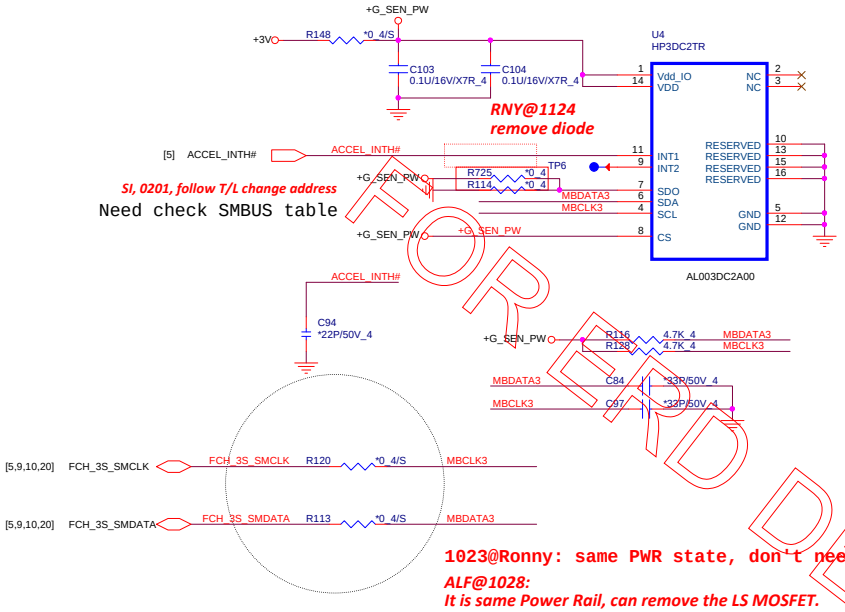
Size	Document Number	Rev
Custom	USB 3.0/USB3 Re-driver	1A

Date: Friday, July 24, 2015 Sheet 27 of 62

400 series 0930 Delete USB 3.0 redriver due to not support docking

Accelerometer Sensor

G-Sensor Power need check



1023@Ronny: same PWR state, don't need MOS?

ALF@1028:
It is same Power Rail, can remove the LS MOSFET.

Touch screen

ALF@1028:
HP Confirmed, 400 Series AMD does NOT support the Touch Screen.

1028@Ronny:
need change pin define

[24,27,31,34,43,44,45,46,47,48,50,52,53,55,56,58] +5VPCU
[7,25,32,33,35,36,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU

NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Accelerometer	1A
Date: Friday, July 24, 2015	Sheet 28 of 62	

NGFF WLAN/BT

Mini Card WLAN/BT(Option) 1.5A for WLAN

ALF@1031: following AMD Leading

SI, 0209, remove WLAN Power control MOS

RNY@1105: check the MOSFET Rating OK

ALF@1031: following AMD Leading

SI, 0209, remove WLAN reset control MOS

ALF@1031: following AMD Leading

NGFF Wifi/BT connector

CN15 — NGFF

400 series 0029

ALF@1031: It does NOT support WLAN_WAKE on 400 Series.

SI, 0203, EMI solution

PROJECT :	400 SERIES
	Quanta Computer Inc.
Size: Custom	Document Number: NGFF WLAN/BT
Rev:	1A
Date: Monday, July 27, 2015	Sheet 29 of 62

NB5

ALF@1025:
400 Series AMD does Not suppport the WWAN.
So, Del the related WWAN_DET# components.

RNY@1209:
400 Series AMD does Not suppport the M.2 SSD

NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	WWAN NGFF or SSD	1A
Date: Friday, July 24, 2015	Sheet 30 of 62	

H13 *O-X73A-4
H1 *H-C315I118D118P2
H17 *H-C315D118P2
H4 *h-c315i118d118p2
H15 *H-TC236BC138D138PT
H7 *H-TC236BC138D138PT
H14 *H-TC236BC138D138PT
H8 *H-TC236BC138D138PT
H5 *H-C315I118D118P2
H2 *H-C315I118D118P2
H6 *H-C315I118D118P2
H10 *O-X73A-2
H9 *H-TC276BC146D146PT
H16 *H-TC276BC146D146PT
H12 *H-C315D118P2
H20 *O-X73A-3
H23 *H-TC276BC315D118P2
H3 *O-0MBC-1
H18 *h-x73a-5
H19 *H-C315I118D118P2
H22 *h-c217d118p2
H21 *O-X73A-6
H24 *O-X73A-5
H25 *SPAD-RE39X513NP
H26 *SPAD-RE39X260NP
H27 *SPAD-RE39X615NP
H28 *O-X73A-7
H29 *O-X73A-8
PAD2 *spad-re276x236np
PAD1 *SPAD-RE236X236NP

EMI CAP

+3V
+5VPCU
C613 0.1U/16V/X7R_4
C614 0.1U/16V/X7R_4
C615 0.1U/16V/X7R_4

C611 C612 C622 C623
Clamp-Diode
ESDGND1
ESDGND2

PV, 0422, reserve one more ESD part at each ESDGND
PV, 0514, stuff varistor

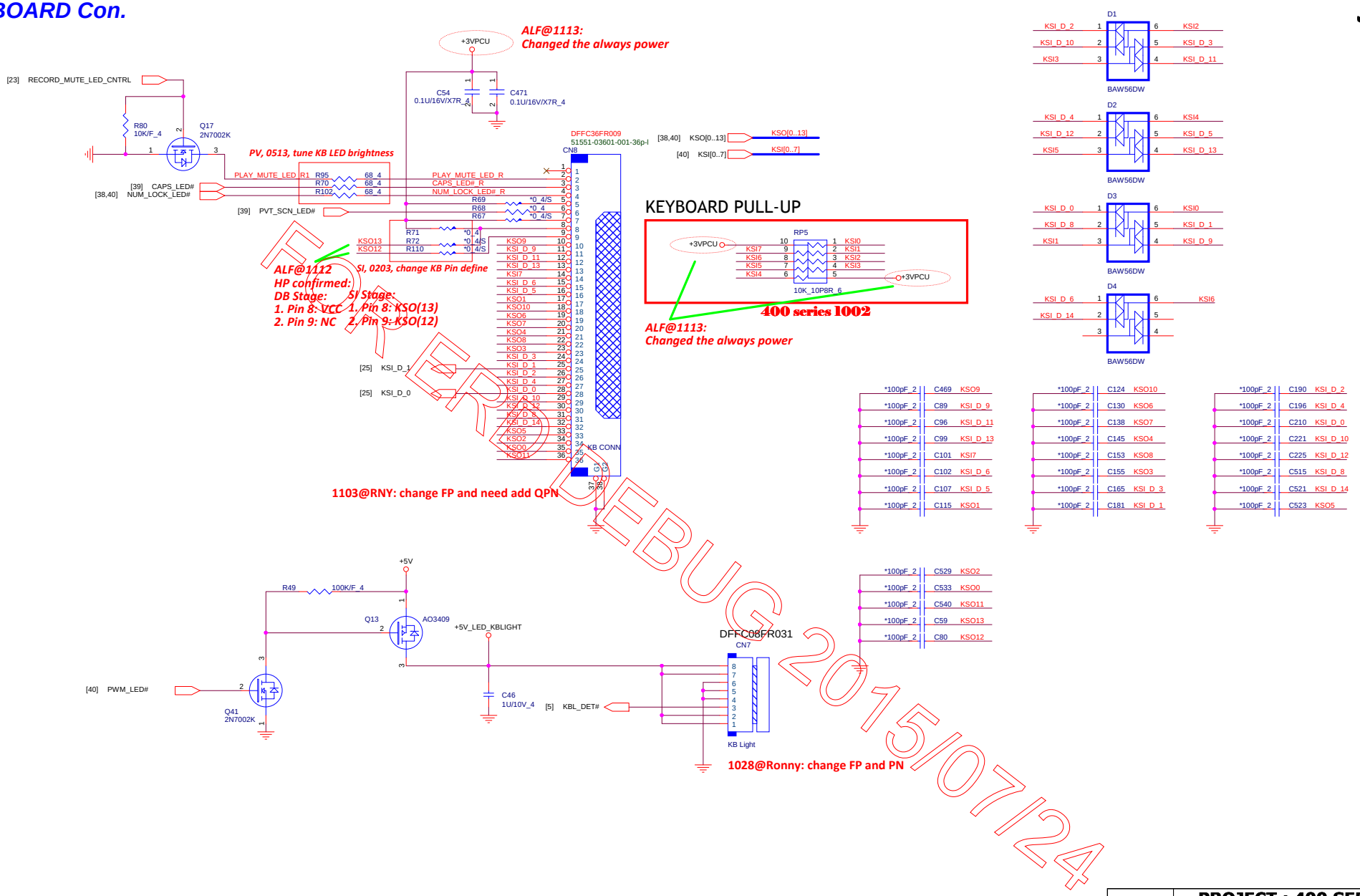
NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HOLE	1A

Date: Friday, July 24, 2015 Sheet 31 of 62

KEYBOARD Con.

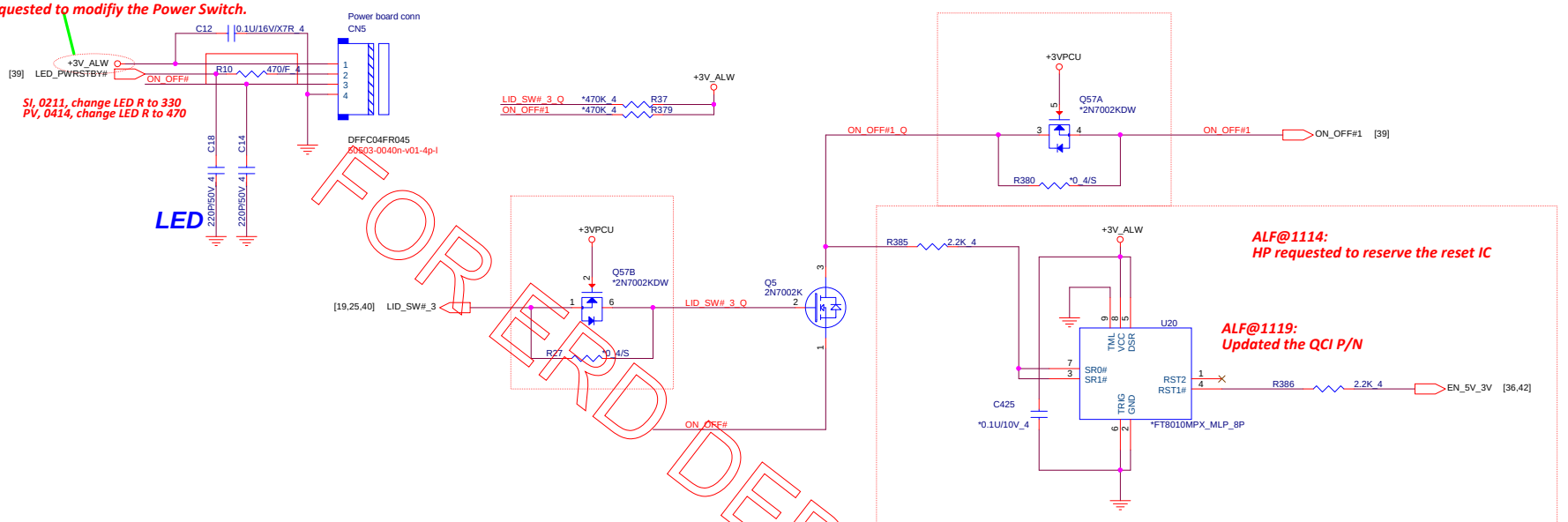


NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
Size: Custom	Document Number: KB/KB light	Rev: 1A
Date: Friday, July 24, 2015	Sheet 32 of 62	

Power Botton Connector

1112@RNY: change to 4Pin FP and PN

ALF@1115:
HP requested to modifiy the Power Switch.

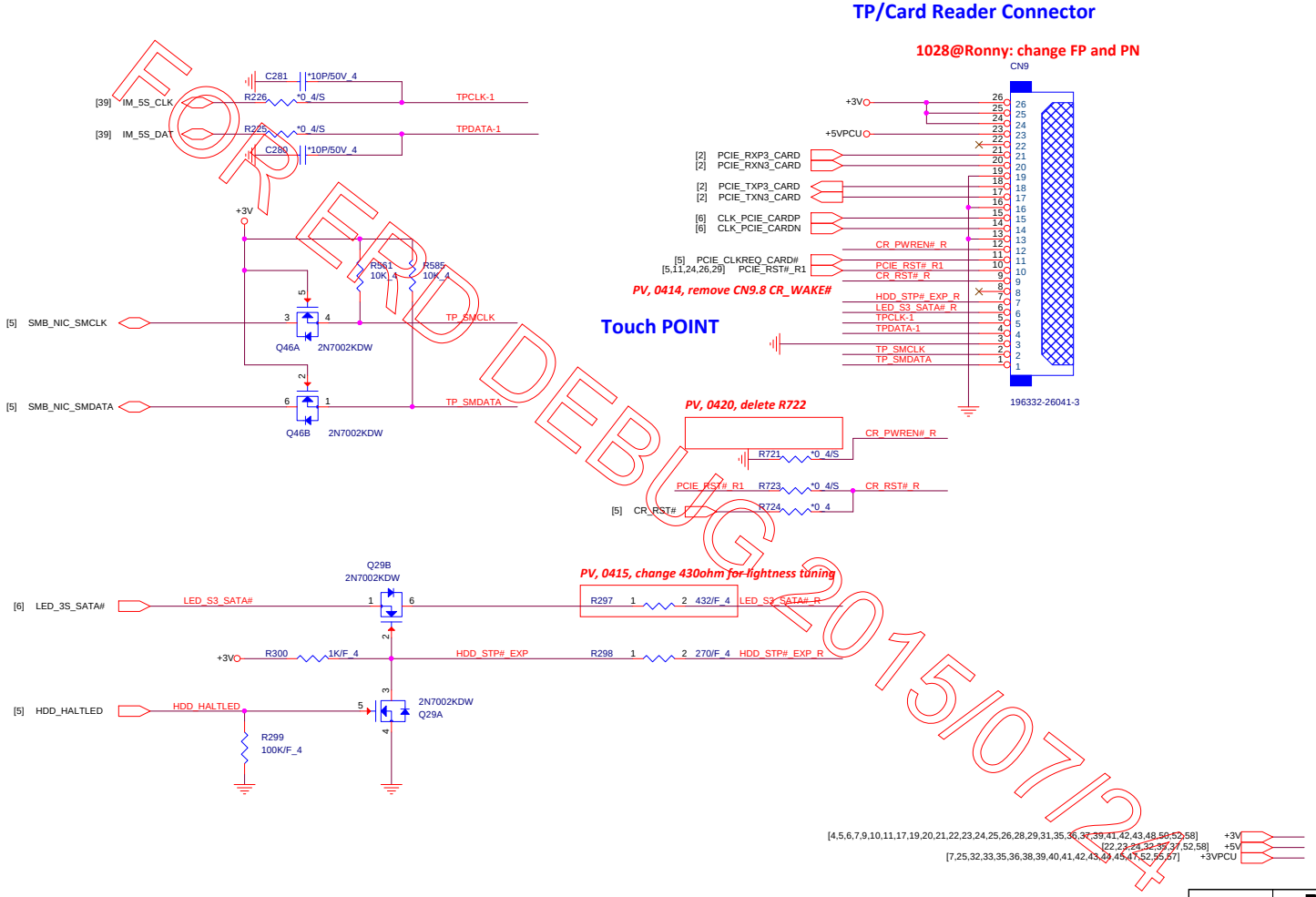


ALF@1114:
HP requested to reserve the reset IC

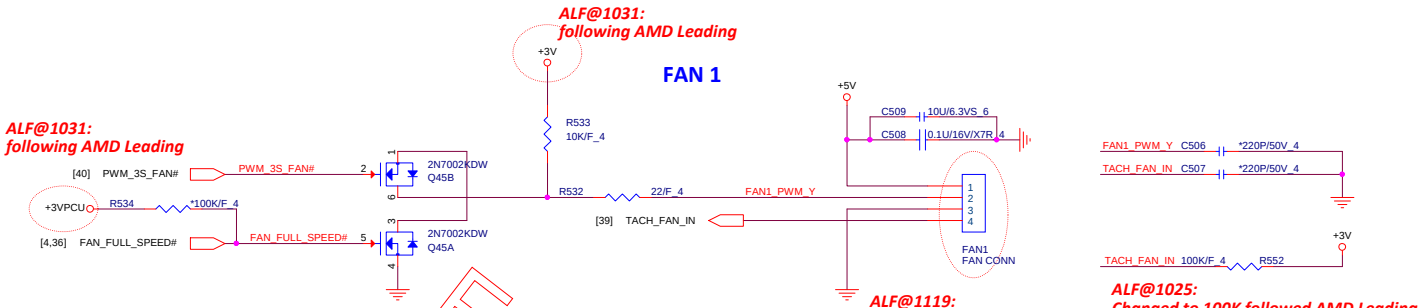
ALF@1119:
Updated the QCI P/N

[42,43,44,57] +3V_ALW
[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,35,36,37,39,41,42,43,48,50,52,58] +3V
[22,23,24,32,35,37,52,58] +5V
[7,25,32,35,36,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU

NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
Size: Custom	Document Number: 33 -- PB/LID	Rev: 1A
Date: Friday, July 24, 2015	Sheet 33 of 62	



NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
Size: Custom	Document Number: 34 -- Forced Pad/Card reader	Rev: 1A
Date: Friday, July 24, 2015	Sheet 34 of 62	



[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,36,37,39,41,42,43,48,50,52,58] +3V
[22,23,24,32,37,52,58] +5V
[7,25,32,33,36,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU
[24,27,31,34,43,44,45,46,47,48,50,52,53,55,56,58] +5VPCU

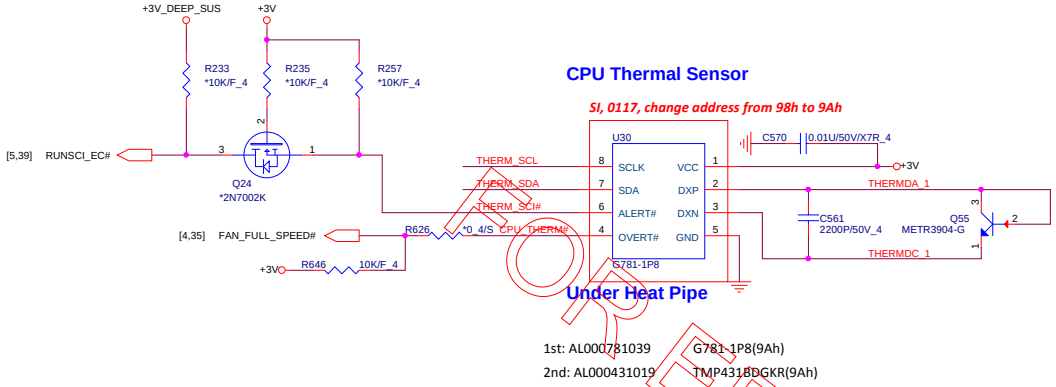
NB5

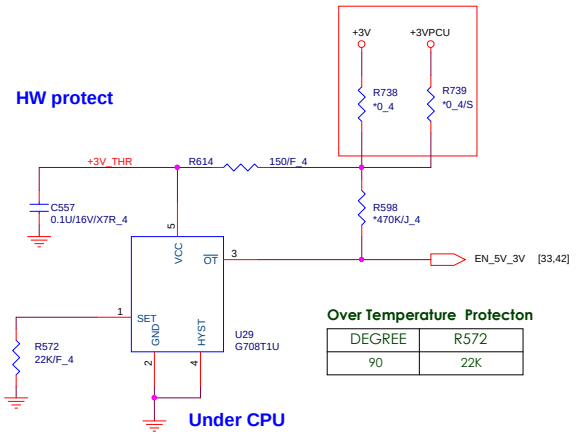
PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	35 -- FAN	1A
Date: Friday, July 24, 2015	Sheet 35 of 62	

Thermal sensor

PV, 0416, change HW thermal protect to +3VPCU

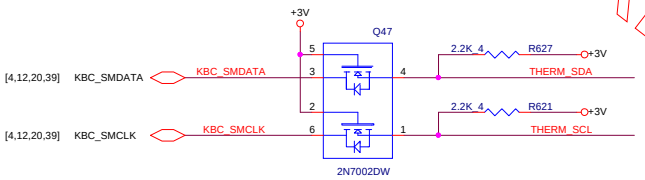




Over Temperature Protecton

DEGREE	R572
90	22K

RSET (K OHM) = 0.0012T^2 - 0.9308T + 96.147



[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,35,37,39,41,42,43,48,50,52,58] +3V
[7,25,32,33,35,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU

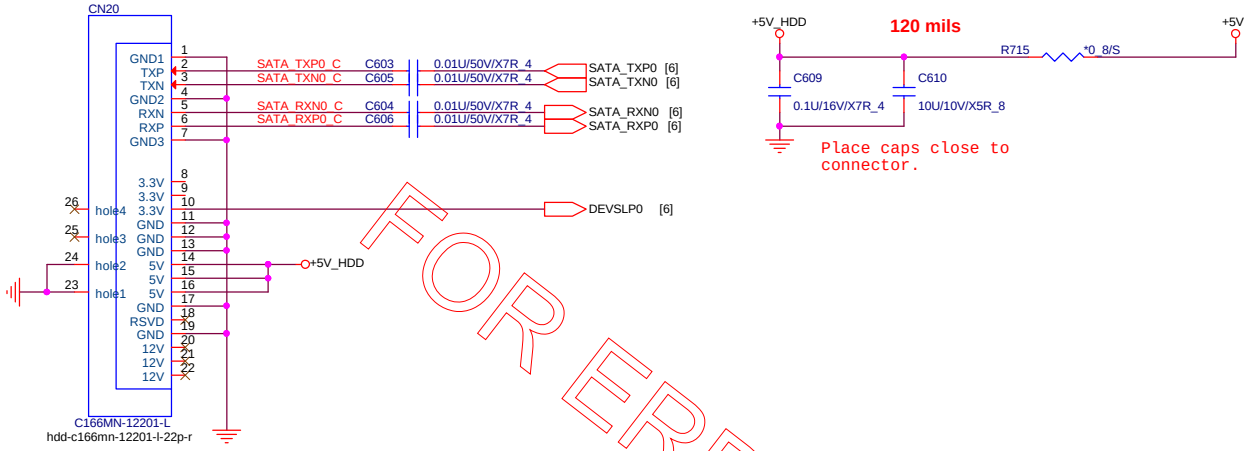
NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	36 -- Thermal IC	1A
Date: Friday, July 24, 2015	Sheet 36 of 62	

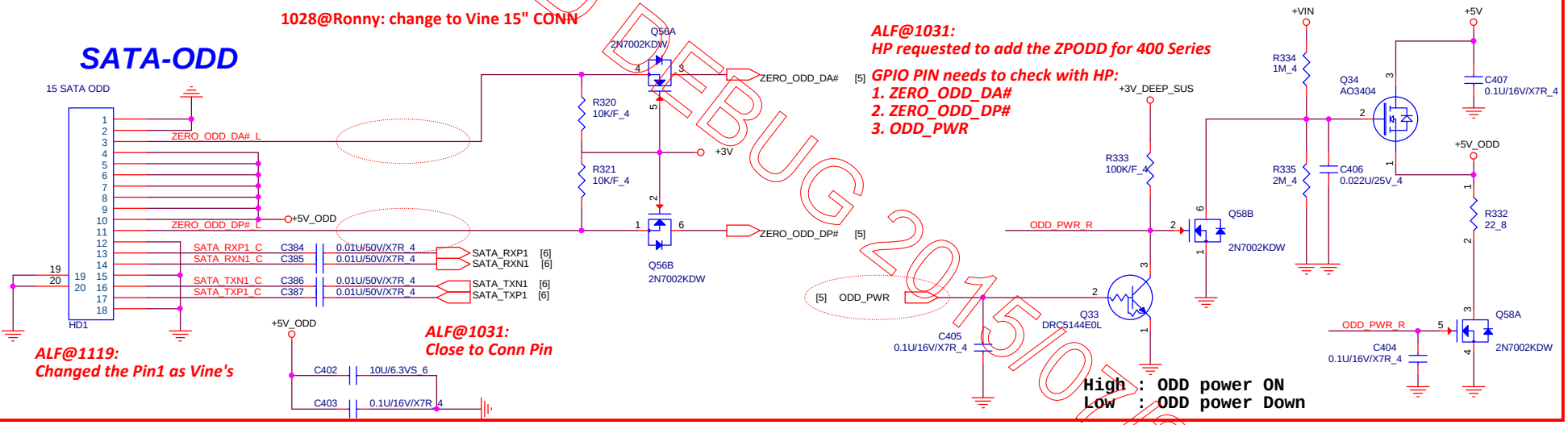
SATA-HDD

400 series 0929
Footprint and P/N TBD



1028@Ronny: change to Vine 15" CONN

SATA-ODD



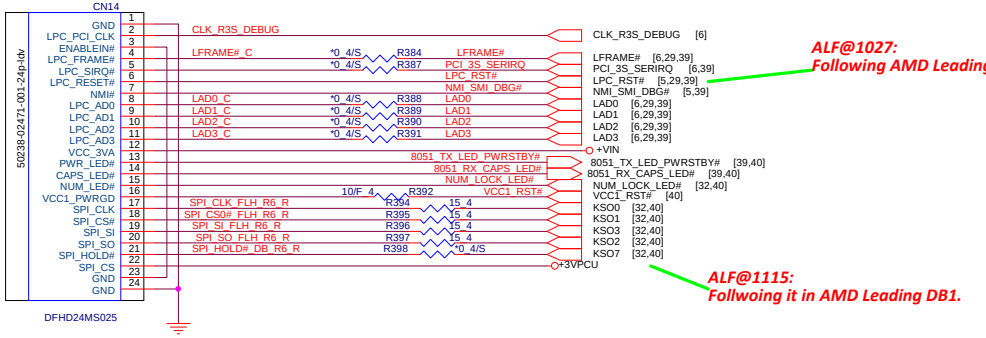
[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,35,36,39,41,42,43,48,50,52,58] +3V
[22,23,24,32,35,52,58] +5V
[7,25,32,33,35,36,38,39,40,41,42,43,44,45,47,52,55,57] +3VPCU

NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
B	37 -- HDD/ODD	1A
Date: Friday, July 24, 2015	Sheet 37 of 62	

EC debug conn.



ALF@1027:
Following AMD Leading.

ALF@1115:
Follwoing it in AMD Leading DB1.

1028@Ronny: change PN to DFHD24MS025

NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	38 -- EC debug conn	1A
Date: Friday, July 24, 2015	Sheet 38 of 62	

400 series 1001 change to NPCE586H_TQFP

ALF@1025:
RTC naming is same as APU's.

Need apply P/N and footprint

ALF@1027:
Following AMD Leading.

for Battery charge/charge

for Thermal IC/ APU, GPU Thermal

U27A

NPCE586H_TQFP

SI, 0209, follow T/L change SHD_DIO2_NE to Pin#123

ALF@1115: T/L DB2
SI, 0201, change LOW_BAT# power state to +3V_DEEP_SUS
PV, 0414, change LOW_BAT# power state to +3V, and connect to NMI_SMI_DBG#
PV, 0415, remove LOW_BAT# reserved pull-up +3VPCU

RNY@1105:
HP request to add SPI_WP to SPI

SI, 0209, AMD no PECI feature, R655 un-stuff

ALF@1025:
Follow AMD Leading 4.7uF.
SI, 0209, change CAP from 4.7u to 1u

ALF@1119:
Updated the QCI P/N

NOTE:
Place a 1 uF capacitor as close to the CAP pin as possible.

NOTE:
Connect GND and AGND planes via an 0R resistor or a one-point layout connection.

ALF@1031:
Needs to confirm EC Vendor, if use +3VPCU, will it has leakage for APU from SPI Bus?
CZ, should be OK!!
CZ-L, it is bypass, need to check?

ALF@1025:
Need to confirm with HP?
Leading is used P3V3DS.

DS=Always Power

Reserve for Pointing Stick

A=S5 Power

SI, 0209, Add FCH_WAKE#_EC PU to +3V_DEEP_SUS same as APU side

Reserve for USB Charging

SI, 0209, remove R378 pull down

ALF@1115:
following Leading DB1

ALF@1115:
T/L DB1

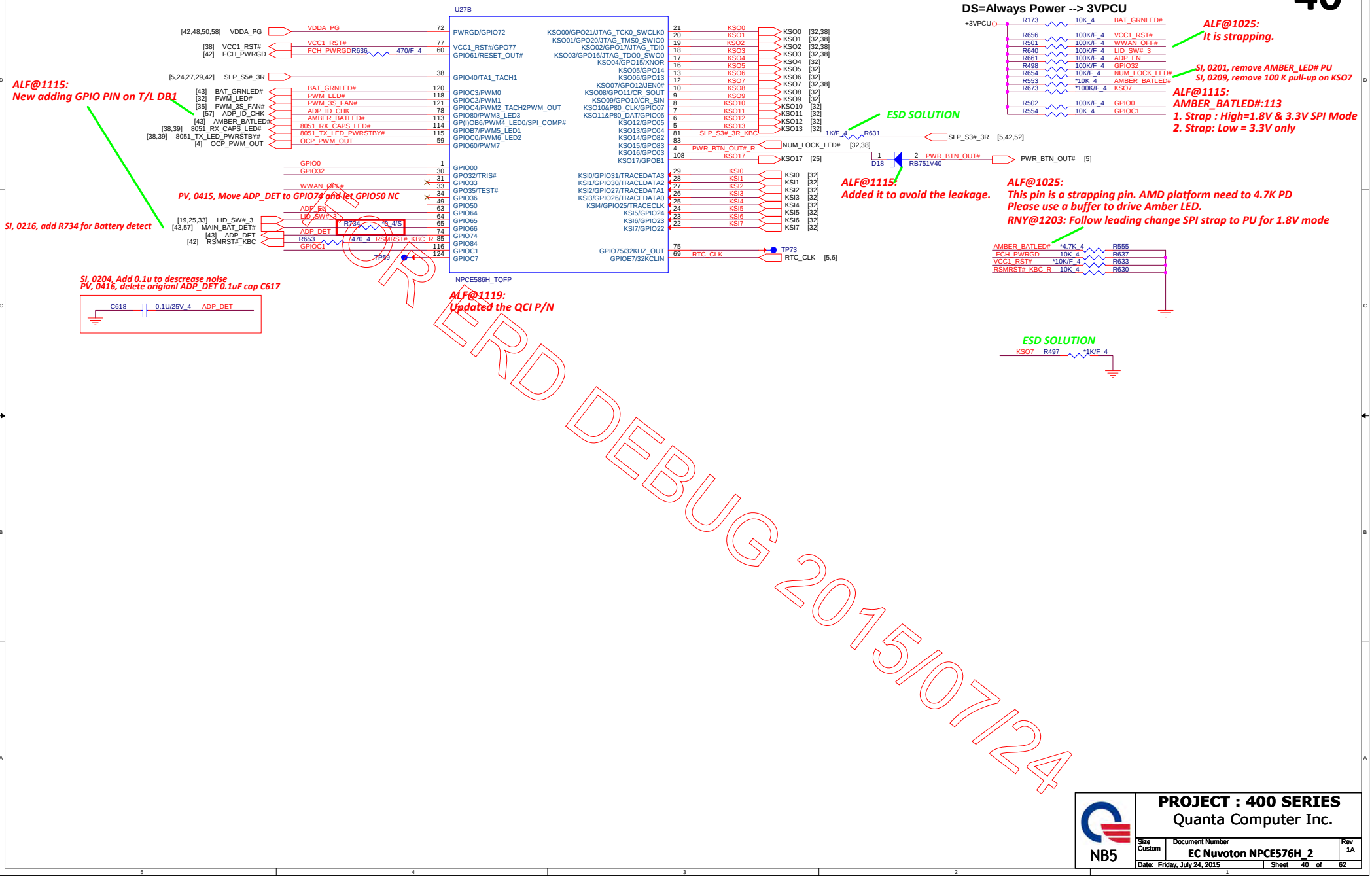
ALF@1028: for PLT_DET#
DIS --> PU
UMA --> PD

ALF@1025:
Needs Pull Always Power

ALF@1115:
Swapped EC GPIO PIN Notes: (following Leading DB1)
1. PLT_DET# from 39 to 102
2. TACH_FAN_IN from 101 to 128
3. KBC_SPI_SI_IN from 128 to 101
4. KBC_SPI_CLK from 3 to 99
5. ADP_PRES_OUT from 99 to 3
6. KBC_PWR_ON from 100 to 127
7. PVT_MOSI from 127 to 100
8. FCH_WAKE#_EC from 103 to 93
9. PVT_SCLK_R from 2 to 98
10. VOLTAGE_ADC from 41 to 39
11. ADP_DET from 31 to 49
12. MAIN_BAT_DET# from 102 to 65
13. New adding for ADP_ID_CHK at 78

PROJECT	400 SERIES
Quanta Computer Inc.	
Size	Custom
Document Number	EC Nuvoton NPCE576H_1
Rev	1A
Date	Friday, July 24, 2015
Sheet	39 of 62
NB5	

400 series 1001 change to NPCE586H_TQFP

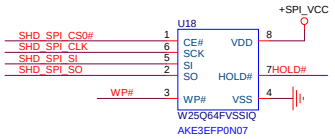


NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
Size: Custom	Document Number: EC Nuvoton NPCE576H_2	Rev: 1A
Date: Friday, July 24, 2015	Sheet 40 of 62	

APU SPI ROM

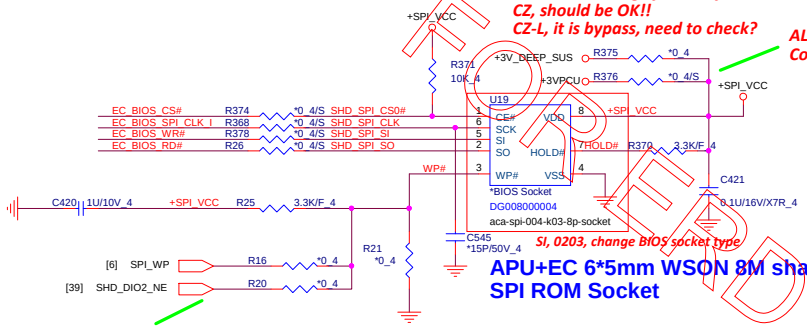
Vender	Size	P/N (3.3V)	
WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
GGD	8M	AKE2EZN0Q00	GD25B64CSIGR
	8M		
Socket		DG008000004	

U18&U19 footprint 要重疊



ALF@1031:
Needs to confirm EC Vendor, if use +3VPCU, will it has leakage for APU from SPI Bus?
CZ, should be OK!!
CZ-L, it is bypass, need to check?

ALF@1113:
Confirmed HP, SPI Power Rail same as EC.



SI, 0203, change BIOS socket type

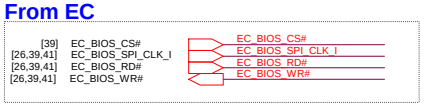
APU+EC 6*5mm WSON 8M share SPI ROM Socket

ALF@1103:
HP request to add SPI_WP to SPI

Alfred@1015:
Add flash ROM for first bring up (2MB ROM)
EC 6*5mm WSON 8M
SPI ROM Socket

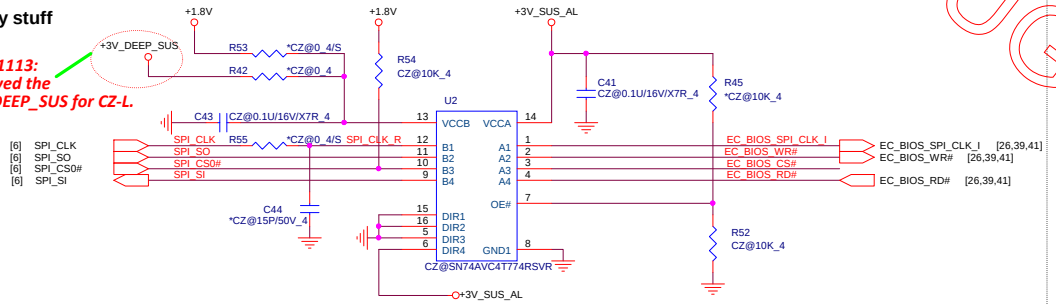
SI, 0203, remove EC debug ROM

From EC

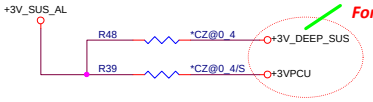


CZ only stuff

ALF@1113:
Reserved the +3V_DEEP_SUS for CZ-L.

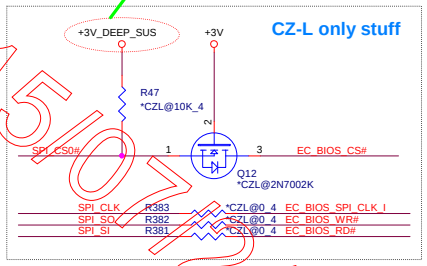


OE#	DIR	OPERATION
L	L	B TO A
L	H	A TO B
H	X	Disconnect



ALF@1113:
For CZ-L, useed the +3V_DEEP_SUS firstly

ALF@1113:
1. SPI bus isolation to FCH



NB5

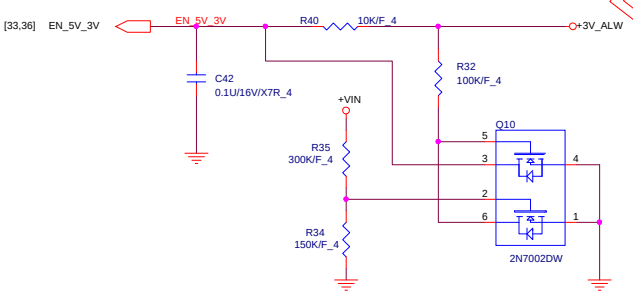
PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Flash(KBC+PCH)	1A
Date: Friday, July 24, 2015	Sheet 41 of 62	

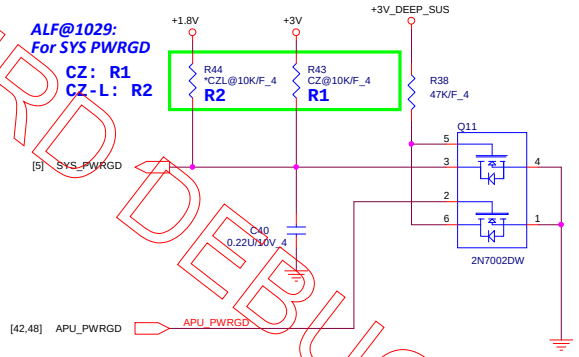
POWER TO EE NET NAME CONNECTION For AMD

ALF@1114:
Deleted the circuit of PWROK Generate followed T/L Leading.

ALF@1029:
For Power Enable



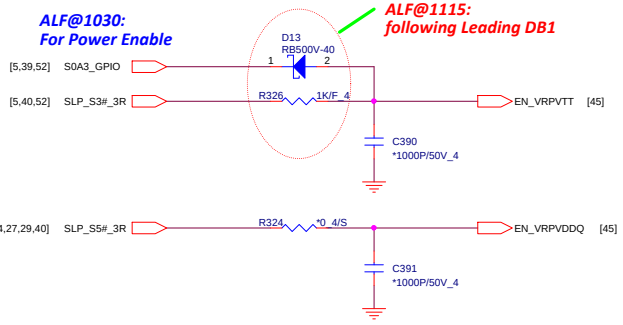
ALF@1029:
For SYS PWRGD
CZ: R1
CZ-L: R2

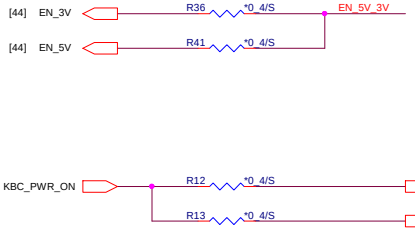


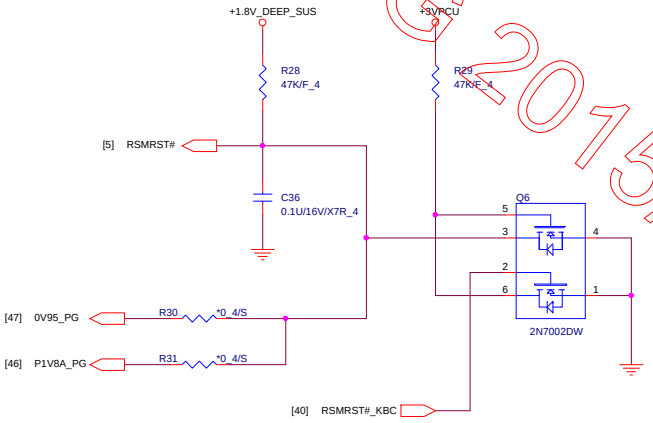
ALF@1030:
For System PG

ALF@1030:
For Power Enable

ALF@1115:
following Leading DB1





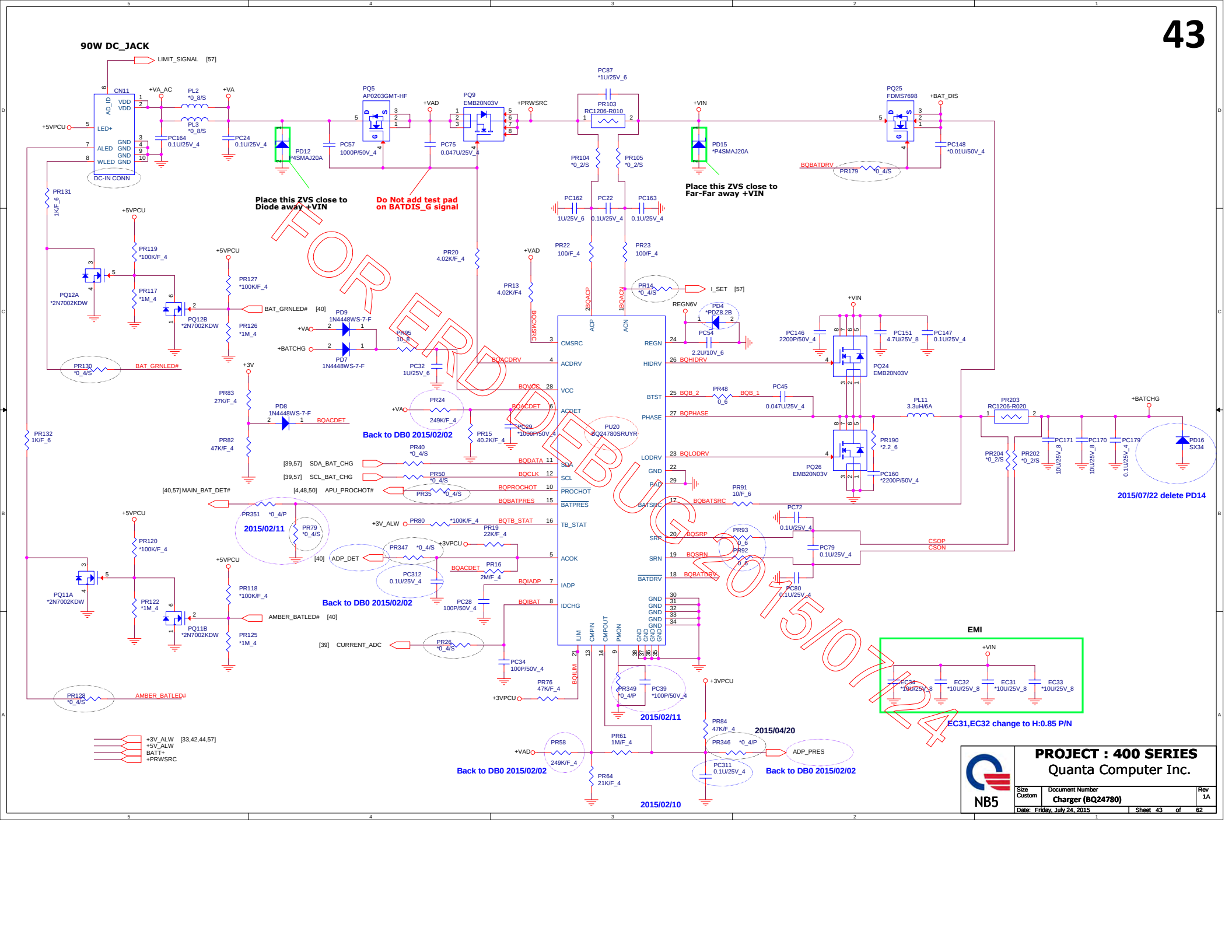


NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	60 -- Commercial Debug card	1A
Date: Friday, July 24, 2015	Sheet 42 of 62	

90W DC_JACK



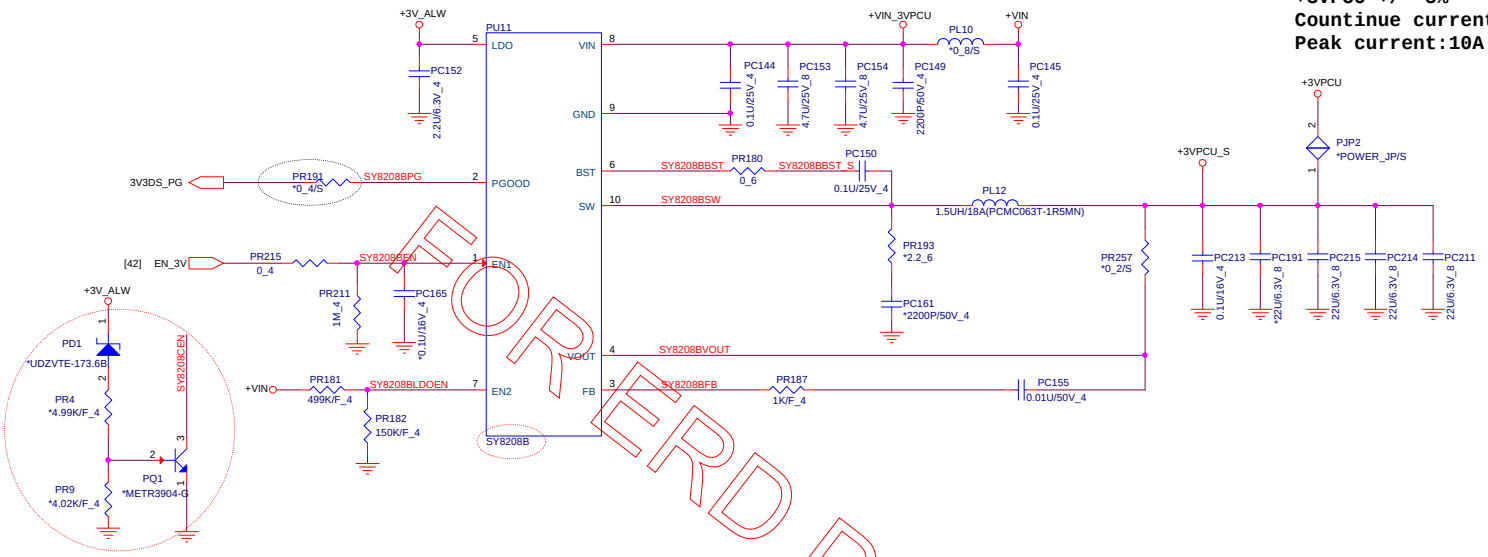
NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
Size: Custom	Document Number: Charger (BQ24780)	Rev: 1A
Date: Friday, July 24, 2015	Sheet 43 of 62	

DC/DC +3VS5/+5VS5

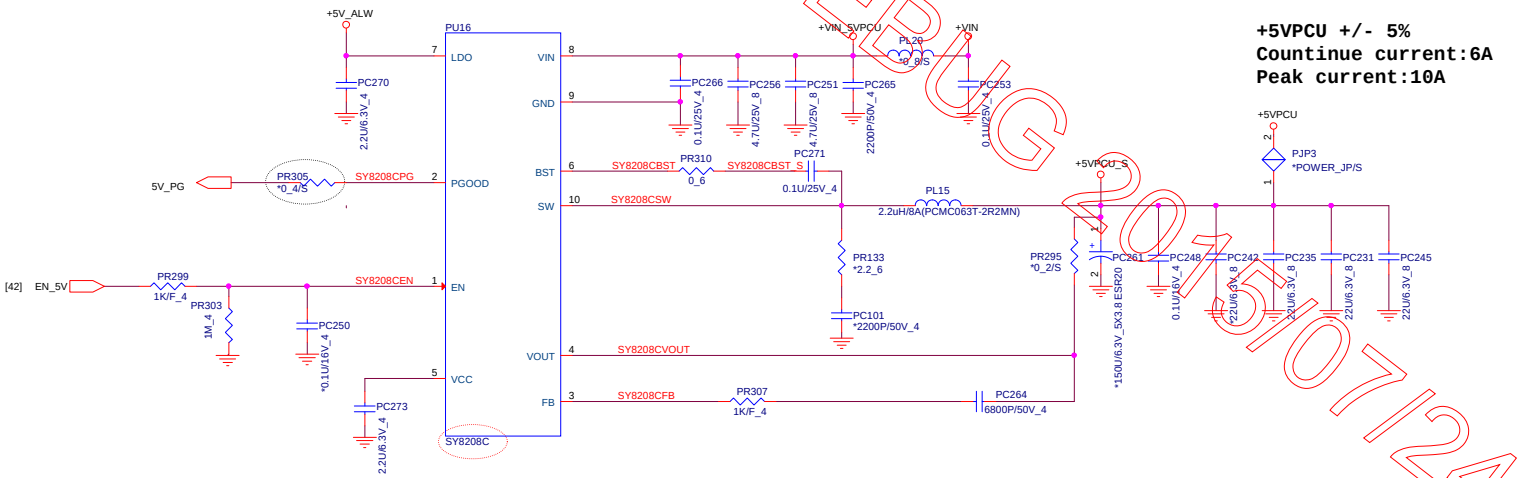
Do Not add test pad on +3VPCU

+3VPCU +/- 5%
Countinue current:6A
Peak current:10A

+3VPCU [7,25,32,33,35,36,38,39,40,41,42,43,45,47,52,55,57]
+5VPCU [24,27,31,34,43,45,46,47,48,50,52,53,55,56,58]



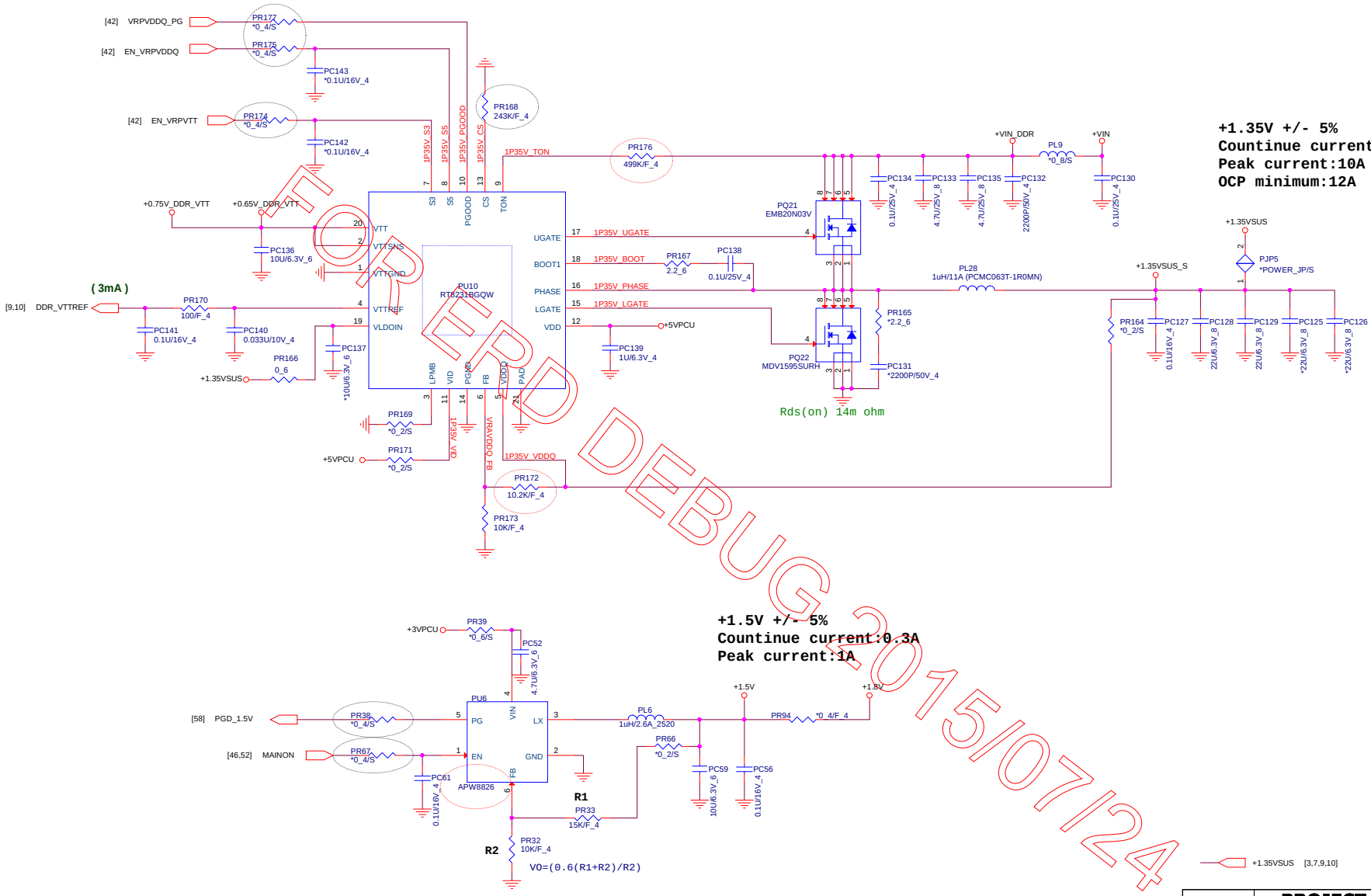
+5VPCU +/- 5%
Countinue current:6A
Peak current:10A



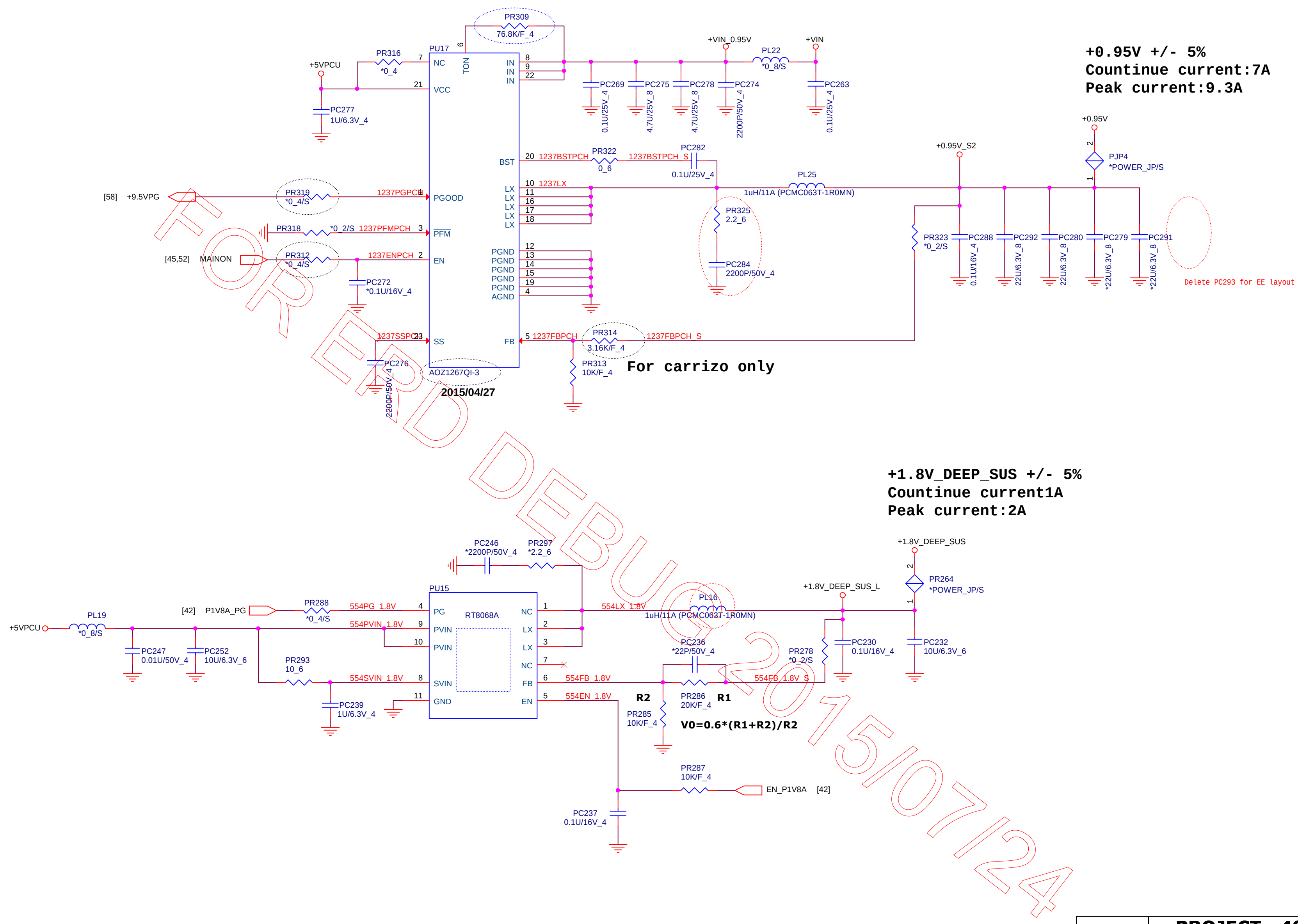
NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VPCU(RT8243A)	1A
Date: Friday, July 24, 2015	Sheet 44 of 62	



PROJECT : 400 SERIES	
Quanta Computer Inc.	
Size: NB5	Document Number: DDR3 (RT8231B)/1.8VS5
Rev: 1A	
Date: Friday, June 26, 2015	Sheet: 45 of 62


+0.95V +/- 5%
Countinue current:7A
Peak current:9.3A
PU17
AOZ1267QI-3
2015/04/27
PR309 76.8K/F_4
PR316 *0_4
+5VPCU
PC277 1U/6.3V_4
+VIN_0.95V
+VIN
PL22 *0_8/S
PC269 0.1U/25V_4
PC275 4.7U/25V_8
PC278 4.7U/25V_8
PC274 2200P/50V_4
PC263 0.1U/25V_4
+0.95V
PJP4 *POWER_JP/S
+0.95V_S2
PR322 0_6
PC282 0.1U/25V_4
1237BSTPCH
1237BSTPCH_S
1237LX
PL25 1uH/11A (PCMC063T-1R0MN)
PR325 2.2_6
PC284 2200P/50V_4
PR323 *0_2/S
PC288 0.1U/16V_4
PC292 22U/6.3V_8
PC280 22U/6.3V_8
PC279 *22U/6.3V_8
PC291 *22U/6.3V_8
Delete PC293 for EE layout
[58] +9.5VPG
PR319 *0_4/S
1237PGPCH
PR318 *0_2/S
1237PFMPCH
[45,52] MAINON
PR312 *0_4/S
1237ENPCH
PC272 *0.1U/16V_4
1237SSPCH
PC276 2200P/50V_4
1237FBPCH
PR314 3.16K/F_4
1237FBPCH_S
PR313 10K/F_4
For carrizo only
FOR ERD DEBUG 2015/07/24
+1.8V_DEEP_SUS +/- 5%
Countinue current1A
Peak current:2A
PU15
RT8068A
PC246 *2200P/50V_4
PR297 *2.2_6
[42] P1V8A_PG
PR288 *0_4/S
554PG_1.8V
554PVIN_1.8V
554SVIN_1.8V
+5VPCU
PL19 *0_8/S
PC247 0.01U/50V_4
PC252 10U/6.3V_6
PR293 10_6
PC239 1U/6.3V_4
554LX_1.8V
PL16 1uH/11A (PCMC063T-1R0MN)
+1.8V_DEEP_SUS_L
+1.8V_DEEP_SUS
PR264 *POWER_JP/S
PC236 *22P/50V_4
PR278 *0_2/S
PC230 0.1U/16V_4
PC232 10U/6.3V_6
554FB_1.8V
554FB_1.8V_S
554EN_1.8V
R2
R1
PR286 20K/F_4
PR285 10K/F_4
VO=0.6*(R1+R2)/R2
PR287 10K/F_4
EN_P1V8A [42]
PC237 0.1U/16V_4

+VIN [19,37,38,42,43,44,45,47,49,51,54,56]
+3VPCU [7,25,32,33,35,36,38,39,40,41,42,43,44,45,47,5
+5VPCU [24,27,31,34,43,44,45,47,48,50,52,53,55,56,58]

PROJECT : 400 SERIES

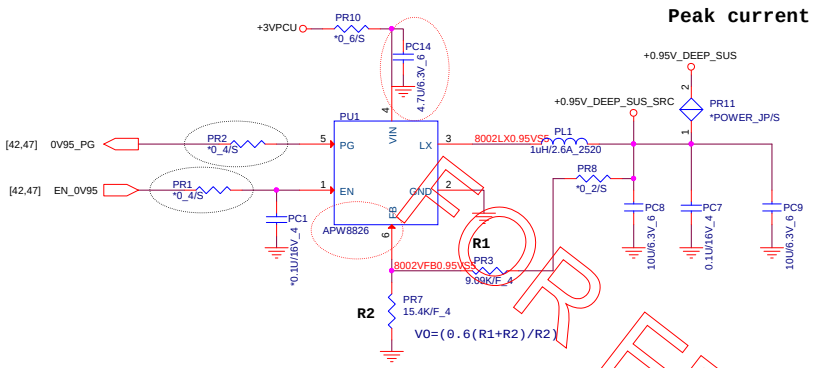
Quanta Computer Inc.

NB5

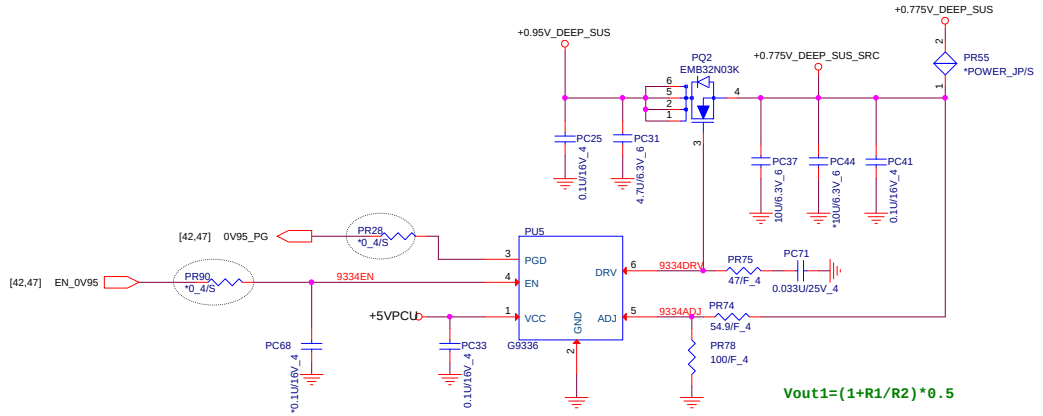
Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	1A

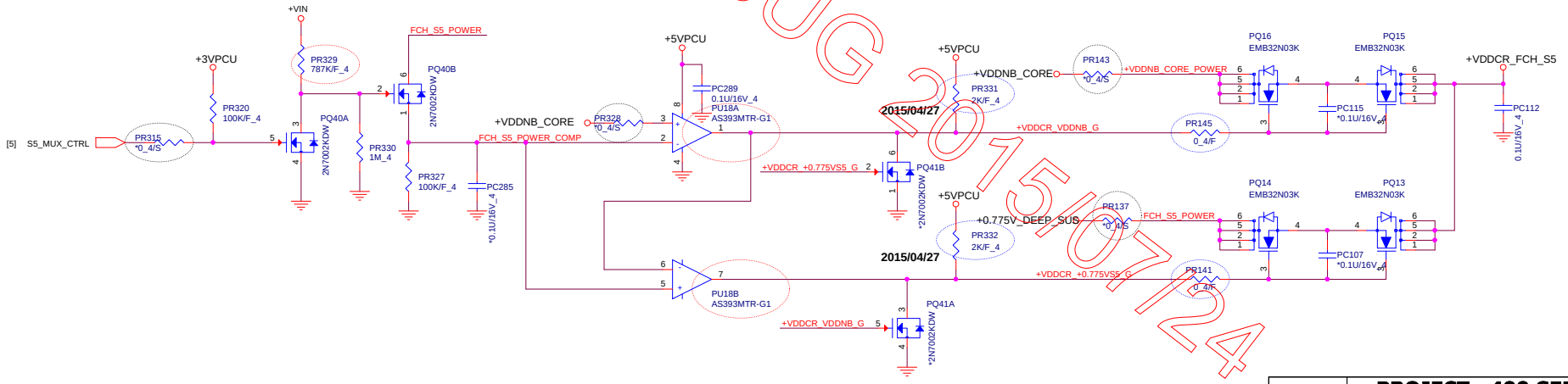
Date: Friday, July 24, 2015 Sheet 46 of 62

+0.95V_DEEP_SUS +/- 5%
Countinue current:1A
Peak current:2A



+0.775V_DEEP_SUS +/- 5%
Countinue current:1A
Peak current:2A

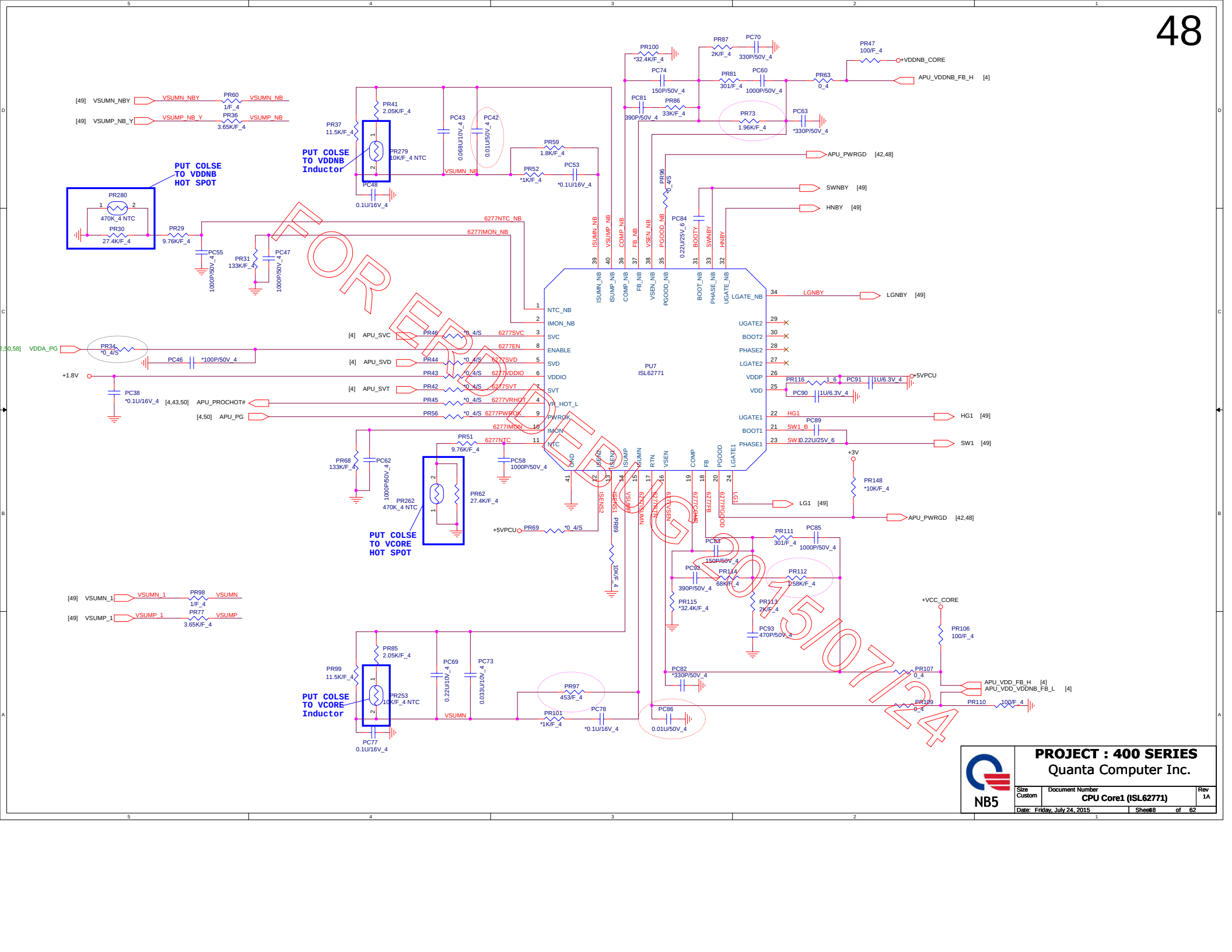




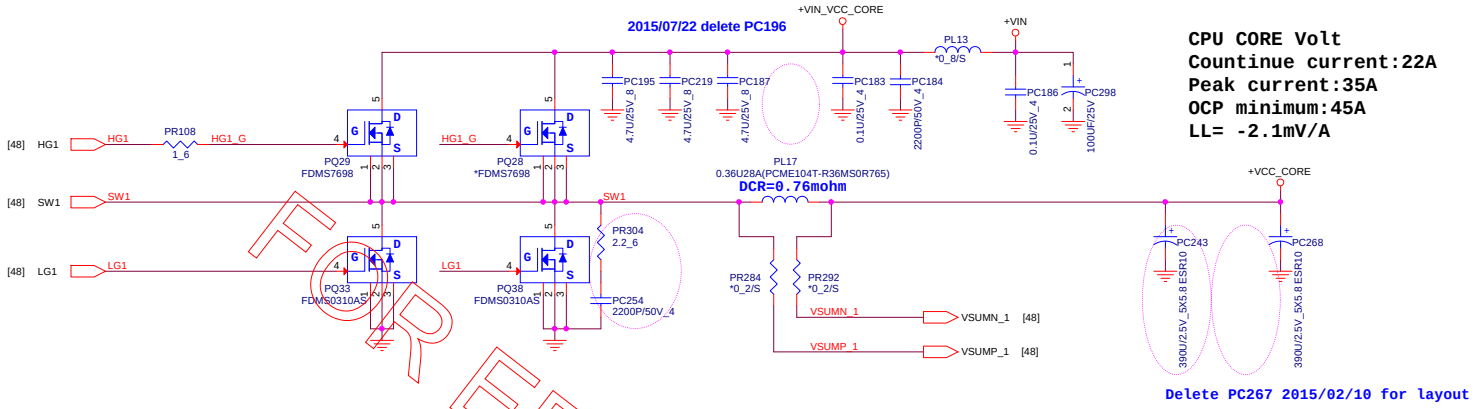
PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
	+VCC_IO (NB681)	1A
Date: Friday, June 26, 2015	Sheet 47 of 62	

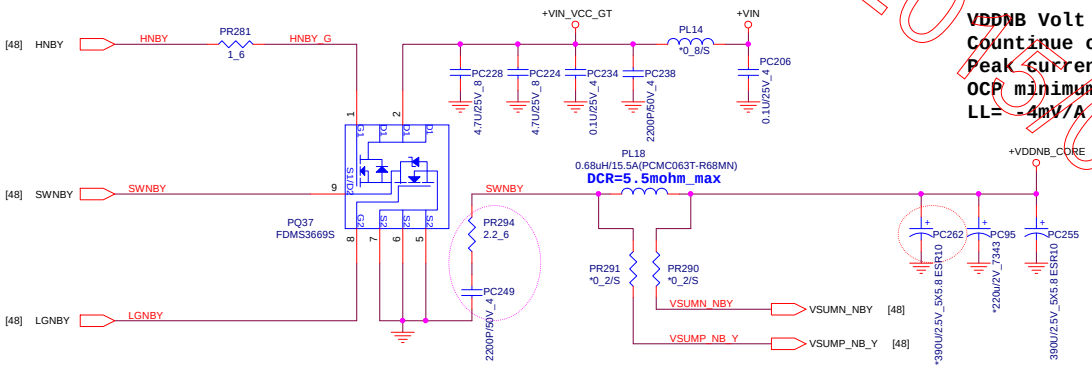
NB5



PROJECT : 400 SERIES	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: CPU Core1 (ISL62771)
Rev: 1A	
Date: Friday, July 24, 2015	Sheet 48 of 62



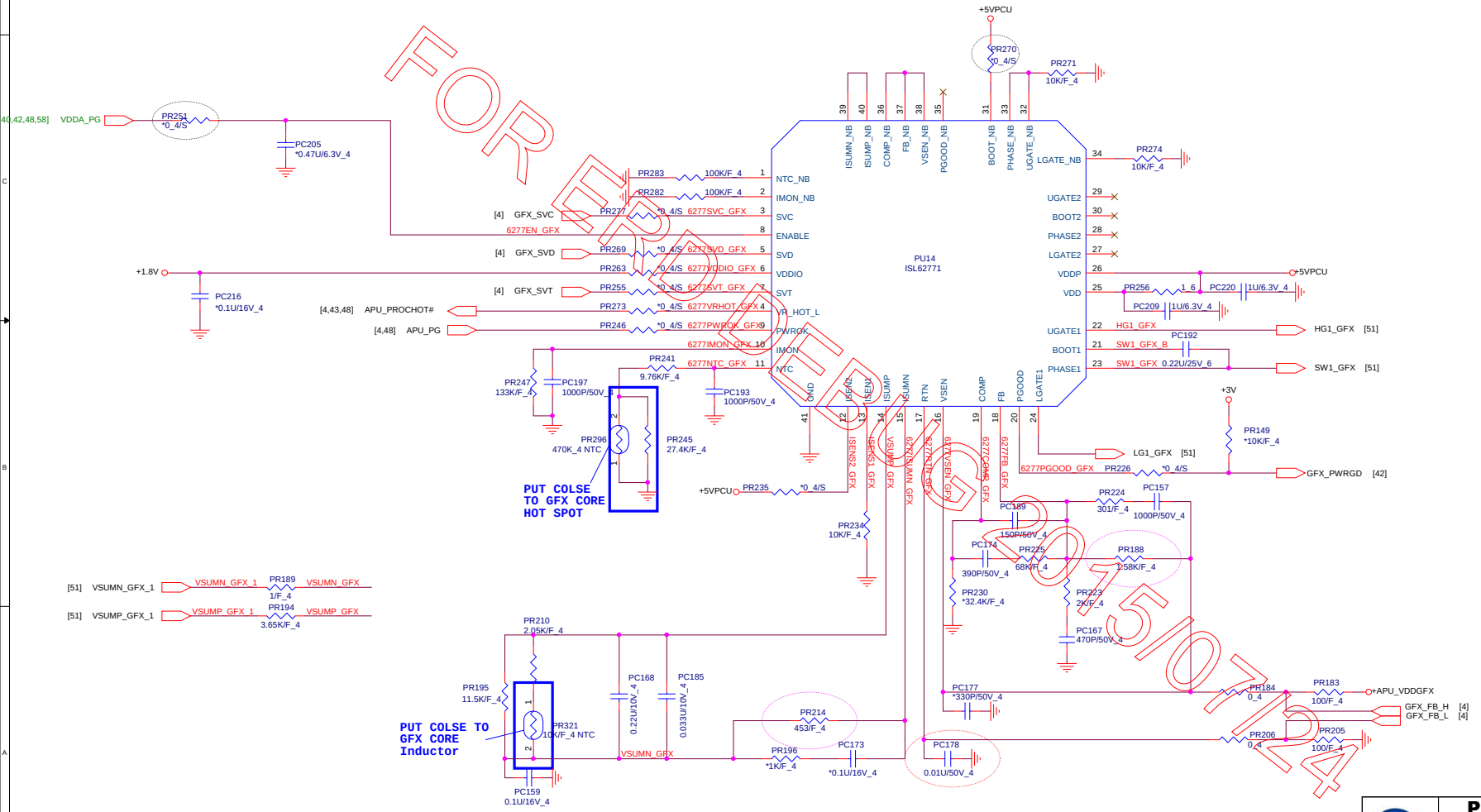
CPU CORE Volt
Countinue current:22A
Peak current:35A
OCP minimum:45A
LL= -2.1mV/A



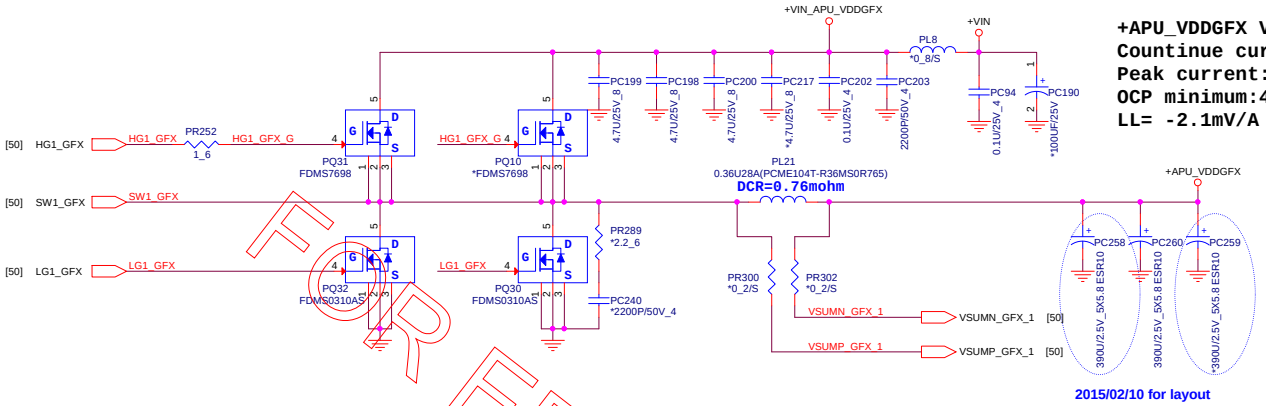
VDDNB Volt
Countinue current:12A
Peak current:17A
OCP minimum:22A
LL= -4mV/A

NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
Size: Custom	Document Number: CPU Core2	Rev: 1A
Date: Friday, July 24, 2015	Sheet 49 of 62	

EC Charge Function	Page 38 & Page 39
Carrizo	Stuff
Carrizo-L	Unstuff



NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
Size: Custom	Document Number: CPU Core1 (ISL62771)	Rev: 1A
Date: Friday, July 24, 2015	Sheet 50 of 62	



+APU_VDDGFX Volt
Countinue current:22A
Peak current:35A
OCP minimum:45A
LL= -2.1mV/A

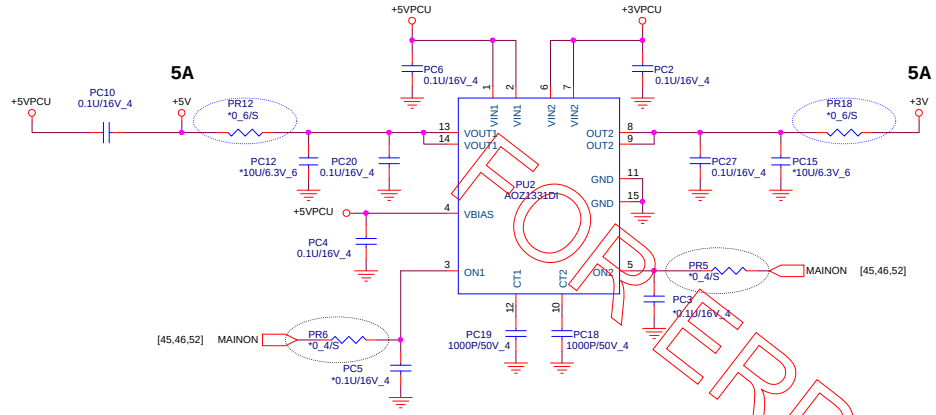
2015/02/10 for layout

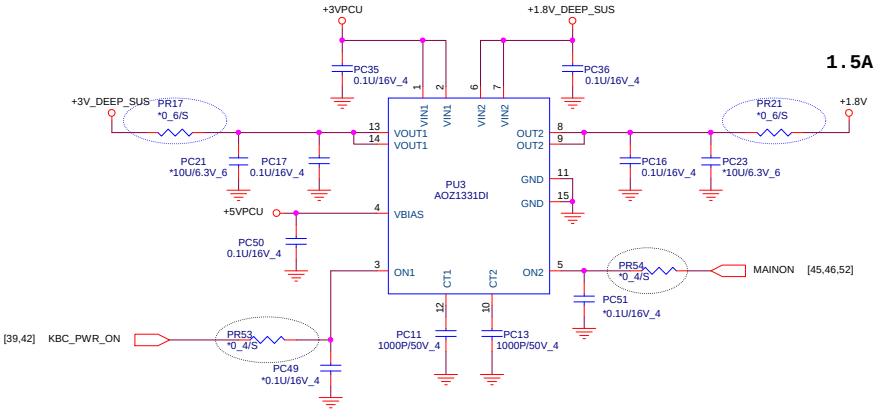
NB5

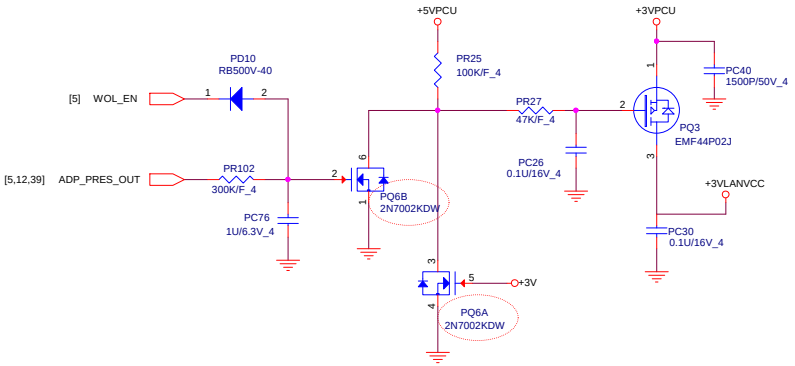
PROJECT : 400 SERIES
Quanta Computer Inc.

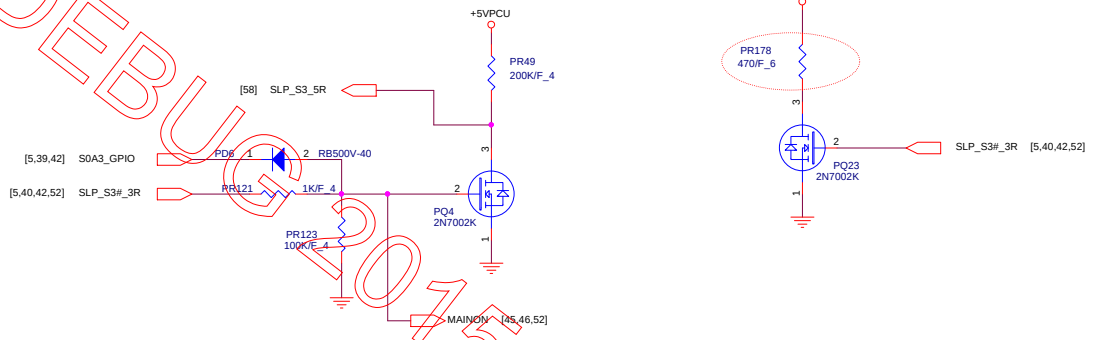
Size	Document Number	Rev
Custom	CPU Core2	1A

Date: Friday, July 24, 2015 | Sheet 51 of 62









[4,5,6,7,9,10,11,17,19,20,21,22,23,24,25,26,28,29,31,34,35,36,37,39,41,42,43,48,50,58] +3V
[22,23,24,32,35,37,58] +5V
[19,37,38,42,43,44,45,46,47,49,51,54,56] +VIN
[7,25,32,33,35,36,38,39,40,41,42,43,44,45,47,55,57] +3VPCU
[24,27,31,34,43,44,45,46,47,48,50,53,55,56,58] +5VPCU
[24] +3VLANVCC

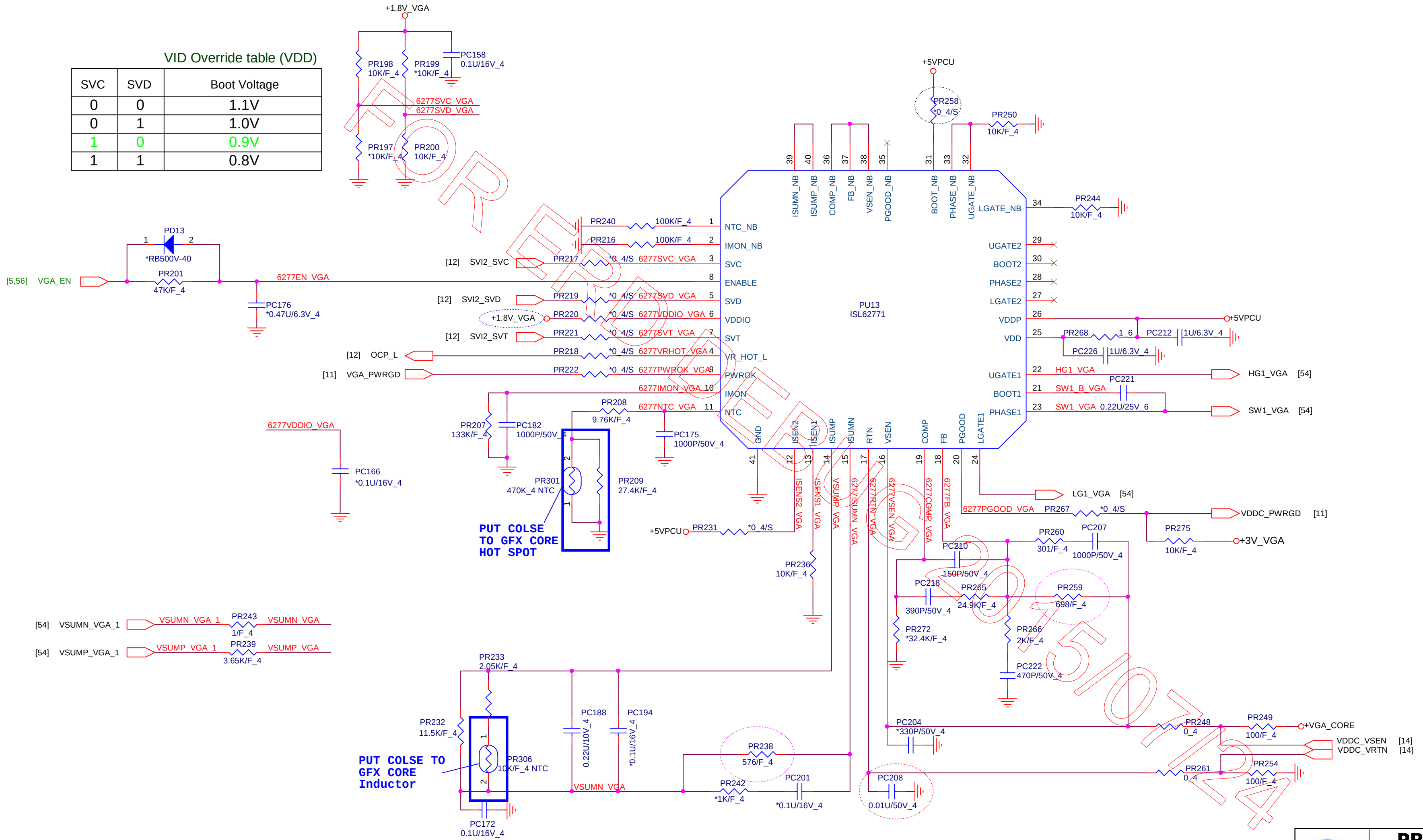
NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448)	1A
Date: Friday, July 24, 2015	Sheet 62 of 62	

VID Override table (VDD)

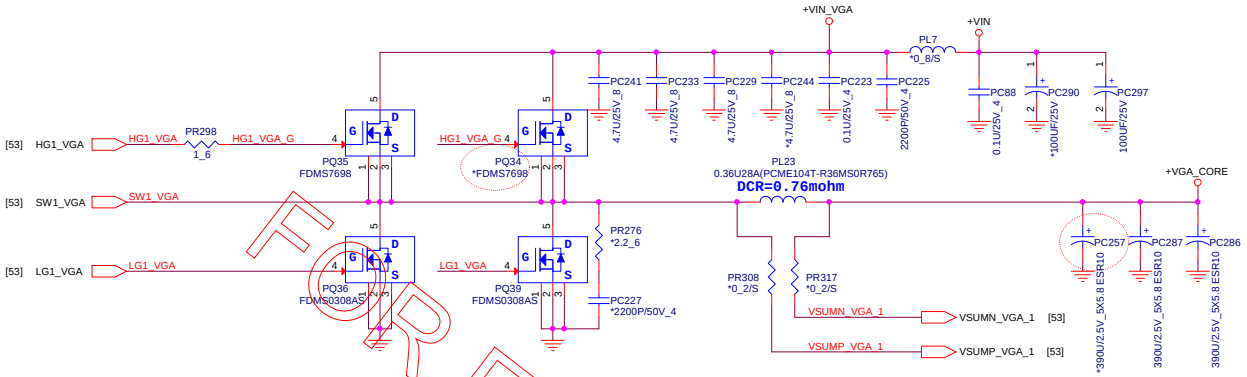
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core1 (ISL62771)	1C

Date: Friday, July 24, 2015 Sheet 53 of 62



VGACORE (Meso PRO (DDR3)_ 25W/38W(1ms))
Countinue current:28A
OCP_SPIKE=47A(1ms)

Vboot=0.9V
LL=1m V/A

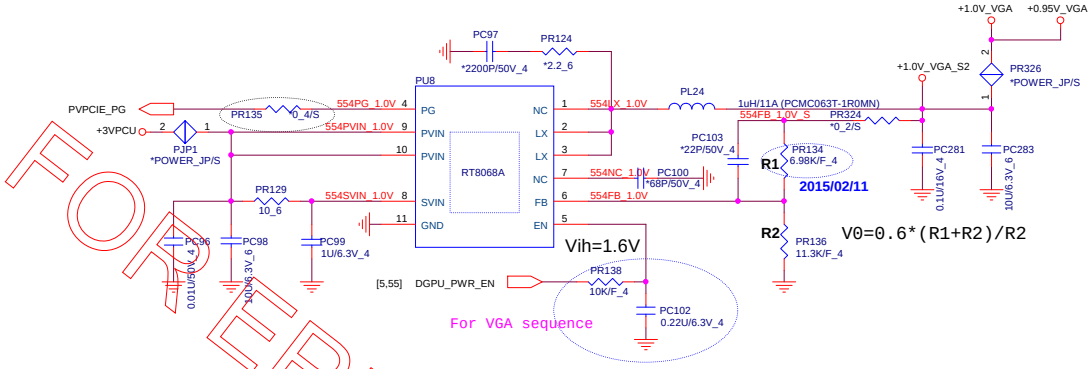
NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

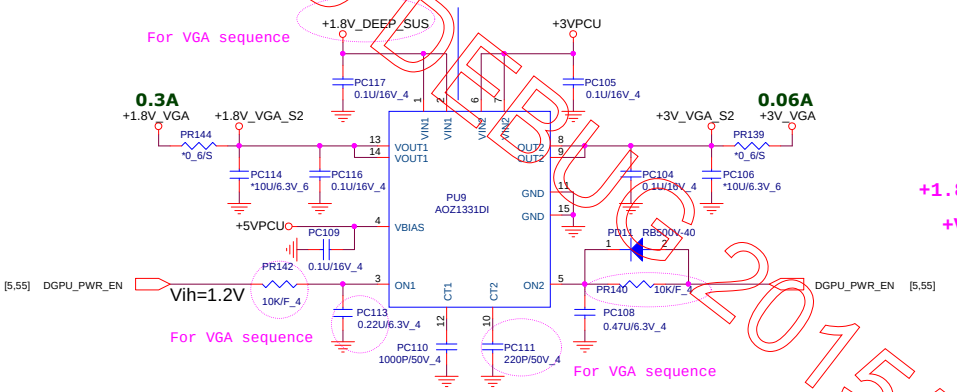
Size	Document Number	Rev
Custom	CPU Core2	1C

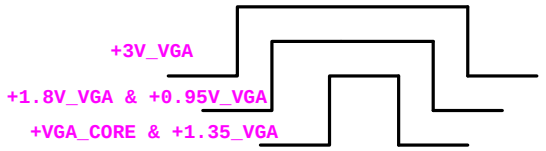
Date: Friday, July 24, 2015 | Sheet 54 of 62

+0.95V_VGA +/- 3%
Countinue current:2A
Peak current:3A



PUT COLSE TO +1.8V power.

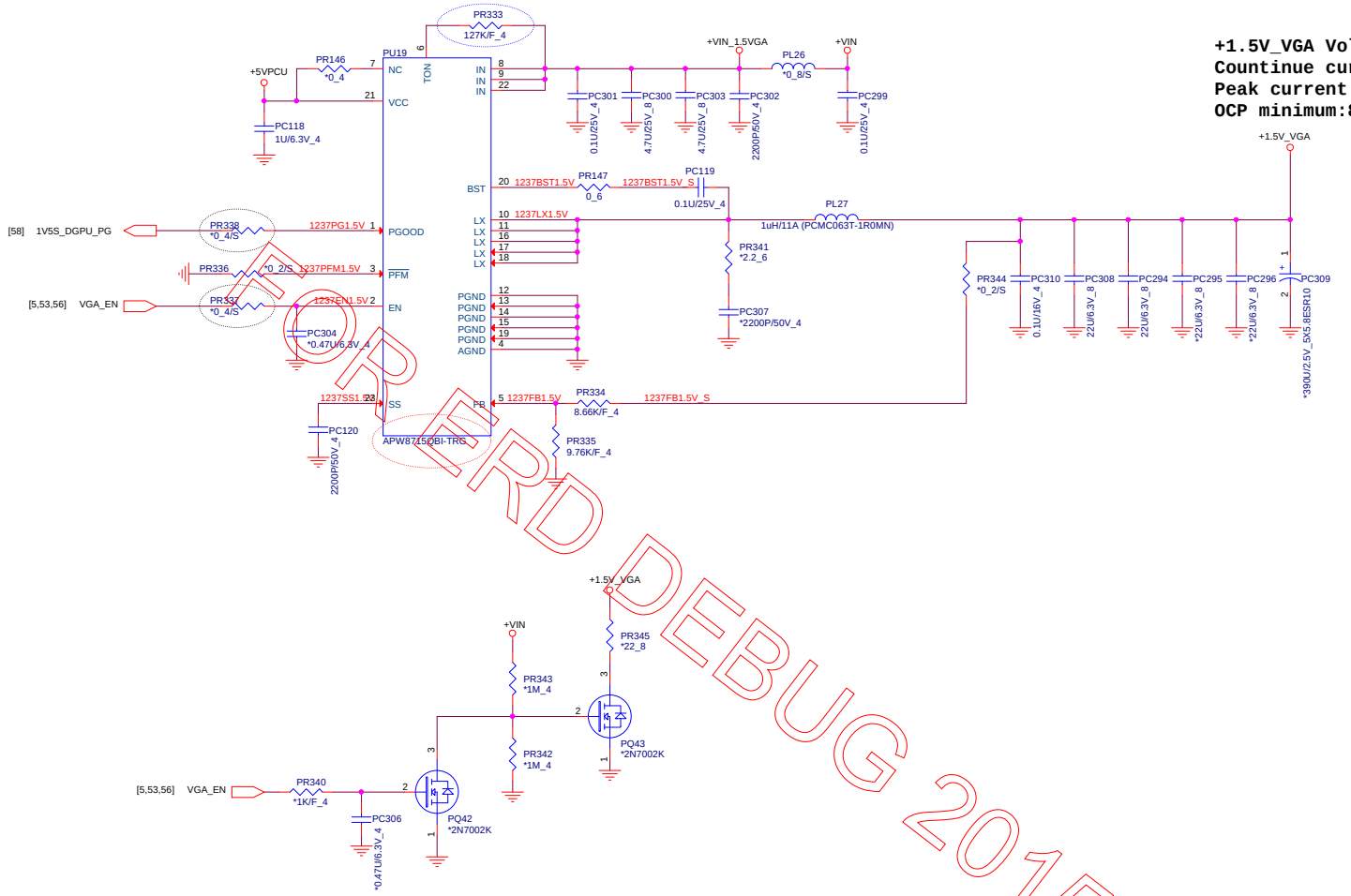




NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGA POWER	1A
Date: Friday, July 24, 2015	Sheet 55 of 62	



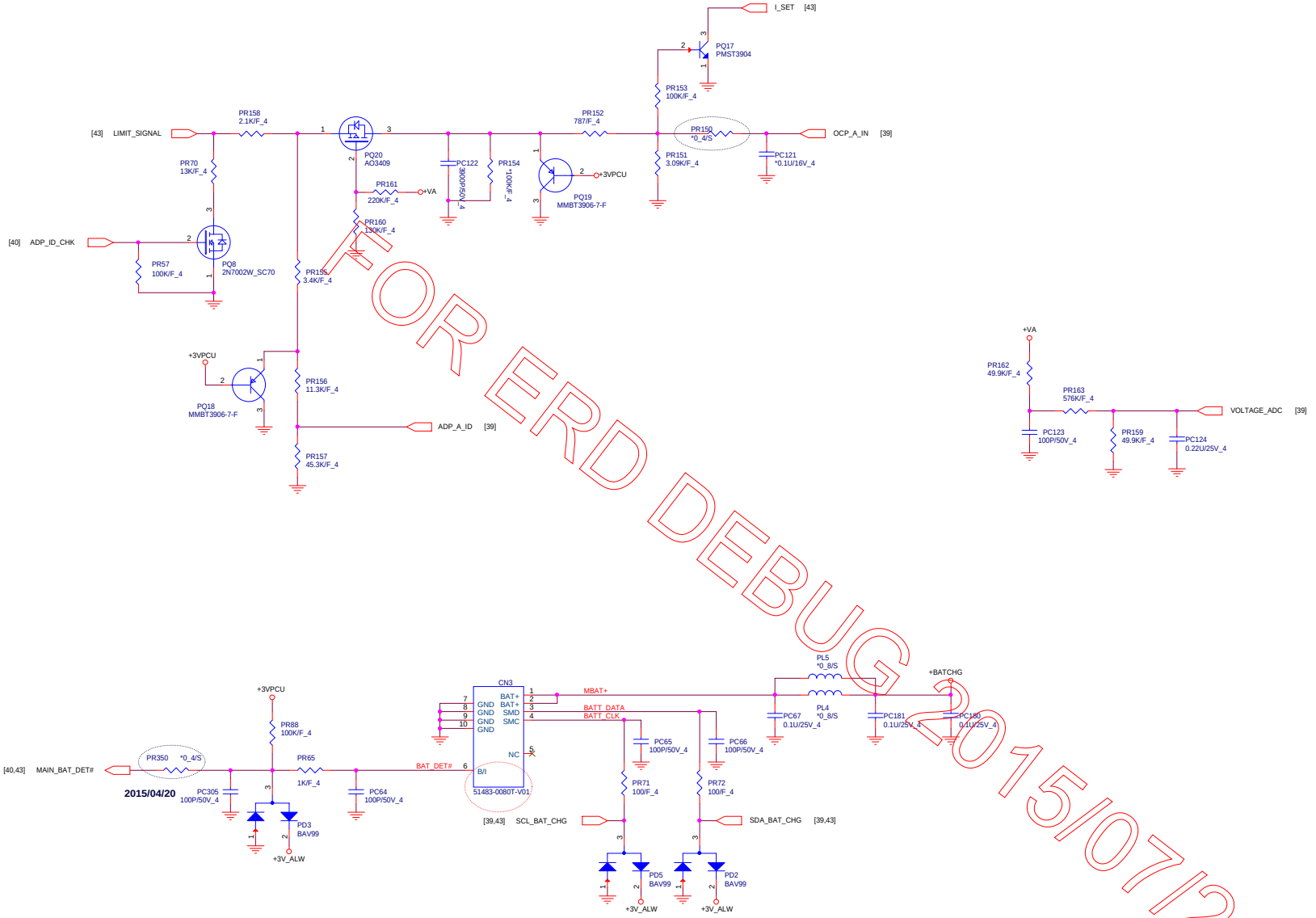
NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

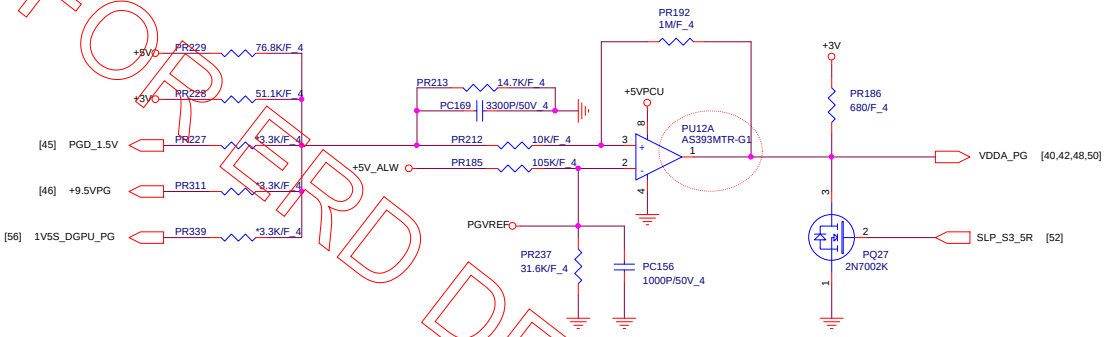
Size	Document Number	Rev
Custom	+1.35V_VGA(AOZ1237)	1A

Date: Friday, July 24, 2015 Sheet 56 of 62

Adapter OCP



NB5	PROJECT : 400 SERIES Quanta Computer Inc.	
	Size: — Document Number: CHARGER II 1A — Rev: —	
	Friday, July 24, 2015 — Sheet 57 of 62	

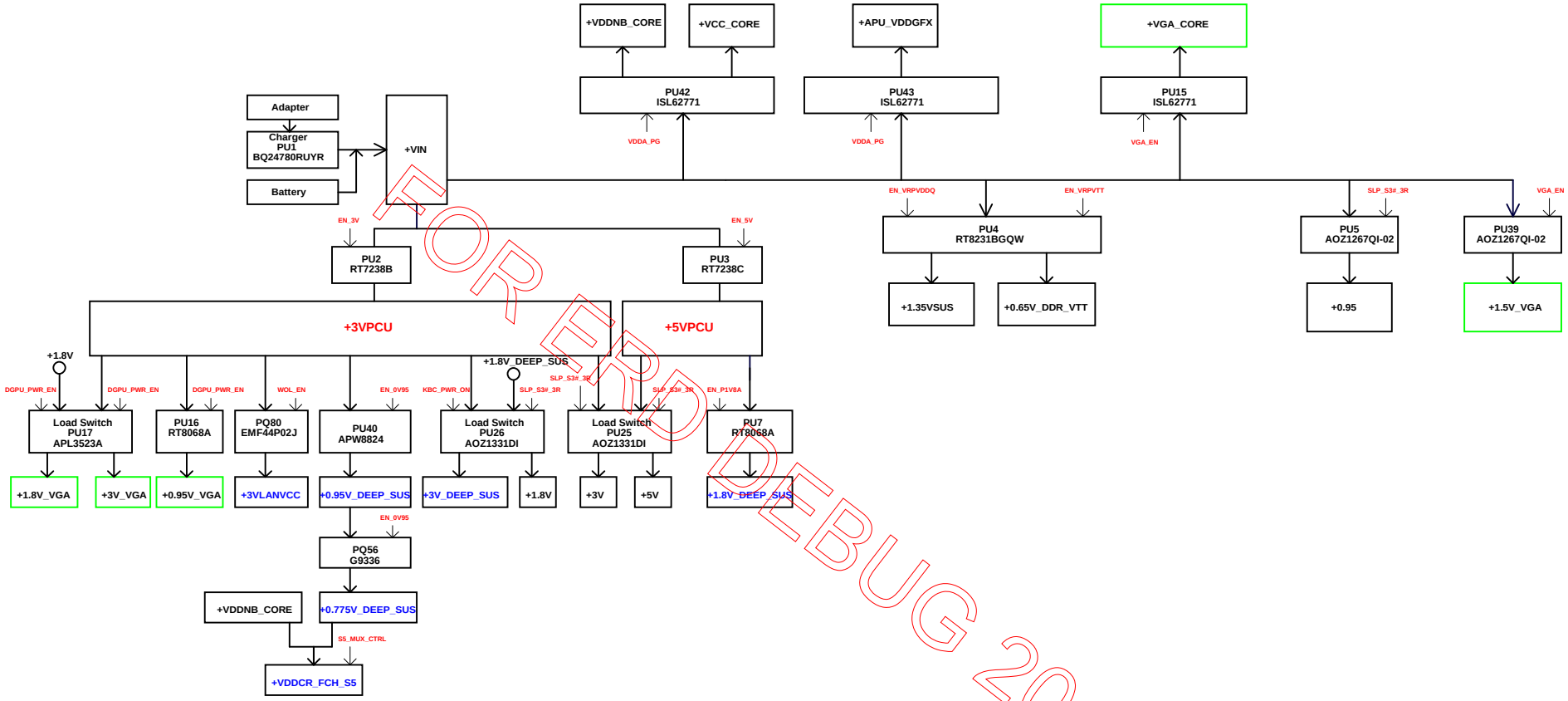


NB5

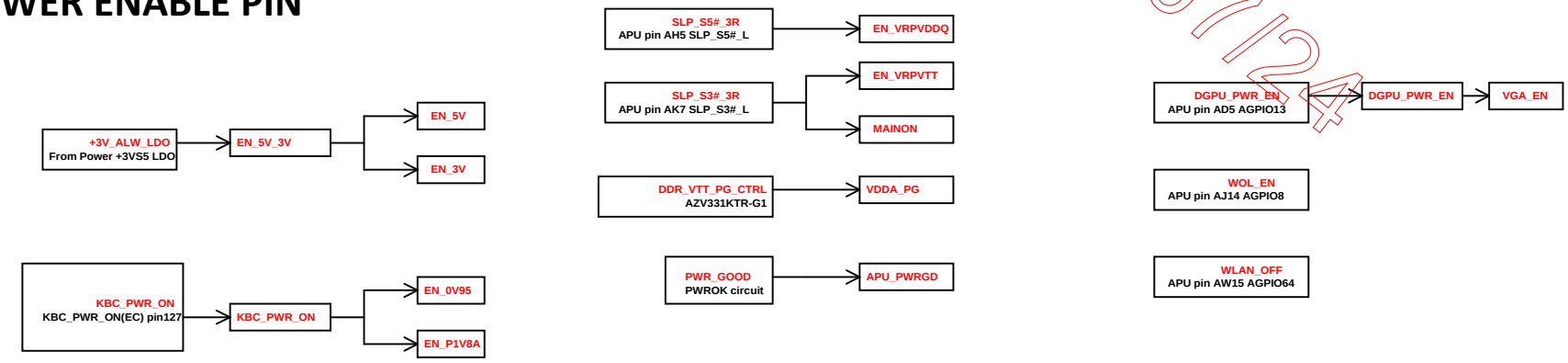
PROJECT : 400 SERIES
Quanta Computer Inc.

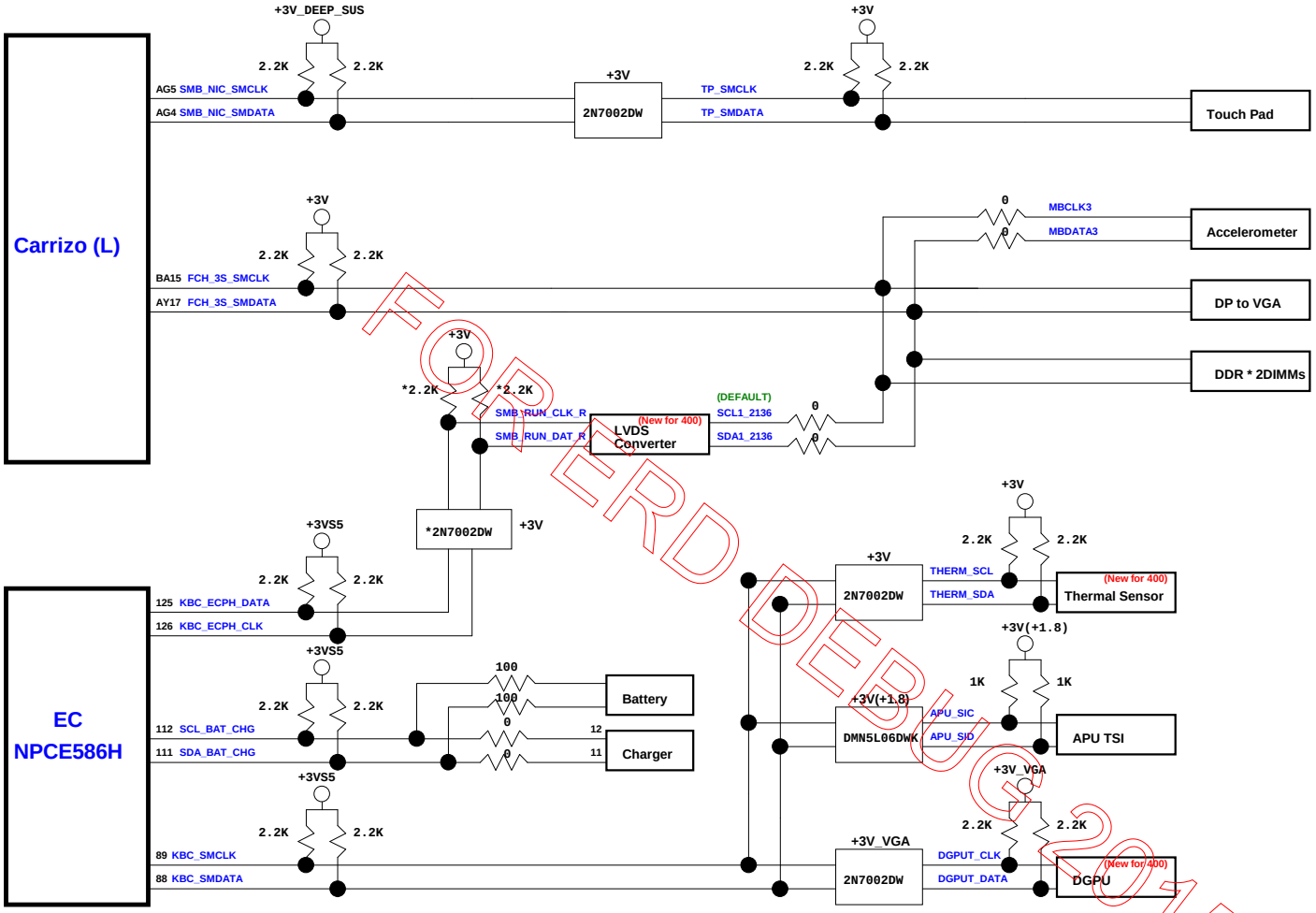
Size	Document Number	Rev
Custom	56 --Power OK	1A
Date: Friday, July 24, 2015	Sheet 58 of 62	

POWER BLOCK DIAGRAM



POWER ENABLE PIN





HSIO Lane	Port Assignment
USB3 #0	NC
USB3 #1	NC
USB3 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3	USB2.0/USB3.0 Combo Jack(Left side down)
PCIE0	NIC
PCIE1	WLAN
PCIE2	NC
PCIE4	Cardreader (PCIE)
DDI0	eDP
DDI1	DP2VGA(CZ) / DP2HDMI(CZ-L)
DDI2	HDMI(CZ)
SATA0	HDD/ BOM 0 ohm Option for M.2 SSD
SATA1	ODD
PEG0~3	dGPU
PEG4~7	NC

USB2.0	Port Assignment
USB2 #0	Camera
USB2 #1	USB2.0(Right side on USB Board)
USB2 #2	USB2.0(Right side on USB Board)
USB2 #3	NC
USB2 #4	Bluetooth
USB2 #5	Finger Print
USB2 #6	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #7	USB2.0/USB3.0 Combo Jack(Left side down)

NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	65 -- SMBus/Port Assignment	1A

Date: Friday, July 24, 2015 Sheet 60 of 62

Carrizo/Carrio-L SKU TABLE wtih Discrete
When setup the BOM, please make sure every item are finalized or not !

Function	Carrizo	Carrizo-L	Page
PEG Speed	GEN3	GEN2	
PEG cap	0.22u	0.1u	02,11
PCIe I/O Compensation			
R81	NoASM	ASM	02
R84	NoASM	ASM	
R78	ASM	NoASM	
R91	ASM	NoASM	
APU I/O Power rail	1.8V	3.3V	
R169	NoASM	ASM	04
R176	ASM	NoASM	
VDDCR_FCH_S5	Support	Not Support	
R175	ASM	NoASM	07
C188	ASM	NoASM	
C187	ASM	NoASM	
C174	ASM	NoASM	
+VDDCR_FCH_S5 MUX control circuit	ASM	NoASM	47
VDDCR_GFX	Support	Not Support	
+APU_VDDGFX cap & Power IC circuit	ASM	NoASM	07,50,51
GPU Speed setting	GEN3	GEN2	
R194	8.45K	NoASM	12
R193	2K	4.75K	
eDP control signal	Thu level shifter	By pass	
Q36	ASM	NoASM	19
Q37	ASM	NoASM	
Q38	ASM	NoASM	
Q39	ASM	NoASM	
Q39	ASM	NoASM	
Q40	ASM	NoASM	
R341	ASM	NoASM	
R348	ASM	NoASM	
R351	ASM	NoASM	
R352	ASM	NoASM	
R355	ASM	NoASM	
R356	ASM	NoASM	
R360	ASM	NoASM	
R361	ASM	NoASM	
R364	ASM	NoASM	
R366	ASM	NoASM	
R367	ASM	NoASM	
R369			
R343	NoASM	ASM	19
R354	NoASM	ASM	
R359	NoASM	ASM	
R365	NoASM	ASM	

Function	Carrizo	Carrizo-L	Page
DP switch	By pass	Thu DP switch	
R200,R201	ASM	NoASM	21
R606,R601	ASM	NoASM	
R261,R262	ASM	NoASM	
R676,R668	ASM	NoASM	
R702,R695	ASM	NoASM	
R223,R224	ASM	NoASM	
R690,R682	ASM	NoASM	
R260,R259	ASM	NoASM	
R662,R647	ASM	NoASM	
R203,R202	ASM	NoASM	
R643	ASM	NoASM	
R221	ASM	NoASM	
R240			
R580,R581	NoASM	ASM	21
R696,R703	NoASM	ASM	
R683,R691	NoASM	ASM	
R677,R669	NoASM	ASM	
R663,R648	NoASM	ASM	
R605,R600	NoASM	ASM	
R582,R583	NoASM	ASM	
R620,R624	NoASM	ASM	
R579	NoASM	ASM	
R239	NoASM	ASM	
DP switch IC circuit			
C332	ASM	NoASM	22
Q27	ASM	NoASM	
R289	ASM	NoASM	
R675,R684	ASM	NoASM	
R688,R694	ASM	NoASM	
R701,R706	ASM	NoASM	
R707,R709	ASM	NoASM	
TPM SPI CS#	Thu level shifter	By pass	
Q25	ASM	NoASM	
R256	NoASM	ASM	
SPI Bus	Thu level shifter	By pass	
R382	ASM	NoASM	41
R383	ASM	NoASM	
R381	ASM	NoASM	
Q12	ASM	NoASM	
R47	ASM	NoASM	
R55	NoASM	ASM	
R53	NoASM	ASM	
R39	NoASM	ASM	
C43	NoASM	ASM	
C41	NoASM	ASM	
R52	NoASM	ASM	
R54	NoASM	ASM	
C44	NoASM	ASM	
U2			

UMA/DIS SKU TABLE

When setup the BOM, please make sure every item are finalized or not !

Function	Carrizo UMA	Carrizo-L UMA	Discrete	Page
GPU				
APU side PEG cap	NoASM	NoASM	ASM	02
GPU circut	NoASM	NoASM	ASM	11,12,13,14, 15,16
GPU Power circut	NoASM	NoASM	ASM	53,54,55,56
GPU enable circuit				
C143	NoASM	NoASM	ASM	05
C470	NoASM	NoASM	ASM	
D16	NoASM	NoASM	ASM	
D17	NoASM	NoASM	ASM	
Q21	NoASM	NoASM	ASM	
R160	NoASM	NoASM	ASM	
R454	NoASM	NoASM	ASM	
VBIOS ID				
R76	ASM	ASM	NoASM	05
R98	ASM	ASM	NoASM	
R82	NoASM	NoASM	ASM	
R105	NoASM	NoASM	ASM	
APU VDDP GFX rail				
C122	ASM	NoASM	ASM	07
C436	ASM	NoASM	ASM	
R402	ASM	NoASM	ASM	
R155	NoASM	ASM	NoASM	

Schematic Value Note:

*** is NO SMT part (empty)**

DIS@ : for VGA mode
CZ@ : for Carrizo
CZL@ : for Carrizo-L