SX7 SYSTEM DIAGRAM

AMD Smarter Choice

01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

DDRIII-SODIMM1 PAGE 6,7 — DDRIII 1066 MHz

DDRIII-SODIMM2 PAGE 6,7 — DDRIII 1066 MHz

AMD Champlain
35mm X 35mm
S1G4 Processor
638P (PGA) 25W
PAGE 3,4,5

CPU THERMAL SENSOR PAGE 5

14.318MHz

CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP628VTR-->HP
RTM880N-796 -->HP
PAGE 2

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

HT3

PCI-E

X1 New Card PAGE 29

X1 LAN Realtek PCIE-LAN RTL8151DH (10/100/1000) PAGE 28

RJ45 PAGE 28

X1 Mini PCI-E Card (Wireless LAN) PAGE 33

NORTH BRIDGE
RS880M
21mm X 21mm, 528pin BGA
PAGE 8,9,10,11

PCI-Express 16X

M93-S3/ Park-S3
64 Bit,DDR3*4
23mm X 23mm, 631pin BGA
PAGE 17,18,19,20,21,22

HDMI PAGE 24

CRT PAGE 23

LVDS PAGE 23

ALINK X4

SBSRC_CLK

SYSTEM CHARGER(bq24740) PAGE 36,37

3/5VS5 RT8206B PAGE 38

+1.1V(RT8029)/+1.1VS5/+1.8V PAGE 39

DDR3 (RT8207)/+1.0V_VGA PAGE 40

VGACORE(1.1V~0.9V)RT8028A PAGE 41

CPU_CORE ISL6265 PAGE 42

SATA - HDD PAGE 31 — SATA0 150MB

SATA - CD-ROM PAGE 31 — SATA4 150MB

E-SATA PAGE 29 — SATA1 150MB

SOUTH BRIDGE
SB820M
23mm X 23mm, 605pin BGA
PAGE 12,13.14.15.16

USB2.0

0,2,3,5 USB2.0 Ports PAGE 29

9 Blueflame PAGE 32

1 Webcam PAGE 23

4 7 Finger Printer PAGE 32

FS1 8 Flash Media RTS5159 PAGE 30

6 New Card PAGE 29

Wireless WAN PAGE 33

PCI-E WLAN Card x1 PAGE 33

Azalia

IDT 92HD80B1 PAGE 25

MDC CONN PAGE 29

LPC

SPI

Keyboard Touch Pad PAGE 32

SMSC KBC
KBC1098
PAGE 27

FAN PAGE 28

SPI ROM PAGE 35

Digital MIC PAGE 23

AUDIO CONN Phone/ MIC PAGE 28

SMBUS TABLE		
SB--SCL0/SD0	Clock gen/ wirless LAN/ New card/ DDR3/ DDR3 thermal/ Accelerometer/system thermal	+3V
EC -- AB1A	Battery charge/discharge	+3VPCU
EC -- AB2A	VGA thermal	+3V

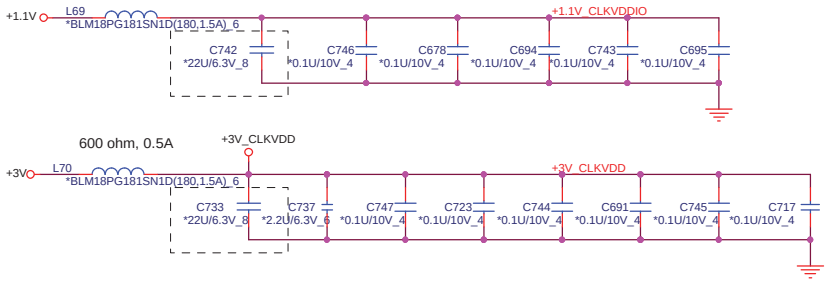
NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

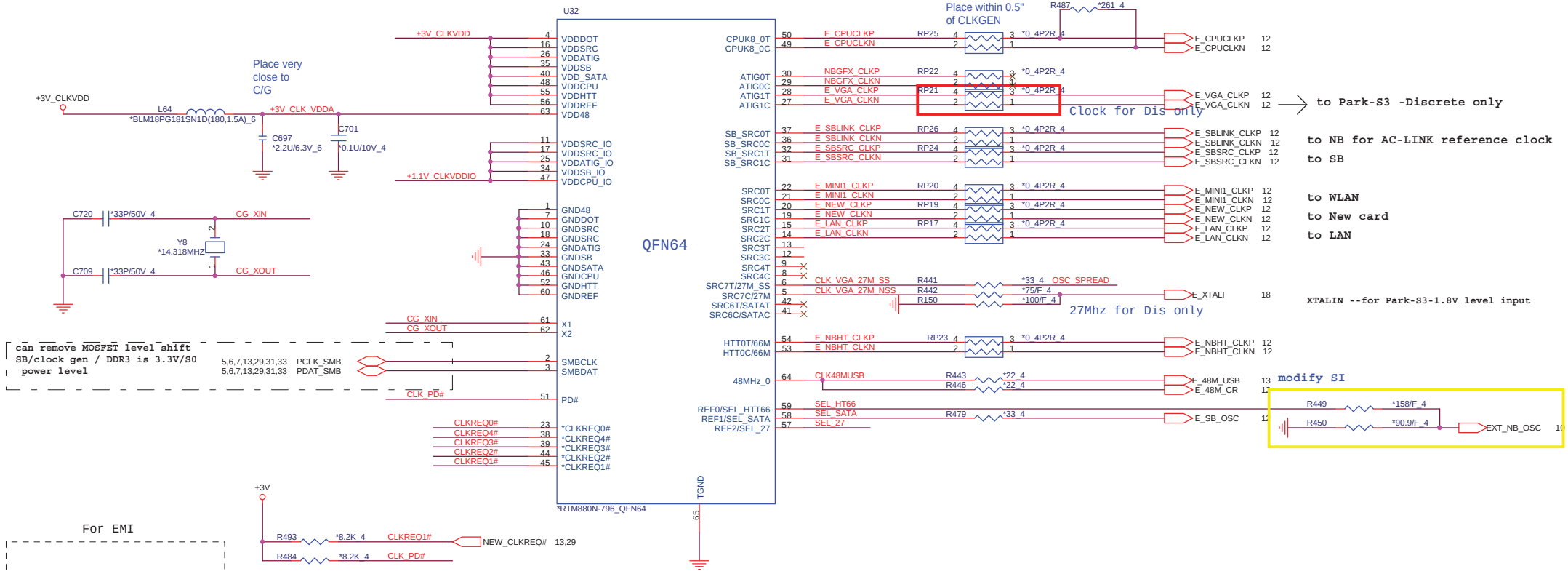
Size	Document Number	Rev
Custom	Block Diagram	3A

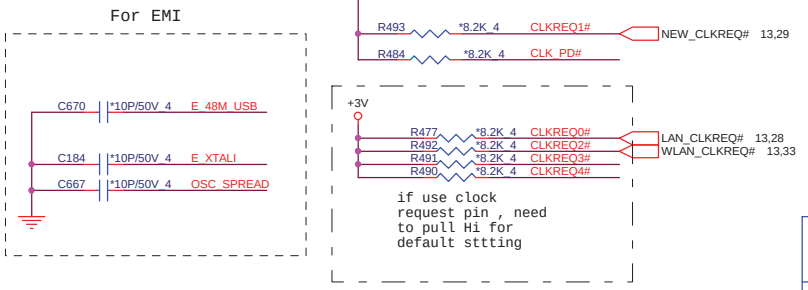
Date: Monday, March 15, 2010 Sheet 1 of 43

CLOCKS name	Discrete	Clock pin function
NBGFX_CLKP NBGFX_CLKN	NA	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP21 STUFF	to Park-S3 external reference clock -Discrete only
SBLINK_CLKP SBLINK_CLKN	RP26 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R441,R442 STUFF	To Park-S3 27Mhz - Discrete only



Need check the net name for the short pad

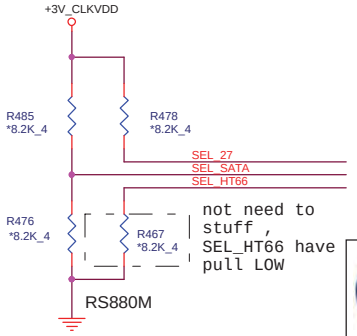




IDT ICS9LPRS480AKLFT--ALPRS480000
SLG SLG8SP628VTR--AL8SP628000
RTL RTM880N-796-- AL000880001

* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock



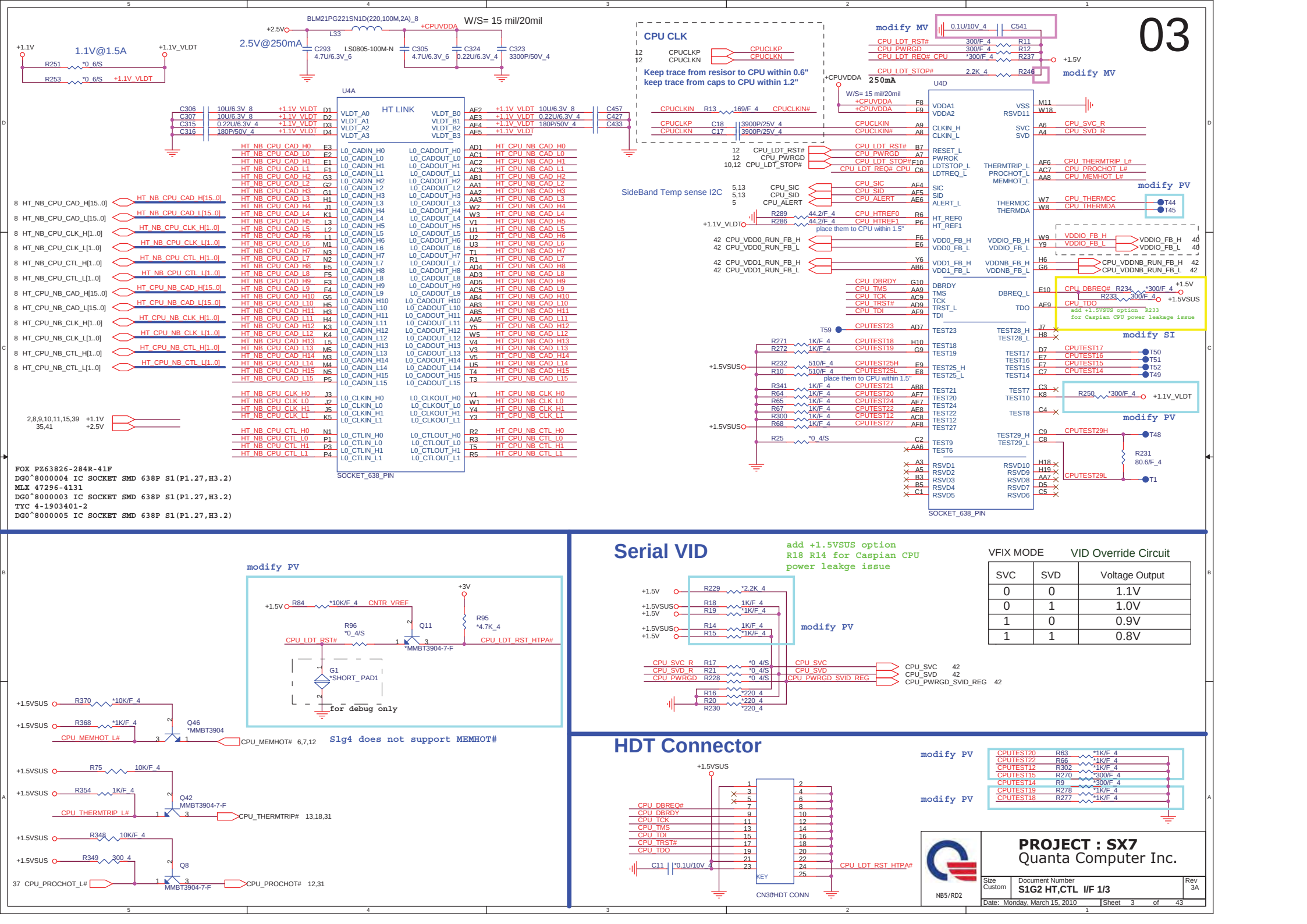
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Generator	3A

NB5/RD2

Date: Monday, March 15, 2010 Sheet 2 of 43


03
CPU CLK
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
modify MV
modify PV
modify SI
SideBand Temp sense I2C
HT LINK
U4A
U4D
SOCKET_638_PIN
FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)
Serial VID
add +1.5VSUS option
R18 R14 for Caspian CPU
power leakge issue
VFIX MODE
VID Override Circuit
SVC SVD Voltage Output
0 0 1.1V
0 1 1.0V
1 0 0.9V
1 1 0.8V
HDT Connector
S1g4 does not support MEMHOT#
for debug only
PROJECT : SX7
Quanta Computer Inc.
NB5/RD2
Size Custom
Document Number S1G2 HT,CTL I/F 1/3
Rev 3A
Date: Monday, March 15, 2010
Sheet 3 of 43

Processor Memory Interface

04

0.9V@1.5A

PLACE THEM CLOSE TO CPU WITHIN 1"

modify PV

U4B

MEM:CMD/CTRL/CLK

SOCKET_638_PIN

U4C

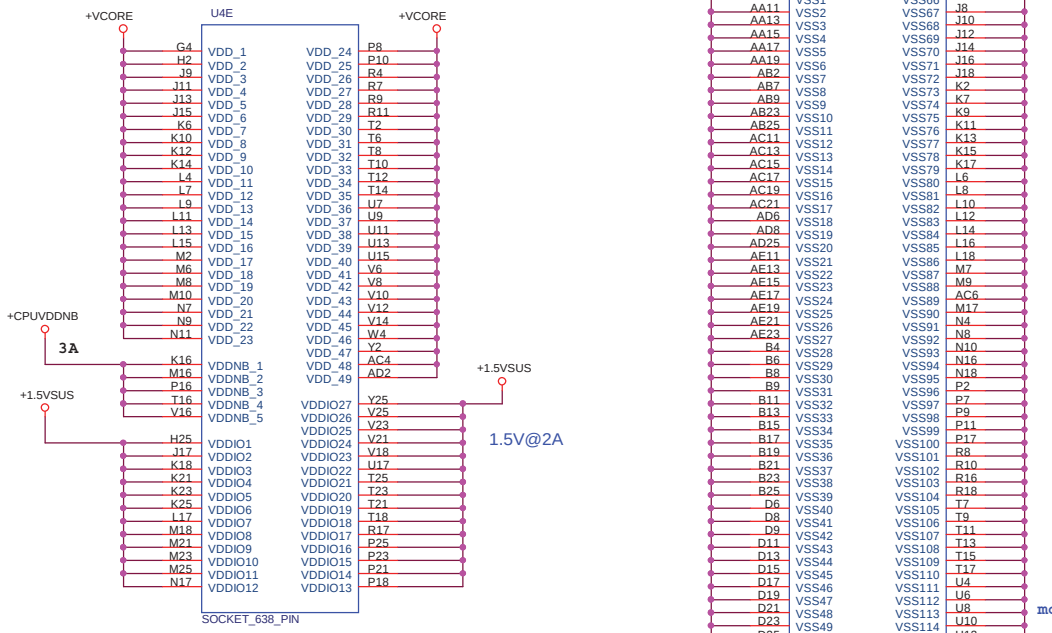
MEM:DATA

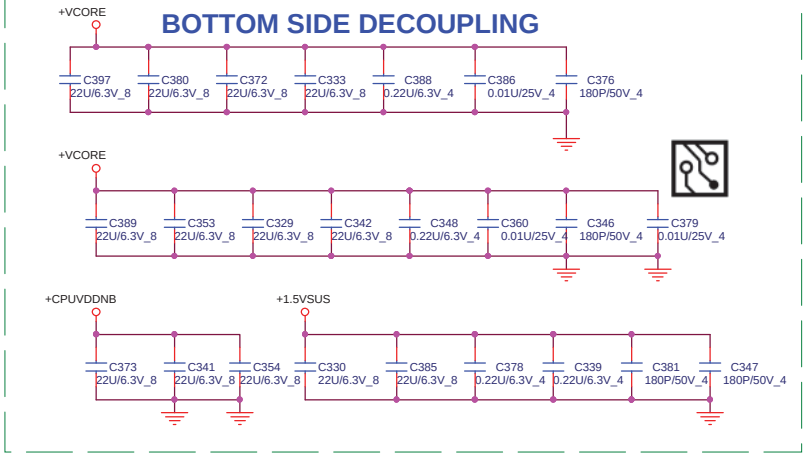
SOCKET_638_PIN

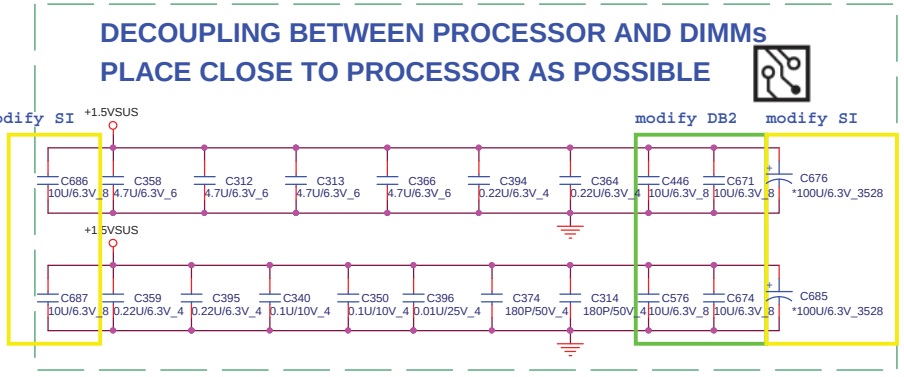
Place close to socket

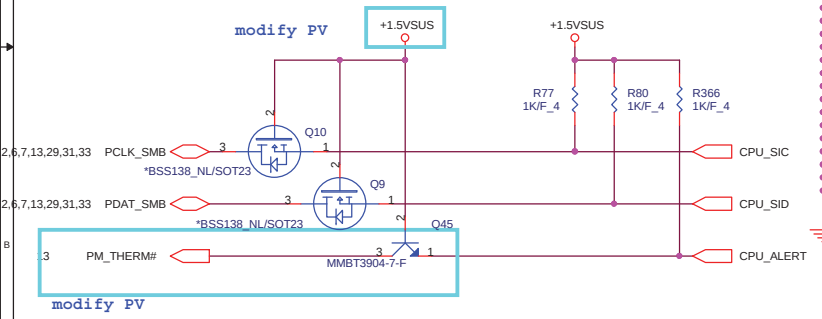
PROJECT :	SX7
	Quanta Computer Inc.
Size: Custom	Document Number: S1G2 DDRII MEMORY I/F 2/3
Rev:	3A
Date: Monday, March 15, 2010	Sheet 4 of 43

NB5/RD2

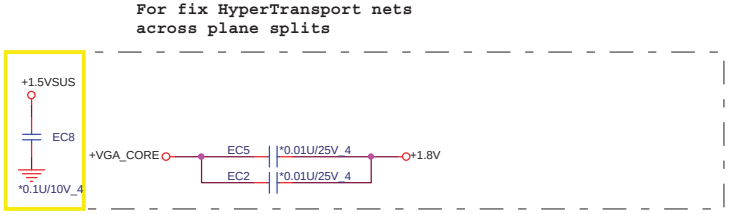


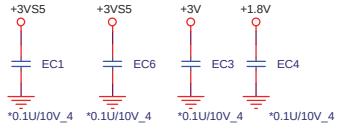






PROCESSOR POWER AND GROUND



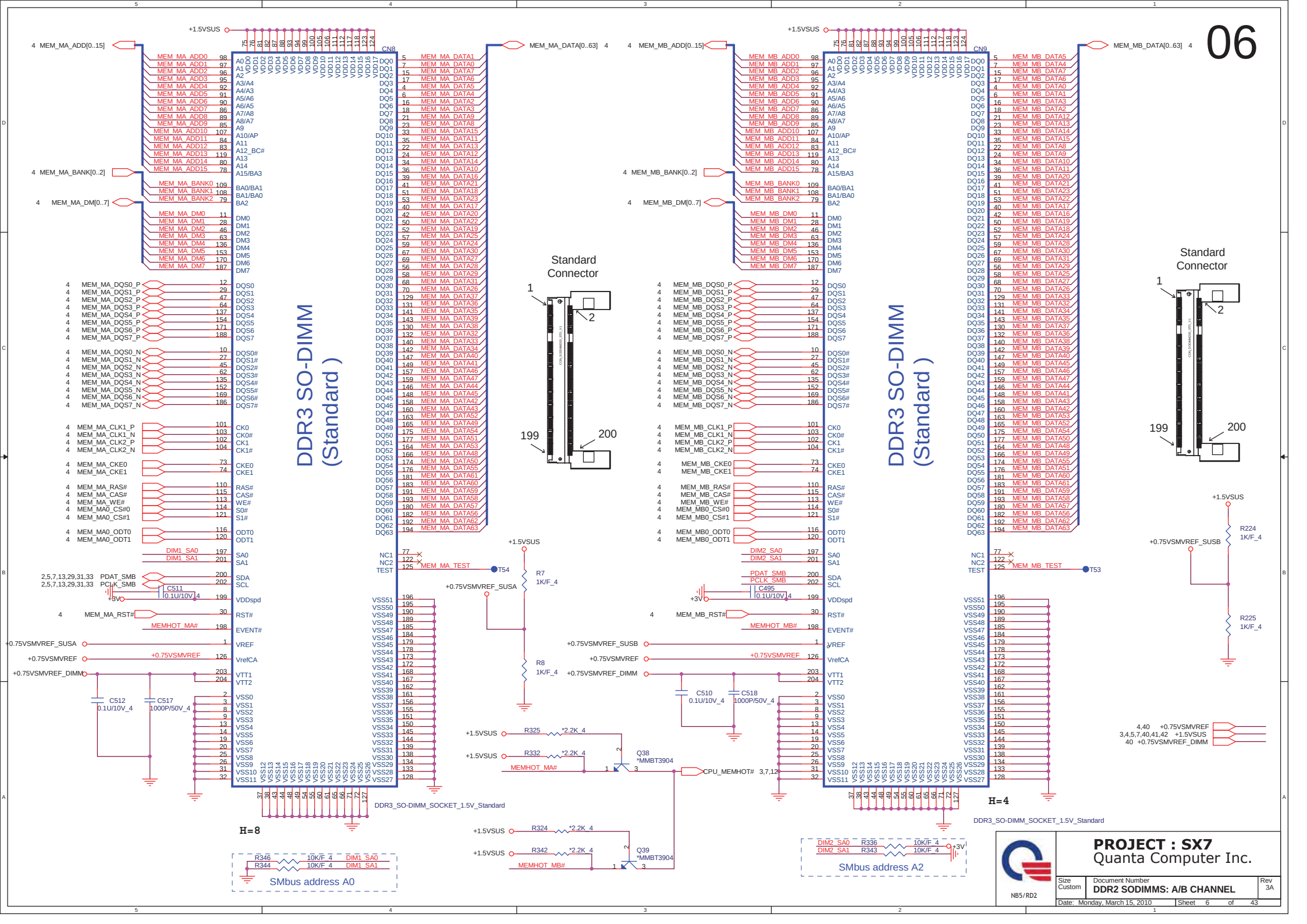


NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G2 PWR & GND 3/3	3A

Date: Monday, March 15, 2010 | Sheet 5 of 43

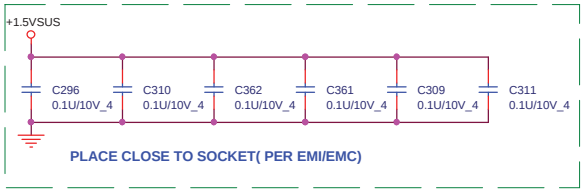


PROJECT : SX7
Quanta Computer Inc.

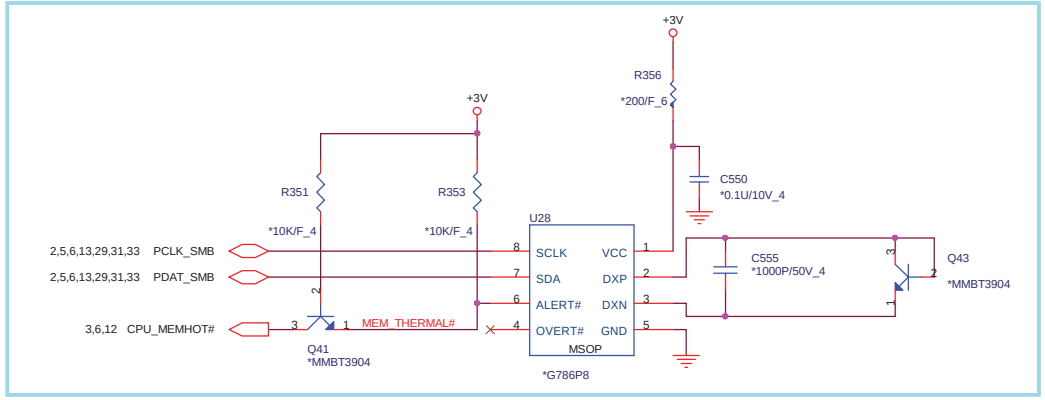
Size	Document Number	Rev
Custom	DDR2 SODIMMS: A/B CHANNEL	3A

NB5/RD2

Date: Monday, March 15, 2010 Sheet 6 of 43



modify PV



PROJECT : SX7
Quanta Computer Inc.

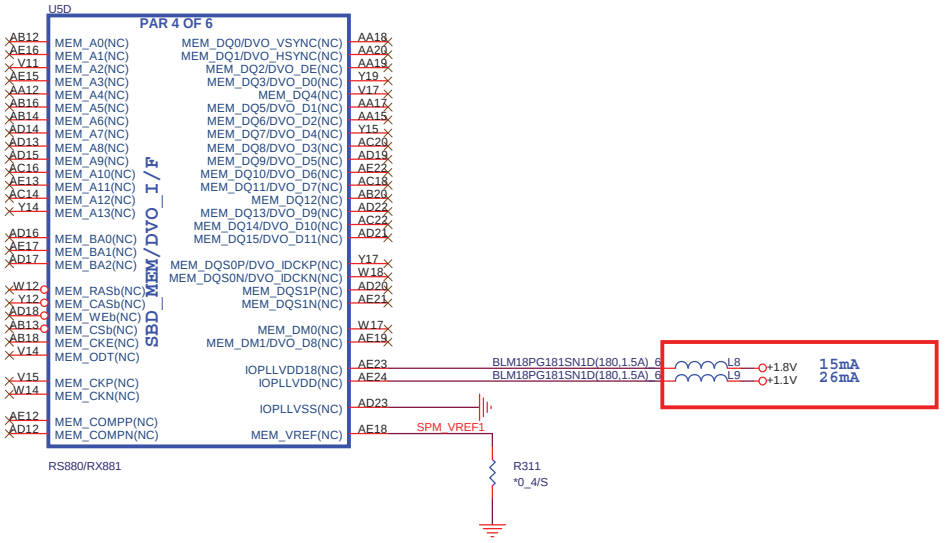
Size	Document Number	Rev
Custom	DDR2 SODIMMS TERMINATIONS	3A

Date: Monday, March 15, 2010 | Sheet 7 of 43

NB5/RD2

signals	RS880M
HT_TXCALP	R430 301 ohm 1%
HT_TXCALN	
HT_RXCALP	R434 301 ohm 1%
HT_RXCALN	

This block is for UMA only , Discrete can remove all component

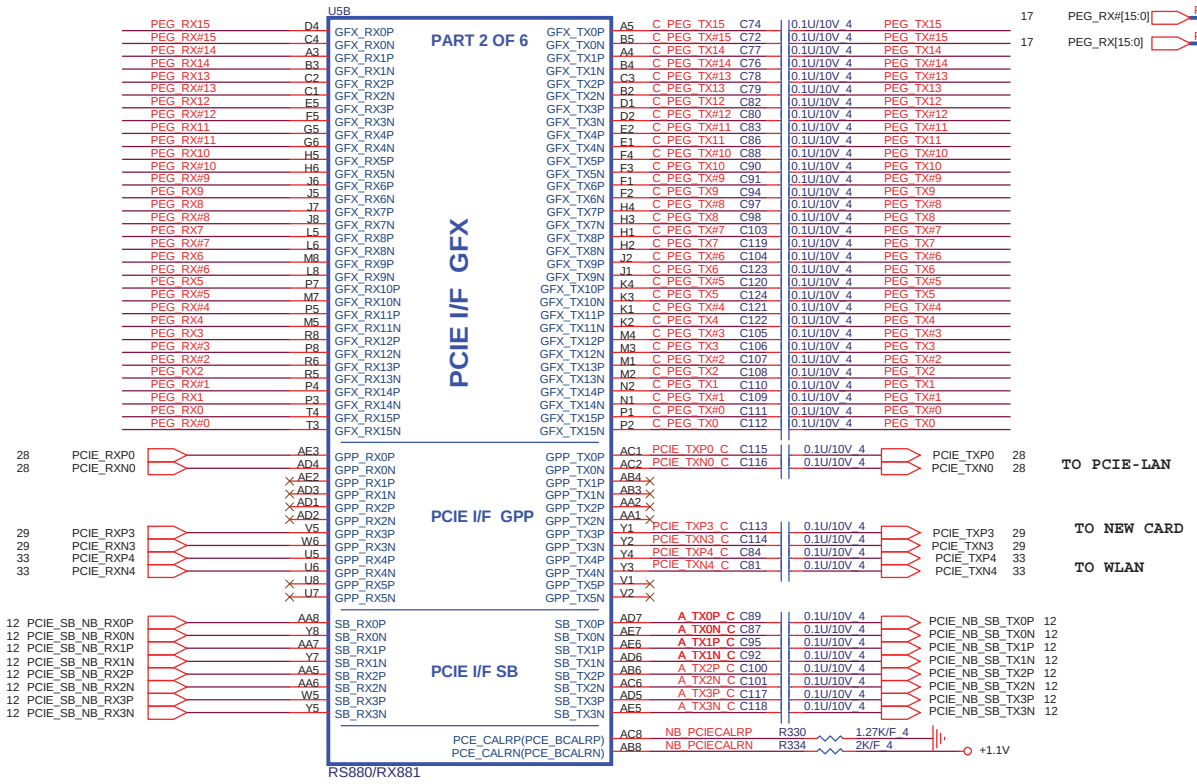


PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS880M-HT LINK I/F 1/5	3A

NB5/RD2

Date: Monday, March 15, 2010 Sheet 8 of 43

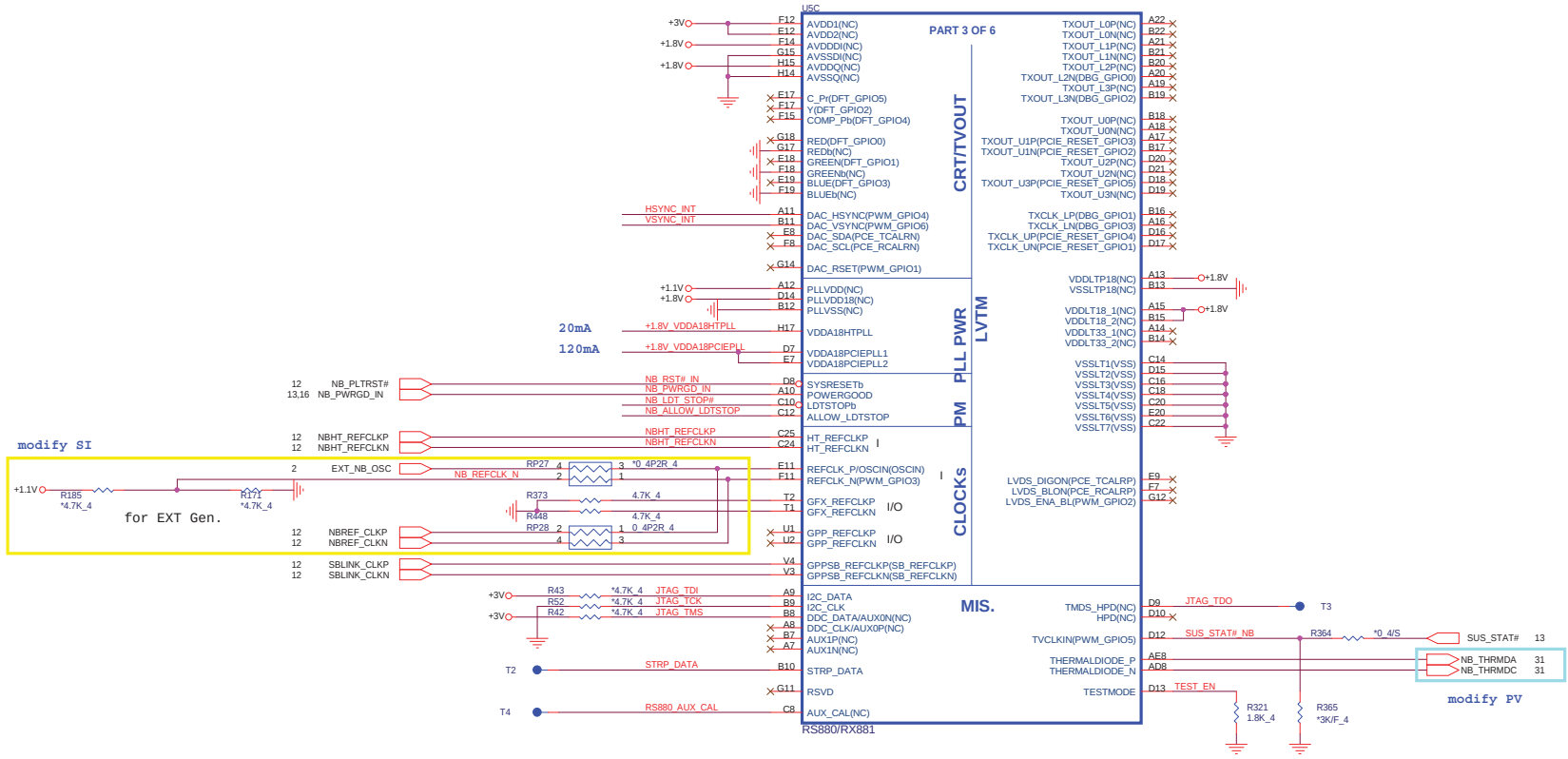


NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

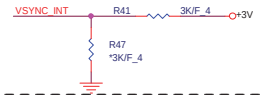
Size	Document Number	Rev
Custom	RS880M-PCIE I/F 2/5	3A

Date: Monday, March 15, 2010 Sheet 9 of 43



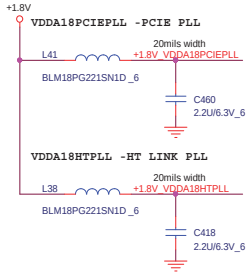
Enables Debug Bus acess
through memory I/O pads and GPIO.
0 : Enable RS880M , Default
1 : Disable RS880M
(RX881 use DAC_VSYNC)

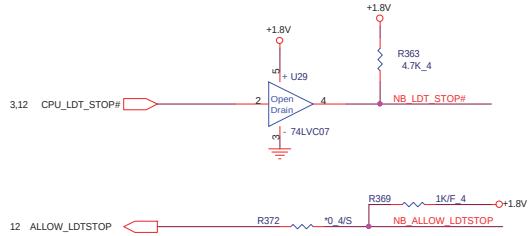
Discrete



Indicates if memory Side port
is available or not
0: Reserved
1: Required setting. Select with a pull-up
resistor on the strap
(RX881 use DAC_HSYNC)

Discrete





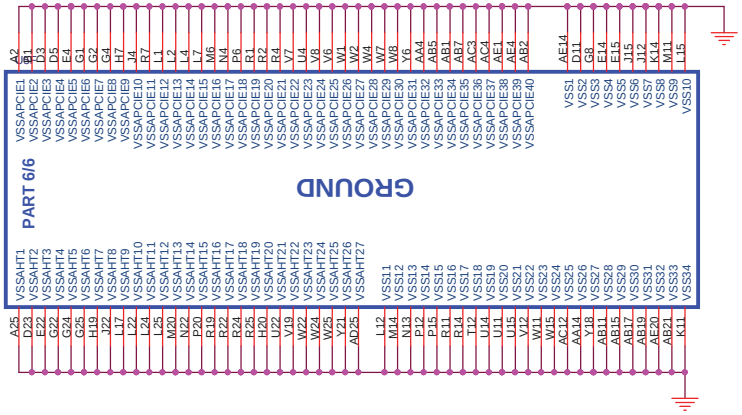
PROJECT : SX7
Quanta Computer Inc.

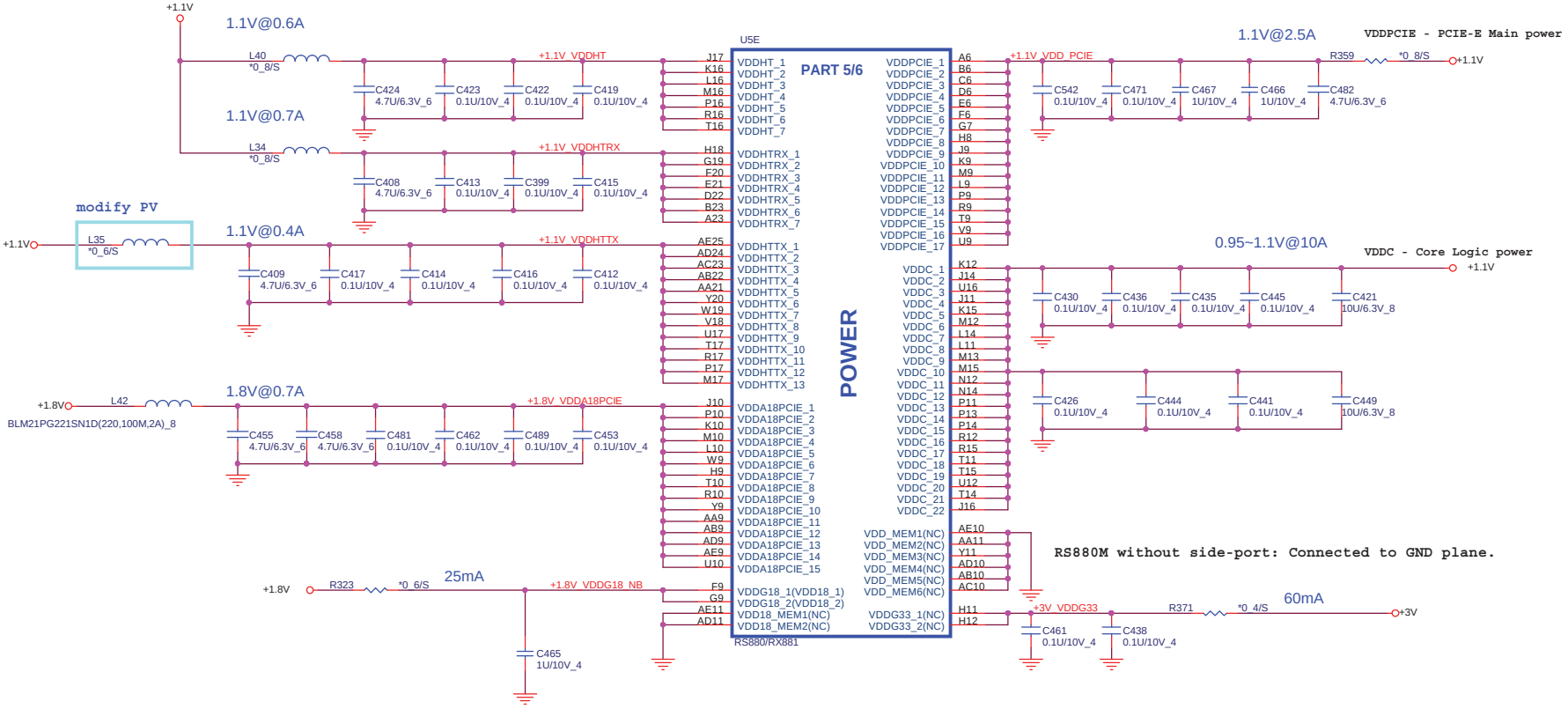
Size	Document Number	Rev
Custom	RS880M-SYSTEM I/F 3/5	3A
Date: Monday, March 15, 2010	Sheet 10 of 43	

NB5/RD2

RX881/RS880 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVDD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVDD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDDG33	+3.3V	+3.3V	VDDLT18	GND	+1.8V
IOPLLVDD18	+1.8V	+1.8V	VDDLT33	NC	NC





NB5/RD2	PROJECT : SX7 Quanta Computer Inc.	
Size: Custom	Document Number: RS880M-POWER5/5	Rev: 3A
Date: Monday, March 15, 2010	Sheet 11 of 43	

modify SI

modify PV

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB820

To RS880

U11A

SB800 Part 1 of 5

PCI CLKS

PCI EXPRESS INTERFACES

PCI INTERFACE

CLOCK GENERATOR

LPC

CPU

RTC

Change from 0ohm to 1K for safty issue

for EMI suggestion

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

SB800 A11

IC CTRL(528P) SB710 A14(218-0660017)
P/N : AJ066000T01

NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-PCIE/PCI/CPU/LPC 1/4	3A

Date: Monday, March 15, 2010 | Sheet 12 of 43

NC only ,Can't be install

+3VS5 R427 *2.2K_4 SB_TEST0
R432 *2.2K_4 SB_TEST1
R423 *2.2K_4 SB_TEST2

+3V SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R377 2.2K_4 PCLK_SMB
R376 2.2K_4 PDAT_SMB
Clock gen/CPU thermal /DDR3/DDR3 thermal/Accelerometer

+3VS5 SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R428 2.2K_4 SB_SMBCLK1
R422 2.2K_4 SB_SMBDATA1

+3VS5 SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R458 2.2K_4 SB_SCLK2
R459 2.2K_4 SB_SDATA2

+3V modify PV
R418 4.7K_4 SUS_STAT#
modify MV

+3VS5
R514 *10K_4 SYS_RST#
R513 *10K_4 SB_RSMRST#
C857 *0.1U/10V_4

RCIN# 27 RCIN# Q47 2N7002E

To Azalia

ACZ_SDOUT R139 33_4 ACZ_SDOUT_AUDIO 25
C166 *10P/50V_4
ACZ_SYNC R138 33_4 ACZ_SYNC_AUDIO 25
C163 *10P/50V_4
ACZ_BCLK R141 33_4 BIT_CLK_AUDIO 25
C169 22P/50V_4 EMI modify PV
ACZ_RST# R137 33_4 ACZ_RST#_AUDIO 25
ACZ_SDIN0 ACZ_SDIN0 25
Remove short pad

To Modem Board

ACZ_SDOUT R404 33_4 ACZ_SDOUT_MDC 29
C625 *10P/50V_4
ACZ_SYNC R402 33_4 ACZ_SYNC_MDC 29
C620 *10P/50V_4
ACZ_BCLK R142 33_4 BIT_CLK_MDC 29
C172 22P/50V_4 EMI modify PV
ACZ_RST# R400 33_4 ACZ_RST#_MDC 29
ACZ_SDIN1 ACZ_SDIN1 29
Remove short pad

modify DB2
T77 LID_SW# SB
27 SUSB# SUSC#
27,31 NBSWON1#
16 SB_PWRGD_IN
10 SUS_STAT#
SB_TEST0 SB_TEST1 SB_TEST2 GATEA20_SB RCIN# 1
modify DB2
27 KBC_SCI# 28 DSM#
T43 T42
modify DB2
28,29,33 PCIE_WAKE#
SB_THERMTRIP#
10,16 WD_PWRGD
27 RSMRST# R512 10K_4 SB_RSMRST#
modify MV
2,29 NEW_CLKREQ# T70
2,28 LAN_CLKREQ#
23 WEBCAM_OFF
33 MC2_DISABLE
25 SPKR
2,5,6,7,29,31,33 PCLK_SMB
2,5,6,7,29,31,33 PDAT_SMB
SB_SMBCLK1 SB_SMBDATA1
modify DB2
2,33 WLAN_CLKREQ# T69
CRD_CLKREQ#
28 LP_EN#
D18 RB501V-40 LID_SW# SB
23,27,31 LID_SW#
D17 RB501V-40 GATEA20_SB
27 GATEA20
modify PV
3,18,31 CPU_THERMTRIP#
D22 RB501V-40 SB_THERMTRIP#
29 NEW_CPPE#
5 PM_THERM#
R438 150K/F_4
27,36,37 ADP_PRES
SB_JTAG_TDO SB_JTAG_TCK SB_JTAG_TDI SB_JTAG_RST#

HD audio interface is +3VS5 voltage

R140 *10K/F_4
16 ACZ_SDOUT
ACZ_BCLK ACZ_SDOUT ACZ_SDIN0 ACZ_SDIN1 ACZ_SYNC ACZ_RST#

T81 ADP_PRES0
modify PV
C689 *10P/50V_4

CN32 +3VS5
SB_JTAG_TCK SB_JTAG_TDO SB_JTAG_TDI SB_TEST1 SB_JTAG_RST#
SB JTAG
*S/W JTAG DEBUG

U11D
SB800 Part 4 of 5

PCI_PME#/GEVENT4# RI#/GEVENT22# SPI_CS3#/GBE_STAT1/GEVENT21# SLP_S3# SLP_S5# PWR_BTN# PWR_GOOD SUS_STAT# TEST0 TEST1/TMS TEST2 GA20IN/GEVENT0# KBRST#/GEVENT1# LPC_PME#/GEVENT3# LPC_SMI#/GEVENT23# GEVENT5# SYS_RESET#/GEVENT19# WAKE#/GEVENT8# IR_RX1/GEVENT20# THRMTRIP#/SMBALERT#/GEVENT2# NB_PWRGD RSMRST#
ACPI / WAKE UP EVENTS
USB 1.1 USB MISC

CLK_REQ4#/SATA_IS0#/GPIO64 CLK_REQ3#/SATA_IS1#/GPIO63 SMARTVOLT1/SATA_IS2#/GPIO50 CLK_REQ0#/SATA_IS3#/GPIO60 SATA_IS4#/FANOUT3/GPIO55 SATA_IS5#/FANIN3/GPIO59 SPKR/GPIO66 SCL0/GPIO43 SDA0/GPIO47 SCL1/GPIO227 SDA1/GPIO228 CLK_REQ2#/FANIN4/GPIO62 CLK_REQ1#/FANOUT4/GPIO61 IR_LED#/LLB#/GPIO184 SMARTVOLT2/SHUTDOWN#/GPIO51 DDR3_RST#/GEVENT7# GBE_LED0/GPIO183 GBE_LED1/GEVENT9# GBE_LED2/GEVENT10# GBE_STAT0/GEVENT11# CLK_REQG#/GPIO65/OSCIN
GPIO
USB 2.0

BLINK/USB_OC7#/GEVENT18# USB_OC6#/IR_TX1/GEVENT6# USB_OC5#/IR_TX0/GEVENT17# USB_OC4#/IR_RX0/GEVENT16# USB_OC3#/AC_PRES/TDO/GEVENT15# USB_OC2#/TCK/GEVENT14# USB_OC1#/TDI/GEVENT13# USB_OC0#/TRST#/GEVENT12#
USB OC

AZ_BITCLK AZ_SDOUT AZ_SDIN0/GPIO167 AZ_SDIN1/GPIO168 AZ_SDIN2/GPIO169 AZ_SDIN3/GPIO170 AZ_SYNC AZ_RST#
HD AUDIO

GBE_COL GBE_CRS GBE_MDCK GBE_MDIO GBE_RXCLK GBE_RXD3 GBE_RXD2 GBE_RXD1 GBE_RXD0 GBE_RXCTL/RXDV GBE_RXERR GBE_TXCLK GBE_TXD3 GBE_TXD2 GBE_TXD1 GBE_TXD0 GBE_TXCTL/TXEN GBE_PHY_PD GBE_PHY_RST# GBE_PHY_INTR
GBE LAN

PS2_DAT/SDA4/GPIO187 PS2_CLK/SCL4/GPIO188 SPI_CS2#/GBE_STAT2/GPIO166 FC_RST#/GPO160 PS2KB_DAT/GPIO189 PS2KB_CLK/GPIO190 PS2M_DAT/GPIO191 PS2M_CLK/GPIO192
EMBEDDED CTRL

SB800 A11

USBCLK/14M_25M_48M_OSC A10 E_48M_USB 2
USB_RCOMP G19 USB_RCOMP_SB R433 11.8K/F_6
for EMI E_48M_USB C198 *2.2P/50V_4

USB_FSD1P/GPIO186 USB_FSD1N J10 H11 USBFSDP1+ 32 USBFSDP1- 32 Finger Printer
USB_FSD0P/GPIO185 USB_FSD0N H9 J8 USB_FDS12P USB_FSD12N T78 T76

USB_HSD13P USB_HSD13N B12 A12
USB_HSD12P USB_HSD12N F11 E11
USB_HSD11P USB_HSD11N E14 E12
USB_HSD10P USB_HSD10N J12 J14
USB_HSD9P USB_HSD9N A13 B13 USBP9+ 32 USBP9- 32 BLUETOOTH
USB_HSD8P USB_HSD8N D13 C13 USBP8+ 33 USBP8- 33 WLAN Min-Card
USB_HSD7P USB_HSD7N G12 G14 USBP7+ 33 USBP7- 33 WWAN
USB_HSD6P USB_HSD6N G16 G18 USBP6+ 30 USBP6- 30 USB card reader
USB_HSD5P USB_HSD5N D16 C16 USBP5+ 29 USBP5- 29 USB Connector
USB_HSD4P USB_HSD4N B14 A14 USBP4+ 23 USBP4- 23 Carama USB
USB_HSD3P USB_HSD3N E18 E16 USBP3+ 29 USBP3- 29 USB Connector
USB_HSD2P USB_HSD2N J16 J18 USBP2+ 29 USBP2- 29 E-SATA and USB Connector
USB_HSD1P USB_HSD1N B17 A17 USBP1+ 29 USBP1- 29 New Card
USB_HSD0P USB_HSD0N A16 B16 USBP0+ 29 USBP0- 29 USB Connector

SCL2/GPIO193 SDA2/GPIO194 SCL3_LV/GPIO195 SDA3_LV/GPIO196 D25 F23 B26 E26 SB_SCLK2 SB_SDATA2 CPU_SIC 3,5 CPU_SID 3,5
EC_PWM0/EC_TIMER0/GPIO197 EC_PWM1/EC_TIMER1/GPIO198 EC_PWM2/EC_TIMER2/GPIO199 EC_PWM3/EC_TIMER3/GPIO200 E25 E22 F22 E21 GPIO199 GPIO200 GPIO199 16 GPIO200 16

KSI_0/GPIO201 KSI_1/GPIO202 KSI_2/GPIO203 KSI_3/GPIO204 KSI_4/GPIO205 KSI_5/GPIO206 KSI_6/GPIO207 KSI_7/GPIO208
KSO_0/GPIO209 KSO_1/GPIO210 KSO_2/GPIO211 KSO_3/GPIO212 KSO_4/GPIO213 KSO_5/GPIO214 KSO_6/GPIO215 KSO_7/GPIO216 KSO_8/GPIO217 KSO_9/GPIO218 KSO_10/GPIO219 KSO_11/GPIO220 KSO_12/GPIO221 KSO_13/GPIO222 KSO_14/GPIO223 KSO_15/GPIO224 KSO_16/GPIO225 KSO_17/GPIO226
EMBEDDED CTRL

U10 TC7SH08FU +3VS5 SUSB# MAINON 20,35,36,40,41,43
U9 TC7SH08FU +3VS5 SUSC# SUSON 28,40,43

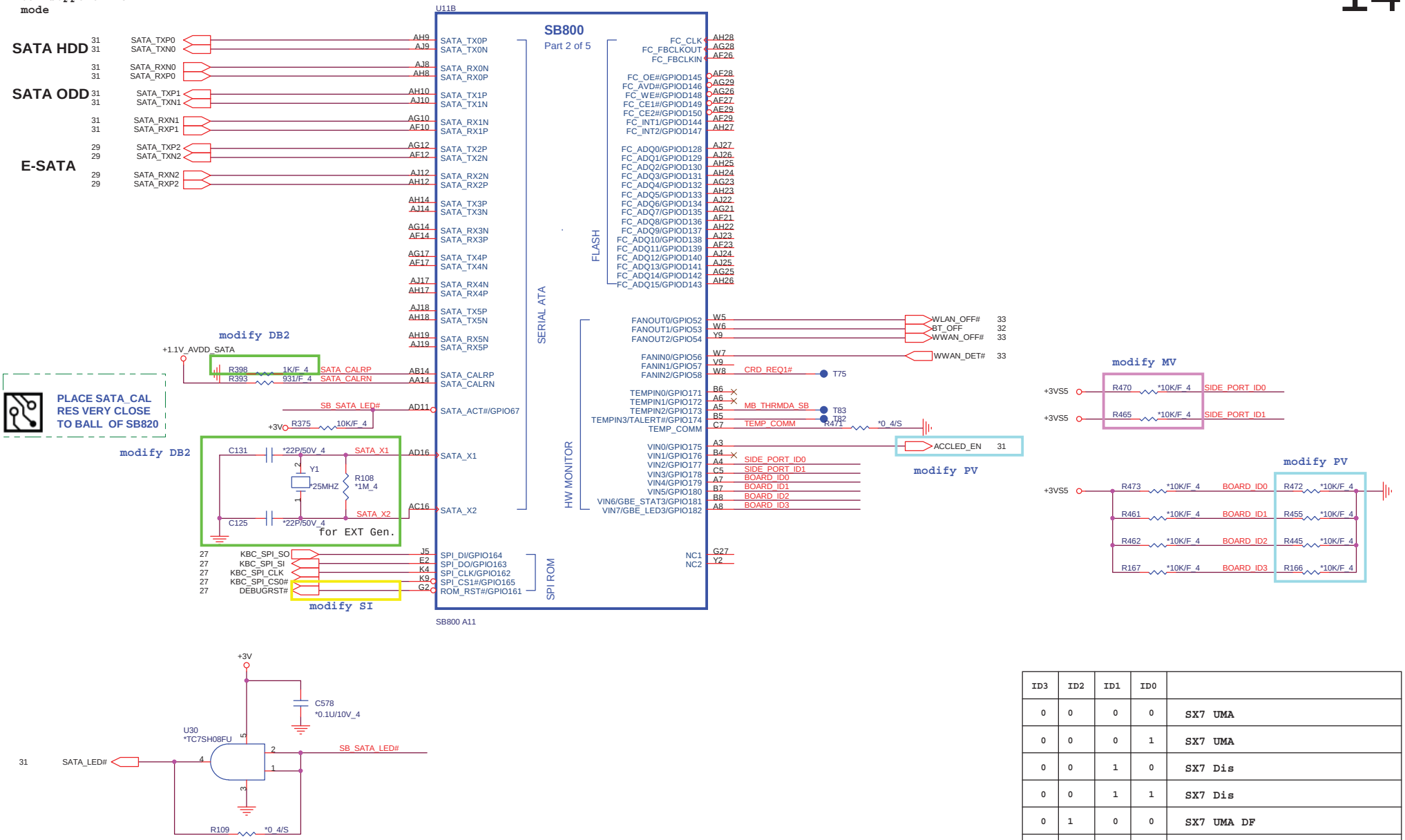
NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-ACPI/GPIO/USB 2/4	3A

Date: Monday, March 15, 2010 Sheet 13 of 43

SATA PORT 0,1,2,3
can support AHCI
mode



ID3	ID2	ID1	ID0	
0	0	0	0	SX7 UMA
0	0	0	1	SX7 UMA
0	0	1	0	SX7 Dis
0	0	1	1	SX7 Dis
0	1	0	0	SX7 UMA DF
0	1	0	1	SX7 UMA DF
0	1	1	0	SX7 Dis DF
0	1	1	1	SX7 Dis DF

NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
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Date: Monday, March 15, 2010 | Sheet 14 of 43

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

VDDQ--3.3V I/O power

VDD-- S/B CORE power

SB820 without GBE: Connected to GND plane.

modify DB2

For support USB wakeup-->3V_S5

SB800 A11

Part 3 of 5

Part 5 of 5

NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size: Custom | Document Number: SB820-PWR/DECOUPLING 4/4 | Rev: 3A

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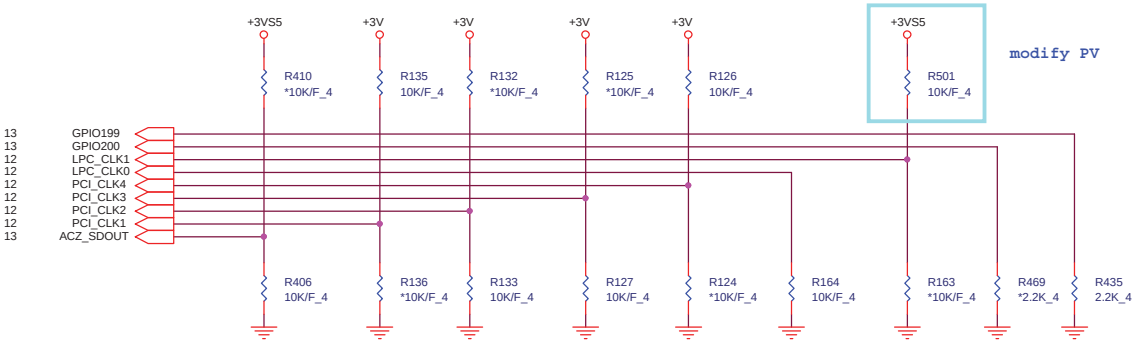
REQUIRED STRAPS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



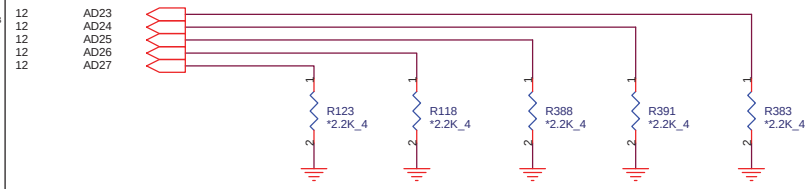
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM DEFAULT
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM L, L=FWH ROM

modify DB2

internal have pull Hi 10K

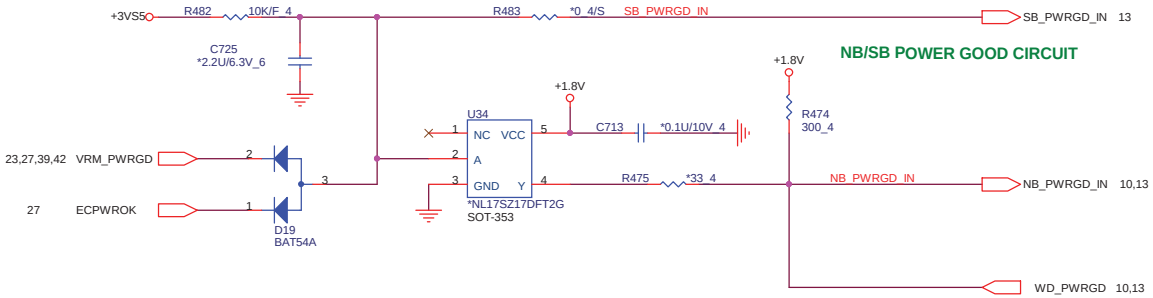
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-STRAPS	3A

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NB5/RD2

POWER
for M9x-S3 DPx_VDD10=1.1V
for Park-S3 DPx_VDD10=1.0V

U6A

2.5GT/s bit rate

PCI EXPRESS INTERFACE

9	PEG_TX0	PEG_TX0	AE30	PCIE_RX0P	PCIE_TX0P	AH30	C_PEG_RX0	C577	0.1U/10V_4	PEG_RX0	9
9	PEG_TX#0	PEG_TX#0	AE31	PCIE_RX0N	PCIE_TX0N	AG31	C_PEG_RX#0	C575	0.1U/10V_4	PEG_RX#0	9
9	PEG_TX1	PEG_TX1	AE29	PCIE_RX1P	PCIE_TX1P	AG29	C_PEG_RX1	C569	0.1U/10V_4	PEG_RX1	9
9	PEG_TX#1	PEG_TX#1	AD28	PCIE_RX1N	PCIE_TX1N	AF28	C_PEG_RX#1	C570	0.1U/10V_4	PEG_RX#1	9
9	PEG_TX2	PEG_TX2	AD30	PCIE_RX2P	PCIE_TX2P	AF27	C_PEG_RX2	C571	0.1U/10V_4	PEG_RX2	9
9	PEG_TX#2	PEG_TX#2	AC31	PCIE_RX2N	PCIE_TX2N	AF26	C_PEG_RX#2	C572	0.1U/10V_4	PEG_RX#2	9
9	PEG_TX3	PEG_TX3	AC29	PCIE_RX3P	PCIE_TX3P	AD27	C_PEG_RX3	C573	0.1U/10V_4	PEG_RX3	9
9	PEG_TX#3	PEG_TX#3	AB28	PCIE_RX3N	PCIE_TX3N	AD26	C_PEG_RX#3	C574	0.1U/10V_4	PEG_RX#3	9
9	PEG_TX4	PEG_TX4	AB30	PCIE_RX4P	PCIE_TX4P	AC25	C_PEG_RX4	C566	0.1U/10V_4	PEG_RX4	9
9	PEG_TX#4	PEG_TX#4	AA31	PCIE_RX4N	PCIE_TX4N	AB25	C_PEG_RX#4	C560	0.1U/10V_4	PEG_RX#4	9
9	PEG_TX5	PEG_TX5	AA29	PCIE_RX5P	PCIE_TX5P	Y23	C_PEG_RX5	C568	0.1U/10V_4	PEG_RX5	9
9	PEG_TX#5	PEG_TX#5	Y28	PCIE_RX5N	PCIE_TX5N	Y24	C_PEG_RX#5	C567	0.1U/10V_4	PEG_RX#5	9
9	PEG_TX6	PEG_TX6	Y30	PCIE_RX6P	PCIE_TX6P	AB27	C_PEG_RX6	C558	0.1U/10V_4	PEG_RX6	9
9	PEG_TX#6	PEG_TX#6	W31	PCIE_RX6N	PCIE_TX6N	AB26	C_PEG_RX#6	C551	0.1U/10V_4	PEG_RX#6	9
9	PEG_TX7	PEG_TX7	W29	PCIE_RX7P	PCIE_TX7P	Y27	C_PEG_RX7	C548	0.1U/10V_4	PEG_RX7	9
9	PEG_TX#7	PEG_TX#7	V28	PCIE_RX7N	PCIE_TX7N	Y26	C_PEG_RX#7	C545	0.1U/10V_4	PEG_RX#7	9
9	PEG_TX8	PEG_TX8	V30	PCIE_RX8P	PCIE_TX8P	W24	C_PEG_RX8	C543	0.1U/10V_4	PEG_RX8	9
9	PEG_TX#8	PEG_TX#8	U31	PCIE_RX8N	PCIE_TX8N	W23	C_PEG_RX#8	C535	0.1U/10V_4	PEG_RX#8	9
9	PEG_TX9	PEG_TX9	U29	PCIE_RX9P	PCIE_TX9P	V27	C_PEG_RX9	C534	0.1U/10V_4	PEG_RX9	9
9	PEG_TX#9	PEG_TX#9	T28	PCIE_RX9N	PCIE_TX9N	U26	C_PEG_RX#9	C525	0.1U/10V_4	PEG_RX#9	9
9	PEG_TX10	PEG_TX10	T30	PCIE_RX10P	PCIE_TX10P	U24	C_PEG_RX10	C450	0.1U/10V_4	PEG_RX10	9
9	PEG_TX#10	PEG_TX#10	R31	PCIE_RX10N	PCIE_TX10N	U23	C_PEG_RX#10	C442	0.1U/10V_4	PEG_RX#10	9
9	PEG_TX11	PEG_TX11	R29	PCIE_RX11P	PCIE_TX11P	T26	C_PEG_RX11	C501	0.1U/10V_4	PEG_RX11	9
9	PEG_TX#11	PEG_TX#11	P28	PCIE_RX11N	PCIE_TX11N	T27	C_PEG_RX#11	C492	0.1U/10V_4	PEG_RX#11	9
9	PEG_TX12	PEG_TX12	P30	PCIE_RX12P	PCIE_TX12P	T24	C_PEG_RX12	C469	0.1U/10V_4	PEG_RX12	9
9	PEG_TX#12	PEG_TX#12	N31	PCIE_RX12N	PCIE_TX12N	T23	C_PEG_RX#12	C456	0.1U/10V_4	PEG_RX#12	9
9	PEG_TX13	PEG_TX13	N29	PCIE_RX13P	PCIE_TX13P	P27	C_PEG_RX13	C503	0.1U/10V_4	PEG_RX13	9
9	PEG_TX#13	PEG_TX#13	M28	PCIE_RX13N	PCIE_TX13N	P26	C_PEG_RX#13	C516	0.1U/10V_4	PEG_RX#13	9
9	PEG_TX14	PEG_TX14	M30	PCIE_RX14P	PCIE_TX14P	P24	C_PEG_RX14	C519	0.1U/10V_4	PEG_RX14	9
9	PEG_TX#14	PEG_TX#14	L31	PCIE_RX14N	PCIE_TX14N	P23	C_PEG_RX#14	C524	0.1U/10V_4	PEG_RX#14	9
9	PEG_TX15	PEG_TX15	L29	PCIE_RX15P	PCIE_TX15P	M27	C_PEG_RX15	C472	0.1U/10V_4	PEG_RX15	9
9	PEG_TX#15	PEG_TX#15	K30	PCIE_RX15N	PCIE_TX15N	N26	C_PEG_RX#15	C488	0.1U/10V_4	PEG_RX#15	9

CLOCK

12	CLK_PCIE_VGA	CLK_PCIE_VGA	AK30	PCIE_REFCLKP
12	CLK_PCIE_VGA#	CLK_PCIE_VGA#	AK32	PCIE_REFCLKN

M9x-S3:PWRGOOD NC
Park-S3:PWRGOOD Pull low 10K

*10K/F_4 1 2 R53 N10 PWRGOOD

12 PCIE_RST# AL27 PERSTB

CALIBRATION

PCIE_CALRP Y22 PCIE_CALRP R320 1.27K/F_4
PCIE_CALRN AA22 PCIE_CALRN R350 2K/F_4 +1.1V_PCIE_VDDC

M9X-S2/S3 + Park-S3

100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing

U6G

DP E/F POWER

1.8V(200mA)
+1.8V_DPE_VDD18 AG15 DPE_VDD18#1 AG16 DPE_VDD18#2
M9x-S3:TMDS 1.1V@170mA LVDS 1.1V@100mA
Park-S3:TMDS 1.0V@110mA LVDS 1.0V@120mA
+1.1V_DPE_VDD10 AG20 DPE_VDD10#1 AG21 DPE_VDD10#2
AG14 DPE_VSSR#1 AH14 DPE_VSSR#2 AM14 DPE_VSSR#3 AM16 DPE_VSSR#4 AM18 DPE_VSSR#5

1.8V(200mA)
+1.8V_DPE_VDD18 AF16 DPF_VDD18#1 AG17 DPF_VDD18#2
M9x-S3:TMDS 1.1V@170mA LVDS 1.1V@100mA
Park-S3:TMDS 1.0V@110mA LVDS 1.0V@120mA
+1.1V_DPE_VDD10 AF22 DPF_VDD10#1 AG22 DPF_VDD10#2
AF23 DPF_VSSR#1 AG23 DPF_VSSR#2 AM20 DPF_VSSR#3 AM22 DPF_VSSR#4 AM24 DPF_VSSR#5

R113 150/F_4 AF17 DPEF_CALR

1.8V(20mA)
+1.8V_DPE_PVDD AG18 DPE_PVDD AF19 DPE_PVSS
1.8V(20mA)
+1.8V_DPE_PVDD AG19 DPF_PVDD AF20 DPF_PVSS

DP A/B POWER

1.8V(130mA)
AE11 DPA_VDD18#1 AE11 DPA_VDD18#2 +1.8V_DPA_PVDD
M9x-S3:1.1V@200mA Park-S3:1.0V@110mA
AF6 +1.1V_DPB_VDD10 DPA_VDD10#1 AF7 DPA_VDD10#2 +1.1V_DPB_VDD10
AE1 DPA_VSSR#1 AE3 DPA_VSSR#2 AC1 DPA_VSSR#3 AG6 DPA_VSSR#4 AH5 DPA_VSSR#5

1.8V(130mA)
AE13 DPB_VDD18#1 AE13 DPB_VDD18#2 +1.8V_DPA_PVDD
M9x-S3:1.1V@200mA Park-S3:1.0V@110mA
BLM18PG181SN1D(180,1.5A)_6
AF8 +1.1V_DPB_VDD10 DPB_VDD10#1 AF9 DPB_VDD10#2 L50 +1.0V_VGA
C588 0.1U/10V_4 C584 10U/6.3V_8 C557 1000P/50V_4
AE10 DPB_VSSR#1 AG9 DPB_VSSR#2 AH8 DPB_VSSR#3 AM6 DPB_VSSR#4 AM8 DPB_VSSR#5

AE10 R358 150/F_4 DPAB_CALR

1.8V(20mA)
AG8 +1.8V_DPA_PVDD DPA_PVDD AG7 DPA_PVSS +1.8V_DPA_PVDD
1.8V(20mA)
AG10 +1.8V_DPA_PVDD DPB_PVDD AG11 DPB_PVSS +1.8V_DPA_PVDD

DP PLL POWER

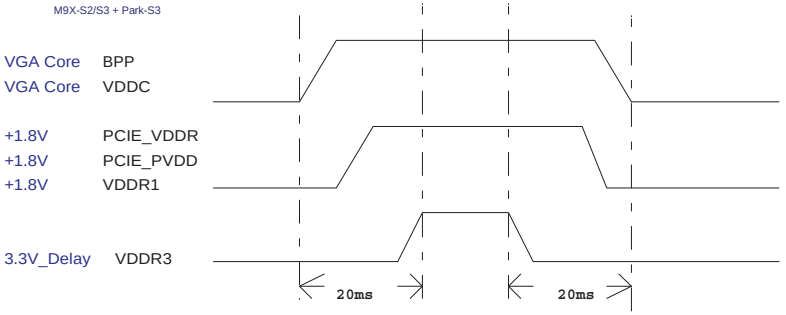
M9X-S2/S3 + Park-S3

+1.1V_DPE_VDD10
+1.1V_DPE_VDD10 L54 +1.0V_VGA
BLM18PG181SN1D(180,1.5A)_6
C580 0.1U/10V_4 C563 1000P/50V_4 C599 10U/6.3V_8

+1.8V_DPA_PVDD
+1.8V_DPA_PVDD L46 +1.8V
BLM18PG181SN1D(180,1.5A)_6
C583 0.1U/10V_4 C561 1000P/50V_4 C591 10U/6.3V_8

+1.8V_DPE_VDD18
+1.8V_DPE_VDD18 L11 +1.8V
BLM18PG181SN1D(180,1.5A)_6
C565 0.1U/10V_4 C552 1U/10V_4 C127 10U/6.3V_8

+1.8V_DPE_PVDD
+1.8V_DPE_PVDD L56 +1.8V
BLM18PG181SN1D(180,1.5A)_6
C602 0.1U/10V_4 C610 1000P/50V_4 C596 10U/6.3V_8



PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Park_PCIE_Interface	3A
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NB5/RD2

MEM_ID[2:0]	Vendor	Type	Vendor P/N
000	Samsung E-die	64M*16-800MHZ	K4W1G1646E-HC12
100	Hynix Orion-die	64M*16-800MHZ	H5TQ1G63BFR-12C
010	Samsung E-die	128M*16-800MHZ	
110	Hynix Orion-die	128M*16-800MHZ	

	PWRCNTL1	PWRCNTL0	V-CORE
	1	1	0.9V
	1	0	0.95V
	0	1	1.05V
	0	0	1.1V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V

No need "CLK_27M_SS" connect to GPIO_16, since M9x chip support memory SS function in VBIOS

modify PV

modify PV

modify PV

modify PV

modify PV

modify SI

Memory ID

R56 10K/F_4 GPIO22

GPIO22(ROMCS#)
PD without external VBIOS ROM

1.8V(200mA DPC_PVDD)

1.8V(130mA DPC_VDD18)

1.1V(110mA DPC_VDD10)

For Park-S3 only

M93-S3/ Park-S3:Use 150R Pull down
Park-S3:NC

1.8V(70mA)

1.8V(90mA VDD1DI+VDD2DI)

ADD VGA TEMP_ FAIL function
M93 is active Hi

1.8V(75mA DPLL_PVDD)

1.0V(125mA DPLL_VDDC)
1.1V(150mA DPLL_VDDC)

1.8V(20mA TSVDD)

CL=20PF

For Int Clk 27Mhz

M9X-S2/S3 + Park-S3

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Park_Main	3A
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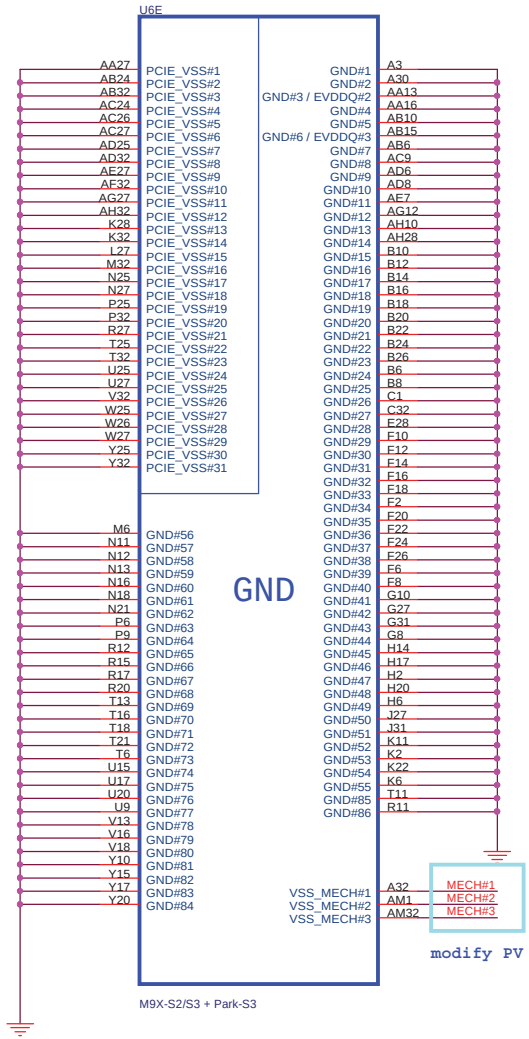
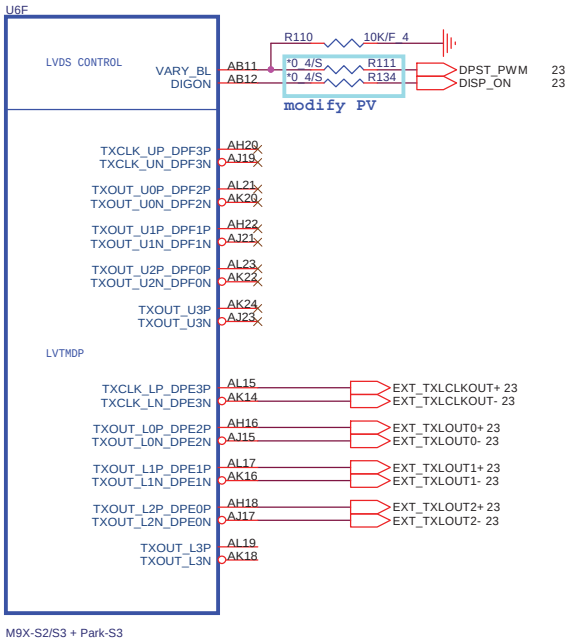
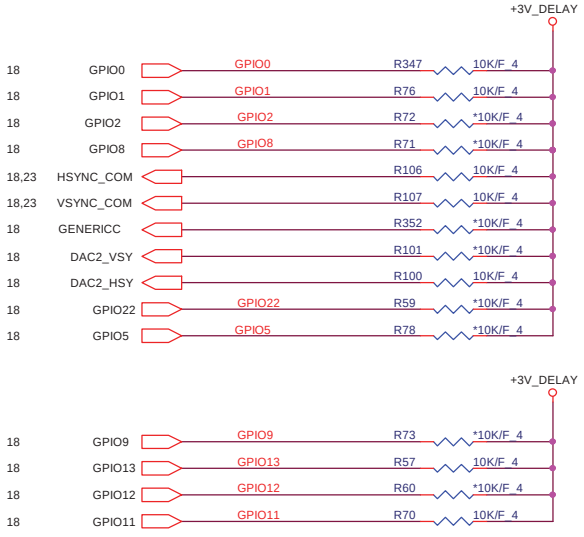
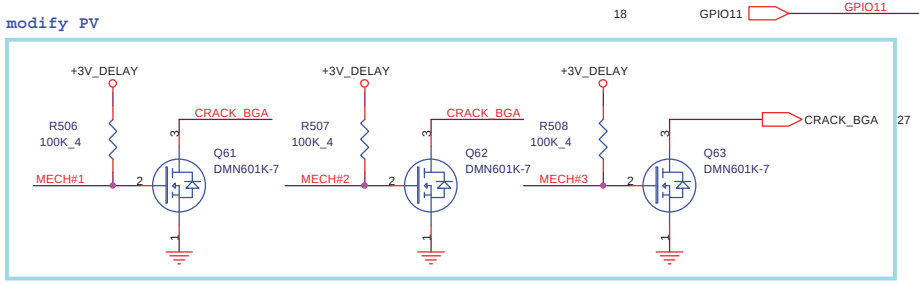
NB5/RD2









Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	**PCI Express Full TX Output Swing** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	**Enable CLKREQ# Power Management** 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0 0 0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	1
AUD[0] AUD(1)	VSYNC HSYNC	**AUD[1] AUD[0]** 00 No Audio function 01 Audio for DisplayPort and HDMI if dongle is detected 10 Audio for DisplayPort only 11 Audio for both DisplayPort and HDMI	1 1
VIP_DEVICE_STRAP_ENA	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
RSVD	GENERICC		0

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

PROJECT : SX7
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	Park_GND / LVDS/ Straps	3A
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PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

1.5V(2.A VDDR1+VDDRHA)

1.8V(110mA VDD_CT)

Gated 3.3V 60mA by VDDC

modify SI

VDD_R3 --IO power for 3.3 V pins (e.g. GPIO's). 3.3 V ± 5%

1.8V(170mA VDDR4)

1.8V(170mA VDDR5)

only for M93-S3 Used

1.8V(68mA PCIE_PVDD)

0.95V~1.1V(35mA SPV10)

1.5/1.8V 120mA

Park-S3 no support Back Bias

VDD_R4 -- Power for DVPDATA_[23:12] - external TMDS or GPIO; corresponds to DVOA_MSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%

VDD_R5 -- Power for DVP control pins (DVPCNTL_[0-2] and DVPCLK) and DVPDATA_[11:0] - external TMDS or GPIO; corresponds to DVOA_LSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%

only for Park-S3 Used

modify MV

BBP -- Connect to VBBP back bias regulator / generator. If back bias is not used, connect directly to VDDC.

Back Bias Enabled: (GPIO_21_BB_EN = 3.3 V): 1.5 V or 1.8 V

Back Bias Disabled: (GPIO_21_BB_EN = 0 V): VDDC

1.8V(500mA)

1.1V(2.0A)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

VDDC+VDDCI 0.95~1.1V(15A peak)(Ripple < 87.2mV)

VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2V (± 5%)

0.95V~1.1V(2A VDDCI)

VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

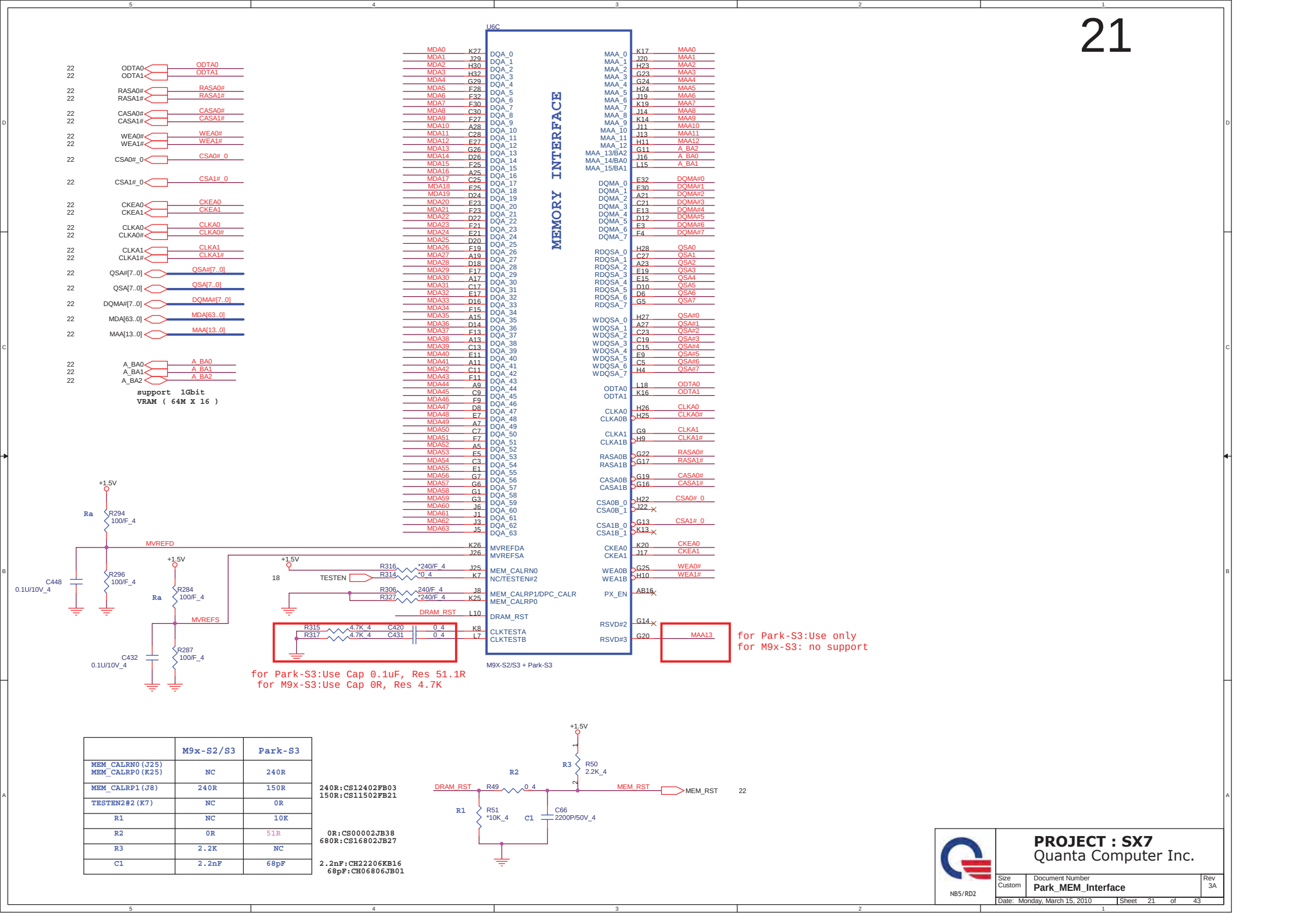
M9X-S2/S3 + Park-S3

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Park_Power_and_NC	3A

Date: Monday, March 15, 2010 Sheet 20 of 43

NB5/RD2



	M9x-S2/S3	Park-S3
MEM_CALRN0(J25) MEM_CALRP0(K25)	NC	240R
MEM_CALRP1(J8)	240R	150R
TESTEN2#2(K7)	NC	0R
R1	NC	10K
R2	0R	51R
R3	2.2K	NC
C1	2.2nF	68pF

240R:CS12402FB03
150R:CS11502FB21

0R:CS00002JB38
680R:CS16802JB27

2.2nF:CH22206KB16
68pF:CH06806JB01

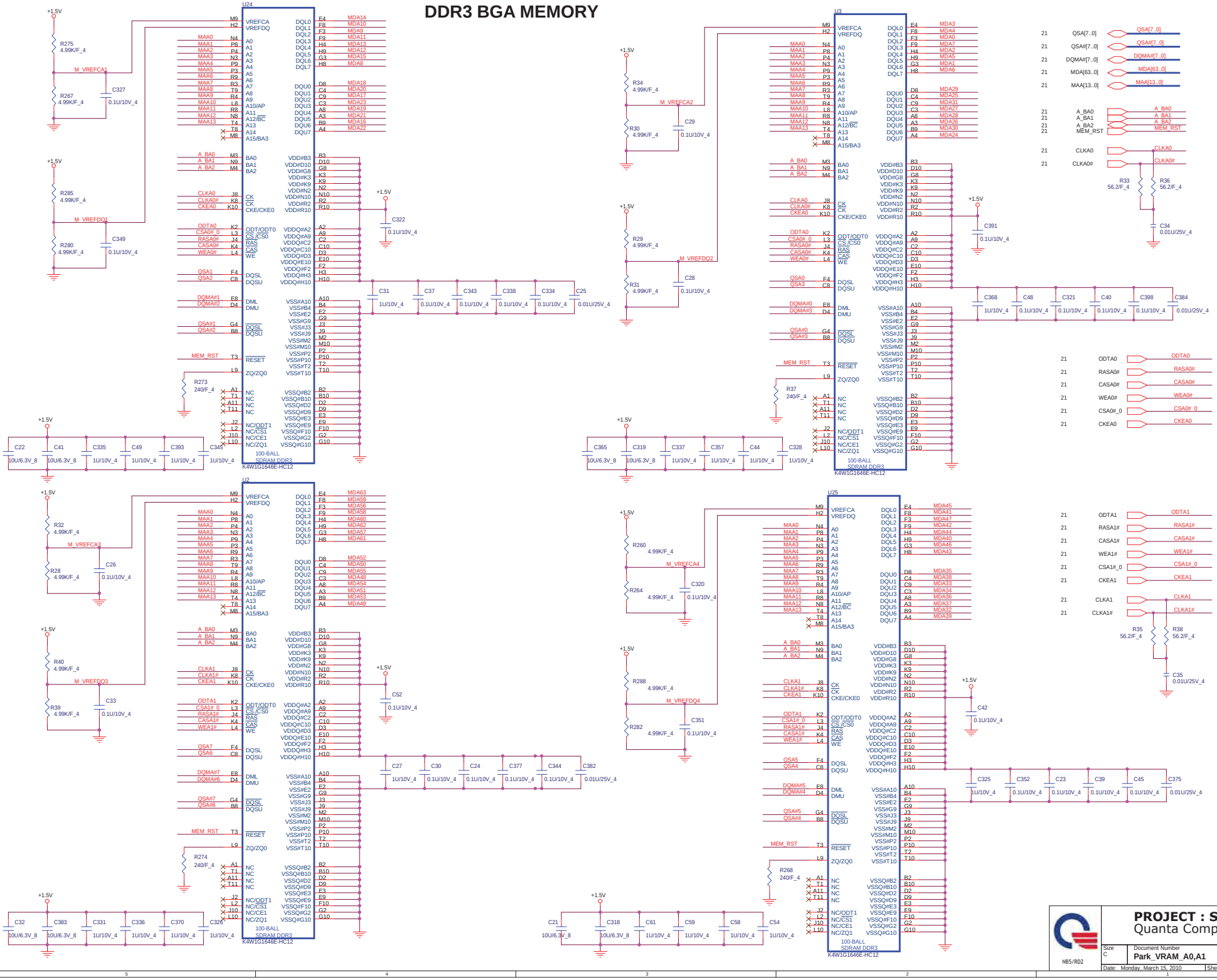
NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Park_MEM_Interface	3A

Date: Monday, March 15, 2010 Sheet 21 of 43

DDR3 BGA MEMORY

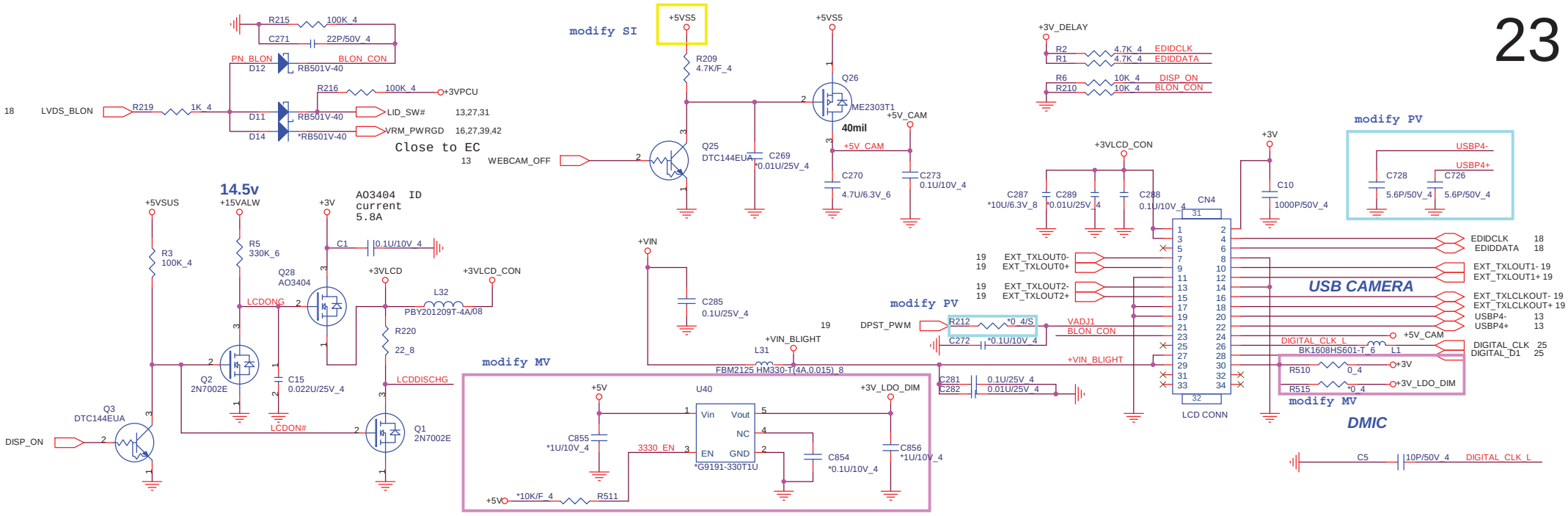


PROJECT : SX7
Quanta Computer Inc.

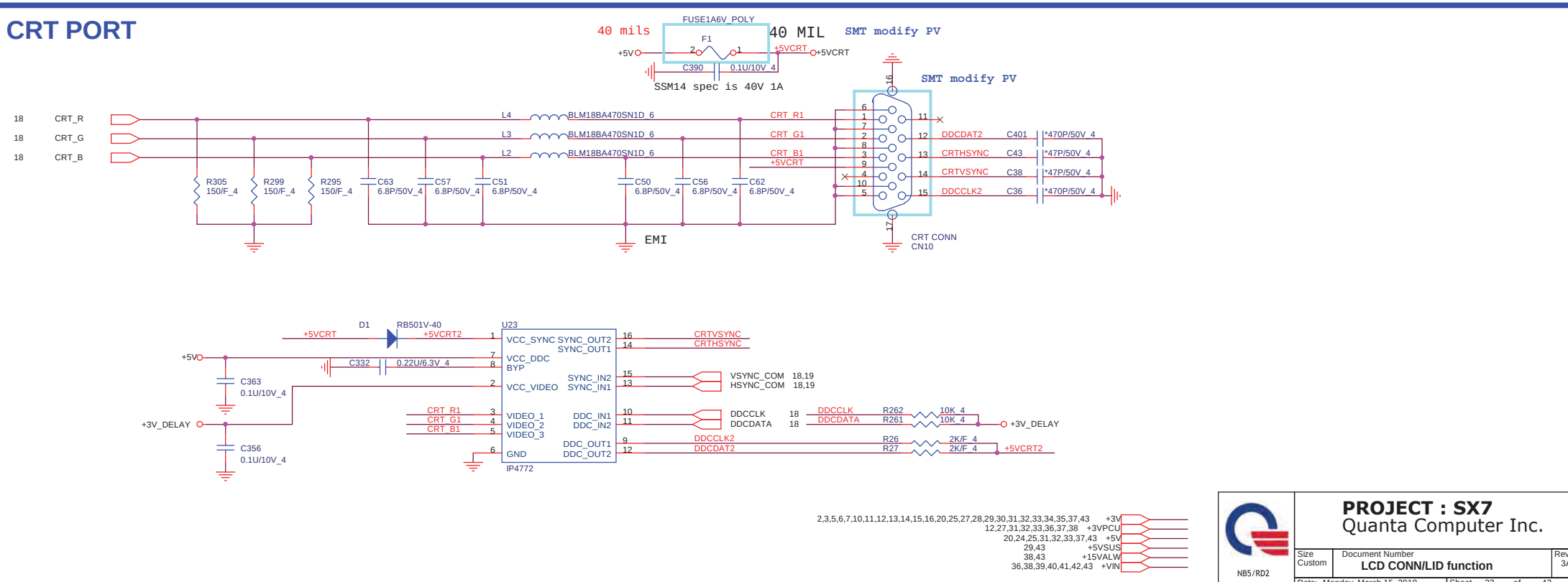
Size	Document Number	Rev
C	Park_VRAM_A0,A1	3A

NB5/RD2

Date: Monday, March 15, 2010 | Sheet 22 of 43



CRT PORT

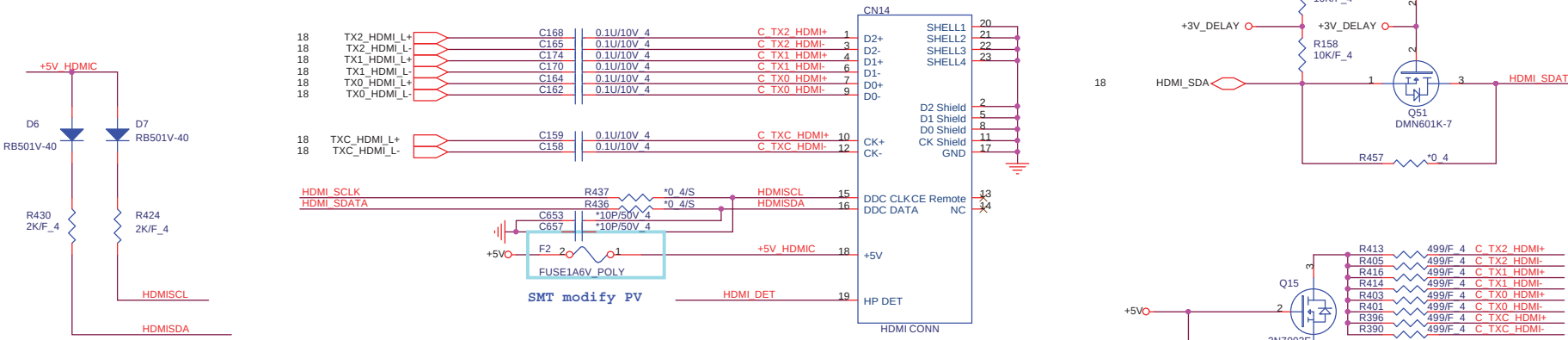


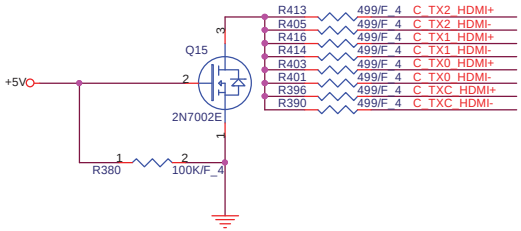
NB5/RD2

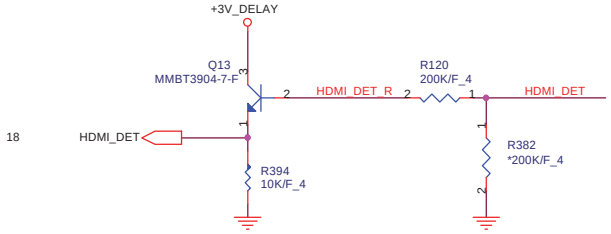
PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID function	3A
Date: Monday, March 15, 2010	Sheet 23 of 43	

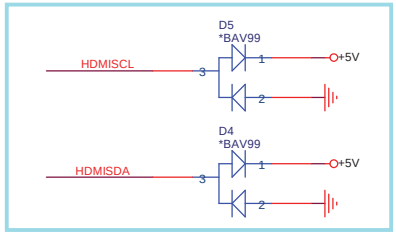
HDMI PORT







SMT modify PV



20,23,25,31,32,33,37,43 +5V

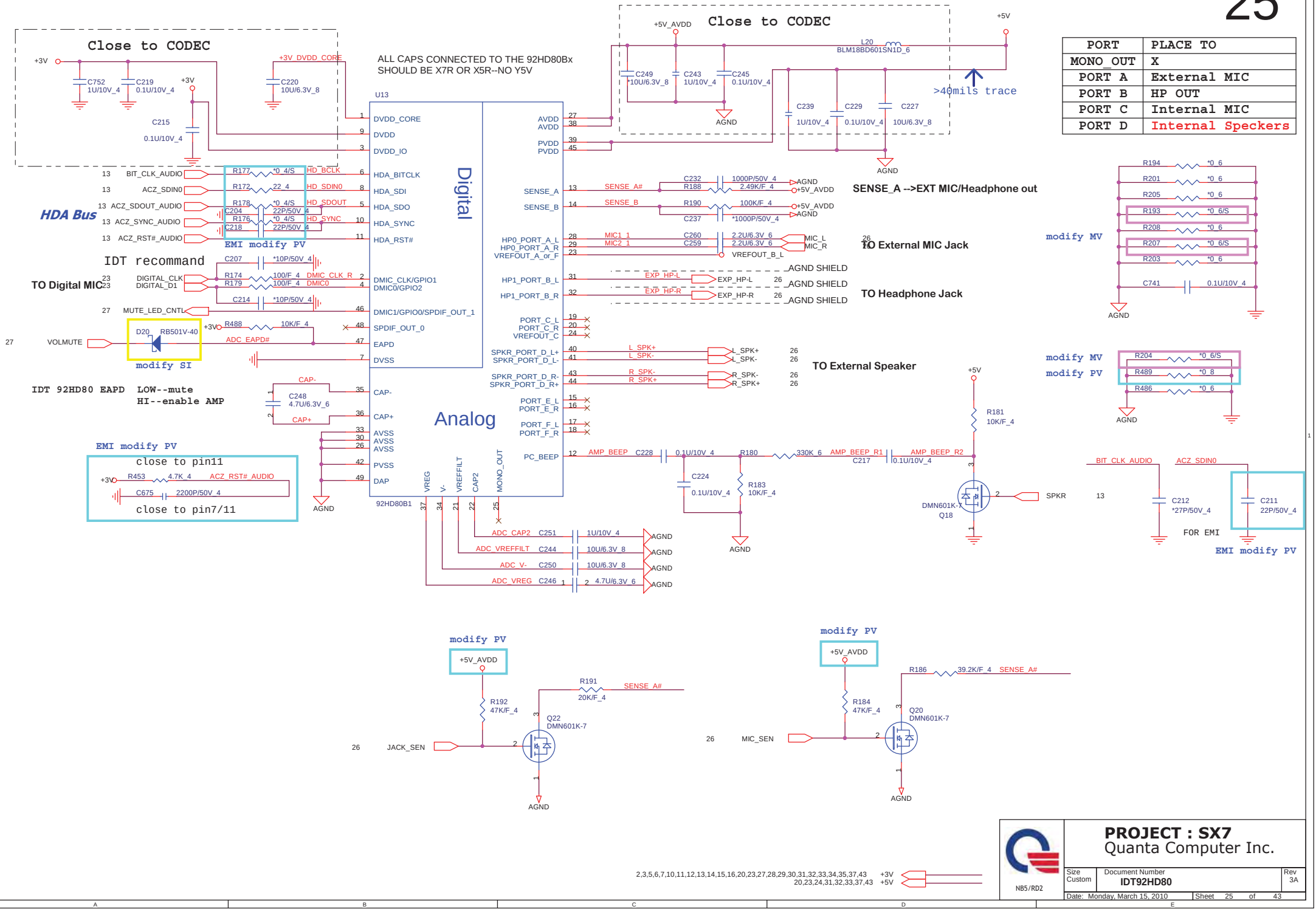
NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**HDMI Conn**	3A

Date: Monday, March 15, 2010 Sheet 24 of 43

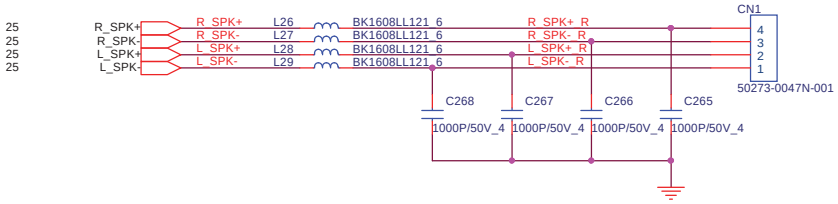
PORT	PLACE TO
MONO_OUT	X
PORT A	External MIC
PORT B	HP OUT
PORT C	Internal MIC
PORT D	Internal Speckers



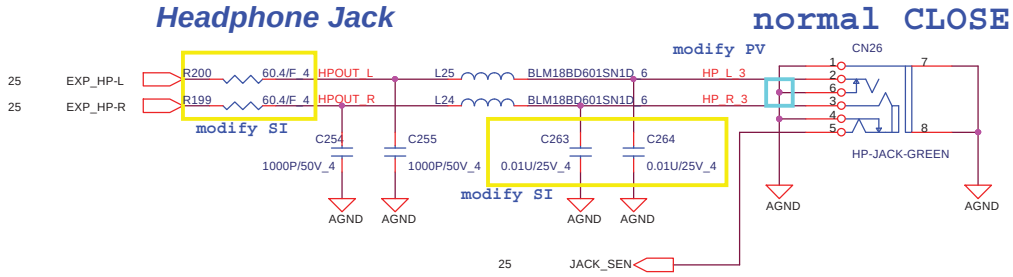
PROJECT : SX7	
Quanta Computer Inc.	
Size: Custom	Document Number: IDT92HD80
Rev: 3A	
Date: Monday, March 15, 2010	Sheet 25 of 43
NB5/RD2	

Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

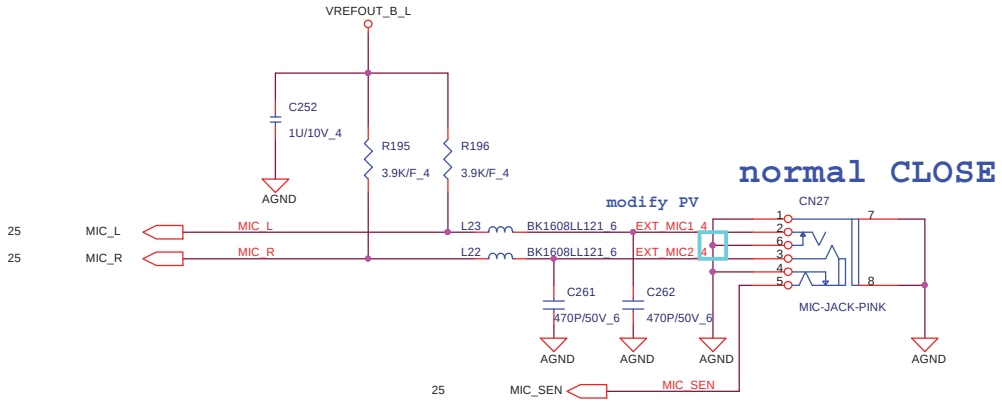
INT. SPEAKER



Headphone Jack

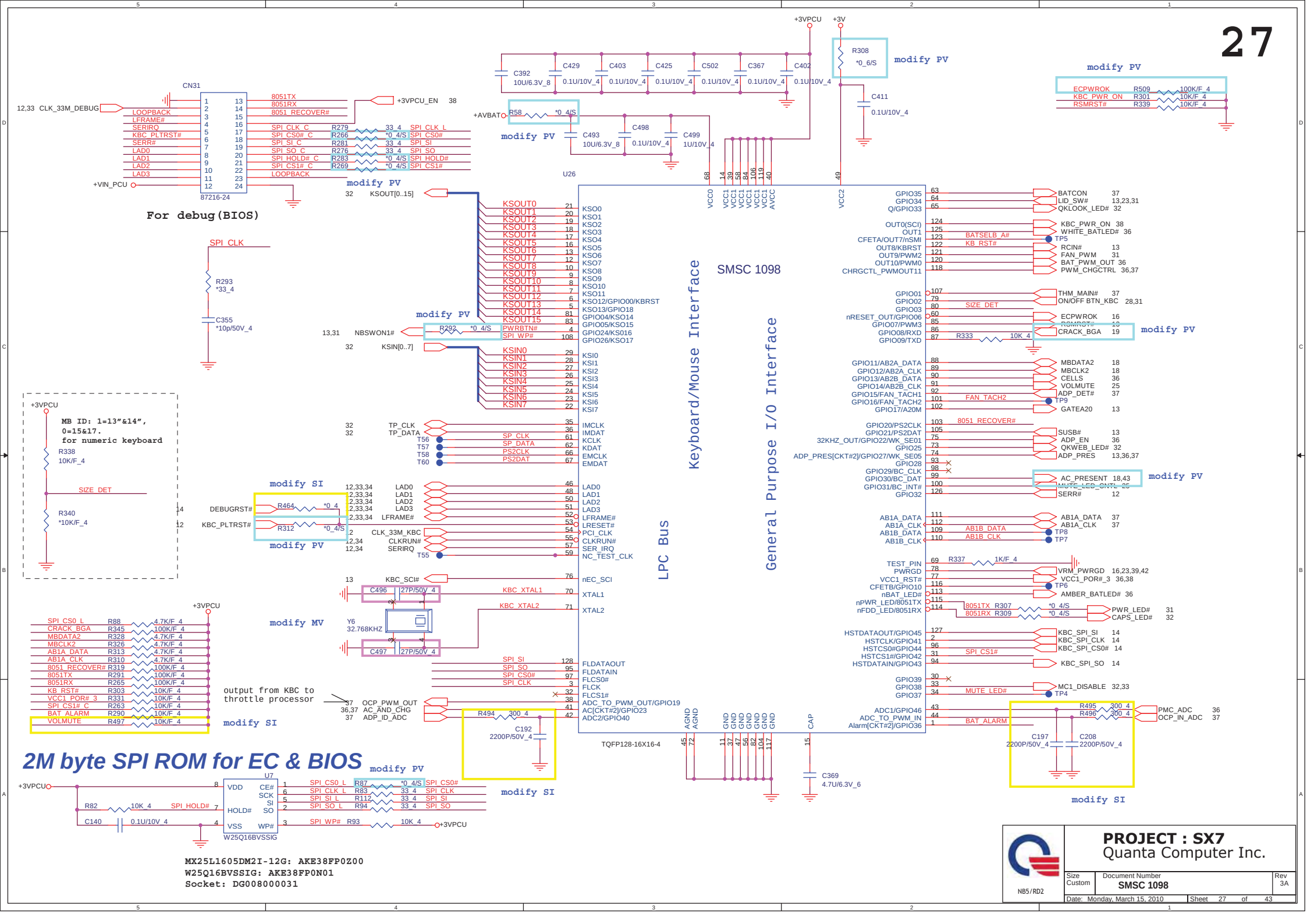


EXT Mic Jack

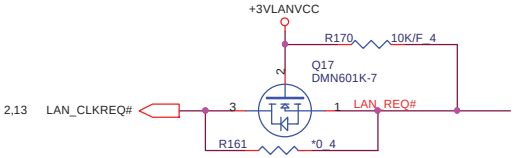


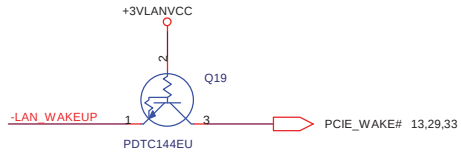
Note: MIC_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

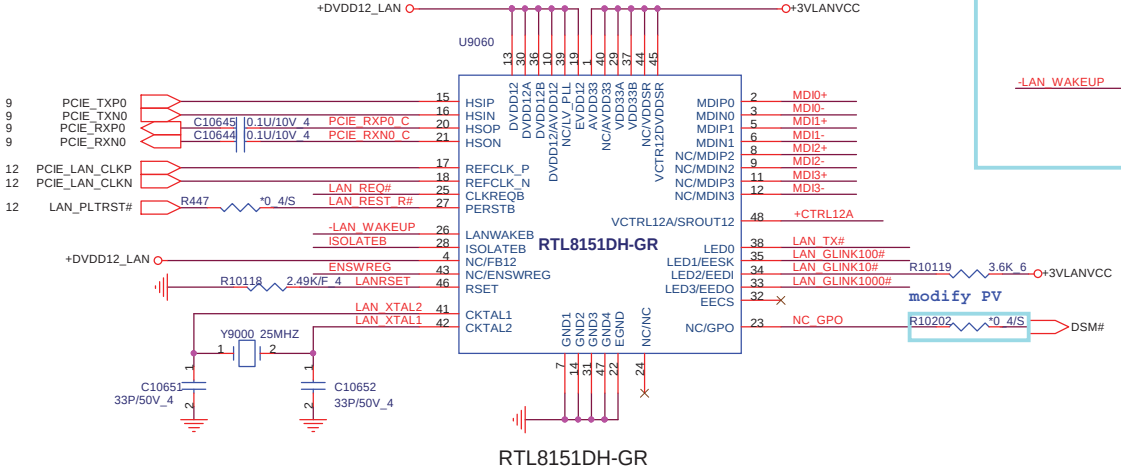
NB5/RD2	PROJECT : SX7 Quanta Computer Inc.	
Size: Custom	Document Number: HP/MIC/SPK	Rev: 3A
Date: Monday, March 15, 2010	Sheet 26 of 43	


SMSC 1098
Keyboard/Mouse Interface
General Purpose I/O Interface
LPC Bus
TQFP128-16X16-4
CN31
87216-24
For debug(BIOS)
modify PV
modify SI
modify MV
+3VPCU
+3V
+AVBAT
+VIN_PCU
U26
SPI_CLK
MB ID: 1=13"&14", 0=15&17. for numeric keyboard
output from KBC to throttle processor
2M byte SPI ROM for EC & BIOS
U7
W25Q16BVSSIG
MX25L1605DM2I-12G: AKE38FP0Z00
W25Q16BVSSIG: AKE38FP0N01
Socket: DG008000031
PROJECT : SX7
Quanta Computer Inc.
NB5/RD2
Document Number
SMSC 1098
Rev 3A
Size Custom
Date: Monday, March 15, 2010
Sheet 27 of 43

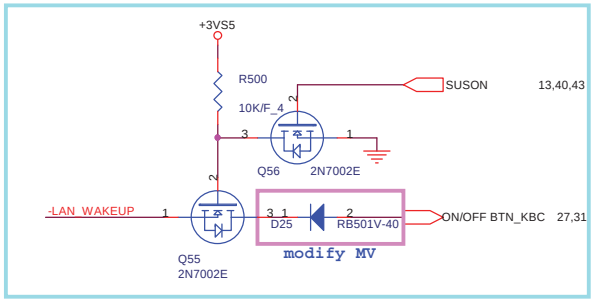
modify DB2

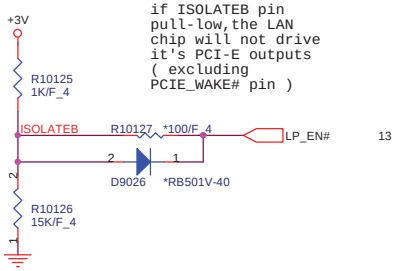




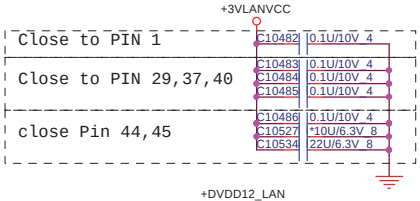


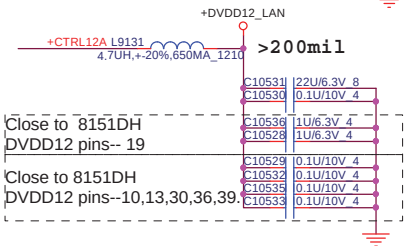
modify PV



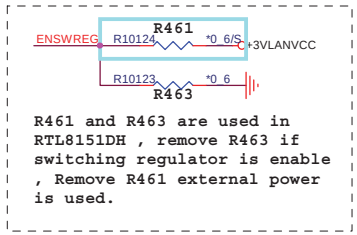


if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

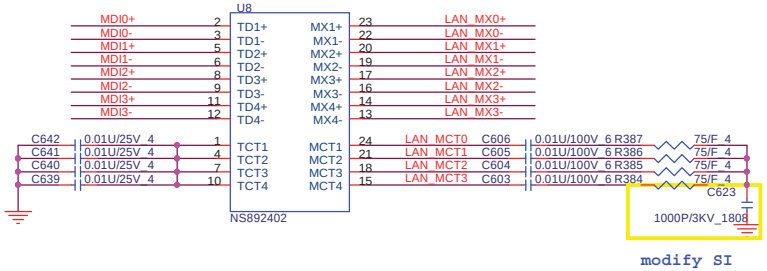




modify PV



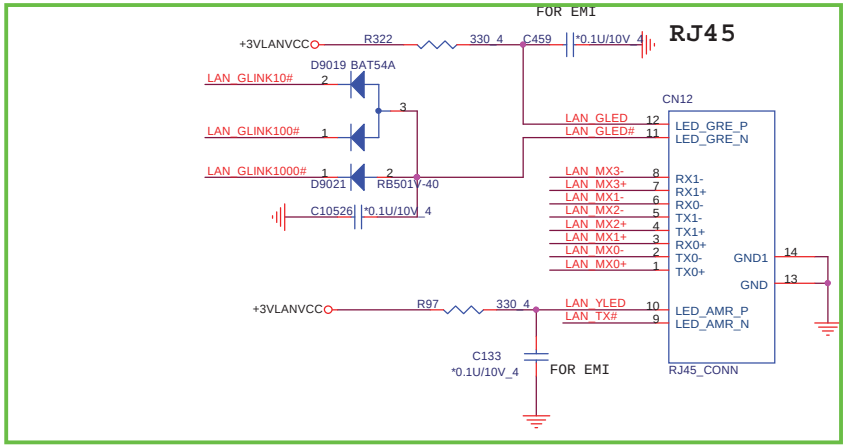
Transformer for 10/100/1000



modify SI

Lan Con.

modify DB2



43 +3VLANVCC
2,3,5,6,7,10,11,12,13,14,15,16,20,23,25,27,29,30,31,32,33,34,35,37,43 +3V

NB5/RD2	PROJECT : SX7 Quanta Computer Inc.	
Size: Custom	Document Number: LAN RTL8151/RJ45	Rev: 3A
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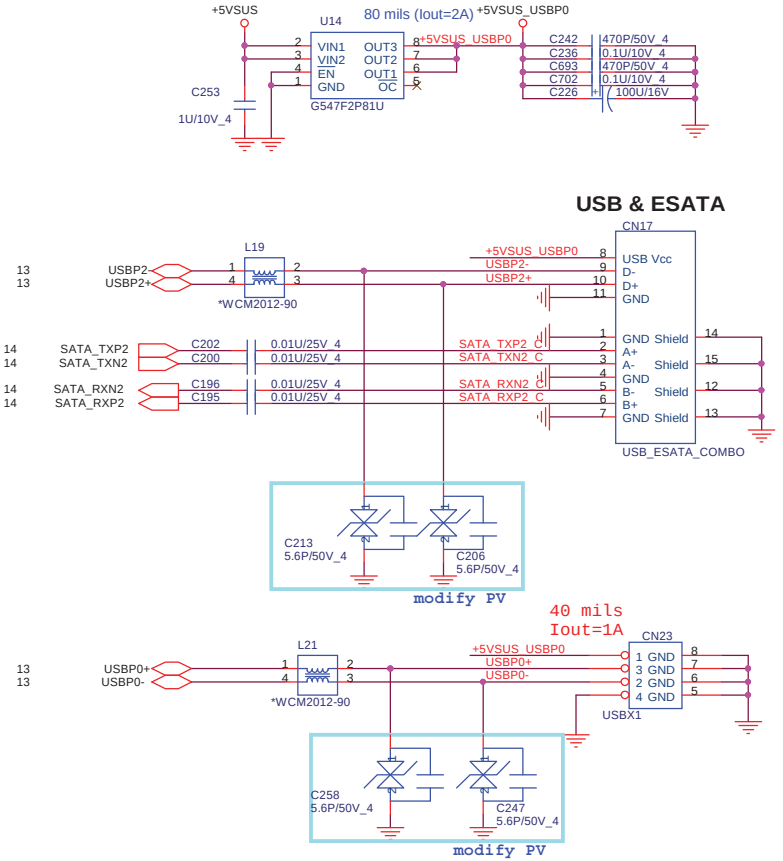
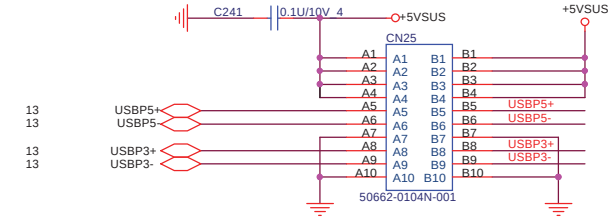
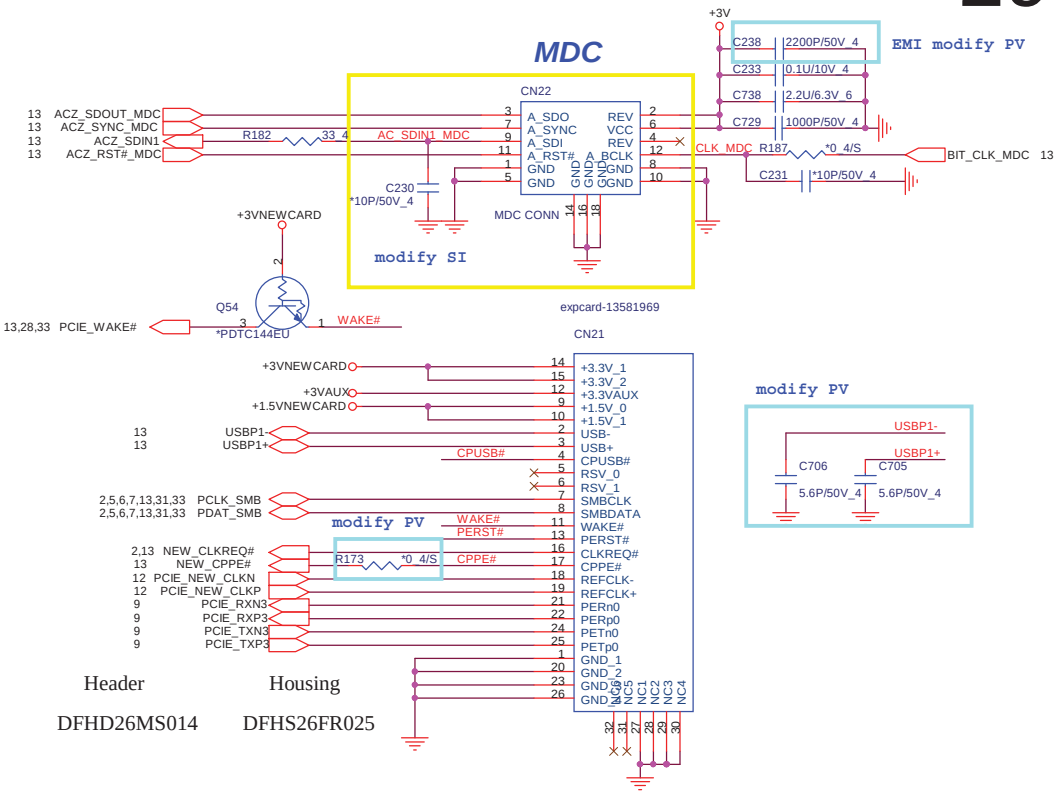
LEFT SIDE USBX1 and E-SATA/USB COMBO



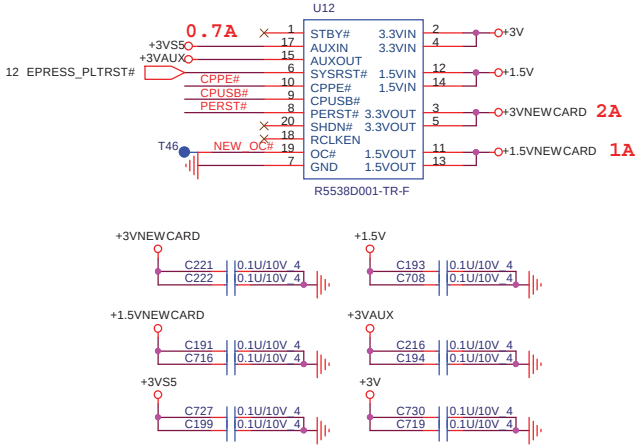
RIGHT SIDE USBX2



Modem CONN



NEWCARD (PCIEXPRESS*1 + USB*1)



NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EXTERNAL USB X2	3A
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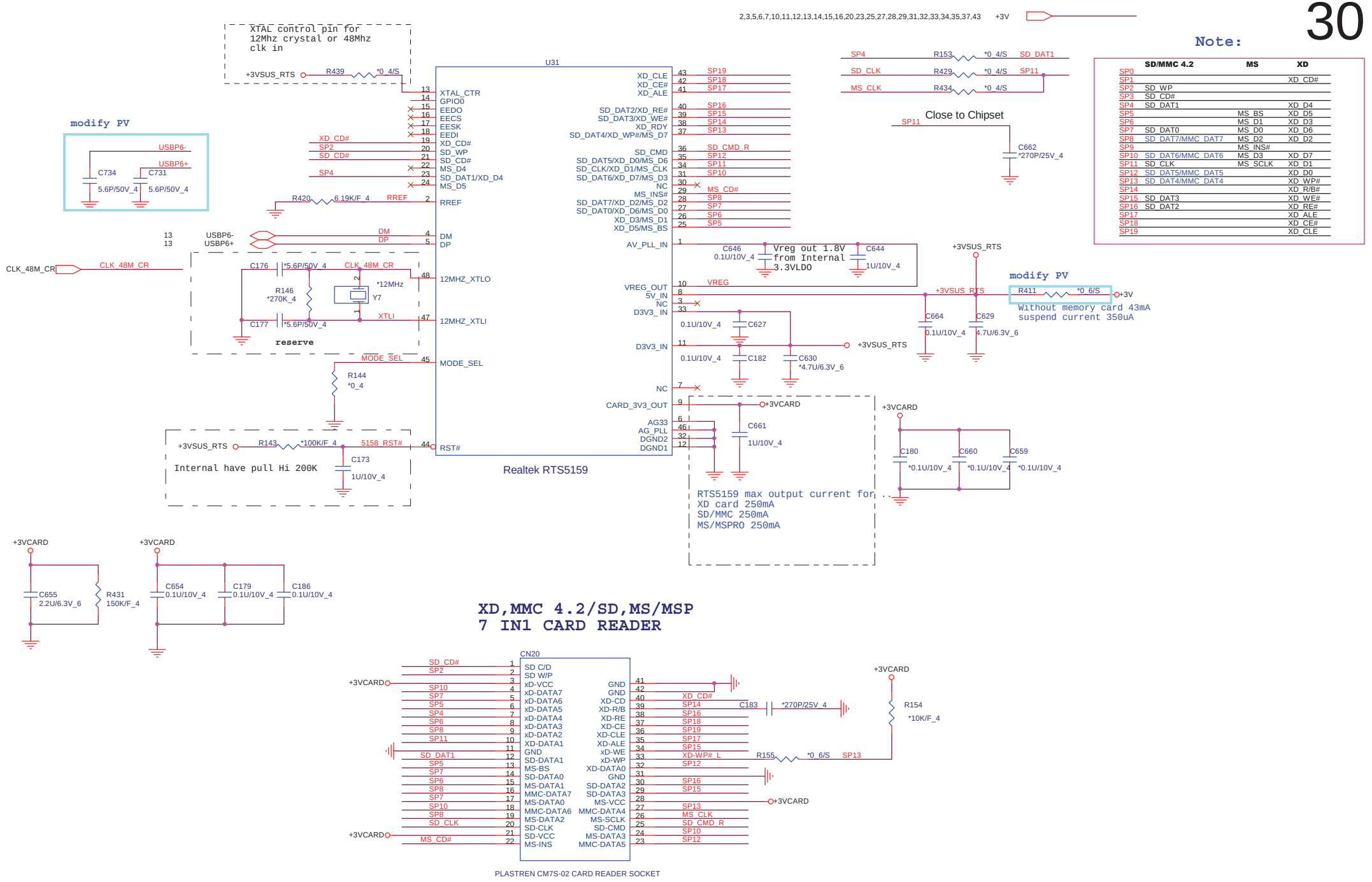
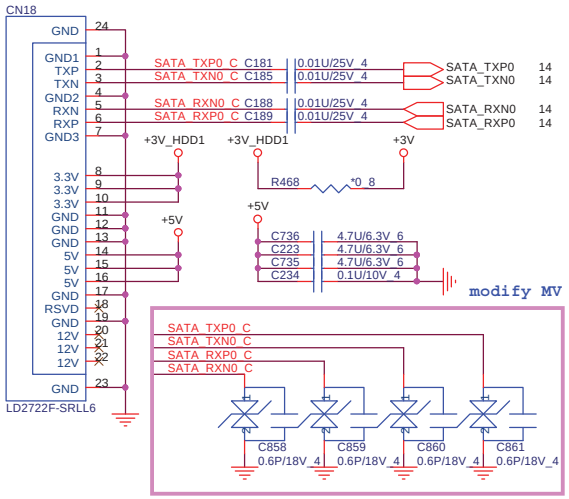
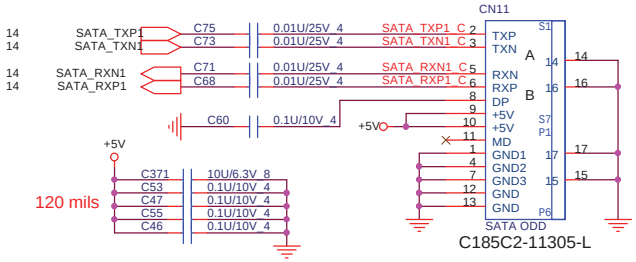


NB5/RD2	PROJECT : SX7 Quanta Computer Inc.	
Size: Custom	Document Number: RTS5159 & CR SOCKET	Rev: 3A
Date: Monday, March 15, 2010	Sheet 30 of 43	

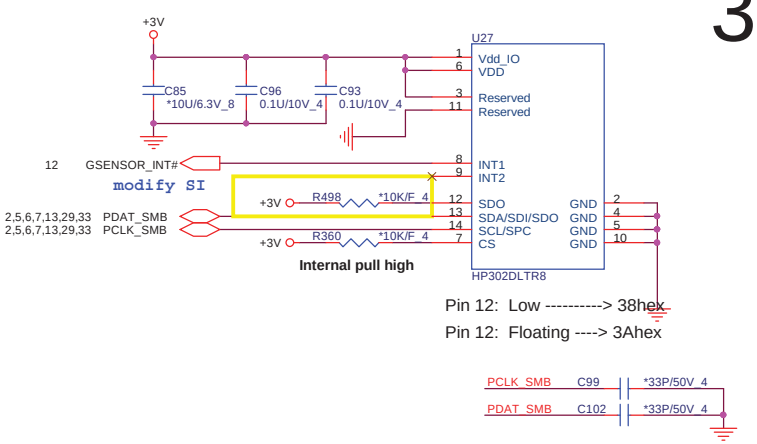
SATA HDD CONNECTOR



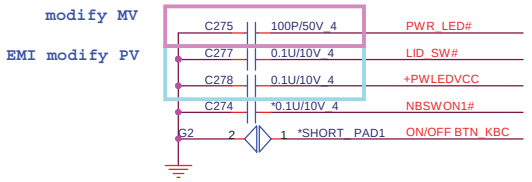
SATA CD-ROM



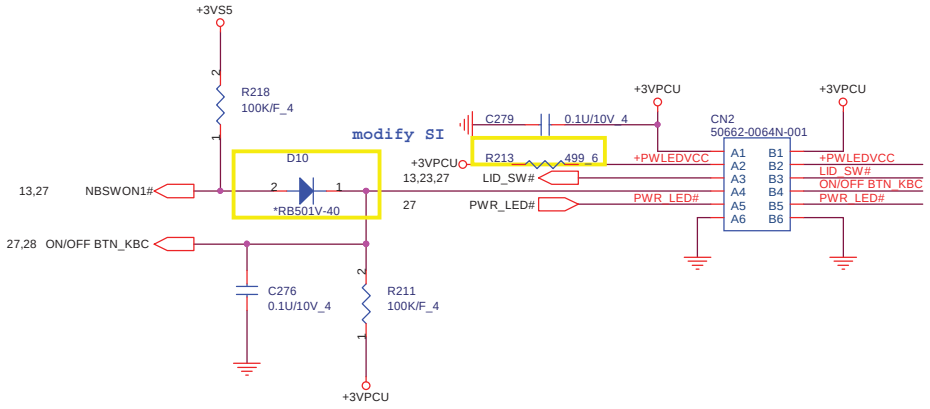
Accelerometer Sensor



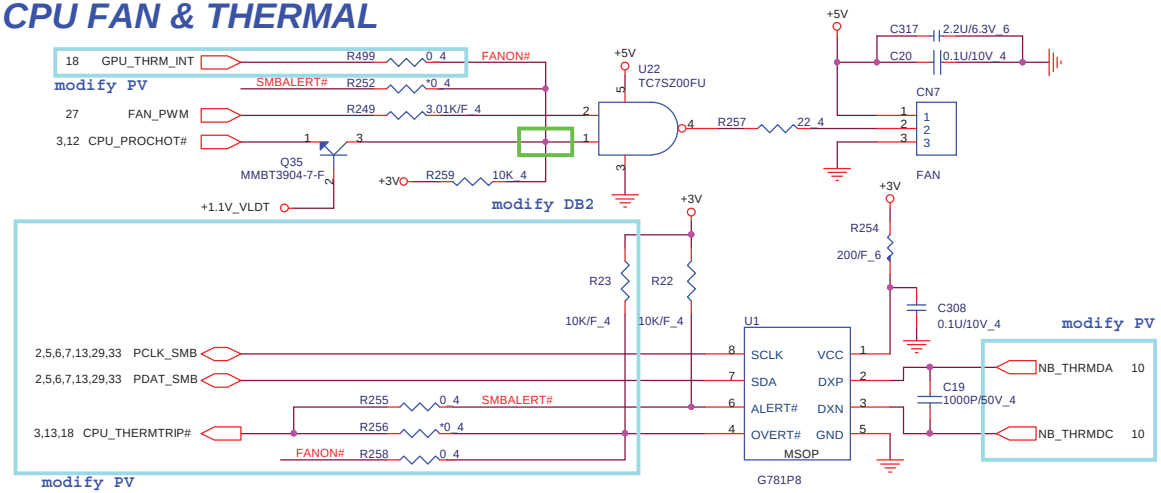
POWER BOTTON CONNECT



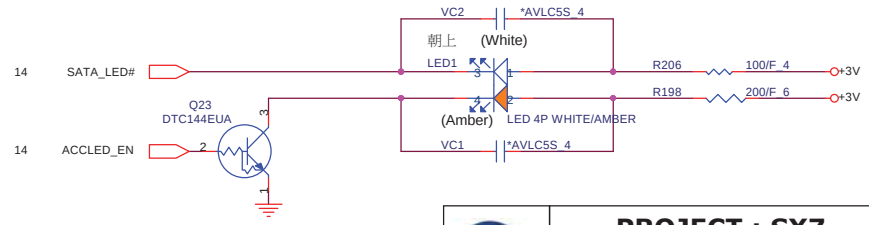
1. +3VPCU(LIDSWITCH PWR)
2. +PWLEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND



CPU FAN & THERMAL



LED



NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ESATA/HDD/ODD/LED/FAN	3A
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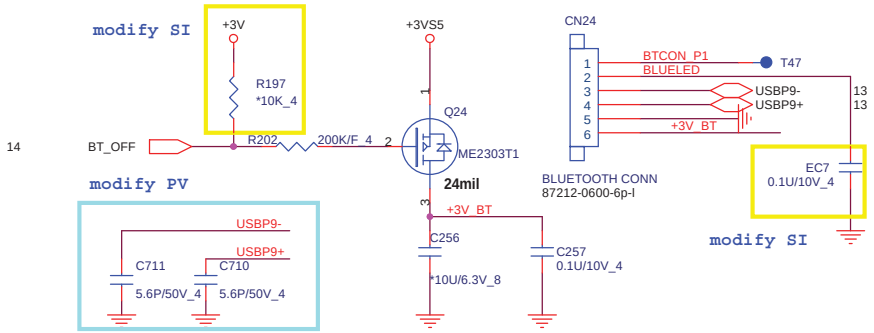
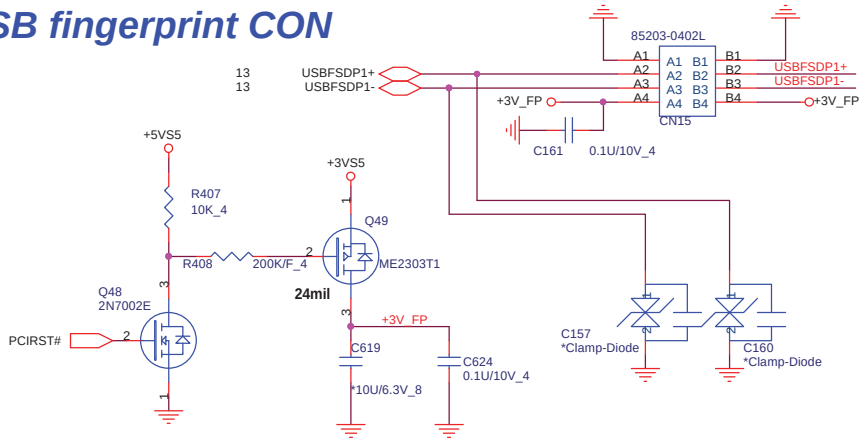
BLUETOOTH

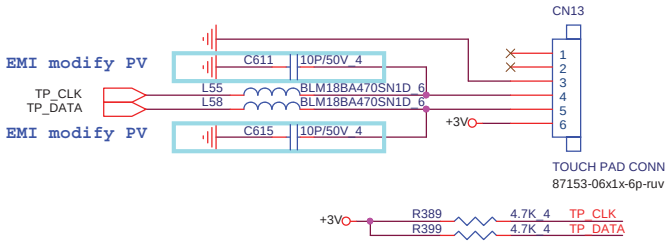


USB fingerprint CON

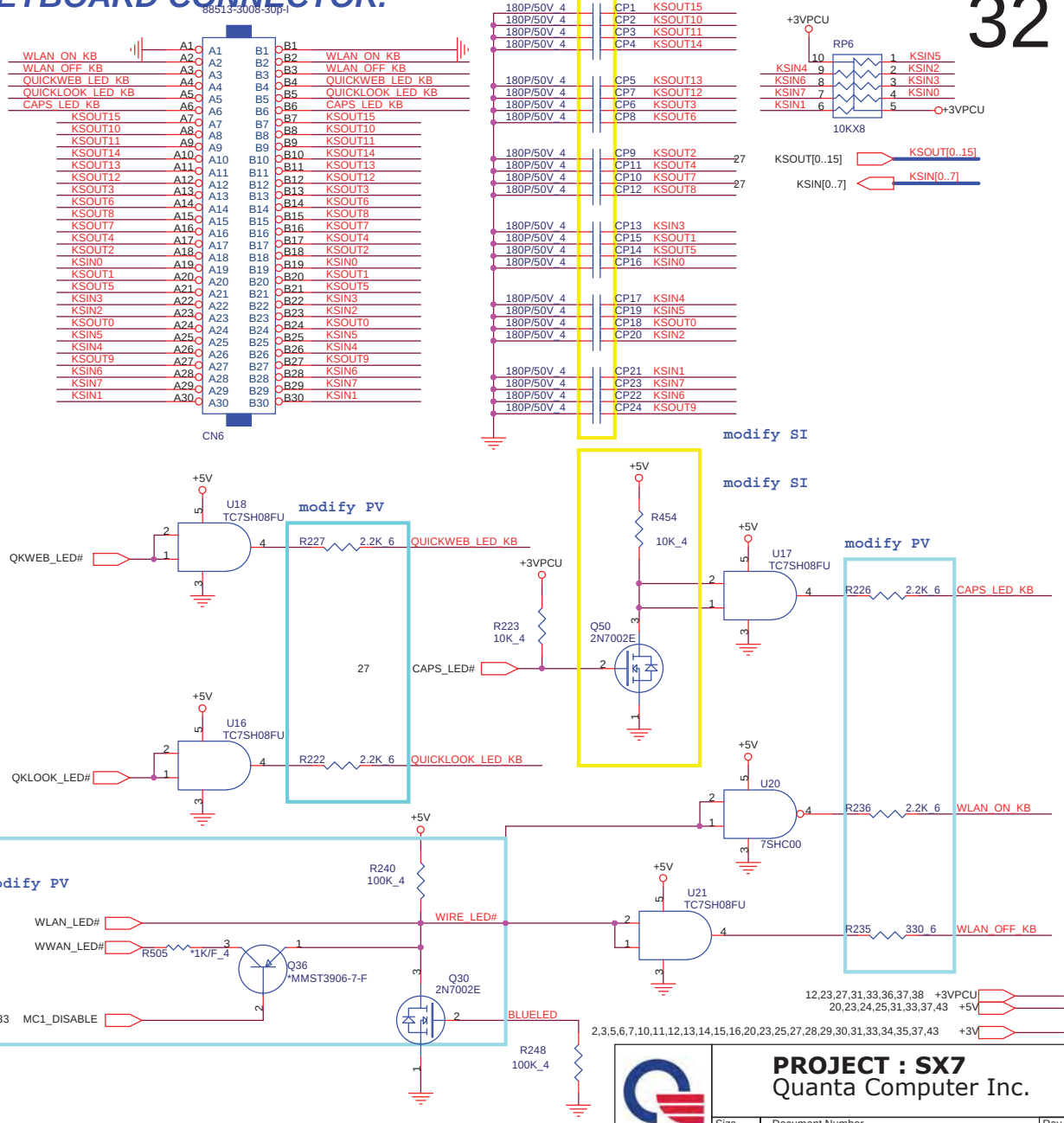


TOUCH PAD CONNECTOR

Pin1	VDD
Pin2	DATA
Pin3	CLK
Pin4	GND
Pin5	X
Pin6	X



KEYBOARD CONNECTOR.



NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/WC/FT/ESATA/USB/LED	3A

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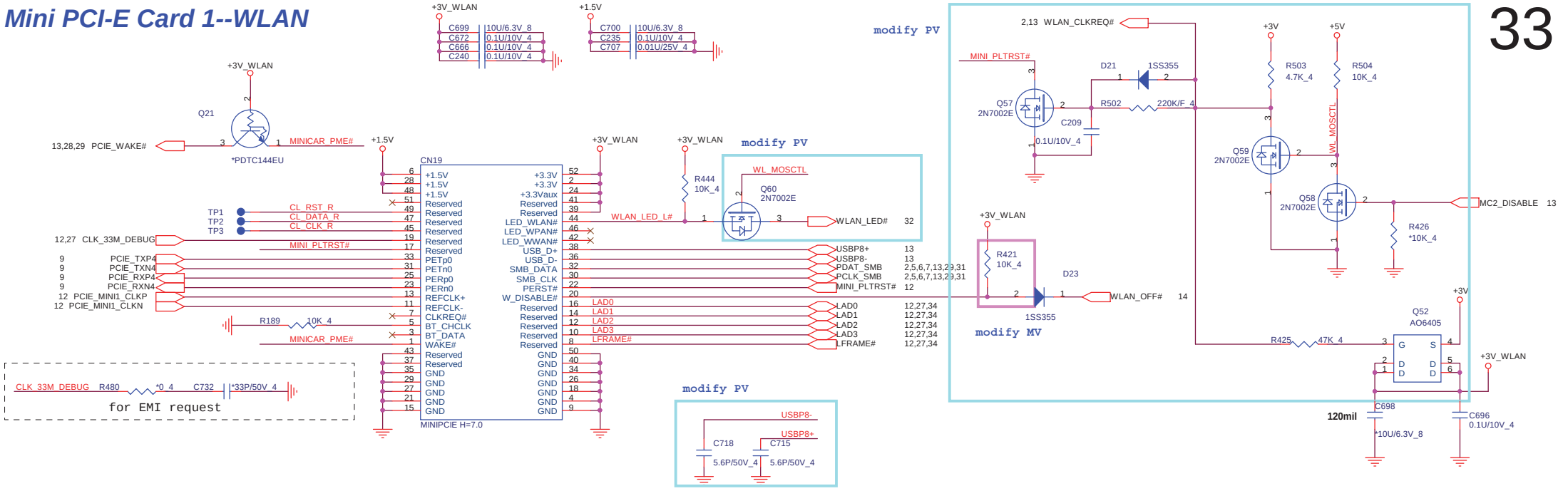
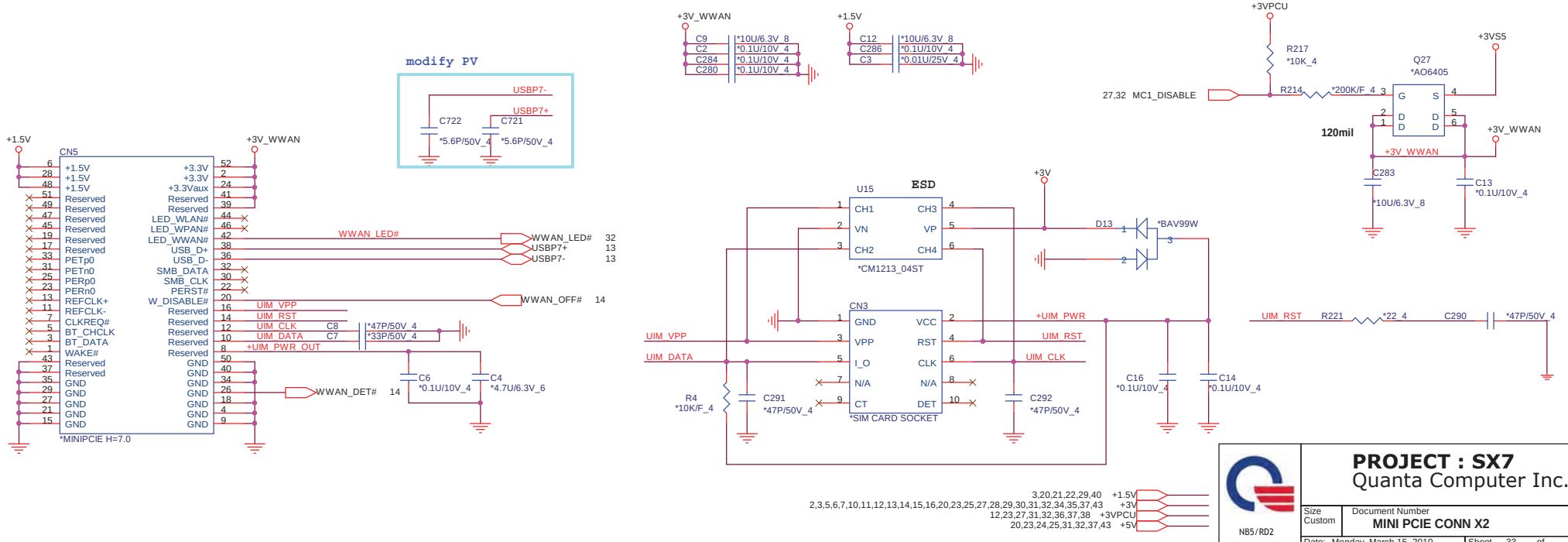
Mini PCI-E Card 1--WLAN



Mini PCI-E Card 2 --WWAN



PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN X2	3A
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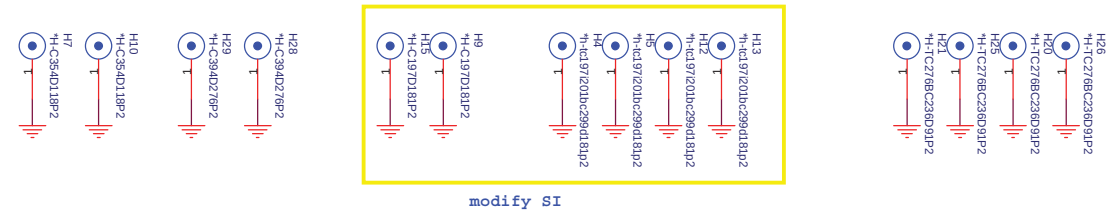
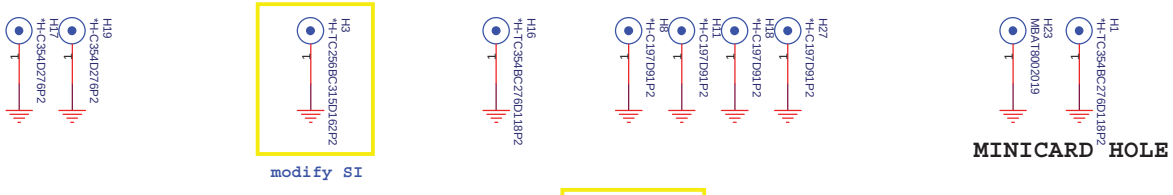
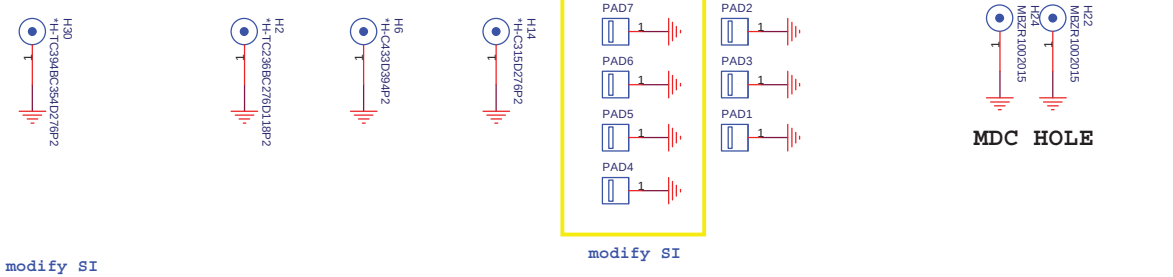
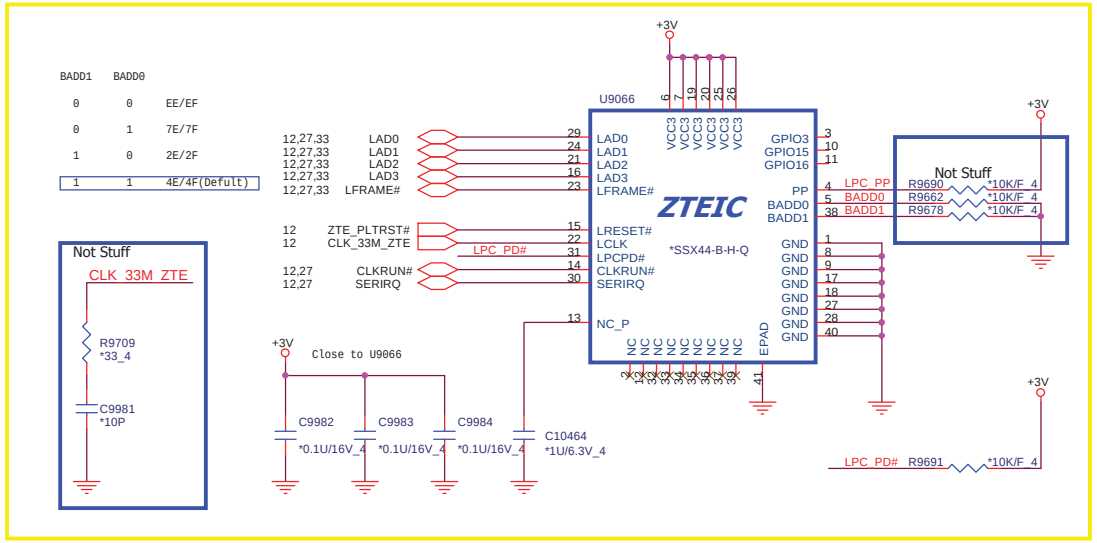
NB5/RD2









PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hole, Nuts	3A
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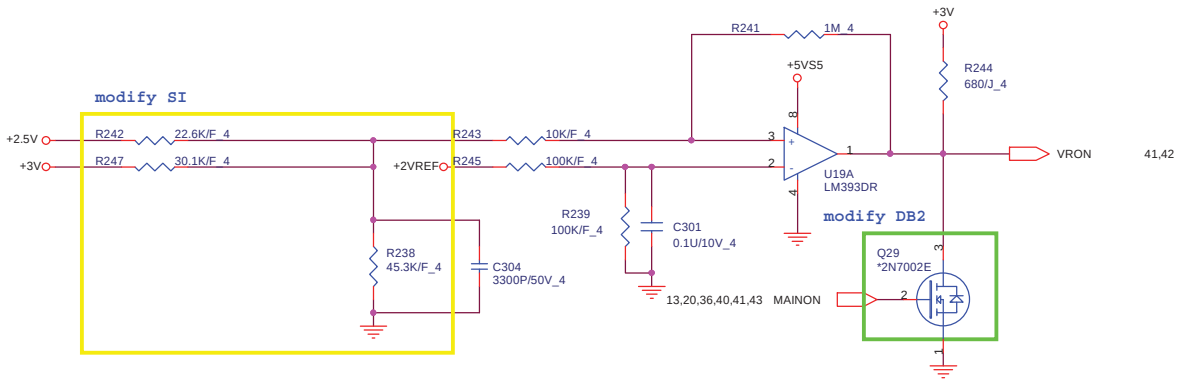
NB5/RD2



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NB5/RD2	Size: Custom Document Number: **POWER Sequance**	Rev: 3A
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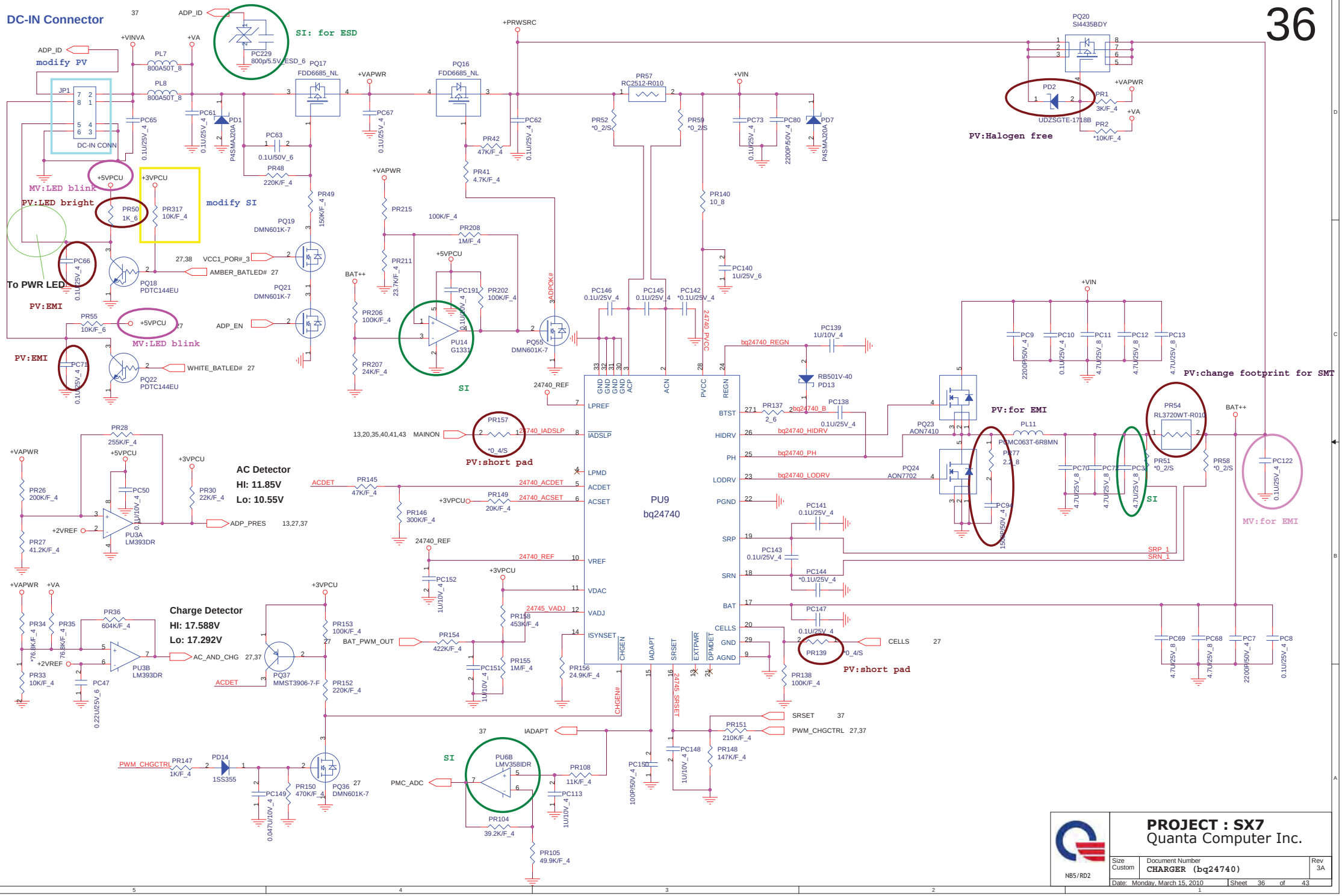
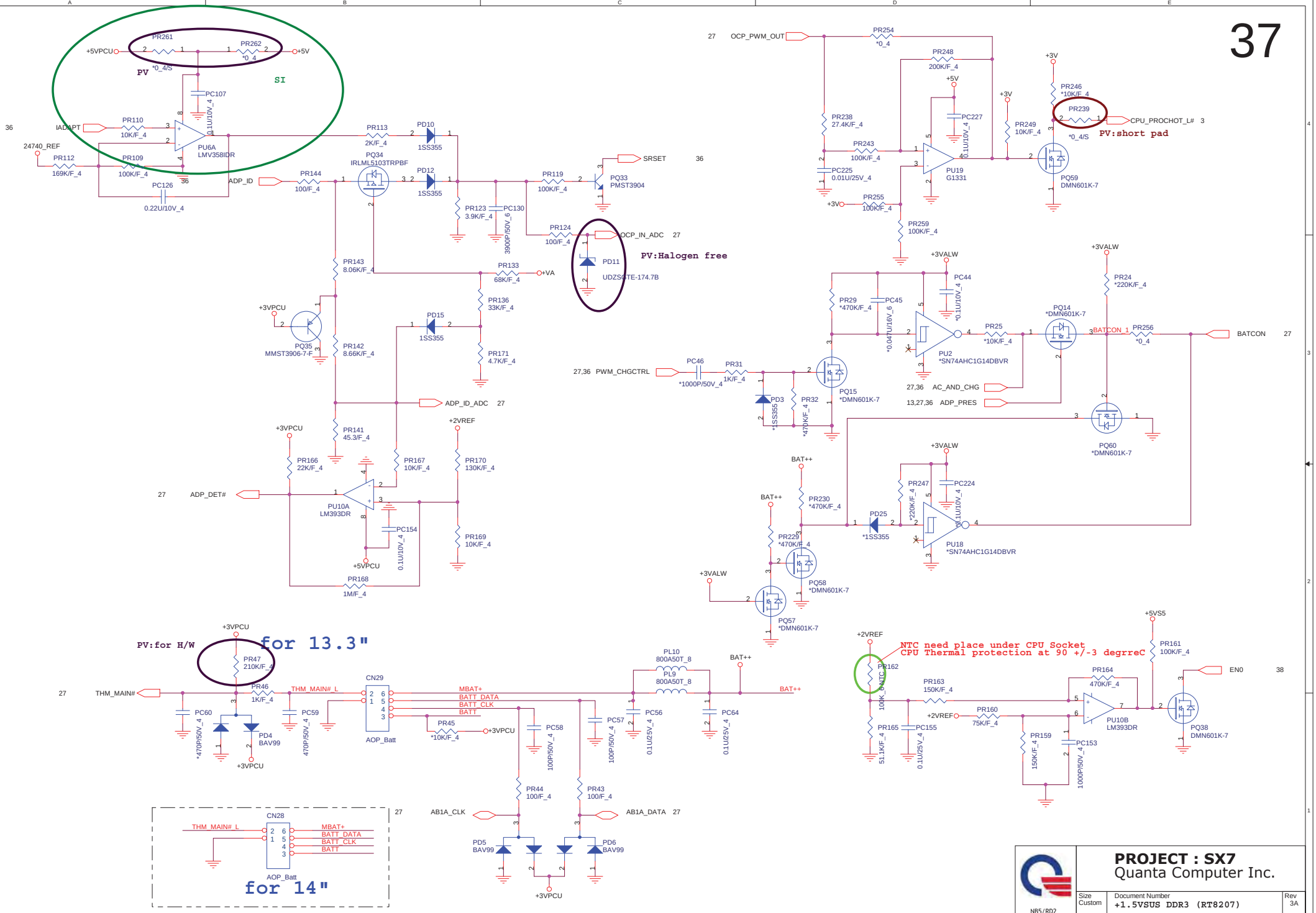

DC-IN Connector
SI: for ESD
modify PV
MV:LED blink
PV:LED bright
modify SI
To PWR LED
PV:EMI
PV:short pad
AC Detector
HI: 11.85V
Lo: 10.55V
Charge Detector
HI: 17.588V
Lo: 17.292V
PU9
bq24740
PV:Halogen free
PV:for EMI
PV:change footprint for SMT
MV:for EMI
SI
PROJECT : SX7
Quanta Computer Inc.
CHARGER (bq24740)
Monday, March 15, 2010
NB5/RD2



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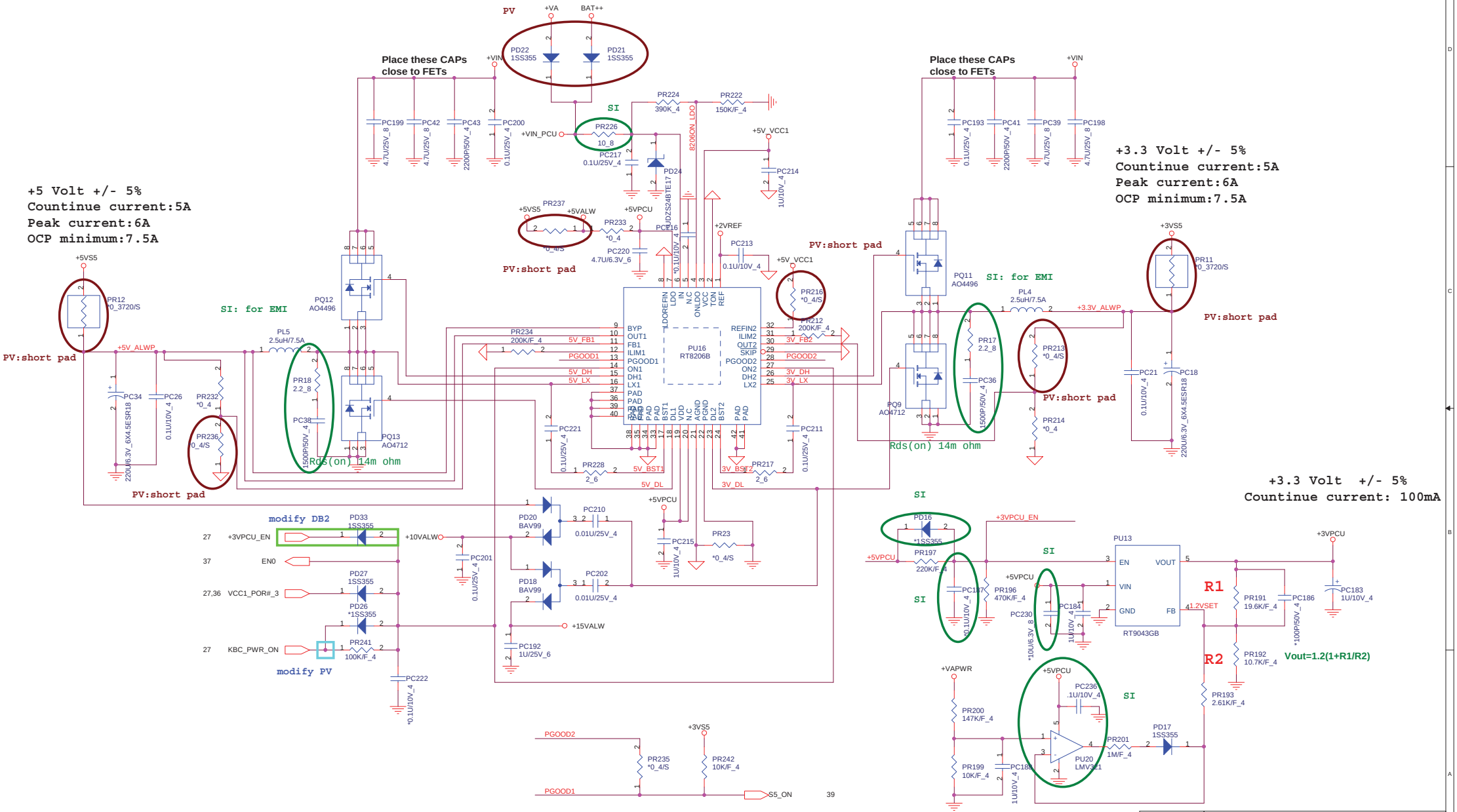
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

+5 Volt +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current: 100mA



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Quanta Computer Inc.

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Custom	+5V/+3V (RT8206B)	3A
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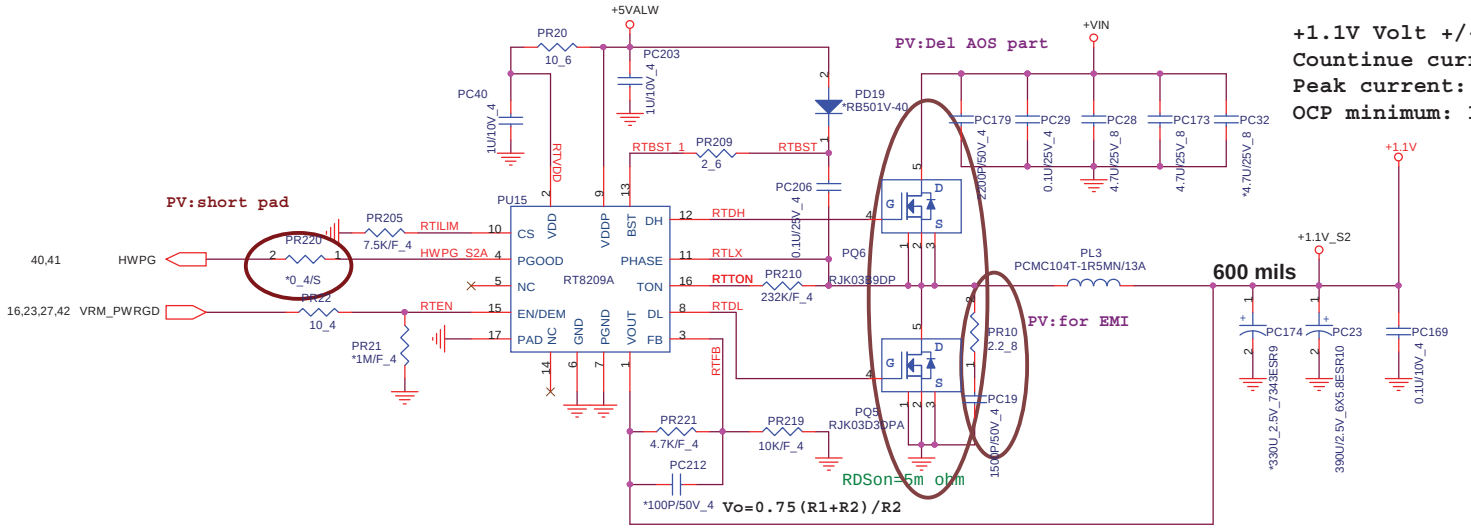
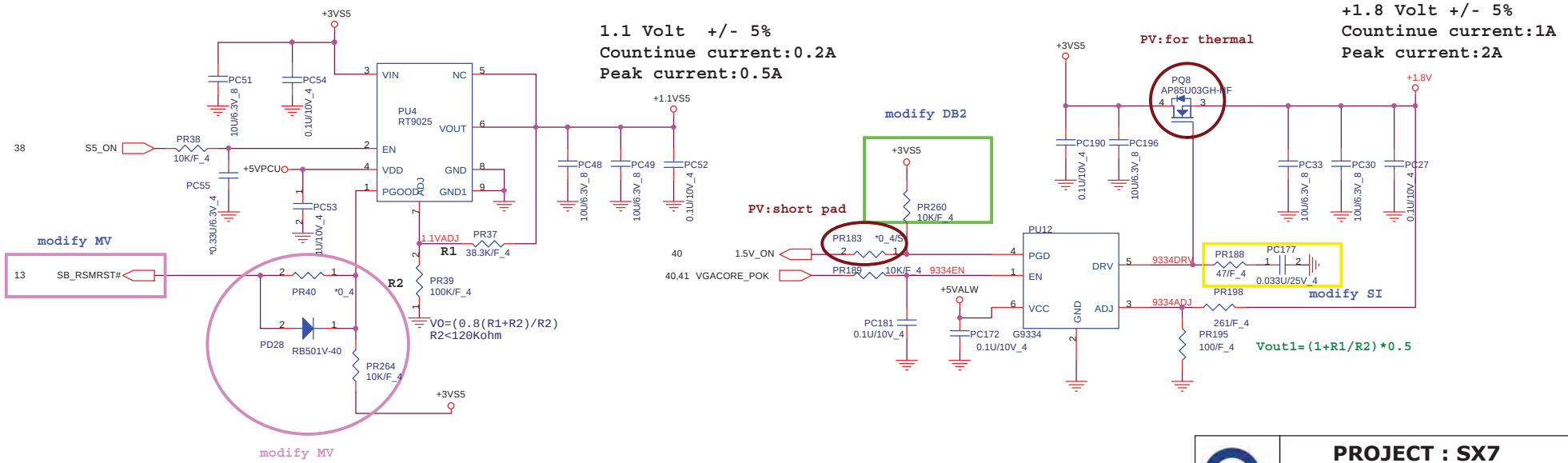
NB5/RD2





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Quanta Computer Inc.

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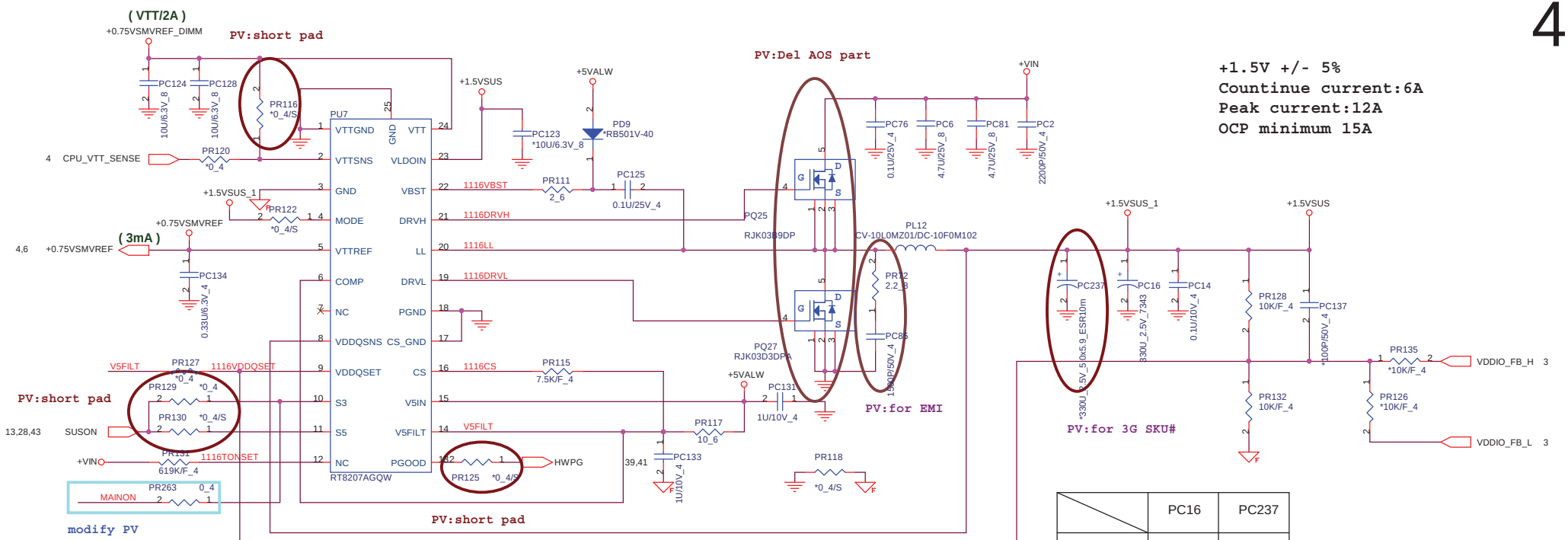
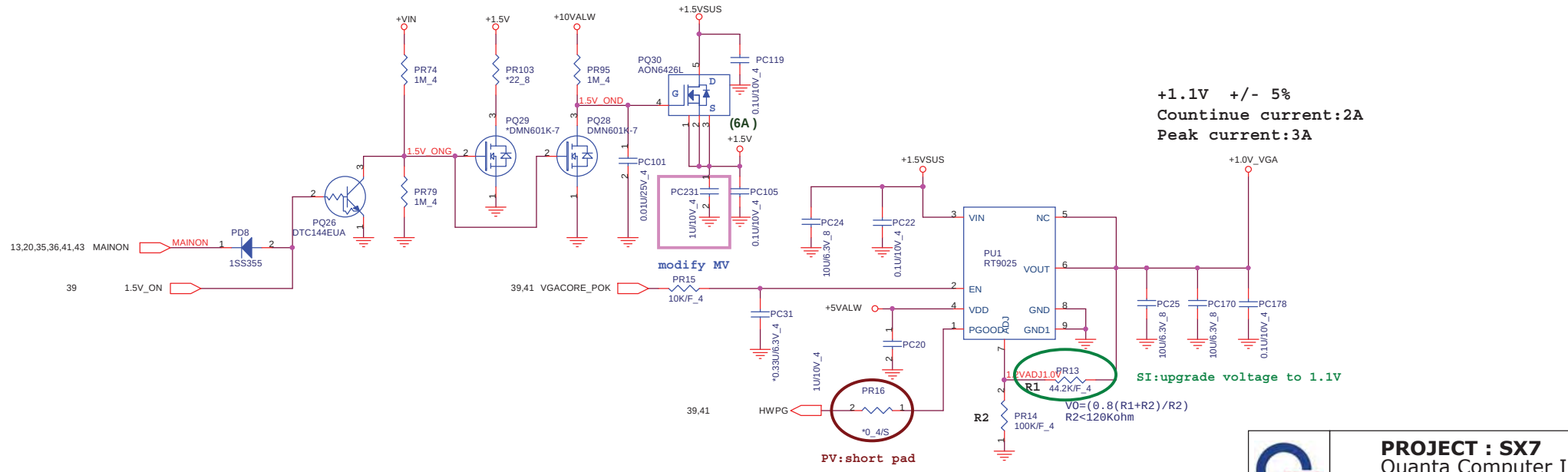
NB5/RD2



	PC16	PC237
For 3G sku	Stuff	NC
non 3G sku	NC	Stuff



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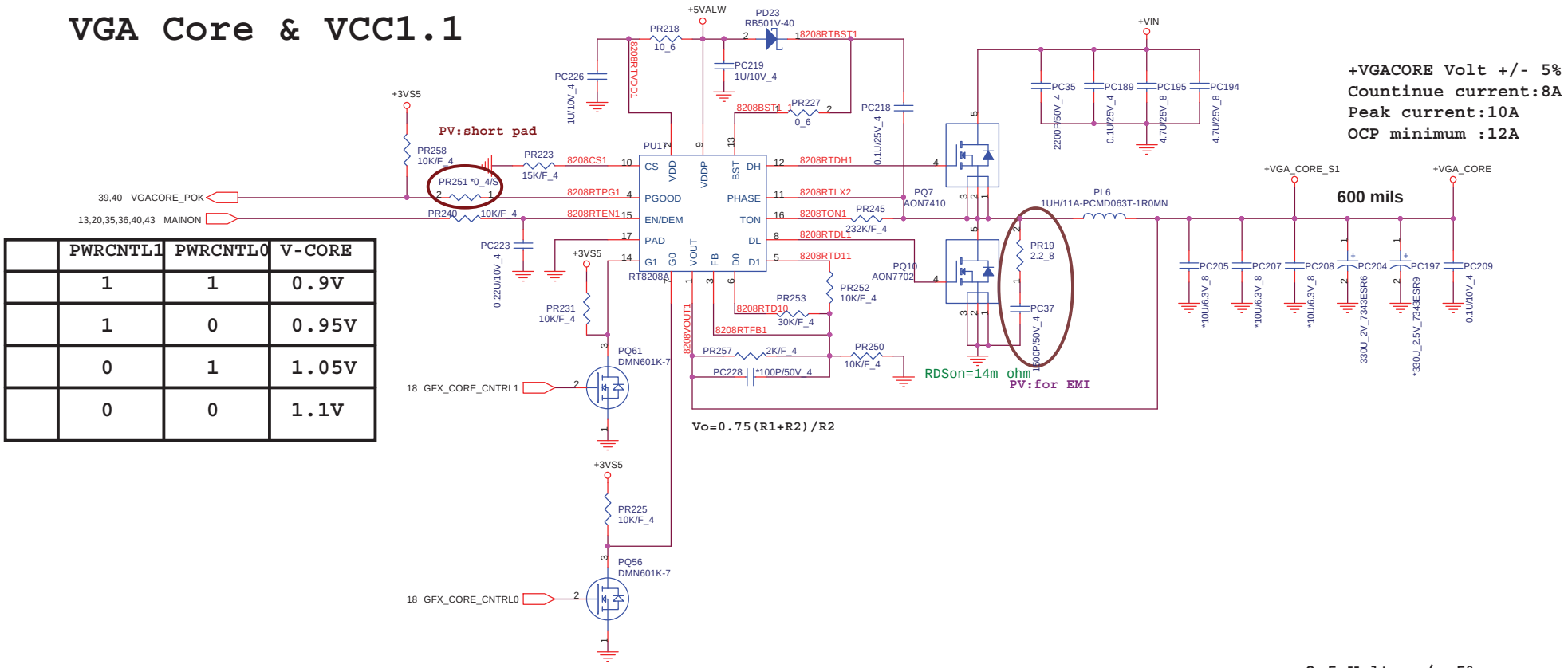
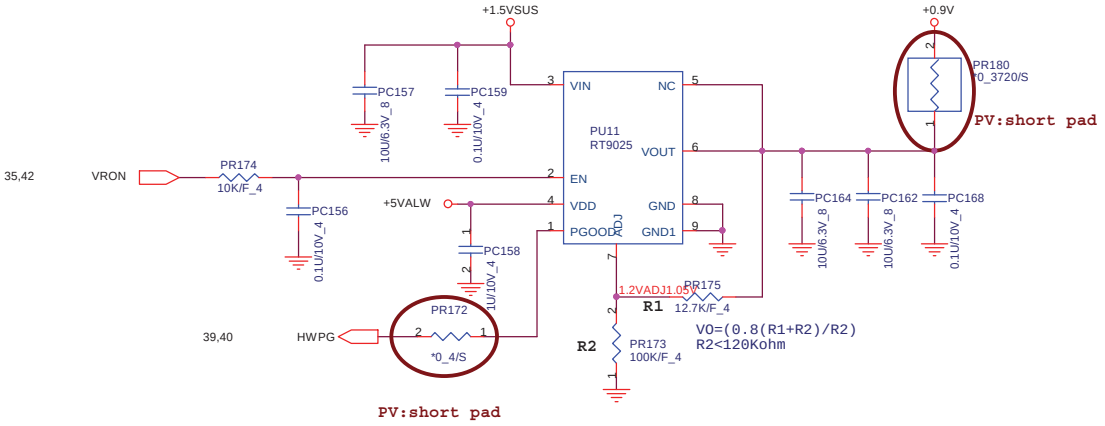
VGA Core & VCC1.1

	PWRCNTL1	PWRCNTL0	V-CORE
	1	1	0.9V
	1	0	0.95V
	0	1	1.05V
	0	0	1.1V

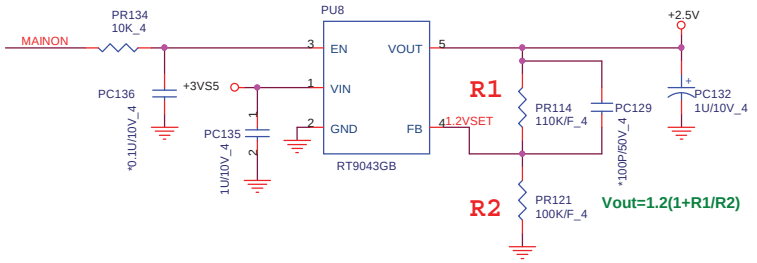


+VGACORE Volt +/- 5%
Countinue current:8A
Peak current:10A
OCP minimum :12A

+0.9V +/- 5%
Countinue current:1.5A
Peak current:2A



+2.5 Volt +/- 5%
Countinue current: 200mA
Peak current: 600mA



NB5/RD2

PROJECT : SX7
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Custom	VGA Core/+1.8VGFX/1.0VGFX	3A

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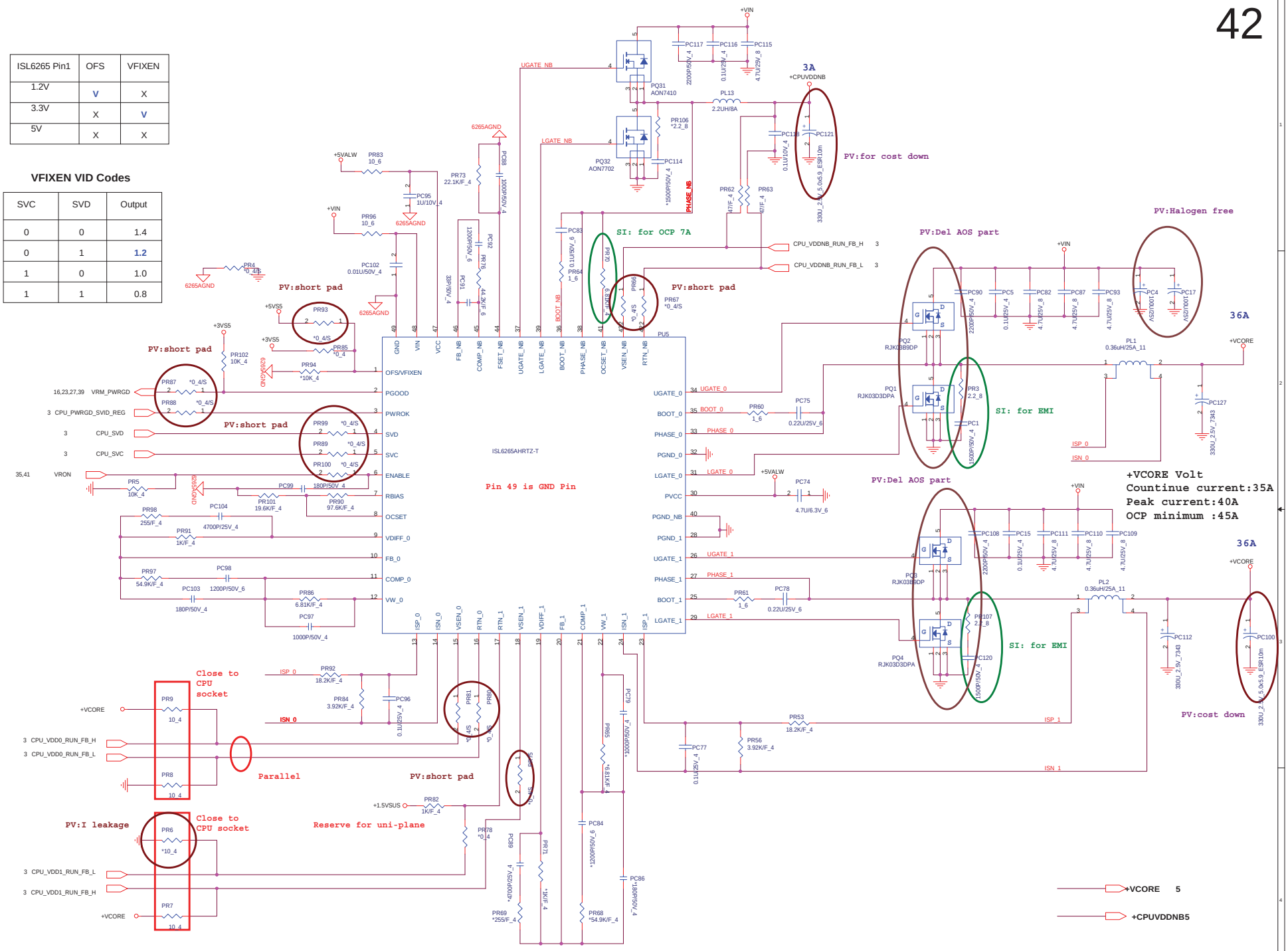
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



NB5/RD2	**PROJECT : SX7** Quanta Computer Inc.	
Size C	Document Number CPU_CORE(ISL6265)	Rev 3A
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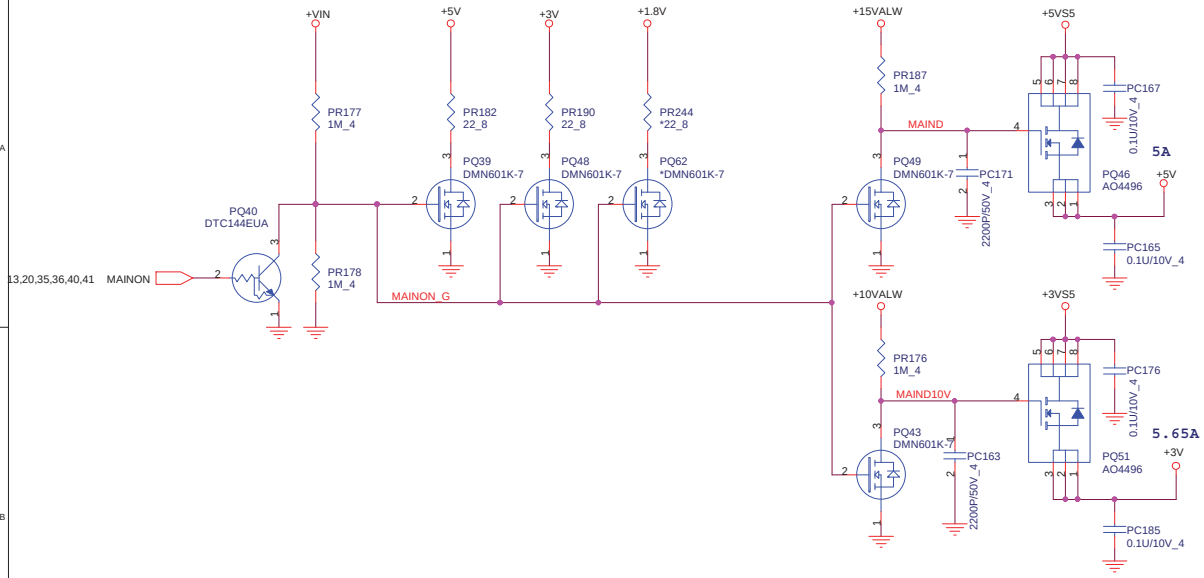

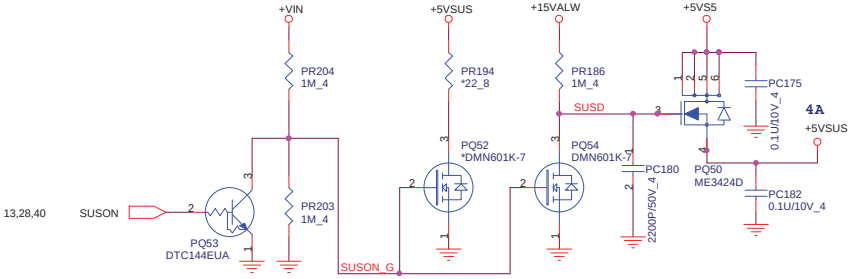

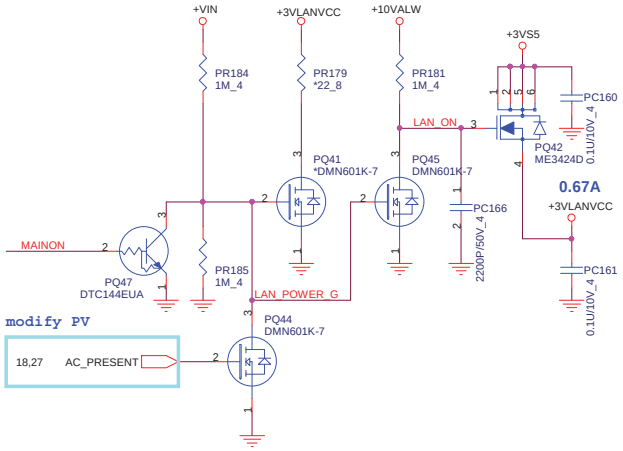

NB5/RD2	**PROJECT : SX7** Quanta Computer Inc.	
Size: Custom	Document Number: **DISCHARGE/3VS5/5VS5/LAN**	Rev: 3A
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