Wistron Confidential

PV1

2009/12/28 REV :PV-01

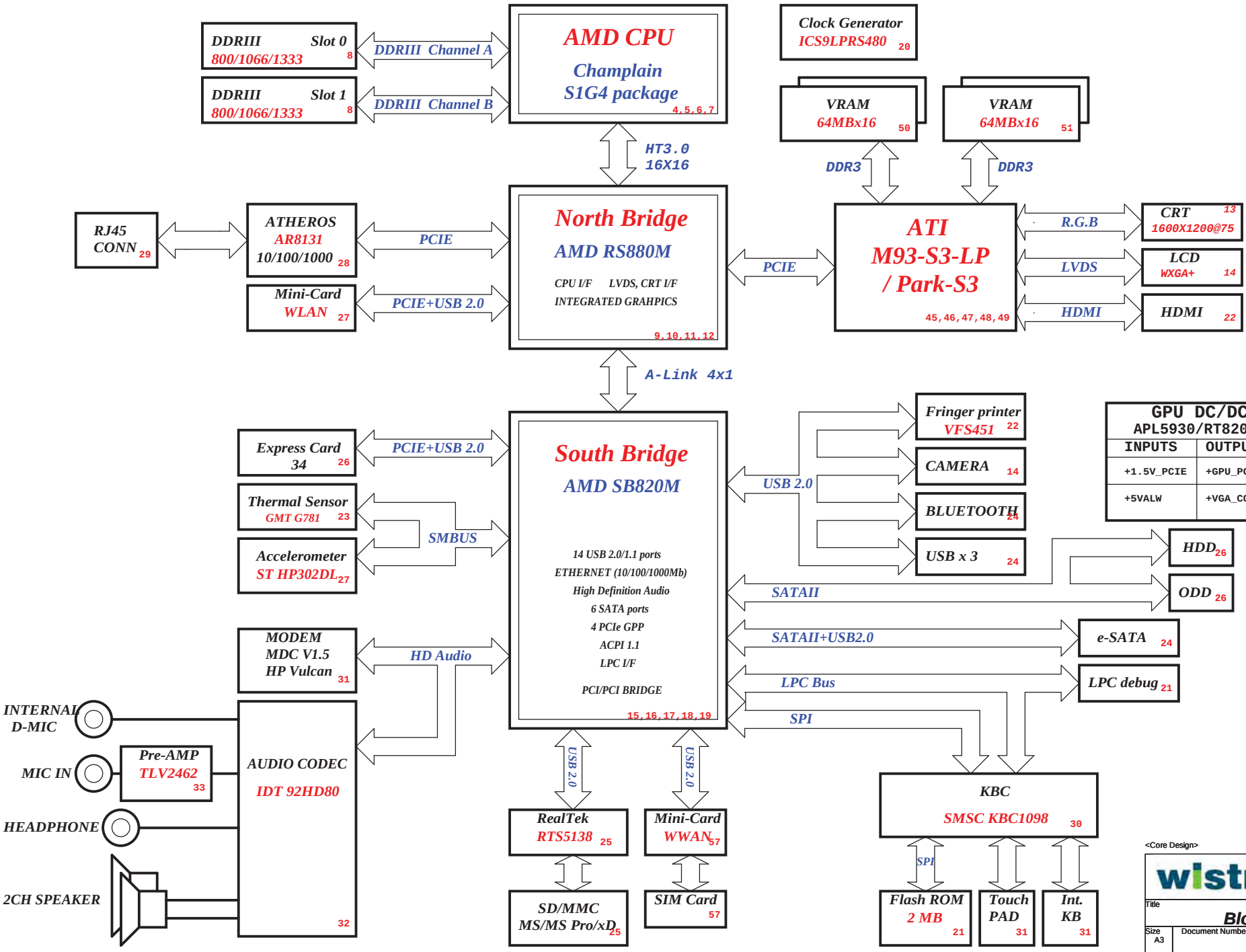
<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: *Cover*		
Size: A3	Document Number: PATEK	Rev: SA
Date: Monday, March 15, 2010	Sheet 1 of 57	

Patek DIS Block Diagram



SYSTEM DC/DC RT8205A

INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VL +3VALW +3VL 39

SYSTEM DC/DC RT8209B

INPUTS	OUTPUTS
+5VALW	+1.1VALW 41

SYSTEM DC/DC G972

INPUTS	OUTPUTS
+3VS	+1.8VS 38

SYSTEM DC/DC G9091/RT9205

INPUTS	OUTPUTS
+3VS	+2.5VS_LDO_CPU
+1.5VS	+1.05VS 37

SYSTEM DC/DC RT8207

INPUTS	OUTPUTS
+5VALW	+1.5V +0.75V 40

GPU DC/DC APL5930/RT8209B

INPUTS	OUTPUTS
+1.5V_PCIE	+GPU_PCIE 38
+5VALW	+VGA_CORE 52

MAXIM CHARGER BQ24740

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 42

CPU DC/DC ISL6265/RT8209B

INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE +VDDNB 36
+5VALW	+NB_VDDC 54

PCB 6 LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Block Diagram

Size	Document Number	Rev
A3	PATEK	SA

Date: Monday, March 15, 2010 Sheet 2 of 57

RS880M strapping

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.(PIN: RS880M--> VSYNC)
0 : Enable * 1 : Disable

RS880: Enables Side port memory (RS880 use HSYNC)

0 : Enable * 1 : Disable

SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected

PCIE routing

Page 9

LANE 0	LAN
LANE 3	NEW CARD
LANE 4	WLAN

USB table

Page 18

Pair	Device
USB-FSD1 FPR	
USB-9 Bluetooth	
USB-8 WLAN	
USB-7 WWAN	
USB-6 USB Card Reader	
USB-5 Right Side	
USB-4 USB Camera	
USB-3 Right Side	
USB-2 Left Side (e-SATA combo)	
USB-1 New Card	
USB-0 Left Side (S/W Debug port)	

SB820M strapping

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK_KBC (LPCCLK0)	LPC_CLK_DB (LPCCLK1)	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	L, H = LPC ROM L, L = FWH ROM

SMBUS Control Table

	SOURCE	BATT	THERMAL SENSOR	CLK GEN	SODIMM	G-SENSOR	SMSC1098	SB-TSI
AB1A_DATA AB1A_CLK	SMSC1098	V	X	X	X	X	X	X
SB_SMB_CLK1 SB_SMB_DAT1	SB820M	X	X	X	X	X	X	X
SB_SMB_CLK0 SB_SMB_DAT0	SB820M	X	V	V	V	V	X	X
CPU_SIC_SB700 CPU_SID_SB700	CPU	X	X	X	X	X	X	V

<Core Design>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: NOTES

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 3 of 57

HT

CPU VLDT MAX 1.5A

LAYOUT: PLACE CLOSE TO CPU
ALONG HT POWER SHAPE

+1.1VS

C1 SCD22U25V3KX-GP
C2 SCD22U25V3KX-GP
C3 SC180P50V2JN-1GP
C4 SC180P50V2JN-1GP

091221-1
6 HDT_RST#
R3 0R0402-PAD-1-GP
LDT_RST#_CPU
LDT_PWROK
CPU_LDT_STOP#

CPU1A
SEC 1 OF 6
LDT

D1 V_HT_A1
D2 V_HT_A2
D3 V_HT_A3
D4 V_HT_A4

B7 RESET*
A7 PWROK
F10 LDTSTOP*

DY
C7 SC4D7U25V5KX-GP
C5 SC4D7U25V5KX-GP
C6 SC4D7U25V5KX-GP
091215-1

V_HT_B1 AE2
V_HT_B2 AE3
V_HT_B3 AE4
V_HT_B4 AE5

LDTREQ* C6 — LDT_REQ#

9 NB0CADOUT[15..0]
9 NB0CADOUTJ[15..0]

CPUCADOUT[15..0] 9
CPUCADOUTJ[15..0] 9

NB0CADOUT15	N5	HT_RXD_P15	HT_TXD_P15 T4 CPUCADOUT15
NB0CADOUT14	M3	HT_RXD_P14	HT_TXD_P14 V5 CPUCADOUT14
NB0CADOUT13	L5	HT_RXD_P13	HT_TXD_P13 V4 CPUCADOUT13
NB0CADOUT12	K3	HT_RXD_P12	HT_TXD_P12 Y5 CPUCADOUT12
NB0CADOUT11	H3	HT_RXD_P11	HT_TXD_P11 AB5 CPUCADOUT11
NB0CADOUT10	G5	HT_RXD_P10	HT_TXD_P10 AB4 CPUCADOUT10
NB0CADOUT9	F3	HT_RXD_P9	HT_TXD_P9 AD5 CPUCADOUT9
NB0CADOUT8	E5	HT_RXD_P8	HT_TXD_P8 AD4 CPUCADOUT8
NB0CADOUT7	N3	HT_RXD_P7	HT_TXD_P7 T1 CPUCADOUT7
NB0CADOUT6	L1	HT_RXD_P6	HT_TXD_P6 U2 CPUCADOUT6
NB0CADOUT5	L3	HT_RXD_P5	HT_TXD_P5 V1 CPUCADOUT5
NB0CADOUT4	J1	HT_RXD_P4	HT_TXD_P4 W2 CPUCADOUT4
NB0CADOUT3	G1	HT_RXD_P3	HT_TXD_P3 AA2 CPUCADOUT3
NB0CADOUT2	G3	HT_RXD_P2	HT_TXD_P2 AB1 CPUCADOUT2
NB0CADOUT1	E1	HT_RXD_P1	HT_TXD_P1 AC2 CPUCADOUT1
NB0CADOUT0	E3	HT_RXD_P0	HT_TXD_P0 AD1 CPUCADOUT0
NB0CADOUTJ15	P5	HT_RXD_N15	HT_TXD_N15 T3 CPUCADOUTJ15
NB0CADOUTJ14	M4	HT_RXD_N14	HT_TXD_N14 U5 CPUCADOUTJ14
NB0CADOUTJ13	M5	HT_RXD_N13	HT_TXD_N13 V3 CPUCADOUTJ13
NB0CADOUTJ12	K4	HT_RXD_N12	HT_TXD_N12 W5 CPUCADOUTJ12
NB0CADOUTJ11	H4	HT_RXD_N11	HT_TXD_N11 AA5 CPUCADOUTJ11
NB0CADOUTJ10	H5	HT_RXD_N10	HT_TXD_N10 AB3 CPUCADOUTJ10
NB0CADOUTJ9	F4	HT_RXD_N9	HT_TXD_N9 AC5 CPUCADOUTJ9
NB0CADOUTJ8	E5	HT_RXD_N8	HT_TXD_N8 AD3 CPUCADOUTJ8
NB0CADOUTJ7	N2	HT_RXD_N7	HT_TXD_N7 R1 CPUCADOUTJ7
NB0CADOUTJ6	M1	HT_RXD_N6	HT_TXD_N6 U3 CPUCADOUTJ6
NB0CADOUTJ5	L2	HT_RXD_N5	HT_TXD_N5 U1 CPUCADOUTJ5
NB0CADOUTJ4	K1	HT_RXD_N4	HT_TXD_N4 W3 CPUCADOUTJ4
NB0CADOUTJ3	H1	HT_RXD_N3	HT_TXD_N3 AA3 CPUCADOUTJ3
NB0CADOUTJ2	G2	HT_RXD_N2	HT_TXD_N2 AA1 CPUCADOUTJ2
NB0CADOUTJ1	F1	HT_RXD_N1	HT_TXD_N1 AC3 CPUCADOUTJ1
NB0CADOUTJ0	E2	HT_RXD_N0	HT_TXD_N0 AC1 CPUCADOUTJ0

9 NB0HTTCLKOUT1	NB0HTTCLKOUT1	J5	HT_RXCLK_P1
9 NB0HTTCLKOUT0	NB0HTTCLKOUT0	J3	HT_RXCLK_P0
9 NB0HTTCLKOUTJ1	NB0HTTCLKOUTJ1	K5	HT_RXCLK_N1
9 NB0HTTCLKOUTJ0	NB0HTTCLKOUTJ0	J2	HT_RXCLK_N0
9 NB0HTTCTLOUT1	NB0HTTCTLOUT1	P3	HT_RXCTL_P1
9 NB0HTTCTLOUT0	NB0HTTCTLOUT0	N1	HT_RXCTL_P0
9 NB0HTTCTLOUTJ1	NB0HTTCTLOUTJ1	P4	HT_RXCTL_N1
9 NB0HTTCTLOUTJ0	NB0HTTCTLOUTJ0	P1	HT_RXCTL_N0

HT_TXCLK_P1	Y4	CPUHTTCLKOUT1
HT_TXCLK_P0	Y1	CPUHTTCLKOUT0
HT_TXCLK_N1	Y3	CPUHTTCLKOUTJ1
HT_TXCLK_N0	W1	CPUHTTCLKOUTJ0
HT_TXCTL_P1	T5	CPUHTTCTLOUT1
HT_TXCTL_P0	R2	CPUHTTCTLOUT0
HT_TXCTL_N1	R5	CPUHTTCTLOUTJ1
HT_TXCTL_N0	R3	CPUHTTCTLOUTJ0

CPUHTTCLKOUT1 9
CPUHTTCLKOUT0 9
CPUHTTCLKOUTJ1 9
CPUHTTCLKOUTJ0 9
CPUHTTCTLOUT1 9
CPUHTTCTLOUT0 9
CPUHTTCTLOUTJ1 9
CPUHTTCTLOUTJ0 9

HTREF1 P6
HTREF0 R6
L0_REF1
L0_REF0
R10 44D2R2F-GP
R11 44D2R2F-GP
+1.1VS
PLACE WITHIN 1"
5MIL TRACE
10MIL SPACE

DANUB

091222-1
+1.5VS
RN141 SRN300J-3-GP
LDT_PWROK
LDT_RST#_CPU
LDT_REQ#
R5 300R2J-4-GP
DY

S1G3 & S1G4 not support LDT_REQ#

091221-1
15 CPU_LDT_RST#
R6 0R0402-PAD-1-GP
LDT_RST#_CPU 10
15 CPU_PWRGD
R7 0R0402-PAD-1-GP
LDT_PWROK 36

+1.5VS
R2 300R2J-4-GP
091222-1
U155 74LVC1G07GW-GP
NC#1 VCC
A
GND Y
15 CPU_LDT_STOP#
+1.8VS
090817-1
R2283 2K2R2F-GP
C994 SCD1U16V2ZY-2GP
LDT_STP#_CPU 10

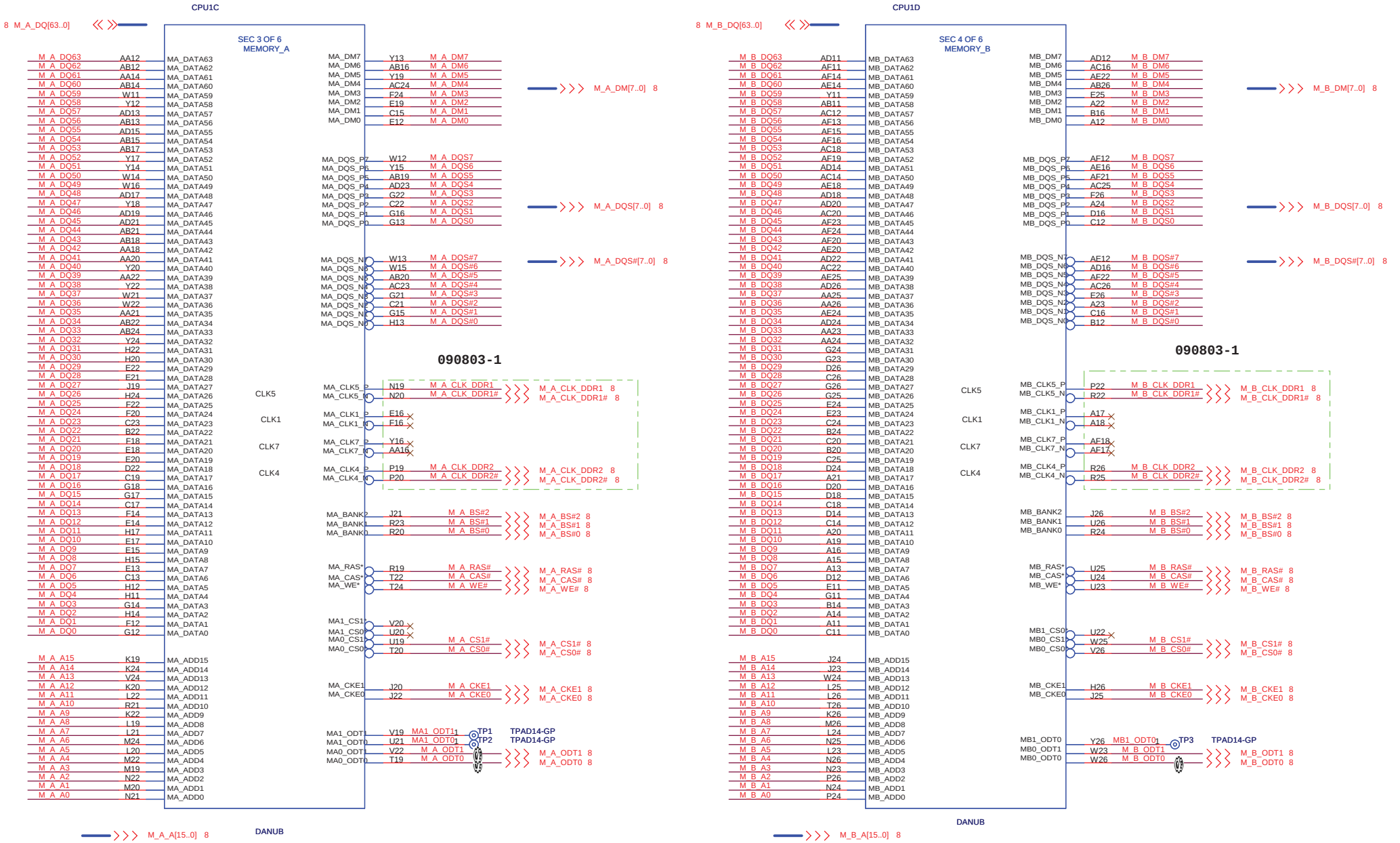
<Core Design>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU(1/4) HT

Size	Document Number	Rev
A3	PATEK	SA

Date: Monday, March 15, 2010 Sheet 4 of 57



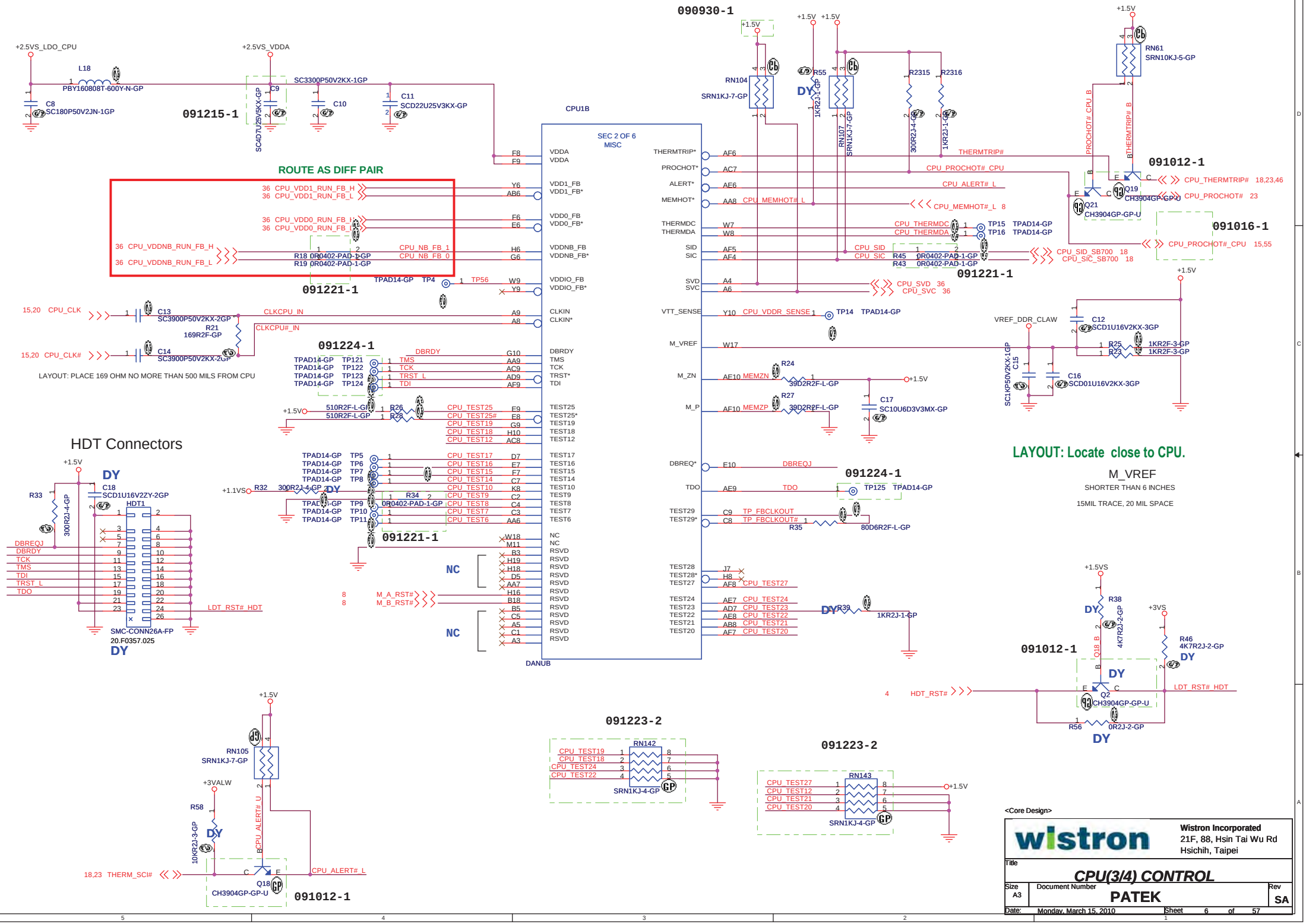
<Core Design>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU(2/4) DDR III

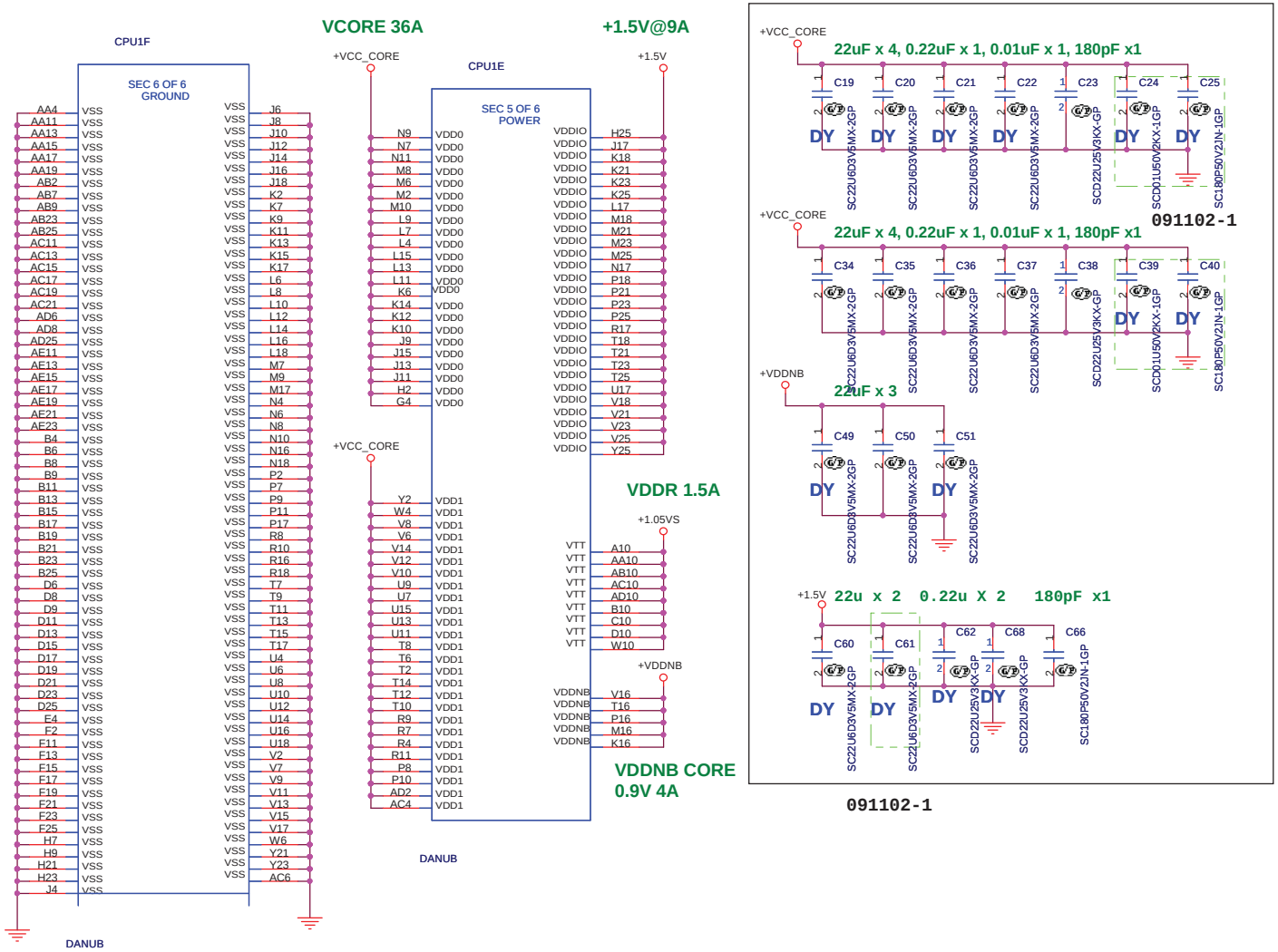
Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 5 of 57

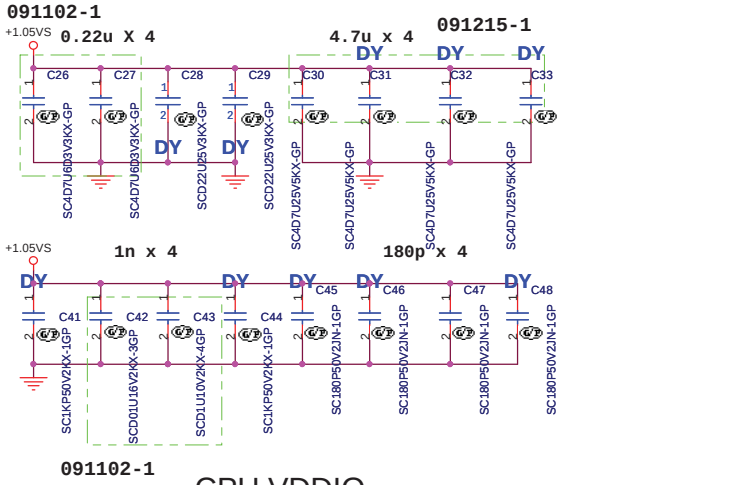

090930-1
091215-1
091221-1
091224-1
091012-1
091016-1
091223-2
CPU1B
SEC 2 OF 6
MISC
DANUB
ROUTE AS DIFF PAIR
LAYOUT: PLACE 169 OHM NO MORE THAN 500 MILS FROM CPU
LAYOUT: Locate close to CPU.
M_VREF
SHORTER THAN 6 INCHES
15MIL TRACE, 20 MIL SPACE
HDT Connectors
SMC-CONN26A-FP
20.F0357.025
NC
DY
+2.5VS_LDO_CPU
+2.5VS_VDDA
+1.5V
+1.5VS
+3VS
+3VALW
THERMTRIP#
PROCHOT# CPU
CPU_PROCHOT# CPU
CPU_ALERT# L
CPU_MEMHOT# L
CPU_THERMDC
CPU_THERMDA
CPU_SID
CPU_SIC
CPU_SVD
CPU_SVC
CPU_VDDR_SENSE
DBREQJ
TDO
TP_FBCLKOUT
TP_FBCLKOUT#
CPU_CLK
CPU_CLK#
CLKCPU_IN
CLKCPU#_IN
DBRDY
TMS
TCK
TRST_L
TDI
LDT_RST# HDT
HDT_RST#
M_A_RST#
M_B_RST#
THERM_SCI#
CPU_ALERT# L
CPU_THERMTRIP# 18,23,46
CPU_PROCHOT# 23
CPU_PROCHOT#_CPU 15,55
CPU_SID_SB700 18
CPU_SIC_SB700 18
CPU_MEMHOT#_L 8
CPU_VDD1_RUN_FB_H 36
CPU_VDD1_RUN_FB_L 36
CPU_VDD0_RUN_FB_H 36
CPU_VDD0_RUN_FB_L 36
CPU_VDDNB_RUN_FB_H 36
CPU_VDDNB_RUN_FB_L 36
CPU_SVD 36
CPU_SVC 36
15,20 CPU_CLK
15,20 CPU_CLK#
18,23 THERM_SCI#
VREF_DDR_CLAW
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
CPU(3/4) CONTROL
Size A3
Document Number
PATEK
Rev SA
Date: Monday, March 15, 2010
Sheet 6 of 57
<Core Design>

CPU MEMORY VTT

LAYOUT: PLACE UNDER CPU ON BACK

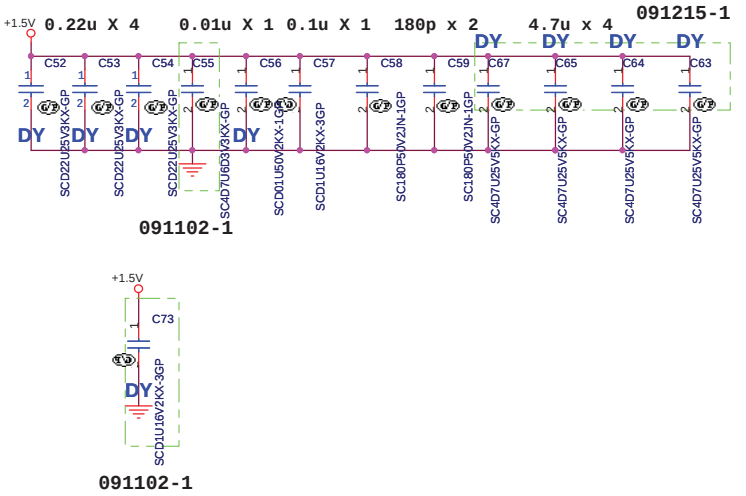


LAYOUT: PLACE CLOSE TO CPU socket



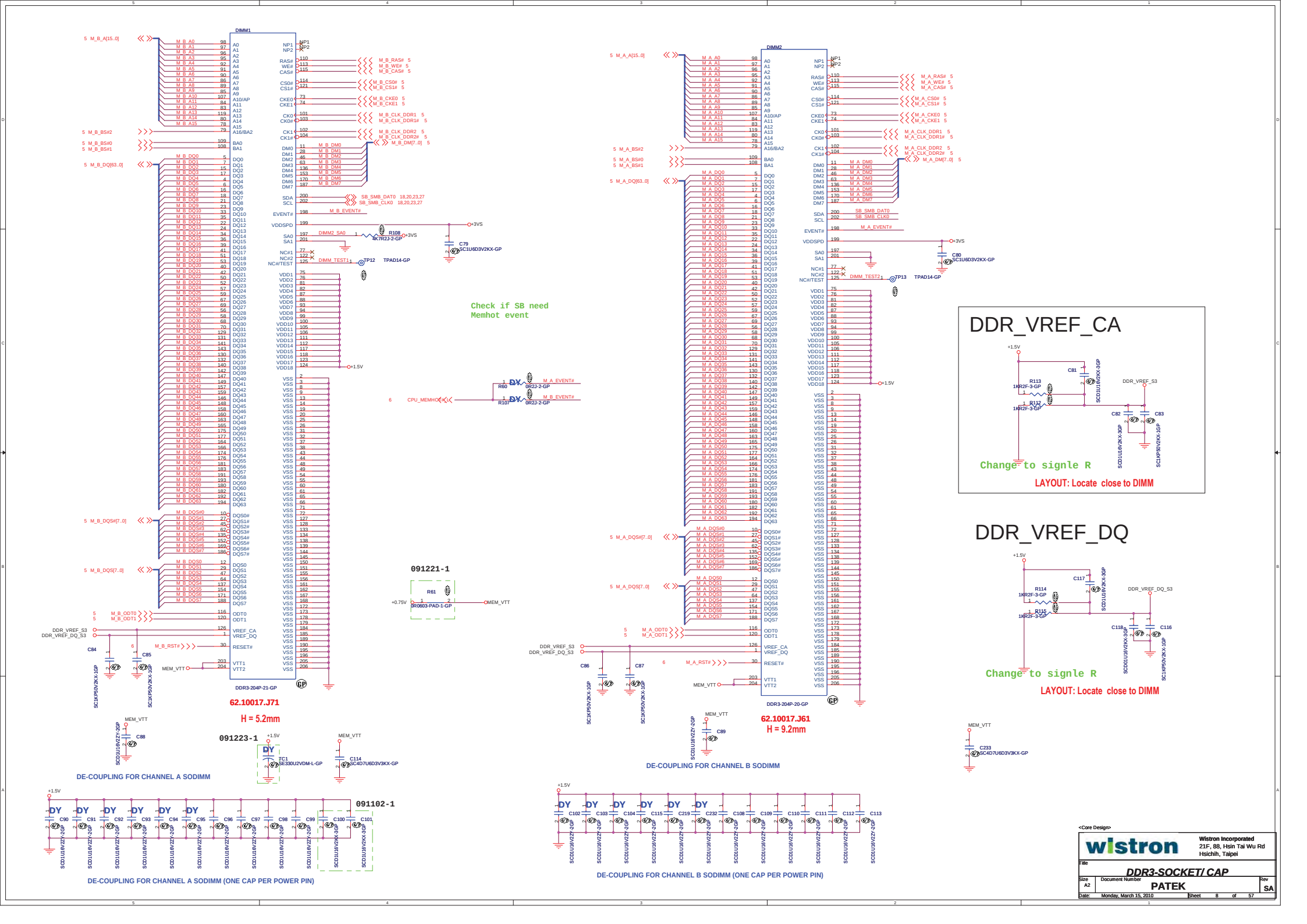
CPU VDDIO

LAYOUT: PLACE CLOSE TO CPU BETWEEN CPU AND MEMORY



<Core Design>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	CPU(4/4) POWER
Size A3	Document Number PATEK
Rev	SA
Date: Monday, March 15, 2010	Sheet 7 of 57



<core_design>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	DDR3-SOCKET/ CAP	
Size A2	Document Number PATEK	Rev SA
Date: Monday, March 15, 2010	Sheet 8 of 57	
</core_design>

SSID = N.B

U1001A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

RS880M-GP

U1001B

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

RS880M-GP

091001-1

LANE REVERSE

LANE REVERSE

LAN

NEW CARD WLAN

A-LINK

LAN

NEW CARD WLAN

Place < 100mils from pin C23 and A24

Place < 100mils from pin B25 and B24

Place < 100mils from pin AC8 and AB8

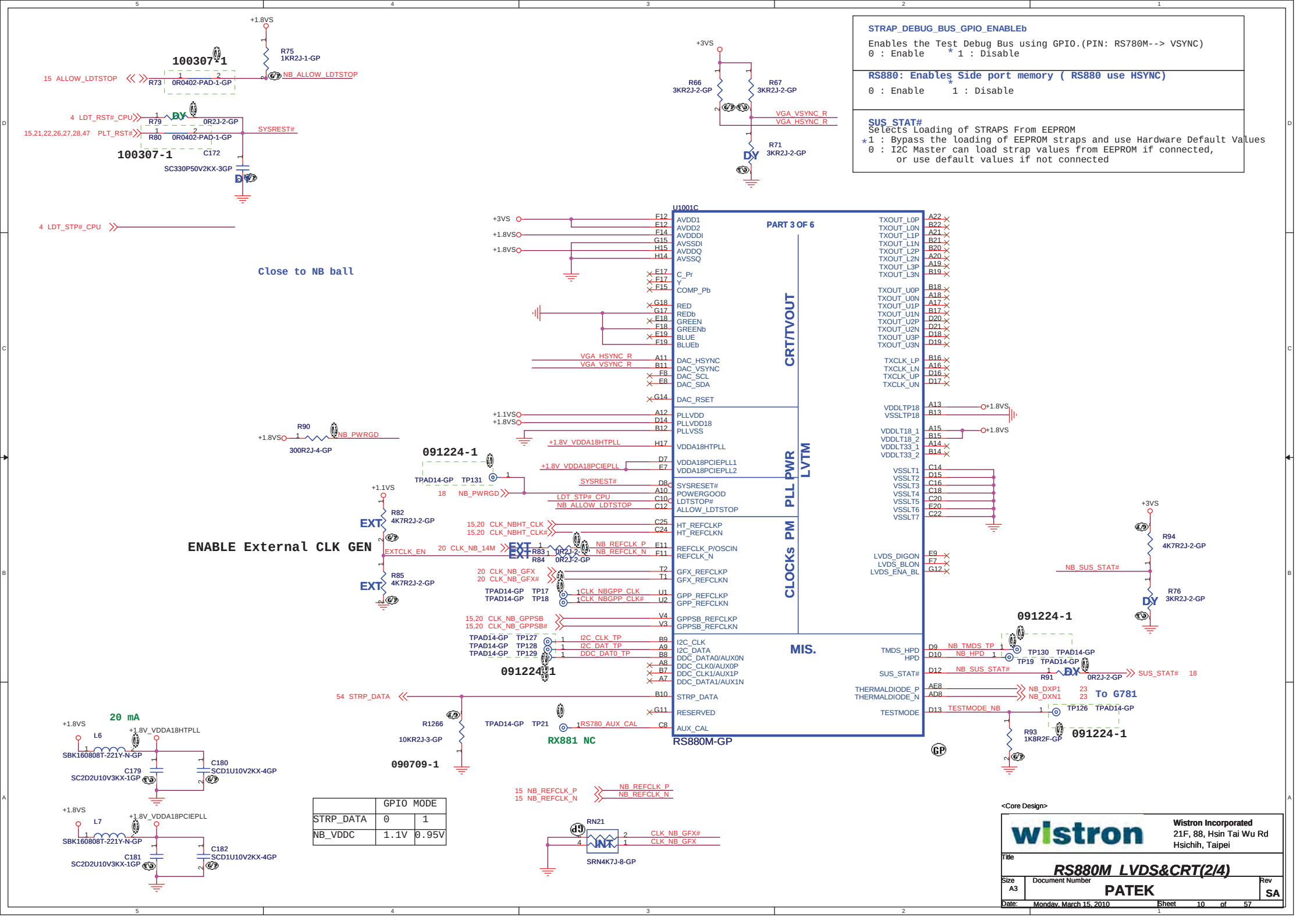
<Core Design>

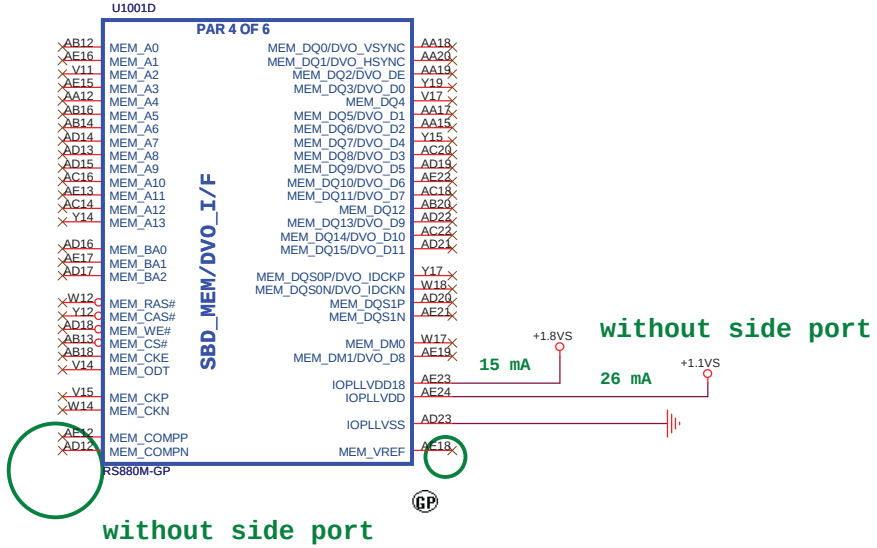
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RS880M HT LINK&PCIe(1/4)

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 9 of 57


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC)
0 : Enable * 1 : Disable
RS880: Enables Side port memory (RS880 use HSYNC)
0 : Enable * 1 : Disable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
Close to NB ball
ENABLE External CLK GEN
U1001C
PART 3 OF 6
RS880M-GP
CRT/TVOUT
PLL PWR
LVTM
CLOCKs PM
MIS.
RX881 NC
To G781
<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
RS880M_LVDS&CRT(2/4)
PATEK
Monday, March 15, 2010



<Core Design>

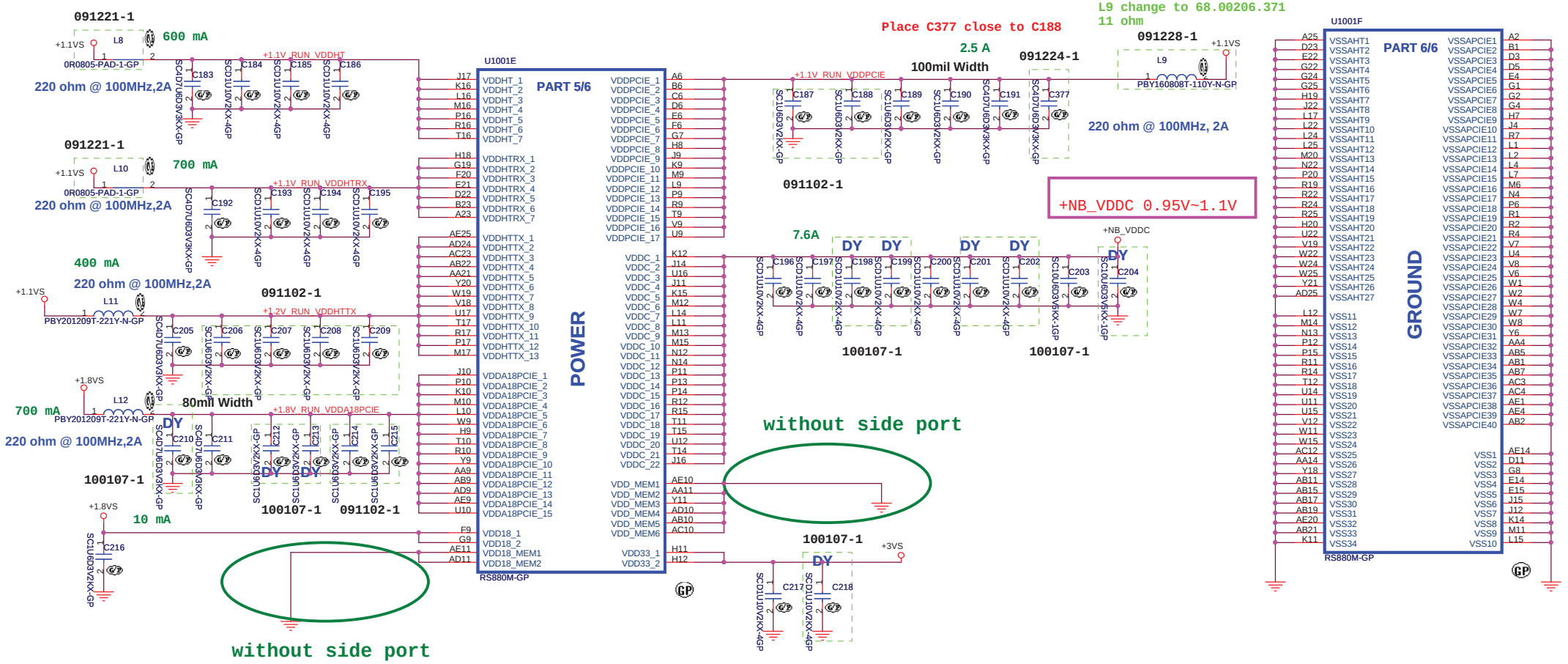
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RS880M Side Port(3/4)

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 11 of 57

SSID = N.B



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RS880M PWR&GND(4/4)

Size	Document Number	Rev
A3	PATEK	SA

Date: Monday, March 15, 2010 Sheet 12 of 57

CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

46 M93_RED
46 M93_GREEN
46 M93_BLUE

L13 NBQ160808T-470Y-N-GP → CRT_R
L14 NBQ160808T-470Y-N-GP → CRT_G
L15 NBQ160808T-470Y-N-GP → CRT_B

C221 C222 C223 C224 C225 C226 SC10P50V2JN-4GP

091225-1

091225-1

Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

M93_RED
M93_GREEN
M93_BLUE
R100 R101 R102 150R2F-1-GP

+5VS_CRT

091125-1

Q87 DMP2305U-7-GP

69.50007.691
F1 FUSE-1D1A6V-4GP-U
+5VS_CRT_FUSE
+5VS

DY C1193 SC4D7U10V5ZY-3GP
C220 SCD1U16V2ZY-2GP

091021-1 091019-1

R1248 10KR2J-3-GP
R1249 10KR2J-3-GP
CRTVDD_EN#

+5VS_CRT +5VS_CRT
EC1369 EC1370 SC1K50V2KX-1GP
DY

Q88 2N7002E-1-GP
SB_PWRGD 18,30
DY C1194 SCD1U16V2ZY-2GP

CRT1
D-SUB-15-27-GP-U2

VCC_CRT
DDC_CRT_DAT
DDC_CRT_CLK
CRT_R
CRT_G
CRT_B
JVGA_VS
JVGA_HS
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
NC#4
NC#11
GND

DY DY C230 C229 SC22P50V2JN-4GP
DY DY C227 C228 SC33P50V2JN-3GP

0803??
0804 check ok

+5VS_CRT 091009-1

C231 SCD1U16V2KX-3GP

46 VGA_HSYNC
46 VGA_VSYNC

U3 U4 74AHCT1G125GW-1-GP
OE# A GND VCC Y

HSYNC_5
VSYNC_5

SRN33J-5-GP-U RN12
JVGA_HS
JVGA_VS

Hsync & Vsync level shift

AFTE14P-GP AFTP82 CRT_R
AFTE14P-GP AFTP85 CRT_G
AFTE14P-GP AFTP86 CRT_B
AFTE14P-GP AFTP87 GND
AFTE14P-GP AFTP88 +5VS_CRT

+5VS_CRT
RN11 SRN4K7J-8-GP
DDC_CRT_DAT 46
DDC_CRT_CLK 46

DDC_CRT_DAT& DDC_CRT_CLK
The signal is 5V-tolerant on RS880M.

ESD
close to connector

+5VS_CRT
CRT_R
D3 BAV99-8-GP

+5VS_CRT
D5 BAV99S-GP
DDC_CRT_CLK
DDC_CRT_DAT

+5VS_CRT
D6 BAV99S-GP
CRT_B
CRT_G

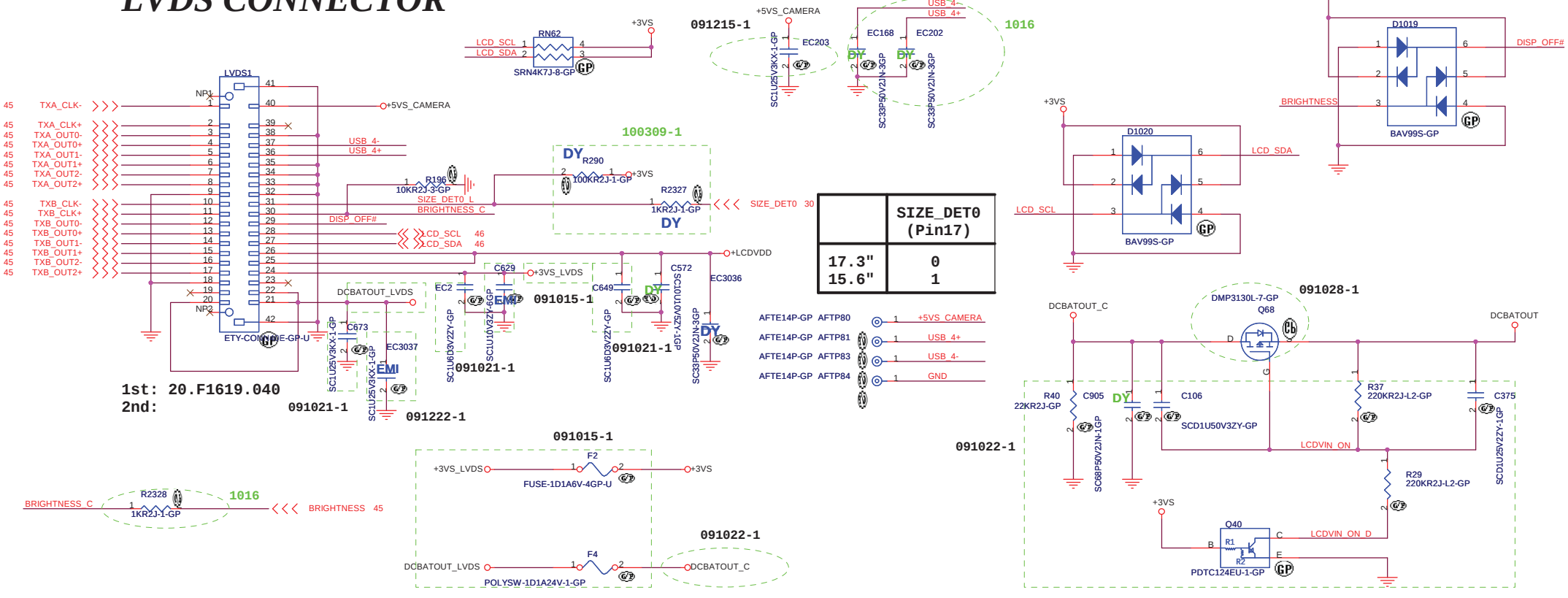
+5VS_CRT
D4 BAV99S-GP
JVGA_HS
JVGA_VS

<Core Design>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

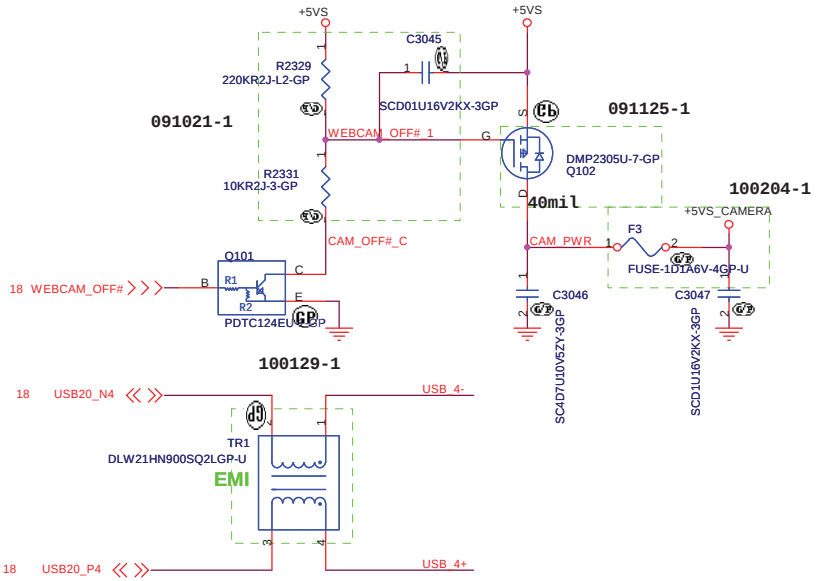
Title: CRT CONNECTOR
Size: A3
Document Number: PATEK
Rev: SA
Date: Monday, March 15, 2010
Sheet 13 of 57

LVDS CONNECTOR



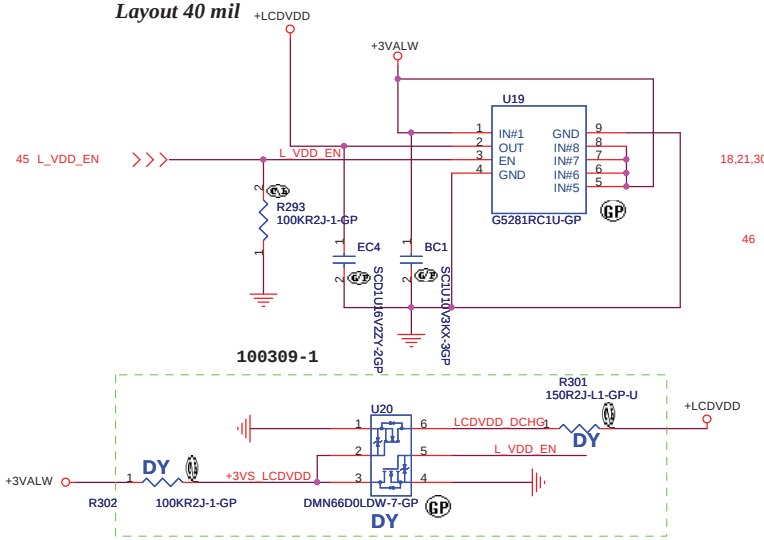
	SIZE_DET0 (Pin17)
17.3"	0
15.6"	1

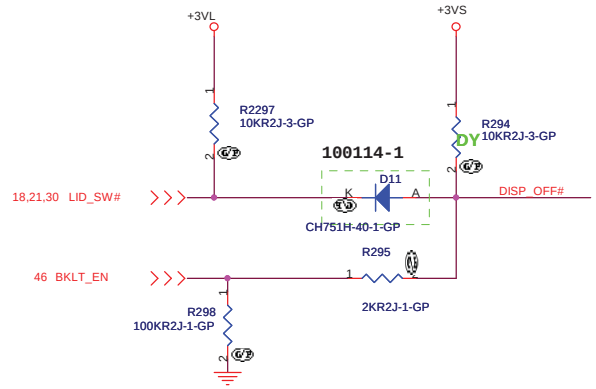
Camera Power&Interface



LCD Power&Discharge

Layout 40 mil





<Core Design>

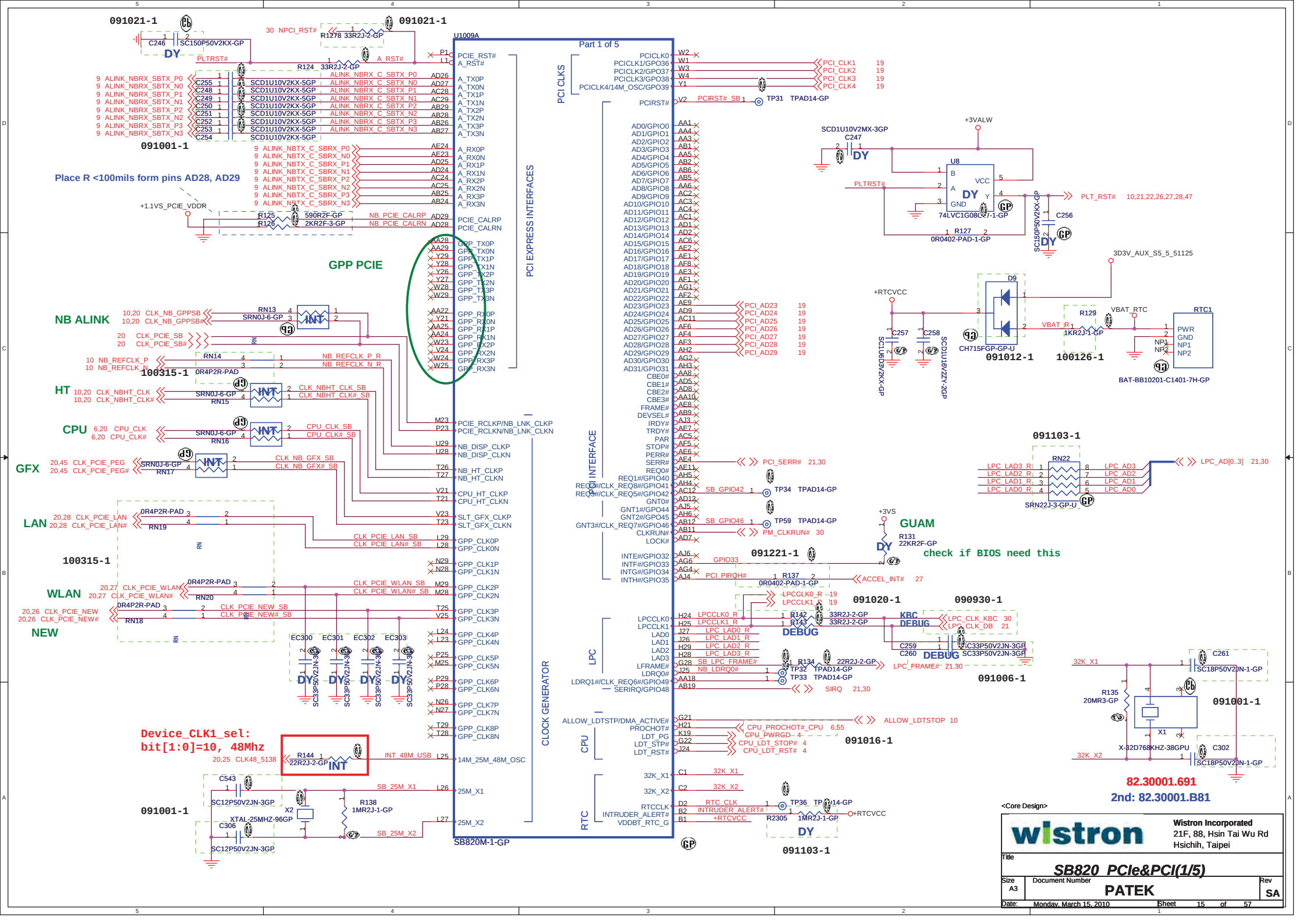
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LVDS Connector/CAMERA

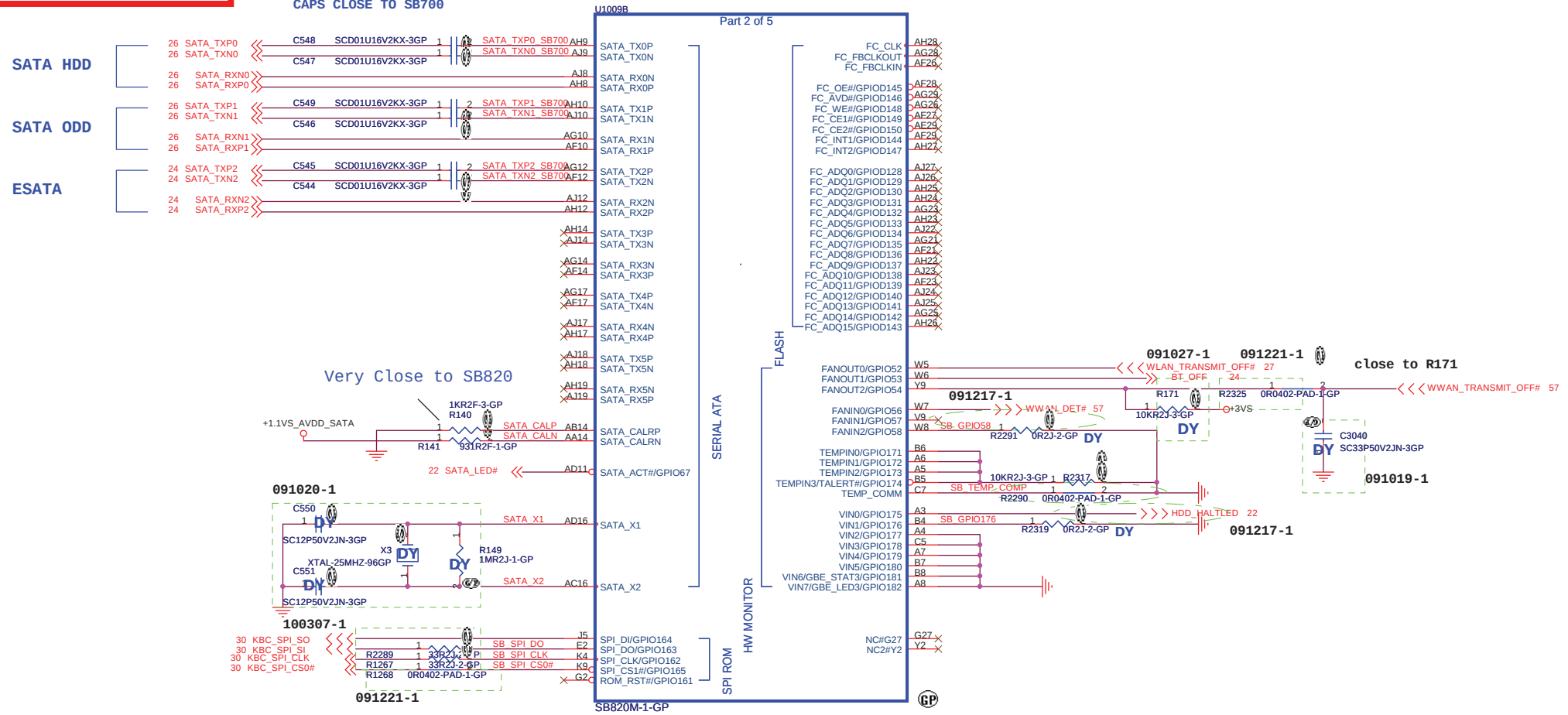
Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 14 of 57


091021-1
C246
SC150P50V2KX-GP
DY
PLTRST#
30 NPCI_RST#
R1278 33R2J-2-GP
091021-1
R124 33R2J-2-GP
A_RST#
U1009A
Part 1 of 5
PCIE_RST#
A_RST#
ALINK_NBRX_SBTX_P0
ALINK_NBRX_SBTX_N0
ALINK_NBRX_SBTX_P1
ALINK_NBRX_SBTX_N1
ALINK_NBRX_SBTX_P2
ALINK_NBRX_SBTX_N2
ALINK_NBRX_SBTX_P3
ALINK_NBRX_SBTX_N3
C255 C248 C249 C250 C251 C252 C253 C254
SCD1U10V2KX-5GP
091001-1
ALINK_NBRX_C_SBTX_P0
ALINK_NBRX_C_SBTX_N0
ALINK_NBRX_C_SBTX_P1
ALINK_NBRX_C_SBTX_N1
ALINK_NBRX_C_SBTX_P2
ALINK_NBRX_C_SBTX_N2
ALINK_NBRX_C_SBTX_P3
ALINK_NBRX_C_SBTX_N3
AD26 AD27 AC28 AC29 AB29 AB28 AB26 AB27
A_TX0P A_TX0N A_TX1P A_TX1N A_TX2P A_TX2N A_TX3P A_TX3N
ALINK_NBTX_C_SBRX_P0
ALINK_NBTX_C_SBRX_N0
ALINK_NBTX_C_SBRX_P1
ALINK_NBTX_C_SBRX_N1
ALINK_NBTX_C_SBRX_P2
ALINK_NBTX_C_SBRX_N2
ALINK_NBTX_C_SBRX_P3
ALINK_NBTX_C_SBRX_N3
AE24 AE23 AD25 AD24 AC24 AC25 AB25 AB24
A_RX0P A_RX0N A_RX1P A_RX1N A_RX2P A_RX2N A_RX3P A_RX3N
Place R <100mils form pins AD28, AD29
+1.1VS_PCIE_VDDR
R125 590R2F-GP
R126 2KR2F-3-GP
NB_PCIE_CALRP
NB_PCIE_CALRN
AD29 AD28
PCIE_CALRP
PCIE_CALRN
PCI EXPRESS INTERFACES
GPP PCIE
GPP_TX0P GPP_TX0N GPP_TX1P GPP_TX1N GPP_TX2P GPP_TX2N GPP_TX3P GPP_TX3N
GPP_RX0P GPP_RX0N GPP_RX1P GPP_RX1N GPP_RX2P GPP_RX2N GPP_RX3P GPP_RX3N
NB ALINK
10,20 CLK_NB_GPPSB
10,20 CLK_NB_GPPSB#
RN13 SRN0J-6-GP
20 CLK_PCIE_SB
20 CLK_PCIE_SB#
10 NB_REFCLK_P
10 NB_REFCLK_N
RN14 0R4P2R-PAD
100315-1
NB_REFCLK_P_R
NB_REFCLK_N_R
HT
10,20 CLK_NBHT_CLK
10,20 CLK_NBHT_CLK#
RN15
CLK_NBHT_CLK_SB
CLK_NBHT_CLK#_SB
CPU
6,20 CPU_CLK
6,20 CPU_CLK#
RN16
CPU_CLK_SB
CPU_CLK#_SB
GFX
20,45 CLK_PCIE_PEG
20,45 CLK_PCIE_PEG#
RN17
CLK_NB_GFX_SB
CLK_NB_GFX#_SB
LAN
20,28 CLK_PCIE_LAN
20,28 CLK_PCIE_LAN#
RN19
100315-1
CLK_PCIE_LAN_SB
CLK_PCIE_LAN#_SB
WLAN
20,27 CLK_PCIE_WLAN
20,27 CLK_PCIE_WLAN#
RN20
CLK_PCIE_WLAN_SB
CLK_PCIE_WLAN#_SB
NEW
20,26 CLK_PCIE_NEW
20,26 CLK_PCIE_NEW#
RN18
CLK_PCIE_NEW_SB
CLK_PCIE_NEW#_SB
EC300 EC301 EC302 EC303
SC33P50V2JN-3GP
M23 P23 U29 U28 T26 T27 V21 T21 V23 T23 L29 L28 N29 N28 M29 M28 T25 V25 L24 L23 P25 M25 P29 P28 N26 N27 T29 T28
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P GPP_CLK0N GPP_CLK1P GPP_CLK1N GPP_CLK2P GPP_CLK2N GPP_CLK3P GPP_CLK3N GPP_CLK4P GPP_CLK4N GPP_CLK5P GPP_CLK5N GPP_CLK6P GPP_CLK6N GPP_CLK7P GPP_CLK7N GPP_CLK8P GPP_CLK8N
CLOCK GENERATOR
Device_CLK1_sel:
bit[1:0]=10, 48Mhz
20,25 CLK48_5138
R144 22R2J-2-GP
INT_48M_USB
14M_25M_48M_OSC
C543
SC12P50V2JN-3GP
X2
XTAL-25MHZ-96GP
C306
SC12P50V2JN-3GP
R138 1MR2J-1-GP
SB_25M_X1
SB_25M_X2
25M_X1
25M_X2
091001-1
SB820M-1-GP
PCI CLKS
PCICLK0 PCICLK1/GPO36 PCICLK2/GPO37 PCICLK3/GPO38 PCICLK4/14M_OSC/GPO39
W2 W1 W3 W4 Y1
PCI_CLK1 19
PCI_CLK2 19
PCI_CLK3 19
PCI_CLK4 19
PCIRST#
V2
PCIRST#_SB
TP31 TPAD14-GP
AD0/GPIO0 AD1/GPIO1 AD2/GPIO2 AD3/GPIO3 AD4/GPIO4 AD5/GPIO5 AD6/GPIO6 AD7/GPIO7 AD8/GPIO8 AD9/GPIO9 AD10/GPIO10 AD11/GPIO11 AD12/GPIO12 AD13/GPIO13 AD14/GPIO14 AD15/GPIO15 AD16/GPIO16 AD17/GPIO17 AD18/GPIO18 AD19/GPIO19 AD20/GPIO20 AD21/GPIO21 AD22/GPIO22 AD23/GPIO23 AD24/GPIO24 AD25/GPIO25 AD26/GPIO26 AD27/GPIO27 AD28/GPIO28 AD29/GPIO29 AD30/GPIO30 AD31/GPIO31
AA1 AA4 AA3 AB1 AA5 AB2 AB6 AB5 AA6 AC2 AC3 AC4 AC1 AD1 AD2 AC6 AE2 AE1 AF8 AE3 AF1 AG1 AF2 AE9 AD9 AC11 AF6 AF4 AF3 AH2 AG2 AH3 AA8 AD5 AD8 AA10 AE8 AB9 AJ3 AE7 AC5 AF5 AE6
PCI_AD23 19
PCI_AD24 19
PCI_AD25 19
PCI_AD26 19
PCI_AD27 19
PCI_AD28 19
PCI_AD29 19
CBE0# CBE1# CBE2# CBE3# FRAME# DEVSEL# IRDY# TRDY# PAR STOP# PERR# SERR# REQ0# REQ1#/GPIO40 REQ2#/CLK_REQ8#/GPIO41 REQ3#/CLK_REQ5#/GPIO42 GNT0# GNT1#/GPO44 GNT2#/GPO45 GNT3#/CLK_REQ7#/GPIO46 CLKRUN# LOCK#
AE4 AE11 AH5 AH4 AC12 AD12 AJ5 AH6 AB12 AB11 AD7
PCI_SERR# 21,30
SB_GPIO42 TP34 TPAD14-GP
SB_GPIO46 TP59 TPAD14-GP
PM_CLKRUN# 30
INTE#/GPIO32 INTF#/GPIO33 INTG#/GPIO34 INTH#/GPIO35
AJ6 AG6 AG4 AJ4
GPIO33
PCI_PIRQH#
R137 0R0402-PAD-1-GP
ACCEL_INT# 27
091221-1
PCI INTERFACE
LPC
LPCCLK0 LPCCLK1 LAD0 LAD1 LAD2 LAD3 LFRAME# LDRQ0# LDRQ1#/CLK_REQ6#/GPIO49 SERIRQ/GPIO48
H24 H25 J27 J26 H29 H28 G28 J25 AA18 AB19
LPCCLK0_R 19
LPCCLK1_R 19
091020-1
090930-1
R142 33R2J-2-GP
R143 33R2J-2-GP
KBC DEBUG
DEBUG
LPC_CLK_KBC 30
LPC_CLK_DB 21
C259 C260 SC33P50V2JN-3GP
LPC_LAD0_R
LPC_LAD1_R
LPC_LAD2_R
LPC_LAD3_R
SB_LPC_FRAME#
NB_LDRQ0#
R134 22R2J-2-GP
TP32 TPAD14-GP
TP33 TPAD14-GP
LPC_FRAME# 21,30
SIRQ 21,30
091006-1
CPU
ALLOW_LDTSTP/DMA_ACTIVE# PROCHOT# LDT_PG LDT_STP# LDT_RST#
G21 H21 K19 G22 J24
ALLOW_LDTSTOP 10
CPU_PROCHOT#_CPU 6,55
CPU_PWRGD 4
CPU_LDT_STOP# 4
CPU_LDT_RST# 4
091016-1
RTC
32K_X1 32K_X2 RTCCLK INTRUDER_ALERT# VDDBT_RTC_G
C1 C2 D2 B2 B1
RTC_CLK
INTRUDER_ALERT#
+RTCVCC
TP36 TPAD14-GP
R2305 1MR2J-1-GP
091103-1
SCD1U10V2MX-3GP C247
+3VALW
U8
74LVC1G08GW-1-GP
PLT_RST# 10,21,22,26,27,28,47
R127 0R0402-PAD-1-GP
C256
SC150P50V2KX-GP
3D3V_AUX_S5_5_51125
D9
CH715FGP-GP-U
091012-1
+RTCVCC
C257 C258
SC1U6D3V2KX-GP
SCD1U16V2ZY-2GP
R129 1KR2J-1-GP
VBAT_R
VBAT_RTC
RTC1
BAT-BB10201-C1401-7H-GP
100126-1
091103-1
RN22 SRN22J-3-GP-U
LPC_LAD3_R LPC_LAD2_R LPC_LAD1_R LPC_LAD0_R
LPC_AD3 LPC_AD2 LPC_AD1 LPC_AD0
LPC_AD[0..3] 21,30
+3VS
GUAM
R131 22KR2F-GP
check if BIOS need this
C261
SC18P50V2JN-1-GP
R135 20MR3-GP
091001-1
X1
X-32D768KHZ-38GPU
C302
SC18P50V2JN-1-GP
32K_X1
32K_X2
82.30001.691
2nd: 82.30001.B81
<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
SB820 PCIe&PCI(1/5)
Size A3
Document Number
PATEK
Rev SA
Date: Monday, March 15, 2010
Sheet 15 of 57

SSID = S.B

PLACE SATA AC DECOUPLING CAPS CLOSE TO SB700



<Core Design>

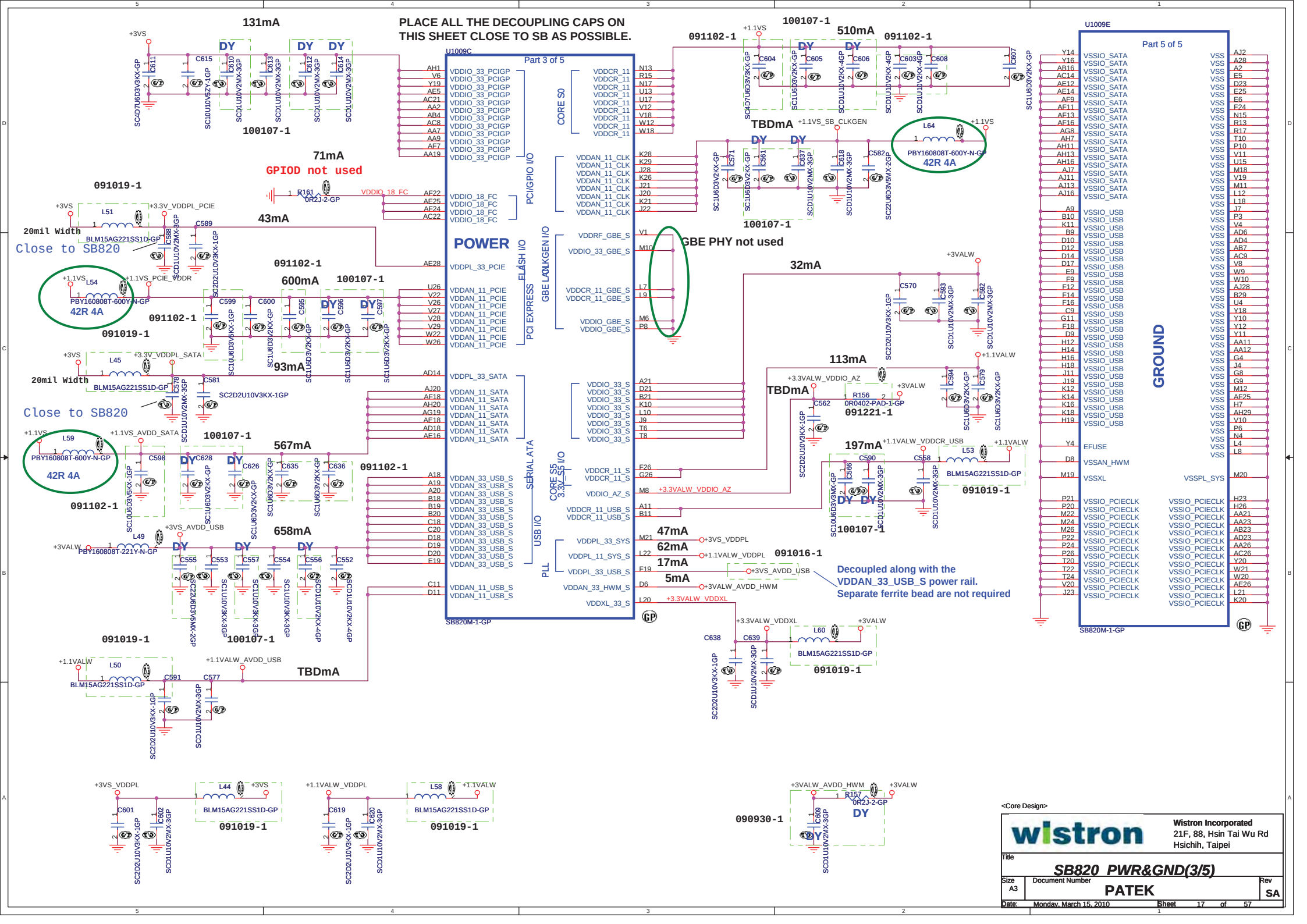
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SB820 SATA&IDE(2/5)

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 16 of 57



<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SB820 PWR&GND(3/5)

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 17 of 57

SSID = S.B

Part 4 of 5

U1009D

SB820M-1-GP

Internal 10K PU

Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.

USB-FSD1 FPR

USB-9 Bluetooth

USB-8 WLAN

USB-7 WWAN

USB-6 USB Card Reader

USB-5 Right Side

USB-4 USB Camera

USB-3 Right Side

USB-2 Left Side (e-SATA combo)

USB-1 New Card

USB-0 Left Side (S/W Debug port)

Need to check leakage

Strap Pin / define to use LPC or SPI ROM

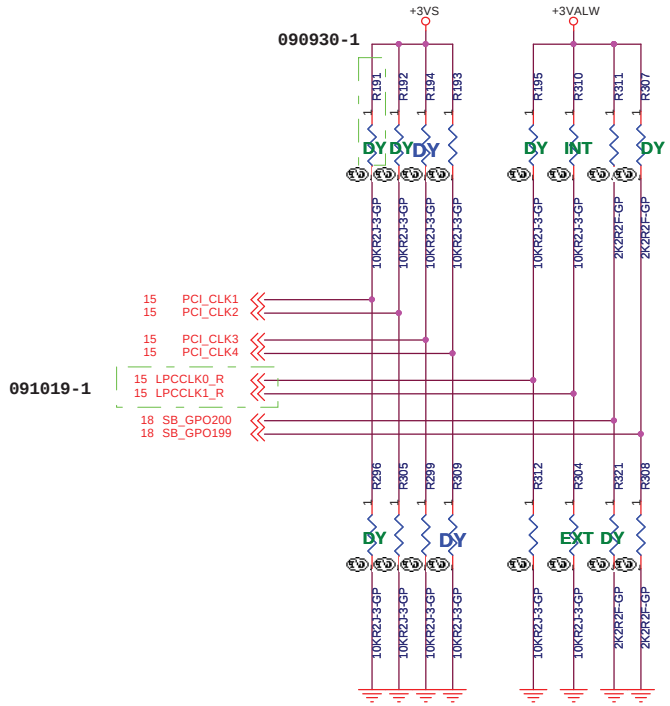
Low Power Mode

Performance Mode

<Core Design>

Wistron Incorporated	21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	SB820 USB&GPIO(4/5)
Size	A3
Document Number	PATEK
Rev	SA
Date:	Monday, March 15, 2010
Sheet	18 of 57

REQUIRED STRAPS

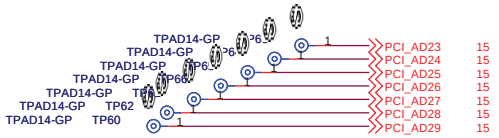


USE this pin to determine INT/EXT CLK

091020-1

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPCCLK0_R (LPCCLK0)	LPCCLK1_R (LPCCLK1)	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	L, H = LPC ROM L, L = FWH ROM

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

<Core Design>

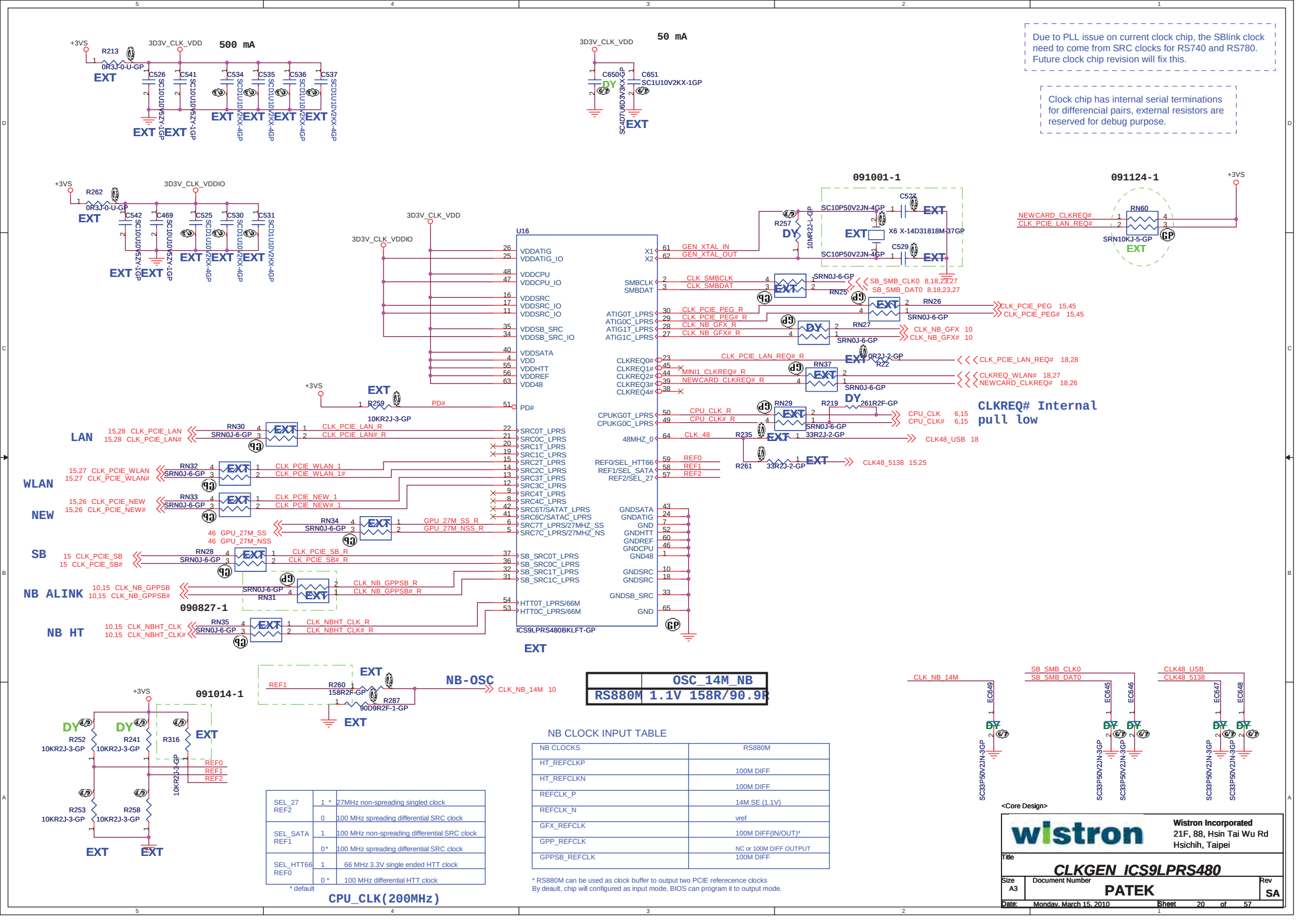
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: *SB820 STRAPPING(5/5)*

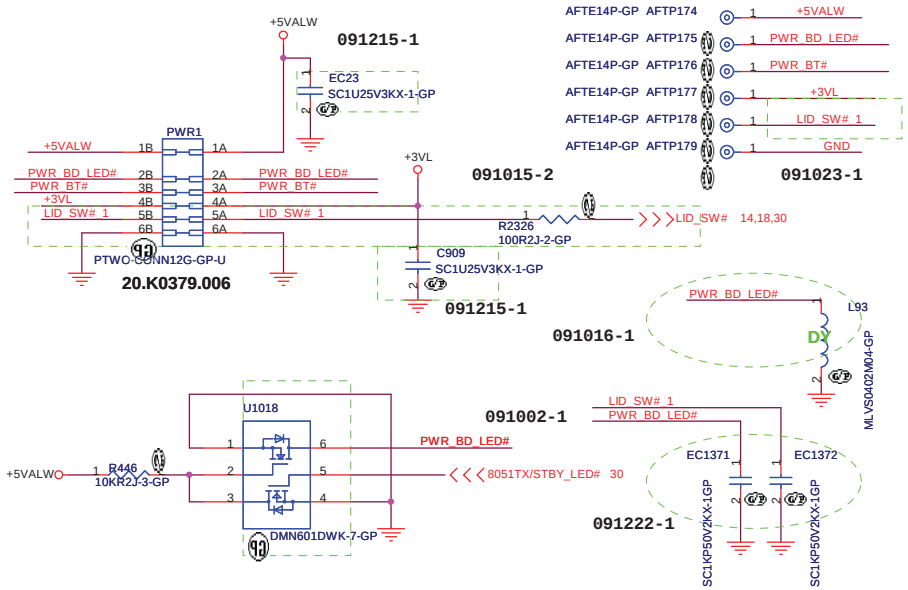
Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 19 of 57

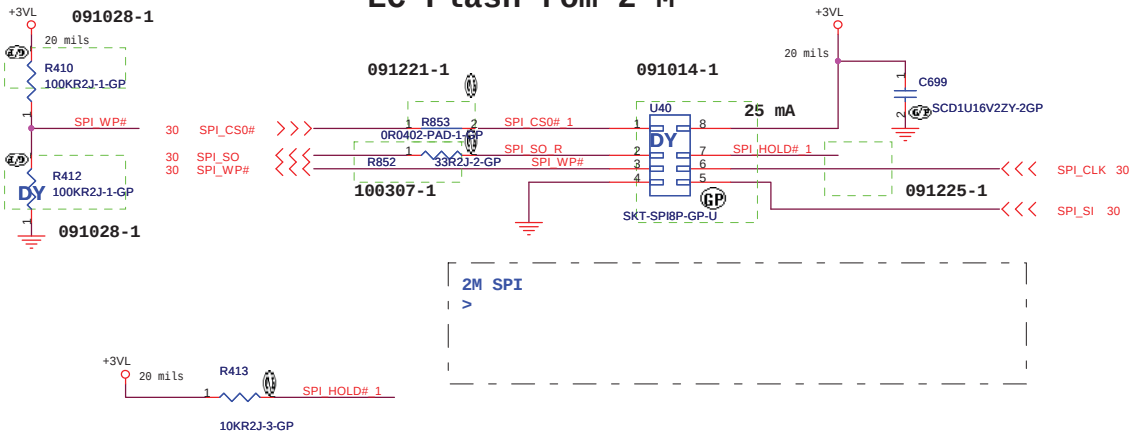

Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.
500 mA
50 mA
091001-1
091124-1
090827-1
091014-1
U16
ICS9LPRS480BKLFT-GP
CLKREQ# Internal pull low
LAN
WLAN
NEW
SB
NB ALINK
NB HT
NB-OSC
OSC_14M_NB
RS880M 1.1V 158R/90.9R
NB CLOCK INPUT TABLE
CPU_CLK(200MHz)
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
CLKGEN_ICS9LPRS480
PATEK
Monday, March 15, 2010

POWER SW CONN.

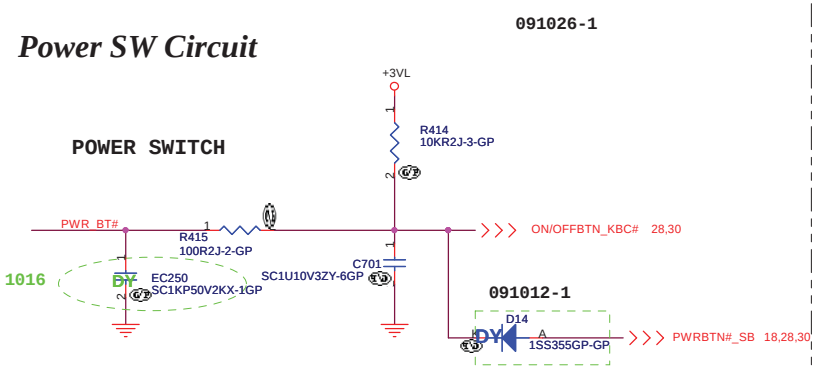
COVER SWITCH

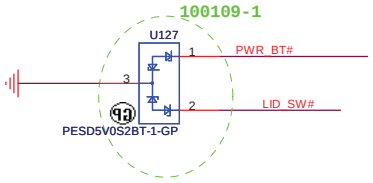


EC Flash rom 2 M

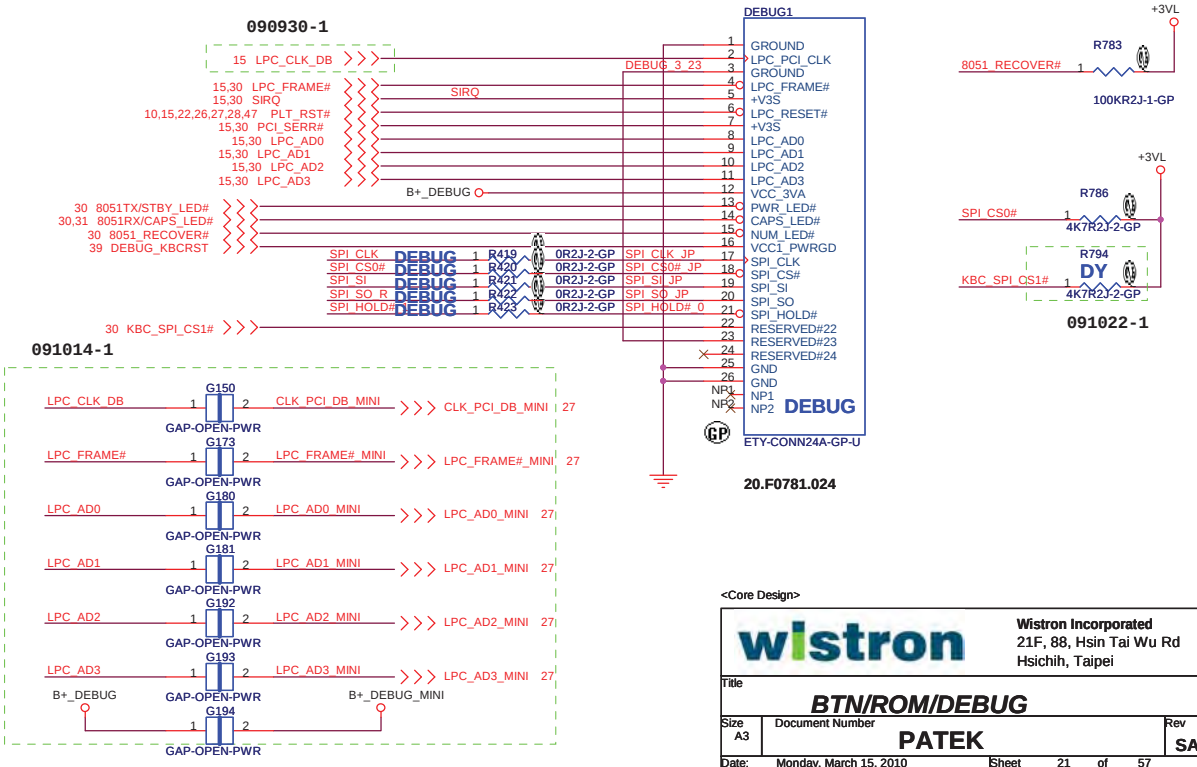


Power SW Circuit





24 PIN LPC DEBUG CONN.



<Core Design>

wistron

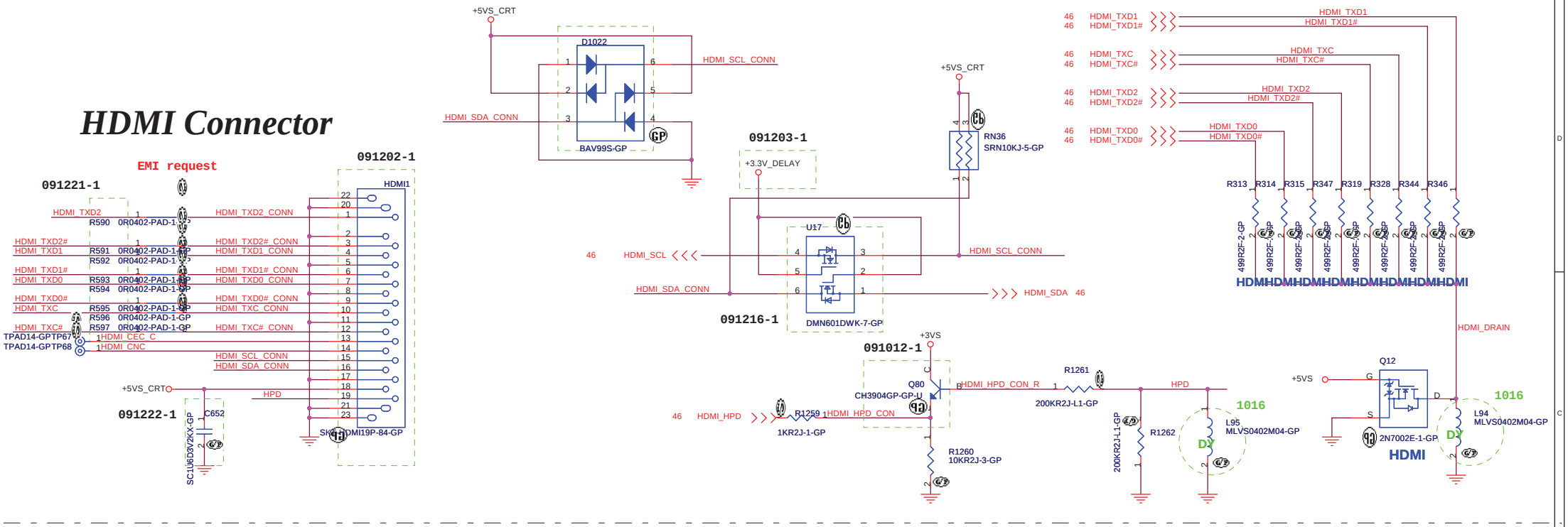
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: BTN/ROM/DEBUG

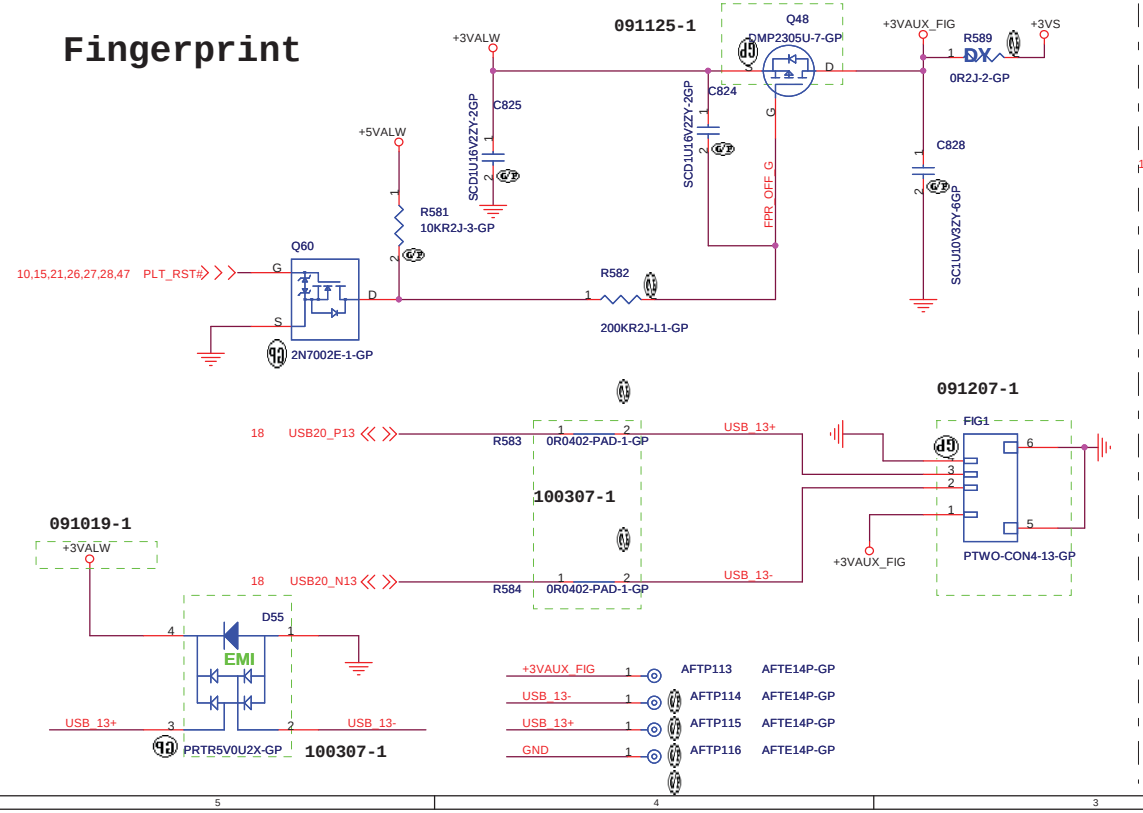
Size	Document Number	Rev
A3	PATEK	SA

Date: Monday, March 15, 2010 Sheet 21 of 57

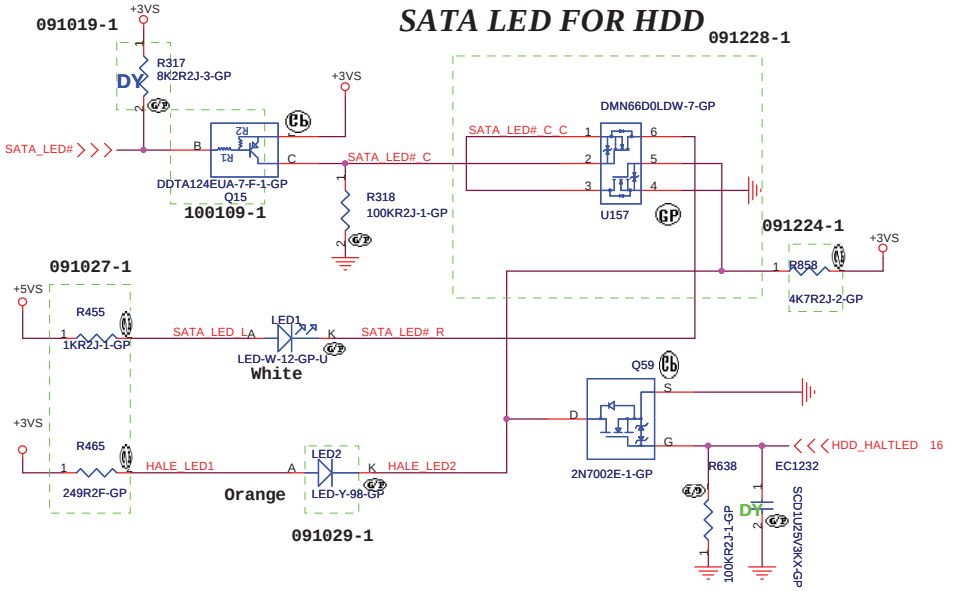
HDMI Connector



Fingerprint



SATA LED FOR HDD



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

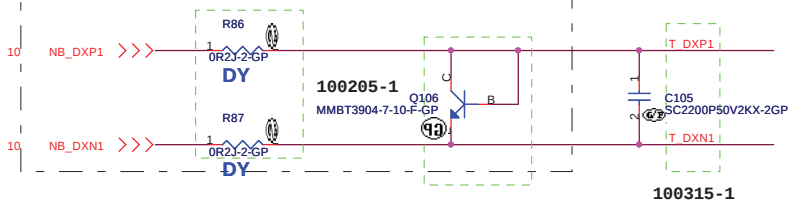
Title: HDMI/FPR/SATA LED

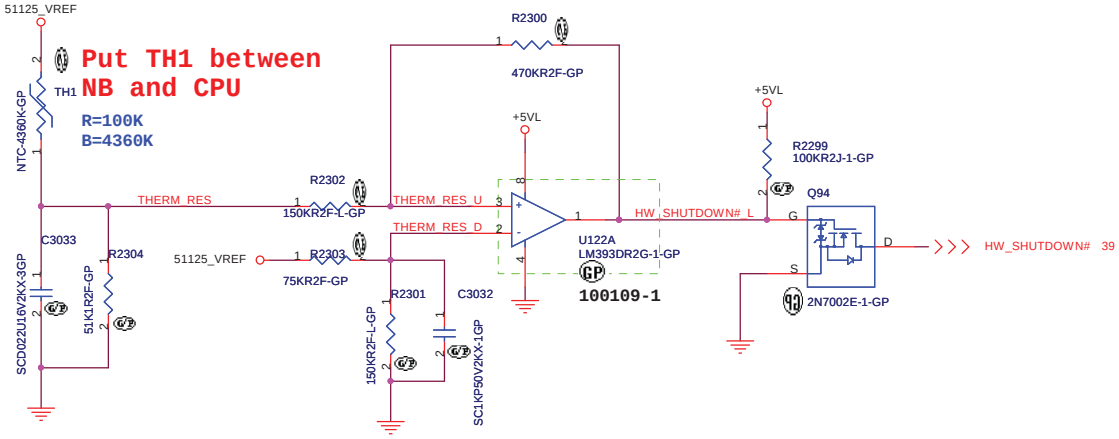
Size	Document Number	Rev
A3	PATEK	SA

Date: Monday, March 15, 2010 Sheet 22 of 57

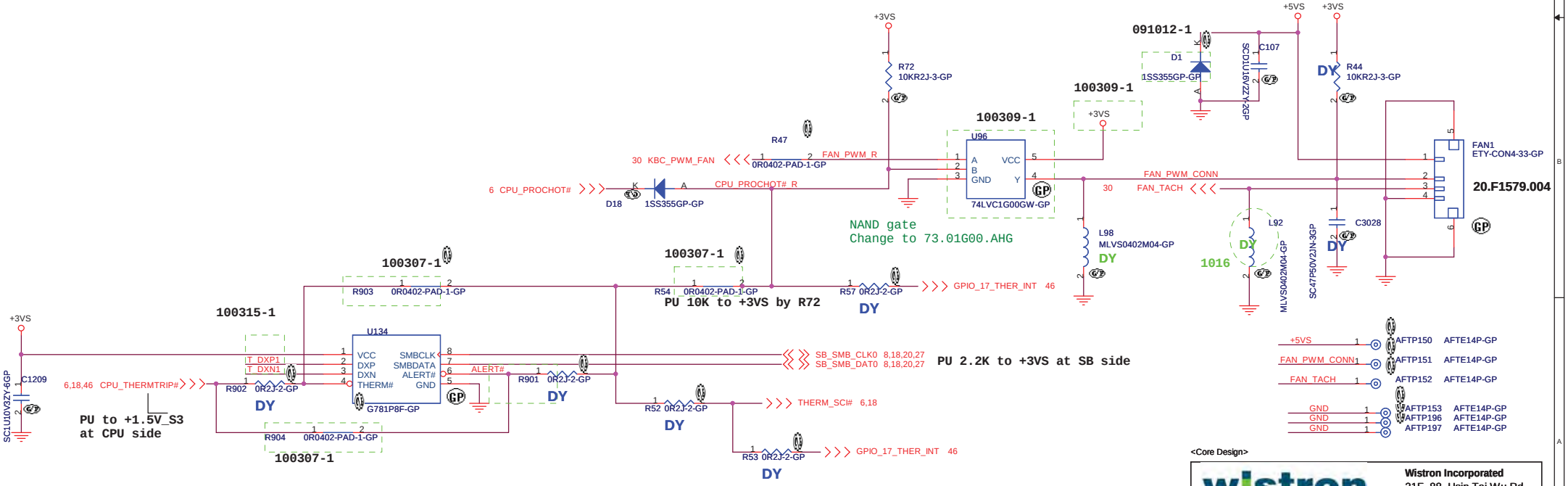
CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal chip.





4 WIRE PWM Fan Control circuit



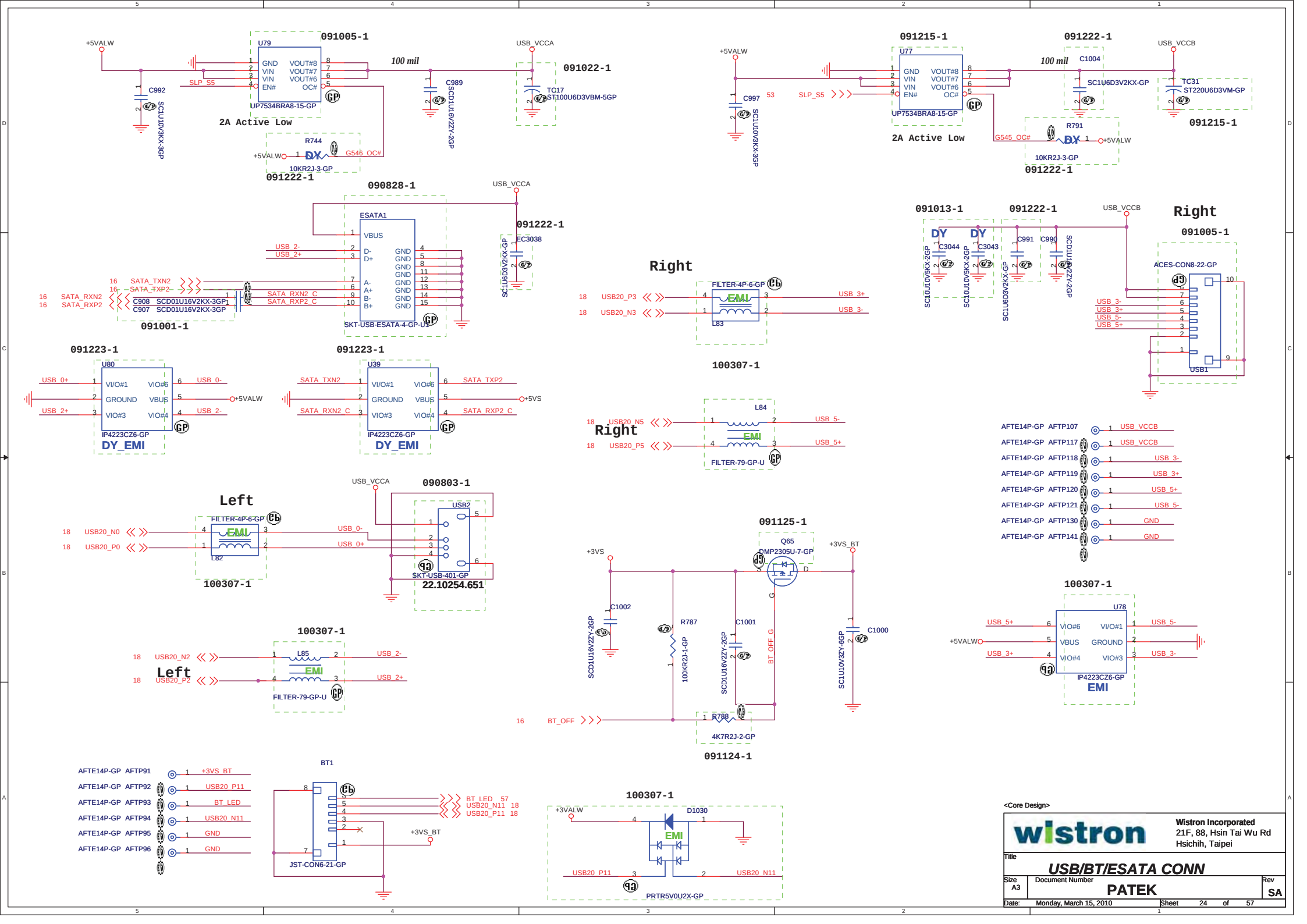
<Core Design>

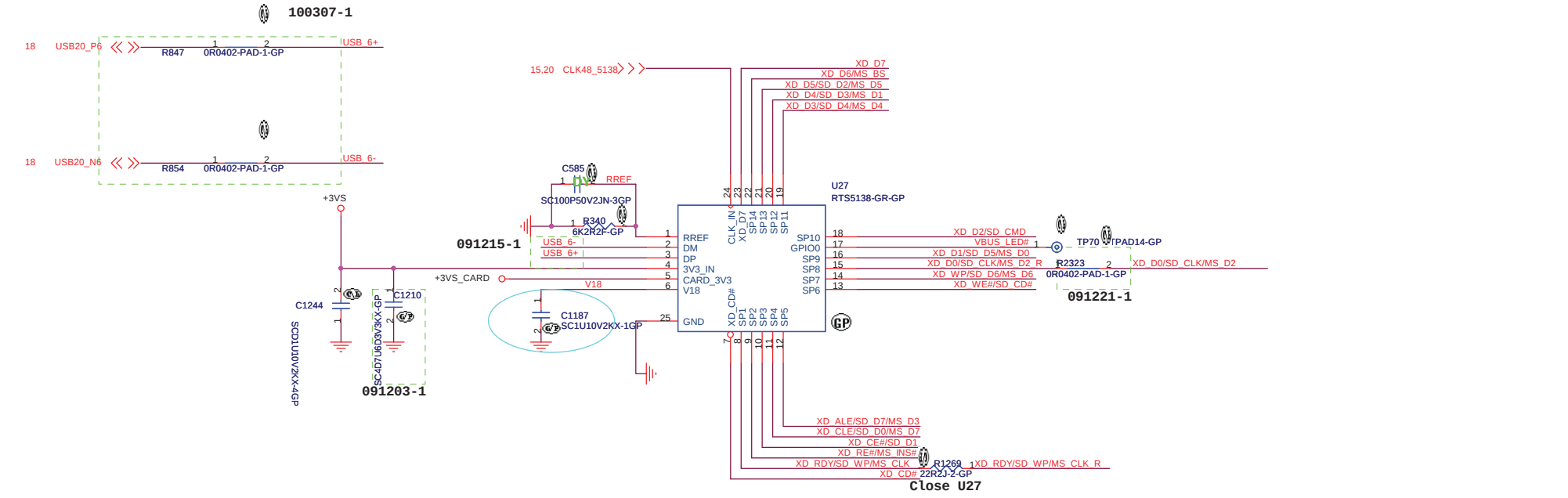
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

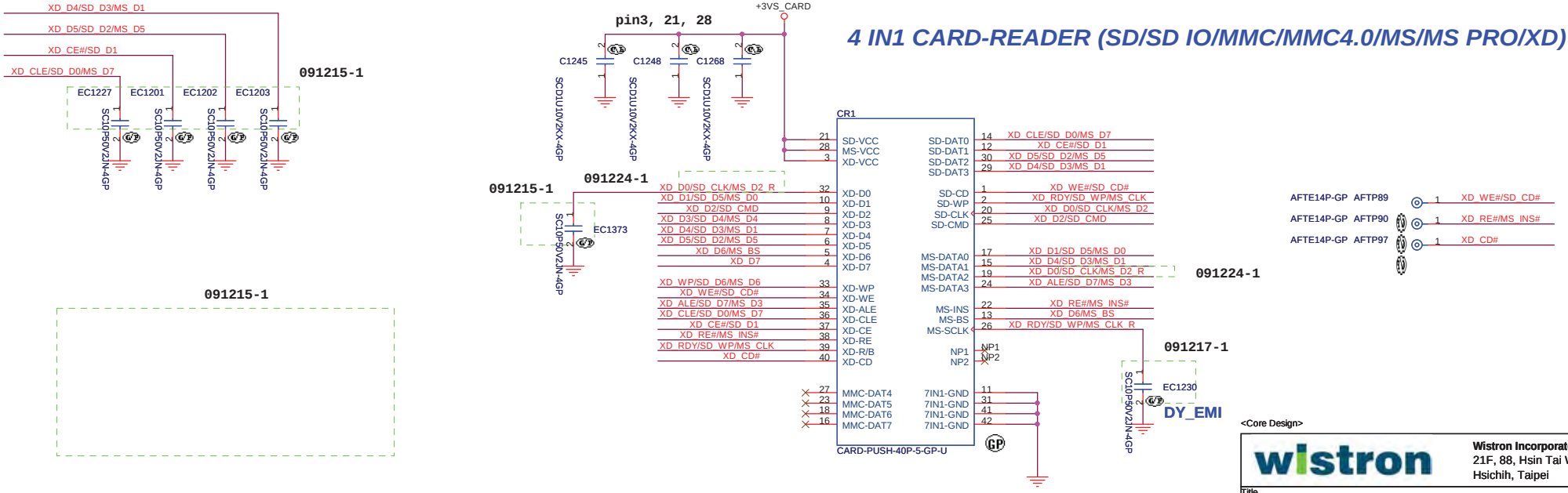
Title: G781P8F THERMAL

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 23 of 57


091005-1
U79
+5VALW
C992
SCU10V3KX-3GP
SLP_S5
GND
VIN
VIN
EN#
VOUT#8
VOUT#7
VOUT#6
OC#
UP7534BRA8-15-GP
2A Active Low
100 mil
C989
SCD1U16V2ZY-2GP
USB_VCCA
091022-1
TC17
ST100U6D3VBM-5GP
R744
10KR2J-3-GP
G546_OC#
091222-1
091215-1
U77
C997
SCU10V3KX-3GP
53
G545_OC#
C1004
SC1U6D3V2KX-GP
TC31
ST220U6D3VM-GP
R791
10KR2J-3-GP
090828-1
ESATA1
VBUS
D-
D+
A-
A+
B-
B+
GND
USB_2-
USB_2+
SATA_TXN2
SATA_TXP2
SATA_RXN2
SATA_RXP2
SATA_RXN2_C
SATA_RXP2_C
C908 SCD01U16V2KX-3GP1
C907 SCD01U16V2KX-3GP
091001-1
SKT-USB-ESATA-4-GP-U1
EC3038
SC1U6D3V2KX-GP
091013-1
DY
C3044
C3043
SC1U10U5KX-2GP
C991
C990
SCD1U16V2ZY-2GP
Right
091005-1
ACES-CON8-22-GP
USB1
USB_3-
USB_3+
USB_5-
USB_5+
091223-1
U80
U39
VI/O#1
VIO#6
GROUND
VBUS
VIO#3
VIO#4
USB_0+
USB_0-
USB_2+
USB_2-
+5VALW
+5VS
IP4223CZ6-GP
DY_EMI
Right
FILTER-4P-6-GP
EMI
L83
USB20_P3
USB20_N3
100307-1
L84
USB20_N5
USB20_P5
FILTER-79-GP-U
AFTE14P-GP AFTP107
AFTE14P-GP AFTP117
AFTE14P-GP AFTP118
AFTE14P-GP AFTP119
AFTE14P-GP AFTP120
AFTE14P-GP AFTP121
AFTE14P-GP AFTP130
AFTE14P-GP AFTP141
USB_VCCB
GND
Left
090803-1
USB2
SKT-USB-401-GP
22.10254.651
USB20_N0
USB20_P0
L82
091125-1
Q65
DMP2305U-7-GP
+3VS
+3VS_BT
C1002
SCD1U16V2ZY-2GP
R787
100KR2J-1-GP
C1001
C1000
SC1U10V3ZY-6GP
BT_OFF
R788
4K7R2J-2-GP
091124-1
100307-1
U78
IP4223CZ6-GP
EMI
L85
USB20_N2
USB20_P2
FILTER-79-GP-U
AFTE14P-GP AFTP91
AFTE14P-GP AFTP92
AFTE14P-GP AFTP93
AFTE14P-GP AFTP94
AFTE14P-GP AFTP95
AFTE14P-GP AFTP96
+3VS_BT
USB20_P11
BT_LED
USB20_N11
GND
BT1
JST-CON6-21-GP
BT_LED 57
USB20_N11 18
USB20_P11 18
D1030
PRTR5V0U2X-GP
<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
USB/BT/ESATA CONN
Size
A3
Document Number
PATEK
Rev
SA
Date:
Monday, March 15, 2010
Sheet
24
of
57





4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)

<Core Design>

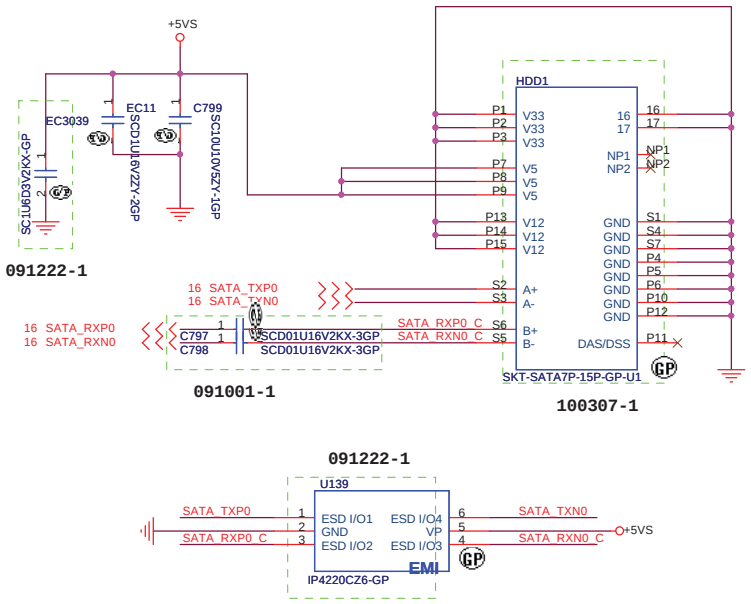
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CardReader RTS5138

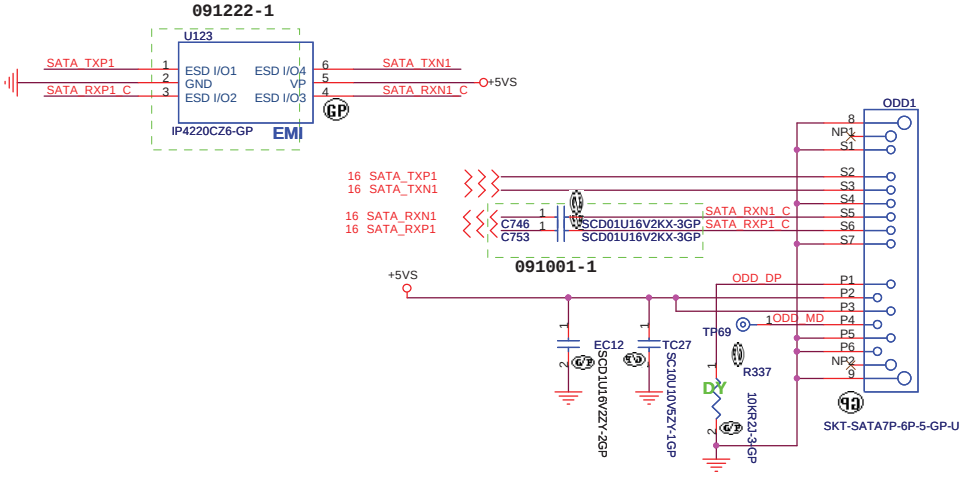
Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 25 of 57

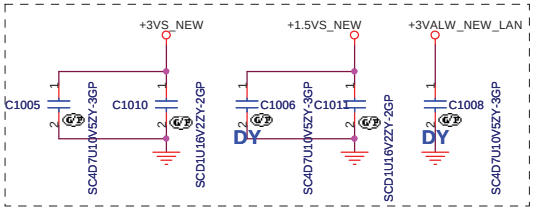
SATA HD Connector

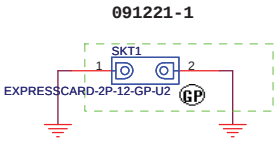


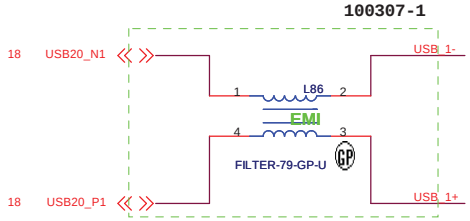
ODD Connector

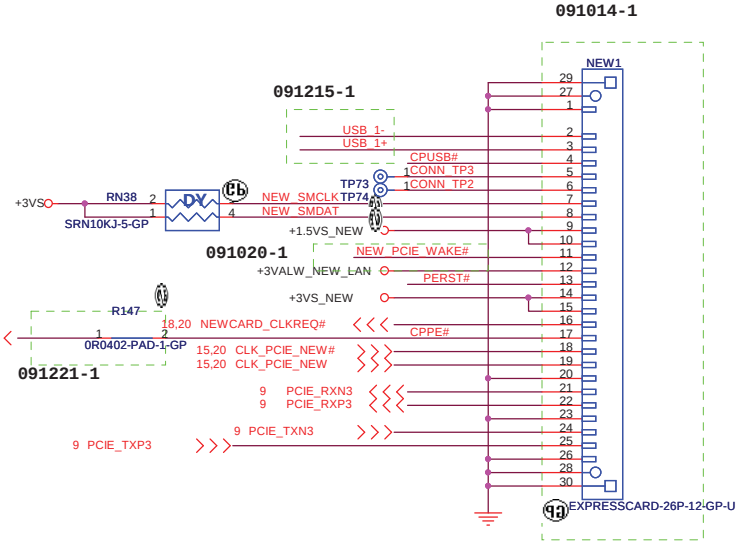


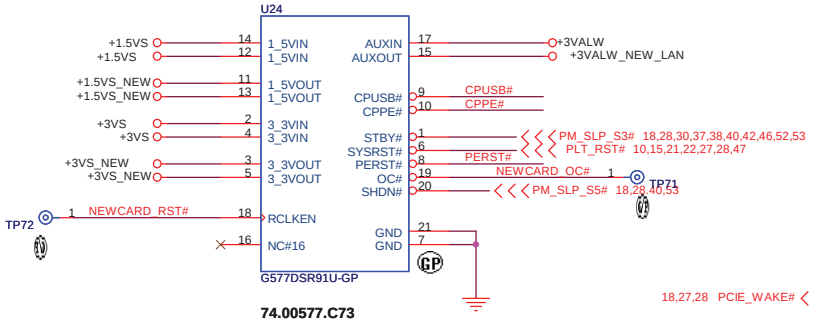
EXPRESS CARD Connector

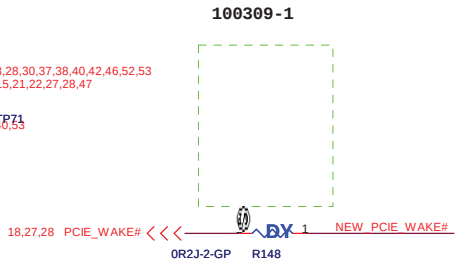


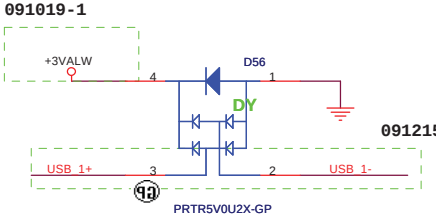












<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

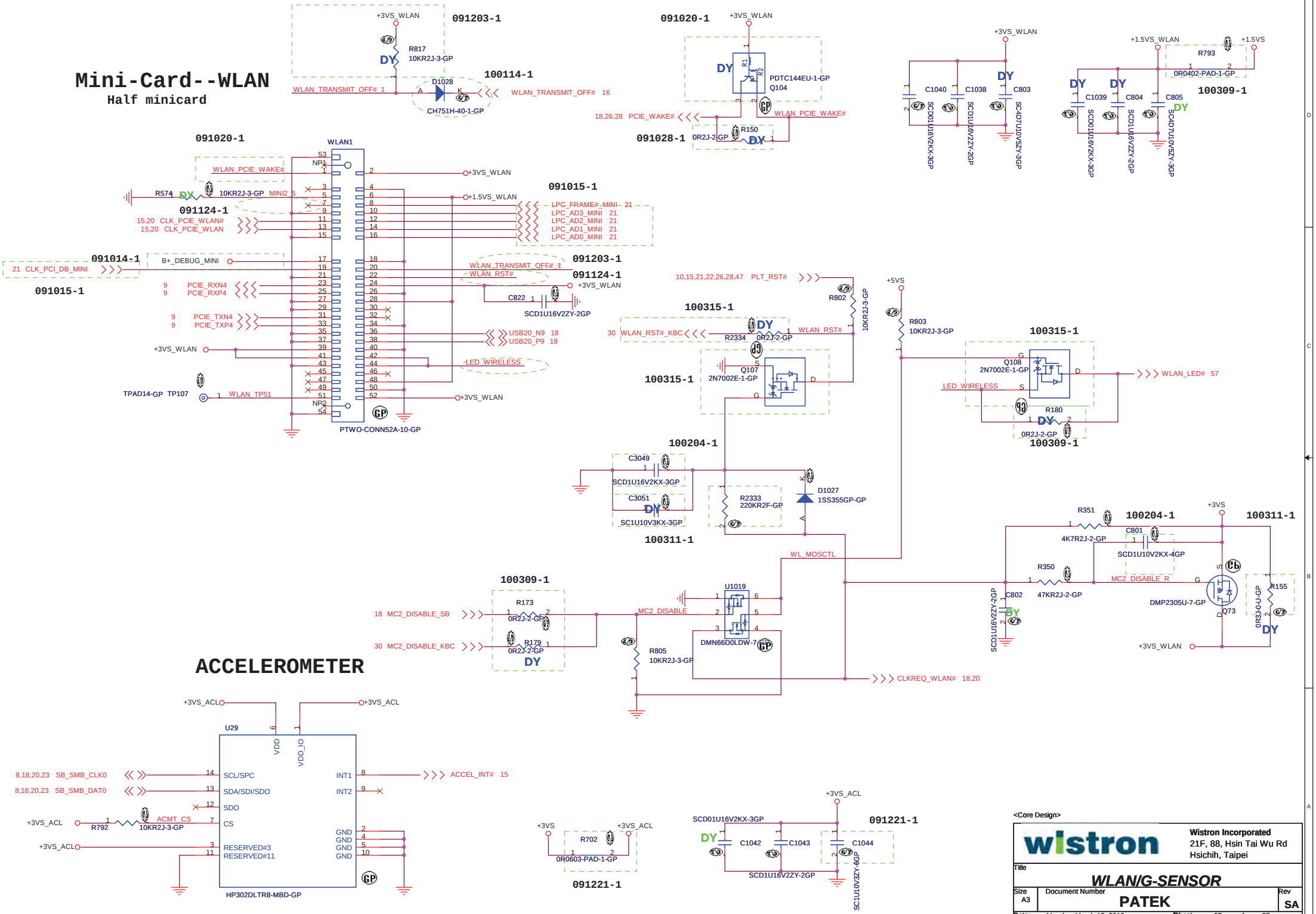
Title: HDD/ODD/NEW CARD

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 26 of 57

Mini-Card--WLAN

Half minicard



<Core Design>

wistron

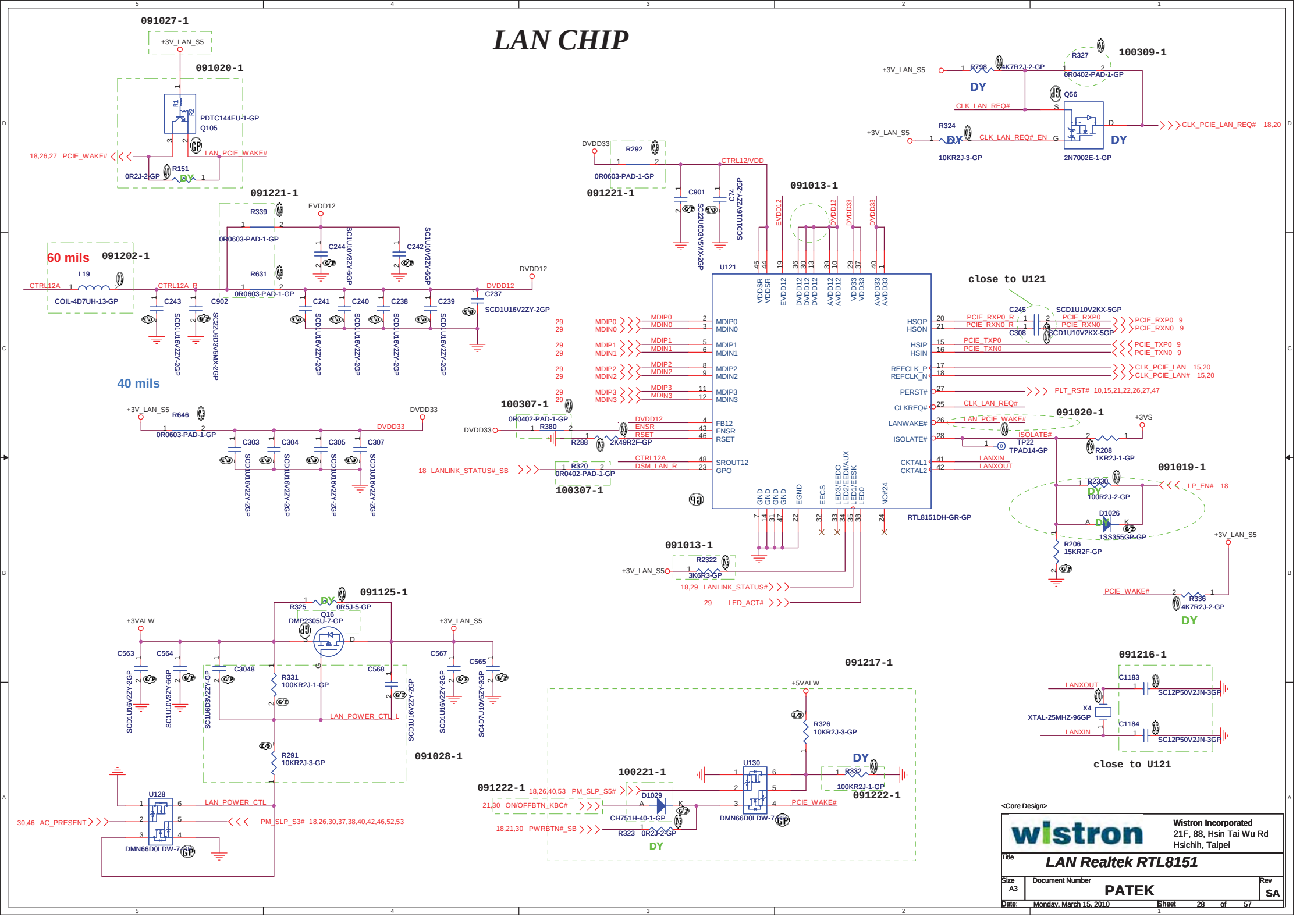
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: WLAN/G-SENSOR

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 27 of 57

LAN CHIP



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LAN Realtek RTL8151

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 28 of 57

close to XF1 pin1,4,7,10

VDD17
C1025 1 SCD01U16V2KX-3GP
C1029 1 SCD01U16V2KX-3GP
C1031 1 SCD01U16V2KX-3GP
C1023 1 SCD01U16V2KX-3GP

Transformer

091014-1
68.89240.30B
XFORM-24P-27-GP

28 MDIP0 → 12
VDD17 → 10
28 MDIN0 → 11
28 MDIP1 → 9
VDD17 → 7
28 MDIN1 → 8
28 MDIP2 → 6
VDD17 → 4
28 MDIN2 → 5
28 MDIP3 → 3
VDD17 → 1
28 MDIN3 → 2

13 MDO0+
14 MDO0-
15 MCT0 → C1215 1 SCD01U50V2KX-1GP → MCT0_R
16 MDO1+
17 MDO1-
18 MCT1 → C1216 1 SCD01U50V2KX-1GP → MCT1_R
19 MDO2+
20 MDO2-
21 MCT2 → C1217 1 SCD01U50V2KX-1GP → MCT2_R
22 MDO3+
23 MDO3-
24 MCT3 → C1218 1 SCD01U50V2KX-1GP → MCT3_R

XF1

MDO_C
C580 1 SC1KP2KV6KX-GP
RN71 SRN75J-1-GP
4 3 2 1 / 6 7 8

090930-1
091016-1

LAN Conn

28 LED_ACT# → LED_ACT#
18,28 LANLINK_STATUS# → LANLINK_STATUS#
C583 SCD1U16V2ZY-2GP DY
C584 SCD1U16V2ZY-2GP DY

091102-1

+3V_LAN_S5 → R335 470R2J-2-GP → LANLINK_STATUS# / LAN_LED_G
+3V_LAN_S5 → R334 470R2J-2-GP → LAN_LED_Y

RJ1 RJ45-8P-10-GP-U2
GREEN
ORANGE
YELLOW
A1 A2 A3 B1 B2
MDO0+ MDO0- MDO1+ MDO2+ MDO2- MDO1- MDO3+ MDO3- LED_ACT#
1 2 3 4 5 6 7 8 9 10

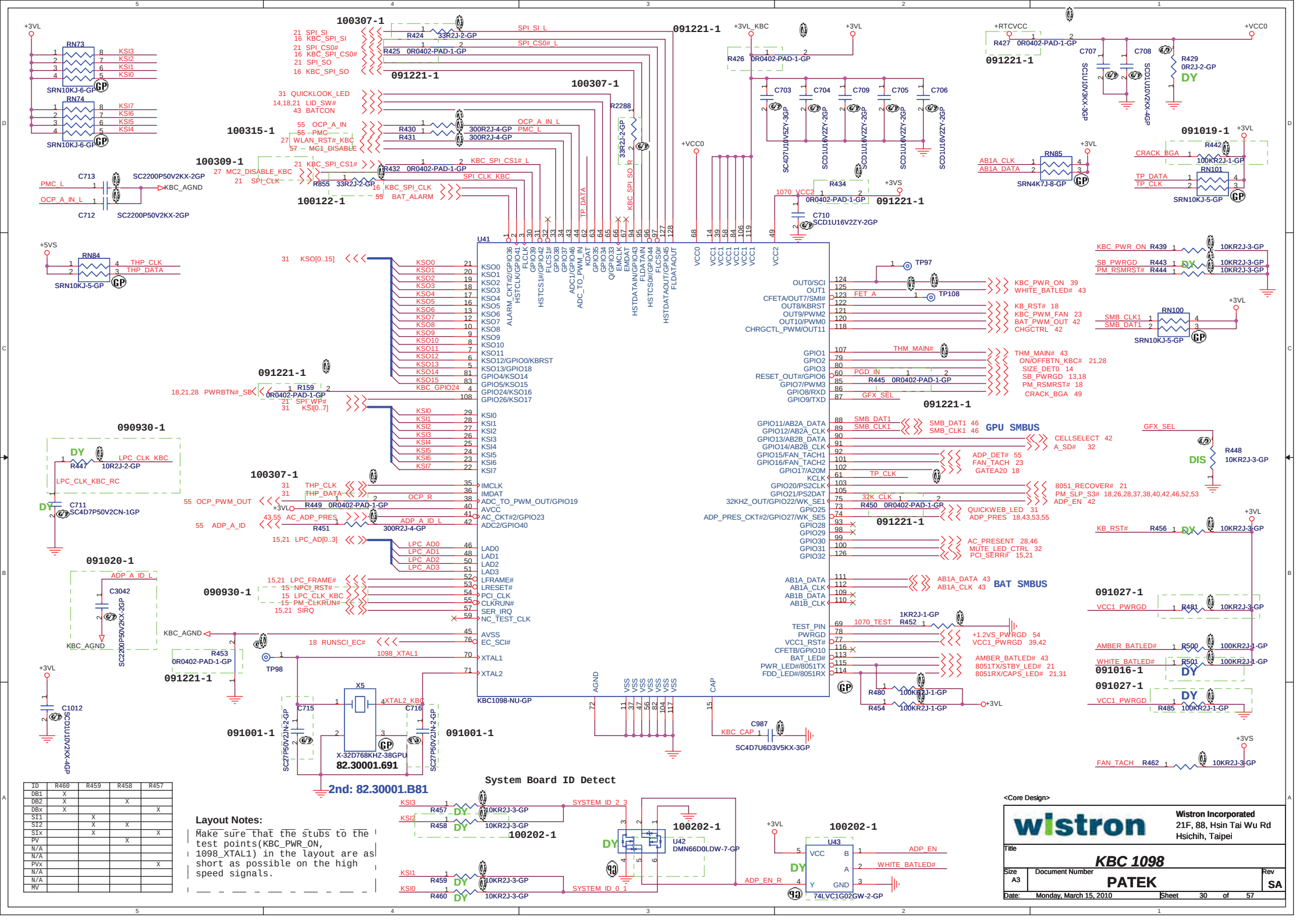
GREEN
YELLOW

Yellow
B1(+),B2(-)
Green
A1(-),A2(+)

<Core Design>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Magnetic & RJ45
Size: A3
Document Number: PATEK
Rev: SC
Date: Monday, March 15, 2010
Sheet 29 of 57



ID	R460	R459	R458	R457
DB1	X			
DB2	X		X	
DBx	X			X
SI1		X		
SI2		X	X	
SIx		X		X
PV			X	
N/A				
N/A				
PVx				X
N/A				
N/A				
MV				

Layout Notes:

Make sure that the stubs to the test points(KBC_PWR_ON, 1098_XTAL1) in the layout are as short as possible on the high speed signals.

<Core Design>

wistron

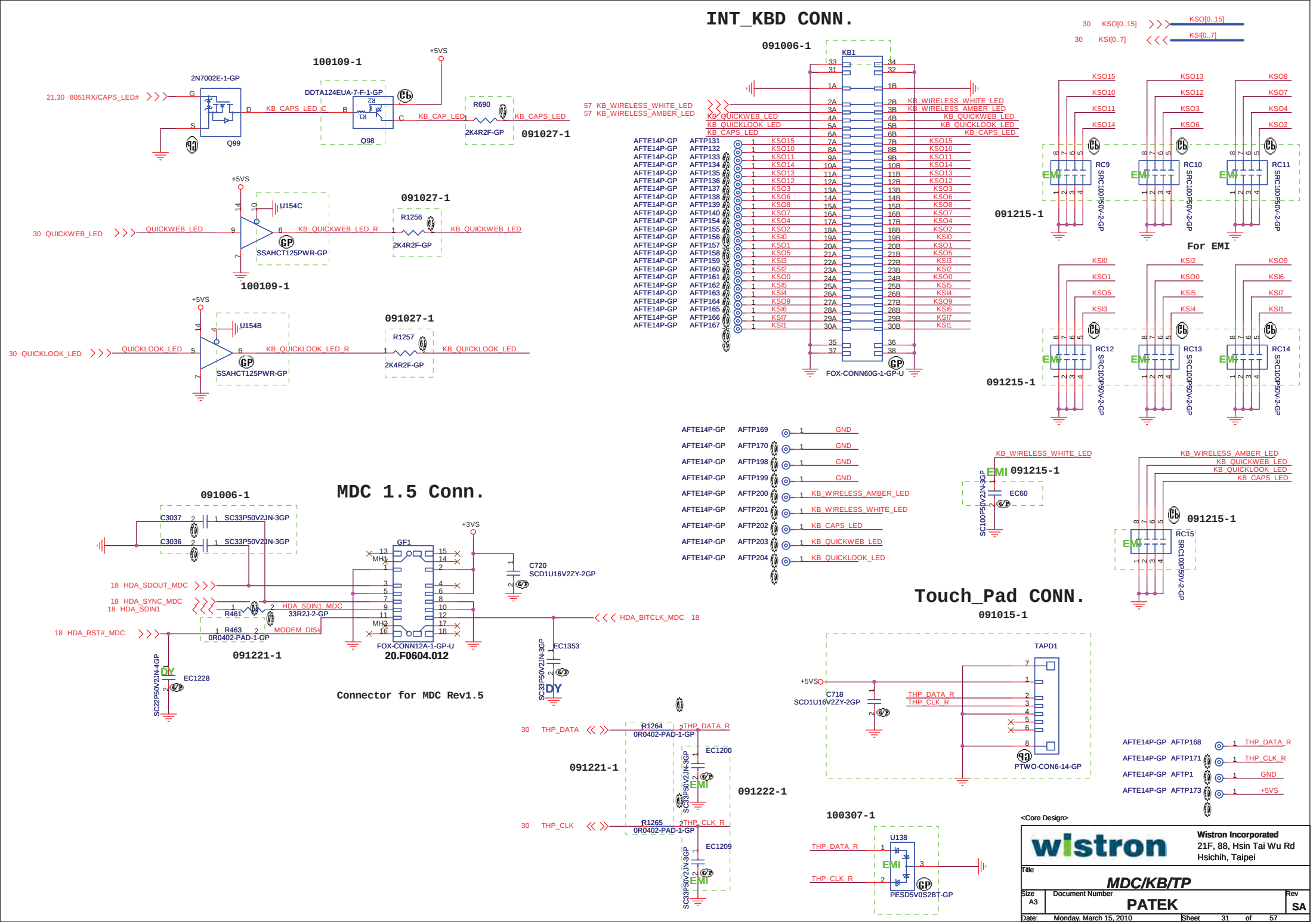
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: KBC 1098

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 30 of 57

INT_KBD CONN.



MDC 1.5 Conn.

Touch_Pad CONN.

091222-1

<Core Design>

wistron

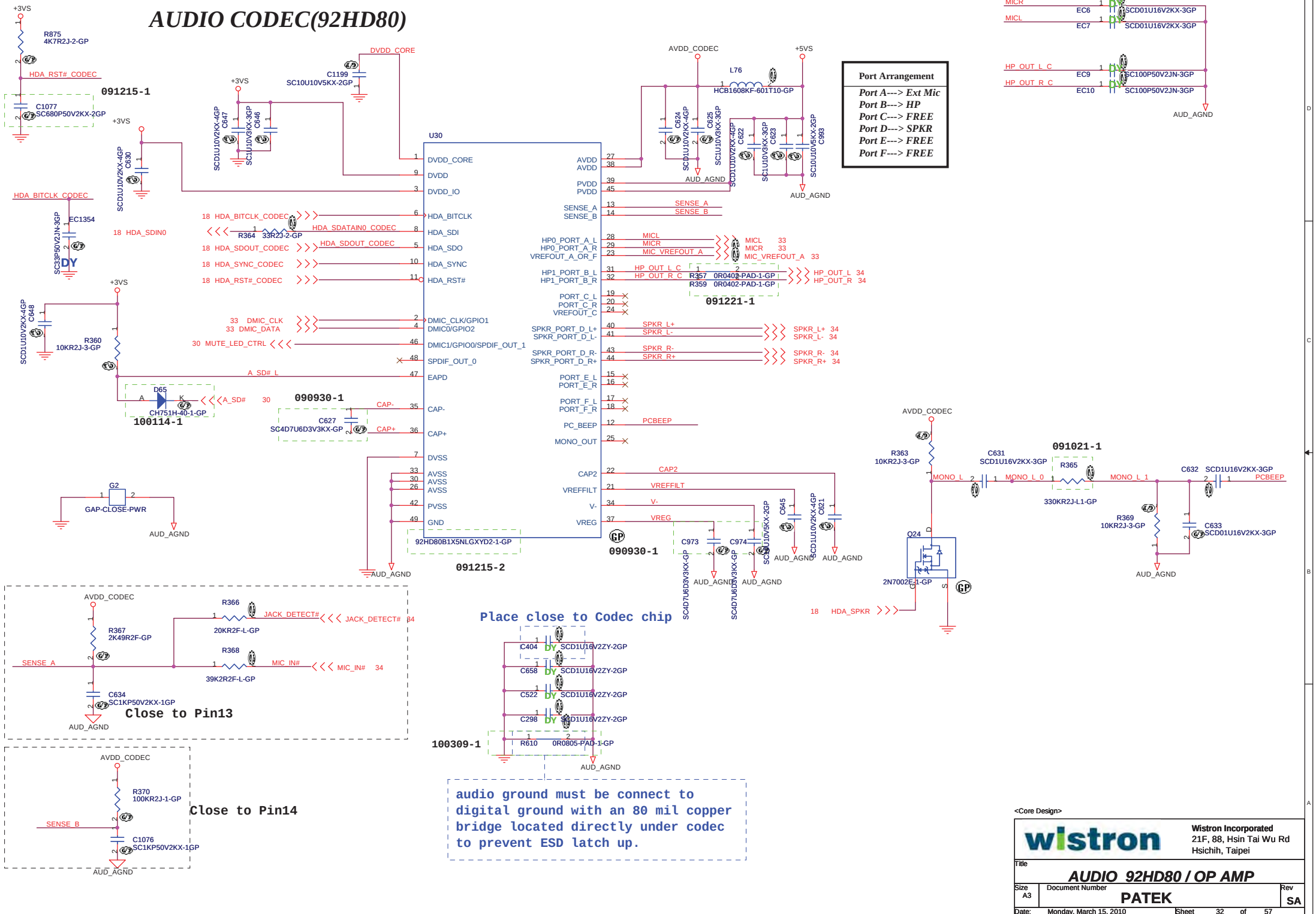
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: MDC/KB/TP

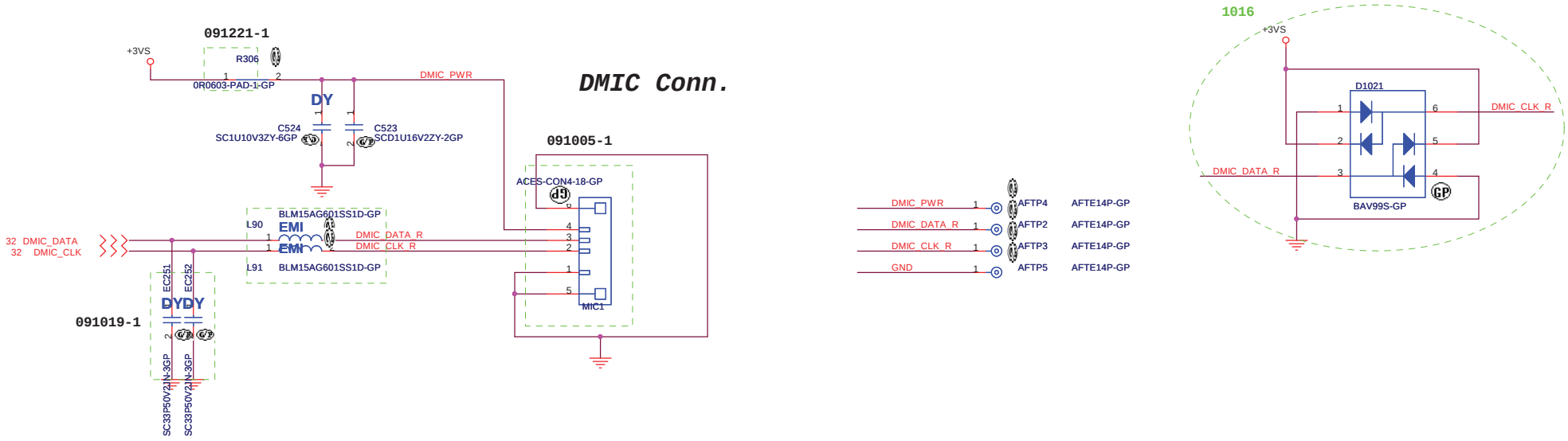
Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 31 of 57

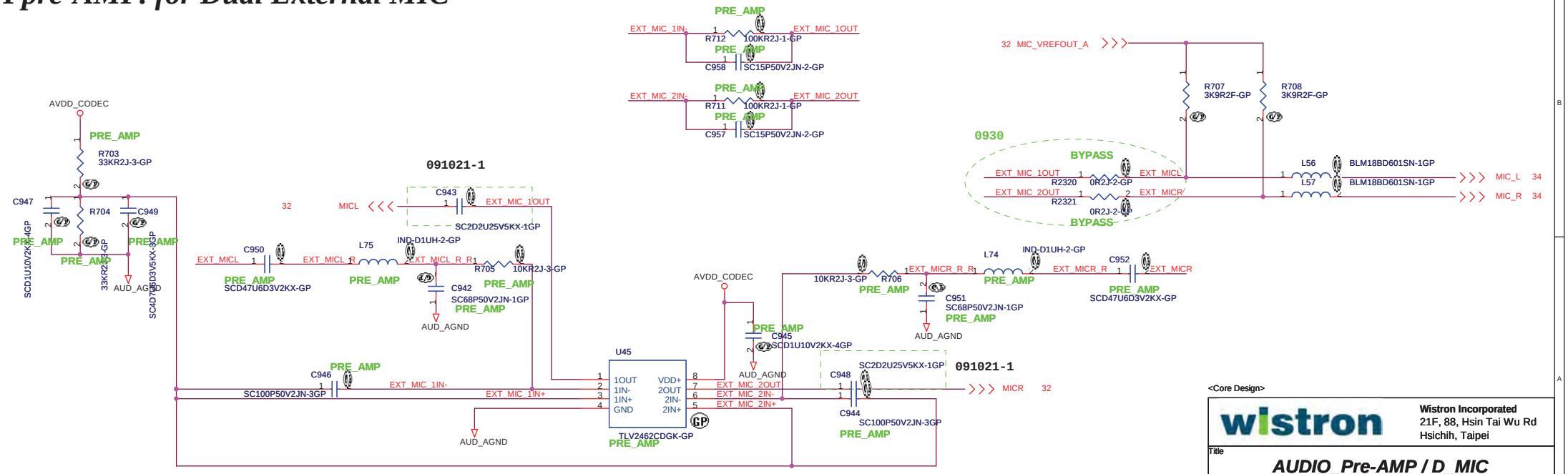
AUDIO CODEC(92HD80)



Dual Internal Digital MIC



Ppre-AMP. for Dual External MIC



<Core Design>

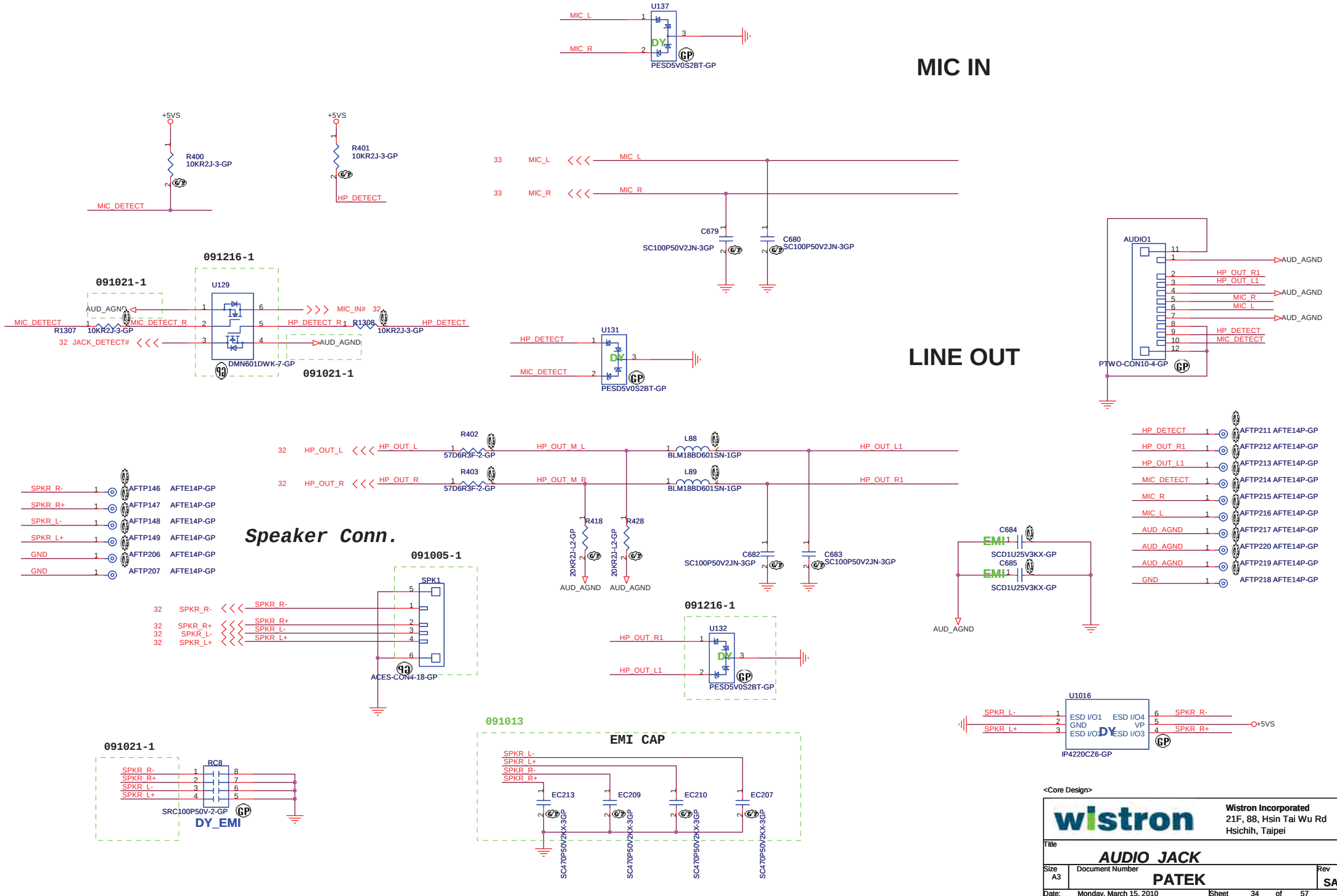
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

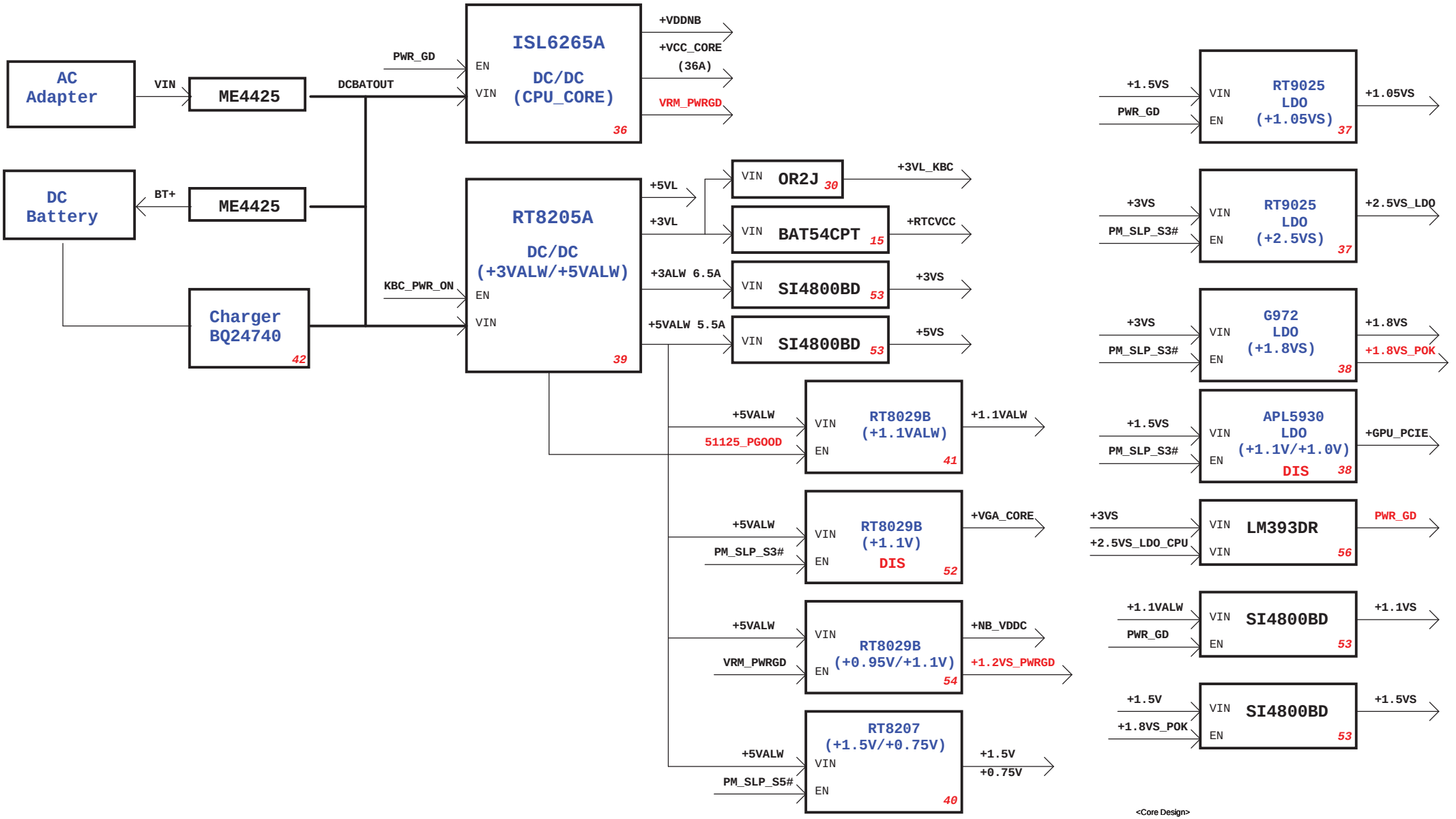
Title: AUDIO Pre-AMP / D MIC

Size	Document Number	Rev
A3	PATEK	SA

Date: Monday, March 15, 2010 Sheet 33 of 57


MIC IN
LINE OUT
Speaker Conn.
EMI CAP
DY_EMI
U137
PESD5V0S2BT-GP
R400
10KR2J-3-GP
R401
10KR2J-3-GP
MIC_DETECT
HP_DETECT
+5VS
091216-1
091021-1
U129
DMN601DWK-7-GP
AUD_AGND
MIC_DETECT_R
HP_DETECT_R
MIC_IN#
JACK_DETECT#
R1307
R1308
C679
C680
SC100P50V2JN-3GP
U131
AUDIO1
PTWO-CON10-4-GP
HP_OUT_L
HP_OUT_R
HP_OUT_M_L
HP_OUT_M_R
HP_OUT_L1
HP_OUT_R1
R402
R403
57D6R3F-2-GP
L88
L89
BLM18BD601SN-1GP
R418
R428
20KR2J-L2-GP
C682
C683
C684
C685
SCD1U25V3KX-GP
AFTP211 AFTE14P-GP
AFTP212 AFTE14P-GP
AFTP213 AFTE14P-GP
AFTP214 AFTE14P-GP
AFTP215 AFTE14P-GP
AFTP216 AFTE14P-GP
AFTP217 AFTE14P-GP
AFTP220 AFTE14P-GP
AFTP219 AFTE14P-GP
AFTP218 AFTE14P-GP
SPKR_R-
SPKR_R+
SPKR_L-
SPKR_L+
GND
AFTP146 AFTE14P-GP
AFTP147 AFTE14P-GP
AFTP148 AFTE14P-GP
AFTP149 AFTE14P-GP
AFTP206 AFTE14P-GP
AFTP207 AFTE14P-GP
091005-1
SPK1
ACES-CON4-18-GP
U132
U1016
IP4220CZ6-GP
ESD I/O1
ESD I/O2
ESD I/O3
ESD I/O4
GND
VP
091013
EC213
EC209
EC210
EC207
SC470P50V2KX-3GP
RC8
SRC100P50V-2-GP
<Core Design>
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
AUDIO JACK
Size
A3
Document Number
PATEK
Rev
SA
Date:
Monday, March 15, 2010
Sheet
34
of
57

Patek DIS POWER Block Diagram



<Core Design>

wistron

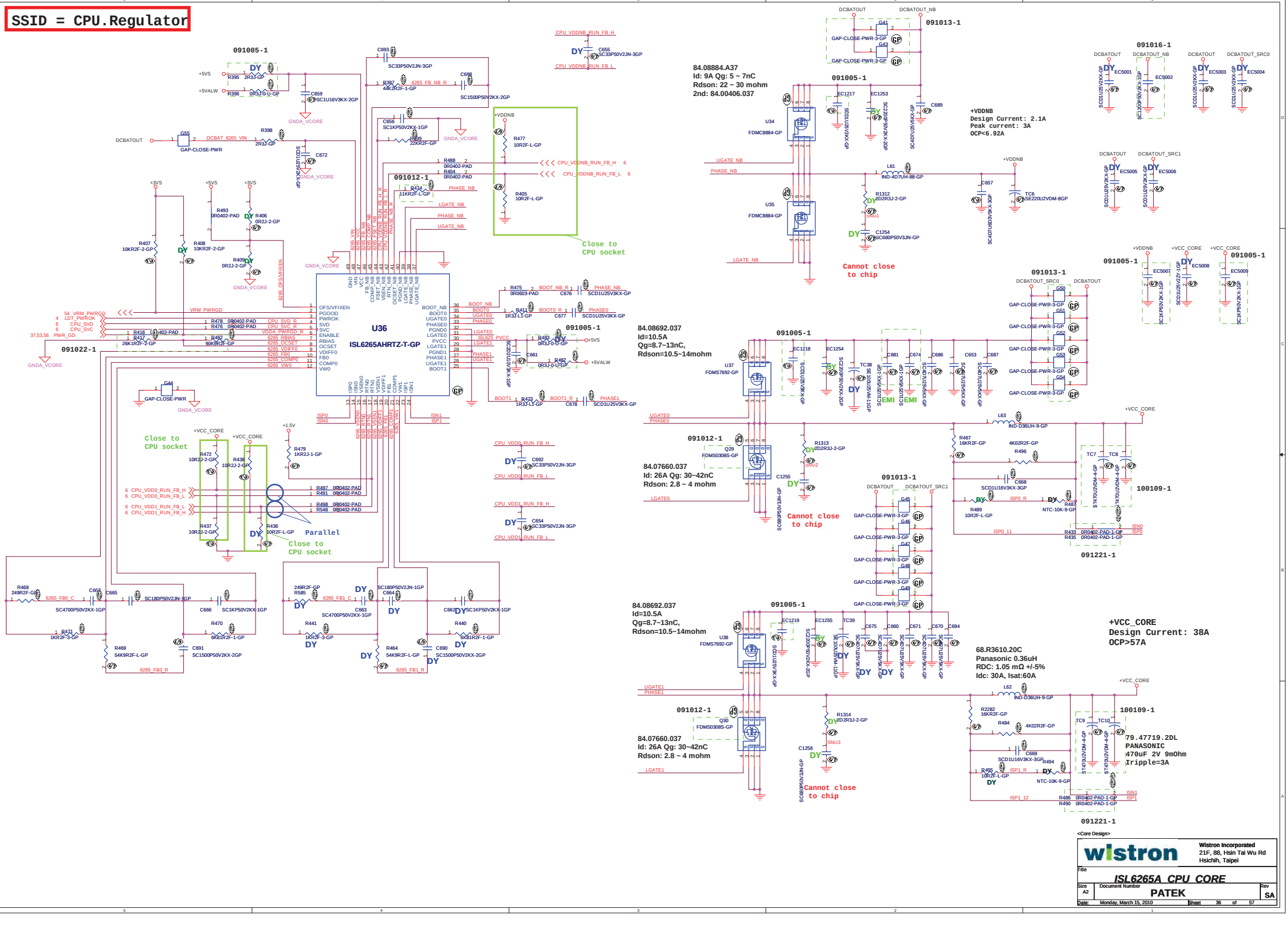
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

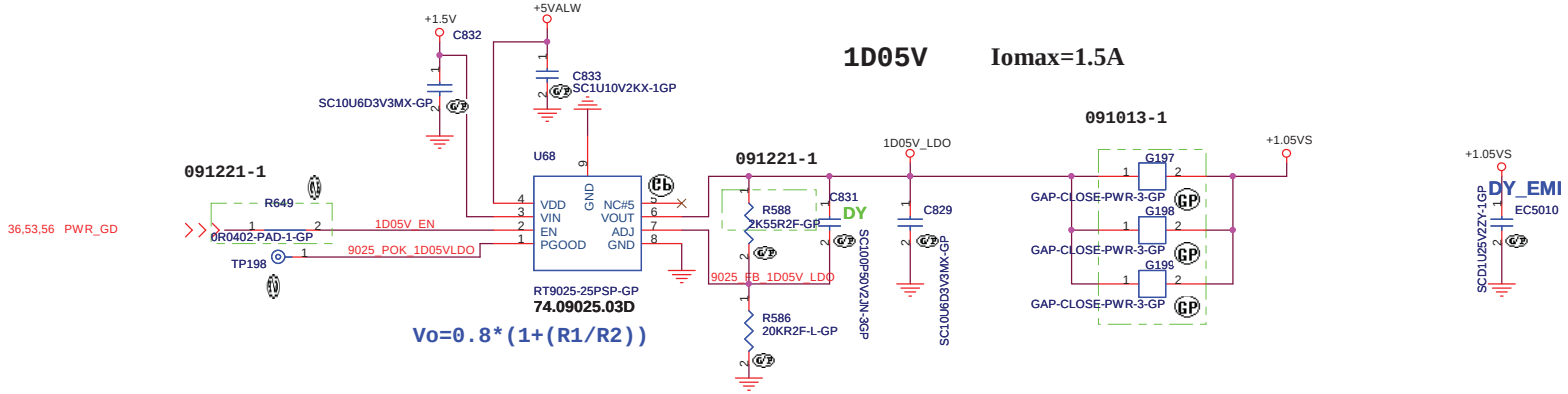
Title: *Power Block Diagram*

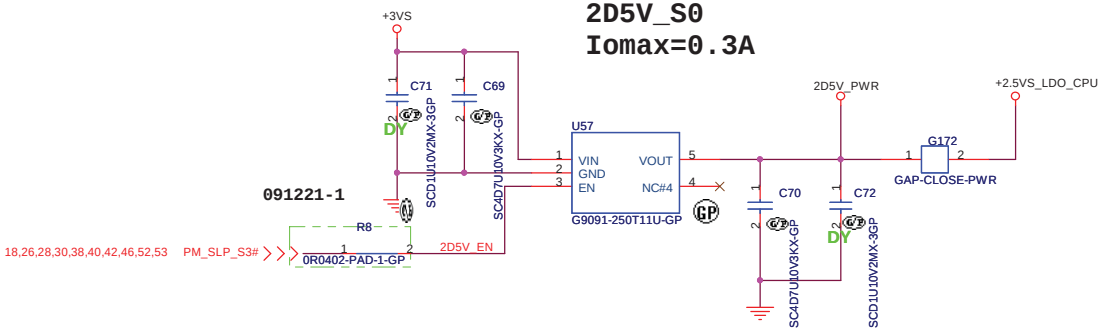
Size	Document Number	Rev
A3	PATEK	SA

Date: Monday, March 15, 2010 Sheet 35 of 57

SSID = CPU.Regulator







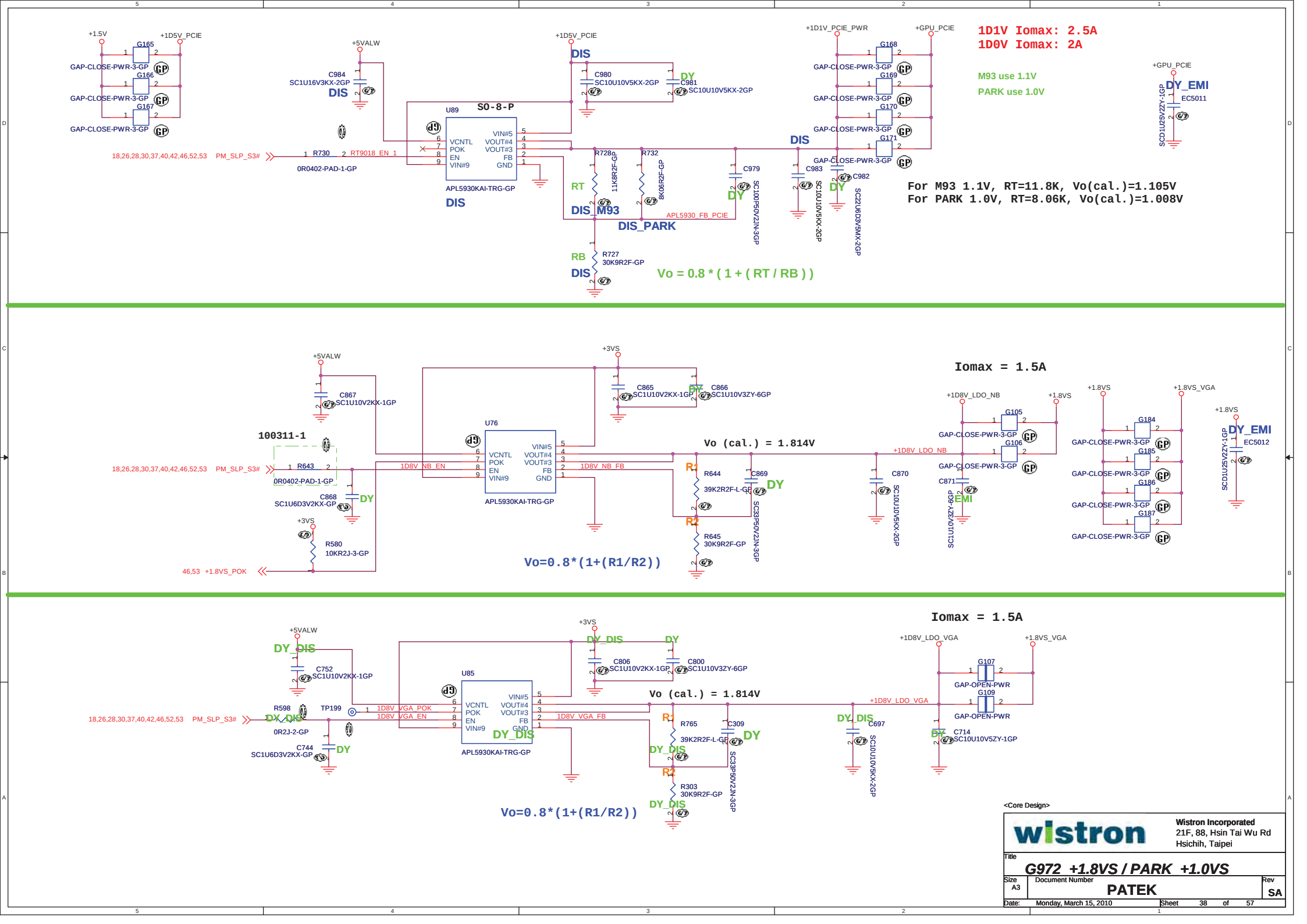
<Core Design>

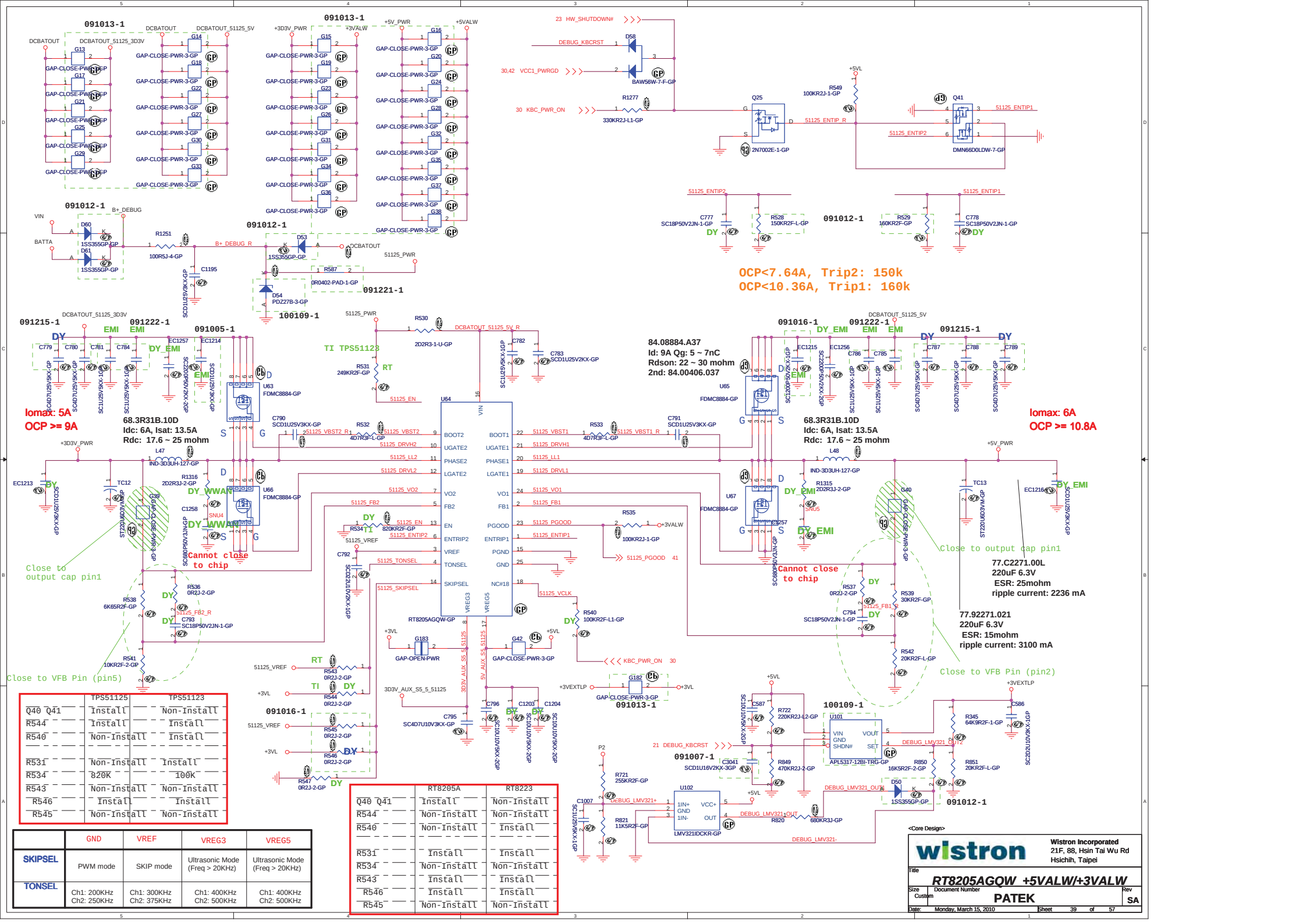
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RT8209B +1.05VS / +2.5VS

Size	Document Number	Rev
A3	PATEK	SA

Date: Monday, March 15, 2010 Sheet 37 of 57


1D1V Iomax: 2.5A
1D0V Iomax: 2A
M93 use 1.1V
PARK use 1.0V
For M93 1.1V, RT=11.8K, Vo(cal.)=1.105V
For PARK 1.0V, RT=8.06K, Vo(cal.)=1.008V
Vo = 0.8 * (1 + (RT / RB))
U89
SO-8-P
APL5930KAI-TRG-GP
DIS
DIS_M93
DIS_PARK
DY
DY_EMI
Iomax = 1.5A
Vo (cal.) = 1.814V
Vo=0.8*(1+(R1/R2))
U76
100311-1
U85
DY_DIS
<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
G972 +1.8VS / PARK +1.0VS
Size A3
Document Number
PATEK
Rev SA
Date: Monday, March 15, 2010
Sheet 38 of 57

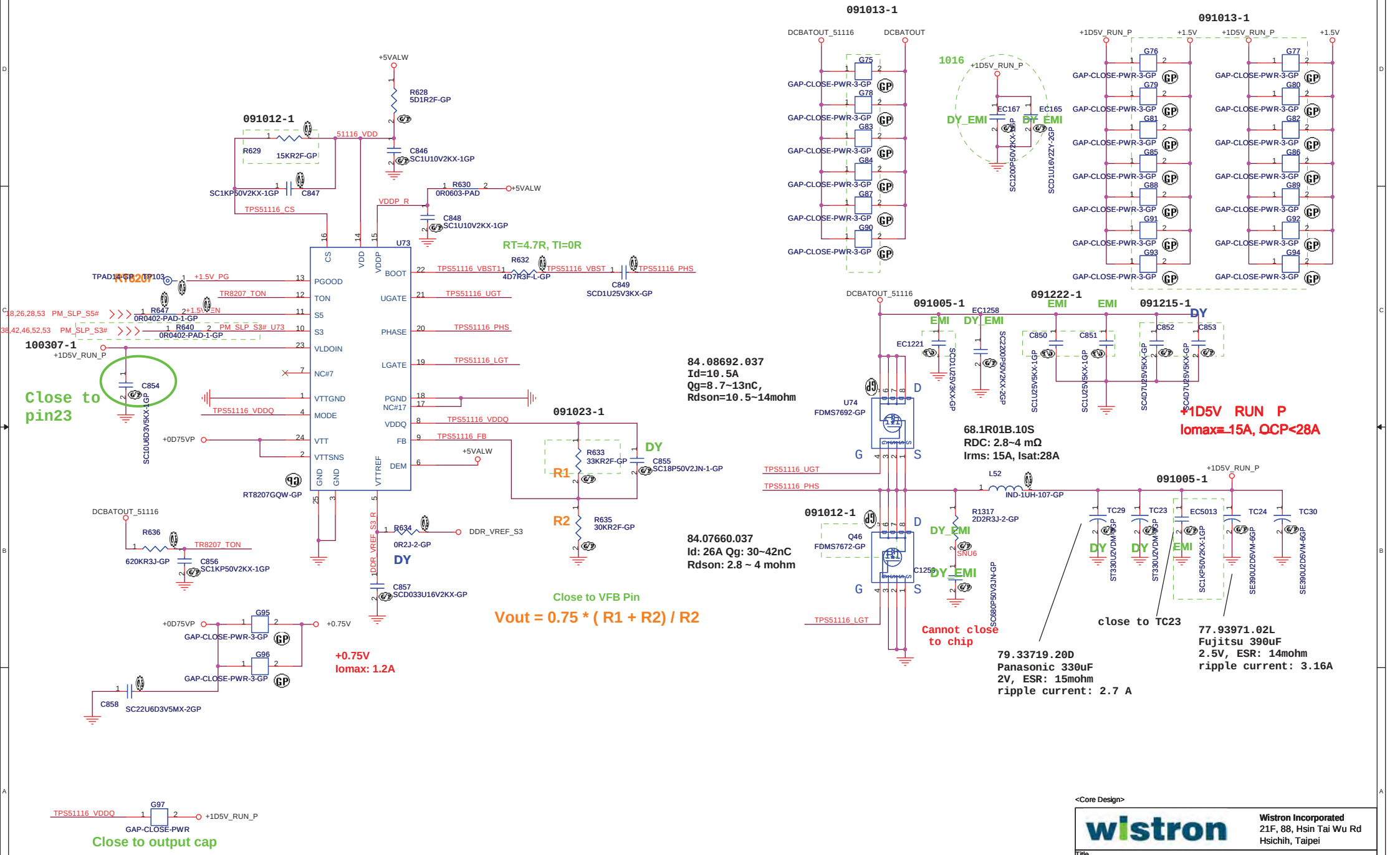


	TPS51125	TPS51123
Q40 Q41	Install	Non-Install
R544	Install	Install
R540	Non-Install	Install
R531	Non-Install	Install
R534	820K	100K
R543	Non-Install	Non-Install
R546	Install	Install
R545	Non-Install	Non-Install

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM mode	SKIP mode	Ultrasonic Mode (Freq > 20KHz)	Ultrasonic Mode (Freq > 20KHz)
TONSEL	Ch1: 200KHz Ch2: 250KHz	Ch1: 300KHz Ch2: 375KHz	Ch1: 400KHz Ch2: 500KHz	Ch1: 400KHz Ch2: 500KHz

	RT8205A	RT8223
Q40 Q41	Install	Non-Install
R544	Non-Install	Non-Install
R540	Non-Install	Install
R531	Install	Install
R534	Non-Install	Non-Install
R543	Install	Install
R546	Install	Install
R545	Non-Install	Non-Install

RT8207 for 1D5V and 0D75V



<Core Design>

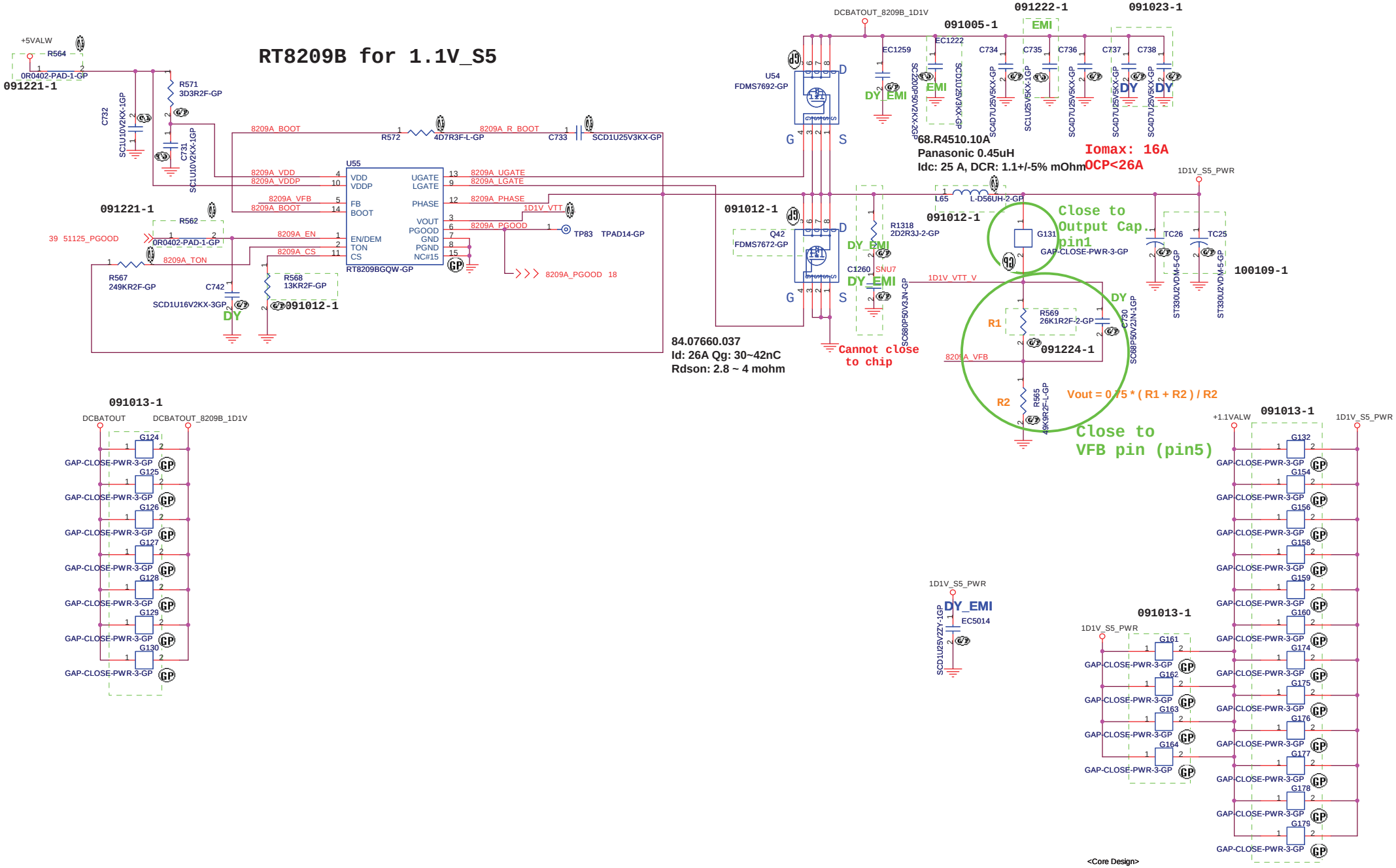
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RT8209B +1.5V / +0.75V

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 40 of 57

RT8209B for 1.1V_S5



<Core Design>

wistron

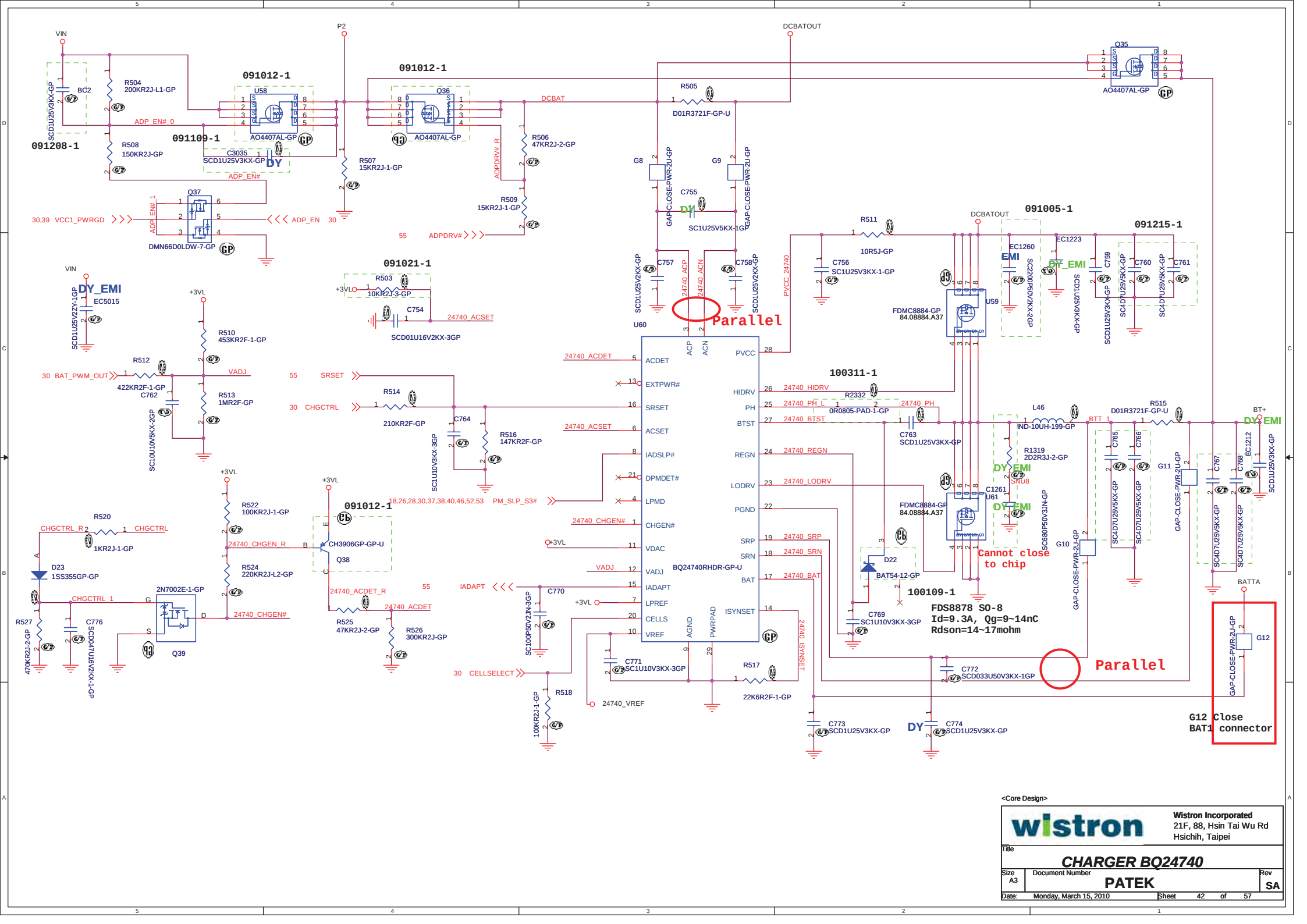
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

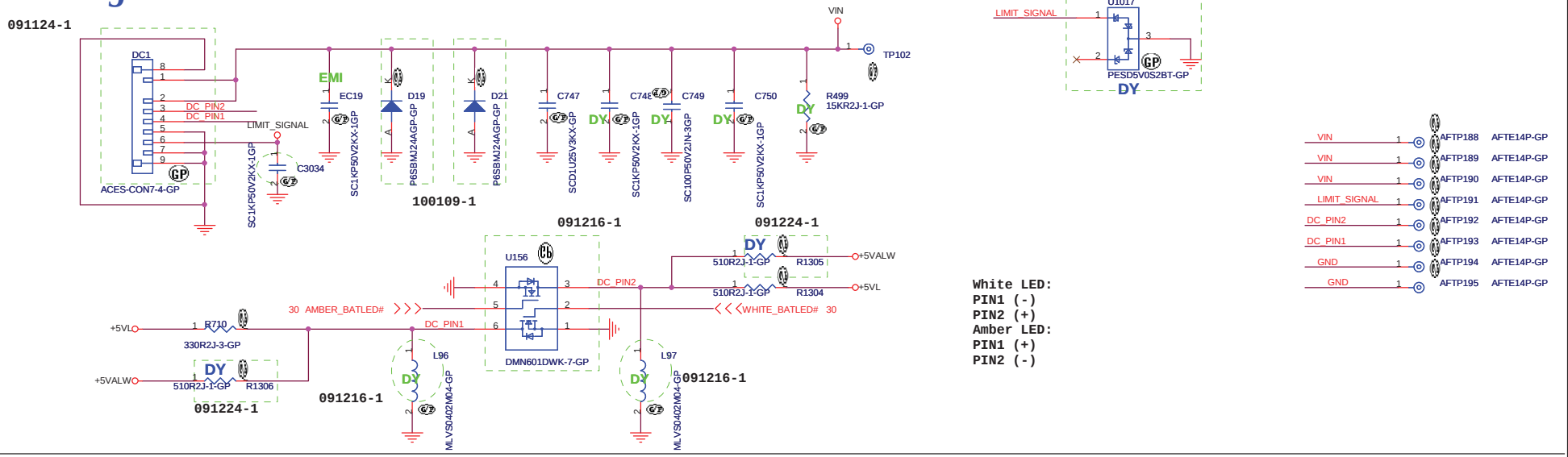
RT8209B +1.1VALW

Size	Document Number	Rev
A3	PATEK	SA

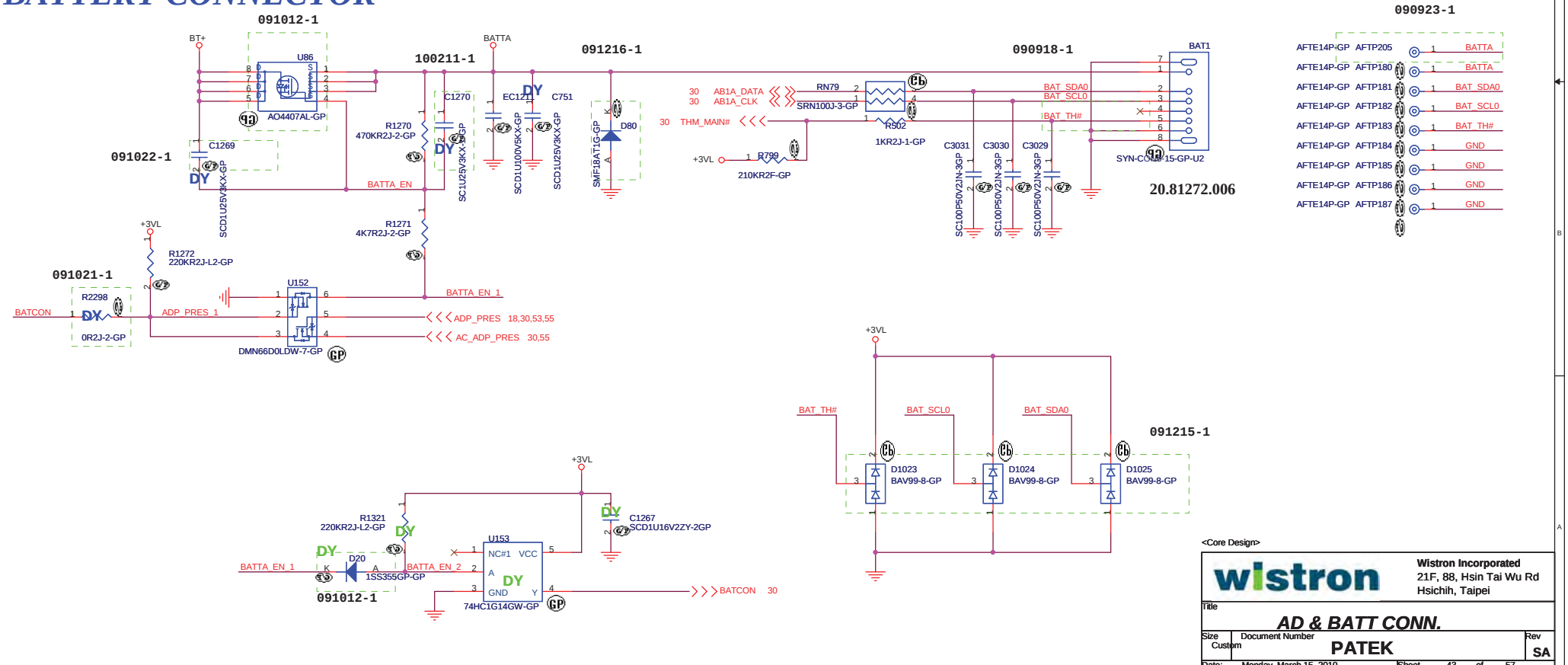
Date: Monday, March 15, 2010 Sheet 41 of 57


VIN
P2
DCBATOUT
091012-1
091208-1
091109-1
091021-1
091005-1
091215-1
100311-1
100109-1
R504 200KR2J-L1-GP
R505 D01R3721F-GP-U
R506 47KR2J-2-GP
R507 15KR2J-1-GP
R508 150KR2J-GP
R509 15KR2J-1-GP
R510 453KR2F-1-GP
R511 10R5J-GP
R512 422KR2F-1-GP
R513 1MR2F-GP
R514 210KR2F-GP
R515 D01R3721F-GP-U
R516 147KR2F-GP
R517 22K6R2F-1-GP
R518 100KR2J-1-GP
R520 1KR2J-1-GP
R522 100KR2J-1-GP
R524 220KR2J-L2-GP
R525 47KR2J-2-GP
R526 300KR2J-GP
R527 470KR2J-2-GP
R503 10KR2J-3-GP
R1319 2D2R3J-2-GP
R2332 0R0805-PAD-1-GP
C3035 SCD1U25V3KX-GP
C754 SCD01U16V2KX-3GP
C755 SC1U25V5KX-1GP
C756 SC1U25V3KX-1-GP
C757 SCD1U25V2KX-GP
C758 SCD1U25V2KX-GP
C759 SCD1U25V3KX-GP
C760 SC4D7U25V5KX-GP
C761 SC4D7U25V5KX-GP
C762 SC10U10V5KX-2GP
C763 SCD1U25V3KX-GP
C764 SC1U10V3KX-3GP
C765 SC4D7U25V5KX-GP
C766 SC4D7U25V5KX-GP
C767 SC4D7U25V5KX-GP
C768 SC4D7U25V5KX-GP
C769 SC1U10V3KX-3GP
C770 SC100P50V2JN-3GP
C771 SC1U10V3KX-3GP
C772 SCD033U50V3KX-1GP
C773 SCD1U25V3KX-GP
C774 SCD1U25V3KX-GP
C776 SCD047U16V2KX-1GP
EC1212 SCD1U25V3KX-GP
EC1223 SCD1U25V3KX-GP
EC1260 SC2200P50V2KX-2GP
EC5015 SCD1U25V2ZY-1GP
BC2 SCD1U25V3KX-GP
U58 AO4407AL-GP
Q36 AO4407AL-GP
Q35 AO4407AL-GP
Q37 DMN66D0LDW-7-GP
Q38 CH3906GP-GP-U
Q39 2N7002E-1-GP
D22 BAT54-12-GP
D23 1SS355GP-GP
U59 FDMC8884-GP 84.08884.A37
U61 FDMC8884-GP 84.08884.A37
U60 BQ24740RHDR-GP-U
L46 IND-10UH-199-GP
SNU8 SC680P50V3JN-GP
G8 GAP-CLOSE-PWR-2U-GP
G9 GAP-CLOSE-PWR-2U-GP
G10 GAP-CLOSE-PWR-2U-GP
G11 GAP-CLOSE-PWR-2U-GP
G12 GAP-CLOSE-PWR-2U-GP
ACDET
EXTPWR#
SRSET
ACSET
IADSLP#
DPMDET#
LPMD
CHGEN#
VDAC
VADJ
IADAPT
LPREF
CELLS
VREF
AGND
PWRPAD
ISYNSET
ACP
ACN
PVCC
HIDRV
PH
BTST
REGN
LODRV
PGND
SRP
SRN
BAT
24740_ACDET
24740_CHGEN#
24740_ACSET
24740_ACDET_R
24740_CHGEN_R
24740_VREF
24740_ISYNSET
24740_HIDRV
24740_PH
24740_BTST
24740_REGN
24740_LODRV
24740_SRP
24740_SRN
24740_BAT
PVCC_24740
ADP_EN# 0
ADP_EN#
ADP_EN
ADP_EN# 1
ADPDRV#
ADPDRV# R
VCC1_PWRGD
BAT_PWM_OUT
CHGCTRL
CHGCTRL_R
CHGCTRL_1
SRSET
VADJ
IADAPT
CELLSELECT
PM_SLP_S3#
BT+
BATTA
BTT_1
DY
DY_EMI
EMI
Parallel
Cannot close to chip
FDS8878 SO-8
Id=9.3A, Qg=9~14nC
Rdson=14~17mohm
G12 Close BAT1 connector
<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
CHARGER BQ24740
Size A3
Document Number
PATEK
Rev SA
Date: Monday, March 15, 2010
Sheet 42 of 57

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<core_design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AD & BATT CONN.

Size: Custom | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 43 of 57
</core_design>

HOLE

091016-1

H18 HOLE335R115-GP

H26 HOLE335R115-GP

H27 HOLE335R115-GP

H28 HOLE335R115-GP

091207-1

H16 HOLE335R115-GP

H41 HOLE256R115-GP

H7 HOLE276R178-GP

H8 HOLE276R178-GP

H9 HOLE276R178-GP

H10 HOLE276R178-GP

H1013 HOLE276R178-GP

H1014 HOLE276R178-GP

H11 HOLE335R115-GP

H12 HOLE335R115-GP

StandOff

H23 STF217R73H123-GP

H24 STF217R73H123-GP

H2 STF217R113H221-GP

H3 STF217R113H221-GP

100112-1

H4 STF217R113H221-GP WWAN

H5 STF217R113H221-GP WWAN

H19 STF217R113H123-1-GP

H20 STF217R113H123-1-GP

Spring

091107-1

SPR1 SPRING-62-GP DY_EMI

SPR2 SPRING-57-GP DY_EMI

091208-1

SPR4 SPRING-62-GP DY_EMI

091016-1

SPR3 SPRING-89-GP EMI

SPR5 SPRING-89-GP EMI

SPR6 SPRING-89-GP EMI

091109-1

SPR8 SPRING-70-GP DY EMI

D1018 MLVS0603K20-GP DY EMI

P/N: ZZ.0HOLE.XXX

Ground PAD

H29 HOLE

H30 HOLE

H31 HOLE

H32 HOLE

H33 HOLE

H34 HOLE

091016-1

H6 HOLE

H21 HOLE

H22 HOLE

091022-1

H39 HOLE

H40 HOLE

EMI CAP

+5VS_CRT EC1263 SCD1U16V2ZY-2GP DY

+5VS_CRT EC1264 SCD1U16V2ZY-2GP DY

+3VALW EC1268 SCD1U16V2ZY-2GP DY

+3VALW EC1269 SCD1U16V2ZY-2GP DY

+3VALW EC1270 SCD1U16V2ZY-2GP EMI

+3VALW EC1271 SCD1U16V2ZY-2GP DY

+3VALW EC1272 SCD1U16V2ZY-2GP EMI

+3VALW EC1273 SCD1U16V2ZY-2GP EMI

+3VALW EC1274 SCD1U16V2ZY-2GP EMI

100307-1

+3VS EC1278 SCD1U16V2ZY-2GP DY

+3VS EC1279 SCD1U16V2ZY-2GP DY

+3VS EC1280 SCD1U16V2ZY-2GP DY

+3VS EC1281 SCD1U16V2ZY-2GP DY

+3VS EC1282 SCD1U16V2ZY-2GP DY

+3VS EC1283 SCD1U16V2ZY-2GP DY

DCBATOUT EC1310 SCD1U25V2ZY-1GP DY

DCBATOUT EC1311 SCD1U25V2ZY-1GP DY

DCBATOUT EC1312 SCD1U25V2ZY-1GP DY

+5VALW EC1288 SCD1U16V2ZY-2GP DY

+5VALW EC1289 SCD1U16V2ZY-2GP DY

+5VALW EC1290 SCD1U16V2ZY-2GP DY

+5VALW EC1291 SCD1U16V2ZY-2GP DY

+5VALW EC1293 SCD1U16V2ZY-2GP DY

DCBATOUT EC1313 SCD1U25V2ZY-1GP DY

DCBATOUT EC1314 SCD1U25V2ZY-1GP DY

DCBATOUT EC1315 SCD1U25V2ZY-1GP DY

091015-1

+1.5V EC1336 SC1KP50V2KX-1GP DY

+1.5V EC1337 SC1KP50V2KX-1GP DY

+1.5V EC1338 SC1KP50V2KX-1GP DY

+1.5V EC1339 SC1KP50V2KX-1GP DY

+1.5V EC1340 SC1KP50V2KX-1GP DY

+1.5V EC1341 SC1KP50V2KX-1GP DY

+1.5V EC1342 SC1KP50V2KX-1GP DY

+1.5V EC1343 SC1KP50V2KX-1GP DY

+1.5V EC1344 SC1KP50V2KX-1GP DY

091215-1

091019-1

+3VS EC1365 SC1KP50V2KX-1GP DY

+3VS EC1366 SC1KP50V2KX-1GP DY

+3VS EC1367 SC1KP50V2KX-1GP DY

+3VS EC1368 SC1KP50V2KX-1GP DY

DCBATOUT EC1319 SCD1U25V2ZY-1GP DY

DCBATOUT EC1320 SCD1U25V2ZY-1GP DY

DCBATOUT EC1321 SCD1U25V2ZY-1GP DY

+1.5V EC1299 SCD1U16V2ZY-2GP DY

+1.5V EC1300 SCD1U16V2ZY-2GP DY

+1.5V EC1301 SCD1U16V2ZY-2GP DY

+1.5V EC1302 SCD1U16V2ZY-2GP DY

+1.5V EC1303 SCD1U16V2ZY-2GP DY

+1.5V EC1304 SCD1U16V2ZY-2GP DY

DCBATOUT EC1318 SCD1U25V2ZY-1GP DY

DCBATOUT EC1322 SCD1U25V2ZY-1GP DY

DCBATOUT EC1323 SCD1U25V2ZY-1GP DY

DCBATOUT EC1324 SCD1U25V2ZY-1GP DY

091005-1

+VDDNB EC1307 SC1KP50V2KX-1GP EMI

+VDDNB EC1308 SC1KP50V2KX-1GP EMI

+VDDNB EC1309 SCD1U16V2ZY-2GP DY

<Core Design>

wistron

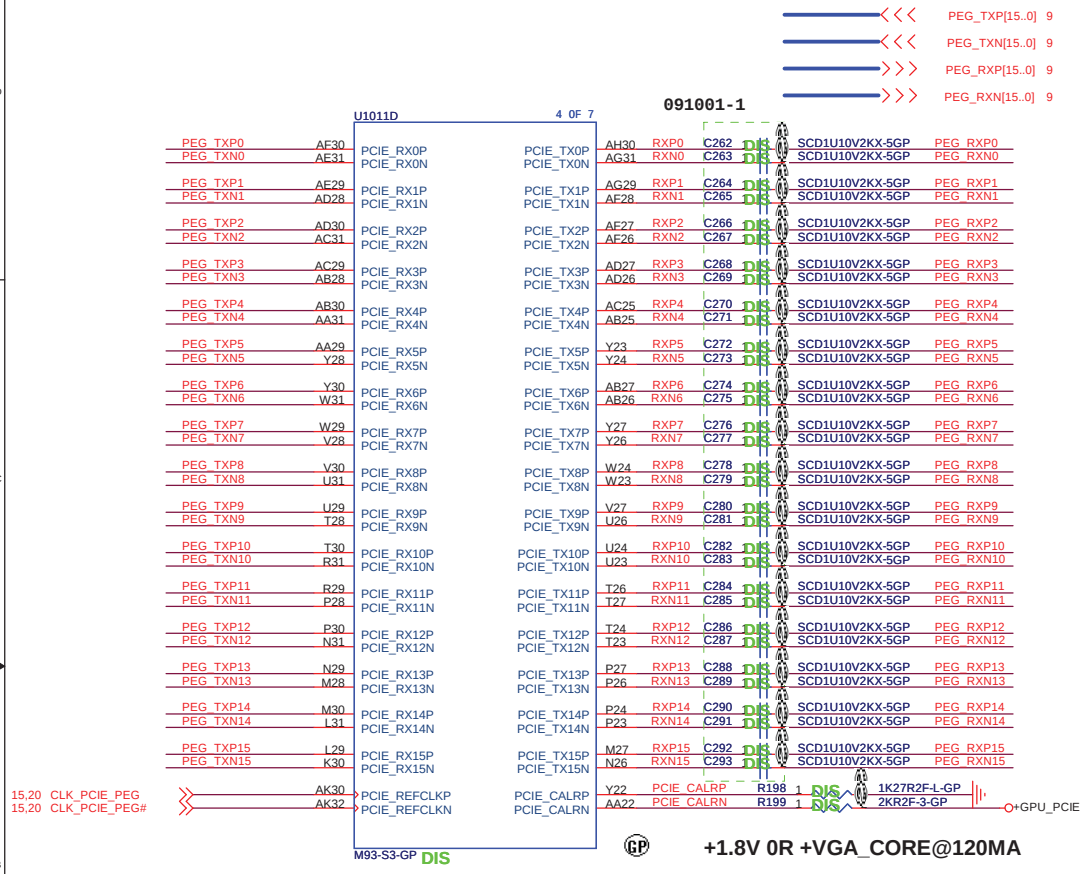
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HOLE

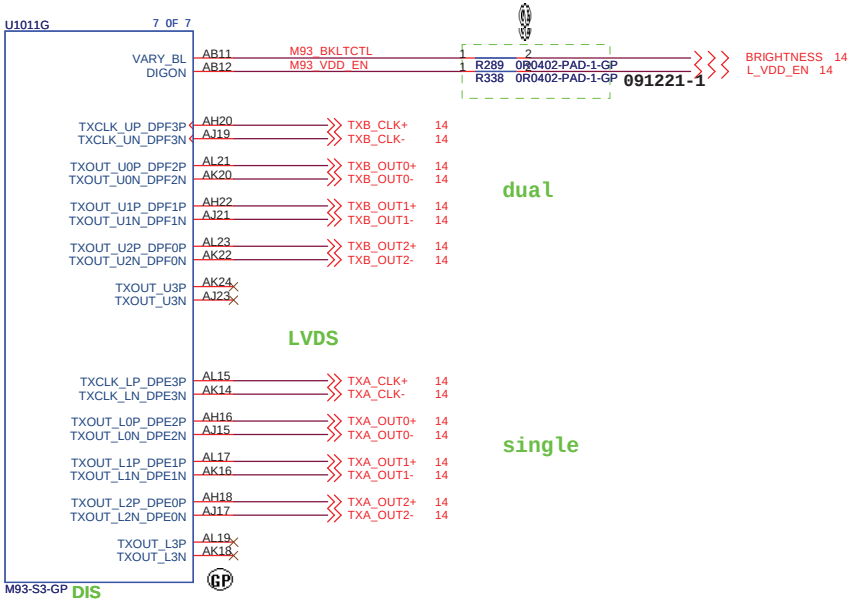
Size: A3 | Document Number: PATEK | Rev: SA

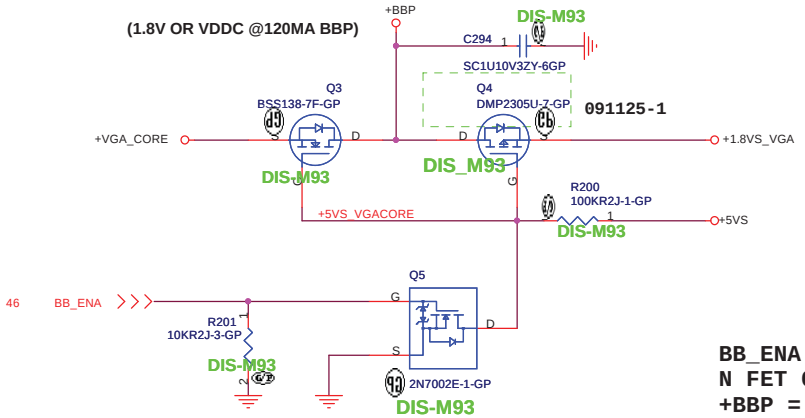
Date: Monday, March 15, 2010 | Sheet 44 of 57

M93 GPU(1/5)



+1.8V 0R +VGA_CORE@120MA





BB_ENA = 0V FOR BACK BIASING DISABLED
N FET Q5 = OFF, P FET Q4 = OFF, N FET Q3 = ON
+BBP = VDD_CORE
BB_ENA = +3.3V FOR BACK BIASING ENABLED
N FET Q5 = ON, P FET Q4 = ON, N FET Q3 = OFF
+BBP = +1.8V

<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VGA-PCIE/LVDS(1/5)

Size	Document Number	Rev
A3	PATEK	SA

Date: Monday, March 15, 2010 Sheet 45 of 57

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

0 = DON'T INSTALL RES
1 = INSTALL 10K RES
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M93-S3
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8		0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROM ID CFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0]	0
AUD[0]	VSYNC	0 0 No audio function	XX
		0 1 Audio for DisplayPort and HDMI if dongle is detected	
		1 0 Audio for DisplayPort only	
		1 1 Audio for both DisplayPort and HDMI	

Aperture Conig. PIN	M93S3 GPIO	Strapping Resistor	64MB	128MB	256MB
CONFIG0	GPIO_11	R209	0	0	1
CONFIG1	GPIO_12	R210	1	0	0
CONFIG2	GPIO_13	R211	0	0	0

M93 VRAM ID

Bit0 Low=Quanta ,H=Wistron

Bit1 Low=512MB, H=1GB

Bit2 Low=Samsung ,H=Hynix

Bit3 Low

VRAM ID

090625

M93 GPU(2/5)

HDMI

U1011E 5 OF 7

M93-S3-GP DIS

M93 LP: VDDC=0.9/1.1V

VID1	VID0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

CRT

DIS_PARK

Only for PARK-S3
DO NOT INSTALL for M93-S3

(1.8V @ 120MA DPLL_PVDD)
470R_1000mA

(1.1V @300MA DPLL_VDDC)
470R_1000mA

(1.8V @20MA TSVDD)

(1.8V @ 70MA AVDD)

(1.8V @ 45MA VDD1DI)

(1.8V @ 2MA A2VDDQ)

VOLTAGE DIVIDER TO MAKE XTALIN VOLTAGE LEVEL OF 1.8V

VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = .6V)

Optional RC network to fine tune PWR SEQ.

<Core Design>

wistron

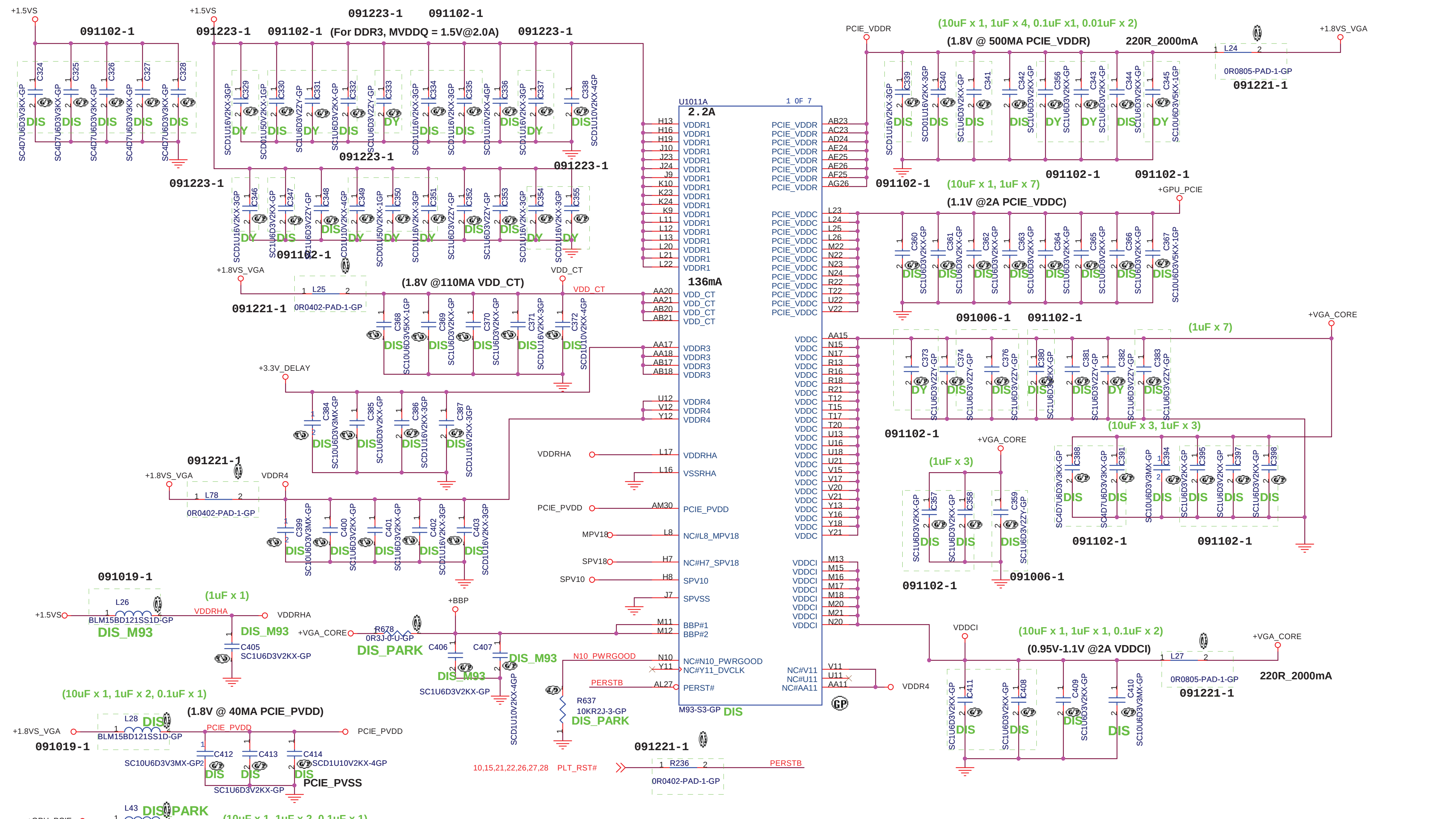
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LCD/CRT/HDMI PORT(2/5)

Size: A2 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 46 of 57

M93 GPU(3/5)



<Core Design>

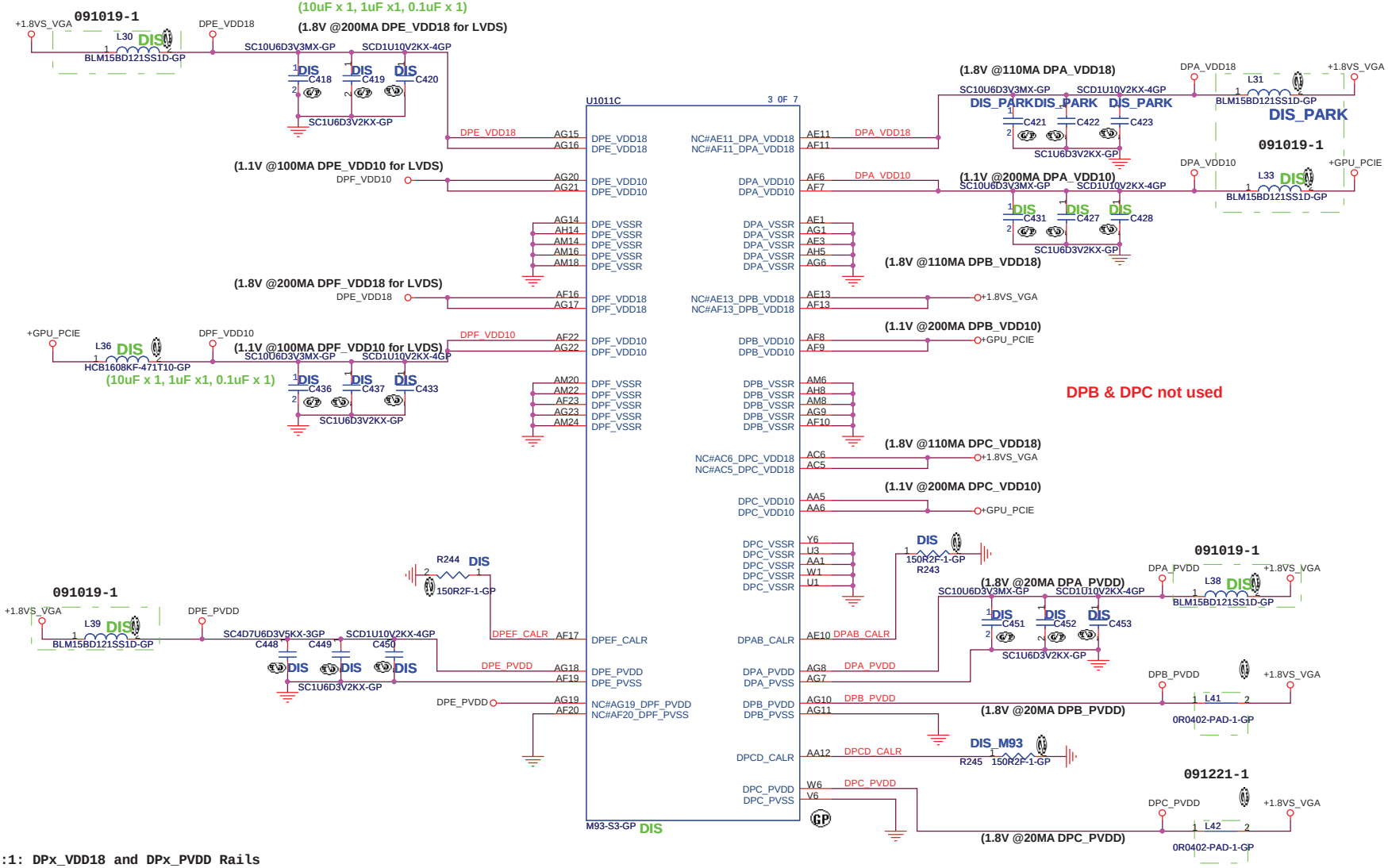
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	VGA-POWER/GND(3/5)	
Size A3	Document Number PATEK	Rev SA
Date: Monday, March 15, 2010	Sheet 47 of 57	

M93 GPU(4/5)

When space is not enough
Consider that use one bead to share



NOTE:1: DPx_VDD18 and DPx_PVDD Rails can be join together and remove Decoupling Capacitors and BEAD for DPx_PVDD if signal integrity for DP lanes are OK.

NOTE:2: DPA_VDD10 / DPB_VDD10 and DPE_VDD10 / DPF_VDD10 Rails can be join together and remove Decoupling Capacitors and BEADfor one rail of each pair if signal integrity for DP lanes are OK.
We also need to Change BEAD to minimum 400mA rating.

NOTE:3: DPx_VDD18 Rails can be join together as shown in schematic for Dual -Link DVI or LVDS setting and remove DecouplingCapacitors and BEAD of any one rail of the pair if signal integrity for DP lanes are OK.
We need at least 500mA Bead to supportjoin rails.

<Core Design>

wistron

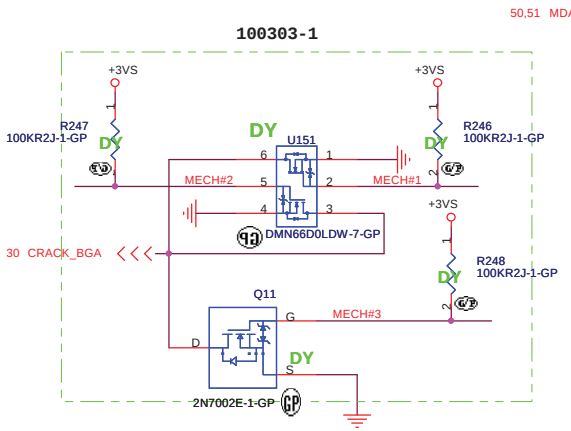
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VGA-POWER/GND(4/5)

Size	Document Number	Rev
A3	PATEK	SA

Date: Monday, March 15, 2010 Sheet 48 of 57

GPU(5/5)



MVREF	0.5 * VDDR1	0.7 * VDDR1
DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

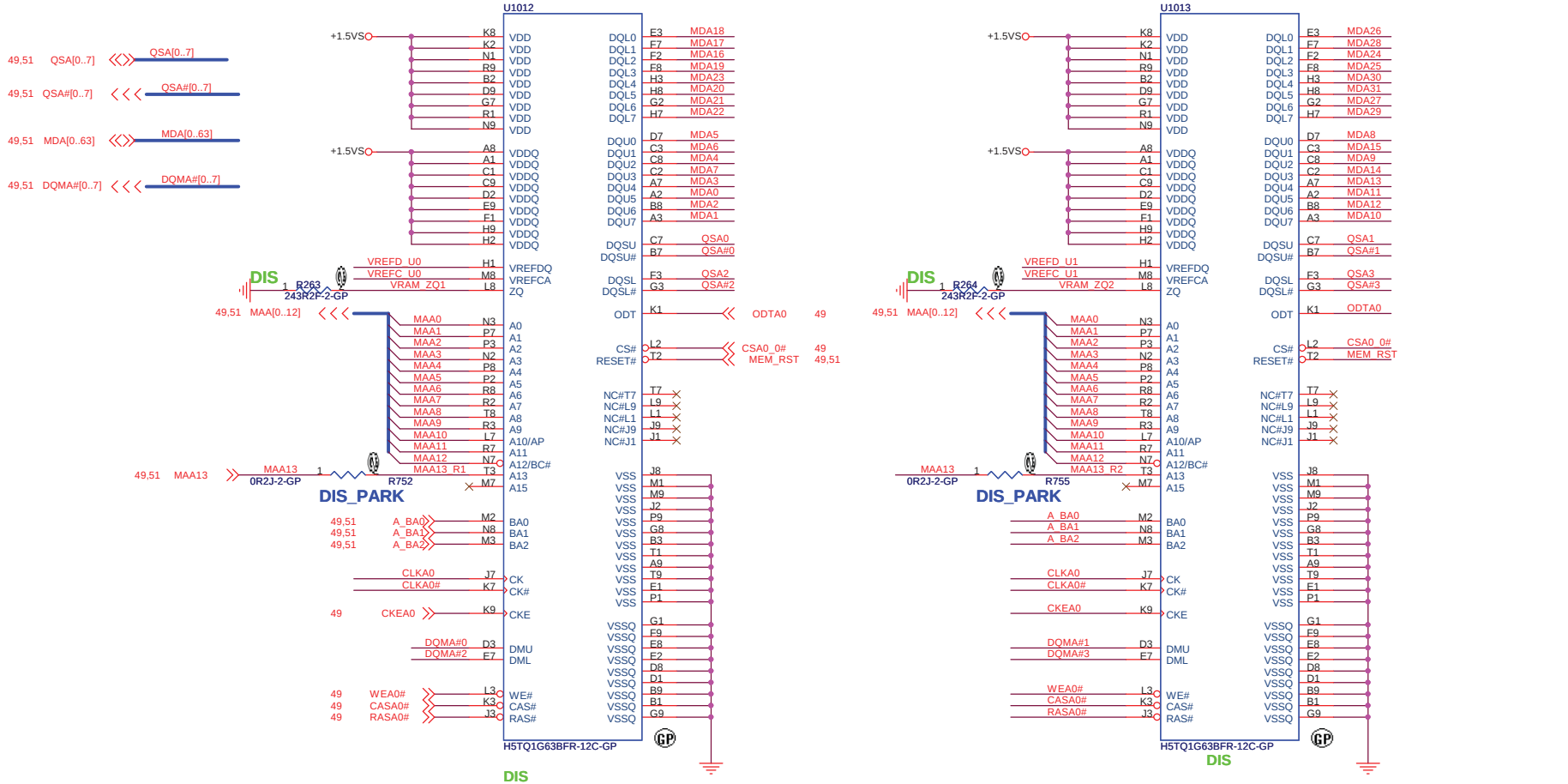
Title: VGA-MEM INTERFACE(5/5)

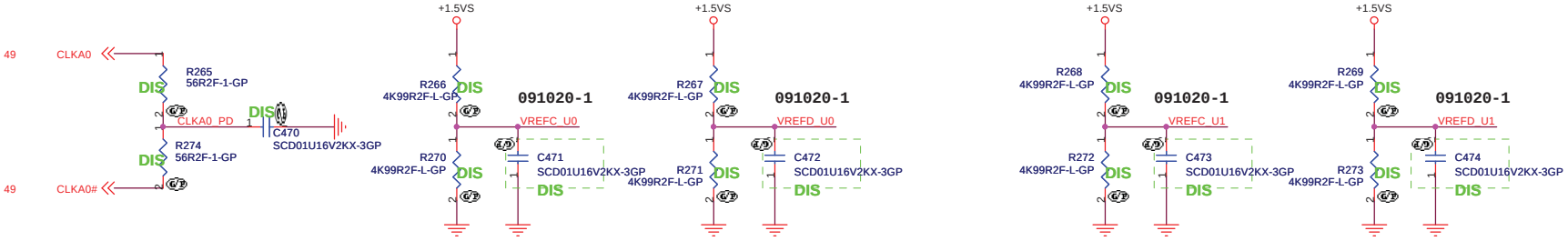
Size: A3 | Document Number: PATEK | Rev: SA

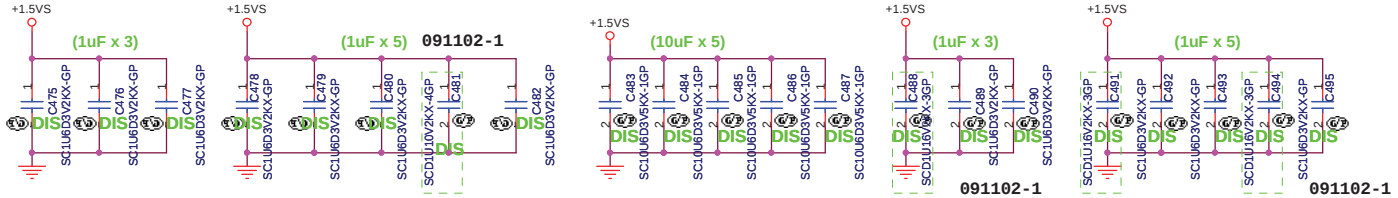
Date: Monday, March 15, 2010 | Sheet 49 of 57

VRAM DDR3 (1/2)

256MB/512MB DDR3







<Core Design>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

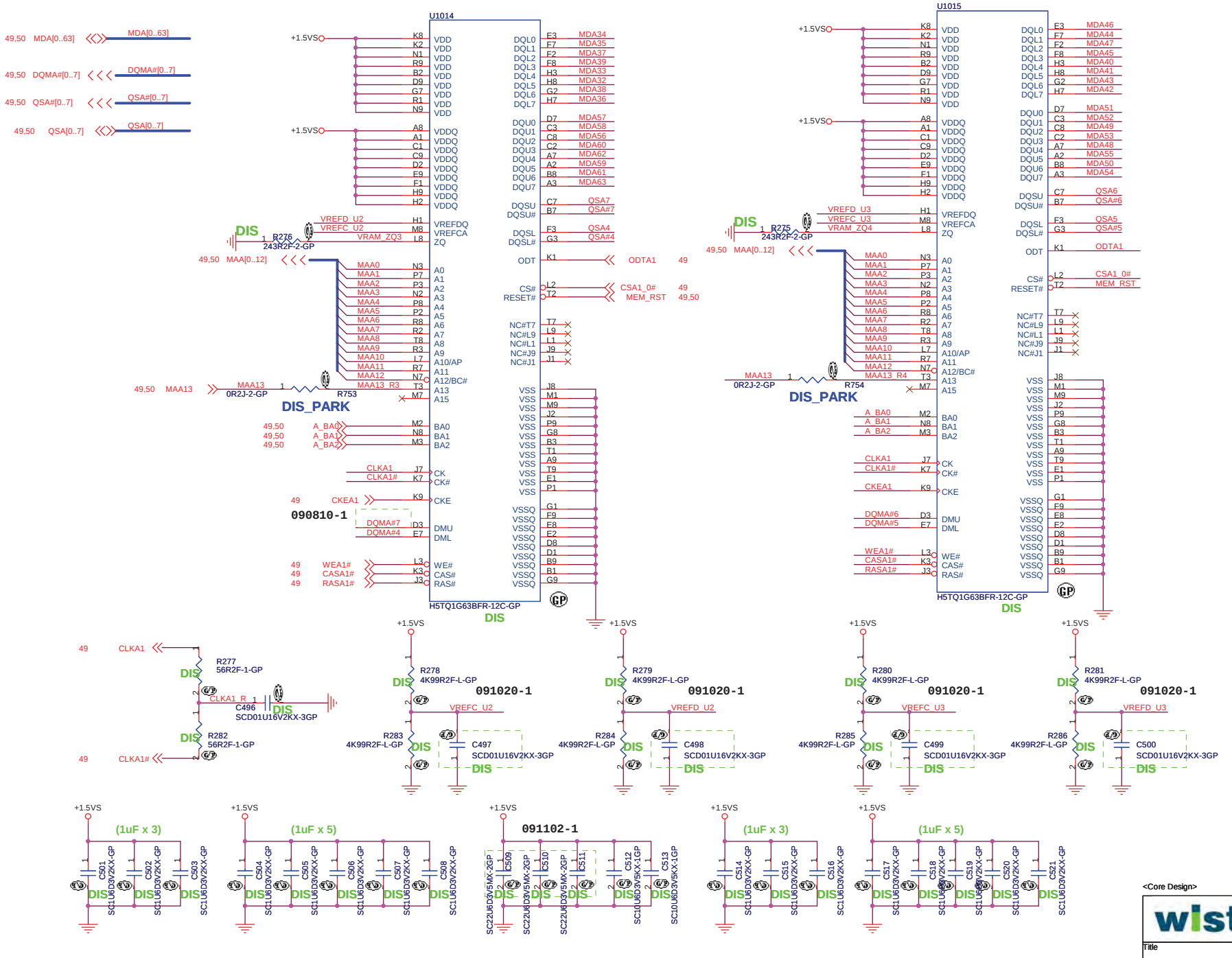
Title: VGA-MEMORY

Size	Document Number	Rev
A3	PATEK	SA

Date: Monday, March 15, 2010 Sheet 50 of 57

VRAM DDR3 (2/2)

256MB/512MB DDR3



<Core Design>

wistron

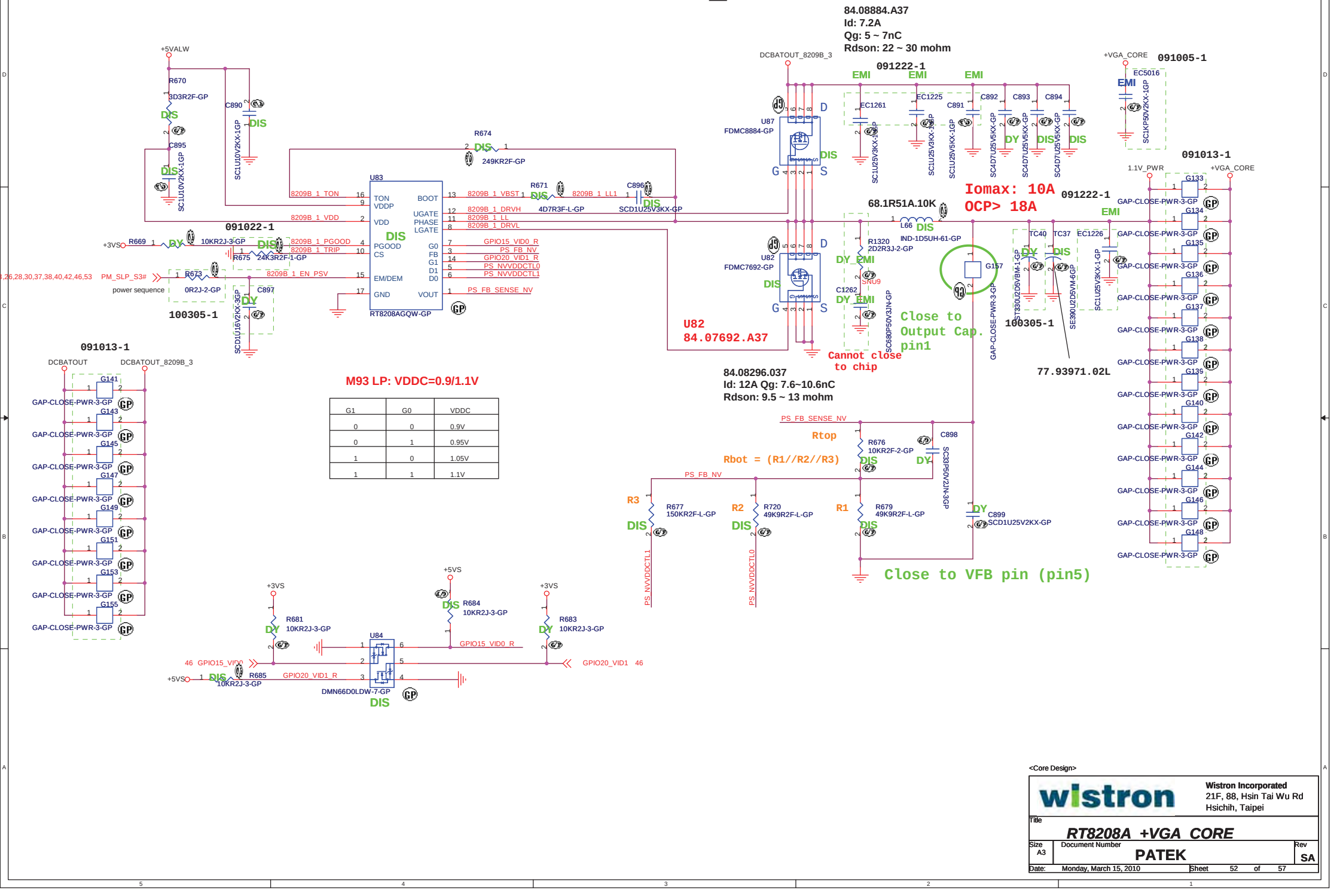
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VGA-MEMORY

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 51 of 57

RT8209B for +VGA_CORE



G1	G0	VDDC
0	0	0.9V
0	1	0.95V
1	0	1.05V
1	1	1.1V

<Core Design>

wistron

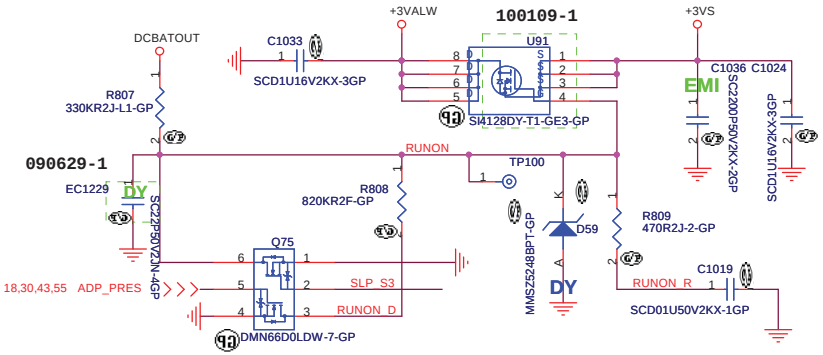
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RT8208A +VGA_CORE

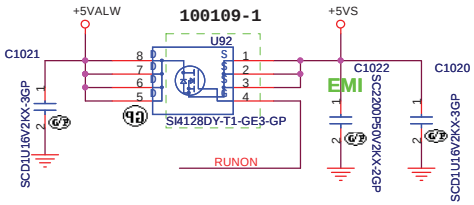
Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 52 of 57

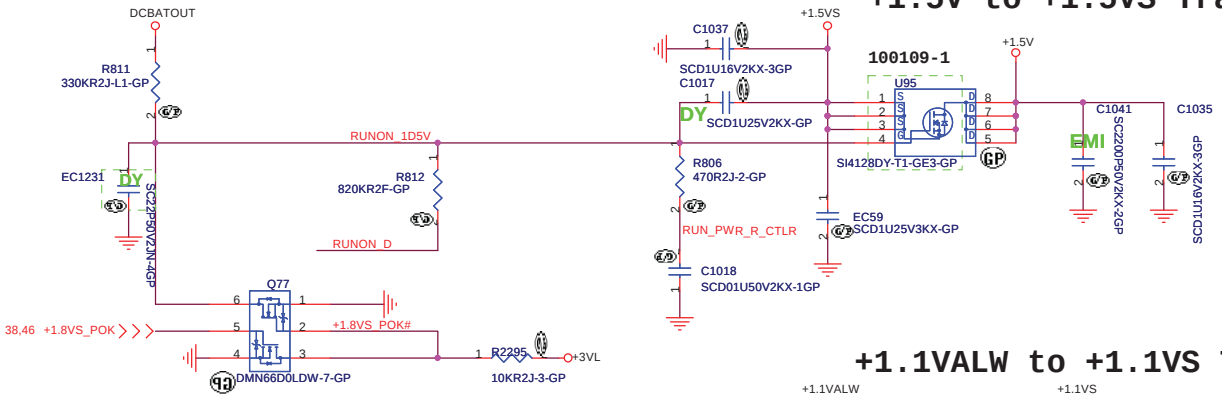
+3VALW to +3VS Transfer



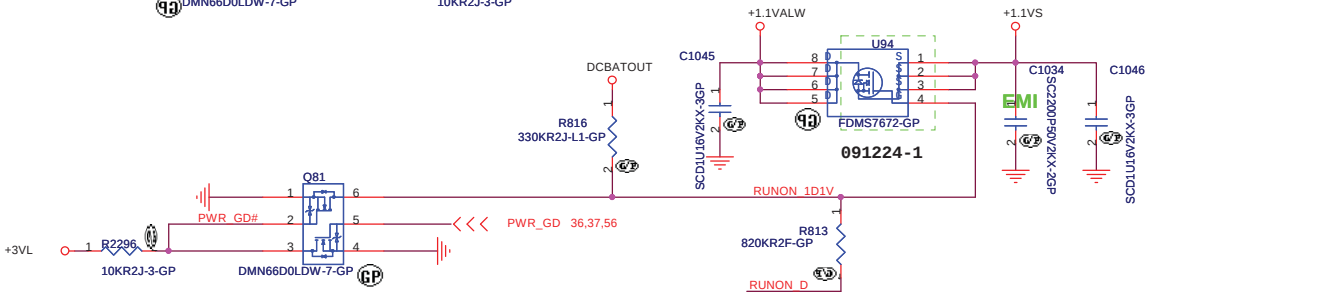
+5VALW to +5VS Transfer

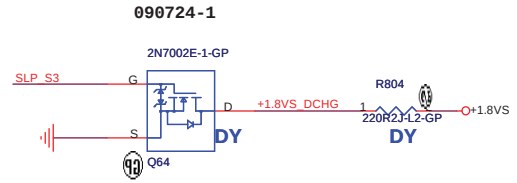


+1.5V to +1.5VS Transfer

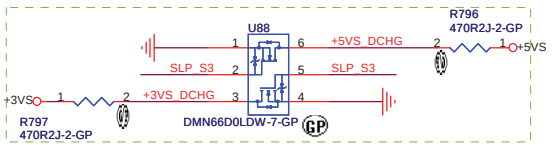


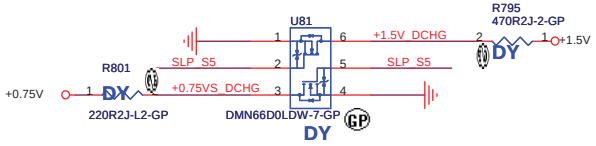
+1.1VALW to +1.1VS Transfer

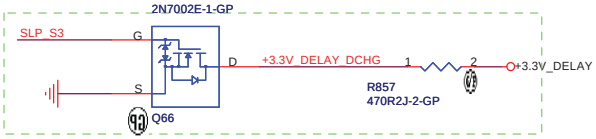


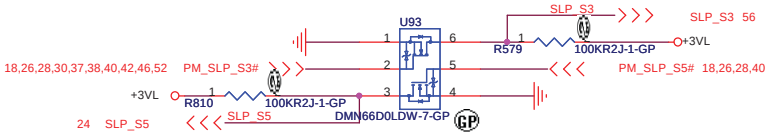


Discharge circuit-1









<Core Design>

wistron

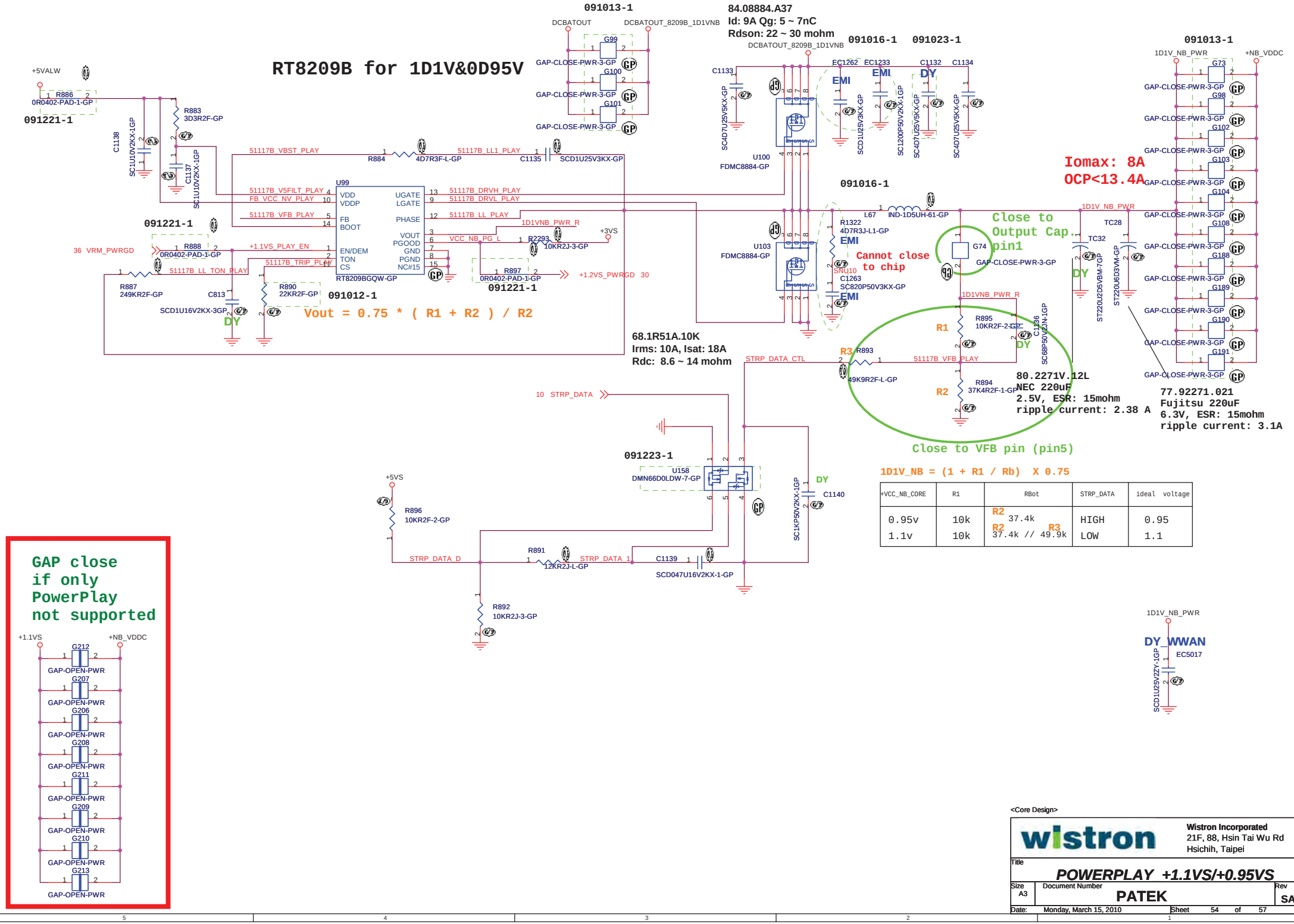
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

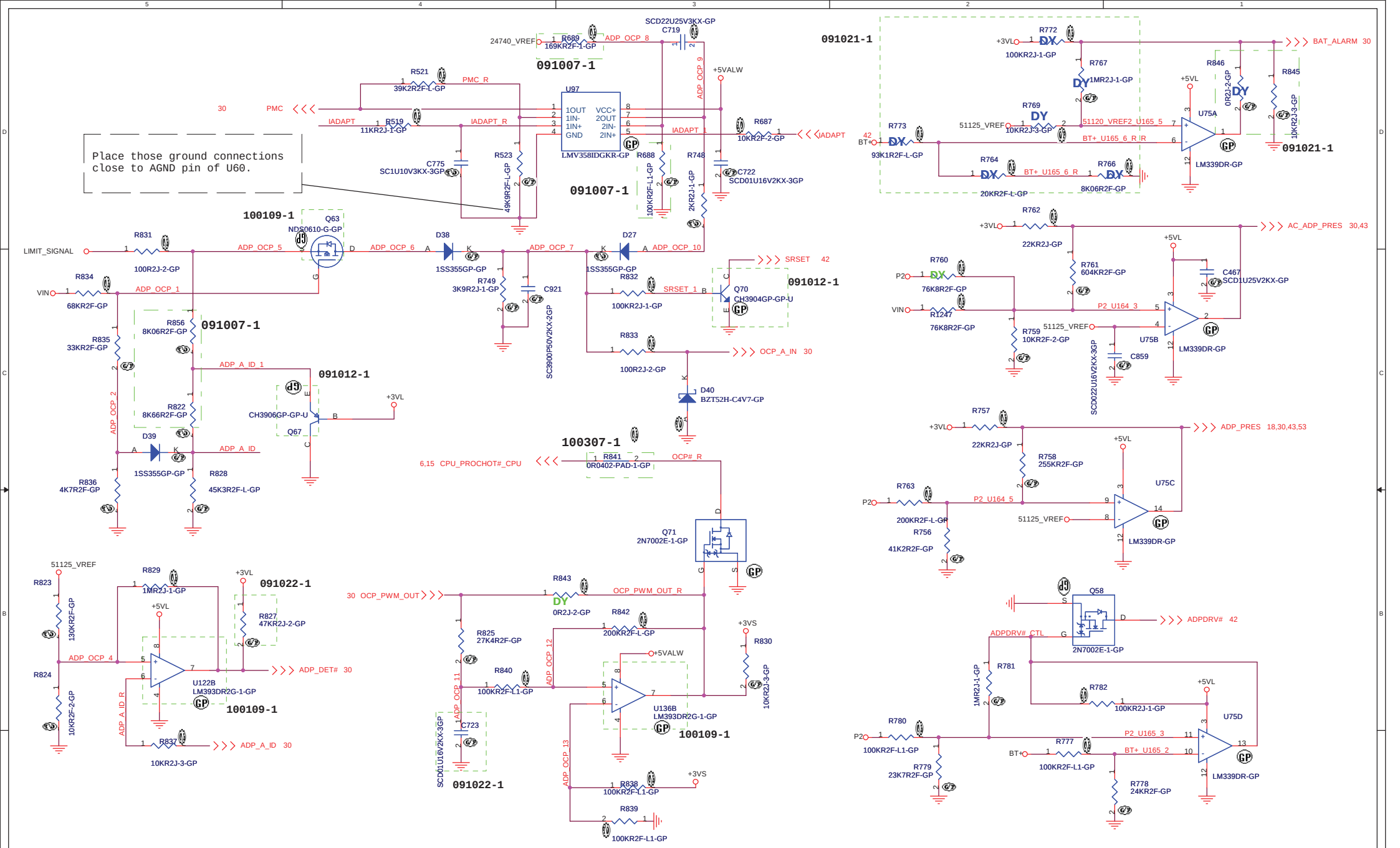
Title: DC/DC

Size	Document Number	Rev
A3	PATEK	SA

Date: Monday, March 15, 2010 Sheet 53 of 57

RT8209B for 1D1V&0D95V





NOTE:
When AC_ADP_PRES=0 -->1
Vin*(R759//R761)/ [(R759//R761)+R1247]=51125_VREF
Vin=17.6145V

When AC_ADP_PRES=1 --> 0
[(Vin-51125_VREF)/R1247]+[(+3VL-51125_VREF)/(R761+R762)]=51125_VREF/R759
Vin=17.212554V

When ADP_PRES=0->1
P2*(R756//R758)/ [(R756//R758)+R763]=51125_VREF
P2=13.325V

When ADP_PRES=1->0
[(P2-51125_VREF)/R756]+[(+3VL-51125_VREF)/(R757+R758)]=51125_VREF/R756
P2=10.894V

<Core Design>

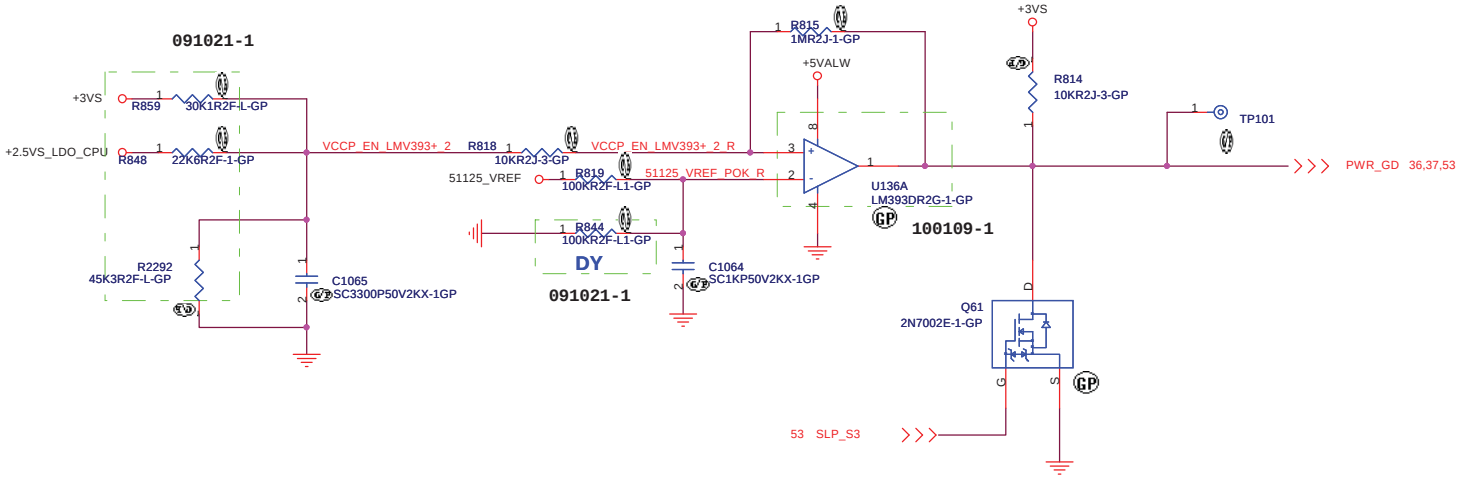
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: **ADP OCP**

Size	Document Number	Rev
A3	PATEK	SC

Date: Monday, March 15, 2010 Sheet 55 of 57



<Core Design>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: POK CKT

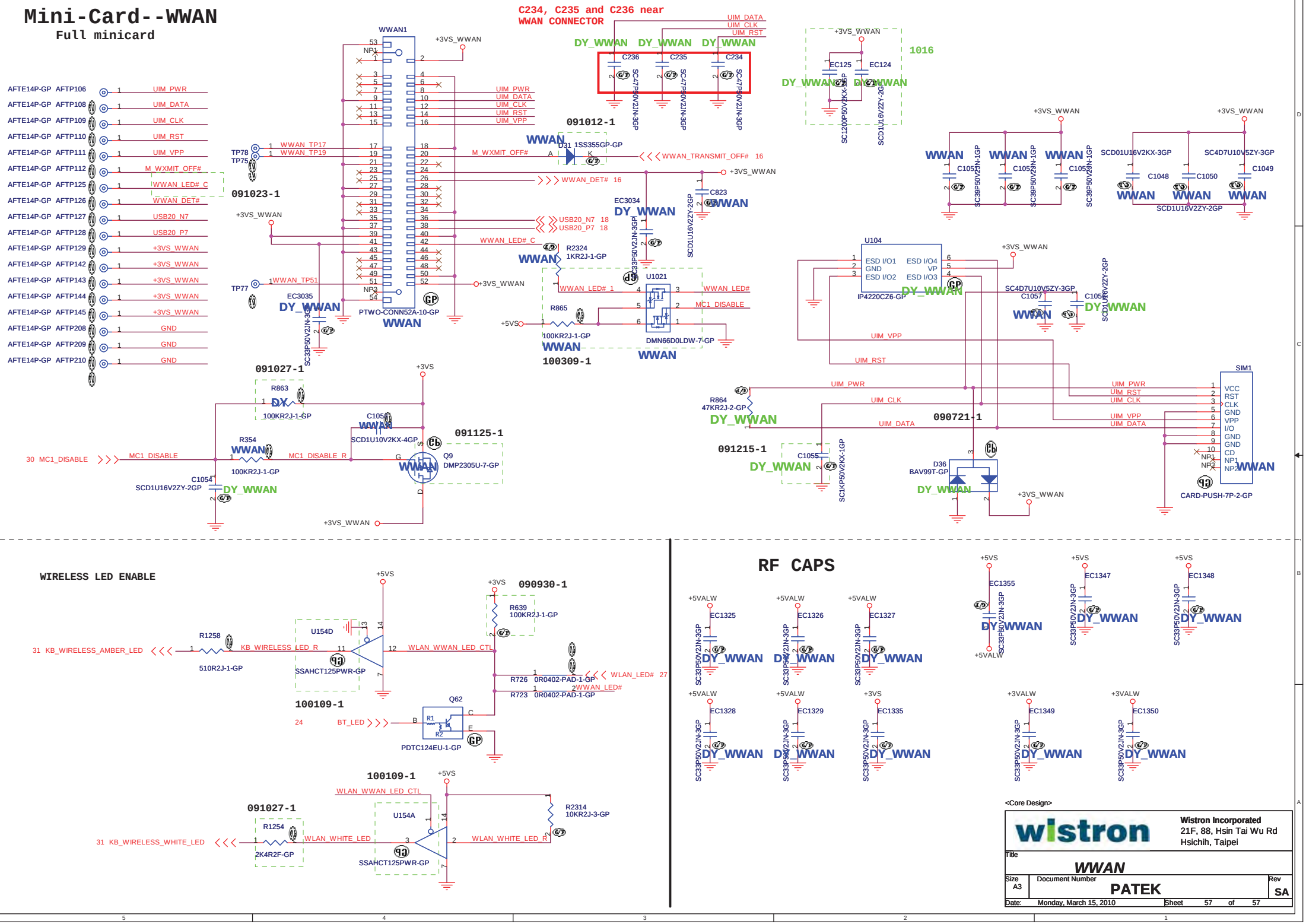
Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 56 of 57

Mini-Card--WWAN

Full minicard

C234, C235 and C236 near WWAN CONNECTOR



WIRELESS LED ENABLE

RF CAPS

<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: WWAN

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 57 of 57