

Compal Confidential

Schematics Document

INTEL Auburndale BGA with IBEX core logic

Fossil 2.0 UMA

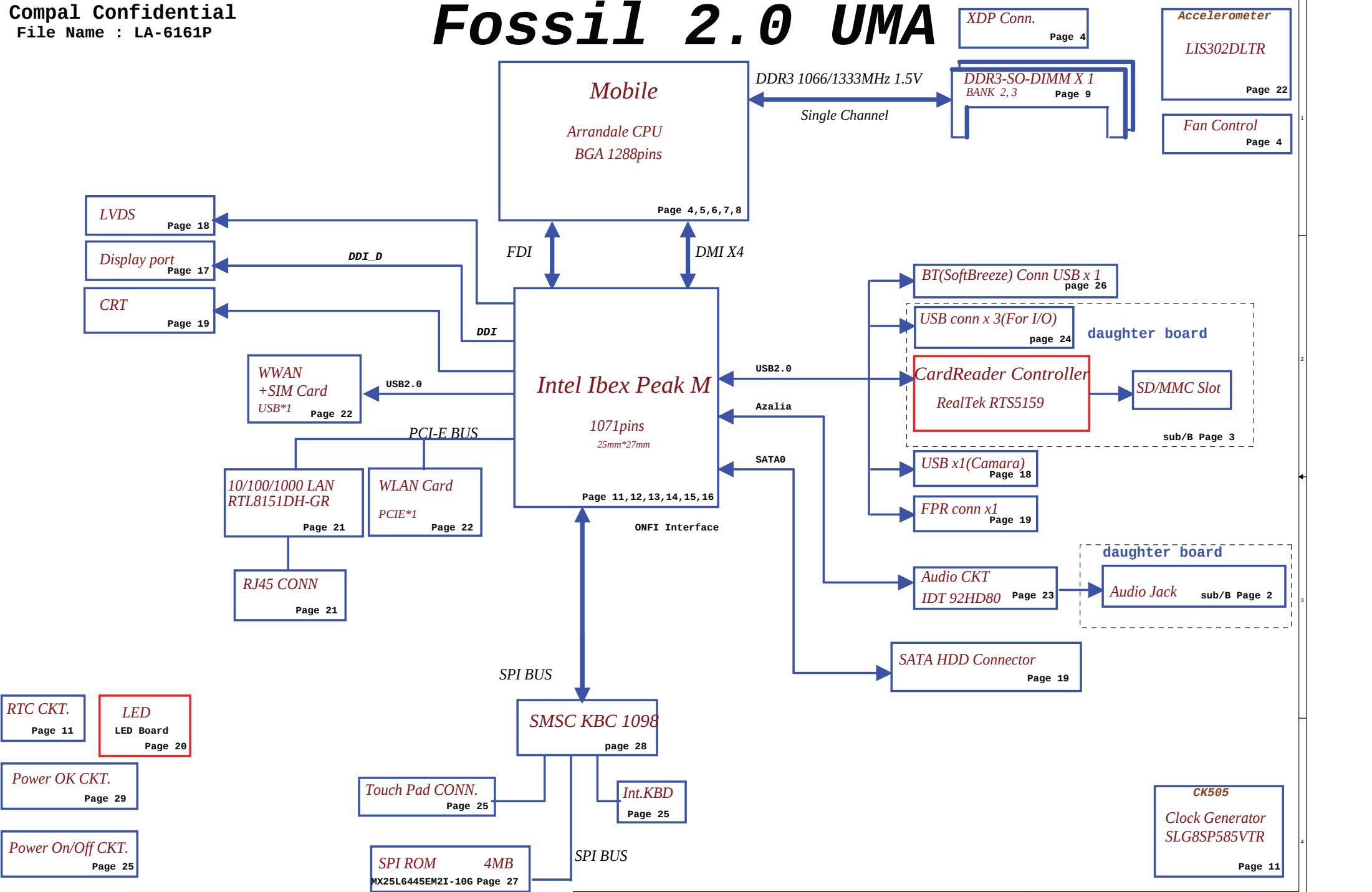
LA-6161P

2010-05-24

REV:1.0

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Fossil 2.0 UMA



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Voltage Rails (0 MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B +3VL	+5VALW +3VALW	+1.5V +0.75V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +1.05VS +1.8VS	
S0	0	0	0	0	0	
S1	0	0	0	0	0	
S3	0	0	0	0	X	
S5 S4/AC	0	0	0	X	X	
S5 S4/ Battery only	0	0	X	X	X	
S5 S4/AC & Battery don't exist	0	X	X	X	X	

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

ULV@ : means just install for ULV CPU

CONN@ : means ME part.

 Layout Notes

07/24 update

 : Question Area Mark.(Wait check)

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.1

DEBUG@ : means just build when PCIE port 80 CARD function enableRemove before MP

SMBUS Control Table

	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	X	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	V	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	V

Strapping Options Flash

CNT1#	CNT0#	Routing
0	1	Reserved
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to SPI
0	0	Flash Cycles Routed to LPC



CFG Straps for PROCESSOR

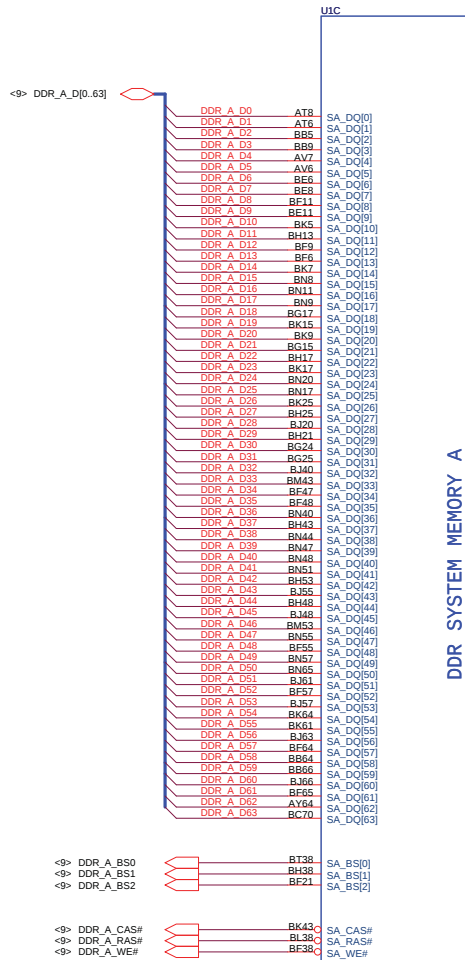
CFG0 R68 1 2 @3.01K 0402 1%
PCI-Express Configuration Select
1: Single PEG
CFG0 0: Bifurcation enabled
Not applicable for Clarkfield Processor

CFG3 R69 1 2 @3.01K 0402 1%
CFG3-PCI Express Static Lane Reversal
1: Normal Operation
CFG3 0: Lane Numbers Reversed
15 -> 0, 14 -> 1,

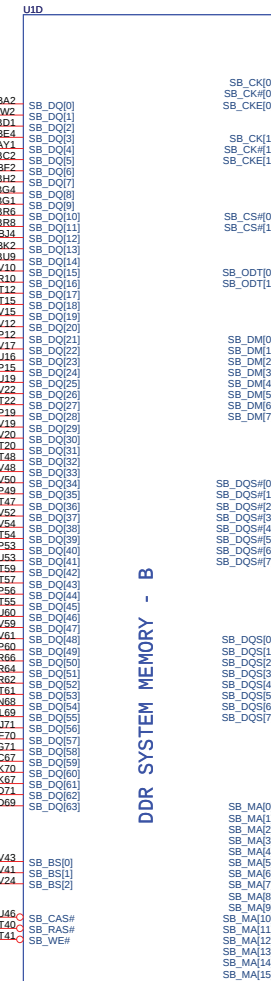
CFG4 R70 1 2 3.01K 0402 1%
ES1 sample need negative voltage
ES2 sample contact to GND

CFG4-Display Port Presence
1: Disabled; No Physical Display Port attached to Embedded Display Port
CFG4 0: Enabled; An external Display Port device is connected to the Embedded Display Port

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DDR SYSTEM MEMORY - A

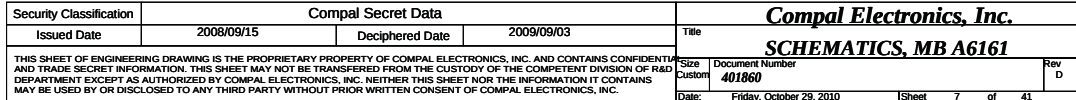


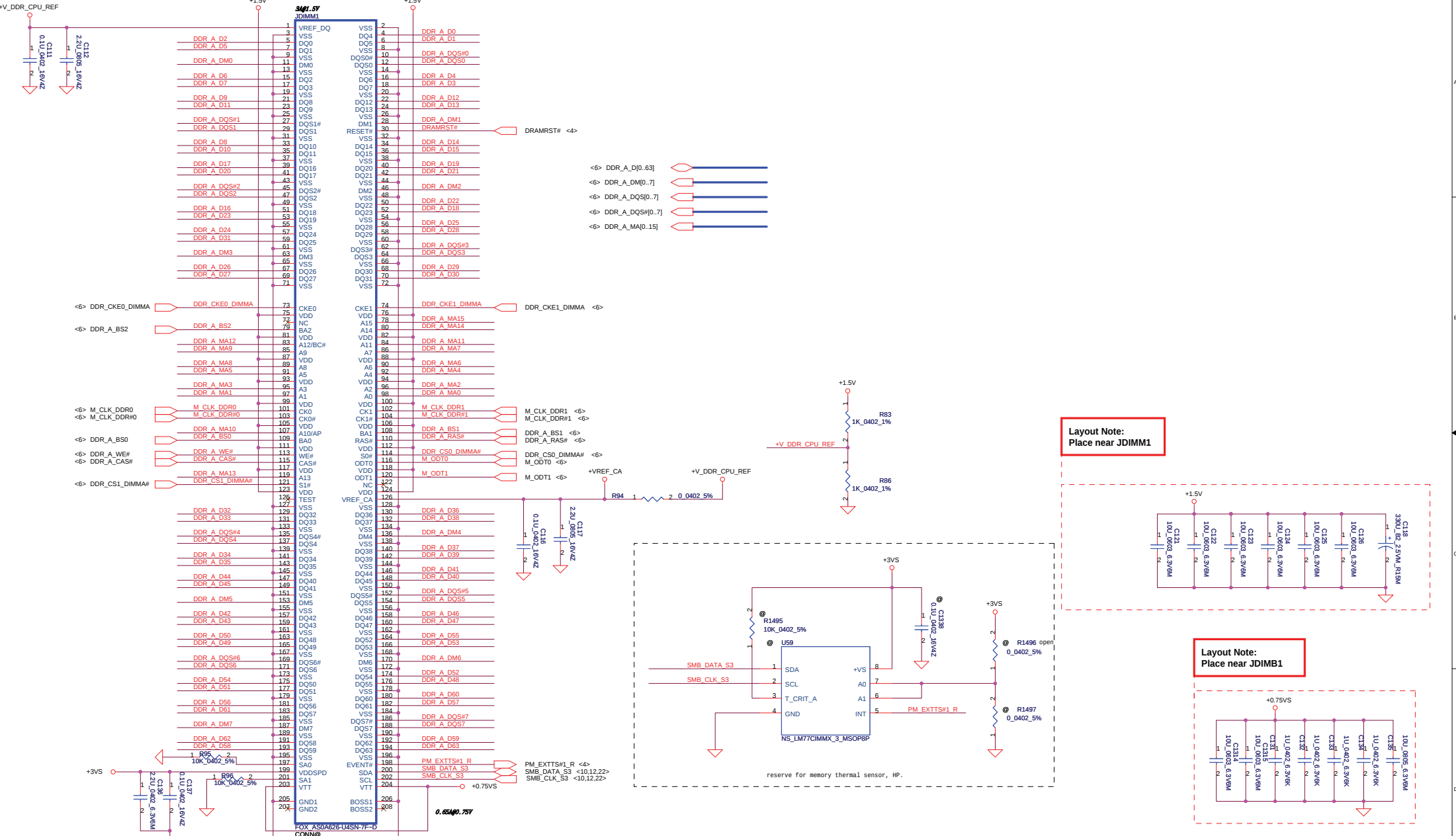
DDR SYSTEM MEMORY - B

INTEL_AUBURNDALE_1288

INTEL_AUBURNDALE_1288

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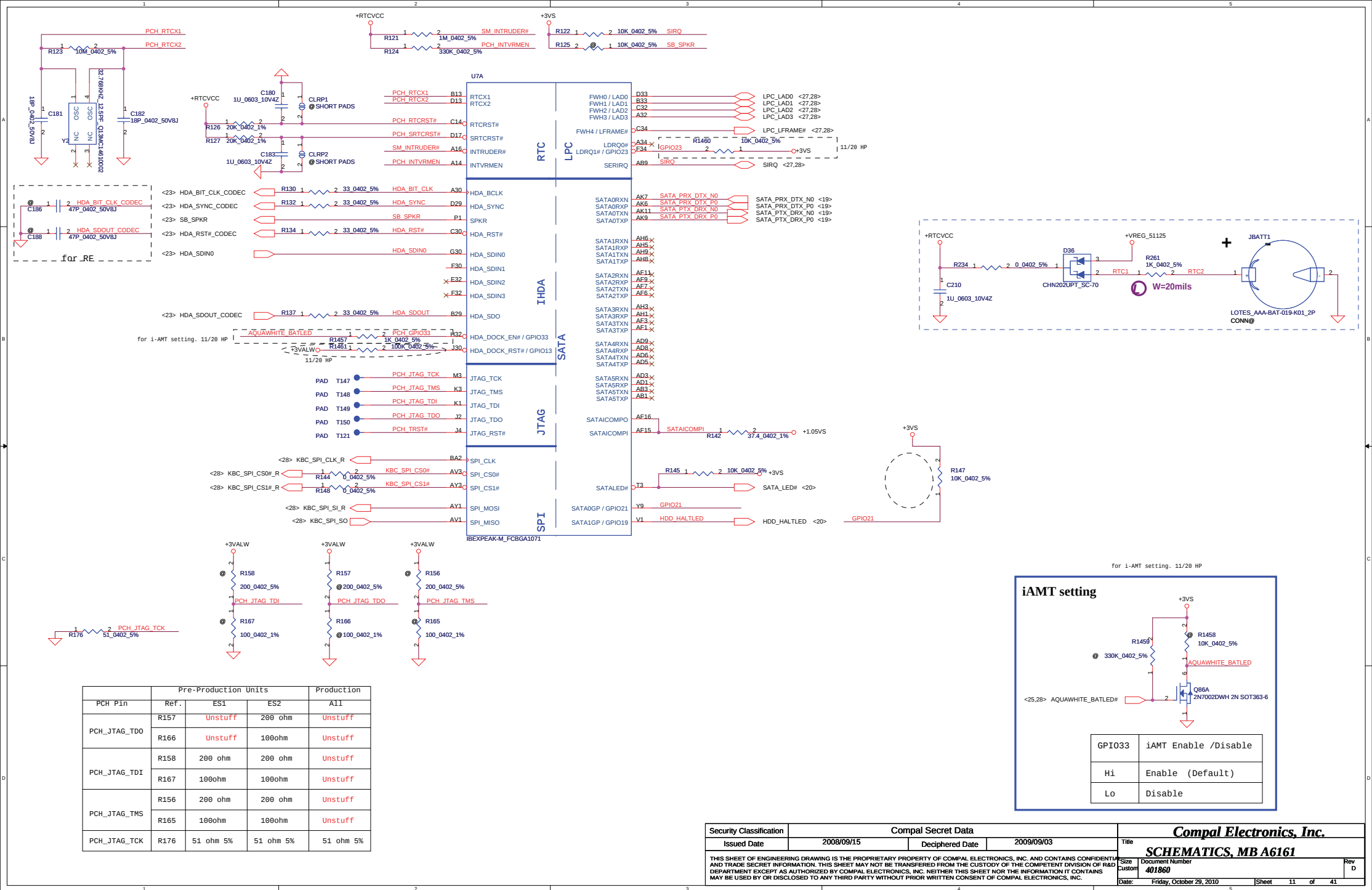




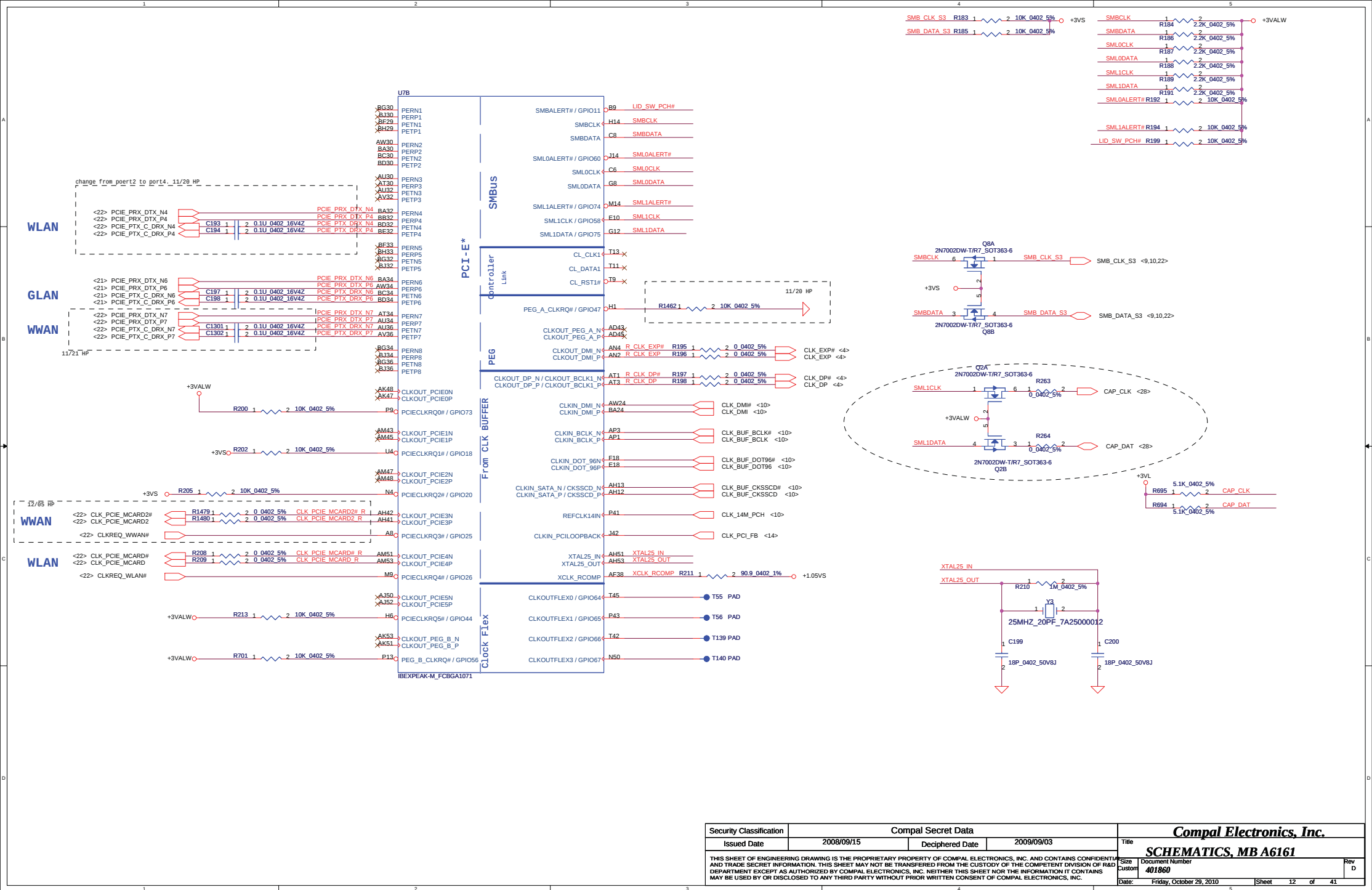
Layout Note:
Place near JDIMM1

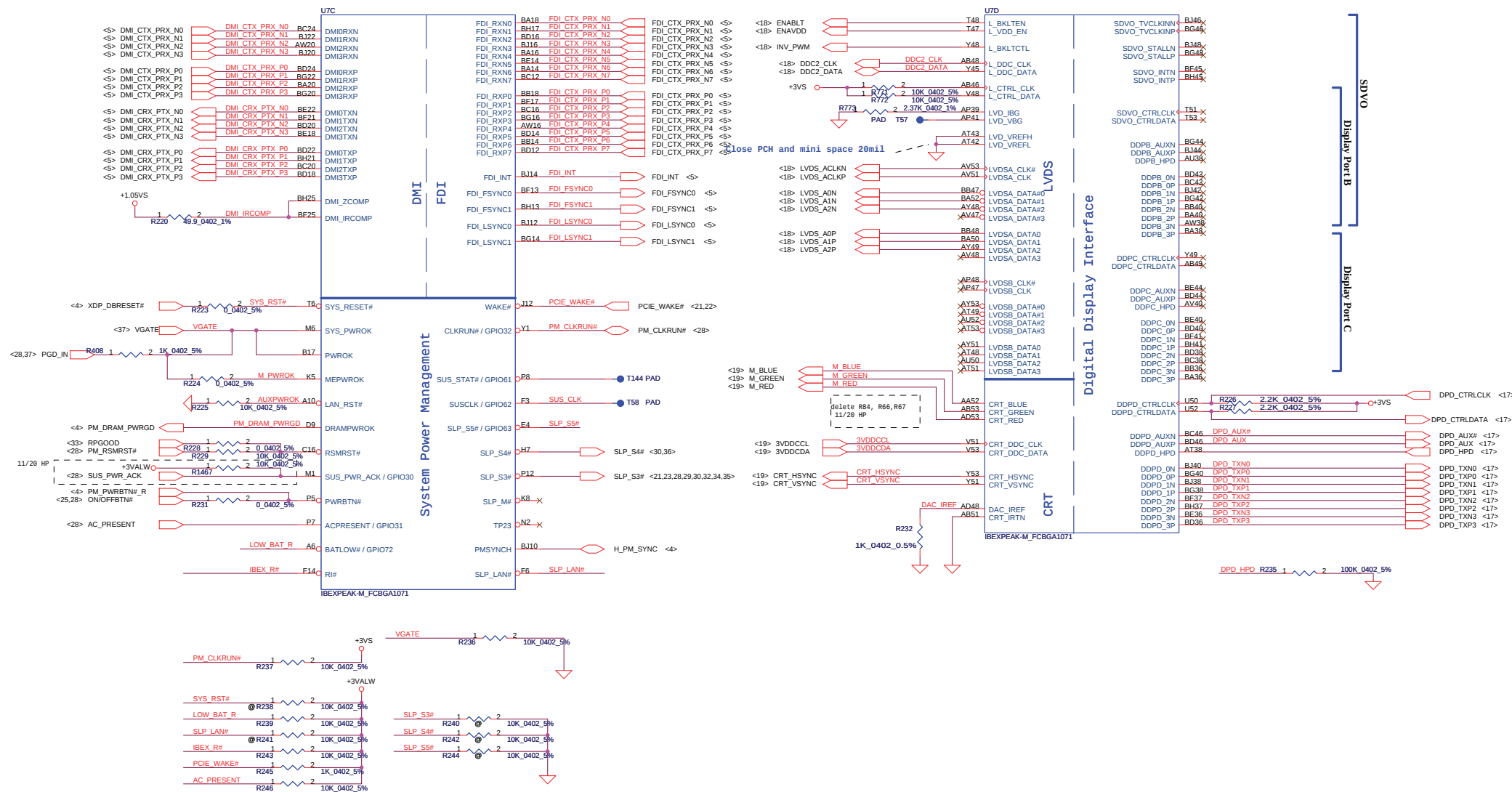
Layout Note:
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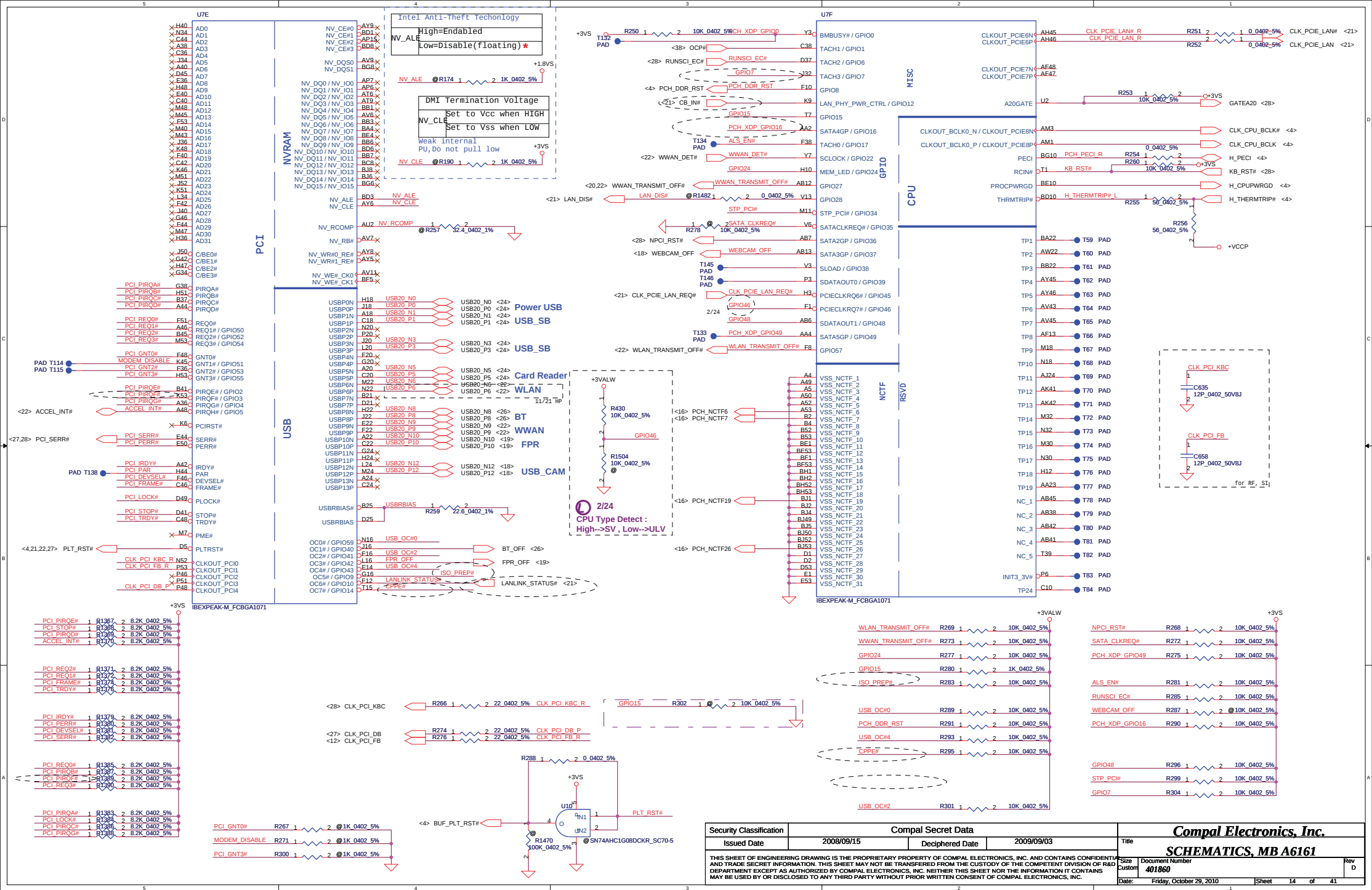
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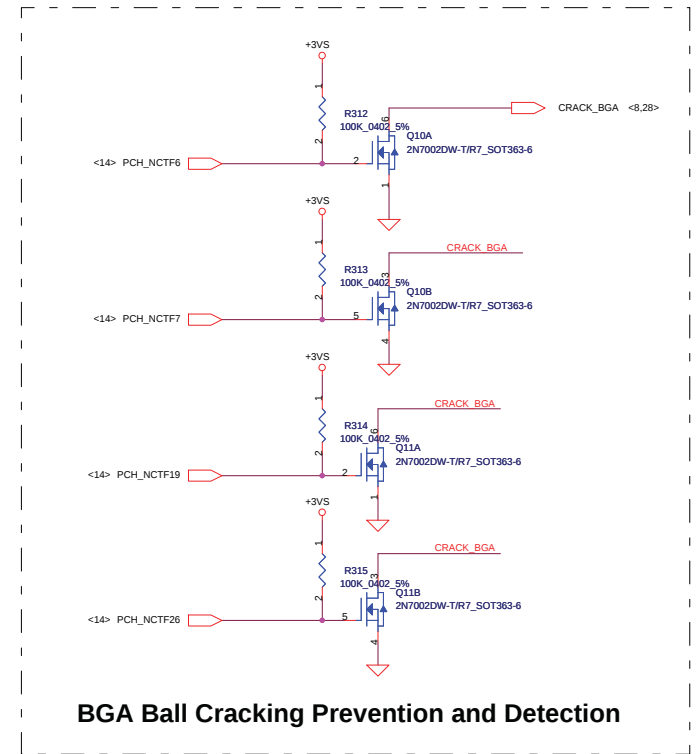
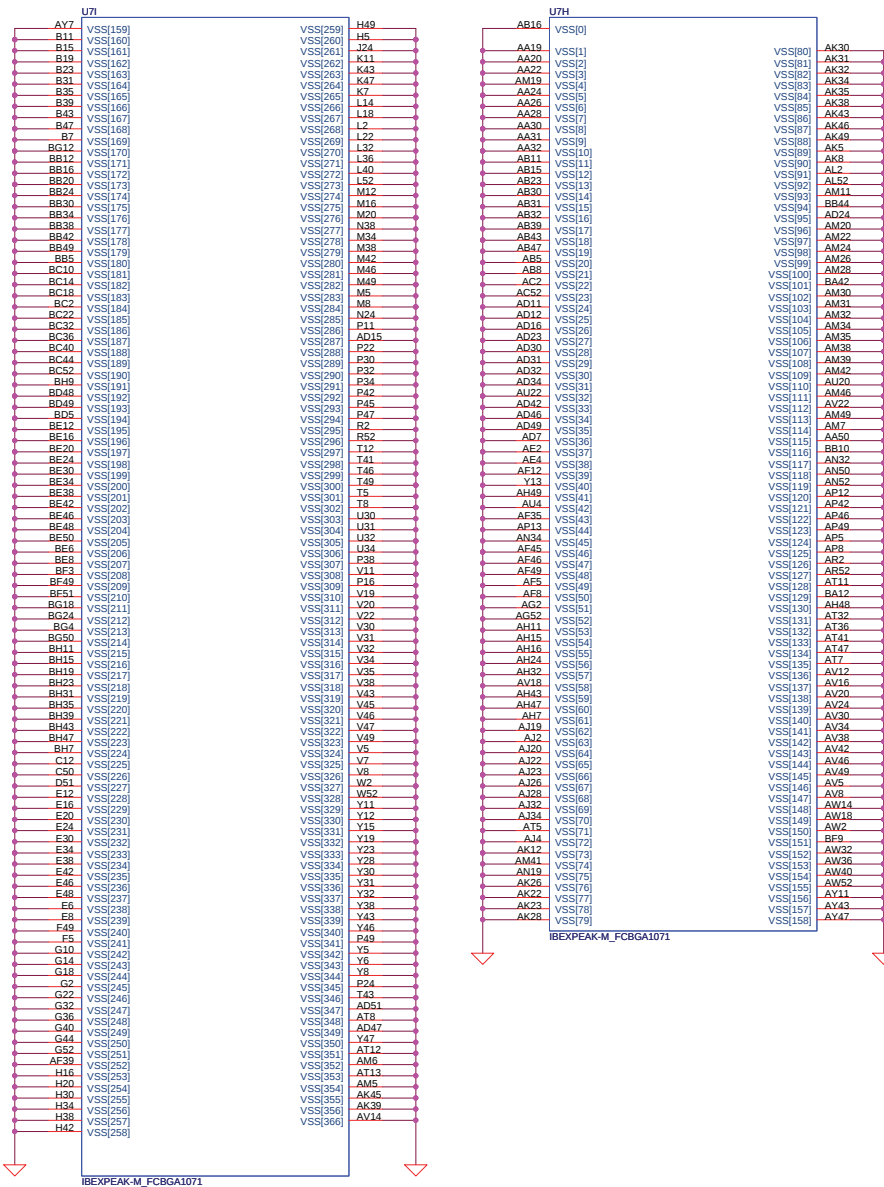


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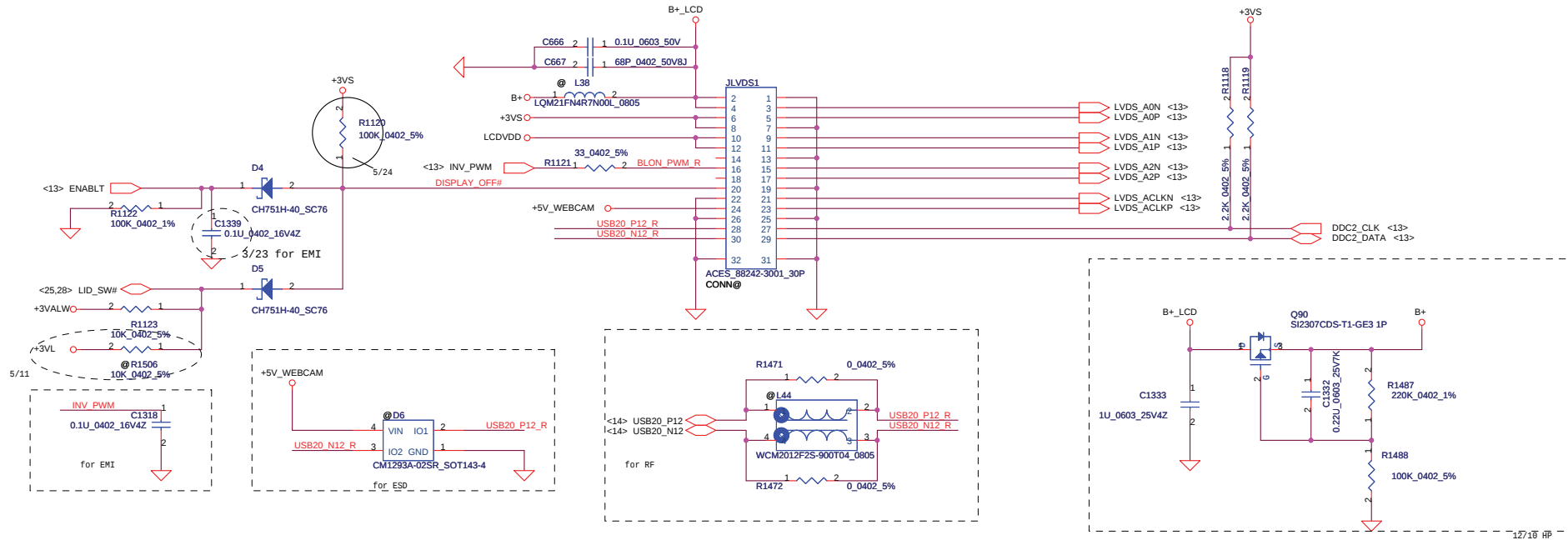




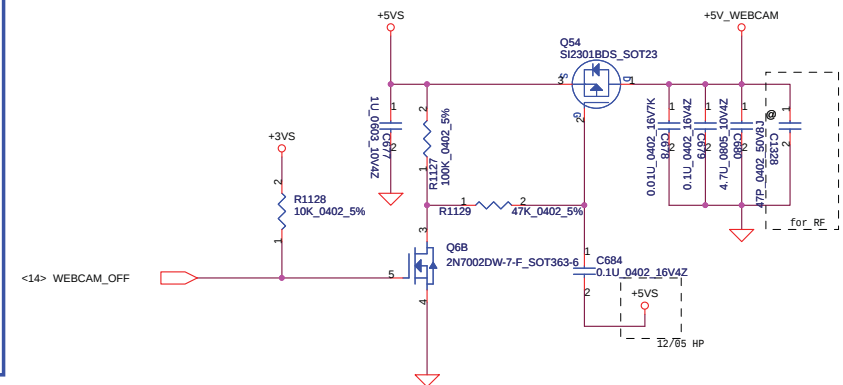
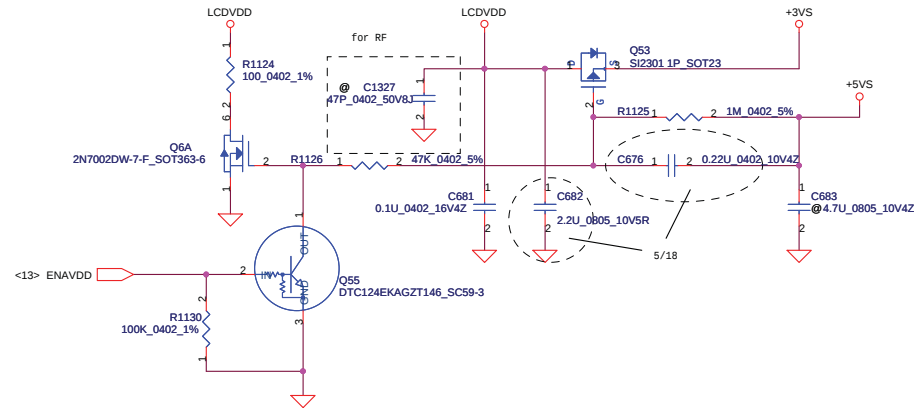


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LED/PANEL BD. CONN.

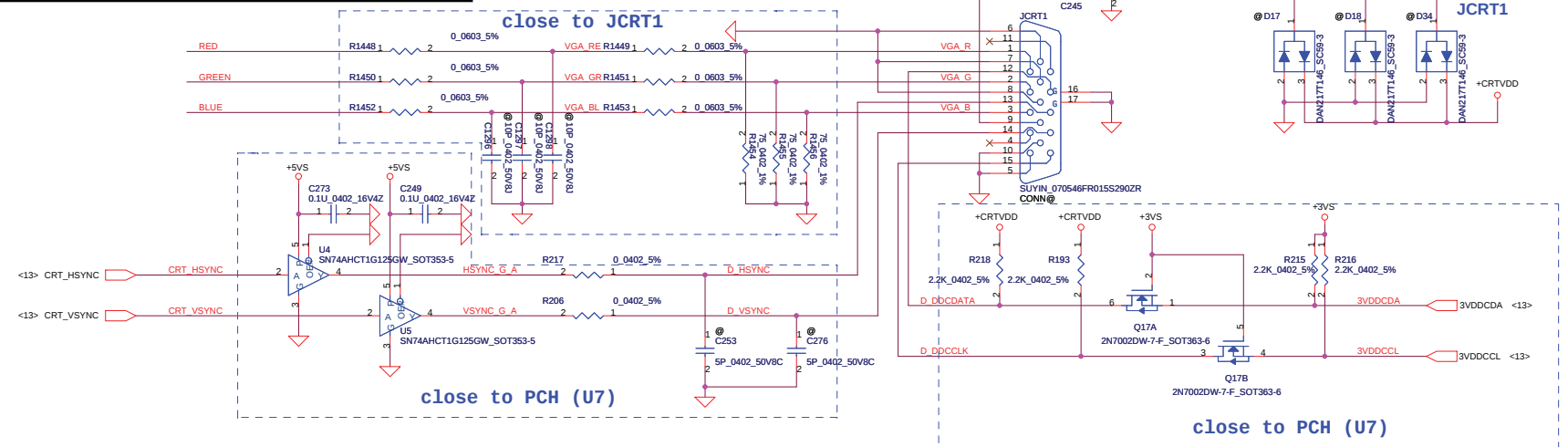
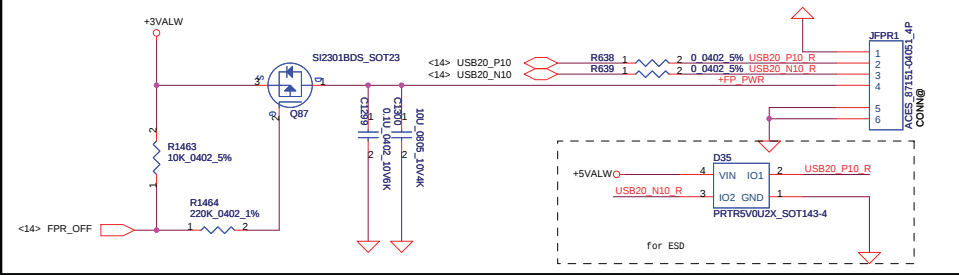


LCD POWER CIRCUIT

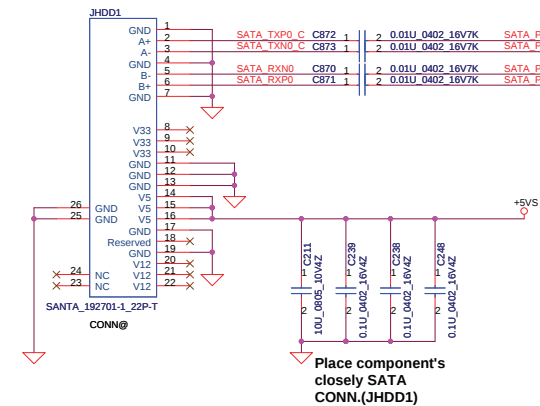


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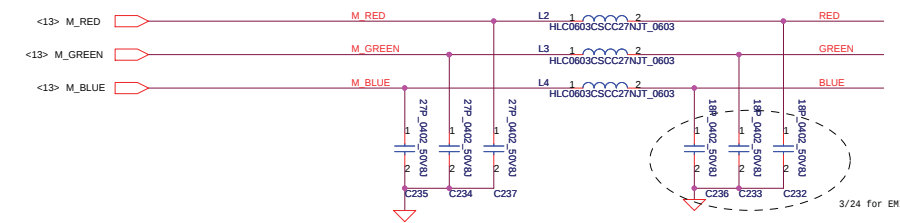
Finger printer



2.5' SATA HDD Connector

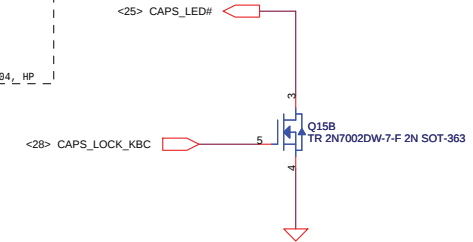
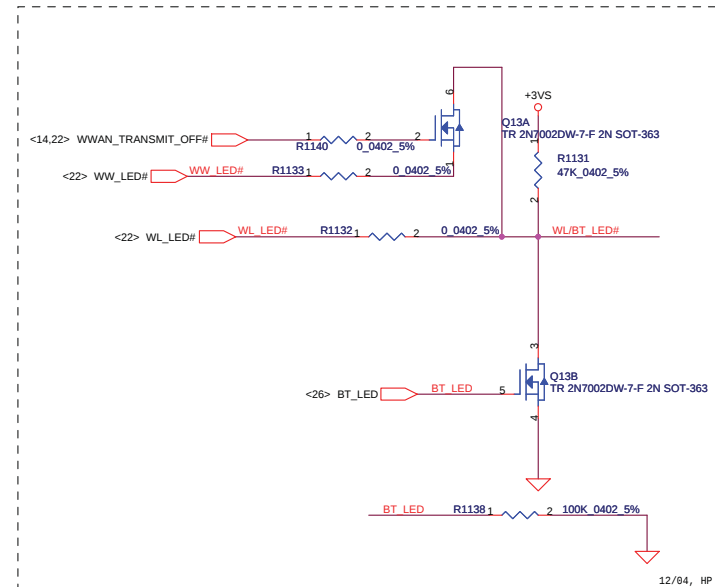
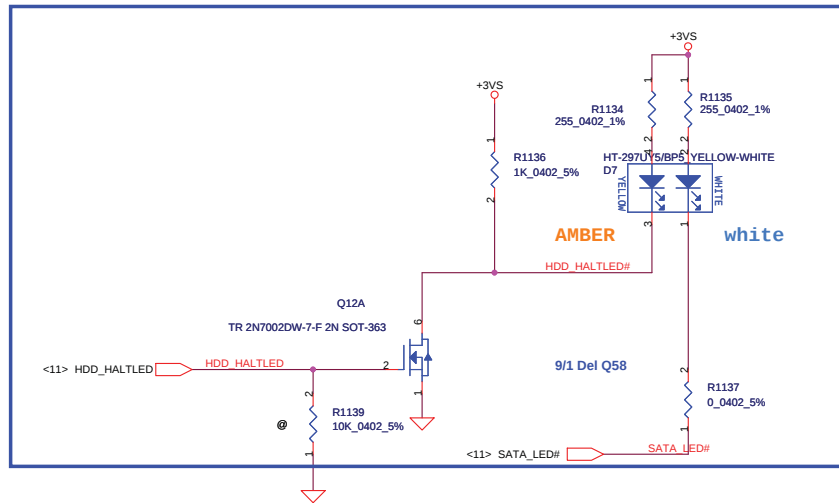


CRT Termination/EMI Filter close to PCH (U7)

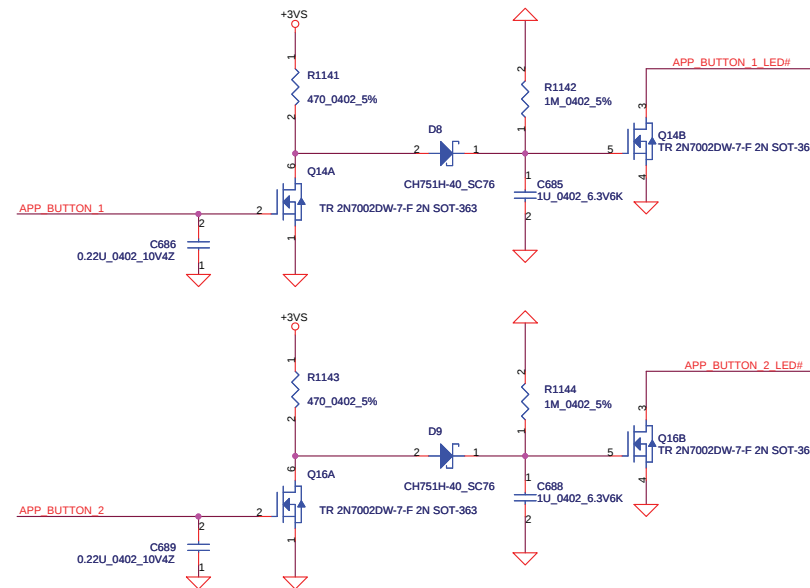
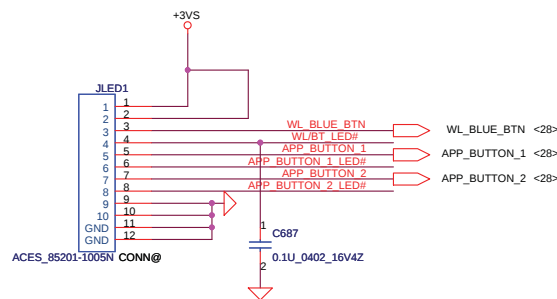


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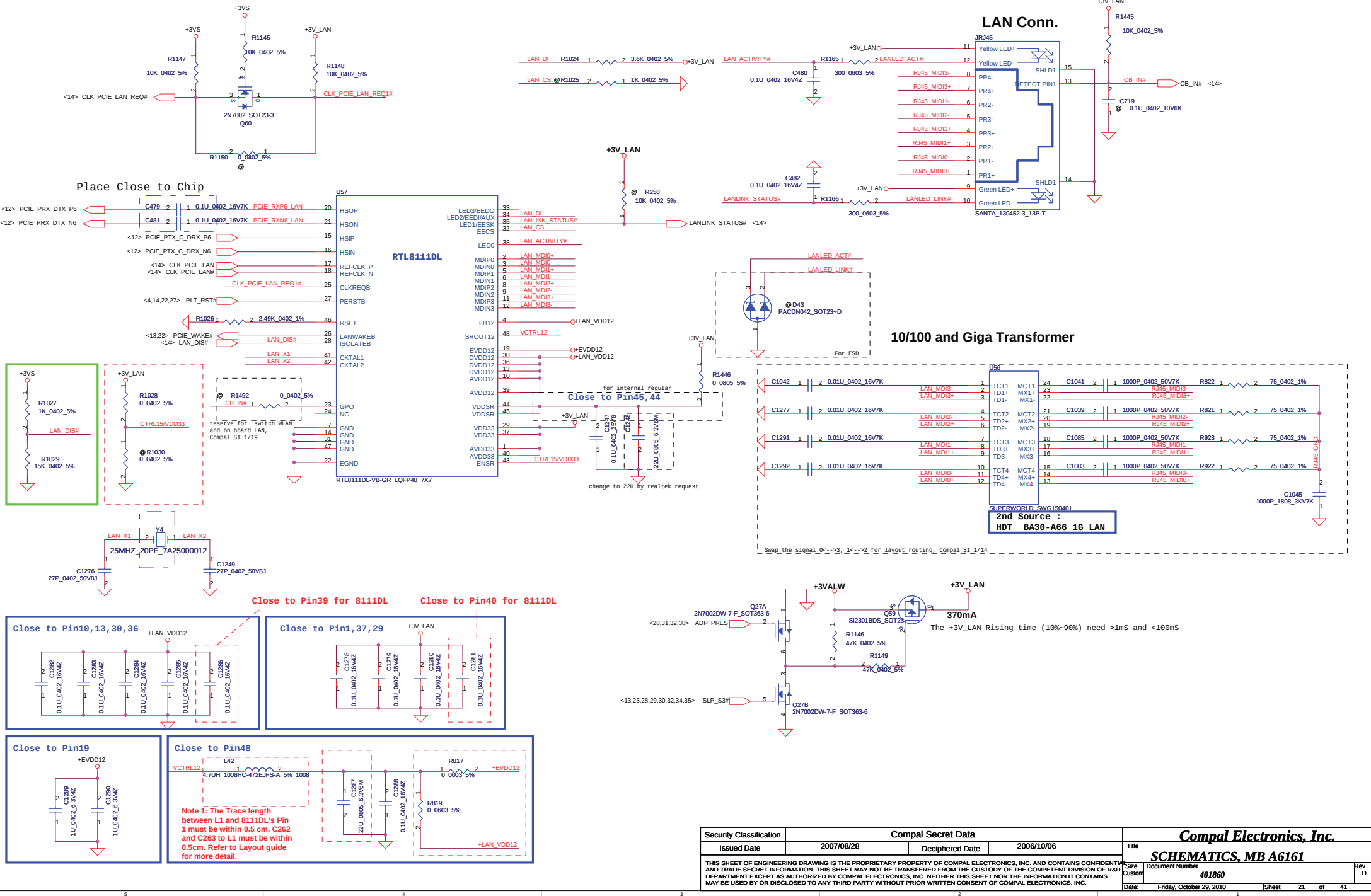
HDD active LED



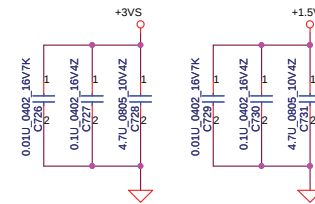
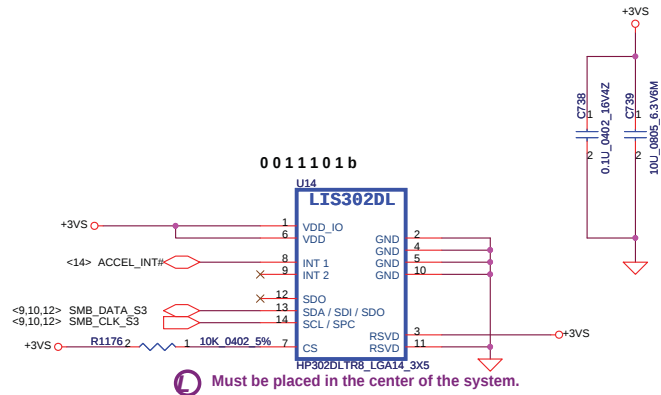
To LED small board



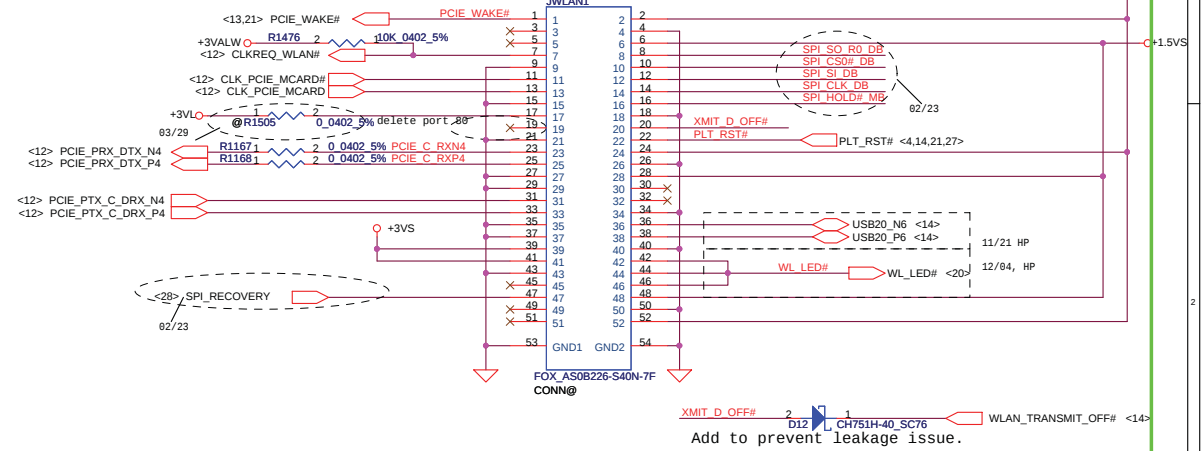
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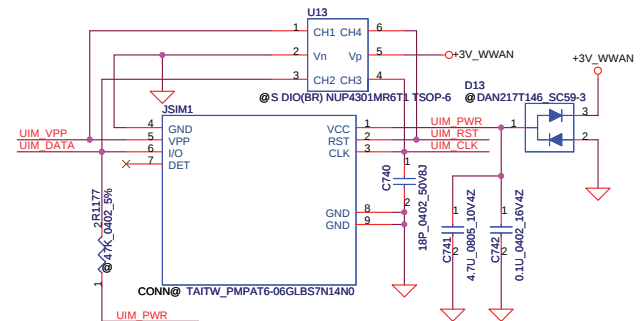
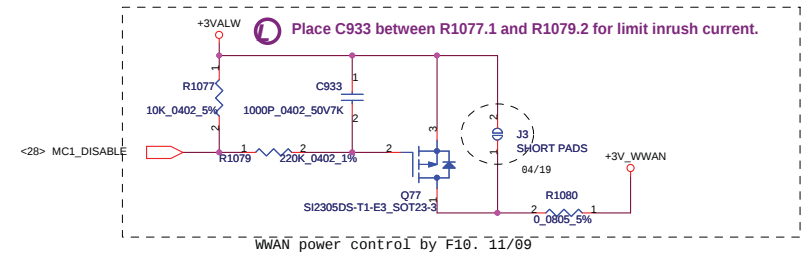
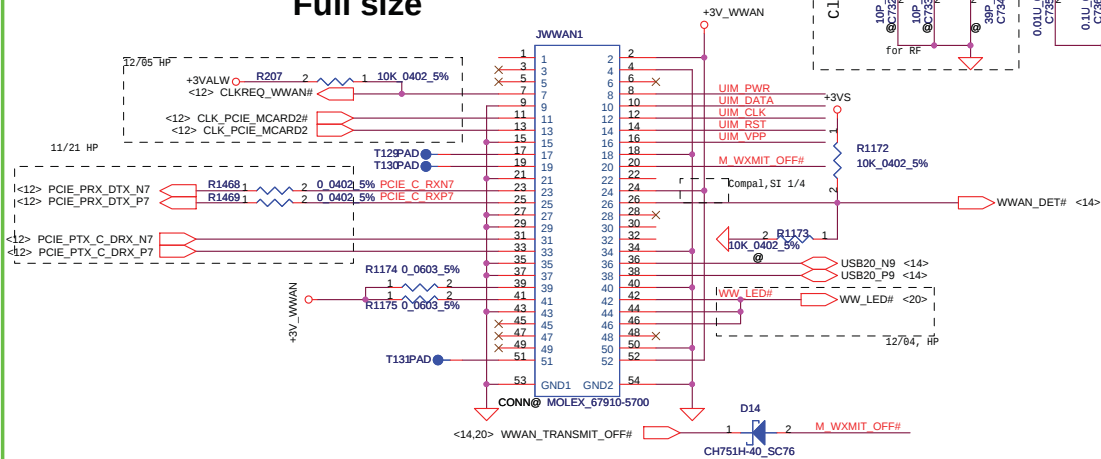
ACCELEROMETER



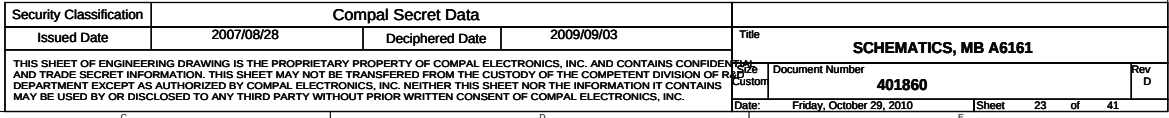
WWLAN/WiMax Mini-Express Card half size

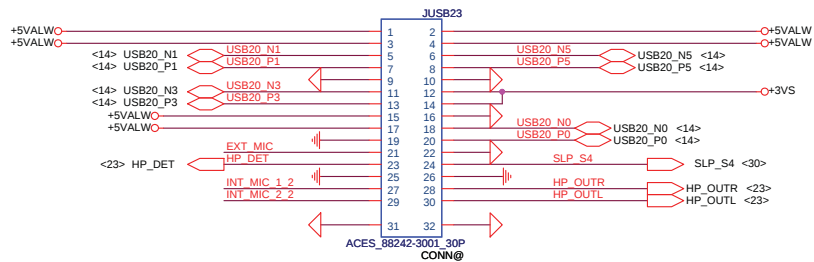


Mini-Express Card--WWAN Full size

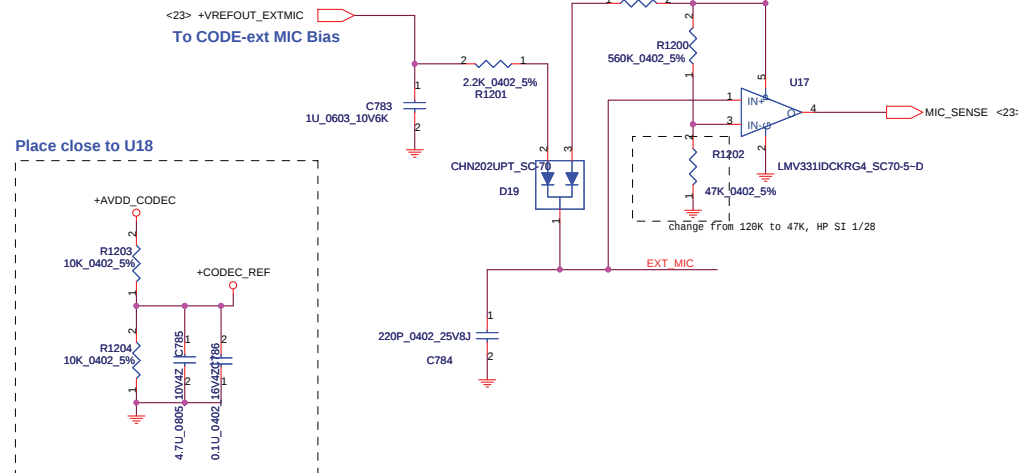


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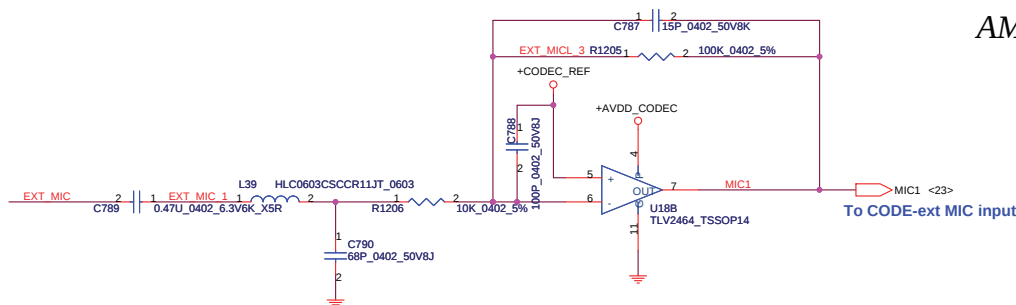




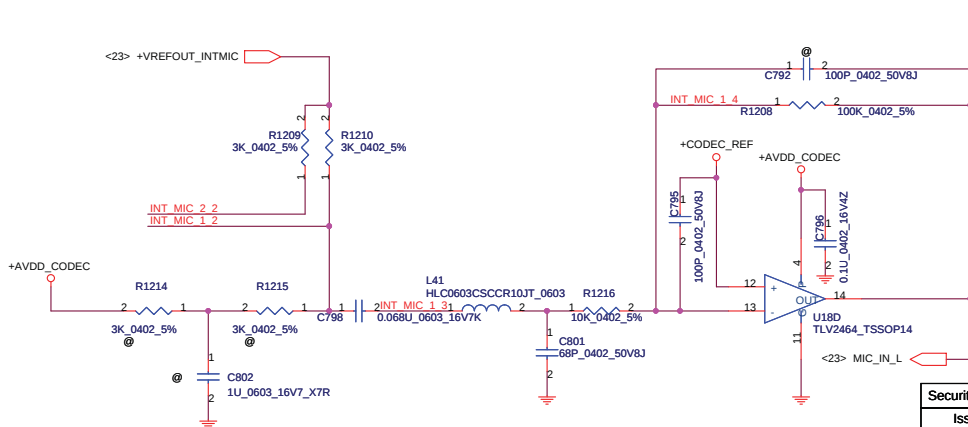
USB I/O connx2 , Aduio JACK
Card reader transfer conn



AMP. FOR EXTERNAL MICROPHONE



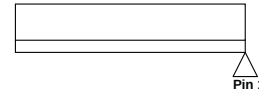
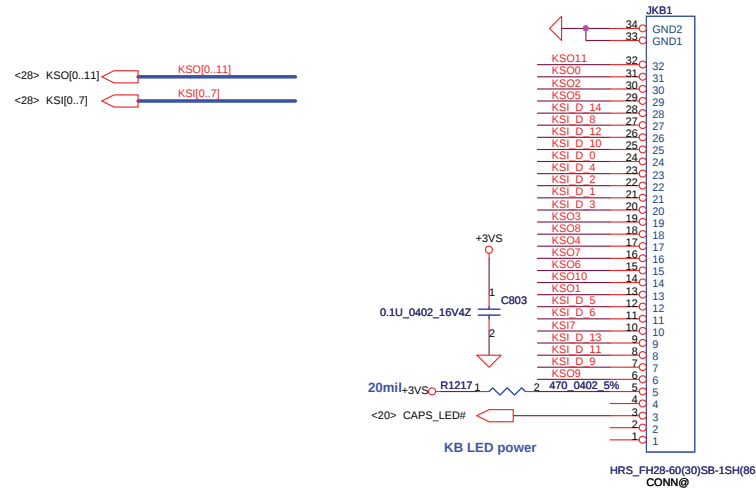
AMP. FOR INTERNAL MICROPHONE



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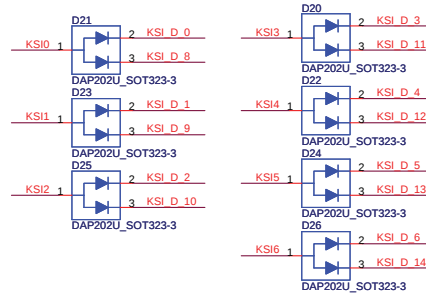
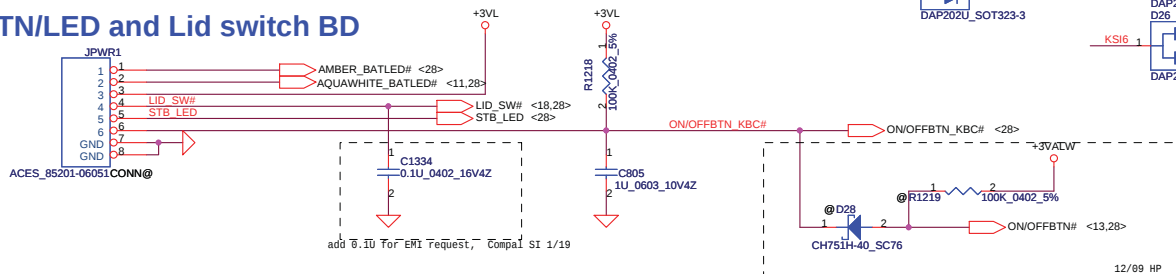
INT_KBD CONN.



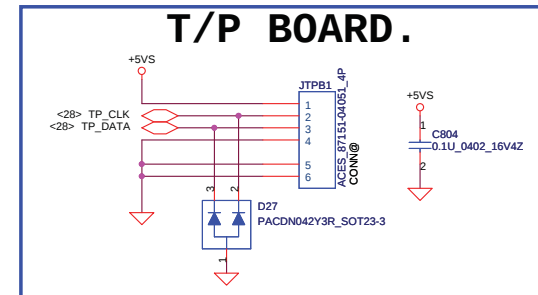
Pin1 reserve , so net name is reserve
for Fossil down contact

KSO11	@ C620	1	2	100P_0402_50V8J
KSO0	@ C656	1	2	100P_0402_50V8J
KSO2	@ C624	1	2	100P_0402_50V8J
KSO5	@ C621	1	2	100P_0402_50V8J
KSI_D_14	@ C622	1	2	100P_0402_50V8J
KSI_D_8	@ C625	1	2	100P_0402_50V8J
KSI_D_12	@ C626	1	2	100P_0402_50V8J
KSI_D_10	@ C627	1	2	100P_0402_50V8J
KSI_D_0	@ C630	1	2	100P_0402_50V8J
KSI_D_4	@ C629	1	2	100P_0402_50V8J
KSI_D_2	@ C631	1	2	100P_0402_50V8J
KSI_D_1	@ C632	1	2	100P_0402_50V8J
KSI_D_3	@ C633	1	2	100P_0402_50V8J
KSO3	@ C634	1	2	100P_0402_50V8J
KSO4	@ C637	1	2	100P_0402_50V8J
KSO7	@ C657	1	2	100P_0402_50V8J
KSO6	@ C638	1	2	100P_0402_50V8J
KSO10	@ C639	1	2	100P_0402_50V8J
KSO1	@ C640	1	2	100P_0402_50V8J
KSI_D_5	@ C660	1	2	100P_0402_50V8J
KSI_D_6	@ C642	1	2	100P_0402_50V8J
KSI7	@ C659	1	2	100P_0402_50V8J
KSI_D_13	@ C654	1	2	100P_0402_50V8J
KSI_D_11	@ C744	1	2	100P_0402_50V8J
KSI_D_9	@ C745	1	2	100P_0402_50V8J
KSO9	@ C724	1	2	100P_0402_50V8J

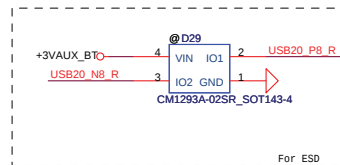
Power BTN/LED and Lid switch BD



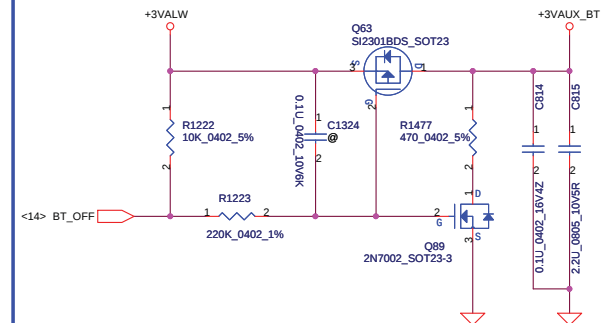
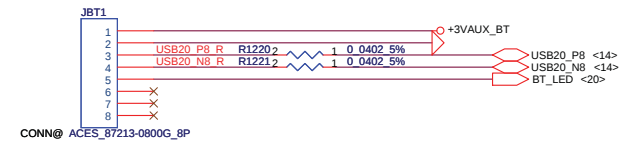
T/P BOARD.



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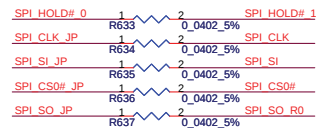
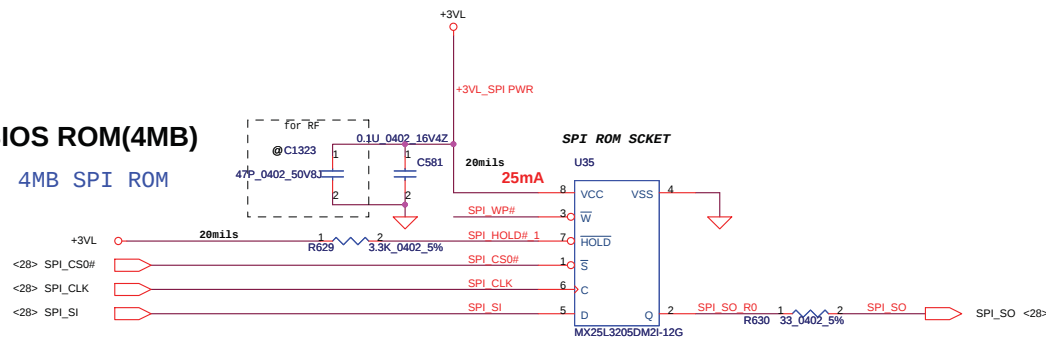
BT(SoftBreeze) Connector



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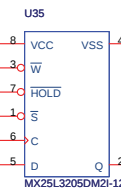
BIOS ROM(4MB)

4MB SPI ROM



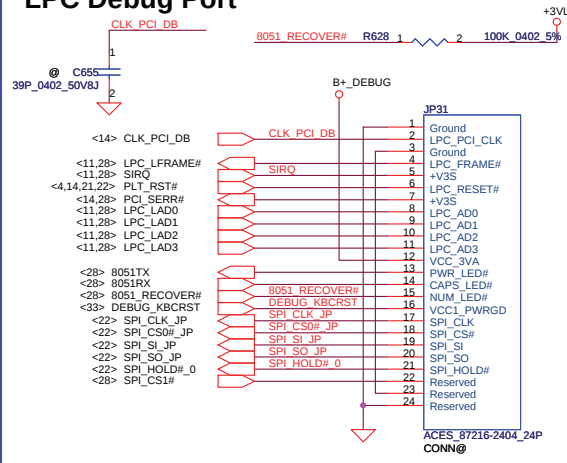
4MB SPI ROM

SPI ROM SCKET



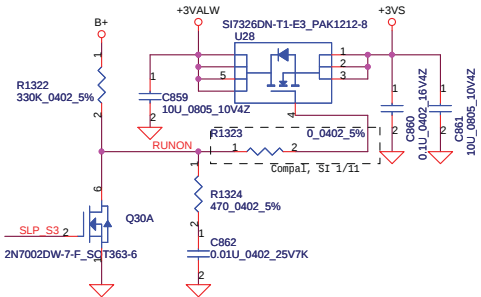
2nd Source :
WINBOND 32M W25Q32BVSSIG
EON 32M EN25F32-100HIP

LPC Debug Port

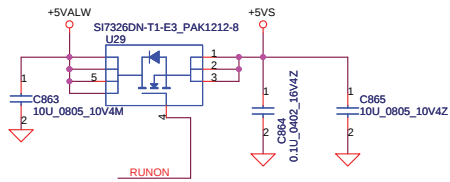


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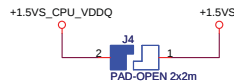
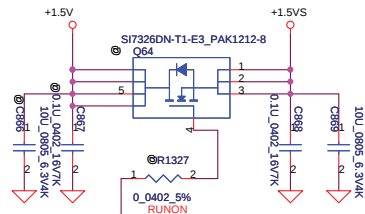
+3VALW to +3VS Transfer



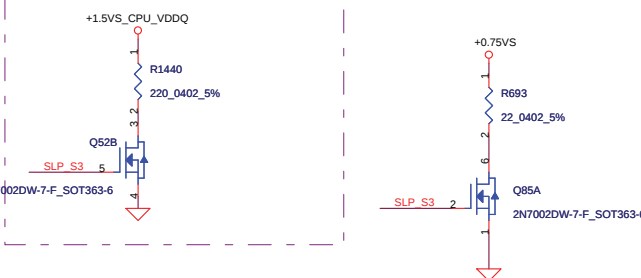
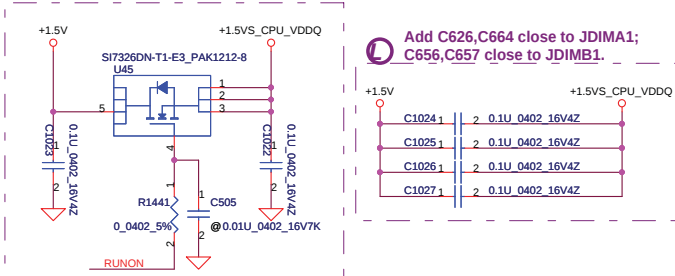
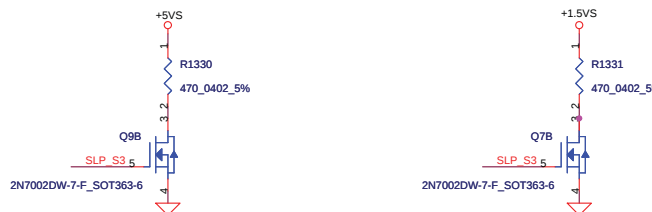
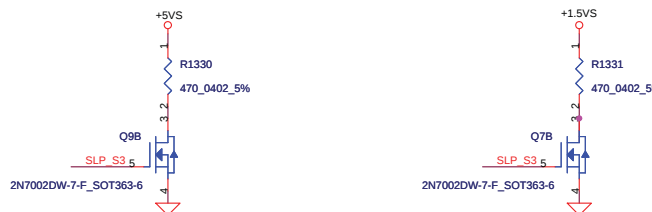
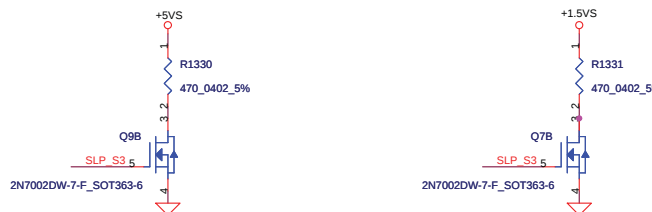
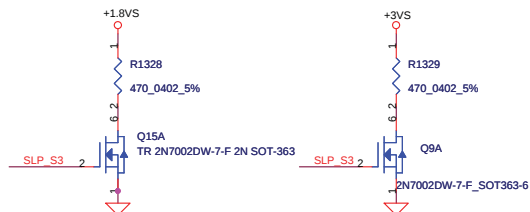
+5VALW to +5VS Transfer



+1.5V to +1.5VS Transfer

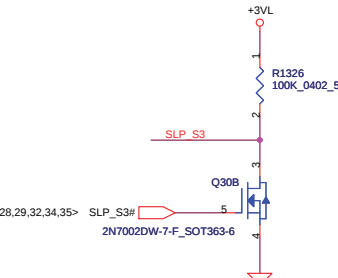
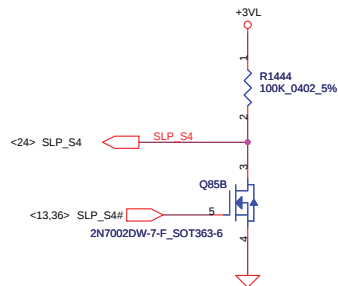
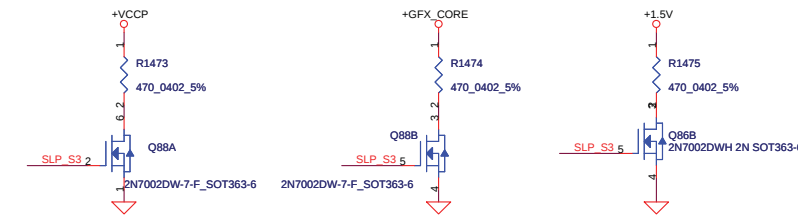


Discharge circuit-1

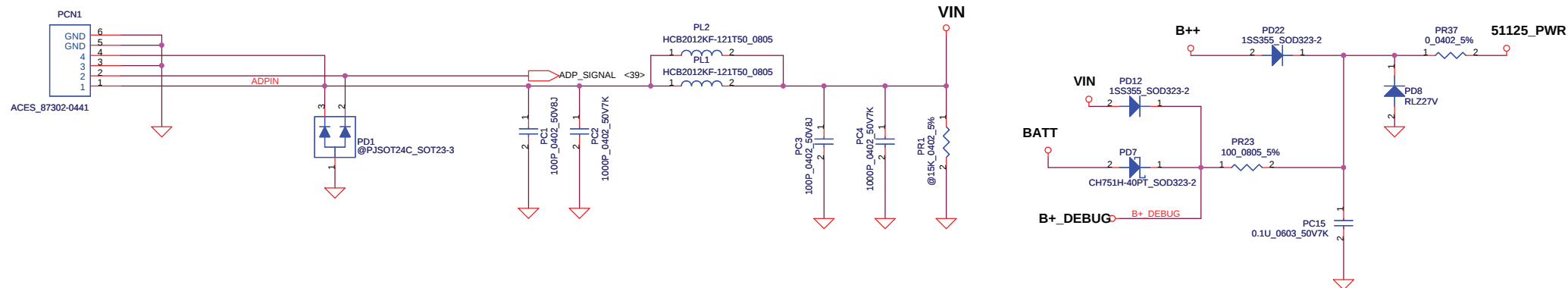


Intel S3 power reduction circuit for Calpella. 11/09

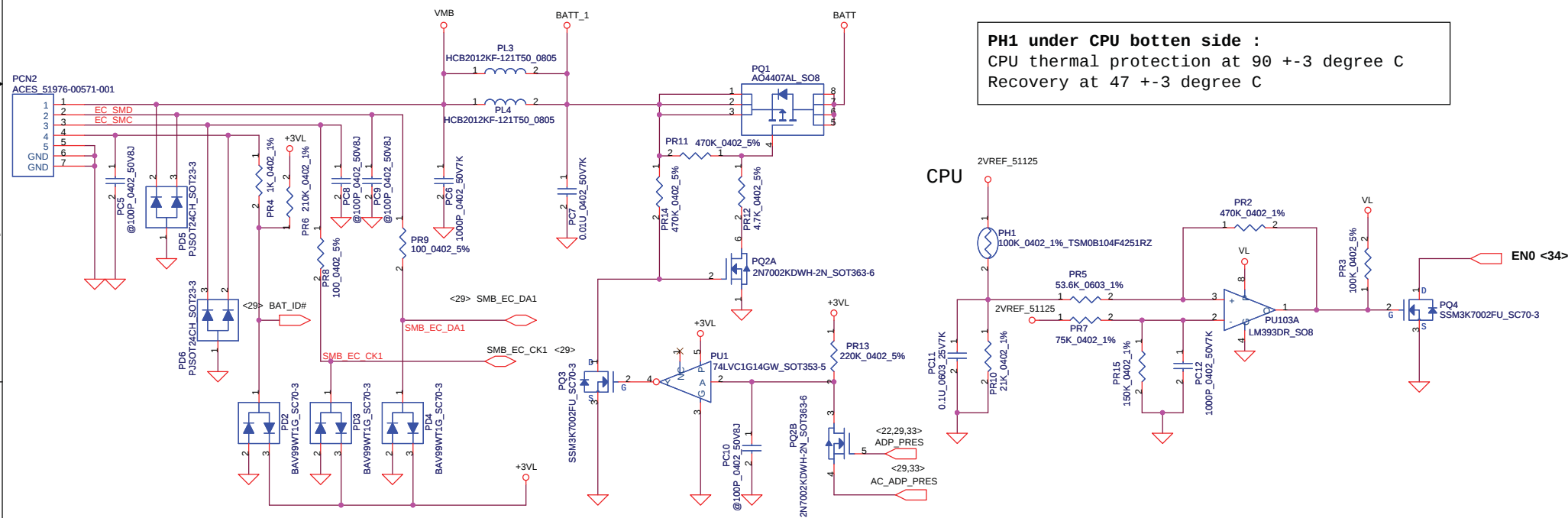
discharge circuit-2



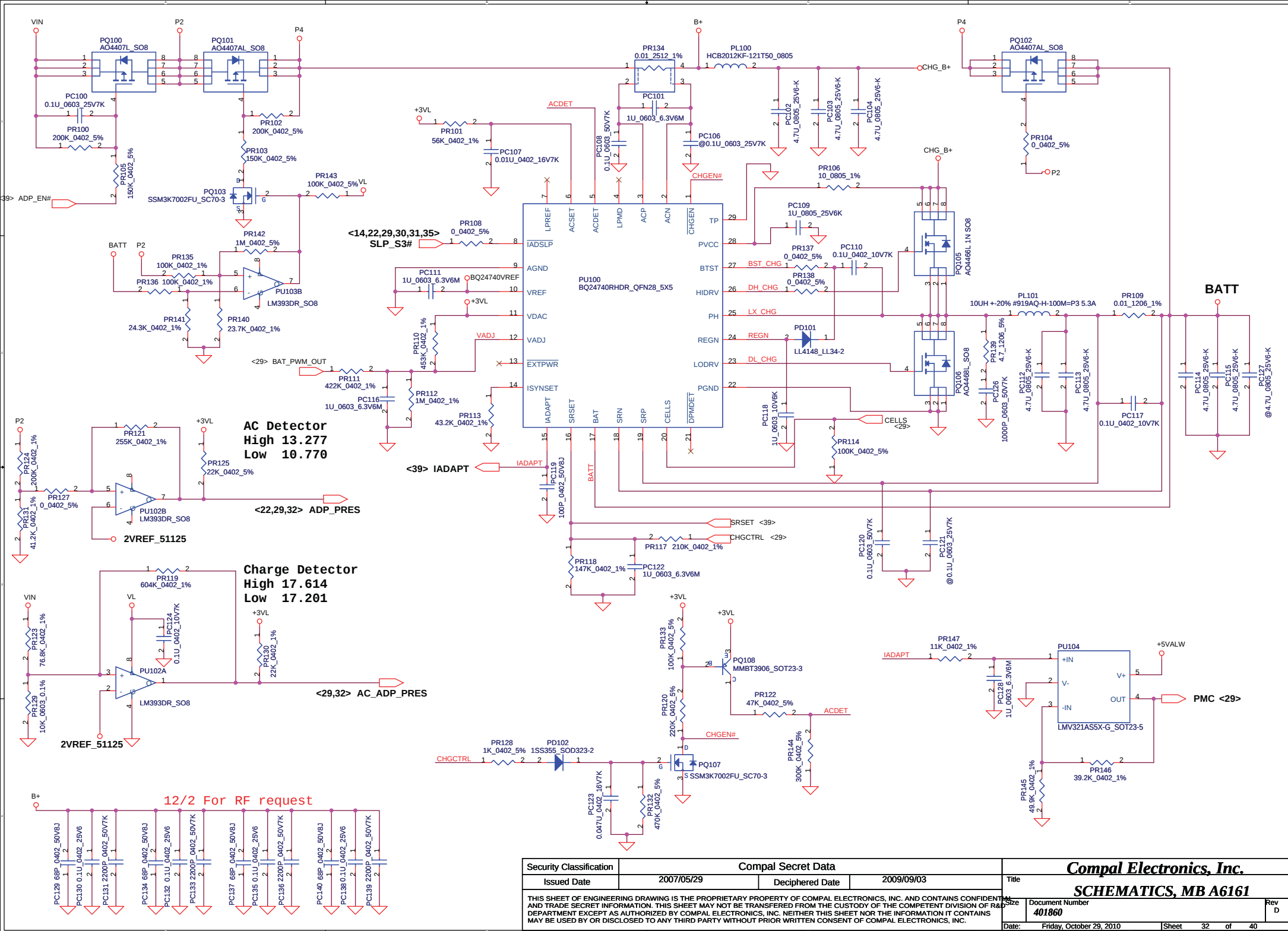
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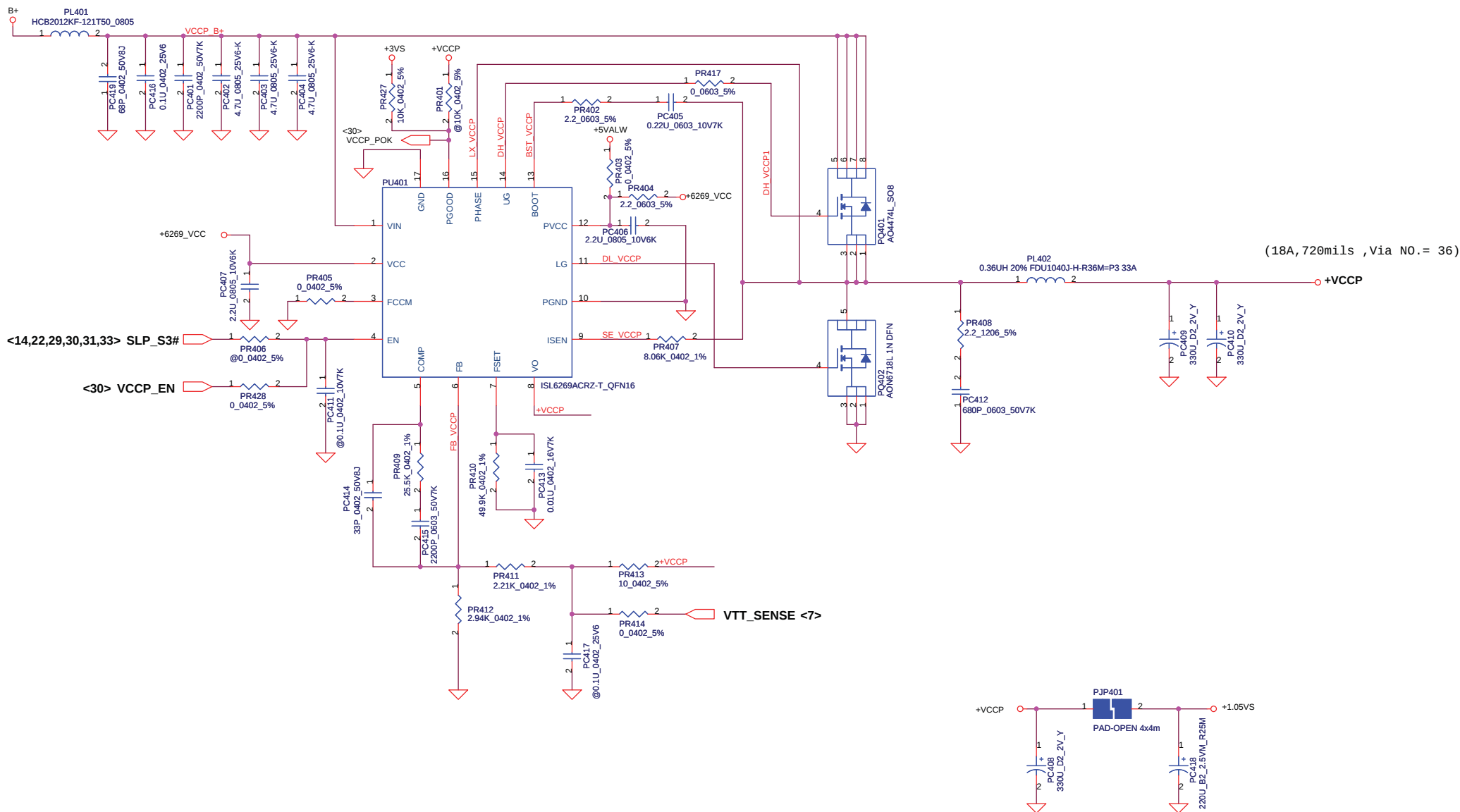


PH1 under CPU bottom side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C

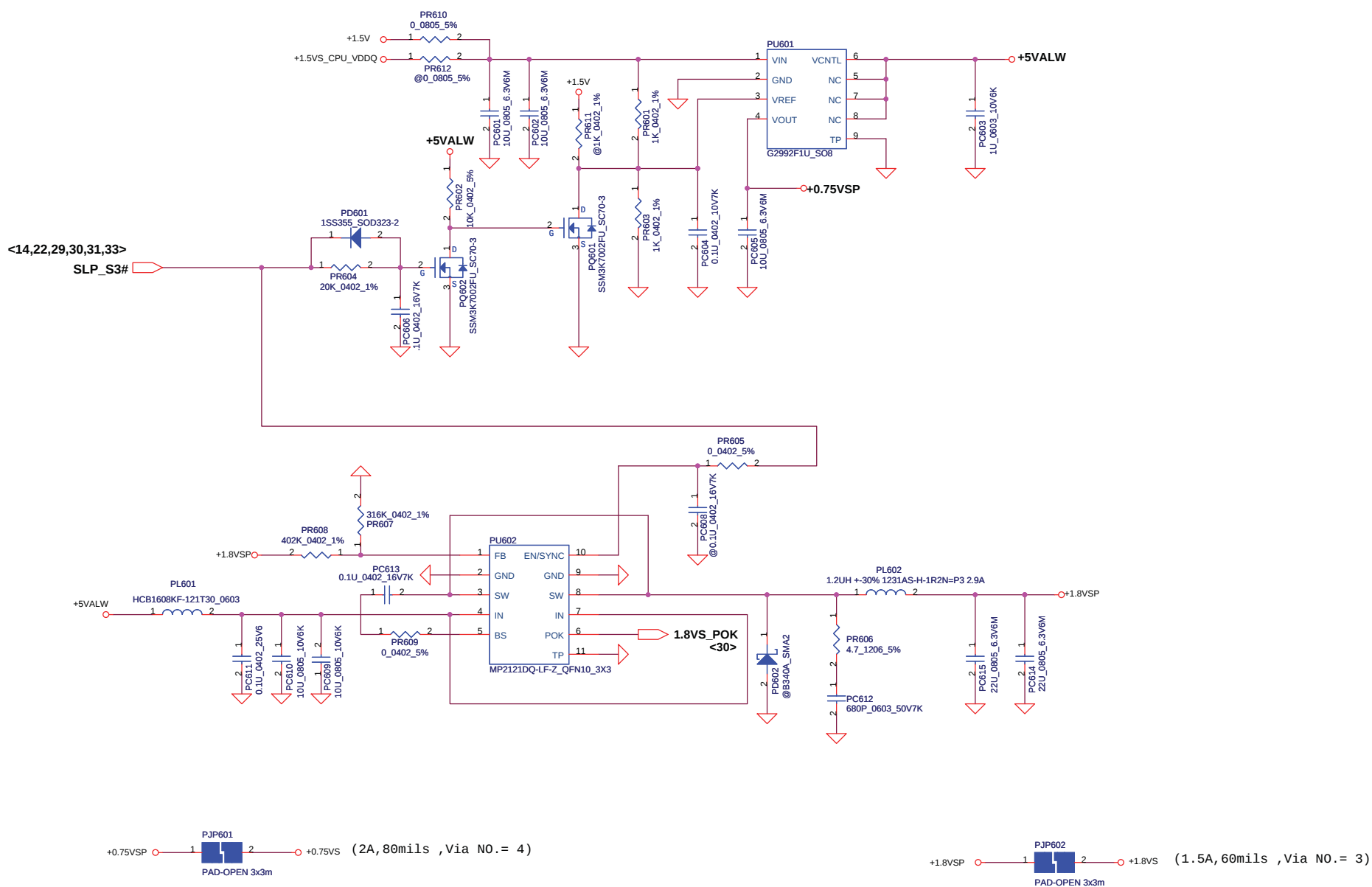


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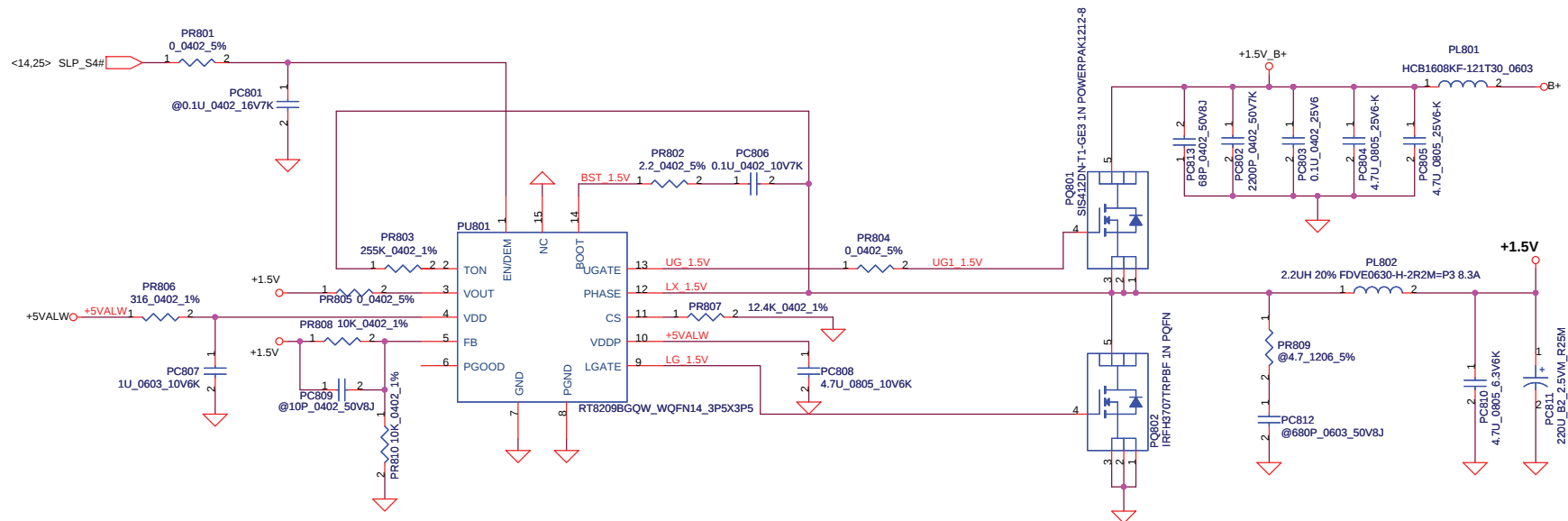




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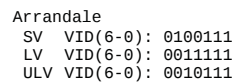


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Version Change List (P. I. R. List) for HW Circuit

[illegible]