Compal Confidential

Intel Haswell rPGA Processor with Lynx Point-H

Afterburn MXM

LA-9371P

2012-11-12

REV : 0.3

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/06/11	Deciphered Date	2013/06/11
Title	Cover Page		
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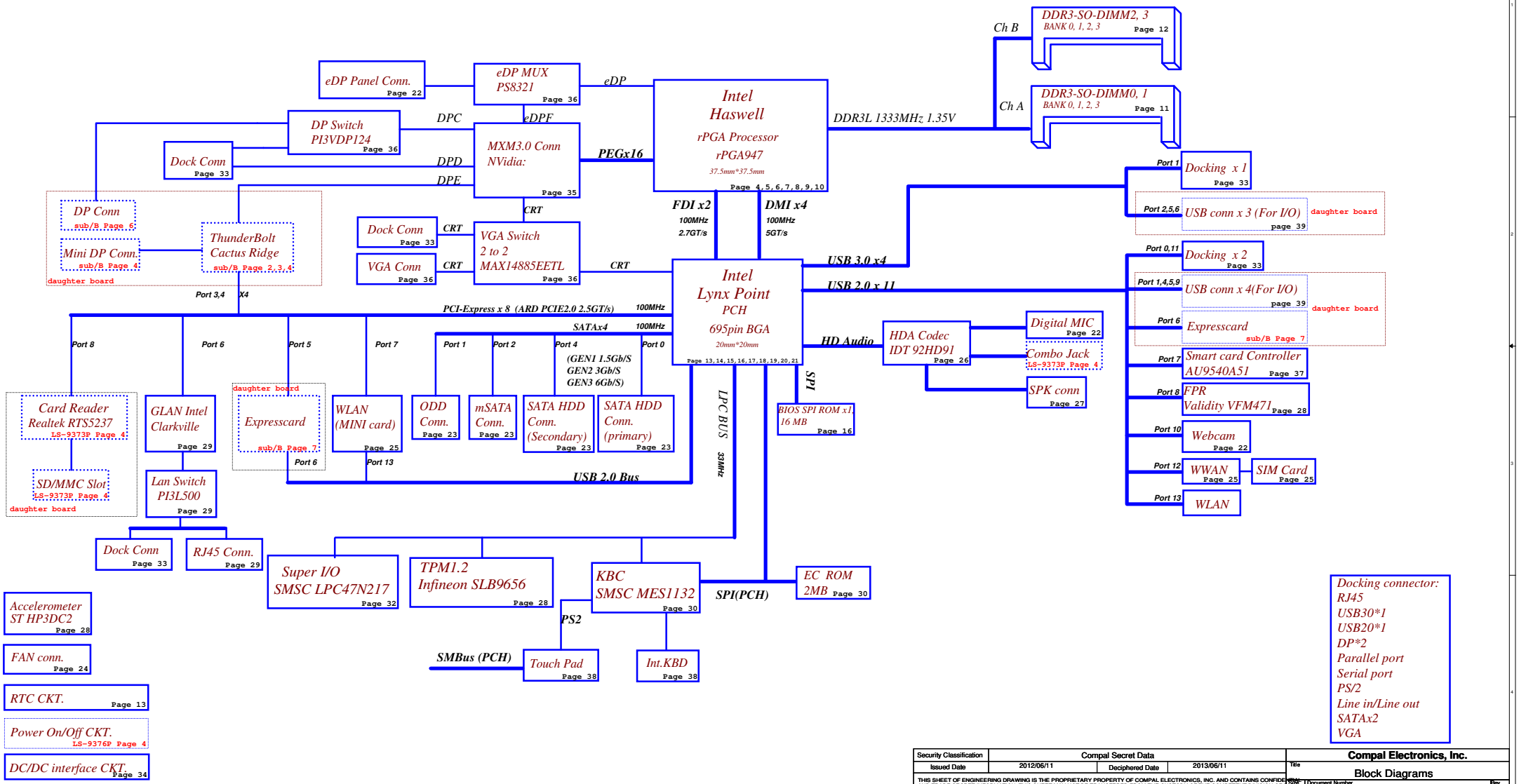
Compal Confidential

Model Name : Afterburn

File Name : LA-9371P



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/06/11	Deciphered Date 2013/06/11	Title: Block Diagrams
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Voltage Rails (O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VDS +3VDS	+1.35V +0.675VS	+5VS +3VS +1.5VS +VCC_CORE +1.05VS +1.05VM	
S0	O	O	O	O	O	
S1	O	O	O	O	O	
S3	O	O	O	O	X	
S5 S4/AC	O	O	O	X	X	
S5 S4/ Battery only	O	O	X	X	X	
S5 S4/AC & Battery don't exist	O	X	X	X	X	

SMBUS Control Table

	SOURCE	BATT	2nd BATT	XDP	SODIMM	G-SENSOR	TP	NIC	NFC	EC	MXM
I2C_MAIN_CLK I2C_MAIN_DAT	SMSC1126	V	X	X	X	X	X	X	X	X	X
I2C_BAY_CLK I2C_BAY_DAT	SMSC1126	X	V	X	X	X	X	X	X	X	X
MEM_SMBCLK MEM_SMBDATA	Haswell	X	X	V	V	V	V	X	X	X	X
LAN_SMBCLK LAN_SMBDATA	Haswell	X	X	X	X	X	X	V	V	X	X
SML1_SMBCLK SML1_SMBDATA	Haswell	X	X	X	X	X	X	X	X	V	V

Stapping Options Flash

GPIO 51 Bit 1	GPIO 19 Bit 0	Boot BIOS Destination
0	0	Reserved
0	1	RSVD
1	0	SPI
1	1	LPC

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build

AMT@ : means just install for support iAMT
CONN@ : means ME part.

Layout Notes

07/24 update

: Question Area Mark.(Wait check)

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.1

DEBUG@ : means just build when PCIE port 80 CARD function enable.*Remove before MP*

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Issued Date	2012/06/11	Deciphered Date 2013/06/11	Title: Notes List
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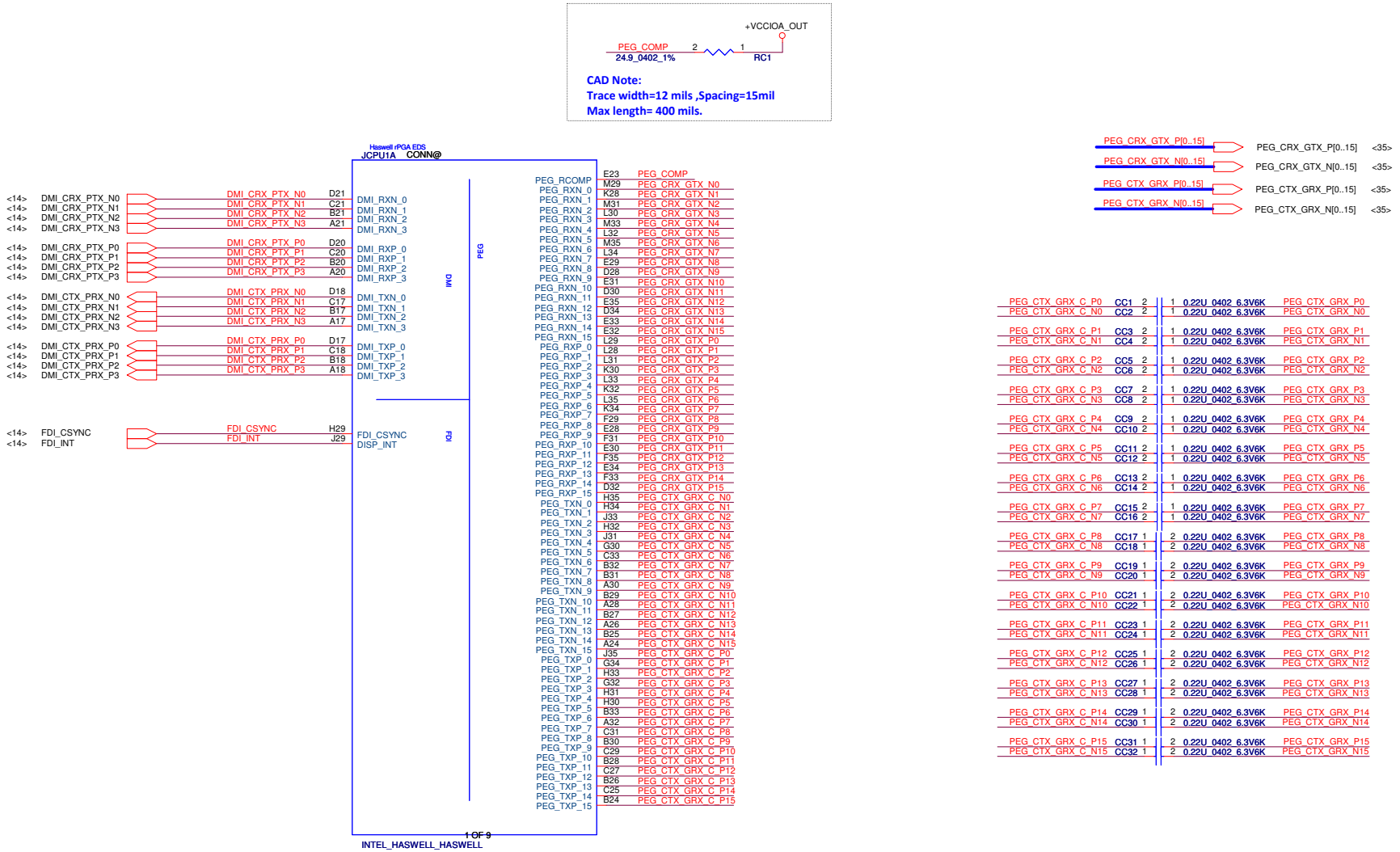

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: DMI,PEG

Size	Document Number	Rev
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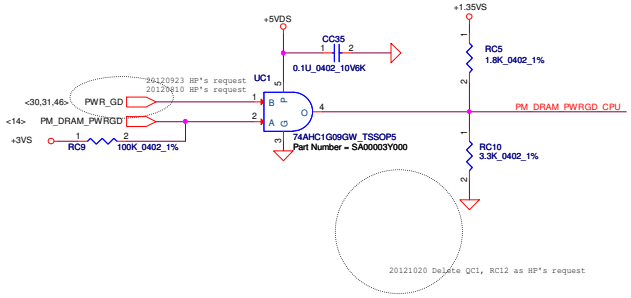
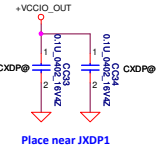
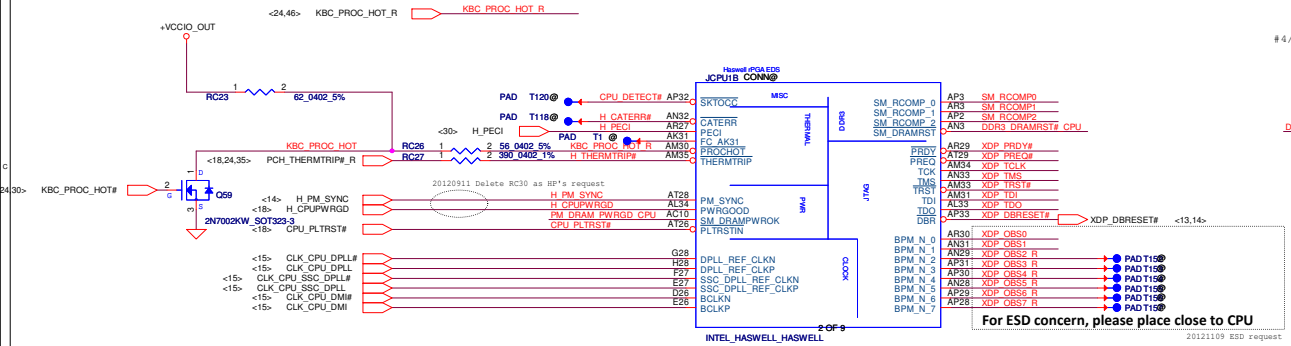
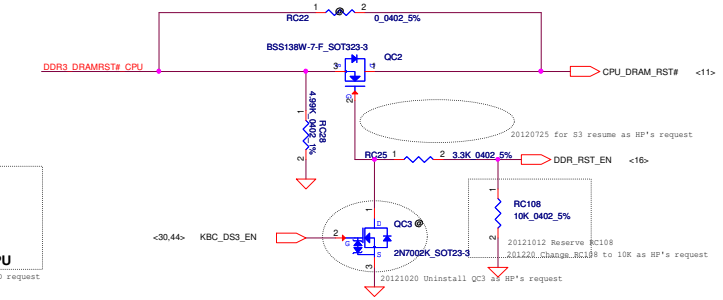
SM_DRAMPWROK with DDR Power Gating Topology

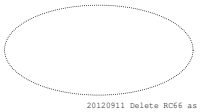


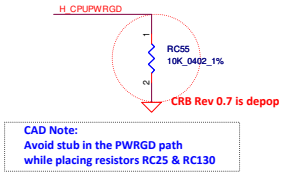


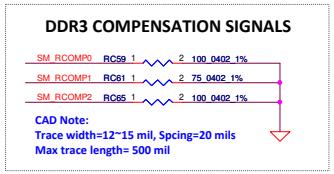




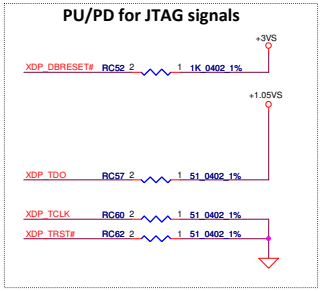
SSC CLOCK TERMINATION, IF NOT USED, stuff RC20,RC21







CRB Rev 0.7 no pull up



Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.			
Title	PM,XDP,CLK		
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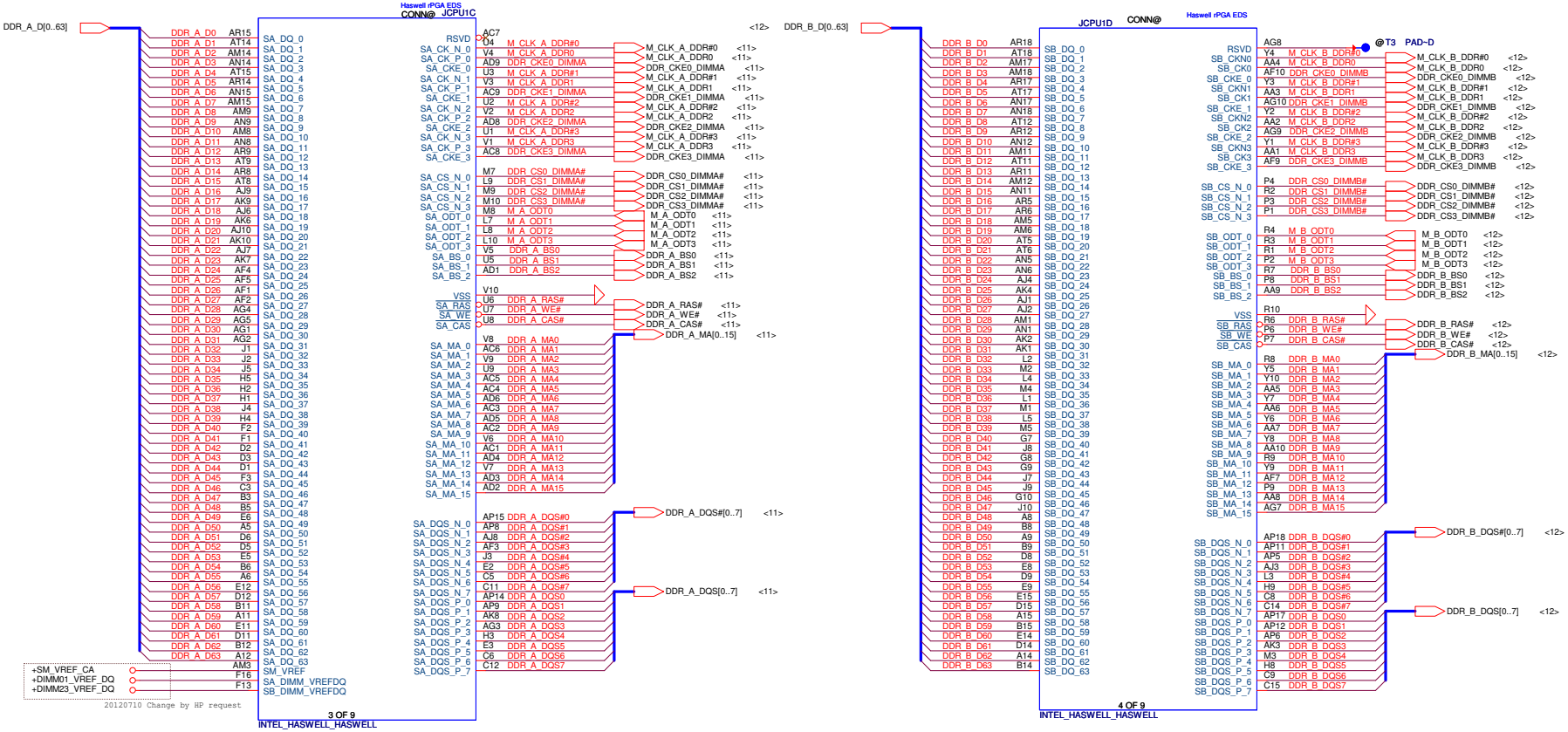

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: DDRIII

Size	Document Number	Rev
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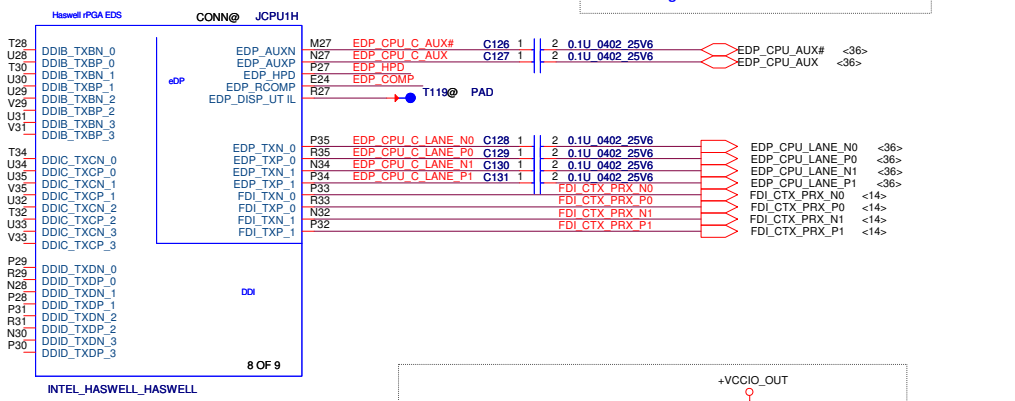

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: CPU-FDI,eDP,DDI

Size	Document Number	Rev
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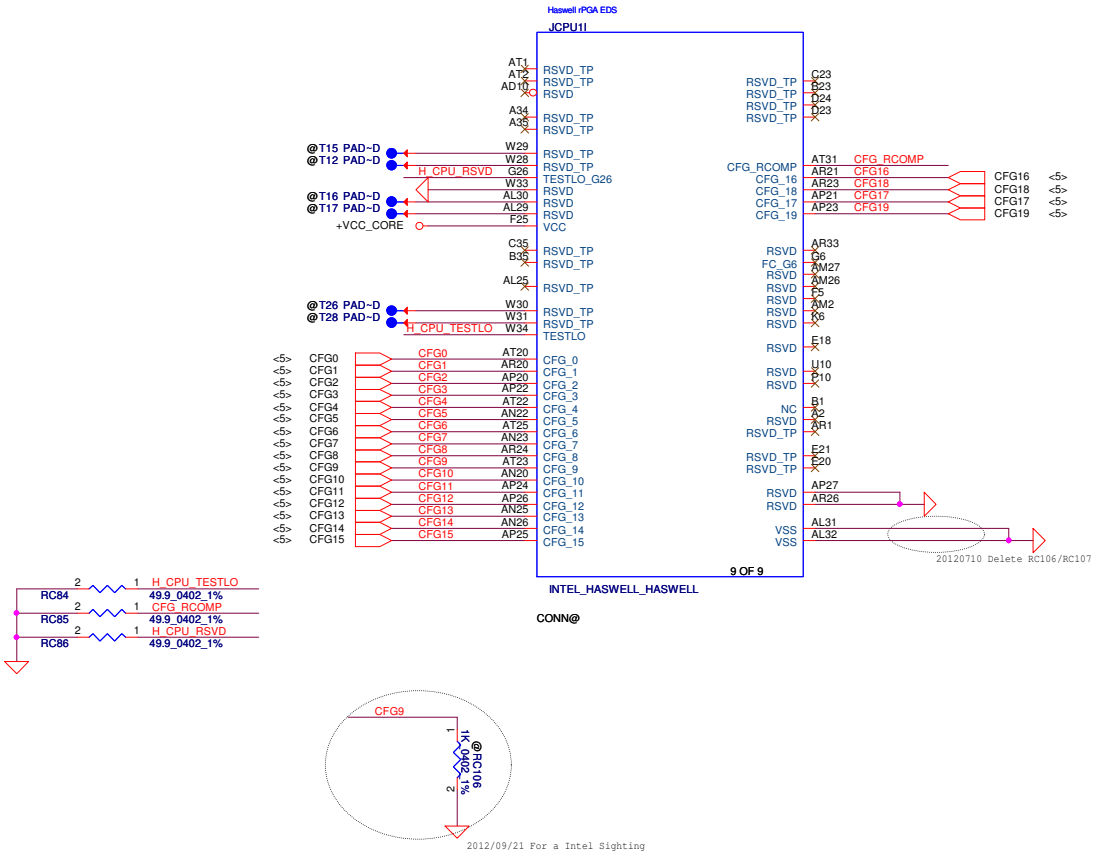
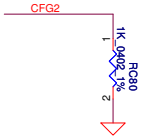
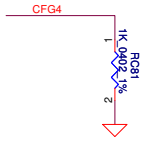
CFG STRAPS for CPU

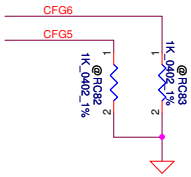




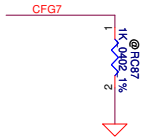
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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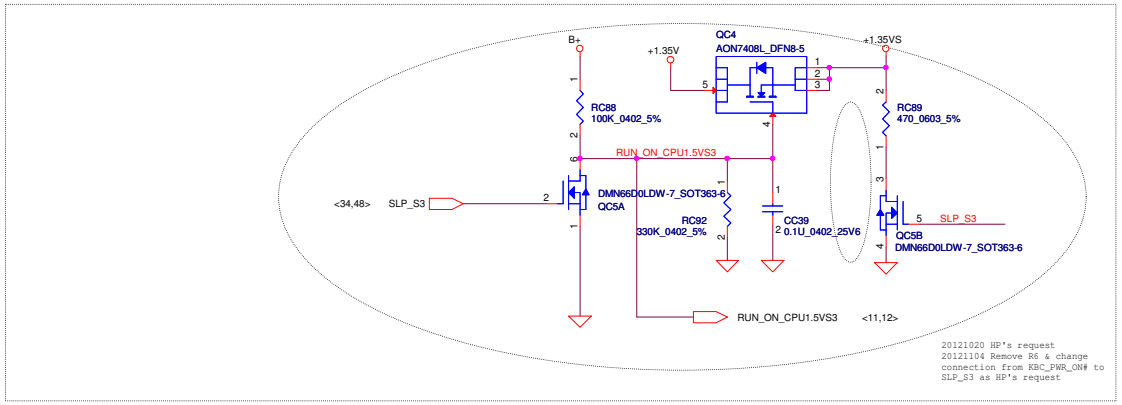
+1.35VS Source

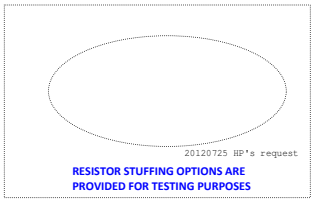


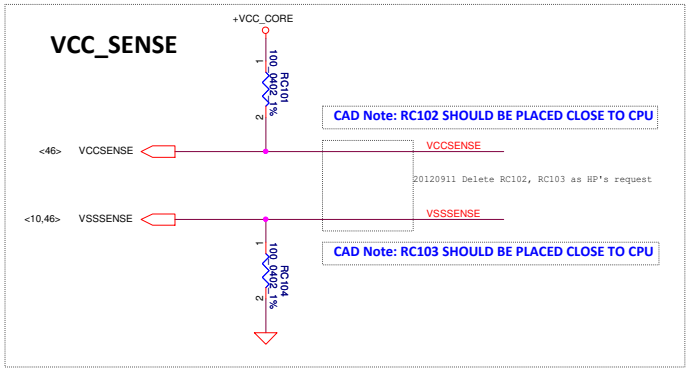
SVID ALERT

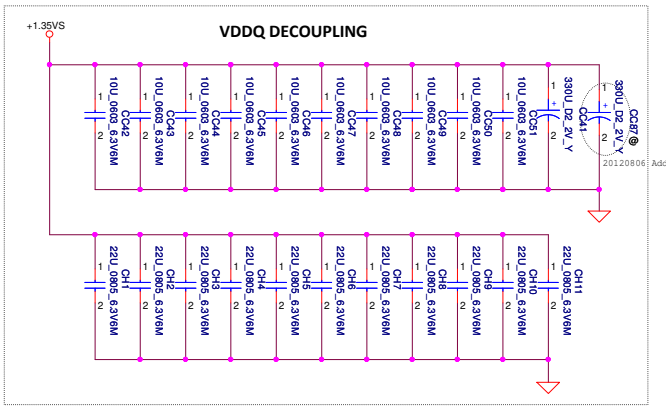
CAD Note: Place the PU resistors close to CPU
RC60 close to CPU 300 - 1500mils

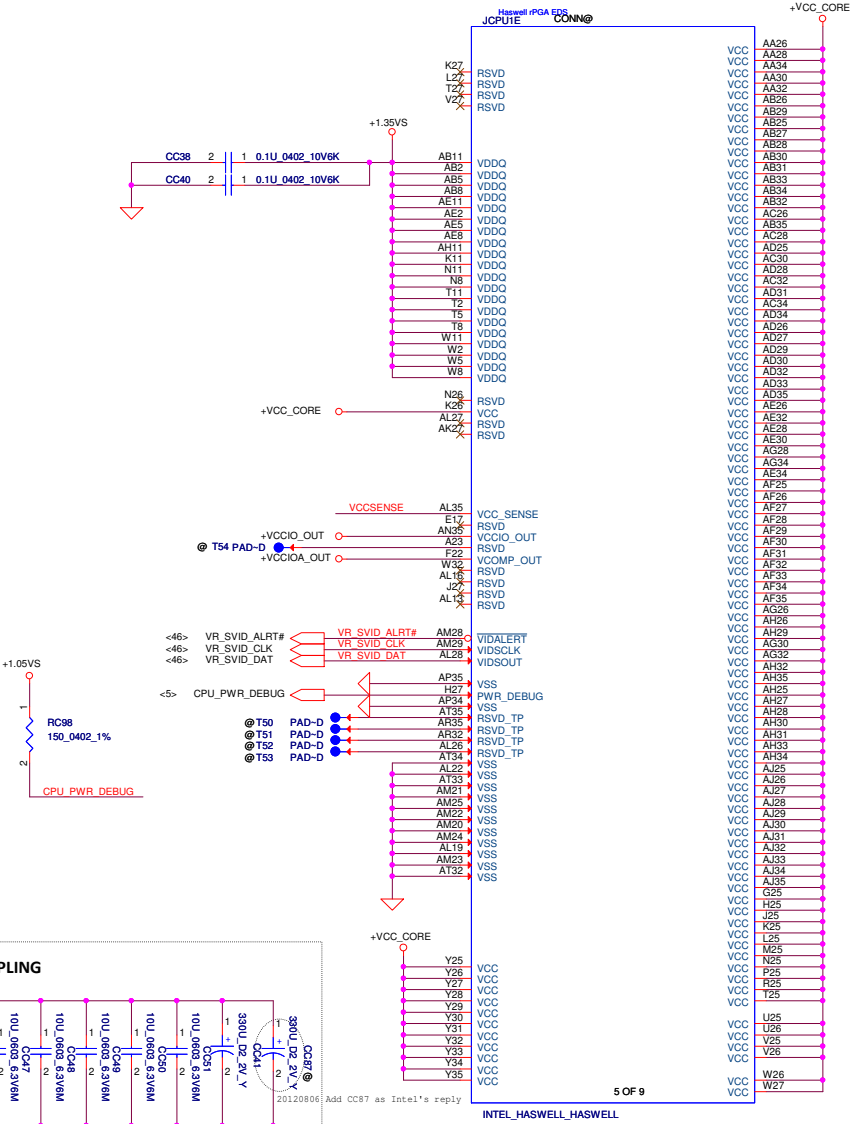
SVID DATA

CAD Note: Place the PU resistors close to CPU
RC63 close to CPU 300 - 1500mils









Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: CPU- PWR

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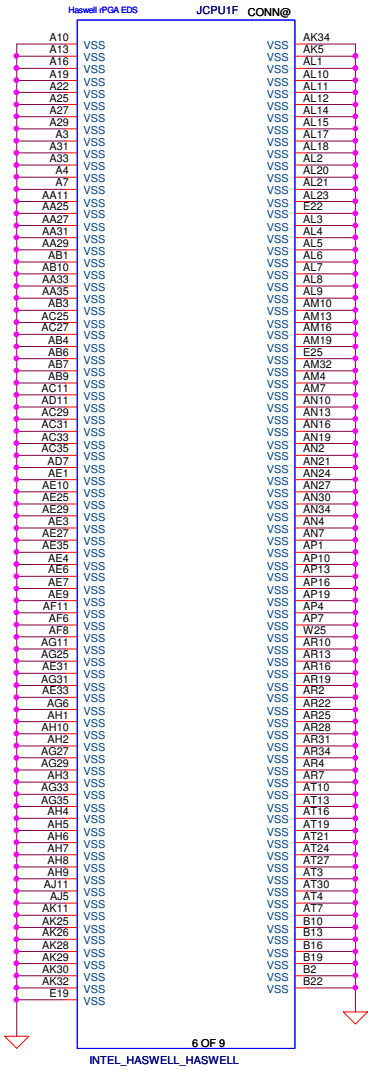

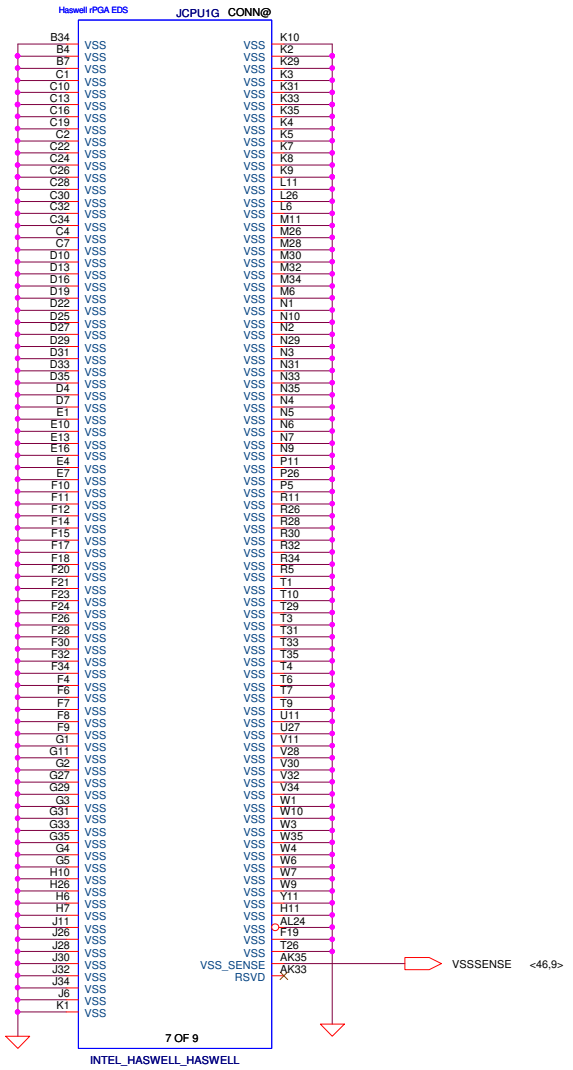

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: CPU-VSS

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Populate RD1, De-Populate RD7 for Intel DDR3
VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3
VREFDQ multiple methods M3

JDIMM1 H=5.2 mm TOP

JDIMM3 H=4.0mm BOT

All VREF traces should have 10 mil trace width

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM1

Layout Note: Place near JDIMM1.203,204

Reverse

Standard

Security Classification	Compal Secret Data		
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Title	DDRIII DIMM1&2
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Compal Electronics, Inc.

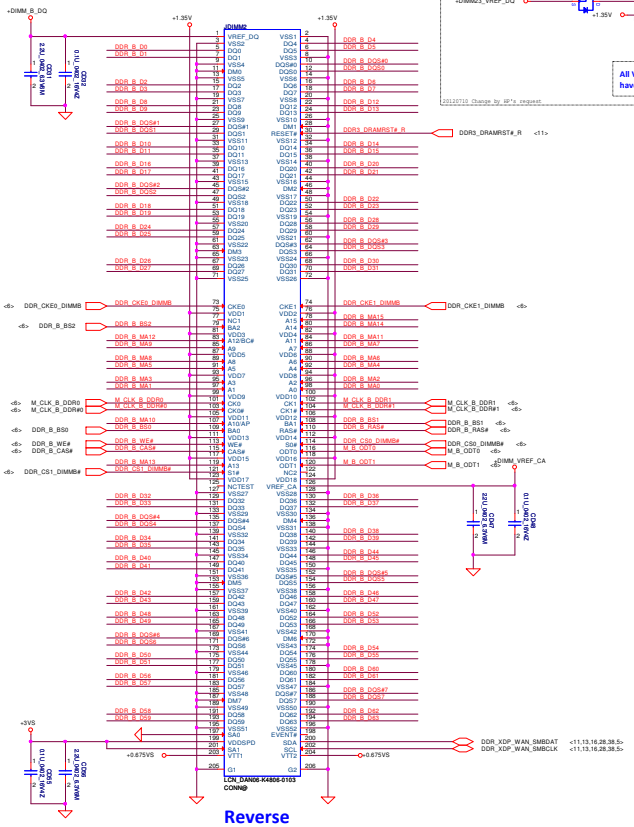
Populate RD4, De-Populate RD8 for Intel DDR3
VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3
VREFDQ multiple methods M3

JDIMM2 H=9.2mm TOP

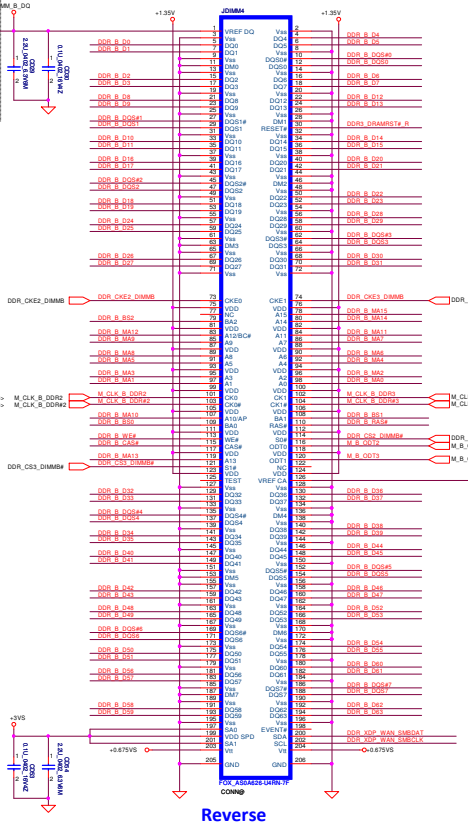
All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM2

Layout Note: Place near JDIMM2.203,204



JDIMM4 H=4.0mm BOT



Reverse

Reverse

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.			
Title: DDRIII DIMM3&4			
Size: Custom	Document Number: LA-9371P		Rev: 0.3
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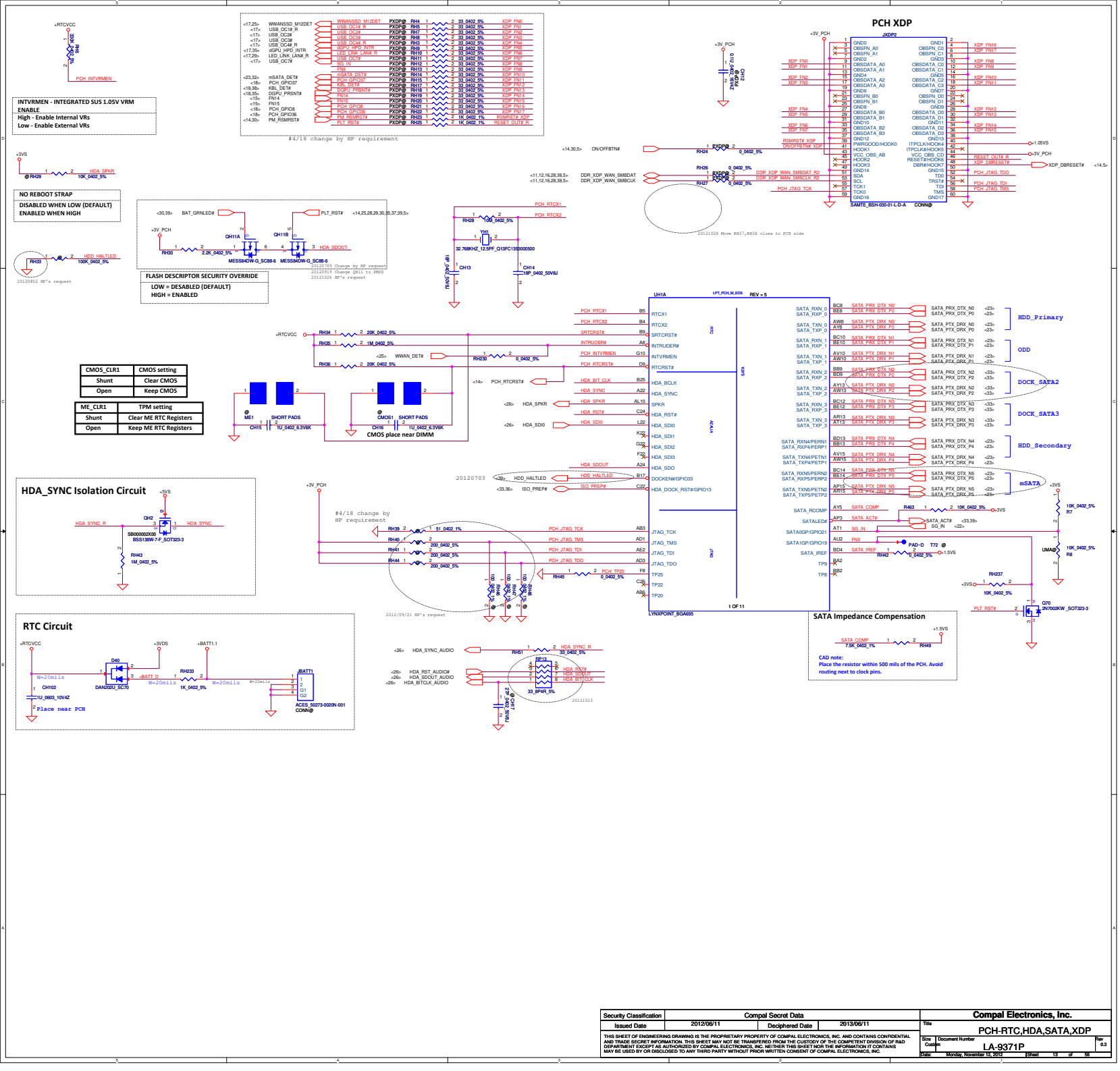
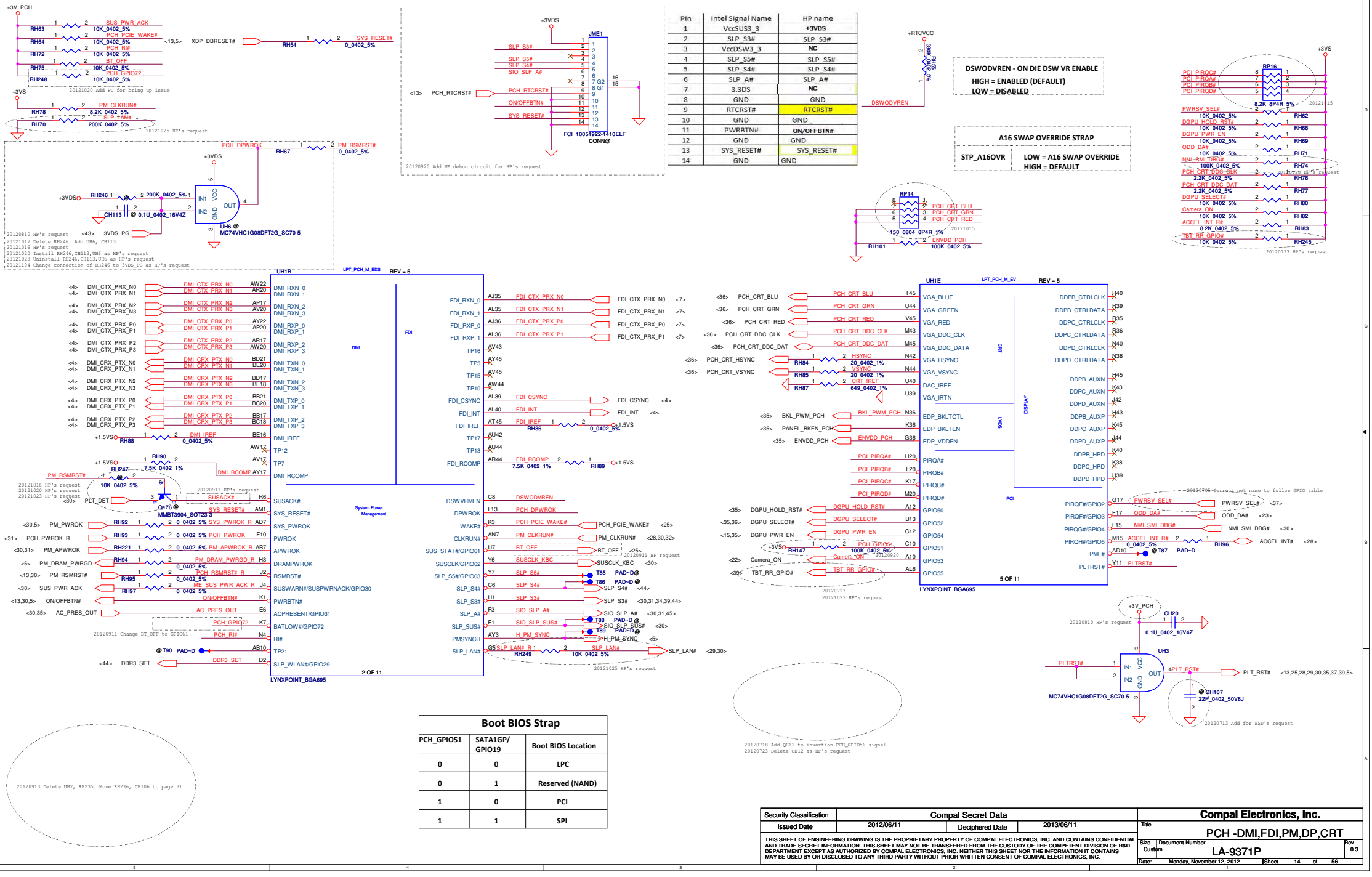

PCH XDP
INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs
NO REBOOT STRAP
DISABLED WHEN LOW (DEFAULT)
ENABLED WHEN HIGH
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED
CMOS_CLR1 | CMOS setting
Shunt | Clear CMOS
Open | Keep CMOS
ME_CLR1 | TPM setting
Shunt | Clear ME RTC Registers
Open | Keep ME RTC Registers
CMOS place near DIMM
HDA_SYNC Isolation Circuit
RTC Circuit
SATA Impedance Compensation
CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.
HDD_Primary
ODD
DOCK_SATA2
DOCK_SATA3
HDD_Secondary
mSATA
Security Classification
Compal Secret Data
Issued Date
2012/06/11
Deciphered Date
2013/06/11
Compal Electronics, Inc.
PCH-RTC,HDA,SATA,XDP
LA-9371P
Monday, November 12, 2012



Pin	Intel Signal Name	HP name
1	VccSUS3_3	+3VDS
2	SLP_S3#	SLP_S3#
3	VccDSW3_3	NC
4	SLP_S5#	SLP_S5#
5	SLP_S4#	SLP_S4#
6	SLP_A#	SLP_A#
7	3.3DS	NC
8	GND	GND
9	RTCRST#	RTCRST#
10	GND	GND
11	PWRBTN#	ON/OFFBTN#
12	GND	GND
13	SYS_RESET#	SYS_RESET#
14	GND	GND

Boot BIOS Strap

PCH_GPIO51	SATA1GP/ GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

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Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: PCH -DMI,FDI,PM,DP,CRT

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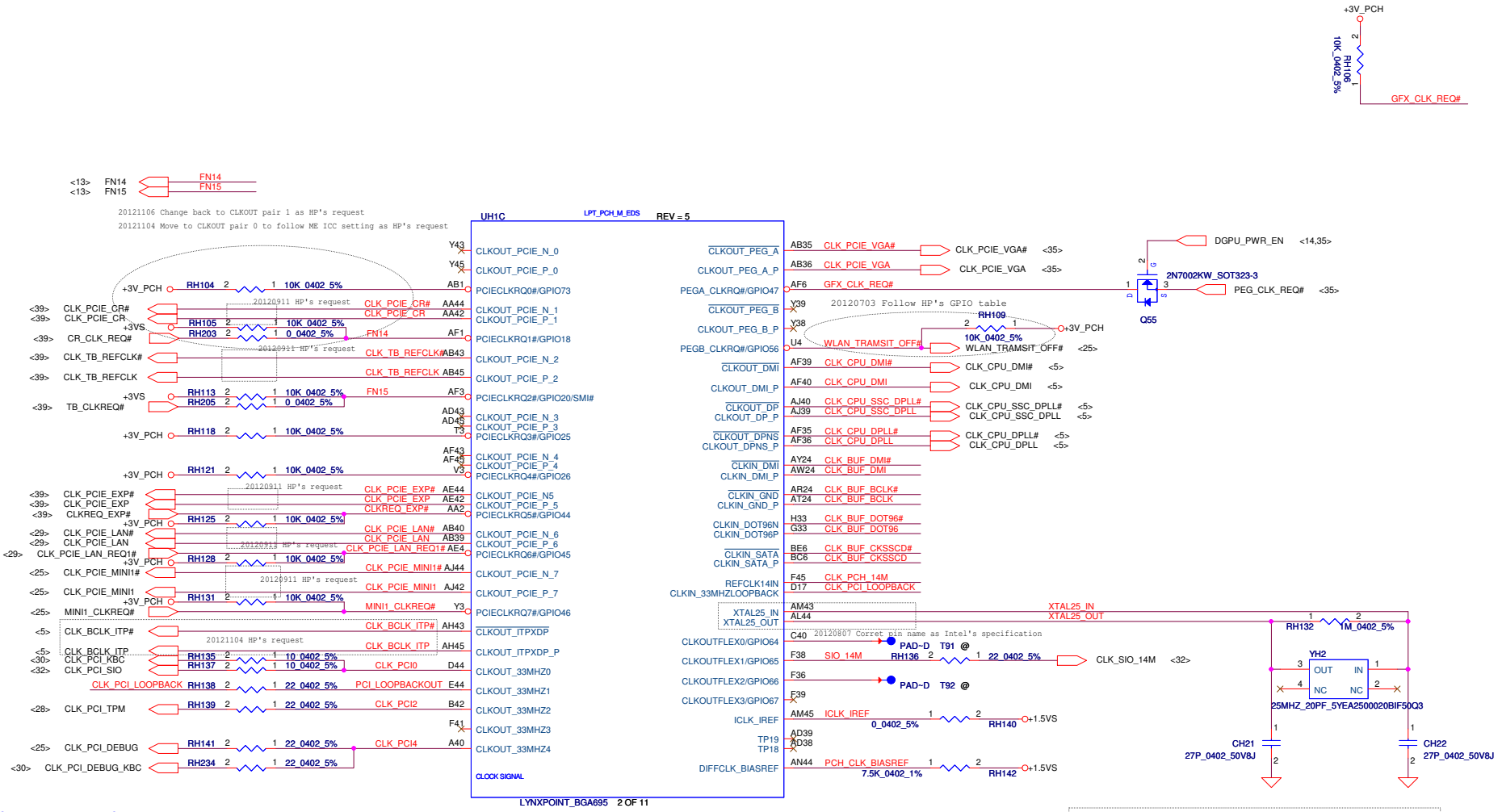

PCIECLK REQ Pull UP Power Rail:
SUS Rail : 0 3 4 5 6 7
Core Rail: 1 2

CLOCK TERMINATION for FCIM and need close to PCH

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Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: PCH- CLK

Size	Document Number	Rev
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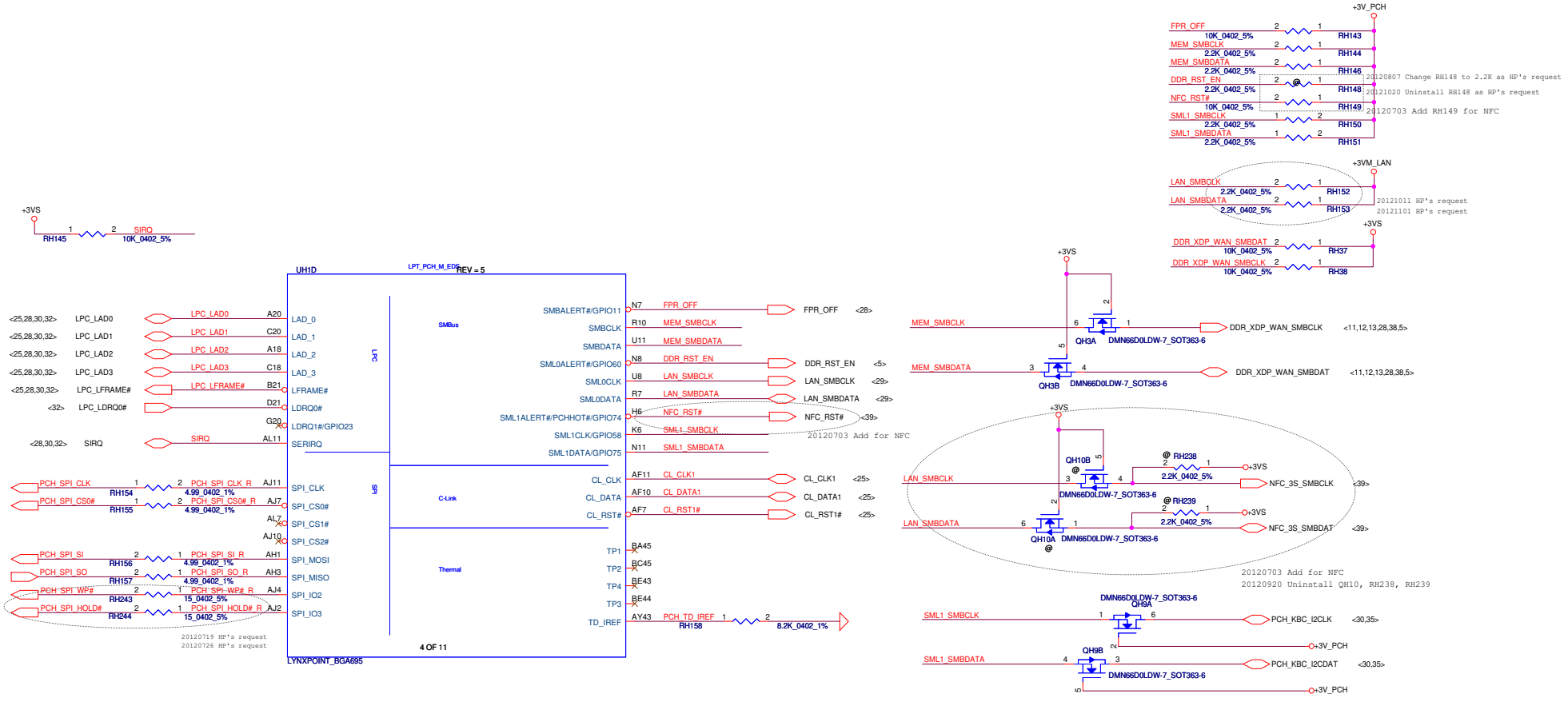

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: PCH - SPI, SMBUS,LPC

Size	Document Number	Rev
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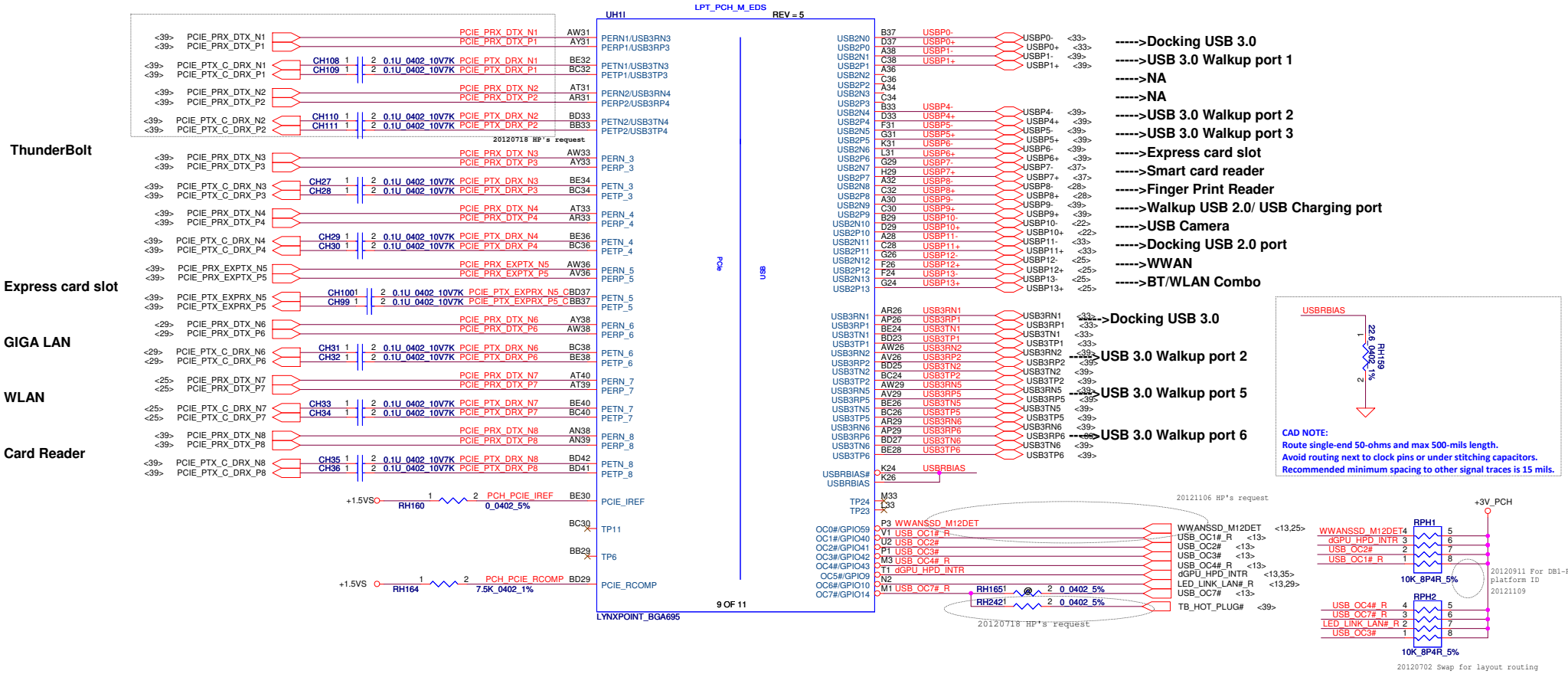

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: PCH-PCIE,USB

Size: Custom | Document Number: LA-9371P | Rev: 0.3

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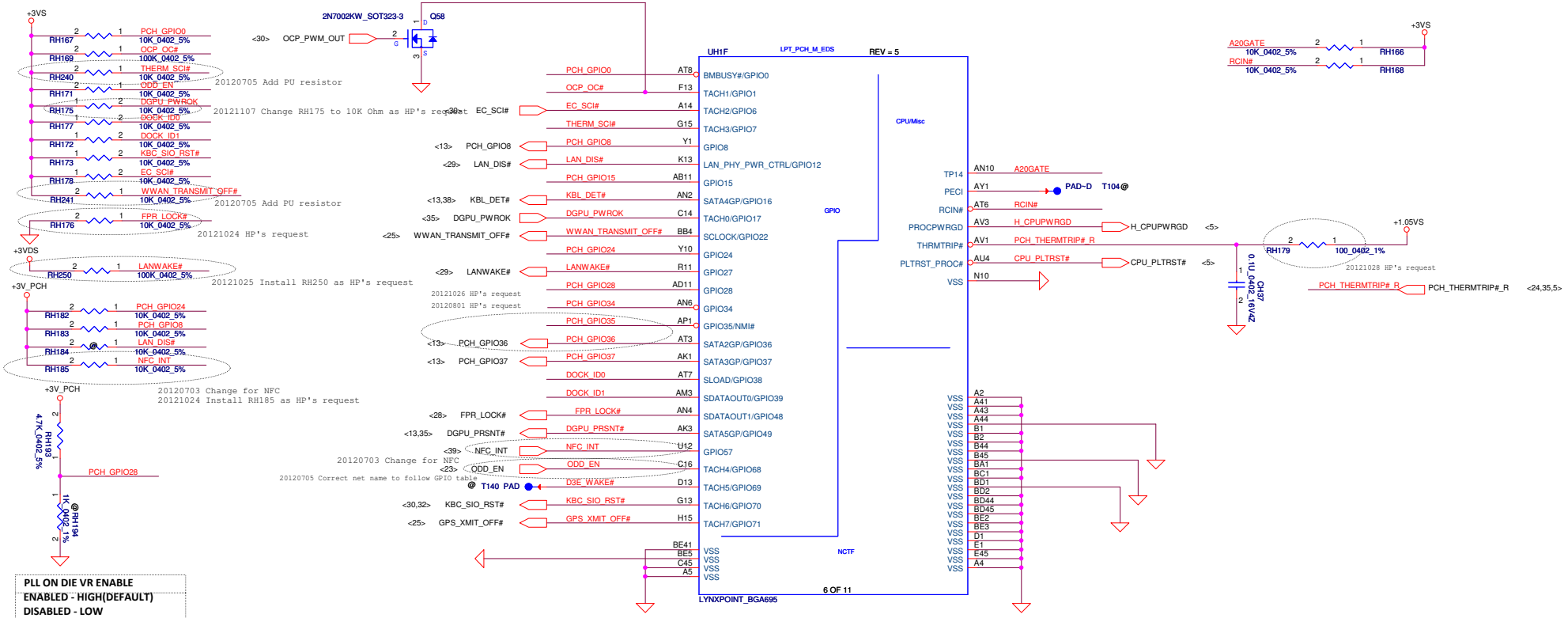

Config	GPIO16,49
USB X4,PCIEX8,SATAX6	11
USB X6,PCIEX8,SATAX4	01

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1 (00)	PCIE 2 (00)	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4 (00)	SATA 5 (00)	SATA 0	SATA 1	SATA 2	SATA 3
				USB3 3 (01)	USB3 4 (01)							PCIE 1 (01)	PCIE 2 (01)				

Board ID	BRD_ID1 GPIO15	BRD_ID2 GPIO34	BRD_ID3 GPIO35	BRD_ID4 GPIO40
DB0	0	0	0	0
DB1	0	0	0	1
DB2	0	0	1	0
SI1	0	1	0	0
SI1B	0	1	0	1
SI2	0	1	1	0
PV1	1	0	0	0
MV	1	1	0	0

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: PCH -GPIO,MISC,NTFC

Size	Document Number	Rev
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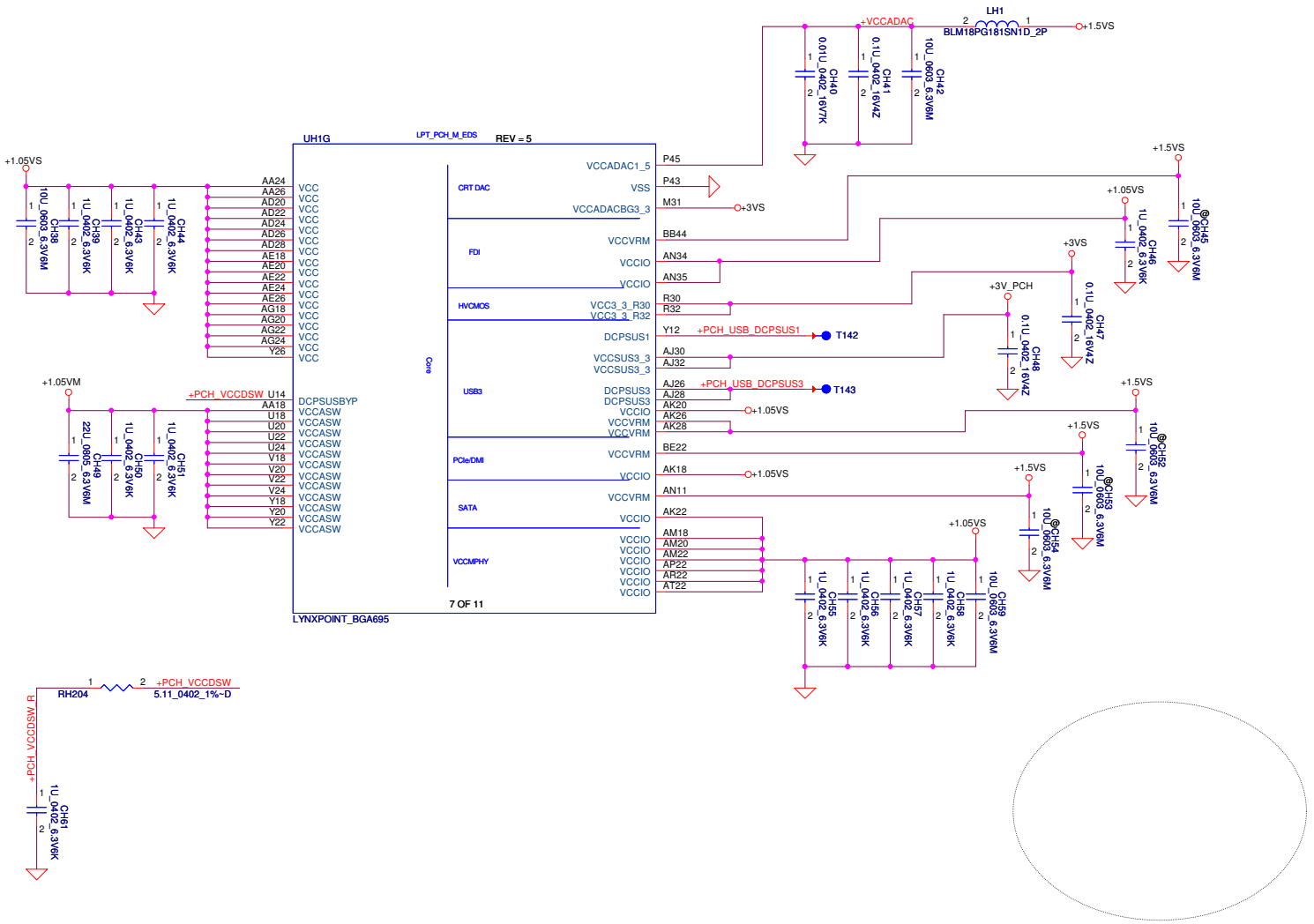

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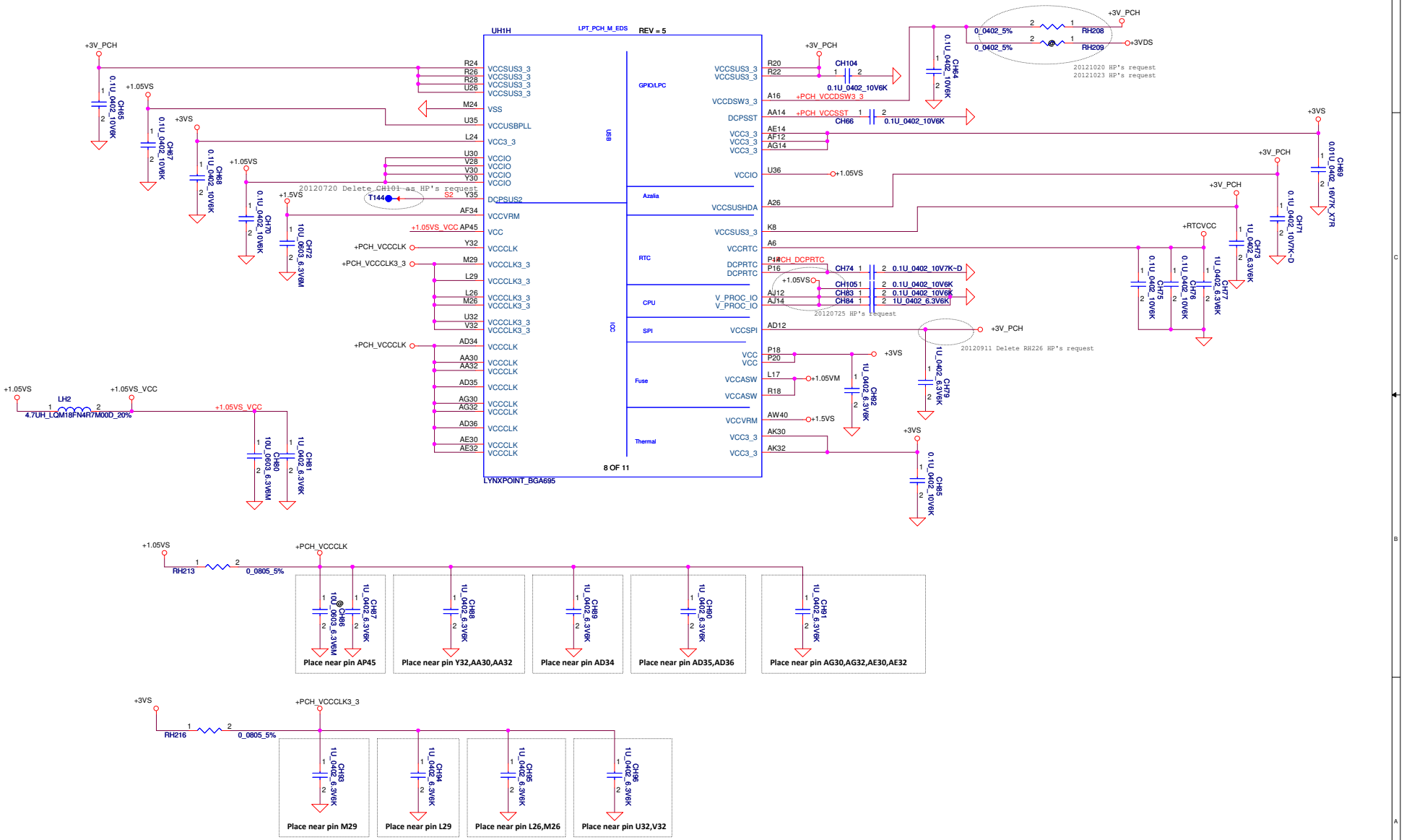
Issued Date	2012/06/11	Deciphered Date 2013/06/11	Title: PCH- Power
			Size: Custom; Document Number: LA-9371P; Rev: 0.3
			Date: Monday, November 12, 2012; Sheet 19 of 56



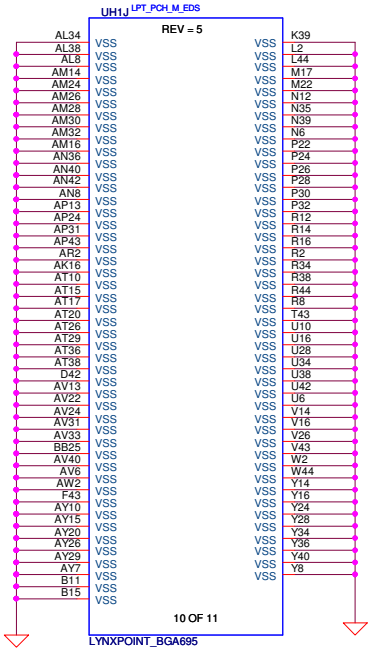
Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

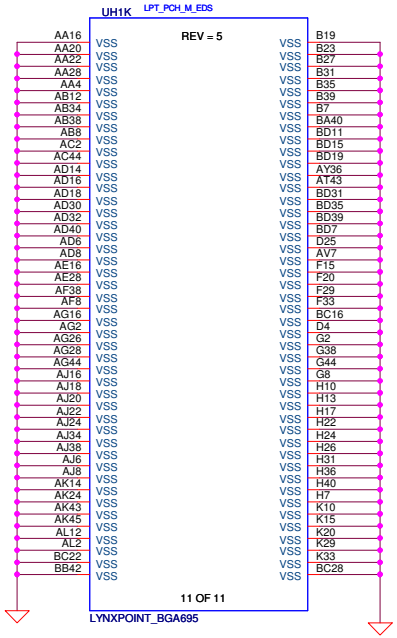
Compal Electronics, Inc.

Title: PCH - Power

Size	Document Number	Rev
Custom	LA-9371P	0.3

Date: Monday, November 12, 2012 | Sheet 20 of 56





Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

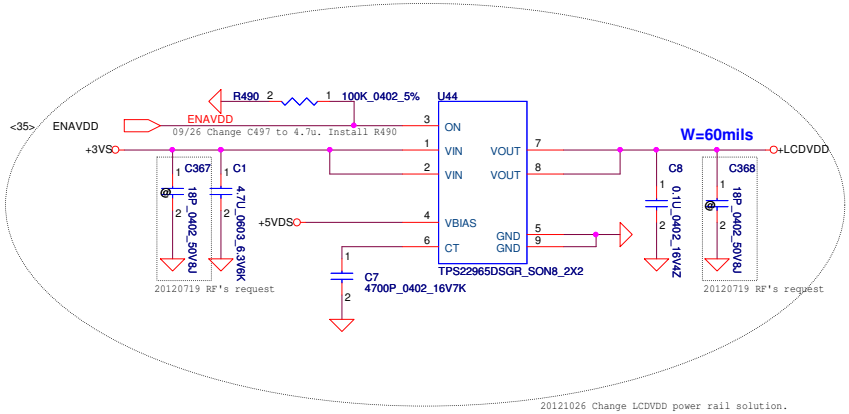
Compal Electronics, Inc.

Title: PCH - GND

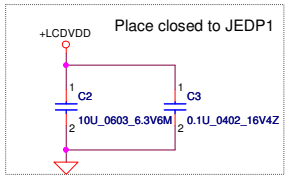
Size	Document Number	Rev
Custom	LA-9371P	0.3

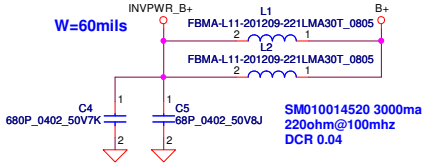
Date: Monday, November 12, 2012 Sheet 21 of 56

LCD POWER CIRCUIT



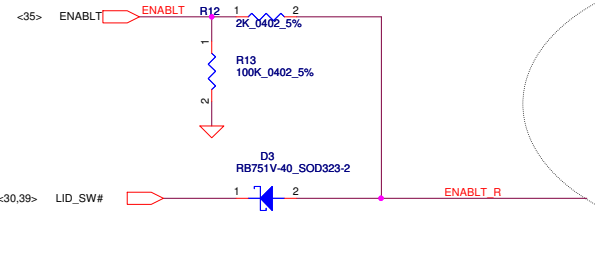
20121026 Change LCDVDD power rail solution.
Delete R9,R10,R11,C6,Q12,Q20



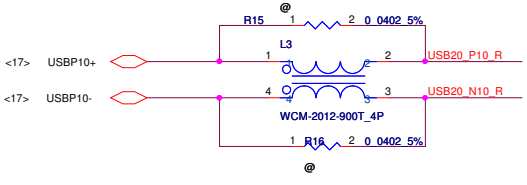


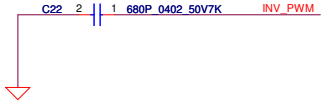
eDP PANEL Conn.

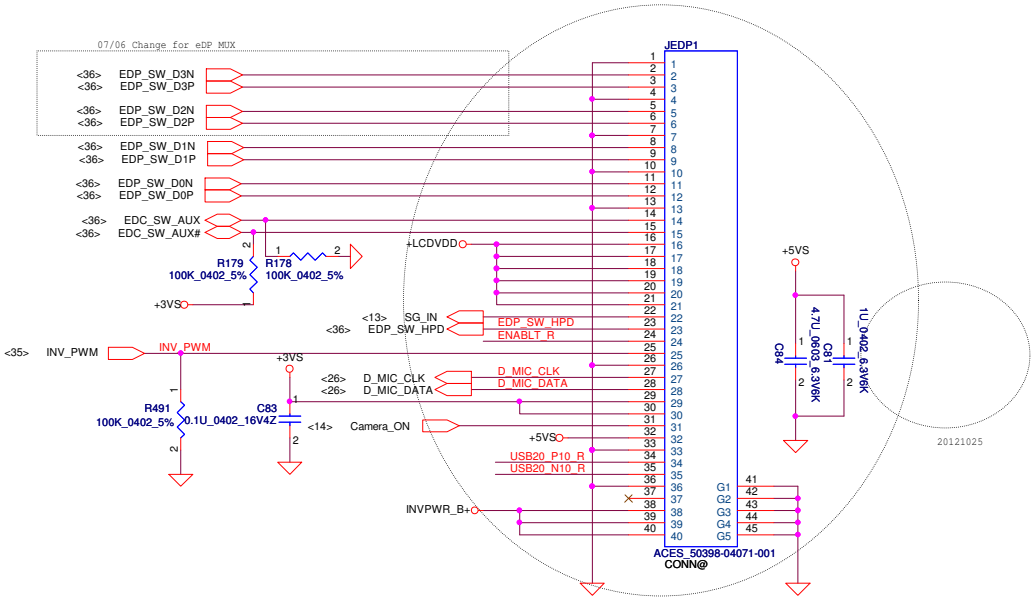
W=60mils W=60mils



20120731 Delete KB LOGO circuit



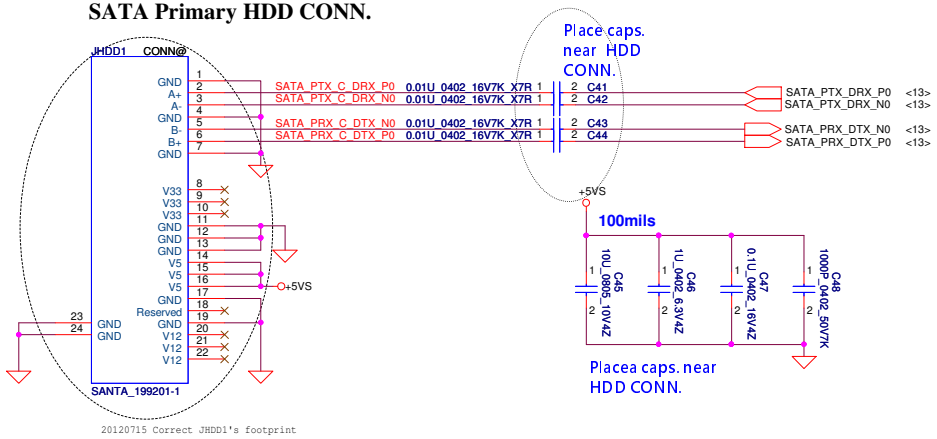




20120911 Change JEDP1's footprint
20120913 Modify pin assignment

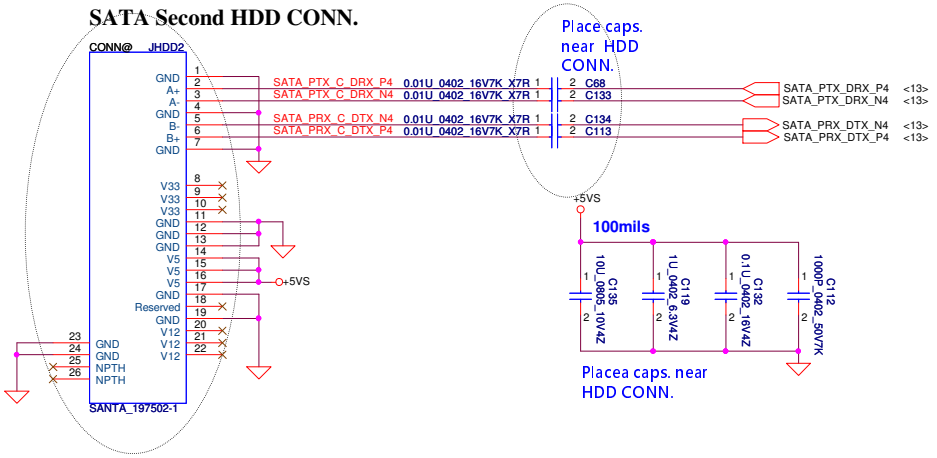
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/06/11	Deciphered Date 2013/06/11	Title: eDP/LVDS CONN & Camera
			Size: Document Number: LA-9371P Rev: 0.3
			Date: Monday, November 12, 2012 Sheet 22 of 56

SATA Primary HDD CONN.



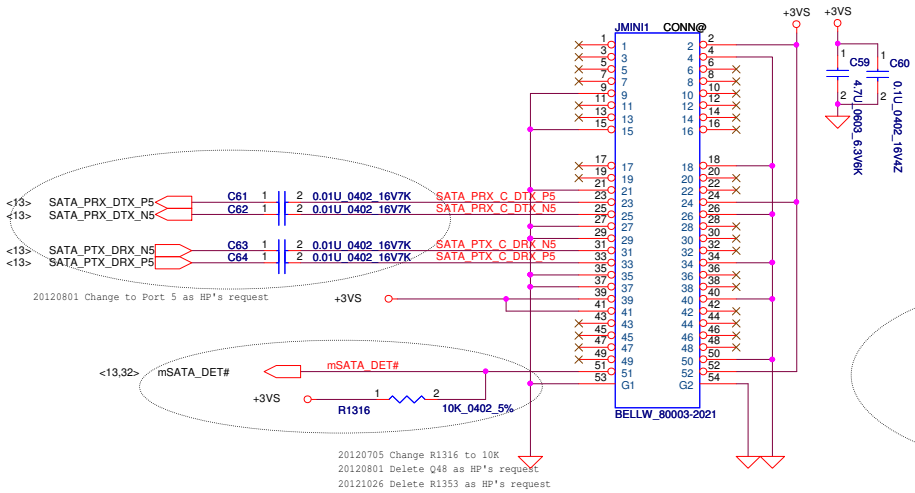
20120715 Correct JHDD1's footprint

SATA Second HDD CONN.



20121024 Update JHDD2's footprint

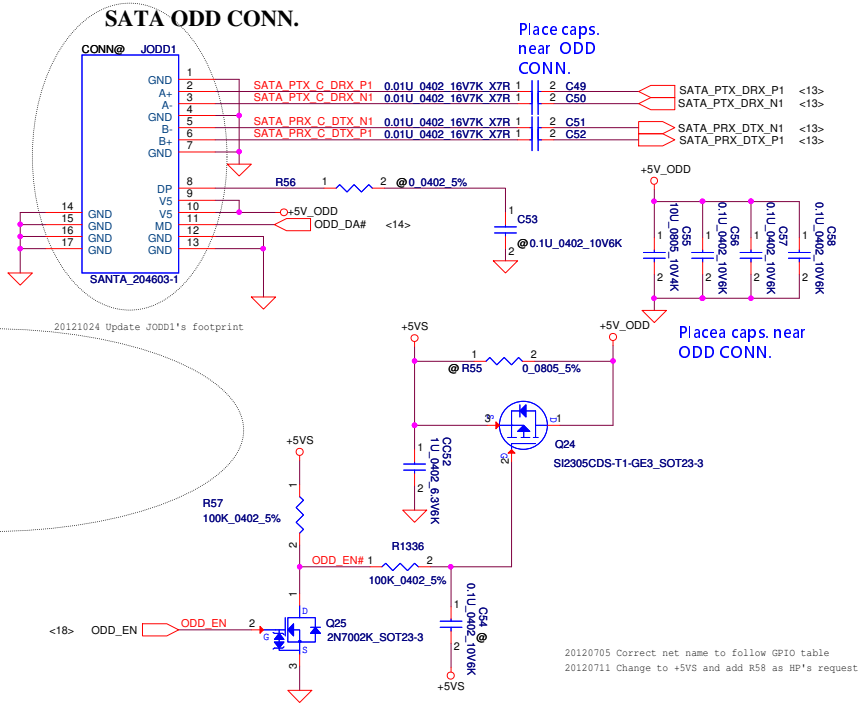
mSATA Conn.



20120801 Change to Port 5 as HP's request

20120705 Change R1316 to 10K
20120801 Delete Q48 as HP's request
20121026 Delete R1353 as HP's request

SATA ODD CONN.



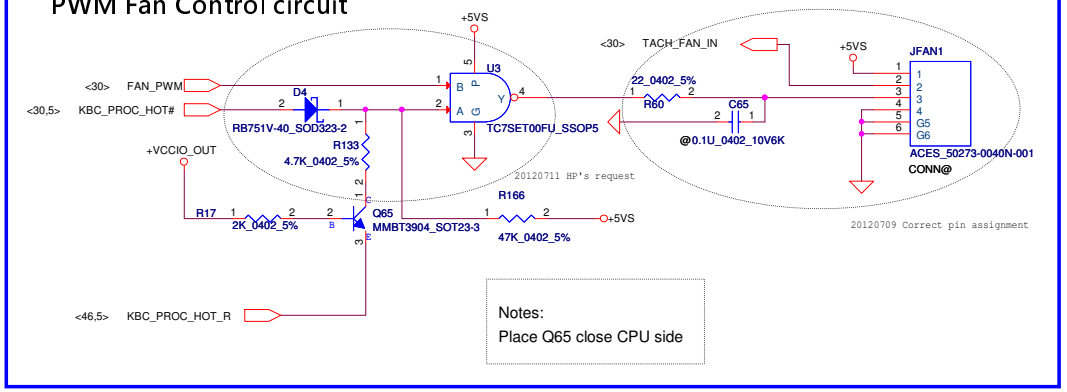
20121024 Update JODD1's footprint

20120705 Correct net name to follow GPIO table
20120711 Change to +5VS and add R58 as HP's request

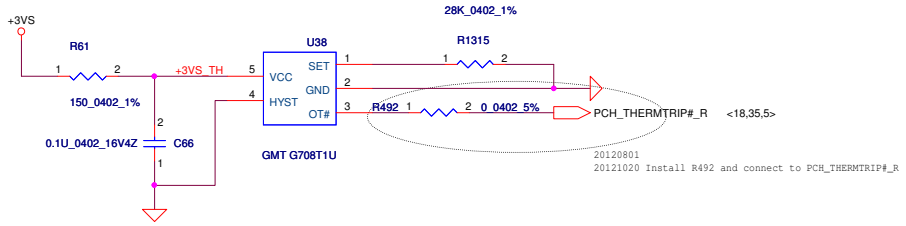
Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.		
Title: IBEX-M(1/6)-HDA/JTAG/SATA		
Size: Custom	Document Number: LA-9371P	Rev: 0.3
Date: Monday, November 12, 2012	Sheet 23 of 56	

PWM Fan Control circuit



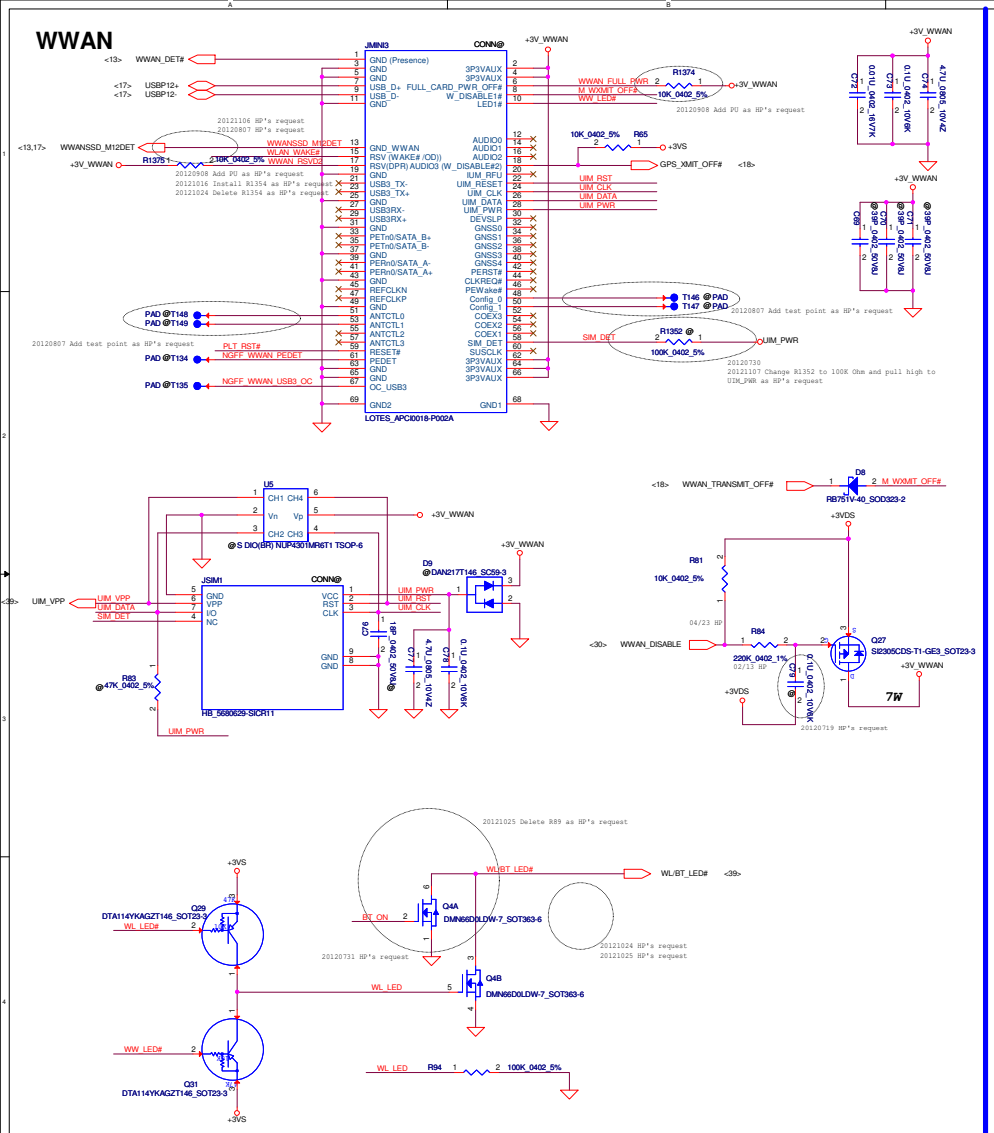
Notes:
Place Q65 close CPU side



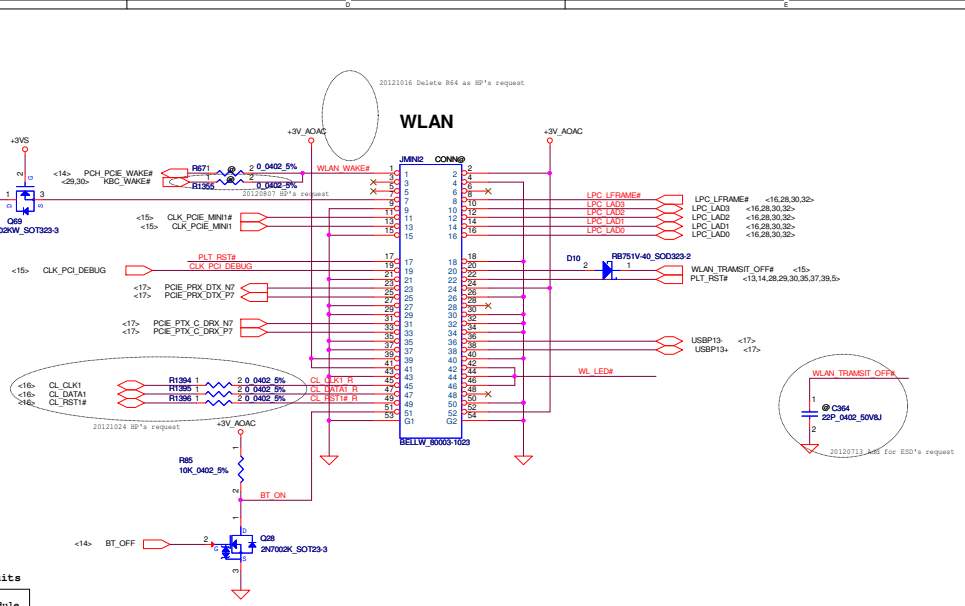
Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.			
Title: Sandy(2/7) PM,XDP,Thermal			
Size: Custom	Document Number: LA-9371P		Rev: 0.3
Date: Monday, November 12, 2012	Sheet 24 of 56		

WWAN



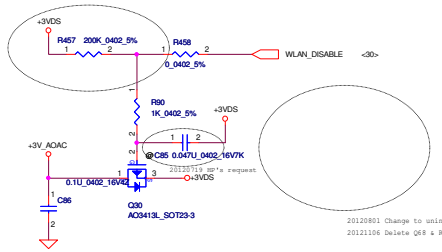
WLAN



WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	HI	LO
BT_ON#	LO	HI

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.			
Title: WWAN/NAND mini			
Size: C	Document Number: LA-9371P		Rev: 0.3
Date: Monday, November 12, 2012	Sheet 25 of 56		

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

Place AVDD ,PVDD,and DVDD capacitor close to Codec

CA8,CA10 near UA5 PIN45
CA9,CA21 near UA5 PIN39

PLACE CLOSE TO U1 PIN 13

If Sense_A total length is greater than 6 inches, chagne C12 to 0.1uF

RA3 2.49K_0402_1%
CA1 1000P_0402_50V7K

PLACE CLOSE TO U1 PIN 14

If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

RA4 2.49K_0402_1%
CA13 1000P_0402_50V7K

External MIC
Combo Jack
Headphone

Internal SPKR(front stereo speaker)

20120702 Delete MIC_SENSE# circuit

20120702 Delete MUTE circuit

Place C209,C210,CA87,CA89 close to Codec

20120920 HP's request

20120719 HP's request

RA53 need under or near UA1

SB Beep

GND GNDA

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

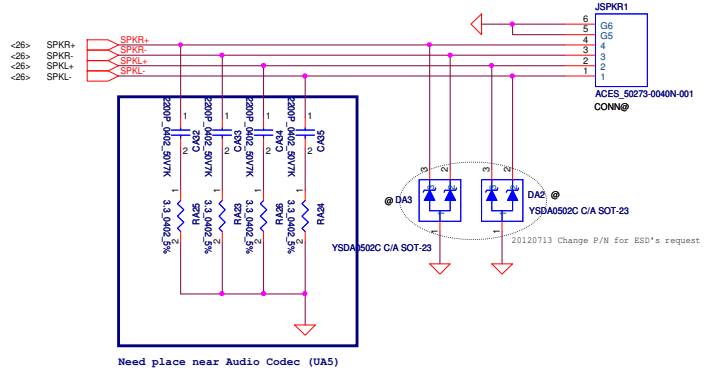
Compal Electronics, Inc.

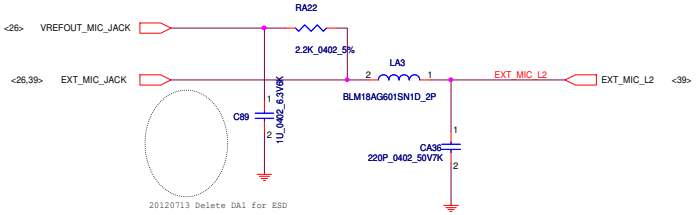
Title: Audio IDT 92HD91

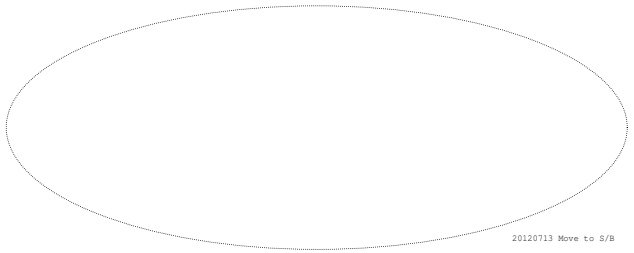
Size: Custom | Document Number: LA-XXXXP | Rev: 0.3

Date: Monday, November 12, 2012 | Sheet 26 of 56

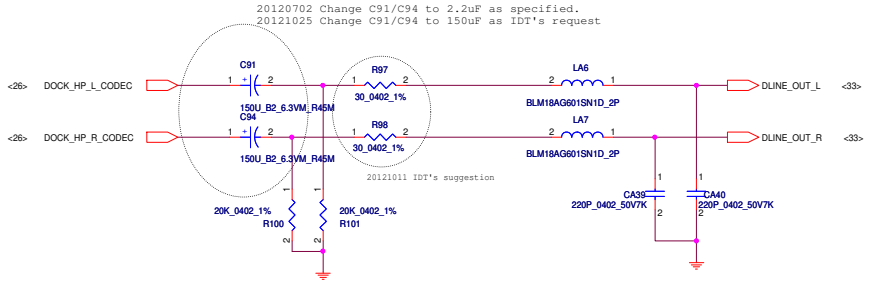
Speaker Connector

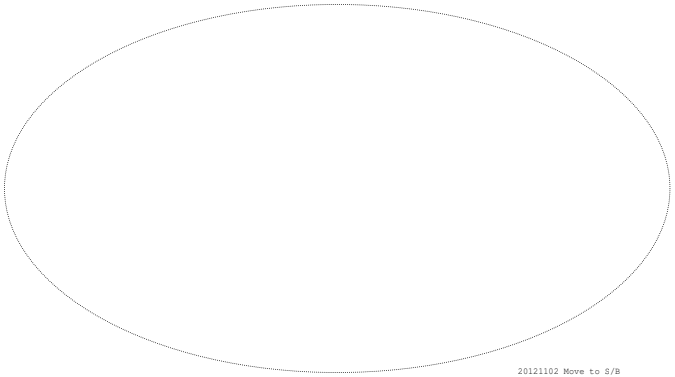






DOCK Audio

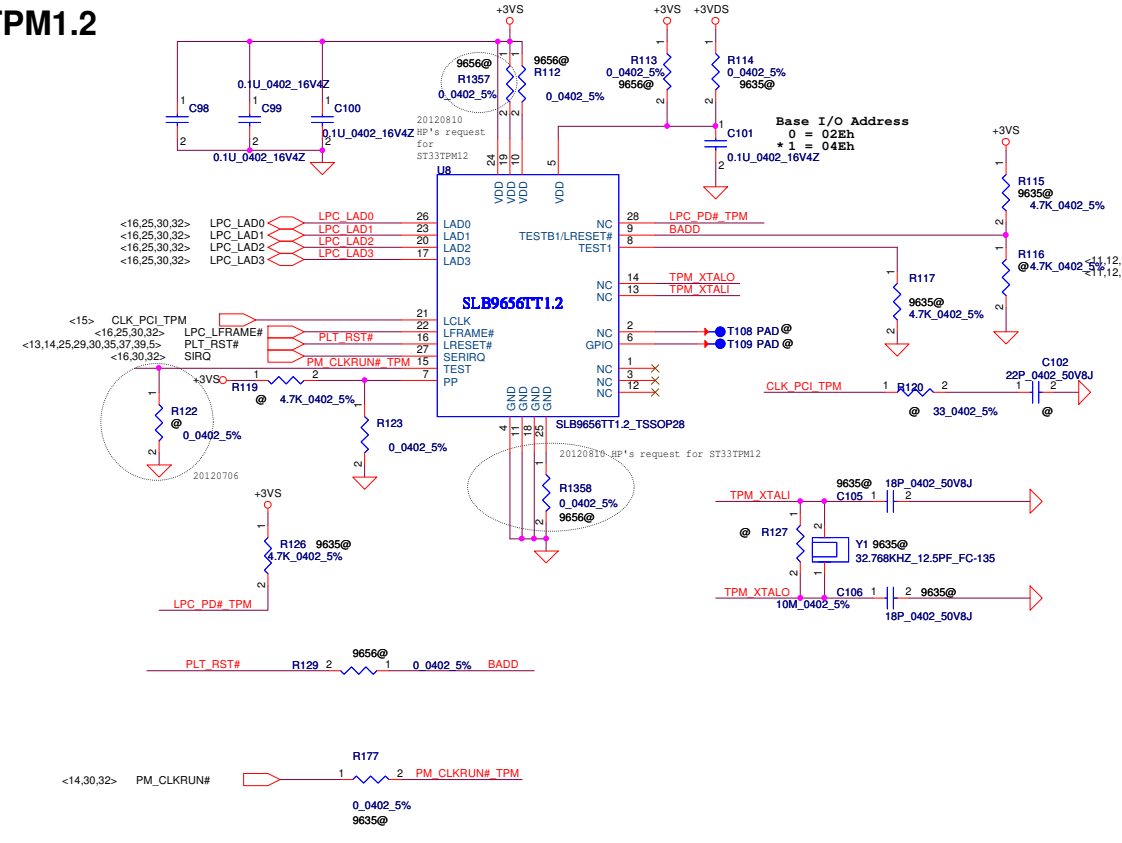




Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

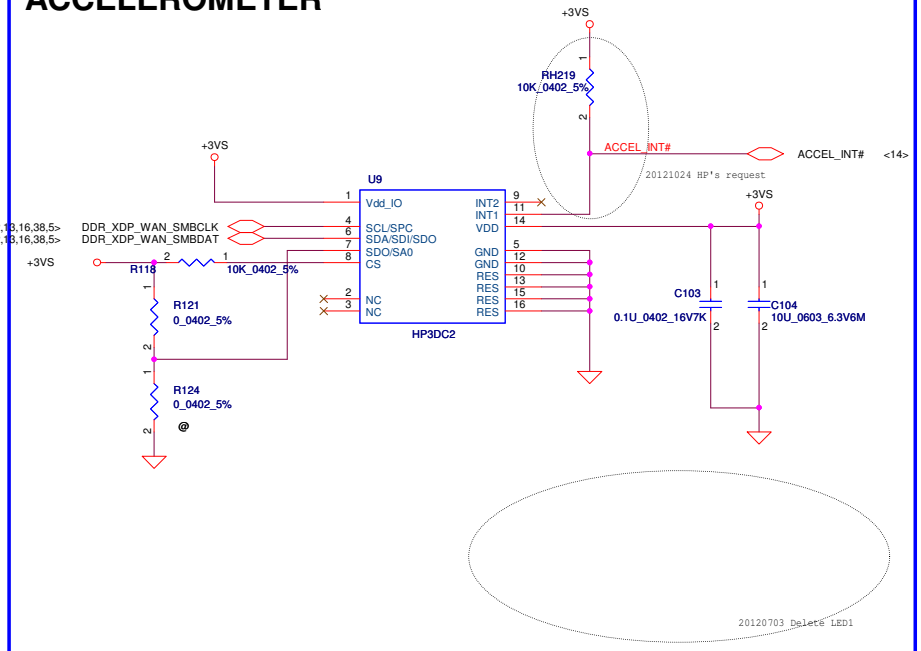
Compal Electronics, Inc.			
Title	Audio SPK Conn/Jack/MIC		
Size C	Document Number LA-9371P		Rev 0.3
Date: Monday, November 12, 2012	Sheet 27 of 56		

TPM1.2

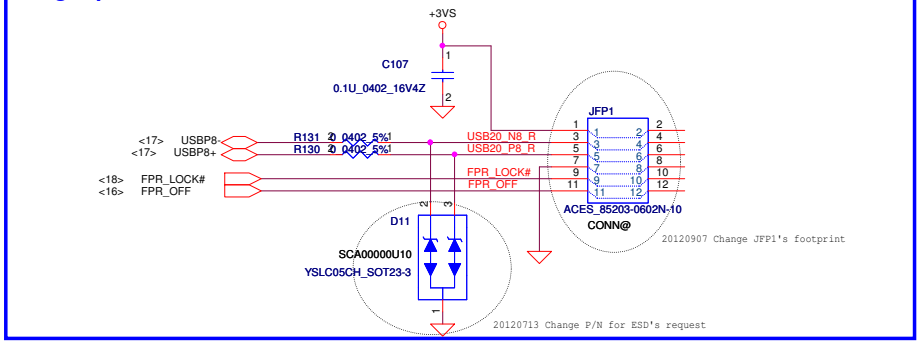


TPM	BOM Option (Not Install)
SLB9635	R112, R113, R129
SLB9656	R114, R115, R117, R126, R177, C105, C106, Y1
ST33TPM12	R113, R129,R114, R115, R117, R126, R177, R1357, R1358,R127,R122,R116,R120, C102, C101, C105, C106, Y1

ACCELEROMETER



Finger printer



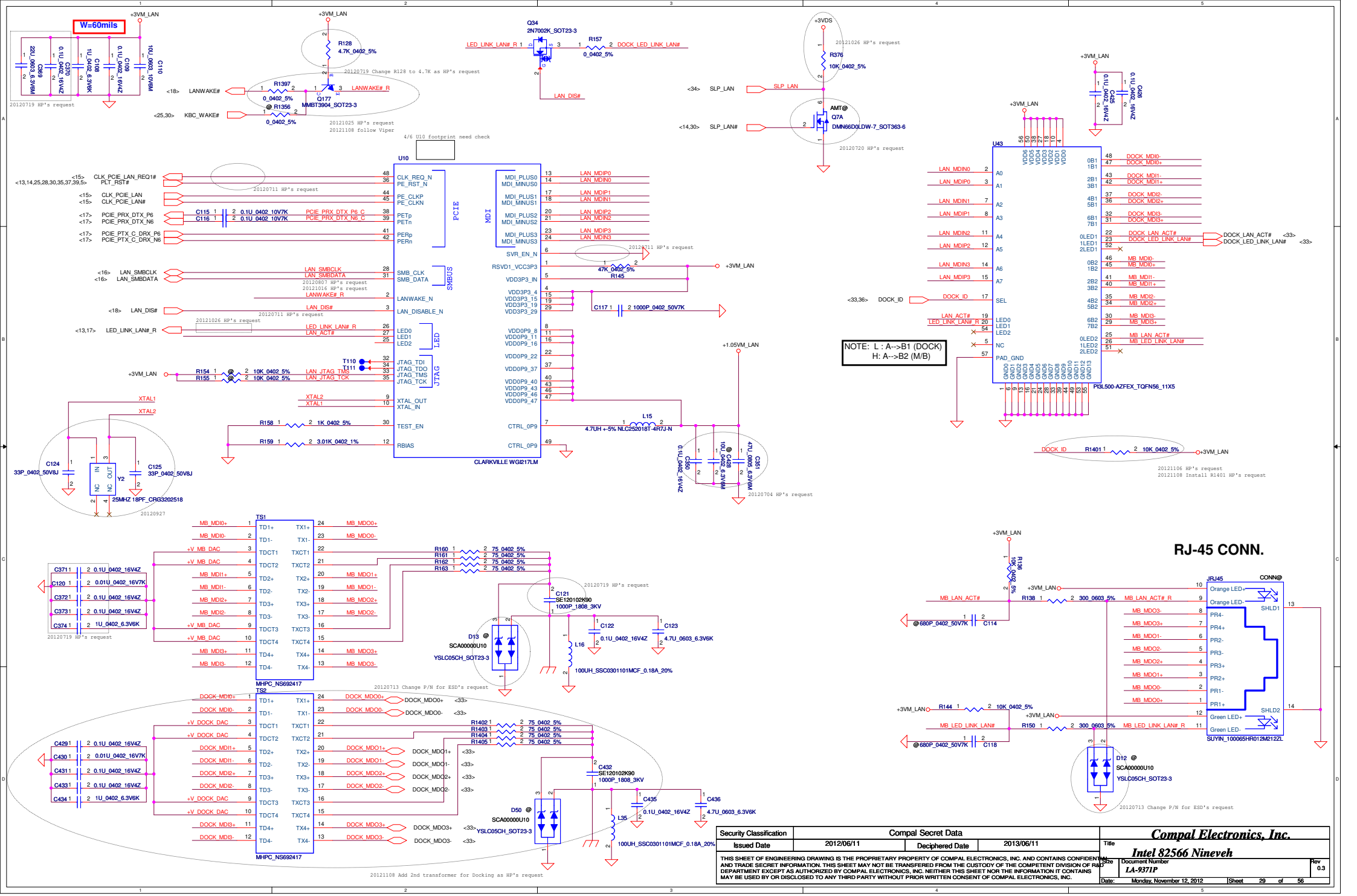
Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: TPM/Gsensor

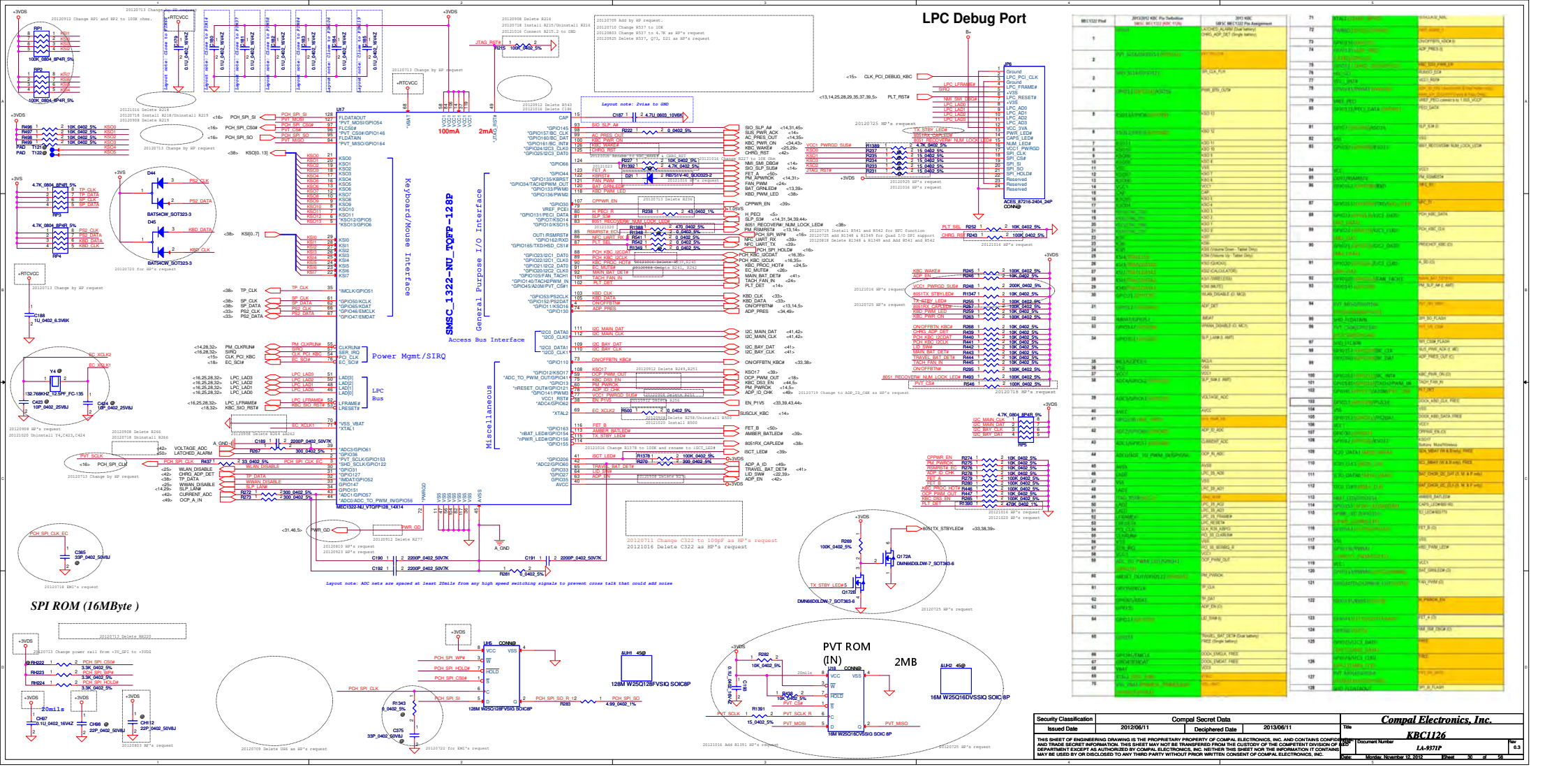
Size | Document Number: LA-9371P | Rev: 0.3

Date: Monday, November 12, 2012 | Sheet 28 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.			
Title: Intel 82566 Nineveh			
Size	Document Number: LA-9371P		Rev: 0.3
Date: Monday, November 12, 2012	Sheet 29 of 56		



Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

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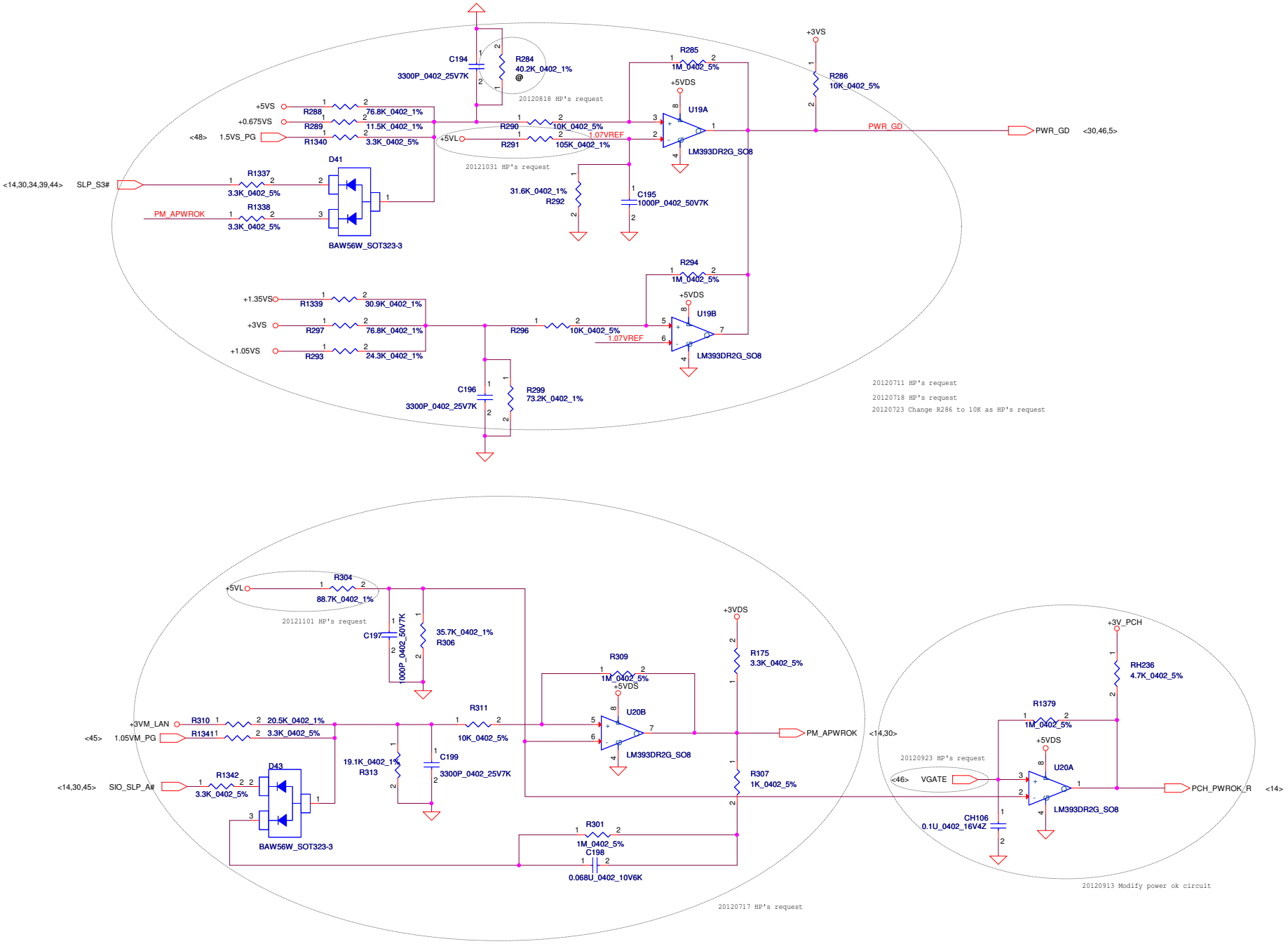
Compal Electronics, Inc.

Title: **KBC1126**

Size: C | Document Number: LA-9371P | Rev: 0.3

Date: Monday, November 12, 2012 | Sheet 30 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

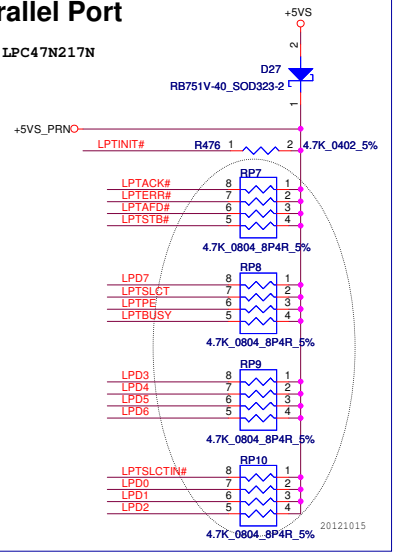
Compal Electronics, Inc.

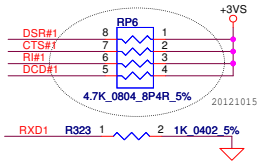
Title: **POK CKT**

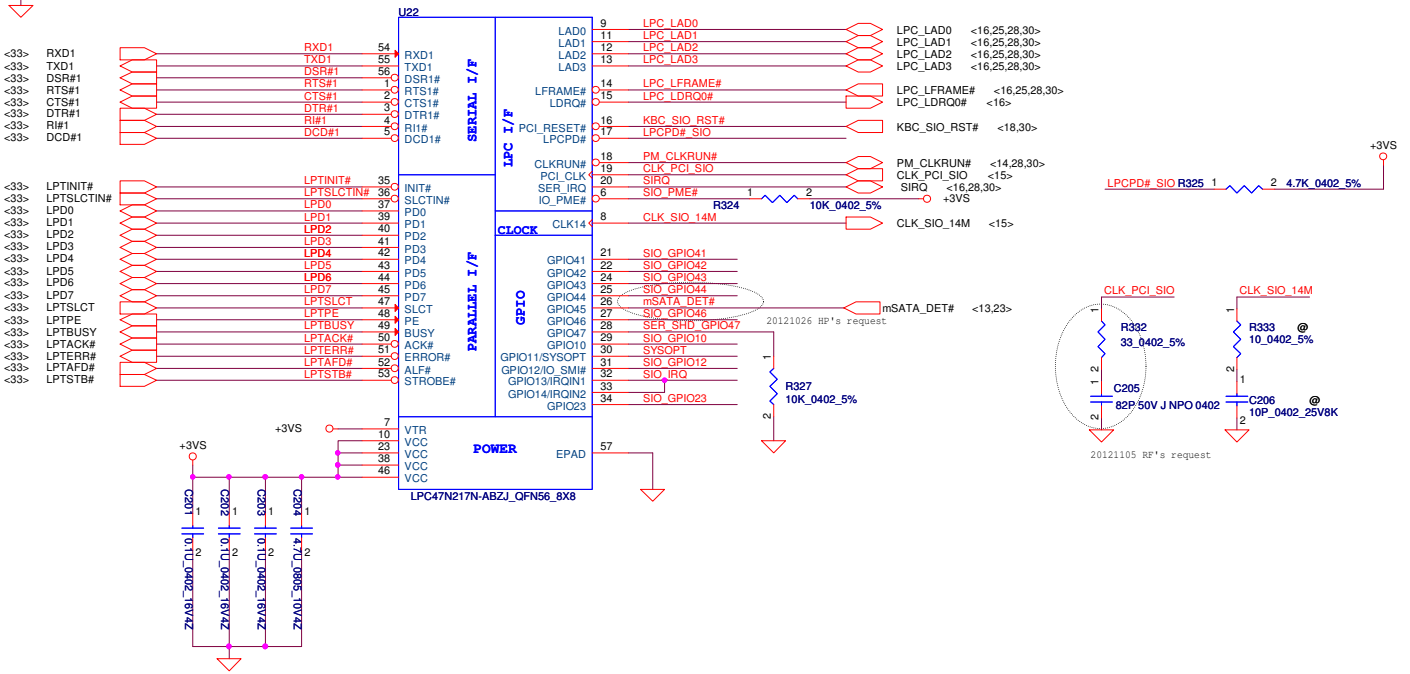
Size: B	Document Number: LA-9371P	Rev: 0.3
Date: Monday, November 12, 2012	Sheet 31 of 56	

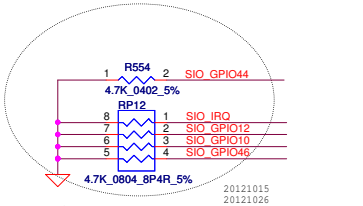
Parallel Port

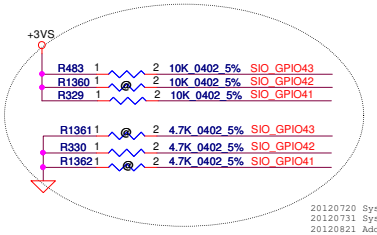
TO LPC47N217N











20120720 System ID for HP's request
20120731 System ID for HP's request
20120821 Add R for 2DIMM & 4DIMM option

Platform IDs (Super I/O GPIOs)

PLT_ID1	PLT_ID2	PLT_ID3					
GPIO43	GPIO42	GPIO41	SYSTEM ID	Series	CPU	Dock	COMMON BIOS
1	0	1	Afterburner 17" 4 DIMM	W	Haswell	Common	8
1	1	1	Afterburner 17" 2 DIMM	W	Haswell	Common	8

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: SUPER I/O LPC47N217N-ABZJ

Document Number: LA-9371P

Rev: 0.3

Date: Monday, November 12, 2012 | Sheet 32 of 56

DOCK CONN. 184PIN

DOCKING CONNECT

(1) PCI Express x1 channels
(2) PS/2 Interfaces
(2) USB 2.channels
(2) SATA Channels
(2) Display Port Channels
(1) Serial Port
(1) Parallel Port
(1) Line In
(1) Line Out
(1) RJ45 (10/100/1000)
(1) VGA
(1) 2 LAN indicator LED's
(1) Power Button
(1) I2C interface

VA
C207 2 0.1U_0603_50V4Z
C209 2 0.1U_0603_50V4Z

VIN
L27 HCB2012KF-121T50_0805
5A
L28 HCB2012KF-121T50_0805
VA

+5VS
C210 2 10U_0805_10V4Z
C211 2 0.1U_0402_16V4Z
C212 2 0.1U_0402_16V4Z
C213 2 0.1U_0402_16V4Z

D42 @ L30ESD24VC3-2_SOT23-3
20120713 ESD's request

VA 12A

JDOCK1A

	P1	190	G1	189	
		188	188	1	1
<29> DOCK_MDO3+		187	187	2	2
<29> DOCK_MDO3-		186	186	3	3
		185	185	4	4
<29> DOCK_MDO2+		184	184	5	5
<29> DOCK_MDO2-		183	183	6	6
		182	182	7	7
		181	181	8	8
DETECT		180	180	9	9
		179	179	10	10
+5VS		178	178	11	11
		177	177	12	12
		176	176	13	13
		175	175	14	14
		174	174	15	15
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<36> DPB_TXP2		152	153	36	37
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		150	151	38	39
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<36> DPB_TXN3		148	149	40	41
		147	148	41	42
<36> DPB_AUX	DPB_AUX	146	147	42	43
<36> DPB_AUX#	DPB_AUX#	145	146	43	44
		144	145	44	45
			144	45	

FOX_QL0094L-D26601-8H

20120912

DOCK_MDO1+ <29>
DOCK_MDO1- <29>
DOCK_MDO0+ <29>
DOCK_MDO0- <29>
DOCK_LED_LINK_LAN# <29>
DOCK_LAN_ACT# <29>
20120912

USB3TN1 <17>
USB3TP1 <17>
USB3RN1 <17>
USB3RP1 <17>
USBP0- <17>
USBP0+ <17>

MXM_DCK_LANE_P0 <35>
MXM_DCK_LANE_N0 <35>
MXM_DCK_LANE_P1 <35>
MXM_DCK_LANE_N1 <35>
MXM_DCK_LANE_P2 <35>
MXM_DCK_LANE_N2 <35>
MXM_DCK_LANE_P3 <35>
MXM_DCK_LANE_N3 <35>
MXM_DCK_AUX <35>
MXM_DCK_AUX# <35>

Quick SW

GPU

+5VS +3V_PCH

DOCK_ID R334 1 @ 2 10K_0402_5%
ISO_PREP# R337 1 2 10K_0402_5%
20121108 Uninstall R334 as HP's request

ON/OFFBTN_KBC#
C299 0.01U_0402_16V7K
20120911 Delete R336 as HP's request

VA_ON#
R335 1K_0402_5%
C208 0.1U_0402_16V4Z

R188 100K_0402_5%
DPB_HPD
ADP_SIGNAL
DPB_AUX R339 2 0_0402_5% DPB_AUX_R
DPB_AUX# R341 2 0_0402_5% DPB_AUX#_R

JDOCK1B

		143	142	46	47
		142	141	47	48
<36> DPB_HPD	DPB_HPD	141	140	48	49
<30,39,43,44> EN_P1V5		140	139	49	50
ADP_SIGNAL	ADP_SIGNAL	139	138	50	51
DPB_AUX	DPB_AUX_R	138	137	51	52
DPB_AUX#	DPB_AUX#_R	137	136	52	53
		136	135	53	54
		135	134	54	55
		134	133	55	56
		133	132	56	57
		132	131	57	58
<32> LPTSTB#	LPTSTB#	131	130	58	59
<32> LPTAFD#	LPTAFD#	130	129	59	60
<32> LPTERR#	LPTERR#	129	128	60	61
<32> LPTACK#	LPTACK#	128	127	61	62
<32> LPTBUSY	LPTBUSY	127	126	62	63
<32> LPTPE	LPTPE	126	125	63	64
<32> LPTSLCT	LPTSLCT	125	124	64	65
<32> LPD7	LPD7	124	123	65	66
<32> LPD6	LPD6	123	122	66	67
<32> LPD5	LPD5	122	121	67	68
<32> LPD4	LPD4	121	120	68	69
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<32> LPD2	LPD2	119	118	70	71
<32> LPD1	LPD1	118	117	71	72
<32> LPD0	LPD0	117	116	72	73
<32> LPTSLCTIN#	LPTSLCTIN#	116	115	73	74
<32> LPTINIT#	LPTINIT#	115	114	74	75
	STB_LED# R	114	113	75	76
<13,39> SATA_ACT#	SATA_ACT#	113	112	76	77
<29,36> DOCK_ID	DOCK_ID	112	111	77	78
<13,36> ISO_PREP#	ISO_PREP#	111	110	78	79
		110	109	79	80
<13> SATA_PTX_DRX_P3		109	108	80	81
<13> SATA_PTX_DRX_N3		108	107	81	82
<13> SATA_PRX_DTX_P3		107	106	82	83
<13> SATA_PRX_DTX_N3		106	105	83	84
		105	104	84	85
<17> USBP11-	USBP11-	104	103	85	86
<17> USBP11+	USBP11+	103	102	86	87
		102	101	87	88
<13> SATA_PTX_DRX_P2		101	100	88	89
<13> SATA_PTX_DRX_N2		100	99	89	90
		99	98	90	91
<13> SATA_PRX_DTX_P2		98	97	91	92
<13> SATA_PRX_DTX_N2		97	96	92	93
		96	95	93	94
		95		94	
		192	191		
	G2	194	193	G1	
	G4	196	195	G3	
	G6	198	197	G5	
	G8	200	199	G7	
	G10			G9	

FOX_QL0094L-D26601-8H

<32> D_DDCDATA
<32> D_DDCCLK
<32> D_VSYNC
<32> D_HSYNC
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R_DOCK_GRN
R_DOCK_BLU
<32> DCD#1
<32> RI#1
<32> DTR#1
<32> CTS#1
<32> RTS#1
<32> DSR#1
<32> TXD1
<32> RXD1

<36> D_DDCDATA
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<36> D_VSYNC
<36> D_HSYNC
R_DOCK_RED <36>
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R_DOCK_BLU <36>
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RI#1 <32>
DTR#1 <32>
CTS#1 <32>
RTS#1 <32>
DSR#1 <32>
TXD1 <32>
RXD1 <32>

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<30> KBD_CLK
<30> PS2_DATA
<30> PS2_CLK
<27> LINE_IN_SENSE
<27> DOCK_HPS#

<27> DOCK_LINE_IN_L
<27> DOCK_LINE_IN_R

<27> DLINE_OUT_L
<27> DLINE_OUT_R

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KBD_CLK <30>
PS2_DATA <30>
PS2_CLK <30>
LINE_IN_SENSE <27>
DOCK_HPS# <27>
DOCK_LINE_IN_L <27>
DOCK_LINE_IN_R <27>
DLINE_OUT_L <27>
DLINE_OUT_R <27>
DETECT

20120801 Change to Port 2 as HP's request

+5VDS
R346 10K_0402_5%
STB_LED# R
<30,38,39> 8051TX_STBYLED#
Q35 2N7002K_SOT23-3
20120718 HP's request

R_DOCK_RED R343 1 2 150_0402_1%
R_DOCK_GRN R344 1 2 150_0402_1%
R_DOCK_BLU R345 1 2 150_0402_1%

R_DOCK_RED C214 1 2 @0.1U_0402_16V4Z
R_DOCK_GRN C215 1 2 @0.1U_0402_16V4Z
R_DOCK_BLU C216 1 2 @0.1U_0402_16V4Z

IN	NC<-->COM	NO<-->COM
L	ON	OFF
H	OFF	ON

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

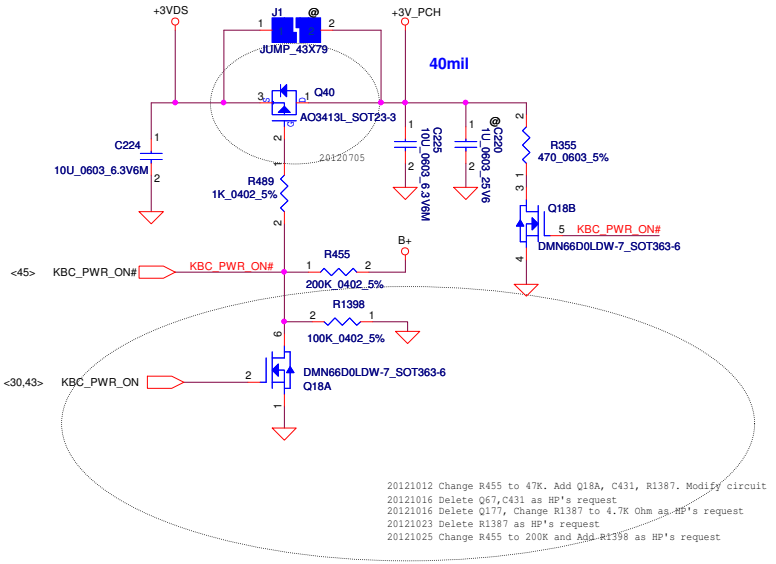
Title: DOCK CONN

Size	Document Number	Rev
Custom	LA-9371P	0.3

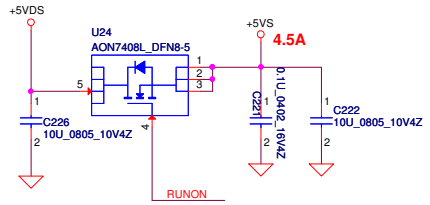
Date: Monday, November 12, 2012 Sheet 33 of 56

+3VALW TO +3VALW(PCH AUX Power)

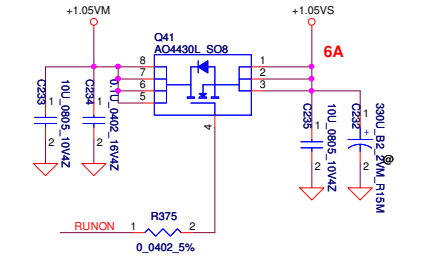
Short J1 for PCH VCCSUS3.3



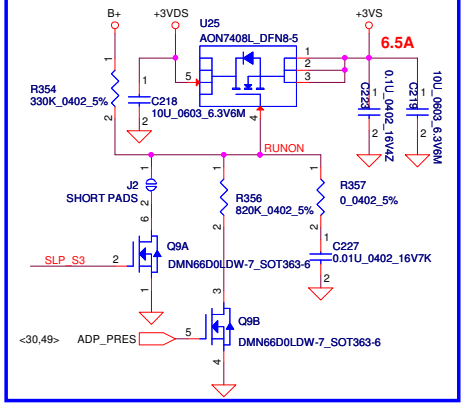
+5VALW to +5VS Transfer



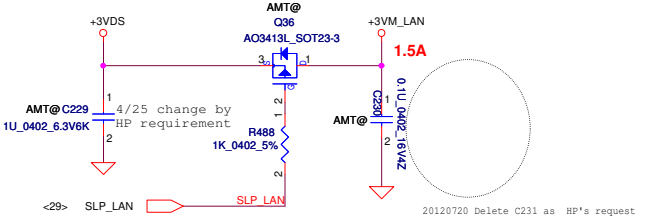
+1.05VM to +1.05VS Transfer

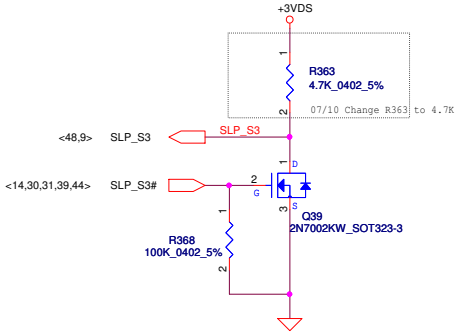


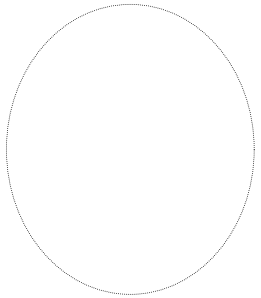
+3VALW to +3VS Transfer



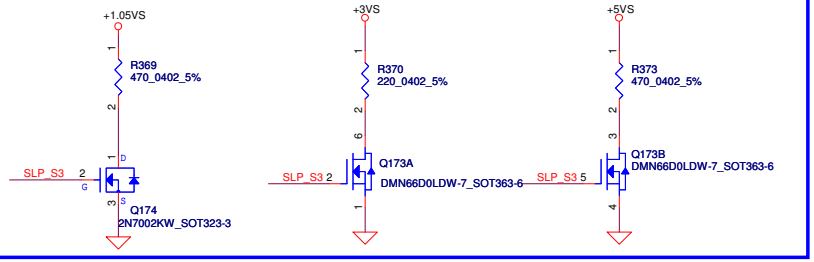
+3VALW to +3VM_LAN Transfer



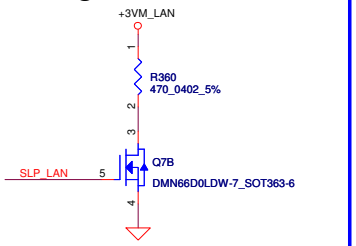


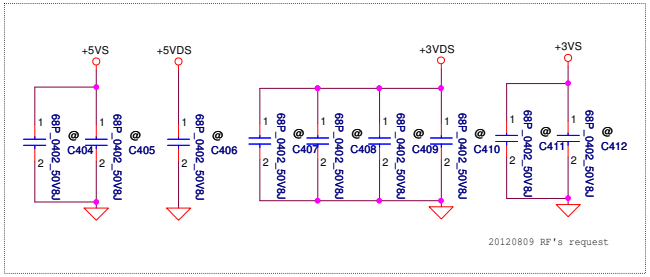


Discharge circuit-1



Discharge circuit-2 for V-M





Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.			
Title: DC/DC Circuits			
Size	Document Number: LA-9371P		Rev: 0.3
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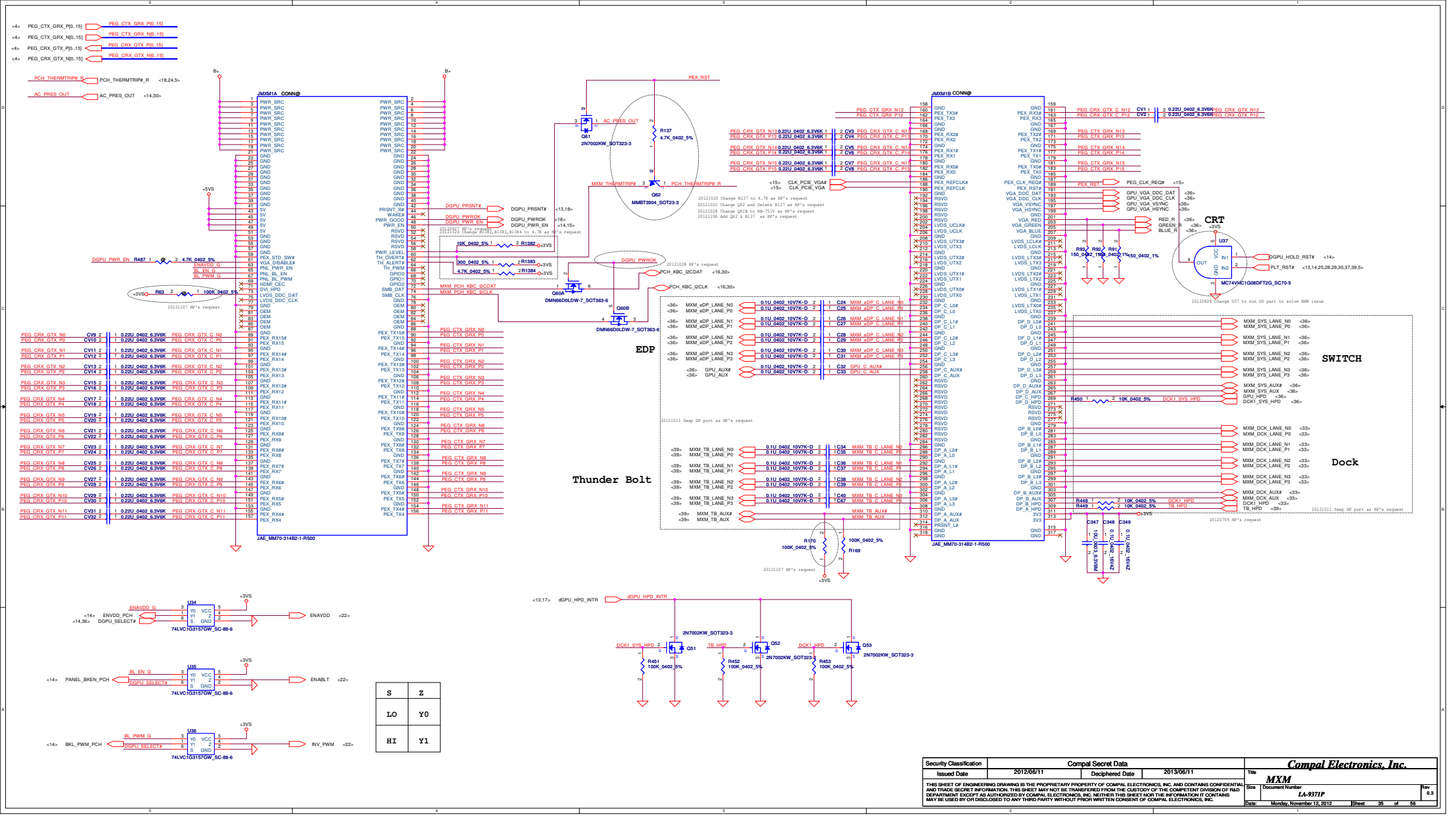

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title			
	MXM		
Size	Document Number		Rev
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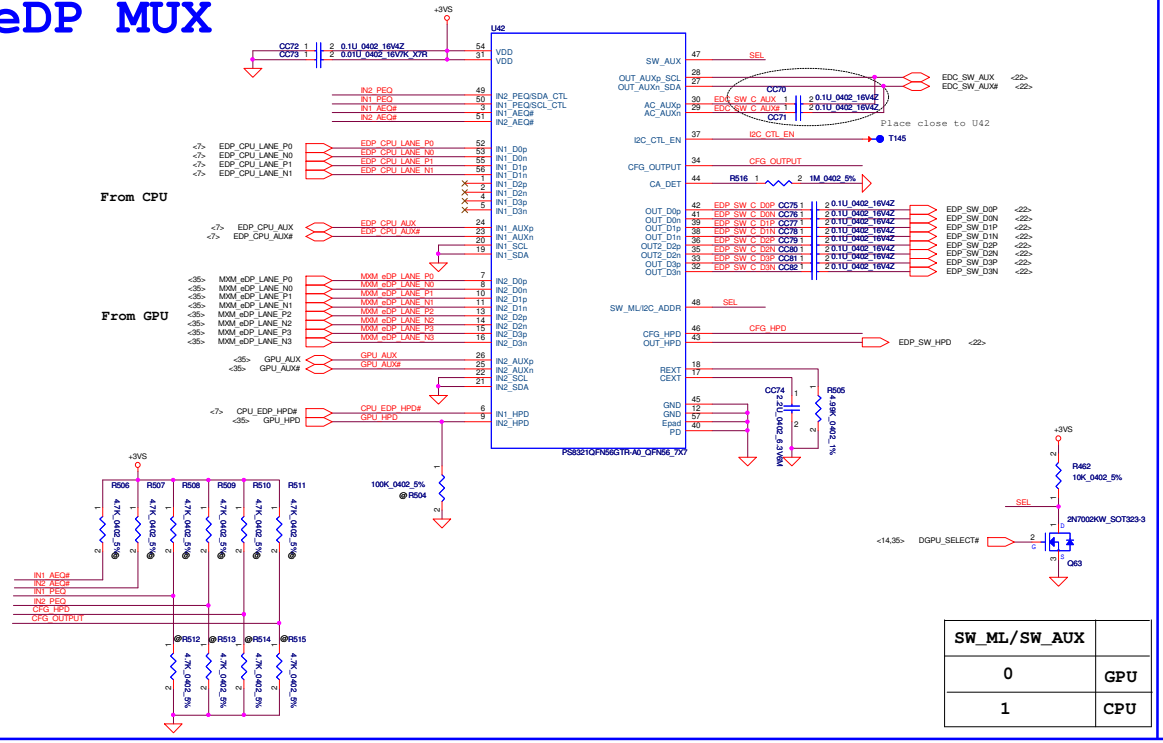
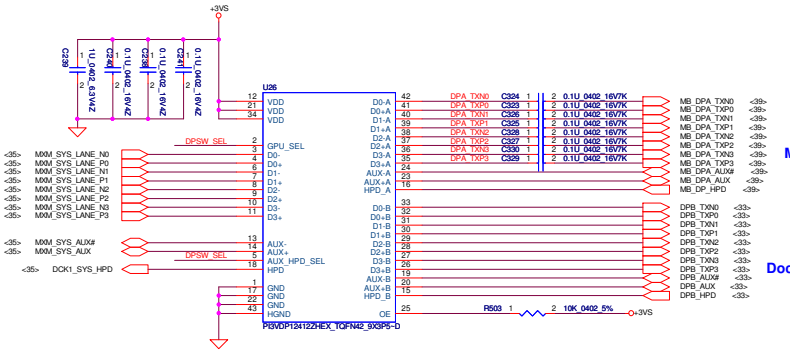
Date: Monday, November 12, 2012	Sheet 35 of 56		

eDP MUX



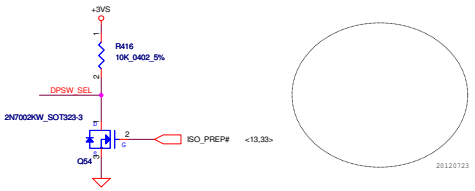
SW_ML/SW_AUX	
0	GPU
1	CPU

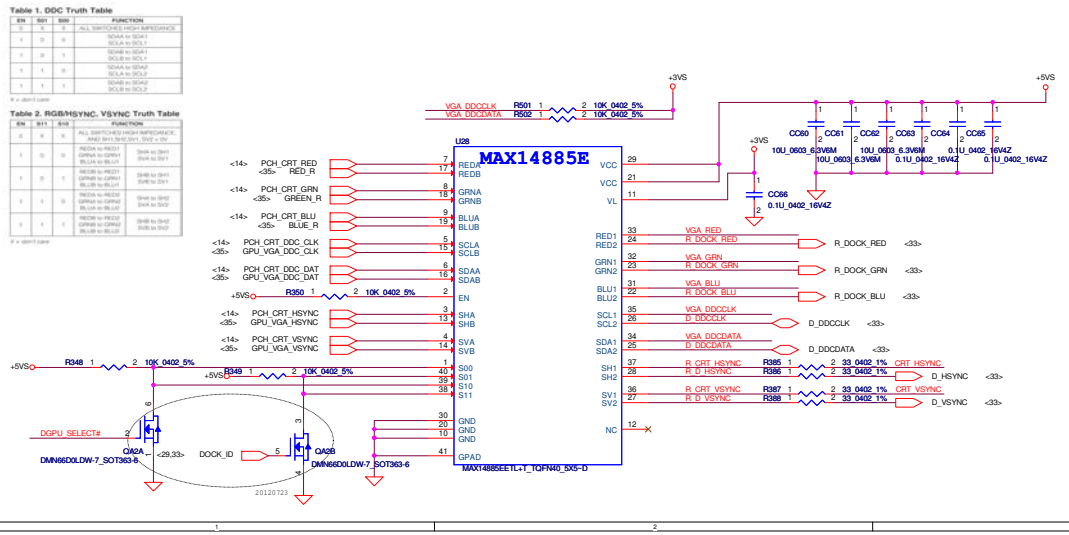
DP Switch

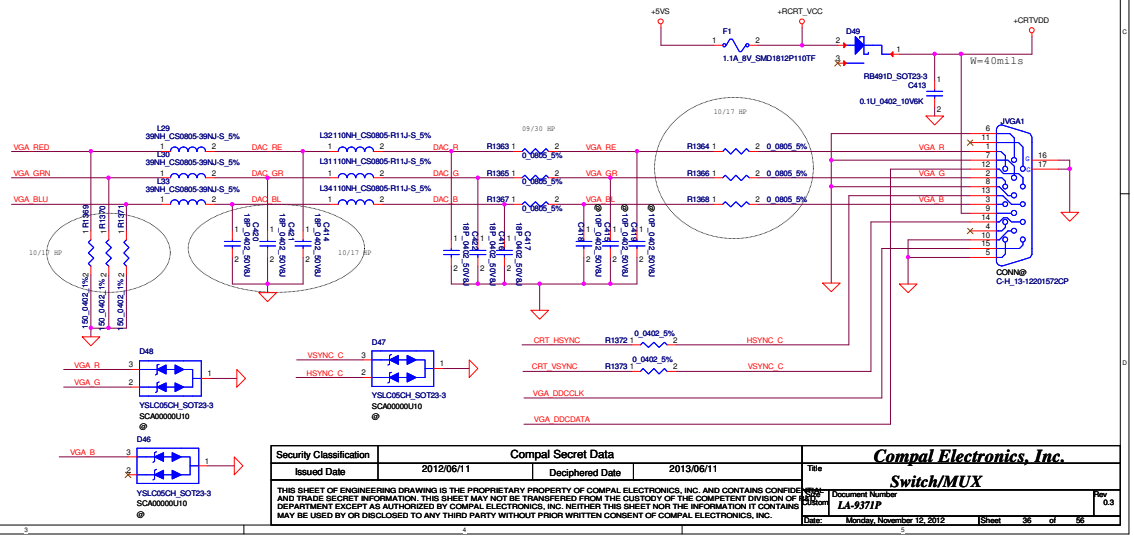


Truth Table for 42 pin package

OE	GPU_SEL	AUX_HPD_SEL	Function
High	Low	Low	Port A active for all channels
High	Low	High	Port A for HS, port B for HPD/AUX
High	High	Low	Port B for HS, port A for HPD/AUX
High	High	High	Port B active for all channels
Low	x	x	All I/O's are hi-z and IC is power down







Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: Switch/MUX

Size: C | Document Number: LA-9371P | Rev: 0.3

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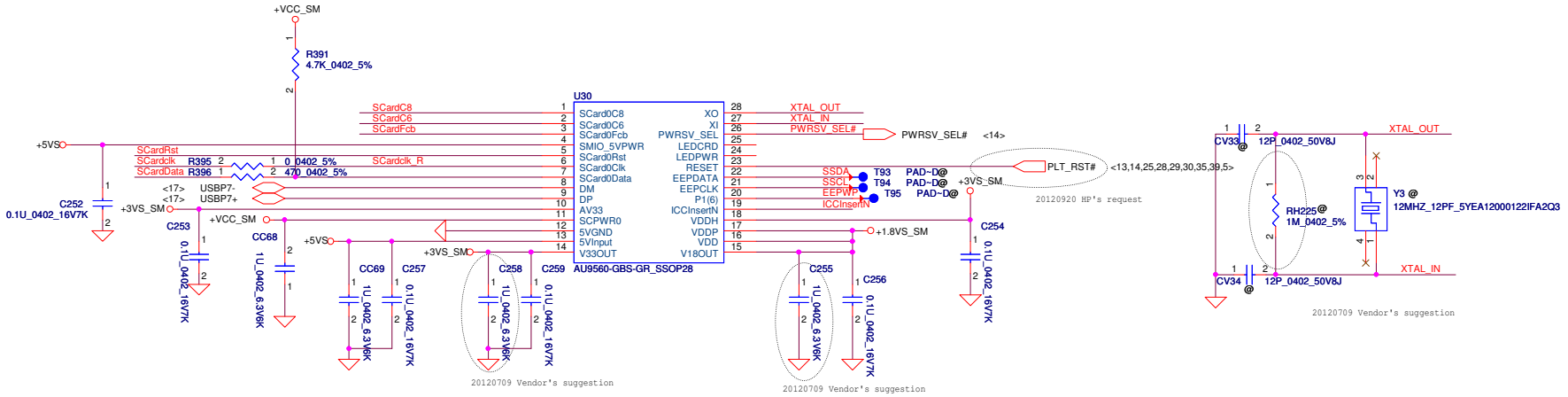

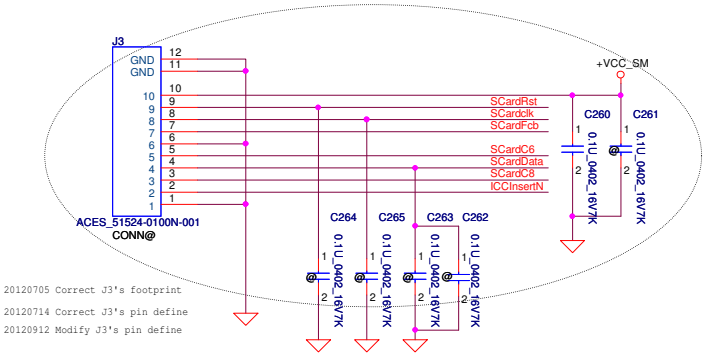

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: Smart Card

Size	Document Number	Rev
Custom		0.3

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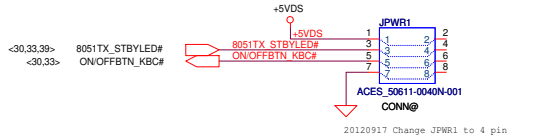
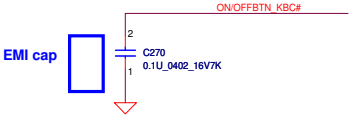
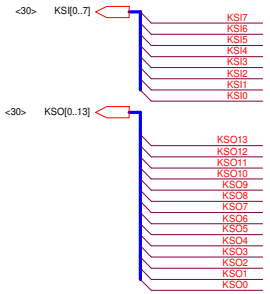
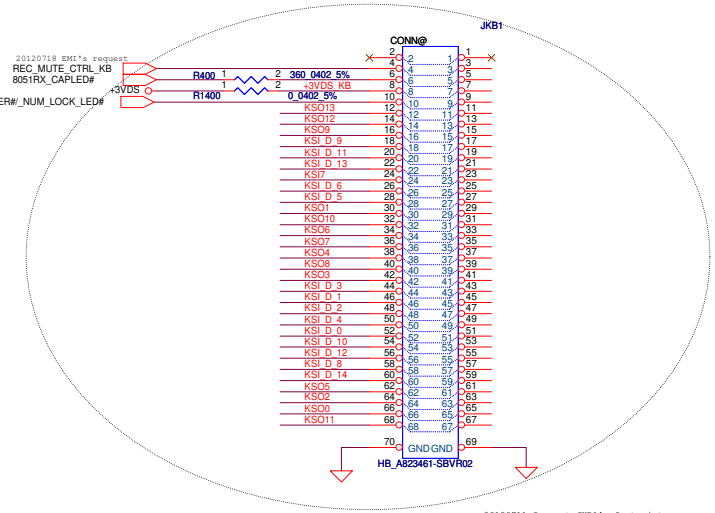


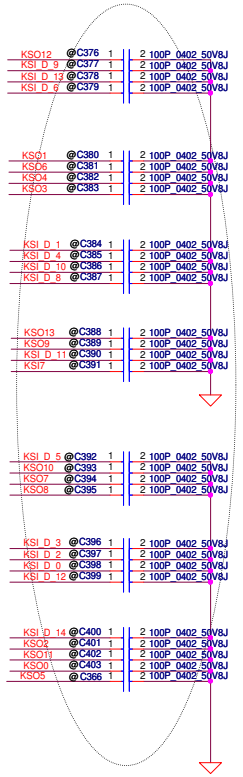
20120917 Change JPWR1 to 4 pin



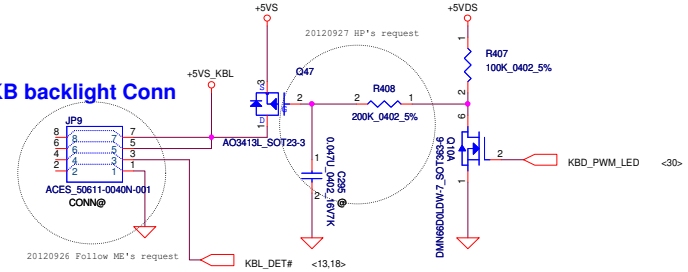


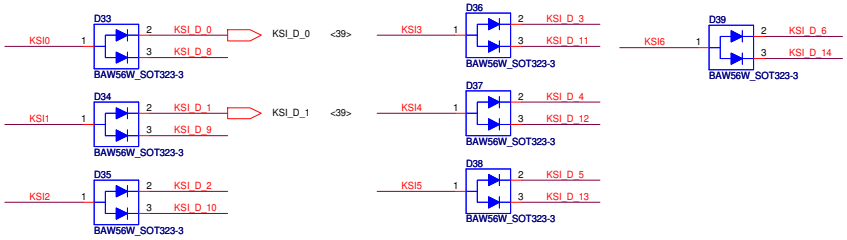


20120711 Correct JKB1's footprint
20120712 Correct connection for JKB1
20120917 Correct connection for JKB1
20121025 Correct connection for JKB1

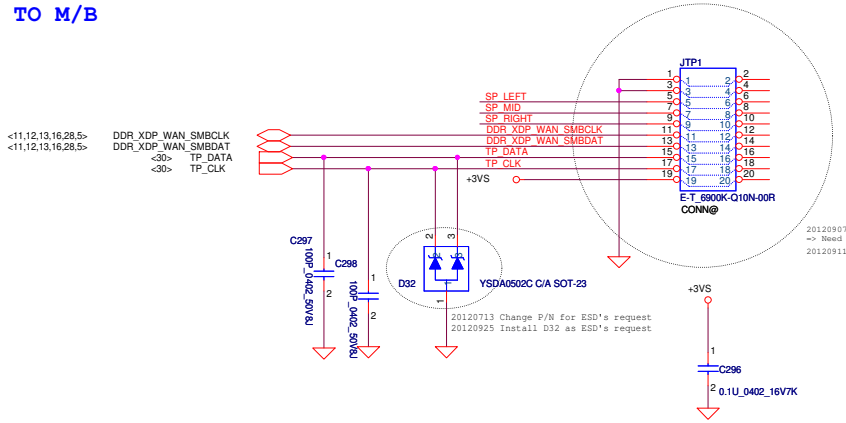


KB backlight Conn





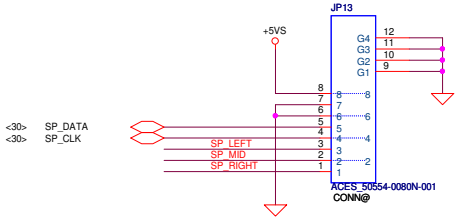
TP/B TO M/B



20120713 Change P/N for ESD's request
20120925 Install D32 as ESD's request

20120907 Change JTP1's footprint & Delete JTP2
-> Need check Pin assigment
20120911 Change JTP1's footprint

Stick Point CONN



Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: KB/TP/PWR CONN

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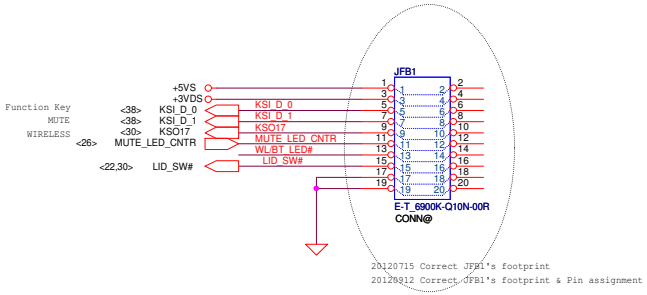
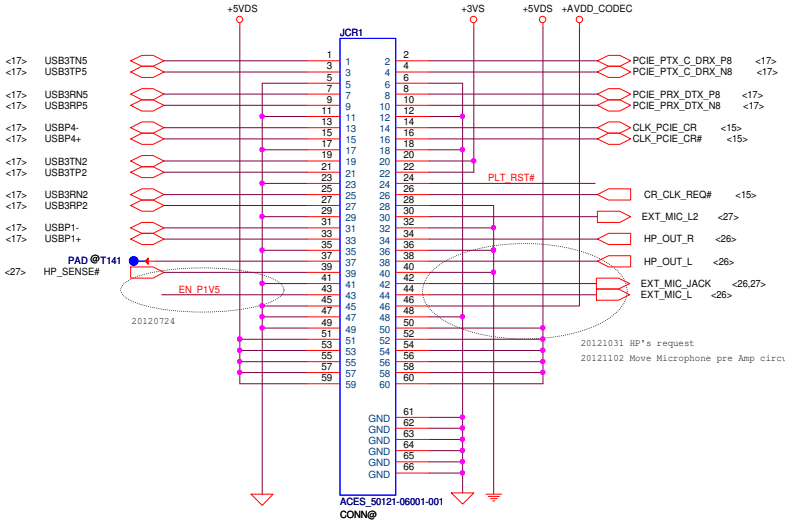
Function Board



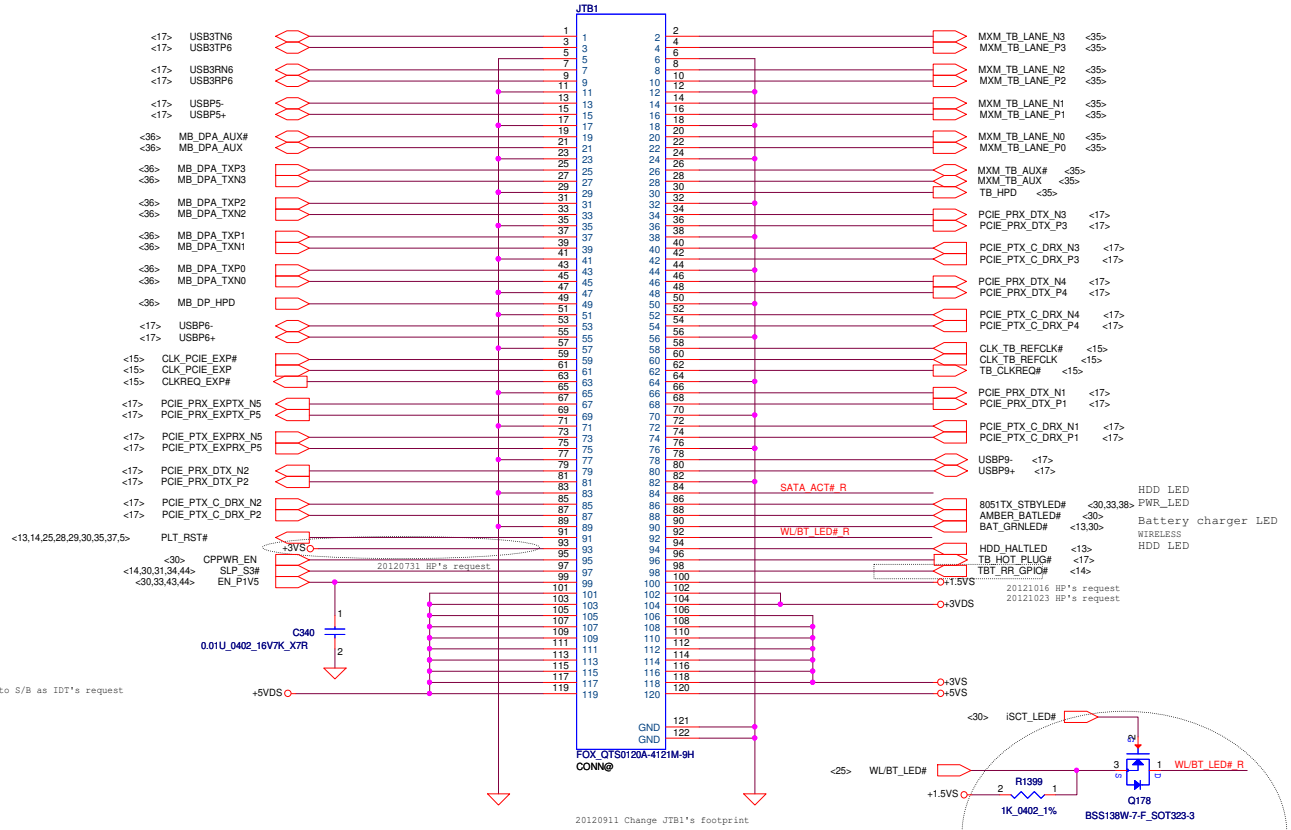
20120715 Correct JFB1's footprint
20120912 Correct JFB1's footprint & Pin assignment

USB & Card Reader Board



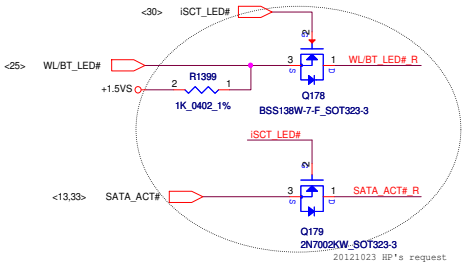
20120724
20121031 HP's request
20121102 Move Microphone pre Amp circuit to S/B as IDT's request

Thunderbolt

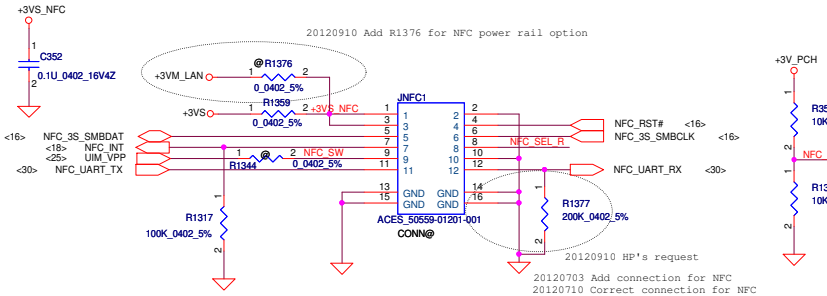


HDD LED
PWR_LED
Battery charger LED
WIRELESS
HDD LED

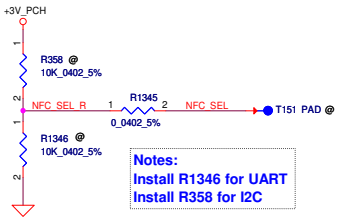
20120731 HP's request
20121016 HP's request
20121023 HP's request
20120911 Change JTB1's footprint



20121023 HP's request
20121025 HP's request



20120910 HP's request
20120703 Add connection for NFC
20120710 Correct connection for NFC
20120724 Add connection as HP's request
20120730 Correct footprint for JNFC1
20120815 Add R1359 for NFC power rail option



Notes:
Install R1346 for UART
Install R358 for I2C

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

Compal Electronics, Inc.

Title: **CONN**

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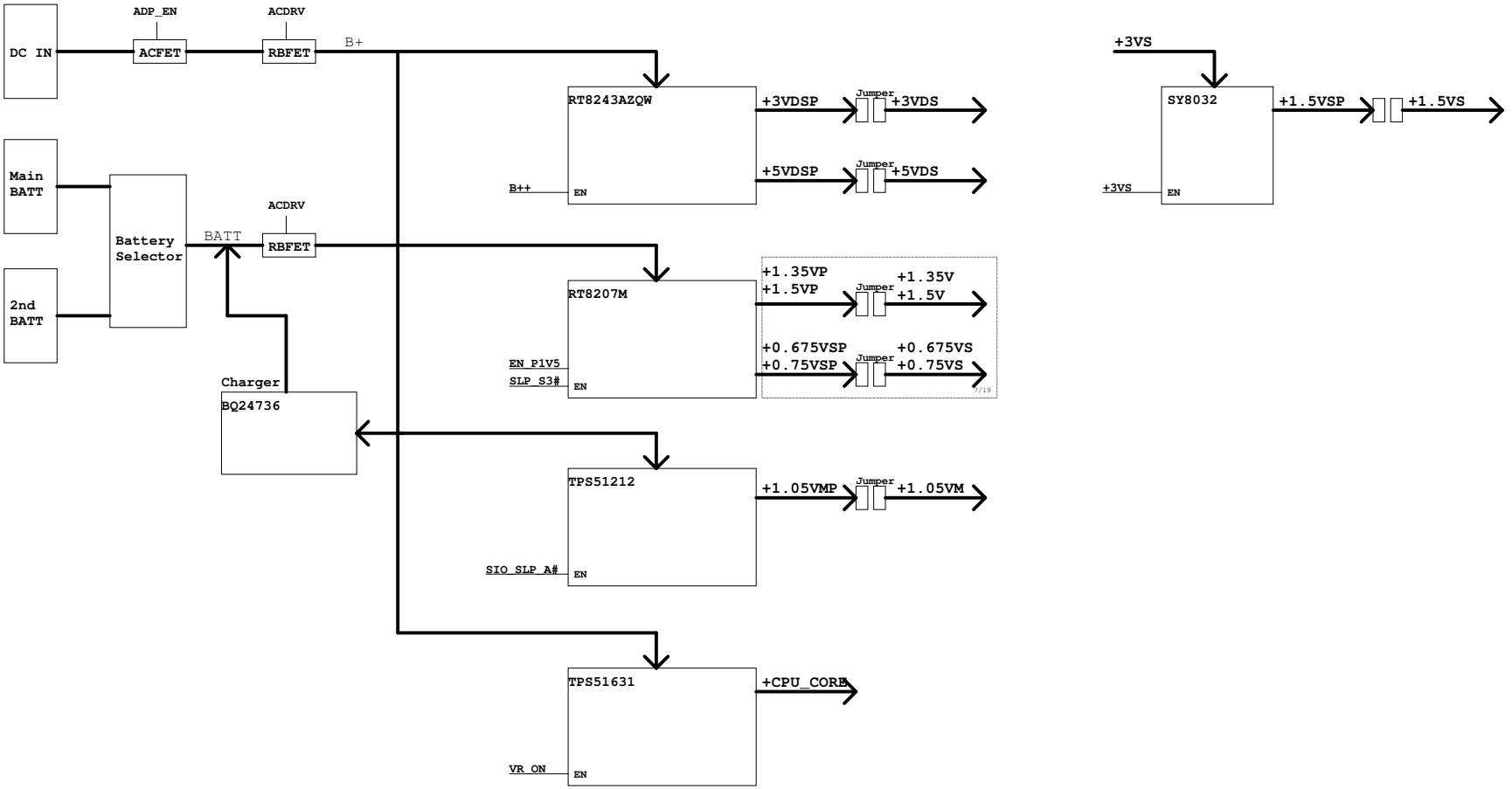
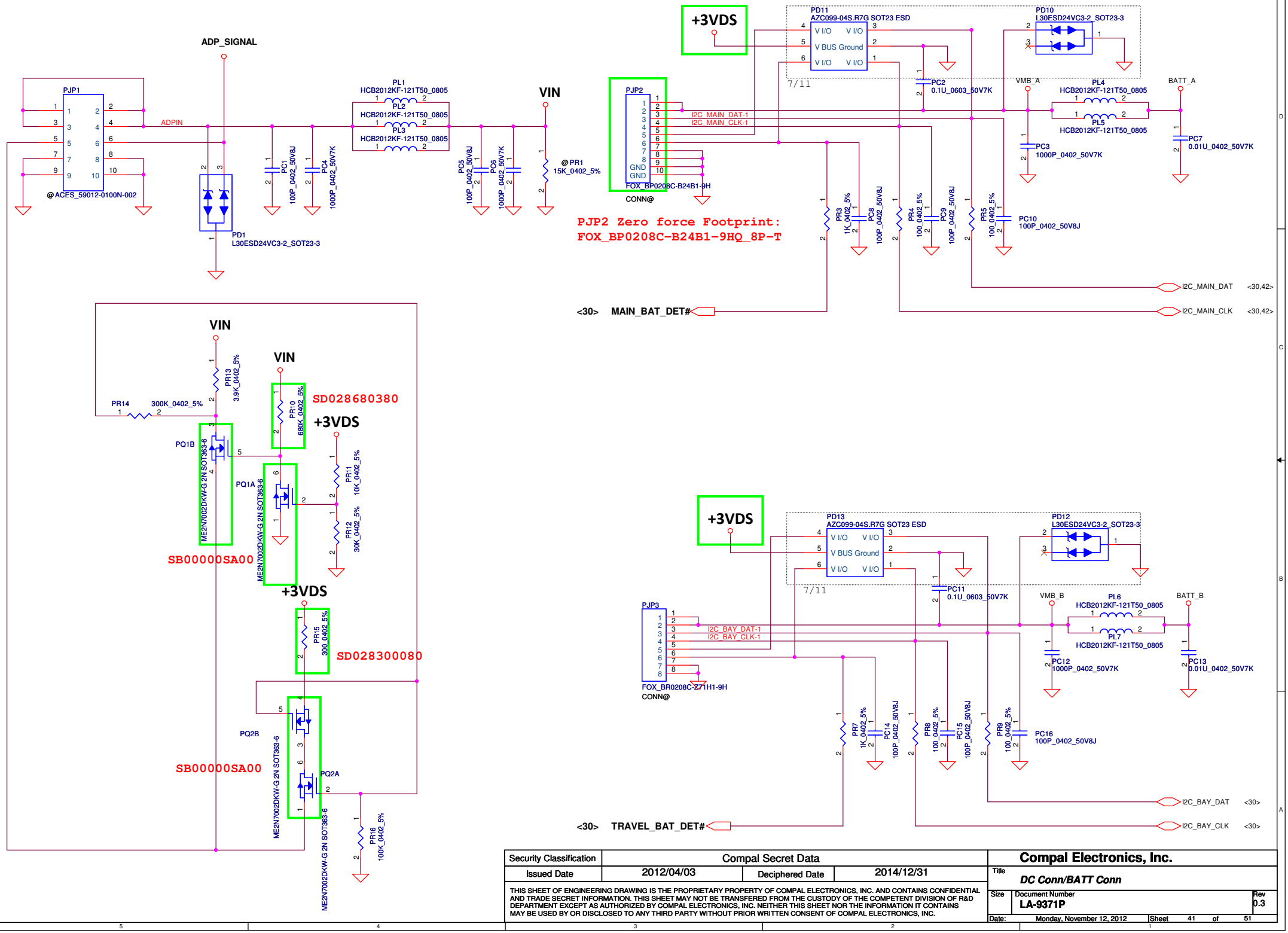

DC IN
ADP_EN
ACFET
ACDRV
RBFET
B+
Main BATT
2nd BATT
Battery Selector
BATT
ACDRV
RBFET
Charger
BQ24736
RT8243AZQW
B++
EN
+3VDSP
Jumper
+3VDS
+5VDSP
Jumper
+5VDS
RT8207M
EN_P1V5
SLP_S3#
EN
+1.35VP
+1.5VP
Jumper
+1.35V
+1.5V
+0.675VSP
+0.75VSP
Jumper
+0.675VS
+0.75VS
TPS51212
SIO_SLP_A#
EN
+1.05VMP
Jumper
+1.05VM
TPS51631
VR_ON
EN
+CPU_CORE
+3VS
SY8032
+3VS
EN
+1.5VSP
+1.5VS



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title	*DC Conn/BATT Conn*		
Size	Document Number: **LA-9371P**		Rev: 0.3
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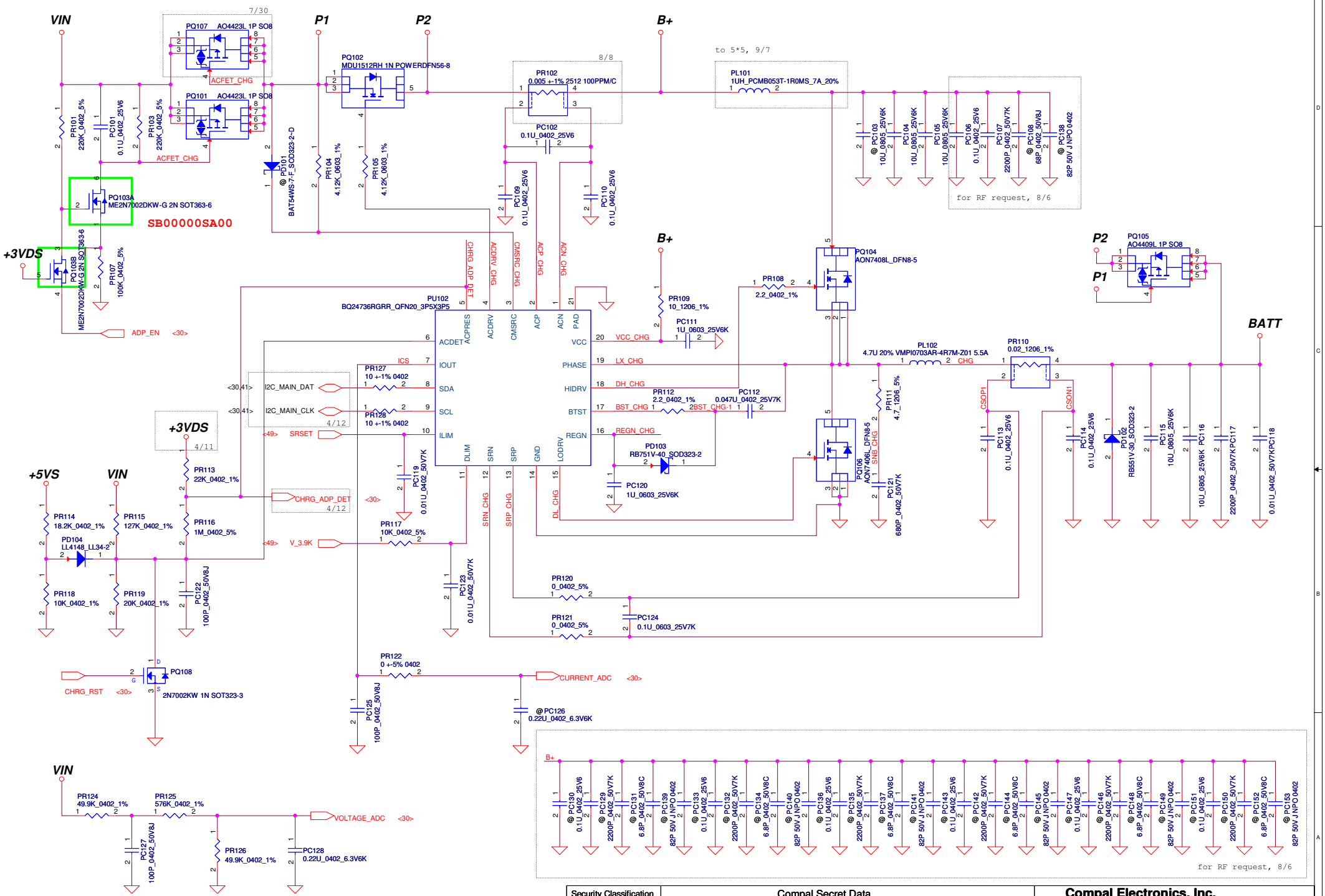

Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.	
Title	CHARGER
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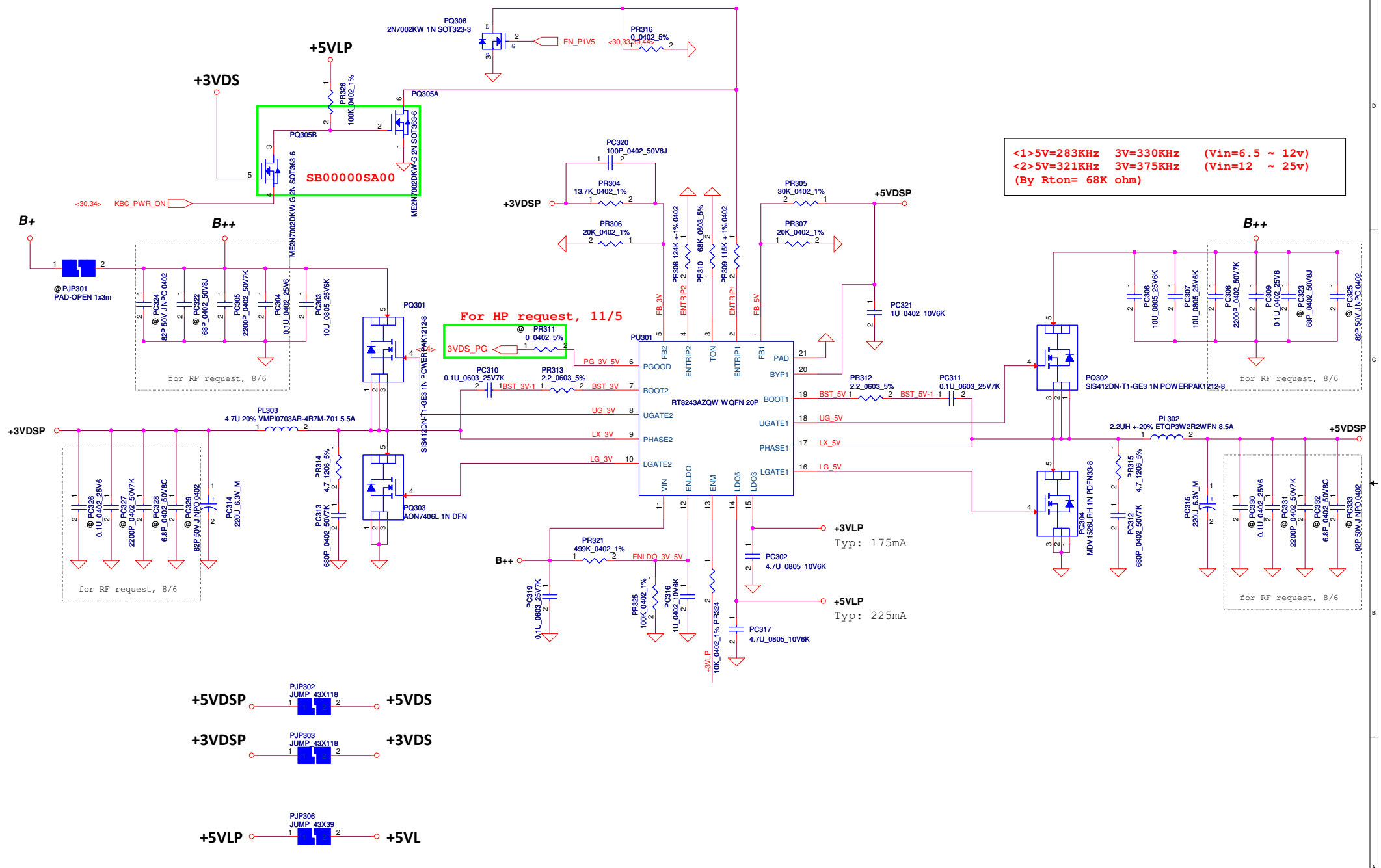

Security Classification	Compal Secret Data		
Issued Date	2011/06/13	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title	3VDSP/5VDSP		
Size: Custom	Document Number: 15W		Rev: 0.3
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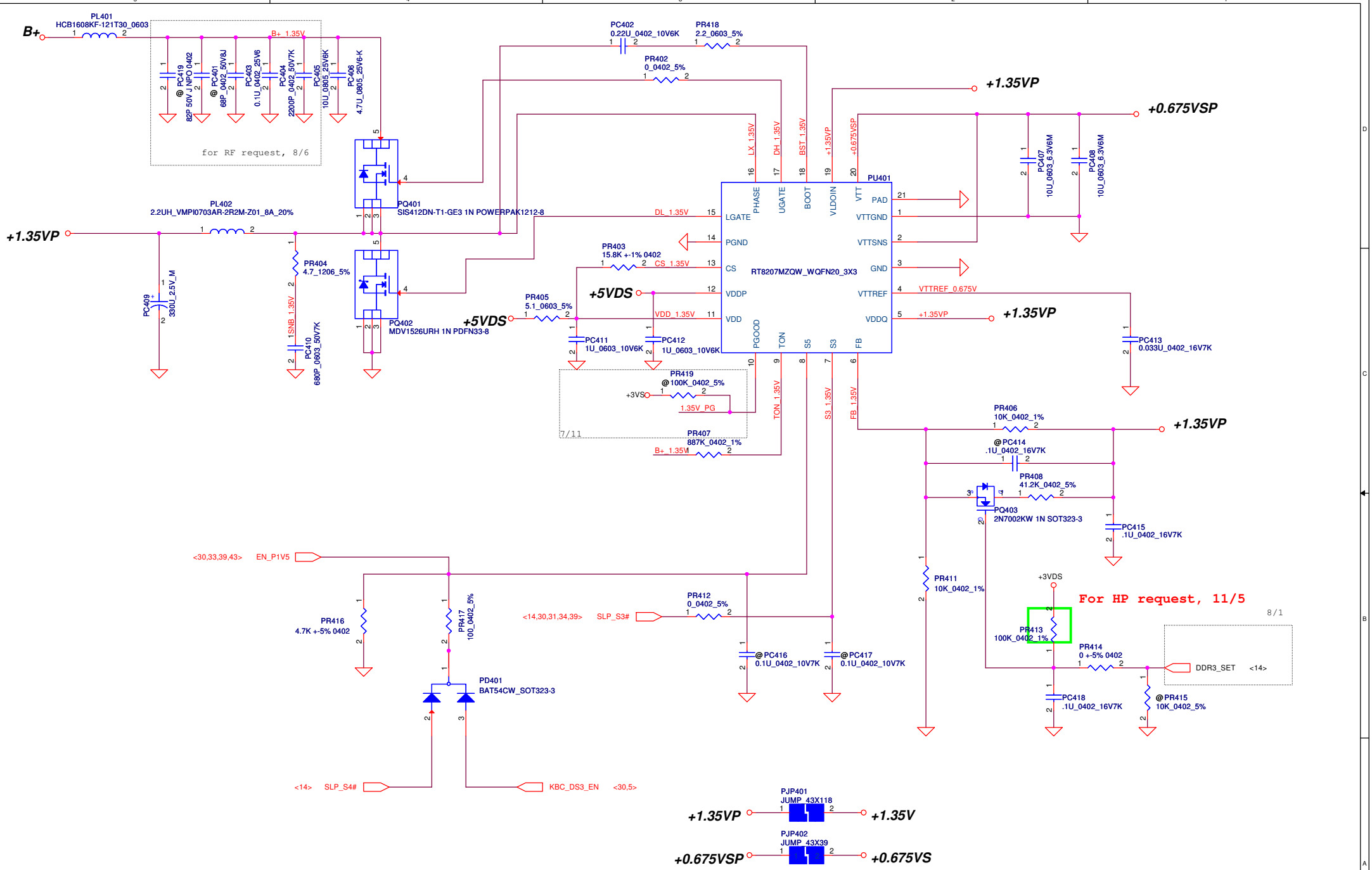

Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title	*DDR Power*		
Size	Document Number: **LA-9371P**		Rev: 0.3
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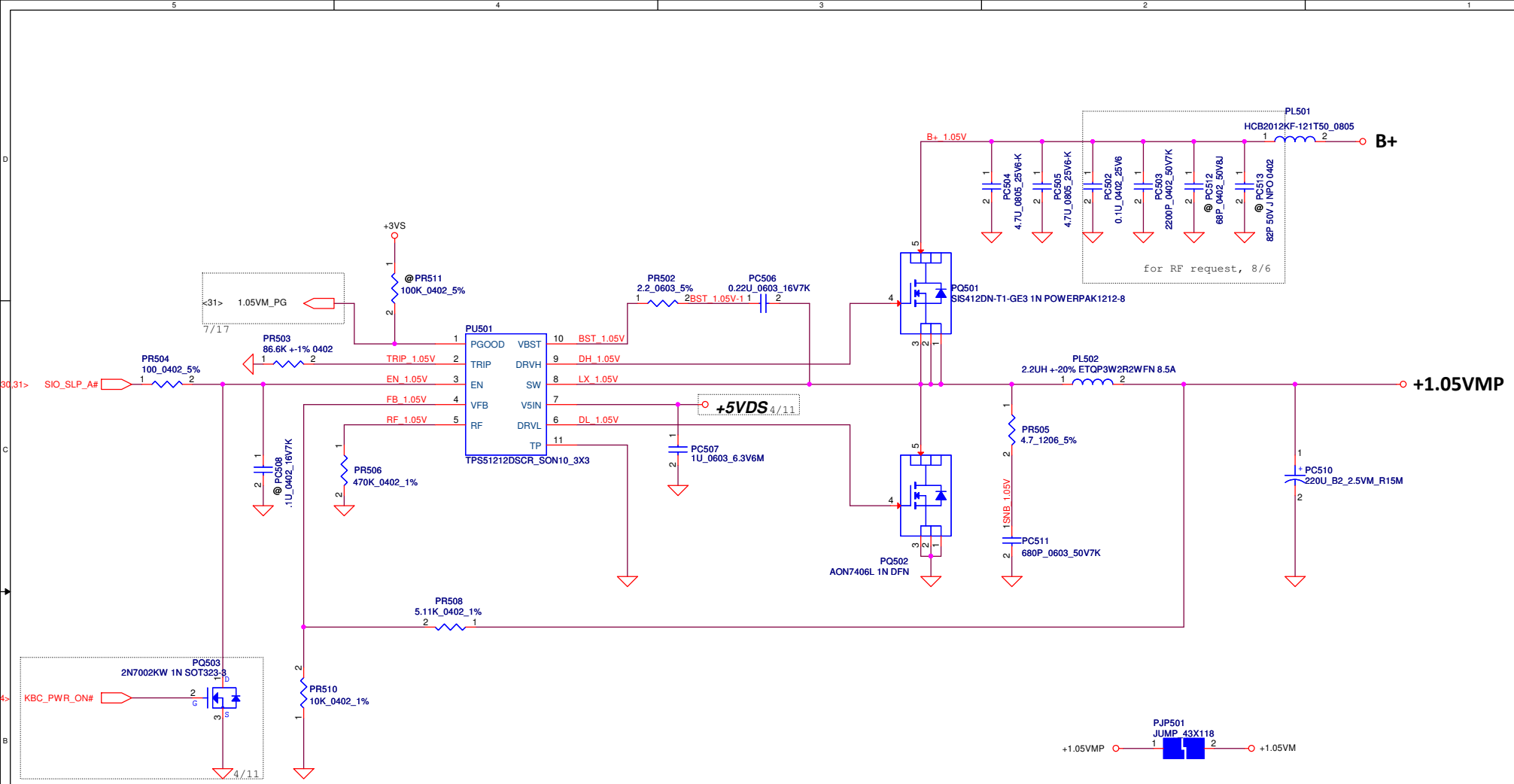

Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title	*1.05VMP*	
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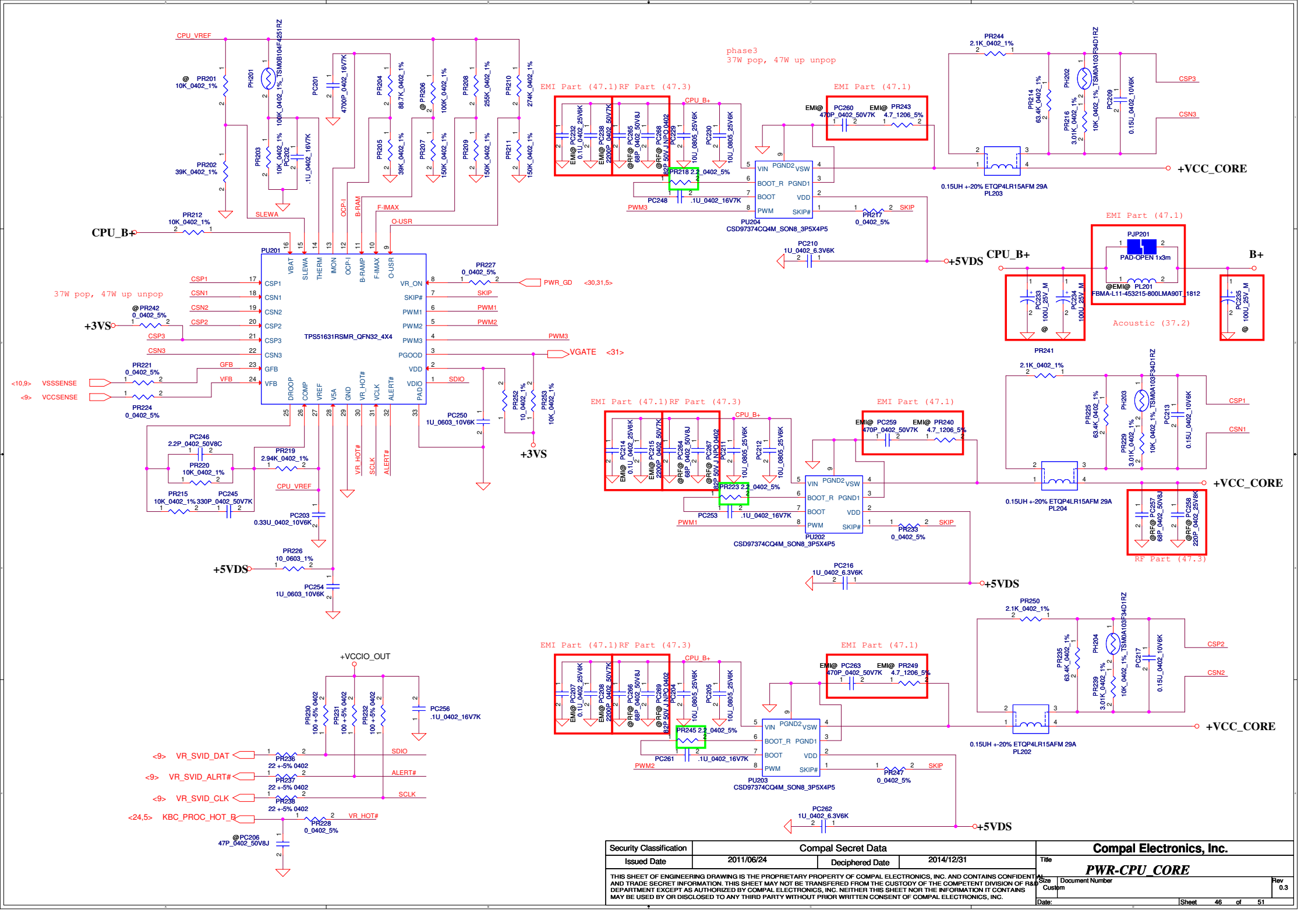

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: ***PWR-CPU_CORE***

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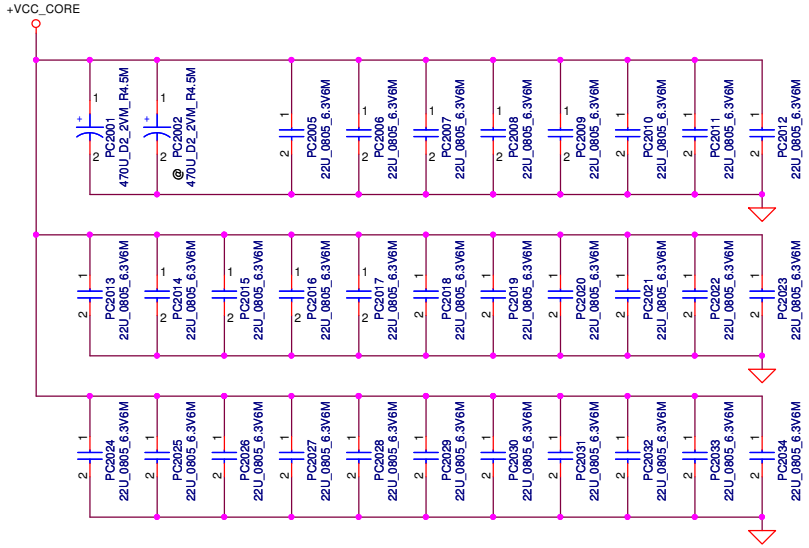
+VCC_CORE

2 X 470u/4m
30 X 22u/0805



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: ***PROCESSOR DECOUPLING***

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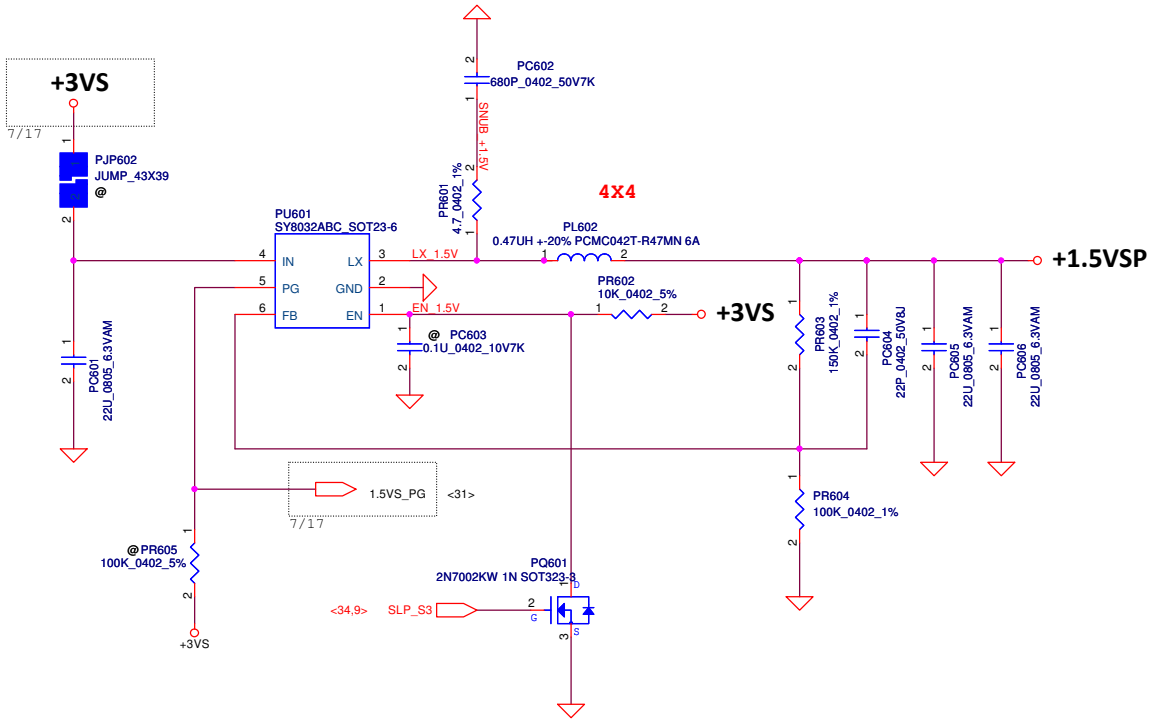

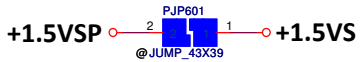

+1.5V_PCIEP
TDC=0.46A
Peak Current=0.66A

Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title	*1.5VSP*	
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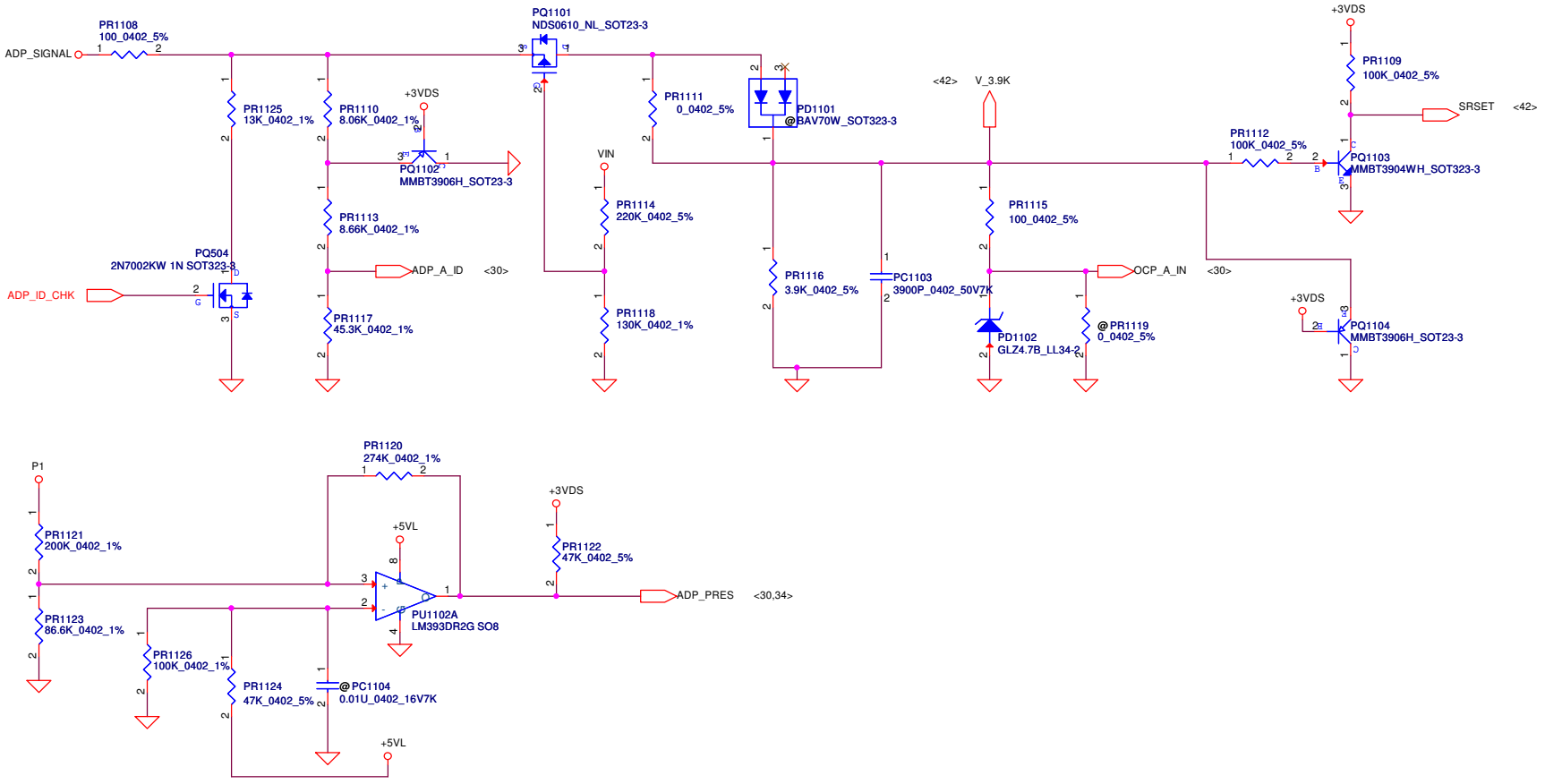

Compal Electronics, Inc.

Title	*ADP_OCP*
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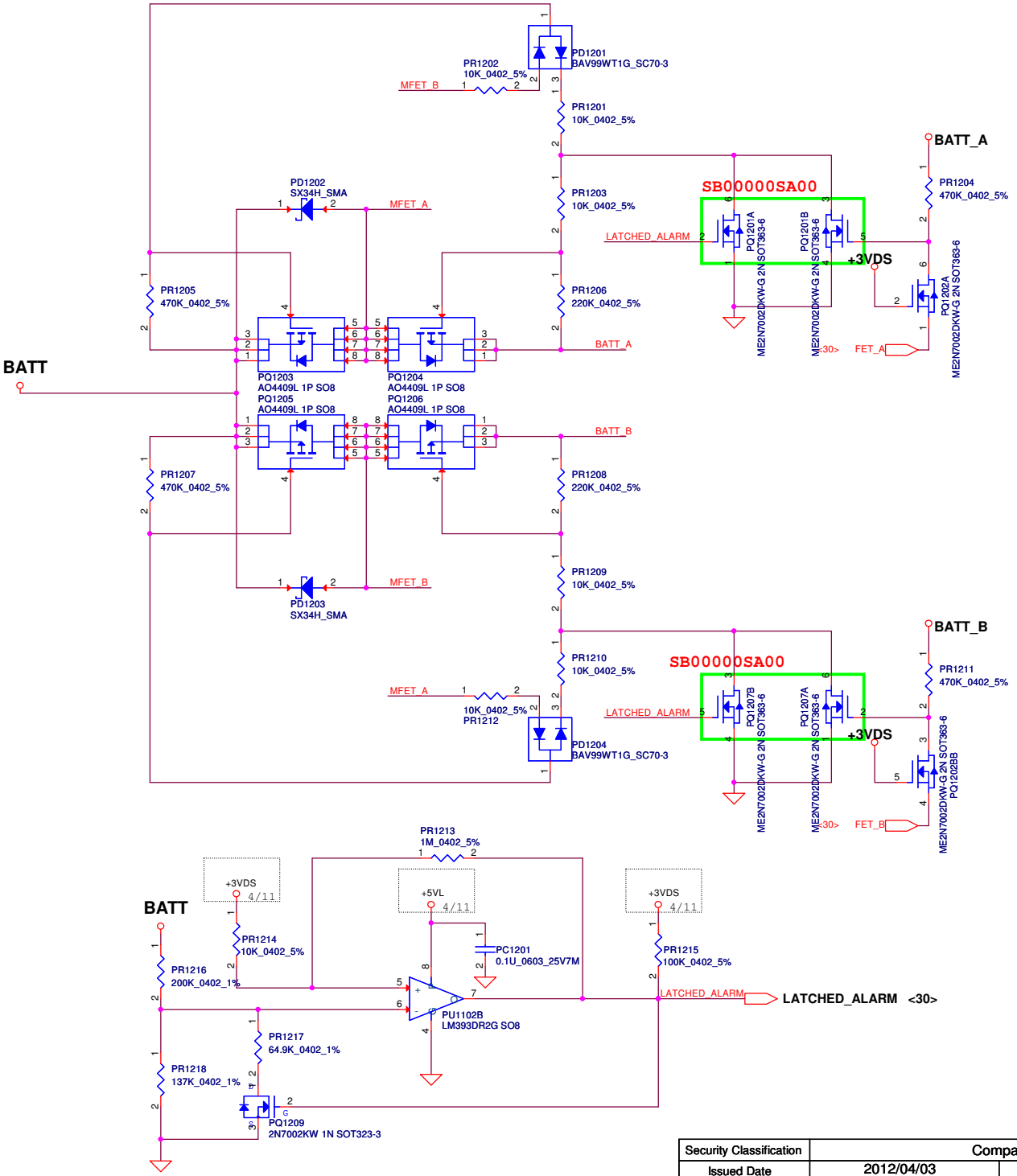

Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: ***Battery selector***

Size | Document Number: **LA-9371P** | Rev: 0.3

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
			2012/08/06				
1	42	Reserve PC130,129,131,139,133,132,134,140,136,135,137,141,143,142,144,145,146,147,148,149,151,150,152,153,138	2012/08/06			RF solution	
2	43	Reserve PC324,322,323,325326,327,328,329,330,331,332,333	2012/08/06			RF solution	
3	43	Add PC305,304,308,309	2012/08/06			RF solution	
4	44	Reserve PC419,401	2012/08/06			RF solution	
5	44	Add PC403,404,405	2012/08/06			RF solution	
6	45	Reserve PC512,513	2012/08/06			RF solution	
7	45	Add PC502,503	2012/08/06			RF solution	
8	47	Reserve PC264,267,266,269,265,268	2012/08/06			RF solution	
9	47	Add PC214,215,207,203,232,236	2012/08/06			RF solution	
10	47	Change PC233,234 from SF000001280 to SF000004M00	2012/08/09			Change the hieght to 6mm	
11	46	Change PR234 from 19.1K to 62K	2012/08/10			HP suggestion	
12	47	Change PQ203,204,211 from SB00000K300 to SB00000U300	2012/09/11			Design change	
13	47	Change PQ201,205,209 from SB00000SJ00 to SB00000W200	2012/09/13			Design change	
14	43	Change PQ301,302 from SB00000JM00 to SB00000IA00	2012/09/17			Design change	
15	43	Change PQ303 from SB00000CT00 to SB00000H700	2012/09/17			Design change	
16	43	Change PQ304 from SB00000N800 to SB00000TZ00	2012/09/17			Design change	
17	44	Change PQ401 from SB00000H800 to SB00000IA00	2012/09/17			Design change	
18	44	Change PQ402 from SB00000N800 to SB00000TZ00	2012/09/17			Design change	
19	45	Change PQ501 from SB00000H800 to SB00000IA00	2012/09/17			Design change	
20	45	Change PQ502 from SB00000N800 to SB00000H700	2012/09/17			Design change	
21	50	Reserve PR1101,1102,1103,1104,1105,1106,1107,PC1101,1102,PD1101	2012/09/25			HP suggestion	
22	44	Change PD401 from SC600000D00 to SCS00006400	2012/10/2			HP suggestion	
23	44	Change PR416 from SD034100380 to SD028470180	2012/10/2			HP suggestion	
24	42	Change PL101 from SH00000MR00 to SH00000NW00	2012/10/2			Design change	
25	47	Change PR240,243,249 from SD001470B80 to SD000010280	2012/10/2			Design change	
26	47	Change PC233 from SF000001280 to SF000004M00	2012/10/2			Design change	

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Title: PWR - PIR

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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	30	KBC	08/18	HP	The quad-mode does not require any GPIO from KBC	Delete R1348 & L R1349 and Add R541 and R542	0.2
2	31	PWR OK	08/18	HP	Makes the power good circuit working.	Non-install R284	0.2
3	26	MXM	08/28	Compal	MXM Card can't be recognized in OS.	Change U37 to MC74VHC1G08DFT2G (Non-OD type)	0.2
4	36	Switch/MUX	09/07	HP	Move D-Sub connector on M/B	Add VGA filter circuit and connector	0.2
5	30	KBC	09/08	HP	SUSCLK is off during DS3 condition	Add Y4, C423, C424 ; Delete R258, R264	0.2
6	30	KBC	09/08	HP	Simplify the KBC solution for MEC1322	Delete R262,R266,R219,R216,R241,R242,R271,R253	0.2
7	25	NGFF	09/08	HP		Add PU resistor for WWAN_FULL_PWR/WWAN_RSVD2	0.2
8	39	NFC	09/10	HP	KBC detection of NFC module	Add 200K (R1377) PD resistor to NFC_UART_RX	0.2
9	39	NFC	09/10	HP	Power rail option for NFC module	Add +3VM_LAN (R1376) for NFC module	0.2
10	9	CPU	09/11	HP		Remove RC102 and RC103	0.2
11	20	PCH	09/11	HP	Connect PCH's pin AD12 to +3V_PCH directly	Remove RH226	0.2
12	5	CPU	09/11	HP	Connect CPU.AT26 pin to CPU_PLTRST# directly	Remove RC66	0.2
13	5	CPU	09/11	HP	Connect CPU.AL34 pin to H_CPUPWRGD directly	Remove RC30	0.2
14	9	CPU	09/11	HP	Connect SLP_S3# to QC5.5 direcly.	Remove RC93	0.2
15	33	DOCKING	09/11	HP	Connect EN_P1V5 to JDOCK1.140 directly.	Remove R351	0.2
16	33	DOCKING	09/11	HP	Connect ON/OFFBTN_KBC# to Docking directly.	Remove R336	0.2
17	15	PCH	09/11	HP	Simplify PCH solution for PCIE CLK Group	Remove RH107,RH103,RH114,RH116,RH122 RH124,RH126,RH127,RH129,RH130	0.2
18	14	PCH	09/11	HP	Reassignement GPIO for "BT_OFF"	Change it from GPIO72 to GPIO61	0.2
19	30	KBC	09/11	HP	Reserve for SUSACK# signal	Uninstall R436 and add R1378	0.2
20	18	PCH	09/11	HP	Reassigned BRD_ID4 to GPIO40 for CP support and update table for DB1-R	Connect RH180.1 to +3VS & RPH1.8 to GND	0.2
21	30	KBC	09/12	HP	Simplify the KBC solution for MEC1322	Delete R249,R251,R256,R277	0.2
22	36	Switch/MUX	09/12	HP	eDP trace length over Intel's specification	Change solution to PS8321	0.2

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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
23	29	LAN	09/12	HP	Avoid IEEE failure with trace stub lines	Add Lan switch solution PI3L500-AZFEX (U43)	0.2
24	39	I/O CONN	09/12	HP	Move Hall sensor IC on Function board	Add +3VDS & LID_SW# pin to JFB1	0.2
25	22	eDP	09/13	Compal	Avoid LVDS Burn out Risk	Rearrange pin assignment of JEDP1	0.2
26	31	POK CKT	09/13	HP	Modify Power OK circuit	Delete UH7, RH235 ; Add R1379	0.2
27	39	I/O CONN	09/19	HP	Prevent Card Reader can't be recognized issue	Add R1380 for PCH_PCIE_WAKE#	0.2
28	13	PCH	09/19	HP	Disable the unlock of ME descriptor	Change QH11 to P-MOSFET	0.2
29	37	Smart Card	09/20	HP	RC delay is NOT good as reset	Delete CC67,R393, then connect U30.23 to PLT_RST#.	0.2
30	26	CODEC	09/20	HP		Uninstall RA13 and CA20	0.2
31	14	PCH	09/20	HP	KBC appears drives high during S3, so the change to aviod the leakage without losing functionality.	Change RH74 from 10K to 100K Ohm	0.2
32	31	PWR OK	09/23	HP	Modify net name for easy read	Modify VR_ON to PWR_GD and PWR_GOOD_3 to VGATE	0.2
33	5	XDP	09/25	HP		Connect PM_PWROK to JXDP1.47 via 0 Ohm (RC107)	0.2
34	30	KBC	09/25	HP	Resolve ME LAN failures	Delete R537, Q73, D21	0.2
35	35	MXM	09/27	HP	There is yellow bang in device manager	Add pull high resistor (R1382,R1383 & R1384) to +3VS	0.2
36	38	KB Backlight	09/27	HP		Change R408 to 200K Ohm, and uninstall C295	0.2
37	35	MXM	10/11	HP	Certain ports have better drive strength than others when the system is in DC mode	DP port re-assignment	0.3
38	26,27	CODEC	10/11	IDT		Change RA14 to 0Ohm, C95 to 0.47uF, R97,R98,R102,R104 to 1%	0.3
39	5,14 30,34	KBC	10/12	HP	To enable Intel Deep SX	Reserve RC108, UH6, CH113, R1388. Change U17.85 and R1388 connection netname to RSMRST#_EC. Change R455 to 47K, Add Q18A, C431, R1387. Modify +3V_PCH power circuit	0.3
40	9	CPU	10/16	HP	To enable Intel Deep SX	Add QC6 and connect to KBC_PWRON	0.3
41	41	CPU	10/16	HP	To enable Intel Deep SX	Add Q176 and add connection to PLT_DET	0.3

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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
42	25	WLAN	10/16	HP	To enable Intel Deep SX	Delete R64, Install R1354	0.3
43	29	LAN	10/16	HP	To enable Intel Deep SX	Change connection of R1359 to KBC_WAKE#	0.3
44	30	KBC	10/16	HP	To enable Intel Deep SX	Change R227 to 3.3K	0.3
45	30	KBC	10/16	HP	To enable Intel Deep SX	Connect R215.2 to GND, Delete C186	0.3
46	30	KBC	10/16	HP	To enable Intel Deep SX	Remove current VCC1_PWRGD connection to JP6.16. Then add a 4.7 K resistor between JP6.16 and new signal VCC1_PWRGD_SUS#.	0.3
47	30	KBC	10/16	HP	To enable Intel Deep SX	Rename CHARGER_CLK & CHARGER_DAT to KBC_WAKE# & CHRG_RST	0.3
48	30,39	KBC & I/O	10/16	HP	To enable Intel Deep SX	Change R1378 to 100K and rename U17.41 to iSCT_LED# Delete C322 Change JTB1.98 to iSCT_LED#.	0.3
49	30	KBC	10/16	HP		add R1391between U18.6 pin and signal PVT_SCLK	0.3
50	30	KBC	10/16	HP	Simplify the KBC circuit	Connect R215.2 to GND, Delete C186 Change R227 to 10K Delete R239, R240 and connect to KBC (U17) directly. Delete R218 andconnect to KBC (U17) directly.	0.3
51	30	KBC	10/16	HP	Simplify the KBC circuit	Delete R1381 and connect JCR1.5 to +5VDS.	0.3
52	5,9,14 16,20,24 25,30, 34,35	KBC	10/20	HP		Change R615 to 470K, R610 to 470Ohm and RH247 to 10K Change R1387,R137,R1382,R1383,R1384 to 4.7K, RC108 to 10K. Delete Q177,QC1,RC12,QC5B,QC6B,R461,Q2,RC90. Install RH209, R492, RC108, RH246, CH113 and UH6. Uninstall QC3, RH148, RH67, RH208. Change R492.2 connection to PCH_THERMTRIP#_R Connect RH247.1 to PM_RSMRST#. Modify +1.35VS power circuit	0.3
53	14	PCH	10/20	Compal	To solve bring up issue	Add PU resistor (RH248) for GPIO72	0.3
54	14,30,34	PCH	10/23	Compal	HP Deep SX implementation	Delete R1387, Uninstall RH246,CH113,UH6,RH209,Q176,RH247 Install RH67,RH208 ;Add 4.7K (R1392) between KBC 124 pin and signal SIO_SLP_SUS#,	0.3

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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
55	14,39	PCH, I/O	10/23	HP	For Intel ThunderBolt REDWOOD	Change PCH.AL6 to TBT_RR_GPIO# Change RH245.2 to TBT_RR_GPIO# Change JTB1.98 to TBT_RR_GPIO#	0.3
56	39	I/O	10/23	HP	For iSCT_LED# function	Add Q177 for control HDD & Wireless LED	0.3
57	25	Wireless LED	10/24	HP	Create about 1.36V with 47K PU when WL LED is off	Add PD 33K (R1393) for WL/BT_LED#	0.3
58	28	G-Sensor	10/24	HP	Current connection is incorrect	Connect ACCEL_INT# to U9 's pin11and leave pin 9 as NC	0.3
59	18	PCH	10/24	HP		Connect RH176.2 to GND (from +3VS) and install RH176 Install RH185	0.3
60	25	WLAN	10/24	HP		Add serial resistor R1394,R1395,R1396 for CLINK signals	0.3
61	14	PCH	10/25	HP		Add RH249 for SLP_LAN# and change RH70 to 200K	0.3
62	14,29	PCH, LAN	10/25	HP	To provide isolation	Add PU RH250 for LANWAKE# and Q177 for isolation	0.3
63	25	WLAN	10/25	HP		Delete R89 and R1393	0.3
64	39	I/O	10/25	HP	For iSCT_LED# function	Change Q178 to BSS138 and Add R1393	0.3
65	35	MXM	10/25	HP	For MXM GPIO8 issue	Combine Q61/Q62 to Dual 2N7002 (Q61) and Delete R137	0.3
66	34	DC-DC	10/25	HP	S5 power consumption concern.	Change R455 to 200K and add PD 100K (R1398)	0.3
67	29	LAN	10/26	HP	+5VDS may disappear during Deep S4/S5	Connect R376.1 to +3VDS and change R376 to 10K	0.3
68	29	LAN	10/26	HP		Connect DOCK_LED_LINK_LAN# to Q34.1and delete R153	0.3
69	18,32	PCH, Super I/O	10/26	HP		Reassign Super I/O GPIO45 as mSATA_DET#	0.3
70	17	PCH	10/26	HP		Reassign GPIO59 as WWAN_DET#_PCH and connect to JMINI3	0.3
71	13	PCH	10/26	HP		Swap QH11A.2 and QH11B.5 connection	0.3
72	35	MXM	10/28	HP	For MXM GPIO8/GPIO9 issue	Change MOS to Diode RB-751(D5) and R1383 to 300 Ohm	0.3
73	35	MXM	10/28	HP		Connect Q60 pin 2 & pin 5 to DGPU_PWROK	0.3
74	31	PWR OK	10/31	HP	To ensuret +5VDS power off	Connect R291.1 to +5VL and change it to 105K Ohm	0.3
75	39	I/O	10/31	HP		Change JCR1.48 & 50 from +3VDS to +3VS	0.3
76	29	LAN	11/2	HP	Avoid NIC internal PHY voltage drop	Reserve 10uF (C428) & change C351 to 47uF	0.3
77	27	Audio	11/2	Compal	OBS#894504- SVTP-DB1R_AB1.0: Can't record sound via audio jack with external headphone	Delete Q1AB & R174 then connect HP_SENSE# to R167	0.3
78	9	CPU	11/4	Compal		Change connection of QC5A.2 & QC5B.5 to SLP_S3	0.3

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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
79	5,15	CPU,PCH	11/04	HP		Add CLKOUT_ITPXDP signals to JXDP1 pin 40 & 42	0.3
80	15	PCH	11/04	HP	To follow ME ICC setting	Change CLK_PCIE_CR# to LPT CLKOUT port 0	0.3
81	14	PCH	11/06	HP	For the down power sequencing	Correct connection of RH246 to 3VDS_PG	0.3
82	15	PCH	11/06	HP	Avoid leckage	Change CLK_PCIE_CR# back to LPT CLKOUT port 1	0.3
83	17,25	PCH	11/06	HP	Follow GPIO table	Correct net name to WWANSSD_M12DET and connection	0.3
84	14,25	PCH	11/06	HP	Follow GPIO table	Correct net name to DDR3_SET and delete Q68,R459	0.3

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