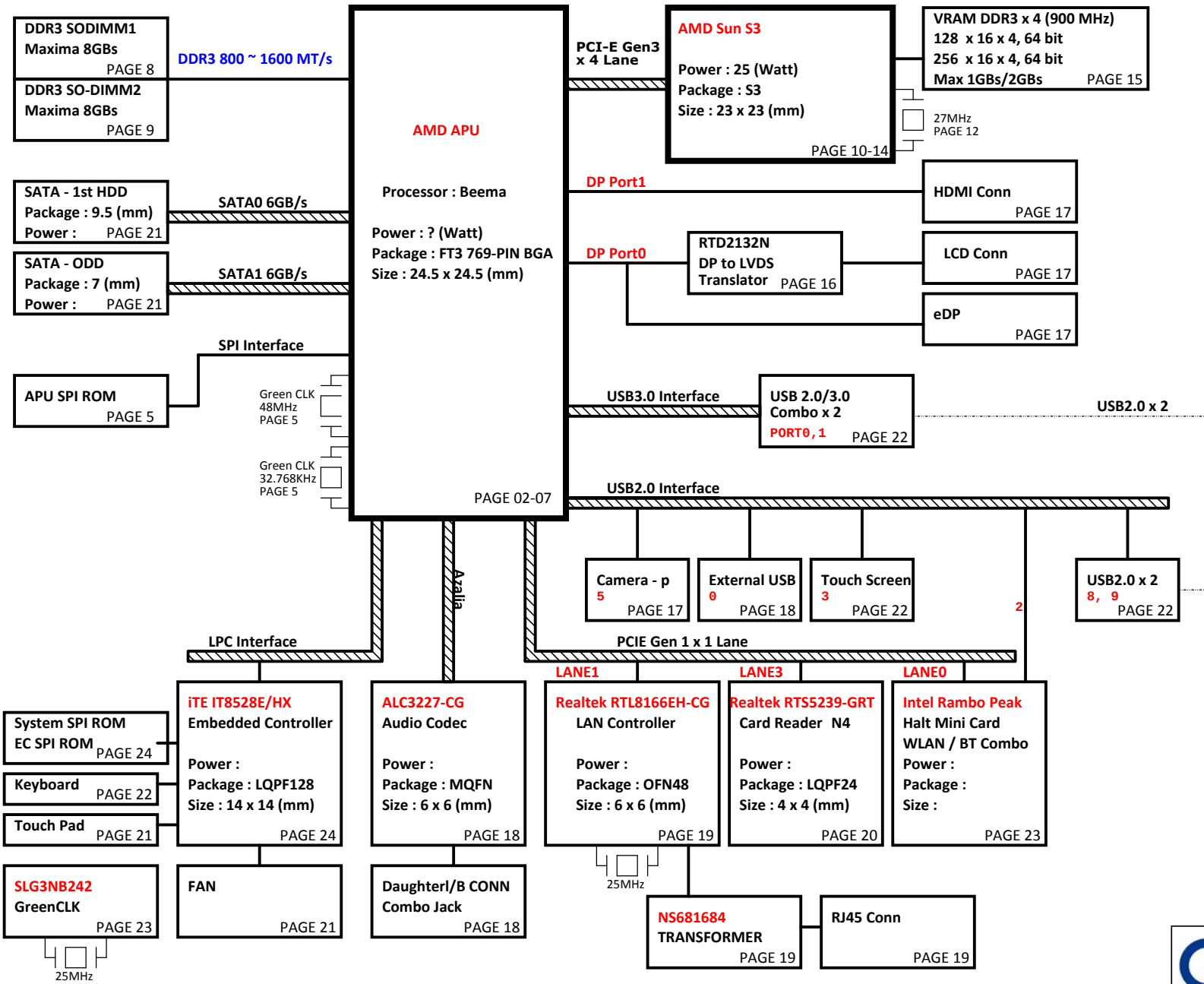
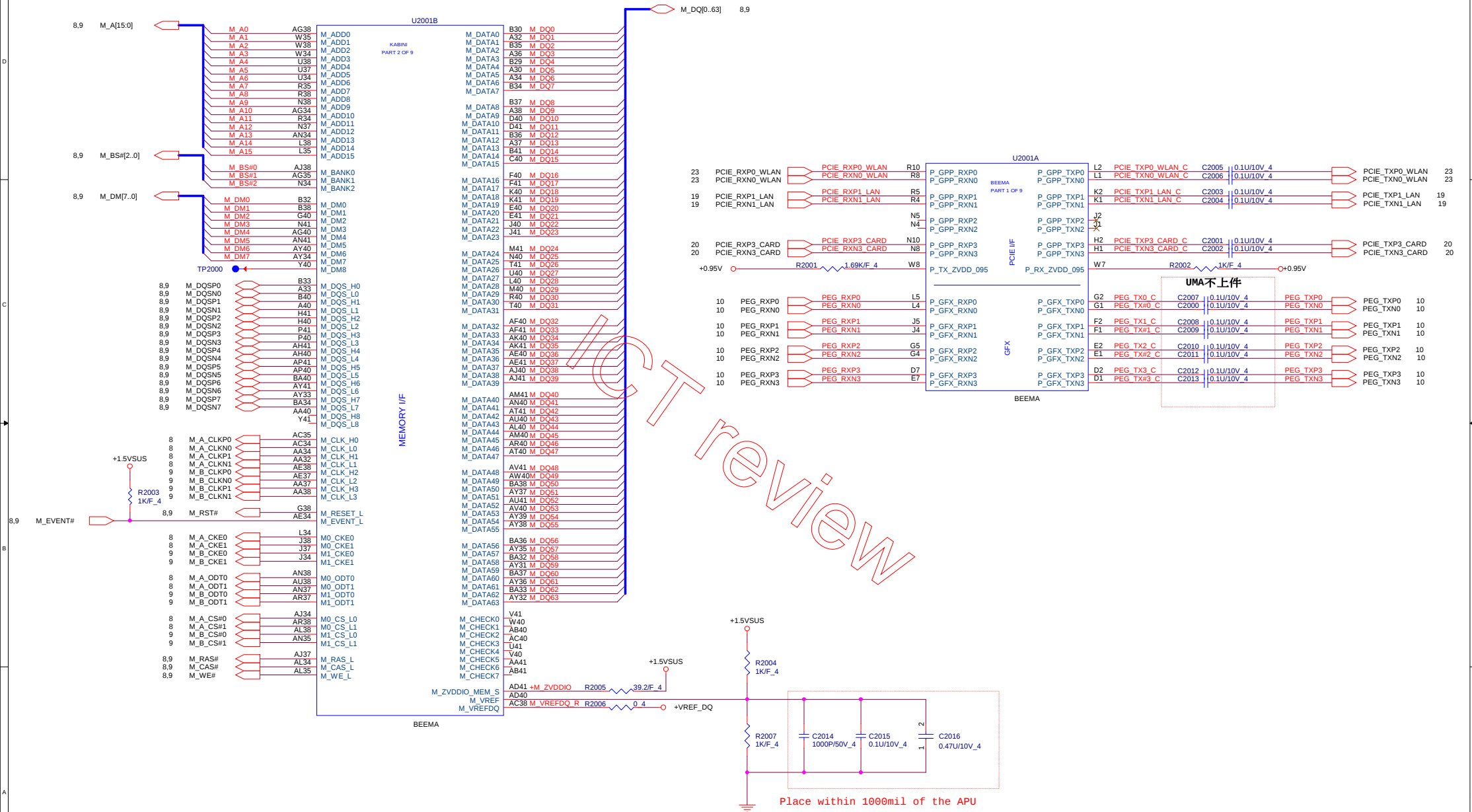


Lean G_AMD Beema DIS/UMA (14"/15.6")

Ultra/Slim⁰¹



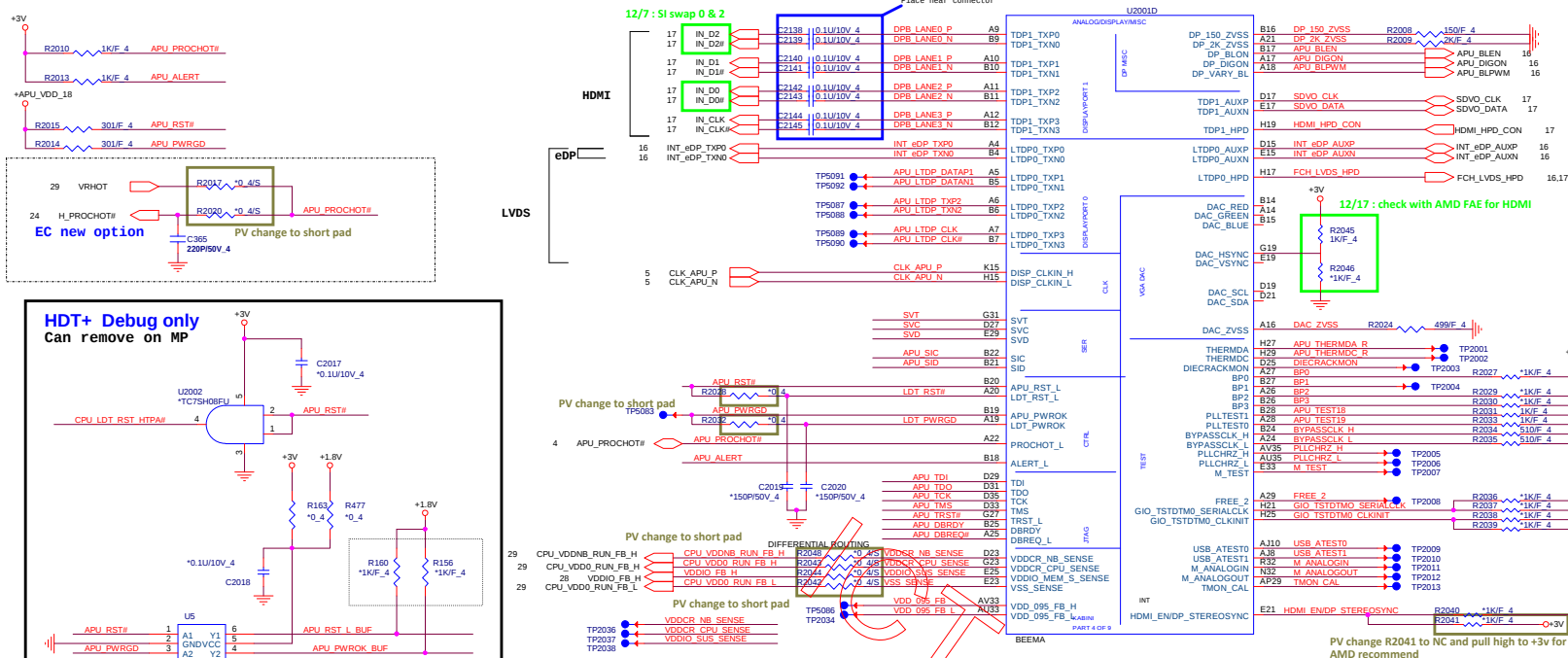
- PCB 6L STACK UP**
- LAYER 1 : TOP
 - LAYER 2 : SGND
 - LAYER 3 : IN1(High)
 - LAYER 4 : IN2(Low)
 - LAYER 5 : SVCC
 - LAYER 6 : BOT
- Power Source**
- TI BQ24728**
System Charge Power (+BATCHG)
PAGE 25
 - Ricteck RT8223PZ**
System Power (+3VPCU/+5VPCU/+3VSS/+5VSS)
PAGE 26
 - AOZ1237QI/APW8824CTI/G9183**
KABINI Power (+0.95V/+0.95VSS/+1.5VSS)
PAGE 27
 - TI TPS51216**
System Memory Power (+1.5VSUS/+0.75V_DDR_VTT)
Ricteck RT8068A
KABINI Power (+1.8VSS)
PAGE 28
 - Intersil ISL6277HRTZ/ISL6208BCRZ**
Processor Power (+VCC_CORE/+VDDNB_CORE)
PAGE 29~30
 - GMT G5934RZ1U**
System Discharge Power (+1.5V/+3V/+5V) (+3VSUS/+3VLAVCC/+1.8V)
PAGE 31
 - On-semi ADP3211A**
VGA Power (+VGA_CORE)
PAGE 32
 - Ricteck RT8086A**
DGPU Power (+1.0V_VGA/+3V_VGA/+1.5V_VGA/+1.8V_VGA/)
PAGE 33



6,8,9,28,31,33
8,9
5,6,27

+1.5VSUS
+VREF_DQ
+0.95V

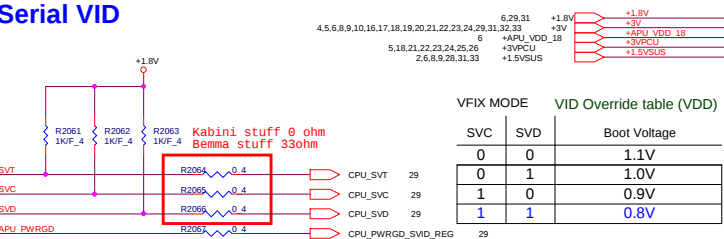
+1.5VSUS
+VREF_DQ
+0.95V



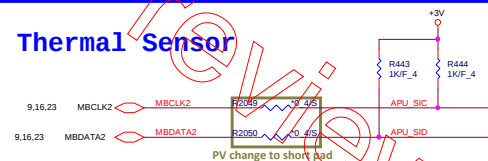
HDT+ Connector for Debug only



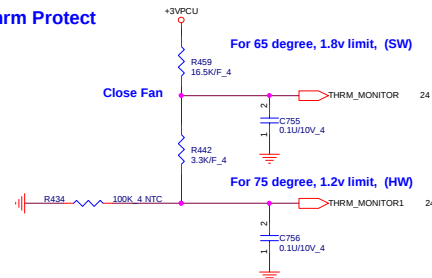
Serial VID

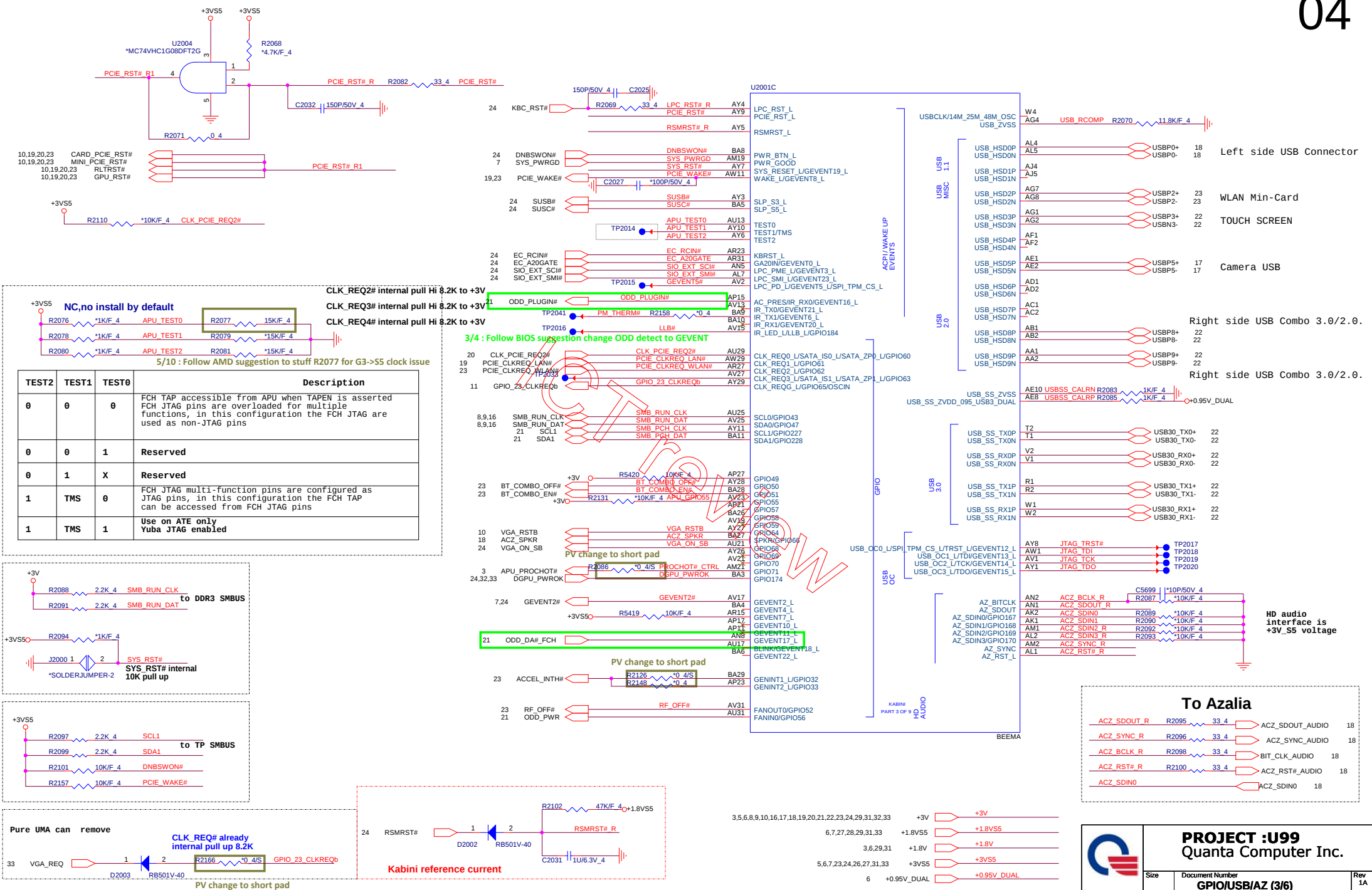


Thermal Sensor



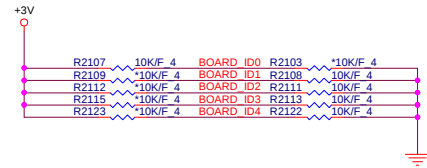
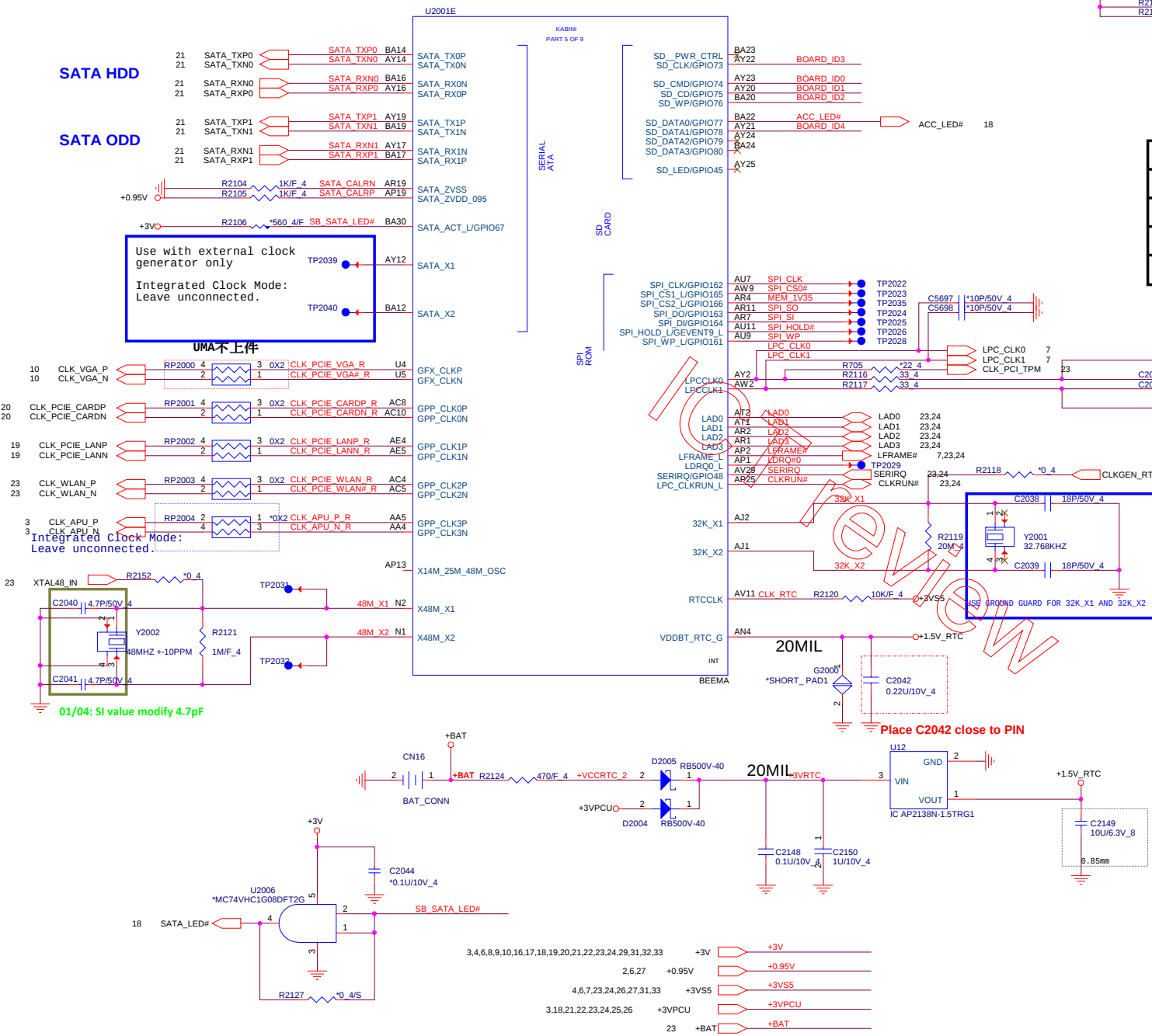
IO Thrm Protect





SATA HDD

SATA ODD

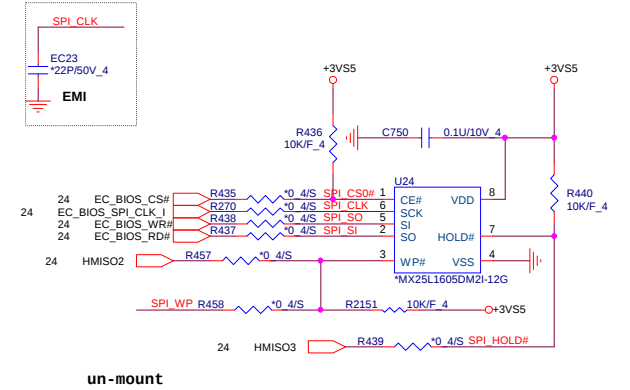


BOARD ID SETTING

Model	BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	BOARD_ID4
14" UMA	0	0	0	0	0
15" UMA	0	1	0	0	0
14" DIS	1	0	0	0	0
15" DIS	1	1	0	0	0

APU SPI ROM
Replace to MX25L6436E

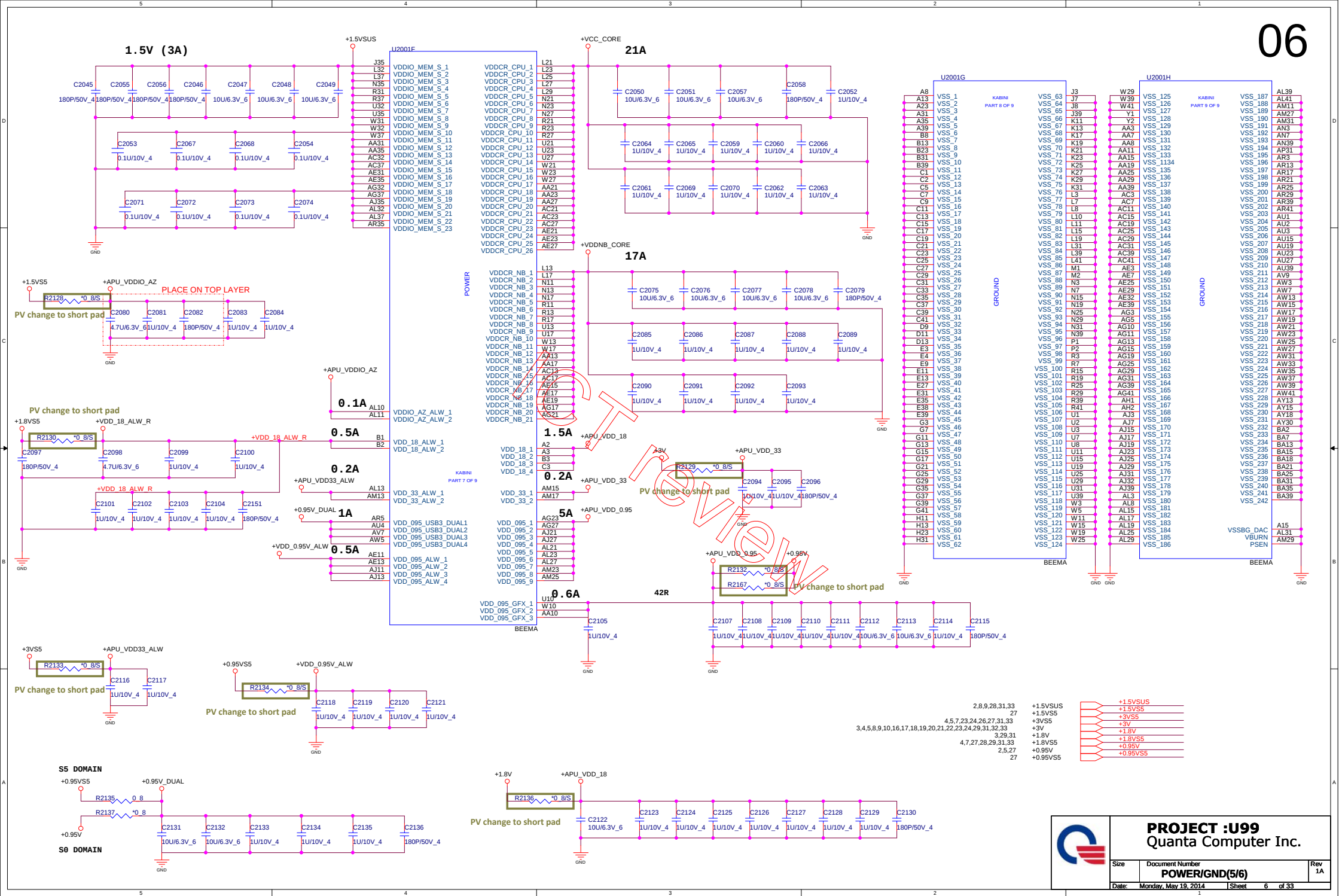
Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023





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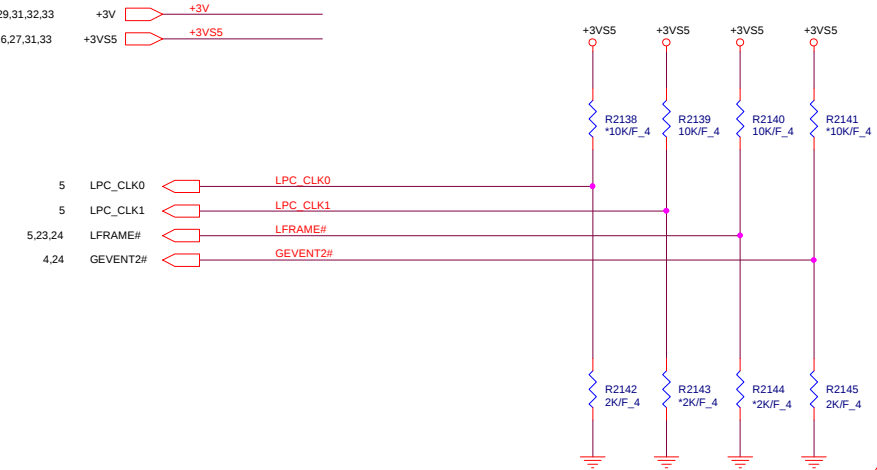
Size	Document Number	Rev
	SATA/CLK (4/6)	1A
Date:	Monday, May 19, 2014	Sheet 5 of 33



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

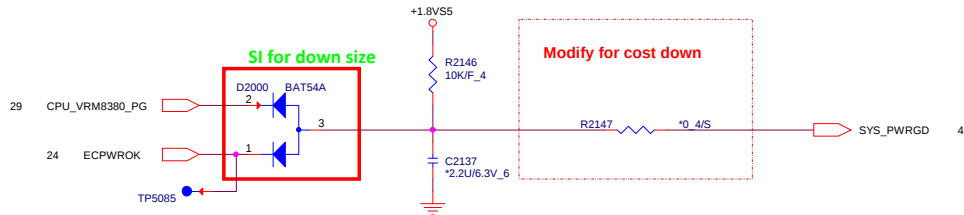
DEBUG STRAPS



REQUIRED STRAPS

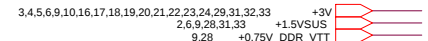
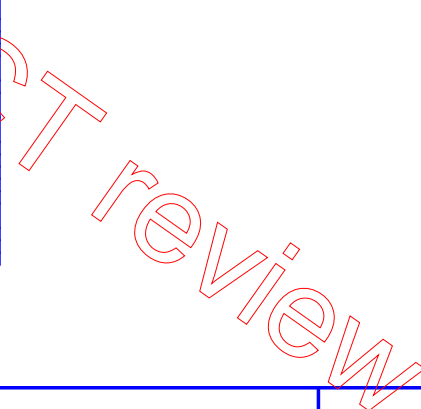
					LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH					BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW					BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT

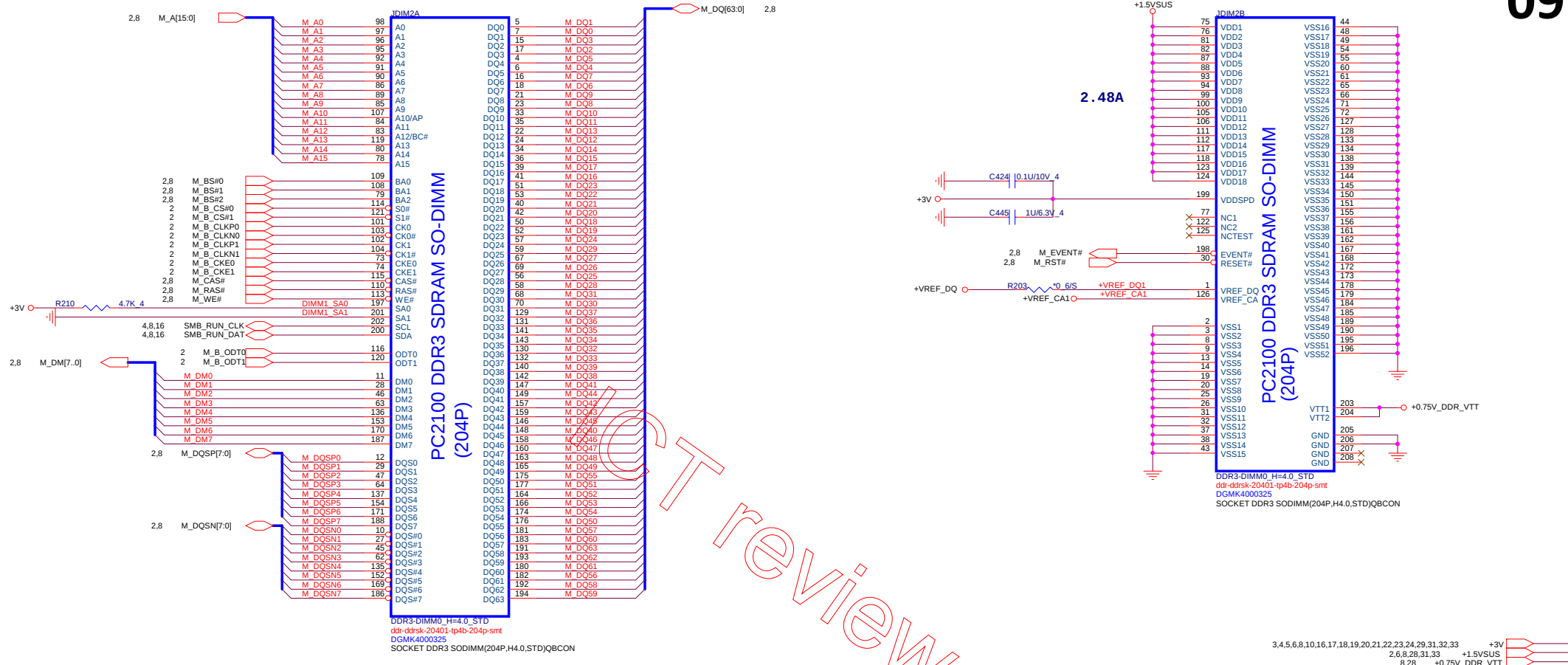
SYS PWGRD



PROJECT :U99
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Size	Document Number	Rev
	STRAP (6/6)	1A
Date:	Monday, May 19, 2014	Sheet 7 of 33





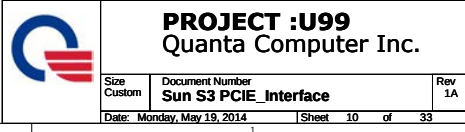
Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)



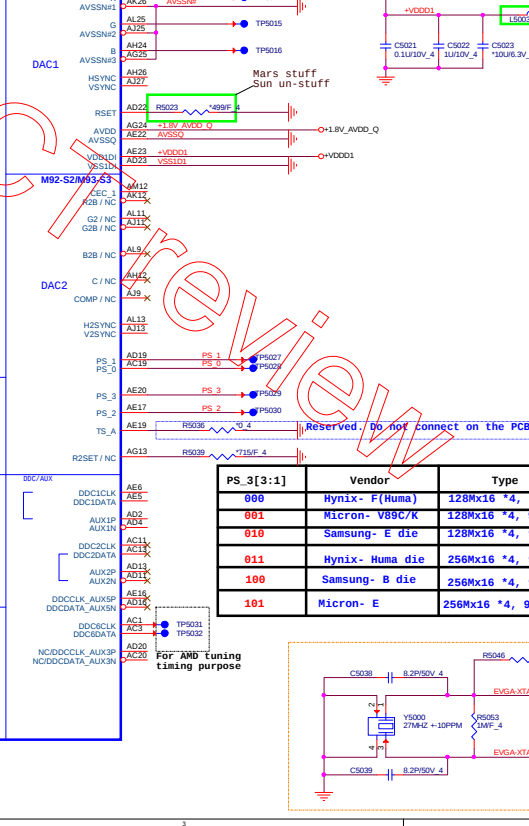
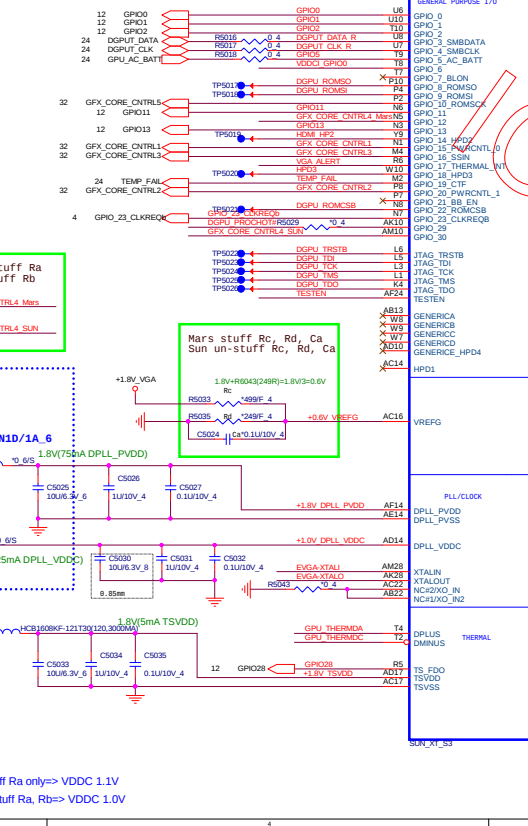
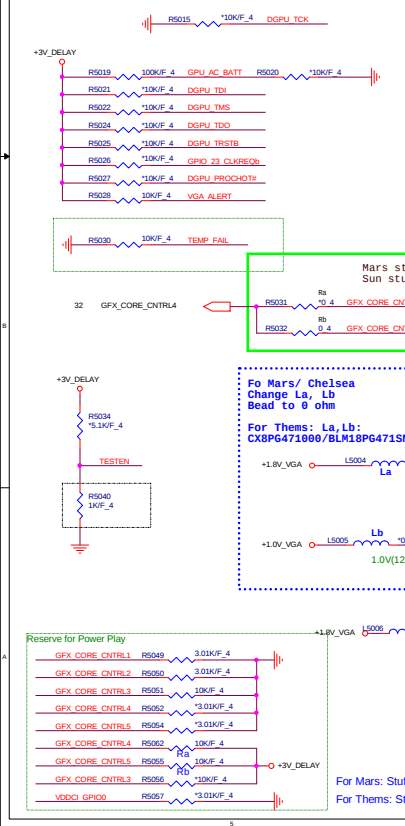
PROJECT :U99
Quanta Computer Inc.

Size	Document Number	Rev
Custom	System Memory 2/2 (9.2H)	1A
Date: Monday, May 19, 2014	Sheet 9 of 33	

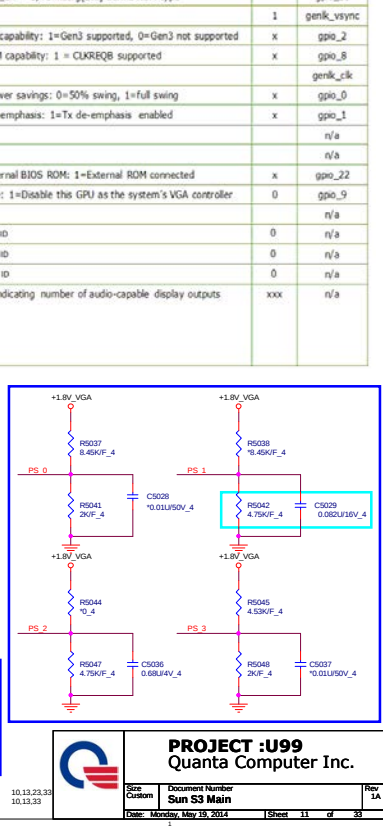


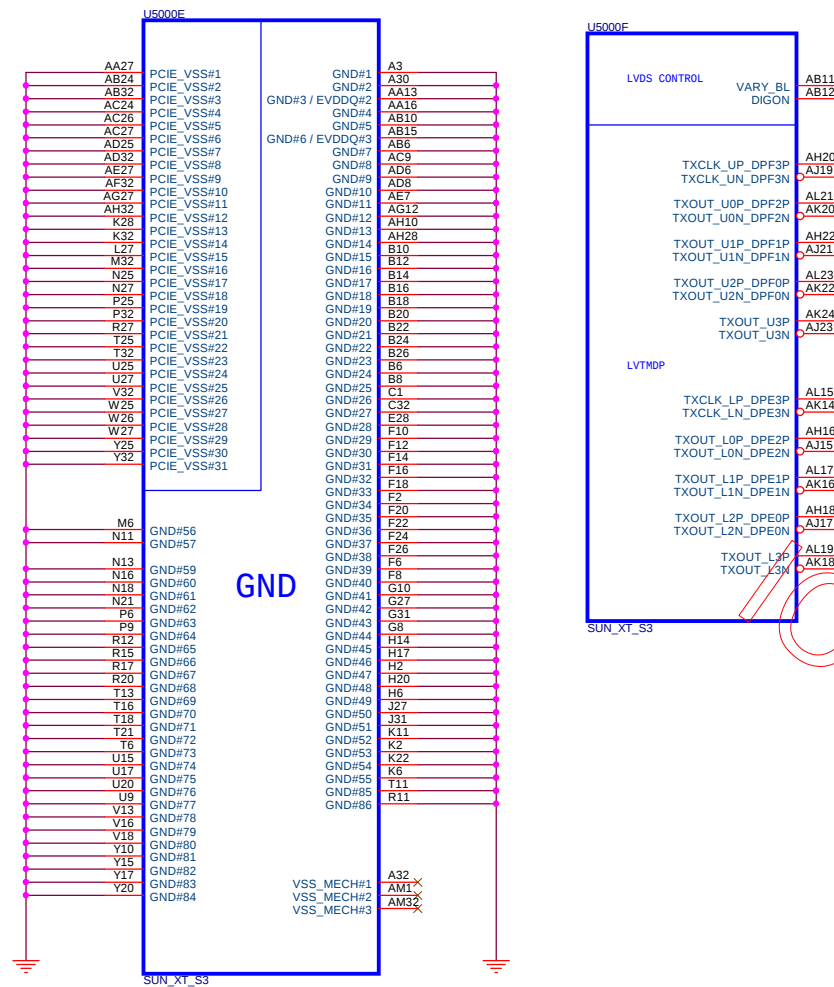
PWRCTL5	PWRCTL4	PWRCTL3	PWRCTL2	PWRCTL1	V-CORE
0	1	1	0	1	1.175V
0	1	1	1	0	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default



Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romiddg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romiddg[2:0] define memory aperture size If bios_rom_en = 1, romiddg[2:0] define ROM type	xxx	gpo_13 gpo_11
PS_0[4]	n/a	Reserved		genk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpo_2
PS_1[2]	bif_clk_pm_en	PCIe CLK PM capability: 1 = CLKREQ# supported	x	gpo_8
PS_1[3]	n/a	Reserved		genk_clk
PS_1[4]	tx_pwr_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpo_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpo_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpo_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpo_9
PS_3[1]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_cp[2]	>bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_cp[1]			
PS_3[5]	aud_port_cp[0]			





CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

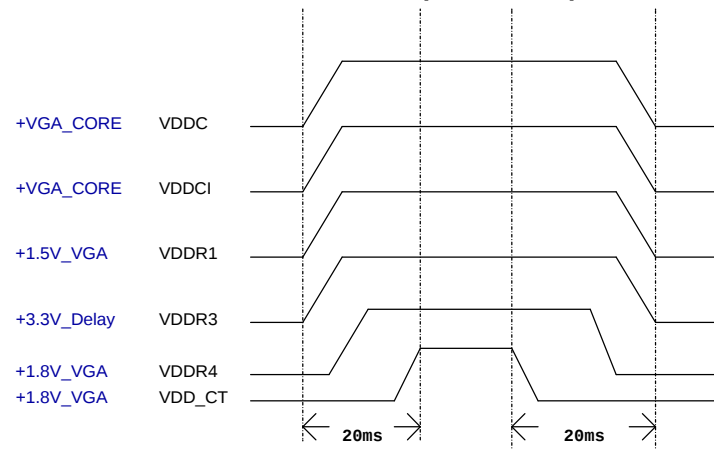
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 3K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

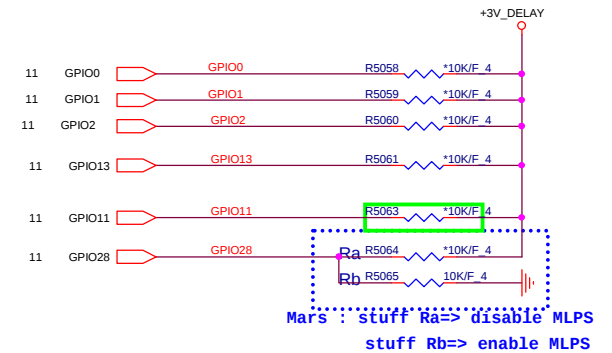
Power Up/Down Sequence



Memory Aperture size(Seymour)

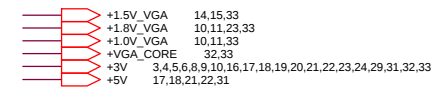
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

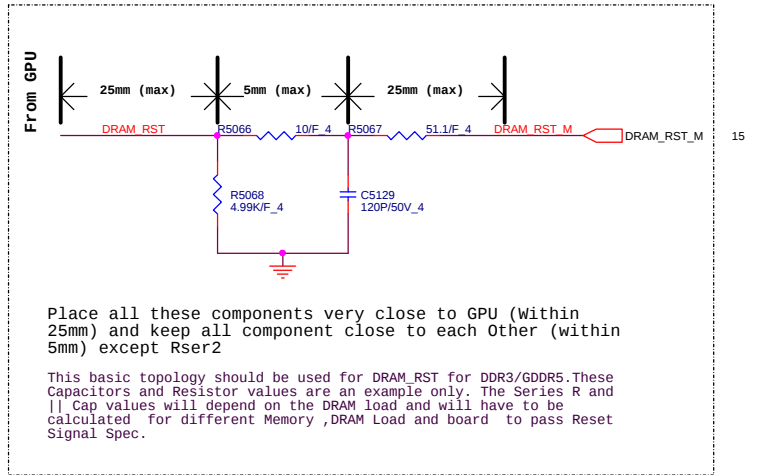
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



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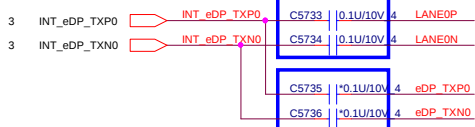
Size Custom	Document Number Sun S3 GND / LVDS/ Straps	Rev 1A
Date: Monday, May 19, 2014	Sheet 12 of 33	





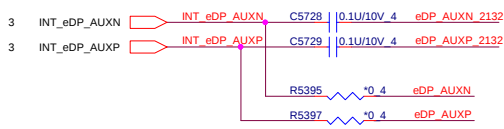
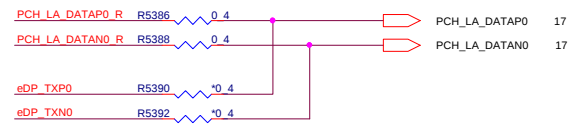


for Bemma LVDS need stuff 0.1u cap ; need change 0.1u on next stage



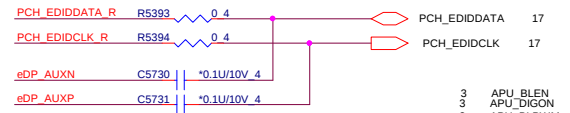
Bemba to LVDS Converter

From LVDS Converter



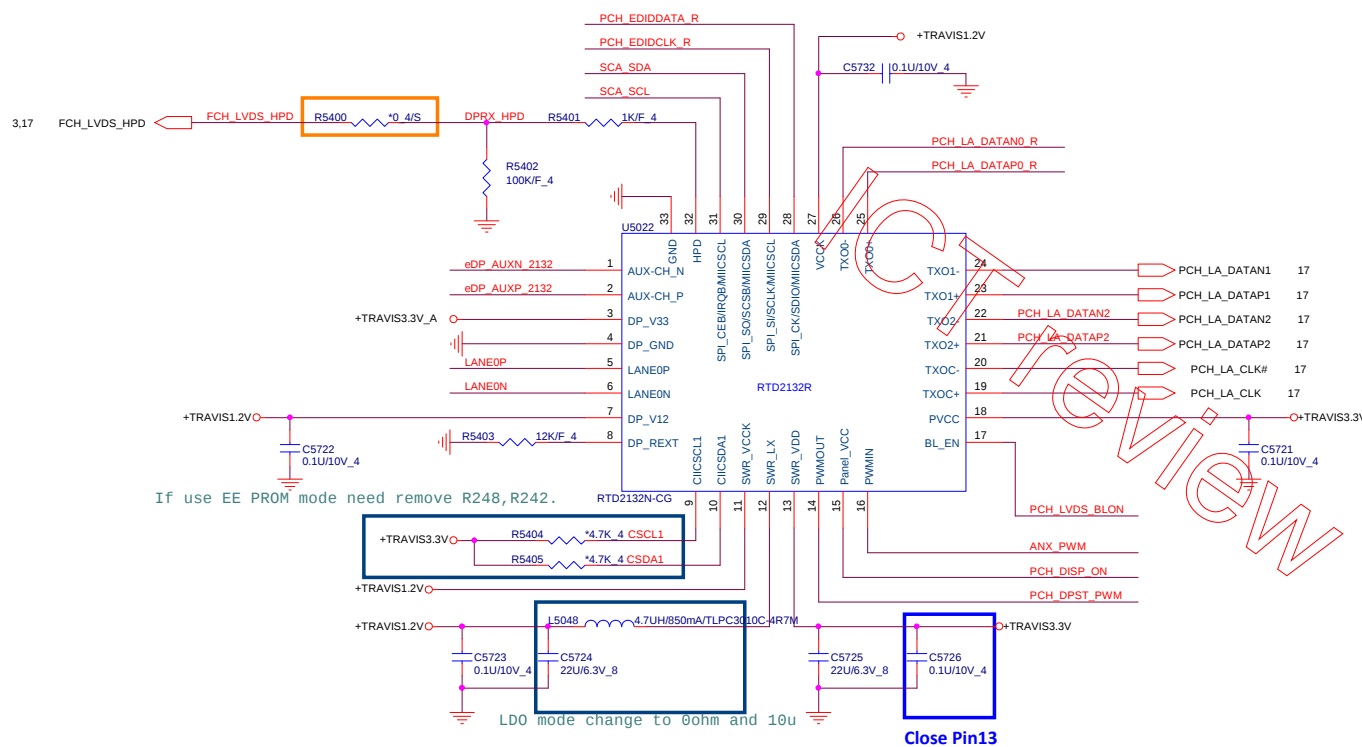
Bemba to LVDS Converter

From LVDS Converter

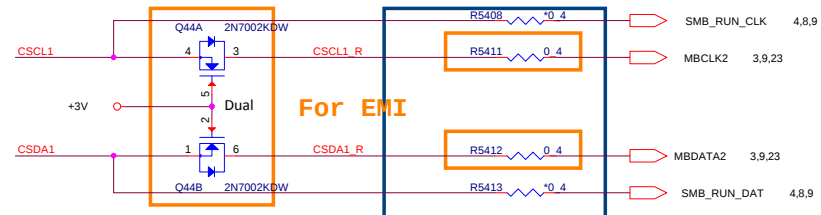
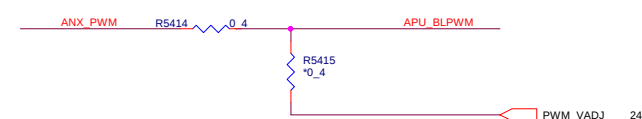
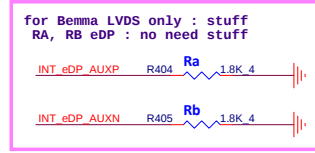
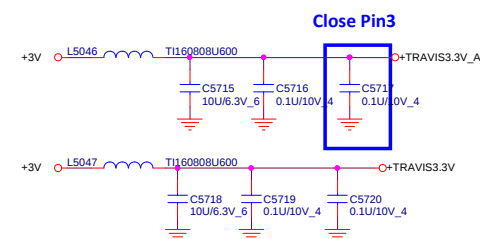


for Bemma eDP : stuff R5396 / R5398 / R5399

for Bemma LVDS : Don't stuff R5396 / R5398 / R5399

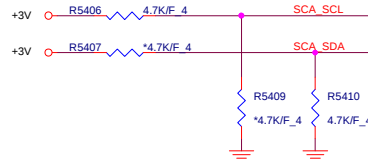


If use EE PROM mode need remove R248,R242.



EE PROM
EC OPTION

R5408, R5413
R5411, R5412



		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

PROJECT :U99
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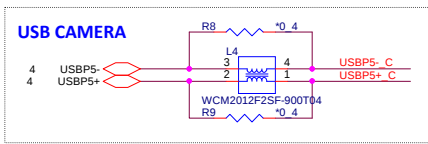
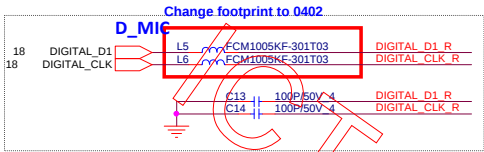
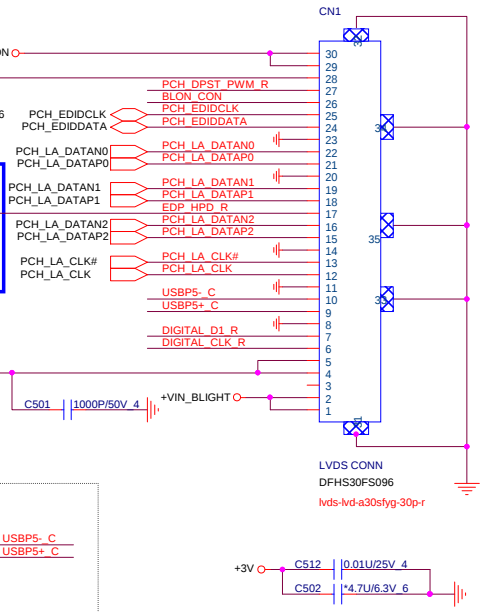
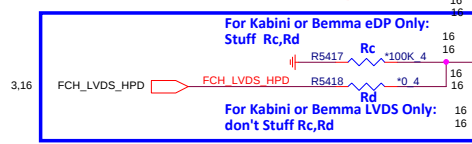
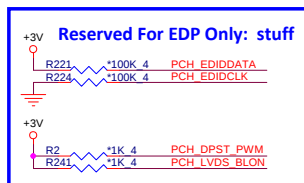
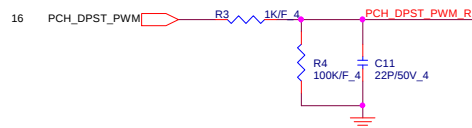
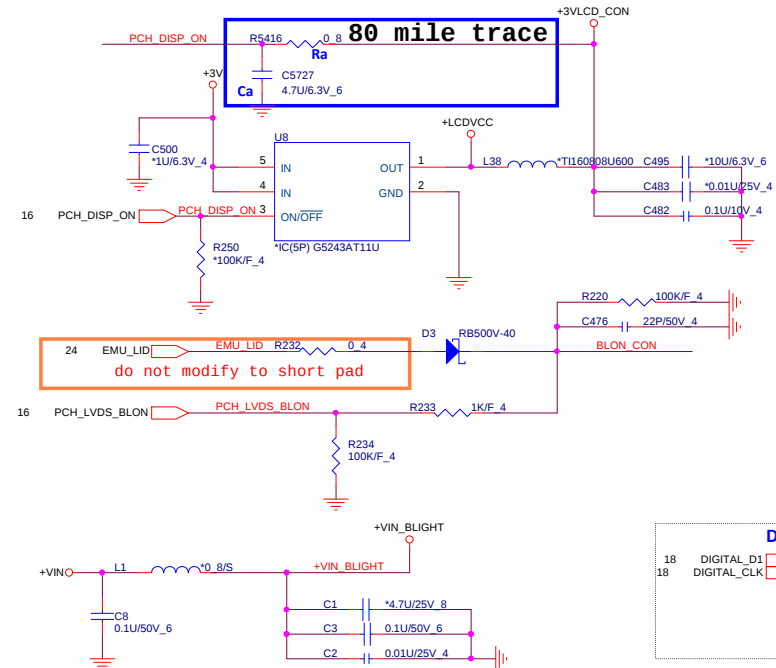
Size Custom Document Number
RTD21325

Date: Monday, May 19, 2014 Sheet 16 of 33

Rev 3A

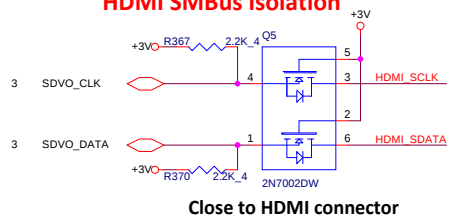
LVDS Conn.

for Bemma eDP : don't stuff Ra / Ca ;
for Bemma LVDS : stuff Ra / Ca ;

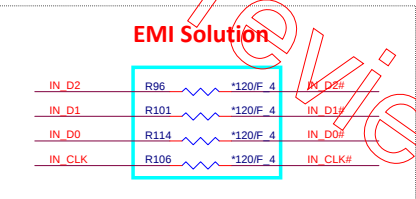


HDMI Conn.

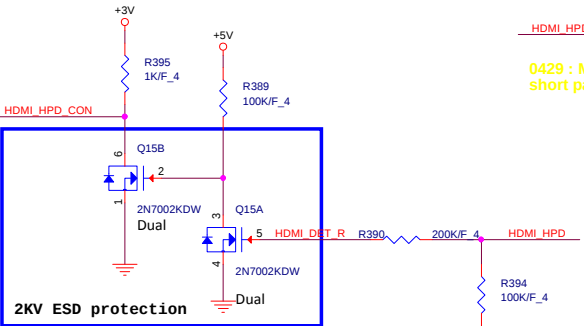
HDMI SMBus Isolation



Close to HDMI connector

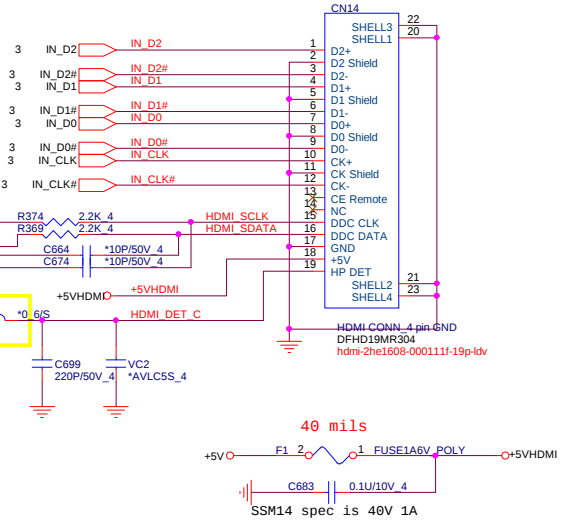


HDMI HPD SENSE



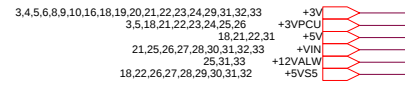
2KV ESD protection

0429 : MV modify to short pad

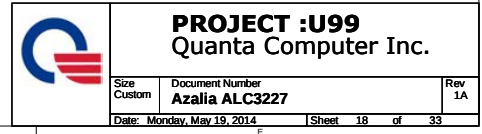


40 mils

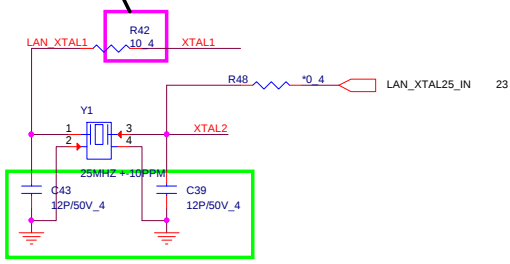
SSM14 spec is 40V 1A



PROJECT :U99 Quanta Computer Inc.			
Size	Document Number	Rev	
Custom	LCD Connector (LVDS)	3A	
Date:	Monday, May 19, 2014	Sheet	17 of 33



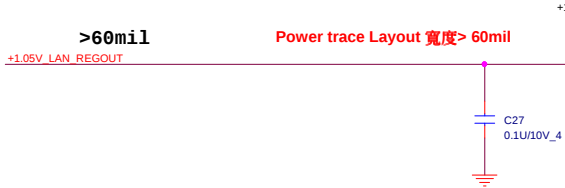
For EMI $\theta \sim 22 \text{ ohm}$



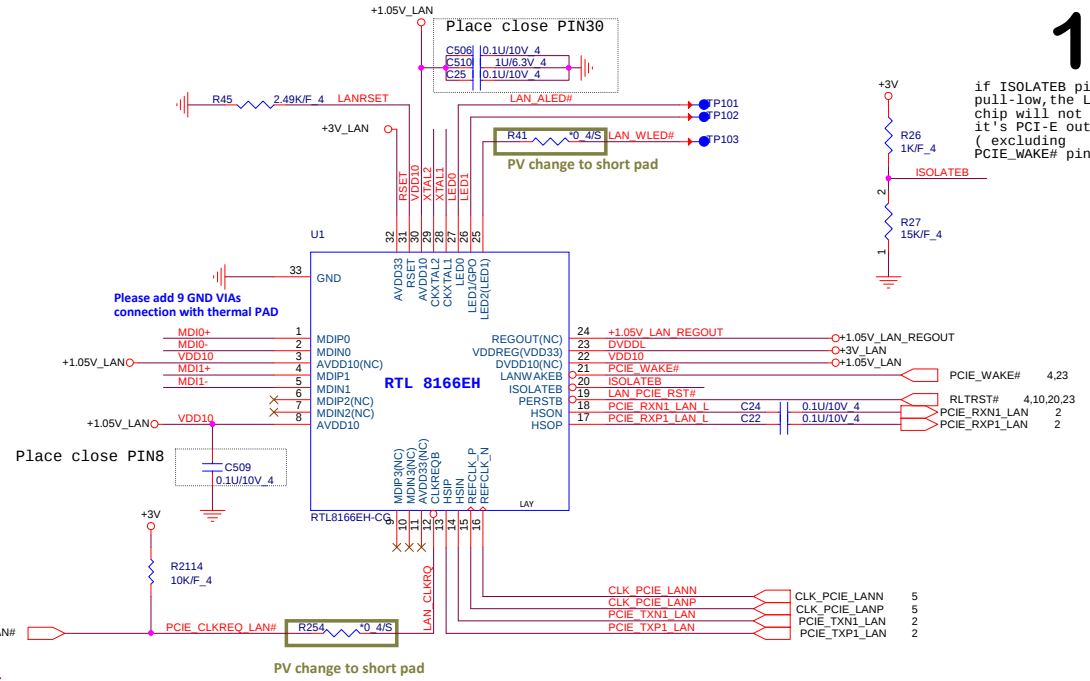
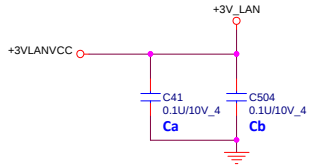
SI change to 12p

>60mil

Power trace Layout 宽度 > 60mil

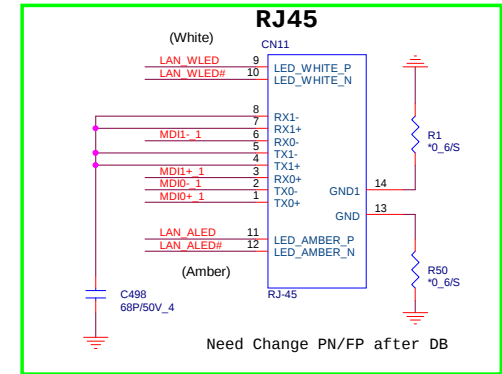


Place close PIN23 and PIN32



if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIe_WAKE# pin)

LAN conn

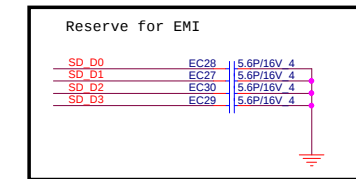


3,4,5,6,8,9,10,16,17,18,20,21,22,23,24,29,31,32,33
23.31

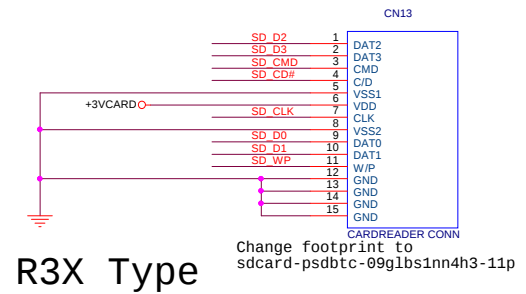
+3V
+3VLANVCC

SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS

Share Pin

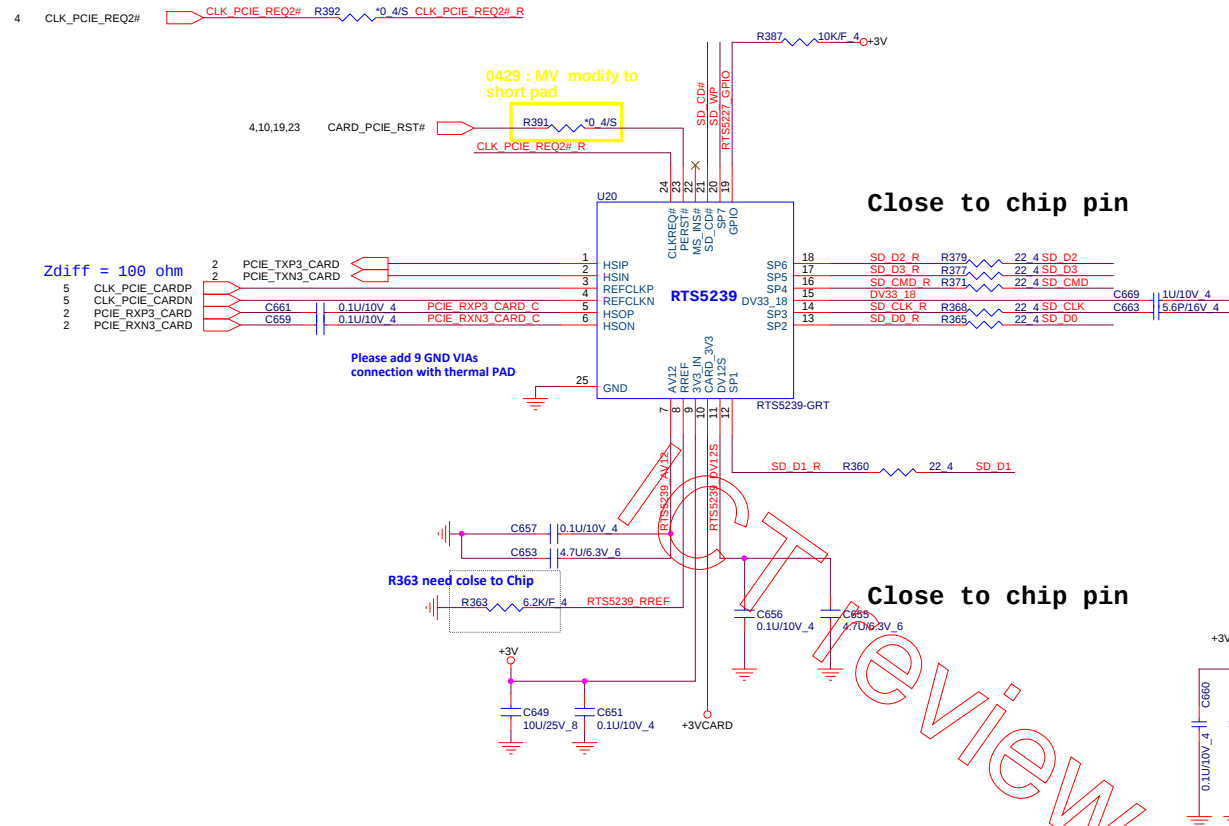


**SD / MMC
CARD READER**



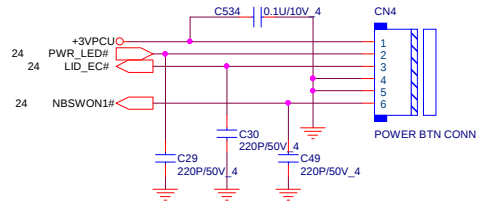
R3X Type

Change footprint to
sdcard-psdbtc-09glbs1nn4h3-11p

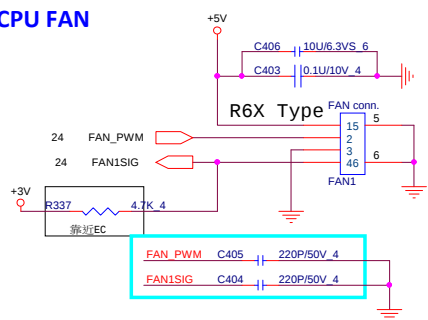


Power Button Connector

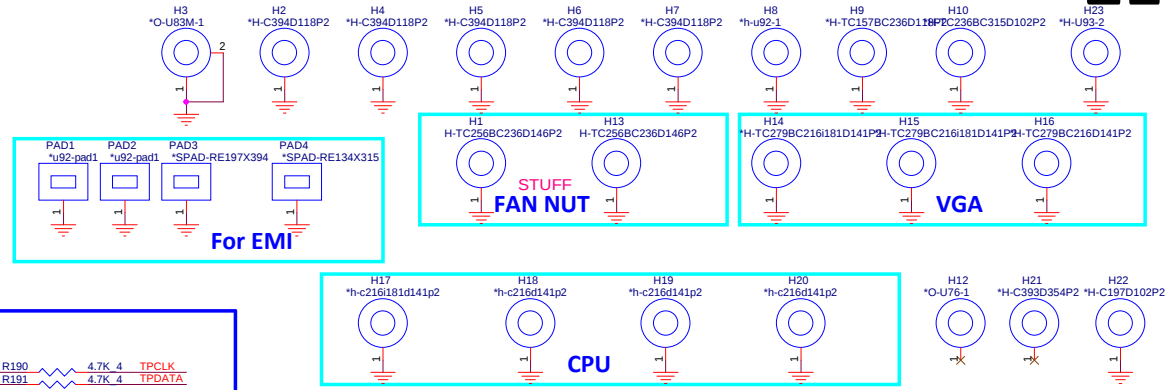
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



CPU FAN

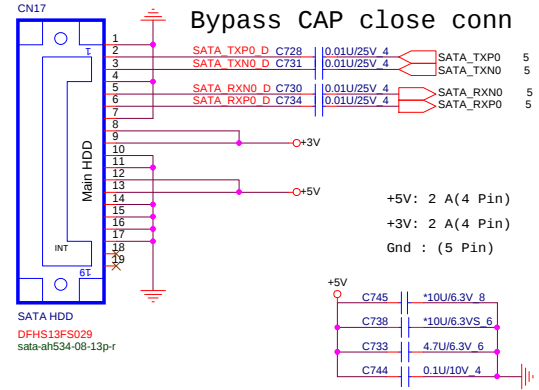


Hole

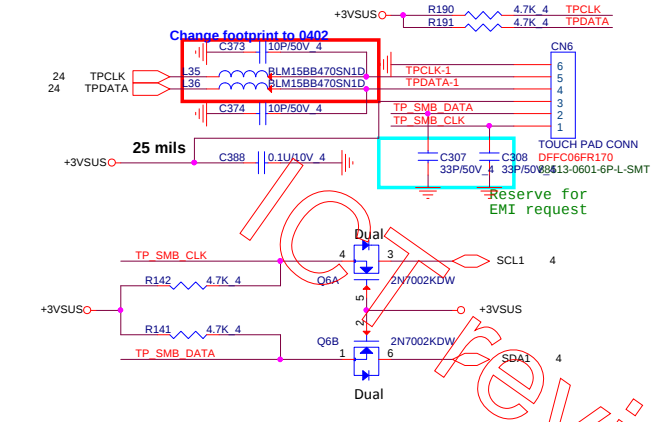


SATA HDD Connector(Cable type)

Bypass CAP close conn

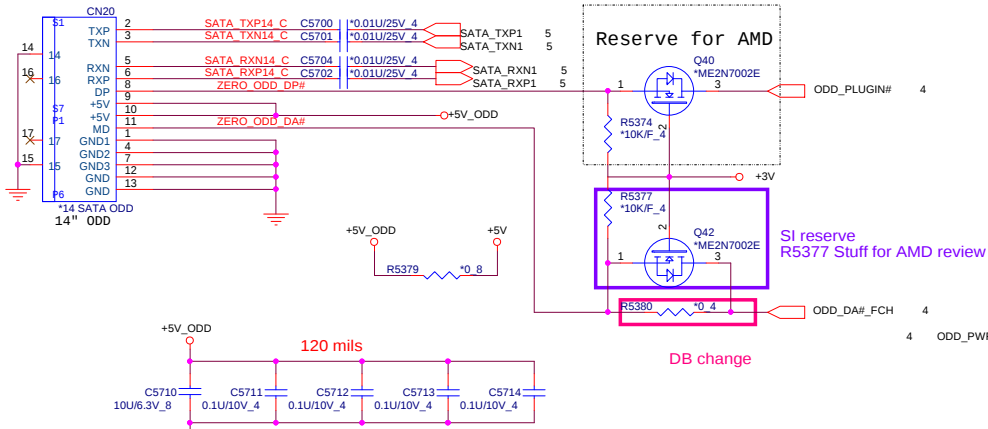


Touch Pad



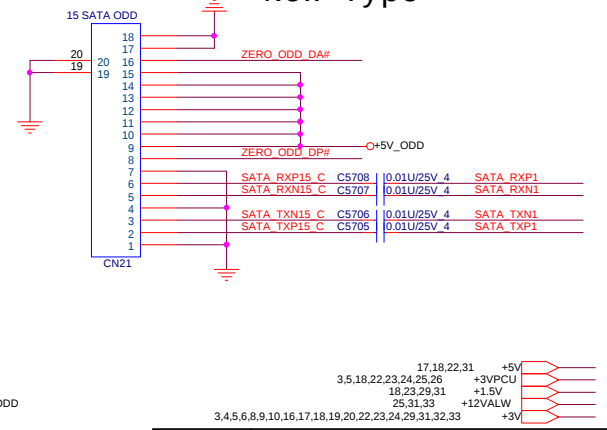
SATA ODD CONNECTOR

14" SATA ODD Bypass CAP close conn

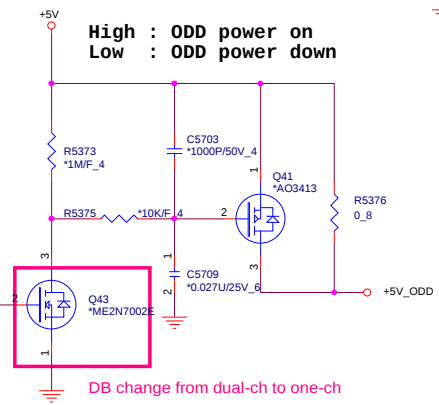


15" SATA ODD

New Type

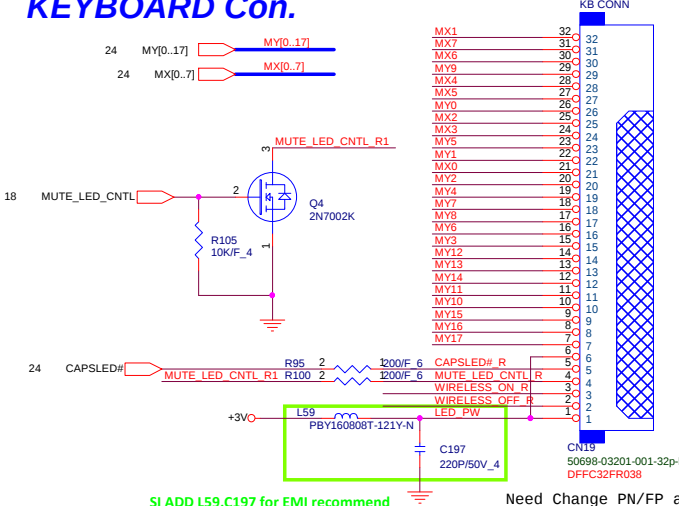


High : ODD power on
Low : ODD power down

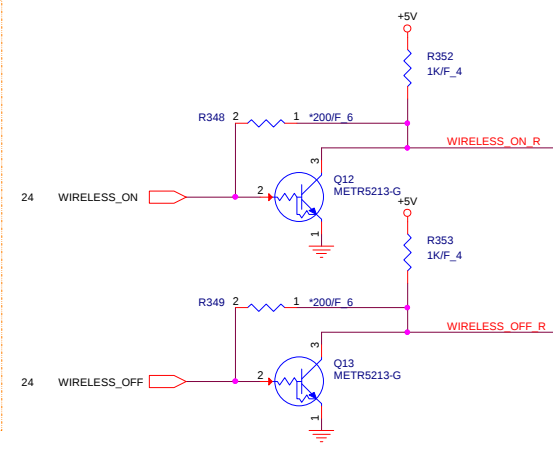
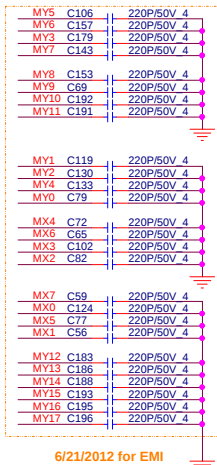
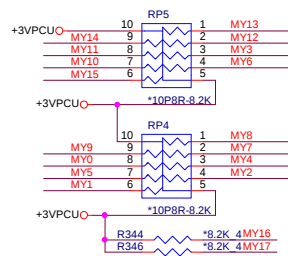


KEYBOARD Con.

22



KEYBOARD PULL-UP

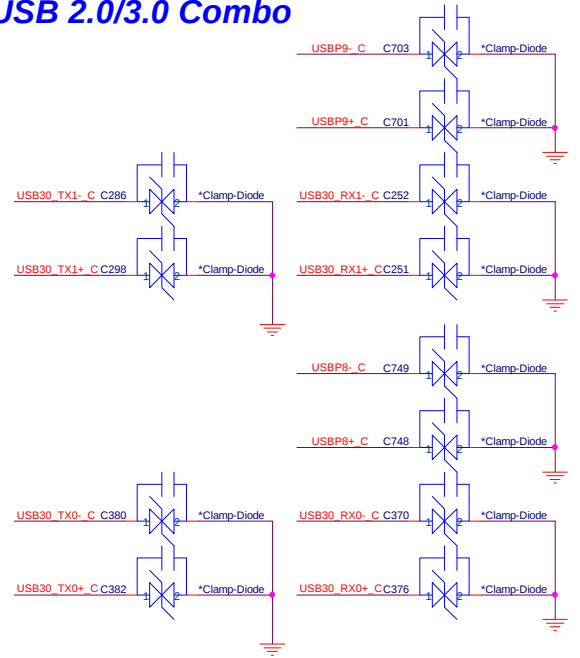


SI ADD L59,C197 for EMI recommend

Need Change PN/FP after DB

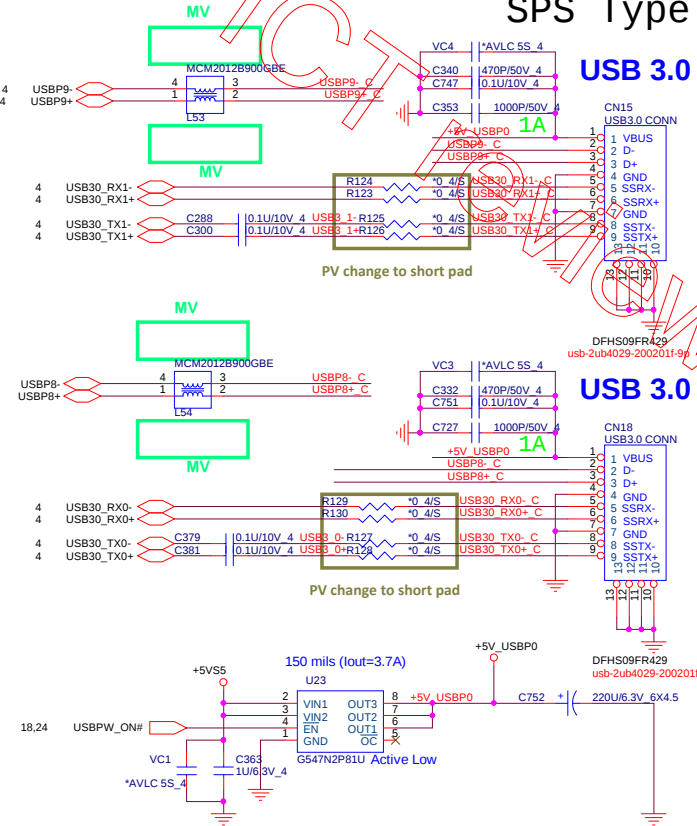
NM9 Type

USB 2.0/3.0 Combo

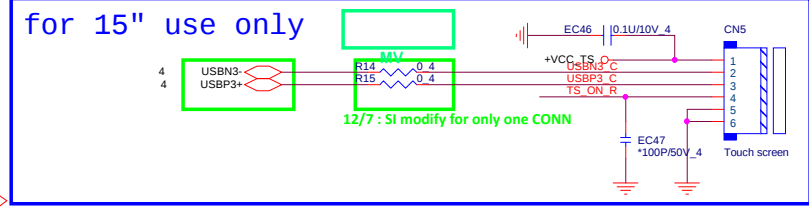


SPS Type

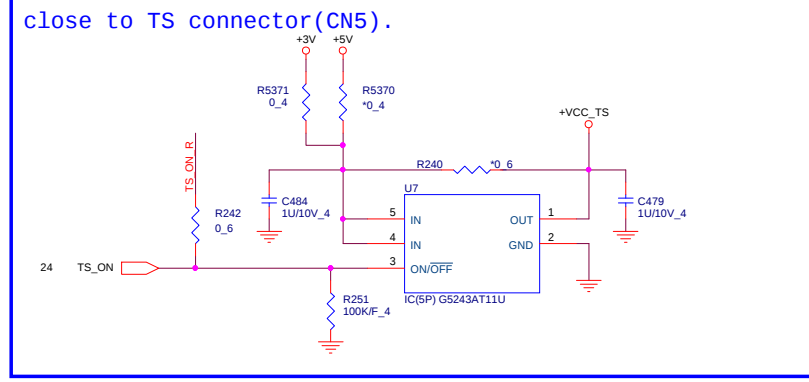
USB 3.0



for 15" use only



close to TS connector (CN5).



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Quanta Computer Inc.

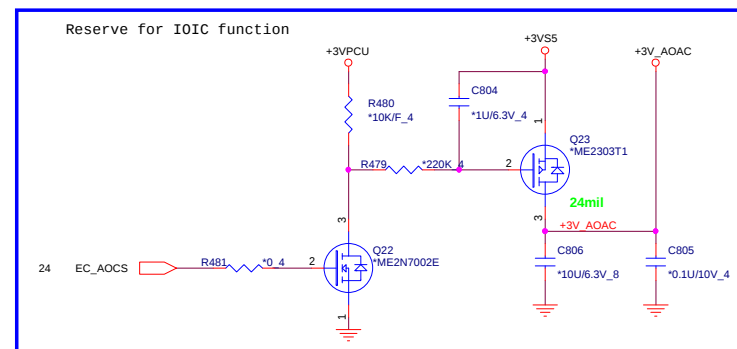
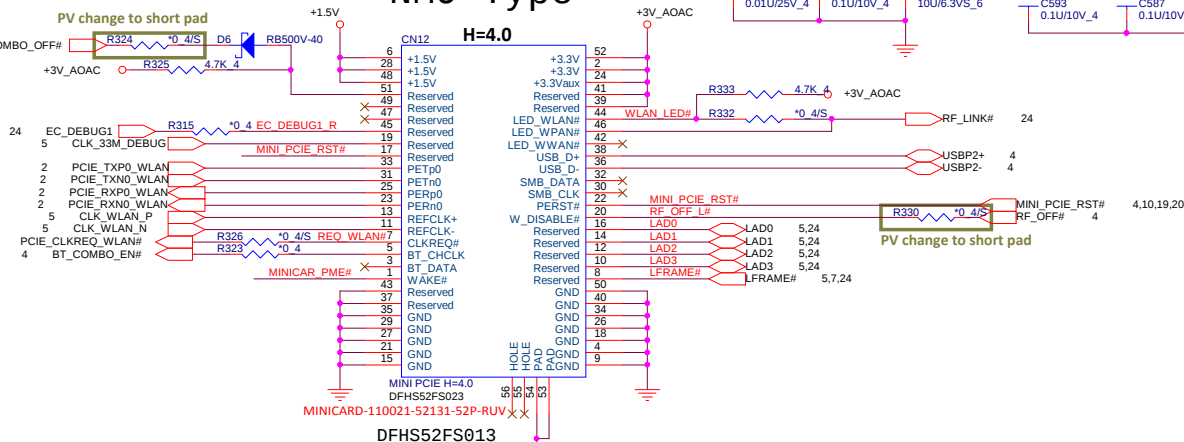
Size	Document Number	Rev
Custom	USB 3.0/KB/Green CLK	1A
Date: Monday, May 19, 2014	Sheet 22of	33

18,26,27,28,29,30,31,32
3,5,18,21,23,24,25,26

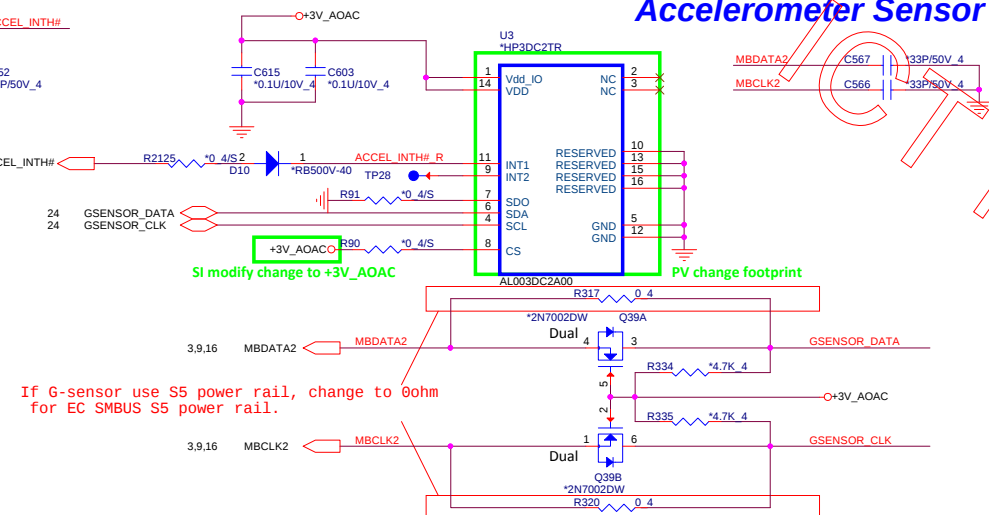
+5VS5
+3VPCU

**Mini Card
WLAN/BT(Optional)**

NM9 Type

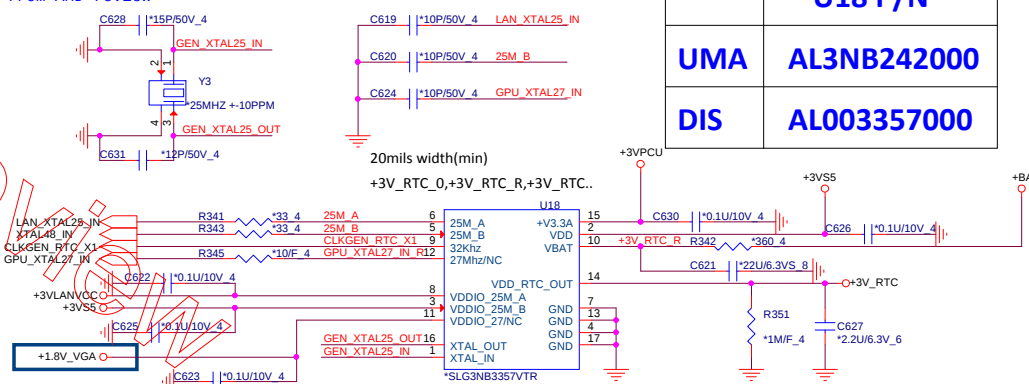


Accelerometer Sensor



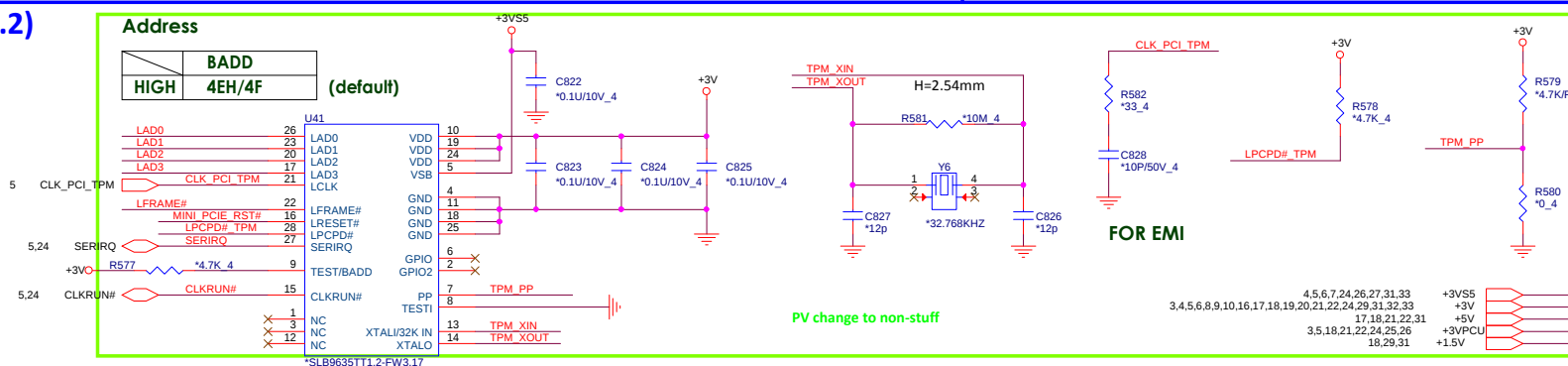
Green CLK Circuitry

Modify from AMD review



	U18 P/N
UMA	AL3NB242000
DIS	AL003357000

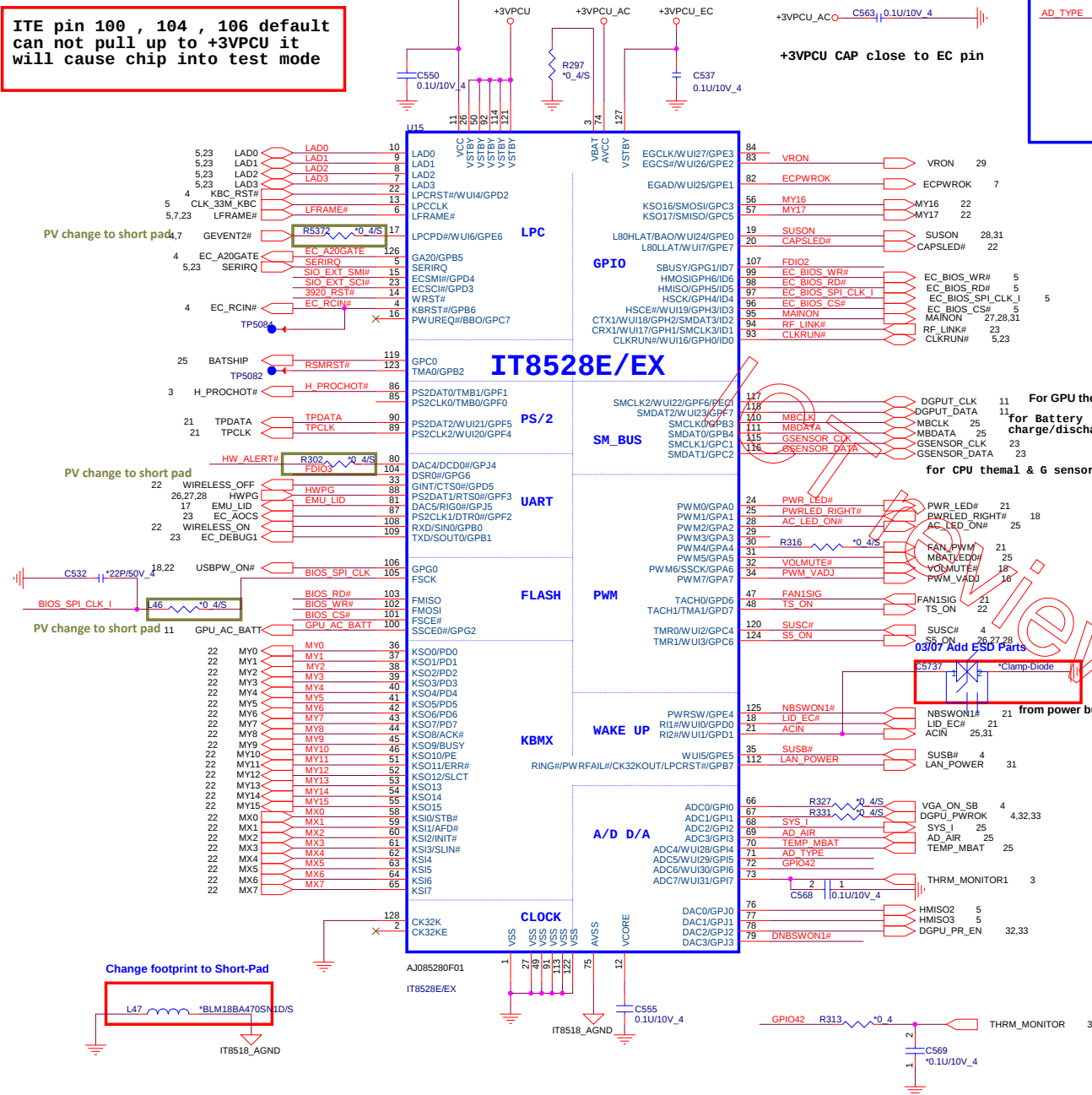
TPM (1.2)



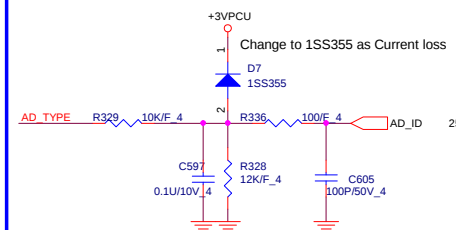
PROJECT :U99
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Size Custom	Document Number MINI-PCIE/LED	Rev 1A
Date: Monday, May 19, 2014	Sheet 23 of	33

ITE pin 100 , 104 , 106 default
can not pull up to +3VPCU it
will cause chip into test mode



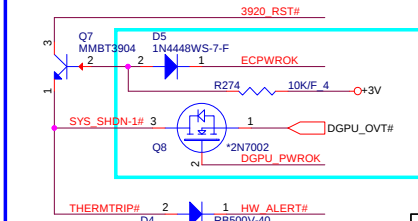
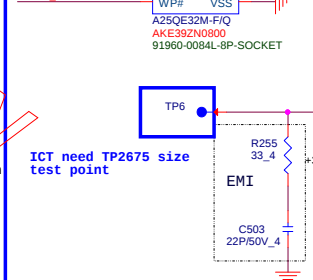
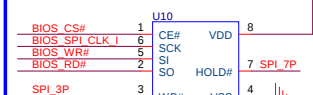
Smart adapter Type check



Timing diagram for +VIN noise. The diagram shows three signals: HWPG, FAN1SIG, and DGPU_PR_EN. Each signal is represented by a horizontal line with a vertical pulse. The scale for each signal is 0.1u/10V_4. The signals are labeled C549, C600, and C539 respectively. The diagram is titled "For +VIN noise".

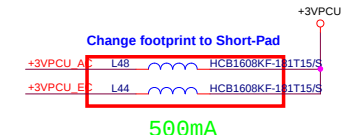
Vender	Size	P/N
AIT	4M	AKE39ZN0800
EON	4M	AKE39ZN0Q03
WND	4M	AKE39FN0N01
Socket		DFHS08FS023

4M SPI EC ROM

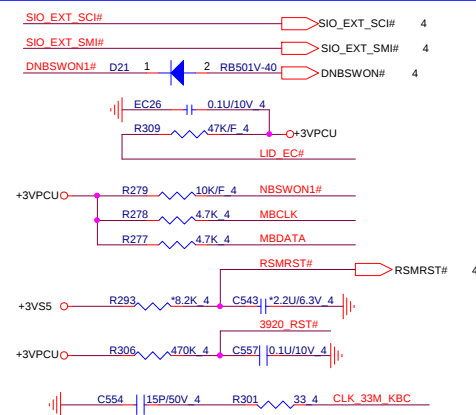
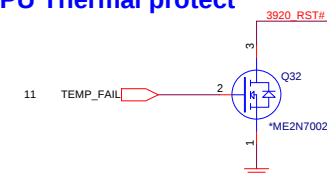


ADD VGA TEMP_FAIL function is active Hi

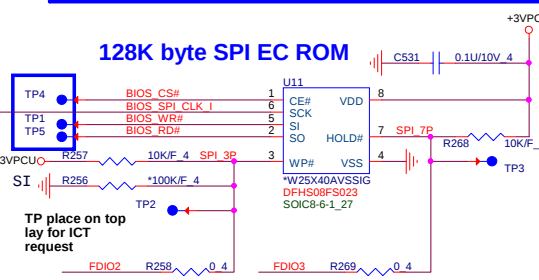
Change footprint to Short-Pad



DGPU Thermal protect



128K byte SPI EC ROM



Adapter select

+3VPCU R319 10K/F 4 GPIO42 R318 *10K/F 4

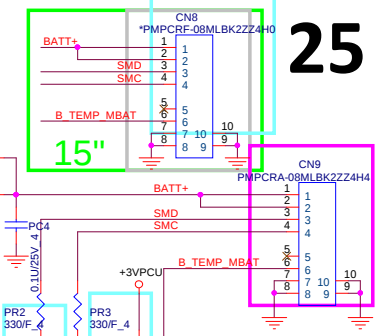
Hi ==> A6-5200 25W CPU + DIS
Low ==>UMA/DIS/SG

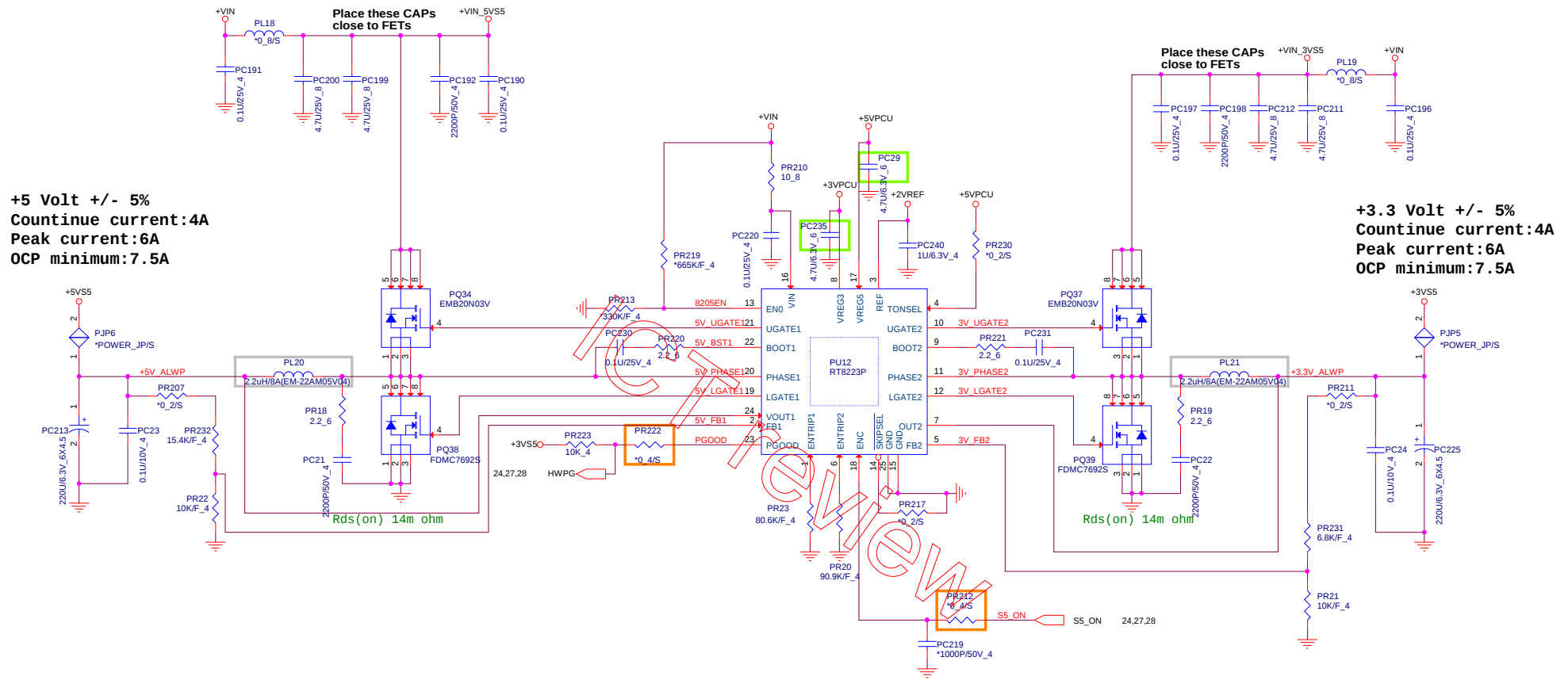
Platform model	GPI042	adapter
A6 25W CPU + DIS	High	90W
DIS/SG/UMA	Low	65W

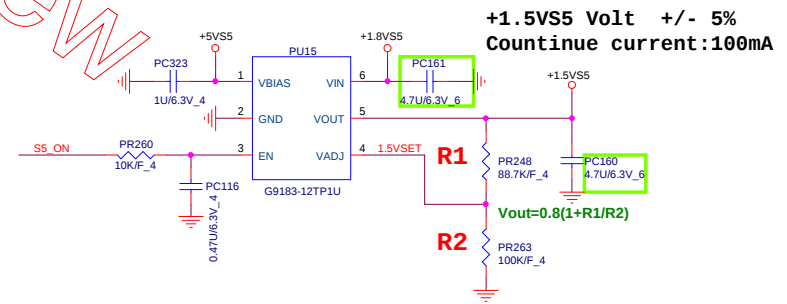
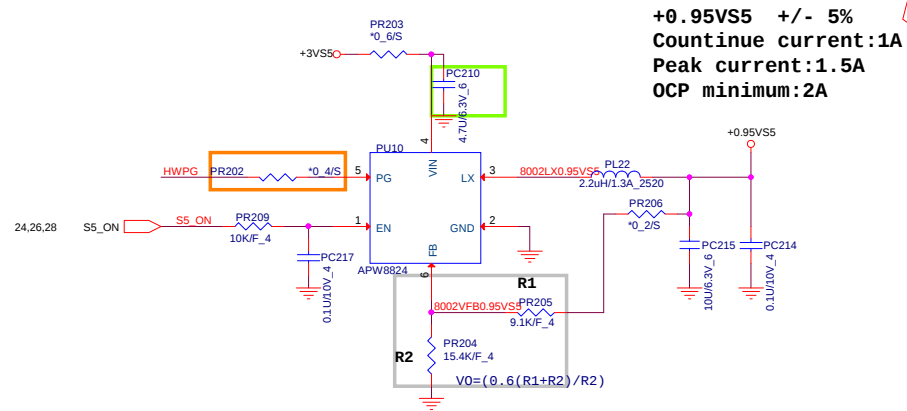
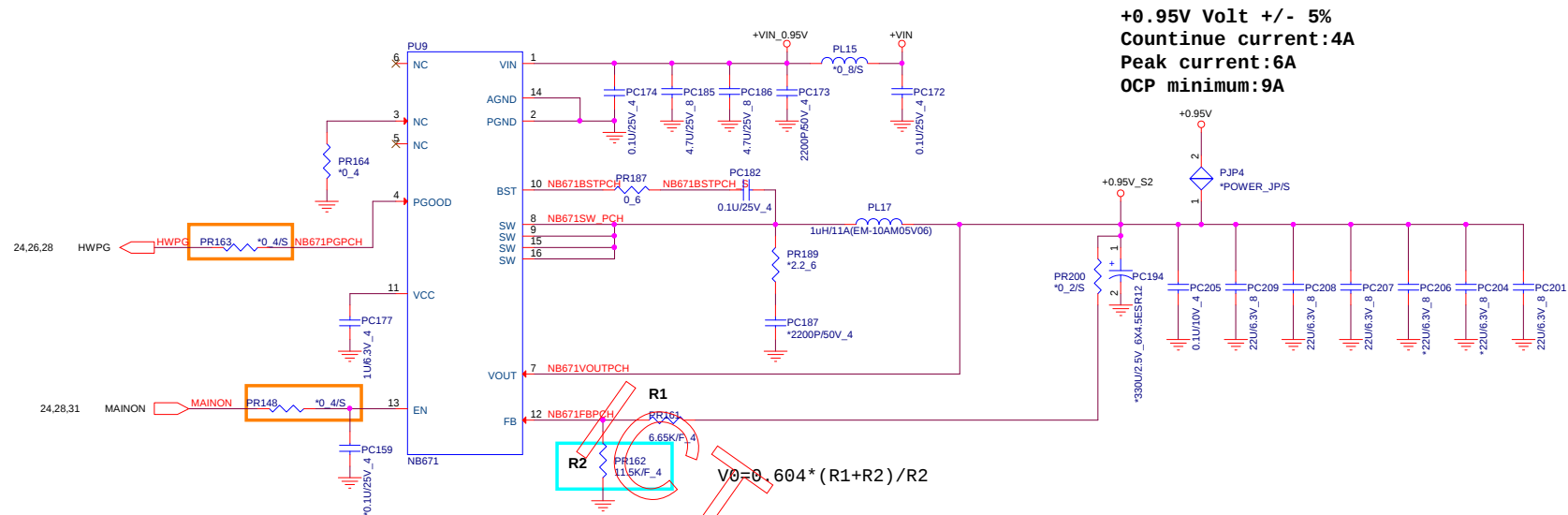


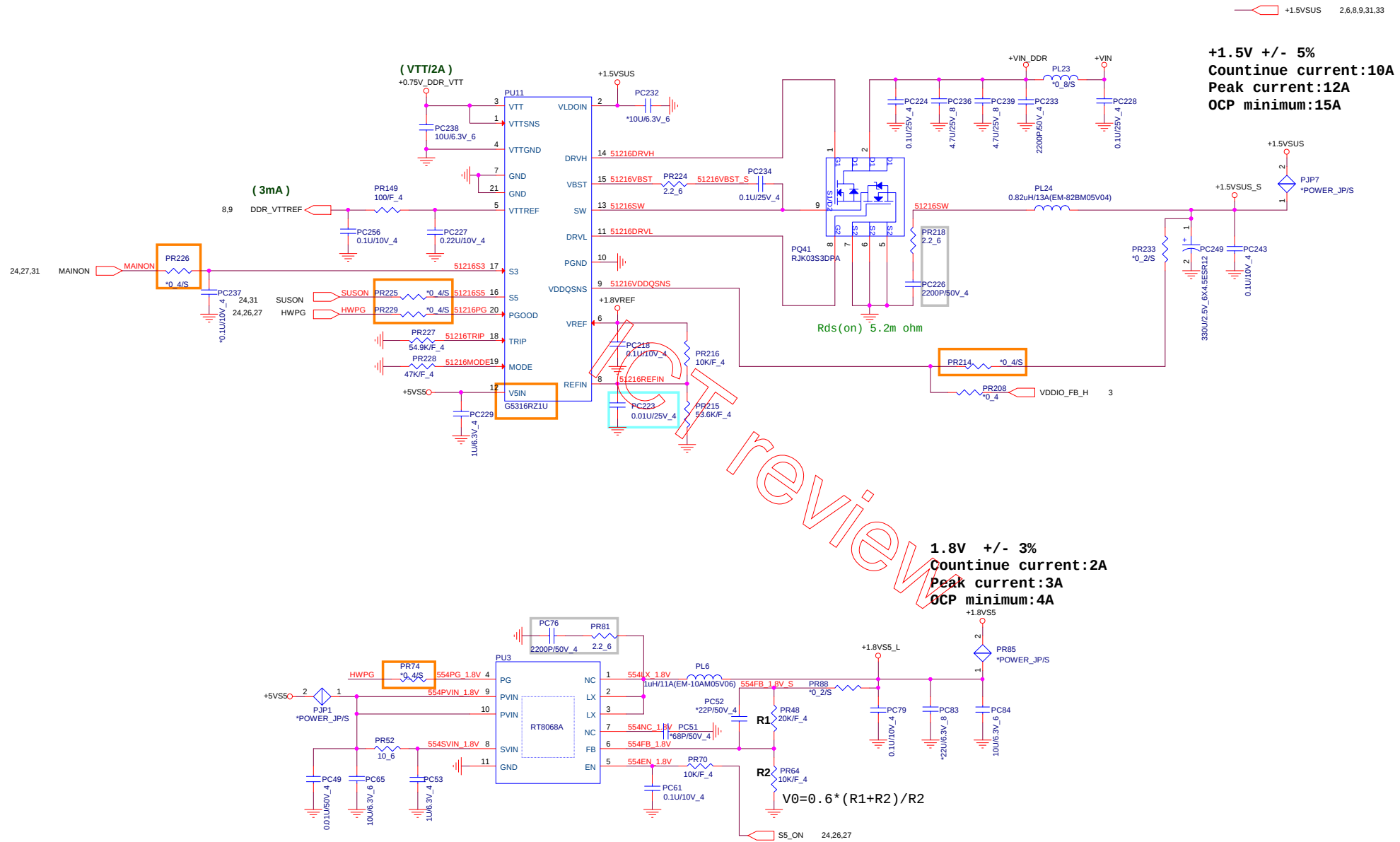
PROJECT :U99
Quanta Computer Inc.

Size Custom	Document Number EC (IT8528E)/ROM	Rev 1A
Date: Monday, May 19, 2014		Sheet 24 of 33



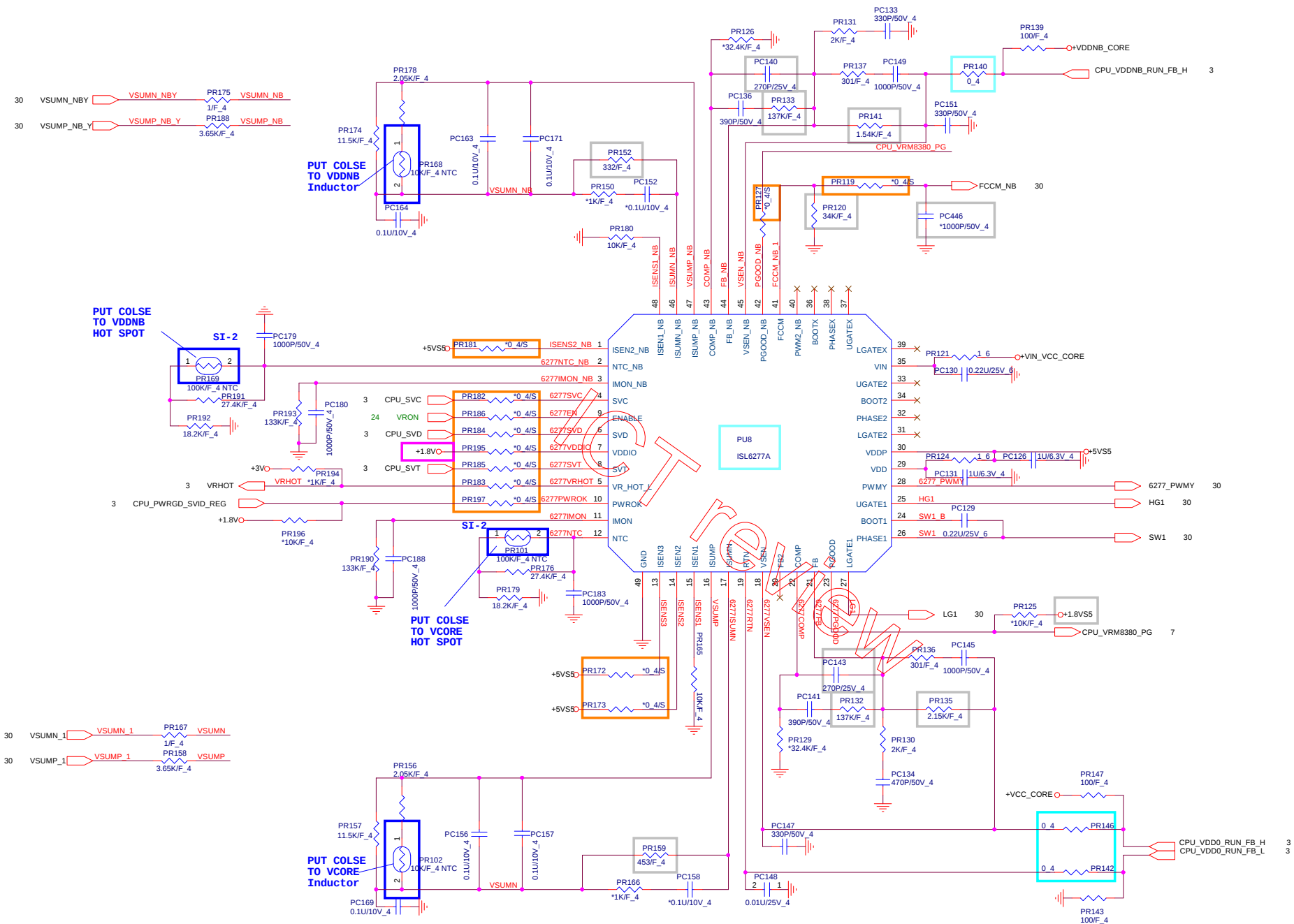


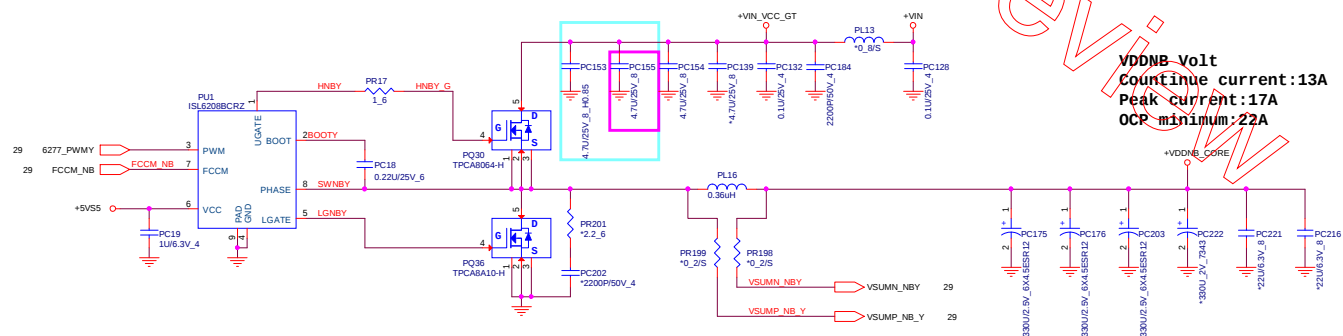
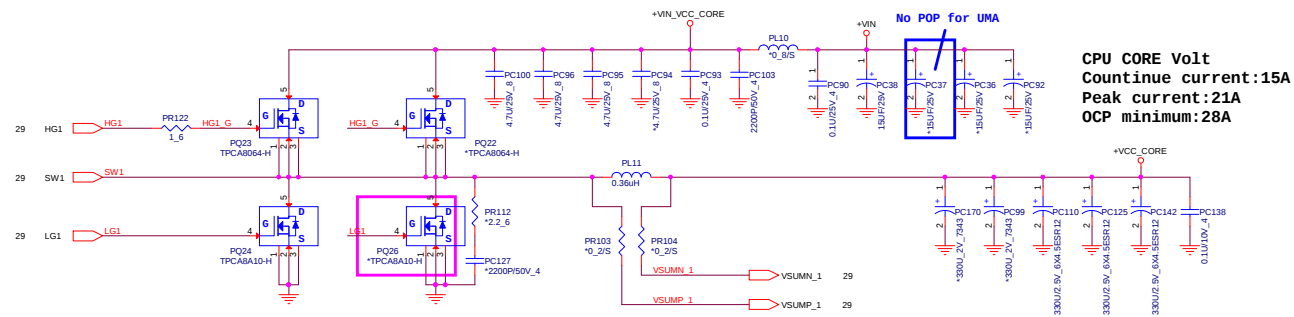




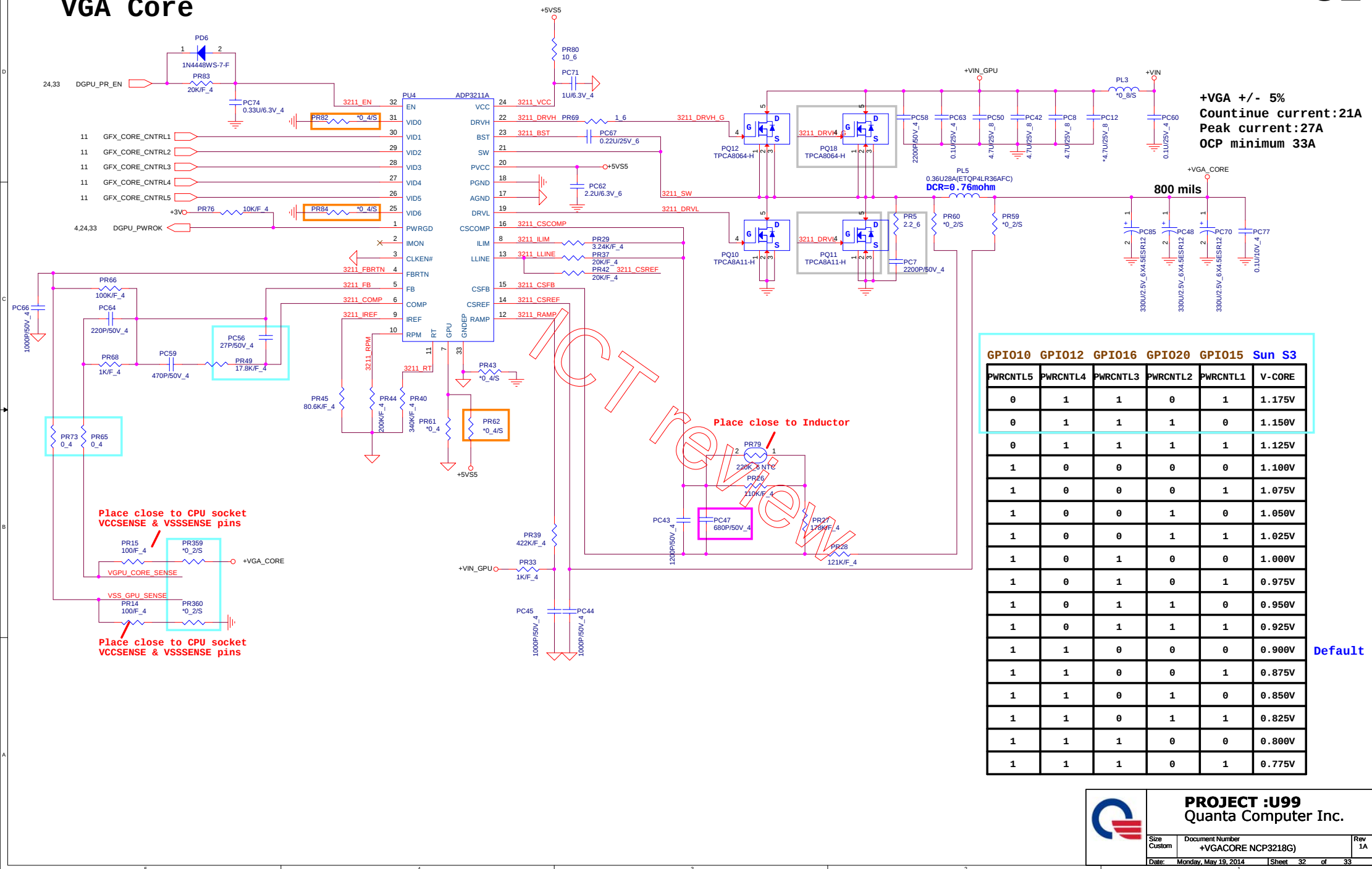
PROJECT :U99
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (TP551216)	1A
Date: Monday, May 19, 2014	Sheet 28 of 33	

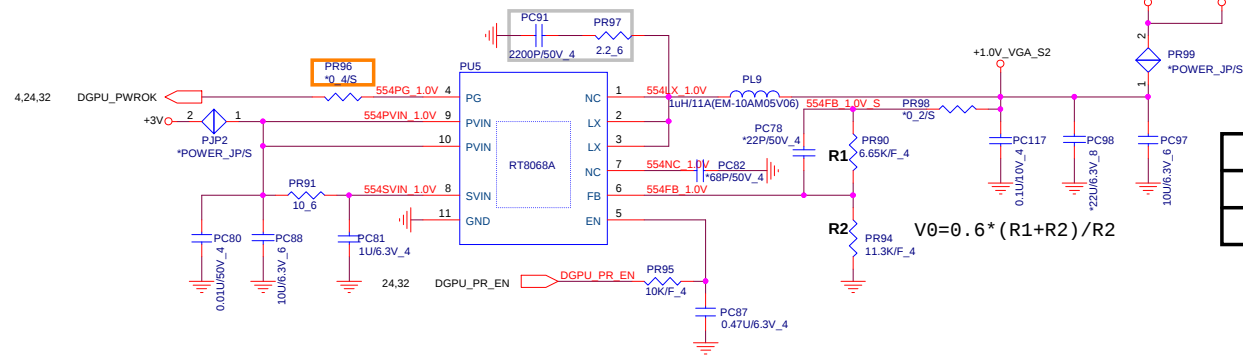




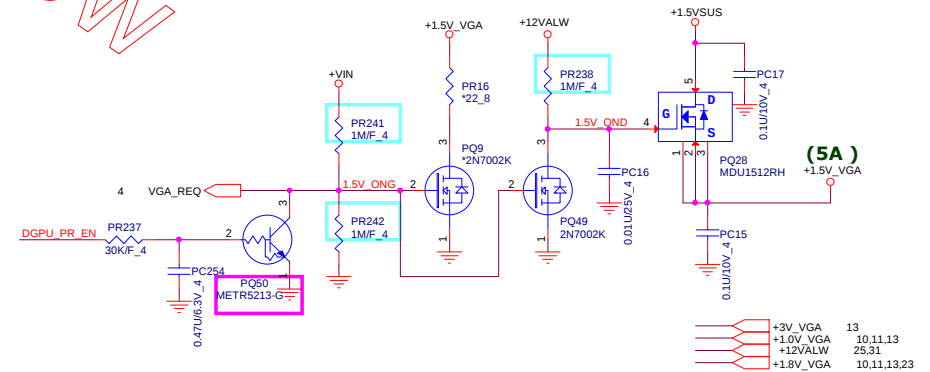
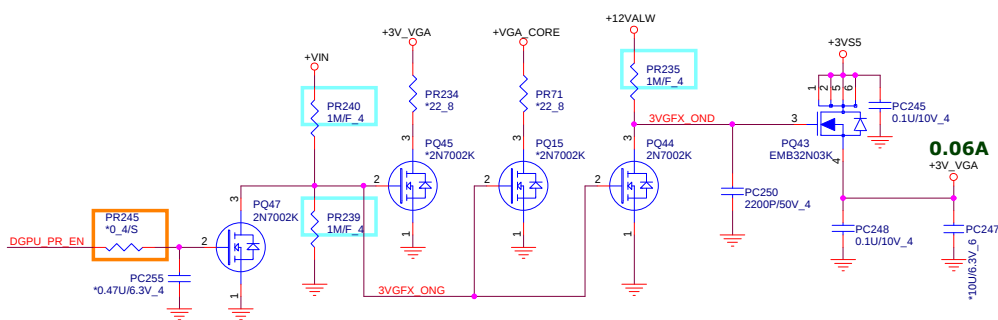
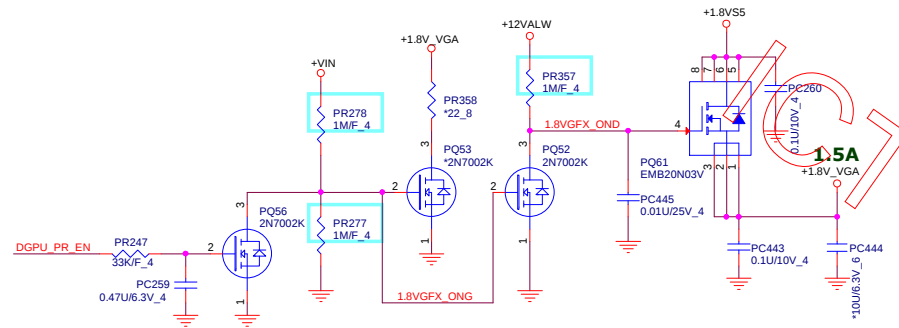
VGA Core



+0.95V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A



R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V



+3V_VGA 13
 +1.0V_VGA 10,11,13
 +12V_VGA 25,31
 +1.8V_VGA 10,11,13,23



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Size	Document Number	Rev
Custom	+VGA POWER	1A
Date: Monday, May 19, 2014	Sheet 33 of 33	