R7X AMD SYSTEM DIAGRAM

01

+3V/+5V S5 PG.35
+1.1VS5/+2.5V PG.36
+1.2V PG.37
CPU Core PG.38~39
DDR3L PG.40
Charge PG.34
Dis-Charge PG.41
+VGACORE PG.42
+1.5 VGA PG.43
+1.0V/+1.8/ +3 VGA PG.44

SODIMM1 Max. 4GB PG.12 — 1600MT/s DDR3 L Channel A
SODIMM2 Max. 4GB PG.13 — 1600MT/s DDR3 L Channel B

AMD
35mm X 35mm
RICHLAND 722 pin uPGA
TDP 35W
PG.2~5

PCI-E x8 → AMD Sun XT 29mm X 29mm 64bit M2 package 25W PG.13~19
DDR3 900MHz → VRAM 128Mx16x4 or 256Mx16x4 1GHz PG.20~21

DP0 → eDP (5.4Gb/s) → eDP PG.23
DP2 → DDI (5.4Gb/s) → REALTEK 2136R DP to LVDS Converter PAGE 22 → LVDS Interface → LVDS PG.23
DP Port B → HDMI PG.25
DP1 → CRT → CRT PG.24

DP / UMI

AMD FCH BOLTON M3
24.5mm X 24.5mm
656pin FCBGA
TDP 4.7W
PG.6~10

PCI-E x 1
HDD PG.31 — SATA0
ODD PG.31 — SATA1

LANE1
LAN RTL8166EH 10/100 PG.29 — LANE0
WLAN BT COMBO PG.32 — USB 2.0 PORT8

PCI-E x 1 — LANE3
Accelerometer PG.32 — SMBUS
Card Reader RTS5239 PG.26

KBC ITE8528 PG.33 — LPC
KB PG.30 | TP PG.30 | ROM PG.33 | FAN PG.31

TPM SLB9635 (option) PG.25

AUDIO CODEC ALC3227-CG PG.27
Speaker PG.27
COMBO JACK HP/MIC PG.28
DIGITAL MIC PG.23

USB 3.0 PORT1, 2 → USB3.0 Ports X2 PG.28 (PORT11, 12)
Webcam PG.23 (PORT2)
USB 2.0 PORT0 → USB2.0 Ports PG.29
PORT3 → Touch Screen (option) PG.26

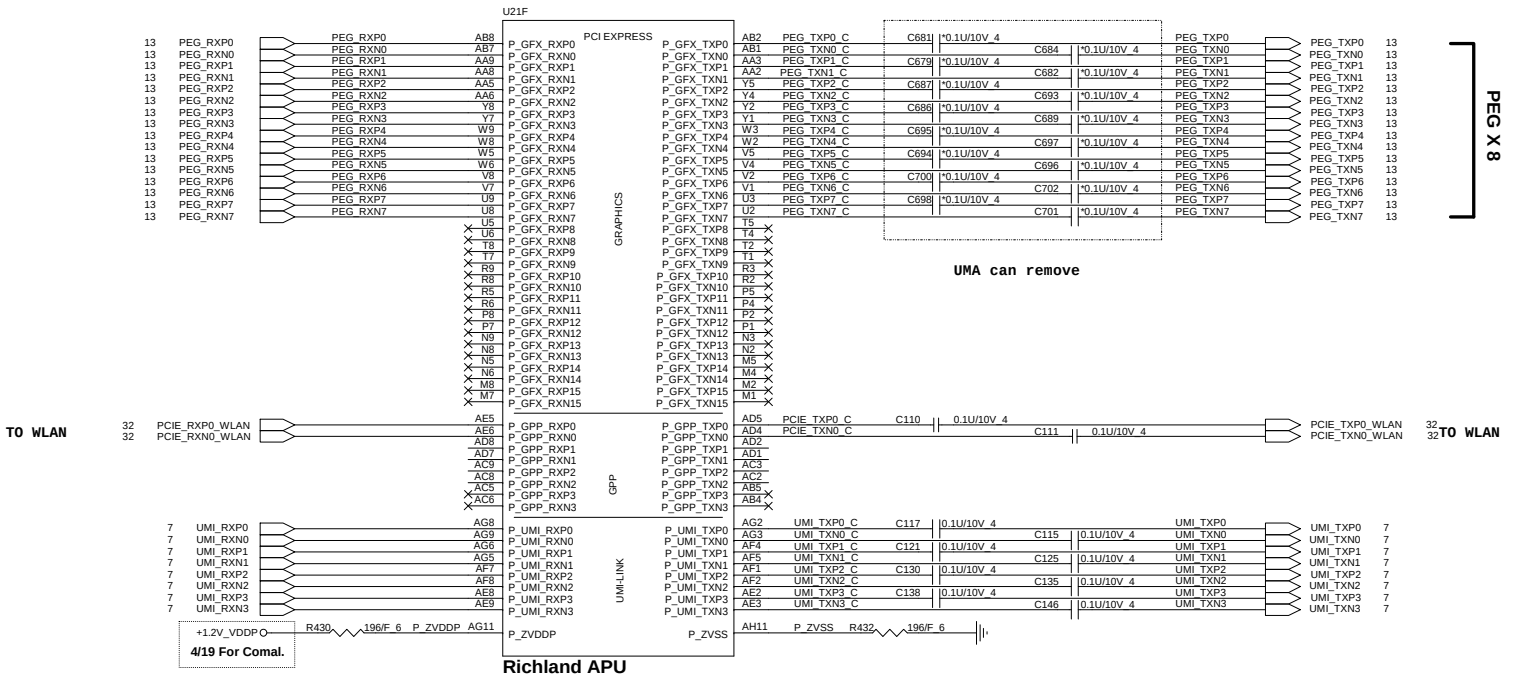
Stackup
TOP
GND
IN1
IN2
VCC
BOT

NB5

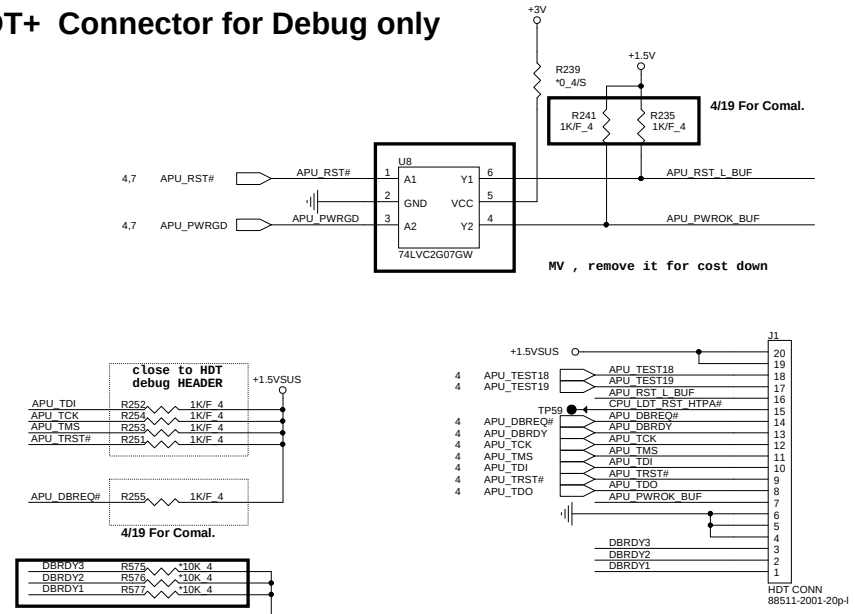
PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Tuesday, March 12, 2013 Sheet 1 of 43

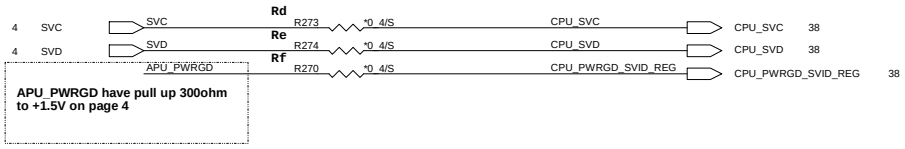


HDT+ Connector for Debug only

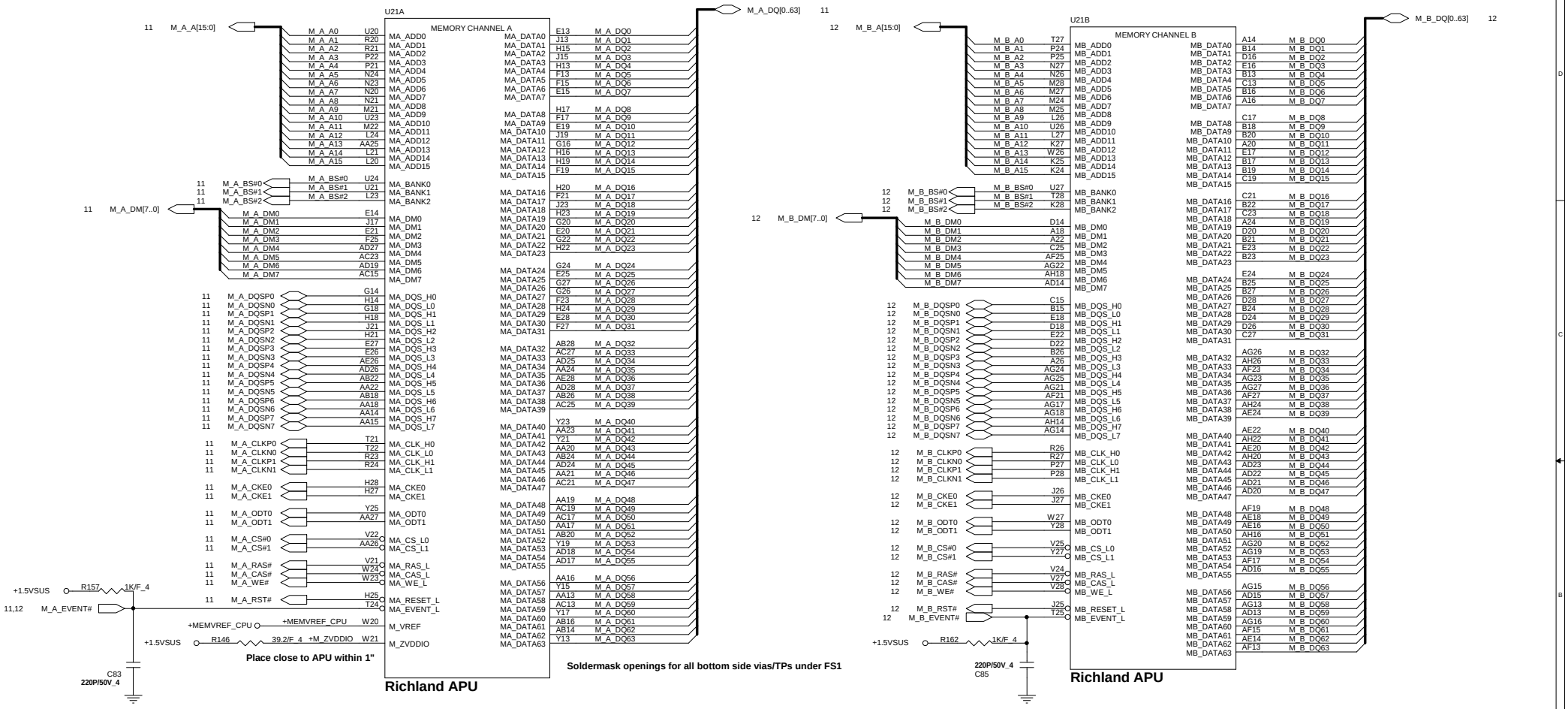


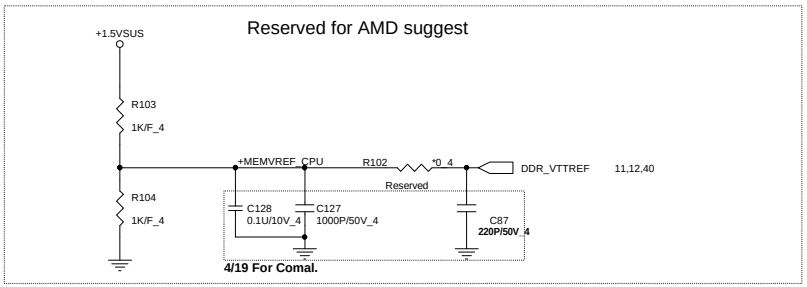
VID Override Circuit

		BOOT VOLTAGE	
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8



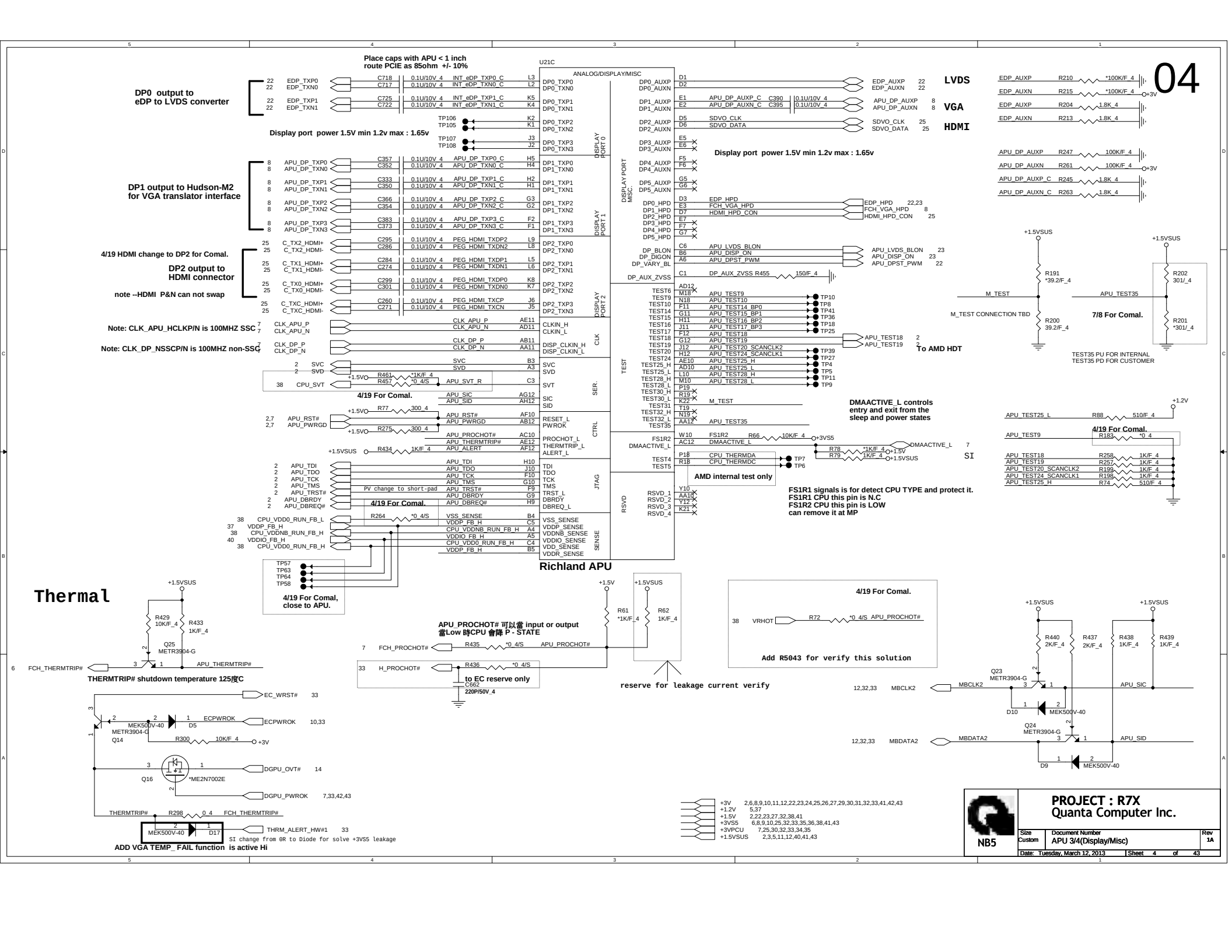
PROJECT :	R7X
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: APU 1/4(PCIE/UMI/GPP/HDT)
Rev: 1A	
Date: Tuesday, March 12, 2013	Sheet 2 of 43





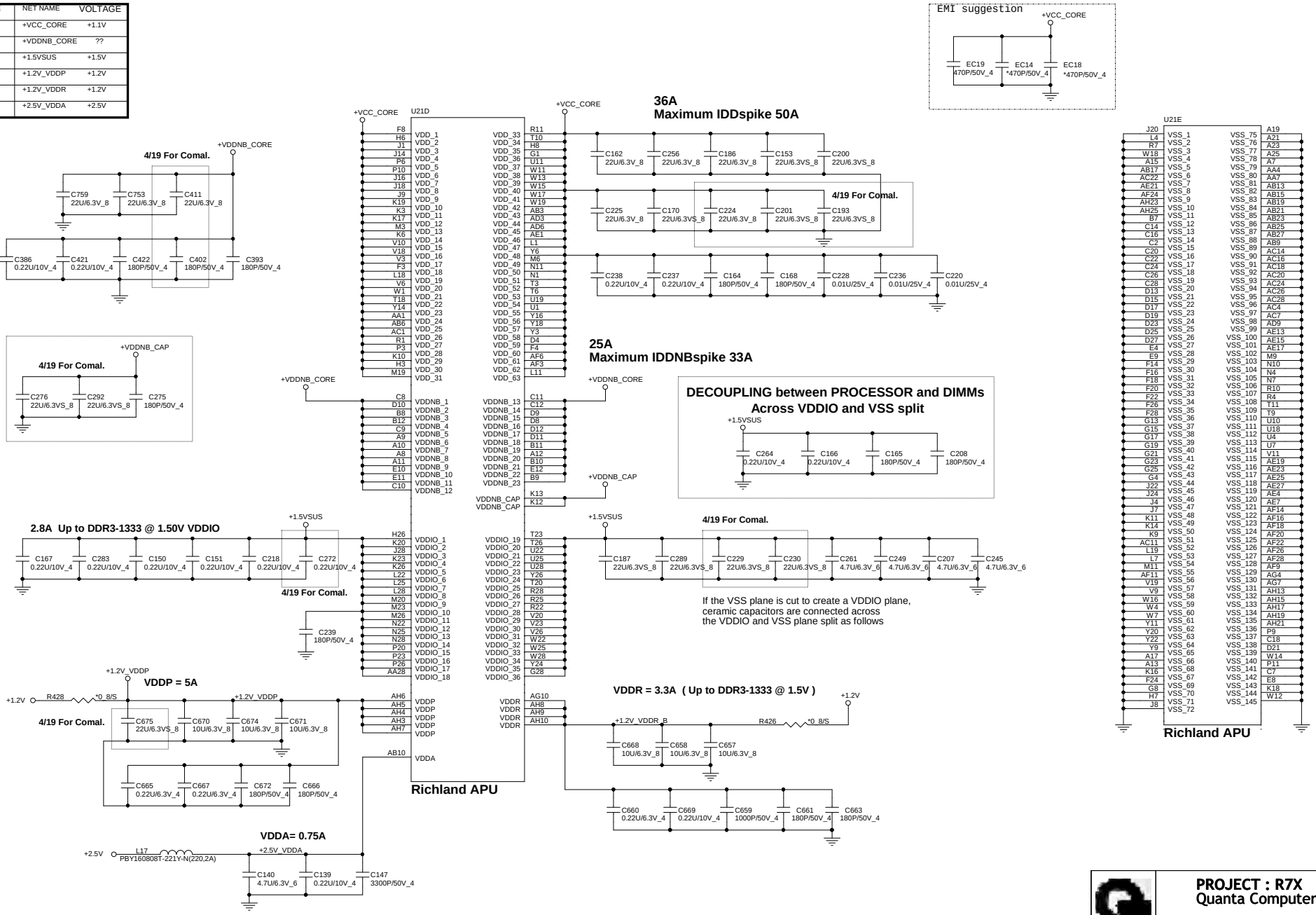
+3VS5 4,6,8,9,10,25,32,33,35,36,38,41,43
+1.5VSUS 2,4,5,11,12,40,41,43

NB5	PROJECT : R7X Quanta Computer Inc.	
Size: Custom	Document Number: APU 2/4(DDR3 MEM I/F)	Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 3 of 43	


04
Place caps with APU < 1 inch
route PCIE as 85ohm +/- 10%
DP0 output to
eDP to LVDS converter
Display port power 1.5V min 1.2v max : 1.65v
DP1 output to Hudson-M2
for VGA translator interface
4/19 HDMI change to DP2 for Comal.
DP2 output to
HDMI connector
note --HDMI P&N can not swap
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC
4/19 For Comal.
4/19 For Comal,
close to APU.
U21C
ANALOG/DISPLAY/MISC
DISPLAY PORT MISC.
DISPLAY PORT 0
DISPLAY PORT 1
DISPLAY PORT 2
CLK
SER.
CTRL
JTAG
TEST
RSVD
SENSE
Richland APU
LVDS
VGA
HDMI
Display port power 1.5V min 1.2v max : 1.65v
7/8 For Comal.
To AMD HDT
TEST35 PU FOR INTERNAL
TEST35 PD FOR CUSTOMER
DMAACTIVE_L controls
entry and exit from the
sleep and power states
4/19 For Comal.
AMD internal test only
FS1R1 signals is for detect CPU TYPE and protect it.
FS1R1 CPU this pin is N.C
FS1R2 CPU this pin is LOW
can remove it at MP
Thermal
THERMTRIP# shutdown temperature 125度C
APU_PROCHOT# 可以當 input or output
當Low 時CPU 會降 P - STATE
to EC reserve only
reserve for leakage current verify
4/19 For Comal.
Add R5043 for verify this solution
ADD VGA TEMP_ FAIL function is active Hi
SI change from 0R to Diode for solve +3VS5 leakage
+3V 2,6,8,9,10,11,12,22,23,24,25,26,27,29,30,31,32,33,41,42,43
+1.2V 5,37
+1.5V 2,22,23,27,32,38,41
+3VS5 6,8,9,10,25,32,33,35,36,38,41,43
+3VPCU 7,25,30,32,33,34,35
+1.5VSUS 2,3,5,11,12,40,41,43
NB5
PROJECT : R7X
Quanta Computer Inc.
Size Custom
Document Number APU 3/4(Display/Misc)
Rev 1A
Date: Tuesday, March 12, 2013
Sheet 4 of 43

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



remove PCIE_RST2# from AMD recommend

BOLTON-M3
Part 4 of 5

4/19 For Comal.

GEVENT0# internal pull Hi 8.2K to +3V
GEVENT1# internal pull Hi 8.2K to +3V

GEVENT23# internal pull Hi 8.2K to +3V
GEVENT5# internal pull Hi 8.2K to +3VS5

PCIE_WAKE# no need to pull
Hi resistor from check list

GEVENT2# internal pull Hi 10K to +3VS5

CLK_REQ4# internal pull Hi 8.2K to +3V
CLK_REQ3# internal pull Hi 8.2K to +3V

CLK_REQ2# internal pull Hi 8.2K to +3V

This pin is used to power down VGA DAC regulators when CRT no connected

LLB# Not Implemented ,left unconnected.

GEVENT16# internal pull Hi 8.2K to +3VS5

GEVENT15# internal pull Hi 8.2K to +3VS5

4/19 For Comal.

For Zero ODD

HD audio interface is +3V_S5 voltage

DB reserve

Left side USB Combo 3.0/2.0.

Left side USB Combo 3.0/2.0.

Camera USB

WLAN Min-Card

Right side USB 2.0 Connector

USB 3.0 Not Implemented: left unconnected

SCL3 of a TSI-capable APU's thermal bus,Pulled up to APU_VDDIO. Resistor value verified in the relevant APU design guide.

No need for GPIO200

Pure UMA can remove

CLK_REQ# already internal pull up 8.2K

Bolton-M3

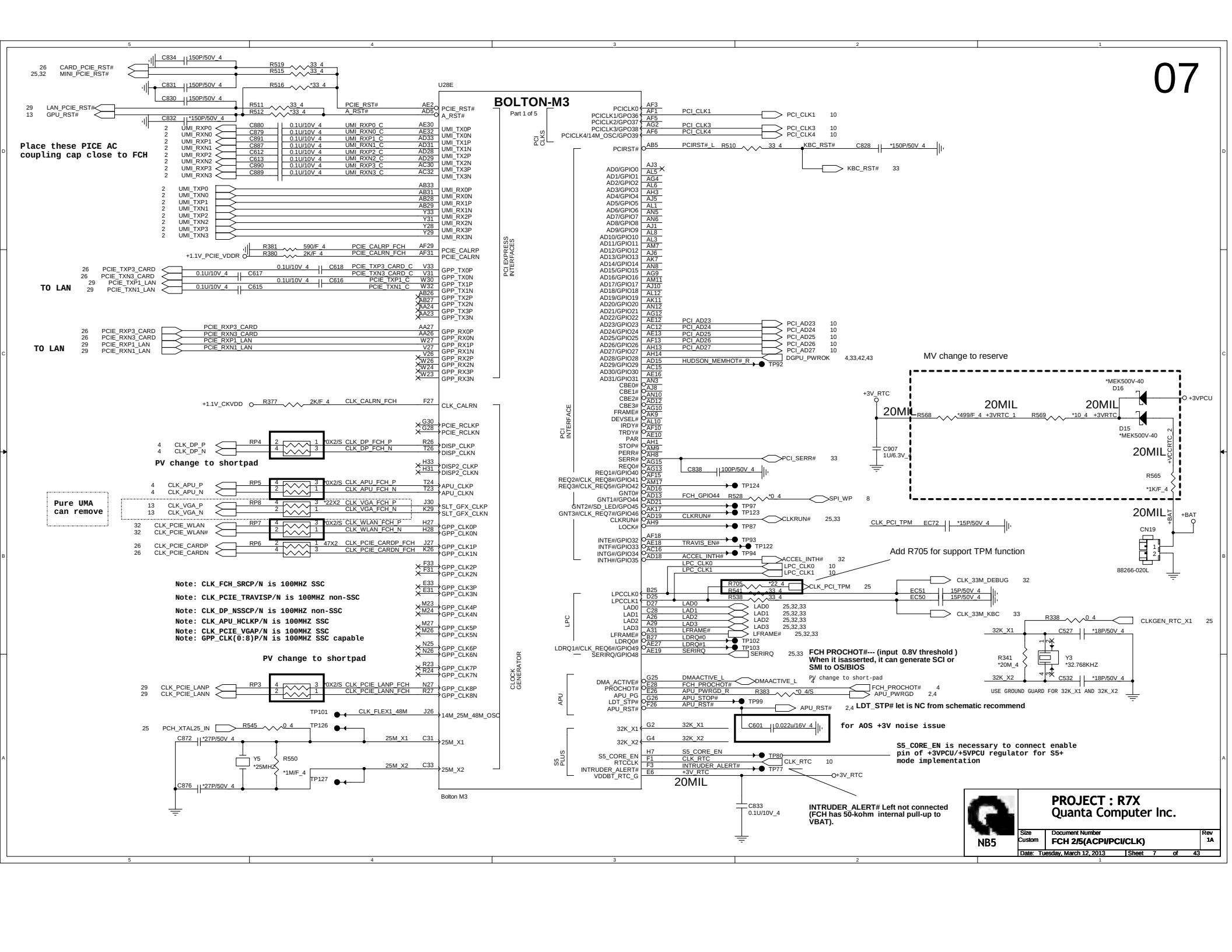
USB_SS_TX/RX0P/N	USB_HSD10P/N
USB_SS_TX/RX1P/N	USB_HSD11P/N
USB_SS_TX/RX2P/N	USB_HSD12P/N
USB_SS_TX/RX3P/N	USB_HSD13P/N

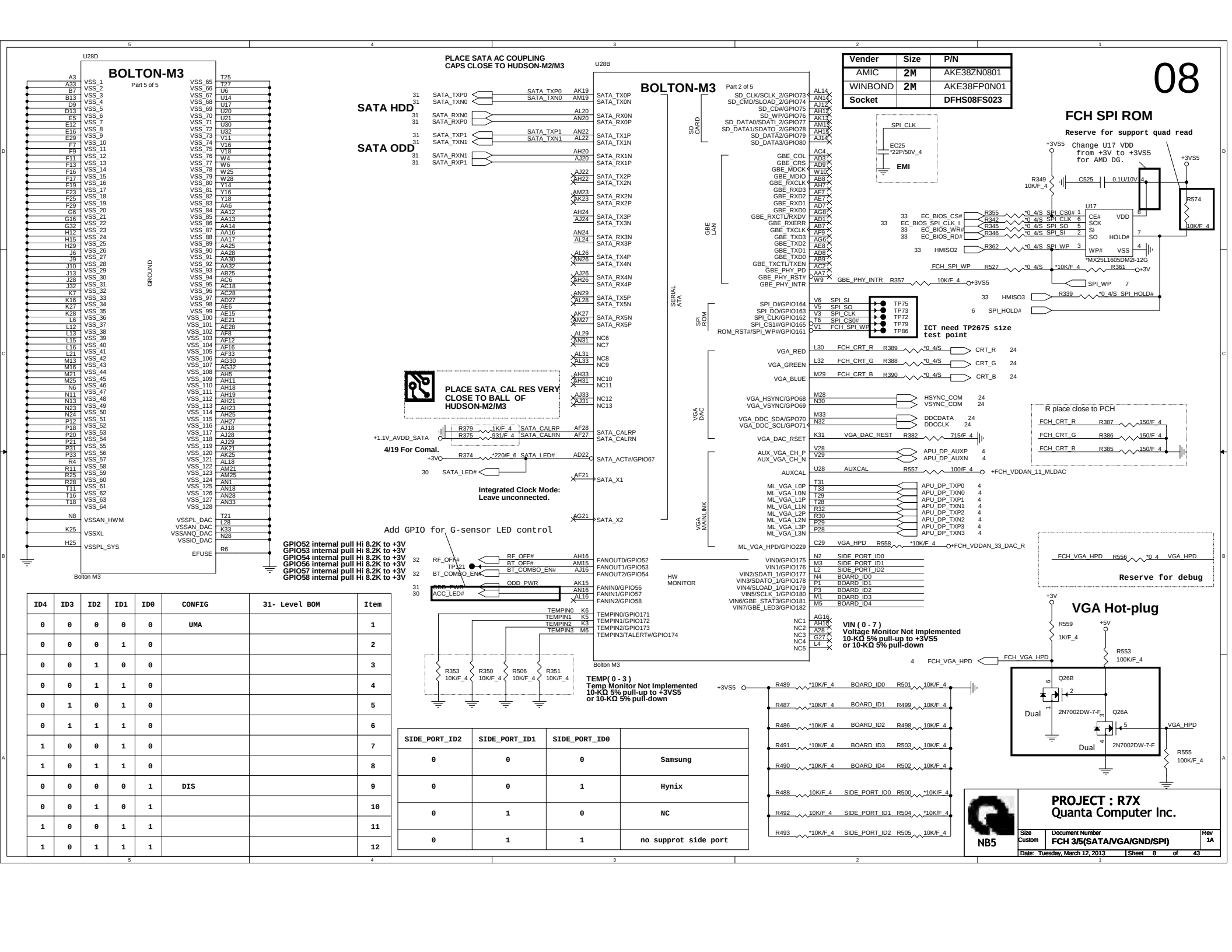
PROJECT : R7X
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	FCH 1/5(GPIO/USB/AZ)	1A

Date: Tuesday, March 12, 2013 Sheet 6 of 43


07
BOLTON-M3
Part 1 of 5
U28E
Bolton M3
Place these PICE AC coupling cap close to FCH
TO LAN
TO LAN
Pure UMA can remove
PV change to shortpad
PV change to shortpad
Note: CLK_FCH_SRCP/N is 100MHZ SSC
Note: CLK_PCIE_TRAVISP/N is 100MHZ non-SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_PCIE_VGAP/N is 100MHZ SSC
Note: GPP_CLK(0:8)P/N is 100MHZ SSC capable
PCI EXPRESS INTERFACES
CLOCK GENERATOR
PCI INTERFACE
LPC
APU
SS PLUS
PCI CLKS
MV change to reserve
Add R705 for support TPM function
FCH PROCHOT#--- (input 0.8V threshold) When it isasserted, it can generate SCI or SMI to OS/BIOS
PV change to short-pad
LDT_STP# let is NC from schematic recommend
for AOS +3V noise issue
S5_CORE_EN is necessary to connect enable pin of +3VPCU/+5VPCU regulator for S5+ mode implementation
INTRUDER_ALERT# Left not connected (FCH has 50-kohm internal pull-up to VBAT).
USE GROUND GUARD FOR 32K_X1 AND 32K_X2
PROJECT : R7X
Quanta Computer Inc.
NB5
FCH 2/5(ACPI/PCI/CLK)
Size Custom
Rev 1A
Date: Tuesday, March 12, 2013
Sheet 7 of 43



Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023

08

ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	DIS		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

BOLTON-M3 Part 3 of 5

VDDQ--3.3V I/O power 102mA

VDDCR-- S/B CORE power 1007mA for M3, 902mA for M2

VDDAN_11_CLK-- Internal clock Generator I/O power 340mA

VDDAN_11_PCIE --PCIE/UMI analog power 1088mA

VDDAN_11_SATA--SATA PHY analog/IO power 1337mA

VDDIO_33_S-- 3.3v S5 I/O power 59mA

VDDXL_33_S-- 25MHZ XTAL IO power 5mA

VDDCR_1.1_S-- 1.1V S5 Core power 187mA

VDDAN_11_ML -- UMI 1.1V analog power 7mA, 226mA

VDDPL_33_USB_S : USB PHY PLL analog power

VDDAN_33_USB_S : USB PHY I/O analog power 470mA

VDDAN_11_USB_S : USB PHY PLL analog power 140mA

VDDCR_11_USB_S : USB PHY core power 42mA

VDDAN_11_SSUSB_S : USB3.0 PHY PLL analog power 282mA

VDDCR_11_SSUSB_S : USB3.0 PHY core power 424mA

VDDIO_AZ_S -- HD Audio Interface I/O power 26mA

VDDPL_11_SYS_S : System Clock Gen PLLs analog power 70mA

VDDAN_33_HWM_S -- Hardware monitor interface I/O power 12mA

VDDPL_11_SYS_S : System Clock Gen PLLs analog power 47mA, 20mA, 20mA, 30mA, 11mA, 14mA, 11mA, 12mA

NOTE : LDO_CAP
A11 stepping : C will install 1nf cap
A12 stepping : C will let it to NC

M2 chipset need to connect to GND
M3 remove

M3 chipset need to stuff for support USB3.0

M2 chipset need to connect to GND M3 remove

M3 chipset need to stuff for support USB3.0

M3 chipset need to stuff for support USB3.0

M3 chipset need to stuff for support USB3.0

if support Modem wake up should be change pull hi to S5 power

if support USB 3.0 wake up should be change pull hi to S5 power

if support USB 3.0 wake up should be change pull hi to S5 power

Reserve for VDDAN_11_CL leakage current issue

This circuit is for switch DAC and UMI analog power 32 mA Max

233 mA Max

VGA will power down when CRT no insert

VGA_PD is generated from FCH

Bolton-M3

+3V	2,4,6,8,10,11,12,22,23,24,25,26,27,29,30
+1.1V	41
+3VS5	4,6,8,10,25,32,33,35,36,38,41,43
+1.1VS5	36,41
+12VALW	34,41,43

PROJECT : R7X
Quanta Computer Inc.

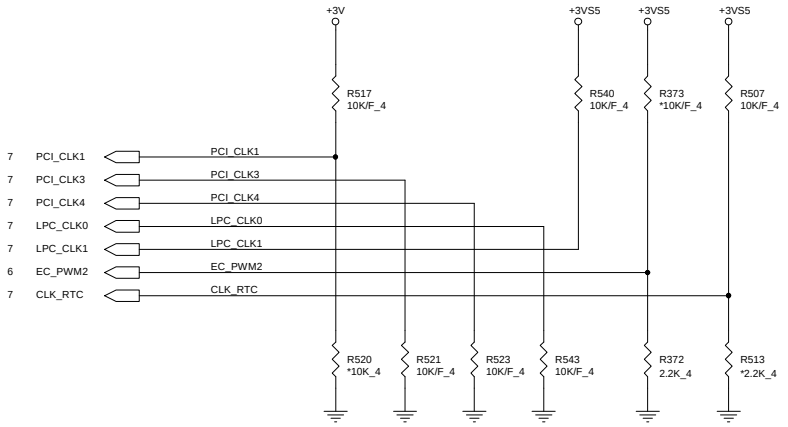
NB5

Size	Document Number	Rev
Custom	FCH 4/5(POWER)	1A

Date: Tuesday, March 12, 2013 Sheet 9 of 43

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



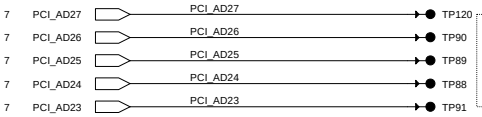
REQUIRED STRAPS

	--------	PCI_CLK1	--------	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

10

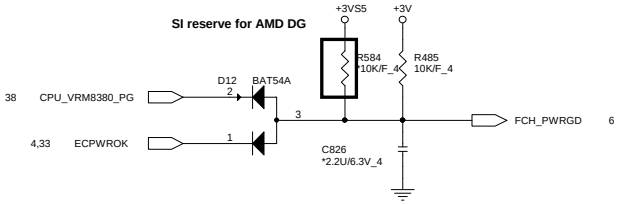
FCH has 15K Internal Pull Up for PCI_AD[27:23]



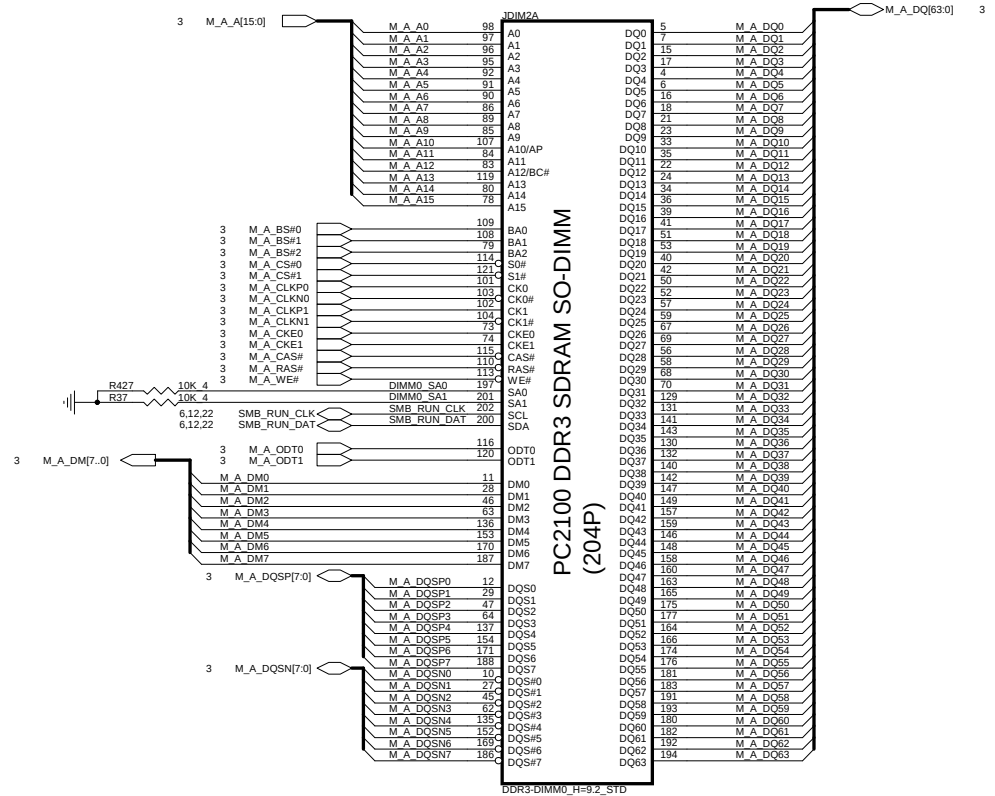
remove reserve pull low resistor
reserve test point only.

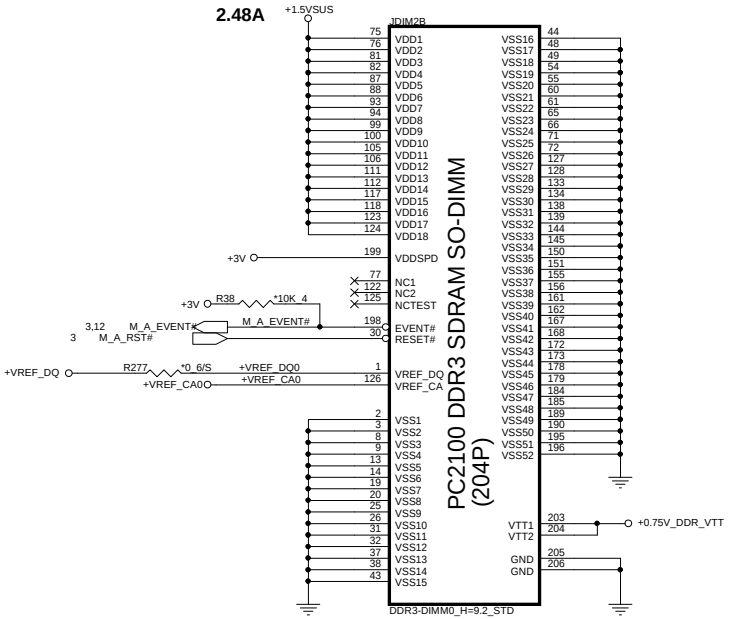
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD

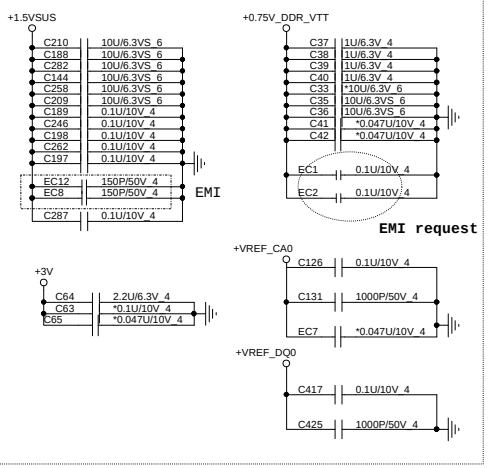


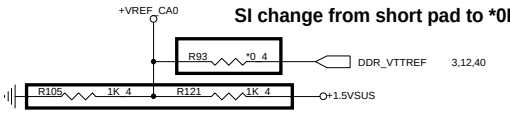
NB5	PROJECT : R7X Quanta Computer Inc.	
Size: Custom	Document Number: FCH 5/5(Strap &PWRGD)	Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 10 of 43	





Place these Caps near So-Dimm0.





SI change from short pad to *0R

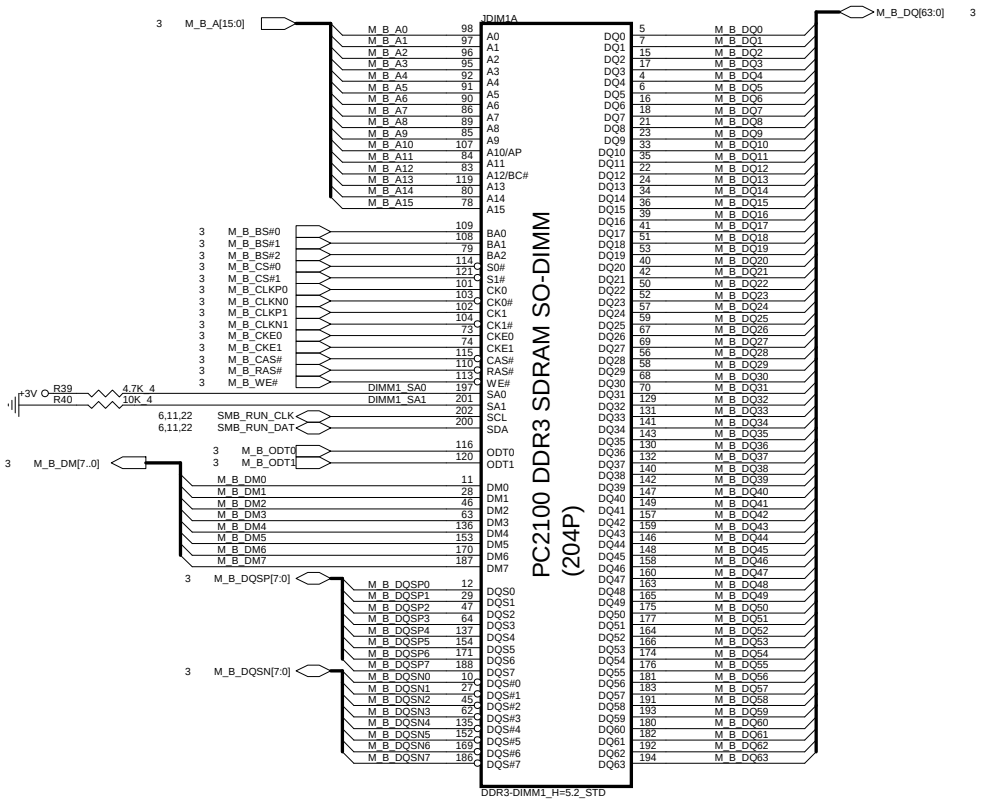
SI stuff

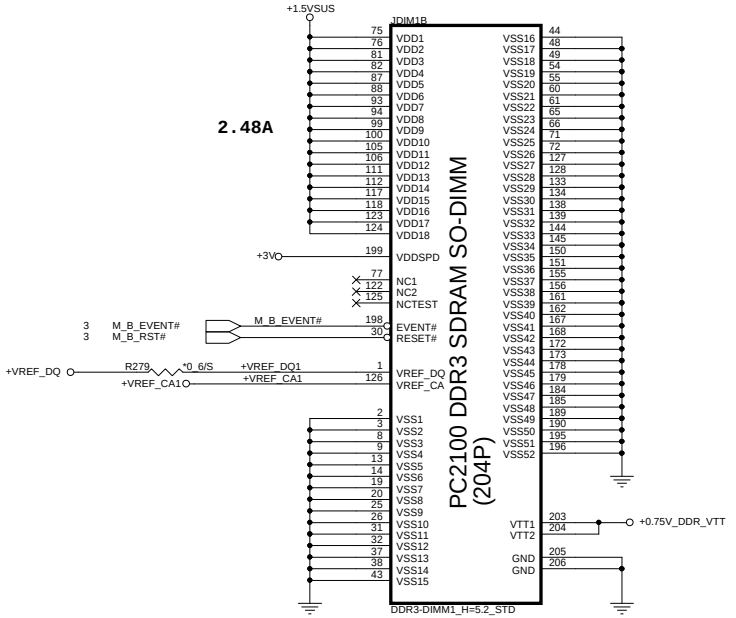
+3V 2,4,6,8,9,10,12,22,23,24,25,26,27,29,30,31,32,33,41,42,43
+1.5V 2,4,22,23,27,32,38,41
+3VPCU 7,25,30,32,33,34,35
+1.5VSUS 2,3,4,5,12,40,41,43
+0.75V_DDR_VTT 12,40

NB5

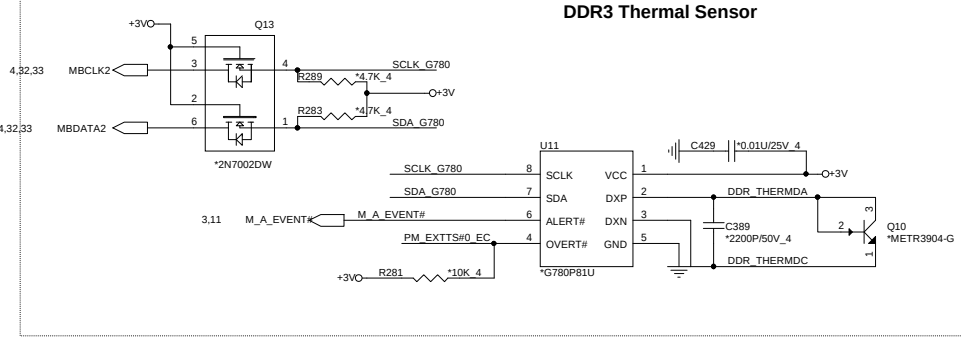
PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-STD (9.2H)	1A
Date: Tuesday, March 12, 2013	Sheet 11 of 43	

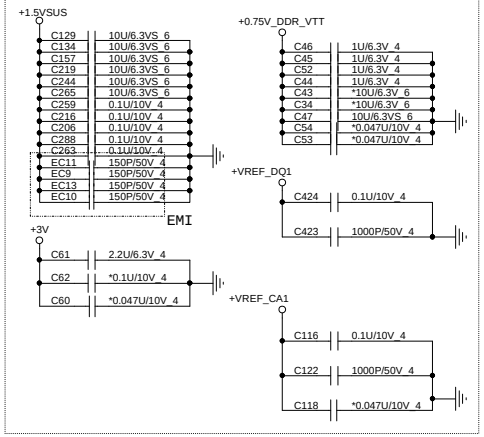


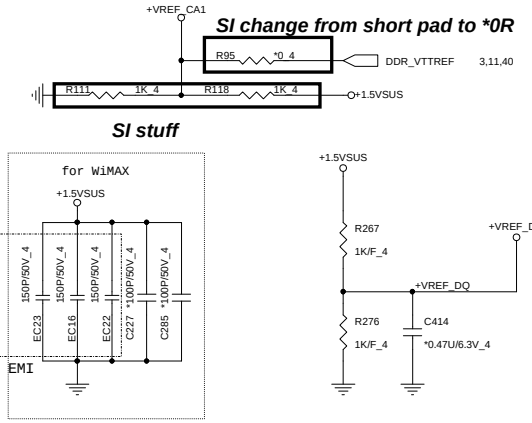


DDR3 Thermal Sensor



Place these Caps near So-Dimm1.





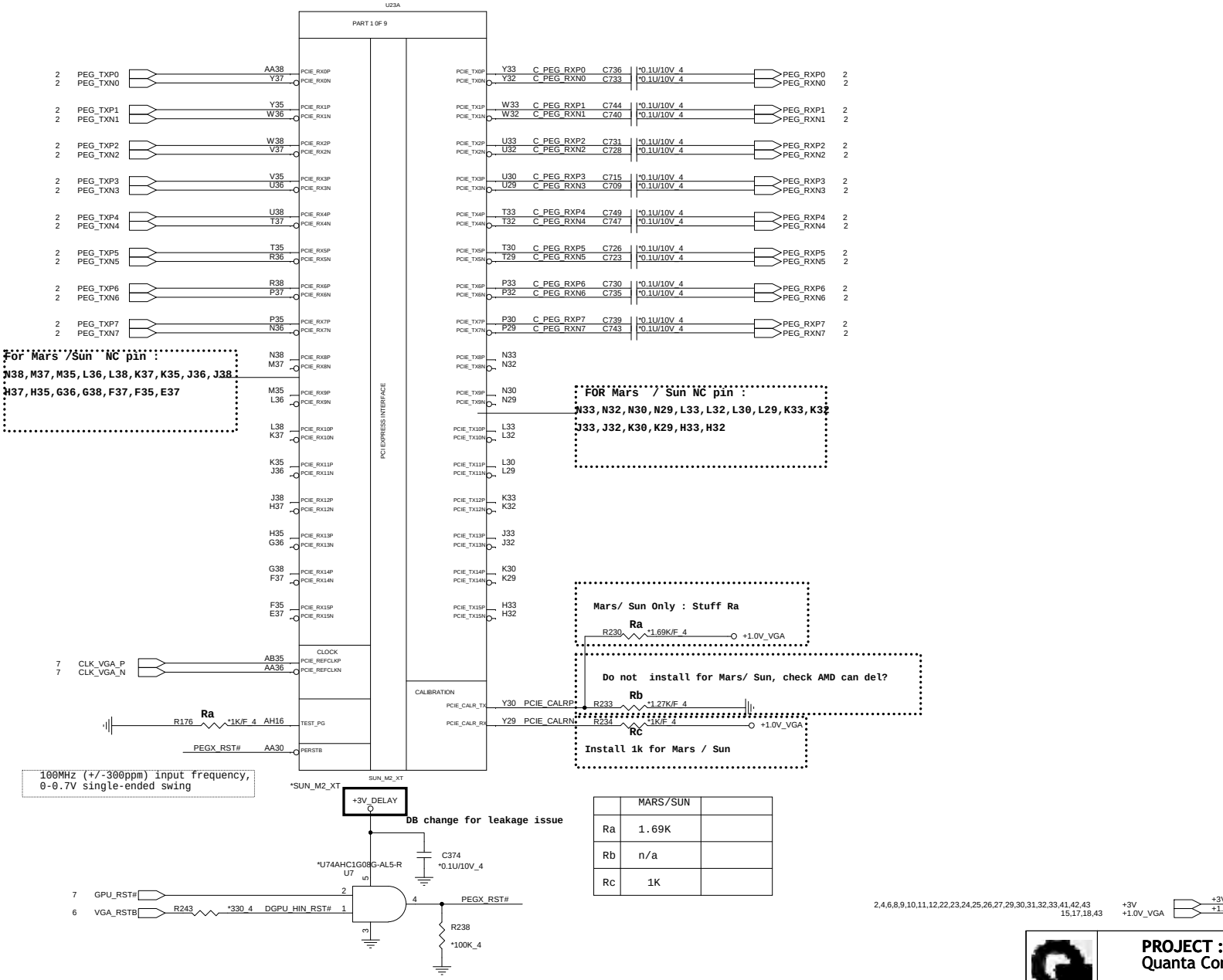
+0.75V_DDR_VTT 11,40
+1.5VSUS 2,3,4,5,11,40,41,43
+3VPCU 7,25,30,32,33,34,35
+3V 2,4,6,8,9,10,11,22,23,24,25,26,27,29,30,31,32,33,41,42,43

NB5

PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-STD (5.2H)	1A

Date: Tuesday, March 12, 2013 Sheet 12 of 43



	MARS/SUN	
Ra	1.69K	
Rb	n/a	
Rc	1K	

2,4,6,8,9,10,11,12,22,23,24,25,26,27,29,30,31,32,33,41,42,43 +3V
15,17,18,43 +1.0V_VGA

NB5

PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SUN_PCIE_Interface	1A

Date: Tuesday, March 12, 2013 Sheet 13 of 43

PS3 BIT3=>BIT1 [3:0]	Vendor		Vendor P/N	QCI P/N (TOP B/S)
011	Hynix	128Mx16 *4	H5TC2G63FFR-11C	AKD5MZDTW02
100	Micron	128Mx16 *4	MT41J128M16JT-093G:K	AKD5MGSTL16
101	Samsung	128Mx16 *4	K4W2G1646E-BC1A	AKD5MGGT534
Only for Test				
PS3 BIT3=>BIT1 [3:0]	Vendor		Vendor P/N	QCI P/N
000	Hynix	256Mx16 *4	H5TC4G63AFR-11C	AKD5PGWTW07
001	Micron	256Mx16 *4	MT41J256M16HA-093G:E	AKD5PZSTL00
010	Samsung	256Mx16 *4	K4W4G1646B-HC1A	AKD5PZDT500

Samsung 2GB VRAM	AKD5MGGT595	K4W2G1646E-BC1A
Samsung 4GB VRAM	AKD5PZDT501	K4W4G1645B-HC1A
Hynix 2GB VRAM	AKD5MZDTW05	H5TC2G63AFR-11C
Hynix 4GB VRAM	AKD5PGWTW08	H5TC4G63AFR-11C
Micron 2G VRAM	AKD5MGSTL17	MT41J128M16JT-093G:E
Micron 4G VRAM	AKD5PZSTL01	MT41J256M16HA-093G:E

For Mars / Sun : AR1/AW8/AR3/AR8/AU8: NC pin

For Sun only : AD29 /AC29 /AJ21 /AK21: NC pin

For Mars / Sun : DP A to D Port: all NC pin

For Sun only :
AP10 /AV11 /AT11 /AR12 /AW12 / AU12 /AP12 : NC pin

SI stuff

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

PV change to shortpad

Base on AMD check list

SI add TEMP FAIL circuit for SUN XT

SI stuff

FOR MARS: AD37/ AE38 / AD35 AVSSN to GND
FOR SUN : AD37/ AE38 / AD35 NC pin
FOR SUN : R222/R224/R225 -->NC

FOR SUN NC PIN : AD34/ AE34 / AC33 / AC34 / AD39 / AE36
AF37/ AC36 / AC38 / AB34 /

FOR SUN GPIO NC PIN : AJ19/ AK19 / AK24 / AM14 / AN14 / AJ24/ AH26 / AH24 / AJ20
AK20/ AH18 / AN16 / AK17 / AK16 / AL16/ AM16

Mars: stuff
For Sun Nc: R140, R124, C148

Thermal Solution(Close to GPU)

Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Reserve for Power Play

For Mars: Stuff Ra, Rc=> VDDC 1.1V
For Thems: Stuff Ra, Rb, Na Rc=> VDDC 1.0V

For Mars / Sun:NC pin
AL30, AM30, AL29, AM29, AN21, AM21, AK30, AK29

For Sun Only :NC pin
AL27, AN27, AM20, AN20, AN26, AM26, AL19, ,
AM19, AJ30, AJ31

MLPS Implementation
- Connect GPIO_20 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms.
- Total DC resistance of trace between C and ground should be less than 2 ohms.
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4980	100
3240	5620	101
3480	10000	110
4750	NC	111

PS_0[3:1]	romsidfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romsidfg[2:0] define memory aperture size If bios_rom_en = 1, romsidfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_s	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_21
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

BIT5 => BIT1

PS0	=>	11001
PS1	=>	11001
PS2	=>	00000
PS3	=>	11011

DB no stuff

PS3 (BIT)=>(BIT)	ID	Memory Type	Configuration	Row x Col x Bank Bit	Channel Size
000	0				
001	1				
010	2				
011	3				
100	4				
101	5				

13,15,17,18,43 +1.0V_VGA +1.0V_VGA
15,17,18,25,43 +1.8V_VGA +1.8V_VGA
13,16,17 +3V_DELAY +3V_DELAY

PROJECT : R7X
Quanta Computer Inc.
NB5
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For Mars/ Sun
Change La, Lb
Bead to 0 ohm

PV change to shortpad

Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

Display Phase Lock Loop Power
DPLL_PVDD : 1.8V @ 75mA

DPLL_VDDC : 0.935V @ 140mA

1.0V(125mA DPLL_VDDC)

MPLL_PVDD : 1.8V @ 150mA

SPLL_PVDD : 1.8V @ 75mA

SPLL_VDDC : 0.935V @ 150mA

1.0V(125mA DPLL_VDDC)

reserve Ra, Rb for future ASIC

DB change from X0_IN for AMD suggestion

DB change to XTAI_IN for AMD suggestion

Debug only,
for clock observation,
if not needed, DNI

route 50ohms
single-ended/
100ohms diff and keep short

Mars/Sun AG22 is nc pin

13,17,18,43 +1.0V_VGA

14,17,18,25,43 +1.8V_VGA

NB5	PROJECT : R7X Quanta Computer Inc.		
	Size: Custom	Document Number: SUN_XTAL	Rev: 1A
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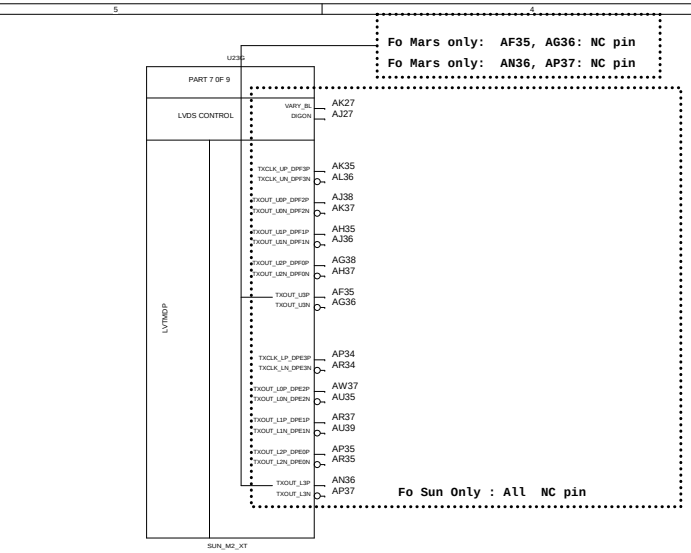
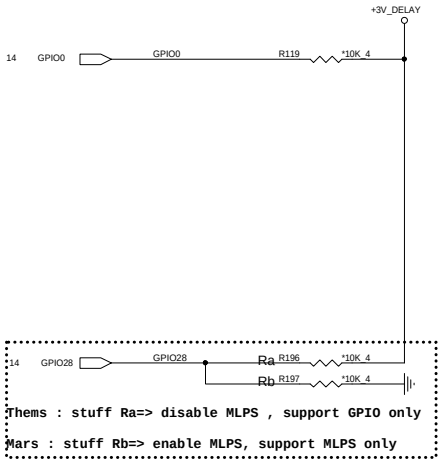
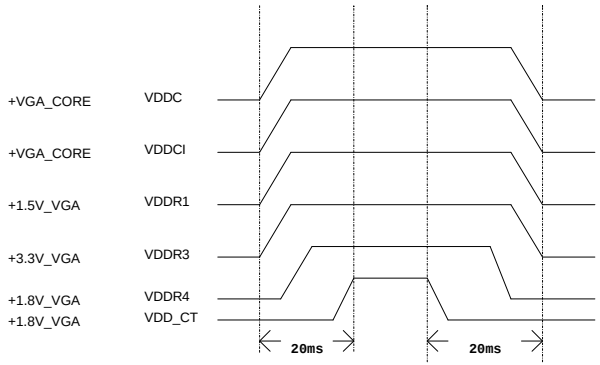




CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	0
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 100 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	001
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	0
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled, It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled Reserve for future ASIC	1
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	111

Power Up/Down Sequence



NB5

PROJECT : R7X
Quanta Computer Inc.

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Custom	SUN_LVDS / STRAP	1A
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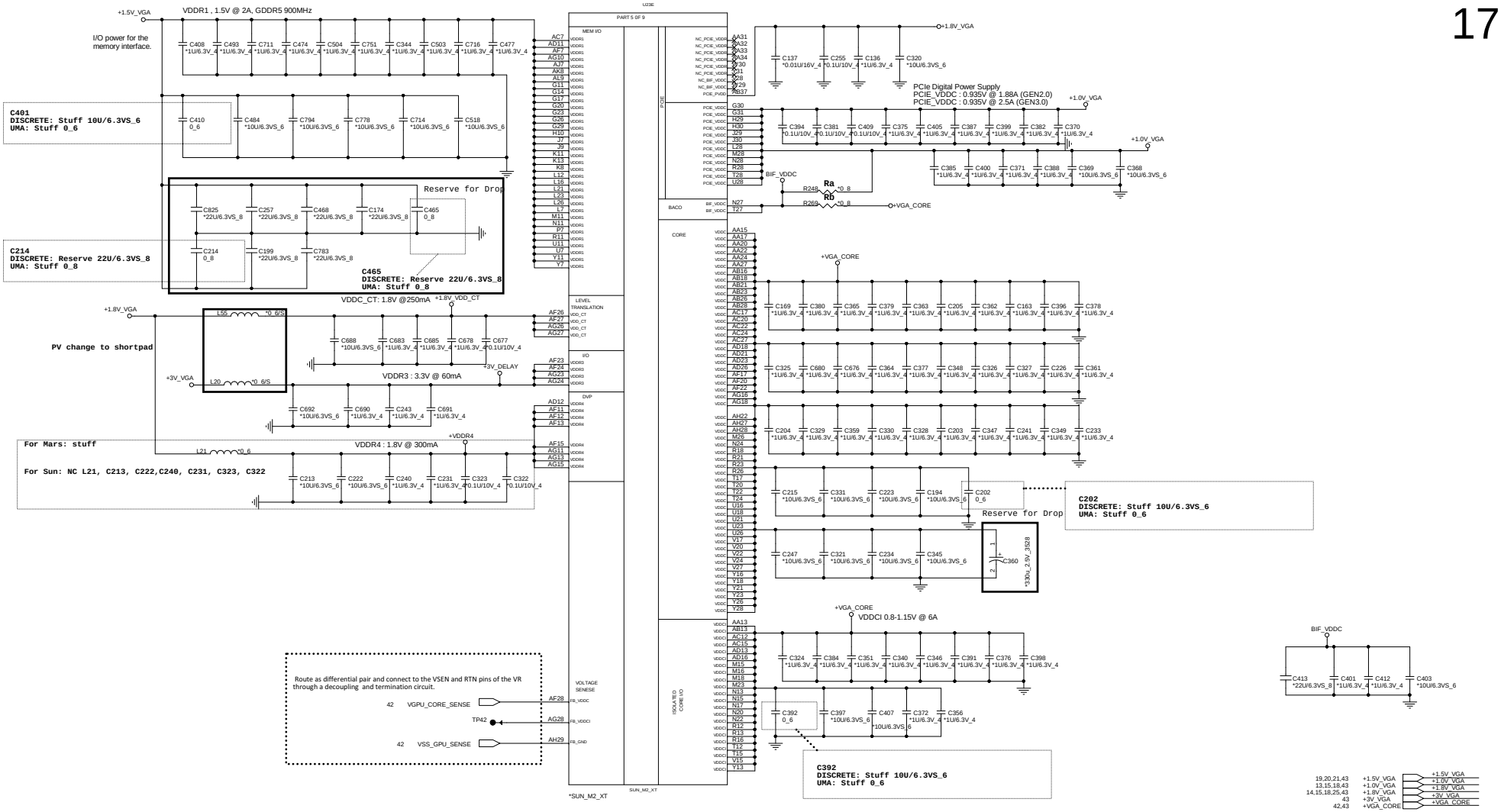

Support BACO Mode

Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

NB5	PROJECT : R7X Quanta Computer Inc.	
Size: Custom	Document Number: SUN_Power & BACO	Rev: 1A
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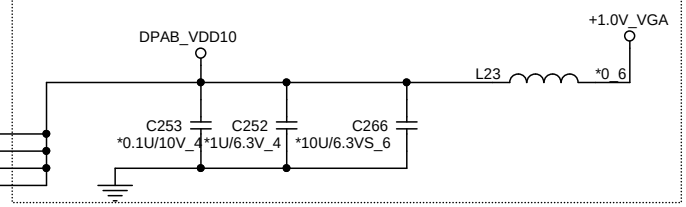
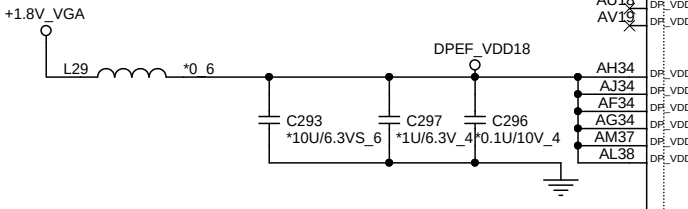
For Mars : L23, C253, C252 sutff

For Sun: L23 , C247 , C266 , C252 NC



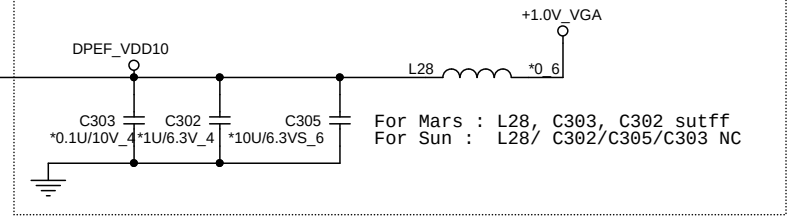
For Mars : L29, C297, C296 sutff

For Sun: L29 , C293 , C297 , C296 NC



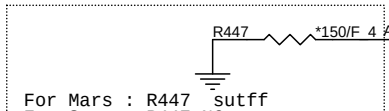
For Mars : L28, C303, C302 sutff

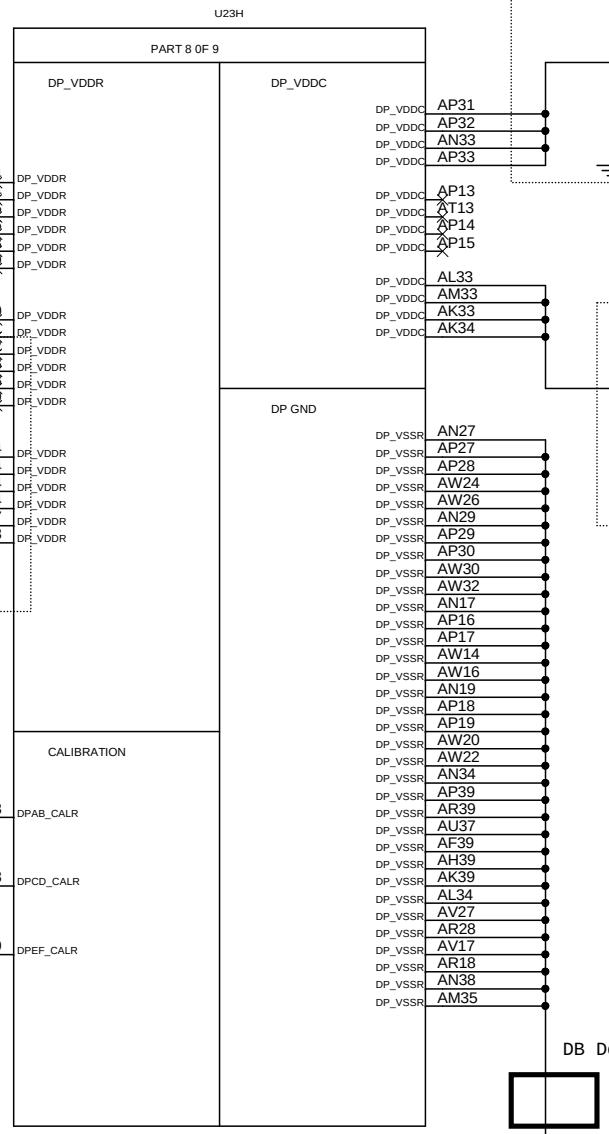
For Sun : L28/ C302/C305/C303 NC



For Mars : R447 sutff

For Sun : R447 NC





DB Del R180 and connect to GND directly, for AMD suggestion

13,15,17,43 +1.0V_VGA

14,15,17,25,43 +1.8V_VGA

+1.0V_VGA

+1.8V_VGA

PROJECT : R7X

Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	**SUN_DP Powers**	1A
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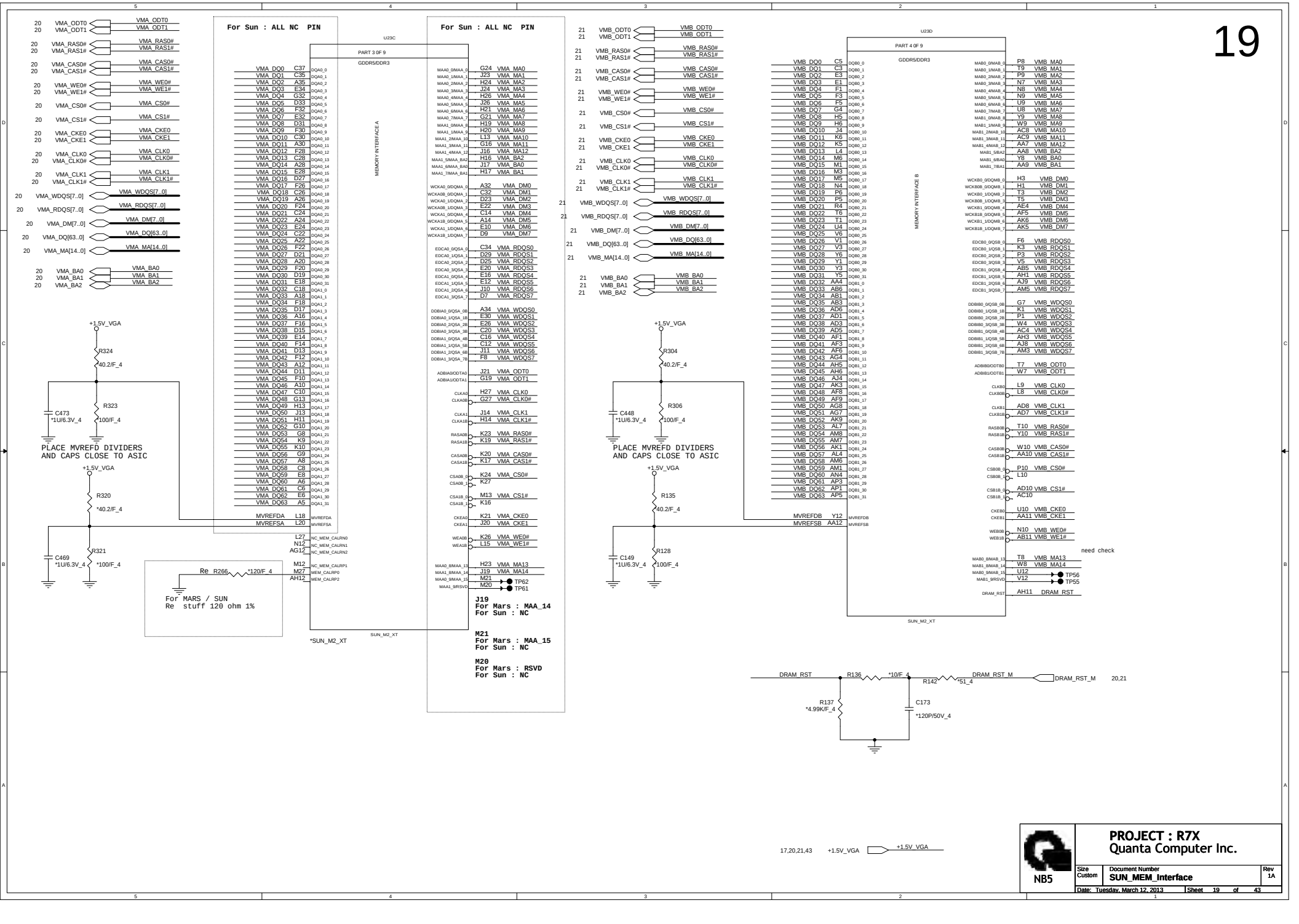

Project	PROJECT : R7X Quanta Computer Inc.
Size / Custom	Document Number: SUN_MEM_Interface
Rev	1A
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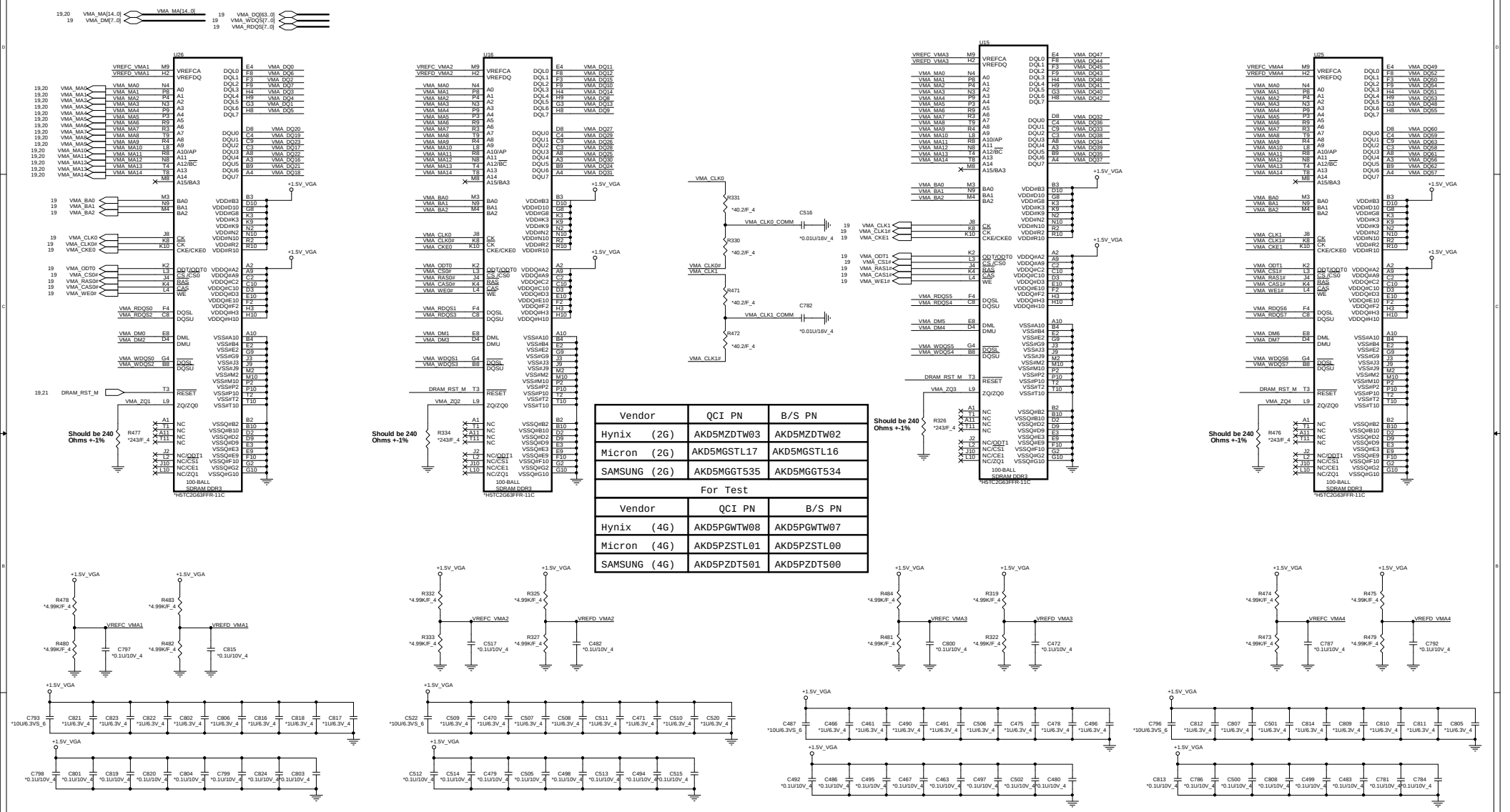
CHANNEL A: 256MB/512MB DDR3



Vendor	QCI PN	B/S PN
Hynix (2G)	AKD5MZDTW03	AKD5MZDTW02
Micron (2G)	AKD5MGSTL17	AKD5MGSTL16
SAMSUNG (2G)	AKD5MGGT535	AKD5MGGT534
For Test		
Vendor	QCI PN	B/S PN
Hynix (4G)	AKD5PGWTW08	AKD5PGWTW07
Micron (4G)	AKD5PZSTL01	AKD5PZSTL00
SAMSUNG (4G)	AKD5PZDT501	AKD5PZDT500

17,19,21,43 +1.5V_VGA +1.5V_VGA

NB5	PROJECT : R7X Quanta Computer Inc.
Size: Custom	Document Number: VRAM-A (DDR3 BGA96) Rev: 3A
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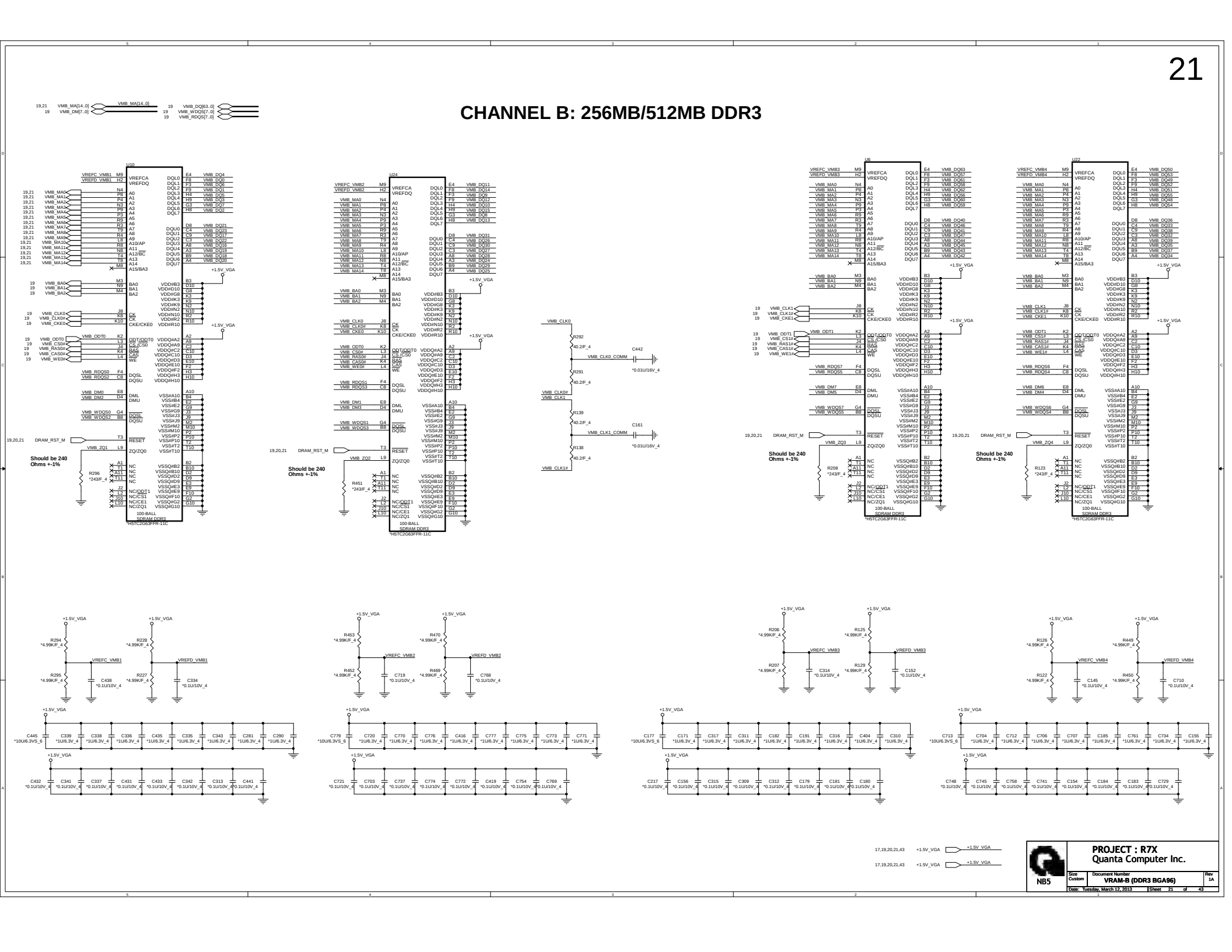
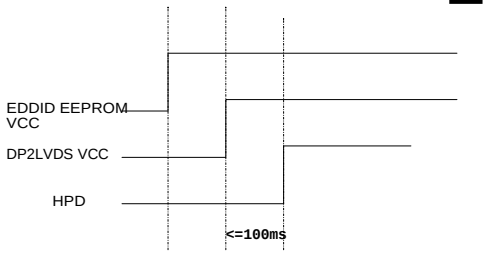
CHANNEL B: 256MB/512MB DDR3



RTD2136S Power Up Sequence



RTD2136 Dual Channel only

Pine 18: keep 80 Mile Trace

Pine 20: keep 80 Mile Trace

IC底部需接GND VIA*9

RTD2136R

EC

SMBUS

PV change to shortpad

DB change from SMB_PCH_CLK/DAT to SMB_RUN_CLK/DAT

Use 1% Res on R5553

RTD2136R combined level shift already

Reserve

*M24C02
Should be using M24C64

L69: need use CV-4709MN00 for Vendor suggestion

RTD2136R
R107;R114: NA
R106;R115: Stuff

SWR: Stuff L5066
LDO: Stuff R9098

keep 80 Mile Trace

USING 60R 1A

CLOSE TO Pin22

Close to Pin18
C2142 close to IC side

Close to Pin5

Close to Pin11

Close to Pin17

Close to Pin43

NB5	PROJECT : R7X Quanta Computer Inc.		
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LID Switch

change to shortpad

33 EMU_LID — R59 *0_4/S — PN_BLON — D1 MEK500V-40 — BLON_CON — C2 22P/50V_4 — R1 100K/F_4

LVDS_BLON1 R54 1K/F_4

LVDS_BLON1 R47 100K/F_4

100mA +VIN_BLIGHT

+VIN — L3 0_8 — +VIN_BLIGHT

L1 0_8 — C1 0.1U/25V_4 — C3 0.01U/25V_4

+VIN

C7 4.7U/25V_8 — C16 0.1U/25V_4 — C21 0.1U/25V_4 — C11 0.1U/25V_4 — C15 0.1U/25V_4

+VIN

C5 4.7U/25V_8 — C10 0.1U/25V_4

BRIGHT — R2 1K/F_4 — VADJ1

R4 100K/F_4 — C4 33P/50V_4

Power Switch Reserve — **80 mile trace**

+3VLCD_CON — R51 0_8 — R45 1K/F_4

C86 4.7U/6.3V_6 — +3V

C73 *1U/6.3V_4

U2: IN, IN, ON/OFF, OUT, GND — *IC(5P) G5243AT11U

DISP_ON_L

L11 *TI160808U600

+3VLCD_CON — C68 0.01U/16V_4 — C67 0.1U/10V_4 — C71 10U/6.3V_8

AL005243001 GMT:G5243AT11U
AL002821000 BCD:AP2821KTR-G1

22 TXECLKOUT- — TXECLKOUT-
22 TXECLKOUT+ — TXECLKOUT+
22 TXEOUT0+ — TXEOUT0+
22 TXEOUT0- — TXEOUT0-
22 TXEOUT1+ — TXEOUT1+
22 TXEOUT1- — TXEOUT1-
22 TXEOUT2+ — TXEOUT2+
22 TXEOUT2- — TXEOUT2-

22 TXOCLKOUT+ — TXOCLKOUT+
22 TXOCLKOUT- — TXOCLKOUT-
22 TXOOUT2+ — TXOOUT2+
22 TXOOUT2- — TXOOUT2-

USBP8-
R3 301/F_4
C8 15P/50V_4

+3V — R5 *0_4/S — +3V_CAM

C6 *0.01U/16V_4 — C9 *4.7U/6.3V_6

RF

+3V — R23 4.7K_4 EDIDCLK — R24 4.7K_4 EDIDDATA

C26 *10P/50V_4 — C27 *10P/50V_4

+3VLCD_CON

C590.047U/10V_4 — C510.047U/10V_4

+VIN_BLIGHT — R41 *0_6 — Ra

+3V — R42 0_6 — Rb — C28 1000P/50V_4

For EDP Only: Stuff Ra

For LVDS Only: Stuff Rb

For EDP Only: Stuff Rd
For LVDS Only: Stuff Rc

Rc — R8 0_4

4,22 EDP_HPD — R9 *0_4 EDP_HPD_R

Rd

27 DIGITAL_D1
27 DIGITAL_CLK

L4 TB160808U301N000 — DIGITAL_CLK_L

C12 *10P/50V_4 — C13 *10P/50V_4

6 USBP8-
6 USBP8+

L2 MCM2012B900GBE-90 — +3V_CAM — USBP8-_R — USBP8+_R

VADJ1

BLON_CON

+VIN_BLIGHT

EDIDCLK
EDIDDATA
TXOOUT0-
TXOOUT0+
TXOOUT1-
TXOOUT1+
TXOOUT2-
TXOOUT2+
TXOCLKOUT-
TXOCLKOUT+
TXEOUT0-
TXEOUT0+
TXEOUT1-
TXEOUT1+
TXEOUT2-
TXEOUT2+
TXECLKOUT-
TXECLKOUT+

CN1
GS12401-1011-9H
DFHS40FS088
GS12407-11141-9H-40P-R

Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

22 EDP_TXP0_R — C24 *0.1U/10V_4 — R15 0_4 — TXOOUT0+
22 TXOOUT0+_2136 — R18 0_4 — TXOOUT0-
22 TXOOUT0-_2136 — C25 *0.1U/10V_4
22 EDP_TXN0_R

22 EDP_TXP1_R — C17 *0.1U/10V_4 — R11 0_4 — TXOOUT1+
22 TXOOUT1+_2136 — R14 0_4 — TXOOUT1-
22 TXOOUT1-_2136 — C22 *0.1U/10V_4
22 EDP_TXN1_R

22 EDP_AUXP_R — C48 *0.1U/10V_4 — R33 0_4 — EDIDCLK
22 EDIDCLK_2136 — R34 0_4 — EDIDDATA
22 EDIDDATA_2136 — C49 *0.1U/10V_4
22 EDP_AUXN_R

For EDP Only: stuff 0 Ohm
For LVDS only stuff Resistor

For EDP Only: stuff

+3V — R36 *100K_4 EDIDDATA — R35 *100K_4 EDIDCLK

+3V — R6 *1K_4 BRIGHT — R48 *1K_4 LVDS_BLON1

For EDP Only

+1.5V — R96 *2.2K_4 — Q3 *METR3904-G — +3V — R110 *10K/F_4

4 APU_LVDS_BLON — LVDS_BLON — R101 *0_4

+1.5V — R89 *2.2K_4 — Q4 *METR3904-G — +3V — R113 *10K/F_4

4 APU_DISP_ON — DISP_ON — R117 *0_4

For LVDS Only: stuff Ra,Rb,Rc

22 DPST_PWM_2136 — Ra R32 0_4 BRIGHT
22 LVDS_BLON_2136 — Rb R50 0_4 LVDS_BLON1
22 DISP_ON_2136 — Rc R55 0_8 DISP_ON_L

For EDP Only: stuff Rd,Re,Rf

22 DPST_PWM — Rd R28 *10_4 BRIGHT
LVDS_BLON — Re R49 *0_4 LVDS_BLON1
DISP_ON — Rf R57 *0_4 DISP_ON_L

2,4,6,8,9,10,11,12,22,24,25,26,27,29,30,31,32,33,41,42,43 — +3V
8,24,25,26,27,30,31,32,41 — +5V
34,35,36,37,39,40,41,42,43 — +VIN
7,25,30,32,33,34,35 — +3VPCU

NB5

PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
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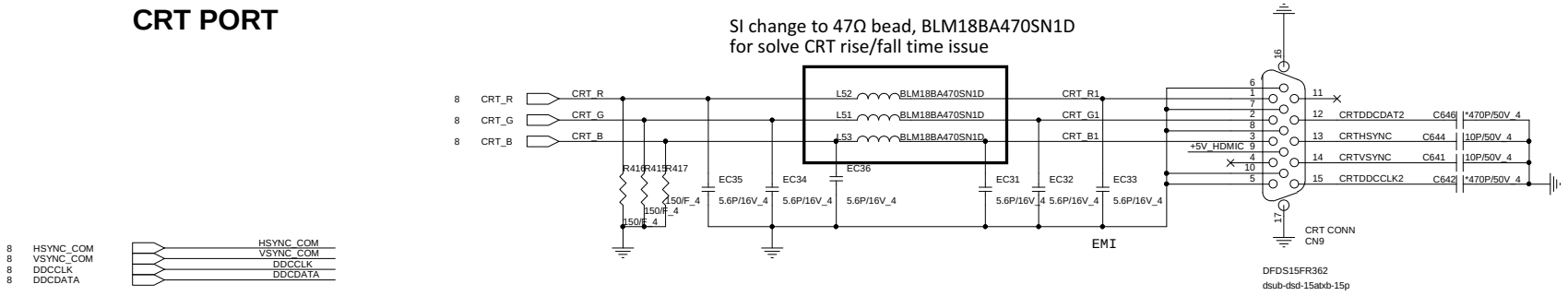
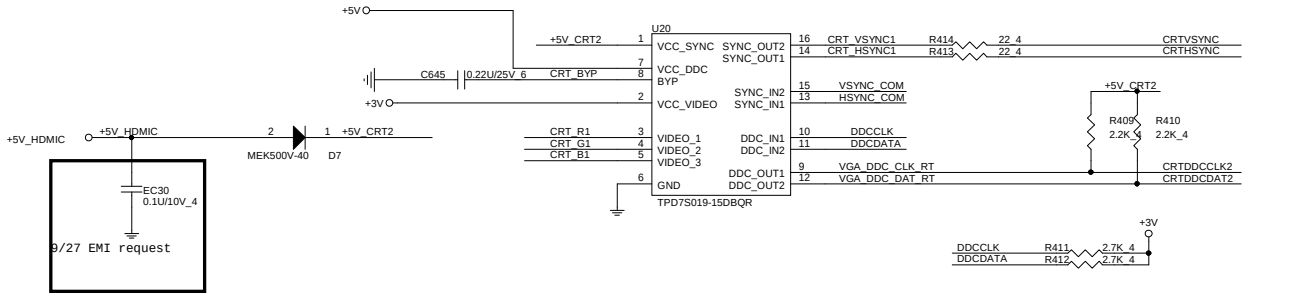
CRT PORT

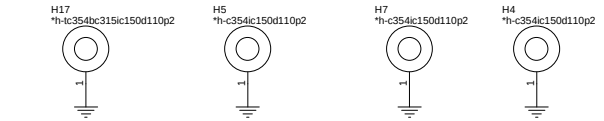
SI change to 47Ω bead, BLM18BA470SN1D
for solve CRT rise/fall time issue

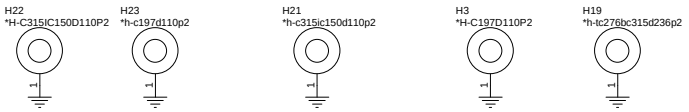


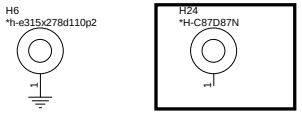


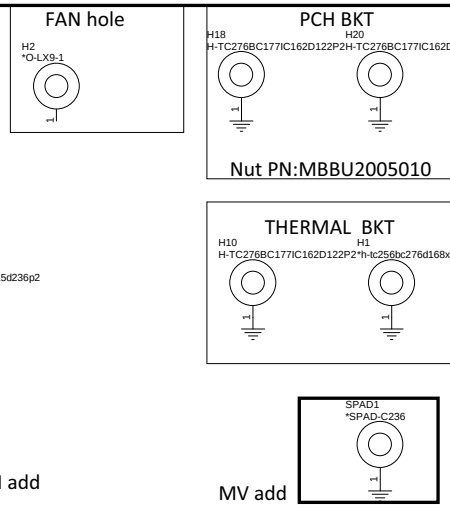
HOLE

HOLE



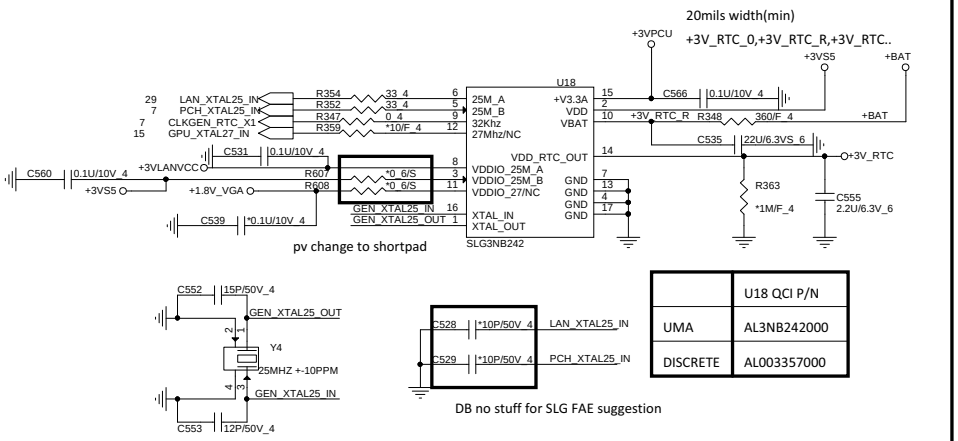






NB5	PROJECT : R7X Quanta Computer Inc.
Size: Custom	Document Number: CRT,Hole
Rev: 1A	
Date: Tuesday, March 12, 2013	Sheet 24 of 43

Green CLK Circuitry



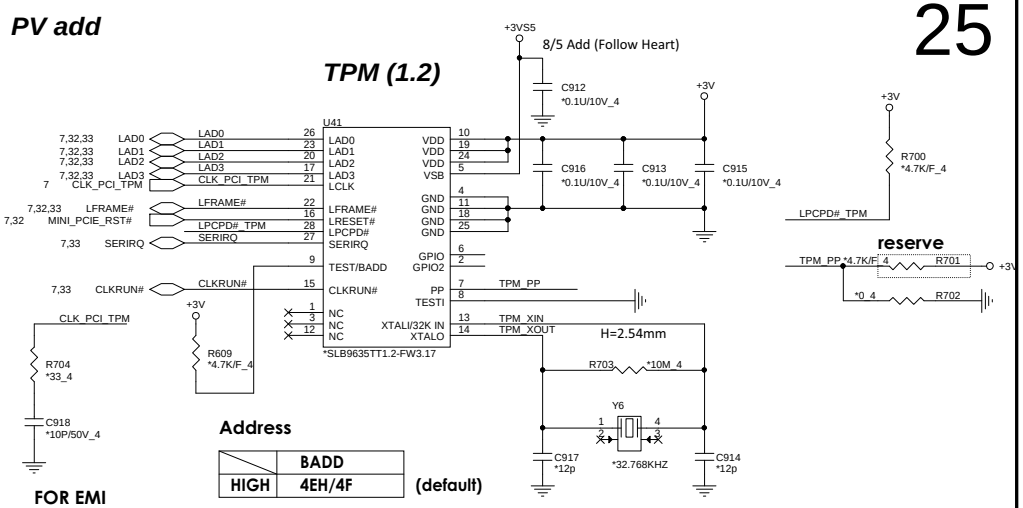
	U18 QCI P/N
UMA	AL3NB242000
DISCRETE	AL003357000

PV add

25

8/5 Add (Follow Heart)

TPM (1.2)



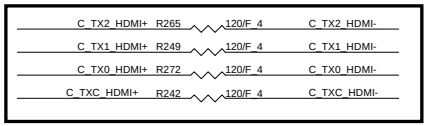
Address

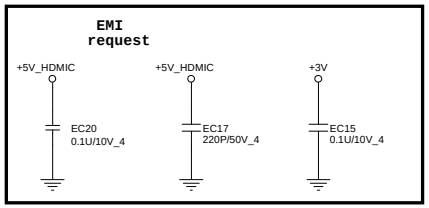
	BADD
HIGH	4EH/4F (default)

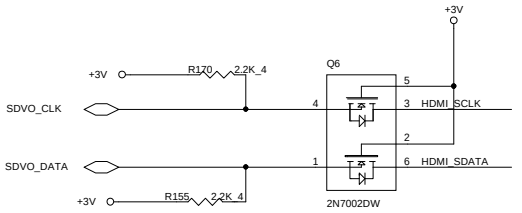
FOR EMI

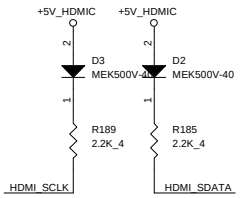
DISCRETE HDMI I2C SELECT
Close to HDMI Connector

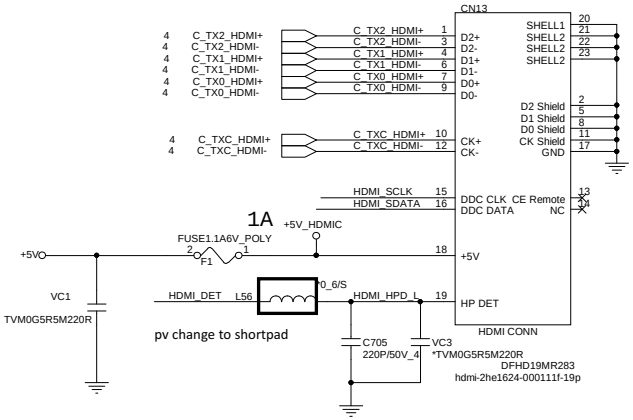
EMI request

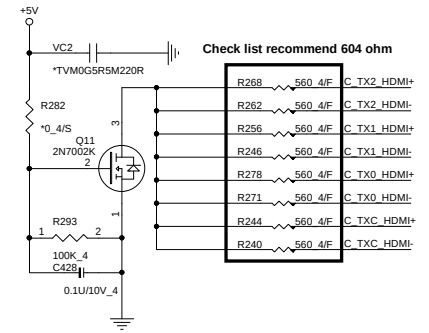


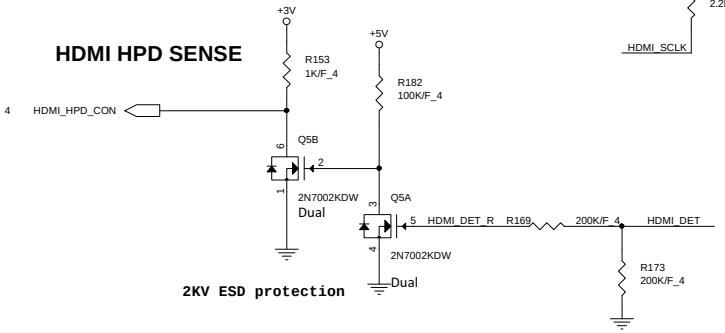




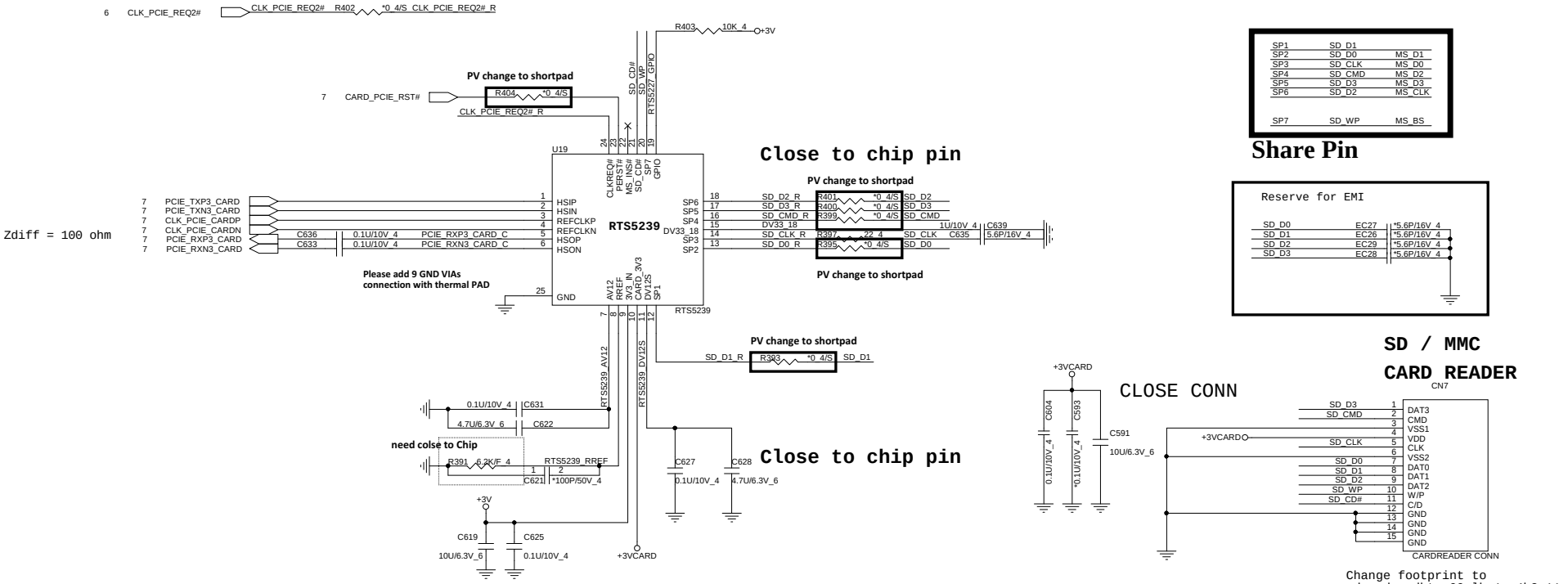








NB5	PROJECT : R7X Quanta Computer Inc.
Size: Custom	Document Number: HDMI
Rev: 1A	
Date: Tuesday, March 12, 2013	Sheet 25 of 43



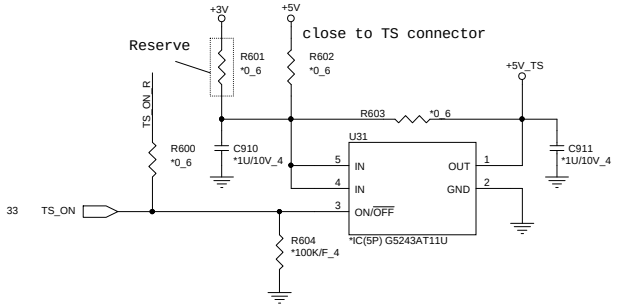
Share Pin

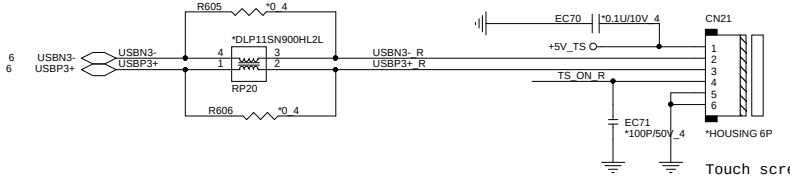
SD / MMC

CARD READER

Change footprint to
sdcard-psdbtc-09glbs1nn4h3-11p

Touch Screen Connector



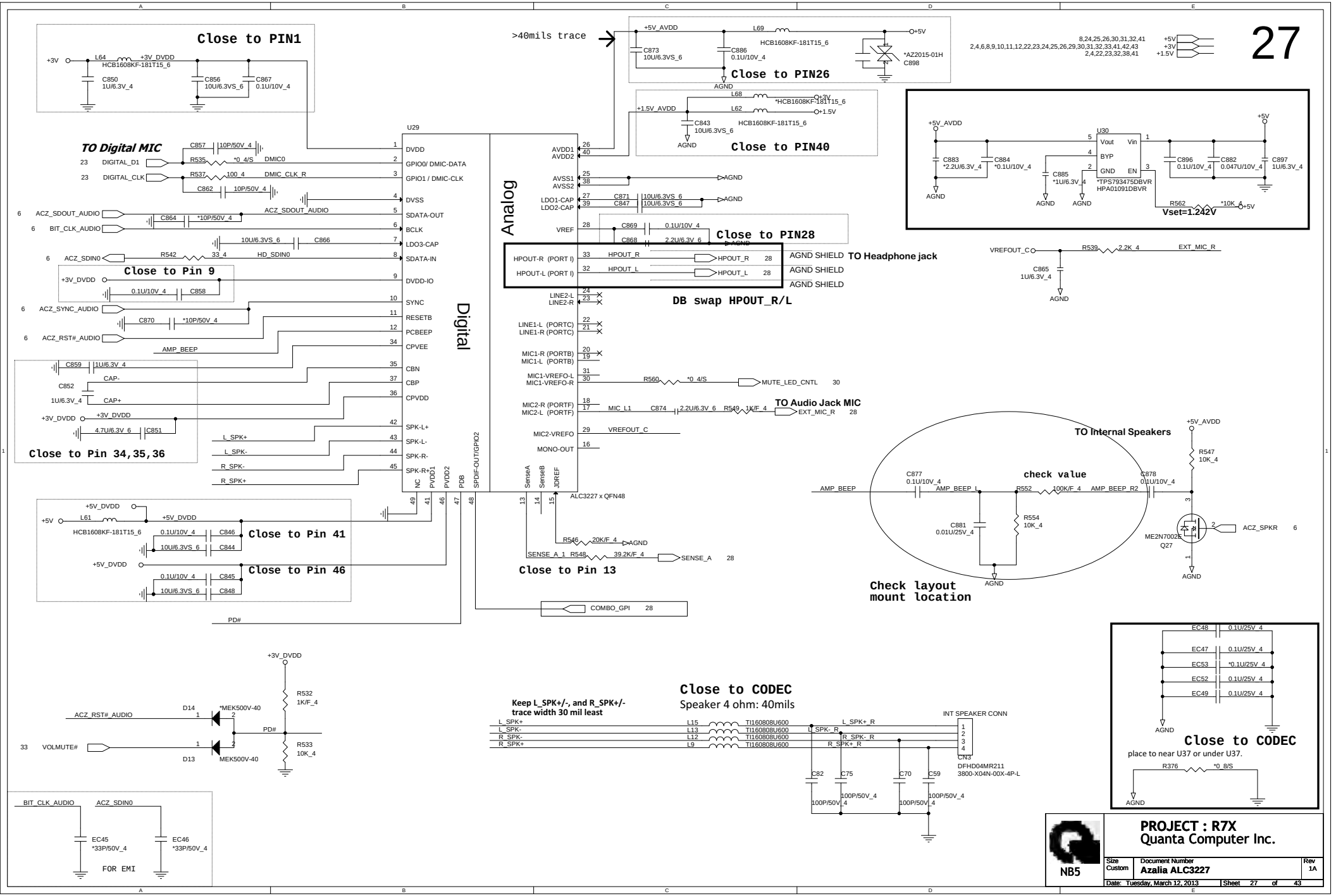


Touch screen Conn

PROJECT : R7X
Quanta Computer Inc.

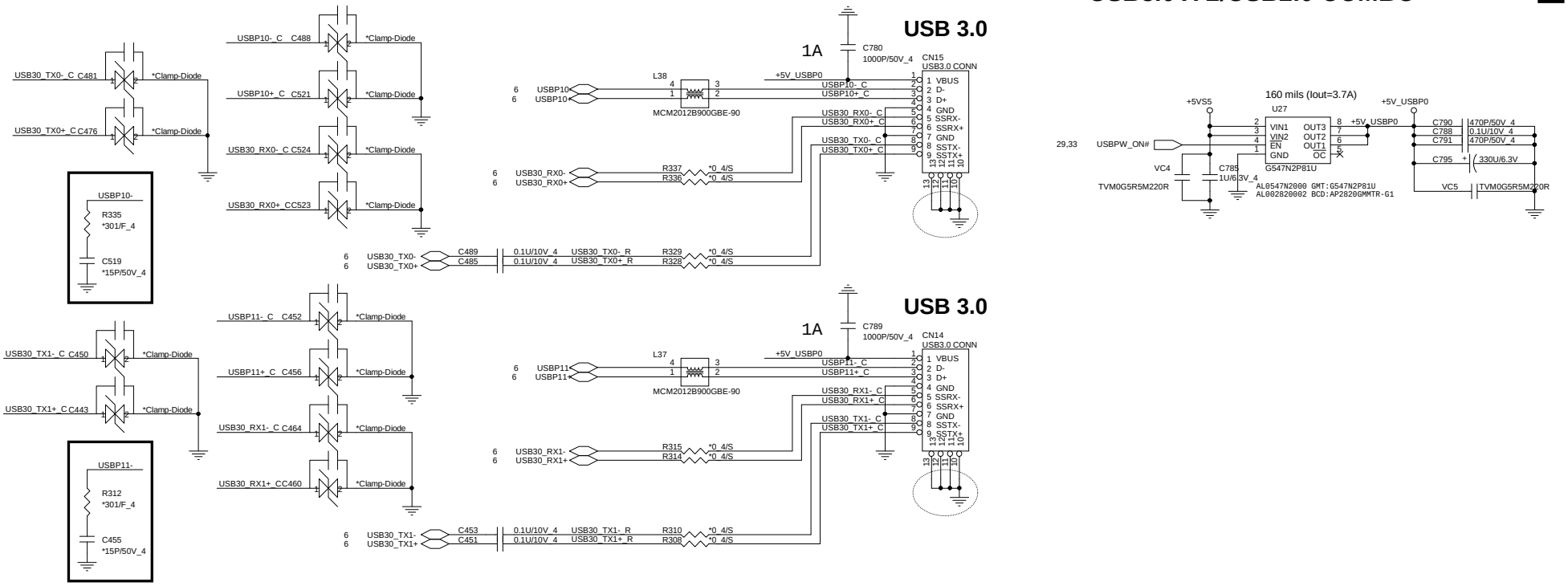
Size	Document Number	Rev
Custom	RTS5229 & CR SOCKET	1A
Date: Tuesday, March 12, 2013	Sheet 26 of 43	

NB5

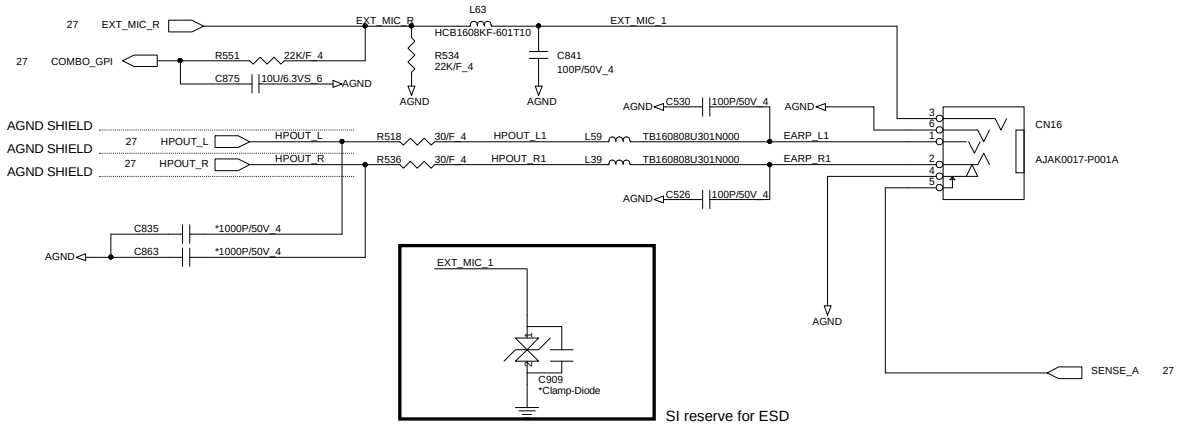


NB5	PROJECT : R7X Quanta Computer Inc.		
	Size: Custom	Document Number: Azalia ALC3227	Rev: 1A
	Date: Tuesday, March 12, 2013	Sheet 27 of 43	

USB3.0 X 2/USB2.0 COMBO



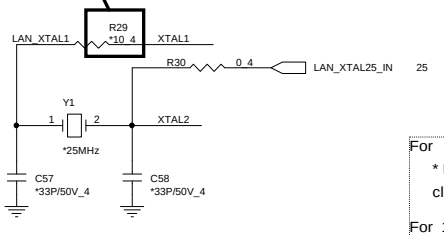
COMBO JACK



SI reserve for ESD

NB5	PROJECT : R7X Quanta Computer Inc.	
	Size: Custom Document Number: USB/Audio JacK	Rev: 1A
	Date: Tuesday, March 12, 2013	Sheet 28 of 43

For EMI 0 ~ 22 ohm

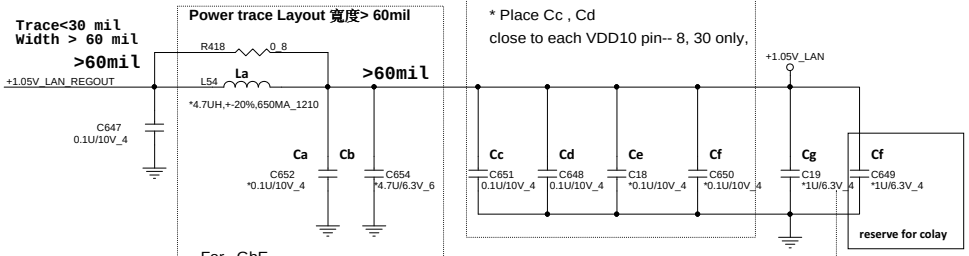


For GbE
* Place Cc,Cd,Ce,Cf close to each VDD10 pin-- 3, 8, 22, 30

For 10/100 NA Ce,Cf
* Place Cc , Cd close to each VDD10 pin-- 8, 30 only,

Trace<30 mil
Width > 60 mil
>60mil

Power trace Layout 寬度> 60mil

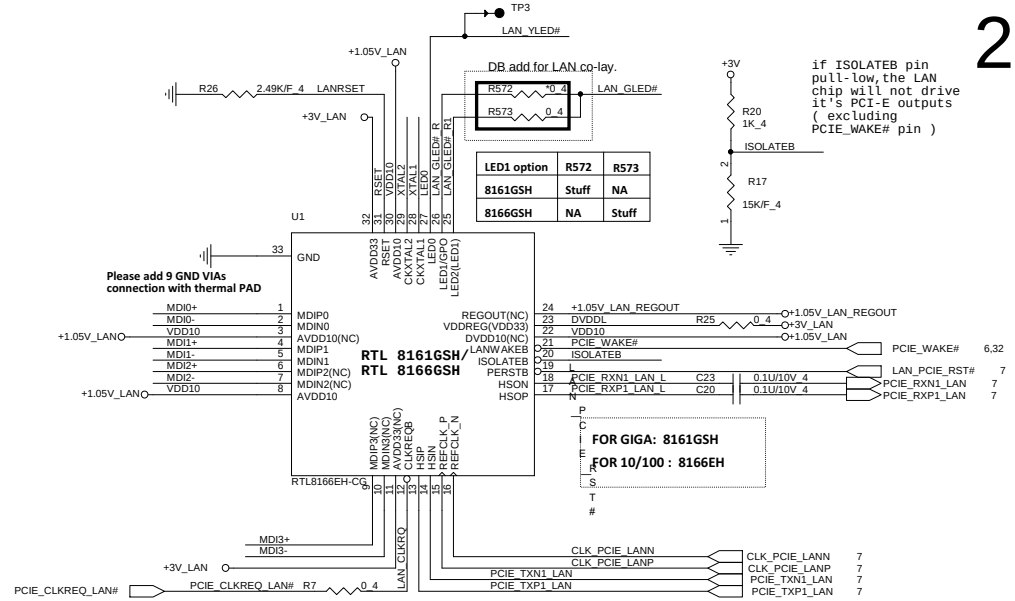


For GbE
Stuff La, Ca ,Cb

For 10/100
NA: La, Ca ,Cb

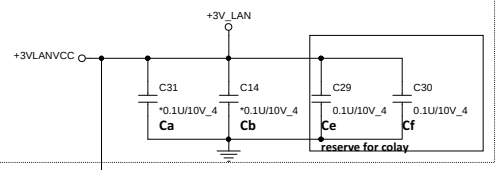
For GbE
* Place Cg close to each VDD10 pin-- 22 (reserve)

For 10/100
* Place Cf close to each VDD10 pin-- 30 (reserve)

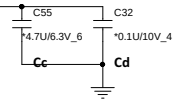


For 10/100
* Stuff Ce and Cf only, close to each VDD33 pin-- 23, 32

For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



* Place Cc and Cd close to each VDD33 pin-- 23, 32

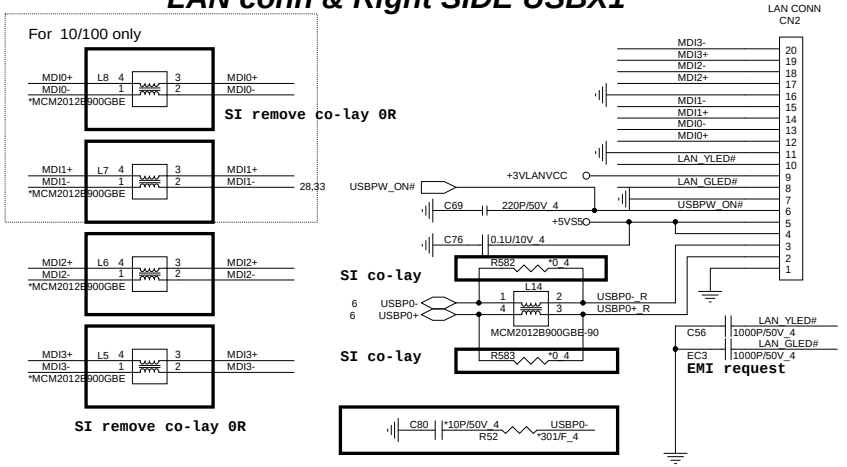


Remove For Not Using SWR mode

For GIGA
Stuff Cc ,Cd

For 10/100
NA: Cc, Cd

LAN conn & Right SIDE USBX1



2,4,6,8,9,10,11,12,22,23,24,25,26,27,30,31,32,33,41,42,43 +3V
25,41 +3VLANVCC

NB5

PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL 8105E/RJ45	1A

Date: Tuesday, March 12, 2013 Sheet 29 of 43

KEYBOARD Con.

33 MY[0..17] MY[0..17]
33 MX[0..7] MX[0..7]

SATA_LED

8 SATA_LED#
8 ACC_LED#
R396 200/F_6
R394 39_6
SATA_R_LED1
LED1
LED 3P WHITE/AMBER
(Amber)
+3V

PV remove C626,C634

CN5

MX1 MX7 MX6 MX9 MX4 MX5 MY0 MX2 MX3 MY5 MY1 MX0 MY2 MY4 MY7 MY8 MY6 MY3 MY12 MY13 MY14 MY11 MY10 MY15 MY16 MY17

KB CONN
DFFC32FR038
50698-03201-001-32p-l

33 CAPSLED#
R172 200/F_6
R179 200/F_6
+3V
CAPSLED# R
MUTE_LED_CNTL_R
WIRELESS_ON_R
WIRELESS_OFF_R

27 MUTE_LED_CNTL
Q7
2N7002K
R158
10K/F_4

SI, add Mute LED feature

KEYBOARD PULL-UP

RP2
+3VPCU
MY6 MY3 MY12 MY13 MY15 MY10 MY11 MY14
*10P8R-8.2K

RP1
+3VPCU
MY9 MY0 MY5 MY1 MY8 MY7 MY4 MY2
*10P8R-8.2K

R167 *8.2K_4 MY16
R168 *8.2K_4 MY17

MY5 C119 *220P/50V_4
MY6 C158 *220P/50V_4
MY3 C159 *220P/50V_4
MY7 C142 *220P/50V_4
MY8 C143 *220P/50V_4
MY9 C92 *220P/50V_4
MY10 C211 *220P/50V_4
MY11 C196 *220P/50V_4
MY1 C124 *220P/50V_4
MY2 C132 *220P/50V_4
MY4 C133 *220P/50V_4
MY0 C112 *220P/50V_4
MX4 C109 *220P/50V_4
MX6 C93 *220P/50V_4
MX3 C120 *220P/50V_4
MX2 C113 *220P/50V_4
MX7 C88 *220P/50V_4
MX0 C123 *220P/50V_4
MX5 C108 *220P/50V_4
MX1 C89 *220P/50V_4
MY12 C175 *220P/50V_4
MY13 C176 *220P/50V_4
MY14 C195 *220P/50V_4
MY15 C212 *220P/50V_4
MY16 C221 *220P/50V_4
MY17 C235 *220P/50V_4

PWR_LED

+3VPCU
R398 39_4
LED2
3P WHITE LED
PWRLED_RIGHT# 33

PV remove C638

C632 SATA_LED# 1000P/50V_4
C637 PWRLED_RIGHT# 1000P/50V_4

PV change from from PWR_LED# to PWRLED_RIGHT#

+5V +3V
R178 1K/F_4
R187 *200_4
R186 *200/F_6
Q8 DRC5144E0L
33 WIRELESS_ON
WIRELESS_ON_R

+5V
R193 1K/F_4
R190 *200/F_6
Q9 DRC5144E0L
33 WIRELESS_OFF
WIRELESS_OFF_R

POWER BOTTON CONNECT

100mA

C95 *4.7U/6.3V_6
C102 1U/10V_4
C101 0.1U/10V_4
+3VPCU
CN4
33 LID_EC#
33 NBSWON1#
33 PWR_LED#
R85 *0_4/S
PWR_LED_R#
pv change to shortpad
PWR BTN CONN
DFFC06FR062
88513-0601-6P-L-SMT

1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

C103 PWR_LED# 0.1U/10V_4
C100 LID_EC# 0.1U/10V_4
C99 NBSWON1# 0.1U/10V_4

TOUCH PAD Con.

+3VSUS
R290 4.7K_4 TP_SMB_CLK
R297 4.7K_4 TP_SMB_DATA

change to +3VSUS
close conn

+3VSUS
R285 4.7K_4 TPCLK
R284 4.7K_4 TPDATA

C430 10P/50V_4
33 TPCLK
33 TPDATA
L35 TB160808B470N-001(47,300MA)
L34 TB160808B470N-001(47,300MA)
TPCLK-1
TPDATA-1
C440 10P/50V_4
TP_SMB_DATA
TP_SMB_CLK
CN6
TOUCH PAD CONN
DFFC06FR062
88513-0601-6P-L-SMT
25 mils
C427 *10P/50V_4
C426 *10P/50V_4
+3VSUS
C439 0.1U/10V_4

+3VSUS
Q12
TP_SMB_CLK
TP_SMB_DATA
SMB_PCH_CLK
SMB_PCH_DAT
2N7002DW

PV , HP request Image sensor
SMBUS reserve to PCH

7,25,32,33,34,35 +3VPCU
8,24,25,26,27,31,32,41 +5V
41 +3VSUS
2,4,6,8,9,10,11,12,22,23,24,25,26,27,29,31,32,33,41,42,43 +3V

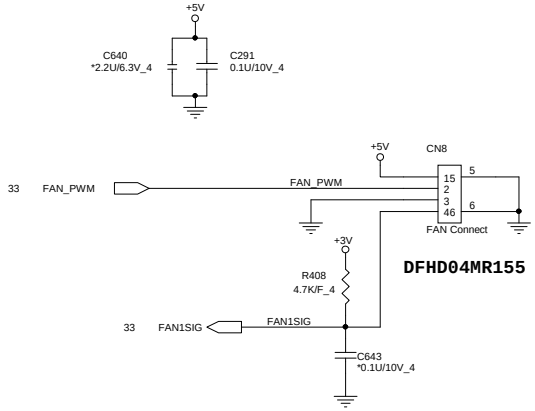
NB5

PROJECT : R7X
Quanta Computer Inc.

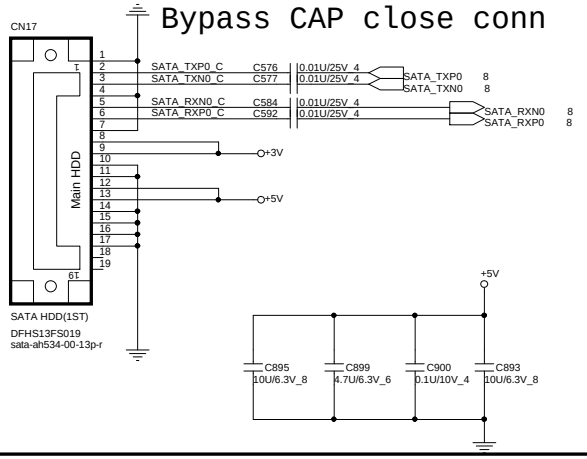
Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A

Date: Tuesday, March 12, 2013 Sheet 30 of 43

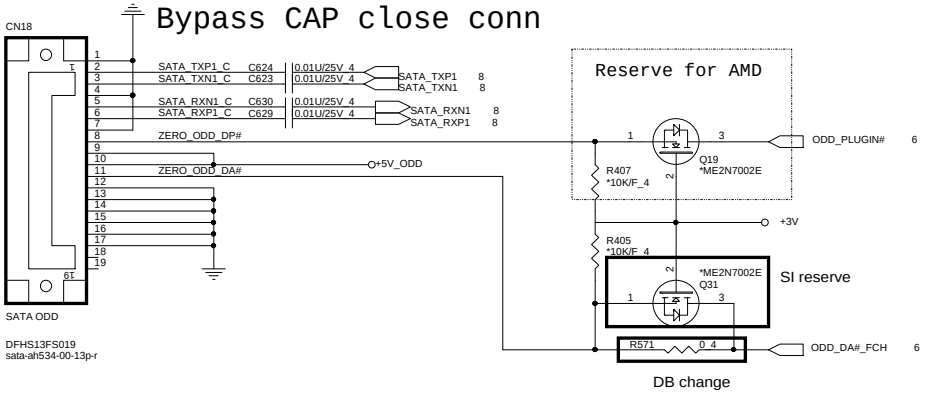
CPU FAN



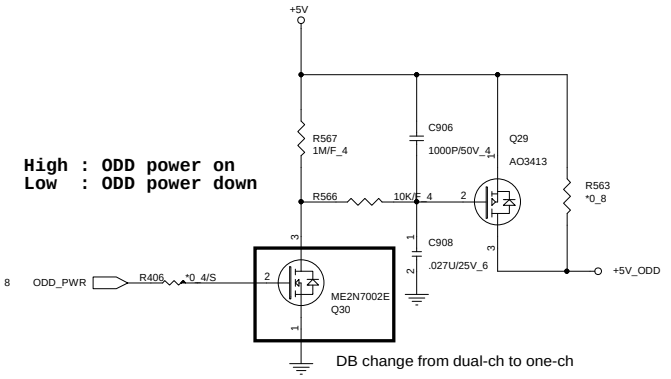
SATA HDD CONNECTOR

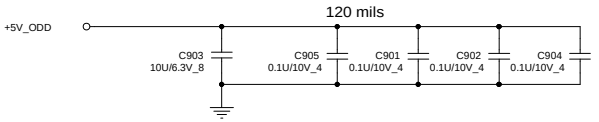


SATA ODD CONNECTOR



High : ODD power on
Low : ODD power down





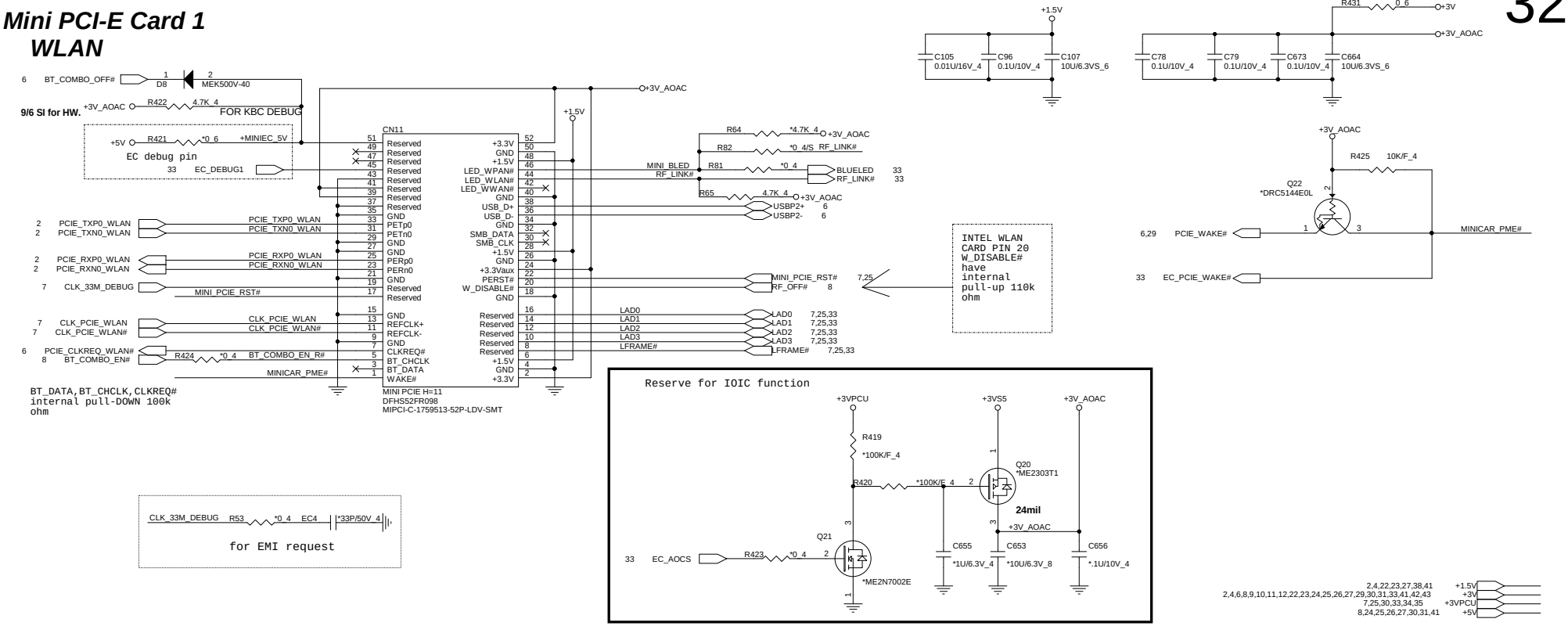
NB5

PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A

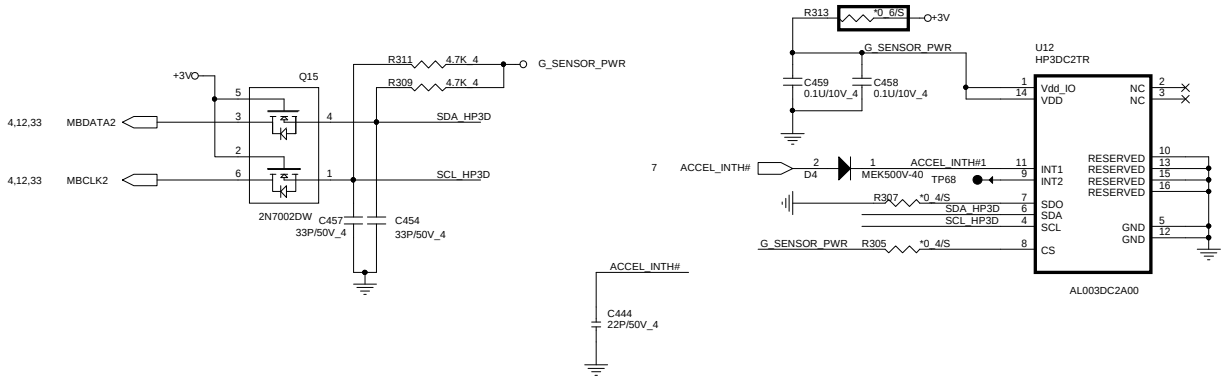
Date: Tuesday, March 12, 2013 Sheet 31 of 43

Mini PCI-E Card 1
WLAN



Accelerometer Sensor

PV change to shortpad



NB5	PROJECT : R7X Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCIE CONN & G-sensor	Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 32 of 43	

ITE pin 100 , 104 , 106 default can not pull up to +3VPCU it will cause chip into test mode

+3VPCU CAP close to EC pin

Smart adapter Type check

Change to 1SS355 as Current loss

D11 1SS355

DGPU Thermal protect

*ME2N7002E

4M SPI EC ROM

A25QE32M-F/Q AKE39FN0N01 SOIC8-8-1_27

128K byte SPI EC ROM

*DFHS08FS023 SOIC8-6-1_27

ICT need TP2675 size test point

TP place on top lay for ICT request

pv change to shortpad

IO Thrm Protect

For 65 degree, 1.8v limit, (SW)

For 75 degree, 1.2v limit, (HW)

Adapter select

Hi ==> DIS/SG
Low ==>UMA

Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

Vender	Size	P/N
AMIC	4M	AKE39ZN0800
EON	4M	AKE39ZN0Q03
WINBOND	4M	AKE39FN0N01
Socket		DFHS08FS023

For +VIN noise

DB reserve for BIOS test

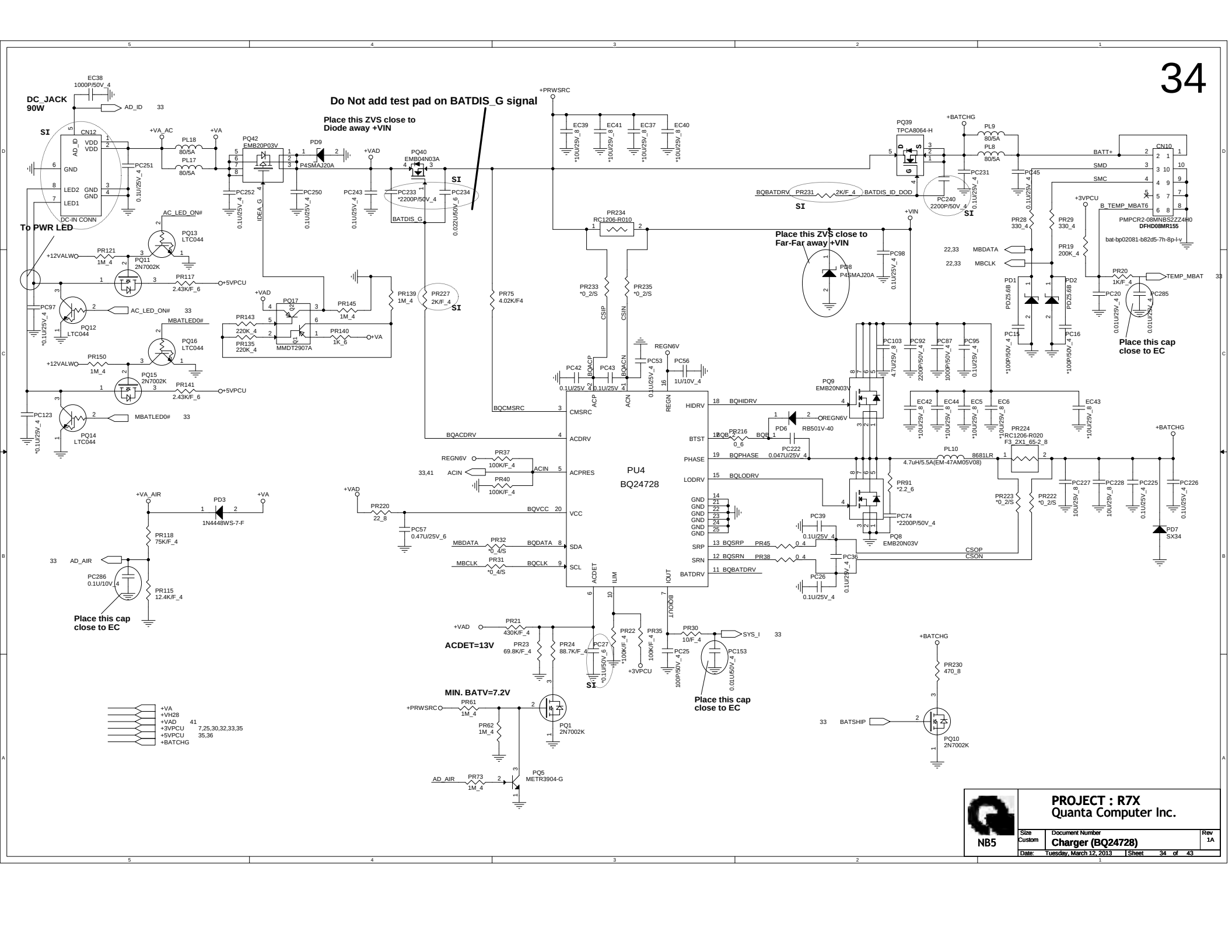
Add G-sensor SMBUS signal

PV , change to short pad

DB Change PV add for control PWR_LED

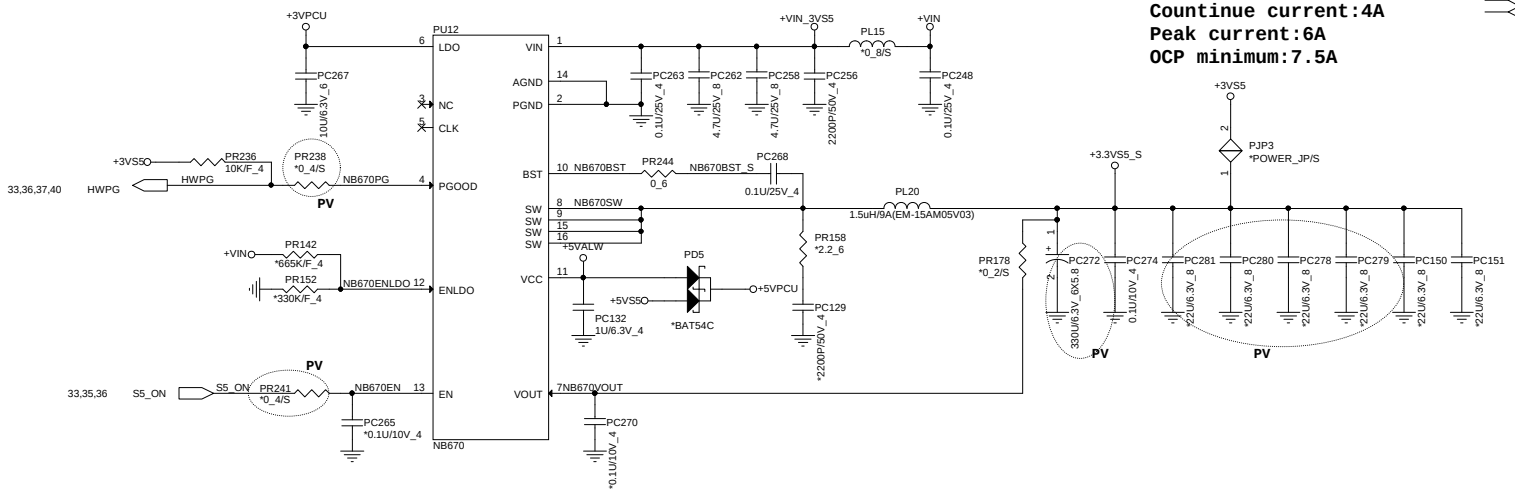
PROJECT :	R7X
Quanta Computer Inc.	
Size: Custom	Document Number: EC (IT8518E/HX)/ROM
Rev: 1A	
Date: Tuesday, March 12, 2013	Sheet 33 of 43

NB5

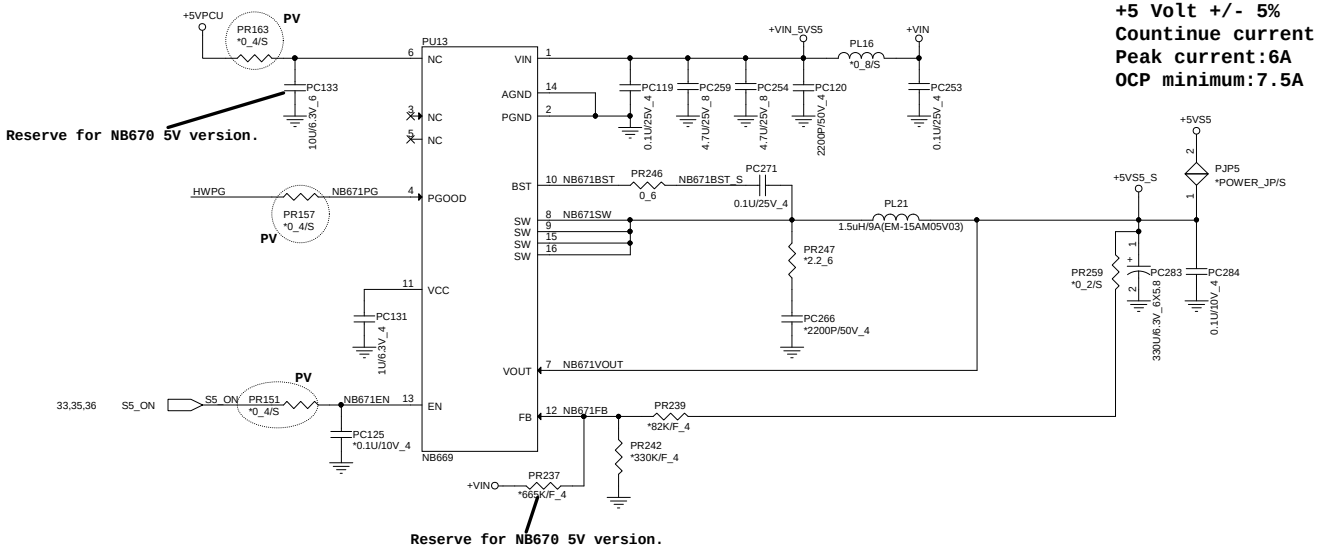

DC_JACK 90W
CN12
DC-IN CONN
Do Not add test pad on BATDIS_G signal
Place this ZVS close to Diode away +VIN
Place this ZVS close to Far-Far away +VIN
To PWR LED
PU4
BQ24728
ACDET=13V
MIN. BATV=7.2V
Place this cap close to EC
Place this cap close to EC
Place this cap close to EC
Place this cap close to EC
PROJECT : R7X
Quanta Computer Inc.
NB5
Charger (BQ24728)
Tuesday, March 12, 2013
Sheet 34 of 43

DC/DC +3VS5/+5VS5

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



+3VS5 4,6,8,9,10,25,32,33,36,38,41,43
+5VS5 28,29,36,37,38,39,40,41,42,43

NB5	PROJECT : R7X Quanta Computer Inc.	
Size: Custom	Document Number: 3/5VS5 (NB670/NB671)	Rev: 1A
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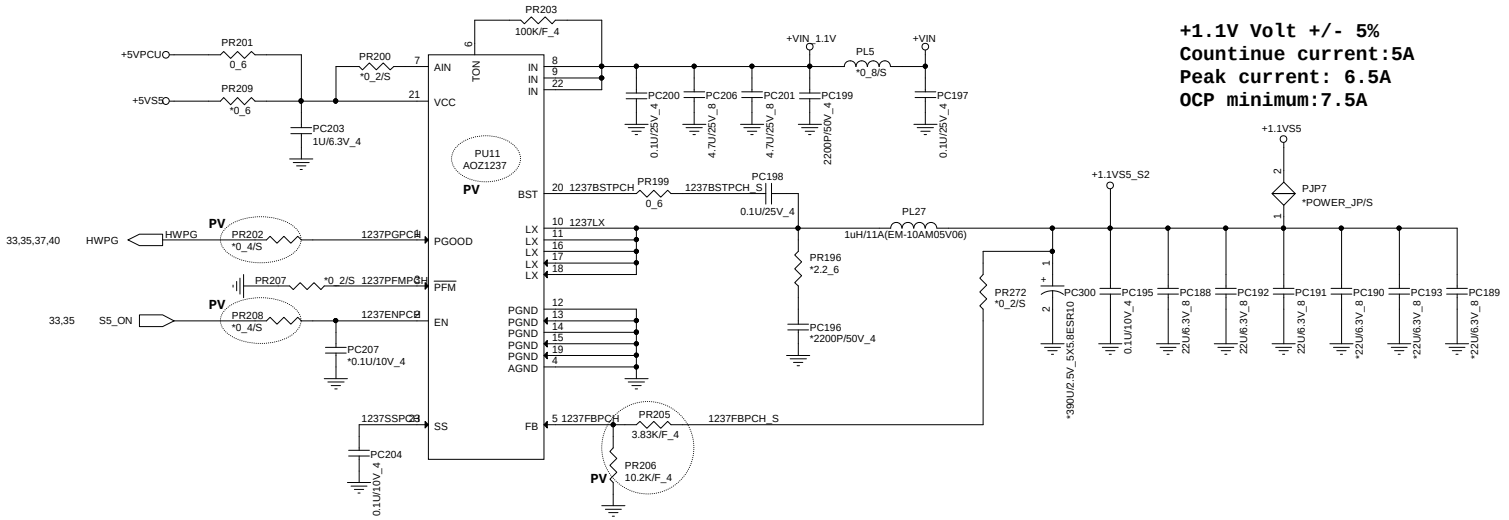
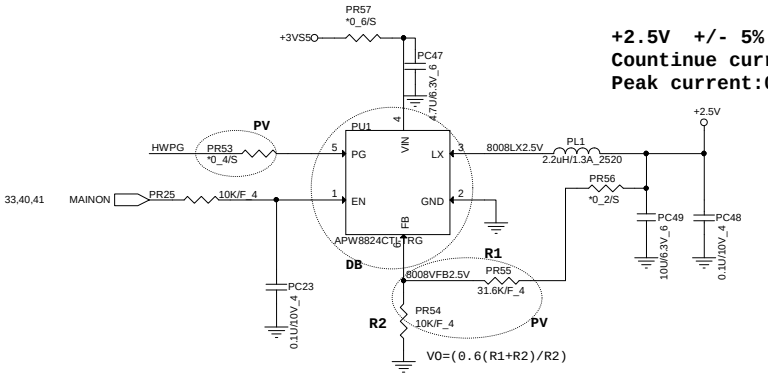


+1.1V Volt +/- 5%
Countinue current:5A
Peak current: 6.5A
OCP minimum:7.5A



+2.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A

+VIN	23,34,35,37,39,40,41,42,43
+2.5V	5
+3VS5	4,6,8,9,10,25,32,33,35,38,41,43
+5VS5	28,29,35,37,38,39,40,41,42,43
+1.1VS5	9,41
+5VPCU	34,35

NB5

PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1VS5 (AOZ1237)/2.5V	1A

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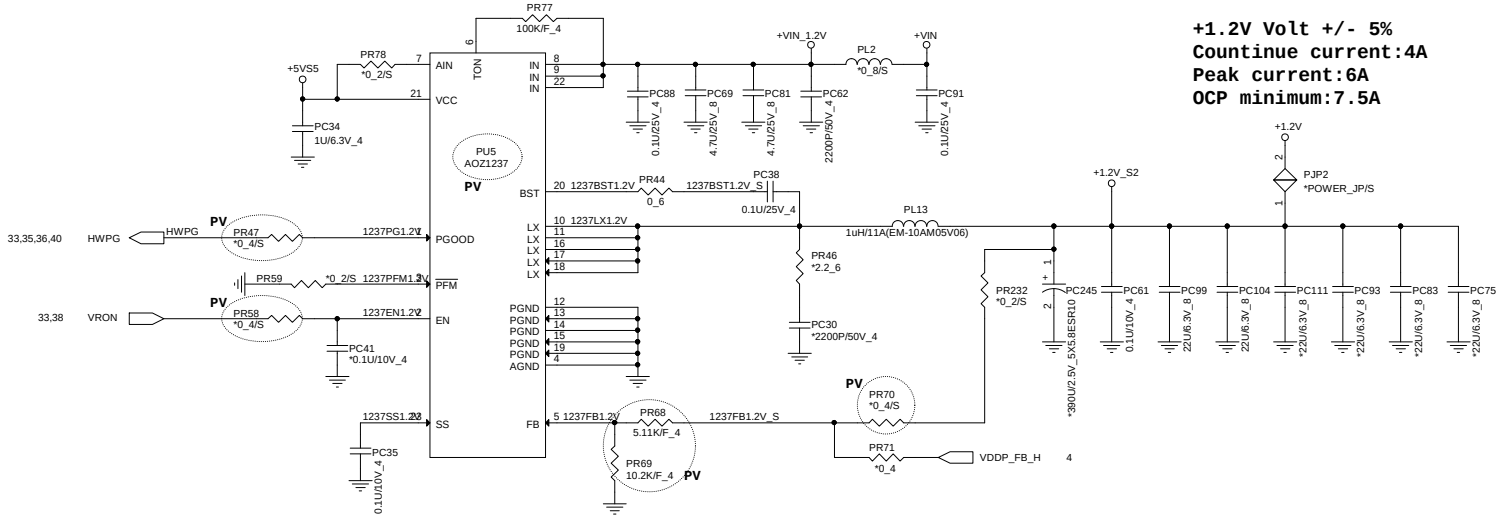
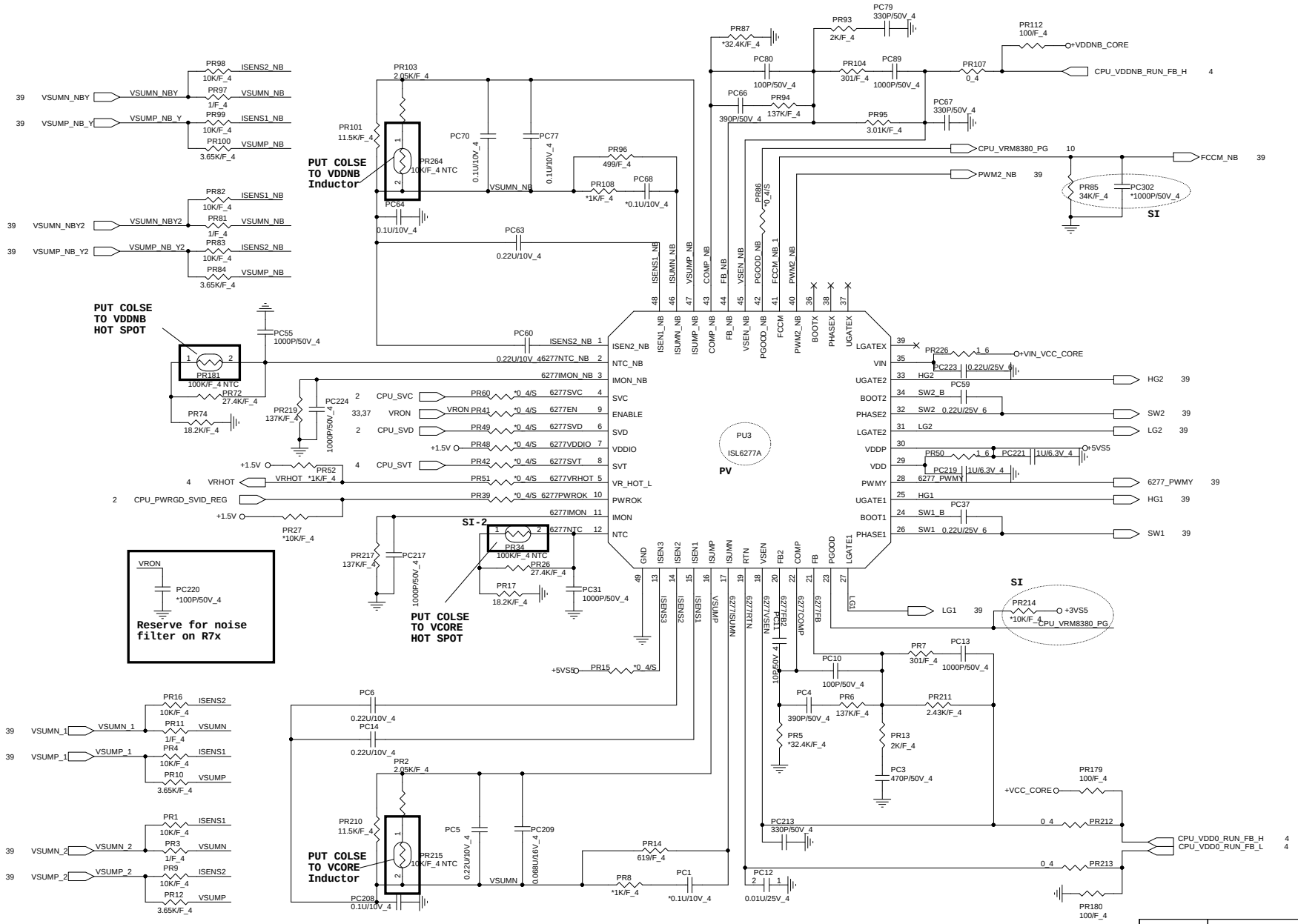
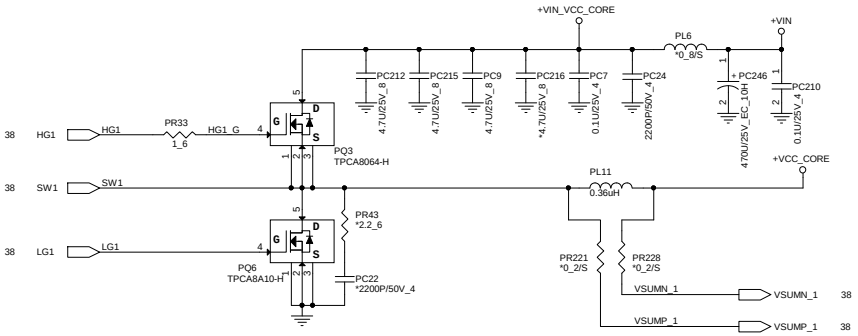
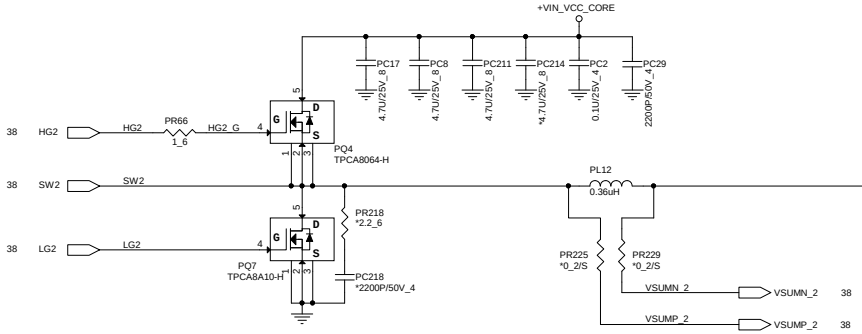


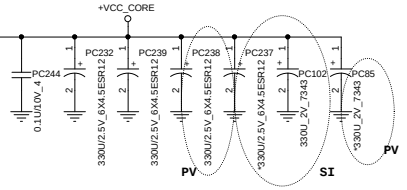
PROJECT : R7X	
Quanta Computer Inc.	
NB5	Size: Custom
Document Number: +1.2V (AOZ1237)	Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 37 of 43

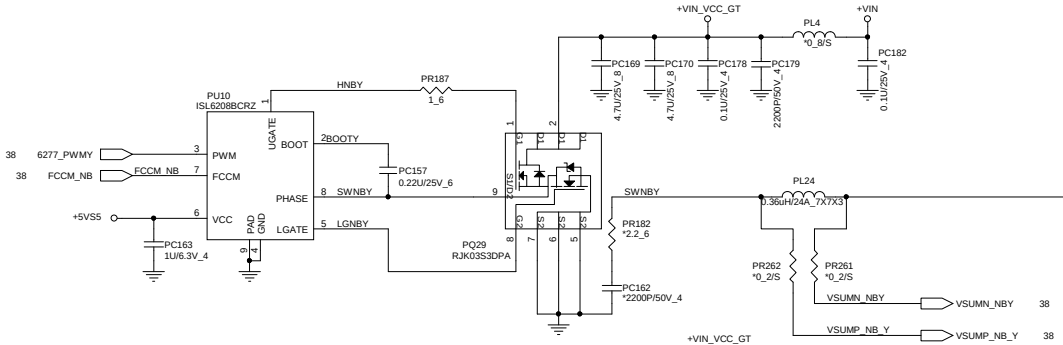

PU3
ISL6277A
PV
PUT COLSE TO VDDNB Inductor
PUT COLSE TO VDDNB HOT SPOT
PUT COLSE TO VCORE HOT SPOT
PUT COLSE TO VCORE Inductor
SI-2
SI
Reserve for noise filter on R7x
VSUMN_NB
VSUMP_NB
ISENS1_NB
ISENS2_NB
ISUMN_NB
ISUMP_NB
COMP_NB
FB_NB
VSEN_NB
PGOOD_NB
FCCM_NB_1
PWM2_NB
BOOTX
PHASEX
UGATEX
LGATEX
ISEN1_NB
ISEN2_NB
ISEN3_NB
ISUMN
ISUMP
RTN
VSEN
FB2
COMP
FB
PGOOD
LGATE1
6277IMON_NB
6277NTC_NB
6277SVC
6277EN
6277SVD
6277VDDIO
6277SVT
6277VRHOT
6277PWROK
6277IMON
6277NTC
6277_PWMY
CPU_VRM8380_PG
CPU_VDDNB_RUN_FB_H
CPU_VDD0_RUN_FB_H
CPU_VDD0_RUN_FB_L
+VDDNB_CORE
+VCC_CORE
+VIN_VCC_CORE
+5VS5
+3VS5
FCCM_NB
PWM2_NB
HG1
HG2
LG1
LG2
SW1
SW2
VRON
CPU_SVC
CPU_SVD
CPU_SVT
CPU_PWRGD_SVID_REG
VRHOT

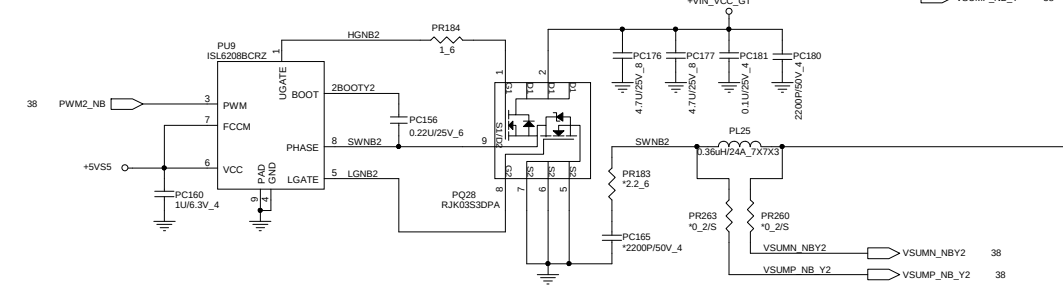




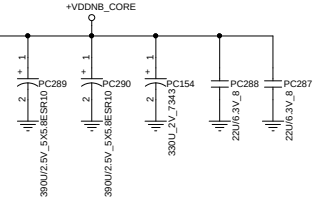
CPU CORE Volt
Countinue current:36A
Peak current:50A
OCP minimum:60A







VDDNB Volt
Countinue current:25A
Peak current:33A
OCP minimum:40A



NB5	PROJECT : R7X Quanta Computer Inc.	
	Size: Custom	Document Number: CPU Core2 (ISL6208) Rev: 1A
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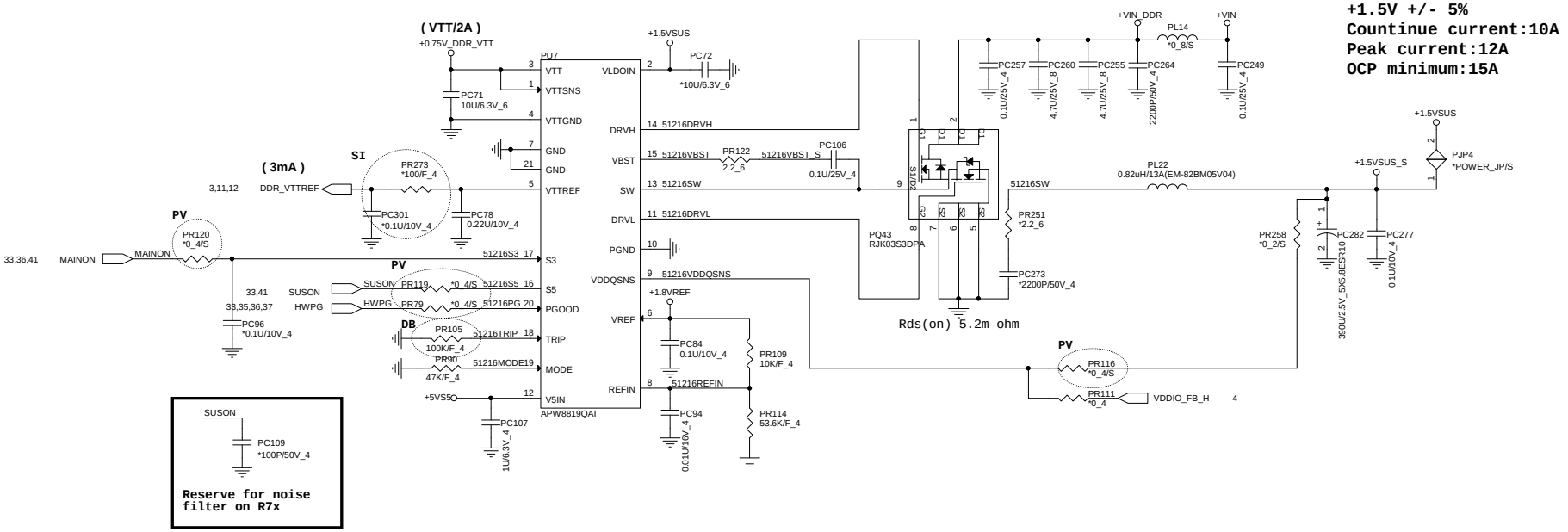
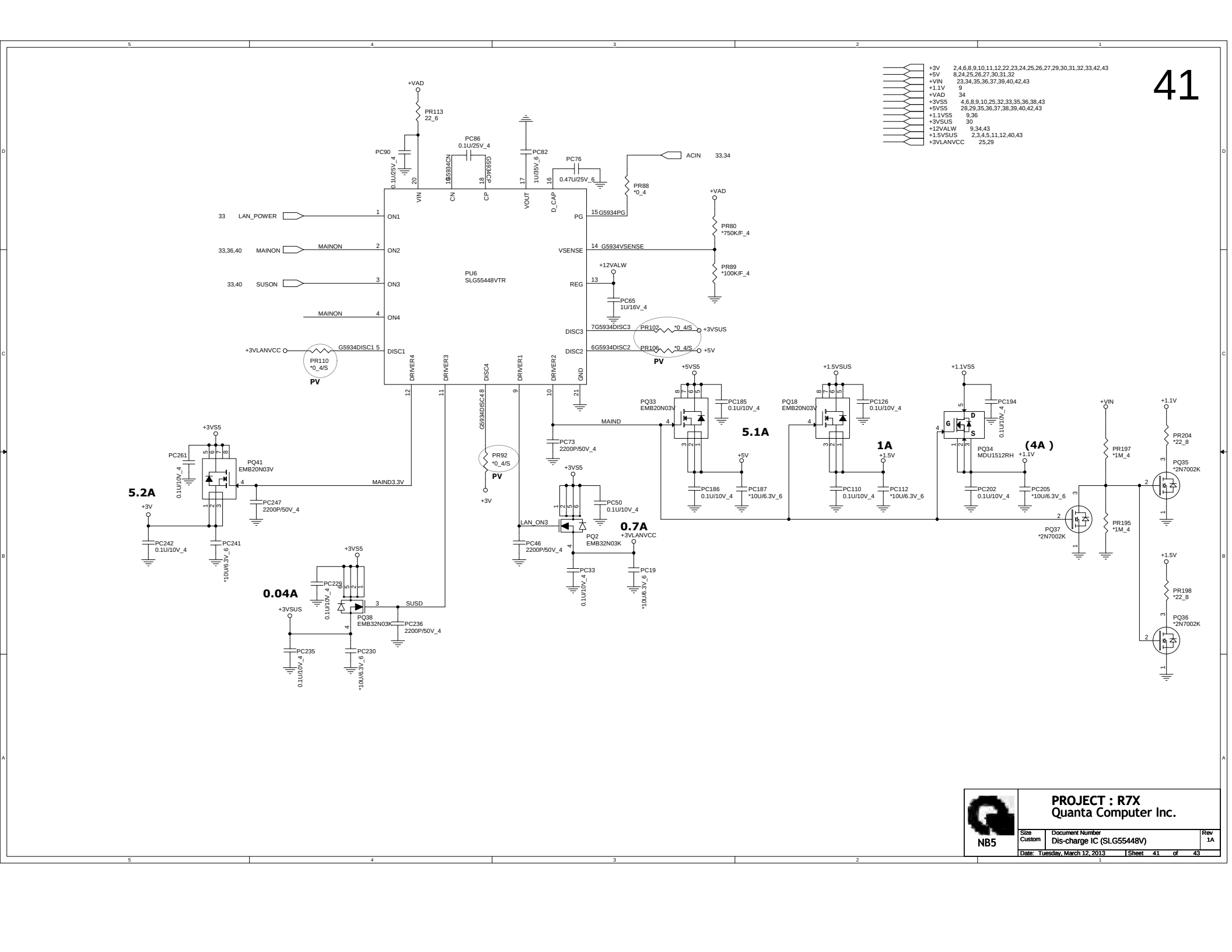


NB5	PROJECT : R7X Quanta Computer Inc.	
Size: Custom	Document Number: DDR3L(TPS51216)	Rev: 1A
Date: Tuesday, March 12, 2013	Sheet 40 of 43	



NB5	**PROJECT : R7X** Quanta Computer Inc.
Size: Custom	Document Number: Dis-charge IC (SLG55448V) — Rev: 1A
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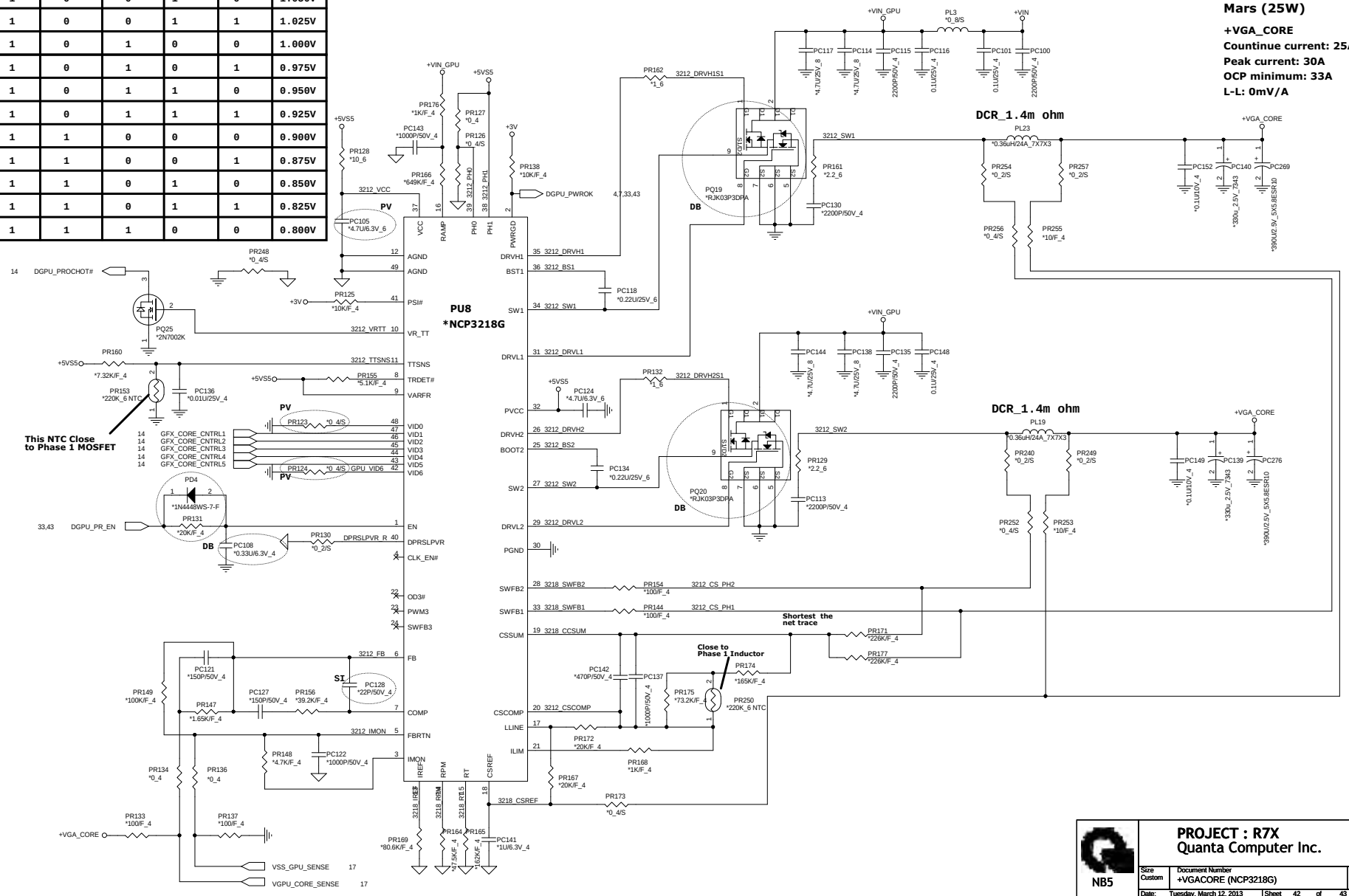
VGA Core

GPIO10	GPIO12	GPIO16	GPIO20	GPIO15	Mars XT
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V

Default

Mars (25W)

+VGA_CORE
Countinue current: 25A
Peak current: 30A
OCP minimum: 33A
L-L: 0mV/A



NB5	PROJECT : R7X Quanta Computer Inc.	
Size: Custom	Document Number: +VGACORE (NCP3218G)	Rev: 1A
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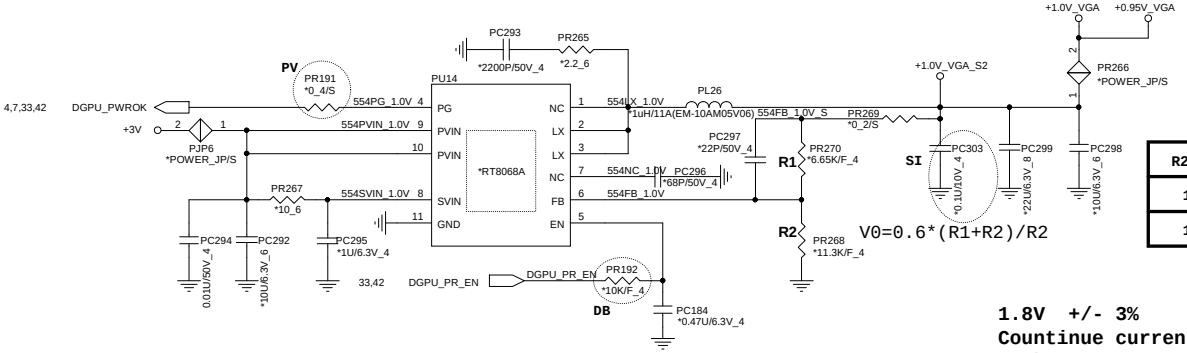
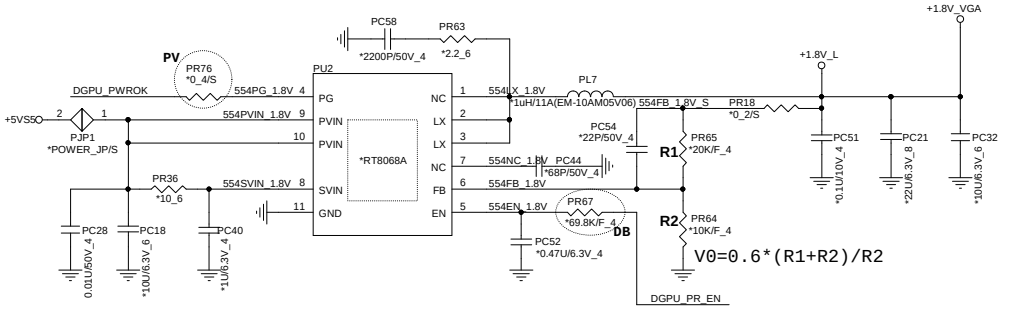
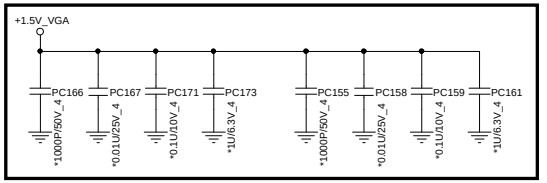
+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A

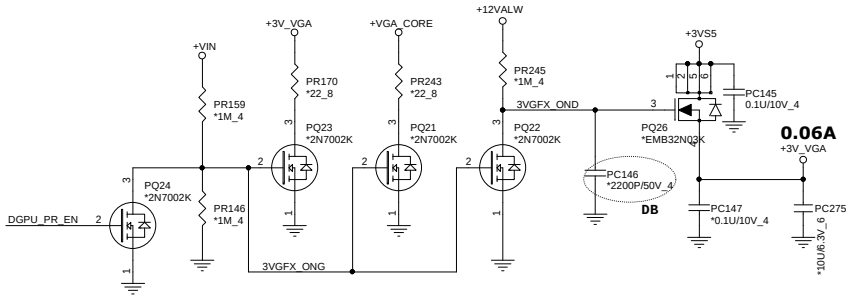


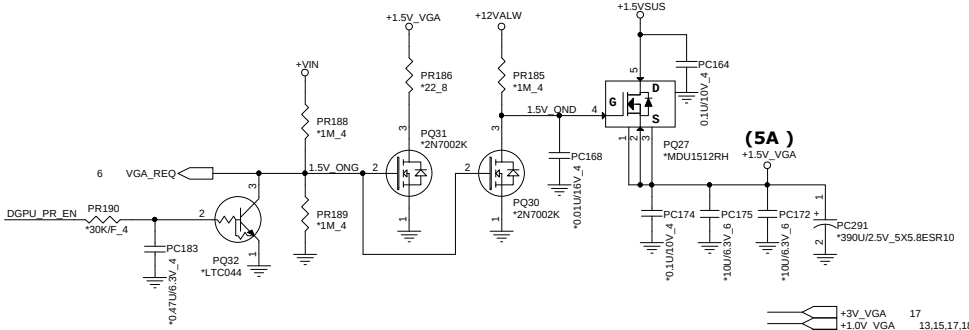
R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V

1.8V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A









PROJECT : R7X
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V_VGA/1.8V_VGA/3V_VGA	1A
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NB5