



LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

BQ24728H
System Charge Power (+BATCHG)

SY8208B / SY8208C
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

RT8231BGQW
System Memory Power (+1.35VSUS/
+0.65V DDR VTT)

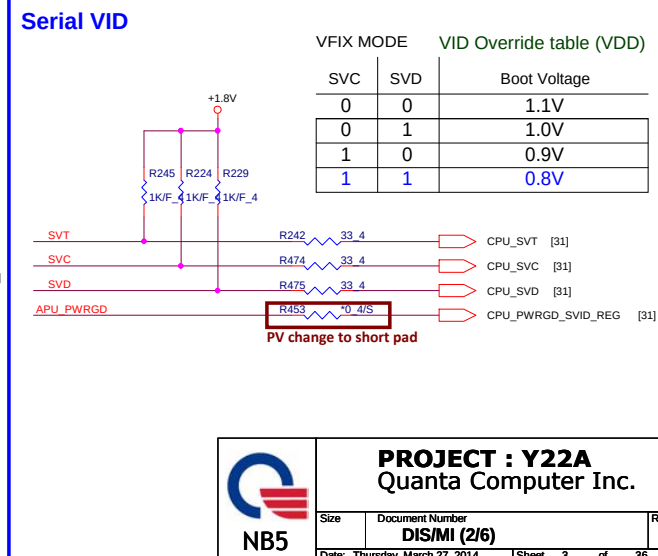
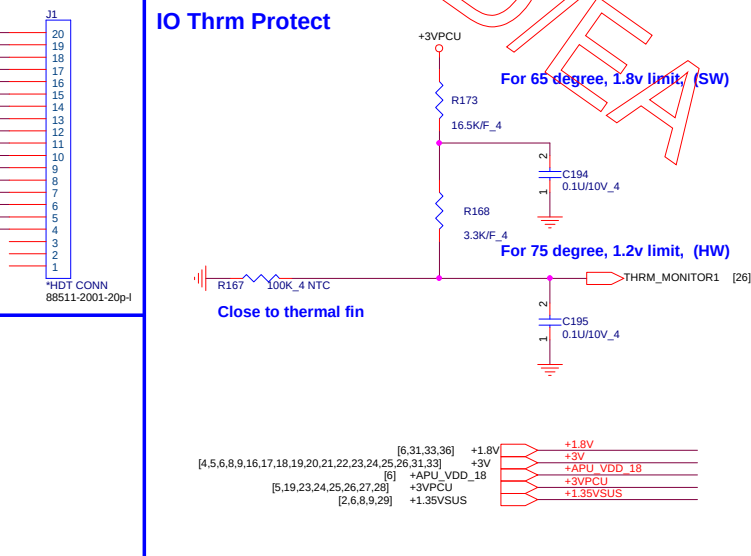
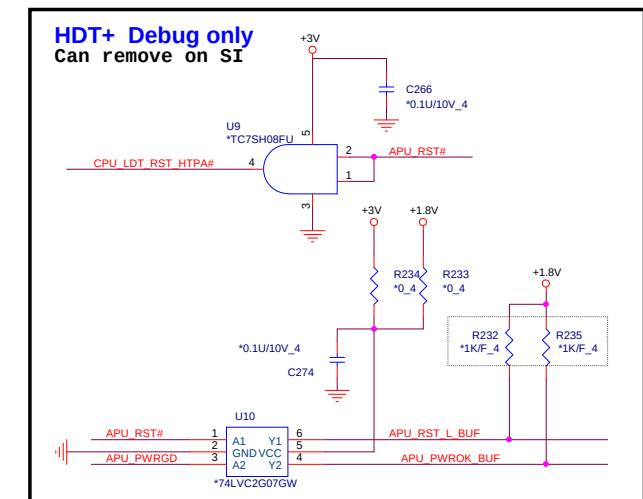
ISL6277A / ISL6208BCRZ
Processor Power
(+VCC CORE/+VDDNB CORE)

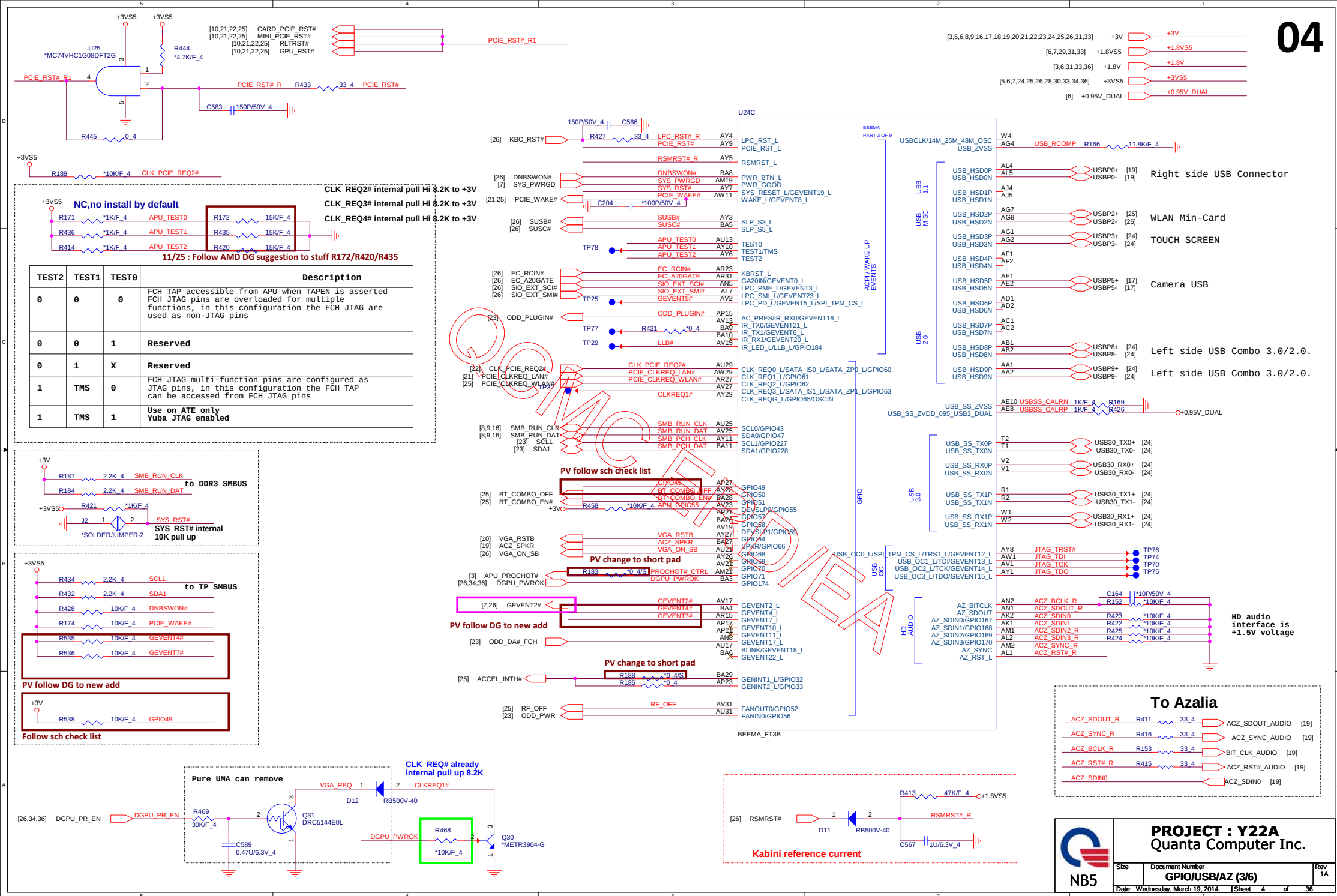
AOZ1267QI-02 / APW8824
Processor Power
 (+0.95V/++0.95VS5/+1.5VS5)

RT8899AGQW
DGPU Power
 (+VGA CORE/+1.35V VGA)

APW8804 / APL3523A
DGPU Power
 (+0.95V VGA/+3V VGA/+1.8V VGA)







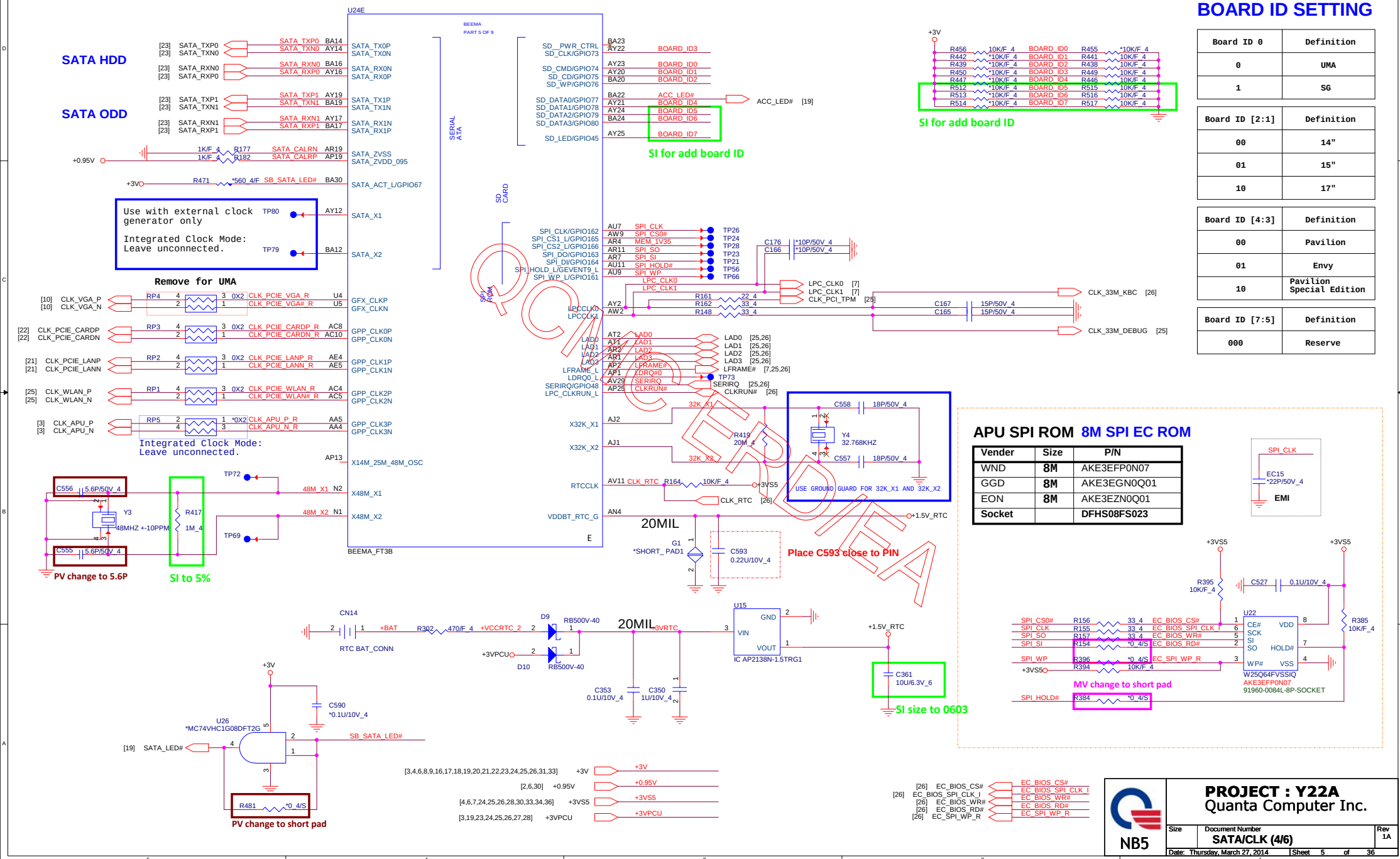
BOARD ID SETTING

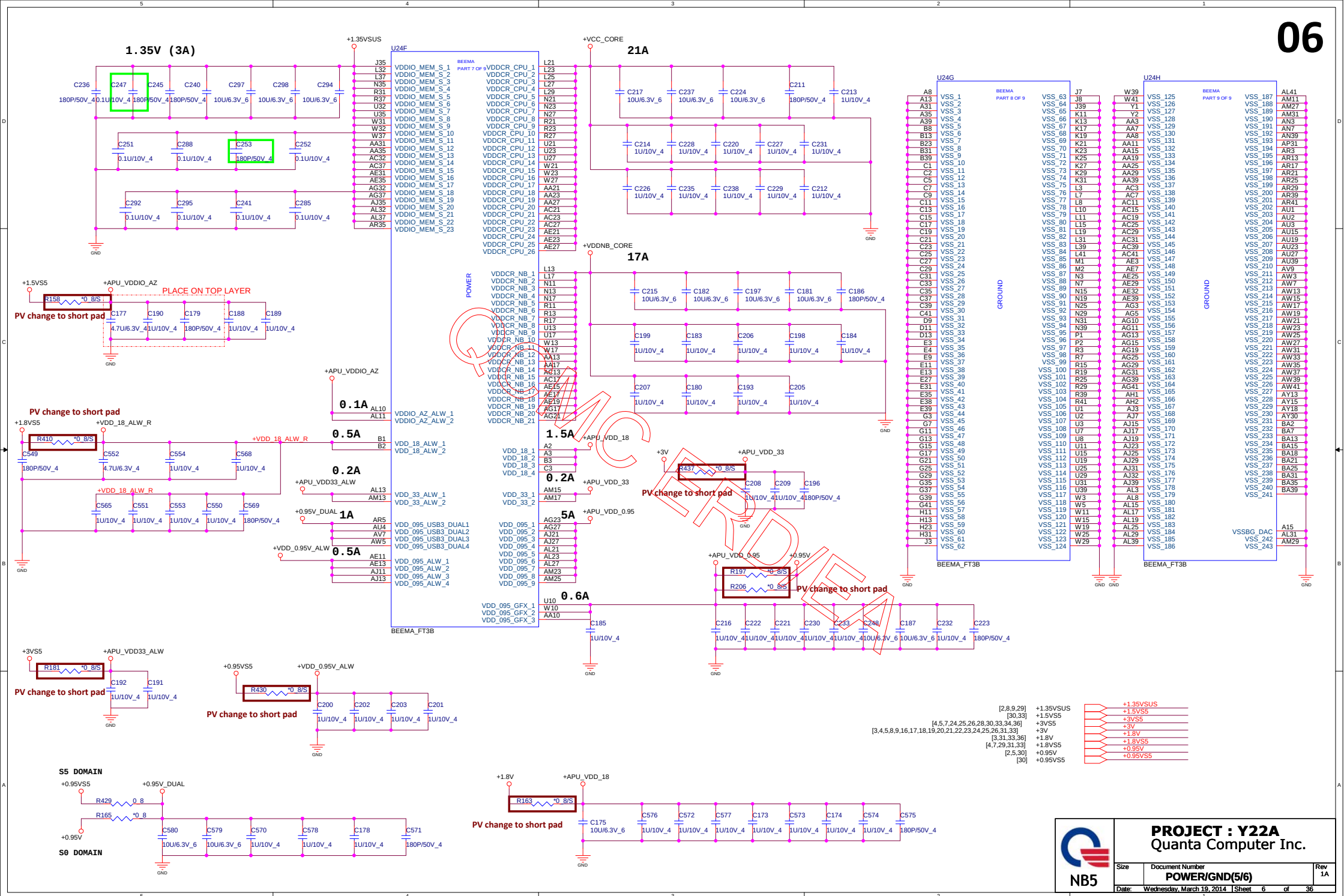
Board ID 0	Definition
0	UMA
1	SG

Board ID [2:1]	Definition
00	14"
01	15"
10	17"

Board ID [4:3]	Definition
00	Pavilion
01	Envy
10	Pavilion Special Edition

Board ID [7:5]	Definition
000	Reserve

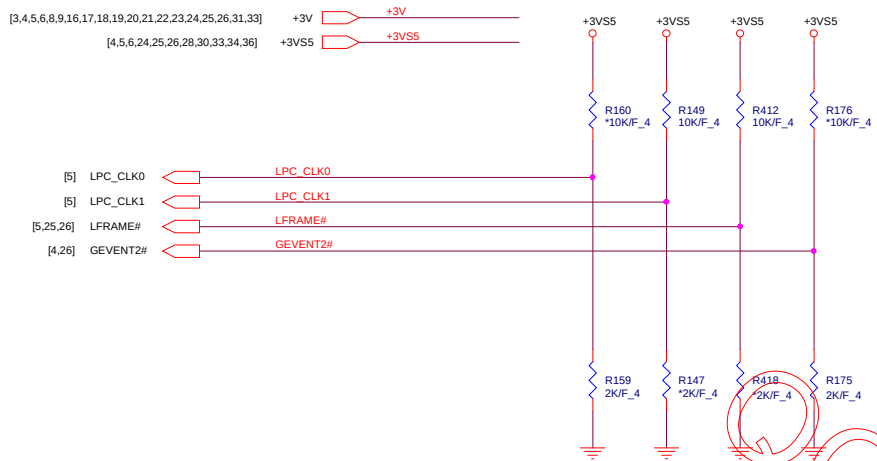






STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

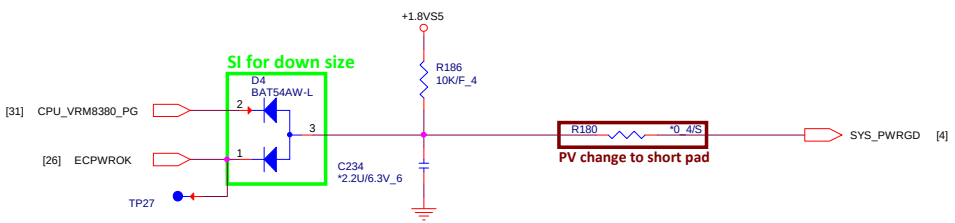


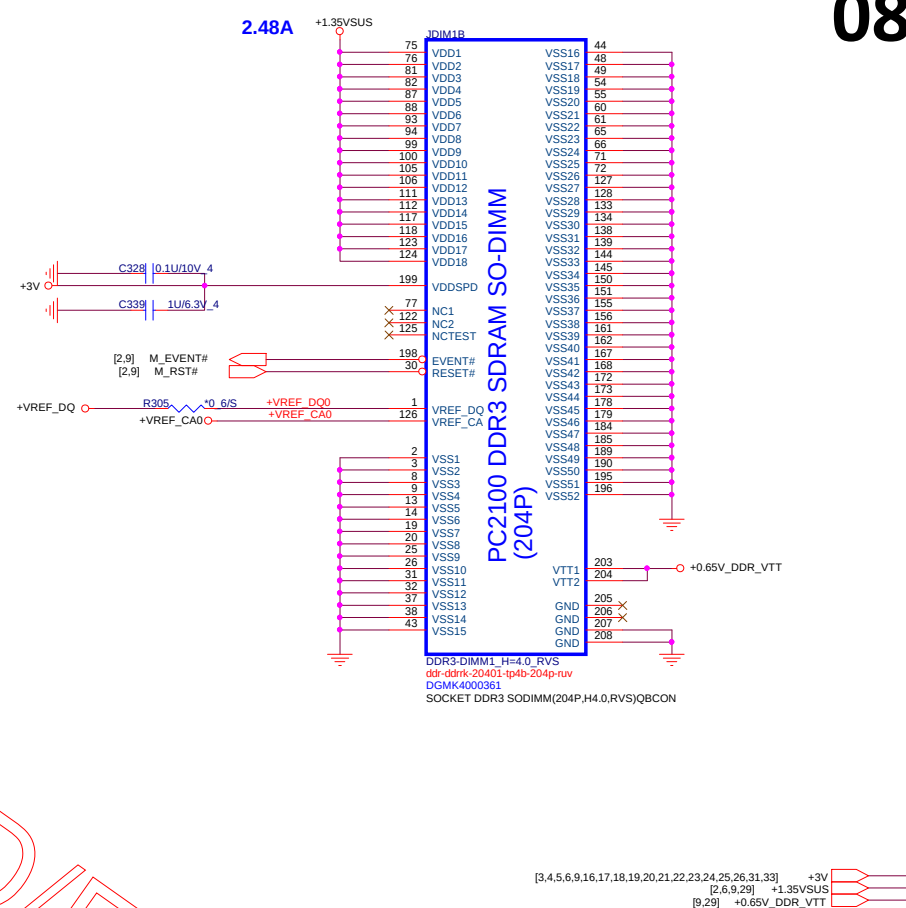
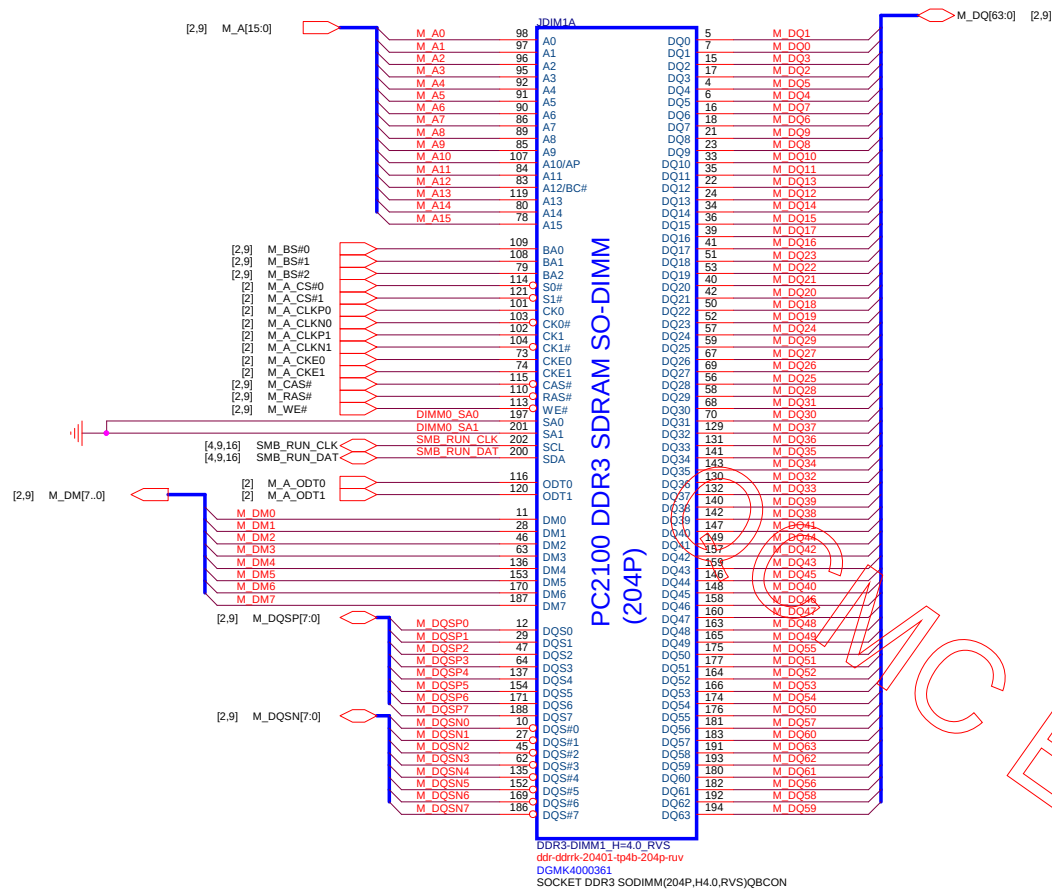
REQUIRED STRAPS

PULL					LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
					BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
HIGH								
LOW					BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT

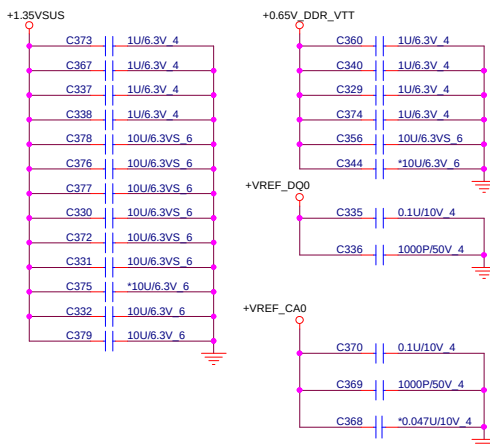
DEBUG STRAPS

SYS_PWRGD

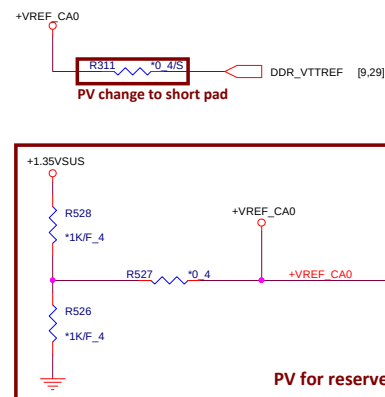
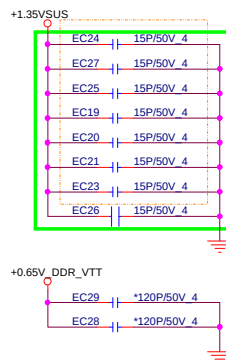




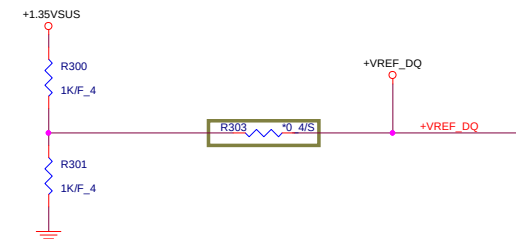
Place these Caps near So-Dimm0.

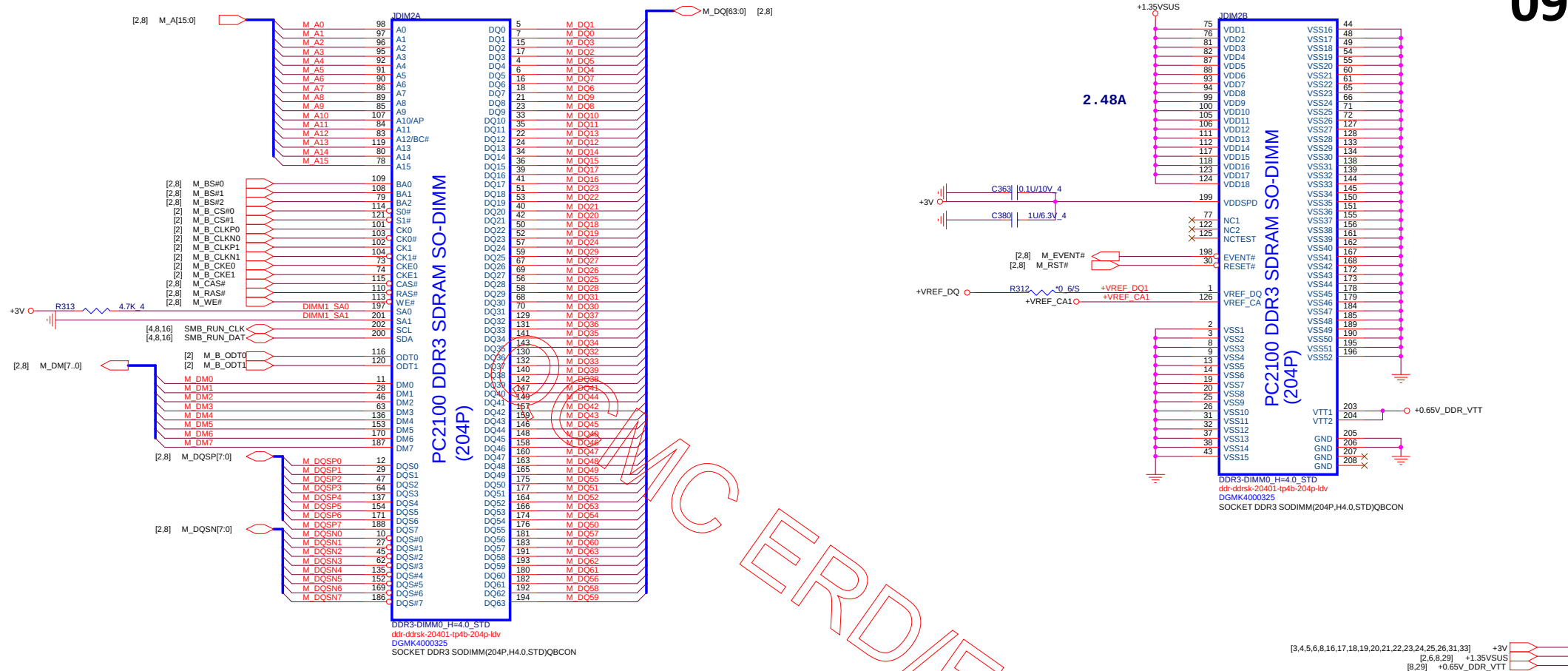


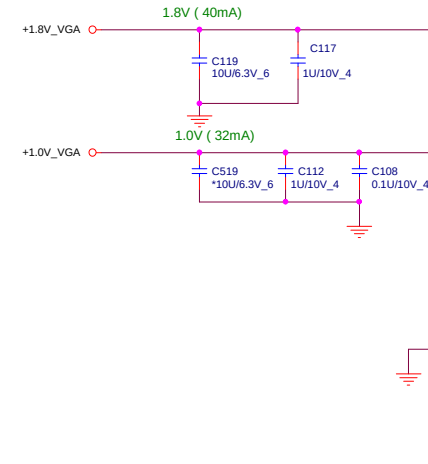
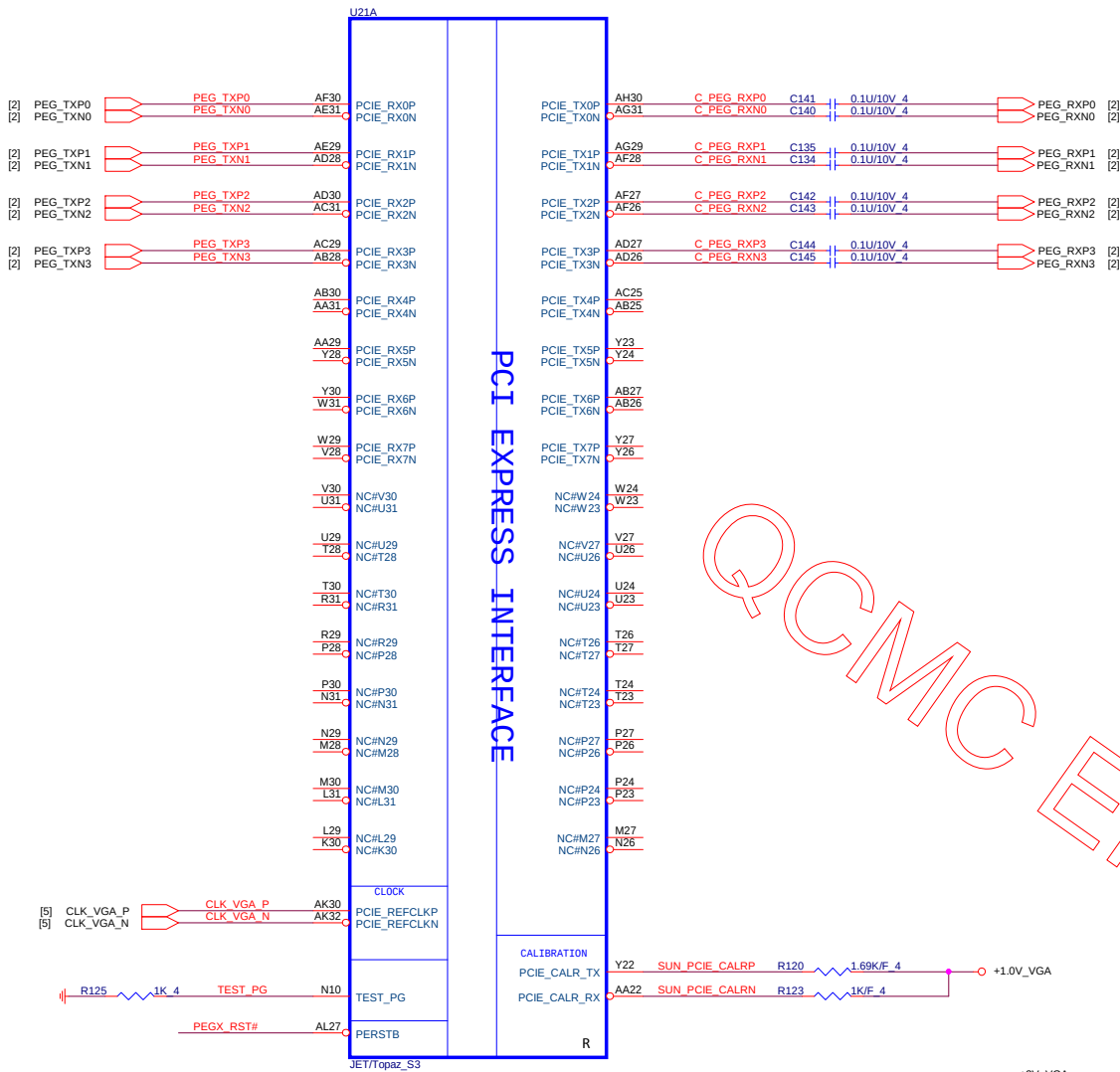
For EMI RESERVE



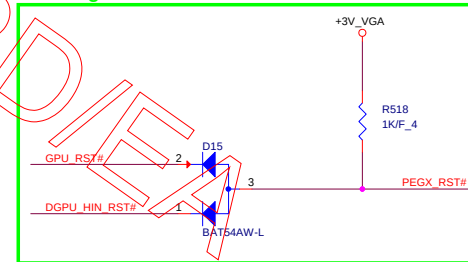
Reserved for AMD suggest



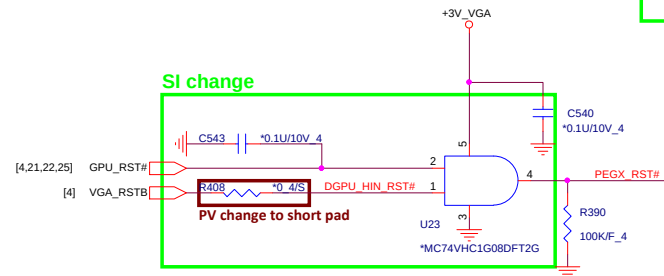




SI change



SI change



[11,13,36] +3V_VGA

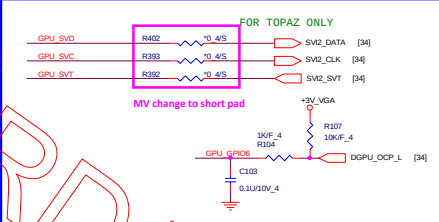
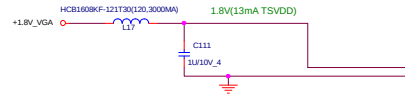
[11,13,34,36] +1.8V_VGA

[13,36] +1.0V_VGA



PROJECT : Y22A
Quanta Computer Inc.

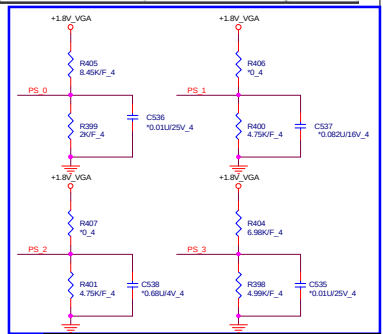
Size	Document Number	Rev
	TOPAZ S3 PCIE/DP power	1A
Date: Thursday, March 27, 2014	Sheet 10 of 36	



C (pF)	Bbts(3,4)
580	00
82	01
10	10
NC	11

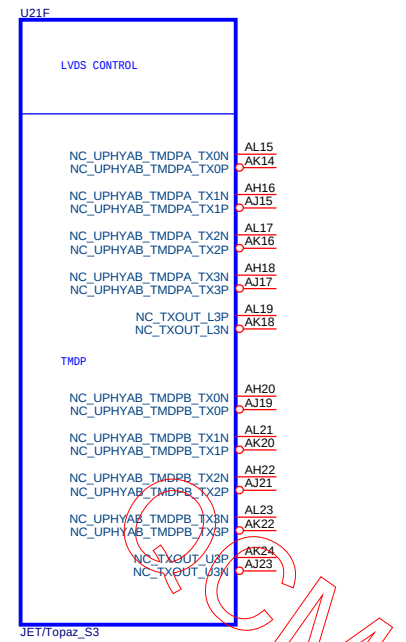
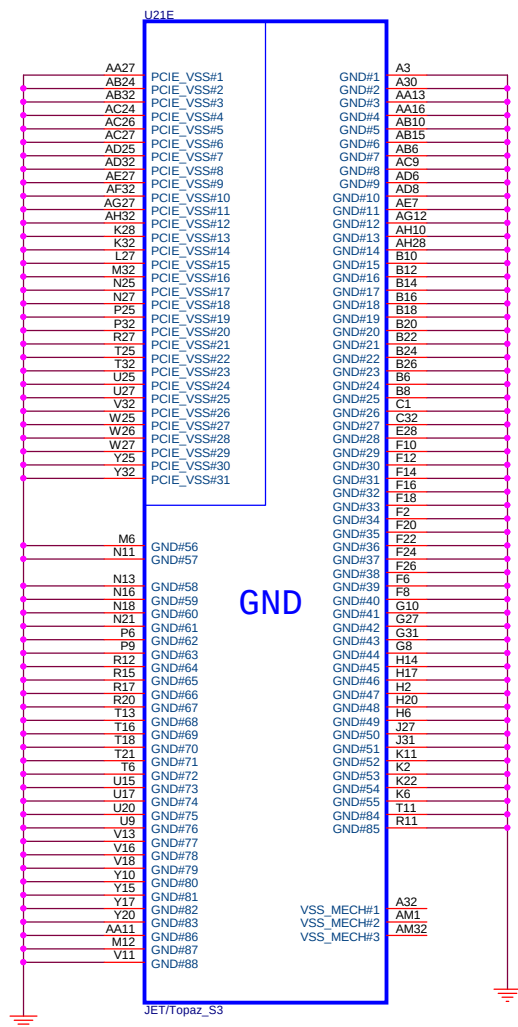
R_u (Ω)	R_pt (Ω/m)	Bbts(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5630	101
3400	10000	110
4750	NC	111

MLPS Bit	Strap Name	Description	Recommended Settings
PS_011	ROM_CONFIG[0]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[0] defines the ROM type.	Design dependent, see the description.
PS_012	ROM_CONFIG[1]	If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[1] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 25).	
PS_013	ROM_CONFIG[2]	Reserved for internal use only. Must be 1 at reset.	
PS_041	N/A	Reserved.	1
PS_053	N/A	Reserved.	1
PS_111	STRAP_BIF_GEN1_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_121	STRAP_BIF_CLK_PN_EN	Determines whether or not the PCIe reference clock per management capability is reported in the PCI configuration space (otherwise known as CLKREQ#). 0 = The CLKREQ# power management capability is disabled 1 = The CLKREQ# power management capability is enabled	0
PS_131	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_141	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-half swing mode. 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_151	STRAP_TX_DEEMP_PN_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx de-emphasis disabled. 1 = Tx de-emphasis enabled.	Design dependent, see the description.
PS_211	N/A	Reserved.	0
PS_212	N/A	Reserved.	0
PS_231	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_241	N/A	Reserved.	1
PS_251	N/A	Reserved	1
PS_311	BOARD_CONFIG[0]	Board configuration related strapting, such as for memory ID	Design dependent, see the description.
PS_321	BOARD_CONFIG[1]		
PS_331	BOARD_CONFIG[2]		
PS_341	N/A	Reserved.	1
PS_351	N/A	Reserved.	1



PS_3[3:1]	Vendor	Type	Vendor P/N	PU	PD
000	Hynix - F (Huma)	128Mx16 *4, 990MHz	H5TC2G63FFR-11C	NC	4.75K
001	Micron - V89C/K	128Mx16 *4, 990MHz	W1J1J2M61GJ7-0939G-K	8.45K	2K
010	Samsung - E die	128Mx16 *4, 990MHz	K4W2G1646E-BC1A	4.53K	2K
011	Hynix - A die	256Mx16 *4, 990MHz	H5TC4G63AAR-11C	6.98K	4.99K
100	Samsung - D die	256Mx16 *4, 990MHz	K4W4G1646D-BC1A	4.53K	4.99K
101	Micron - E die	256Mx16 *4, 990MHz	W1J1J2S6M16HA-0939G-E	3.24K	5.62K

BIT5 => BIT0	
PS0	=> 11001
PS1	=> 11000
PS2	=> 11000
PS3	=> 11011



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/W/histler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

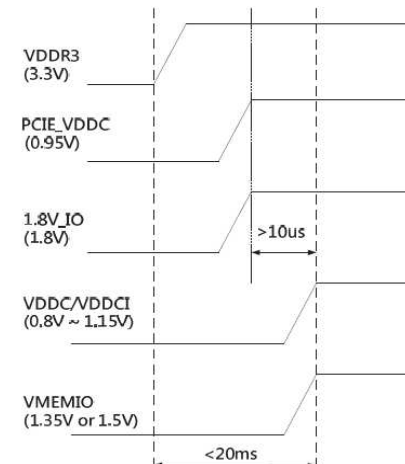
NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

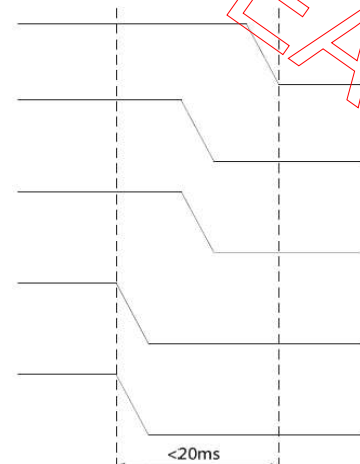
GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE

POWER UP

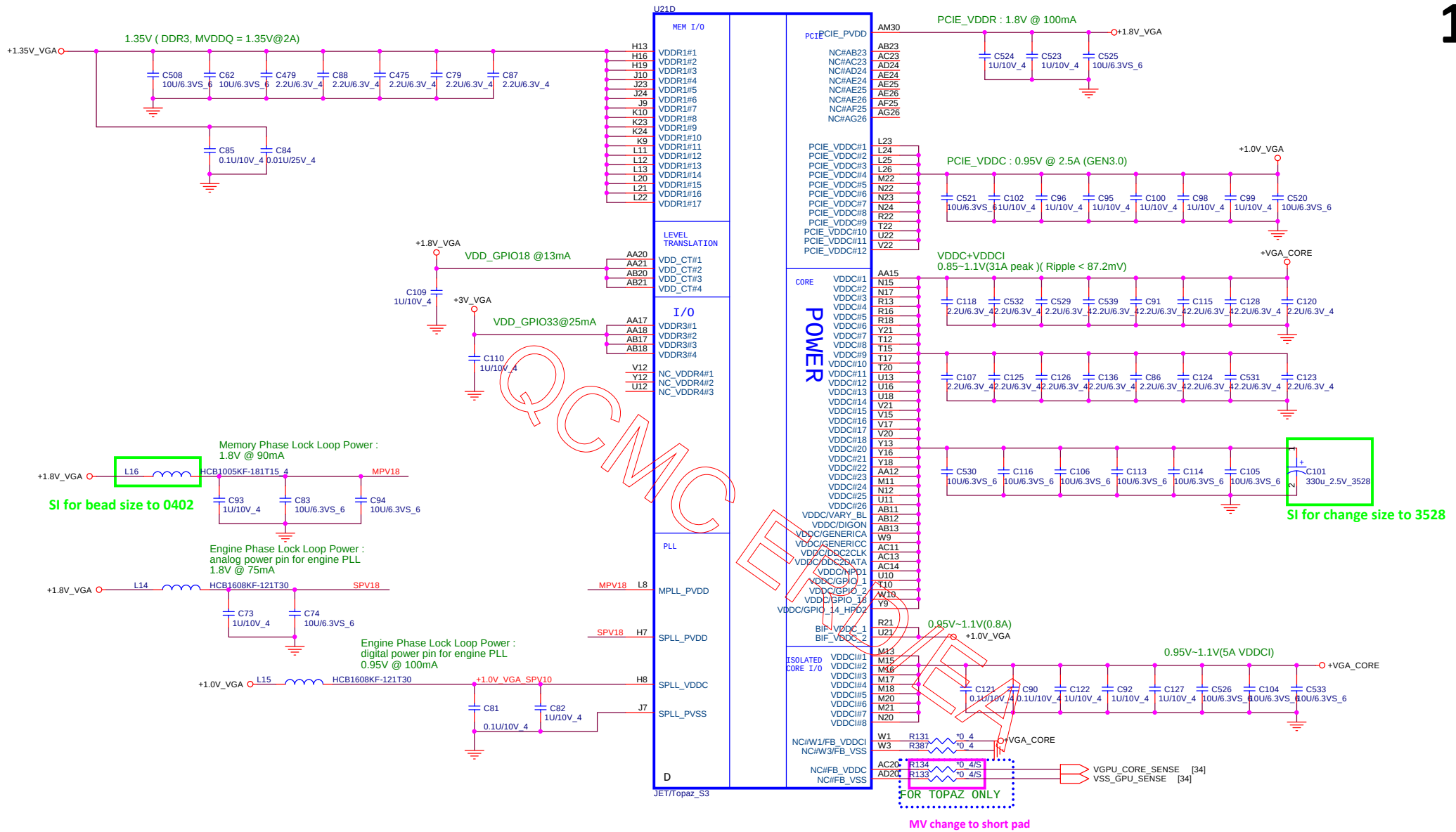


POWER DOWN



PROJECT : Y22A
Quanta Computer Inc.

Size	Document Number	Rev
	TOPAZ_S3_GND/LVDS/Strap	1A
Date: Wednesday, March 19, 2014	Sheet 12 of 36	

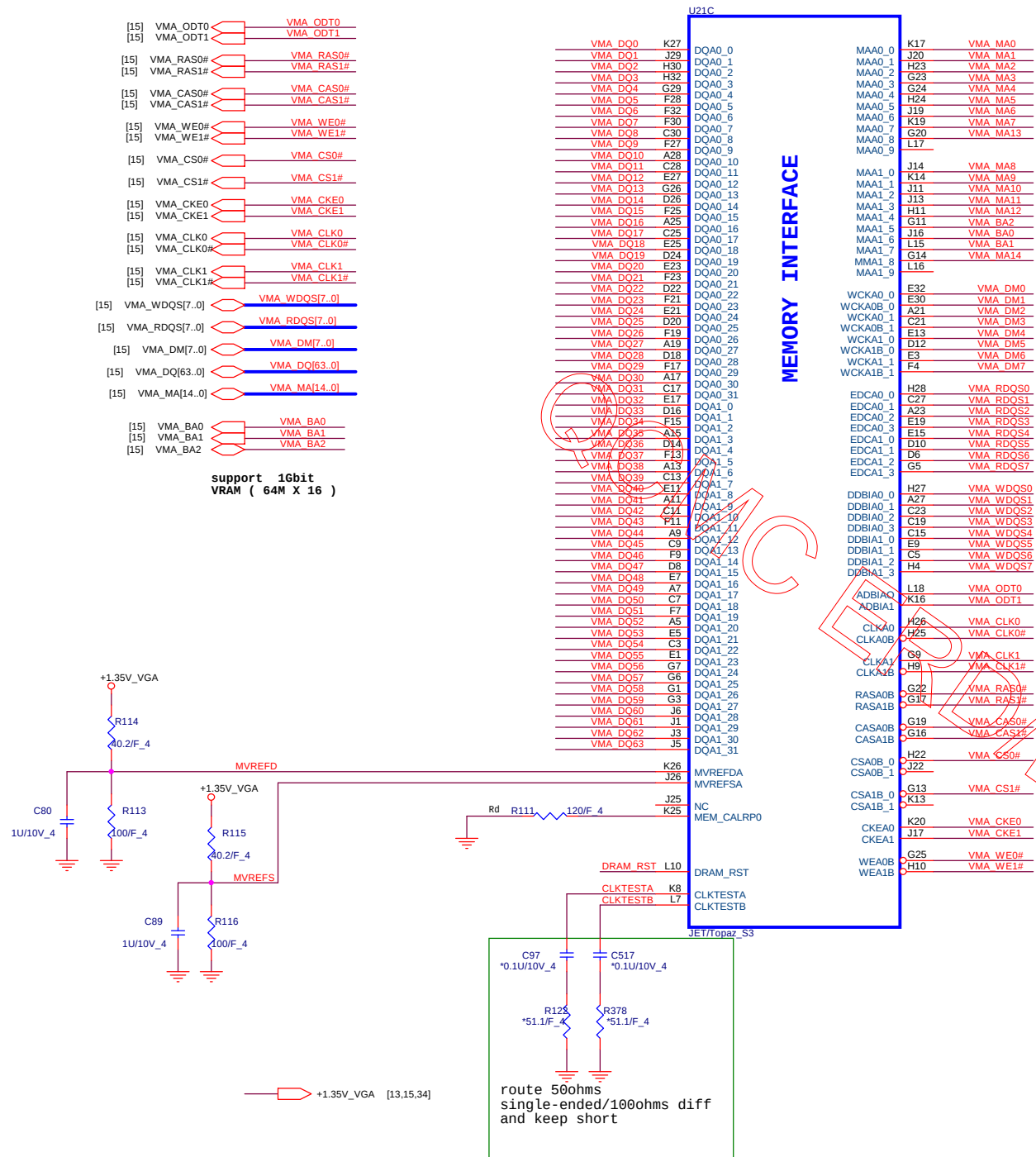


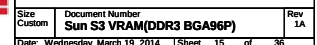
+1.35V_VGA [14,15,34]
 +1.8V_VGA [10,11,34,36]
 +1.0V_VGA [10,36]
 +VGA_CORE [34,35]

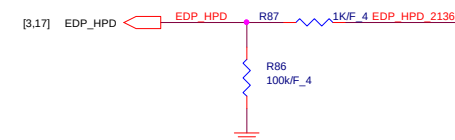
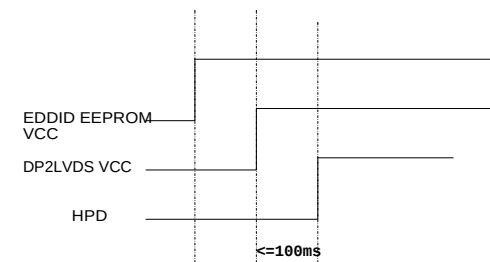


PROJECT : Y22A
Quanta Computer Inc.

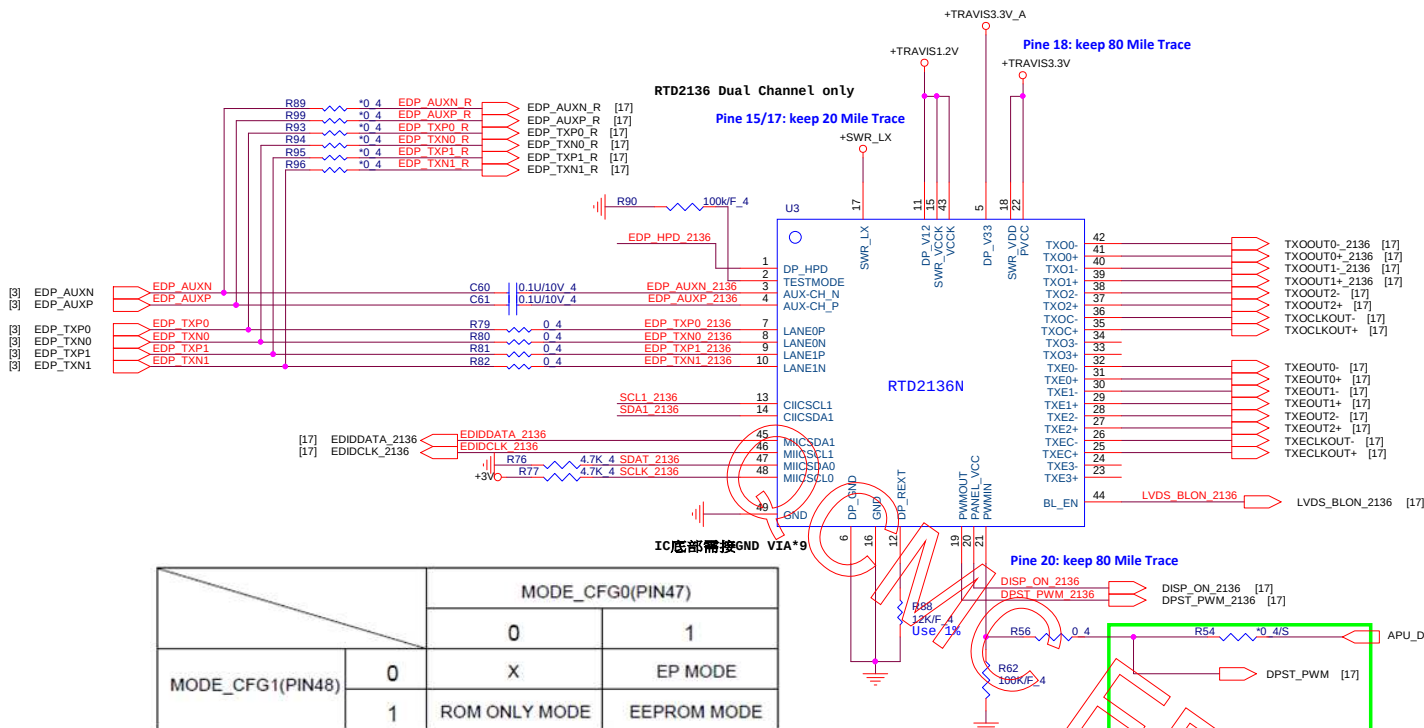
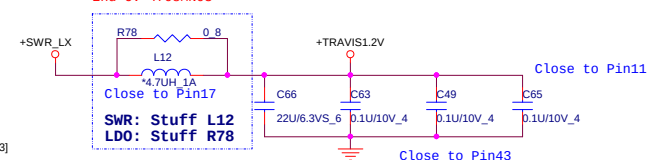
Size	Document Number	Rev
	TOPAZ S3 Power	1A
Date: Thursday, March 27, 2014	Sheet 13 of 36	



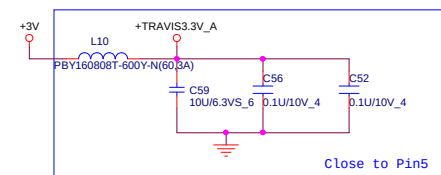
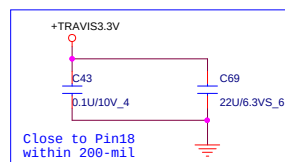
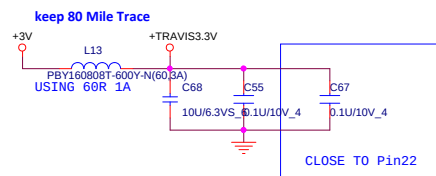
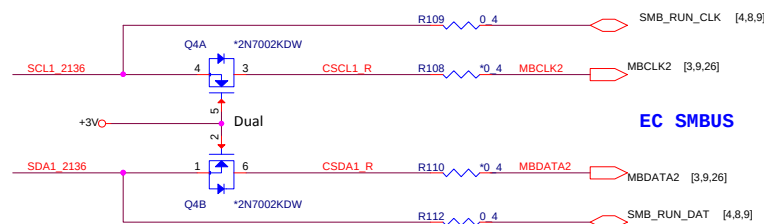




L12: need use CV-4709MN00 for Vendor suggestion
2nd CV-4708MN03

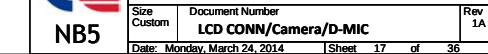


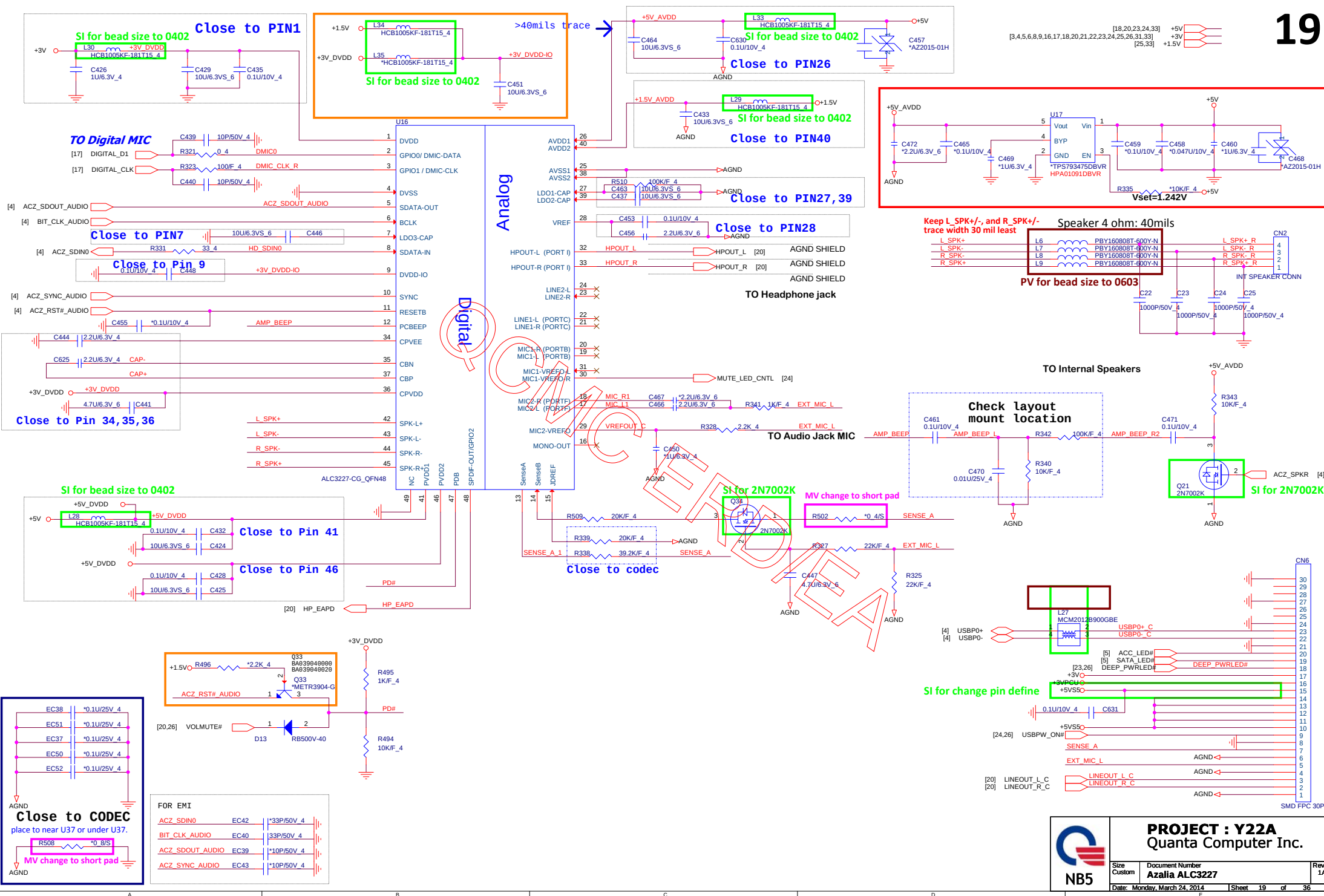
		MODE_CFG0(PIN47)	
		0	1
MODE_CFG1(PIN48)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

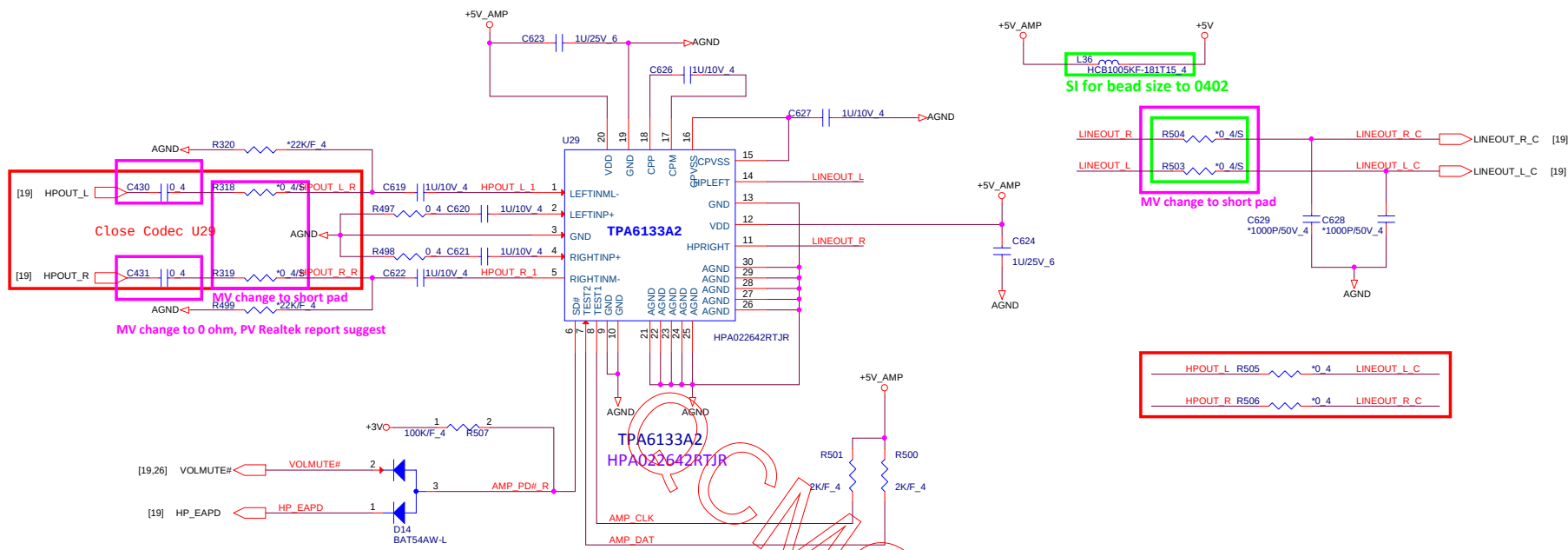


SI for Level shift is needless

17

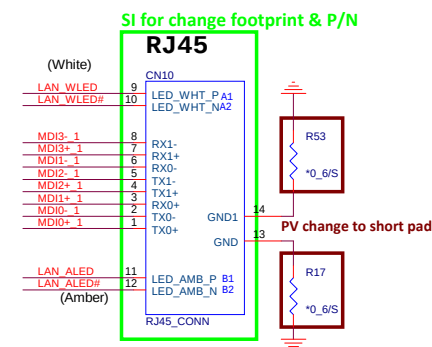
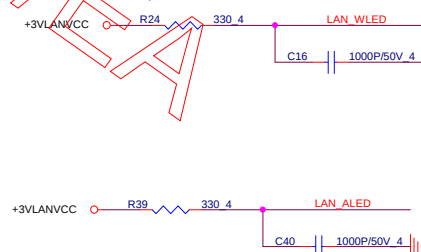
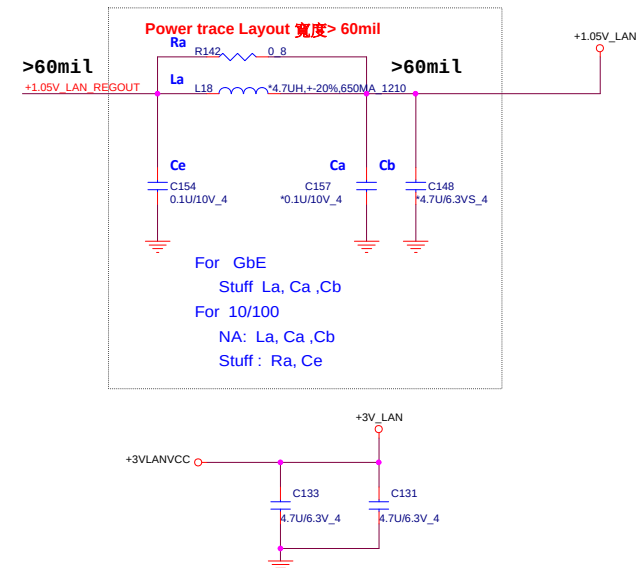


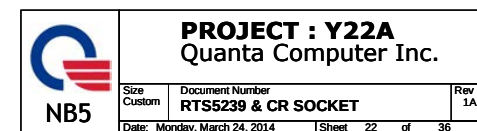
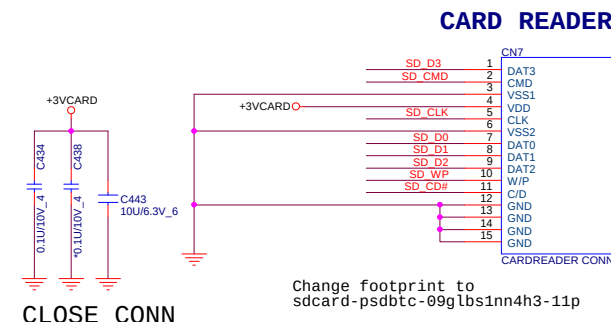




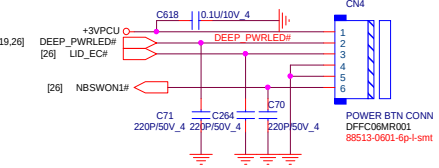
[19,24,28,29,30,31,32,33,34,36] +5VS5
 [3,4,5,6,8,9,16,17,18,19,21,22,23,24,25,26,31,33] +3V
 [18,19,23,24,33] +5V
 [3,5,19,23,24,25,26,27,28] +3VPCU

	PROJECT : Y22A		
	Quanta Computer Inc.		
	Size Custom	Document Number AMP TPA6130A2	Rev 1A
	Date: Monday, March 24, 2014	Sheet 20	of 36

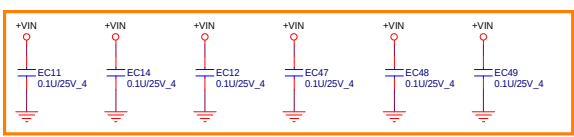
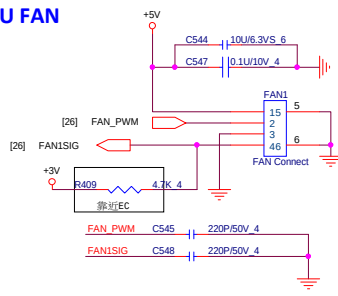




Power Button Connector

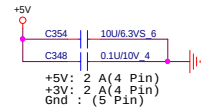
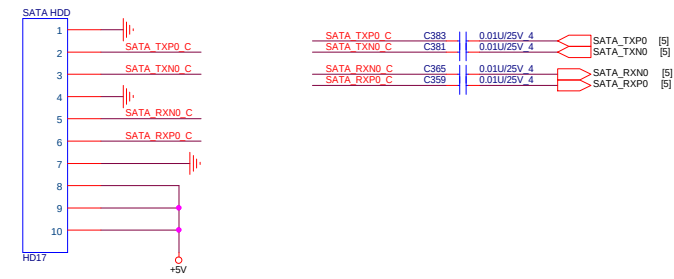


CPU FAN

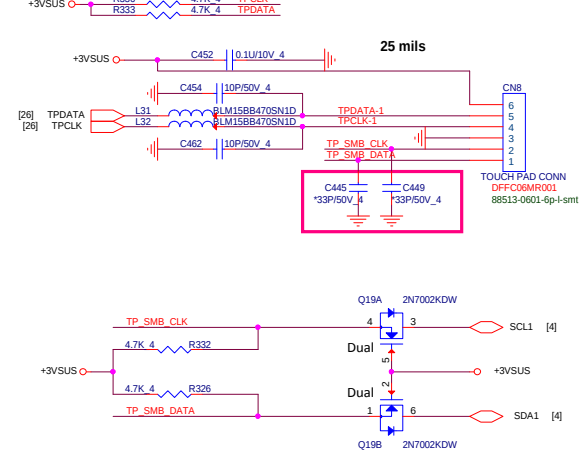


FOR EMI

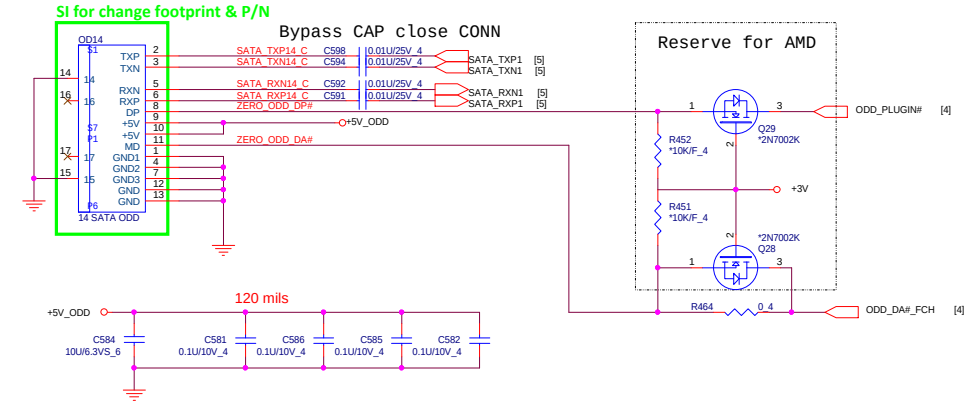
SATA HDD Connector(Cable type)



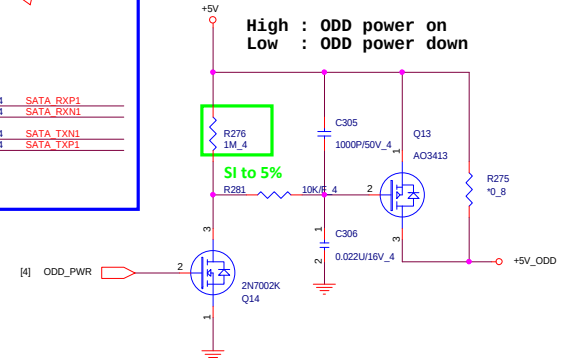
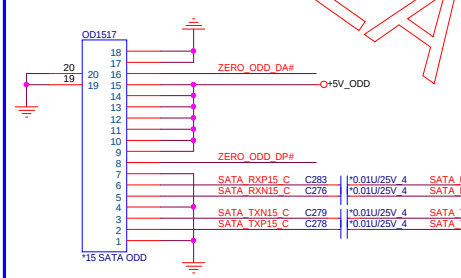
Touch Pad



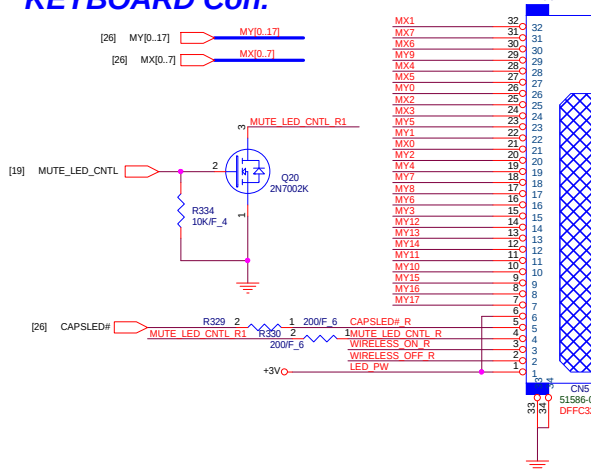
SATA ODD CONNECTOR



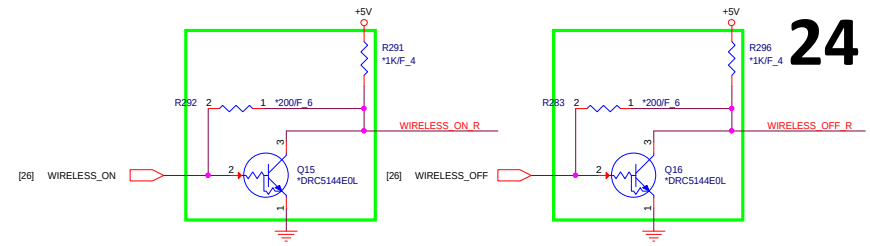
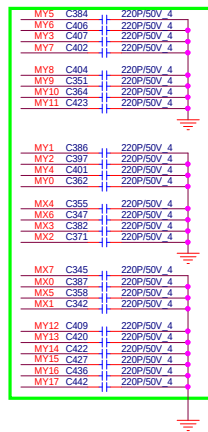
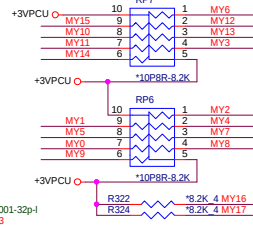
15"&17" SATA ODD



KEYBOARD Con.

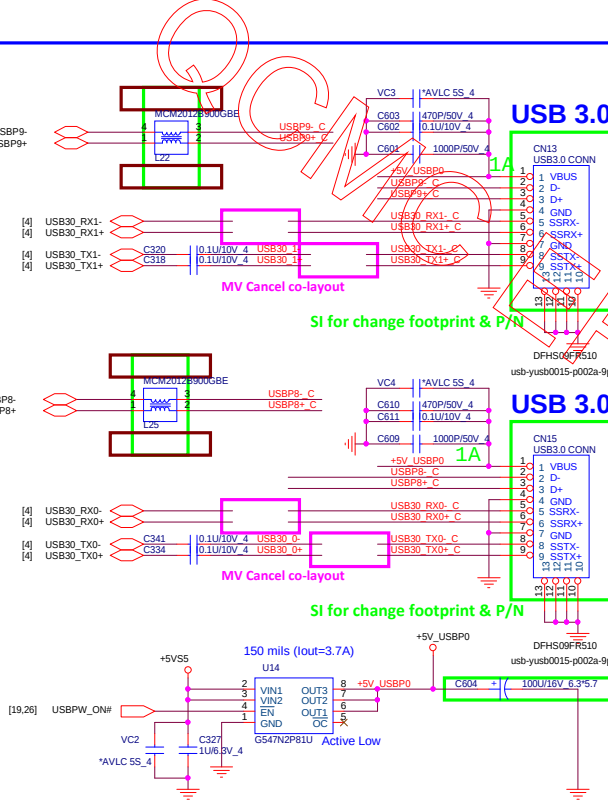
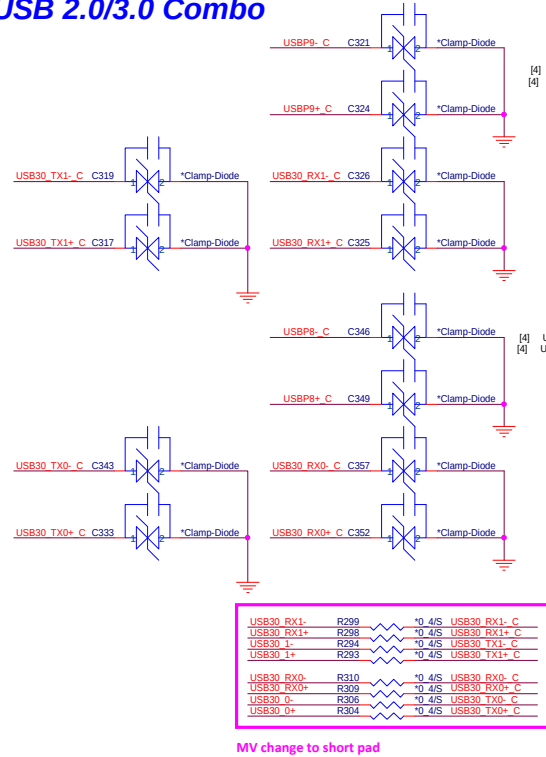


KEYBOARD PULL-UP

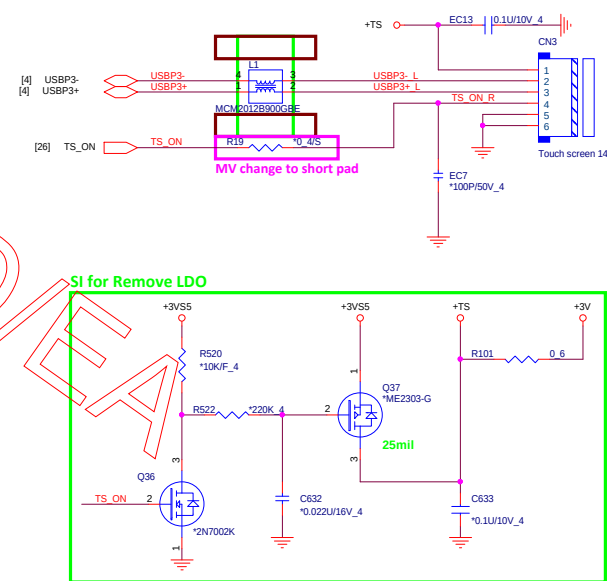


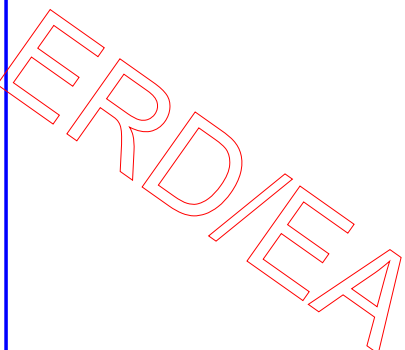
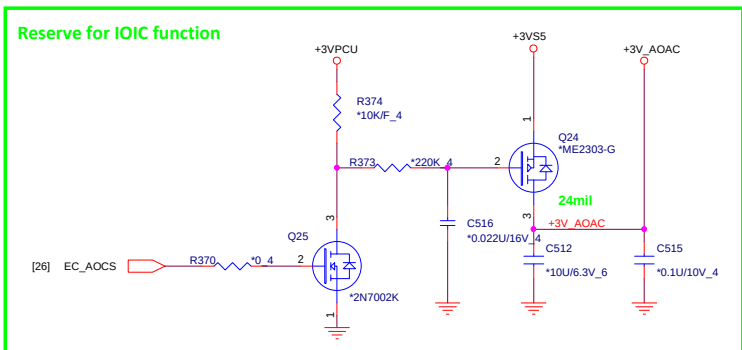
24

USB 2.0/3.0 Combo

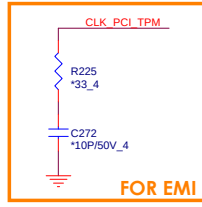


Touch screen

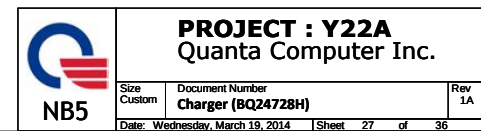


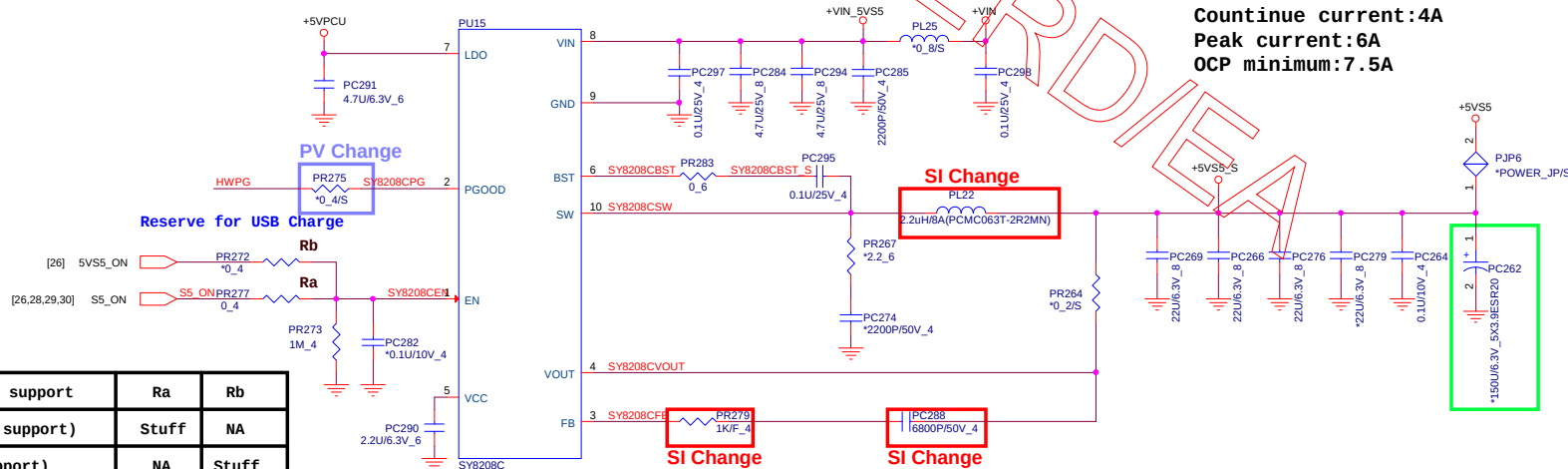
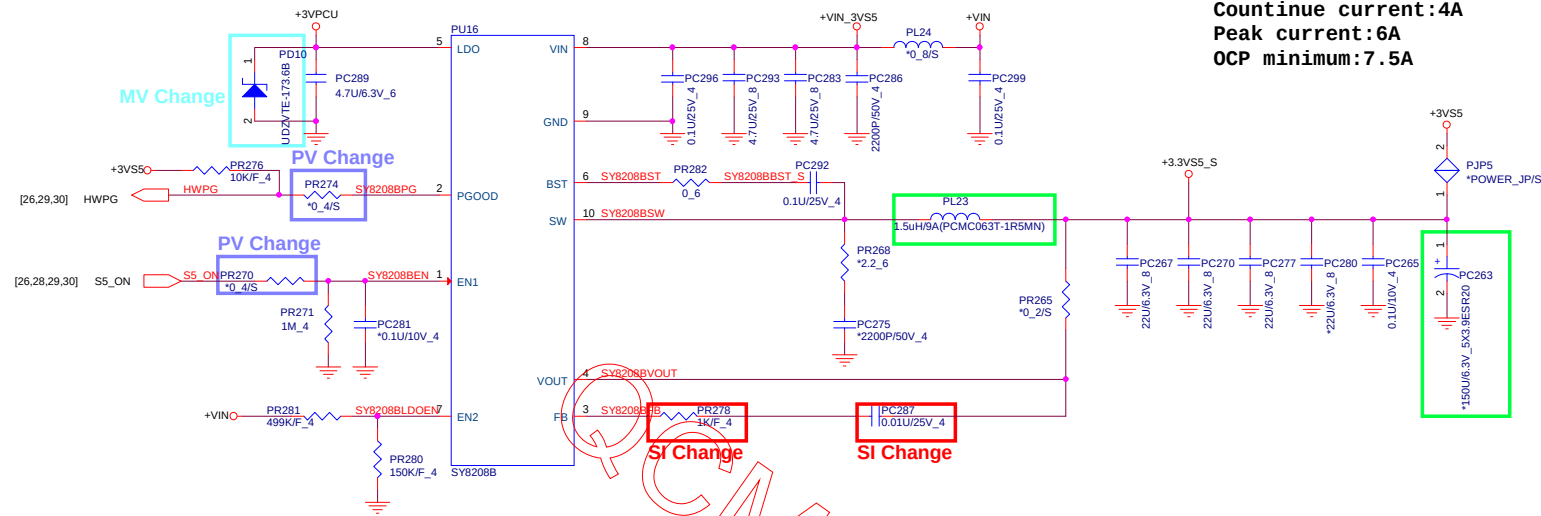


TPM (1.2)



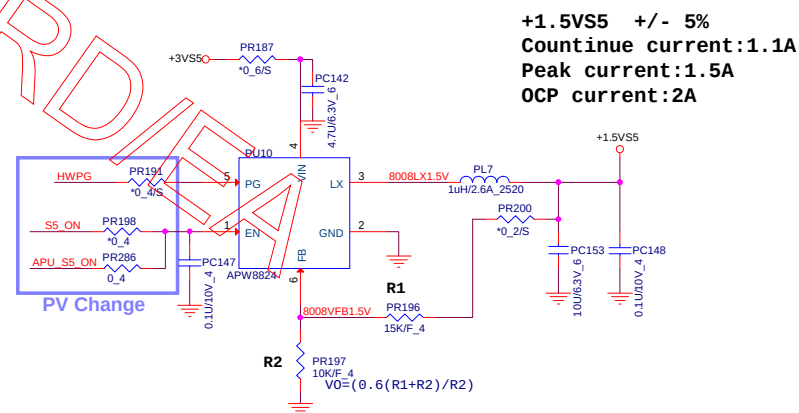
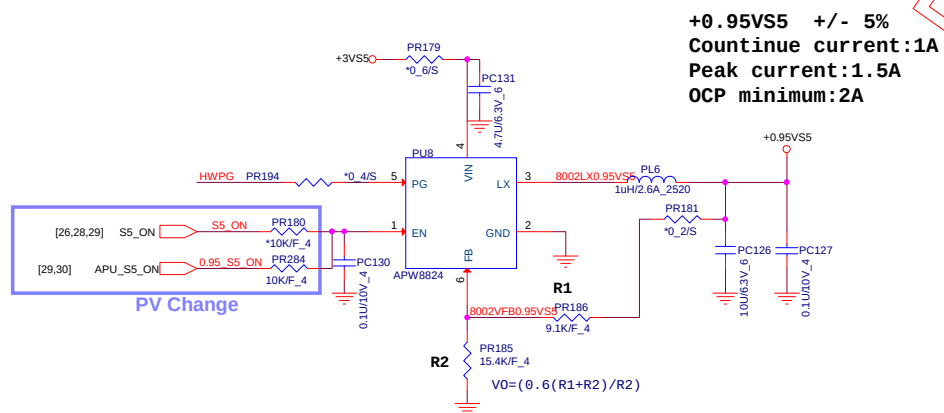
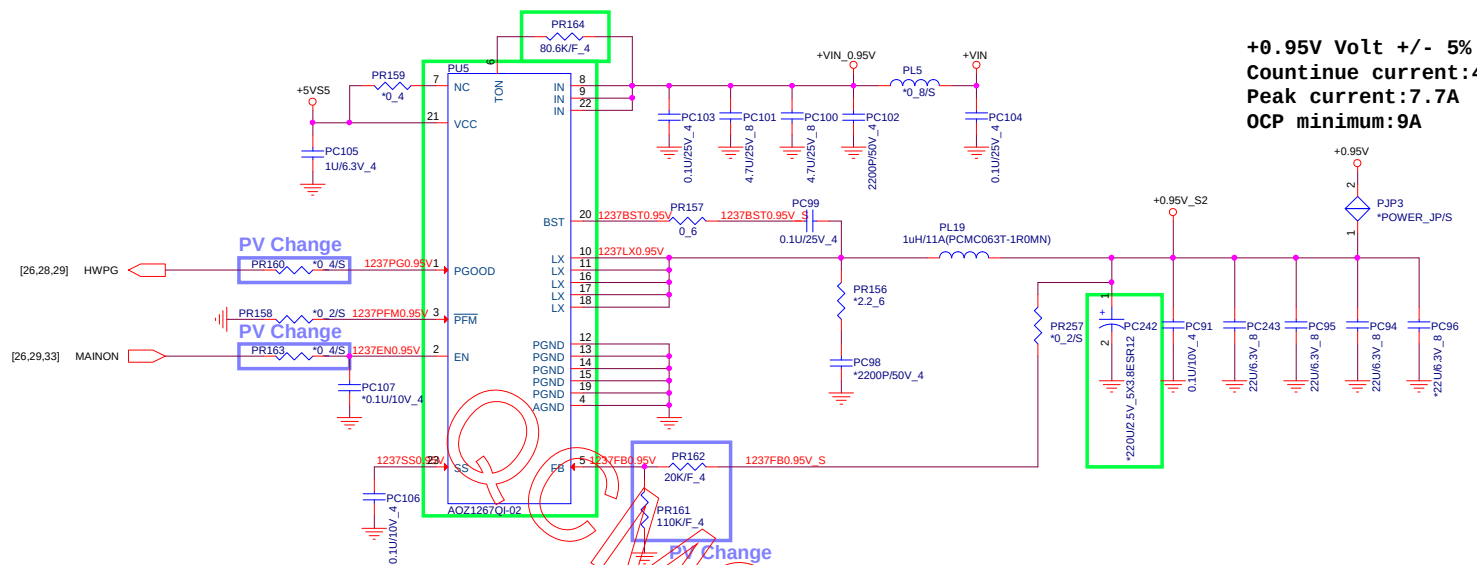
 NB5	PROJECT : Y22A Quanta Computer Inc.		
	Size Custom	Document Number WLAN/G-Sensor/GCLK/TPM	Rev 1A
	Date: Thursday, March 20, 2014 Sheet 25 of 36		

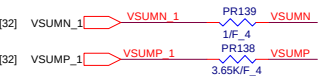


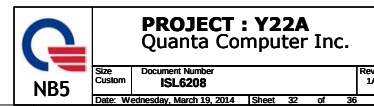
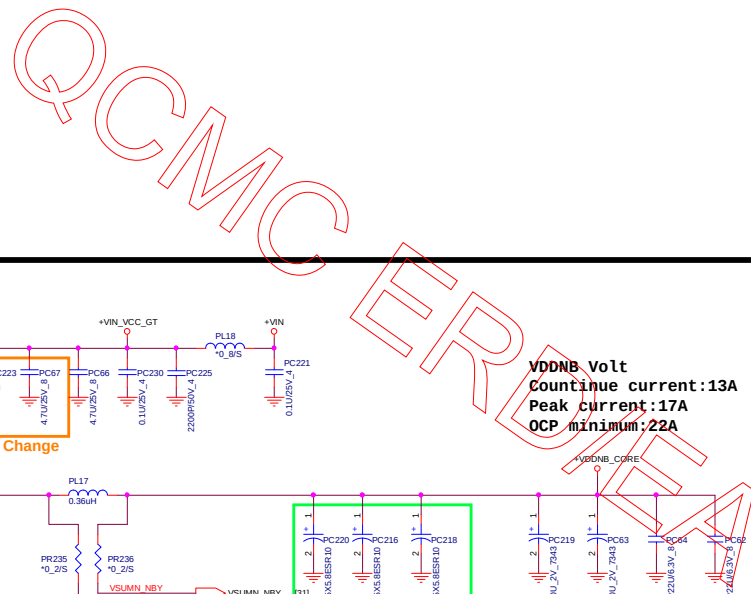


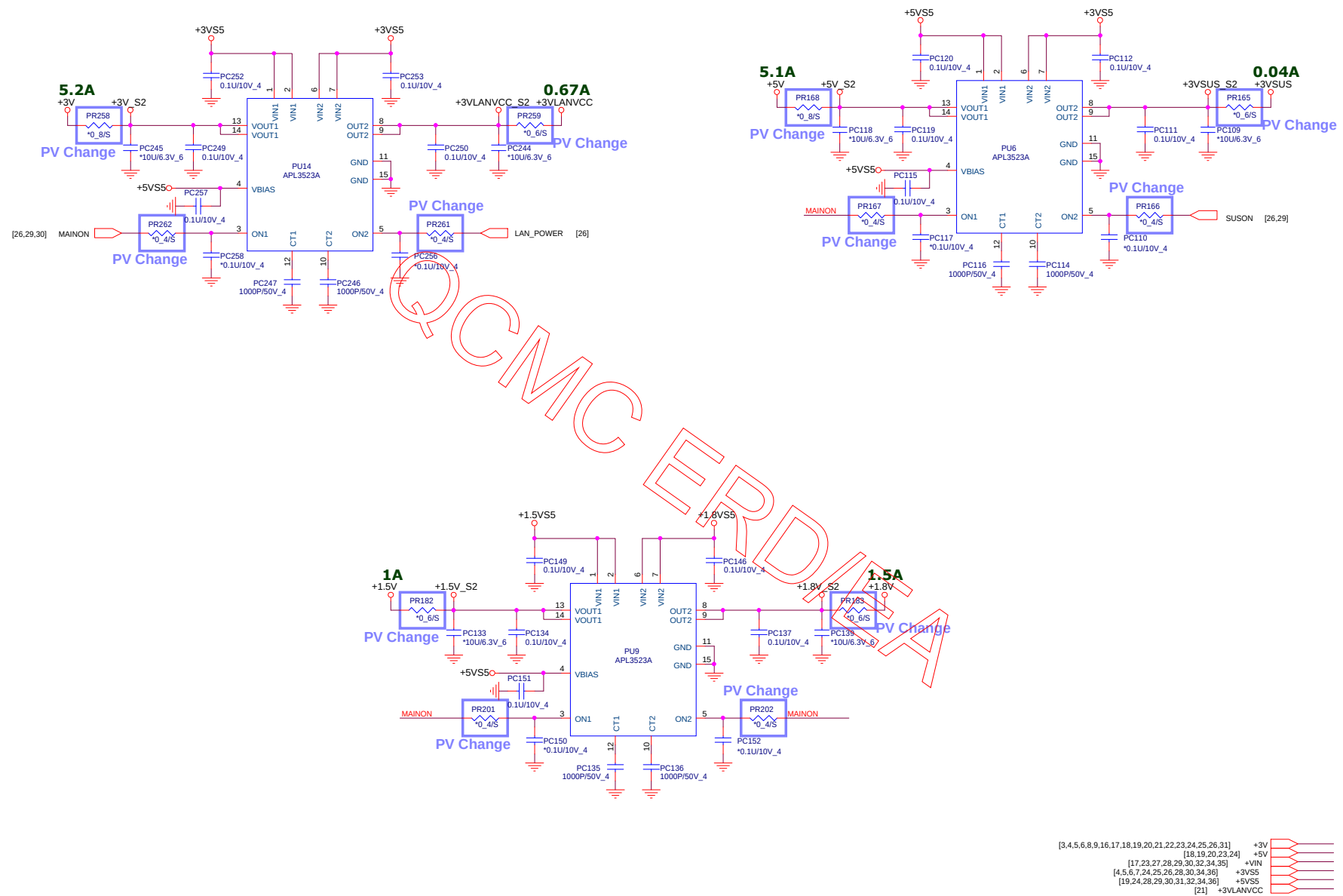
USB Charge support	Ra	Rb
Vine (No support)	Stuff	NA
Envy (Support)	NA	Stuff

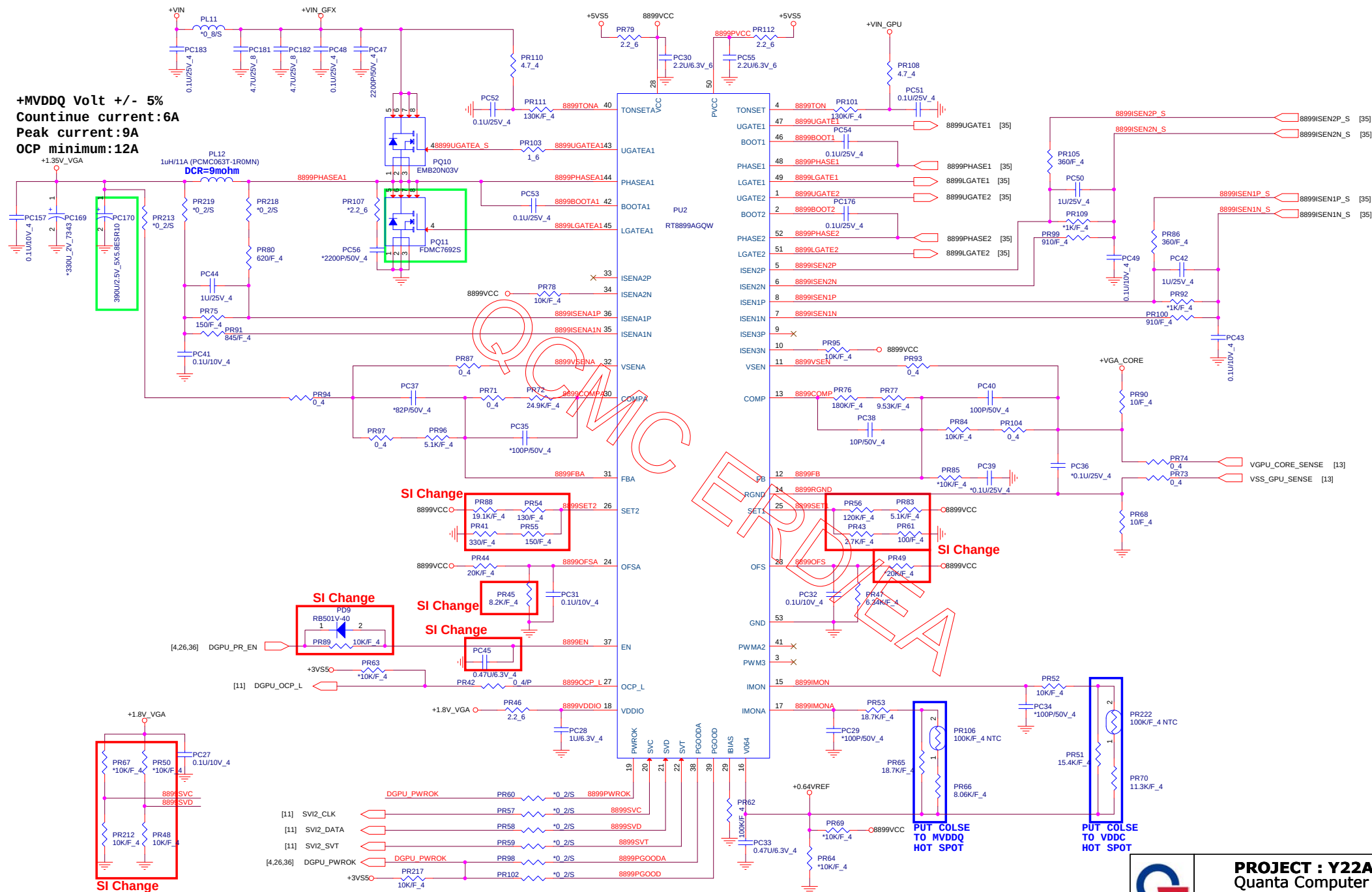


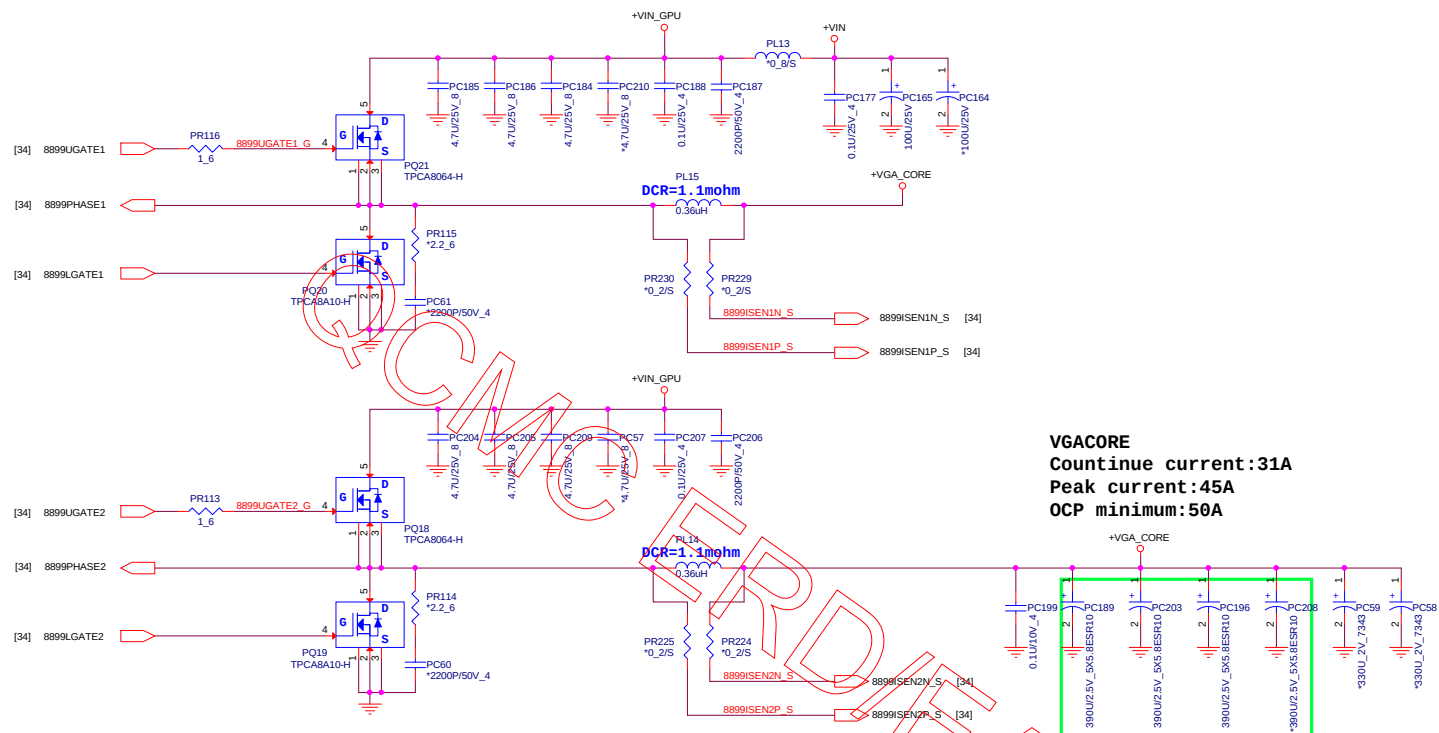


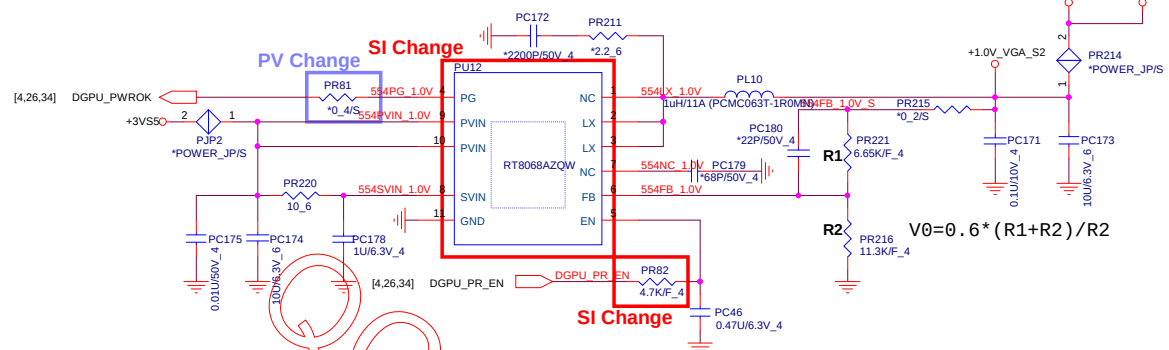











$$V_0 = 0.6 * (R_1 + R_2) / R_2$$

PUT COLSE TO
+1.8V power.

