QT8 SYSTEM DIAGRAM

AMD Smarter Choice

01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : IN1
LAYER 3 : IN2
LAYER 4 : VCC
LAYER 5 : IN3
LAYER 6 : BOT

DDRII-SODIMM1 PAGE 7,8
DDRII-SODIMM2 PAGE 7,8
DDRII 667/800 MHz

AMD Griffin Lion Sabie
S1G2 Processor
638P (uPGA)/35W
PAGE 3,4,5,6

CPU THERMAL SENSOR PAGE 5

14.318MHz
CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP626VTR-->HP
RTM880N-795 -->HP
PAGE 2
CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK
SBSRC_CLK

HT3

PCI-E
PCI-Express 16X

NORTH BRIDGE
RX781 / RS780MN
A12
21mm X 21mm, 528pin BGA
PAGE 8,9,10,11,

HDMI PAGE 23
CRT PAGE 24
LVDS PAGE 23

ATI M82-S for Discrete only
64 Bit,DDR2*4
M82-SCE A11
PAGE 17,18,19 20,21,22

Side port
256mb RAM for UMA only PAGE 8

ALINK X4

SOUTH BRIDGE
SB700 A12
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13.14.15.16

USB2.0
1,8,9 USB2.0 Ports X3 PAGE 30
5 Blueflame PAGE 30
2 Webcam X1 PAGE 30
6 Fingerprint PAGE 30
3 Flash Media for UMA only RTS5158 PAGE 25
Touch Screen for Discrete only

10 PCI-E WLAN Card x1 PAGE 36
11 TV-TUNER Card x1 PAGE 36
7 Express Card x1 PAGE 33
4 Cable Docking x1 PAGE 37

X1 LAN
Realtek PCIE-LAN RTL8102E/8111C (10/100/GagaLAN)
PAGE 31,32
RJ45 PAGE 31

X1 Express Card (NEW CARD) PAGE 33

X3 Mini PCI-E Card (Wireless LAN/TV TUNNER) PAGE 36

Cable Docking PAGE 37
VGA
RJ-45
CIR/Pwr btn
SPDIF Out
Stereo MIC
Headphone Jack
USB Port
VOL Cntr

SYSTEM CHARGER(ISL6251A) PAGE 44
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DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 41
VCCP +1.1V AND +1.2V(MAX8717) PAGE 39
VGACORE(1.1V~1.2V)Oz8118 PAGE 42
CPU CORE ISL6265A PAGE 40

TWO SATA - HDD PAGE 33 — SATA0,1 150MB
SATA - CD-ROM PAGE 33 — SATA0 150MB
E-SATA PAGE 30 — SATA4 150MB

PCIE BUS
Azalia
SMBUS
LPC

JMICRON JMD380 for Discrete only PAGE 27

IDT 92HD71B7 PAGE 27

AUDIO Amplifier TPA6017A2 PAGE 28

MDC CONN PAGE 29

IEEE1394 connect for Discrete only PAGE 26

Memory CardReader PAGE 25

Accelerometer LIS3LV02DL PAGE 28
Keyboard PAGE 34
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CIR (AUDIO CONN) PAGE 27
Capacitive Sense SW PAGE 34

ENE KBC
KB3926 Cx
PAGE 35

FAN PAGE 37
SPI PAGE 35

Digital MIC PAGE 30
AUDIO CONN (Phone/ MIC) PAGE 27
Audio Conn PAGE 28

SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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CLOCKS name	RX780	RS780	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP64 STUFF	RP64 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGPP_CLKP NBGPP_CLKN	RP70 STUFF	RP70 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP72 STUFF	RP72 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R653,R656,R612 STUFF	R653,R656,R612 NC	To M82-S 27Mhz - RX780 only

+1.2V L49 BLM18PG181SN1D(180,1.5A)_6 60 ohm, 0.5A +1.2V_CLKVDDIO
600 ohms@100Mhz C523 10U/6.3V_8 C518 C496 C527 C521 C476 C515 0.1U/10V_4

DCR: 0.5 ohm
600 ohms@100Mhz +3V_CLKVDD
+3V L51 BLM18PG181SN1D(180,1.5A)_6 60 ohm, 0.5A +3V_CLKVDD
C541 10U/6.3V_8 C468 C473 C512 C522 C508 C500 C474 C471 C469 0.1U/10V_4

Place very close to C/G

+3V_CLKVDD L42 BLM18PG181SN1D(180,1.5A)_6 +3V_CLK_VDDA
C464 10U/6.3V_8 C482 C470 0.1U/10V_4

U10A

49	VDDA	CPUKG0T_LPRS	56 CPUCLKP
48	GNDA	CPUKG0C_LPRS	55 CPUCLKN
62	VDDREF	ATIG0T_LPRS	33 NBGFX_CLKP
66	GNDREF	ATIG0C_LPRS	32 NBGFX_CLKN
69	VDD48	ATIG1T_LPRS	31 EXT_GFX_CLKP
29	VDDATIG	ATIG1C_LPRS	30 EXT_GFX_CLKN
54	VDDCPU	ATIG2T_LPRS	26
61	VDDHTT	ATIG2C_LPRS	25
38	VDDSB_SRC	SB_SRC0T_LPRS	40 PCIE_MINI2_CLKP
17	VDDSRC	SB_SRC0C_LPRS	39 PCIE_MINI2_CLKN
44	VDDSATA	SB_SRC1T_LPRS	35 CLK_PCIE_CARD
3	VDDDOT	SB_SRC1C_LPRS	34 CLK_PCIE_CARD#
53	VDDCPU_IO	SRC0T_LPRS	23 NBGPP_CLKN_R
28	VDDATIG_IO	SRC0C_LPRS	22 NBGPP_CLKN_L
37	VDDSB_SRC_IO	SRC1T_LPRS	21 PCIE_NEW_CLKP
12	VDDSRC_IO1	SRC1C_LPRS	20 PCIE_NEW_CLKN
18	VDDSRC_IO2	SRC2T_LPRS	16 PCIE_MINI1_CLKP
		SRC2C_LPRS	15 PCIE_MINI1_CLKN
72	GND48	SRC3T_LPRS	14 SBLINK_CLKP
27	GNDATIG1	SRC3C_LPRS	13 SBLINK_CLKN
6	GNDDOT	SRC4T_LPRS	10 SBSRC_CLKP
52	GNDCPU	SRC4C_LPRS	9 SBSRC_CLKN
58	GNDHTT	SRC5T_LPRS	8 PCIE_LAN_CLKP
47	GNDSATA	SRC5C_LPRS	7 PCIE_LAN_CLKN
36	GNDSB_SRC	SRC6T/SATAT_LPRS	46
11	GNDSRC1	SRC6C/SATAC_LPRS	45
19	GNDSRC2	SRC7T_LPRS/27Mhz_SS	5 CLK_VGA_27M_SS
		SRC7C_LPRS/27Mhz_NS	4 CLK_VGA_27M_NSS
67	X1	HTT0T/66M_LPRS	60
68	X2	HTT0C/66M_LPRS	59 NBHTREFCLK0P
57	PD#	48MHz_0	71 NBHTREFCLK0N
1	SMBCLK	48MHz_1	70 CLK_48M_CR_L
2	SMBDAT	REF0/SEL_HTT66	65 SEL_HT66
		REF1/SEL_SATA	64 SEL_SATA
		REF2/SEL_27	63 SEL_27
41	SB_SRC_SLOW#	CLKREQ0#	24 CLKREQ0#
		CLKREQ1#	51 EXT_NWD_CLK_REQ#
		CLKREQ2#	50 CLKREQ2#
		CLKREQ3#	43 CLKREQ3#
		CLKREQ4#	42 CLKREQ4#

SLG8SP626VTR

THERMAL GND
73 eGND73, 74 eGND74, 75 eGND75, 77 eGND77, 76 eGND76, 78 eGND78
U10B SLG8SP626VTR

+3V_CLKVDD
+1.2V_CLKVDDIO

C466 33P/50V_4 CG_XIN
Y2 14.318MHZ
C465 33P/50V_4 CG_XOUT

CG_XIN
CG_XOUT
CLK_PD#
PCLK_SMB
PDAT_SMB
6,7,13,28,36 PCLK_SMB
6,7,13,28,36 PDAT_SMB

14 CHIPSET_PCIE_SLOW_SB# D17 *CH501H-40PT L-F SB_SRC_SLOW#

can remove MOSFET level shift
SB/clock gen / DDR2 is 3.3V/S0
power level

when driven low SB_SRC clocks slow only supported with to reduced setpoint custom CG IC

Place within 0.5" of CLKGEN
R196 *261_4

Del RP for TP on PV

RP43	4	3	*0_4P2R_4	CPUCLKP	CPUCLKP 3
	2	1		CPUCLKN	CPUCLKN 3
RP54	4	3	*0_4P2R_4	NBGFX_CLKP	NBGFX_CLKP 10
	2	1		NBGFX_CLKN	NBGFX_CLKN 10
RP53	4	3	*0_4P2R_4	EXT_GFX_CLKP	EXT_GFX_CLKP 17
	2	1		EXT_GFX_CLKN	EXT_GFX_CLKN 17
RP48	4	3	*0_4P2R_4	PCIE_MINI2_CLKP	PCIE_MINI2_CLKP 36
	2	1		PCIE_MINI2_CLKN	PCIE_MINI2_CLKN 36
RP55	4	3	*0_4P2R_4	CLK_PCIE_CARD	CLK_PCIE_CARD 26
	2	1		CLK_PCIE_CARD#	CLK_PCIE_CARD# 26
RP51	4	3	*0_4P2R_4	PCIE_NEW_CLKP	PCIE_NEW_CLKP 33
	2	1		PCIE_NEW_CLKN	PCIE_NEW_CLKN 33
RP49	4	3	*0_4P2R_4	PCIE_MINI1_CLKP	PCIE_MINI1_CLKP 36
	2	1		PCIE_MINI1_CLKN	PCIE_MINI1_CLKN 36
RP47	4	3	*0_4P2R_4	SBLINK_CLKP	SBLINK_CLKP 10
	2	1		SBLINK_CLKN	SBLINK_CLKN 10
RP45	4	3	*0_4P2R_4	SBSRC_CLKP	SBSRC_CLKP 12
	2	1		SBSRC_CLKN	SBSRC_CLKN 12
RP44	4	3	*0_4P2R_4	PCIE_LAN_CLKP	PCIE_LAN_CLKP 31
	2	1		PCIE_LAN_CLKN	PCIE_LAN_CLKN 31

T196 T84 T59 T62 T58 T167

to NB for external Graphics reference clock
to M82-S -RX780 only
to TV TUNER CARD
to PCIE-CARD READER
Del RP52 for NBGPP CLK
to EPRESS CARD
to WLAN
to NB for AC-LINK reference clock
to SB
to PCIE-LAN
SI-1 Modified --remove to ROBSON

R527 33_4 OSC_SPREAD
R515 75/F_4
R490 100/F_4
OSC_SPREAD 18
EVGA-XTALI 18

SSIN - for M82 - 3.3V level input
X_TALIN --for M82 -1.8V level input

R193 0_4 NBHT_REFCLKP
R194 0_4 NBHT_REFCLKN
R201 33_4 CLK_48M_CR
R192 33_4 CLK_48M_USB
NBHT_REFCLKP 10
NBHT_REFCLKN 10
CLK_48M_CR 25
CLK_48M_USB 13

EXT_NWD_CLK_REQ# 33

Clock chip has internal serial terminations
for differential pairs, external resistors are
reserved for debug purpose.

R186 Ra 158/F_4
R184 1 2 90.9/F_4 Rb
EXT_NB_OSC 10

	RX780	RS780
	1.8V	1.1V
Ra	82.5R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11

C952 C953 C954 C955 C956 *10P/50V_4
EXT_NB_OSC
CLK_48M_USB
CLK_48M_CR
EVGA-XTALI
OSC_SPREAD
SI-1 modified -- reserve for EMT

+3V
R756 R757 R758 R759 *8.2K_4
CLKREQ0# CLKREQ2# CLKREQ3# CLKREQ4#
if use clock request pin , need to pull Hi for default sttting

ICS ICS9LPR476BKLFT--AJRS4760000
SLG SLG8SP626VTR--AJ006260000
RTL RTM880N-795-- AJ008800000

* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

+3V_CLKVDD
R189 *8.2K_4 R195 8.2K_4
SEL_27 SEL_SATA SEL_HT66
R203 8.2K_4 R202 *8.2K_4
RS780M/RX780M

+3V
EXT_NWD_CLK_REQ# 8.2K_4 R219
CLK_PD# 8.2K_4 R204
SB_SRC_SLOW# 8.2K_4 R261

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Generator	1A

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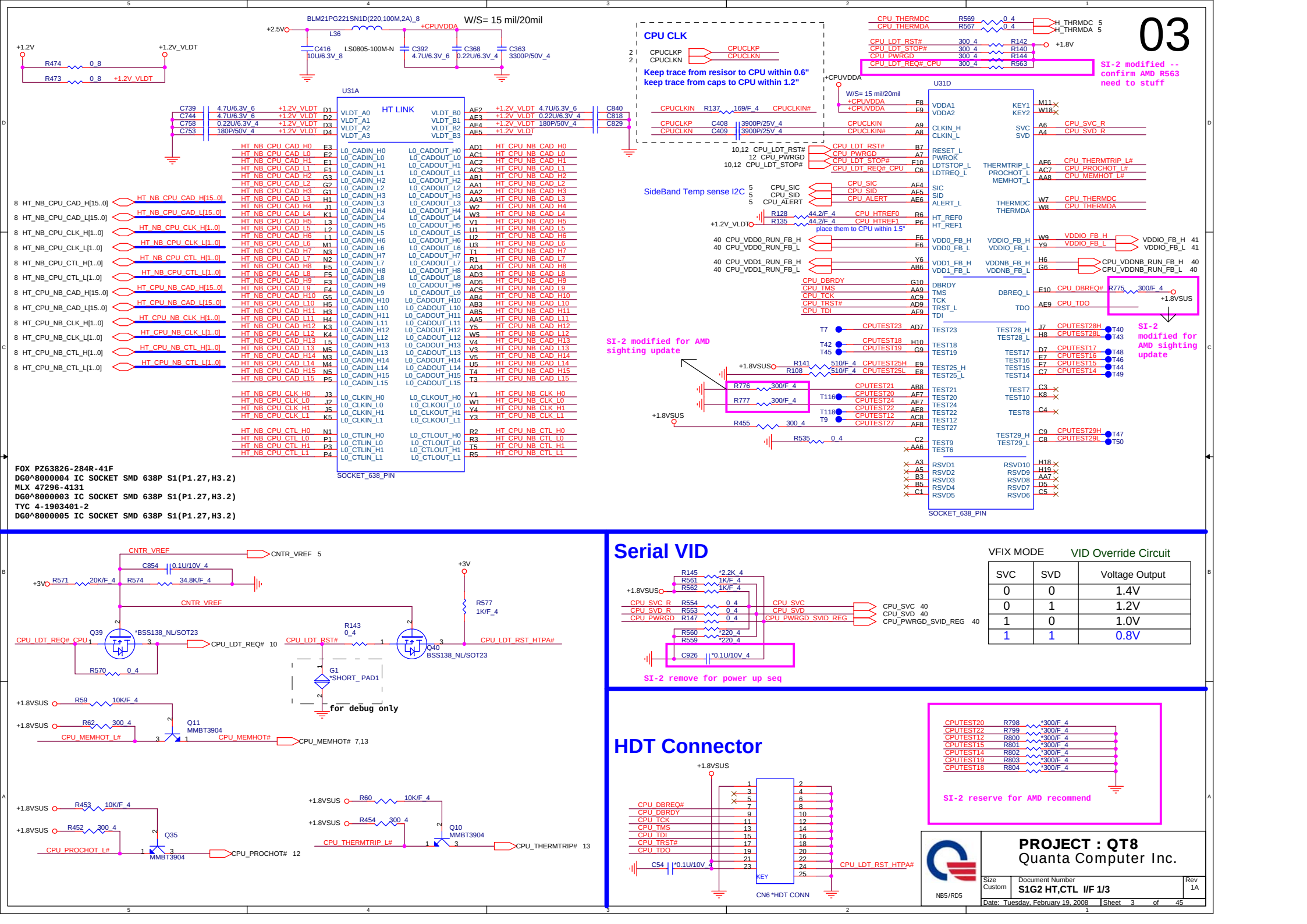
03
CPU CLK
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
SI-2 modified -- confirm AMD R563 need to stuff
SideBand Temp sense I2C
place them to CPU within 1.5"
SI-2 modified for AMD sighting update
SI-2 modified for AMD sighting update
FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)
Serial VID
SI-2 remove for power up seq
VFIX MODE
VID Override Circuit
SVC SVD Voltage Output
0 0 1.4V
0 1 1.2V
1 0 1.0V
1 1 0.8V
HDT Connector
SI-2 reserve for AMD recommend
for debug only
PROJECT : QT8
Quanta Computer Inc.
S1G2 HT,CTL I/F 1/3
NB5/RD5
Date: Tuesday, February 19, 2008
Sheet 3 of 45

Processor Memory Interface

04

PLACE THEM CLOSE TO CPU WITHIN 1"

U31B

SOCKET_638_PIN

750 mA

U31C

MEM:DATA

SOCKET_638_PIN

Place close to socket

Close to CPU within 1500 mils

PROJECT : QT8 Quanta Computer Inc.			
NB5/RD5	Size: Custom	Document Number: S1G2 DDRII MEMORY I/F 2/3	Rev: 1A
	Date: Tuesday, February 19, 2008	Sheet 4 of 45	

PROCESSOR POWER AND GROUND

BOTTOM SIDE DECOUPLING

+VCORE0
C287 22U/6.3V_8, C308 22U/6.3V_8, C307 22U/6.3V_8, C306 22U/6.3V_8, C285 0.22U/6.3V_4, C286 0.01U/16V_4, C301 180P/50V_4

+VCORE1
C230 22U/6.3V_8, C272 22U/6.3V_8, C273 22U/6.3V_8, C267 22U/6.3V_8, C206 0.22U/6.3V_4, C226 0.01U/16V_4, C205 180P/50V_4, C225 0.01U/16V_4

+CPUVDDNB
C264 22U/6.3V_8, C231 22U/6.3V_8, C279 22U/6.3V_8

+1.8VSUS
C248 22U/6.3V_8, C284 22U/6.3V_8, C309 0.22U/6.3V_4, C247 0.22U/6.3V_4, C214 180P/50V_4, C315 180P/50V_4

DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE

+1.8VSUS
C750 4.7U/6.3V_6, C802 4.7U/6.3V_6, C236 4.7U/6.3V_6, C749 4.7U/6.3V_6, C803 0.22U/6.3V_4, C240 0.22U/6.3V_4

+1.8VSUS
C238 0.22U/6.3V_4, C751 0.22U/6.3V_4, C752 0.01U/16V_4, C120 0.01U/16V_4, C118 180P/50V_4

U31E — SOCKET_638_PIN

+VCORE0: VDD0_1 G4, VDD0_2 H2, VDD0_3 J9, VDD0_4 J11, VDD0_5 J13, VDD0_6 J15, VDD0_7 K6, VDD0_8 K10, VDD0_9 K12, VDD0_10 K14, VDD0_11 L4, VDD0_12 L7, VDD0_13 L9, VDD0_14 L11, VDD0_15 L13, VDD0_16 L15, VDD0_17 M2, VDD0_18 M6, VDD0_19 M8, VDD0_20 M10, VDD0_21 N7, VDD0_22 N9, VDD0_23 N11

+VCORE1: VDD1_1 P8, VDD1_2 P10, VDD1_3 R4, VDD1_4 R7, VDD1_5 R9, VDD1_6 R11, VDD1_7 T2, VDD1_8 T6, VDD1_9 T8, VDD1_10 T10, VDD1_11 T12, VDD1_12 T14, VDD1_13 U7, VDD1_14 U9, VDD1_15 U11, VDD1_16 U13, VDD1_17 U15, VDD1_18 V6, VDD1_19 V8, VDD1_20 V10, VDD1_21 V12, VDD1_22 V14, VDD1_23 W4, VDD1_24 Y2, VDD1_25 AC4, VDD1_26 AD2

+CPUVDDNB 3A: VDDNB_1 K16, VDDNB_2 M16, VDDNB_3 P16, VDDNB_4 T16, VDDNB_5 V16

+1.8VSUS 2A: VDDIO1 H25, VDDIO2 J17, VDDIO3 K18, VDDIO4 K21, VDDIO5 K23, VDDIO6 K25, VDDIO7 L17, VDDIO8 M18, VDDIO9 M21, VDDIO10 M23, VDDIO11 M25, VDDIO12 N17

+1.8VSUS: VDDIO27 Y25, VDDIO26 V25, VDDIO25 V23, VDDIO24 V21, VDDIO23 V18, VDDIO22 U17, VDDIO21 T25, VDDIO20 T23, VDDIO19 T21, VDDIO18 T18, VDDIO17 R17, VDDIO16 P25, VDDIO15 P23, VDDIO14 P21, VDDIO13 P18

U31F — SOCKET_638_PIN

VSS1 AA4, VSS2 AA11, VSS3 AA13, VSS4 AA15, VSS5 AA17, VSS6 AA19, VSS7 AB2, VSS8 AB7, VSS9 AB9, VSS10 AB23, VSS11 AB25, VSS12 AC11, VSS13 AC13, VSS14 AC15, VSS15 AC17, VSS16 AC19, VSS17 AC21, VSS18 AD6, VSS19 AD8, VSS20 AD25, VSS21 AE11, VSS22 AE13, VSS23 AE15, VSS24 AE17, VSS25 AE19, VSS26 AE21, VSS27 AE23, VSS28 B4, VSS29 B6, VSS30 B8, VSS31 B9, VSS32 B11, VSS33 B13, VSS34 B15, VSS35 B17, VSS36 B19, VSS37 B21, VSS38 B23, VSS39 B25, VSS40 D6, VSS41 D8, VSS42 D9, VSS43 D11, VSS44 D13, VSS45 D15, VSS46 D17, VSS47 D19, VSS48 D21, VSS49 D23, VSS50 D25, VSS51 F4, VSS52 F2, VSS53 F11, VSS54 F13, VSS55 F15, VSS56 F17, VSS57 F19, VSS58 F21, VSS59 F23, VSS60 F25, VSS61 H7, VSS62 H9, VSS63 H21, VSS64 H23, VSS65 J4

VSS66 J6, VSS67 J8, VSS68 J10, VSS69 J12, VSS70 J14, VSS71 J16, VSS72 J18, VSS73 K2, VSS74 K7, VSS75 K9, VSS76 K11, VSS77 K13, VSS78 K15, VSS79 K17, VSS80 L6, VSS81 L8, VSS82 L10, VSS83 L12, VSS84 L14, VSS85 L16, VSS86 L18, VSS87 M7, VSS88 M9, VSS89 AC6, VSS90 M17, VSS91 N4, VSS92 N8, VSS93 N10, VSS94 N16, VSS95 N18, VSS96 P2, VSS97 P7, VSS98 P9, VSS99 P11, VSS100 P17, VSS101 R8, VSS102 R10, VSS103 R16, VSS104 R18, VSS105 T7, VSS106 T9, VSS107 T11, VSS108 T13, VSS109 T15, VSS110 T17, VSS111 U4, VSS112 U6, VSS113 U8, VSS114 U10, VSS115 U12, VSS116 U14, VSS117 U16, VSS118 U18, VSS119 V2, VSS120 V7, VSS121 V9, VSS122 V11, VSS123 V13, VSS124 V15, VSS125 V17, VSS126 W6, VSS127 Y21, VSS128 Y23, VSS129 N6

+1.8VSUS
R164 390_4, R166 390_4, R167 1K/F_4

3 CNTR_VREF

18,35 MBCLK2 — MBCLK2 3 — Q14 *BSS138_NL/SOT23 — CPU_SIC — CPU_SIC 3

18,35 MBDATA2 — MBDATA2 3 — Q15 *BSS138_NL/SOT23 — CPU_SID — CPU_SID 3

SMBALERT# — Q13 *BSS138_NL/SOT23 — CPU_ALERT — CPU_ALERT 3

+3V
R149 10K/F_4, R151 10K/F_4, R148 10K/F_4

Del R150, R152 on PV

18,35 MBCLK2
18,35 MBDATA2
13 PM_THERM#

U36 G781P8 MSOP: SCLK 8, SDA 7, ALERT# 6, OVERT# 4, VCC 1, DXP 2, DXN 3, GND 5

SI-2 Modified for H/W thermal shutdown

+3V
R572 200/F_6 — Update U36 P/N on PV
C856 0.1U/10V_4
C855 2200P/50V_4

H_THRMDA 3
H_THRMDC 3

reserve for power shutdown (if can)

R170 *0_4 — SYS_SHDN# — SYS_SHDN# 38,44
D34 *CH500H
R168 0_4 — 3920_RST# — 3920_RST# 35,44
Q16 MMBT3904
D33 CH501H-40PT — ECPWROK — ECPWROK 16,35
R172 10K/F_4 — +3V

SMBALERT#

+1.8VSUS R805 *10K/F_4
+1.8VSUS R806 *300_4
Q71 *MMBT3904
CPU_THERMTRIP_L# — CPU_THERMTRIP_L# — SMBALERT#

PQ60 *2N7002E-G
R760 *10K/F_4 — TEMP_FAIL 18

ADD VGA TEMP_ FAIL function
M8X is active Hi , M7X acvite Low

+3VS5 EC13 *0.1U/10V_4, +3VS5 EC14 *0.1U/10V_4, +3V EC11 *0.1U/10V_4, +1.8V EC12 *0.1U/10V_4

+1.8VSUS EC10 0.01U/16V_4 +3VPCU
+1.8V EC5 0.01U/16V_4 +3VPCU
+1.8V EC4 0.01U/16V_4 +3V
+3VPCU EC7 0.01U/16V_4 +3V
+5V EC1 *0.01U/16V_4 +3V
EC2 *0.01U/16V_4
+VGA_CORE EC8 0.01U/16V_4 +1.8V
EC9 0.01U/16V_4

+VCORE0: C69 0.01U/16V_4, C71 0.01U/16V_4, C67 0.01U/16V_4, C64 0.01U/16V_4
+VCORE1

+1.8VSUS EC3 0.01U/16V_4 +5V
+5V EC6 0.01U/16V_4 +3VPCU

For fix HyperTransport nets across plane splits

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G2 PWR & GND 3/3	1A

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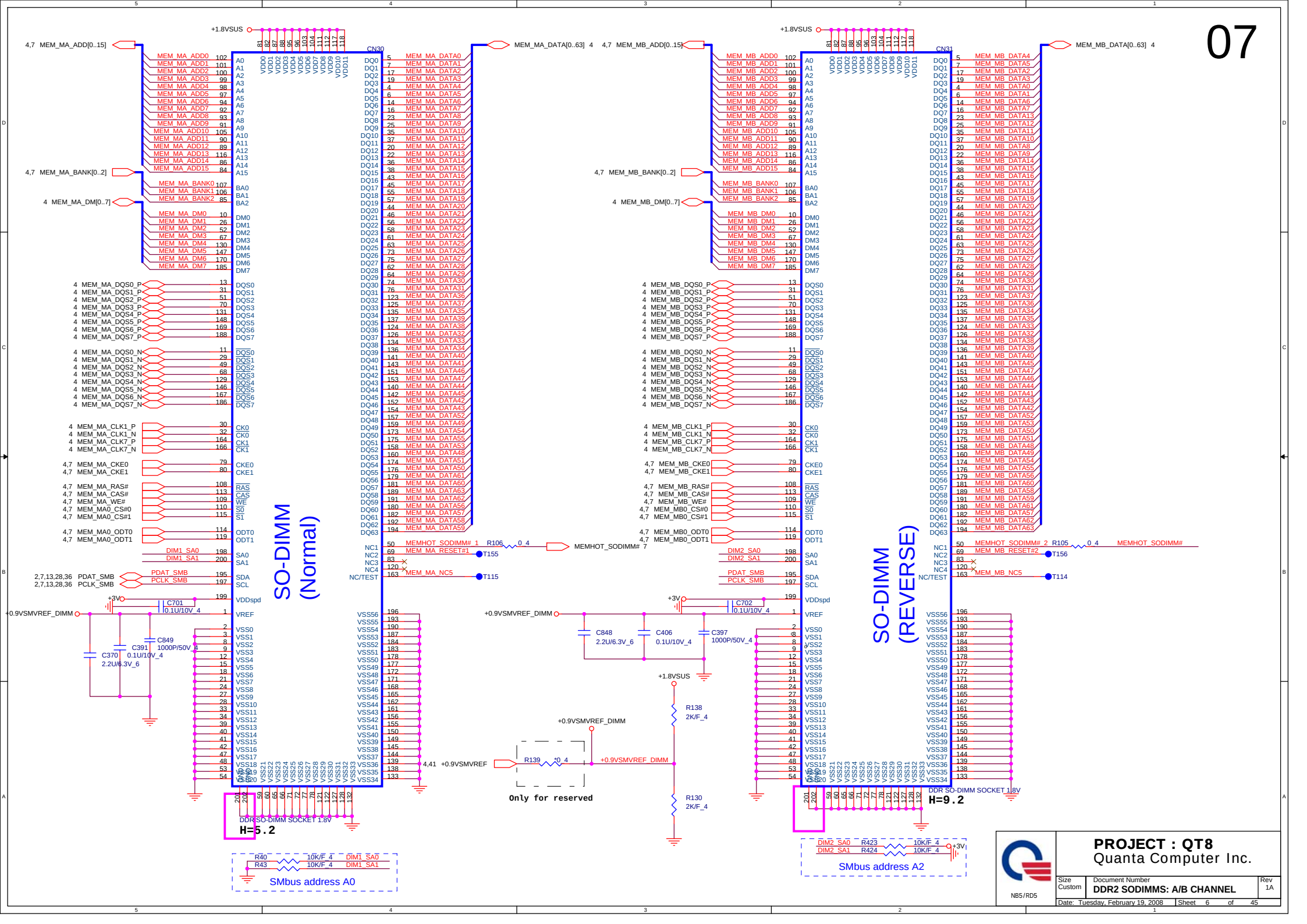

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SODIMMS: A/B CHANNEL	1A

NB5/RD5

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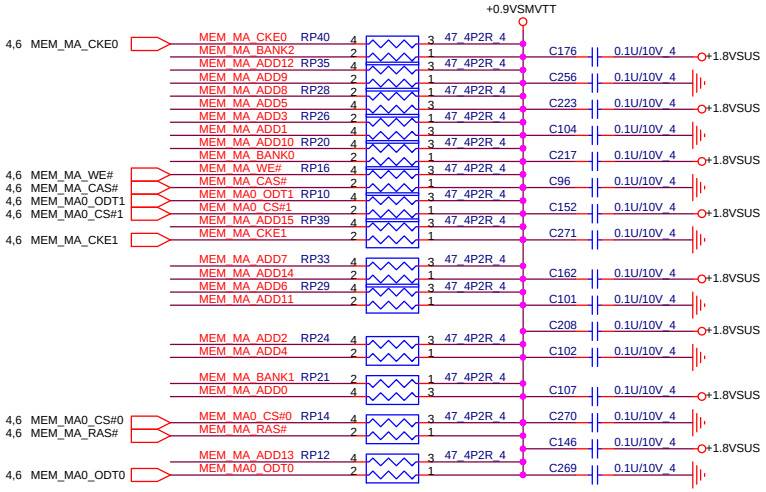
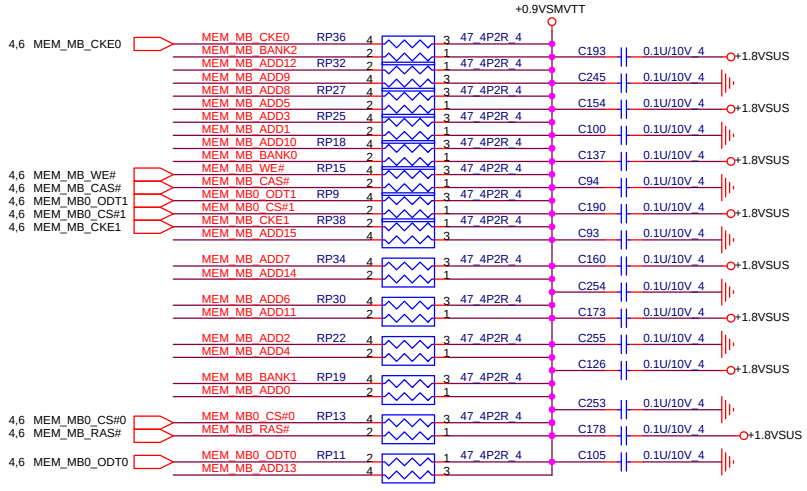
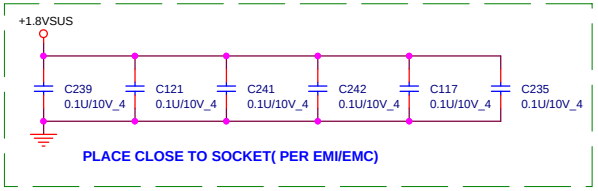
4,6 MEM_MA_ADD[0..15] — MEM_MA_ADD[0..15]
4,6 MEM_MA_BANK[0..2] — MEM_MA_BANK[0..2]

4,6 MEM_MB_ADD[0..15] — MEM_MB_ADD[0..15]
4,6 MEM_MB_BANK[0..2] — MEM_MB_BANK[0..2]

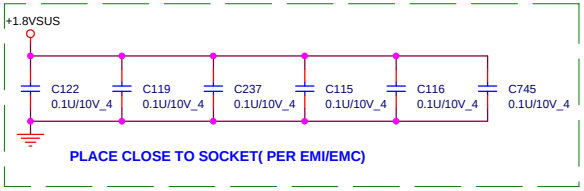


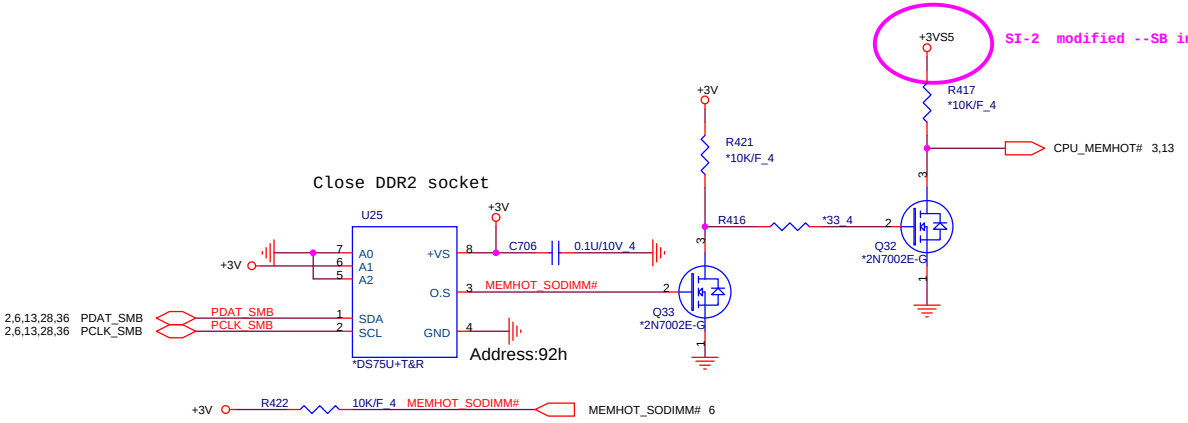


PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH





NB5/RD5	**PROJECT : QT8** Quanta Computer Inc.	
Size: Custom	Document Number: **DDR2 SODIMMS TERMINATIONS**	Rev: 1A
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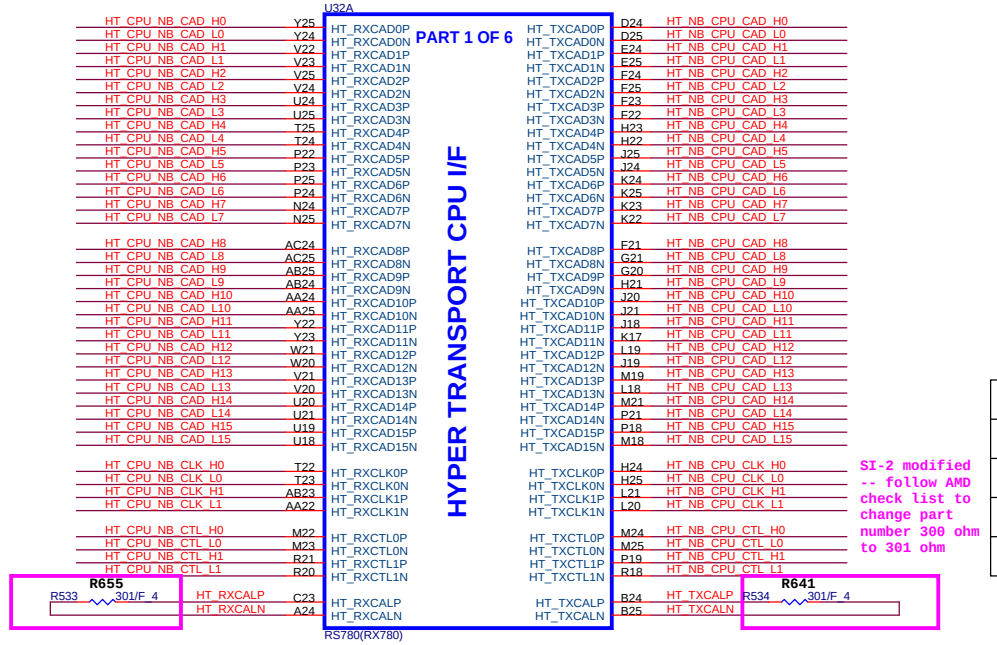
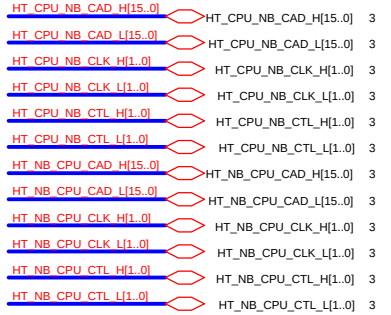
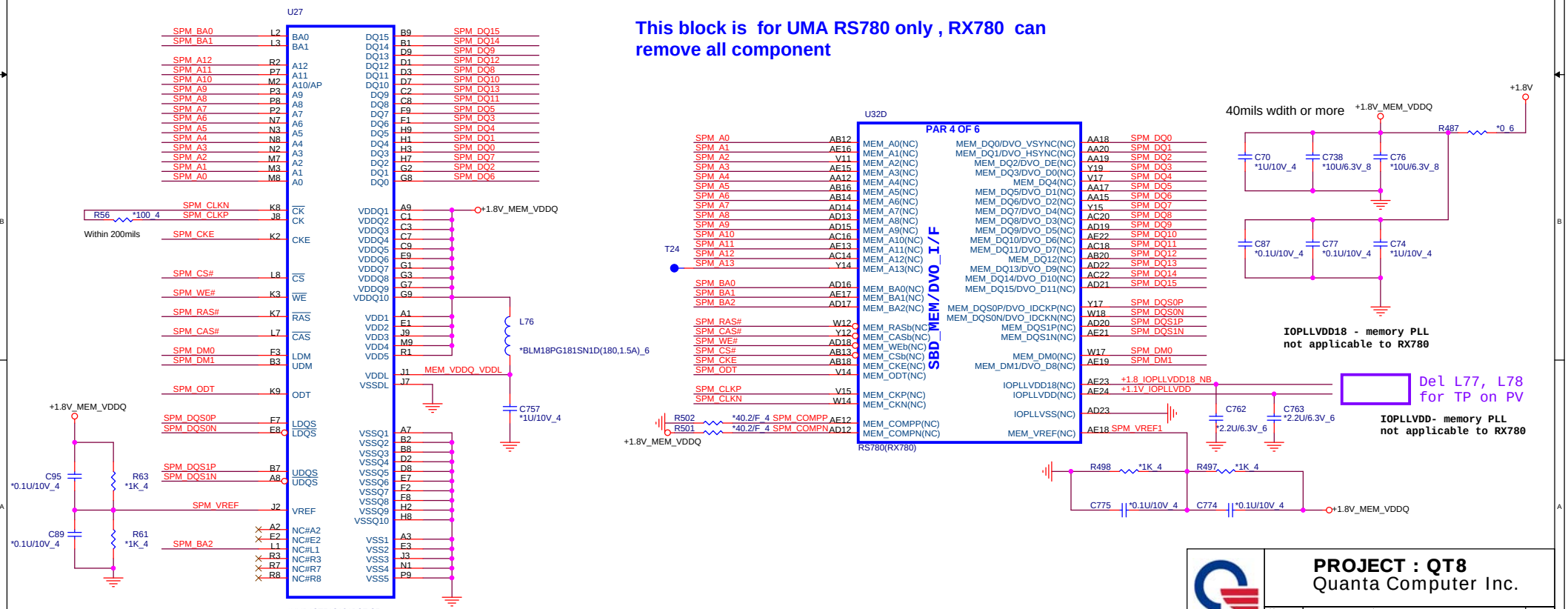


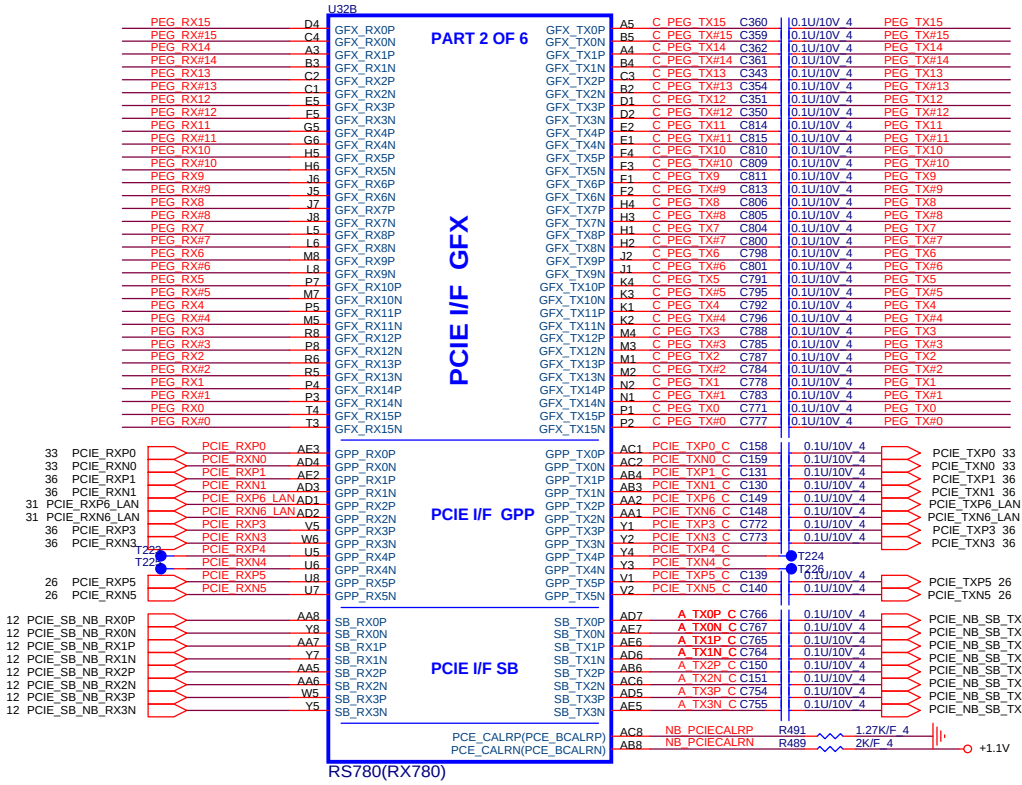


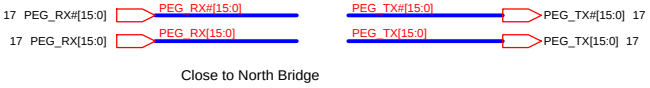
signals	RS780	RX780
HT_TXCALP	R641 301 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 301 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

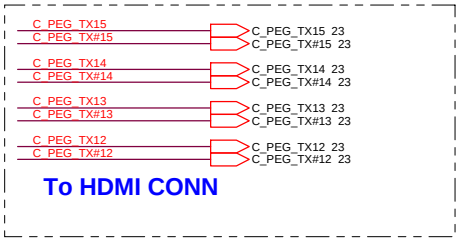
RES CHIP 301 1/16W +-1%(0402)
P/N : CS13012FB14







Close to North Bridge



TO EPRESS CARD

TO WLAN

TO PCIE-LAN

TO TV TUNNER

TO PCIE CARD READER

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

NB5/RD5

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RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

RX780
3,12 CPU_LDT_RST# — R157 *0_4 — NB_RST# IN
RS780
12 NB_PLTRST# — R160 0_4
North Bridge RESET

R109 for UAM use 140 ohm

U32C — PART 3 OF 6 — RS780(RX780)

CRT/TVOUT
18,24 CRT_R — R446 *0_4, R109 *150/F_4 — CRT_R_1 — G18
18,24 CRT_G — R445 0_4, R110 *150/F_4 — CRT_G_1 — G17
18,24 CRT_B — R444 0_4, R111 *150/F_4 — CRT_B_1 — F18
18,19,24 HSYNC_COM — R549 *0_4 — HSYNC_INT — A11
18,19,24 VSYNC_COM — R540 *0_4 — VSYNC_INT — B11
18,24 DDCDATA — R133 *0_4 — DDCDATA_INT — E8
18,24 DDCCLK — R134 *0_4 — DDCCLK_INT — F8
R119 *715/F_6 — DAC_RSET_NB — G14

PLL PWR
+1.1V_PLLVDD — A12
+1.8V_PLLVDD18 — D14, B12
+1.8V_VDDA18HTPLL — H17
+1.8V_VDDA18PCIEPLL — D7, E7

PM
16 NB_PWRGD_IN — NB_RST# IN — D8
NB_PWRGD_IN — A10
NB_LDT_STOP# — C10
NB_ALLOW_LDTSTOP — C12

CLOCKS
2 NBHT_REFCLKP — NBHT_REFCLKP — C25
2 NBHT_REFCLKN — NBHT_REFCLKN — C24
2 EXT_NB_OSC — R117 0_4 — NB_REFCLK_P — E11
NB_REFCLK_N — F11
+1.1V — R125 4.7K_4, R120 4.7K_4 — RS780 RS780
2 NBGFX_CLKP — NBGFX_CLKP — T2
2 NBGFX_CLKN — NBGFX_CLKN — T1
T168, T169
2 SBLINK_CLKP — NBGPP_CLKP — U1
2 SBLINK_CLKN — NBGPP_CLKN — U2
SBLINK_CLKP — V4
SBLINK_CLKN — V3
Del NBGPP CLK

I/O
GFX_REFCLKP, GFX_REFCLKN
GPP_REFCLKP, GPP_REFCLKN
GPPSB_REFCLKP(SB_REFCLKP), GPPSB_REFCLKN(SB_REFCLKN)

MIS.
I2C_DATA, I2C_CLK, DDC_DATA/AUX0N(NC), DDC_CLK/AUX0P(NC), AUX1P(NC), AUX1N(NC)
STRP_DATA — 39 DYN_PWR_EN — R27 0_4 STRP_DATA — B10
RSVD — G11
AUX_CAL(NC) — T164 RS780_AUX_CAL — C8
HPD(NC)
TVCLKIN(PWM_GPIO5)
THERMALDIODE_P, THERMALDIODE_N
TESTMODE — D13 TEST_EN — R541 1.82K/F_4

LVTM
TXOUT_L0P(NC) A22 LA_DATAP0 — LA_DATAP0 23
TXOUT_L0N(NC) B22 LA_DATAN0 — LA_DATAN0 23
TXOUT_L1P(NC) A21 LA_DATAP1 — LA_DATAP1 23
TXOUT_L1N(NC) B21 LA_DATAN1 — LA_DATAN1 23
TXOUT_L2P(NC) B20 LA_DATAP2 — LA_DATAP2 23
TXOUT_L2N(DBG_GPIO0) A20 LA_DATAN2 — LA_DATAN2 23
TXOUT_L3P(NC) A19 LA_DATAP3 — T159
TXOUT_L3N(DBG_GPIO2) B19 LA_DATAN3 — T157
TXOUT_U0P(NC) B18 LB_DATAP0 — LB_DATAP0 23
TXOUT_U0N(NC) A18 LB_DATAN0 — LB_DATAN0 23
TXOUT_U1P(PCIE_RESET_GPIO3) A17 LB_DATAP1 — LB_DATAP1 23
TXOUT_U1N(PCIE_RESET_GPIO2) B17 LB_DATAN1 — LB_DATAN1 23
TXOUT_U2P(NC) D20 LB_DATAP2 — LB_DATAP2 23
TXOUT_U2N(NC) D21 LB_DATAN2 — LB_DATAN2 23
TXOUT_U3P(PCIE_RESET_GPIO5) D18 LB_DATAP3 — T163
TXOUT_U3N(NC) D19 LB_DATAN3 — T160
TXCLK_LP(DBG_GPIO1) B16 LA_CLK — LA_CLK 23
TXCLK_LN(DBG_GPIO3) A16 LA_CLK# — LA_CLK# 23
TXCLK_UP(PCIE_RESET_GPIO4) D16 LB_CLK — LB_CLK 23
TXCLK_UN(PCIE_RESET_GPIO1) D17 LB_CLK# — LB_CLK# 23
VDDLTP18(NC) A13 +1.8V_VDDLTP18_NB — B13
VSSLTP18(NC)
VDDLT18_1(NC) A15 +1.8V_VDDLT_18_NB — B15
VDDLT18_2(NC)
VDDLT33_1(NC) A14 +3V_VDLT33_NB — B14
VDDLT33_2(NC)
VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22

RS780 only

LVDS_DIGON(PCE_TCALRP) E9 — R132 *0_4 — DISP_ON — DISP_ON 19,23
LVDS_BLON(PCE_RCALRP) E7 — R126 *0_4 — LVDS_BLON — LVDS_BLON 18,23
LVDS_ENA_BL(PWM_GPIO2) G12 — R118 *0_4 — DPST_PWM — DPST_PWM 19,23
R121 *1.27K/F_4
R127 *1.27K/F_4
For RX780 only

TMDS_HPD0 D9 — R545 *0_4 — TMDS_HPD — TMDS_HPD 18,23
TMDS_HPD1 D10 — T162
SUS_STAT# NB D12 — R131 0_4 — SUS_STAT# 13
R_NB_THRMDA AE8 — T136
R_NB_THRMDC AD8 — T135
UMA only

RS780 only
+3V — R536 4.7K_4 HDTV_DET
R539 4.7K_4 NB_I2C_DATA
R538 4.7K_4 NB_I2C_CLK
18,23 EDIDDATA — R547 *0_4 — NB_I2C_DATA — A9
18,23 EDIDCLK — R546 *0_4 — NB_I2C_CLK — B9
23 HDMI_DDC_DATA — R537 *0_4 — HDTV_DET — B8
23 HDMI_DDC_CLK — R544 *0_4 — RS740_DFT_GPIO0 — A8
RS740_DFT_GPIO1 — B7
T161, T158 — A7

---

selects Loading of straps from EPROM
1 : use default vaule , default
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT

RX780
RS780_AUX_CAL — R543 3K_4

Enables Debug Bus acess through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)

RS780
VSYNC_COM — R124 3K_4 — +3V

Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)

RS780
HSYNC_COM — R129 3K_4 — +3V
R136 *3K_4

For extrnal EEPROM Debug only

RS780/RX780
STRP_DATA — R548 10K/F_4 — +VDDG_NB
R558 *10K/F_4

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RX780 , Default
0 : Disable RX780

RX780
S-CD1 — R810 *3K_4
Reserved only

RX780 -->NC / RS780 --- ADD

AVDD-DAC Analog not applicable to RX780
+3V — L35 BLM18PG181SN1D(180,1.5A)_6 — +3V_AVDD_NB
C340 2.2U/6.3V_6

PLLVDD18 - Graphics PLL not applicable to RX780
+1.8V — L33 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_PLLVDD18
C405 10U/6.3V_8
C333 2.2U/6.3V_6

PLLVDD - Graphics PLL not applicable to RX780
+1.1V — L82 BLM18PG181SN1D(180,1.5A)_6 — +1.1V_PLLVDD
C842 2.2U/6.3V_6

AVDDI-DAC Digital not applicable to RX780
+1.8V — R107 0_6 — +1.8V_AVDDDI_NB
C321 2.2U/6.3V_6

AVDDQ-DAC Bandgap Reference not applicable to RX780
L34 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_AVDDQ_NB
C349 2.2U/6.3V_6

VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780
+1.8V — L83 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_VDDLTP18_NB
C841 2.2U/6.3V_6

VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780
L85 BLM21PG221SN1D(220,100M,2A)_8 — +1.8V_VDDLT_18_NB
C846 4.7U/6.3V_6
C838 0.1U/10V_4

VDDA18PCIEPLL -PCIE PLL
+1.8V — L32 BLM18PG181SN1D(180,1.5A)_6 — 20mils width — +1.8V_VDDA18PCIEPLL
C358 2.2U/6.3V_6

VDDA18HTPLL -HT LINK PLL
L31 BLM18PG181SN1D(180,1.5A)_6 — 20mils width — +1.8V_VDDA18HTPLL
C356 2.2U/6.3V_6

RS780
Q37 BSS138_NL/SOT23
3,12 CPU_LDT_STOP# — R555 *0_4 — NB_LDT_STOP#
+1.8V — R556 4.7K_4 — +VDDG_NB
RX780

RS780
Q38 BSS138_NL/SOT23
3 CPU_LDT_REQ# — R568 0_4 — NB_ALLOW_LDTSTOP
12 ALLOW_LDTSTOP — R564 *0_4
+1.8V — R557 4.7K_4 — +VDDG_NB
RX780

RX780
R566 *0_6 — +1.8V — +VDDG_NB
RS780
R565 0_6 — +3V

VDDLT33 - LVDS or DVI/HDMI ANALOG RS740 only
L84 *BLM21PG221SN1D(220,100M,2A)_8 — +3V_VDLT33_NB
C844 *2.2U/6.3V_6

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-SYSTEM I/F 3/5	1A
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RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC

PART 6/6 — GROUND

VSSAPCIE1 VSSAPCIE2 VSSAPCIE3 VSSAPCIE4 VSSAPCIE5 VSSAPCIE6 VSSAPCIE7 VSSAPCIE8 VSSAPCIE9 VSSAPCIE10 VSSAPCIE11 VSSAPCIE12 VSSAPCIE13 VSSAPCIE14 VSSAPCIE15 VSSAPCIE16 VSSAPCIE17 VSSAPCIE18 VSSAPCIE19 VSSAPCIE20 VSSAPCIE21 VSSAPCIE22 VSSAPCIE23 VSSAPCIE24 VSSAPCIE25 VSSAPCIE26 VSSAPCIE27 VSSAPCIE28 VSSAPCIE29 VSSAPCIE30 VSSAPCIE31 VSSAPCIE32 VSSAPCIE33 VSSAPCIE34 VSSAPCIE35 VSSAPCIE36 VSSAPCIE37 VSSAPCIE38 VSSAPCIE39 VSSAPCIE40

VSSAHT1 VSSAHT2 VSSAHT3 VSSAHT4 VSSAHT5 VSSAHT6 VSSAHT7 VSSAHT8 VSSAHT9 VSSAHT10 VSSAHT11 VSSAHT12 VSSAHT13 VSSAHT14 VSSAHT15 VSSAHT16 VSSAHT17 VSSAHT18 VSSAHT19 VSSAHT20 VSSAHT21 VSSAHT22 VSSAHT23 VSSAHT24 VSSAHT25 VSSAHT26 VSSAHT27

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34

+1.1V 2A for RS780M

VDDHT - HT LINK digital I/O for RX780/RS780

+1.1V — 0.6A — L72 BLM21PG221SN1D(220,100M,2A)_8 — +1.1V_VDDHT

C770 4.7U/6.3V_6, C274 0.1U/10V_4, C313 0.1U/10V_4, C280 0.1U/10V_4

VDDHTRX - HT LINK RX I/O for RX780/RS780

0.45A — L81 BLM21PG221SN1D(220,100M,2A)_8 — +1.1V_VDDHTRX

C847 4.7U/6.3V_6, C323 0.1U/10V_4, C843 0.1U/10V_4, C839 0.1U/10V_4

+1.2V 2A for RS780M+SB700

+1.2V — L12 BLM21PG221SN1D(220,100M,2A)_8

+1.35V — L13 BLM21PG221SN1D(220,100M,2A)_8

0.5A — +1.2V_VDDHTTX

C124 4.7U/6.3V_6, C195 0.1U/10V_4, C194 0.1U/10V_4, C249 0.1U/10V_4, C199 0.1U/10V_4

+1.35V for A1-1 chip bug , A1-2 can remove

VDDHTTX - HT LINK TX I/O for RX780/RS780

+1.8V 1A for RS780M+SB700

+1.8V — L22 BLM21PG221SN1D(220,100M,2A)_8 — 600mA — +1.8V_VDDA18PCIE

C188 4.7U/6.3V_6, C175 4.7U/6.3V_6, C258 0.1U/10V_4, C209 0.1U/10V_4, C302 0.1U/10V_4, C234 0.1U/10V_4

VDDA18PCIE - PCIE TX stage I/O for RX780/RS780

VDD18 - RS780 I/O transform

+1.8V — R122 0_6 — 0.005A — C317 1U/10V_4 — +1.8V_VDDG18_NB

+1.8V — R499 0_6 — 0.005A — C769 1U/10V_4 — +1.8V_VDD18_MEM

VDD18_MEM For UMA RS780 only Not applicable to RX780 memory I/O transform

U32E — PART 5/6 — POWER — RS780(RX780)

VDDHT_1 VDDHT_2 VDDHT_3 VDDHT_4 VDDHT_5 VDDHT_6 VDDHT_7 — J17 K16 L16 M16 P16 R16 T16

VDDHTRX_1 VDDHTRX_2 VDDHTRX_3 VDDHTRX_4 VDDHTRX_5 VDDHTRX_6 VDDHTRX_7 — H18 G19 F20 E21 D22 B23 A23

VDDHTTX_1 VDDHTTX_2 VDDHTTX_3 VDDHTTX_4 VDDHTTX_5 VDDHTTX_6 VDDHTTX_7 VDDHTTX_8 VDDHTTX_9 VDDHTTX_10 VDDHTTX_11 VDDHTTX_12 VDDHTTX_13 — AE25 AD24 AC23 AB22 AA21 Y20 W19 V18 U17 T17 R17 P17 M17

VDDA18PCIE_1 VDDA18PCIE_2 VDDA18PCIE_3 VDDA18PCIE_4 VDDA18PCIE_5 VDDA18PCIE_6 VDDA18PCIE_7 VDDA18PCIE_8 VDDA18PCIE_9 VDDA18PCIE_10 VDDA18PCIE_11 VDDA18PCIE_12 VDDA18PCIE_13 VDDA18PCIE_14 VDDA18PCIE_15 — J10 P10 K10 M10 L10 W9 H9 T10 R10 Y9 AA9 AB9 AD9 AE9 U10

VDDG18_1(VDD18_1) VDDG18_2(VDD18_2) VDD18_MEM1(NC) VDD18_MEM2(NC) — F9 G9 AE11 AD11

VDDPCIE_1 VDDPCIE_2 VDDPCIE_3 VDDPCIE_4 VDDPCIE_5 VDDPCIE_6 VDDPCIE_7 VDDPCIE_8 VDDPCIE_9 VDDPCIE_10 VDDPCIE_11 VDDPCIE_12 VDDPCIE_13 VDDPCIE_14 VDDPCIE_15 VDDPCIE_16 VDDPCIE_17 — A6 B6 C6 D6 E6 F6 G7 H8 J9 K9 M9 L9 P9 R9 T9 V9 U9

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22 — K12 J14 U16 J11 K15 M12 L14 L11 M13 M15 N12 N14 P11 P13 P14 R12 R15 T11 T15 U12 T14 J16

VDD_MEM1(NC) VDD_MEM2(NC) VDD_MEM3(NC) VDD_MEM4(NC) VDD_MEM5(NC) VDD_MEM6(NC) — AE10 AA11 Y11 AD10 AB10 AC10

VDDG33_1(NC) VDDG33_2(NC) — H11 H12

VDDPCIE - PCIE-E Main power

+1.1V_VDD_PCIE — 0.7A — R542 0_8 — +1.1V

C275 0.1U/10V_4, C337 0.1U/10V_4, C318 1U/10V_4, C328 1U/10V_4, C845 4.7U/6.3V_6

VDDC - Core Logic power

7A — +1.1V_DYN

C251 0.1U/10V_4, C292 0.1U/10V_4, C297 0.1U/10V_4, C303 0.1U/10V_4, C59 10U/6.3V_8

C281 0.1U/10V_4, C278 0.1U/10V_4, C250 0.1U/10V_4, C60 10U/6.3V_8

VDD_MEM For UMA RS780 only Not applicable to RX780 memory I/O transform

+1.8V_VDD_MEM — 1.8V(0.15A) — L23 BLM21PG221SN1D(220,100M,2A)_8 — +1.8V

C192 0.1U/10V_4, C179 0.1U/10V_4, C172 0.1U/10V_4, C216 0.1U/10V_4, C153 4.7U/6.3V_6

+3V_VDDG33 — R123 RS780 0_6 — 3.3V(0.03A) — +3V

C336 0.1U/10V_4, C329 0.1U/10V_4

VDD33 - 3.3V I/O Not applicable to RX780

NB5/RD5	PROJECT : QT8 Quanta Computer Inc.	
Size: Custom	Document Number: RS740/RS780-POWER5/5	Rev: 1A
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PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600

To RS780

U37A
SB700
Part 1 of 5

PCIE_PVDD-- PCIE PLL POWER

+1.2V_PCIE_VDDR
+1.2V
L44 BLM18PG181SN1D(180,1.5A)_6
+1.2V_PCIE_PVDD
40mA
C485 10U/6.3V_8
C503 1U/10V_4

PCI EXPRESS INTERFACE
PCI CLKS
PCI INTERFACE
CLOCK GENERATOR
RTC XTAL
LPC
CPU
RTC

Del R639, R640, R641, R642 on PV

PCI_CLK_TPM 16
PCI_CLK3 16
PCI_CLK4 16
PCI_CLK5 16

PCIRST# 35

All the PCI bus has build-in Pull-UP/Down resistors

change D21, D20 type for PV

SI-2 mofified for satify -- remove R560 , add R796 ,R797

SI-2 Modified-- for power leakage issue

Del R783 for TP on PV

SI-2 Modified-- Add GPIO pin for control D3E wake up (need low 1ms for Jmicron request)

R589 change to 10 ohm on PV

100MHZ

32.768KHZ

If CPU have pull Hi ,this pin should be not need

PV-1 Modified -- change to pull hi to 3VS5 for power leakage issue

SI-1 Modified - for EMI

SI-2 modified -- for EMI suggestion

SI-2 Modified--reserve

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

SB700
IC CTRL(528P) SB700 A11(218S7EALA11FG)
P/N : AJALA110T00

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

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NC only ,Can't be install

+3VSUS R297 *2.2K_4 SB_TEST0
R240 *2.2K_4 SB_TEST1
R287 *2.2K_4 SB_TEST2

+3VSUS R289 *10K/F_4 SWI#

+3V SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R245 2.2K_4 PCLK_SMB
R253 2.2K_4 PDAT_SMB

Clock gen/Robson/TV tuner
/DDR2/DDR2
thermal/Accelerometer

+3VS5 SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R648 *2.2K_4 SB_SMBCLK1
R649 *2.2K_4 SB_SMBDATA1

remove pull hi
(chip internal
have pull hi)

+3VS5 SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R222 *2.2K_4 SB_SCLK2
R227 *2.2K_4 SB_SDATA2

+3V R276 4.7K_4 SUS_STAT#
G4
2 1 SYS_RST#
*SHORT_ PAD1

+3VS5 R763 2.2K_4 DNBSWON#

SI-2 modified add D3E function

SI-2 modified -- Change lan disable control from SB to EC SB reserve

D3E_SCI# from Gevent5# change to Gevent7# on PV

SI-2 modified Del D35

HD audio interface is 3.3S5 voltage

SI-2 Modified --for EMI suggestion

SI-2 Modified -- discrete remove RP56

U37D

SB700 Part 4 of 5

NEWCARD_DETECT E1
RI# E2
SLP_S2 H7
SUSB# F5
SUSC# G1
DNBSWON# H2
SB_PWRGD_IN H1
SUS_STAT# K3
SB_TEST2 H5
SB_TEST1 H4
SB_TEST0 H3
GATEA20 Y15
RCIN# W15
SCI# K4
KBSMI# K24
GEVENT5# F1
SYS_RST# J2
PCIE_WAKE# H6
SWI# F2
SB_THERMTRIP# J6
WD_PWRGD W14
RSMRST# D3

PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS

SATA_IS1 AE18
LAN_DISABLE# SB AD18
SB_NWD_CLK_REQ# AA19
W17
Y17
W20
W21
AA18
W18
K1
K2
AA20
Y18
C1
Y19
G5

SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#

GPIO

USB_OC6#/IR_TX1/GEVENT6# B9
USB_OC5#/IR_TX0/GPM5# B8
USB_OC4#/IR_RX0/GPM4# A8
USB_OC3#/IR_RX1/GPM3# A9
USB_OC2#/GPM2# E5
USB_OC1#/GPM1# F8
USB_OC0#/GPM0# E4

USB OC

ACZ_BCLK M1
ACZ_SDOUT M2
ACZ_SDIN0_R J7
ACZ_SDIN1_R J8
L8
M3
L6
M4
L5

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#

HD AUDIO

H19 IMC_GPIO0
H20 IMC_GPIO1
H21 SPI_CS2#/IMC_GPIO2
F25 IDE_RST#/F_RST#/IMC_GPO3
D22 IMC_GPIO4
E24 IMC_GPIO5
E25 IMC_GPIO6
D23 IMC_GPIO7

INTEGRATED uC

USBCLK/14M_25M_48M_OSC C8 CLK_48M_USB CLK_48M_USB 2
USB_RCOMP G8 USB_RCOMP_SB R267 11.8K/F_6

USB MISC

USB_FSD13P E6 USB_FSD13P T101
USB_FSD13N E7 USB_FSD13N T199
USB_FSD12P F7 USB_FSD12P T91
USB_FSD12N E8 USB_FSD12N T93

USB 1.1

USB_HSD11P H11 USBP11+ 36 TV Min-Card
USB_HSD11N J10 USBP11- 36
USB_HSD10P E11 USBP10+ 36 WLAN Min-Card
USB_HSD10N F11 USBP10- 36
USB_HSD9P A11 USBP9+ 30 USB Connector
USB_HSD9N B11 USBP9- 30
USB_HSD8P C10 USBP8+ 30 USB Connector
USB_HSD8N D10 USBP8- 30
USB_HSD7P G11 USBP7+ 33 NEW CARD
USB_HSD7N H12 USBP7- 33
USB_HSD6P E12 USBP6+ 30 FINGERPRINT
USB_HSD6N E14 USBP6- 30
USB_HSD5P C12 USBP5+ 30 BLUETOOTH
USB_HSD5N D12 USBP5- 30
USB_HSD4P B12 USBP4+ 37 Docking
USB_HSD4N A12 USBP4- 37
USB_HSD3P G12 USBP3+ USB card reader or Touch screen
USB_HSD3N G14 USBP3-
USB_HSD2P H14 USBP2+ 30 Carama USB
USB_HSD2N H15 USBP2- 30
USB_HSD1P A13 USBP1+ 30 E-SATA and USB Connector
USB_HSD1N B13 USBP1- 30
USB_HSD0P B14 USBP0+ 30 USB Connector
USB_HSD0N A14 USBP0- 30

USB 2.0

IMC_GPIO8 A18
IMC_GPIO9 B18
IMC_PWM0/IMC_GPIO10 F21
SCL2/IMC_GPIO11 D21 SB_SCLK2
SDA2/IMC_GPIO12 F19 SB_SDATA2
SCL3_LV/IMC_GPIO13 E20 SB_SCLK3 T64
SDA3_LV/IMC_GPIO14 F21 SB_SDATA3 T70
IMC_PWM1/IMC_GPIO15 E19
IMC_PWM2/IMC_GPO16 D19 SB_GPIO16 SB_GPIO16 16
IMC_PWM3/IMC_GPO17 E18 SB_GPIO17 SB_GPIO17 16 SPI/LPC define

IMC_GPIO18 G20
IMC_GPIO19 G21
IMC_GPIO20 D25
IMC_GPIO21 D24
IMC_GPIO22 C25
IMC_GPIO23 C24
IMC_GPIO24 B25
IMC_GPIO25 C23
IMC_GPIO26 B24
IMC_GPIO27 B23
IMC_GPIO28 A23
IMC_GPIO29 C22
IMC_GPIO30 A22
IMC_GPIO31 B22
IMC_GPIO32 B21
IMC_GPIO33 A21
IMC_GPIO34 D20
IMC_GPIO35 C20
IMC_GPIO36 A20
IMC_GPIO37 B20
IMC_GPIO38 B19
IMC_GPIO39 A19
IMC_GPIO40 D18
IMC_GPIO41 C18

INTEGRATED uC

SB700

CLK_48M_USB
C554 *2.2P/50V_4

for EMI & del R268 change 2.2P

To Azalia

ACZ_SDOUT R644 33_4 ACZ_SDOUT_AUDIO 27
C908 *10P/50V_4
ACZ_SYNC R290 33_4 ACZ_SYNC_AUDIO 27
C569 *10P/50V_4
ACZ_BCLK R646 33_4 BIT_CLK_AUDIO 27
C910 10P/50V_4
ACZ_RST# R296 33_4 ACZ_RST#_AUDIO 27
ACZ_SDIN0_R R295 0_4 ACZ_SDIN0 27

To Modem Board

ACZ_SDOUT R645 33_4 ACZ_SDOUT_AUDIO_MDC 29
C909 *10P/50V_4
ACZ_SYNC R292 33_4 ACZ_SYNC_AUDIO_MDC 29
C577 *10P/50V_4
ACZ_BCLK R647 33_4 BIT_CLK_AUDIO_MDC 29
C911 10P/50V_4
ACZ_RST# R293 33_4 ACZ_RST#_AUDIO_MDC 29
ACZ_SDIN1_R R286 0_4 ACZ_SDIN1 29

+3VS5 R592 22K_4 HDD_AUX_RST#

SB JTAG
CN16
+3VSUS C462 10P/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG

USBP3-
USBP3+
CLOSE TO SB
RP50 *0_4P2R_4
USBP6_CR- 25
USBP6_CR+ 25
UMA

+3VS5 R764 2K/04 +3V
33,36 SCLK_WLAN Q66 PCLK_SMB
2N7002EPT

+3VS5 R765 2K/04 +3V
33,36 SDATA_WLAN PDAT_SMB
2N7002EPT Q67

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NB5/RD5

SATA PORT 0,1,2,3 can support AHCI mode

SATA1

SATA ODD

E-SATA

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

U37B

SB700
Part 2 of 5

SERIAL ATA

SATA_TX0P / SATA_TX0N — AD9 / AE9
SATA_RX0N / SATA_RX0P — AB10 / AC10
SATA_TX1P / SATA_TX1N — AE10 / AD10
SATA_RX1N / SATA_RX1P — AD11 / AE11
SATA_TX2P / SATA_TX2N — AB12 / AC12
SATA_RX2N / SATA_RX2P — AE12 / AD12
SATA_TX3P / SATA_TX3N — AD13 / AE13
SATA_RX3N / SATA_RX3P — AB14 / AC14
SATA_TX4P / SATA_TX4N — AE14 / AD14
SATA_RX4N / SATA_RX4P — AD15 / AE15
SATA_TX5P / SATA_TX5N — AB16 / AC16
SATA_RX5N / SATA_RX5P — AE16 / AD16
SATA_CAL — V12
SATA_X1 — Y12
SATA_X2 — AA12
SATA_ACT#/GPIO67 — W11

SATA PWR

PLLVDD_SATA — AA11
XTLVDD_SATA — W12

ATA 66/100/133

IDE_IORDY AA24 — T231
IDE_IRQ AA25 — T232
IDE_A0 Y22 — T233
IDE_A1 AB23 — T234
IDE_A2 Y23 — T235
IDE_DACK# AB24 — T236
IDE_DRQ AD25 — T237
IDE_IOR# AC25 — T238
IDE_IOW# AC24 — T239
IDE_CS1# Y25 — T240
IDE_CS3# Y24 — T241

IDE_D0/GPIO15 AD24 — T242
IDE_D1/GPIO16 AD23 — T243
IDE_D2/GPIO17 AE22 — T244
IDE_D3/GPIO18 AC22 — T245
IDE_D4/GPIO19 AD21 — T246
IDE_D5/GPIO20 AE20 — T247
IDE_D6/GPIO21 AB20 — T248
IDE_D7/GPIO22 AD19 — T249
IDE_D8/GPIO23 AE19 — T250
IDE_D9/GPIO24 AC20 — T251
IDE_D10/GPIO25 AD20 — T252
IDE_D11/GPIO26 AE21 — T253
IDE_D12/GPIO27 AB22 — T254
IDE_D13/GPIO28 AD22 — T255
IDE_D14/GPIO29 AE23 — T256
IDE_D15/GPIO30 AC23 — T257

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

SPI ROM

SPI_DI/GPIO12 G6 — T100
SPI_DO/GPIO11 D2 — T219
SPI_CLK/GPIO47 D1 — T218
SPI_HOLD#/GPIO31 E4 — T111
SPI_CS#/GPIO32 E3 — T220

LAN_RST#/GPIO13 U15 — R265 0_4 — BT_OFF# 30
ROM_RST#/GPIO14 J1 — ROM_RST# — T215

FANOUT0/GPIO3 M8 — SB_FANOUT0 — T96
FANOUT1/GPIO48 M5 — SB_FANOUT1 — T97
FANOUT2/GPIO49 M7 — CHIPSET_PCIE_SLOW_SB# 2

HW MONITOR

FANIN0/GPIO50 P5 — SB_FANTACH0 — T104
FANIN1/GPIO51 P8 — SB_FANTACH1 — T92
FANIN2/GPIO52 R8 — PORT_80_PWR_DWN — T95

TEMP_COMM C6 — TEMP_COMM — T208
TEMPIN0/GPIO61 B6 — TEMPIN0 — T202
TEMPIN1/GPIO62 A6 — TEMPIN1 — T203
TEMPIN2/GPIO63 A5 — MB_THRMDA_SB — T207
TEMPIN3/TALERT#/GPIO64 B5 — T259

Del R220 for TP on PV

VIN0/GPIO53 A4 — R216 0_4 — ACCLED_EN 29
VIN1/GPIO54 B4 — BT_COMBO_EN# 36
VIN2/GPIO55 C4
VIN3/GPIO56 D4 — BOARD_ID0
VIN4/GPIO57 D5 — BOARD_ID1
VIN5/GPIO58 D6 — BOARD_ID2
VIN6/GPIO59 A7 — BOARD_ID3
VIN7/GPIO60 B7 — BOARD_ID4

Del WAN off# and R597 on PV

AVDD F6 — 5mA — +3V_VDD_HWM — L52 0_6 — +3VS5
AVSS G7 — C571 *0.1U/10V_4 — C572 *2.2U/6.3V_6

AVDD--H/W monitor Analog power

SI-2 modified -- for fix +3V power leakage in S5 mode

SB700

SATA PORT 4,5 are only support IDE mode

R361 R264 1K/F_4 — SATA_RBIAS_PN

NOTE:
PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700
R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

PLVDD_SATA-- SATA PLL POWER

SB_SATA_LED# — R382 10K/F_4 — +3V
+1.2V_PLLVDD_SATA
+3V_XTLVDD_SATA

XTLVDD_SATA-- SATA crystal power

C534 27P/50V_4 — Y4 25MHZ — R262 10M_6 — C517 27P/50V_4 — SATA_X1 / SATA_X2

SI-2 modified -- SB internal pull Hi to 3VS5 , modified to same power rail with SB

+3VS5
R221 10K/F_4 BOARD_ID0 R229 *10K/F_4
R247 *10K/F_4 BOARD_ID1 R248 *10K/F_4
R225 *10K/F_4 BOARD_ID2 R228 *10K/F_4
R230 *10K/F_4 BOARD_ID3 R242 *10K/F_4
R596 *10K/F_4 BOARD_ID4 R600 *10K/F_4

ID4	ID3	ID2	ID1	ID0	
X	X	X	0	0	UMA
X	X	X	0	1	discrete
X	X	X	X	X	
X	X	X	X	X	

+3V — C655 0.1U/10V_4 — U20 TC7SH08FU — 29 SATA_LED# — SB_SATA_LED#

SI-2 modified for SATA LED fail issue

+1.2V (1.2V @ 60mA) — L47 BLM18PG181SN1D(180,1.5A)_6 — +1.2V_PLLVDD_SATA 77mA
C524 1U/10V_4 — C550 0.1U/10V_4

+3V (3.3V @ 1.2mA) — L46 BLM18PG181SN1D(180,1.5A)_6 — +3V_XTLVDD_SATA 1mA
C539 1U/10V_4

Place near ball

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

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PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

For SB700 issue(6/22)
A1-1 chip bug
use A1-2 chip can remove

23

Del R285 for TP on PV

VDDQ--3.3V I/O power

0.8A

VDD-- S/B CORE power

604mA

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power

0.45A

CKVDD_1.2V-- Internal clock Generator I/O power

286mA

POWER

PCIE_VDDR--PCIE I/O power

844mA

S5_3.3--3.3v standby power

0.01A

AVDD_SATA--SATA phy power

0.2A

S5_1.2V--1.2V standby power

0.22A

Del R661 for TP on PV

0.2A

For support USB wakeup-->3V_S5

AVDDTX--USB Phy Analog I/O power

0.2A

V5_VREF--PCI 5V TOLERANCE

4mA

7mA

44mA

16mA

USB_PHY_1.2V--USB Phy digital power

AVDDC--USB Analog PLL power

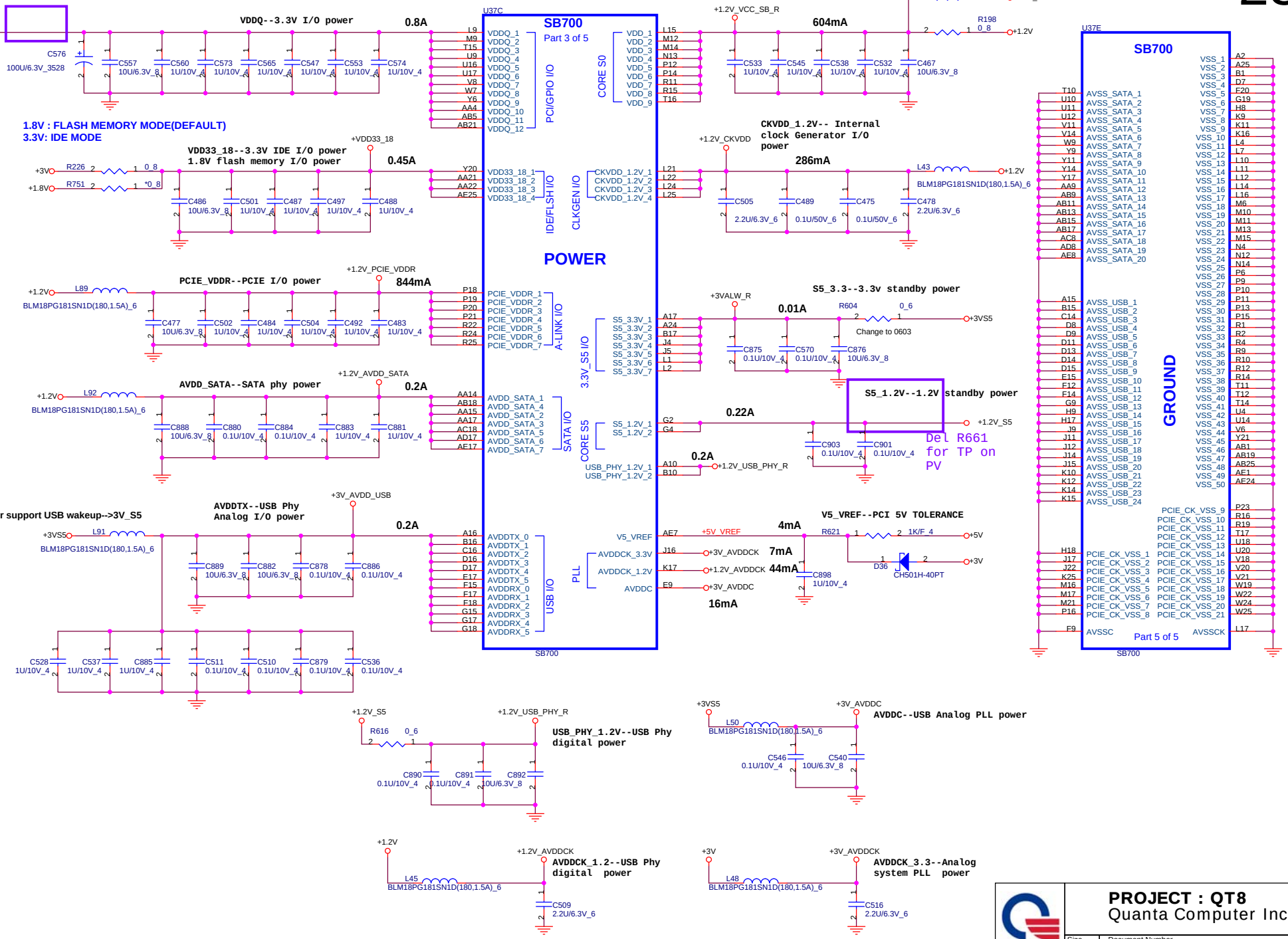
AVDDCK_1.2--USB Phy digital power

AVDDCK_3.3--Analog system PLL power

SB700
Part 3 of 5

SB700
Part 5 of 5

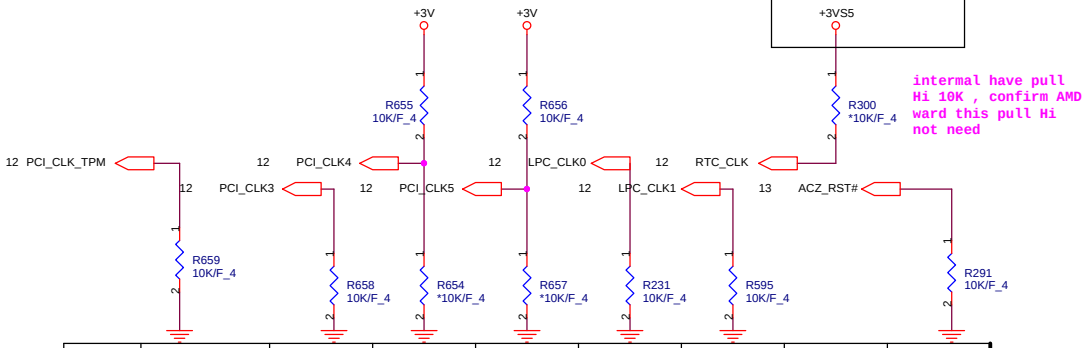
GROUND



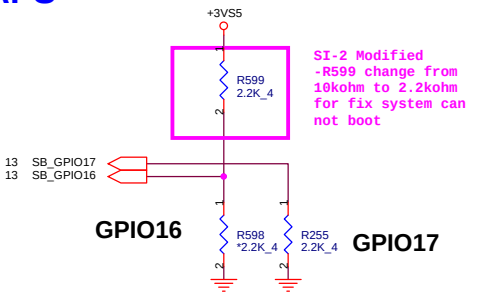
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

REQUIRED STRAPS



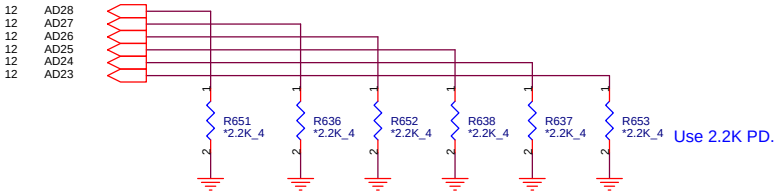
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

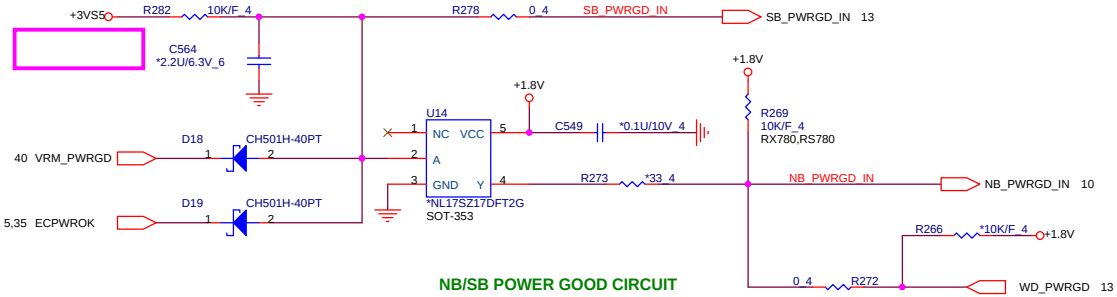


	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

SI-2 modified -- confirm AMD R563 need to stuff

SI-2 modified -- remove +3V pull Hi resistor .



NB/SB POWER GOOD CIRCUIT

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

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IC CTRL(632P) 216-0707001-00(BGA)
VGA P/N : AJ070700T00

2.5Gb/s bit rate

PART 1 OF 6

PCI-EXPRESS INTERFACE

9	PEG_TX0	PEG_TX0	AC30	PCIE_RX0P	PCIE_TX0P	AA28	C_PEG_RXP0	C163	0.1U/10V_4	PEG_RX0	9
9	PEG_TX#0	PEG_TX#0	AC31	PCIE_RX0N	PCIE_TX0N	AA27	C_PEG_RXN0	C156	0.1U/10V_4	PEG_RX#0	9
9	PEG_TX1	PEG_TX1	AC29	PCIE_RX1P	PCIE_TX1P	AA25	C_PEG_RXP1	C167	0.1U/10V_4	PEG_RX1	9
9	PEG_TX#1	PEG_TX#1	AB29	PCIE_RX1N	PCIE_TX1N	AA24	C_PEG_RXN1	C170	0.1U/10V_4	PEG_RX#1	9
9	PEG_TX2	PEG_TX2	AB31	PCIE_RX2P	PCIE_TX2P	Y28	C_PEG_RXP2	C180	0.1U/10V_4	PEG_RX2	9
9	PEG_TX#2	PEG_TX#2	AB30	PCIE_RX2N	PCIE_TX2N	Y27	C_PEG_RXN2	C196	0.1U/10V_4	PEG_RX#2	9
9	PEG_TX3	PEG_TX3	AA31	PCIE_RX3P	PCIE_TX3P	Y25	C_PEG_RXP3	C164	0.1U/10V_4	PEG_RX3	9
9	PEG_TX#3	PEG_TX#3	AA30	PCIE_RX3N	PCIE_TX3N	Y24	C_PEG_RXN3	C157	0.1U/10V_4	PEG_RX#3	9
9	PEG_TX4	PEG_TX4	W30	PCIE_RX4P	PCIE_TX4P	V28	C_PEG_RXP4	C218	0.1U/10V_4	PEG_RX4	9
9	PEG_TX#4	PEG_TX#4	W31	PCIE_RX4N	PCIE_TX4N	V27	C_PEG_RXN4	C204	0.1U/10V_4	PEG_RX#4	9
9	PEG_TX5	PEG_TX5	W29	PCIE_RX5P	PCIE_TX5P	V25	C_PEG_RXP5	C203	0.1U/10V_4	PEG_RX5	9
9	PEG_TX#5	PEG_TX#5	V29	PCIE_RX5N	PCIE_TX5N	V24	C_PEG_RXN5	C187	0.1U/10V_4	PEG_RX#5	9
9	PEG_TX6	PEG_TX6	V31	PCIE_RX6P	PCIE_TX6P	T28	C_PEG_RXP6	C220	0.1U/10V_4	PEG_RX6	9
9	PEG_TX#6	PEG_TX#6	V30	PCIE_RX6N	PCIE_TX6N	T27	C_PEG_RXN6	C224	0.1U/10V_4	PEG_RX#6	9
9	PEG_TX7	PEG_TX7	U31	PCIE_RX7P	PCIE_TX7P	T25	C_PEG_RXP7	C243	0.1U/10V_4	PEG_RX7	9
9	PEG_TX#7	PEG_TX#7	U30	PCIE_RX7N	PCIE_TX7N	T24	C_PEG_RXN7	C252	0.1U/10V_4	PEG_RX#7	9
9	PEG_TX8	PEG_TX8	P30	PCIE_RX8P	PCIE_TX8P	P28	C_PEG_RXP8	C276	0.1U/10V_4	PEG_RX8	9
9	PEG_TX#8	PEG_TX#8	P31	PCIE_RX8N	PCIE_TX8N	P27	C_PEG_RXN8	C268	0.1U/10V_4	PEG_RX#8	9
9	PEG_TX9	PEG_TX9	P29	PCIE_RX9P	PCIE_TX9P	P25	C_PEG_RXP9	C259	0.1U/10V_4	PEG_RX9	9
9	PEG_TX#9	PEG_TX#9	N29	PCIE_RX9N	PCIE_TX9N	P24	C_PEG_RXN9	C246	0.1U/10V_4	PEG_RX#9	9
9	PEG_TX10	PEG_TX10	N31	PCIE_RX10P	PCIE_TX10P	M28	C_PEG_RXP10	C289	0.1U/10V_4	PEG_RX10	9
9	PEG_TX#10	PEG_TX#10	N30	PCIE_RX10N	PCIE_TX10N	M27	C_PEG_RXN10	C277	0.1U/10V_4	PEG_RX#10	9
9	PEG_TX11	PEG_TX11	M31	PCIE_RX11P	PCIE_TX11P	M25	C_PEG_RXP11	C290	0.1U/10V_4	PEG_RX11	9
9	PEG_TX#11	PEG_TX#11	M30	PCIE_RX11N	PCIE_TX11N	M24	C_PEG_RXN11	C296	0.1U/10V_4	PEG_RX#11	9
9	PEG_TX12	PEG_TX12	K30	PCIE_RX12P	PCIE_TX12P	L28	C_PEG_RXP12	C288	0.1U/10V_4	PEG_RX12	9
9	PEG_TX#12	PEG_TX#12	K31	PCIE_RX12N	PCIE_TX12N	L27	C_PEG_RXN12	C295	0.1U/10V_4	PEG_RX#12	9
9	PEG_TX13	PEG_TX13	K29	PCIE_RX13P	PCIE_TX13P	L25	C_PEG_RXP13	C330	0.1U/10V_4	PEG_RX13	9
9	PEG_TX#13	PEG_TX#13	J29	PCIE_RX13N	PCIE_TX13N	L24	C_PEG_RXN13	C324	0.1U/10V_4	PEG_RX#13	9
9	PEG_TX14	PEG_TX14	J31	PCIE_RX14P	PCIE_TX14P	J28	C_PEG_RXP14	C325	0.1U/10V_4	PEG_RX14	9
9	PEG_TX#14	PEG_TX#14	J30	PCIE_RX14N	PCIE_TX14N	J27	C_PEG_RXN14	C331	0.1U/10V_4	PEG_RX#14	9
9	PEG_TX15	PEG_TX15	H31	PCIE_RX15P	PCIE_TX15P	G28	C_PEG_RXP15	C304	0.1U/10V_4	PEG_RX15	9
9	PEG_TX#15	PEG_TX#15	H30	PCIE_RX15N	PCIE_TX15N	G27	C_PEG_RXN15	C316	0.1U/10V_4	PEG_RX#15	9

Clock

2	EXT_GFX_CLKP	EXT_GFX_CLKP	AD29	PCIE_REFCLKP
2	EXT_GFX_CLKN	EXT_GFX_CLKN	AD30	PCIE_REFCLKN

100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing

SM BUS

AC28	NC_SMBCLK	
AC27	NC_SMBDATA	

12	PCIE_RST#	R71 0_4	AG25	PERSTB

Calibration

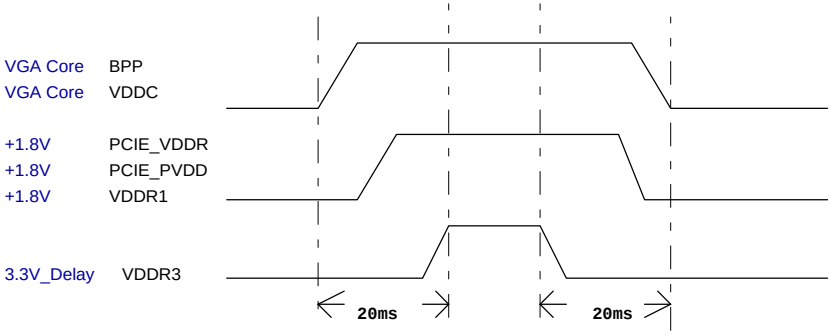
PCIE_CALRN	AF25	M72_PCIE_CALRN	R74	2K/F_4	+1.1V_PCIE_VDDC	
PCIE_CALRP	AE25	M72_PCIE_CALRP	R70	1.27K/F_4		

1.27K for M82-S

NC_1	AE23	
NC_2	AH30	

M72-S/M82-S
U29A

POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=1.0~1.1V - M62S,M71S
0.95~1.1V - M72S



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Quanta Computer Inc.

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Custom	M7X/M8X_PCIE_Interface	1A

NB5/RD5

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R100 1K/F_4 GPIO_24_JMODE — NA- M62S,M71S PD 1K- M72S

R522 10K/F_4 ROMCS# — GPIO22(ROMCS#) PD without external VBIOS ROM

R87 10K/F_4 BBEN — NA - M64/M62, M71 BBEN- M66 BBEN(10K PD)- M76

R95 10K/F_4 TEMP_FAIL — NA- M62S,M71S PU to 3.3V- M72S

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Qimonda (Infineon)	16*16	HYB18T256161BF-25
0001	Qimonda (Infineon)	32*16-500MHZ	HYB18T512161BZF-20
0010	Hynix	16*16	HY5PS561621AFP-25
0011	Hynix	32*16-500MHZ	H5PS5162FFR-20L
0100	Samsung	16*16	K4N56163QG-ZC25
0101	Samsung	32*16-500MHZ	K4N51163QG-HC20
0110			Reserved
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V

U29B PART 2 OF 6 — INTEGRATED TMDS/DP PORT

TXCM_DPA0P TXCP_DPA0N TXC_HDMI_L- TXC_HDMI_L+ — Remove 180R SHUNT RESISTOR for M82-S from AMD Jackson confirm

TX0M_DPA1P TX0P_DPA1N TX0_HDMI_L- TX0_HDMI_L+

TX1M_DPA2P TX1P_DPA2N TX1_HDMI_L- TX1_HDMI_L+

TX2M_DPA3P TX2P_DPA3N TX2_HDMI_L- TX2_HDMI_L+

DPA_PVDD / DPB_PVDD — DP/TMDS PLL Power (Link A) DP/TMDS PLL Power (Link B) 1.8 V ± 3%

DPA_VDDR / DPB_VDDR — DP/TMDS Transmitter Power (Link A) DP/TMDS Transmitter Power (Link B) 1.1 V ± 3%

ENABLE HD AUDIO (M8X-M) — R488 *0_4 VIP_3

M82-S — R476 0_4 150 OHM

DVALID PSYNC_NEW — 19 PSYNC

DVPCNTL_MVP_0 DVPCNTL_MVP_1 DVPCNTL_0 DVPCNTL_1 DVPCNTL_2 DVPCLK

DVPDATA_0 … DVPDATA_23 — EXT TMDS DVO

TMDS_HPD — R85 *100K/F_4, R463 150/F_4, R449 0_4 — CRT_R 10,24 / CRT_G 10,24 / CRT_B 10,24

Del R481, R482, R483, R68, R464, R486 for TP on PV

HSYNC_COM 10,19,24 VSYNC_COM 10,19,24

Memory ID — R495 R496 R493 R492 10K/F_4 *10K/F_4 — MEM_ID0 MEM_ID1 MEM_ID2 MEM_ID3

GPIO_0 … GPIO_28_TDO — GENERAL PURPOSE I/O

19 GPIO0 GPIO1 T151 T18 T152 GPIO5 — 10,23 LVDS_BLON — R93 0_4 EXT_LVDS_BLON — 19 GPIO8 GPIO9 T153 GPIO11 GPIO12 GPIO13 T154

42 GFX_CORE_CNTRL0 2 OSC_SPREAD — R526 0_4 OSC_SPREAD VGA_ALERT

5 TEMP_FAIL 42 GFX_CORE_CNTRL1 20 BBEN — T37 HPD3 — R99 0_4 TEMP_FAIL PWRCNTL_1 BBEN ROMCS# — +3VD R91 10K/F_4 GPIO_23_CLKREQb GPIO_24_JMODE

T36 T34 T35 T38

GENERICC — +1.8V 1.8V+R6043(249R)=1.8V/3=0.6V — R75 499/F_4 R76 249/F_4 — +0.6V_M72_VREFG

DAC1 / CRT — R — RB — G — GB — B — BB — HSYNC — VSYNC — RSET — AVDD — AVSSQ — VDD1DI — VSS1DI — R2 — R2B — G2 — G2B — B2 — B2B — DAC2 (TV/CRT2) — C — Y — COMP — V2SYNC — H2SYNC — A2VDD — A2VDDQ — A2VSSQ — VDD2DI — VSS2DI — R2SET

AVDD — DAC1 Analog Power Dedicated power for DAC1. 1.8 V ± 5%

VDD1DI — DAC1 Digital Power. 1.8 V ± 5%

A2VDD — DAC2 Analog Power. 3.3 V ± 5%

A2VDDQ — DAC2 Band Gap (clean) power supply. 1.8 V ± 5%

VDD2DI — DAC2 Digital Power. 1.8 V ± 5%

Del R470, R478, R450, R472, R471, R469, R451 for TP on PV

Del L25 for TP on PV

DAC2_VSY DAC2_HSY — T13 T10

SCL SDA — SERIAL BUSES DDC1DATA DDC1CLK DDC2DATA DDC2CLK DDC3DATA_DP3_AUXN DDC3CLK_DP3_AUXP DDC4DATA_DP4_AUXN DDC4CLK_DP4_AUXP

EDIDCLK 10,23 EDIDDATA 10,23 — DDCDATA 10,24 DDCCLK 10,24 — VTHM_DAT VTHM_CLK — R511 R510 *4.7K_4 +3V_DELAY

Del R84, R85, R466, R467 for TP on PV

DDC 3V tolerance --DDC1, DDC2, SDA/SCL DDC 5V tolerance --DDC3, DDC4

HDMI_SDA 23 HDMI_SCL 23

TS_FDO — THERMAL — DPLUS DMINUS — VGATHRM+ VGATHRM-

DPLL_PVDD PLL & XTAL — DPLL_PVSS — PCIE_PVDD — MPVDD MPVSS — DPLL_VDDC — XTALIN — XTALOUT

TESTEN PLLTEST — TEST

M72-S/M82-S

DPLL_PVDD — Phase Lock Loop Power — Dedicated analog power pin for display PLLs. 1.8 V ± 3%

+1.8V — BLM18PG181SN1D(180,1.5A)_6 L17 — 1.8V(40mA) — C114 10U/6.3V_8 C147 0.1U/10V_4

+1.8V_DPLL_PVDD — +1.8V_DPLL_PVSS — +1.8V_VPCIE_PVDD

PCIE_PVDD — PCI-E PLL power. 1.8 V ± 5%

+1.8V — BLM18PG181SN1D(180,1.5A)_6 L71 — 1.8V(40mA) — C743 10U/6.3V_8 C747 1U/10V_4 C746 0.1U/10V_4

MPVDD — Memory Phase Lock Loop Power Same as VDDC

+VGA_CORE — BLM18PG181SN1D(180,1.5A)_6 L79 — VDDC(345mA) — C822 10U/6.3V_8 C824 1U/10V_4 C823 0.1U/10V_4

+VGACORE_MPVDD — MPVSS — +1.1V_DPLL_VDDC

2 EVGA-XTALI — EVGA-XTALI — EVGA-XTALO

DPLL_VDDC — Phase Lock Loop Power — Dedicated digital power pin for display PLLs. 1.1 V ± 5%

+1.1V — BLM18PG181SN1D(180,1.5A)_6 L18 — 1.1V(100mA) — C106 10U/6.3V_8 C169 1U/10V_4 C161 0.1U/10V_4

1K/F_4 R67 — AH26 AD12

C741 *22P/50V_4 — Y7 *27MHZ — R468 *10M_6 — C735 *22P/50V_4 — CL=20PF — For Int Clk 27Mhz — EVGA-XTALI EVGA-XTALO

Thermal Sensor — U30 G781-1P8@EV — SMCLK SMDATA -ALT GND VCC DXP DXN -OVT

5,35 MBCLK2 R524 0_4 — MBCLK2

5,35 MBDATA2 R525 0_4 — MBDATA2

VTHM_CLK R518 *0_4 — VTHM_DAT R519 *0_4 — +3V_DELAY R516 10K/F_4 — VGA_ALERT

761-1_3V R509 200/F_6 — C790 0.1U/10V_4 — VGATHRM+ — C793 2200P/50V_4 — VGATHRM- — -VGATHRM R513 10K/F_4 — +3V_DELAY

w/s 10 / 10

I2C ADDRESS: 9AH

+1.8V_A2VDD_Q — L16 BLM18PG181SN1D(180,1.5A)_6 — 1.8V(65mA) — C129 0.1U/10V_4 C168 1U/10V_4 C98 10U/6.3V_8

DPB_PVDD — L24 BLM18PG181SN1D(180,1.5A)_6 — 1.8V(20mA) — C165 0.1U/10V_4 C182 1000P/50V_4 C145 10U/6.3V_8

+VDDD1 — L15 BLM18PG181SN1D(180,1.5A)_6 — 1.8V(100mA) — C110 0.1U/10V_4 C135 1U/10V_4 C97 10U/6.3V_8

+1.8V_TPVDD — L20 BLM18PG181SN1D(180,1.5A)_6 — 1.8V(20mA) — C113 0.1U/10V_4 C108 1000P/50V_4 C134 10U/6.3V_8

DPA_B_VDDR — L70 BLM18PG181SN1D(180,1.5A)_6 — 1.1V(S100,D200mA) — C740 0.1U/10V_4 C742 1000P/50V_4 C737 10U/6.3V_8

N85/RD5

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Custom	M7X/M8X_Main	1A

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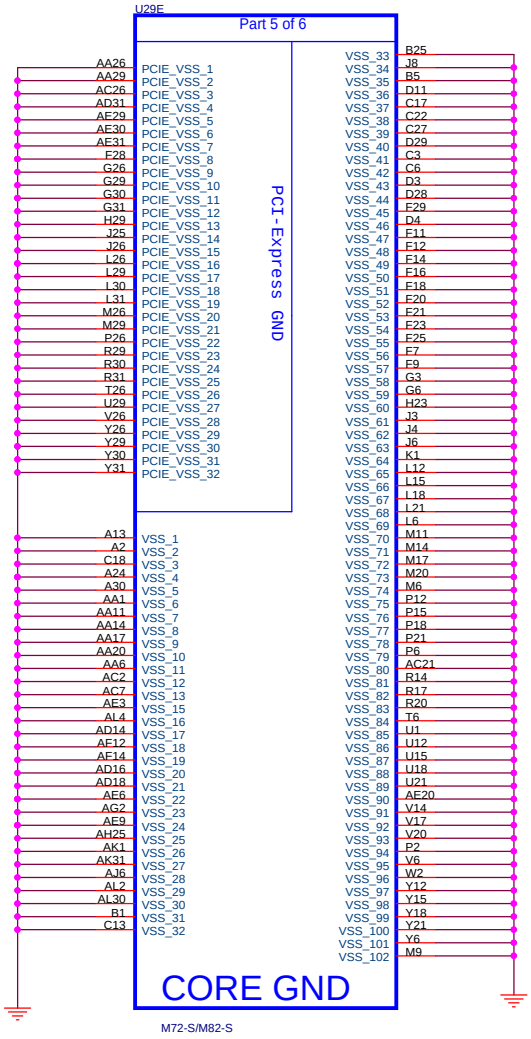
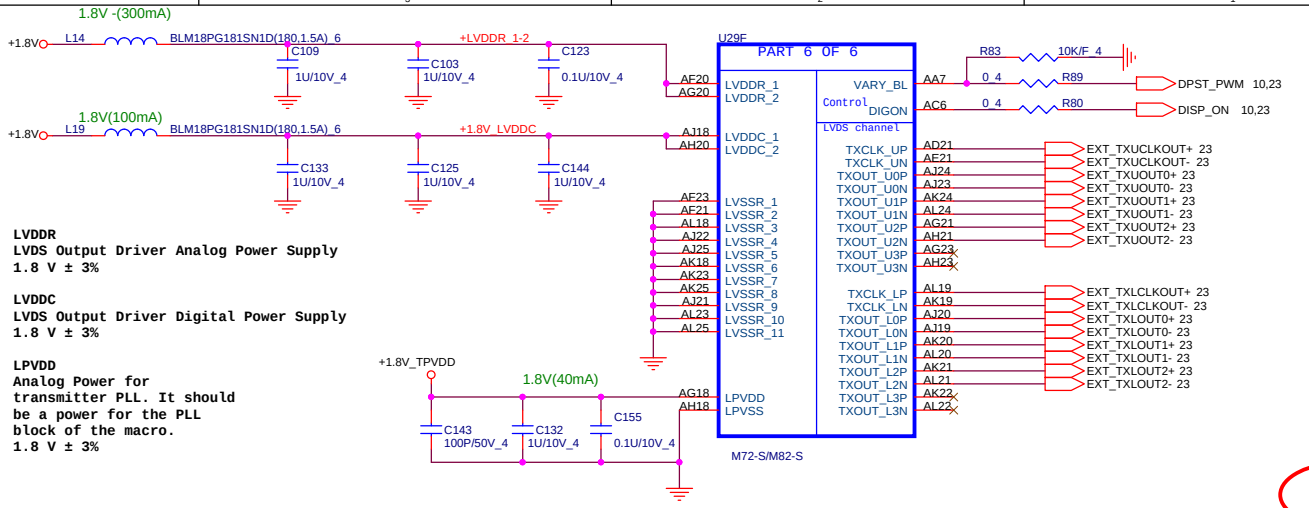




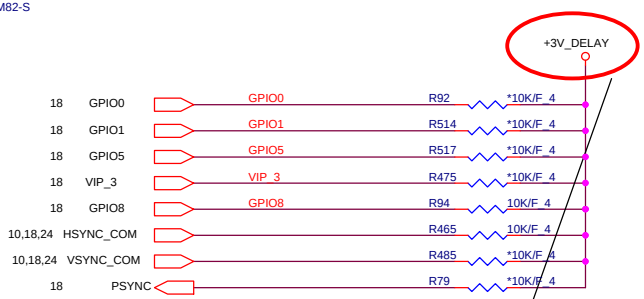
LVDDR
LVDS Output Driver Analog Power Supply
1.8 V ± 3%

LVDDC
LVDS Output Driver Digital Power Supply
1.8 V ± 3%

LPVDD
Analog Power for transmitter PLL. It should be a power for the PLL block of the macro.
1.8 V ± 3%

CONFIGURATION STRAPS

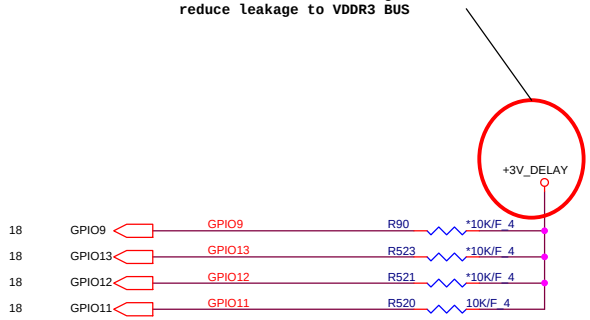
PIN	DESCRIPTION OF DEFAULT SETTINGS	M82-S
GPIO0	PCIE FULL TX OUTPUT SWING	0
GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
GPIO5	Allows eitherPCIe 2.5GT/s or 5GT/s operation	REV
VIP3	ENABLE HD AUDIO (M8X-M)	1
GPIO8	ENABLE HD AUDIO (M82-S)	1
HSYNC	ENABLED HDMI	1



SI-1 Modified -- follow AMD reference schematic change for reduce leakage to VDDR3 BUS

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1



It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

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Custom	M7X/M8X_GND / LVDS/ Straps	1A

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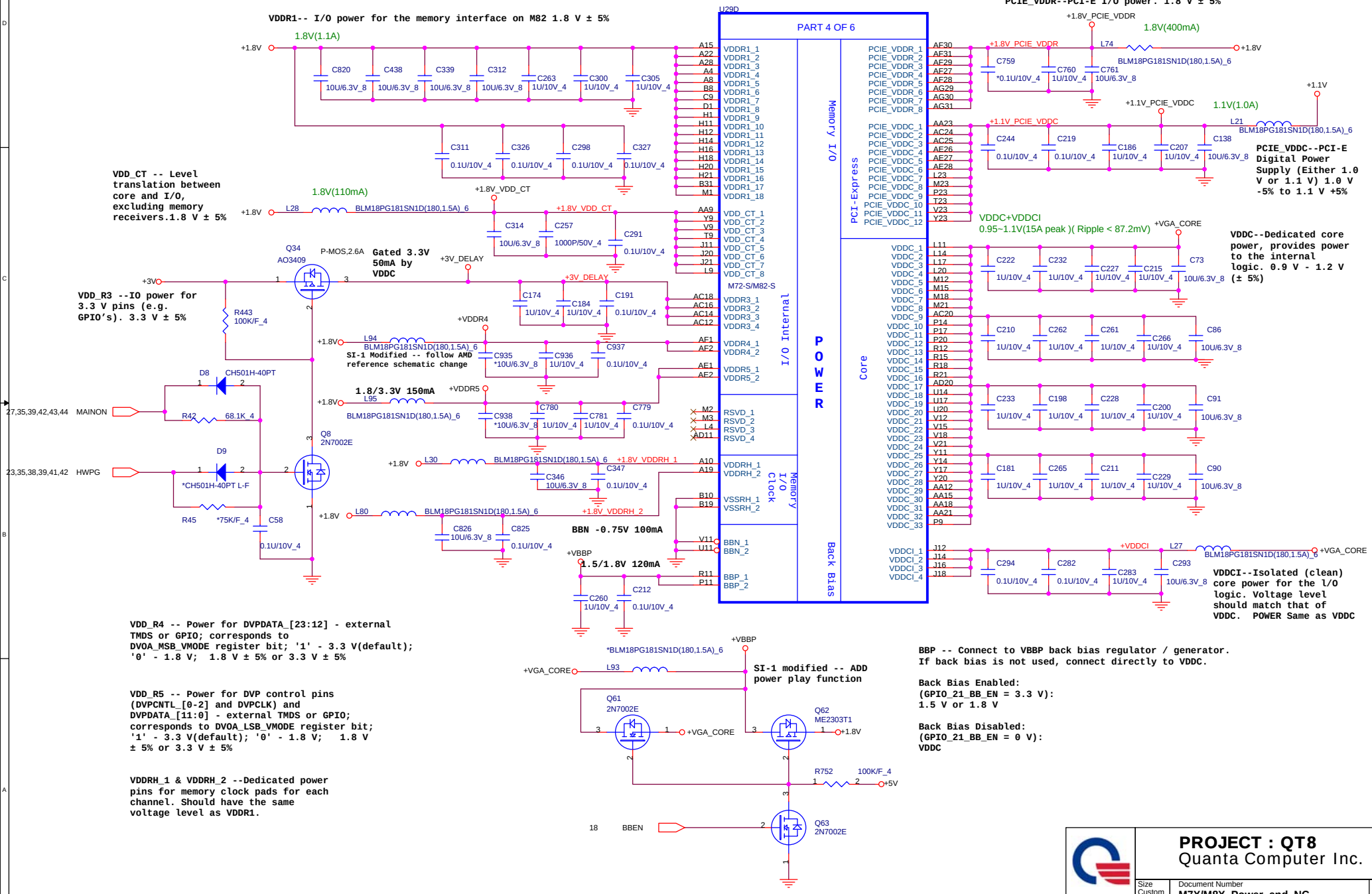
VDDR1-- I/O power for the memory interface on M82 1.8 V ± 5%
1.8V(1.1A)
U29D
PART 4 OF 6
Memory I/O
PCI-Express
I/O Internal
POWER
Core
Clock
Memory I/O
Back Bias
M72-S/M82-S
PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%
1.8V(400mA)
PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%
1.1V(1.0A)
VDD_CT -- Level translation between core and I/O, excluding memory receivers.1.8 V ± 5%
1.8V(110mA)
Gated 3.3V 50mA by VDDC
VDDC+VDDCI
0.95~1.1V(15A peak)(Ripple < 87.2mV)
VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)
VDD_R3 --IO power for 3.3 V pins (e.g. GPIO's). 3.3 V ± 5%
SI-1 Modified -- follow AMD reference schematic change
1.8/3.3V 150mA
BBN -0.75V 100mA
1.5/1.8V 120mA
VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC
VDD_R4 -- Power for DVPDATA_[23:12] - external TMDS or GPIO; corresponds to DVOA_MSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%
VDD_R5 -- Power for DVP control pins (DVPCNTL_[0-2] and DVPCLK) and DVPDATA_[11:0] - external TMDS or GPIO; corresponds to DVOA_LSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%
VDDRH_1 & VDDRH_2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.
SI-1 modified -- ADD power play function
BBP -- Connect to VBBP back bias regulator / generator. If back bias is not used, connect directly to VDDC.
Back Bias Enabled: (GPIO_21_BB_EN = 3.3 V): 1.5 V or 1.8 V
Back Bias Disabled: (GPIO_21_BB_EN = 0 V): VDDC
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Quanta Computer Inc.
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Size Custom
Document Number M7X/M8X_Power_and_NC
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U29C

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MEMORY INTERFACE

M72-S/M82-S

MDA0	E29	DQ_0	MA_0	B14	MAA0		
MDA1	E30	DQ_1	MA_1	A14	MAA1		
MDA2	E31	DQ_2	MA_2	B13	MAA2		
MDA3	D31	DQ_3	MA_3	E14	MAA3		
MDA4	C29	DQ_4	MA_4	B17	MAA4		
MDA5	B29	DQ_5	MA_5	A17	MAA5		
MDA6	B30	DQ_6	MA_6	C15	MAA6		
MDA7	A29	DQ_7	MA_7	G16	MAA7		
MDA8	E26	DQ_8	MA_8	E16	MAA8		
MDA9	D26	DQ_9	MA_9	C14	MAA9		
MDA10	E25	DQ_10	MA_10	A12	MAA10		
MDA11	D25	DQ_11	MA_11	B12	MAA11		
MDA12	G23	DQ_12	MA_BA0	C12	A_BA0		
MDA13	G21	DQ_13	MA_BA1	D14	A_BA1		
MDA14	E21	DQ_14	MA_A12	B15	MAA12		
MDA15	D21	DQ_15	MA_BA2	G14	A_BA2		
MDA16	C28	DQ_16					
MDA17	B28	DQ_17	DQMb_0	D30	DQMA#0		
MDA18	B27	DQ_18	DQMb_1	G25	DQMA#1		
MDA19	A27	DQ_19	DQMb_2	C26	DQMA#2		
MDA20	C25	DQ_20	DQMb_3	C21	DQMA#3		
MDA21	A25	DQ_21	DQMb_4	C5	DQMA#4		
MDA22	C24	DQ_22	DQMb_5	D6	DQMA#5		
MDA23	B24	DQ_23	DQMb_6	D2	DQMA#6		
MDA24	C23	DQ_24	DQMb_7	K3	DQMA#7		
MDA25	B23	DQ_25					
MDA26	A23	DQ_26	QS_0	C30	QSA0		
MDA27	B22	DQ_27	QS_1	D23	QSA1		
MDA28	C20	DQ_28	QS_2	B26	QSA2		
MDA29	B20	DQ_29	QS_3	B21	QSA3		
MDA30	A20	DQ_30	QS_4	B6	QSA4		
MDA31	C19	DQ_31	QS_5	E7	QSA5		
MDA32	C8	DQ_32	QS_6	E2	QSA6		
MDA33	C7	DQ_33	QS_7	J2	QSA7		
MDA34	B7	DQ_34					
MDA35	A7	DQ_35	QS_0B	C31	QSA#0		
MDA36	A5	DQ_36	QS_1B	E23	QSA#1		
MDA37	C4	DQ_37	QS_2B	A26	QSA#2		
MDA38	B4	DQ_38	QS_3B	A21	QSA#3		
MDA39	A3	DQ_39	QS_4B	A6	QSA#4		
MDA40	G9	DQ_40	QS_5B	D7	QSA#5		
MDA41	E9	DQ_41	QS_6B	E1	QSA#6		
MDA42	D9	DQ_42	QS_7B	J1	QSA#7		
MDA43	G7	DQ_43					
MDA44	G5	DQ_44	ODT0	E20	ODTA0		
MDA45	F5	DQ_45	ODT1	C11	ODTA1		
MDA46	G4	DQ_46					
MDA47	F4	DQ_47	CLK0	A18	CLKA0		
MDA48	B3	DQ_48	CLK1	A11	CLKA1		
MDA49	B2	DQ_49					
MDA50	C2	DQ_50	CLK0b	B18	CLKA0#		
MDA51	C1	DQ_51	CLK1b	B11	CLKA1#		
MDA52	E3	DQ_52					
MDA53	F3	DQ_53	RAS0b	G20	RASA0#		
MDA54	F2	DQ_54	RAS1b	D12	RASA1#		
MDA55	F1	DQ_55					
MDA56	G2	DQ_56	CAS0b	D20	CASA0#		
MDA57	G1	DQ_57	CAS1b	E12	CASA1#		
MDA58	H3	DQ_58					
MDA59	H2	DQ_59	CS0b_0	E18	CSA0# 0		
MDA60	K2	DQ_60	CS0b_1	G18			
MDA61	L3	DQ_61					
MDA62	L2	DQ_62	CS1b_0	G11	CSA1# 0		
MDA63	L1	DQ_63	CS1b_1	E11			
F30		MVREFD	CKE0	D18	CKEA0		
F31		MVREFS	CKE1	G12	CKEA1		
L5		TEST_MCLK	WE0b	D16	WEA0#		
L7		TEST_YCLK	WE1b	C10	WEA1#		
J7		MEMTEST	DRAM_RST	J5	+1.8V		

write strobe
read strobe

22 ODTA0 — ODTA0
22 ODTA1 — ODTA1

22 RASA0# — RASA0#
22 RASA1# — RASA1#

22 CASA0# — CASA0#
22 CASA1# — CASA1#

22 WEA0# — WEA0#
22 WEA1# — WEA1#

22 CSA0#_0 — CSA0# 0

22 CSA1#_0 — CSA1# 0

22 CKEA0 — CKEA0
22 CKEA1 — CKEA1

22 CLKA0 — CLKA0
22 CLKA0# — CLKA0#

22 CLKA1 — CLKA1
22 CLKA1# — CLKA1#

22 QSA#[7..0] — QSA#[7..0]

22 QSA[7..0] — QSA[7..0]

22 DQMA#[7..0] — DQMA#[7..0]

22 MDA[63..0] — MDA[63..0]

22 MAA[12..0] — MAA[12..0]

22 A_BA0 — A_BA0
22 A_BA1 — A_BA1

A_BA2 — 22

SI-1 modified -- for support 1Gbit VRAM (64M X 16)

+1.8V
R116 100/F_4
MVREFD
+1.8V
C338 0.1U/10V_4
R113 100/F_4
R532 100/F_4
MVREFS
C817 0.1U/10V_4
R529 100/F_4
R98 4.7K_4
R102 4.7K_4
R97 240/F_4

Change MEMTEST to 240 1% ohm to GND , AMD update

R101 4.7K_4 — +1.8V

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
B	M7X/M8X/MEM_Interface	1A

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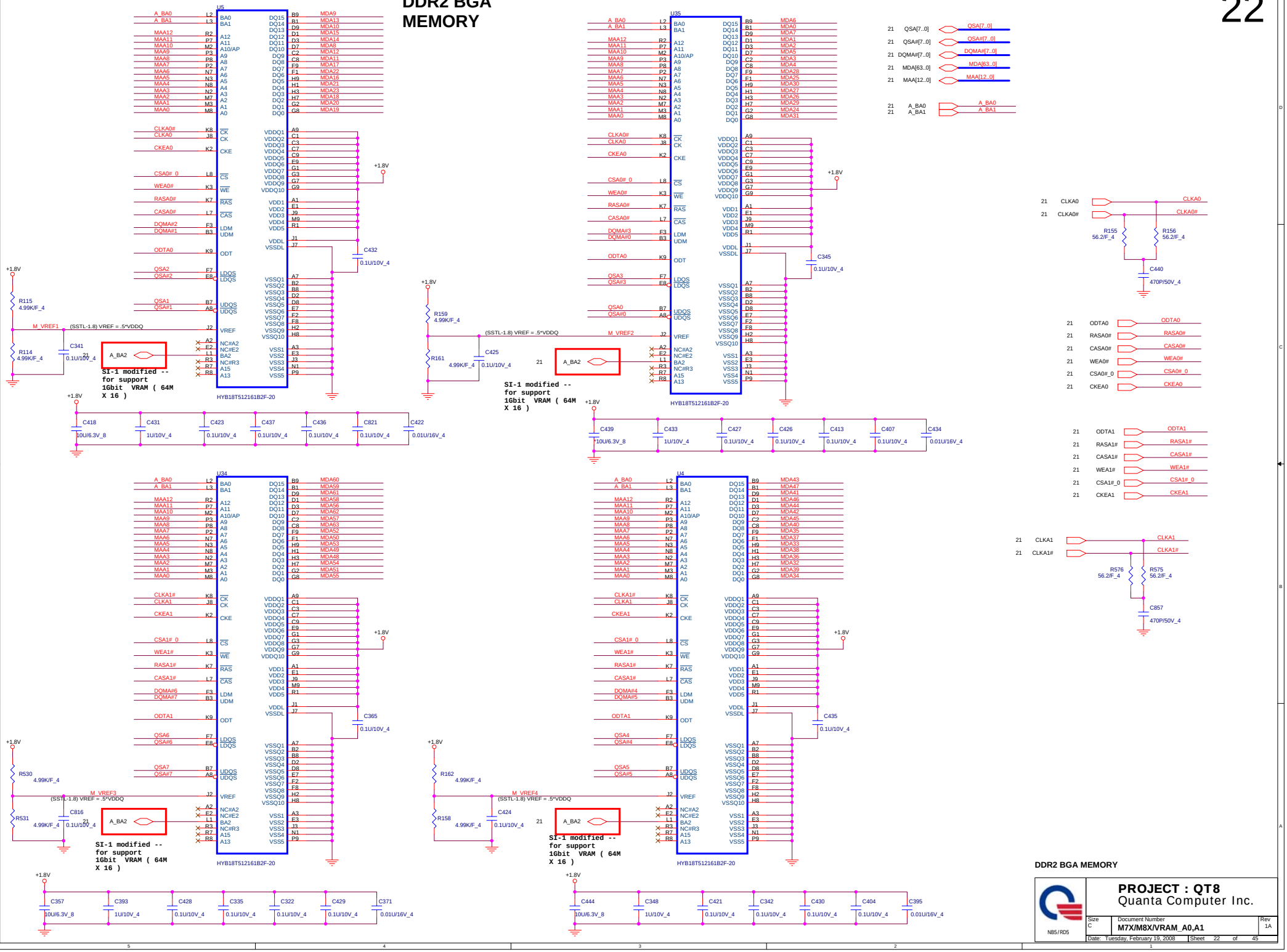
DDR2 BGA MEMORY



DDR2 BGA MEMORY

NB5/RD5	**PROJECT : QT8** Quanta Computer Inc.	
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1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB to LVDS for UMA

10 LA_CLK — LA_CLK — RP3 — *0_4P2R_4 — TXLCLKOUT+
10 LA_CLK# — LA_CLK# — TXLCLKOUT-
10 LA_DATAP0 — LA_DATAP0 — RP1 — *0_4P2R_4 — TXLOUT0+
10 LA_DATAN0 — LA_DATAN0 — TXLOUT0-
10 LA_DATAP1 — LA_DATAP1 — RP4 — *0_4P2R_4 — TXLOUT1+
10 LA_DATAN1 — LA_DATAN1 — TXLOUT1-
10 LA_DATAP2 — LA_DATAP2 — RP5 — *0_4P2R_4 — TXLOUT2+
10 LA_DATAN2 — LA_DATAN2 — TXLOUT2-

10 LB_CLK — LB_CLK — RP2 — *0_4P2R_4 — TXUCLKOUT+
10 LB_CLK# — LB_CLK# — TXUCLKOUT-
10 LB_DATAP0 — LB_DATAP0 — RP6 — *0_4P2R_4 — TXUOUT0+
10 LB_DATAN0 — LB_DATAN0 — TXUOUT0-
10 LB_DATAP1 — LB_DATAP1 — RP8 — *0_4P2R_4 — TXUOUT1+
10 LB_DATAN1 — LB_DATAN1 — TXUOUT1-
10 LB_DATAN2 — LB_DATAN2 — RP7 — *0_4P2R_4 — TXUOUT2+
10 LB_DATAP2 — LB_DATAP2 — TXUOUT2+

OPTION SIGNAL FROM M8X to LVDS for discrete

19 EXT_TXLCLKOUT- — EXT_TXLCLKOUT- — RP59 — 0_4P2R_4 — TXLCLKOUT-
19 EXT_TXLCLKOUT+ — EXT_TXLCLKOUT+ — TXLCLKOUT+
19 EXT_TXLOUT0- — EXT_TXLOUT0- — RP57 — 0_4P2R_4 — TXLOUT0-
19 EXT_TXLOUT0+ — EXT_TXLOUT0+ — TXLOUT0+
19 EXT_TXLOUT1- — EXT_TXLOUT1- — RP60 — 0_4P2R_4 — TXLOUT1-
19 EXT_TXLOUT1+ — EXT_TXLOUT1+ — RP61 — 0_4P2R_4 — TXLOUT1+
19 EXT_TXLOUT2+ — EXT_TXLOUT2+ — TXLOUT2+
19 EXT_TXLOUT2- — EXT_TXLOUT2- — TXLOUT2-

19 EXT_TXUCLKOUT- — EXT_TXUCLKOUT- — RP58 — 0_4P2R_4 — TXUCLKOUT-
19 EXT_TXUCLKOUT+ — EXT_TXUCLKOUT+ — TXUCLKOUT+
19 EXT_TXUOUT0+ — EXT_TXUOUT0+ — RP62 — 0_4P2R_4 — TXUOUT0+
19 EXT_TXUOUT0- — EXT_TXUOUT0- — TXUOUT0-
19 EXT_TXUOUT1- — EXT_TXUOUT1- — RP64 — 0_4P2R_4 — TXUOUT1-
19 EXT_TXUOUT1+ — EXT_TXUOUT1+ — TXUOUT1+
19 EXT_TXUOUT2- — EXT_TXUOUT2- — RP63 — 0_4P2R_4 — TXUOUT2-
19 EXT_TXUOUT2+ — EXT_TXUOUT2+ — TXUOUT2+

UMA/DISCRETE select for HDMI

From RS780M

for Layout concern ,placement close north bridge

9 C_PEG_TX#15 — C_PEG_TX#15 — C386 — *0.1U/10V_4 — TX2_HDMI-L — TX2_HDMI+L — RP31 — *0_4P2R_4 — TX2_HDMI+
9 C_PEG_TX15 — C_PEG_TX15 — C387 — *0.1U/10V_4 — TX2_HDMI+L — TX2_HDMI-L — TX2_HDMI-
9 C_PEG_TX#14 — C_PEG_TX#14 — C388 — *0.1U/10V_4 — TX1_HDMI-L — TX1_HDMI+L — RP23 — *0_4P2R_4 — TX1_HDMI+
9 C_PEG_TX14 — C_PEG_TX14 — C389 — *0.1U/10V_4 — TX1_HDMI+L — TX1_HDMI-L — TX1_HDMI-
9 C_PEG_TX#13 — C_PEG_TX#13 — C355 — *0.1U/10V_4 — TX0_HDMI-L — TX0_HDMI+L — RP37 — *0_4P2R_4 — TX0_HDMI+
9 C_PEG_TX13 — C_PEG_TX13 — C344 — *0.1U/10V_4 — TX0_HDMI+L — TX0_HDMI-L — TX0_HDMI-
9 C_PEG_TX#12 — C_PEG_TX#12 — C827 — *0.1U/10V_4 — TXC_HDMI-L — TXC_HDMI+L — RP17 — *0_4P2R_4 — TXC_HDMI-
9 C_PEG_TX12 — C_PEG_TX12 — C828 — *0.1U/10V_4 — TXC_HDMI+L — TXC_HDMI-L — TXC_HDMI+

From M82-S

18 TX2_HDMI_L- — TX2_HDMI_L- — C794 — 0.1U/10V_4 — TX2_HDMI-
18 TX2_HDMI_L+ — TX2_HDMI_L+ — C789 — 0.1U/10V_4 — TX2_HDMI+
18 TX1_HDMI_L- — TX1_HDMI_L- — C782 — 0.1U/10V_4 — TX1_HDMI-
18 TX1_HDMI_L+ — TX1_HDMI_L+ — C786 — 0.1U/10V_4 — TX1_HDMI+
18 TX0_HDMI_L- — TX0_HDMI_L- — C799 — 0.1U/10V_4 — TX0_HDMI-
18 TX0_HDMI_L+ — TX0_HDMI_L+ — C797 — 0.1U/10V_4 — TX0_HDMI+
18 TXC_HDMI_L- — TXC_HDMI_L- — C768 — 0.1U/10V_4 — TXC_HDMI-
18 TXC_HDMI_L+ — TXC_HDMI_L+ — C776 — 0.1U/10V_4 — TXC_HDMI+

for Layout concern ,placement close HDMI conn

+5V — Q36 2N7002E — R528 100K/F_4

R507 499/F_4 TX2_HDMI+
R508 499/F_4 TX2_HDMI-
R506 499/F_4 TX1_HDMI+
R505 499/F_4 TX1_HDMI-
R512 499/F_4 TX0_HDMI+
R515 499/F_4 TX0_HDMI-
R504 499/F_4 TXC_HDMI+
R500 499/F_4 TXC_HDMI-

UMA RS780M
上 750 ohm CS17502FB19

DIS M82-S
上 499 ohm CS14992FB24

Close to HDMI Connector

+12VALW / +3V / +5VSUS / +3VLCD

+12VALW — R19 330K_6 — A03404 ID current 5.8A — N-MOS,5.8A Q1 AO3404 — +3VLCD
+3V — C16 0.1U/10V_4
+5VSUS — R14 100K/F_4 — Q3 PDTC144EU — Q4 2N7002E — C22 0.1U/10V_4 — R10 22_8 — LCDDISCHG
LCDON — LCDON# — Q2 2N7002E
10,19 DISP_ON — R17 2.2K_4

+5V — R401 75R/F_6 — +LOGO_PWR

SI-2 modified-delete R402 and R401 from 0ohm to 75ohm

+3V — R8 2.2K_4 EDIDCLK — R7 2.2K_4 EDIDDATA

+3VLCD — L1 PBY201209T-4A_8 — +3VLCD_CON — C12 10U/6.3V_8 — C10 0.1U/10V_4 — C13 0.01U/16V_4

+VIN_BLIGHT — +3VLCD_CON

C6 1000P/50V_4 — C678 1000P/50V_4

10,18 EDIDDATA — EDIDDATA — +LOGO_PWR — BLONCON

CN1 (41 / 42)

EDIDCLK 10,18 — VADJ1 — Camera Pin

TXLCLKOUT+ / TXLCLKOUT- — TXLOUT0+ / TXLOUT0- — TXLOUT1+ / TXLOUT1- — TXLOUT2+ / TXLOUT2- — TXUCLKOUT+ / TXUCLKOUT- — TXUOUT0+ / TXUOUT0- — TXUOUT1+ / TXUOUT1- — TXUOUT2+ / TXUOUT2-

Backlight

PN_BLON — D5 CH501H-40PT — BLONCON — C28 22P/50V_4 — R22 100K/F_4
+3VPCU — R24 33K_6 — D6 CH501H-40PT — LID_EC#
10,18 LVDS_BLON — LVDS_BLON — R23 1K/F_4 — PN_BLON — LID_EC# 34,35
D7 CH501H-40PT — HWPG 20,35,38,39,41,42
12 LCD_BK — LCD_BK — Q5 PDTC144EU — R259 *10K/F_4 — +3VS5

Del R21 and Pull hi R259 to +3VS5, add D7 to HWPG on PV

PV del logo light

10,19 DPST_PWM — DPST_PWM — R88 — *0_4
35 PWM_VADJ — PWM_VADJ — R96 — 0_4 — LCD CONN — VADJ1
C5 *4.7U/6.3V_6 — C7 0.1U/10V_4

+VIN / +VIN_BLIGHT

+VIN — L2 FBM2125 HM330-T(4A,0.015) 8 — +VIN_BLIGHT
C15 0.1U/50V_6 — C11 0.01U/50V_4 — C9 0.1U/50V_6 — C14 *10U/25V_12 — C8 0.1U/50V_6

HDMI HPD SENSE

10,18 TMDS_HPD — TMDS_HPD — R66 20K/F_4 — HDMI_DET
check 3v or 5v
D10 UDZS2.7BTE-17 — R64 100K/F_4

+5V_HDMVCC

+5V_HDMVCC — D31 CH501H-40PT — R494 4.7K_4 — HDMI_SCLK
+5V_HDMVCC — D32 CH501H-40PT — R503 4.7K_4 — HDMI_SDATA

Change R494, R503 to 4.7K for AMD on PV

HDMI PORT

CN29 HDMI CONN

TX2_HDMI+ / TX2_HDMI- / TX1_HDMI+ / TX1_HDMI- / TX0_HDMI+ / TX0_HDMI- / TXC_HDMI+ / TXC_HDMI-
SHELL1 SHELL3 D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET SHELL4 SHELL2

Del C748, C756 for HDMI on PV

HDMI_SCLK — L73 0_6 — HDMISCL
HDMI_SDATA — L75 0_6 — HDMISDA
+5V_HDMVCC
+5V — FUSE1A6V_POLY F1 — C128 *0.1U/10V_4
HDMI_DET

UMA AND DISCRETE HDMI I2C SELECT

Close to HDMI Connector

18 HDMI_SDA — HDMI_SDA — RP65 0_4P2R_4 — HDMI_SDATA
18 HDMI_SCL — HDMI_SCL — HDMI_SCLK

Discrete DDC4 is 5V tolerance , the MOSFET level shifter no need
UMA DDC is 3V tolerance,the MOSFET level shifter is need

DIS

+3V — R680 *2K/04 — +5V
10 HDMI_DDC_CLK — HDMI_DDC_CLK — R753 *0_4 — HDMI_SCLK — Q59 *FDV301N — 3 HDMI_SCLK
HDMI_DDC_DATA — R755 *0_4 — HDMI_SDATA — Q60 *FDV301N — 3 HDMI_SDATA
+3V — R681 *2K/04 — +5V
10 HDMI_DDC_DATA

Change 2N7002 to FDV301N for AMD on PV

UMA

CRT PORT

SI-2 modified --Change Layout footprint 12/27

+5VCRT — C670 0.1U/10V_4

+5V — F2 40 mils — +5VCRT

40 MIL

FUSE1A6V_POLY

CRT_R_1_L — L61 BLM18BA470SN1(47,300MA)_6 — CRT_R1

CRT_G_1_L — L60 BLM18BA470SN1(47,300MA)_6 — CRT_G1

CRT_B_1_L — L59 BLM18BA470SN1(47,300MA)_6 — CRT_B1

R400 150/F_4 | R399 150/F_4 | R398 150/F_4 | C677 5.6P/50V_6 | C675 5.6P/50V_6 | C672 5.6P/50V_6 | C671 5.6P/50V_6 | C674 5.6P/50V_6 | C676 5.6P/50V_6

EMI

CRT CONN CN20

close conn within 600mils

R400 for UAM use 140 ohm on PV(AMD)

+5V — C673 0.1U/10V_4

U21 AHCT1G125DCH

U22 AHCT1G125DCH

10,18,19 VSYNC_COM — PR_VSYNC 37

10,18,19 HSYNC_COM — PR_HSYNC 37

R1 0_4 CRTDDCCLK2

R3 33_4 CRTVSYNC

R4 33_4 CRTHSYNC

R5 0_4 CRTDDCDAT2

C1 *470P/50V_4 | C2 *47P/50V_4 | C3 *47P/50V_4 | C4 *47P/50V_4

follow AMD reference schematic change for reduce leakage to VDDR3 BUS

+3V_DELAY — R761 4.7K_4 — +3V — R25 *4.7K_4

10,18 DDCCLK — DDCCLK — Q6 2N7002E — DDCCLK2 — DDCCLK2 37

+3V_DELAY — R762 4.7K_4 — +3V — R26 *4.7K_4

10,18 DDCDATA — DDCDATA — Q7 2N7002E — DDCDAT2 — DDCDAT2 37

R2 6.81K_4 | R6 6.81K_4

+5VCRT — +5VCRT — D25 CH501H-40PT — +5V_CRT2

+3V

D28 *BAV99W — CRT_R1

D27 *BAV99W — CRT_G1

D26 *BAV99W — CRT_B1

D1 *BAV99W — DDCCLK2

D2 *BAV99W — CRTVSYNC

D3 *BAV99W — CRTHSYNC

D4 *BAV99W — DDCDAT2

U23

37 PR_RED — PR_RED — CRT_R_1_L

37 PR_GEN — PR_GEN — CRT_G_1_L

37 PR_BLU — PR_BLU — CRT_B_1_L

35,37 PR_INSERT#

IA0 IA1 IB0 IB1 IC0 IC1 ID0 ID1 SEL /E — YA YB YC YD — VCC GND

74CBT3257

CRT_R CRT_G CRT_B — CRT_R 10,18 | CRT_G 10,18 | CRT_B 10,18

+5V_SW — R403 0_6 — +5V

C679 0.1U/10V_4

EMI

R404 10K/F_4

CRT SWITCH

inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT	1A

NB5/RD5

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For 5158E

2 CLK_48M_CR — R397 *0_4 — XTLO

+3VSUS — R321 *100K/F_4

UMA BOM need to add

26,29 CARD_LED# — R320 *0_4 — CARD_LEDO

U19

CF_CD# GPIO0 CF_D10 CF_D9 CF_D2 CF_D8/SM_CD# CF_D1/XD_CD# CF_D0/SM_WPM#/SD_WP CF_A0/SD_CD# CF_DMACK# CF_A1/XD_D4 CF_DMARQ

XD_CD# — SP2 — SD_CD# — SP4

SI-2 modified --Fix Y5 layout footprint to XTAL-5X3_2-3_8 (ME placement)

R362 *6.19K/F_4 — RREF

13 USBP6_CR- — DM
13 USBP6_CR+ — DP

C665 *5.6P/50V_4 — XTLO — *12MHz — Y5 — XTLI — C668 *5.6P/50V_4

R395 *270K_4

For 5158 BG6120000717

MODE_SEL — R394 *10K/F_4 — C667 *47P/50V_4

For 5158

+3VSUS — R667 *100K/F_4 — 5158_RST# — C925 *1U/10V_4

If SD_DAT1 connect to SP4 , MOD_SEL need to let it to N.C

XD_CLE/CF_D3 XD_CE#/CF_D11 XD_ALE/CF_D4

SD_DAT2/XD_RE#/CF_D12 SD_DAT3/XD_WE#/CF_D5 XD_RDY/CF_D13 SD_DAT4/XD_WP#/CF_D6

SD_CMD SD_DAT5/XD_D0/CF_D14 SD_CLK/XD_D1/MS_CLK/CF_D7 SD_DAT6/XD_D7/MS_D3/CF_D15 CF_CS0#

MS_INS#/CF_IORD# SD_DAT7/XD_D2/MS_D2/CF_IOWR# SD_DAT0/XD_D6/MS_D0/CF_RST# SD_DAT1/XD_D3/MS_D1/CF_IORDY XD_D5/MS_BS/CF_A2

AV_PLL_IN — C647 *0.1U/10V_4 — C918 *1U/10V_4

VREG_OUT 5V_IN A3V3_IN D3V3_IN — VREG

D3V3_OUT — C633 *0.1U/10V_4 — C634 *0.1U/10V_4 — C612 *0.1U/10V_4 — C589 *4.7U/6.3V_6 — +3VSUS

A3V3_OUT — +3VSUS

CARD_3V3_OUT — +3VCARD

AG33 AG_PLL DGND2 DGND1 — C629 *1U/10V_4 — C624 *0.1U/10V_4 — C917 *0.1U/10V_4

*RTS5158

For 5158

SP6 — R339 *0_4 — SD_DAT1

SP4 — R333 *0_4

For 5158E

AL005158B10 -->RTS5158E

AL005158B00 -->RTS5158

SI-2 remove R673 not need -- UMA BOM remove

+3VSUS_RTS — R323 *0_6 — +3VSUS

C593 *0.1U/10V_4 — C598 *4.7U/6.3V_6

+3VCARD — C628 *0.1U/10V_4 — C618 *0.1U/10V_4 — C617 *0.1U/10V_4

Note:

	SD/MMC	MS	XD
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6	SD_DAT1	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

SP7	R315 *0_4	MS_DATA0_SD_DAT0	
	R316 *0_4	XD-D6	
SP6	R334 *0_4	MS_DATA1	
	R338 *0_4	XD-D3	
SP8	R345 *0_4	MS_DATA2_XD_D2	
SP16	R666 *0_4	SD_DAT2	
	R676 *0_4	XD-RE#	
SP5	R327 *0_4	MS_BS	
	R335 *0_4	XD-D5	
SP15	R675 *0_4	SD_DAT3	
	R390 *0_4	XD_WE	
SP11	R354 *0_4	SD_CLK_MS_CLK	
	R358 *0_4	XD-D1	
SP2	R319 *0_4	SD_WP	
SP13	R677 *0_4	XD-WP#	
SP19	R393 *0_4	XD-CLE	
SP4	R317 *0_4	XD-D4	
SP10	R351 *0_4	MS_DATA3	
	R348 *0_4	XD-D7	
SP14	R389 *0_4	XD-RB#	
SP12	R369 *0_4	XD-D0	
SP17	R391 *0_4	XD-ALE	
SP18	R392 *0_4	XD-CE#	
SD_CMD_R	R372 *0_4	SD_CMD	

CH501H-40PT — D23 — MS_CD# — XD_CD# — SD_CD# — CH501H-40PT

C873 270P/25V_4

RTS5158 need to remove D23/D24/C873

JMB 380 Note:

	SD/MMC	MS	XD
MDID0	SD_DAT0	MS_D0	XD_D0
MDID1	SD_DAT1	MS_D1	XD_D1
MDID2	SD_DAT2	MS_D2	XD_D2
MDID3	SD_DAT3	MS_D3	XD_D3
MDID4	SD_CMD	MS_BS	XD_WE#
MDID5	SD_CLK	MS_SCLK	XD_CE#
MDID6	SD_WP		XD_WP#
MDID7			XD_CLE
MDID8	SD_DAT4		XD_D4
MDID9	SD_DAT5		XD_D5
MDID10	SD_DAT6		XD_D6
MDID11	SD_DAT7		XD_D7
MDID12			XD_RE#
MDID13			XD_R/B#
MDID14			XD_ALE
CR1_LEDN	SD1_LED#	MS1_LED#	XD_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#	XD1_PCTL#
CR1_CD0	SD1_CD#		XD_CV#
CR1_CD1		MS1_CD#	XD_CD#

5 IN1 CARD READER
XD,MMC/SD,MS/MSP

C905 *270P/25V_4

+3VCARD — R678 *10K/F_4 — XD-WP#

Del R625 for TP on PV

CN36

XD-R/B XD-RE XD-CE XD-CLE XD-ALE XD_WE XD-WE XD-WP XD-DATA0 XD-DATA1 XD-DATA2 SD-DATA3 SD-CMD GND MS-VCC MS-SDLK MS-DATA3 MS-INS MS-DATA2 MS-DATA0 MS-DATA1 MS-BS GND

GND GND GND GND GND SD-C/D SD-CD-SW SD-W/P SD-WP-SW XD-CD XD-VCC XD-DATA7 XD-DATA6 XD-DATA5 XD-DATA4 XD-DATA3 XD-DATA2 XD-DATA1 SD-DATA0 SD-CLK SD-VCC

XD-RB# XD-RE# XD-CE# XD-CLE XD-ALE XD_WE XD-WP# XD-D0 XD-D1 SD_DAT2 SD_DAT3 SD_CMD

SD_CD# SD_CD# SD_WP XD_CD# XD-D7 XD-D6 XD-D5 SD_DAT1 XD-D4 XD-D3 MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 SD_CLK_MS_CLK

SD_CLK_MS_CLK MS_DATA3 MS_CD# MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 MS_DATA1 MS_BS

26 MS_CD#

5IN1 CARD READER SOCKET

+3VCARD — C872 2.2U/6.3V_6 — R607 150K/F_4

CLOSE CONN

+3VCARD — C887 0.1U/10V_4 — C894 0.1U/10V_4 — C874 0.1U/10V_4

+3V — Q25 *AO3409 — +3VCARD

26 MC_PWR_CTRL_0# — XD_PWON R387 *10K/F_4 — +5V

+3VCARD — R332 0_8

RESERVED for JMicron -- after programming can out-put +3.3V throught MC_PWR_CTRL_0# signal

SI-2 for 台端Conn

+3VCARD — +3VCARD

CN42

xD-R/B xD-RE xD-CE xD-CLE xD-ALE xD-WE xD-WP xD-D0 xD-D1 SD-DATA2 SD-DATA3 SD-CMD GND MS-VCC MS-SDLK MS-DATA3 MS-INS MS-DATA2 MS-DATA0 MS-DATA1 MS-BS GND

GND GND GND GND NC NC SD-CD SD-WP xD-CD xD-VCC xD-D7 xD-D6 xD-D5 SD-DATA1 xD-D4 xD-D3 xD-D2 SD-DATA0 SD-CLK SD-VCC

XD-RB# XD-RE# XD-CE# XD-CLE XD-ALE XD_WE XD-WP# XD-D0 XD-D1 SD_DAT2 SD_DAT3 SD_CMD

SD_CD# SD_WP XD_CD# XD-D7 XD-D6 XD-D5 SD_DAT1 XD-D4 XD-D3 MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 SD_CLK_MS_CLK

26 SD_CD#

SD_CLK_MS_CLK MS_DATA3 MS_CD# MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 MS_DATA1 MS_BS

*TAI TWUM 5IN1 CARD READER SOCKET

26 MDIO00 — R611 0_4 — MS_DATA0_SD_DAT0
26 MDIO01 — R623 0_4 — XD-D0
R608 0_4 — SD_DAT1
R610 0_4 — MS_DATA1
R622 0_4 — XD-D1
26 MDIO02 — R612 0_4 — MS_DATA2_XD_D2
R620 0_4 — SD_DAT2
26 MDIO03 — R614 0_4 — MS_DATA3
R619 0_4 — SD_DAT3
R606 0_4 — XD-D3
26 MDIO04 — R618 0_4 — SD_CMD
R609 0_4 — MS_BS
R627 0_4 — XD_WE
26 MDIO05 — R617 47/F_4 — SD_CLK_MS_CLK
R634 47/F_4 — XD-CE#
26 MDIO06 — R593 0_4 — SD_WP
R591 0_4 — XD-WP#
26 MDIO07 — R633 0_4 — XD-CLE
26 MDIO08 — R605 0_4 — XD-D4
26 MDIO09 — R603 0_4 — XD-D5
26 MDIO10 — R602 0_4 — XD-D6
26 MDIO11 — R601 0_4 — XD-D7
26 MDIO12 — R679 0_4 — XD-RE#
26 MDIO13 — R635 0_4 — XD-RB#
26 MDIO14 — R628 0_4 — XD-ALE

SI-2 modified - for Jmicron updae

PAD8 MDC_SPRING — PAD9 MDC_SPRING — PAD10 MDC_SPRING — PAD11 MDC_SPRING

H32 *H-S315D110P2 — H31 *H-S315D110P2 — H13 *H-C273X118D173X118N — PAD7 — *MDC_SPRING

H22 *H-S315D110P2 — H23 *H-C244D118P2 — H6 *H-C217D157P2 — H9 *H-C217D157P2 — H8 *H-C217D157P2 — H3 *H-C256D157P2

H12 *H-C315D118P2 — H7 *H-S315D110P2 — H25 *H-C315D118P2 — H18 *H-C256D217P2 — H17 *H-C256D217P2

K/B SCREW HOLE — VGA Hole

H5 *H-S315D110P2 — H11 *H-S315D110P2 — H4 *H-C217D181P2 — H10 *H-C217D181P2 — H1 *H-C315D118P2

PAD4 — PAD5 — PAD6 — MDC_SPRING — *MDC_SPRING

Del PAD1 for TP on PV

PAD2 — PAD3 — *MDC_SPRING — *MDC_SPRING

for MDC cable routing

Mini Card Hole

H20 *H-C256D217P2 — H14 *H-C256D217P2

SI-2 for CN37

H28 *H-C236D87P2 — H29 *H-C236D87P2 — H30 *H-C236D87P2

H26 *H-C256D217P2 — H27 *H-C256D217P2

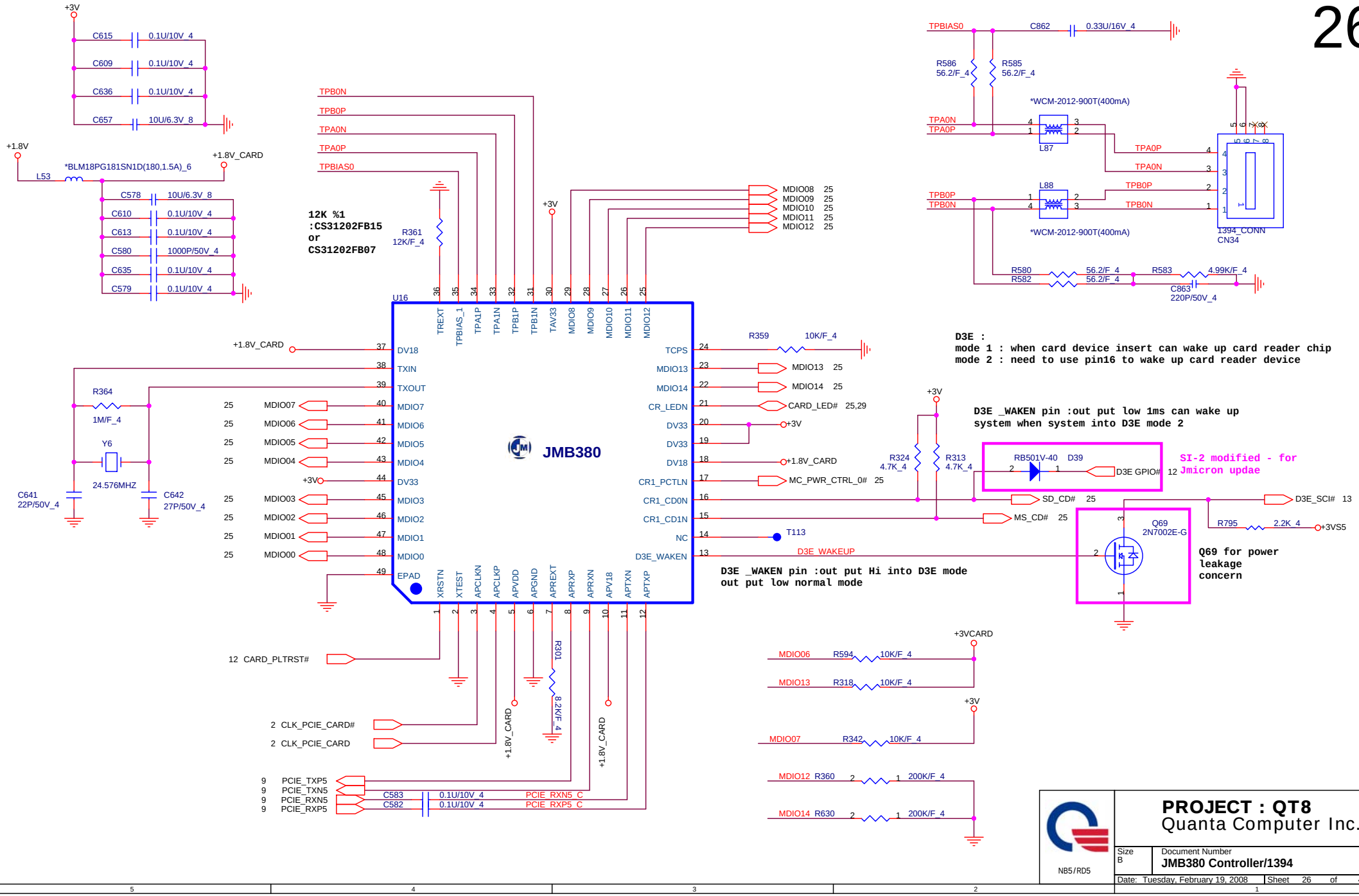
PAD12 — MDC_SPRING

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5158 & CR SOCKET &HOLE	1A

Date: Tuesday, February 19, 2008 — Sheet 25 of 45



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
B	JMB380 Controller/1394	1A

Date: Tuesday, February 19, 2008 Sheet 26 of 45

NB5/RD5

SI-2 Modified -- change footrint QFN48-7X7-5-49P-1H for datasheet update

SI-2 Modified

EAPD#--DEFAULT is Hi

SI-2 for EMI

92HD71B7

TO Internal Speakers

TO Headphone jack

Change C923, 924 footprint

Del R672 direct on PV

Del R686, R356, R349 direct on PV

Audio JACK: Normal Open
SA_A# -->EXT HP
SA_B# -->EXT MIC
SB_E#-->DOCK MIC

Change to SHORT-1A for EMI on PV

recommand use X7R /10V

TO EXTERNAL MIC

TO DOCK MIC

TO AUDIO/B CON.

SI-2 modified -- Change footprint for ME request , pin 13,14 are 固定pin

DOCK MIC DETECT

R807 change to 330K for HP on PV

Change C962, 963 footprint

Del R814, R815 on PV

TO DOCK Headphone

Add C141 for soft star on PV

TO Headphone jack

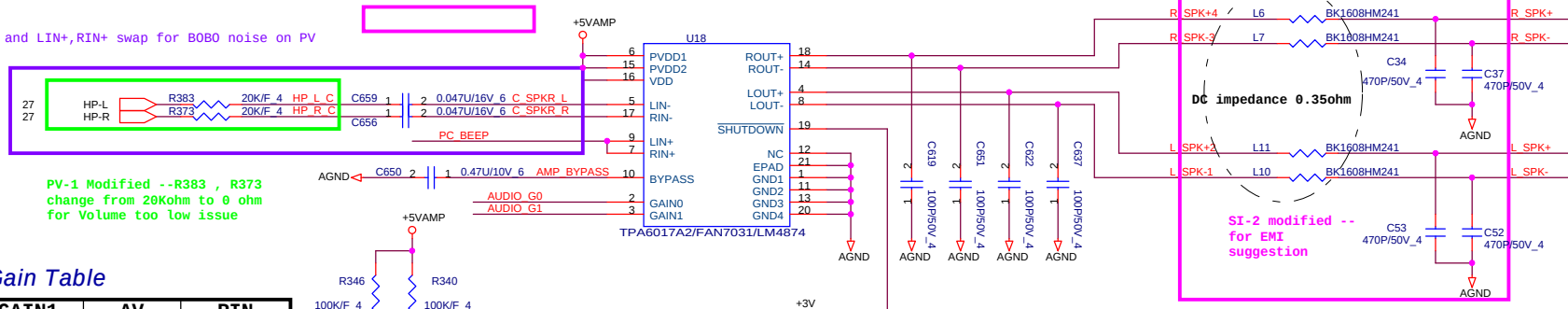
PROJECT : QT8		
Quanta Computer Inc.		
Size: Custom	Document Number: Azalia AD1883	Rev: 1A
Date: Tuesday, February 19, 2008	Sheet 27 of 45	

NB5/RD5

AUDIO AMPLIFIER

SI-2 Modified -- remove C621/C623

LIN-,RIN- and LIN+,RIN+ swap for BOBO noise on PV



PV-1 Modified --R383 , R373 change from 20Kohm to 0 ohm for Volume too low issue

INT. SPEAKER

Vrms = Vpp / 2 √2

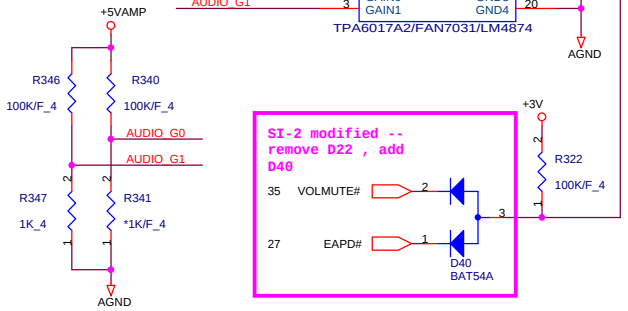
Power = (Vrms)²/ R

QT8 speaker -- 3.2ohm / 2W

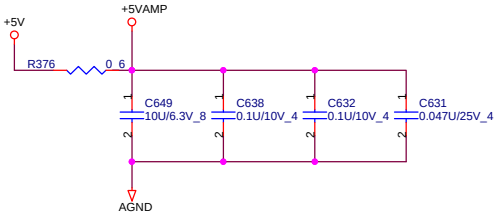
SI-2 modified -- for EMI suggestion

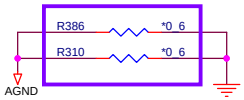
6017A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K



SI-2 modified -- remove D22 , add D40

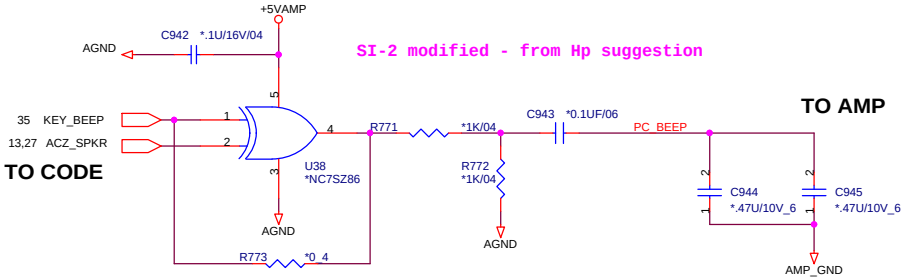




R386, R310 change to SHORT-1A on PV

PC-BEEP

SI-2 modified - from Hp suggestion



MUTE_LED

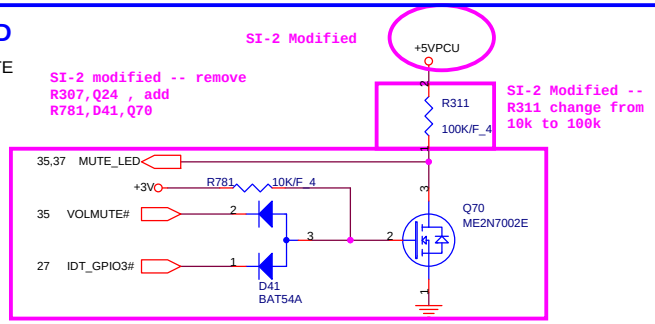
Low -->un-MUTE

High-->Mute

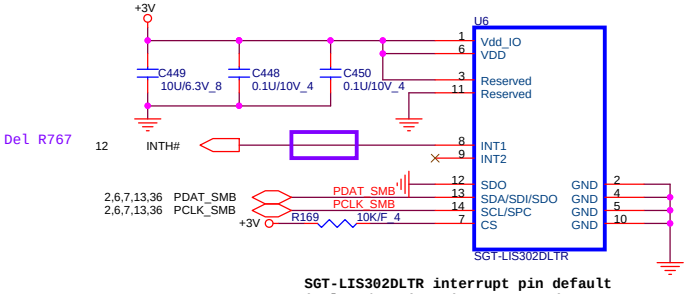
SI-2 Modified

SI-2 modified -- remove R307,Q24 , add R781,D41,Q70

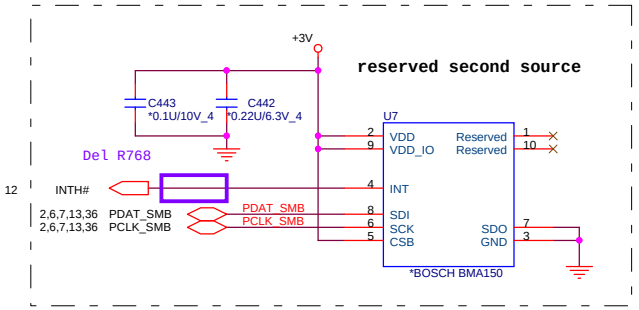
SI-2 Modified -- R311 change from 10k to 100k



Acceleration sensor



SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



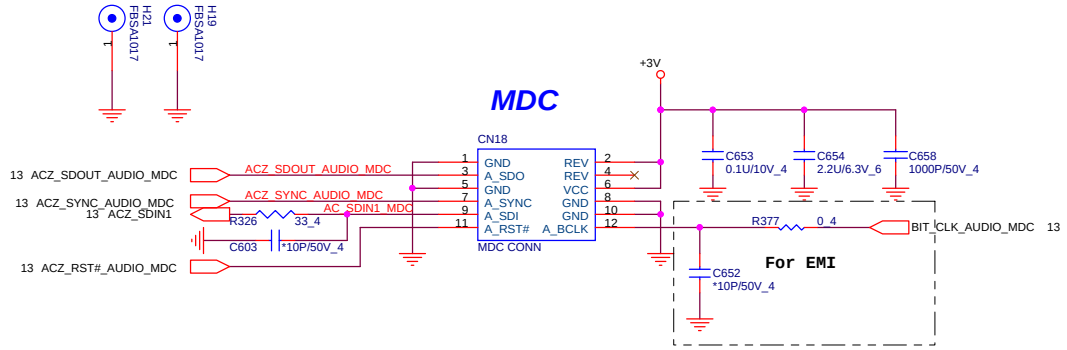
PROJECT : QT8
Quanta Computer Inc.

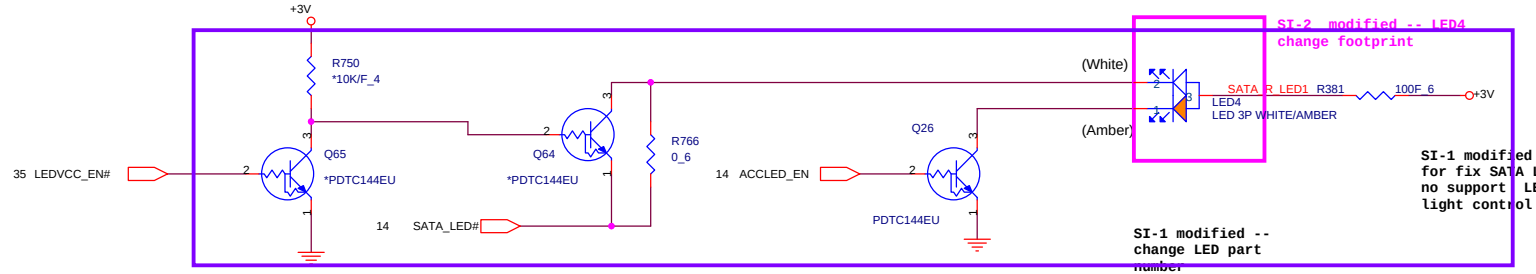
Size	Document Number	Rev
Custom	AMP_TPA6017/INT SPK	1A

NB5/RD5

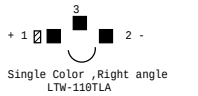
Date: Tuesday, February 19, 2008 Sheet 28 of 45

Modem CONN

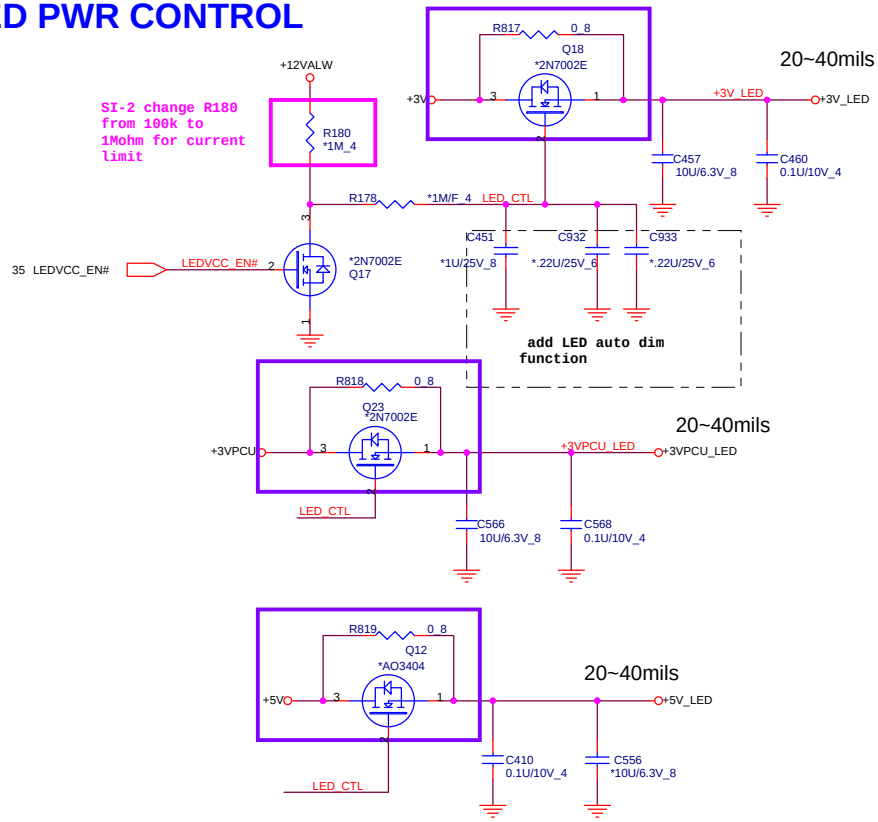




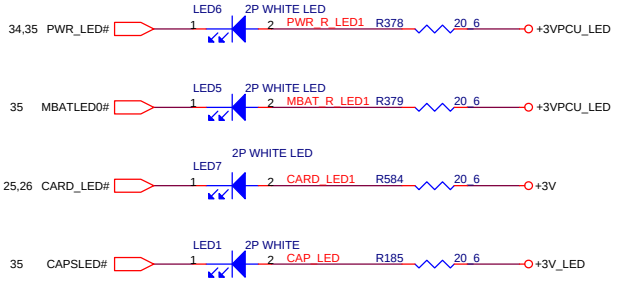
LED

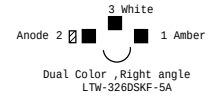


LED PWR CONTROL

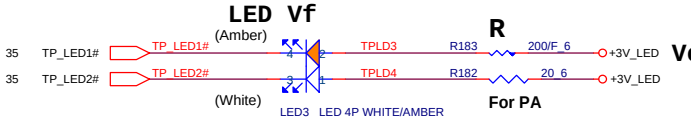


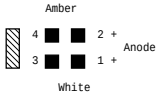
Del R380
Change R381 to 100
Add R766, R817, R818, R819
LED PWR control no-stuff on PV





I = Vcc -Vf / R





NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MDC1.5 Con Accelerometer/ILED	1A

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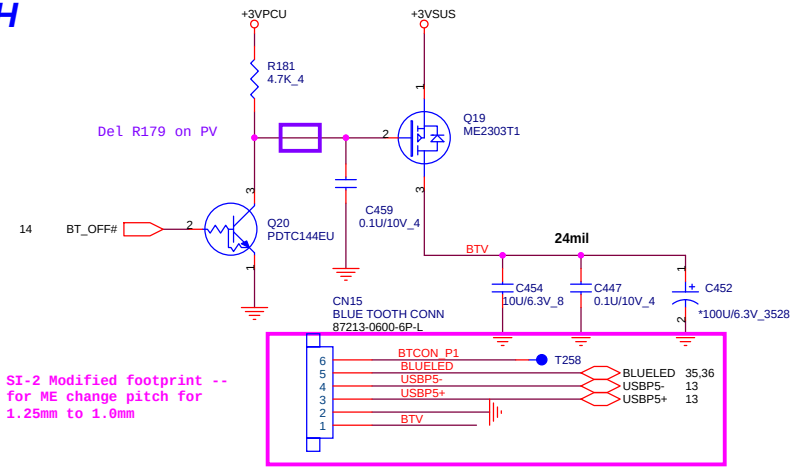
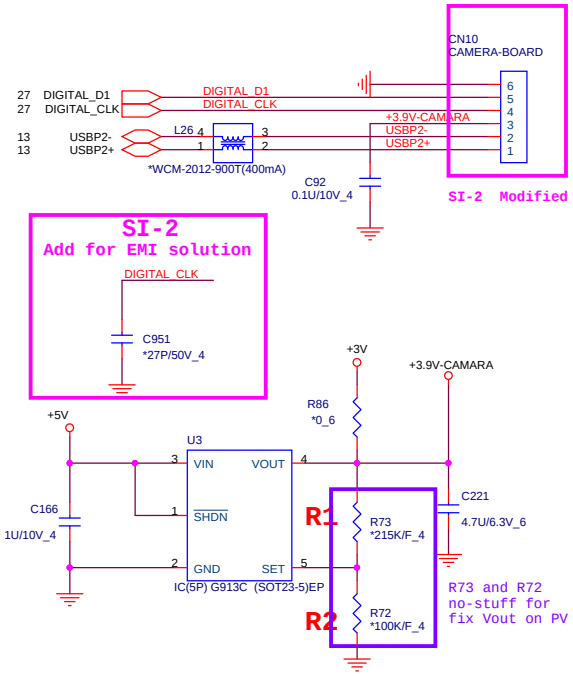
BLUETOOTH



For Discrete Touch-Screen

SI-2 Modified -- remove touch-screen function

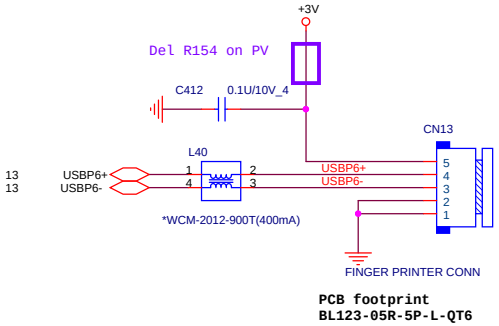
USB CAMERA CONNECT



Vout=1.25(1+R1/R2)

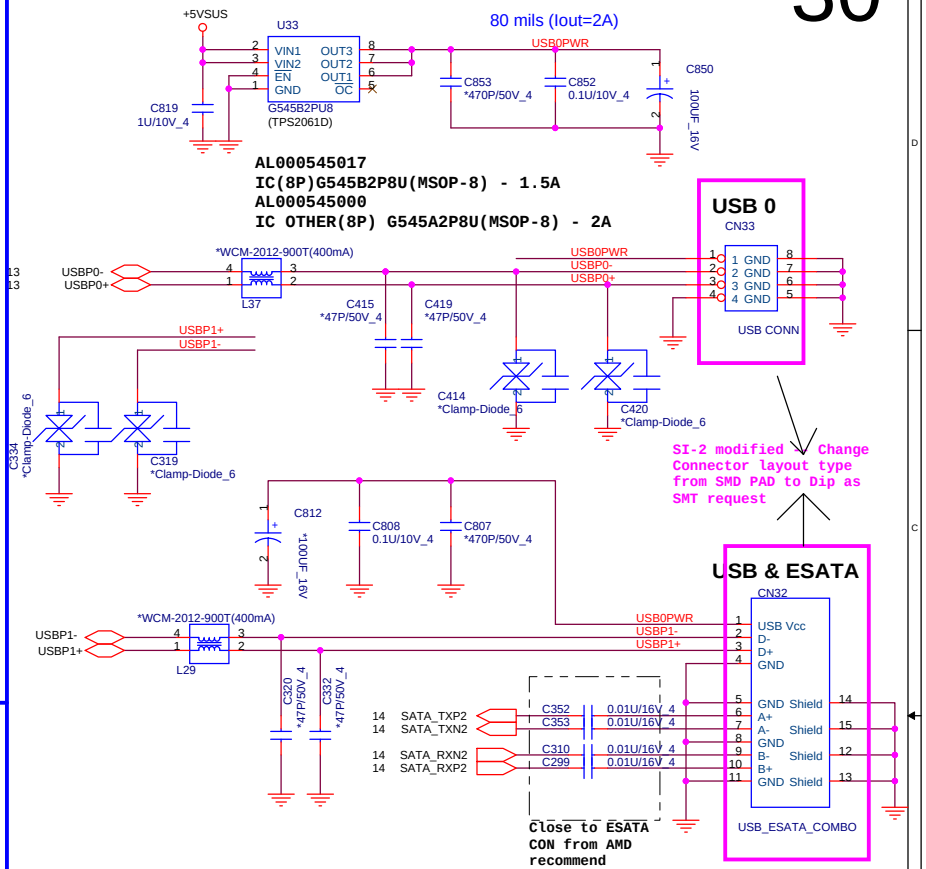
USB Fingerprint CON

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

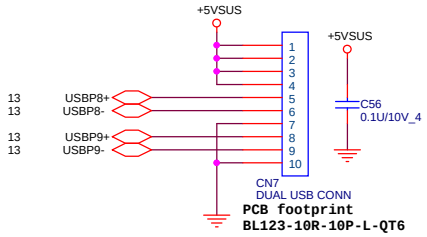


PCB footprint
BL123-05R-5P-L-QT6

LEFT SIDE USBX1 and E-SATA/USB COMBO



RIGHT SIDE USBX2



PCB footprint
BL123-10R-10P-L-QT6

NB5/RD5	PROJECT : QT8 Quanta Computer Inc.	
	Size: Custom Document Number: BT/WEBCAM/FT/USBX4/ESATA	Rev: 1A
	Date: Tuesday, February 19, 2008	Sheet 30 of 45

Stuffed for 8101E/8102E/RTL8111C

Stuffed for RTL8111C(10/100/1000)

Stuffed for 8102E/RTL8101E

Del R50 on PV

Del R36, C712, C710 on PV

Del R766 for TP on PV

Del U1, R46 on PV

use BIOS to programming EEPROM , EEDI should be pull Hi

R46 only for 8111B, 8101E&8102E&8111C can remove

Remove R456 and Add D42 on PV

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

R778 SI-2 modified -- RTL8111C remove , RTL8111B,8101E,8102E need to stuff

Del R429, R431, R433, R435, C718, C726 for 8111B on PV

Del R428 on PV

SI-2 modified -- LAN_PLTRST# is 3VS5 power rail , Maybe can remove NAND GATE

Link

AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)

AL08101E005 IC(64P)RTL8101E-GR(QFN)

NS892402:GIGABIT DB0AT9LAN05

NS892405:10/100 DB0ZB1LAN04

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8111C/8101E/RJ11-RJ45 CN	1A

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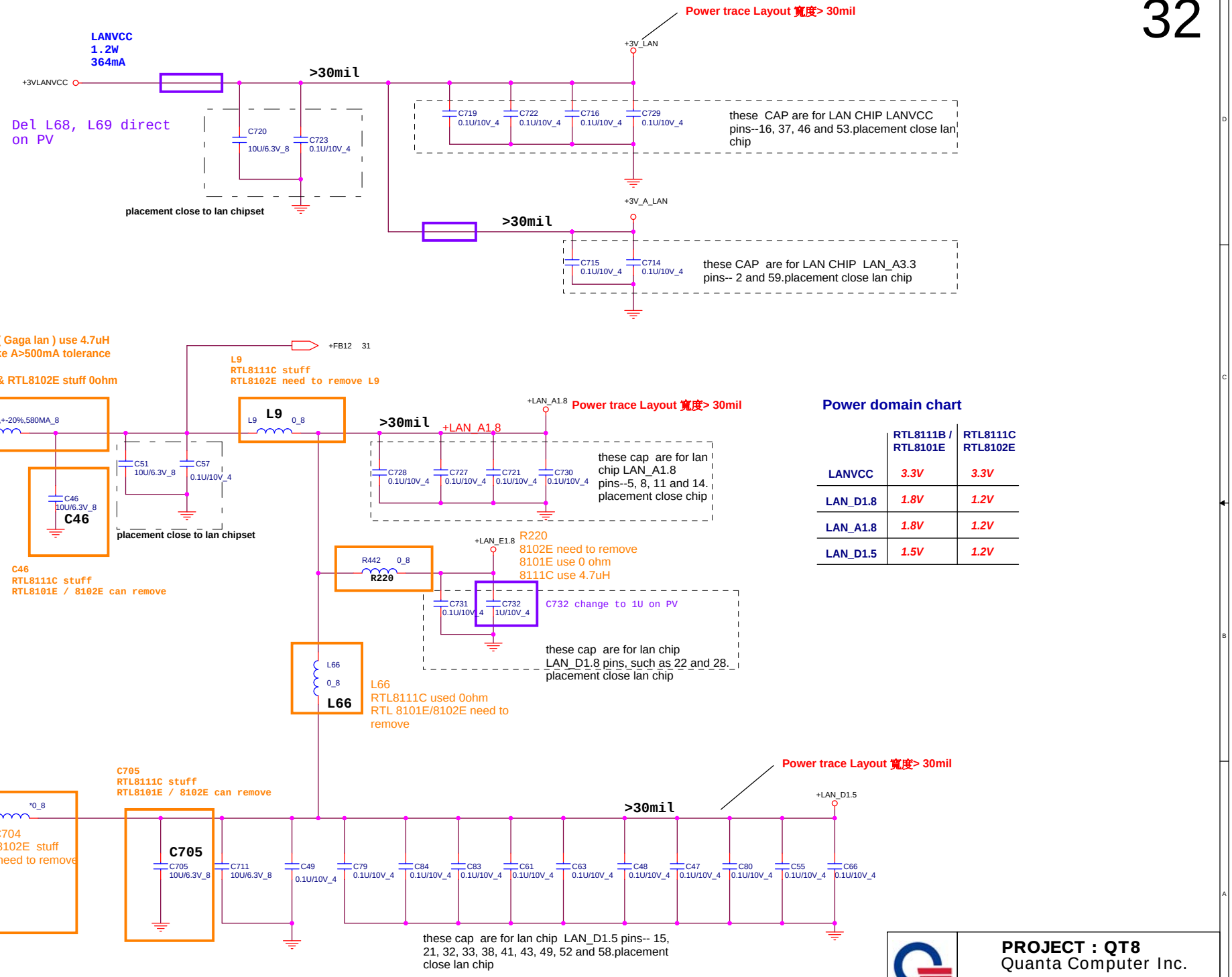
NB5/RD5



Power domain chart

	RTL8111B / RTL8101E	RTL8111C RTL8102E
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN Power	1A

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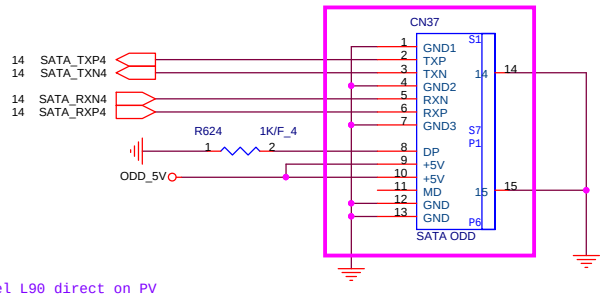
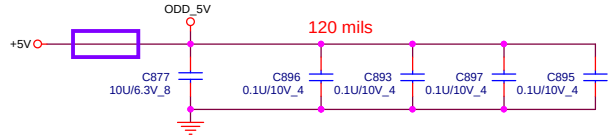
NB5/RD5

SATA CD-ROM

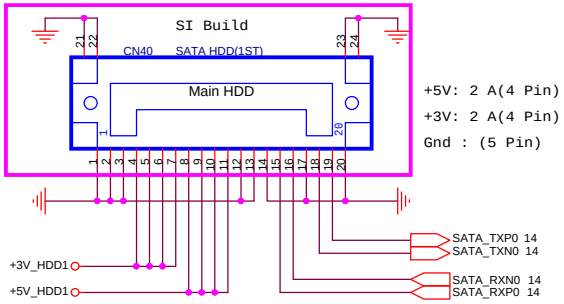
SI-2 Modified footprint -- Modify 12/27



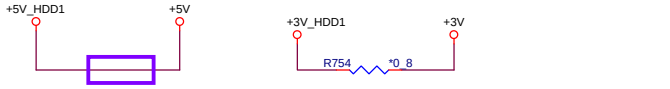
Del L90 direct on PV



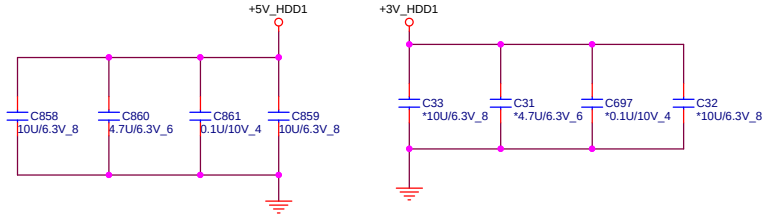
SI-2 Modified footprint -- Modify 固定孔 Size as SMT request



+5V: 2 A(4 Pin)
+3V: 2 A(4 Pin)
Gnd : (5 Pin)



Del R578 direct on PV

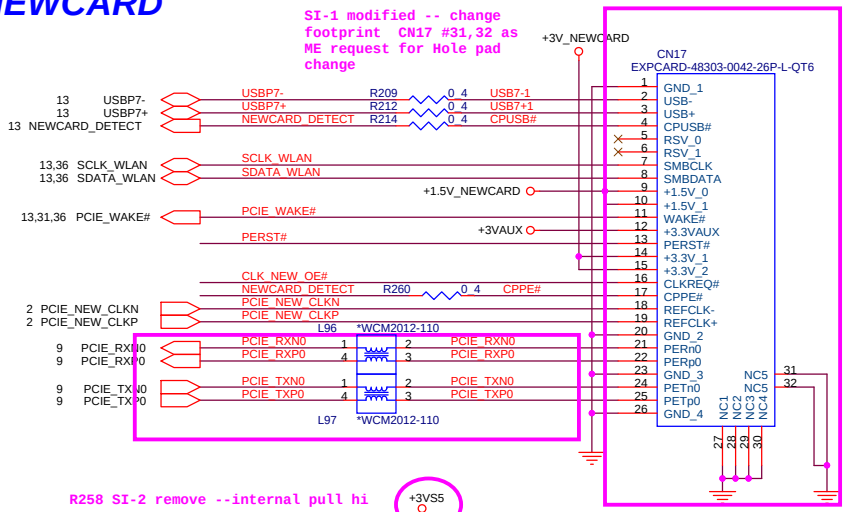


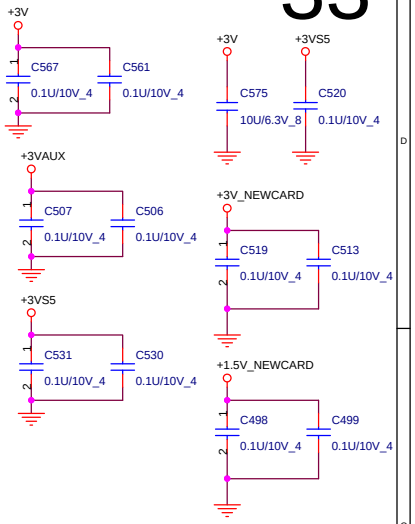
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)

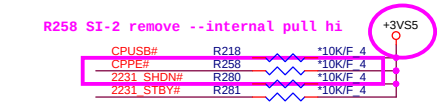
33

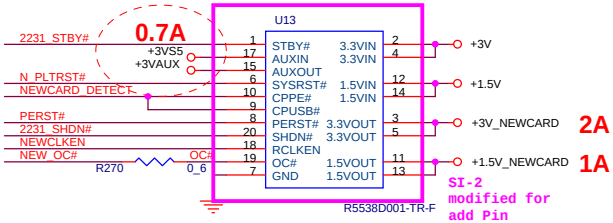
SI-1 modified -- change footprint CN17 #31,32 as ME request for Hole pad change





R258 SI-2 remove --internal pull hi





2A

1A

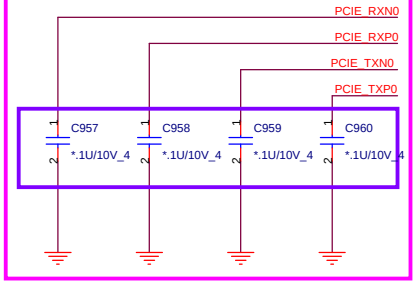
Del R790, R791, R792, R793 for RF on PV

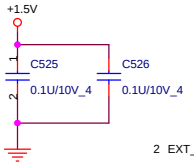
SI-2 modified for add Pin 21~25 as U25 Thermal pad tied to Gnd

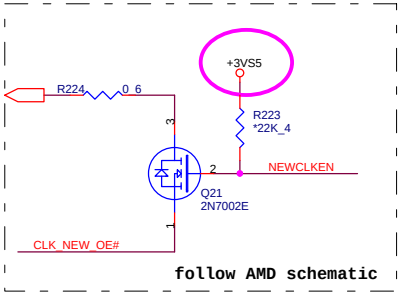
R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN

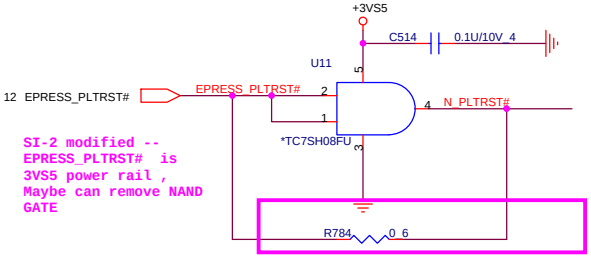
SI-2

For HP request to reserve



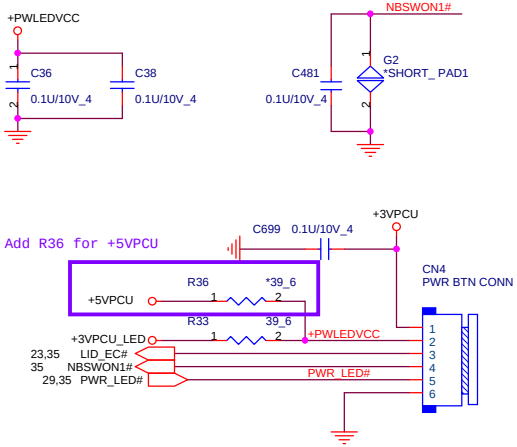






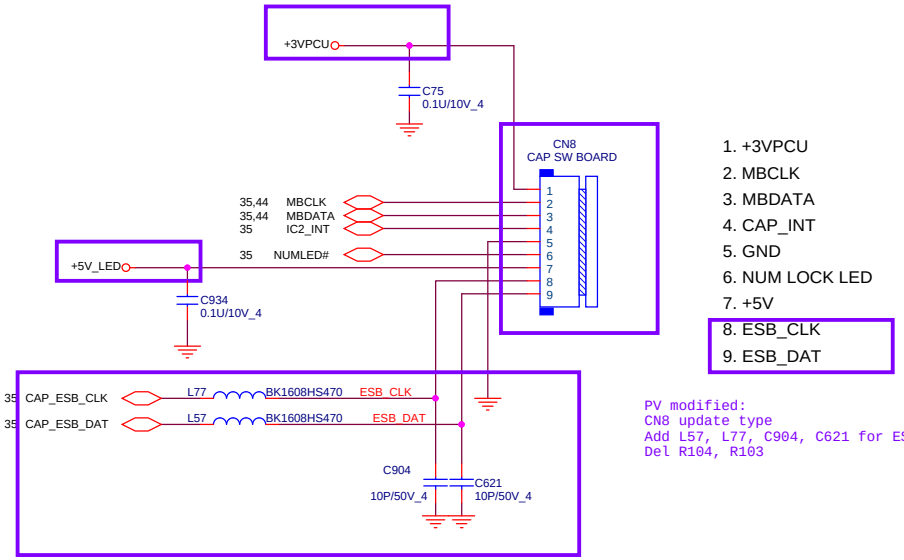
SI-2 modified -- EPRESS_PLTRST# is 3VS5 power rail , Maybe can remove NAND GATE

POWER BUTTON CONNECT



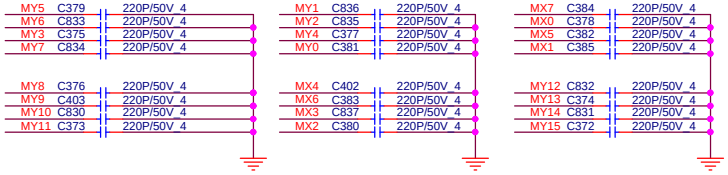
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

CAP SW CONNECT



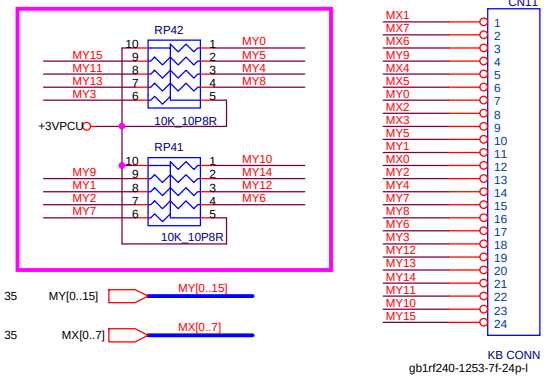
1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V
8. ESB_CLK
9. ESB_DAT

PV modified:
CN8 update type
Add L57, L77, C904, C621 for ESB
Del R104, R103



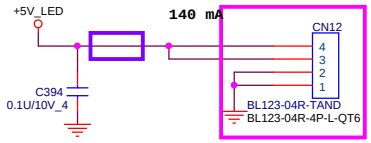
SI-2 Modified
-- net swap for
layout concern

KEYBOARD PULL-UP



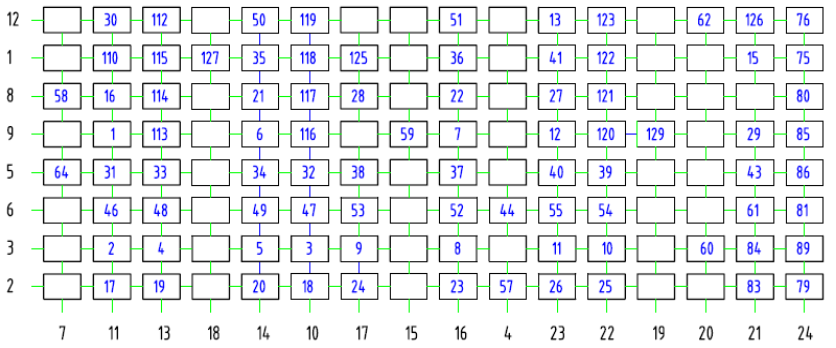
Del R770 on PV

SI-2 Modified 12/27



1.LEDVCC
2.LEDVCC
3. NC
4. GND

SI-2 Modified



NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KEYBOARD/SW	1A

Date: Tuesday, February 19, 2008 Sheet 34 of 45

Change U9 layout footprint
to LQFP128-16X16-4-AA1

U9

KB3926

For KB3926 C version

SI-2 for fix cpu vcore

SI-2 Modified for hp request

Battery charge/discharge
Cap button

VGA thermal
system thermal

Pin 17 (GPIO0B) ==> assigned for
ESB_CLK / Pull high 4.7K
Pin 18 (GPIO0C) ==> assigned for
ESB_DAT / Pull high 4.7K

LAN_RESET# move to Pin 25
pin 18 (SWI#1) move to Pin 31

reserved for H/W CIR

Del R256 for TP on PV

SI-2 ADD R256 for H/W CIR

SB780 internal have pull hi

SI-1 modified -- change vaule

change D11 type for PV

UMA BOM missing

64.9K -->65W

33.7K -->90W

SI-2 modified for avoid AD-_ID noise

SI-2 Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier

SB internal pull Hi 10k to 3v_s5

Change D12, D16 to RB500 for current loss

SB internal pull Hi 10k to 3v_s5

close conn

TOUCH PAD CONNECTOR

Del L86 on PV

25 mils

CN14
TOUCH PAD CONN

PCB footprint
BL121-12R-12P-L-QT6

PA

Update SW2, SW4, SW6 P/N on PV

TOUCH PAD ON/OFF

TOUCH PAD L/R

Blue LED change to 100K ohm pull low on PV

Del R246, R254 direct on PV

SST	AKE5GFK0Z09	**1M byte SPI BIOS**	
WINBOND	AKE3GFP0N08		
PME	AKE3GZP0500		
EON	AKE3GZP0Q00		

CS36492FB17	RES CHIP 64.9K 1/16W +-1%(0402)	
CS33322FB13	RES CHIP 33.2K 1/16W +-1% (0402)	

PROJECT : QT8
Quanta Computer Inc.

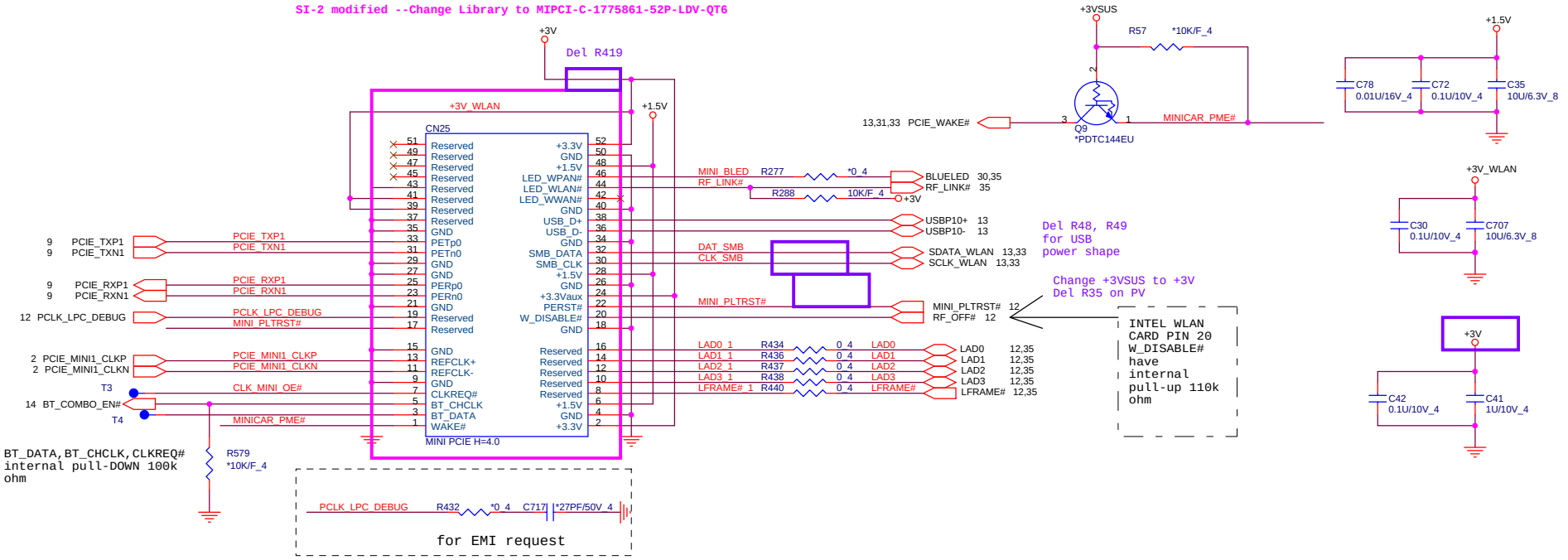
Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A

Date: Tuesday, February 19, 2008 | Sheet 35 of 45

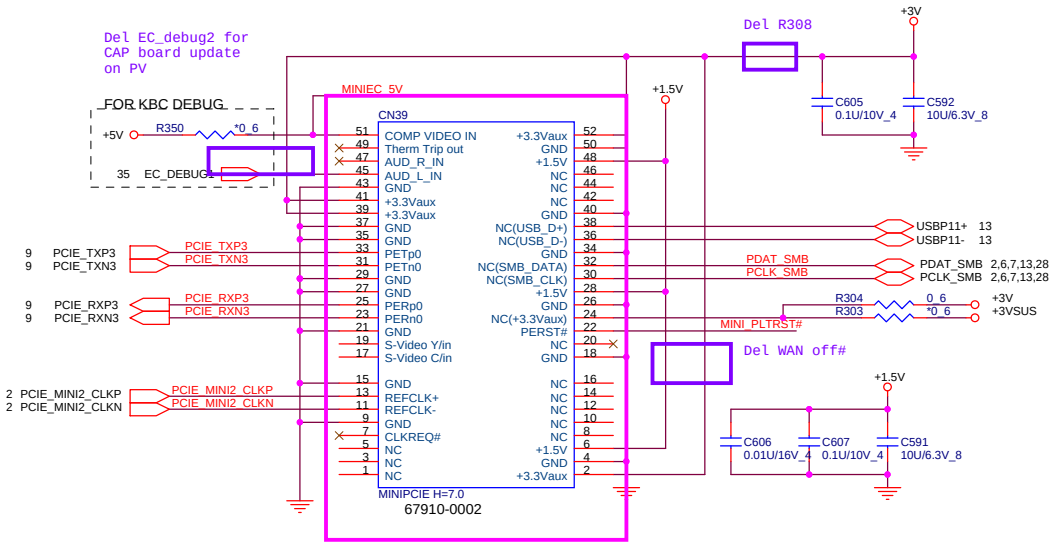
NB5/RD5

Mini PCI-E Card 1 WLAN

SI-2 modified --Change Library to MIPCI-C-1775861-52P-LDV-QT6



Mini PCI-E Card 2 TV tuner card



SI-2 modified --Change Library to MIPCIE-P04-FJ504-170-52P-QT6

NB5/RD5	PROJECT : QT8 Quanta Computer Inc.	
Size: Custom	Document Number: Mini CARD X 3	Rev: 1A
Date: Tuesday, February 19, 2008	Sheet 36 of 45	

CABLE DOCK

support 6A 200mils
CX000480005

SI-2 modified follow QT6 schematic
remove R671,R670,C916,Q30,L65,C669,R388

27 SPDIF — R779 221/F_4 — C949 .1U/50V_6 — SPDIF_DOCK
R780 100/F_4
C950 220P/50V_4

44 +DOCK_VA — L5 48/6A_12 — VA_P
C29 0.1U/50V_6
C17 0.1U/50V_6

13 USBP4-
13 USBP4+
L4 *WCM-2012-900T(400mA)
USBP4-
USBP4+

CN21 DOCKING CONN

VA_P	44 VDD	VDD 43	VA_P
CRT_GDK	38	39	
CRT_RDK	40	37	
	34	35	
CRT_BDK	36	33	
24 DDCDAT2	30	31	
24 PR_HSYNC — R18 33_6 — PR_HSYNC_D	32	29	CIR_IN 27,35
24 DDCCLK2	26	27	PWR_ON
USBP4-	28	25	MUTE_LED
24 PR_VSYNC — R20 33_6 — PR_VSYNC_D	22	23	SLP_BTN#
USBP4+	24	21	JACK_SEN#
31 LAN_MX3+	18	19	VOLME_UP#
31 LAN_MX3-	20	17	VOLME_DN#
		15	SPDIF_DOCK
31 LAN_MX2+	14	13	AGND
31 LAN_MX2-	16	11	RSPK_DK_L
31 LAN_MX1+	10	9	LSPK_DK_L
31 LAN_MX1-	12	7	
31 LAN_MX0+	6	5	DOCK_MIC_R
31 LAN_MX0-	8	3	DOCK_MIC_L
+VIN	2	1	DOCK_PRESENT
	4		
	VSS 42	VSS 41	
	46	45	

MUTE_LED 28,35
SLP_BTN# 35
JACK_SEN# 27
VOLME_UP# 35
VOLME_DN# 35
Remove R410, R411
AGND
RSPK_DK 27
LSPK_DK 27
DOCK_MIC_R 27
DOCK_MIC_L 27
AGND

C698 0.1U/50V_6

SI-2 modified --
for power leakage
concern

+3V — R413 100K/F_4
+3VPCU — R415 *100K_4
PR_INSERT# — PR_INSERT# 24,35

docking
insert is HI
voltage

Q31 MMBT3904
DOCK_PRESENT — R412 — DKPR# 1K/F_4
R414 2K/F_4

+5V
+5VSUS — R409 10K/F_4 — DK_PWRON
D29 RB500V-40
D30 RB500V-40
PWR_ON

Change D29, D30 to RB500
for current loss on PV

S0: 4V
S3: 2.5V
S4/S5:
0V

*Check
voltage on
DB

R408 15K/F_4

24 PR_GEN — R12 0_6 CRT_GDK
24 PR_RED — R11 0_6 CRT_RDK
24 PR_BLU — R15 0_6 CRT_BDK

R16 150/F_4
R9 150/F_4
R13 150/F_4
C25 5.6P/50V_6
C19 5.6P/50V_6
C23 5.6P/50V_6
C24 5.6P/50V_6
C20 5.6P/50V_6
C21 5.6P/50V_6

filter for docking CRT

CPU FAN

+3V — R177 4.7K_6
35 FAN1SIG
20 mil
+5VFAN1
CN26 FAN CONN
C725 2.2U/6.3V_6
C724 0.1U/10V_4

+5V
C687 1U/10V_4
R420 10K/F_4
U24 G995
VIN VO
/FON GND
GND
VSET GND
+5VFAN1
FAN_SMBALERT#
35 FAN1ON

G955 /FON
signal have
internal
pull Hi to
VIN , R420
maybe can
remove

FANPWR = 1.6*VSET

8 7 6 5
Gnd shape
1 2 3 4

G995 layout notice

VOLME_DN#
CIR_IN
PR_HSYNC_D
PR_VSYNC_D
C27 *47P/50V_4
C26 *47P/50V_4
C688 *100P/50V_4
C692 *100P/50V_4

DOCK_MIC_R
DOCK_MIC_L
RSPK_DK_L
LSPK_DK_L
JACK_SEN#
C691 *270P/25V_4
C693 *180P/50V_4
C694 *180P/50V_4
C696 *180P/50V_4
C695 *180P/50V_4
AGND AGND AGND AGND AGND

SI-2 modified

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CABLE DOCKING/FAN	1A

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DC/DC +3VPCU/+ 5VPCU/ +12VALW

+3V 2,3,5,6,7,10,11,12,13,14,15,16,18,20,23,24,25,26,27,28,29,30,31,33,35,36,37,39,43

+5VPCU 27,28,34,35,39,40,41,42,43
+3VPCU 5,12,23,29,30,34,35,37,40,41,42,44
+3VSUS 13,25,30,36,39,41,43
+3VS5 5,7,12,13,14,15,16,23,26,33,43
+5VSUS 23,30,35,37,43
+5V 5,15,20,23,24,25,27,28,29,30,33,36,37,39,42,43
+LANVCC

TON: 5V / 3.3V
GND = 400 / 500KHz
REF = 400 / 300KHz
VCC = 200 / 300KHz

5 Volt +/- 5%
+5VPCU
C/C:8A
P/C:10A

Place these CAPs close to FETs

Vout=0.7(Ra+Rb)/Rb
Rb around 49.9k

SI-1 Modified - ECAP6_3X6_1-7_2-QT8

Rds(on) 15m ohm

I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM

Del PR159 for TP on PV

3.3 Volt +/- 5%
+3VPCU
C/C:8A
P/C:10A

SI-1 Modified -ECAP6_3X6_1-7_2-QT8

+3V
6.76A
S0-S1

+3VS5
0.5A
S0-S5

+3VSUS
1.84A
S0-S3

+5V
4.31A
S0-S1

+5VSUS
4.5A
S0-S3

+LANVCC
0.27A

5,7,12,13,14,15,16,23,26,33,43 +3VS5
+3VSUS 13,25,30,36,39,41,43
+5V 5,15,20,23,24,25,27,28,29,30,33,36,37,39,42,43
+5VSUS 23,30,35,37,43
+3VLANVCC 31,32,43
HWPG 20,23,35,39,41,42

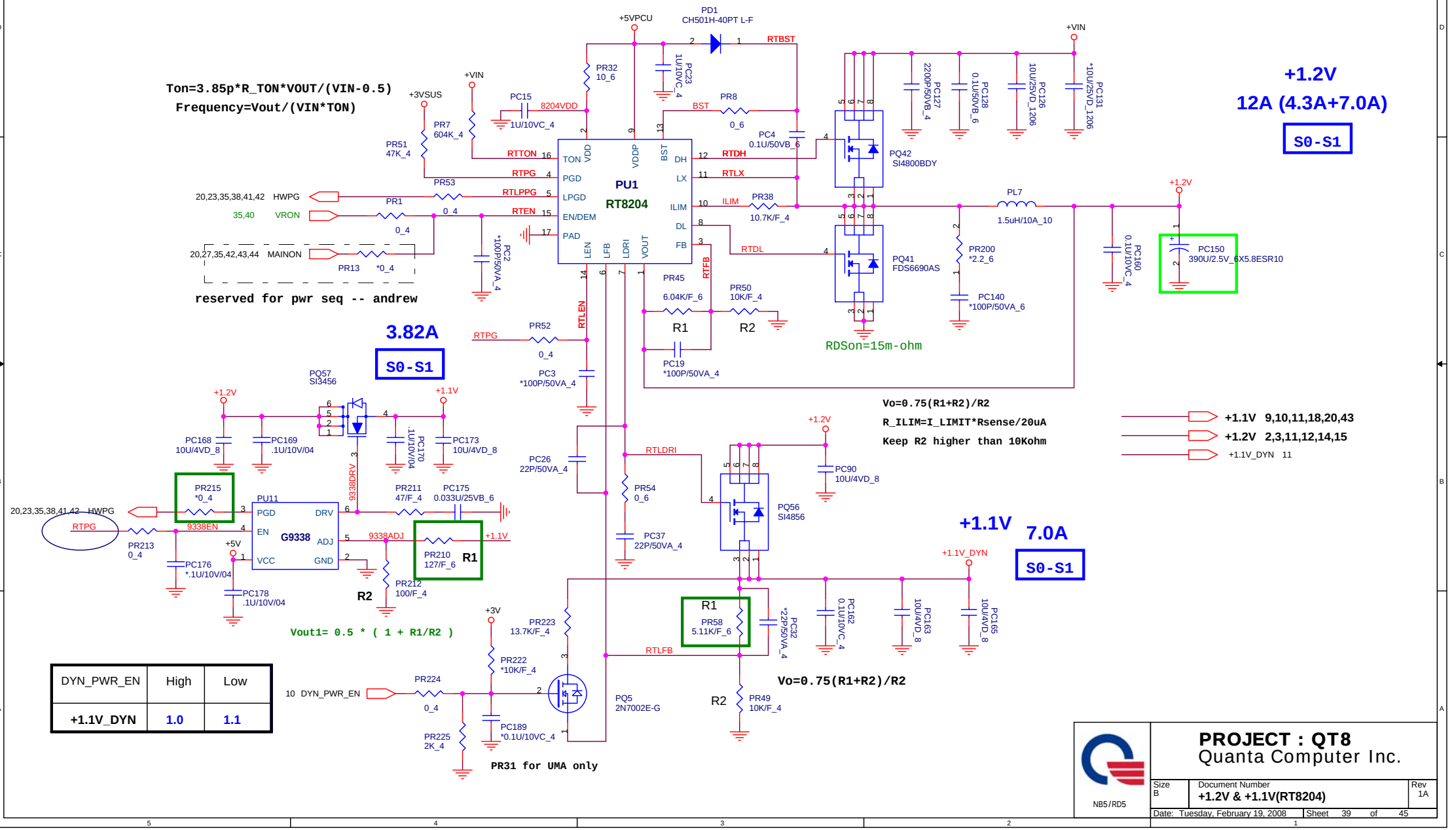
For EMI-SI

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V(ISL6237)	1A
Date: Tuesday, February 19, 2008	Sheet 38 of 45	

NB5/RD5

+1.1V & +1.2V

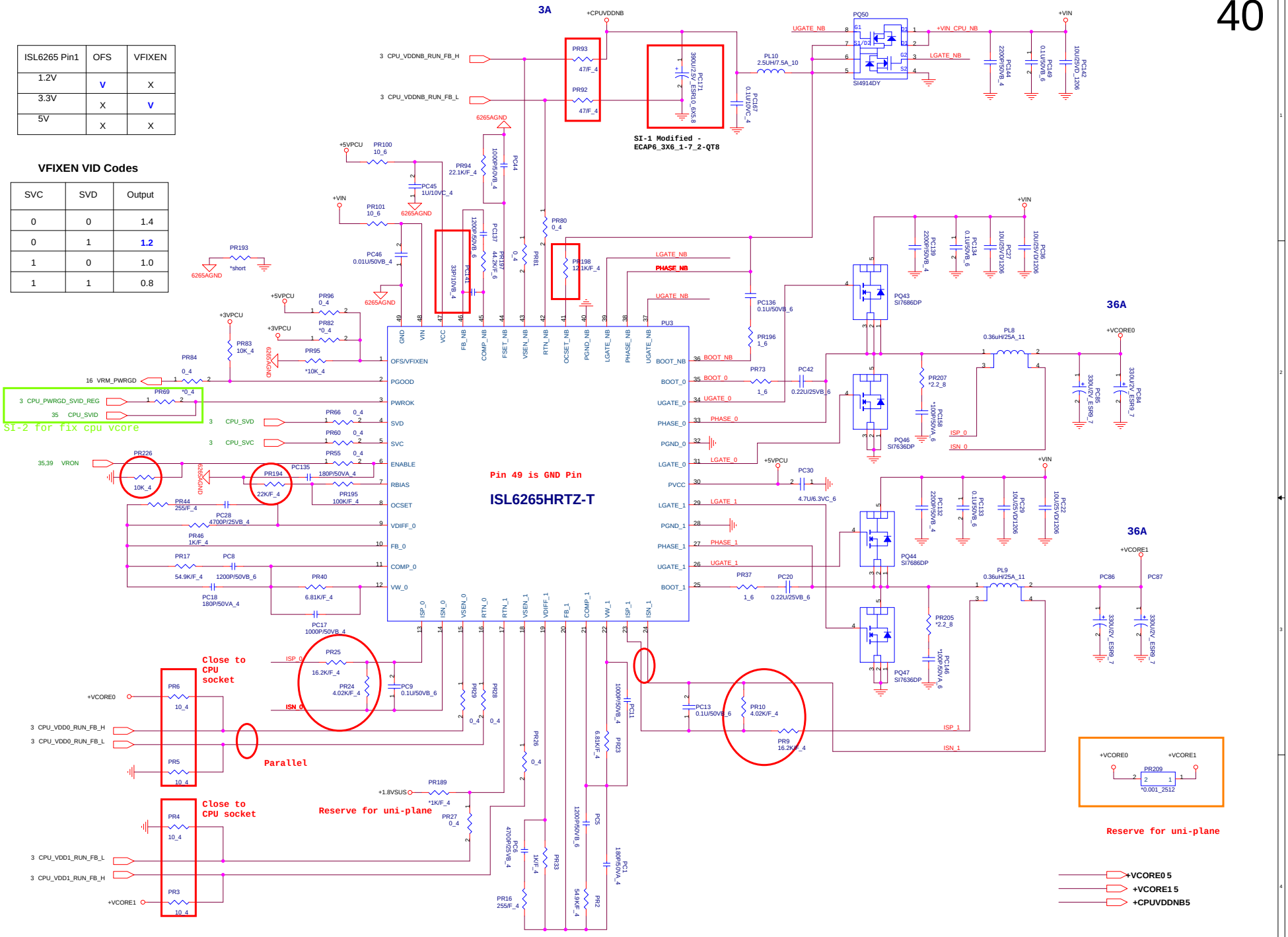


DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

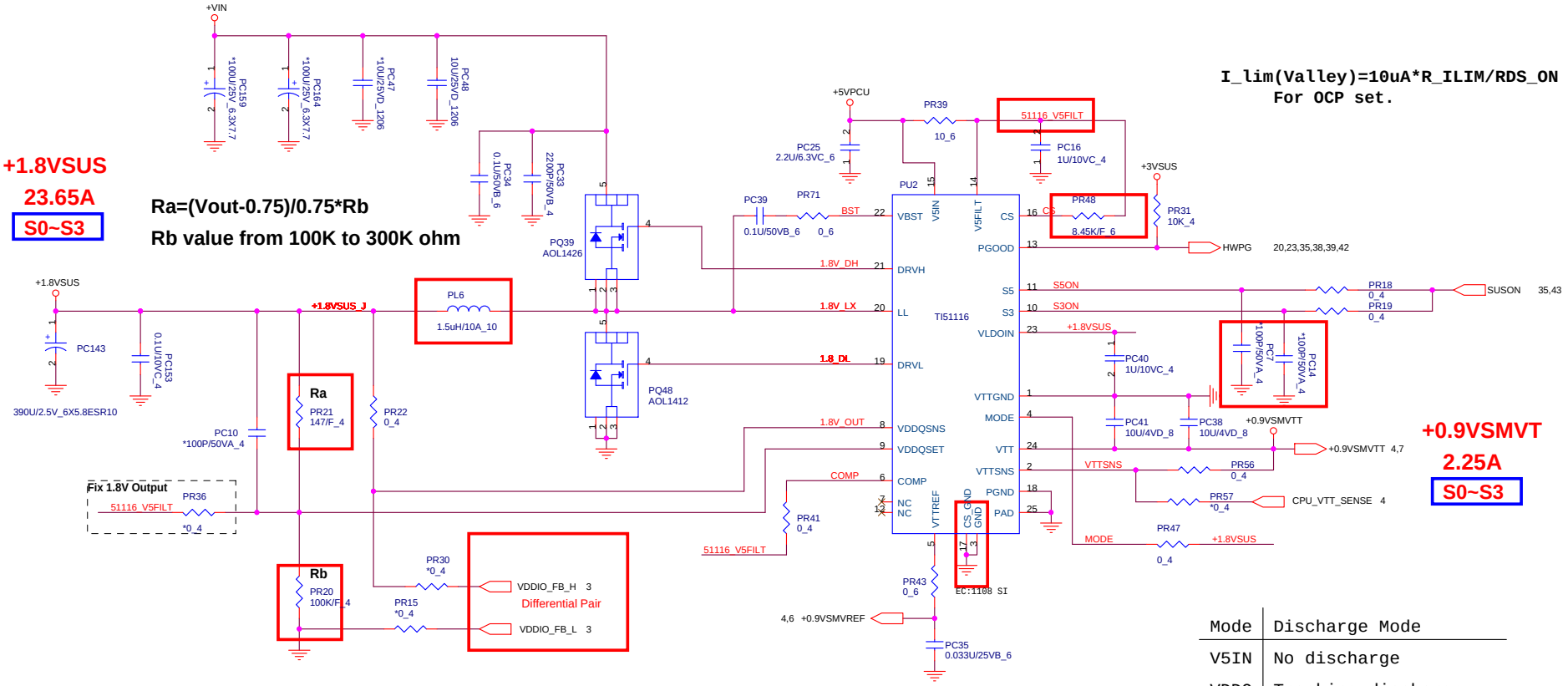


+2.5V 3
+1.8VSUS 3,4,5,6,7,40,42,43

+1.8VSUS
23.65A
S0~S3

Ra=(Vout-0.75)/0.75*Rb
Rb value from 100K to 300K ohm

I_lim(Valley)=10uA*R_ILIM/RDS_ON
For OCP set.

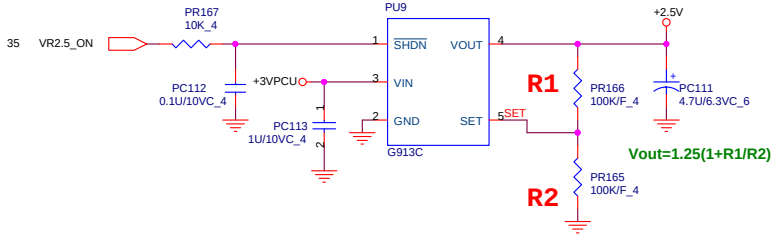


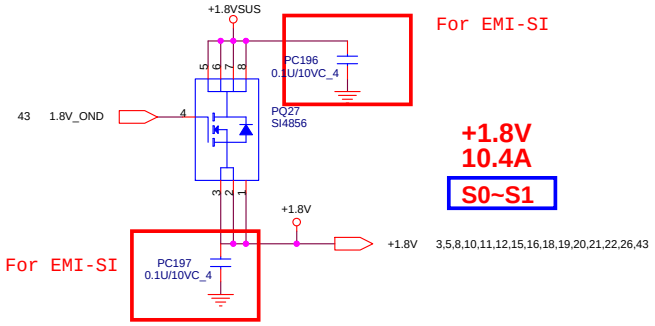
+0.9VSMVT
2.25A
S0~S3

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

+2.5V
0.25A
S0~S1

Close to CPU
SI power





+1.8V
10.4A
S0~S1

Discrete:SI4856
UMA:SI4800

V_TRIP(mV)=R_TRIP(Kohm)*10(uA)

I_OCP=V_trip/Rds_on+I_Ripple/2

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V

PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	1.8VSUS/DDR_VTER/+1.8V/2.5V	1A

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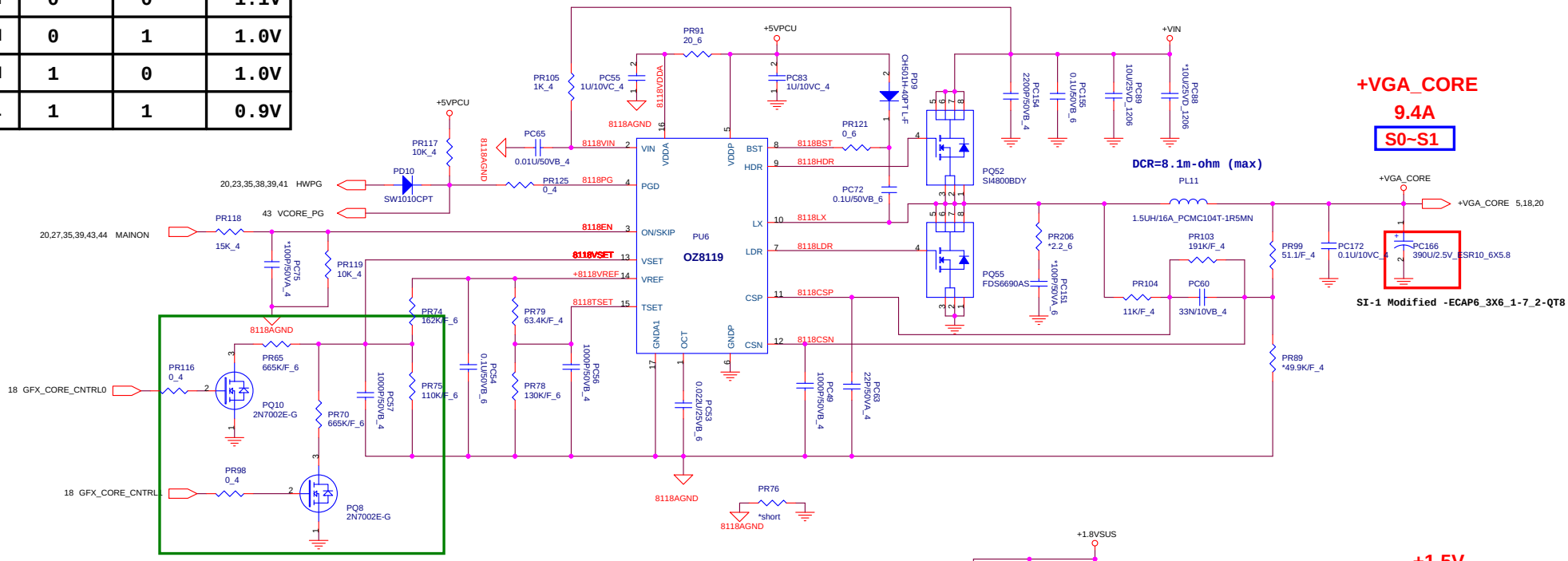
ATI M82-SE

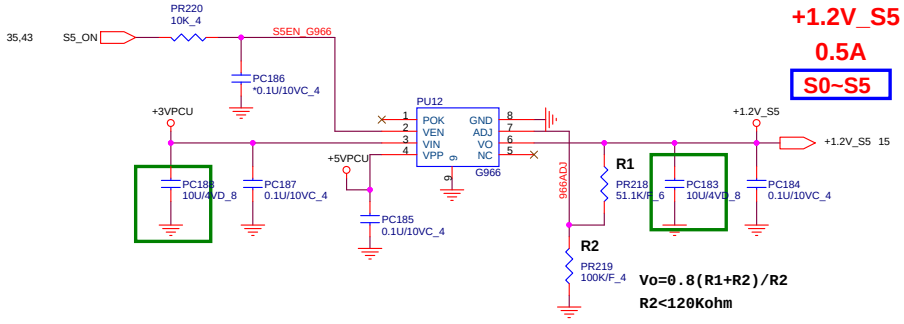
	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

+VGA_CORE5,18,20
+1.2V_S5 15
+1.5V 33,36

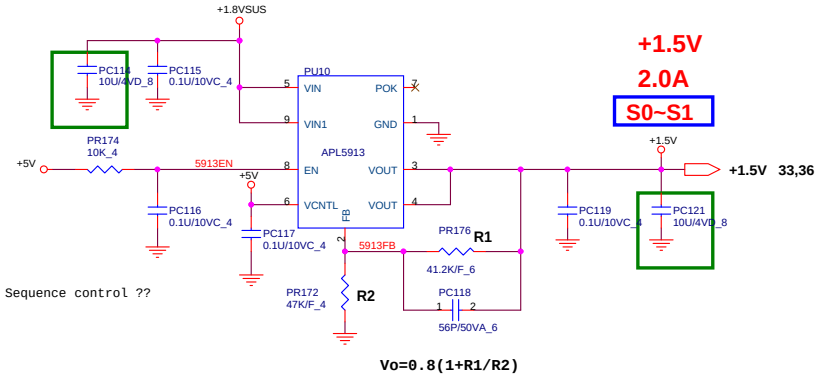
+VGA_CORE
9.4A
S0~S1



+1.2V_S5
0.5A
S0~S5

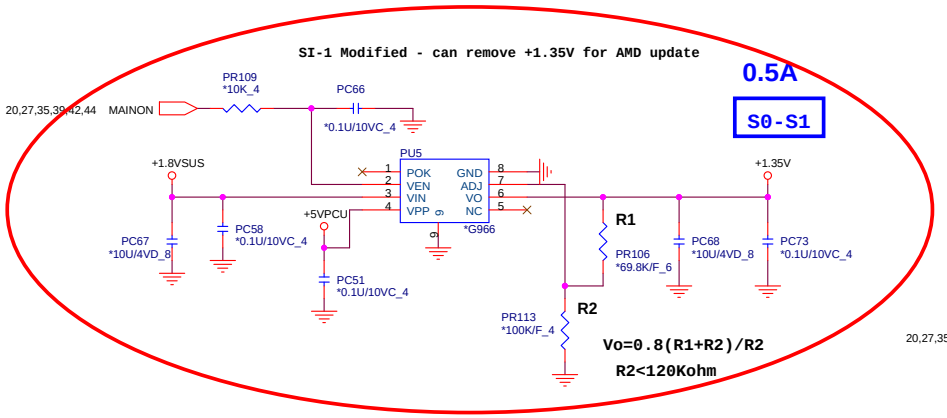


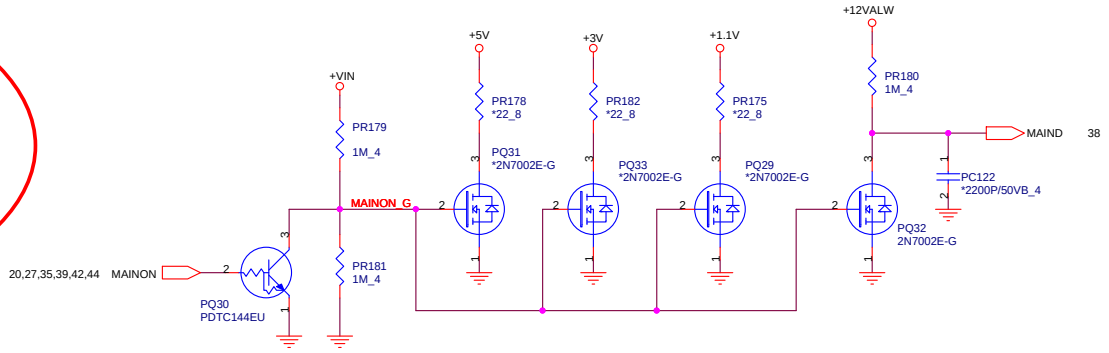
+1.5V
2.0A
S0~S1

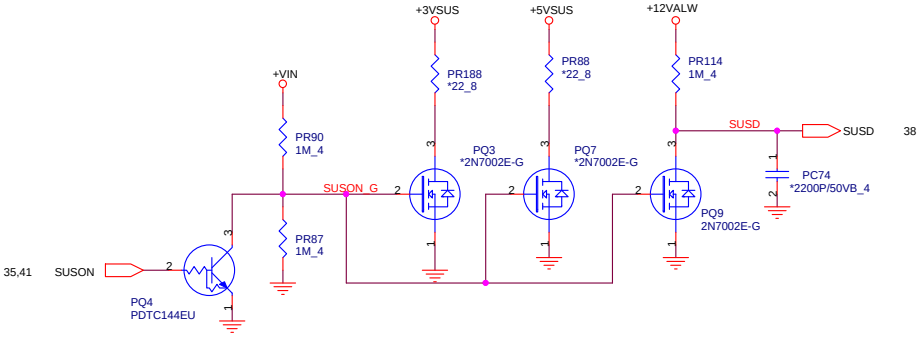


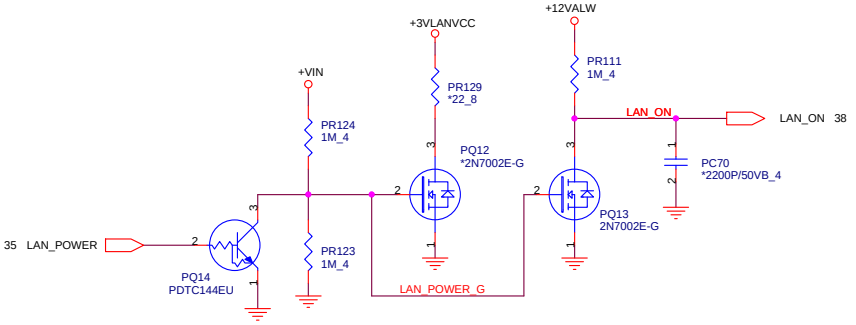
PROJECT : QT8	
Quanta Computer Inc.	
Size: Custom	Document Number: VGA PWR OZ8118/1.2V_S5/+1.5
Rev: 1A	
Date: Tuesday, February 19, 2008	Sheet 42 of 45

N85/RD5

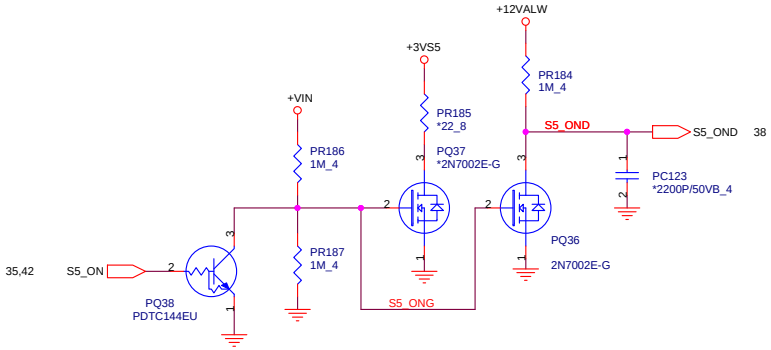


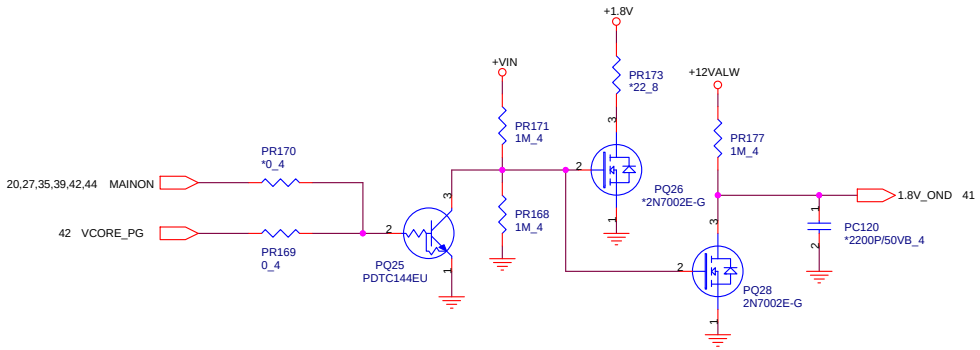






For Discrete Only





N85/RD5	PROJECT : QT8 Quanta Computer Inc.	
Size: Custom	Document Number: DISCHARGE	Rev: 1A
Date: Tuesday, February 19, 2008	Sheet 43 of 45	

TOP DC_JACK
65W/90W

ISL6251A

SI-2 modified -- EMI

Close to AC soft start MOSFET

ONLY for 3S battery pack

Setting the Vin min to 11.42V For ACSET 1.26V

Setting the Vin min to 15.88V For EN = 1.06V

VADJ = VERF >> 4.2V +5% Float >> 4.2V GND >> 4.2 -5%

V ACLIM = VREF * (Rhi // 152K) / (Rhi // 152K + Rlow// 152K) Input curretn = 2.9A (71.5K , 10K) (0.05/Vref * Vaclim + 0.05) / Rsense

Charging Curret setting = I chg = 165mV / Rsense * (Vchlim / 3.3V)

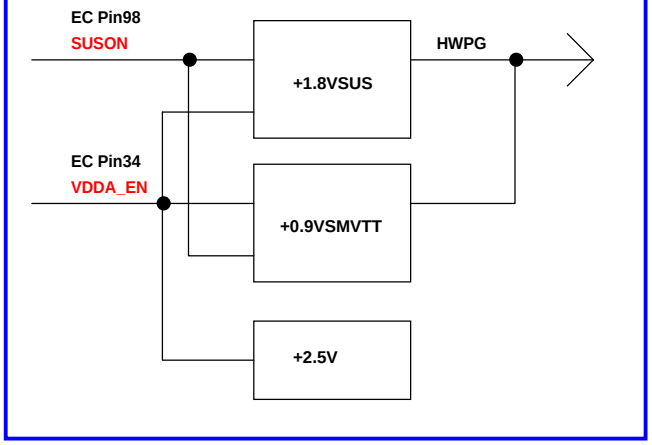
Input Current monitor V icm = 19.9 * (Vcsip - Vcsin)

ADP TYPE	PR72 Value	P/N
65W	102K/F	CS41022FB19
90W	7.5K/F	CS27502FB11

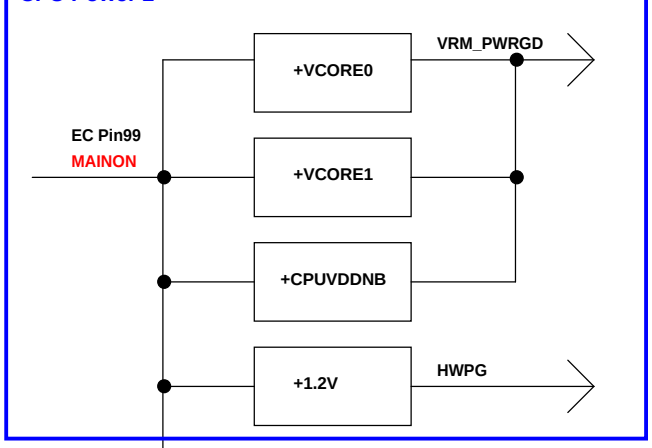
PROJECT : QT8
Quanta Computer Inc.

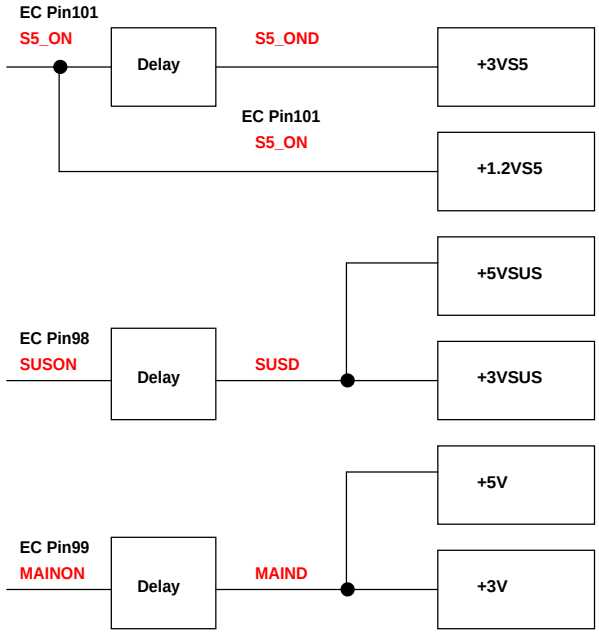
Size: Custom | Document Number: CHARGER (ISL6251) | Rev: 1A
Date: Tuesday, February 19, 2008 | Sheet 44 of 45
NB5/RD5

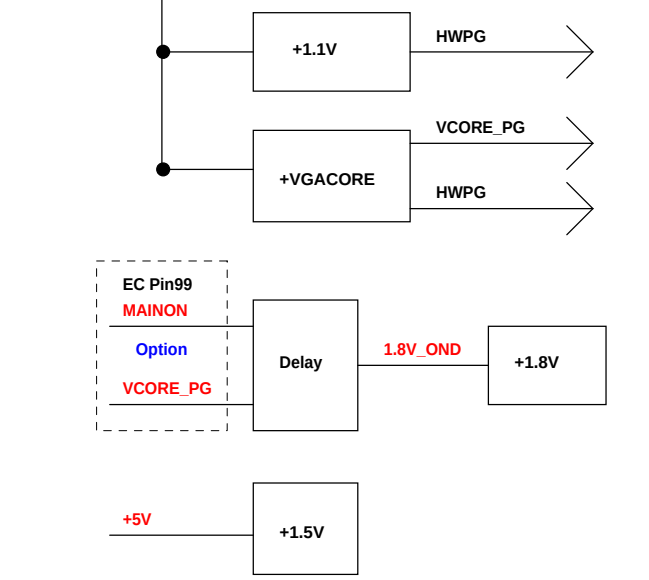
CPU Power 1



CPU Power 2







1 S5_ON, S5_OND, RSMRST# → 2 SUSON, SUSD → 3 MAINON, MAIND → 4 HWPG, VCORE_PG, VRM_PWRGD → EC Pin76 ECPWROK, Delay 600ms → SB_PWRGD_IN, 3.3V → NB_PWRGD_IN, 1.8V

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power control	1A

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