Jones/Cujo BLOCK DIAGRAM

01

PCB STACK UP

8L Dis.

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN2
- LAYER 4 : SGND1
- LAYER 5 : SVCC
- LAYER 6 : IN2
- LAYER 7 : SGND2
- LAYER 8 : BOT

Cable Docking PAGE 36
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 37
- SYSTEM POWER ISL6237IRZ-T PAGE 38
- DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 42
- VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 39
- VGACORE(1.025V)Oz8119 PAGE 41
- CPU CORE ISL6262A PAGE 40

CPU Penryn 478P (uPGA)/35W PAGE 3,4

CPU THERMAL SENSOR PAGE 4

FSB 667/800/1066

14.318MHz

CLOCK GEN ALPRS355B MLF64PIN PAGE 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

NORTH BRIDGE Cantiga PM45,GM45 PAGE 5~9

Level Shift PAGE 20

27MHz

DDRII-SODIMM1 PAGE 10 — DDRII 667/800 MHz

DDRII-SODIMM2 PAGE 10 — DDRII 667/800 MHz

PCI-Express 16X

nVIDIA NB9M-GE 64 Bit NB9P-GS 128 Bit PAGE 12~18 969p

Dual Link

HDMI CON PAGE 20

CRT PAGE 20

LCD CONN PAGE 19

Mini PCI-E Card x2 Express Card x1 Cable Docking x1

4,7,10,11

DMI LINK

32.768KHz

NBSRCCLK, NBSRCCLK#

SOUTH BRIDGE ICH9-M PAGE 21,22,23,24

- **SATA - HDD** PAGE 32 — SATA0 150MB
- **SATA - CD-ROM** PAGE 32 — SATA1 150MB
- **SATA - 2ndHDD** PAGE 32 — SATA4 150MB
- **E-SATA** PAGE 29 — SATA5 150MB
- Accelerometer LIS3LV02DL PAGE 27 — SMBUS

USB2.0

0,1,8,9

- **USB2.0 Ports X4** PAGE 29
- **BlueTooth** PAGE 29 — 5
- **Webcam** PAGE 29 — 3
- **Fingerprint** PAGE 29 — 2

PCI-E

24.576Hz

Azalia

- **Mini PCI-E Card** (Wireless LAN/TV) PAGE 35 — X2
- **LAN** Realtek PCIE-LAN RTL8102E/8111C (10/100/GagaLAN) PAGE 30,31 — X1
- **Express Card** (NEW CARD) PAGE 32 — X1
- **JMICRO 380 for Discrete** PAGE25 — X1

25MHz

- **IEEE1394** connect for Discrete only PAGE 25
- **Memory CardReader** PAGE 25
- **RJ45** PAGE 30

Analog IDT92HD75B3 PAGE 26

- **AUDIO Amplifier TPA6047** PAGE 27
- **AUDIO Amplifier TPA3007D1** PAGE 28
- Jack to Speaker PAGE 27
- Jack to Sub-Woofer PAGE 28
- microphone PAGE 28
- Audio Jacks (Phone/ MIC) PAGE 28

MDC CONN PAGE 33

LPC

32.768KHz

ENE KBC KB3926 C0 PAGE 34

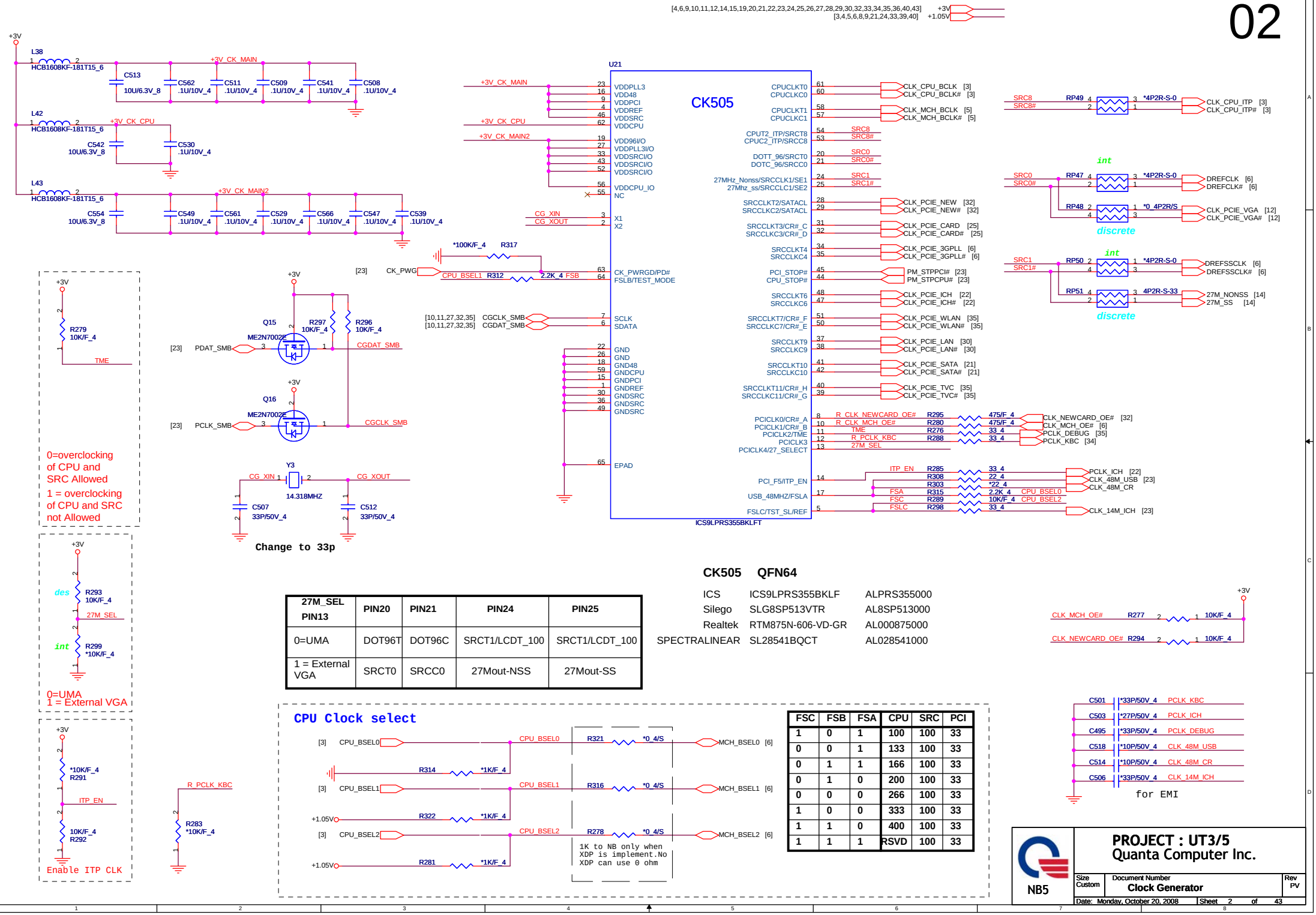
- Keyboard Touch Pad PAGE 33 PAGE 34
- Capacitive Sense SW PAGE 33
- SPI PAGE 22
- SPI PAGE 34
- GMT G9931P1U FAN PAGE 36

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	PV

Date: Monday, October 20, 2008 Sheet 1 of 43



27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

CK505 QFN64

ICS	ICS9LPRS355BKLF	ALPRS355000
Silego	SLG8SP513VTR	AL8SP513000
Realtek	RTM875N-606-VD-GR	AL000875000
SPECTRALINEAR	SL28541BQCT	AL028541000

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PROJECT : UT3/5
Quanta Computer Inc.
NB5
Size: Custom | Document Number: Clock Generator | Rev: PV
Date: Monday, October 20, 2008 | Sheet 2 of 43

DGT^8000021

U34A

ADDR GROUP_0

ADDR GROUP_1

XDP/ITP SIGNALS

CONTROL

THERMAL

MISC

H CLK

Quard Core Only

Penryn Ball-out Rev 1a

U34B

DATA GRP 0

DATA GRP 1

DATA GRP 2

DATA GRP 3

Penryn Ball-out Rev 1a

For QC CPU

DB modified

Add R61

R542 -->1.74K for Quad Core

	Rc
Dual Core	2K Ohm
Quard Core	1.74K Ohm

MODEL	UT5 Quad Core	UT3 Dual Core
R28	*0_4	0_4

	COMP0/2	COMP1/3
Dual Core	27.4 Ohm (CS02742FB19)	54.9 Ohm (CS05492FB19)
Quard Core	24.9 Ohm (CS02492FB29)	49.9 Ohm (CS04992FB31)

For QC Support

Don't install for DC

Change to +5V

Q10 *ME2N7002E

Q11 *MMBT3904-7-F

Populate ITP700Flex for bringup

JITP1

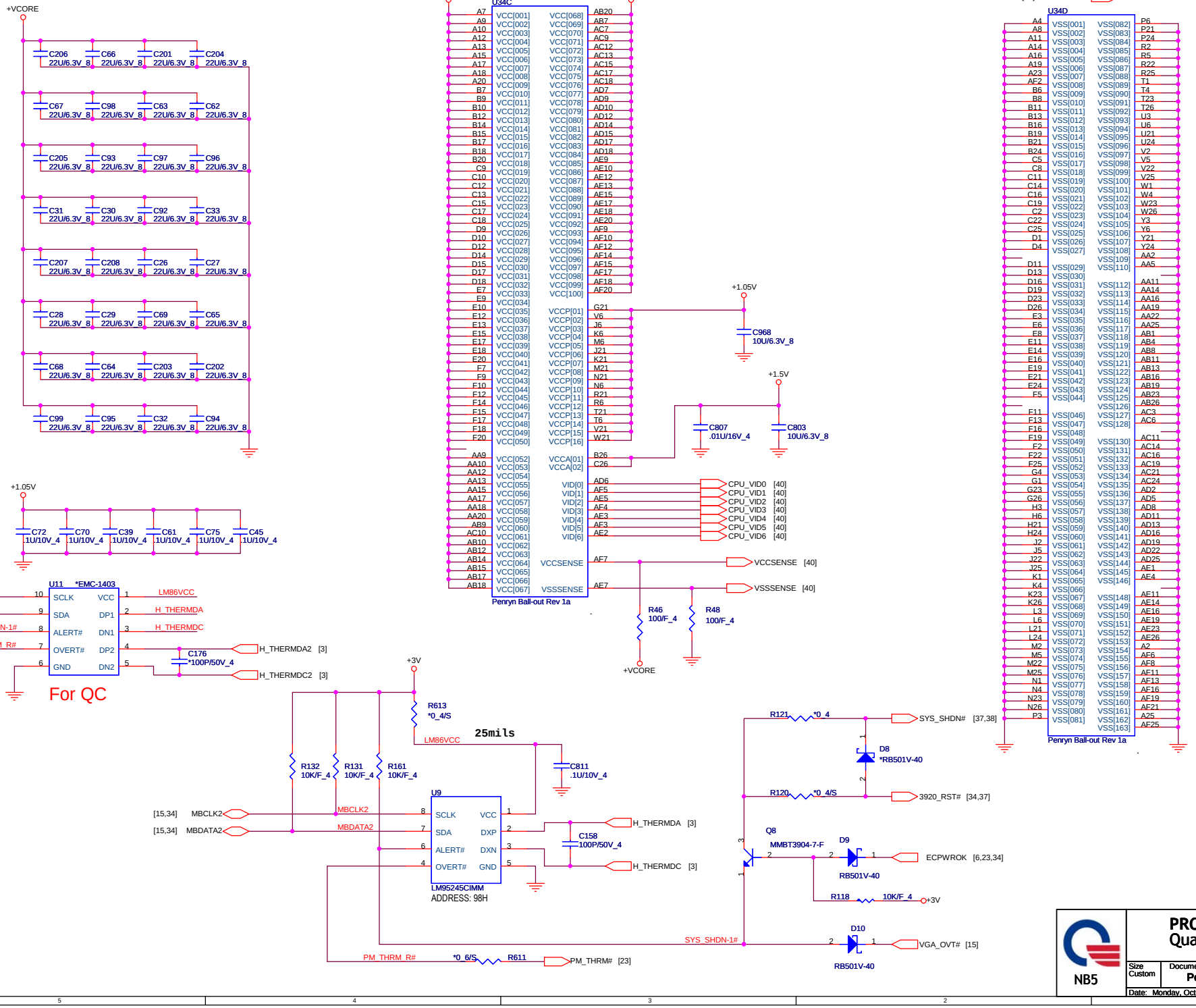
*ITP700Flex

PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size: Custom | Document Number: Penryn 1/2 | Rev: PV

Date: Monday, October 20, 2008 | Sheet 3 of 43

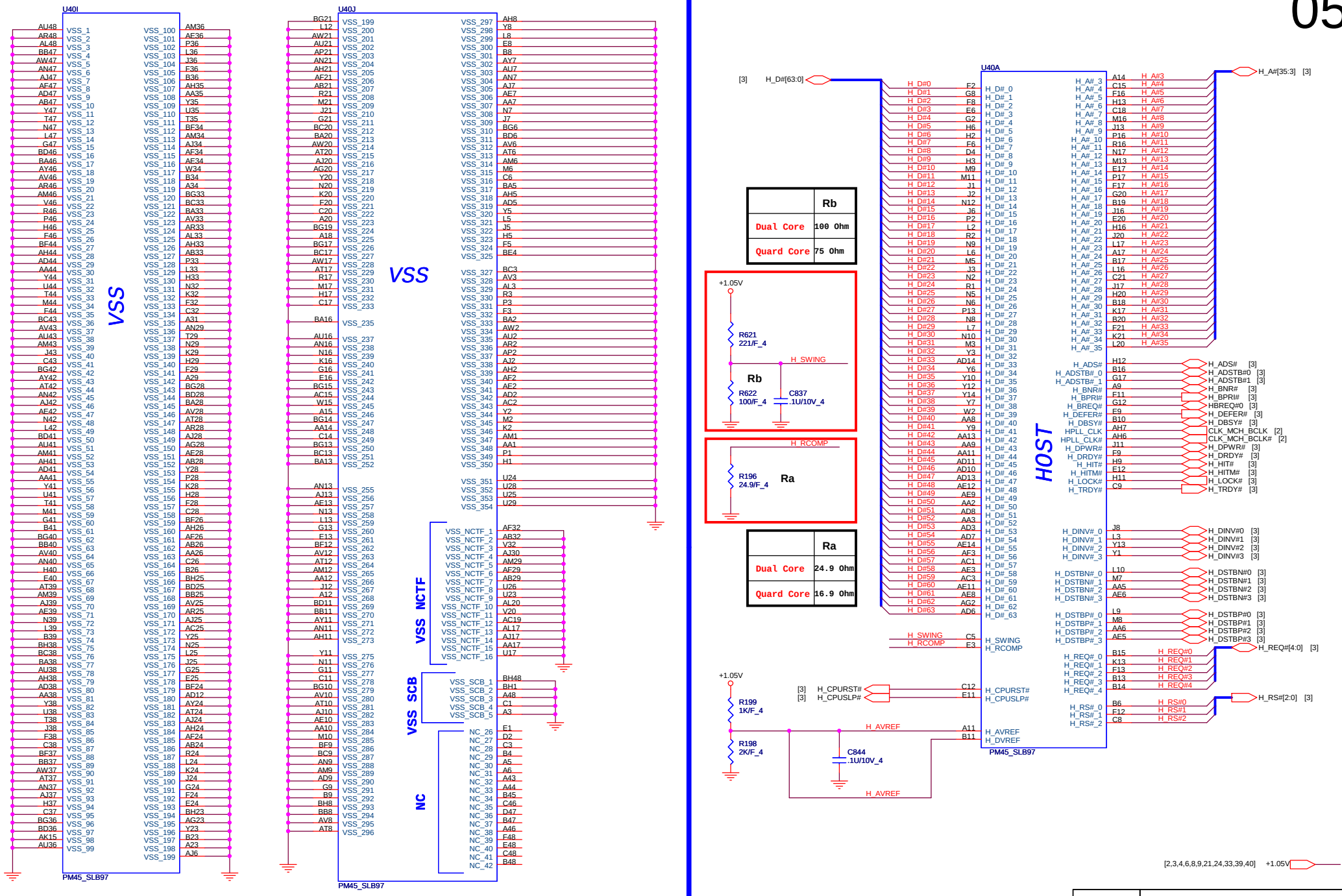


PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Penryn & TH Monitor 2/2	PV

Date: Monday, October 20, 2008 Sheet 4 of 43



PROJECT :	UT3/5
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Cantiga Host & VSS 1/5
Rev: PV	
Date: Monday, October 20, 2008	Sheet 5 of 43

MCH_CFG_5 DMIx2 selection
Low = DMI X2
High = DMI X4 (Default)

MCH_CFG_16 FSB Dynamic ODT
Low = Dynamic ODT disabled
High = Dynamic ODT enabled (default)

MCH_CFG_9 PCI Express Graphic Lane
Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal
Low = Normal operation (Default)
High = Reverse Lanes

MCH_CFG_6 iTPM Host Interface
Low =The iTPM Host Interface is enabled2
High = The iTPM Host Interface is disabled (default)

MCH_CFG_7 Intel (R) Management Engine Crypto
Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable
Low = Enabled3
High: Disabled (Default)

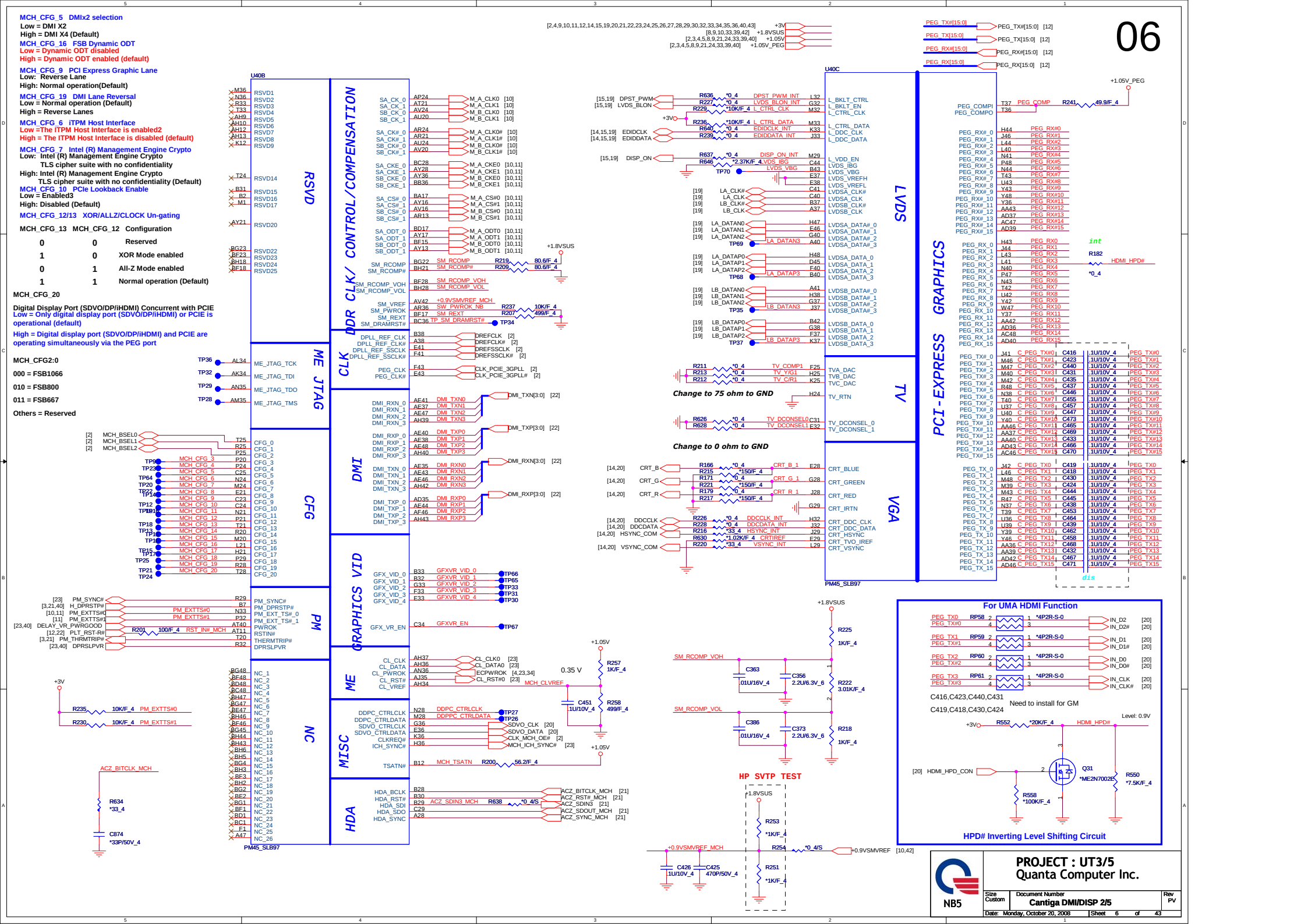
MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

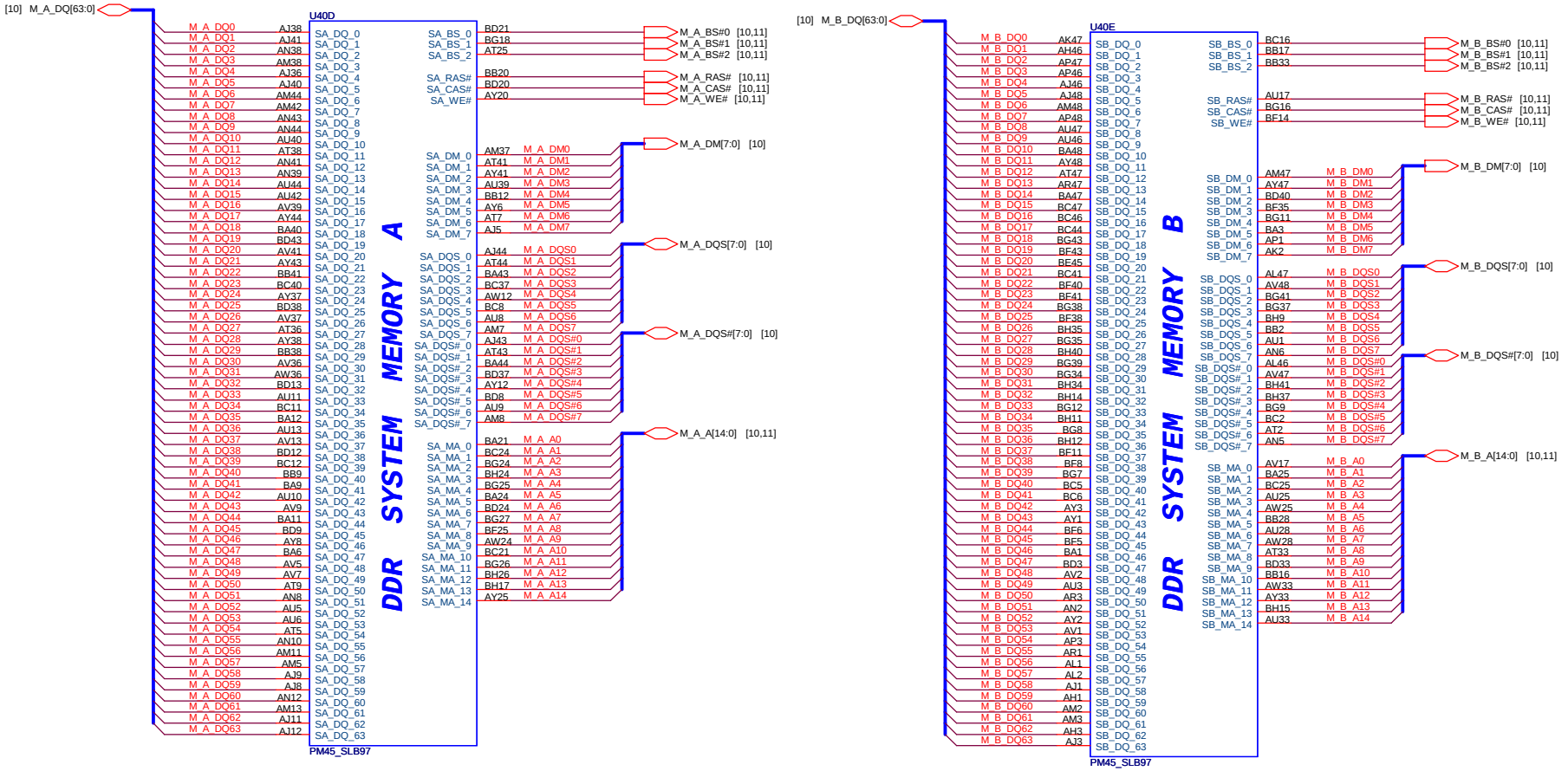
MCH_CFG_20

Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE
Low = Only digital display port (SDVO/DP/iHDMI) or PCIE is operational (default)
High = Digital display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via the PEG port

MCH_CFG2:0
000 = FSB1066
010 = FSB800
011 = FSB667
Others = Reserved



PROJECT :	UT3/5
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Cantiga DMI/DISP 2/5
Rev: PV	
Date: Monday, October 20, 2008	Sheet 6 of 43



NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga DDR2 3/5	PV

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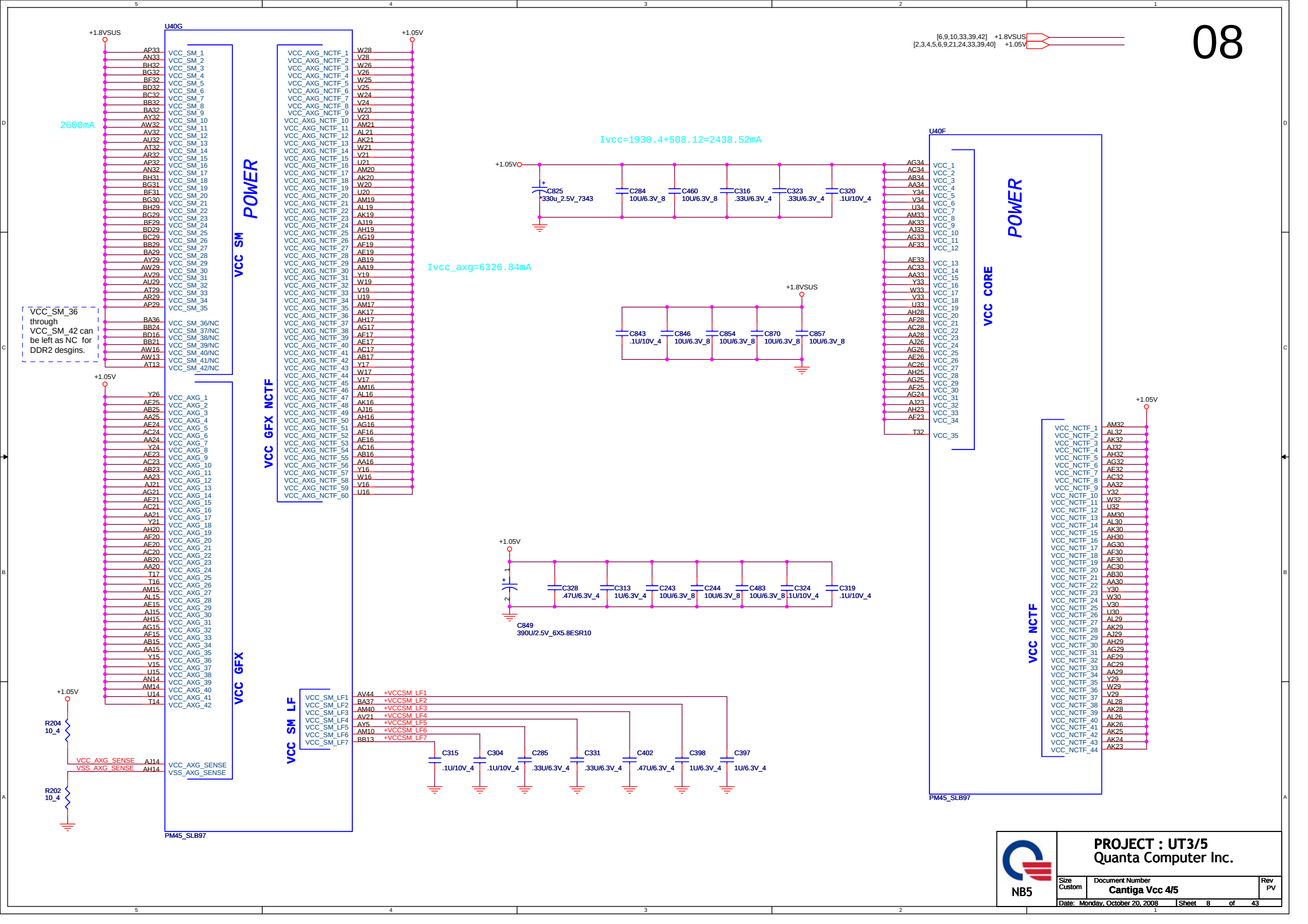


PROJECT :	UT3/5
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Cantiga Vcc 4/5
Rev: PV	
Date: Monday, October 20, 2008	Sheet 8 of 43

+1.05V [2,3,4,5,6,8,21,24,33,39,40]
+3V [2,4,6,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43]
+1.5V [4,21,22,24,26,32,33,35,39,43]
+1.8VSUS [6,8,10,33,39,42]
+1.05V_PEG [2,3,4,5,6,8,21,24,33,39,40]

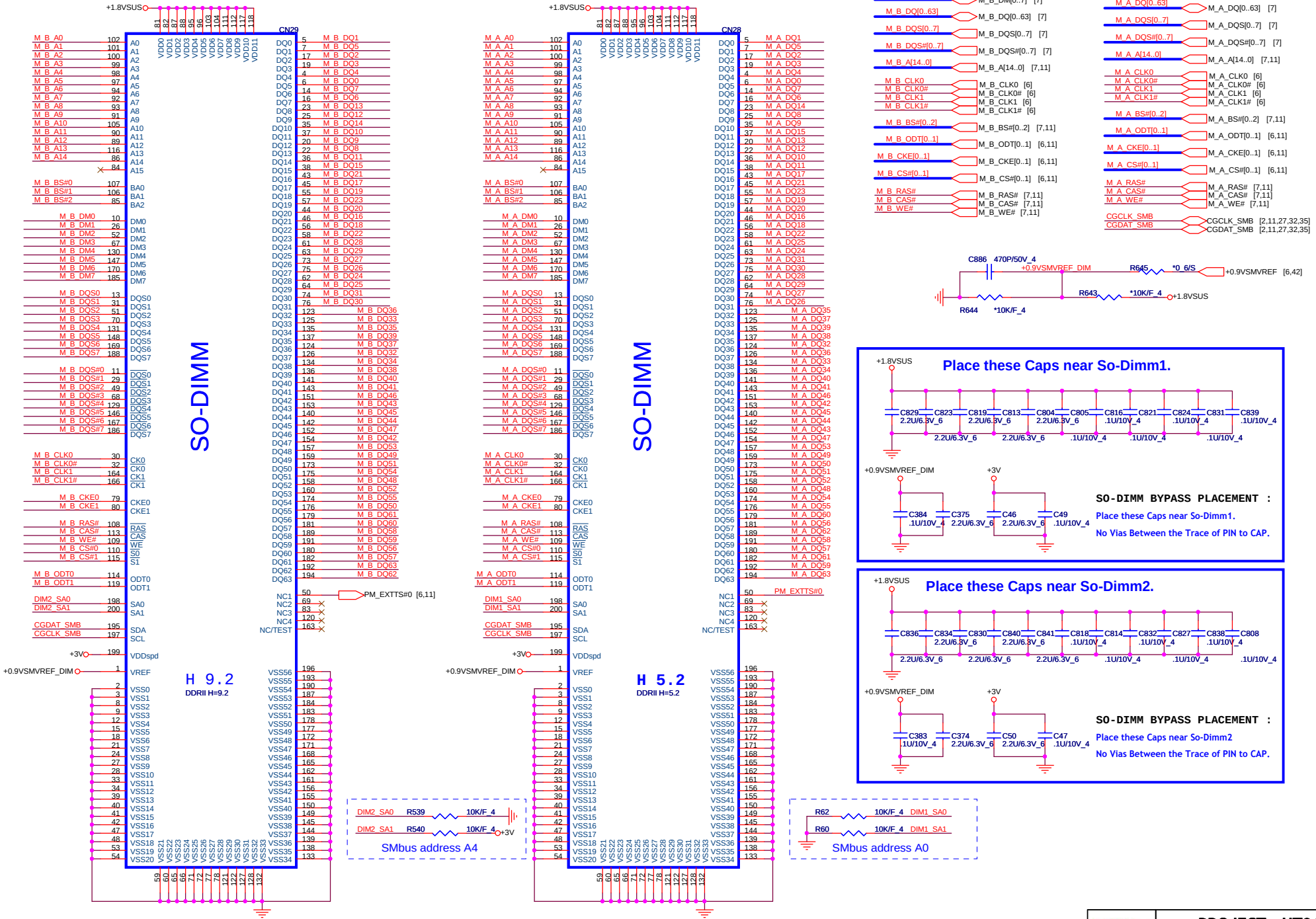
Change to CX000181016(180 ohm,1.5A) as current request
(L21,L22)

Intel Design Guide 1.5
thermal management is enabled on discrete graphics motherboard

Modify to U40#AF1 power to +1.05V_MPLL as CRB change

POWER

PROJECT : UT3/5
Quanta Computer Inc.
NB5
Size Custom | Document Number Cantiga Power 5/5 | Rev PV
Date: Monday, October 20, 2008 | Sheet 9 of 43



PROJECT : UT3/5
Quanta Computer Inc.

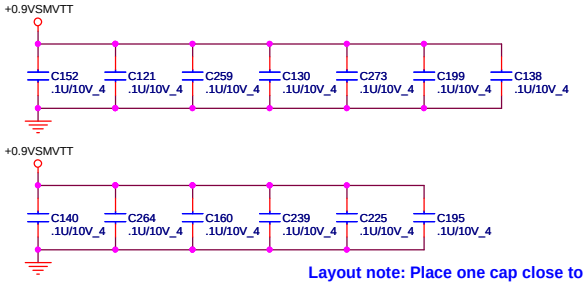
Size	Document Number	Rev
Custom	DDR2 DIMM	PV

NB5

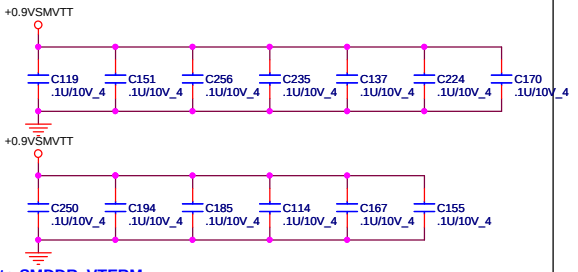
Date: Monday, October 20, 2008 Sheet 10 of 43

DDRII DUAL CHANNEL A,B.

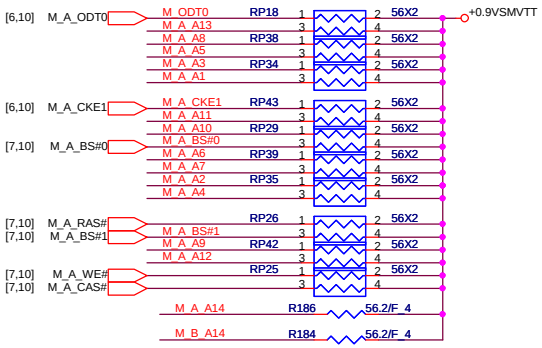
DDRII A CHANNEL

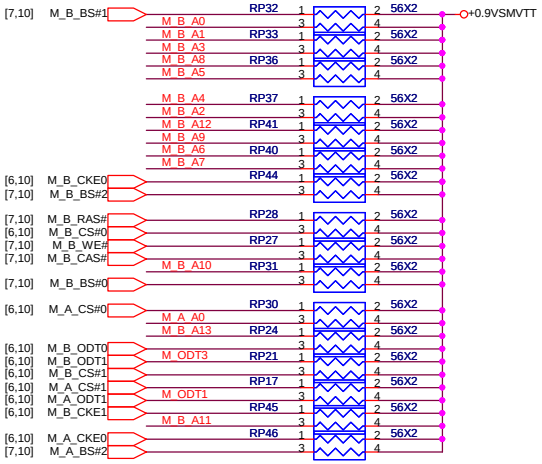


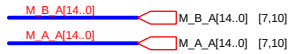
DDRII B CHANNEL

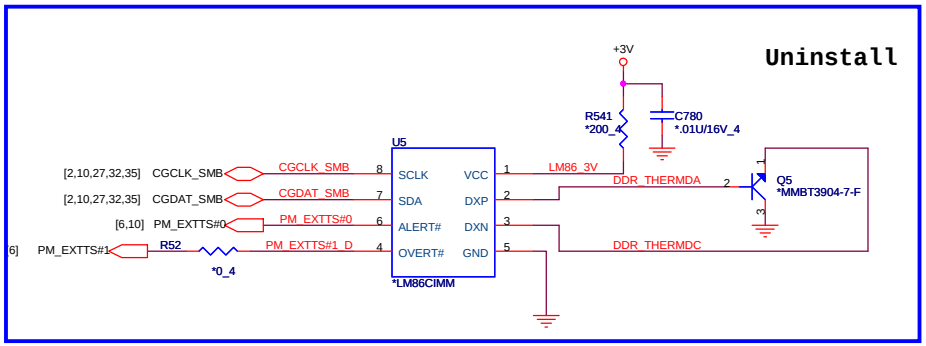


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM









+0.9VSMVTT [42]

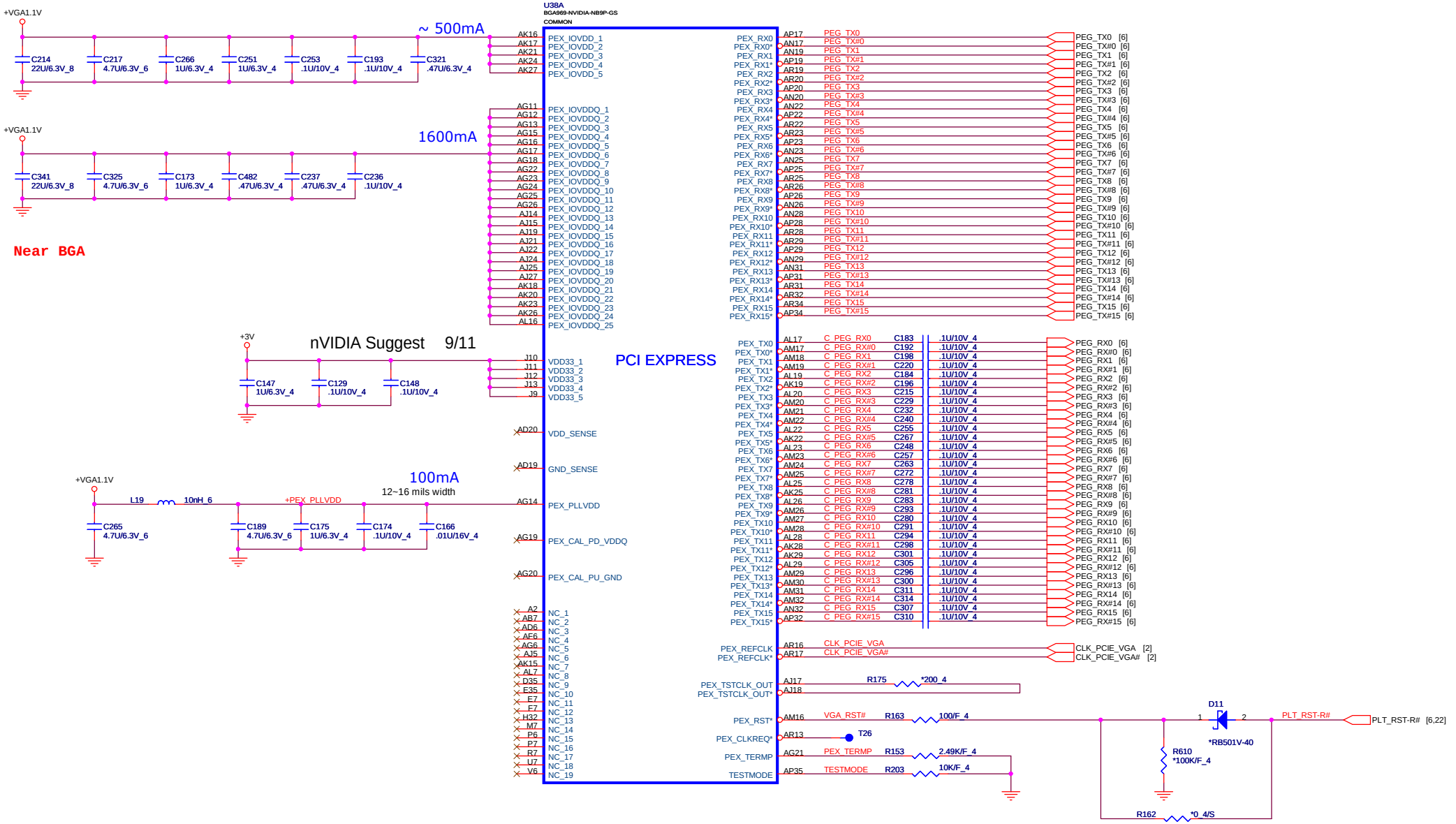
+3V [2,4,6,9,10,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43]

PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	DDR2 termination	PV

Date: Monday, October 20, 2008 Sheet 11 of 43



PROJECT : UT3/5	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: NV9X (PCIE I/F) 1/5
Rev: PV	
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U38B
BGA969-NVIDIA-NB9P-GS
COMMON

MEMORY I/F A

DB modified

U38C
BGA969-NVIDIA-NB9P-GS
COMMON

MEMORY I/F B

DB modified

for DDR2 need use CMD11(CKE) and CMD12(ODT)

use internal Vref, ext divider no stuff

15mils width

For Debug only

G96 only

R178 no stuff

R192 Install for DDR3

For G96 only
For NB9P-GS only

U38D

BGA969-NVIDIA-N89P-GS
COMMON

IFPAB(LVDS)

+1.8V
L58 HCB1608KF-181T15_6
C801 4.7U/6.3V_6 C806 4700P/25V_4 C144 470P/50V_4
+IFPAB_PLLVDD
100 mA
IFPAB_PLLVDD AK9
R106 *1K/F_4
IFPAB_RSET AJ11
50 mA
IFPA_IOVDD AG9
50 mA
IFPB_IOVDD AG10
L9 HCB1608KF-181T15_6
C76 4.7U/6.3V_6 C74 4.7U/6.3V_6 C83 4700P/25V_4 C157 4700P/25V_4 C78 470P/50V_4 C141 470P/50V_4
+IFPAB_IOVDD

IFPA_TXC	AM11	EXT_TXLCLKOUT+	[19]
IFPA_TXC*	AM12	EXT_TXLCLKOUT-	[19]
IFPA_TXD0	AM8	EXT_TXLOUT0+	[19]
IFPA_TXD0*	AL8	EXT_TXLOUT0-	[19]
IFPA_TXD1	AM10	EXT_TXLOUT1+	[19]
IFPA_TXD1*	AM9	EXT_TXLOUT1-	[19]
IFPA_TXD2	AK10	EXT_TXLOUT2+	[19]
IFPA_TXD2*	AL10	EXT_TXLOUT2-	[19]
IFPA_TXD3	AK11		
IFPA_TXD3*	AL11		
IFPB_TXC	AP13	EXT_TXUCLKOUT+	[19]
IFPB_TXC*	AN13	EXT_TXUCLKOUT-	[19]
IFPB_TXD4	AN8	EXT_TXUOUT0+	[19]
IFPB_TXD4*	AP8	EXT_TXUOUT0-	[19]
IFPB_TXD5	AP10	EXT_TXUOUT1+	[19]
IFPB_TXD5*	AN10	EXT_TXUOUT1-	[19]
IFPB_TXD6	AN11	EXT_TXUOUT2+	[19]
IFPB_TXD6*	AP10	EXT_TXUOUT2-	[19]
IFPB_TXD7	AN11		
IFPB_TXD7*	AP11		

IFPCD

+1.8V
L13 HCB1608KF-181T15_6
C231 1U/6.3V_4 0827b C116 4.7U/6.3V_6 C135 4700P/25V_4 C123 470P/50V_4
+IFPCD_PLLVDD
IFPCD_PLLVDD AJ9
R736 1K/F_4
IFPCD_RSET AK7
IFPC_IOVDD AJ8
+VGA1.1V
L14 HCB1608KF-181T15_6
C794 4.7U/6.3V_6 C128 1U/6.3V_4 C795 1U/6.3V_4 C127 4700P/25V_4 C136 470P/50V_4 C124 470P/50V_4
+IFPCD_IOVDD
IFPD_IOVDD AK8

IFPC

AUX-	AP2			
AUX	AR2	N_TXC_HDMI-	N_TXC_HDMI-	[20]
DPL3_TXC	AP1	N_TXC_HDMI+	N_TXC_HDMI+	[20]
DPL2_TXD0	AM4	N_TX0_HDMI-	N_TX0_HDMI-	[20]
DPL2_TXD0	AM3	N_TX0_HDMI+	N_TX0_HDMI+	[20]
DPL1_TXD1	AM5	N_TX1_HDMI-	N_TX1_HDMI-	[20]
DPL1_TXD1	AL5	N_TX1_HDMI+	N_TX1_HDMI+	[20]
DPL0_TXD2	AM6	N_TX2_HDMI-	N_TX2_HDMI-	[20]
DPL0_TXD2	AM7	N_TX2_HDMI+	N_TX2_HDMI+	[20]
AUX	AN4			

Fix Ball out and Pin Name

IFPD

AUX	AP4
AUX	AR4
DPL3_TXC	AR5
DPL3_TXC	AP5
DPL2_TXD0	AN5
DPL2_TXD0	AN7
DPL1_TXD1	AP7
DPL1_TXD1	AR7
DPL0_TXD2	AR8
DPL0_TXD2	

TMDS channel two

IFPEF

IFPEF_PLLVDD AJ6
R140 10K/F_4 T23
IFPEF_RSET AL1
IFPE_IOVDD AE7
R85 10K/F_4
IFPF_IOVDD AD7

IFPE_AUX	AE4				
IFPE_AUX*	AD4				
IFPE_L0	AH6				
IFPE_L0*	AH5				
IFPE_L1	AH4				
IFPE_L1*	AG4				
IFPE_L2	AF4				
IFPE_L2*	AF5				
IFPE_L3	AF6				
IFPE_L3*	AF5				
IFPF_AUX	AF3				
IFPF_AUX*	AF2				
IFPF_L0	AL2				
IFPF_L0*	AL3				
IFPF_L1	AJ3				
IFPF_L1*	AJ2				
IFPF_L2	AJ1				
IFPF_L2*	AH1				
IFPF_L3	AH2				
IFPF_L3*	AH3				

Display port output

DACA(CRT)

+3V
L10 HCB1608KF-181T15_6
C105 4.7U/6.3V_6 0827b C154 4700P/25V_4 C108 470P/50V_4 C159 .1U/10V_4
+DACA_VDD
DACA_VDD AJ12
DACA_VREF AK12
DACA_RSET AK13
R602 124/F_4

DACA_RED	AM15	L_CRT_R	R176	*0_4/S	CRT_R	[6,20]
DACA_GREEN	AM14	L_CRT_G	R169	*0_4/S	CRT_G	[6,20]
DACA_BLUE	AL14	L_CRT_B	R164	*0_4/S	CRT_B	[6,20]
DACA_HSYNC	AM13	CRT_HSYNC	R156	33_4	HSYNC_COM	[6,20]
DACA_VSYNC	AL13	CRT_VSYNC	R160	33_4	VSYNC_COM	[6,20]
I2CA_SCL	G1	L_DDCCLK	R566	*0_4/S	DDCCLK	[6,20]
I2CA_SDA	G4	L_DDCDAT	R565	*0_4/S	DDCDATA	[6,20]

L_CRT_R R172 150/F_4
L_CRT_G R168 150/F_4
L_CRT_B R165 150/F_4
Close to GPU

DACC(CRT2)

+DACB_VDD
R79 10K/F_4
DACC_VDD AG7
T25 AK6
T24 AH7
DACC_VREF
DACC_RSET

DACC_RED	AK4			
DACC_GREEN	AL4			
DACC_BLUE	AJ4			
DACC_HSYNC	AM1			
DACC_VSYNC	AM2			
I2CB_SCL	G3	I2CB_SCL	R76	2.2K_4
I2CB_SDA	G2	I2CB_SDA	R77	2.2K_4

+3V

DACB(TV)

10K/F_4 R749 +DACC_VD
DACB_VDD AC6
T34 AC5
T35 AB6
DACB_VREF
DACB_RSET

DACB_RED	AA4
DACB_GREEN	AB4
DACB_BLUE	Y4
DACB_CSYNC	AB5

T1

XTAL_PLL

+VGA1.1V
L17 HCB1608KF-181T15_6
C156 1U/6.3V_4 C134 1U/6.3V_4 C143 1U/6.3V_4 C149 .1U/10V_4 C126 .1U/10V_4
+NV_PLLVDD
65mA
50mA
25mA
PLLVDD AE9
VID_PLLVDD AD9
SP_PLLVDD AF9

XTAL_SSIN	D2	XTAL_SSIN	R97	*0_4/S	27M_SS [2]
XTAL_OUTBUFF	D1	BXTALOUT			
XTALIN	B1	XTALIN			
XTALOUT	B2	XTALOUT	R88	*0_4/S	27M_NONSS [2]

Y1 *27MHZ
C85 *18P/50V_4 5*3 package C86 *18P/50V_4

PLACE CLOSE TO GPU

STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED

SPREAD SPECTRUM

SI Build

+3V R64 *10K/F_4
+3V R65 *10K/F_4
R80 *22_4 XTAL_SSIN
C73 *10P/50V_4
GFX27M_L
+3V_SSC
R117 *4.7_6 +3V

U8 *ICS91730AMLF-T

ICSS_PD	8	PD#	VDD 2
BXTALOUT	1	CLKIN	CLKOUT 4
			REFOUT 5 ICSS_RFO
EDIDCLK	7	SCL	GND 3
EDIDDATA	6	SDA	

[6,15,19] EDIDCLK
[6,15,19] EDIDDATA
R90 *10K/F_4
C91 *470P/50V_4
C87 *.1U/10V_4
C109 *4.7U/6.3V_6
C106 *4.7U/6.3V_6

I2C ADDRESS: 0xD4H

27M_SS
BXTALOUT
R107 *10K/F_4
R586 *10K/F_4
Install it when not connected to Spread spectrum device

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X (DISPLAY) 3/5	PV

Date: Monday, October 20, 2008 Sheet 14 of 43

U38E
BGA969-NVIDIA-NB9P-GS
COMMON

MIOA
MIOB
MISC1 (GPIOS,JTAG,THERM,I2C)
MISC2(ROM)

Delete C122,R145,R148,R127,R99

Delete R155,R556,R104,R105,C90 as Nvidia recommand

Delete T31

Add for VGA Power switch

HD Audio Level :3V

NB9P-GS (G96) Straps
NB9M-GE (G98) Straps
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

PCI_DEVID[4]/SUBVENDOR

SEE Datasheet for details on G9x Straps!

SI Build

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_277	TVMODE2]	TVMODE[1]	TVMODE[0]	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VGA THERMAIL CIRCUIT

I2C ADDRESS: 0x98H

THERMAL TRACE CONSTRAINTS
Use 10MIL Guard(GND) Trace around THERMDC and THERMDA

HDCP ROM

Waiting Confirm from Nvidia

Fill U36 to correct p/n as Top B/S P/N(AR0QT6VB002)

PV-2

Change R562 and R137 from 10k to 2.2k as Nvidia request

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

NB9X VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor	
0111 0110 0101 other	DDR2 32Mx16x8, 128bit, 512MB DDR2 32Mx16x8, 128bit, 512MB DDR2 32Mx16x8, 128bit, 512MB Reserved	Hynix Qimonda Samsung	HY5PS121621CFP-25 HYB18T512161B2F-25 K4N51163QE-ZC25
0000 0001	DDR2 64Mx16x4, 128bit, 512MB DDR2 64Mx16x4, 128bit, 512MB	Hynix Samsung	HY5PS1G1631CFR-25 K4N1G164QQ-HC25

PCI_DEVID: STRAP2 R554

NB9M-GE	0x06E	8	1000	PU	5K
NB9M-GS	0x06E	9	1001	PU	10K
NB9P-GE2	0x064	8	1000	PU	5K
NB9P-GS	0x064	9	1001	PU	10K

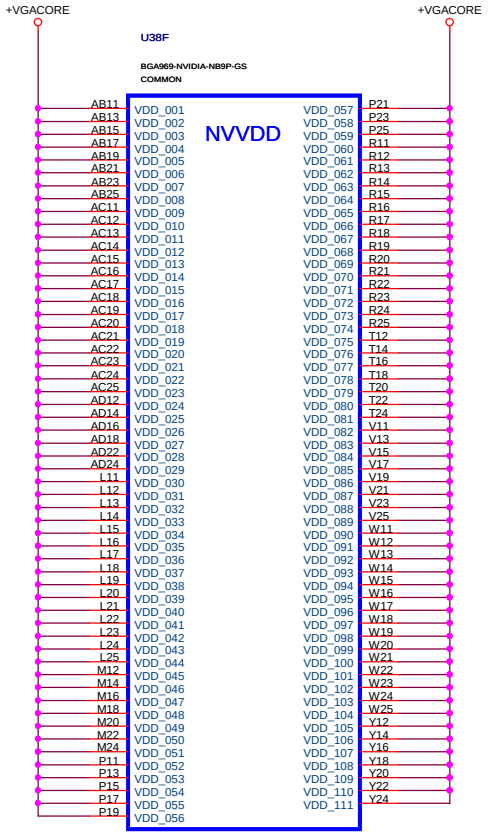
CS33012FB18 RES CHIP 30.1K 1/16W +-1%(0402)
CS33572FB13 RES CHIP 35.7K 1/16W +-1%(0402)
CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)

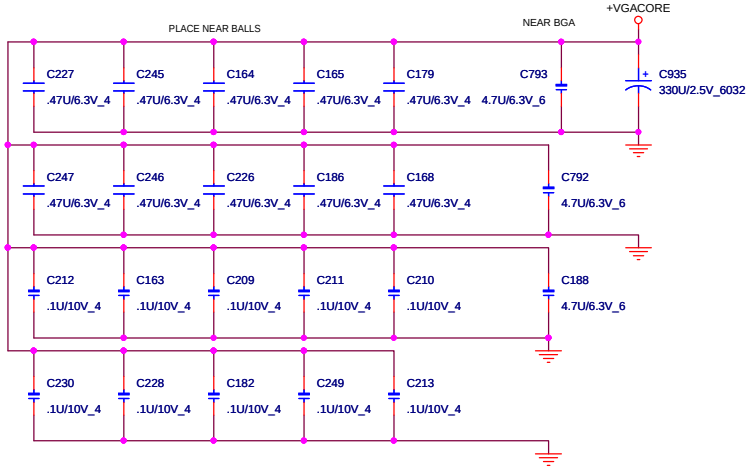
RAM ID: ROM_SI R585

32M*16	SAM	0101	PD	30.1K
	QIM	0110	PD	35.7K
	HYN	0111	PD	45.3K
64M*16	HYN	0000	PD	5K
	SAM	0001	PD	10K

PROJECT : UT3/5
Quanta Computer Inc.
NB5
Size C | Document Number NV9X (GPIO & STRRAPS) 4/5 | Rev PV
Date: Monday, October 20, 2008 | Sheet 15 of 43

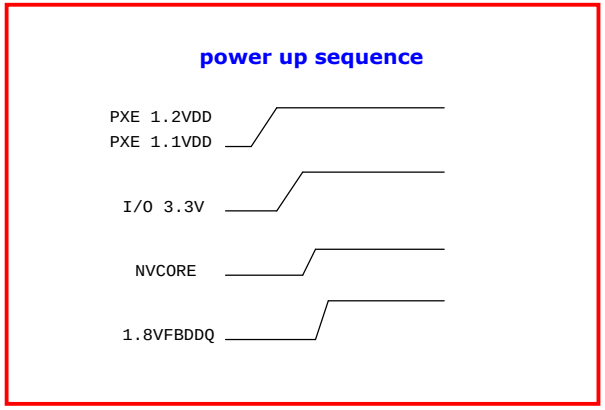
NVVDD Decoupling

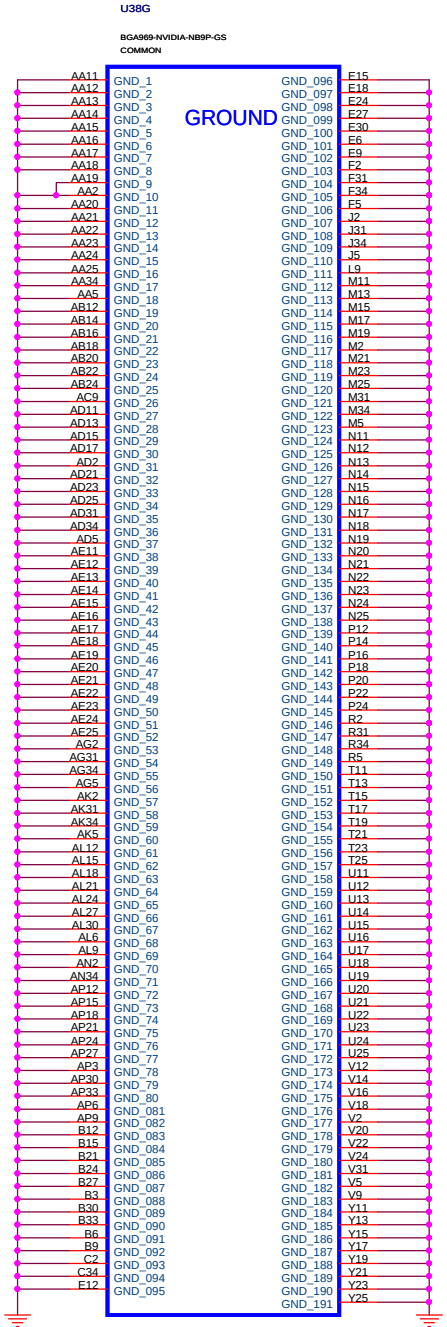




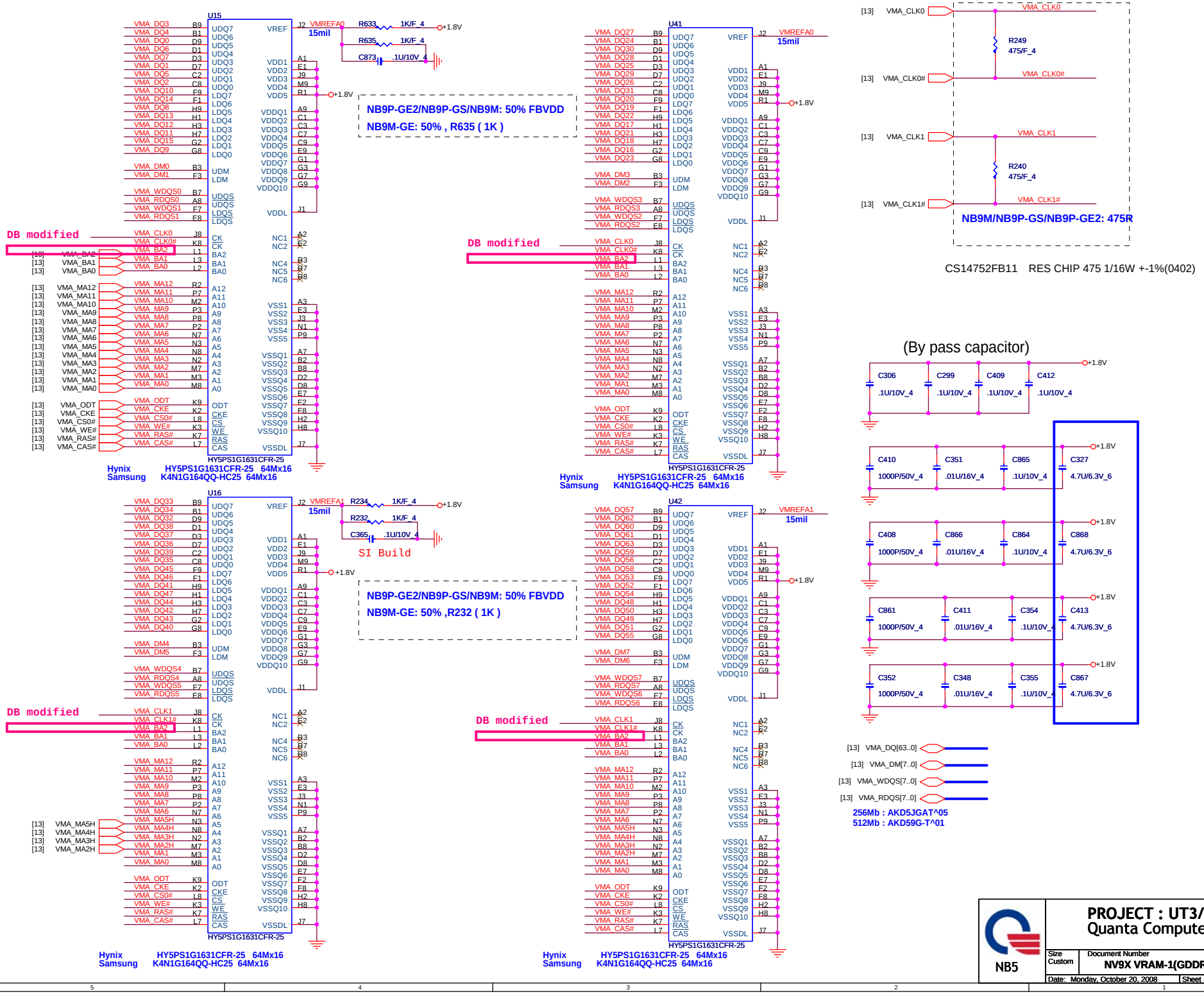
Follow Design Guide DG-03276-001 4.7uFx3 and 0.47x10 uF instead of 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V





PROJECT : UT3/5	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: NV9X (POWER & GND) 5/5; Rev: PV
	Date: Monday, October 20, 2008; Sheet 16 of 43

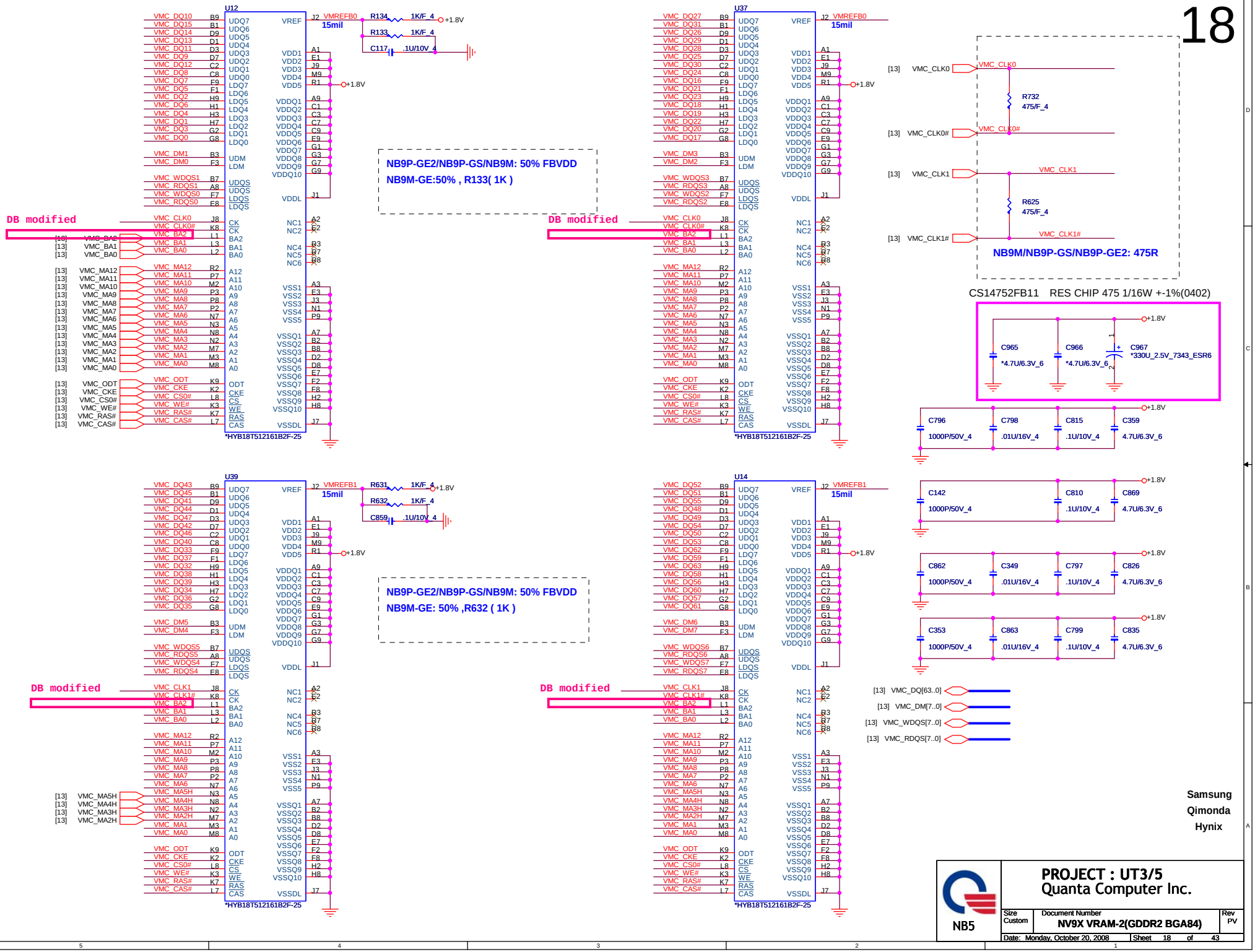


PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	NV9X VRAM-1(GDDR2 BGA84)	PV

Date: Monday, October 20, 2008 Sheet 17 of 43



PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X VRAM-2(GDDR2 BGA84)	PV

NB5

Date: Monday, October 20, 2008 Sheet 18 of 43

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB FOR UMA VGA

[6]	LA_CLK	RP9	*4P2R-S-0	TXLCLKOUT+		
[6]	LA_CLK#			TXLCLKOUT-		
[6]	LA_DATAP0	RP1	*4P2R-S-0	TXLOUT0+		
[6]	LA_DATAN0			TXLOUT0-		
[6]	LA_DATAP1	RP4	*4P2R-S-0	TXLOUT1+		
[6]	LA_DATAN1			TXLOUT1-		
[6]	LA_DATAP2	RP7	*4P2R-S-0	TXLOUT2+		
[6]	LA_DATAN2			TXLOUT2-		
[6]	LB_CLK#	RP20	*4P2R-S-0	TXUCLKOUT-		
[6]	LB_CLK			TXUCLKOUT+		
[6]	LB_DATAP0	RP11	*4P2R-S-0	TXUOUT0+		
[6]	LB_DATAN0			TXUOUT0-		
[6]	LB_DATAP1	RP15	*4P2R-S-0	TXUOUT1+		
[6]	LB_DATAN1			TXUOUT1-		
[6]	LB_DATAN2	RP23	*4P2R-S-0	TXUOUT2-		
[6]	LB_DATAP2			TXUOUT2+		

OPTION SIGNAL FROM Nvidia to VGA

[14]	EXT_TXLCLKOUT+	RP8	*0_4P2R/S	TXLCLKOUT+		
[14]	EXT_TXLCLKOUT-			TXLCLKOUT-		
[14]	EXT_TXLOUT0-	RP2	*0_4P2R/S	TXLOUT0-		
[14]	EXT_TXLOUT0+			TXLOUT0+		
[14]	EXT_TXLOUT1+	RP3	*0_4P2R/S	TXLOUT1+		
[14]	EXT_TXLOUT1-			TXLOUT1-		
[14]	EXT_TXLOUT2+	RP6	*0_4P2R/S	TXLOUT2+		
[14]	EXT_TXLOUT2-			TXLOUT2-		
[14]	EXT_TXUCLKOUT+	RP19	*0_4P2R/S	TXUCLKOUT+		
[14]	EXT_TXUCLKOUT-			TXUCLKOUT-		
[14]	EXT_TXUOUT0+	RP10	*0_4P2R/S	TXUOUT0+		
[14]	EXT_TXUOUT0-			TXUOUT0-		
[14]	EXT_TXUOUT1-	RP14	*0_4P2R/S	TXUOUT1-		
[14]	EXT_TXUOUT1+			TXUOUT1+		
[14]	EXT_TXUOUT2-	RP22	*0_4P2R/S	TXUOUT2-		
[14]	EXT_TXUOUT2+			TXUOUT2+		

+3V — R520 2.2K_4 EDIDCLK
R522 2.2K_4 EDIDDATA

+VIN_BLIGHT
+VIN — L53 FBM2125 HM330-T — +VIN_BLIGHT
C753 .1U/50V_6 | C751 .01U/50V_4 | C750 .1U/50V_6 | C6 *10U/25V_12

0090 use 100 ohm and must change back to 75ohm

+5V — R12 75R/F_6 — +LOGO_PWR1
C758 1000P/50V_4

[6,15] DPST_PWM — R526 *0_4
[34] PWM_VADJ — R524 *0_4/S — VADJ1
C754 *4.7U/6.3V_6 | C756 .1U/10V_4

[2,4,6,9,10,11,12,14,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +3V
[3,20,24,26,27,29,32,33,36,43] +5V
[28,36,37,38,39,40,41,42,43] +VIN
[21,29,33,34,36,37,38,43] +3VPCU
[29,33,38,43] +12VALW

+3VLCD_CON
+3V — C9 1000P/50V_4
[6,14,15] EDIDCLK
[6,14,15] EDIDDATA

CN1 GS12401-1011-9F
TXLOUT0- TXLOUT0+ TXLOUT1- TXLOUT1+ TXLOUT2- TXLOUT2+ TXLCLKOUT- TXLCLKOUT+ TXUOUT0- TXUOUT0+ TXUOUT1- TXUOUT1+ TXUOUT2- TXUOUT2+ TXUCLKOUT- TXUCLKOUT+ VADJ1 BLON_CON +VIN_BLIGHT +LOGO_PWR1

PV MODIFY

DISP_ON R525 100K/F_4
LVDS_BLON R7 100K/F_4

PN_BLON — D1 RB501V-40 — BLON_CON
R4 100K/F_4 | C8 22P/50V_4

+3VPCU — R8 33K_6
[6,15] LVDS_BLON — R6 1K/F_4 — D2 RB501V-40 — LID_EC# [33,34]
Close to EC

[23] LCD_BK — Q2 DTC144EUA

+5VSUS | 14.5v | +12VALW
R527 100K/F_4
R10 330K_6
AO3404 ID current 5.8A
Q1 AO3404
LCDONG
+3V — C12 .1U/10V_4
+3VLCD
L52 PBY201209T-4A/08
R516 22_8
LCDDISCHG
+3VLCD_CON
C757 .01U/16V_4 | C746 .1U/10V_4 | C748 10U/6.3V_8
Q26 ME2N7002E
C759 .022U/16V_4
LCDON#
Q27 ME2N7002E
Q25 DTC144EUA
[6,15] DISP_ON

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
B	LCD CONN/Lid function	PV

Date: Monday, October 20, 2008 Sheet 19 of 43

CRT PORT

Change Layout footprint to dsub-070546fr015sx68zr-15p-v

Change ESD protection to +5V

CRT CONN CN18

EMI

CRT SWITCH

U3 74CBT3257

inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

For UMA HDMI function

U35 *PI3VDP411LSZDE

POWER / CONTROL / GND

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCL/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

For EXT VGA

UMA : 0R
NB9M-GE/NB9P-GS: 0.1uF

Only for NVIDIA

HDMI PORT

DFHD19MR021

HDMI CONN

for EMI request

PROJECT :	UT3/5
	Quanta Computer Inc.
Size: C	Document Number: CRT/PS8101 HDMI Conn
Rev: PV	
Date: Monday, October 20, 2008	Sheet 20 of 43

NB5

[19,29,33,34,36,37,38,43] +3VPCU
[24] +3VRTC
[2,4,6,9,10,11,12,14,15,19,20,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +3V
[4,9,22,24,26,32,33,35,39,43] +1.5V
[2,3,4,5,6,8,9,24,33,39,40] +1.05V
[22,23,24,32,43] +3VS5

SI build
RB500V-40
D19
D20
RB500V-40
SI build
+3VPCU
+3VRTC
+3VRTC_2
C905 1U/6.3V_4
R375 20K/F_4
R378 180K_4
C599 1U/6.3V_4
C624 .1U/10V_4
G4 *SHORT_PAD1
G3 *SHORT_PAD1
C908 15P/50V_4
C909 15P/50V_4
Y7 32.768KHZ
R335 10M_4
R393 1K/F_4
R346 1M/F_4
20MIL
+3VRTC_BAT
For CR2032(Large)
BT1
BAT_CONN
update footprint (0830)
+3V
C569 .1U/10V_4
R409 10K/F_4
[29] SATA_LED#
U26
MC74VHC1G08DFT2G
ICH_SATA_LED#
+1.5V
R320 24.9/F_4
GLAN_COMP

U45A

RTCX1 C23
RTCX2 C24
RTC_X1
RTC_X2
RTC_RST# A25
SRTC_RST F20
SM_INTRUDER# C22
RTCRST#
SRTCRST#
INTRUDER#
RTC

ICH_INTVRMEN B22
LAN100_SLP A22
INTVRMEN
LAN100_SLP
LPC

TP38 GLAN_CLK E25
TP47 LAN_RSTSYNC C13
TP48 LAN_RXD0 F14
TP50 LAN_RXD1 G13
TP56 LAN_RXD2 D14
TP51 LAN_TXD0 D13
TP54 LAN_TXD1 D12
TP49 LAN_TXD2 E13
TP53 GPIO56 B10
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GPIO56
GLAN_COMPI B28
GLAN_COMPO B27
LAN / GLAN

ACZ_BCLK AE6
ACZ_SYNC AH4
ACZ_RST# AE7
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
[26] ACZ_SDIN0 AF4
[33] ACZ_SDIN1 AG4
[15] ACZ_SDIN2 AH3
[6] ACZ_SDIN3 AE5
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
ACZ_SDOUT AG5
HDA_SDOUT
TP87 AG7
[35] BT_COMBO_EN# AE8
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
ICH_SATA_LED# AG8
SATALED#
IHDA

SATA0RXN AJ16
SATA0RXP AH16
SATA0TXN AF17
SATA0TXP AG17
SATA1RXN AH13
SATA1RXP AJ13
SATA1TXN AG14
SATA1TXP AF14
SATA

ICH9BM_SLB8Q

FWH0/LAD0 K5
FWH1/LAD1 K4
FWH2/LAD2 L6
FWH3/LAD3 K2
FWH4/LFRAME# K3
LDRQ0# J3
LDRQ1#/GPIO23 J1
A20GATE N7
A20M# AJ27
DPRSTP# AJ25
DPSLP# AE23
FERR# AJ26
CPUPWRGD AD22
IGNNE# AF25
INIT# AE22
INTR AG25
RCIN# L3
NMI AF23
SMI# AF24
STPCLK# AH27
THRMTRIP# AG26
TP12 AG27
SATA4RXN AH11
SATA4RXP AJ11
SATA4TXN AG12
SATA4TXP AF12
SATA5RXN AH9
SATA5RXP AJ9
SATA5TXN AE10
SATA5TXP AF10
SATA_CLKN AH18
SATA_CLKP AJ18
SATARBIAS# AJ7
SATARBIAS AH7

LAD0 [34,35]
LAD1 [34,35]
LAD2 [34,35]
LAD3 [34,35]
LFRAME# [34,35]
ICH_DRQ#0
ICH_DRQ#1
TP60
TP80
R382 10K/F_4
GATEA20 [34]
H_A20M# [3]
R329 *56.2/F_4
R337 *56.2/F_4
R331 49.9/F_4
H_DPRSTP# [3,6,40]
H_DPSLP# [3]
R330 49.9/F_4
H_FERR# [3]
H_PWRGD [3]
H_IGNNE# [3]
H_INIT# [3]
H_INTR [3]
RCIN# [34]
R421 10K/F_4
H_NMI [3]
H_SMI# [3]
H_STPCLK# [3]
H_THERMTRIP_R
R326 49.9/F_4
R327 49.9/F_4
PM_THRMTRIP# [3,6]
ICH_TP12
TP71

Change R331,R327 to 49.9 ohm

For UT5 17" 2nd HDD only
SATA HDD2
DB modified

C940 *.01U/16V_4 SATA_RXN4 [32]
C937 *.01U/16V_4 SATA_RXP4 [32]
C939 *.01U/16V_4 SATA_TXN4 [32]
C938 *.01U/16V_4 SATA_TXP4 [32]
SATA_RXN4_C
SATA_RXP4_C
SATA_TXN4_C
SATA_TXP4_C

E-SATA CONNECT

C611 .01U/16V_4 SATA_RXN5 [29]
C606 .01U/16V_4 SATA_RXP5 [29]
C614 .01U/16V_4 SATA_TXN5 [29]
C623 .01U/16V_4 SATA_TXP5 [29]
SATA_RXN5_C
SATA_RXP5_C
SATA_TXN5_C
SATA_TXP5_C

CLK_PCIE_SATA# [2]
CLK_PCIE_SATA [2]
SATA_RBIAS_PN
R396 24.9/F_4

Notice: GPIO33 is also a strap pin. Don't pull it to high.

HP Request
BT_COMBO_EN#
R381 *1K/F_4

SATA HDD1

[32] SATA_RXN0 C583 .01U/16V_4 SATA_RXN0_C AJ16
[32] SATA_RXP0 C579 .01U/16V_4 SATA_RXP0_C AH16
[32] SATA_TXN0 C576 .01U/16V_4 SATA_TXN0_C AF17
[32] SATA_TXP0 C578 .01U/16V_4 SATA_TXP0_C AG17
[32] SATA_RXN1 C590 .01U/16V_4 SATA_RXN1_C AH13
[32] SATA_RXP1 C592 .01U/16V_4 SATA_RXP1_C AJ13
[32] SATA_TXN1 C588 .01U/16V_4 SATA_TXN1_C AG14
[32] SATA_TXP1 C584 .01U/16V_4 SATA_TXP1_C AF14

SATA ODD

For HD Audio
ACZ_RST# R388 33_4 ACZ_RST#_AUDIO [26]
ACZ_SDOUT R404 33_4 ACZ_SDOUT_AUDIO [26]
ACZ_SYNC R400 33_4 ACZ_SYNC_AUDIO [26]
ACZ_BCLK R390 33_4 BIT_CLK_AUDIO [26]
C622 *10P/50V_4
C632 *10P/50V_4
C633 *10P/50V_4

For MDC
ACZ_RST# R387 33_4 ACZ_RST#_MDC [33]
ACZ_SDOUT R394 33_4 ACZ_SDOUT_MDC [33]
ACZ_SYNC R406 33_4 ACZ_SYNC_MDC [33]
ACZ_BCLK R398 33_4 BIT_CLK_MDC [33]
C635 *10P/50V_4
C656 *10P/50V_4
C657 *10P/50V_4

For UMA
ACZ_RST# R389 *33_4 ACZ_RST#_MCH [6]
ACZ_SDOUT R376 *33_4 ACZ_SDOUT_MCH [6]
ACZ_SYNC R377 *33_4 ACZ_SYNC_MCH [6]
ACZ_BCLK R395 *33_4 ACZ_BITCLK_MCH [6]
C631 *10P/50V_4
C602 *10P/50V_4
C601 *10P/50V_4

Close to U45
For Discrete
ACZ_RST# R745 22_4 NV_HDA_RST
ACZ_SDOUT R747 22_4 NV_HDA_SDO
ACZ_SYNC R748 22_4 NV_HDA_SYNC
ACZ_BCLK R744 22_4 NV_HDA_BCLK
NV_HDA_RST [15]
NV_HDA_SDO [15]
NV_HDA_SYNC [15]
NV_HDA_BCLK [15]
C691 *10P/50V_4
C605 *10P/50V_4
C693 *10P/50V_4

SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

+3VRTC R677 332K/F_4 ICH_INTVRMEN R674 *0_4
+3VRTC R679 332K/F_4 LAN100_SLP R678 *0_4
+3V R399 *1K/F_4 ACZ_SDOUT ICH_TP3 [23] R681 *1K/F_4

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

*1K/F_4 R392 GNT0# [22]

A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

*1K/F_4 R391 GNT3# [22]

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

+3V R384 *1K/F_4 ACZ_SPKR [23,26,27]

TPM physical presence	
ICH_GPIO57	Low: Default

+3VS5 R704 *10K/F_4 ICH_GPIO57 [23] R706 100K/F_4

PROJECT : UT3/5
Quanta Computer Inc.
NB5
Size: Custom
Document Number: ICH9-M Host 1/4
Rev: PV
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SWAP PCIE PORT6 to PORT2 (Lan and New card swap) -->Rename the port name by function and port

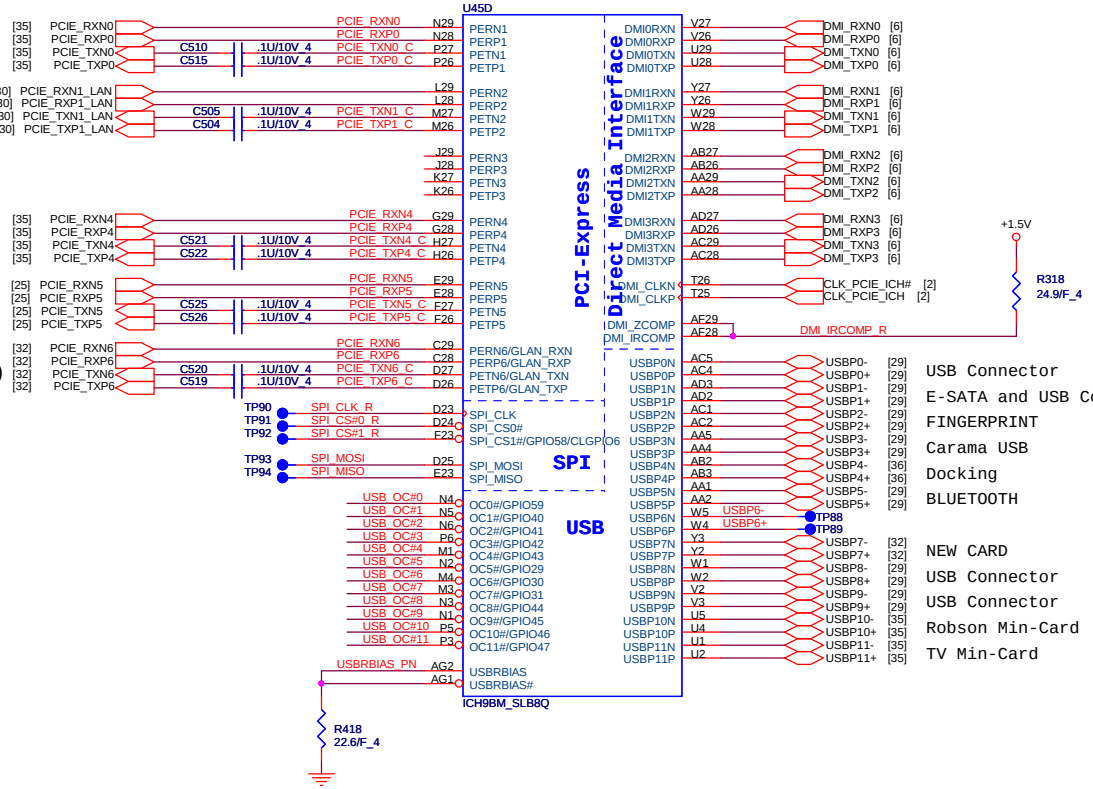
[4,9,21,24,26,32,33,35,39,43] +1.5V
[2,4,6,9,10,11,12,14,15,19,20,21,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +3V
[23,29,35,39,40,41,43] +3VSUS

MINI CARD PCI-E(WLAN)

PCIE-LAN

TV CARD PCI-E

EXPRESS CARD (NEW CARD)



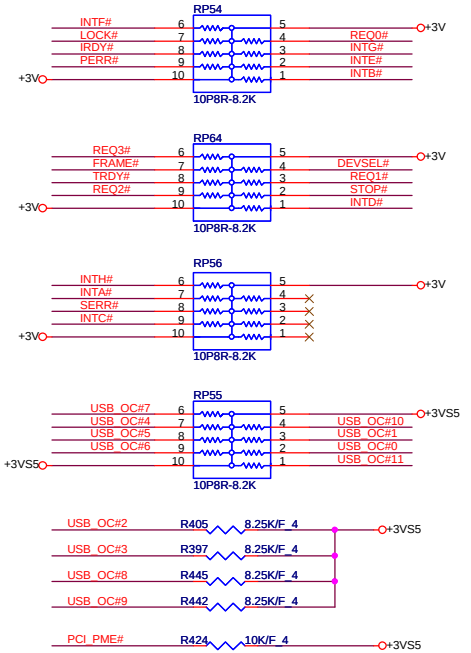
USB Connector
E-SATA and USB Connector
FINGERPRINT
Carama USB
Docking
BLUETOOTH

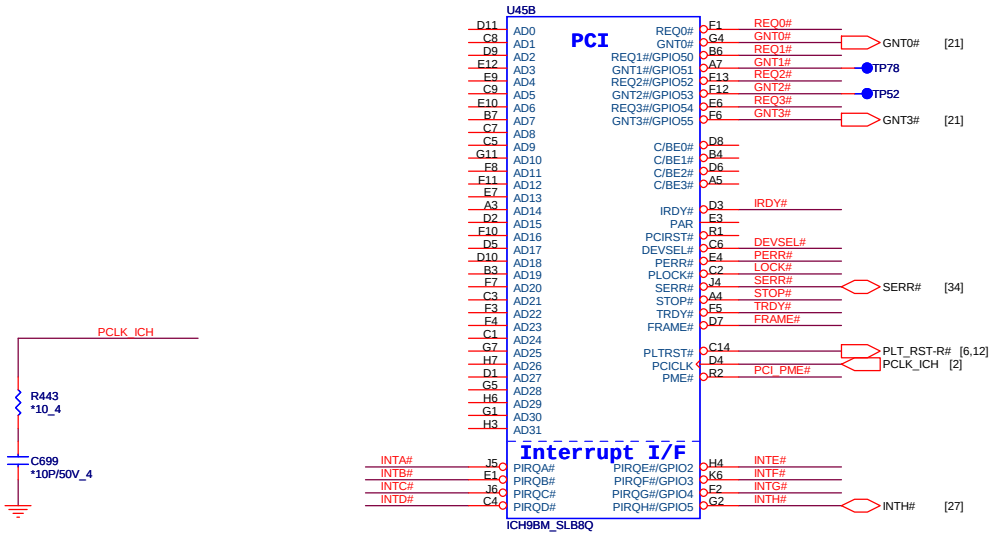
NEW CARD
USB Connector
USB Connector
Robson Min-Card
TV Min-Card

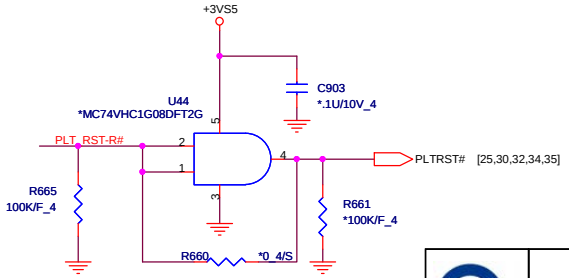
SI-2 Delete
Delete RP53,RP57 and tied from SB to CR(USB6)

des

int

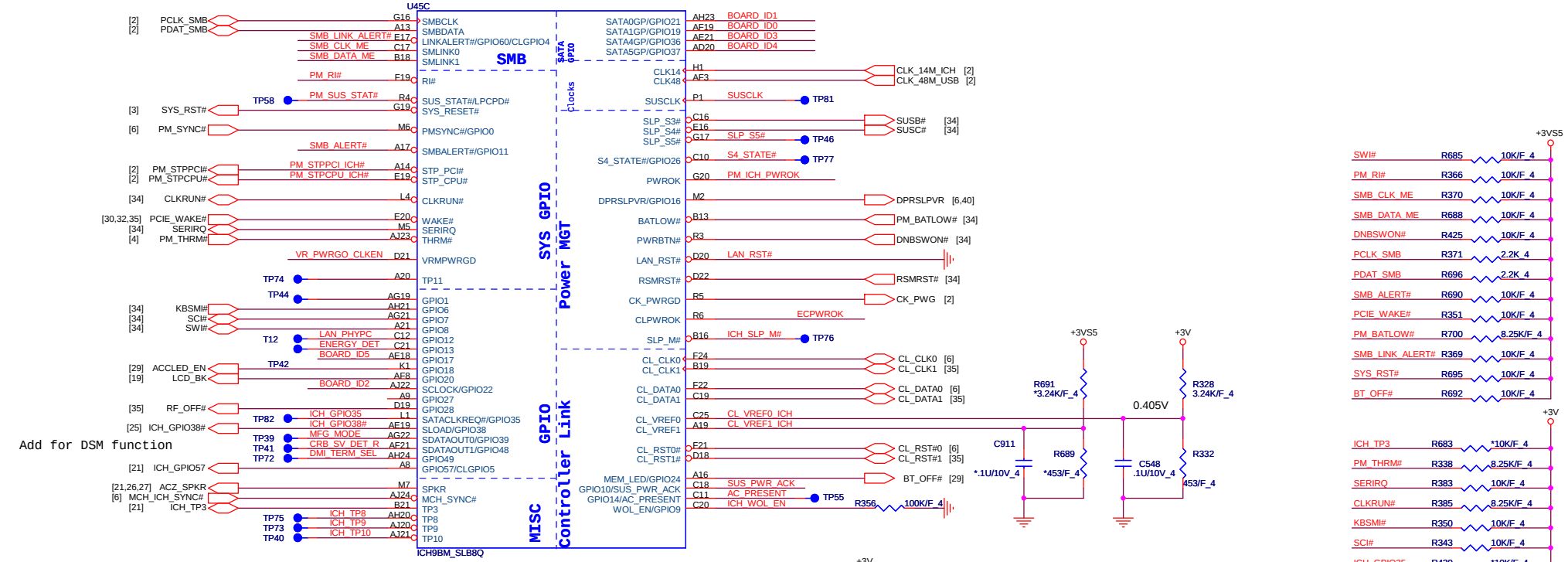






NB5	PROJECT : UT3/5 Quanta Computer Inc.
Size: Custom	Document Number: ICH9-M PCIE 2/4
Rev: PV	
Date: Monday, October 20, 2008	Sheet 22 of 43

[4,9,21,22,24,26,32,33,35,39,43] +1.5V
[2,4,6,9,10,11,12,14,15,19,20,21,22,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +3V
[21,22,24,32,43] +3VS5
[29,35,39,40,41,43] +3VSUS



Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UT3/Dis./9M	RD0 (0)	RU1 (1)	RD2 (0)	NC	NC	RD5 (0)
UT3/UMA	RD0 (0)	RD1 (0)	NC	NC	NC	NC
UT5/Dis./M92	RU0 (1)	RU1 (1)	RD2 (0)	NC	NC	RU5 (1)
UT5/Dis./M96	RU0 (1)	RU1 (1)	RU2 (1)	NC	NC	RD5 (0)
UT5/UMA	RU0 (1)	RD1 (0)	NC	NC	NC	NC
UT3D/Dis./M92	RD0 (0)	RU1 (1)	RD2 (0)	NC	NC	RU5 (1)
UT3D/Dis./M96	RD0 (0)	RU1 (1)	RU2 (1)	NC	NC	RD5 (0)

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UT3/5	0=UT3 1=UT5					
UMA/Dis.		0=UMA 1=Dis.				
NV9M			0			0
ATI M92			0			1
ATI M96			1			0

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M GPIO 3/4	PV

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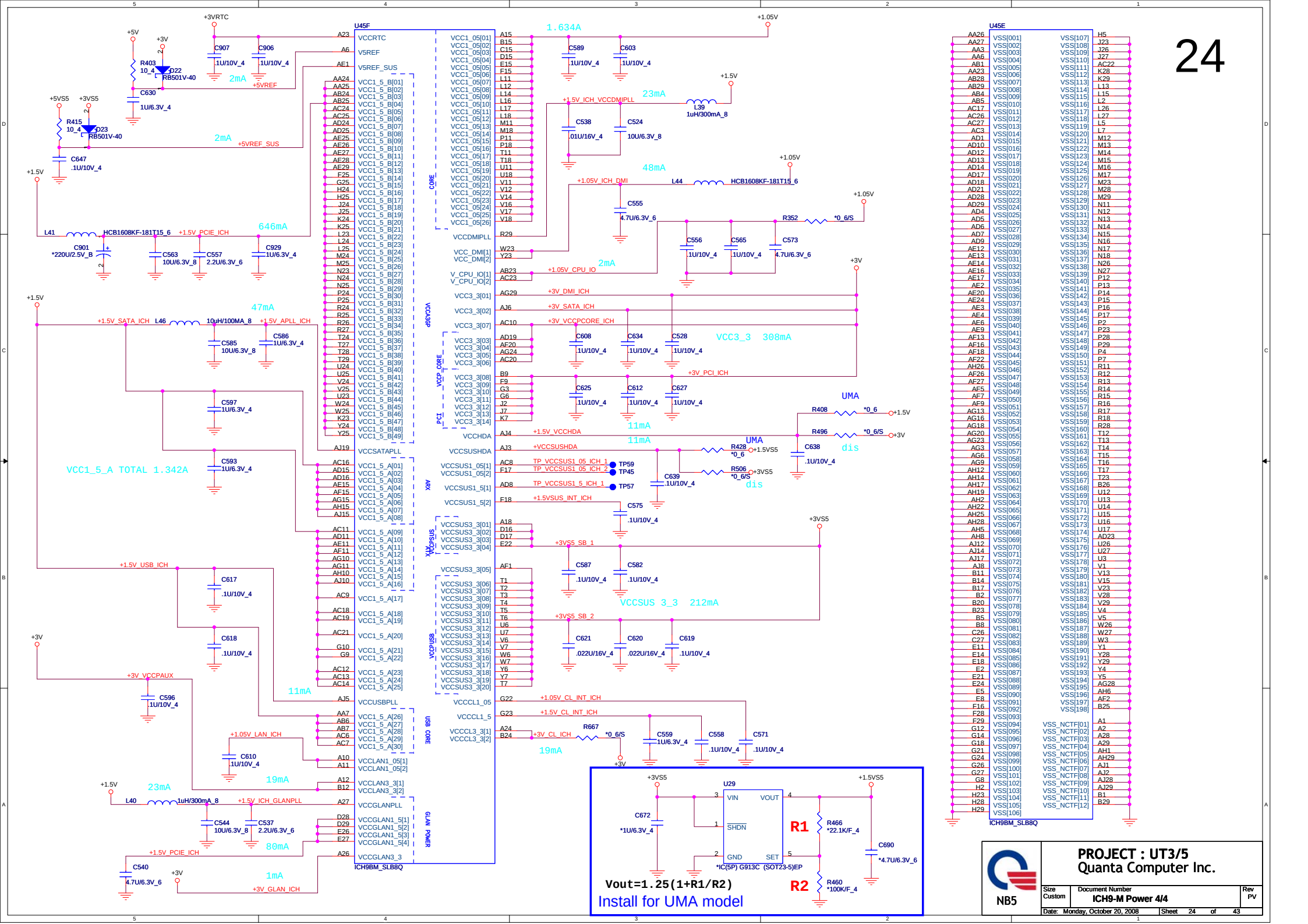
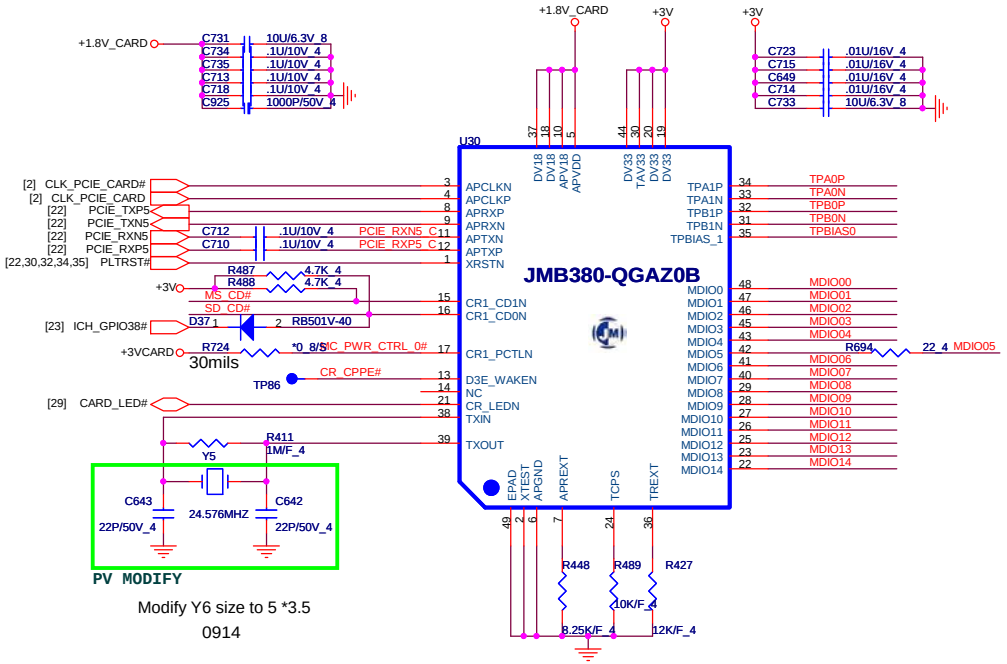


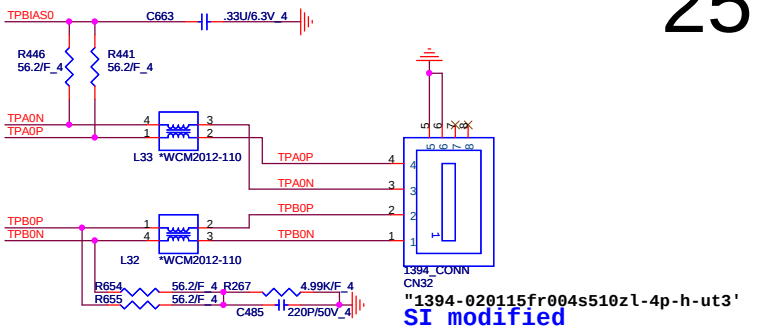
PROJECT : UT3/5 Quanta Computer Inc.			
Size: Custom	Document Number: ICH9-M Power 4/4		Rev: PV
Date: Monday, October 20, 2008	Sheet 24 of 43		
NB5			



PV MODIFY

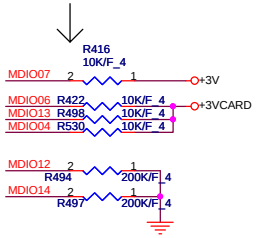
Modify Y6 size to 5 *3.5

0914



SI modified

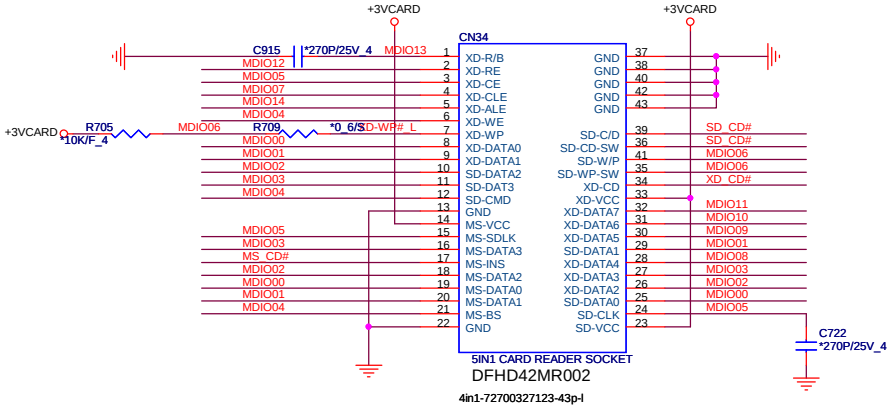
Change to 10K

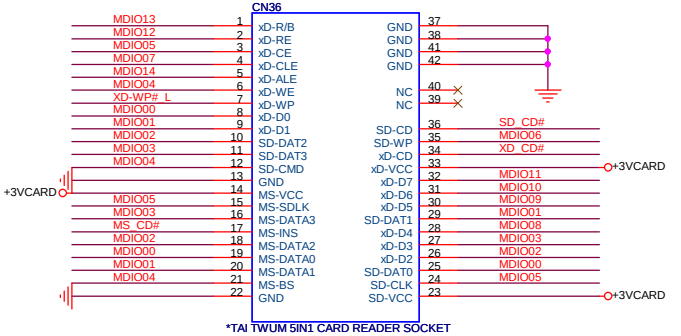


JMB 380 Note:

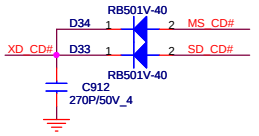
SD/MMC	MS	XD
MDID0 SD_DAT0	MS_D0	XD_D0
MDID1 SD_DAT1	MS_D1	XD_D1
MDID2 SD_DAT2	MS_D2	XD_D2
MDID3 SD_DAT3	MS_D3	XD_D3
MDID4 SD_CMD	MS_BS	XD_WE#
MDID5 SD_CLK	MS_SCLK	XD_CE#
MDID6 SD_WP		XD_WP#
MDID7		XD_CLE
MDID8 SD_DAT4		XD_D4
MDID9 SD_DAT5		XD_D5
MDID10 SD_DAT6		XD_D6
MDID11 SD_DAT7		XD_D7
MDID12		XD_RE#
MDID13		XD_R/B#
MDID14		XD_ALE
CR1_LEDN SD1_LED#	MS1_LED#	XD_LED#
CR1_PCTLN SD1_PCTL#	MS1_PCTL#	XD1_PCTL#
CR1_CD0 SD1_CD#		XD_CV#
CR1_CD1	MS1_CD#	XD_CD#

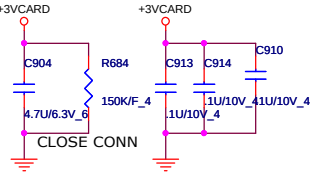
5 IN1 CARD READER
XD,MMC/SD,MS/MSP





*TAI TWUM 5IN1 CARD READER SOCKET





PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	RTS5158 & CR SOCKET &HOLE	PV

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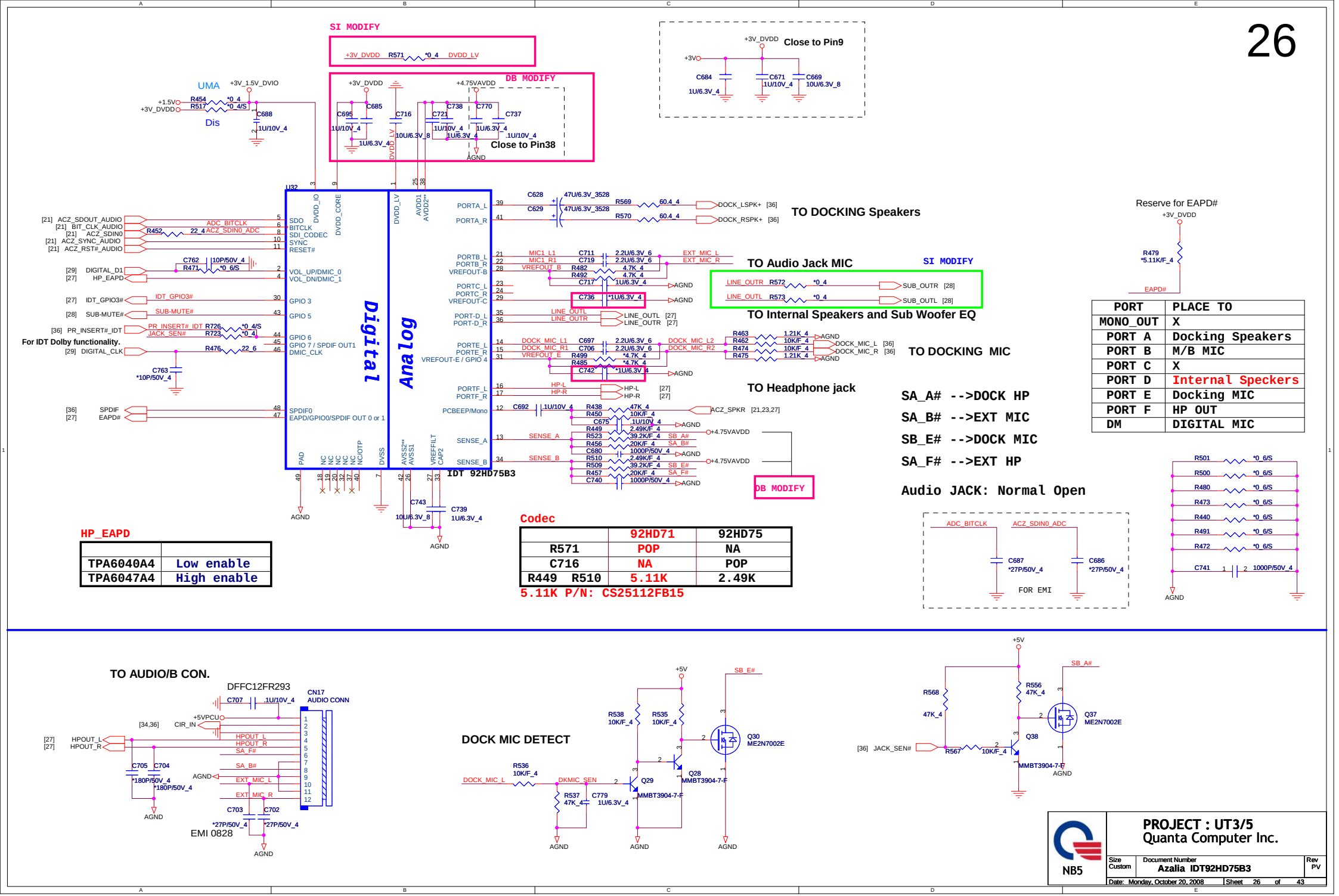

HP_EAPD

TPA6040A4	Low enable
TPA6047A4	High enable

Codec

	92HD71	92HD75
R571	POP	NA
C716	NA	POP
R449 R510	5.11K	2.49K

5.11K P/N: CS25112FB15

PORT	PLACE TO
MONO_OUT	X
PORT A	Docking Speakers
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	HP OUT
DM	DIGITAL MIC

PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Azalia IDT92HD75B3	PV

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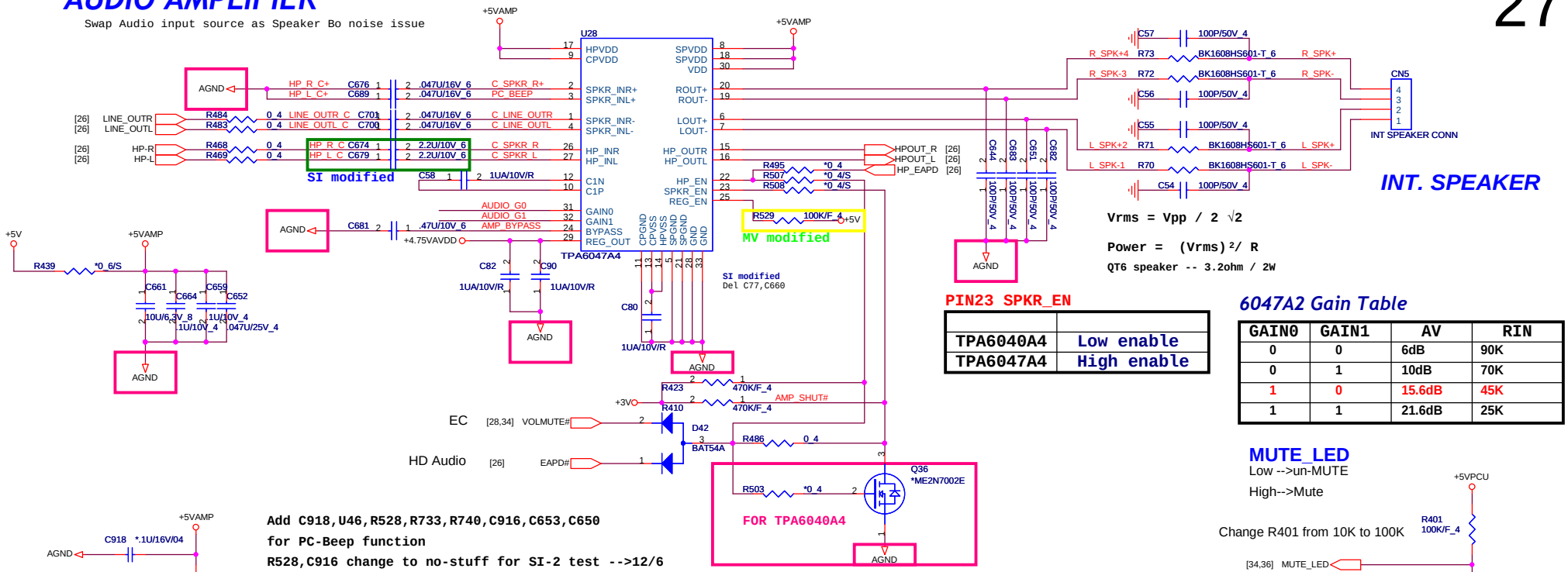
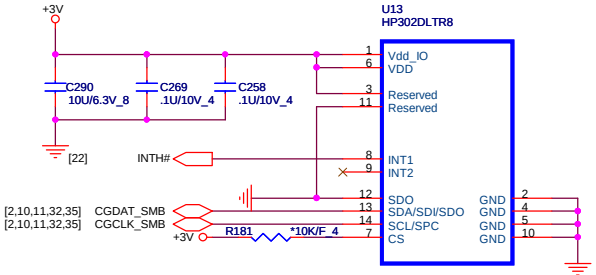
AUDIO AMPLIFIER

Swap Audio input source as Speaker Bo noise issue



Accelerometer Sensor

SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



Change R181 to no stuff as internal pull high

Pin 12: Low 38hex

Pin 12: unconnected/floating 3Ahex

NB5	PROJECT : UT3/5 Quanta Computer Inc.
Size: Custom	Document Number: AMP_TPA6017/Accelerometer
Rev: PV	
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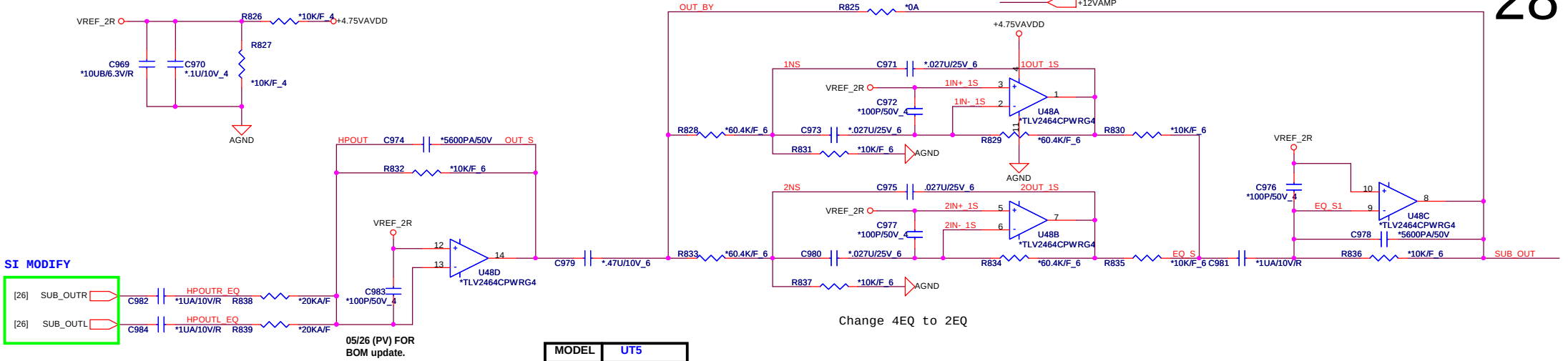
EQ FOR SUBWOOFER

+3V [2,4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,29,30,32,33,34,35,36,40,43]
+5VAMP [27]
+4.75VAVDD [26,27]
+12VAMP

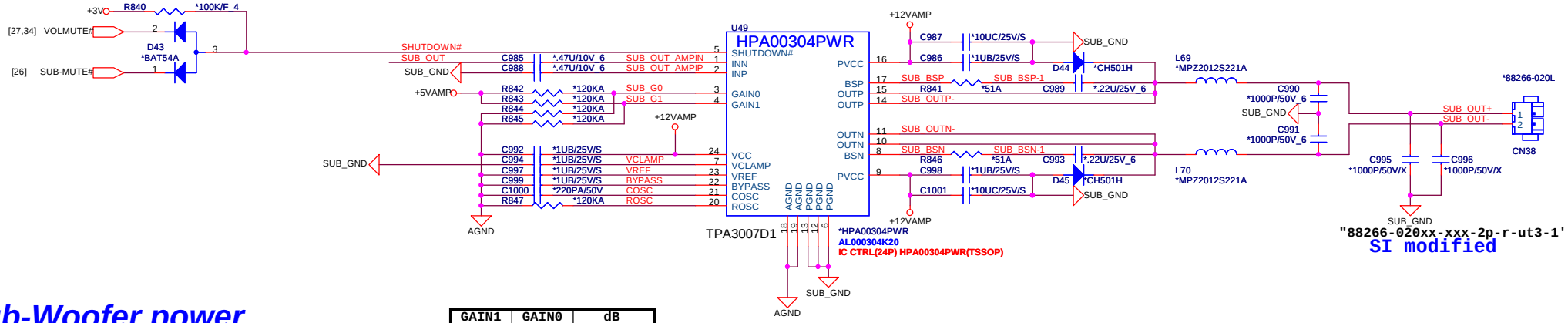


SI MODIFY

05/26 (PV) FOR BOM update.

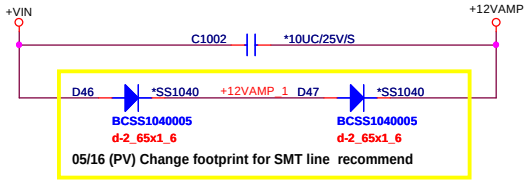
Change 4EQ to 2EQ

MODEL	UT5
R316	60.4K/F_6
R319	60.4K/F_6
R330	60.4K/F_6
R314	60.4K/F_6
C509	0.027U/25V_6
C510	0.027U/25V_6
C529	0.027U/25V_6
C543	0.027U/25V_6



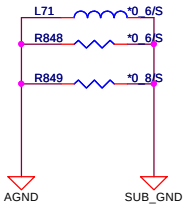
"88266-020xx-xxx-2p-r-ut3-1'
SI modified

Sub-Woofer power



05/16 (PV) Change footprint for SMT line recommend

GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36



NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SUBWOOFER(EQ & AMP.)	PV

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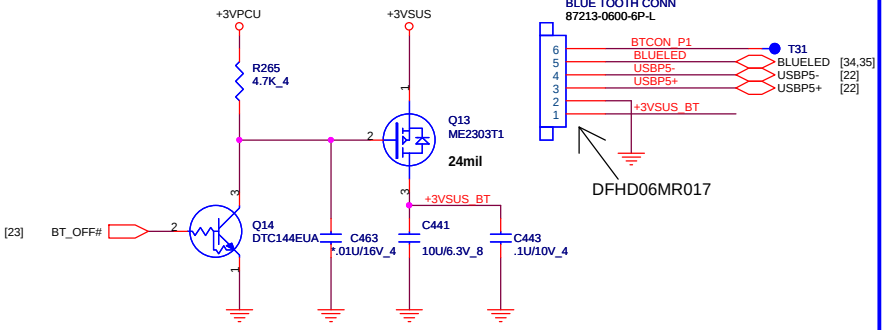
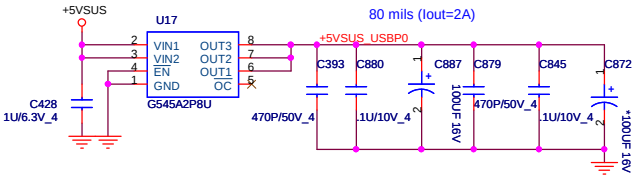
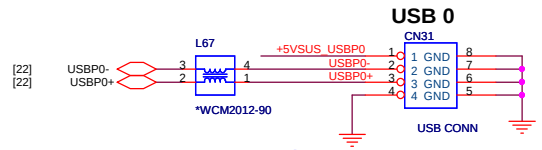
BLUETOOTH



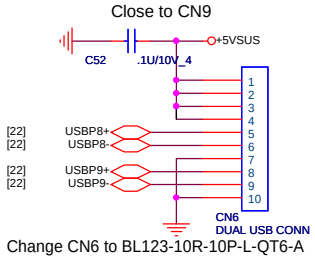
LEFT SIDE USBX1 and E-SATA/USB COMBO





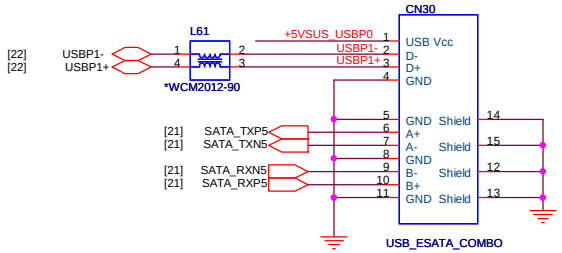
SI modified
usb-020173mr004s51-4p-r-h-ut3

RIGHT SIDE USBX2



Change CN6 to BL123-10R-10P-L-QT6-A

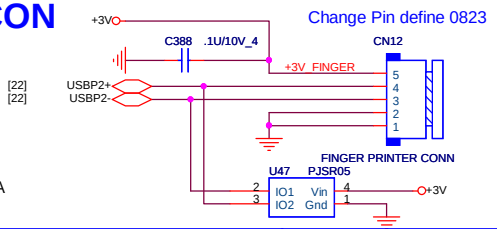
USB & ESATA



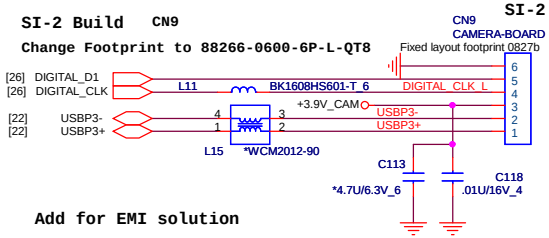
USB fingerprint CON

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

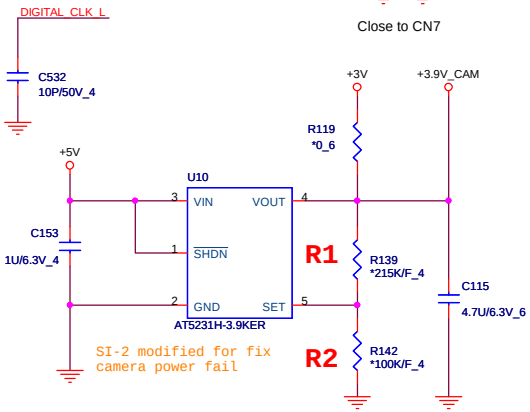
Change CN12 to BL123-05R-5P-L-QT6-A
Add U47 for Finger print USB signal



USB CAMERA /DIGITAL MIC CONNECT

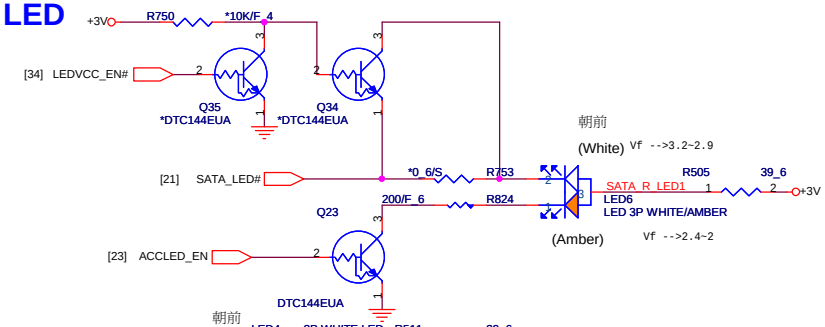


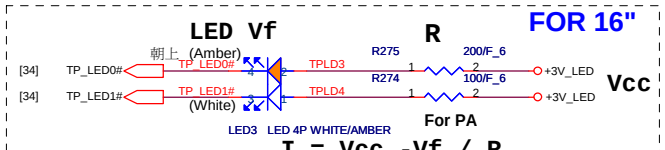
Close to CN7

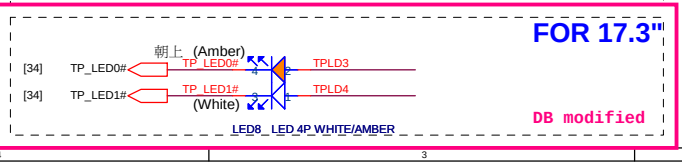


Vout=1.25(1+R1/R2)

LED

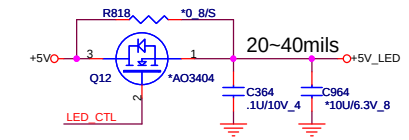


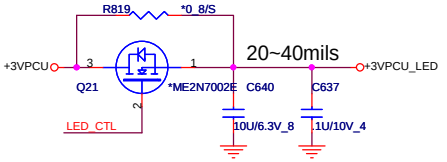


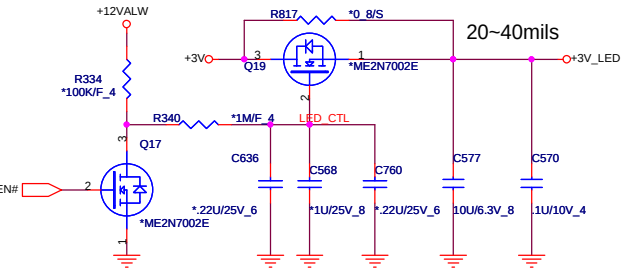


LED PWR CONTROL

Change Q12 to AO3404 as LED current limited







NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/WC/FT/TS/ESATA/USB	PV
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T : Stuffed for RTL8111C(10/100/1000)

E : Stuffed for 8101E/8102E(10/100)

For 8102E/8111C

[31] +CTRL15 — R648 *0_6 — +CTRL15_E
Stuffed for 8102E

[31] +FB12 — R641 *0_6/S — +LAN_A1.8_FB12
Stuffed for RTL8111C and nostuff 8102E

+LAN_D1.5 — R649 *0_6/S — +LAN_D1.5_SRVDD
Stuffed for 8102E/RTL8111C

+3VLANVCC — R647 *0_6/S — +CTRL15_E
C894 10U/6.3V_8 — C889 10U/6.3V_8 — C890 .1U/10V_4
+3VLANVCC — R247 *0_6/S — +3V_GVDD
enable switch regular
Stuffed for RTL8111C(10/100/1000)

Y2 25MHZ
C427 33P/50V_4 — C420 33P/50V_4
PV MODIFY
8102E No Mount
8111C No Mount ,R247 mount

C414 *.1U/10V_4 — C417 *.1U/10V_4 — R233 2.49K/F_4 — LANRSET

U18#63 wider than 40 mils
U18#1 wider than 60 mils

U18 RTL8111C-VB-GR
Pin 65

Isolate pull low:
1.Can only disable RTL8111C.
2.RTL8101E can't disable

for 93C56 used. NC if 93C46 is used.
R653 *10K/F_4 — U43 *M93C46-WMN6TP — C897 *.1U/10_4
3.24K/F_4 R652

R263 *1K/F_4 — R262 15K/F_4
Change back to R261 at 1/24
ISOLATEB — R261 100/F_4 — D38 *RB501V-40 — LAN_DISABLE# [34]

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

R252 *0_6/S — R259 *0_6/S — LAN-AGND

C531 .1U/10V_4
New add and Close to Pin 5
From Vendor EMI suggest

R434 *0_4
8111C = No Mount
8102E = Mount

T3 T4

PCIE_RXN1_LAN_L — C452 .1U/10V_4 — C442 .1U/10V_4 — PCIE_RXN1_LAN [22]
PCIE_RXP1_LAN_L — PCIE_RXP1_LAN [22]
CLK_PCIE_LAN# — CLK_PCIE_LAN# [2]
CLK_PCIE_LAN — CLK_PCIE_LAN [2]

Swap PCIE from Port 6 to PCIE Port 1

Swap PCIE from Port 6 to PCIE Port 2

[22,25,32,34,35] PLTRST# — R248 *0_4/S
[34] LAN_REST# — R246 *0_4

AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)
AL08102E001 IC CTRL(64P) RTL8102E-VB-GR(QFN)

Remove 8111B and 8101E support in PV Build
1. Delete R264 (For 8111B)
2. Delete R650 and T28
3. Delete R651 and U18#33 for 8111B support
4. Delete R231 as RSET
5. Delete R242,R243,R244,R245,C394,C395 8101E support

Stuffed for RTL8101E
R589 *0_4

Add C898,C899,C900,C902 as HP request

U33 NS892402
C782 .01U/16V_4 — C783 .01U/16V_4 — C789 .01U/16V_4 — C790 .01U/16V_4
R544 75/F_4 — R545 75/F_4 — R547 75/F_4 — R548 75/F_4
C898 0.01U/100V_0603 — C899 0.01U/100V_0603 — C900 0.01U/100V_0603 — C902 0.01U/100V_0603
C781 1000P/3KV_1808

Link
D36 BAT54A — D35 RB501V-40 — R109 *0_4/S
C48 *.01U/16V_4 — C88 *.01U/16V_4

RJ45 CN24
C89 *.1U/10V_4 — R89 330/F_4 — C87 *.1U/10V_4 — R87 330/F_4
C81 *.1U/10V_4
RJ45_CONN

NS892402:GIGABIT
NS892405:10/100

DB0AT9LAN05
DB0ZB1LAN04

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8111C/8101E/RJ45	PV

Date: Monday, October 20, 2008 Sheet 30 of 43

T : Stuffed for RTL8111C(10/100/1000)

E : Stuffed for 8101E/8102E(10/100)

LANVCC
1.2W
364mA

+3VLANVCC

Power trace Layout 寬度> 30mil

+3V_LAN

C454 .1U/10V_4
C475 .1U/10V_4
C477 .1U/10V_4
C399 .1U/10V_4

these CAP are for LAN CHIP LANVCC pins--16, 37, 46 and 53.placement close lan chip

C385 4.7U/6.3V_6
C480 .1U/10V_4

+3V_A_LAN

C401 .1U/10V_4
C434 .1U/10V_4

these CAP are for LAN CHIP LAN_A3.3 pins-- 2 and 59.placement close lan chip

8111C CV-4706MN00
8102E CS00004JA40

For Giga must change L65 to Inductor (Chipset include switch power)

+CTRL18 will become to switch power phase

placement close to lan chipset

L54 for Gaga lan use 4.7uH power choke
A>500mA tolerance ±15%

SI Build

+CTRL18

L65 4.7UH_2016

+FB12 [30]

L63 *0_8/S

Power trace Layout 寬度> 30mil

+LAN_A1.8

C884 *4.7U/6.3V_6

C931 *10U/6.3V_8 SI build
C930 10U/6.3V_8 SI build
C881 4.7U/6.3V_6
C876 4.7U/6.3V_6
C878 .1U/10V_4

For 8102E

C891 .1U/10V_4
C892 .1U/10V_4
C875 .1U/10V_4
C893 .1U/10V_4

these cap are for lan chip LAN_A1.8 pins--5, 8, 11 and 14. placement close chip

STUFF 100 ohm BEAD

+LAN_E1.8

R250 *0_8/S

C422 Change to 1u for 8102E

C421 .1U/10V_4
C422 1U/6.3V_4

LAN-AGND

these cap are for lan chip LAN_D1.8 pins, such as 22 and 28. placement close lan chip

Remove R250,L63,L66 -->For 8102E

L66 *0_8/S

Only For 8111C application

[30] +CTRL15

L64 *0_8

C883 *4.7U/6.3V_6
C888 *4.7U/6.3V_6
C895 *4.7U/6.3V_6
C896 *.1U/10V_4

For 8102E

+LAN_D1.5

Power trace Layout 寬度> 30mil

C474 .1U/10V_4
C479 .1U/10V_4
C459 .1U/10V_4
C456 .1U/10V_4
C472 .1U/10V_4
C461 .1U/10V_4
C476 .1U/10V_4
C415 .1U/10V_4
C478 .1U/10V_4
C400 .1U/10V_4

these cap are for lan chip LAN_D1.5 pins-- 15, 21, 32, 33, 38, 41, 43, 49, 52 and 58.placement close lan chip

Power domain chart

	RTL8111C(P) RTL8102E
LANVCC	3.3V
LAN_D1.8	1.2V
LAN_A1.8	1.2V
LAN_D1.5	1.2V

C422 change to 1uf

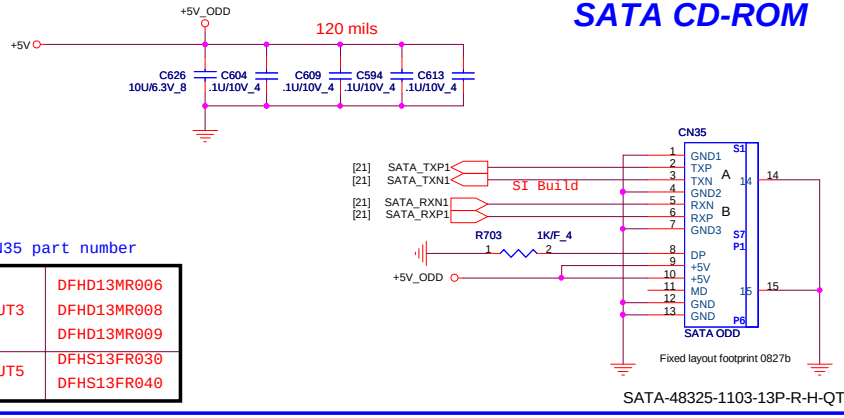
PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size A3 | Document Number LAN Power | Rev PV

Date: Monday, October 20, 2008 | Sheet 31 of 43

SATA CD-ROM



CN35 part number

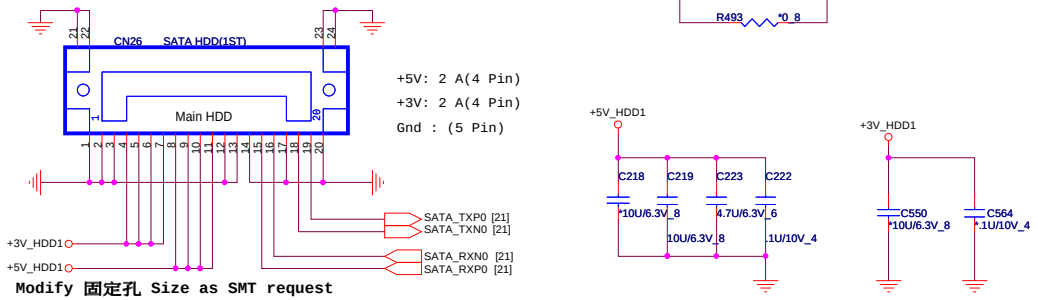
UT3	DFHD13MR006
	DFHD13MR008
	DFHD13MR009
UT5	DFHS13FR030
	DFHS13FR040

SATA-48325-1103-13P-R-H-QT6

SATA HDD CONNECTOR

DFHD20MR005

DC Current rating: 0.5 A



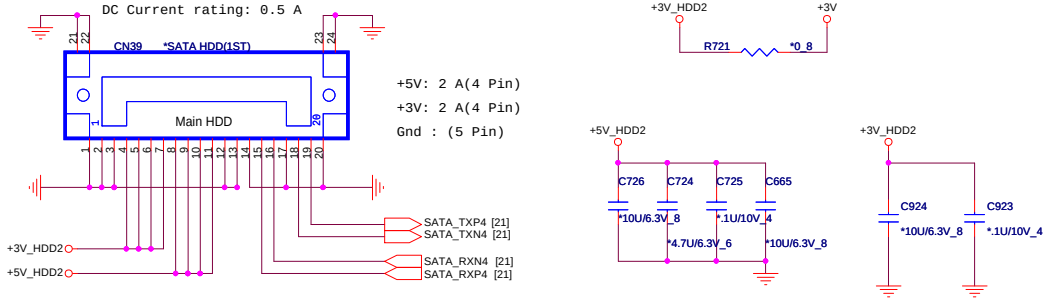
Modify 固定孔 Size as SMT request

GS12201-1011-9F-20P-L-QT6

DB modified

SATA_2 CONNECTOR

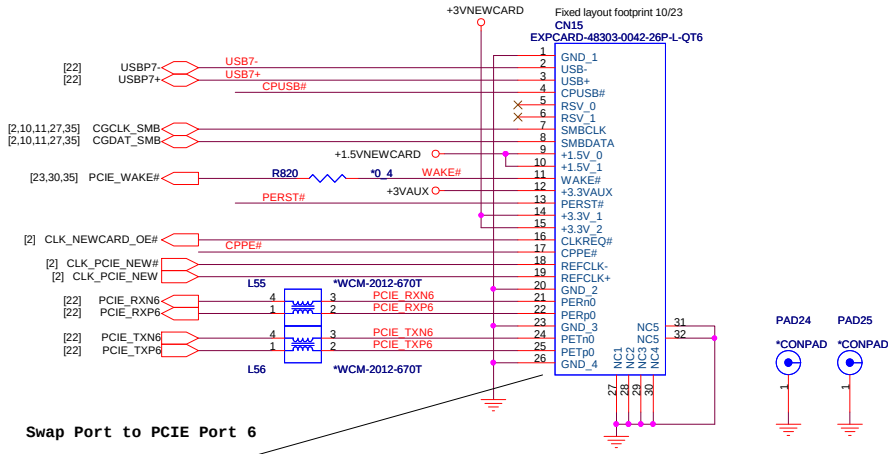
DC Current rating: 0.5 A



NEWCARD

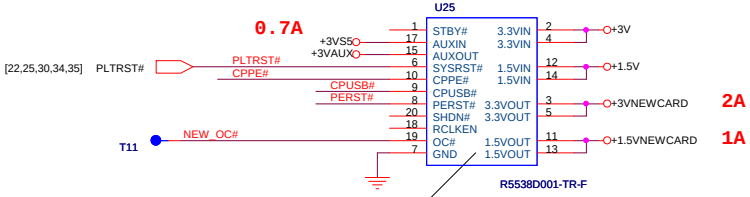
NEWCARD (PCIEXPRESS*1 + USB*1)

32

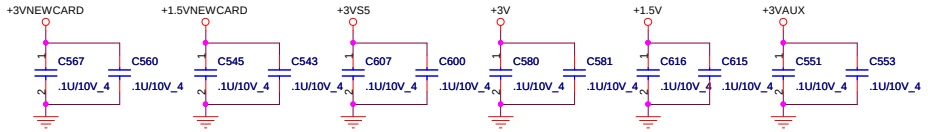


Swap Port to PCIE Port 6

Change CN15#31,32 as ME request for Hole pad
expcard-48303-0042-26p-l-qt6 as ME modify Pad size(pin31,32)
Move CN15#29,30 Pin as ME request(Molex confirm drawing)



add Pin 21~25 as U25 Thermal pad tied to Gnd



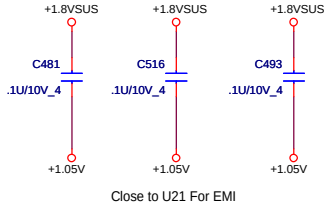
	Header	Housing
MLX	DFHD26MS012	DFHS26FR023
FOX	DFHD26MS013	DFHS26FR024
DGN	DFHD26MS017	DFHS26FR028

NB5

PROJECT : UT3/5
Quanta Computer Inc.

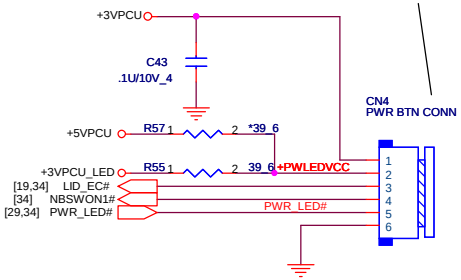
Size	Document Number	Rev
Custom	ODD/HDD/NEW CARD	PV

Date: Monday, October 20, 2008 Sheet 32 of 43



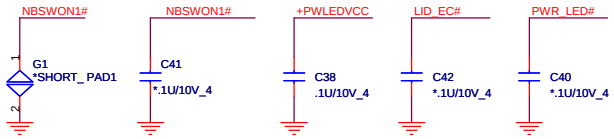
Close to U21 For EMI

Change CN4 to BL123-06R-6P-L-QT6-A



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

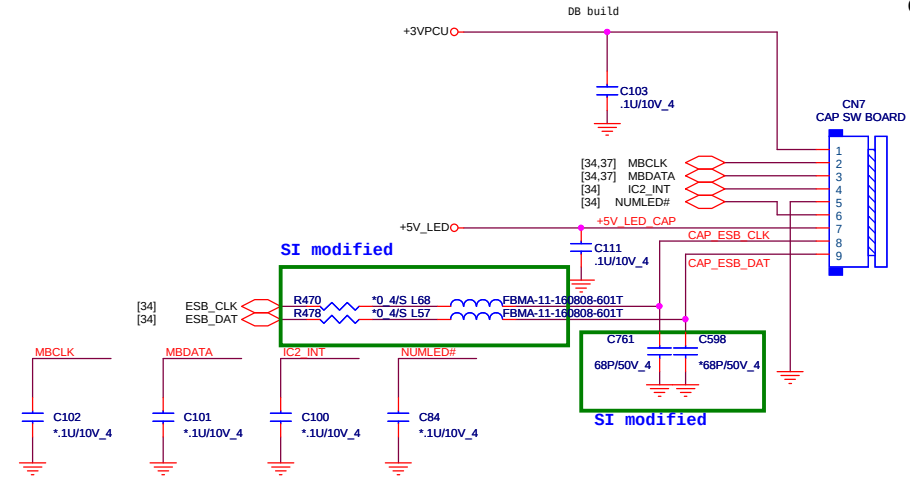
POWER BOTTON CONNECT



EMI 0828

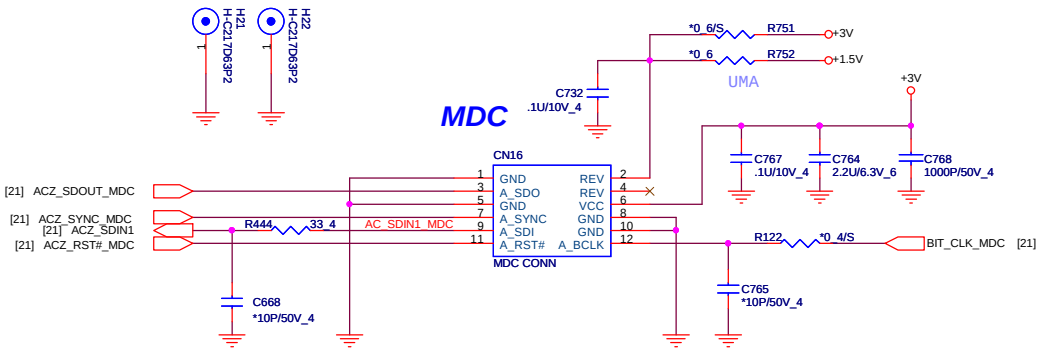
POWRER SW CONNECT

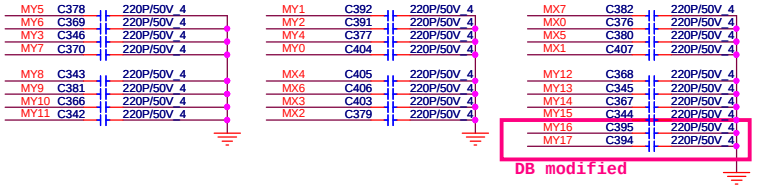
CAP SW CONNECT



1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V_LED
8. ESB_CLK
9. ESB_DAT

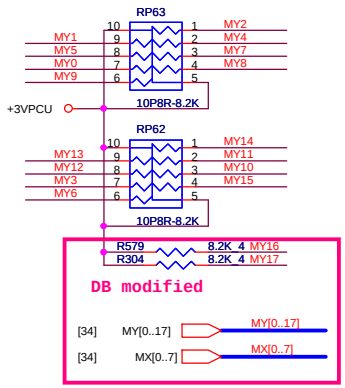
Modem CONN

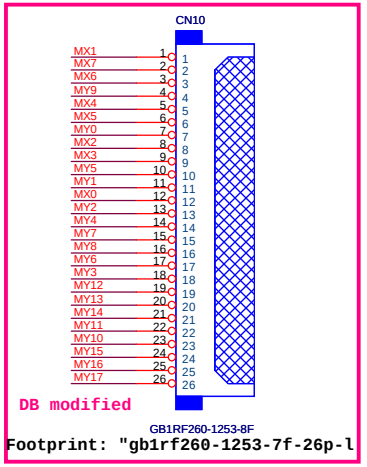




DB modified

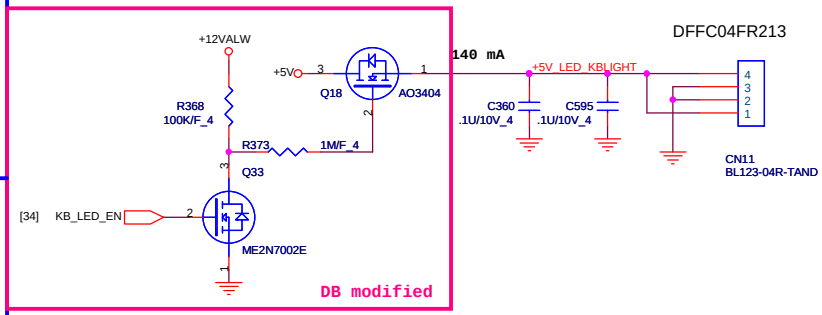
KEYBOARD PULL-UP





clear ABS 758 resin for key cap.
7 LEDs for 15.4" (total LED current 140mA)
11 LEDs for 17" (Total LED current 220mA)

DFFC04FR213



NB5	PROJECT : UT3/5 Quanta Computer Inc.	
Size: Custom	Document Number: KB/CAP/POWER CONN/MDC	Rev: PV
Date: Monday, October 20, 2008	Sheet 33 of 43	

Change U20 layout footprint
to LQFP128-16X16-4-AA1

U20

KB3926QF C0

DB modified

SI modified

R323 remove for KB3926 C version

For KB3926 B, C version

Hi ==> 120W
Low ==> 65W/90W

ID	R374	R379
UT3	10K	N/A
UT5	N/A	10K

R430 Change to 100k ohm ,pull low

Change to RB500 as Current loss

Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier
Add T37,T38,T39 for EC
Delete T10 and tie pin 117 from Lan for DSM

TOUCH PAD CONNECTOR

25 mils

CN13
TOUCH PAD CONN
DFFC12FR293

TOUCH PAD L/R FOR 16"

TOUCH PAD ON/OFF FOR 16"

close conn

TOUCH PAD L/R FOR 17.3"

TOUCH PAD ON/OFF FOR 17.3"

DB modified

Socket: DG008000031

MXIC AKE38FP0Z00
WINBOND AKE38ZP0N01
EON AKE38ZA0Q00

2M byte
SPI
BIOS

R273
64.9K -->65W CS36492FB17
33.2K -->90W CS33322FB13
Change to 1SS355 as Current loss

PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	KB3926/ROM/TP	PV

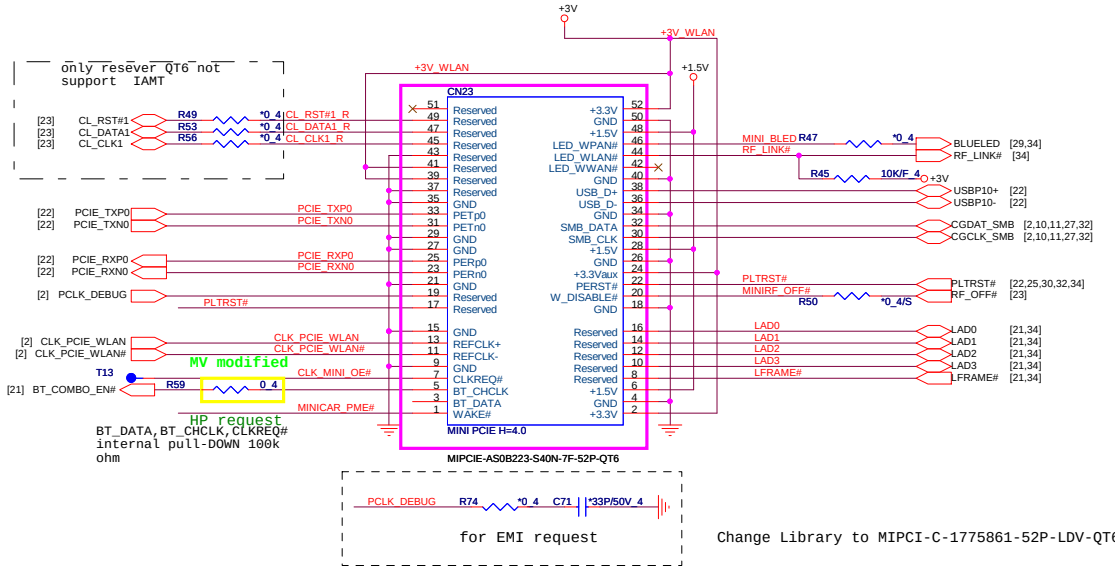
Date: Monday, October 20, 2008 | Sheet 34 of 43

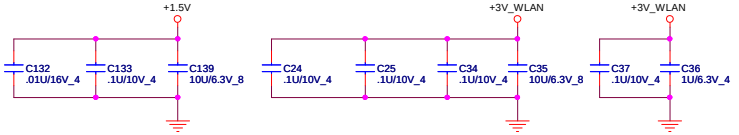
Mini PCI-E Card 1
WLAN

Delete R78 and tied the CN23#24 to R110 direction
Change CN23 layout footprint to MIPCIE-AS0B223-S40N-7F-52P-QT6 as ME drawing

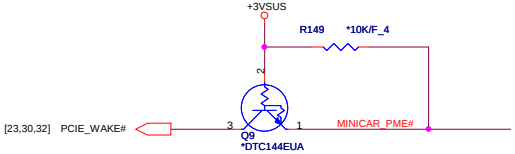
Change net name

35





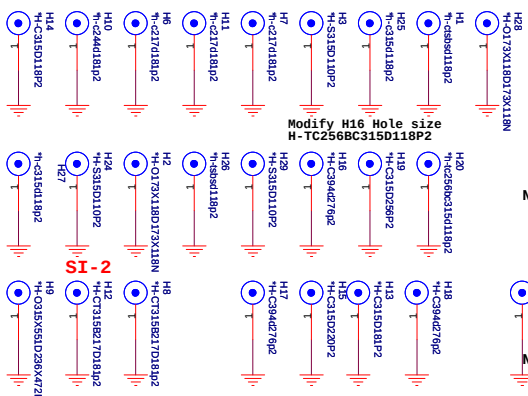
INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm



Change Library to MIPCI-C-1775861-52P-LDV-QT6 12/11

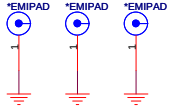
M/B Screw Hole

SI-2,h-e276x315d118p2

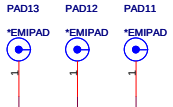


New add as ME request

RF PAD

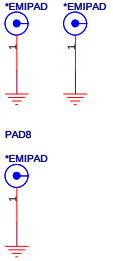


New add as RF request



New add as RF request

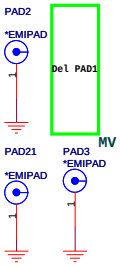
ME PAD



Routed spring

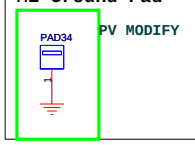
Delete PAD14

EMI PAD

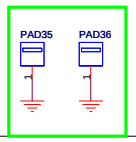


ME Routed spring

ME-Ground Pad

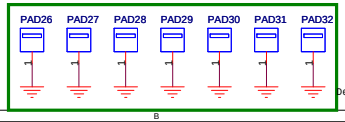


ME-Ground Pad

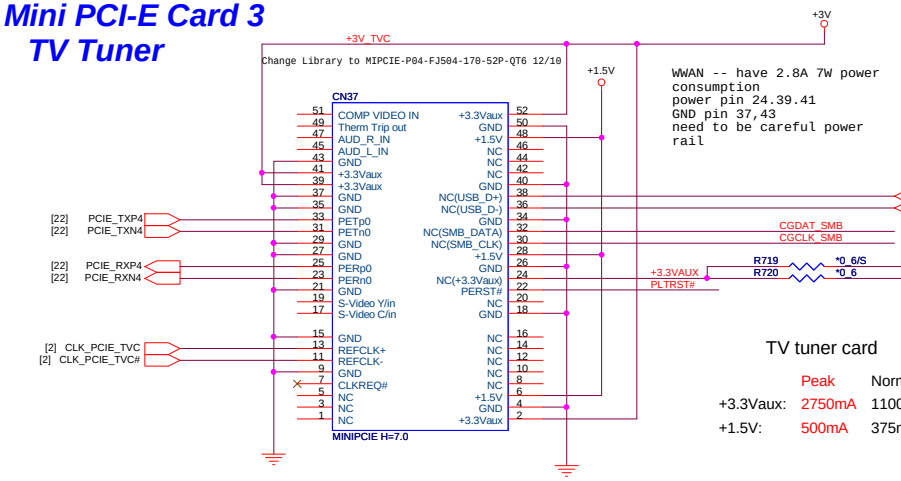


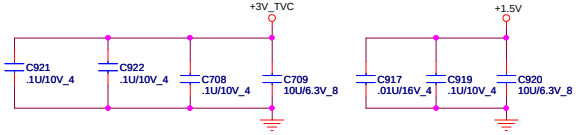
SI modified

ME-Ground Pad



Mini PCI-E Card 3
TV Tuner





NB5

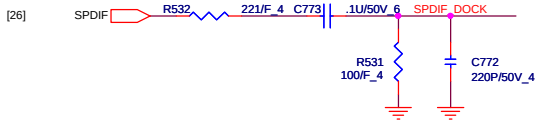
PROJECT : UT3/5
Quanta Computer Inc.

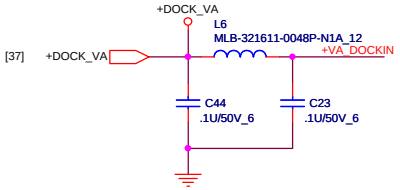
Size	Document Number	Rev
Custom	MINI PCIE CONN X2 & HOLE	PV

Date: Monday, October 20, 2008 Sheet 35 of 43

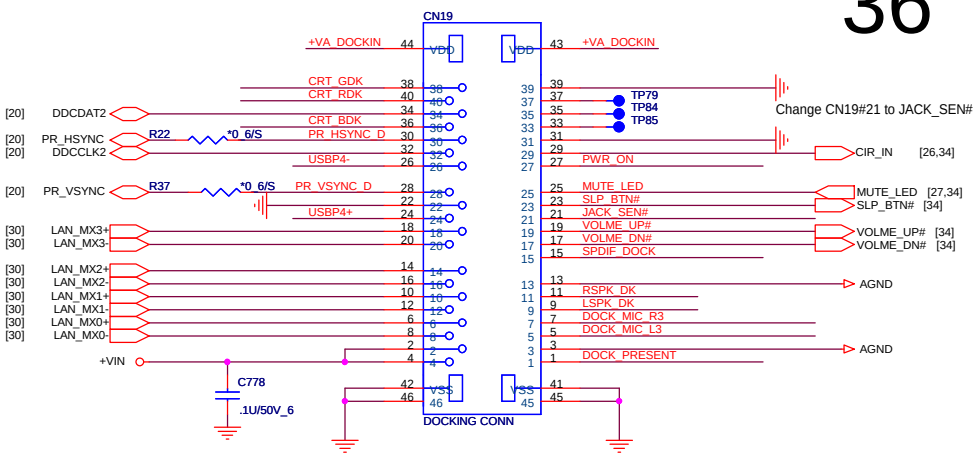
CABLE DOCK

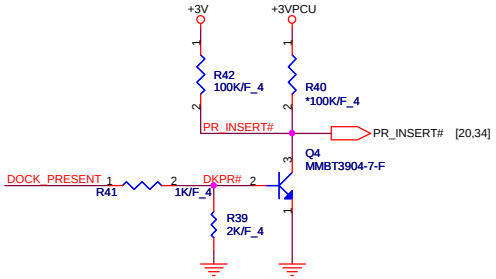
support 6A 200mils
CX000480005

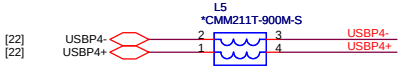




DFHS44FRC04

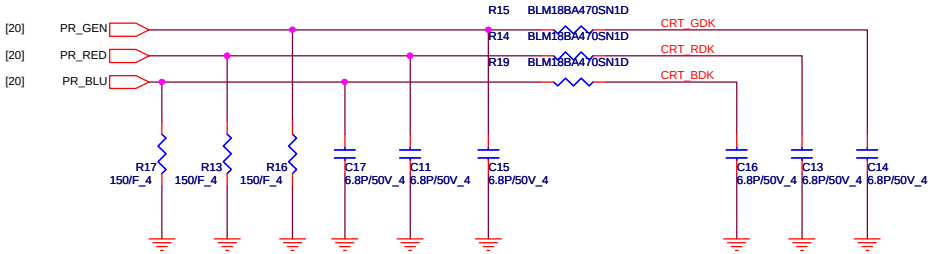






R13,R16,R17 Change to install

Delete CX08T470000 as CRT rising time and falling time request

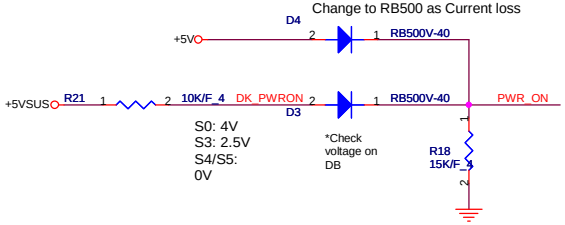


For IDT Dolby functionality.

DB modified

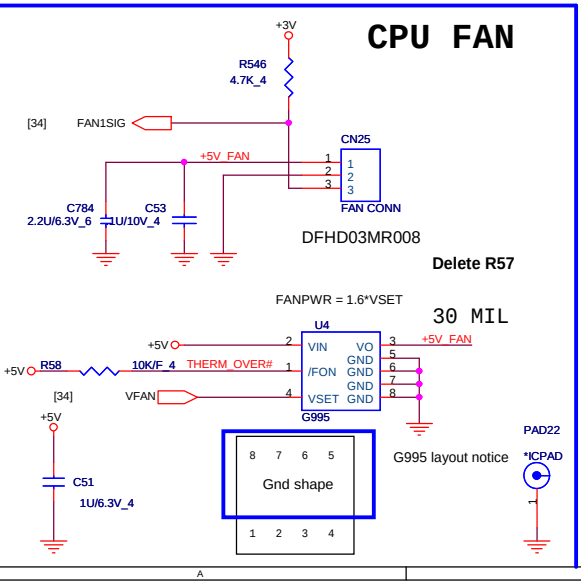
[26] PR_INSERT#_IDT — PR_INSERT#_IDT — R730 *0_4/S — R_INSERT#

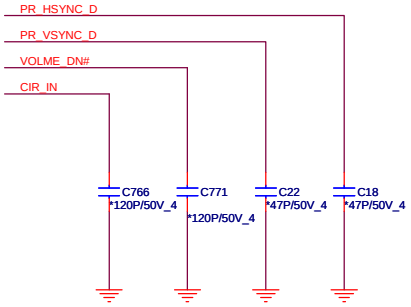
Change to RB500 as Current loss

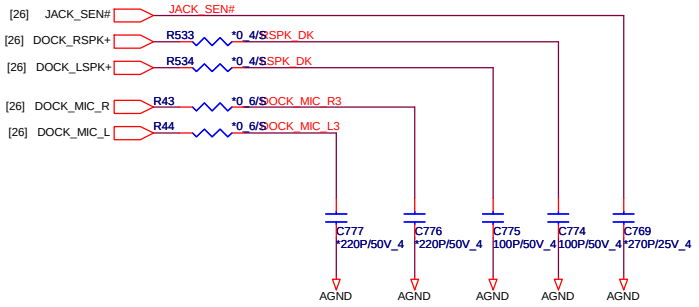


Add Loss net(GND Net)

CPU FAN



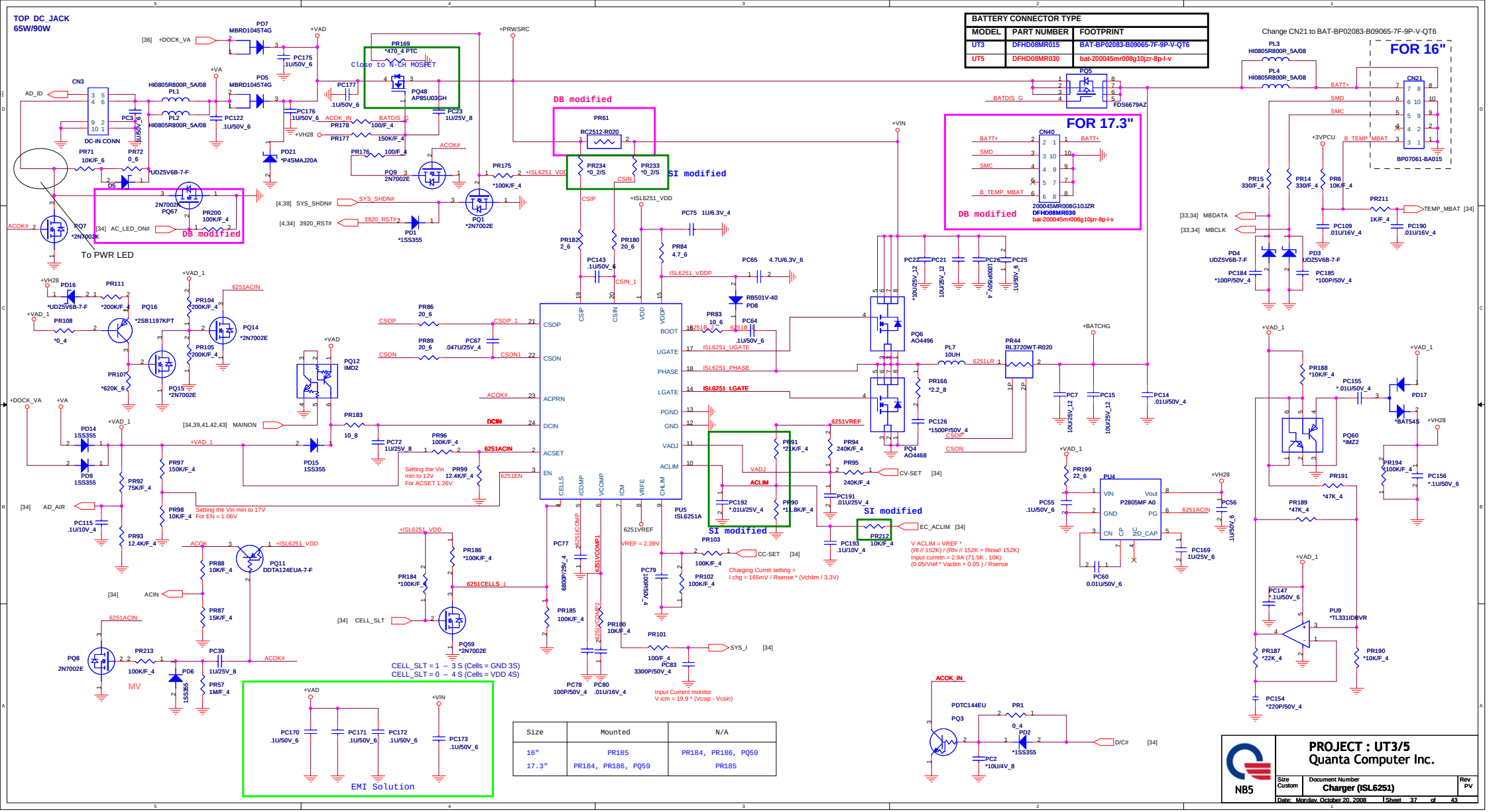




Change to Analog Gnd

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CABLE DOCKING/FAN	PV
NB5	Date: Monday, October 20, 2008	Sheet 36 of 43



Size	Mounted	N/A
16"	PR185	PR184, PR186, PQ59
17.3"	PR184, PR186, PQ59	PR185

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs

5 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 9A

SI modified

SI modified

Rds(on) 20m ohm

Rds(on) 20m ohm

[4,37] SYS_SHDN#

HWPG [34,39,41,42]

NB5	PROJECT : UT3/5 Quanta Computer Inc.	
Size B	Document Number +5V/+3V (ISL6237)	Rev PV
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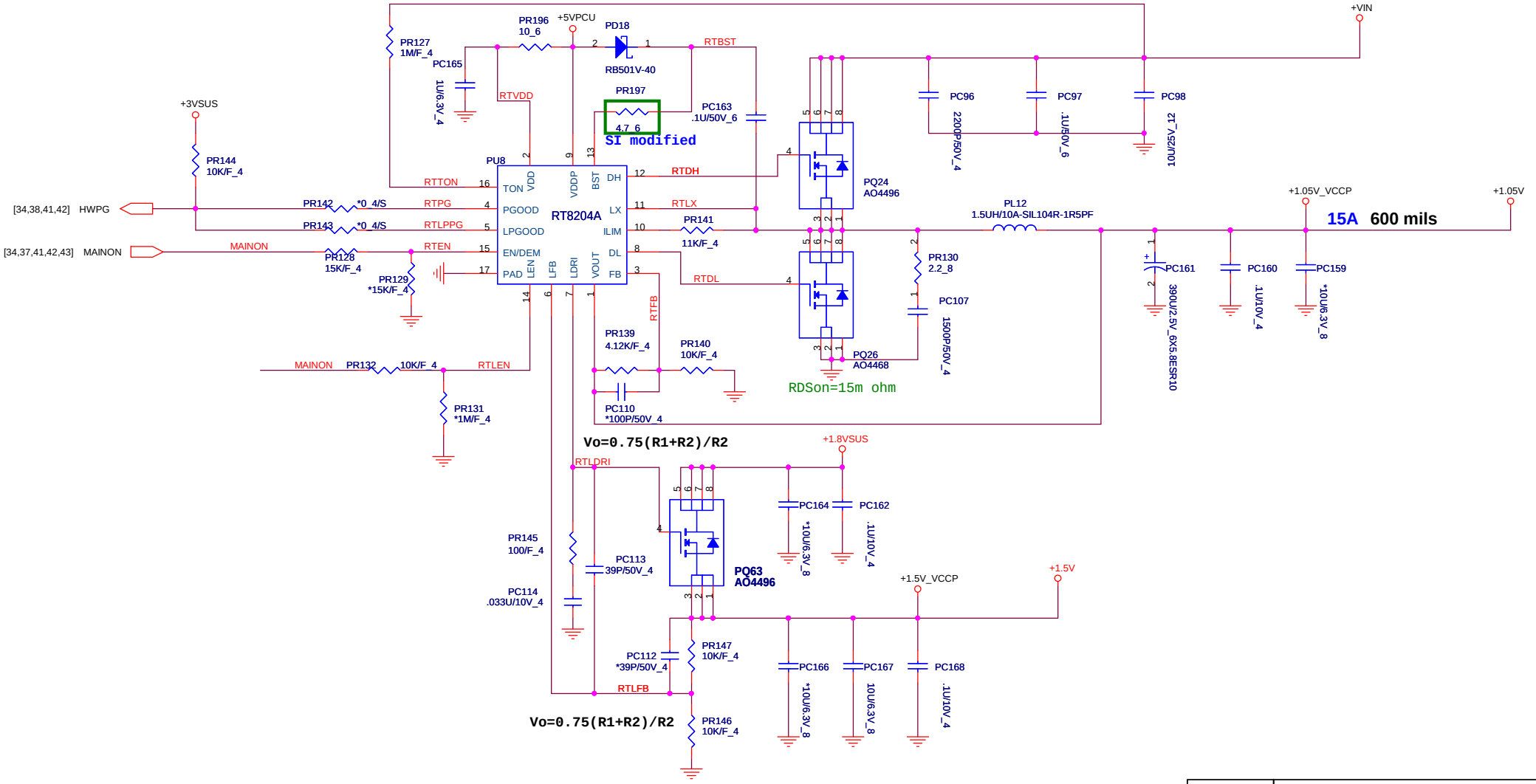
VCCP1.05V & +1.5V

+1.05Volt +/- 5%
Countinue current:7.5A
Peak current:10A
OCP minimum 15A



NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.05V/+1.5V (RT8204)	PV

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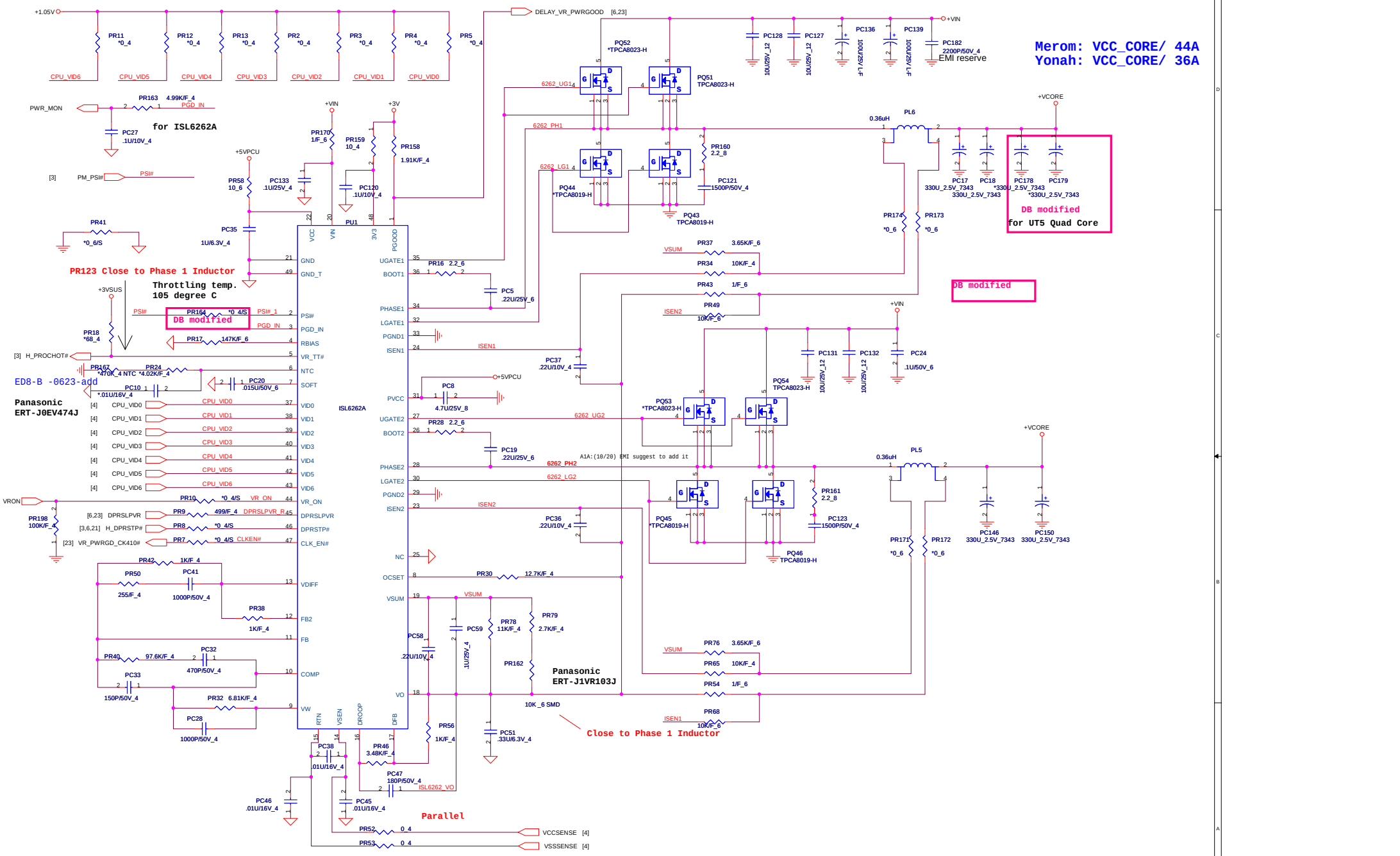
Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A
for ISL6262A
PR123 Close to Phase 1 Inductor
Throttling temp.
105 degree C
DB modified
DB modified
DB modified
for UT5 Quad Core
ED8-B -0623-add
Panasonic
ERT-J0EV474J
Panasonic
ERT-J1VR103J
ISL6262A
Close to Phase 1 Inductor
Parallel
EMI reserve
A1A:(10/20) EMI suggest to add it
+1.05V
+VIN
+3V
+3VSUS
+5VPCU
+VCORE
DELAY_VR_PWRGOOD [6,23]
PWR_MON
PM_PSI#
PSI#
PGD_IN
H_PROCHOT#
VRON
VR_ON
CLKEN#
DPRSLPVR
DPRSTP#
VR_PWRGD_CK410#
CPU_VID0
CPU_VID1
CPU_VID2
CPU_VID3
CPU_VID4
CPU_VID5
CPU_VID6
6262_UG1
6262_PH1
6262_LG1
6262_UG2
6262_PH2
6262_LG2
ISEN1
ISEN2
VSUM
ISL6262_VO
VCCSENSE [4]
VSSSENSE [4]
PROJECT : UT3/5
Quanta Computer Inc.
NB5
CPU Core (ISL6262A)
Monday, October 20, 2008
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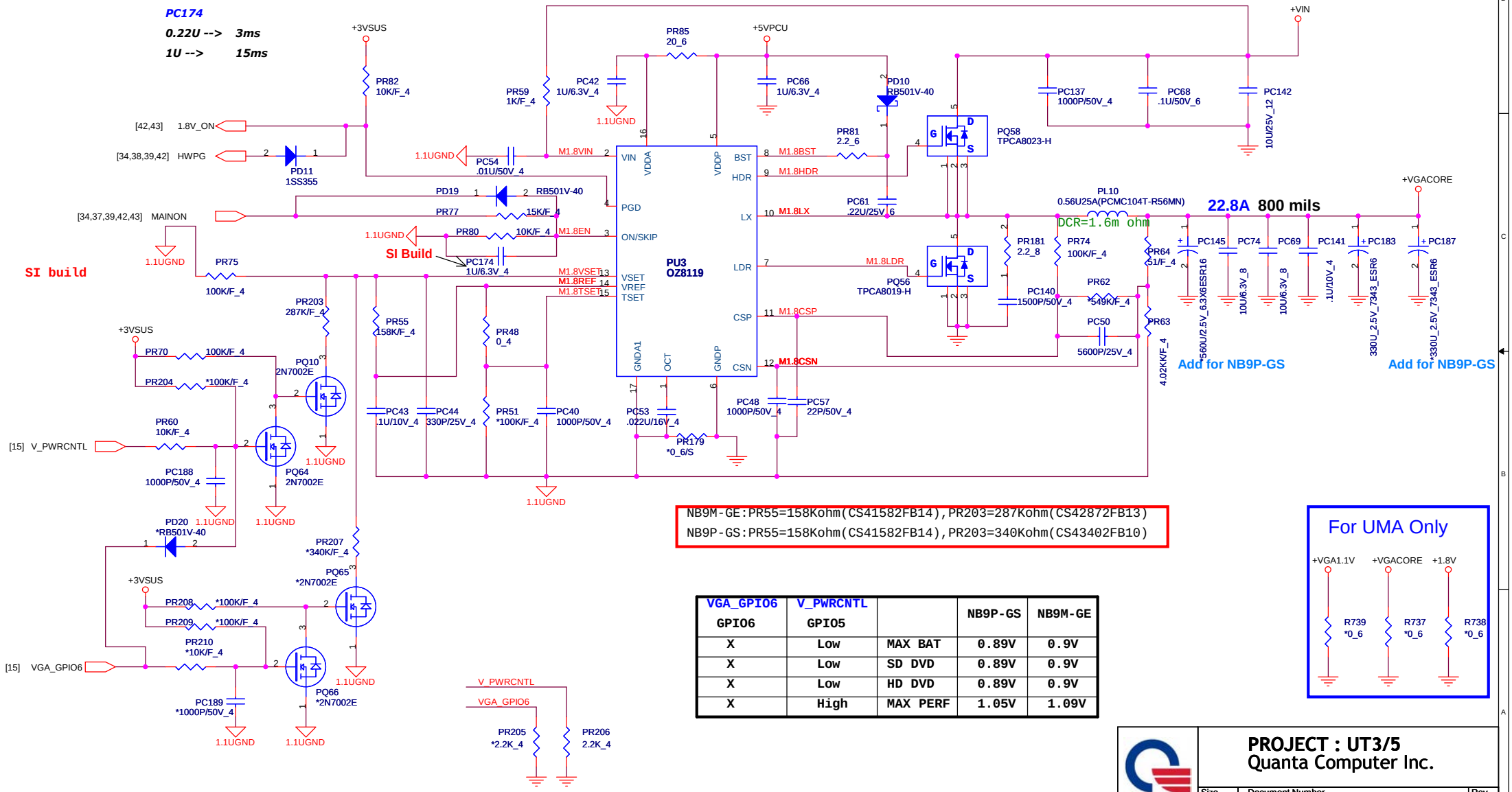
VGA Core & VCC1.1

+1.1Volt +/- 5%
Countinue current:17.54A
Peak current:22.8A
OCP minimum 23A



NB9M-GE:PR55=158Kohm(CS41582FB14),PR203=287Kohm(CS42872FB13)
NB9P-GS:PR55=158Kohm(CS41582FB14),PR203=340Kohm(CS43402FB10)

VGA_GPIO6 GPIO6	V_PWRCNTL GPIO5		NB9P-GS	NB9M-GE
X	Low	MAX BAT	0.89V	0.9V
X	Low	SD DVD	0.89V	0.9V
X	Low	HD DVD	0.89V	0.9V
X	High	MAX PERF	1.05V	1.09V

NB5

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B	VGA Core OZ8119	PV

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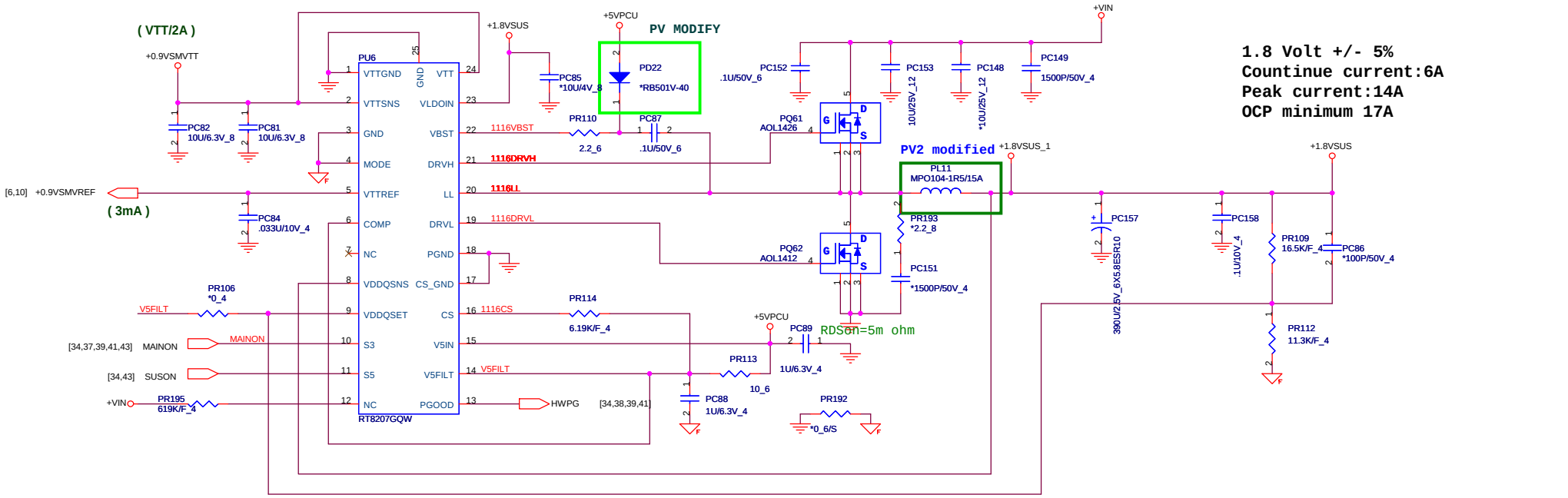
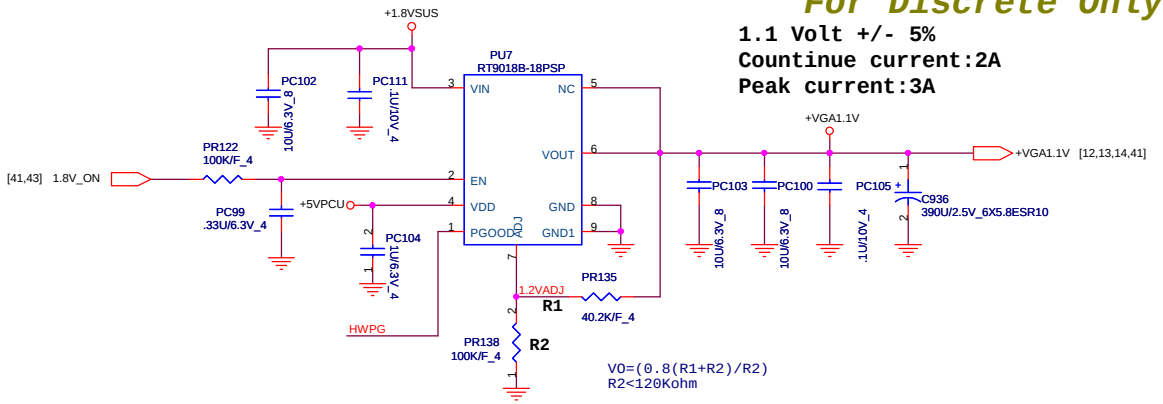
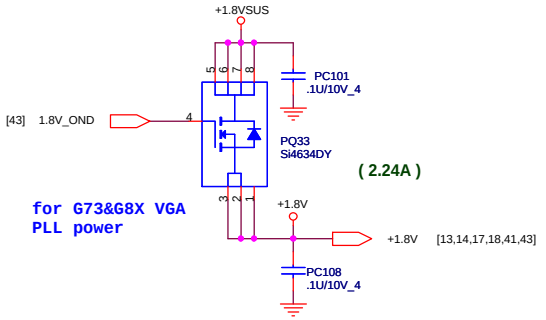


Change PR122 tied to 1.8V_ON as power sequence reuqest





NB5	PROJECT : UT3/5 Quanta Computer Inc.	
	Size: Custom Document Number: 1.8V/DDR_VTER/+1.8v/+1.1V	Rev: PV
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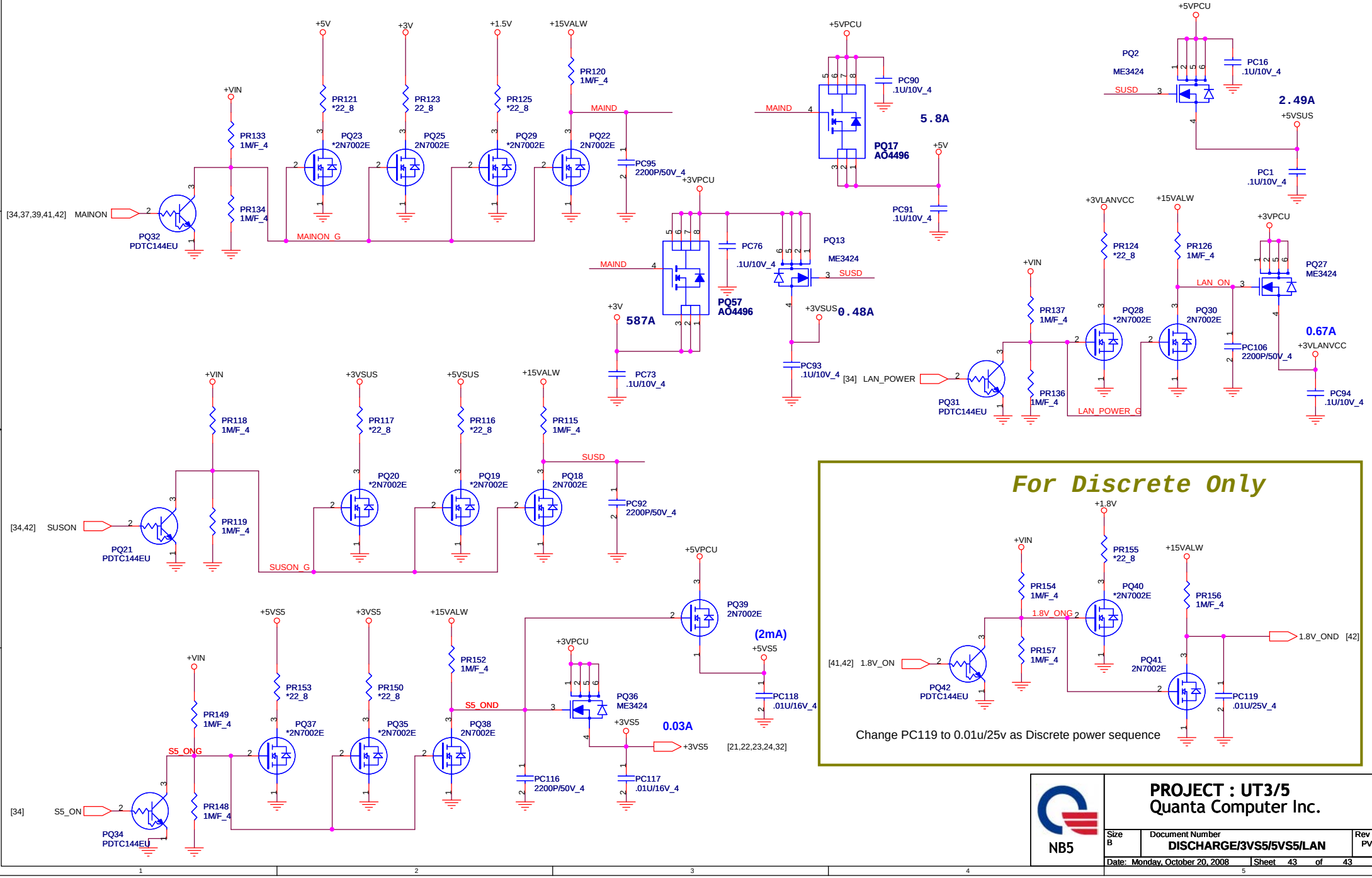
+5V
+3V
+1.5V
+15VALW
+VIN
PR121 *22_8
PR123 22_8
PR125 *22_8
PR120 1M/F_4
PR133 1M/F_4
PR134 1M/F_4
PQ23 *2N7002E
PQ25 2N7002E
PQ29 *2N7002E
PQ22 2N7002E
MAIND
PC95 2200P/50V_4
[34,37,39,41,42] MAINON
PQ32 PDTC144EU
MAINON_G
+5VPCU
PC90 .1U/10V_4
PQ17 AO4496
5.8A
PC91 .1U/10V_4
+3VPCU
PC76 .1U/10V_4
PQ13 ME3424
SUSD
PQ57 AO4496
587A
PC73 .1U/10V_4
+3VSUS
0.48A
PC93 .1U/10V_4
PQ2 ME3424
PC16 .1U/10V_4
2.49A
PC1 .1U/10V_4
+3VLANVCC
+15VALW
PR124 *22_8
PR126 1M/F_4
PR137 1M/F_4
PR136 1M/F_4
PQ28 *2N7002E
PQ30 2N7002E
PQ27 ME3424
LAN_ON
PC106 2200P/50V_4
0.67A
PC94 .1U/10V_4
[34] LAN_POWER
PQ31 PDTC144EU
LAN_POWER_G
+3VSUS
+5VSUS
PR118 1M/F_4
PR117 *22_8
PR116 *22_8
PR115 1M/F_4
PR119 1M/F_4
PQ20 *2N7002E
PQ19 *2N7002E
PQ18 2N7002E
SUSD
PC92 2200P/50V_4
[34,42] SUSON
PQ21 PDTC144EU
SUSON_G
PQ39 2N7002E
(2mA)
PC118 .01U/16V_4
+5VS5
+3VS5
+15VALW
PR152 1M/F_4
PR153 *22_8
PR150 *22_8
PR149 1M/F_4
PR148 1M/F_4
PQ37 *2N7002E
PQ35 *2N7002E
PQ38 2N7002E
S5_OND
S5_ONG
PQ36 ME3424
0.03A
PC116 2200P/50V_4
PC117 .01U/16V_4
[34] S5_ON
PQ34 PDTC144EU
[21,22,23,24,32]
For Discrete Only
+1.8V
PR155 *22_8
PR154 1M/F_4
PR157 1M/F_4
PR156 1M/F_4
1.8V_ONG
PQ40 *2N7002E
PQ41 2N7002E
PC119 .01U/25V_4
1.8V_OND [42]
[41,42] 1.8V_ON
PQ42 PDTC144EU
Change PC119 to 0.01u/25v as Discrete power sequence
NB5
PROJECT : UT3/5
Quanta Computer Inc.
Size B
Document Number
DISCHARGE/3VS5/5VS5/LAN
Rev PV
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