SP7(Nikita) BLOCK DIAGRAM PV

01

PCB STACK UP

12L Dis.

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(High)
LAYER 5 : SGND
LAYER 6 : IN3(High)
LAYER 7 : SVCC1
LAYER 8 : SVCC2
LAYER 9 : IN4
LAYER10 : IN5(High)
LAYER11 : GND
LAYER12 : BOT

A Channel
DDR3-SODIMM1
DDR3-SODIMM2
PAGE 13,14

DDR3 800,1066,1333 MT/s

B Channel
DDR3-SODIMM3
DDR3-SODIMM4
PAGE 15,16

DDR3 800,1066,1333 MT/s

Intel Clarksfield
CPU 45Watt
4 Core
(rPGA 989)
PAGE 3-6

PCI-Express Gen2 X8

PCI-Express Gen2 X1

VRAM DDR3*8 (1Gb) PAGE 23-24

ATI M97/Broadway/Madison (128bit)
(FCBGA)
962p 29X29mm
PAGE 18-22

27MHz

Dual Channel LVDS

HDMI CON (1920*1200) PAGE 25

LCD CONN for dual channel (15.6") PAGE 25

USB3.0 Port x2 PAGE 26

NEC USB3.0 Controller PAGE 26

DMI*4

BCLK133M
DMI100M
DP120M

32.768KHz

100M PCIE

133M BCLK
100M PCIE
96M DOT
REF CLK

14.318MHz

CLOCK GEN 9LRS3197 PAGE 02

PCH 3.5Watt
Platform Controller Hub
PAGE 7-12

ONFI

Braiwood (NAND Flash Memory) PAGE 34

CPU THERMAL SENSOR PAGE 27

32.768KHz

SATA 2.5" HDD
SATA 1.8" SSD1
PAGE 30

SATA0 150MB

SATA 1.8" SSD2 PAGE 30

SATA1 150MB

E-SATA(USB2.0) PAGE 26

SATA2 150MB

USB2.0 48M

6,7 USB2.0 Port X2 PAGE 26

5 BlueTooth PAGE 31

4 Webcam w/ Mic PAGE 31

3

2 Card Reader
Realtek
RTS5159
PAGE 30

2-in-1 flash media slot(SD/MMC) PAGE 30

Accelerometer
LIS3LV02DL PAGE 31

SMBUS

32.768KHz

LPC

PCI-E 100M

Azalia

X1 LAN
Atheros
PCIE-LAN
AR8131(M)
GigaLAN
PAGE 32

25MHz

RJ45 PAGE 32

X1 half size mini-card
(Wireless LAN
Shirley Peak
802.11a/b/g/n)
PAGE 34

Keyboard Touch Pad
Light Sensor
PAGE 31

GMT G9931P1U
SYSTEM/VGA FAN
PAGE 27

SPI
(SYSTEM BIOS)
PAGE 33

ENE KBC
KB3926 C2
PAGE 33

Audio
IDT92HD75B2
PAGE 28

AUDIO Amplifier TPA6047A4
PAGE 29

Internal Micophones (MEMs)
PAGE 31

Combo Jack (Headphone/MIC)
PAGE 28

Jack to Speaker
PAGE 29

BATTERY SELECTOR PAGE 42
SYSTEM CHARGER(BQ24704) PAGE 41
SYSTEM POWER ISL6237IRZ-T PAGE 35
DDR III SMDDR_VTERM 1.8V/1.8VSUS(VT356/VT357) PAGE 39
VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 36
VGACORE RT8208 PAGE 38
CPU CORE VT1312M/VT1317 PAGE 37

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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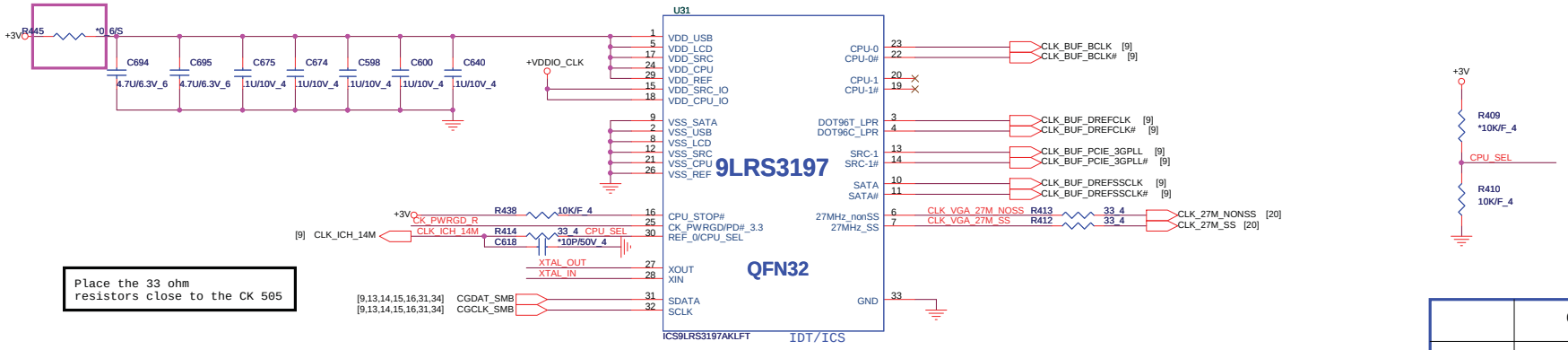
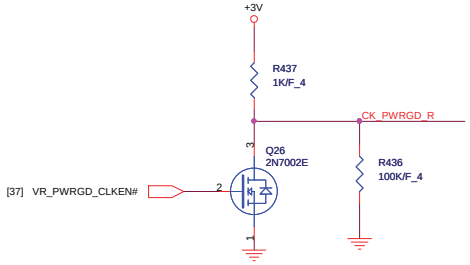
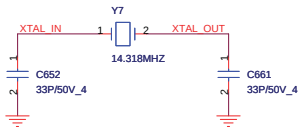
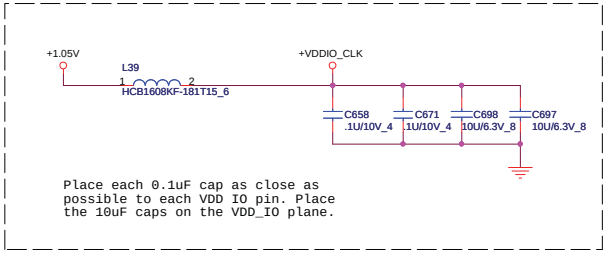


Place the 33 ohm resistors close to the CK 505

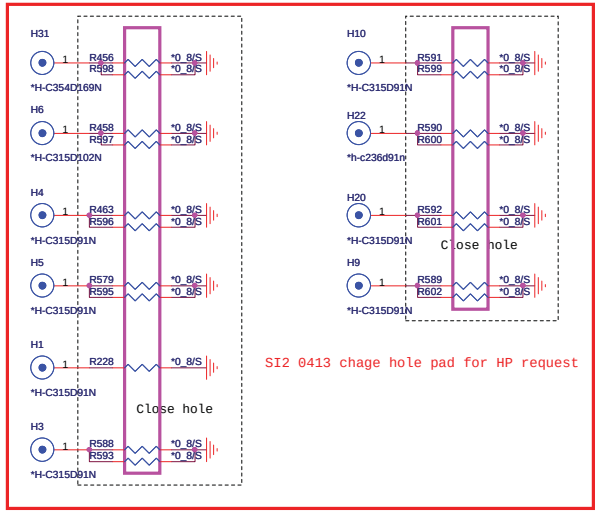
	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz



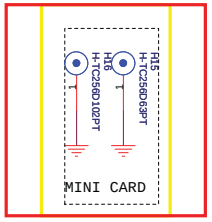




M/B Screw Hole



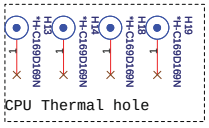
MINI CARD



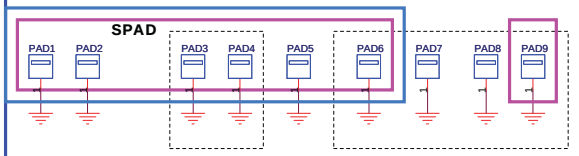
SI 0223 change footprint

SI2 0413 change BOM

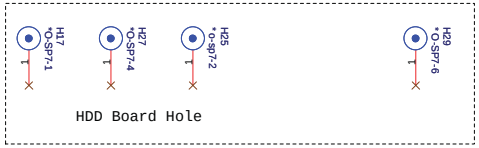
CPU Thermal hole

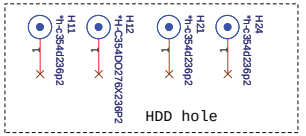


PV 0605 MODIFY PV 0605 MODIFY



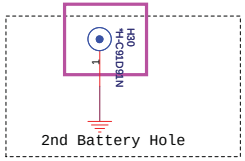
PV-2 0702 MODIFY



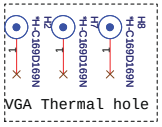


2nd Battery Hole

PV 0605 MODIFY



VGA Thermal hole



[3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[7,8,9,11,26,27,36,37] +1.05V

NB5	PROJECT : SP7 Quanta Computer Inc.		
	Size: Custom	Document Number: CLOCK & Screw Holes	Rev: 1A
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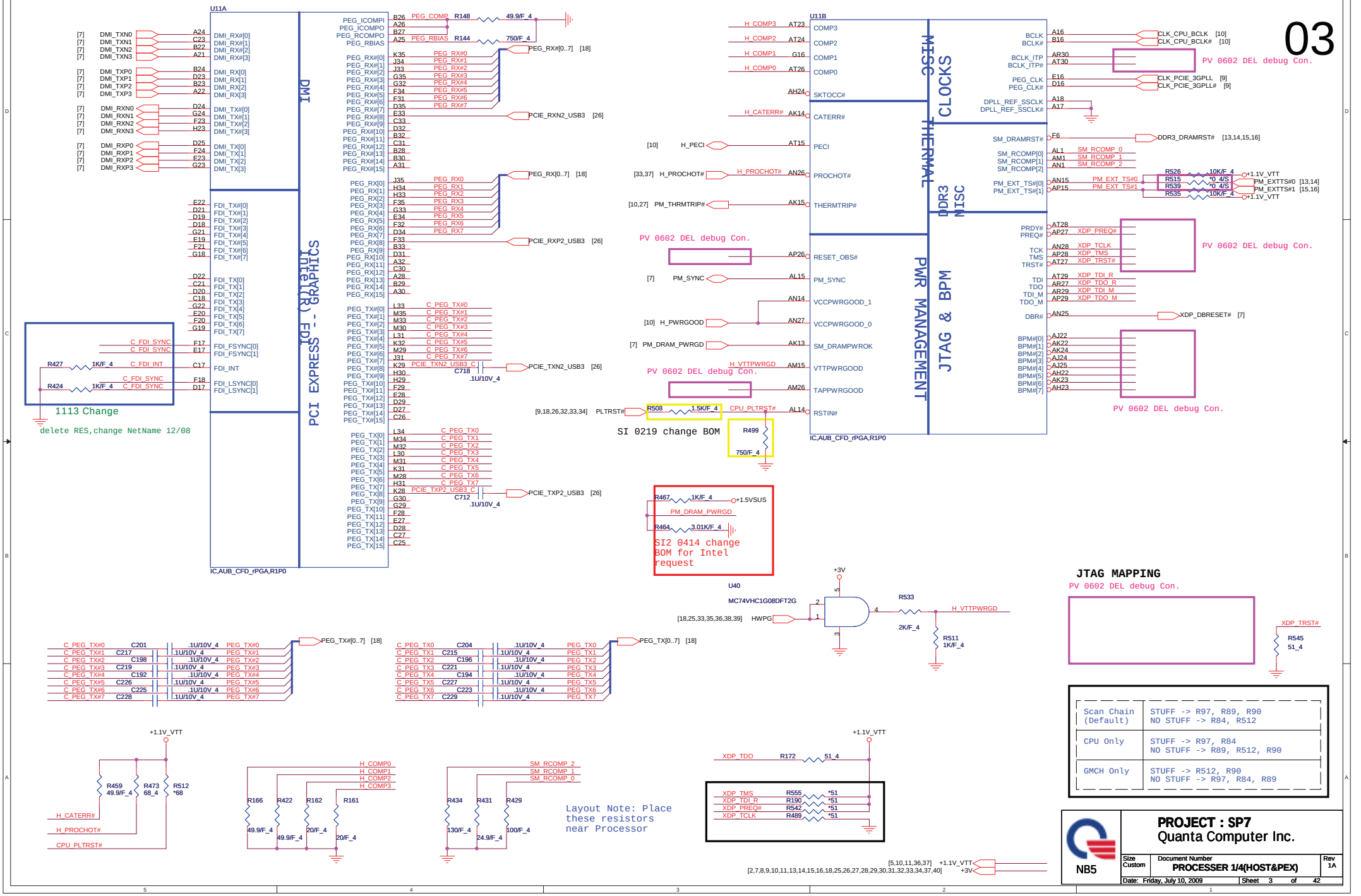
03
U11A
DMI_RX#[0]
DMI_RX#[1]
DMI_RX#[2]
DMI_RX#[3]
DMI_RX[0]
DMI_RX[1]
DMI_RX[2]
DMI_RX[3]
DMI_TX#[0]
DMI_TX#[1]
DMI_TX#[2]
DMI_TX#[3]
DMI_TX[0]
DMI_TX[1]
DMI_TX[2]
DMI_TX[3]
DMI
PCI EXPRESS - GRAPHICS
Intel(R) FDI
FDI_TX#[0]
FDI_TX#[1]
FDI_TX#[2]
FDI_TX#[3]
FDI_TX#[4]
FDI_TX#[5]
FDI_TX#[6]
FDI_TX#[7]
FDI_TX[0]
FDI_TX[1]
FDI_TX[2]
FDI_TX[3]
FDI_TX[4]
FDI_TX[5]
FDI_TX[6]
FDI_TX[7]
C_FDI_SYNC
C_FDI_SYNC
FDI_FSYNC[0]
FDI_FSYNC[1]
R427 1K/F_4 C_FDI_INT
FDI_INT
C_FDI_SYNC
R424 1K/F_4 C_FDI_SYNC
FDI_LSYNC[0]
FDI_LSYNC[1]
1113 Change
delete RES,change NetName 12/08
IC,AUB_CFD_rPGA,R1P0
PEG_ICOMPI
PEG_ICOMPO
PEG_RCOMPO
PEG_RBIAS
PEG_COMP R148 49.9/F_4
PEG_RBIAS R144 750/F_4
PEG_RX#[0..7] [18]
PEG_RX#[0]
PEG_RX#[1]
PEG_RX#[2]
PEG_RX#[3]
PEG_RX#[4]
PEG_RX#[5]
PEG_RX#[6]
PEG_RX#[7]
PEG_RX#[8]
PEG_RX#[9]
PEG_RX#[10]
PEG_RX#[11]
PEG_RX#[12]
PEG_RX#[13]
PEG_RX#[14]
PEG_RX#[15]
PCIE_RXN2_USB3 [26]
PEG_RX[0..7] [18]
PEG_RX[0]
PEG_RX[1]
PEG_RX[2]
PEG_RX[3]
PEG_RX[4]
PEG_RX[5]
PEG_RX[6]
PEG_RX[7]
PEG_RX[8]
PEG_RX[9]
PEG_RX[10]
PEG_RX[11]
PEG_RX[12]
PEG_RX[13]
PEG_RX[14]
PEG_RX[15]
PCIE_RXP2_USB3 [26]
PEG_TX#[0]
PEG_TX#[1]
PEG_TX#[2]
PEG_TX#[3]
PEG_TX#[4]
PEG_TX#[5]
PEG_TX#[6]
PEG_TX#[7]
PEG_TX#[8]
PEG_TX#[9]
PEG_TX#[10]
PEG_TX#[11]
PEG_TX#[12]
PEG_TX#[13]
PEG_TX#[14]
PEG_TX#[15]
C_PEG_TX#0
C_PEG_TX#1
C_PEG_TX#2
C_PEG_TX#3
C_PEG_TX#4
C_PEG_TX#5
C_PEG_TX#6
C_PEG_TX#7
PCIE_TXN2_USB3_C
C718 .1U/10V_4
PCIE_TXN2_USB3 [26]
PEG_TX[0]
PEG_TX[1]
PEG_TX[2]
PEG_TX[3]
PEG_TX[4]
PEG_TX[5]
PEG_TX[6]
PEG_TX[7]
PEG_TX[8]
PEG_TX[9]
PEG_TX[10]
PEG_TX[11]
PEG_TX[12]
PEG_TX[13]
PEG_TX[14]
PEG_TX[15]
C_PEG_TX0
C_PEG_TX1
C_PEG_TX2
C_PEG_TX3
C_PEG_TX4
C_PEG_TX5
C_PEG_TX6
C_PEG_TX7
PCIE_TXP2_USB3_C
C712 .1U/10V_4
PCIE_TXP2_USB3 [26]
U11B
MISC
CLOCKS
THERMAL
DDR3 MISC
JTAG & BPM
PWR MANAGEMENT
H_COMP3 AT23 COMP3
H_COMP2 AT24 COMP2
H_COMP1 G16 COMP1
H_COMP0 AT26 COMP0
AH24 SKTOCC#
H_CATERR# AK14 CATERR#
[10] H_PECI AT15 PECI
[33,37] H_PROCHOT# H_PROCHOT# AN26 PROCHOT#
[10,27] PM_THRMTRIP# AK15 THERMTRIP#
PV 0602 DEL debug Con.
AP26 RESET_OBS#
[7] PM_SYNC AL15 PM_SYNC
AN14 VCCPWRGOOD_1
[10] H_PWRGOOD AN27 VCCPWRGOOD_0
[7] PM_DRAM_PWRGD AK13 SM_DRAMPWROK
H_VTTPWRGD AM15 VTTPWRGOOD
PV 0602 DEL debug Con.
AM26 TAPPWRGOOD
[9,18,26,32,33,34] PLTRST# R508 1.5K/F_4 CPU_PLTRST# AL14 RSTIN#
SI 0219 change BOM
R499 750/F_4
IC,AUB_CFD_rPGA,R1P0
BCLK A16
BCLK# B16
CLK_CPU_BCLK [10]
CLK_CPU_BCLK# [10]
BCLK_ITP AR30
BCLK_ITP# AT30
PV 0602 DEL debug Con.
PEG_CLK E16
PEG_CLK# D16
CLK_PCIE_3GPLL [9]
CLK_PCIE_3GPLL# [9]
DPLL_REF_SSCLK A18
DPLL_REF_SSCLK# A17
SM_DRAMRST# F6
DDR3_DRAMRST# [13,14,15,16]
SM_RCOMP[0] AL1 SM_RCOMP_0
SM_RCOMP[1] AM1 SM_RCOMP_1
SM_RCOMP[2] AN1 SM_RCOMP_2
PM_EXT_TS#[0] AN15 PM_EXT_TS#0
PM_EXT_TS#[1] AP15 PM_EXT_TS#1
R526 10K/F_4 +1.1V_VTT
R515 *0_4/S PM_EXTTS#0 [13,14]
R539 *0_4/S PM_EXTTS#1 [15,16]
R535 10K/F_4 +1.1V_VTT
PRDY# AT28
PREQ# AP27 XDP_PREQ#
TCK AN28 XDP_TCLK
TMS AP28 XDP_TMS
TRST# AT27 XDP_TRST#
TDI AT29 XDP_TDI_R
TDO AR27 XDP_TDO_R
TDI_M AR29 XDP_TDI_M
TDO_M AP29 XDP_TDO_M
PV 0602 DEL debug Con.
DBR# AN25 XDP_DBRESET# [7]
BPM#[0] AJ22
BPM#[1] AK22
BPM#[2] AK24
BPM#[3] AJ24
BPM#[4] AJ25
BPM#[5] AH22
BPM#[6] AK23
BPM#[7] AH23
PV 0602 DEL debug Con.
R467 1K/F_4 +1.5VSUS
PM_DRAM_PWRGD
R464 3.01K/F_4
SI2 0414 change BOM for Intel request
U40
MC74VHC1G08DFT2G
[18,25,33,35,36,38,39] HWPG
+3V
R533 2K/F_4
H_VTTPWRGD
R511 1K/F_4
JTAG MAPPING
PV 0602 DEL debug Con.
XDP_TRST#
R545 51_4
C_PEG_TX#0 C201 .1U/10V_4 PEG_TX#0
C_PEG_TX#1 C217 .1U/10V_4 PEG_TX#1
C_PEG_TX#2 C198 .1U/10V_4 PEG_TX#2
C_PEG_TX#3 C219 .1U/10V_4 PEG_TX#3
C_PEG_TX#4 C192 .1U/10V_4 PEG_TX#4
C_PEG_TX#5 C226 .1U/10V_4 PEG_TX#5
C_PEG_TX#6 C225 .1U/10V_4 PEG_TX#6
C_PEG_TX#7 C228 .1U/10V_4 PEG_TX#7
PEG_TX#[0..7] [18]
C_PEG_TX0 C204 .1U/10V_4 PEG_TX0
C_PEG_TX1 C215 .1U/10V_4 PEG_TX1
C_PEG_TX2 C196 .1U/10V_4 PEG_TX2
C_PEG_TX3 C221 .1U/10V_4 PEG_TX3
C_PEG_TX4 C194 .1U/10V_4 PEG_TX4
C_PEG_TX5 C227 .1U/10V_4 PEG_TX5
C_PEG_TX6 C223 .1U/10V_4 PEG_TX6
C_PEG_TX7 C229 .1U/10V_4 PEG_TX7
PEG_TX[0..7] [18]
+1.1V_VTT
R459 49.9/F_4
R473 68_4
R512 *68
H_CATERR#
H_PROCHOT#
CPU_PLTRST#
H_COMP0
H_COMP1
H_COMP2
H_COMP3
R166 49.9/F_4
R422 49.9/F_4
R162 20/F_4
R161 20/F_4
SM_RCOMP_2
SM_RCOMP_1
SM_RCOMP_0
R434 130/F_4
R431 24.9/F_4
R429 100/F_4
Layout Note: Place these resistors near Processor
+1.1V_VTT
XDP_TDO R172 51_4
XDP_TMS R555 *51
XDP_TDI_R R190 *51
XDP_PREQ# R542 *51
XDP_TCLK R489 *51
[5,10,11,36,37] +1.1V_VTT
[2,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V
Scan Chain (Default) | STUFF -> R97, R89, R90 NO STUFF -> R84, R512
CPU Only | STUFF -> R97, R84 NO STUFF -> R89, R512, R90
GMCH Only | STUFF -> R512, R90 NO STUFF -> R97, R84, R89
NB5
PROJECT : SP7
Quanta Computer Inc.
Size Custom
Document Number PROCESSER 1/4(HOST&PEX)
Rev 1A
Date: Friday, July 10, 2009
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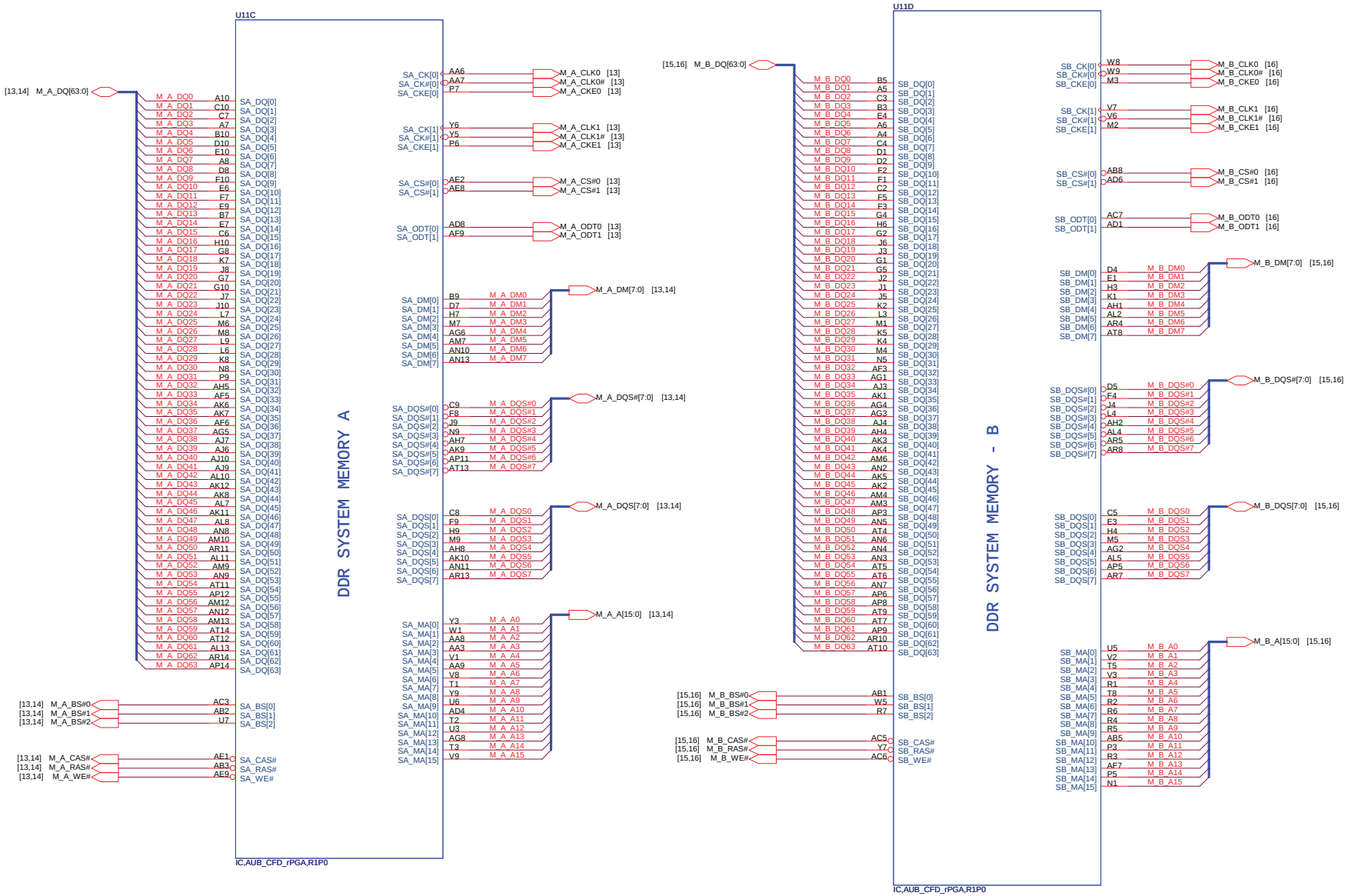
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

04



PROJECT : SP7	
Quanta Computer Inc.	
NB5	Size: Custom
Document Number: PROCESSER 2/4(DDR)	Rev: 1A
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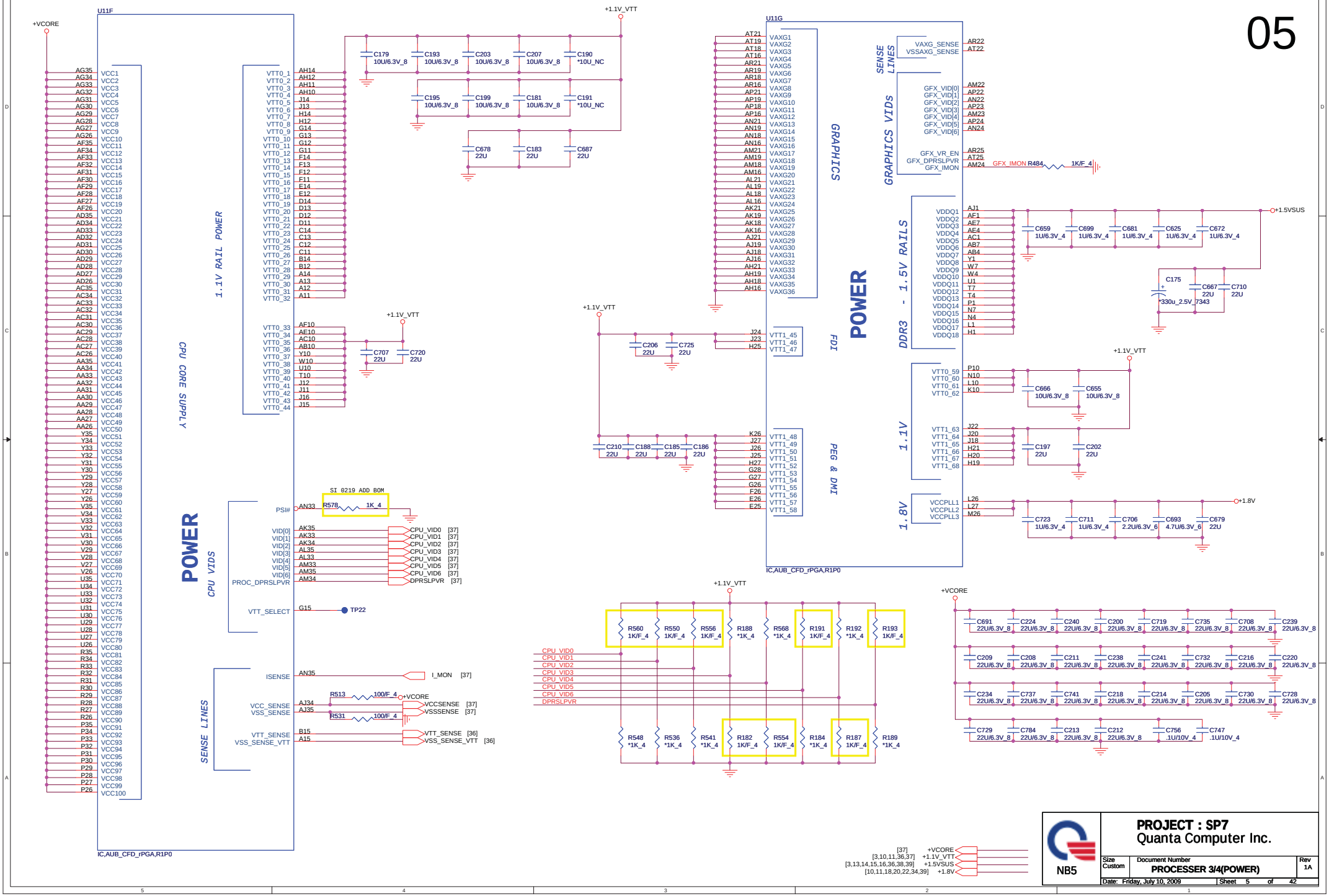
05
U11F
U11G
POWER
CPU CORE SUPPLY
1.1V RAIL POWER
CPU VIDS
SENSE LINES
GRAPHICS
GRAPHICS VIDS
SENSE LINES
DDR3 - 1.5V RAILS
1.1V
1.8V
FDI
PEG & DMI
+VCORE
+1.1V_VTT
+1.5VSUS
+1.8V
SI 0219 ADD BOM
IC,AUB_CFD_rPGA,R1P0
PROJECT : SP7
Quanta Computer Inc.
NB5
PROCESSER 3/4(POWER)
Size Custom
Rev 1A
Date: Friday, July 10, 2009
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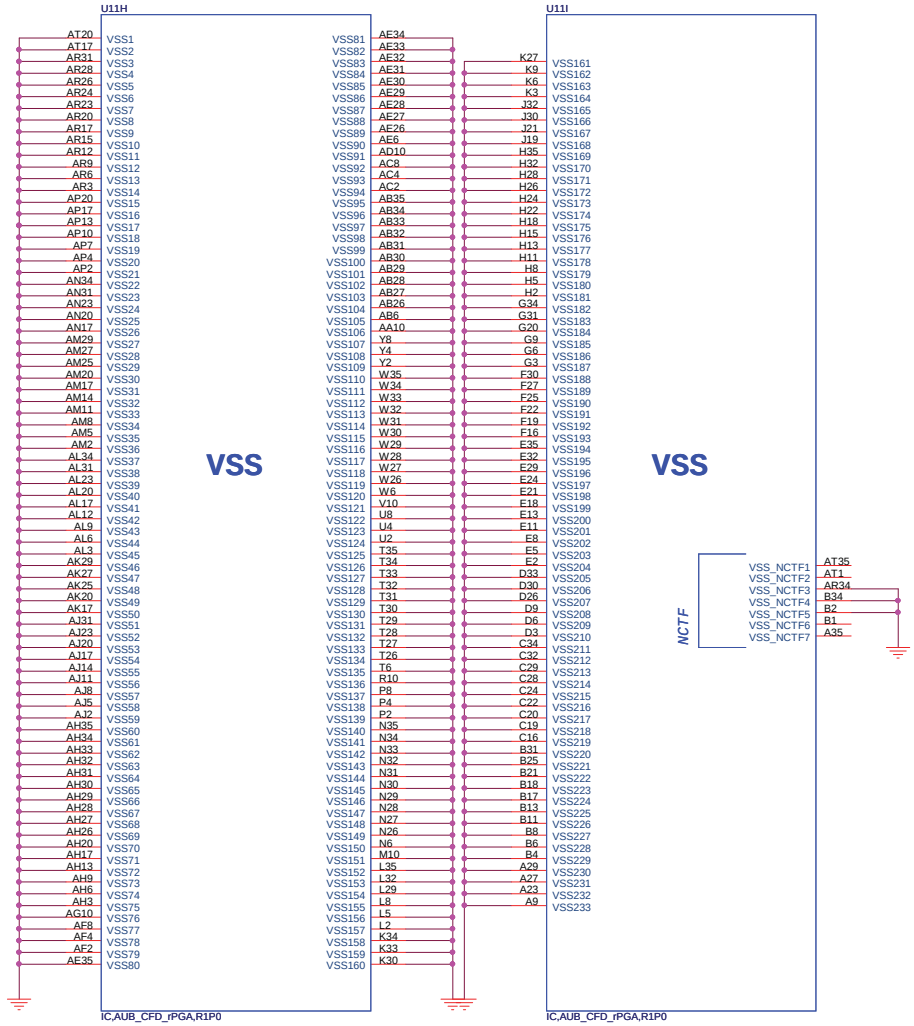
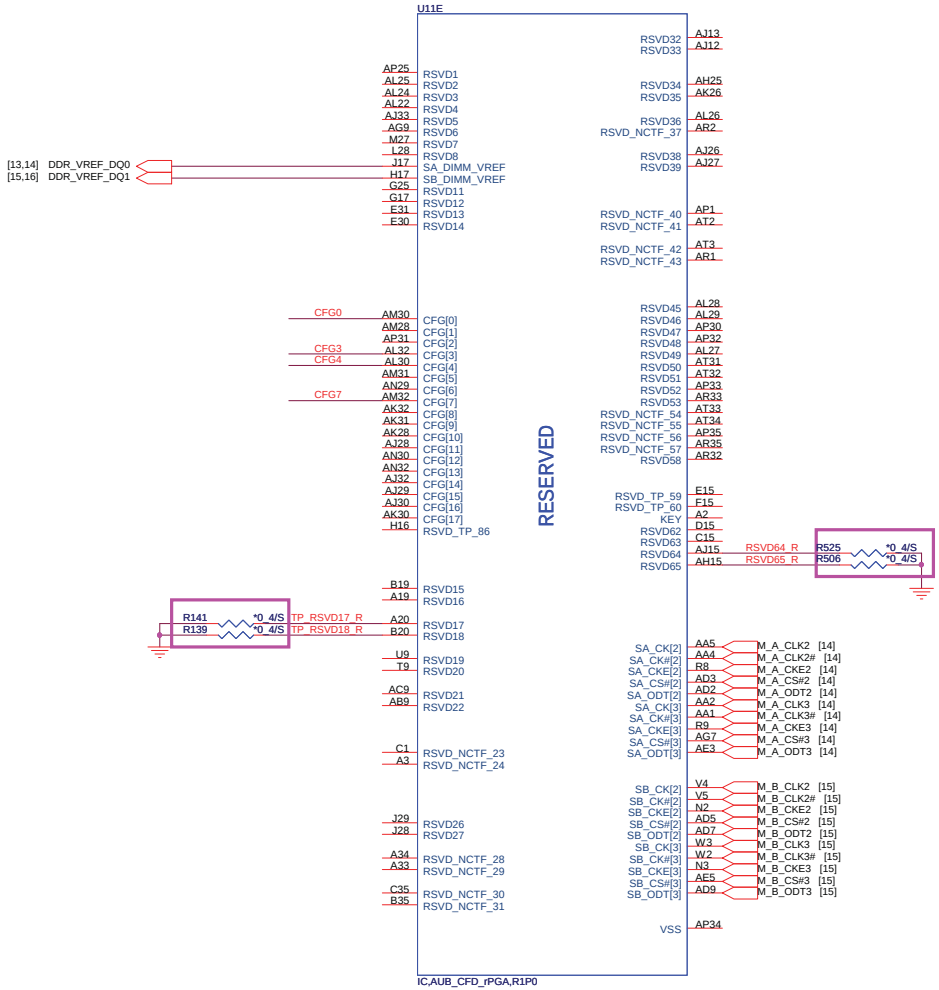
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



06

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

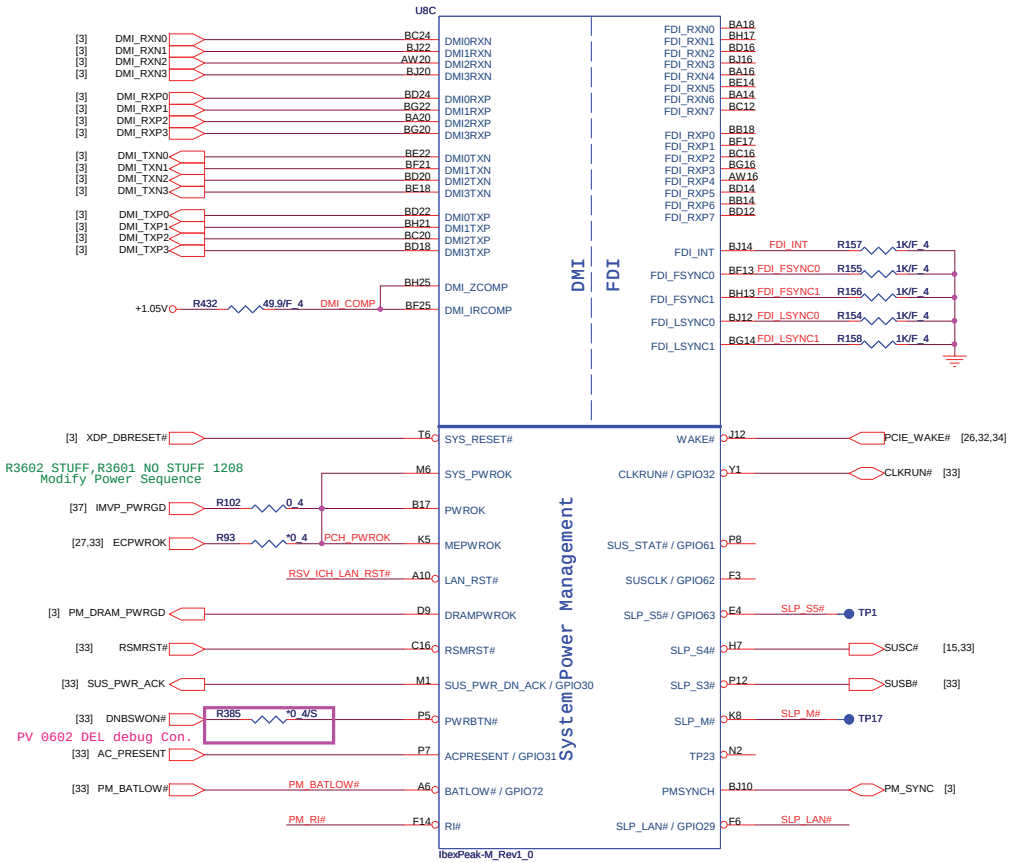
PROJECT : SP7
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PROCESSER 4/4(GND)	1A

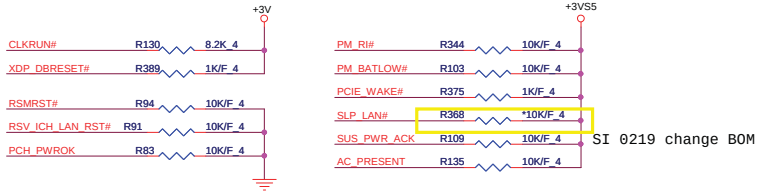
Date: Friday, July 10, 2009 | Sheet 6 of 42

IBEX PEAK-M (DMI,FDI,GPIO)



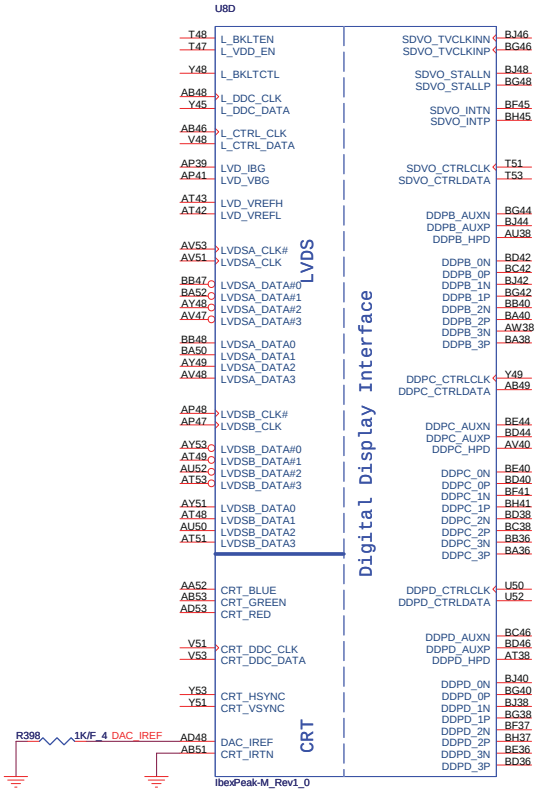
R3602 STUFF,R3601 NO STUFF 1208
Modify Power Sequence

PV 0602 DEL debug Con.



SI 0219 change BOM

IBEX PEAK-M (LVDS,DDI)

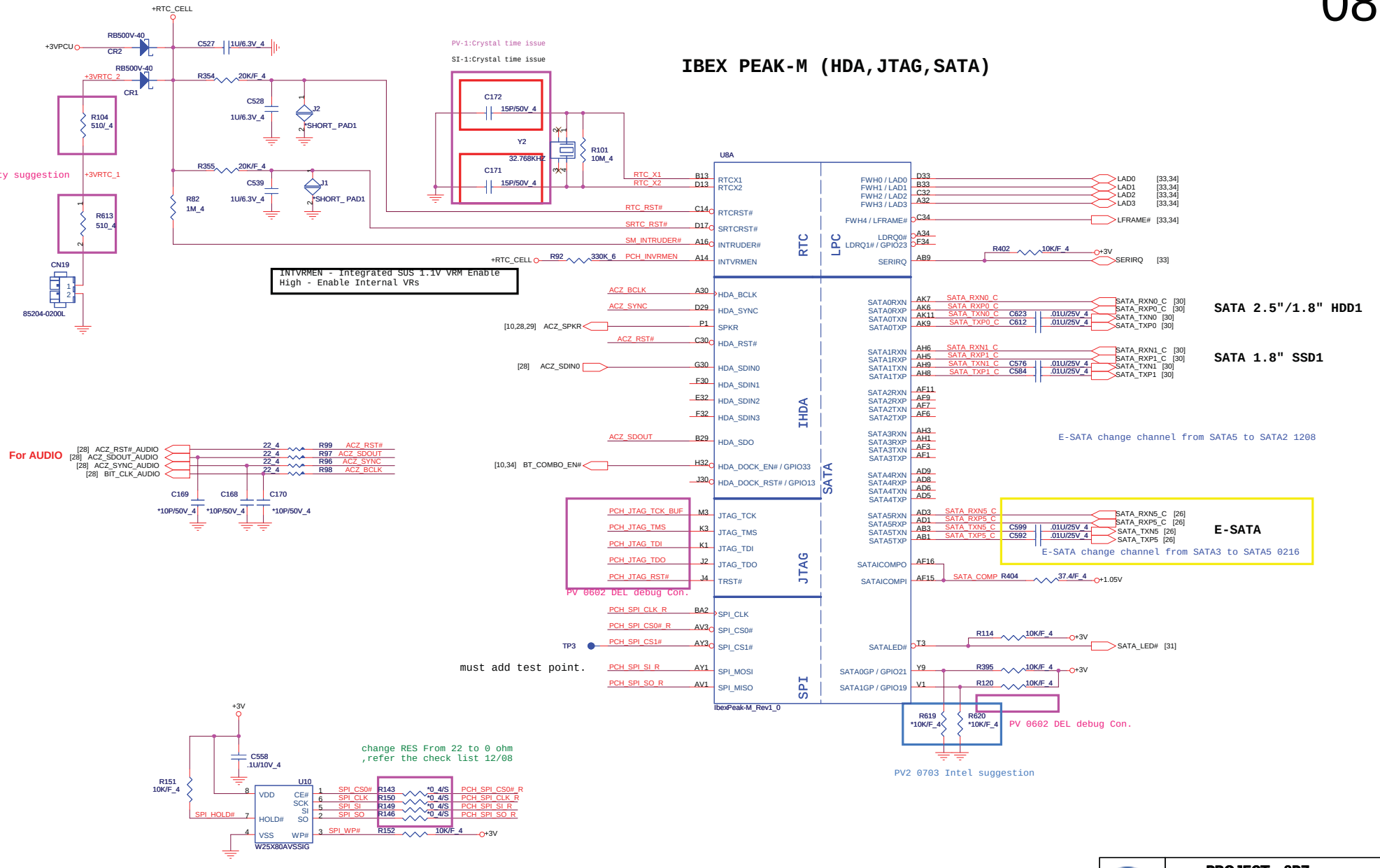


[2,8,9,11,26,27,36,37] +1.05V
[2,3,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[9,10,11,25,40] +3VS5

07

NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: PCH 1/6 (DMI,PM,VIDEO)	Rev: 1A
Date: Friday, July 10, 2009	Sheet 7 of 42	

IBEX PEAK-M (HDA,JTAG,SATA)



NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA,HDA,LPC)	1A
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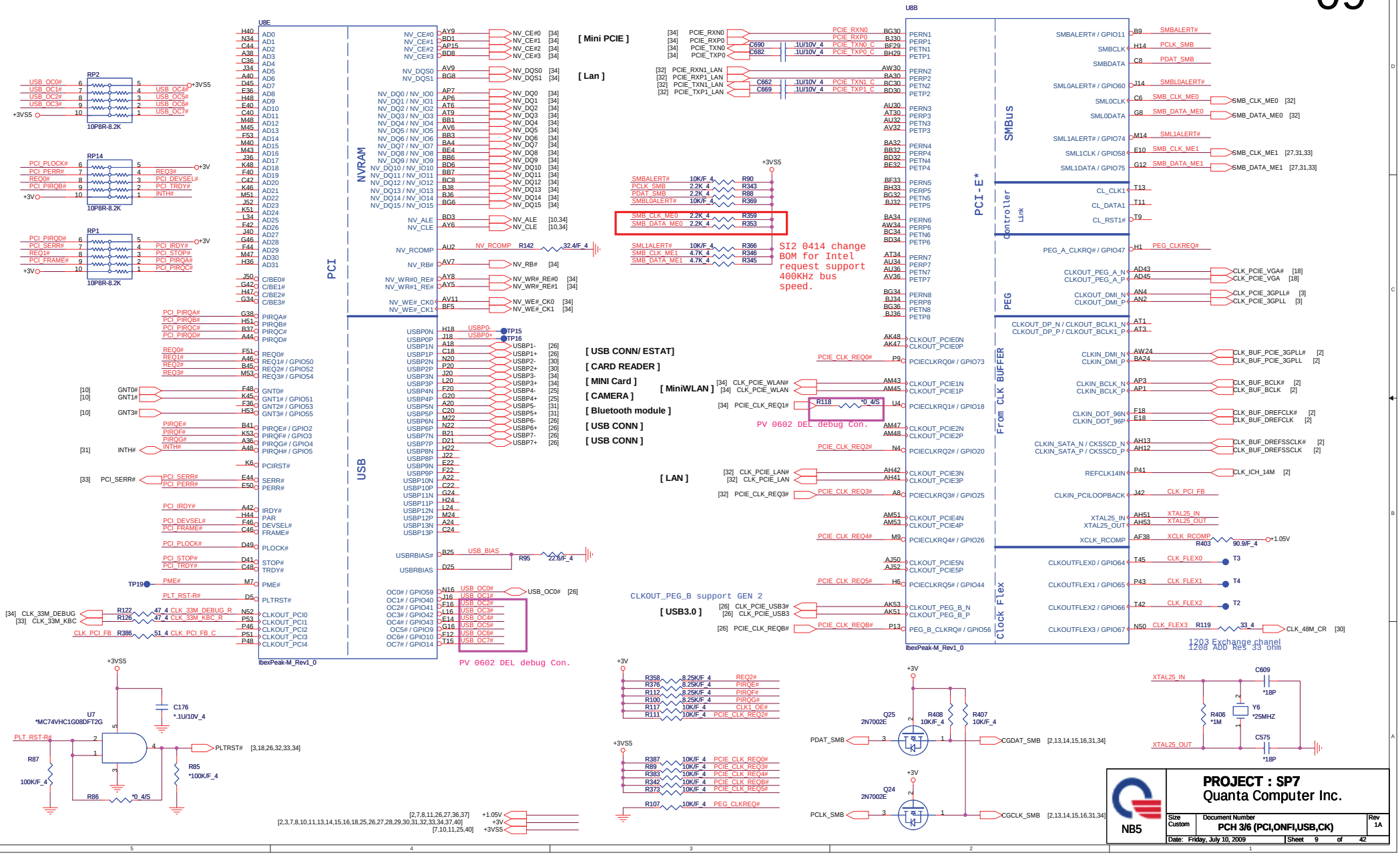
IBEX PEAK-M (PCI,USB,NVRAM)

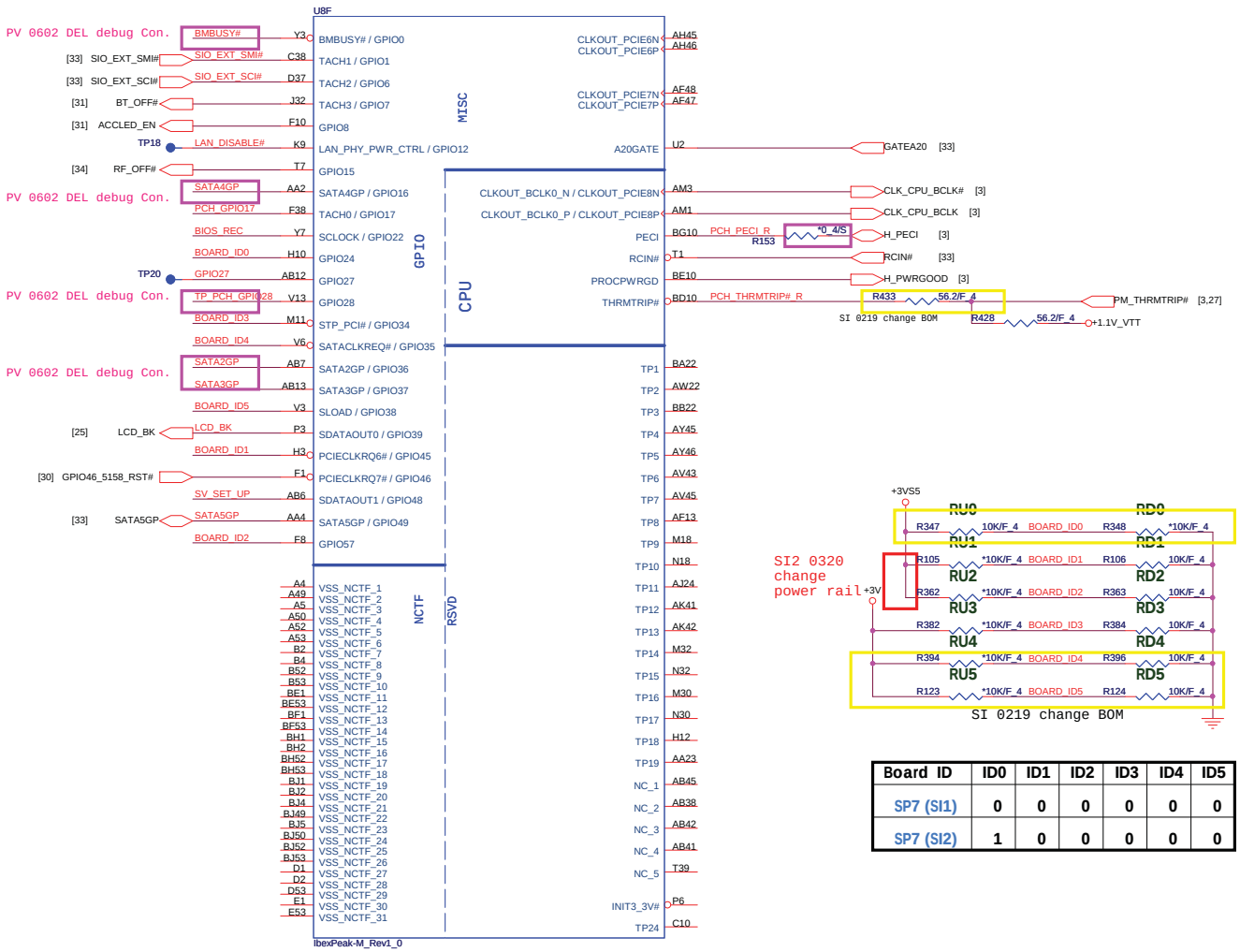
IBEX PEAK-M (PCI-E,SMBUS,CLK)

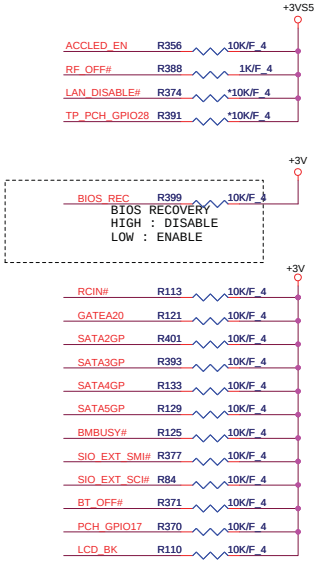
09



PROJECT : SP7	
Quanta Computer Inc.	
NB5	Size: Custom
Document Number: PCH 3/6 (PCI,ONFI,USB,CK)	Rev: 1A
Date: Friday, July 10, 2009	Sheet 9 of 42

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

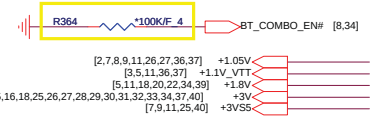


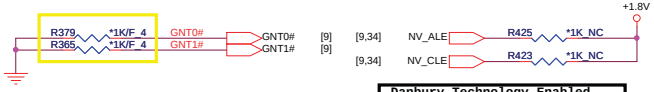


Board ID	ID0	ID1	ID2	ID3	ID4	ID5
SP7 (SI1)	0	0	0	0	0	0
SP7 (SI2)	1	0	0	0	0	0

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP	1-X High = Strong (Default)





Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO & Strap)	1A

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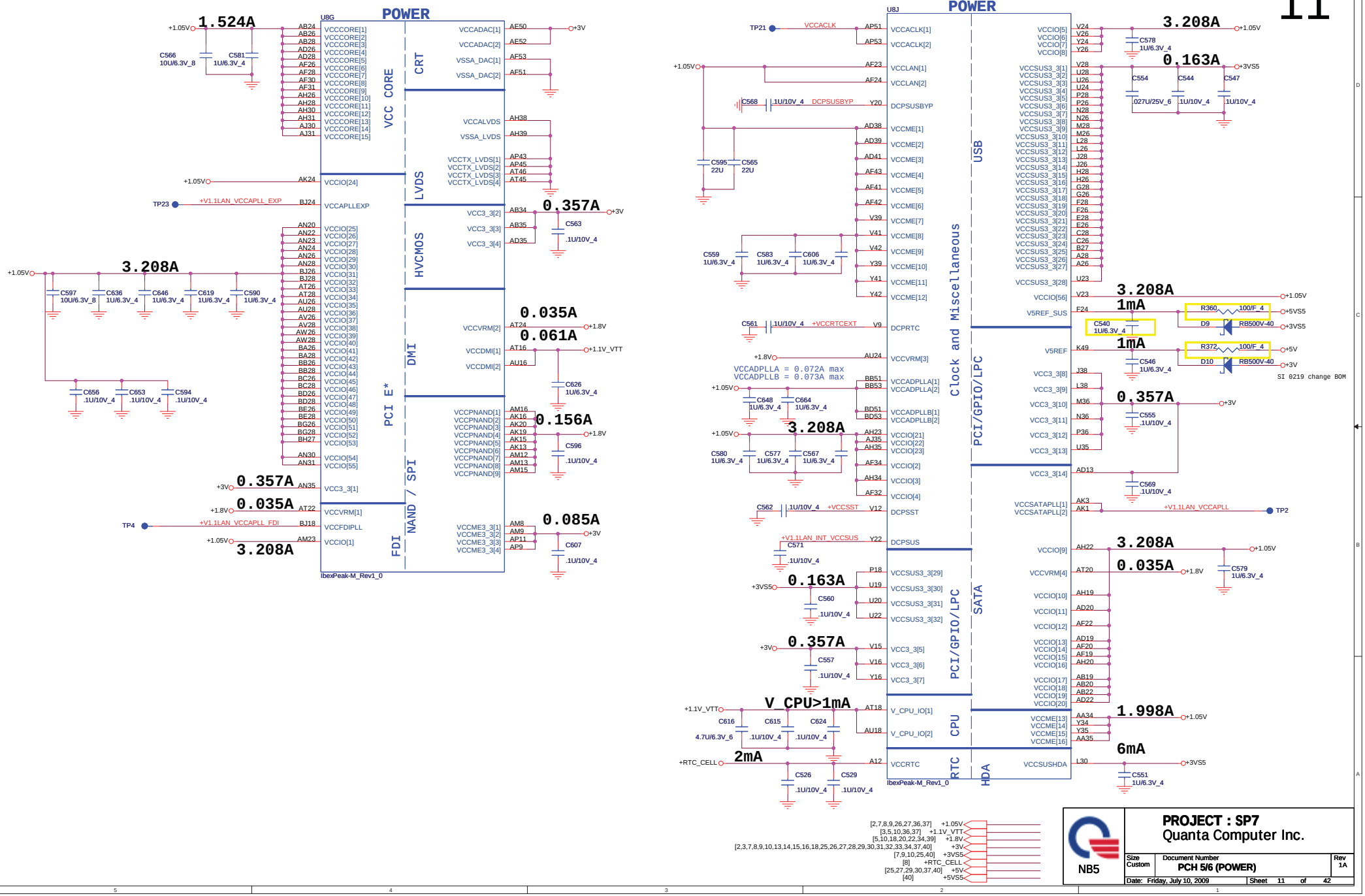
POWER
U8G
1.524A
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
VCCADAC[1]
VCCADAC[2]
VSSA_DAC[1]
VSSA_DAC[2]
VCCALVDS
VSSA_LVDS
VCCTX_LVDS[1]
VCCTX_LVDS[2]
VCCTX_LVDS[3]
VCCTX_LVDS[4]
VCC3_3[2]
VCC3_3[3]
VCC3_3[4]
0.357A
3.208A
0.035A
0.061A
0.156A
0.085A
VCCVRM[2]
VCCDMI[1]
VCCDMI[2]
VCCPNAND[1]
VCCPNAND[2]
VCCPNAND[3]
VCCPNAND[4]
VCCPNAND[5]
VCCPNAND[6]
VCCPNAND[7]
VCCPNAND[8]
VCCPNAND[9]
VCCME3_3[1]
VCCME3_3[2]
VCCME3_3[3]
VCCME3_3[4]
VCCRVRM[1]
VCCFDIPLL
VCCIO[1]
VCC3_3[1]
ibexPeak-M_Rev1_0
U8J
POWER
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
VCCACLK
VCCACLK[1]
VCCACLK[2]
VCCLAN[1]
VCCLAN[2]
DCPSUSBYP
VCCME[1]
VCCME[2]
VCCME[3]
VCCME[4]
VCCME[5]
VCCME[6]
VCCME[7]
VCCME[8]
VCCME[9]
VCCME[10]
VCCME[11]
VCCME[12]
DCPRTC
VCCVRM[3]
VCCADPLLA = 0.072A max
VCCADPLLB = 0.073A max
VCCADPLLA[1]
VCCADPLLA[2]
VCCADPLLB[1]
VCCADPLLB[2]
VCCIO[21]
VCCIO[22]
VCCIO[23]
VCCIO[2]
VCCIO[3]
VCCIO[4]
DCPSST
DCPSUS
VCCSUS3_3[29]
VCCSUS3_3[30]
VCCSUS3_3[31]
VCCSUS3_3[32]
VCC3_3[5]
VCC3_3[6]
VCC3_3[7]
V_CPU_IO[1]
V_CPU_IO[2]
VCCRTC
V_CPU>1mA
2mA
3.208A
0.163A
0.357A
1.998A
6mA
1mA
VCCIO[5]
VCCIO[6]
VCCIO[7]
VCCIO[8]
VCCSUS3_3[1]
VCCSUS3_3[2]
VCCSUS3_3[3]
VCCSUS3_3[4]
VCCSUS3_3[5]
VCCSUS3_3[6]
VCCSUS3_3[7]
VCCSUS3_3[8]
VCCSUS3_3[9]
VCCSUS3_3[10]
VCCSUS3_3[11]
VCCSUS3_3[12]
VCCSUS3_3[13]
VCCSUS3_3[14]
VCCSUS3_3[15]
VCCSUS3_3[16]
VCCSUS3_3[17]
VCCSUS3_3[18]
VCCSUS3_3[19]
VCCSUS3_3[20]
VCCSUS3_3[21]
VCCSUS3_3[22]
VCCSUS3_3[23]
VCCSUS3_3[24]
VCCSUS3_3[25]
VCCSUS3_3[26]
VCCSUS3_3[27]
VCCSUS3_3[28]
VCCIO[56]
V5REF_SUS
V5REF
VCC3_3[8]
VCC3_3[9]
VCC3_3[10]
VCC3_3[11]
VCC3_3[12]
VCC3_3[13]
VCC3_3[14]
VCCSATAPLL[1]
VCCSATAPLL[2]
VCCIO[9]
VCCVRM[4]
VCCIO[10]
VCCIO[11]
VCCIO[12]
VCCIO[13]
VCCIO[14]
VCCIO[15]
VCCIO[16]
VCCIO[17]
VCCIO[18]
VCCIO[19]
VCCIO[20]
VCCME[13]
VCCME[14]
VCCME[15]
VCCME[16]
VCCSUSHDA
R360
R372
D9
D10
RB500V-40
SI 0219 change BOM
ibexPeak-M_Rev1_0
[2,7,8,9,26,27,36,37] +1.05V
[3,5,10,36,37] +1.1V_VTT
[5,10,18,20,22,34,39] +1.8V
[2,3,7,8,9,10,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[7,9,10,25,40] +3VS5
[8] +RTC_CELL
[25,27,29,30,37,40] +5V
[40] +5VS
NB5
PROJECT : SP7
Quanta Computer Inc.
Size Custom
Document Number
PCH 5/6 (POWER)
Rev 1A
Date: Friday, July 10, 2009
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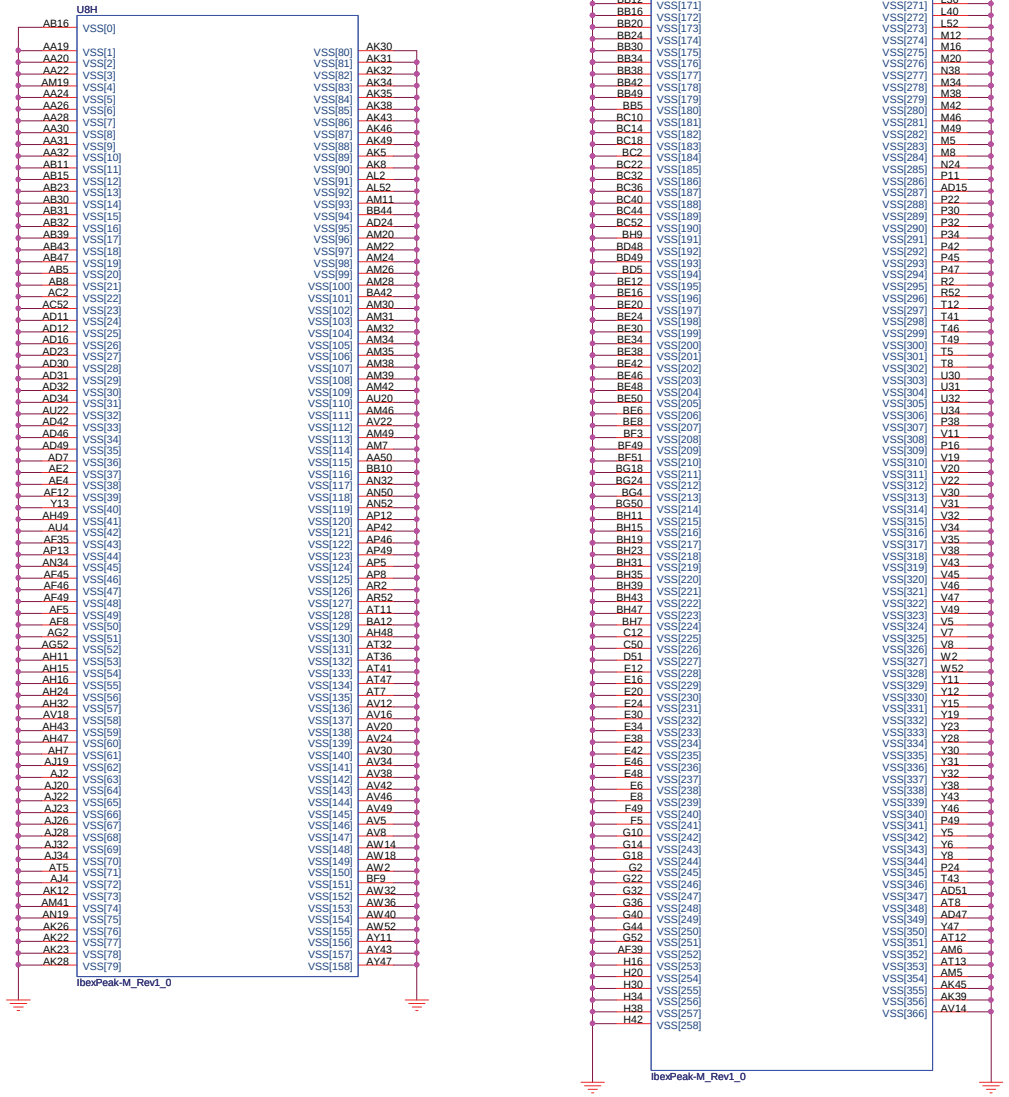
IBEX PEAK-M (GND)



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NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
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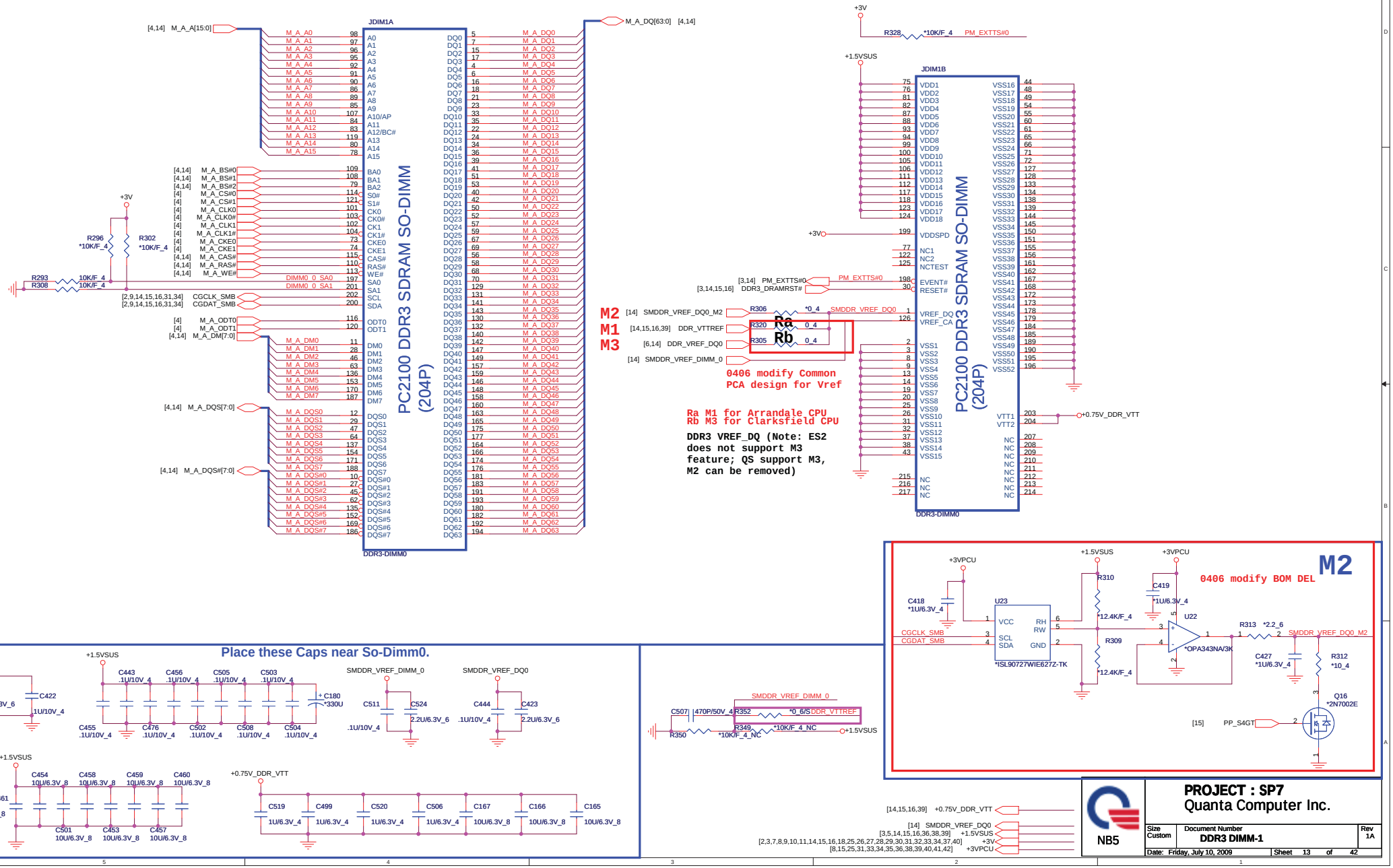
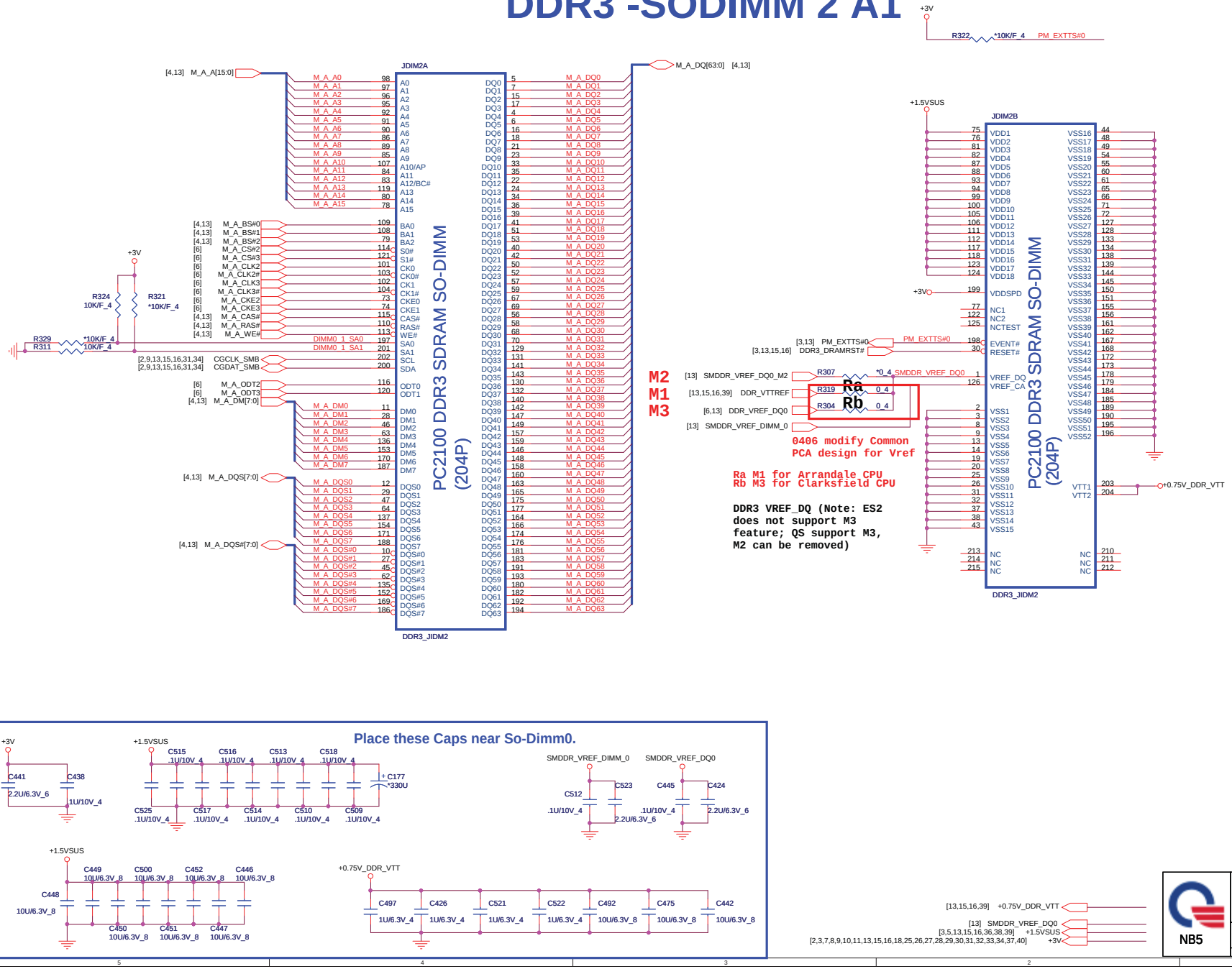
DDR3 -SODIMM 1 A0



DDR3 -SODIMM 2 A1



[13,15,16,39] +0.75V_DDR_VTT
[13] SMDDR_VREF_DQ0
[3,5,13,15,16,36,38,39] +1.5VSUS
[2,3,7,8,9,10,11,13,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-2	1A

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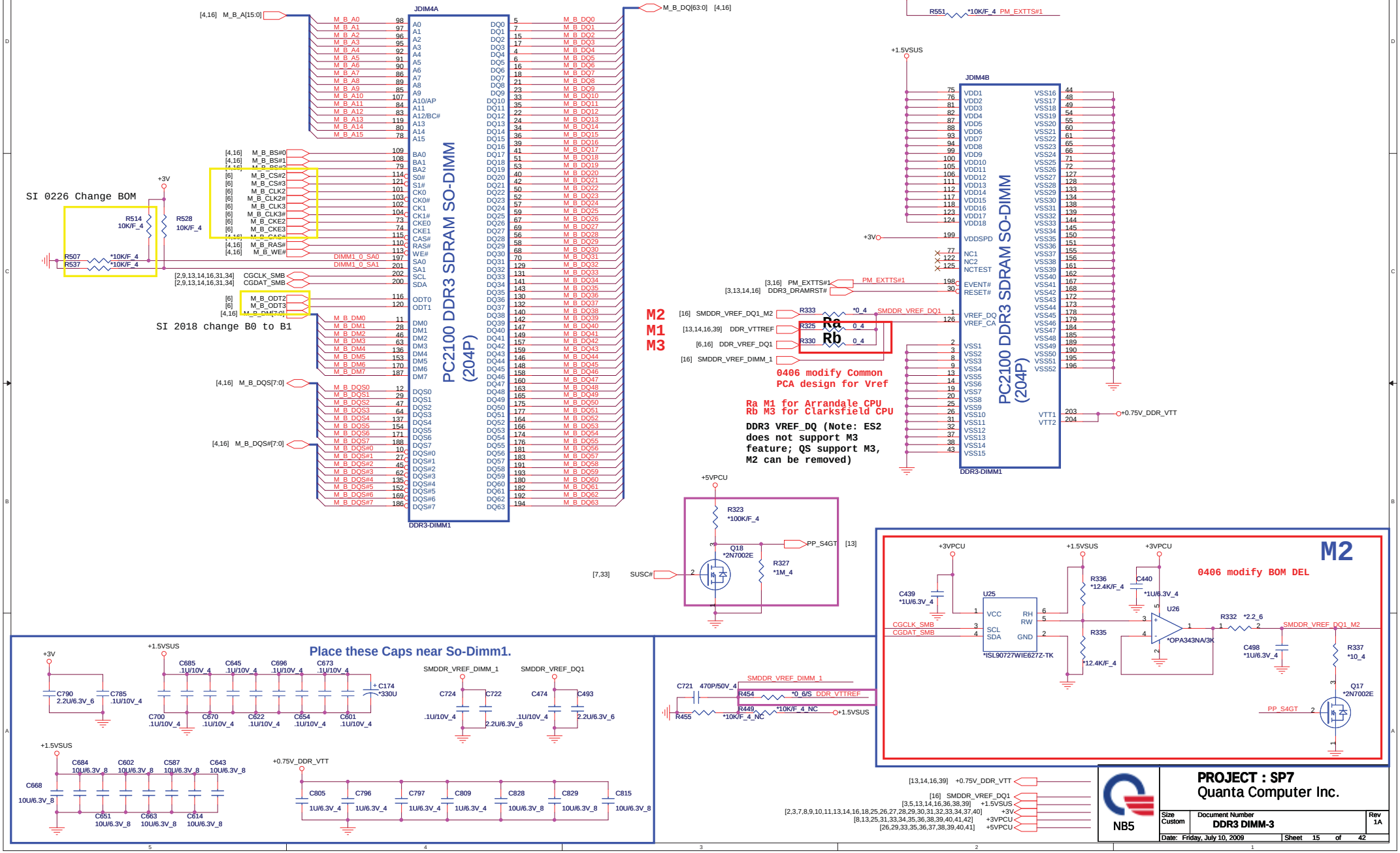
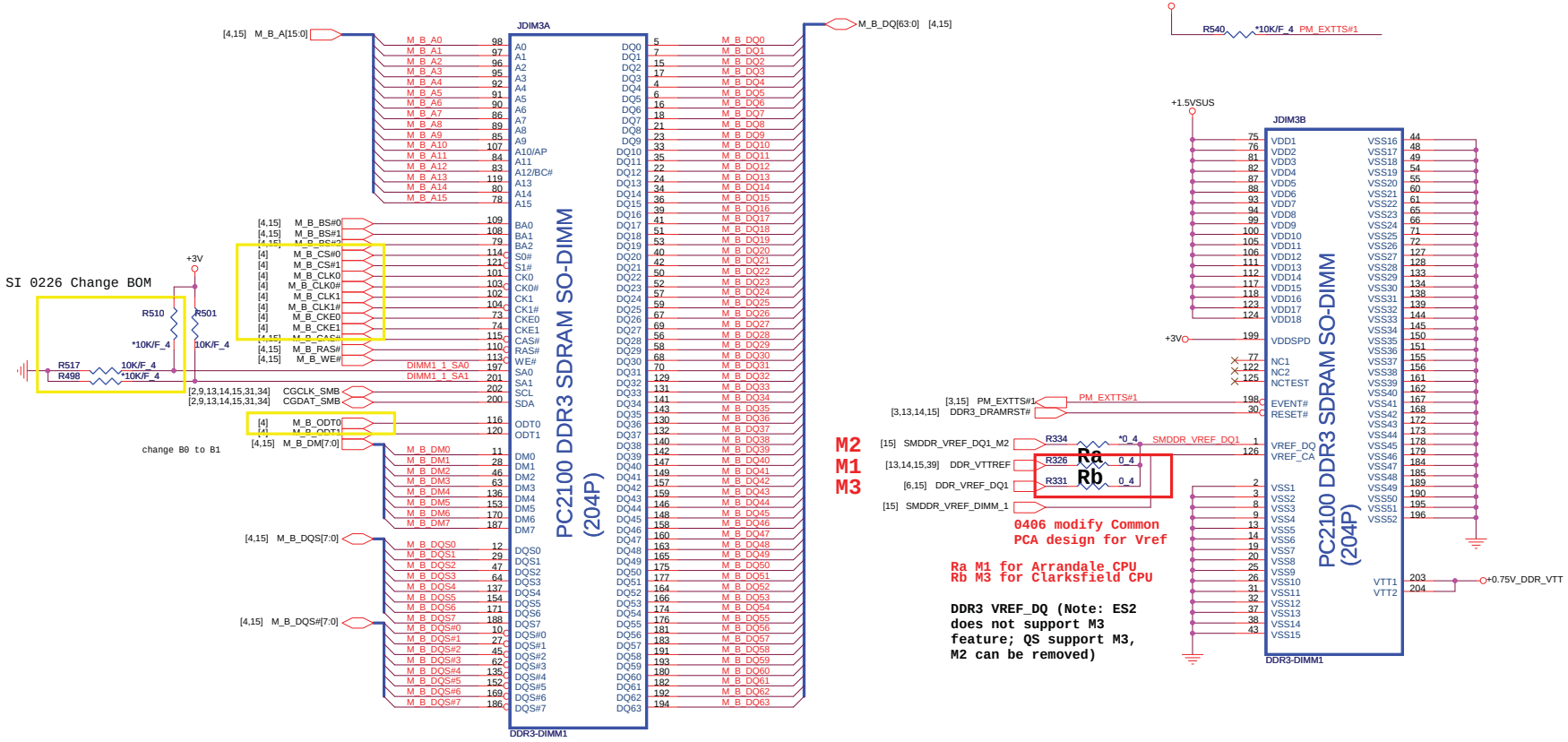
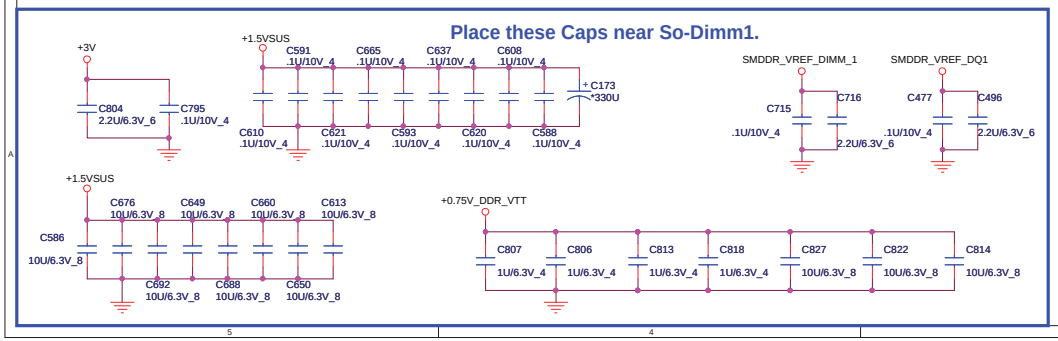
DDR3 -SODIMM 3 B1



DDR3 -SODIMM 4 B0





NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM-4	Rev: 1A
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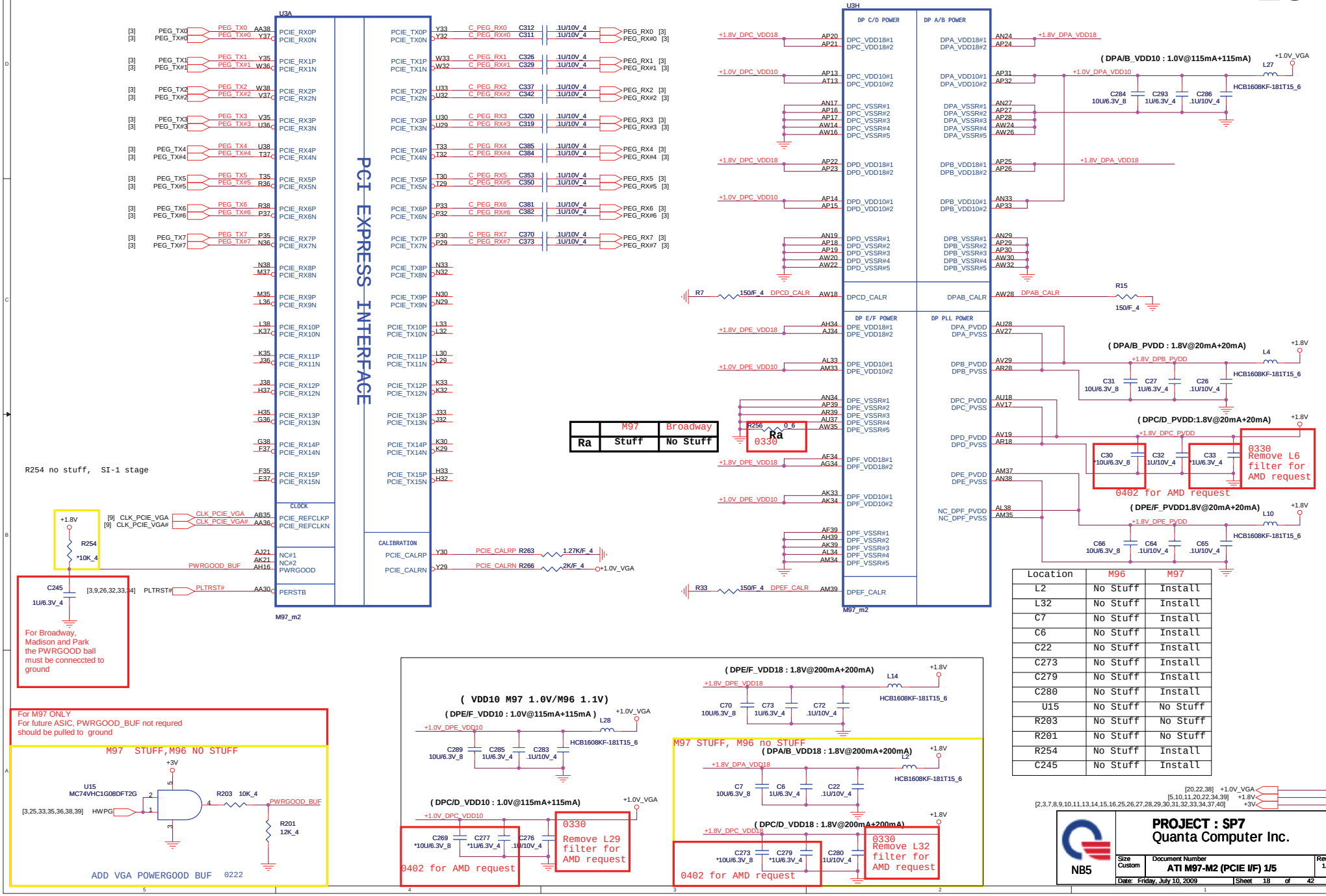
[2,7,8,9,11,26,27,36,37] +1.05V
[3,5,10,11,36,37] +1.1V_VTT
[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V
[7,9,10,11,25,40] +3VS5

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	XDP	1A
Date: Friday, July 10, 2009	Sheet 17 of 42	


U3A
PCI EXPRESS INTERFACE
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
CLOCK
PCIE_REFCLKP
PCIE_REFCLKN
NC#1
NC#2
PWRGOOD
PERSTB
CALIBRATION
PCIE_CALRP
PCIE_CALRN
M97_m2
R254 no stuff, SI-1 stage
R254
*10K_4
PWRGOOD_BUF
C245
1U/6.3V_4
PLTRST#
For Broadway, Madison and Park the PWRGOOD ball must be connecctd to ground
R263 1.27K/F_4
R266 2K/F_4
+1.0V_VGA
U3H
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
DPC_VDD18#1
DPC_VDD18#2
DPC_VDD10#1
DPC_VDD10#2
DPC_VSSR#1
DPC_VSSR#2
DPC_VSSR#3
DPC_VSSR#4
DPC_VSSR#5
DPD_VDD18#1
DPD_VDD18#2
DPD_VDD10#1
DPD_VDD10#2
DPD_VSSR#1
DPD_VSSR#2
DPD_VSSR#3
DPD_VSSR#4
DPD_VSSR#5
DPCD_CALR
DPE_VDD18#1
DPE_VDD18#2
DPE_VDD10#1
DPE_VDD10#2
DPE_VSSR#1
DPE_VSSR#2
DPE_VSSR#3
DPE_VSSR#4
DPE_VSSR#5
DPF_VDD18#1
DPF_VDD18#2
DPF_VDD10#1
DPF_VDD10#2
DPF_VSSR#1
DPF_VSSR#2
DPF_VSSR#3
DPF_VSSR#4
DPF_VSSR#5
DPEF_CALR
DPA_VDD18#1
DPA_VDD18#2
DPA_VDD10#1
DPA_VDD10#2
DPA_VSSR#1
DPA_VSSR#2
DPA_VSSR#3
DPA_VSSR#4
DPA_VSSR#5
DPB_VDD18#1
DPB_VDD18#2
DPB_VDD10#1
DPB_VDD10#2
DPB_VSSR#1
DPB_VSSR#2
DPB_VSSR#3
DPB_VSSR#4
DPB_VSSR#5
DPAB_CALR
DPA_PVDD
DPA_PVSS
DPB_PVDD
DPB_PVSS
DPC_PVDD
DPC_PVSS
DPD_PVDD
DPD_PVSS
DPE_PVDD
DPE_PVSS
NC_DPF_PVDD
NC_DPF_PVSS
M97_m2
R7 150/F_4 DPCD_CALR
R33 150/F_4 DPEF_CALR
R15 150/F_4 DPAB_CALR
(DPA/B_VDD10 : 1.0V@115mA+115mA)
L27 HCB1608KF-181T15_6
C284 10U/6.3V_8
C293 1U/6.3V_4
C286 .1U/10V_4
(DPA/B_PVDD : 1.8V@20mA+20mA)
L4 HCB1608KF-181T15_6
C31 10U/6.3V_8
C27 1U/6.3V_4
C26 .1U/10V_4
(DPC/D_PVDD:1.8V@20mA+20mA)
C30 *10U/6.3V_8
C32 1U/10V_4
C33 *1U/6.3V_4
0330 Remove L6 filter for AMD request
0402 for AMD request
(DPE/F_PVDD1.8V@20mA+20mA)
L10 HCB1608KF-181T15_6
C66 10U/6.3V_8
C64 .1U/10V_4
C65 .1U/10V_4
R256 0_6 Ra 0330
M97 Broadway
Ra Stuff No Stuff
Location M96 M97
L2 No Stuff Install
L32 No Stuff Install
C7 No Stuff Install
C6 No Stuff Install
C22 No Stuff Install
C273 No Stuff Install
C279 No Stuff Install
C280 No Stuff Install
U15 No Stuff No Stuff
R203 No Stuff No Stuff
R201 No Stuff No Stuff
R254 No Stuff Install
C245 No Stuff Install
For M97 ONLY
For future ASIC, PWRGOOD_BUF not requred should be pulled to ground
M97 STUFF,M96 NO STUFF
U15 MC74VHC1G08DFT2G
R203 10K_4
R201 12K_4
ADD VGA POWERGOOD BUF 0222
(VDD10 M97 1.0V/M96 1.1V)
(DPE/F_VDD10 : 1.0V@115mA+115mA)
L28 HCB1608KF-181T15_6
C289 10U/6.3V_8
C285 1U/6.3V_4
C283 .1U/10V_4
(DPC/D_VDD10 : 1.0V@115mA+115mA)
C269 *10U/6.3V_8
C277 *1U/6.3V_4
C276 .1U/10V_4
0330 Remove L29 filter for AMD request
0402 for AMD request
(DPE/F_VDD18 : 1.8V@200mA+200mA)
L14 HCB1608KF-181T15_6
C70 10U/6.3V_8
C73 1U/6.3V_4
C72 .1U/10V_4
M97 STUFF, M96 no STUFF
(DPA/B_VDD18 : 1.8V@200mA+200mA)
L2 HCB1608KF-181T15_6
C7 10U/6.3V_8
C6 1U/6.3V_4
C22 .1U/10V_4
(DPC/D_VDD18 : 1.8V@200mA+200mA)
C273 *10U/6.3V_8
C279 *1U/6.3V_4
C280 .1U/10V_4
0330 Remove L32 filter for AMD request
0402 for AMD request
[20,22,38] +1.0V_VGA
[5,10,11,20,22,34,39] +1.8V
[2,3,7,8,9,10,11,13,14,15,16,25,26,27,28,29,30,31,32,33,34,37,40] +3V
PROJECT : SP7
Quanta Computer Inc.
NB5
Size Custom
Document Number ATI M97-M2 (PCIE I/F) 1/5
Rev 1A
Date: Friday, July 10, 2009
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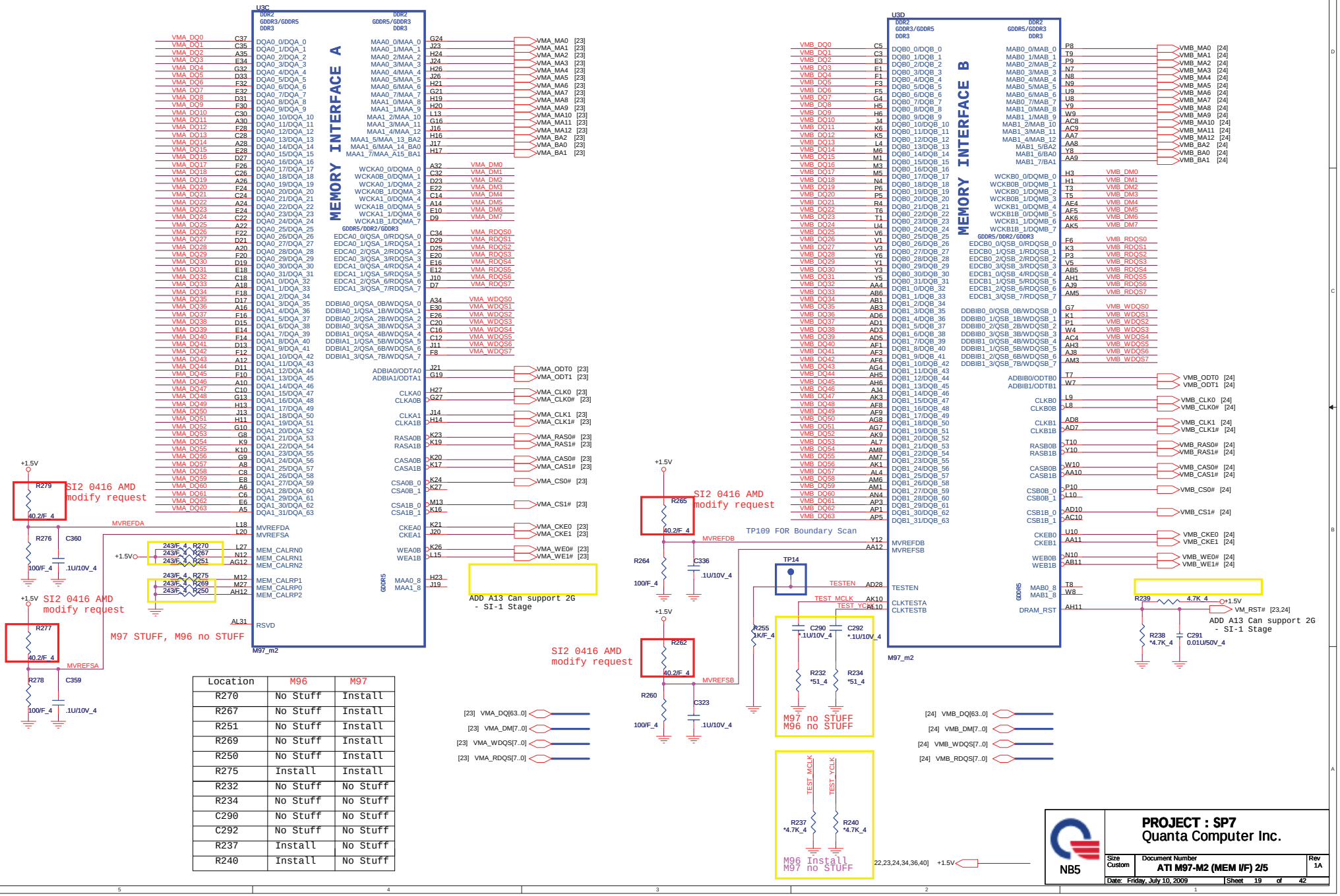
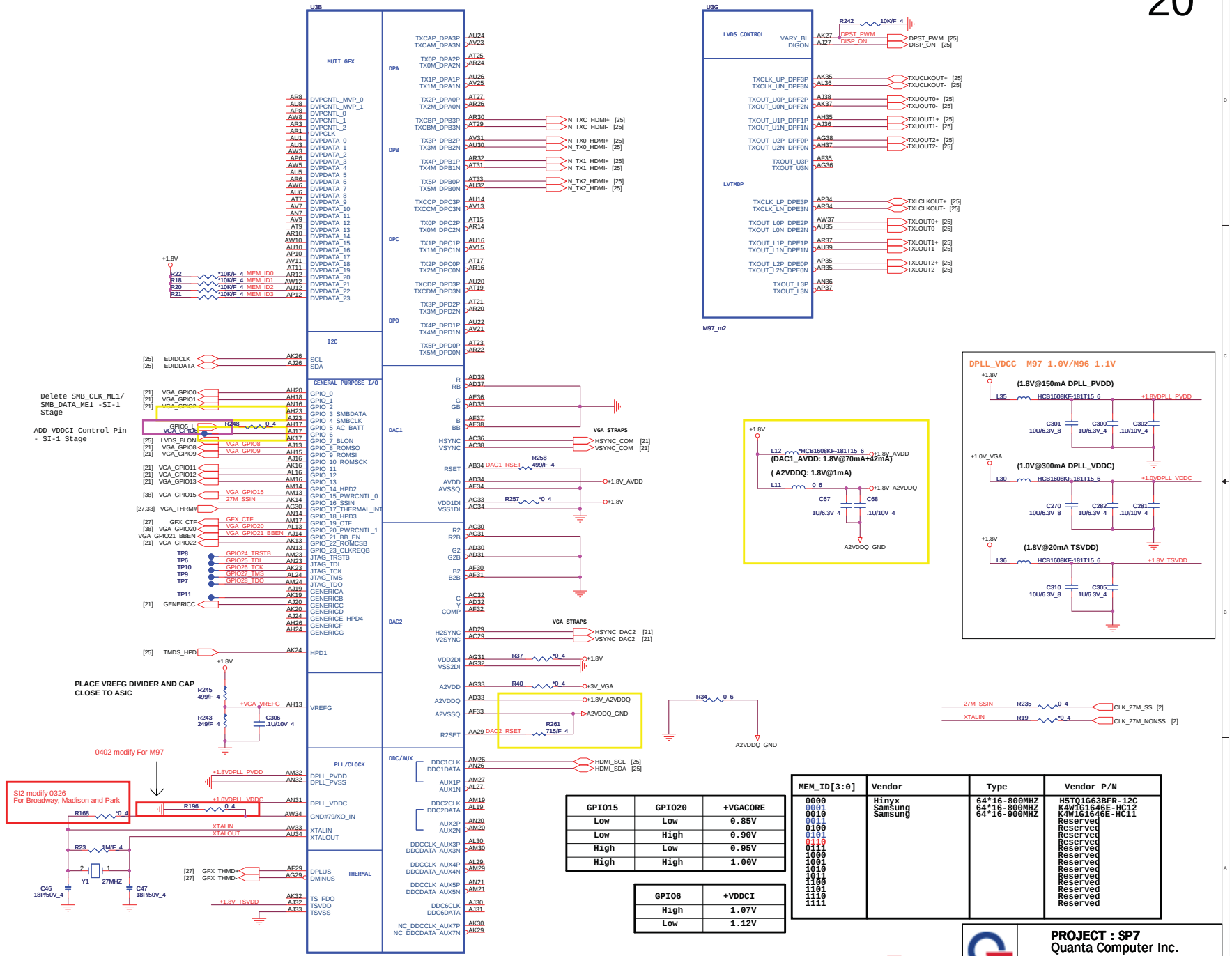


Location	M96	M97
R270	No Stuff	Install
R267	No Stuff	Install
R251	No Stuff	Install
R269	No Stuff	Install
R250	No Stuff	Install
R275	Install	Install
R232	No Stuff	No Stuff
R234	No Stuff	No Stuff
C290	No Stuff	No Stuff
C292	No Stuff	No Stuff
R237	Install	No Stuff
R240	Install	No Stuff



GPIO15	GPIO20	+VGACORE
Low	Low	0.85V
Low	High	0.90V
High	Low	0.95V
High	High	1.00V

GPIO6	+VDDCI
High	1.07V
Low	1.12V

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hinyx	64*16-800MHZ	H5TQ1G63BFR-12C
0001	Samsung	64*16-800MHZ	K4W1G1646E-HC12
0010	Samsung	64*16-900MHZ	K4W1G1646E-HC11
0011			Reserved
0100			Reserved
0101			Reserved
0110			Reserved
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved

PROJECT : SP7
Quanta Computer Inc.
NB5
Size: Custom
Document Number: ATI M97-M2 (DISPLAY) 3/5
Rev: 1A
Date: Friday, July 10, 2009
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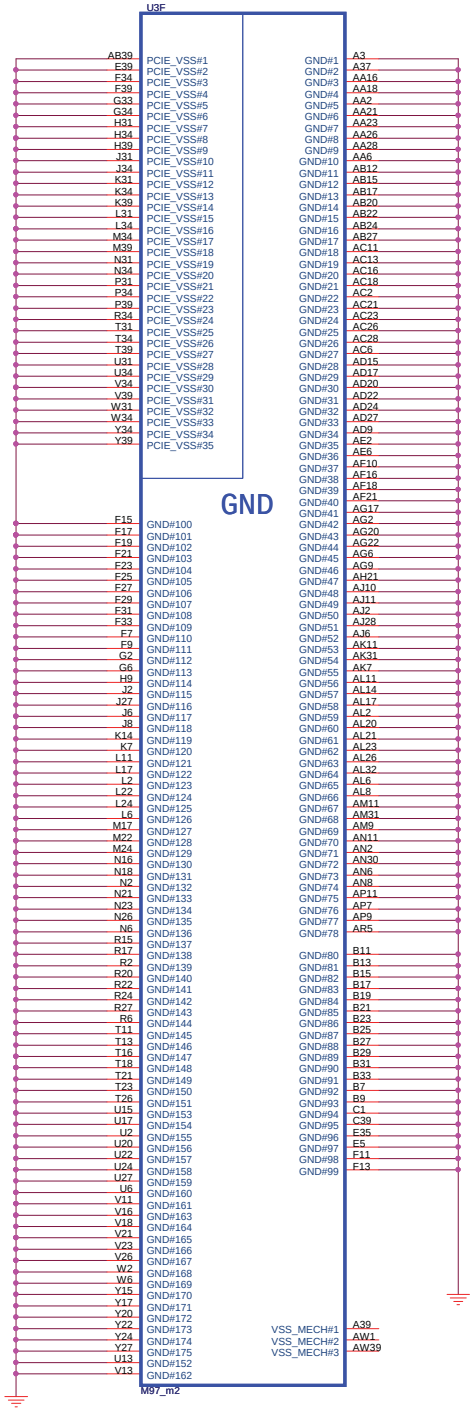
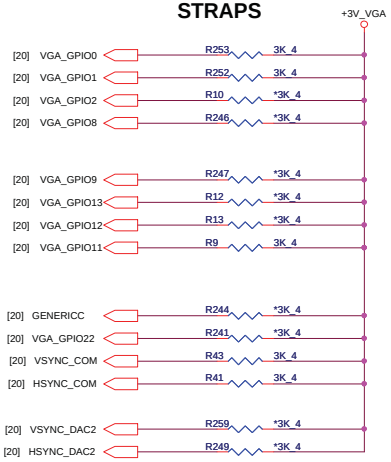
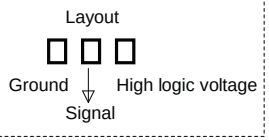


STRAPS



Location	M96	M97
pull-up for straps	10K (CS31002FB26)	3K (CS23002FB11)

Overlap pads to save space and to prevent assembly of both resistors.



Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
STRAP_BIF_CLK_PM_EN	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11	GPIO9,13,12,11 (config 3,2,1,0): a> If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM Type: b> If BIOS_ROM_EN = 0, then Config[3:0] defines the Aperture size:Size of the primary memory apertures claimed in PCI configuration space 000 = 128MB 001 = 256MB 010 = 64MB 011 = 32MB 100 = 512MB 101 = 1GB 110 = 2GB 111 = 4GB	0001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
AUDIO[0]	VSYNC		0
AUD(1)	HSYNC	HSYNC - HDMI_EN HDMI connector presence. 0 ?No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	1
VSYNC_DAC2	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
HSYNC_DAC2	H2SYNC		0
	GENERICC		0

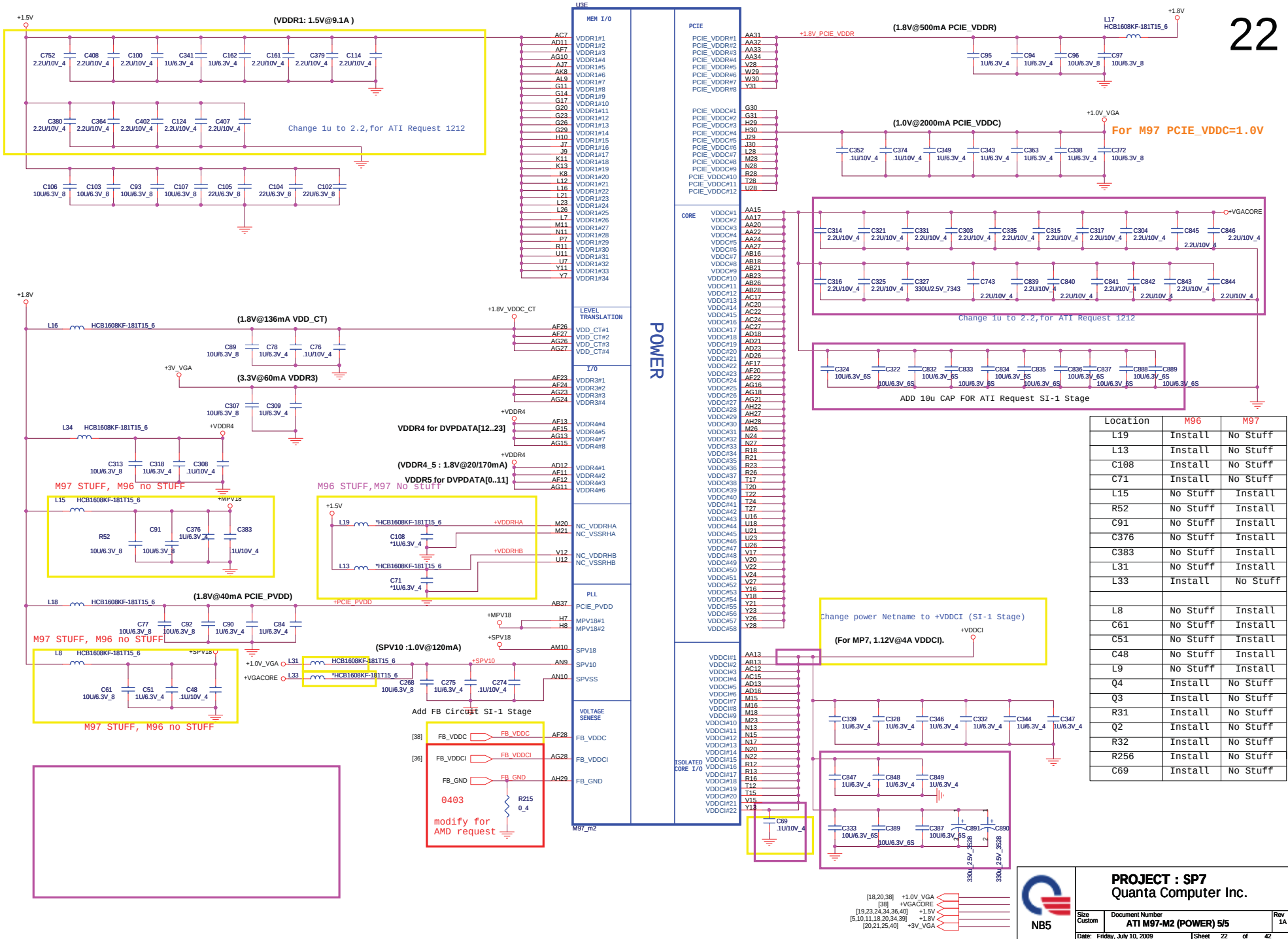
[20,22,25,40] +3V_VGA

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M97(GND&Str&Ther)4/5	1A

Date: Friday, July 10, 2009 Sheet 21 of 42



Location	M96	M97
L19	Install	No Stuff
L13	Install	No Stuff
C108	Install	No Stuff
C71	Install	No Stuff
L15	No Stuff	Install
R52	No Stuff	Install
C91	No Stuff	Install
C376	No Stuff	Install
C383	No Stuff	Install
L31	No Stuff	Install
L33	Install	No Stuff
L8	No Stuff	Install
C61	No Stuff	Install
C51	No Stuff	Install
C48	No Stuff	Install
L9	No Stuff	Install
Q4	Install	No Stuff
Q3	Install	No Stuff
R31	Install	No Stuff
Q2	Install	No Stuff
R32	Install	No Stuff
R256	Install	No Stuff
C69	Install	No Stuff

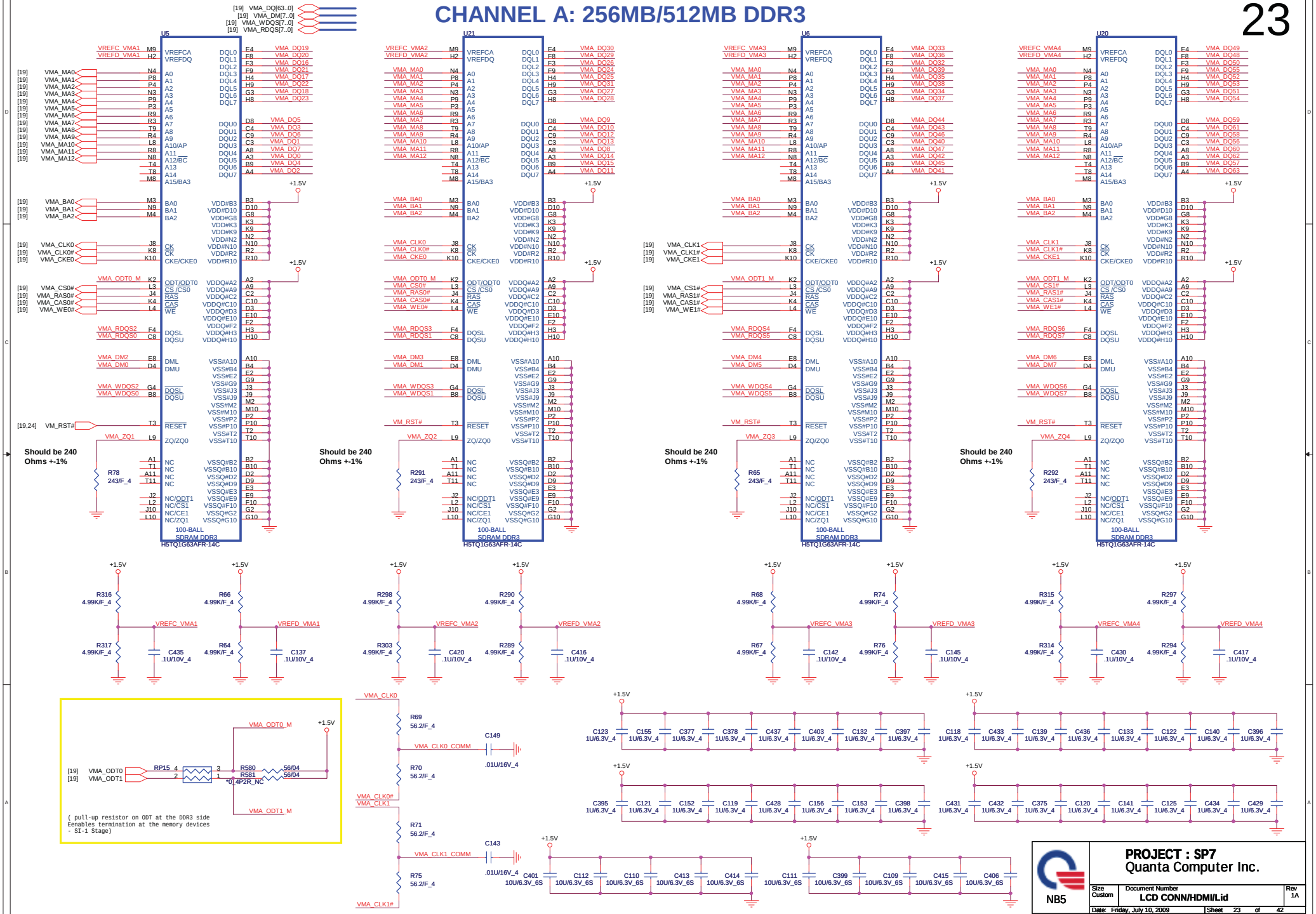
[18,20,38] +1.0V_VGA
[38] +VGACORE
[19,23,24,34,36,40] +1.5V
[5,10,11,18,20,34,39] +1.8V
[20,21,25,40] +3V_VGA

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M97-M2 (POWER) 5/5	1A
Date: Friday, July 10, 2009	Sheet 22 of 42	

CHANNEL A: 256MB/512MB DDR3



PROJECT : SP7
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	LCD CONN/HDMI/Lid	1A

Date: Friday, July 10, 2009 Sheet 23 of 42

CHANNEL B: 256MB/512MB DDR3

[19] VMB_DQ[63..0]
[19] VMB_DM[7..0]
[19] VMB_WDQS[7..0]
[19] VMB_RDQS[7..0]

U4 / U19 / U2 / U18 — H5TQ1G63AFR-14C — 100-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R50 243/F_4 (U4) · R61 243/F_4 (U19) · R29 243/F_4 (U2) · R51 243/F_4 (U18)

R272 4.99K/F_4 · R271 4.99K/F_4 · VREFC_VMB1 · C361 .1U/10V_4
R59 4.99K/F_4 · R60 4.99K/F_4 · VREFD_VMB1 · C116 .1U/10V_4
R62 4.99K/F_4 · R63 4.99K/F_4 · VREFC_VMB2 · C115 .1U/10V_4
R274 4.99K/F_4 · R273 4.99K/F_4 · VREFD_VMB2 · C362 .1U/10V_4
R30 4.99K/F_4 · R24 4.99K/F_4 · VREFC_VMB3 · C62 .1U/10V_4
R48 4.99K/F_4 · R49 4.99K/F_4 · VREFD_VMB3 · C83 .1U/10V_4
R38 4.99K/F_4 · R35 4.99K/F_4 · VREFC_VMB4 · C75 .1U/10V_4
R25 4.99K/F_4 · R26 4.99K/F_4 · VREFD_VMB4 · C56 .1U/10V_4

RP16 4/2/3/1 · R582 56/04 · R583 56/04 · *0_4P2R_NC · VMB_ODT0_M · VMB_ODT1_M

(pull-up resistor on ODT at the DDR3 side
Eenables termination at the memory devices
- SI-1 Stage)

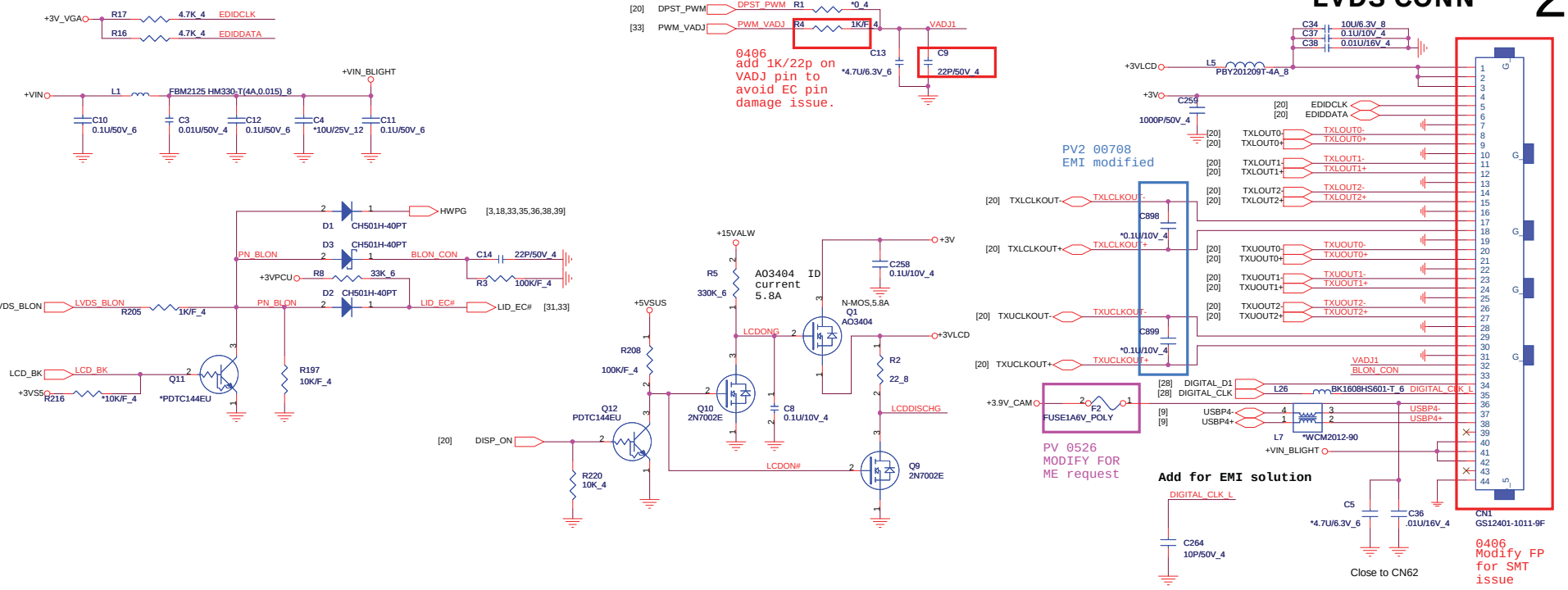
VMB_CLK0 · R282 56.2/F_4 · VMB_CLK0_COMM · C390 .01U/16V_4 · R281 56.2/F_4 · VMB_CLK0#
VMB_CLK1 · R27 56.2/F_4 · VMB_CLK1_COMM · C57 .01U/16V_4 · R28 56.2/F_4 · VMB_CLK1#

C85 C81 C368 C86 C80 C53 C113 C87 1U/6.3V_4
C299 C101 C367 C348 C99 C60 C117 C298 1U/6.3V_4
C358 C369 C88 C82 C98 C79 C297 C356 1U/6.3V_4
C357 C366 C355 C59 C55 C54 C52 C58 1U/6.3V_4
C296 C394 C393 C388 C392 C391 C63 C294 C386 C295 10U/6.3V_6S

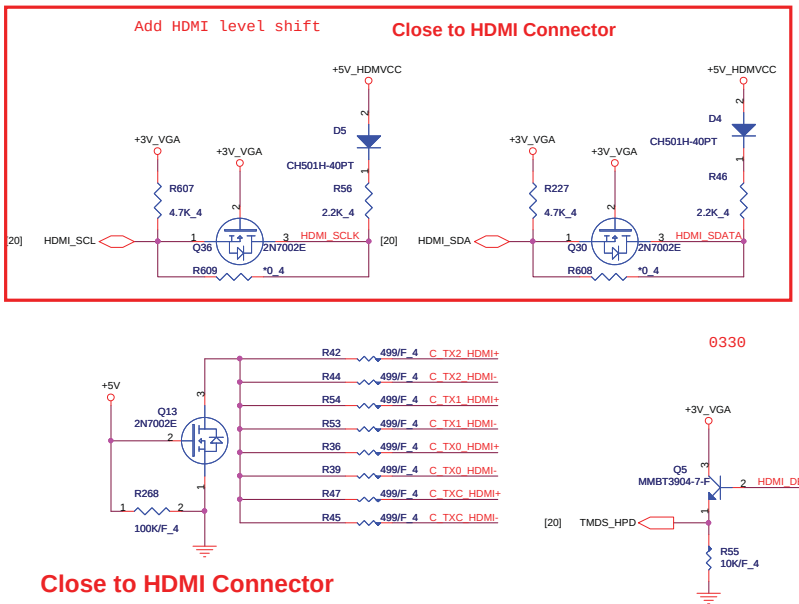
PROJECT : SP7
Quanta Computer Inc.
NB5
Size: Custom | Document Number: LCD CONN/HDMI/Lid | Rev: 1A
Date: Friday, July 10, 2009 | Sheet 24 of 42

LVDS CONN

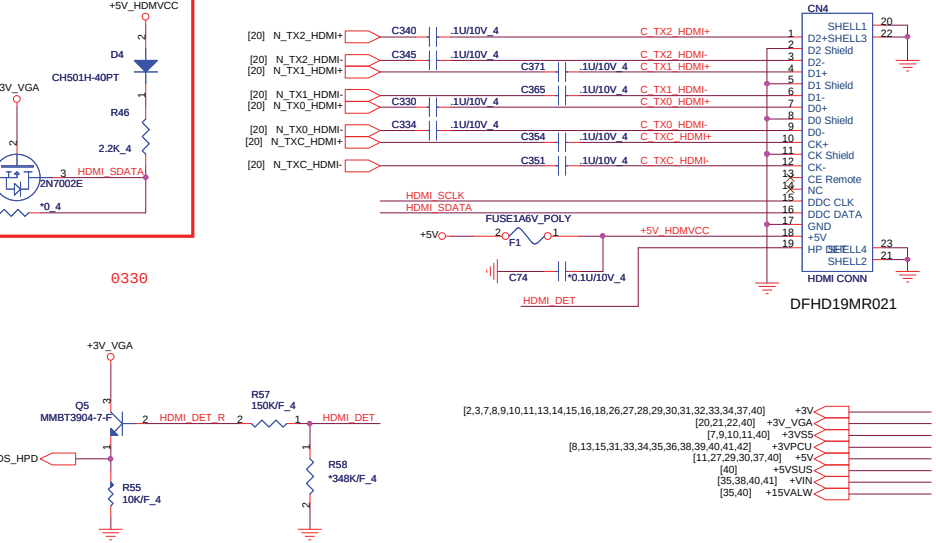
25



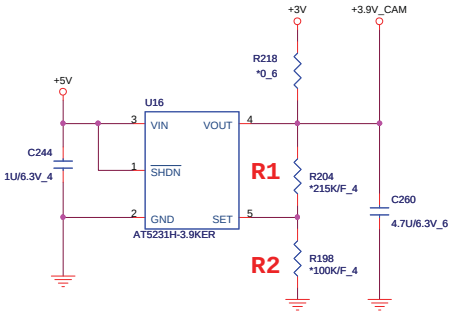
HDMI PORT



HDMI HPD SENSE



USB CAMERA /DIGITAL MIC CONNECT



Vout=1.25(1+R1/R2)

[2,3,7,8,9,10,11,13,14,15,16,18,26,27,28,29,30,31,32,33,34,37,40] +3V
[20,21,22,40] +3V_VGA
[7,9,10,11,40] +3VS5
[8,13,15,31,33,34,35,36,38,39,40,41,42] +3VPCU
[11,27,29,30,37,40] +5V
[40] +5VSUS
[35,38,40,41] +VIN
[35,40] +15VALW

NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: LCD CONN/HDMI/Lid	Rev: 1A
Date: Friday, July 10, 2009	Sheet 25 of 42	

USB3.0 X 2 and E-SATA/USB2.0 COMBO

26

*nPD720200

SI U29.P13 Change to +3V

SI2 0414 NEC request

SI 0219 change BOM

SI2 0320 change Footprint

close USB3

150 mils (Iout=3.5A)

Low: Enable AC Mode

High: Disable DC Mode

1125 Modify

PV2 stage modify

1119 Modify

6.3V to 25V from NEC

USB CON. co-lay

USB3.0 PORT1

USB3.0 PORT2

USB2.0 PORT6

USB2.0 PORT7

AT25F512A or AT25F512B (Atmel)

MX25L512 (Macronix)

SI2 0325 change Footprint

*MX25L8005M2C-15G

PV-2 0702 Change Footprint

PV-2 0702 EMI add

PV-2 0702 EMI add

E_SATA change channel from SATA2 to SATA5 0216

Clock select signal	
USB3.0_CSEL	High = External 48Mhz Low = 24MHz X'tal

PROJECT : SP7
Quanta Computer Inc.

NB5

Size: Custom | Document Number: NEC USB 3.0 | Rev: 1A

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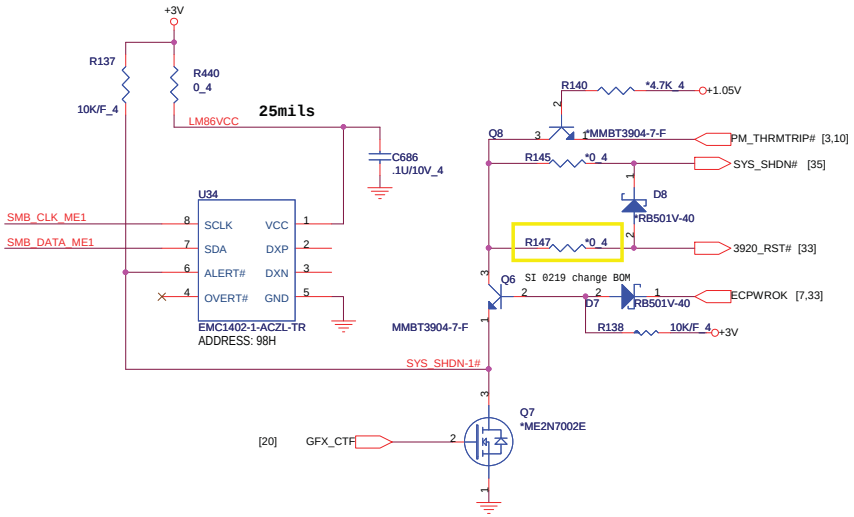
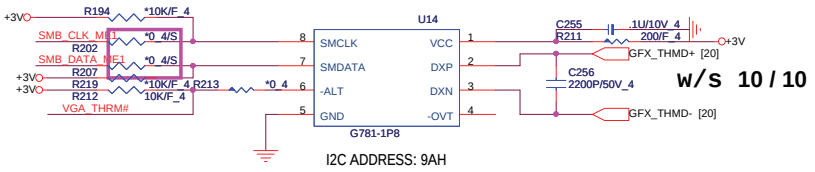
CPU THERMAL MONITOR

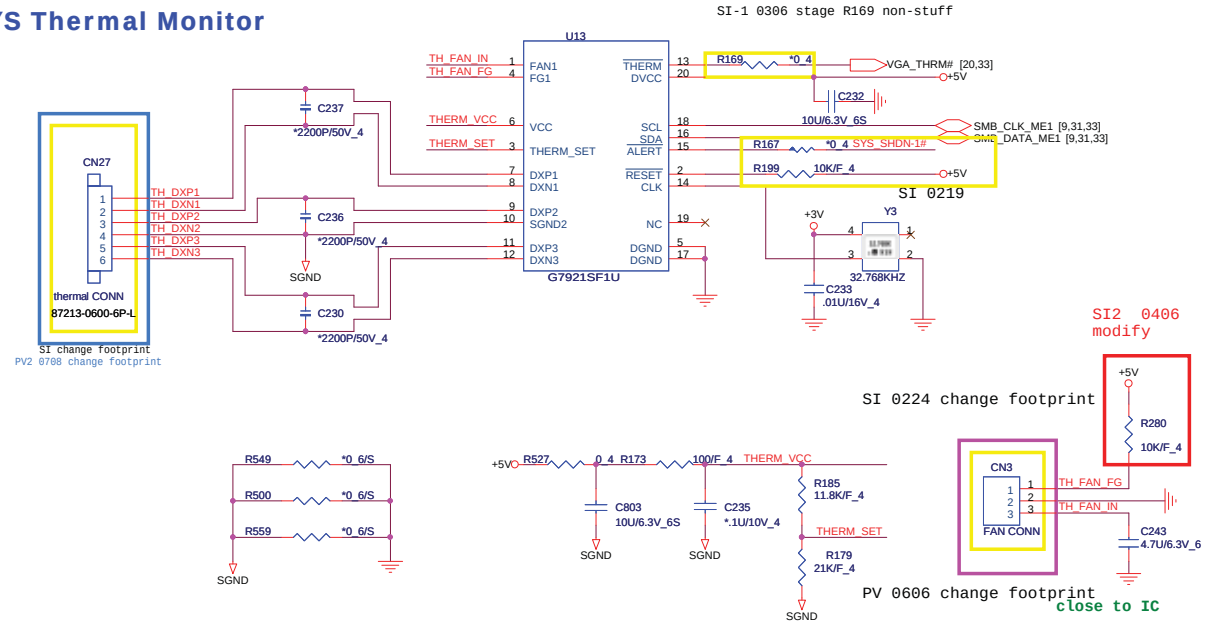


GPU Thermal Sensor



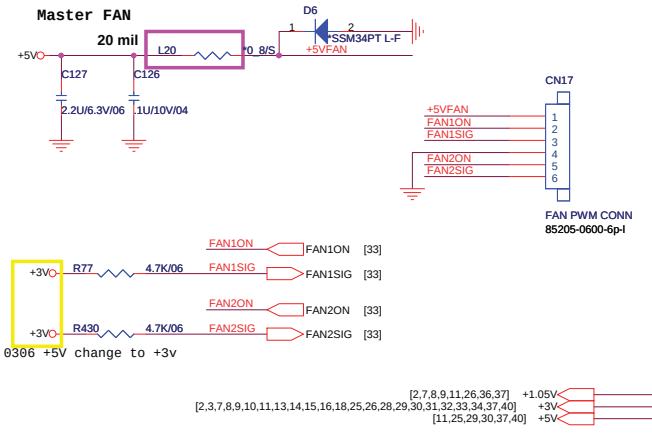
w/s 10 / 10

SYS Thermal Monitor



CPU FAN1/2 CONN

RPM Control

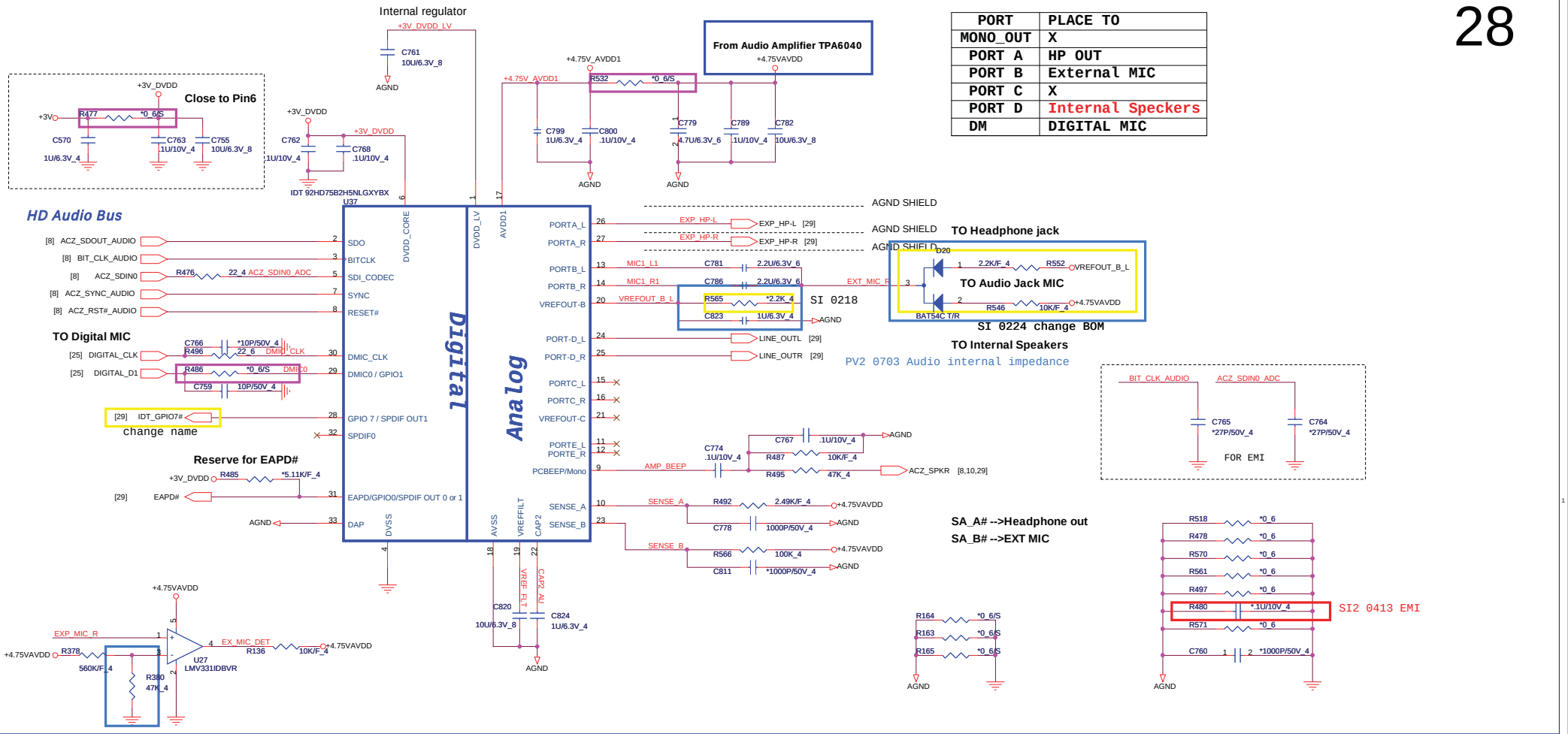


NB5

PROJECT : SP7
Quanta Computer Inc.

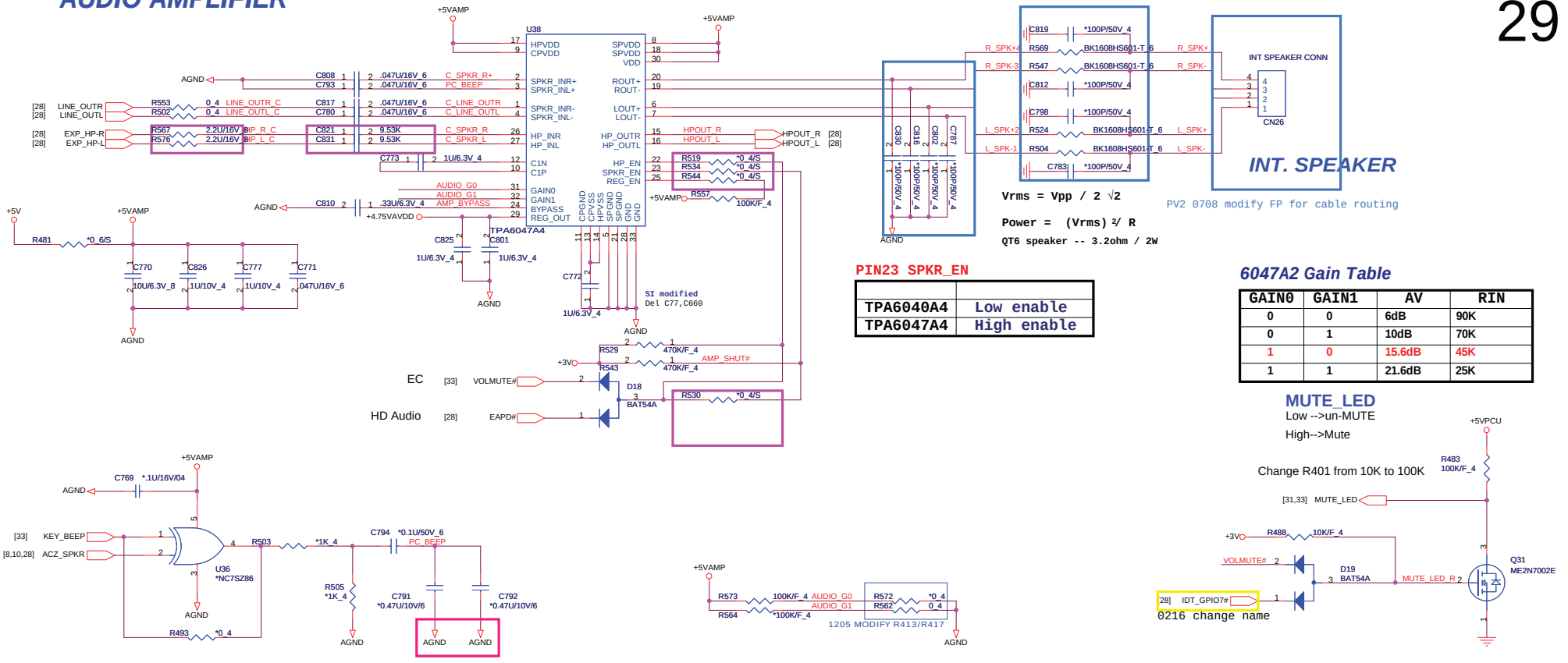
Size	Document Number	Rev
Custom	CPU/VGA/SYSTEM THERMAL	1A
Date: Friday, July 10, 2009	Sheet 27 of 42	

PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT
PORT B	External MIC
PORT C	X
PORT D	Internal Speckers
DM	DIGITAL MIC



PROJECT : SP7	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Azalia 92HD75
Rev: 1A	
Date: Friday, July 10, 2009	Sheet 28 of 42

AUDIO AMPLIFIER



Vrms = Vpp / 2 √2

Power = (Vrms)² / R

QT6 speaker -- 3.2ohm / 2W

PV2 0708 modify FP for cable routing

PIN23 SPKR_EN

TPA6040A4	Low enable
TPA6047A4	High enable

6047A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

MUTE_LED

Low -->un-MUTE

High-->Mute

Change R401 from 10K to 100K

0216 change name

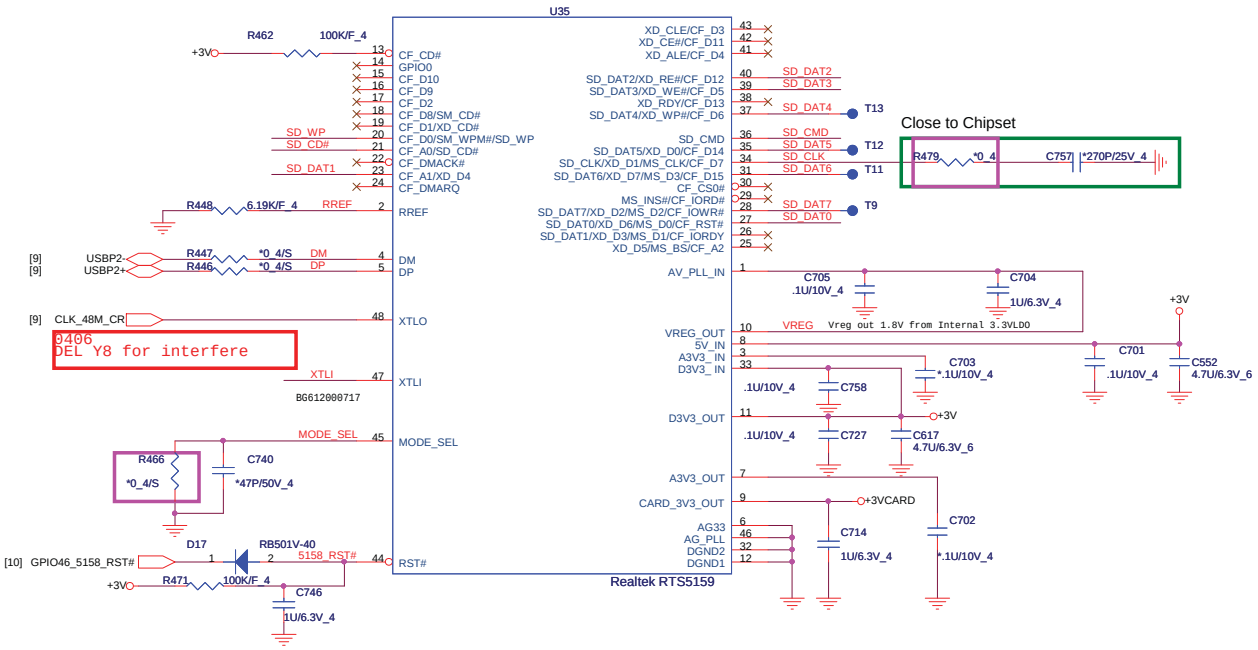
[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,30,31,32,33,34,37,40] +3V
[28] +4.75VAVDD
[11,25,27,30,37,40] +5V
[15,26,33,35,36,37,38,39,40,41] +5VPCU

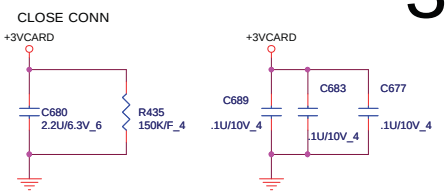
NB5

PROJECT : SP7
Quanta Computer Inc.

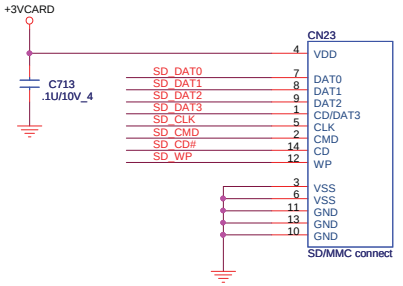
Size	Document Number	Rev
Custom	AMP_TPA6047	1A

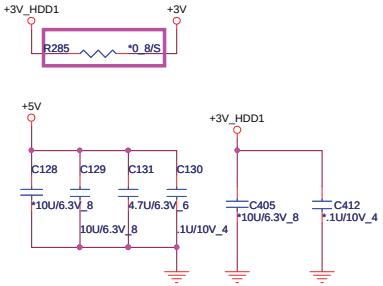
Date: Friday, July 10, 2009 Sheet 29 of 42





2 IN1 CARD READER SD/MMC



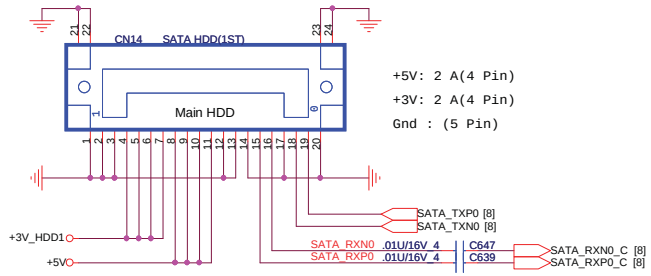


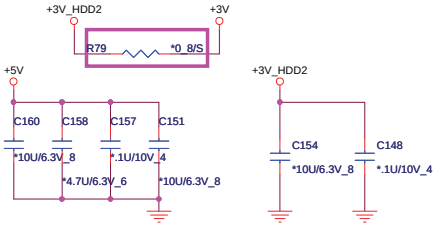
SATA 1.8"/2.5" HDD CONNECTOR

MASTER

DFHD20MR005

DC Current rating: 0.5 A

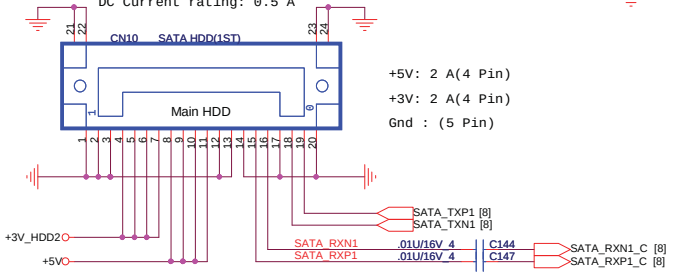




SSD(1) 1.8" CONNECTOR

SLAVE

DC Current rating: 0.5 A



[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,31,32,33,34,37,40] +3V

[11,25,27,29,37,40] +5V

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5159 & CR SOCKET	1A

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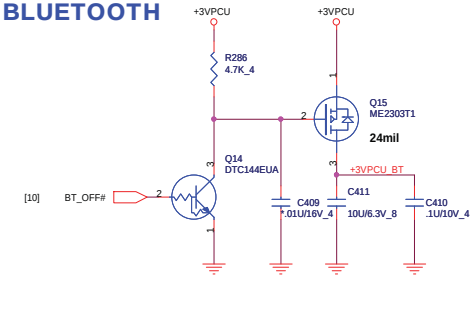
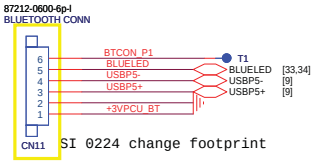
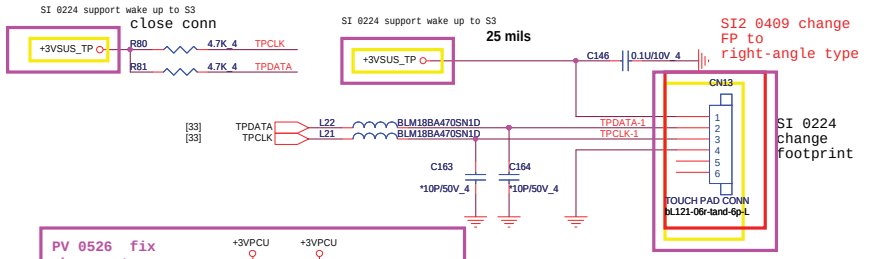
BLUETOOTH

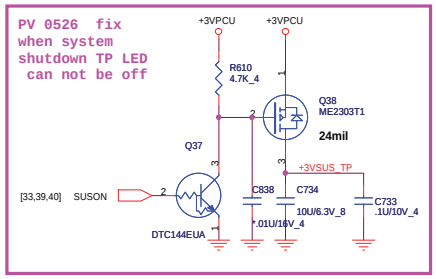




SI 0224 change footprint

TOUCH PAD CONNECTOR



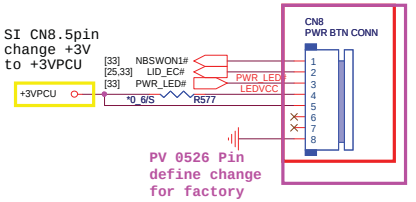


PV 0526 Pin define change for factory

Pin1	VDD
Pin2	DATA
Pin3	CLK
Pin4	GND
Pin5	X
Pin6	X

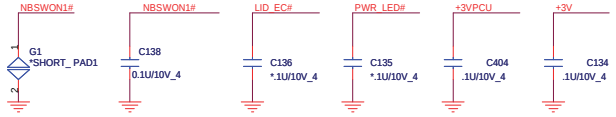
Power Botton

SI2 0413 change FP to right-angle type

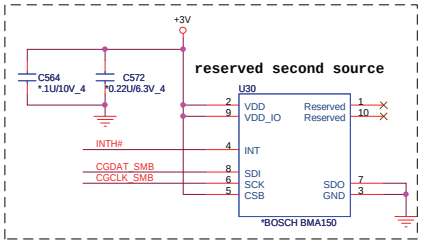


1. GND
2. RESERVE
3. RESERVE
4. +3VPCU
5. LEDVCC(+3VPCU)
6. PWRLED#
7. LIDSWITCH
8. POWER ON#

POWER BOTTON CONNECT

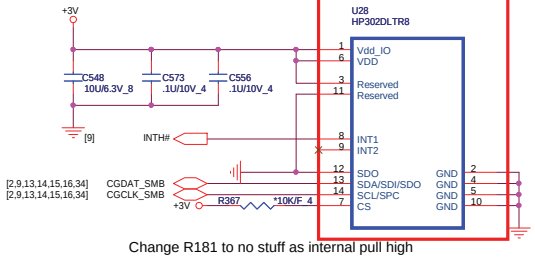


Accelerometer Sensor



SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

SI2 0331 FP modify same as SP6 for SMT request

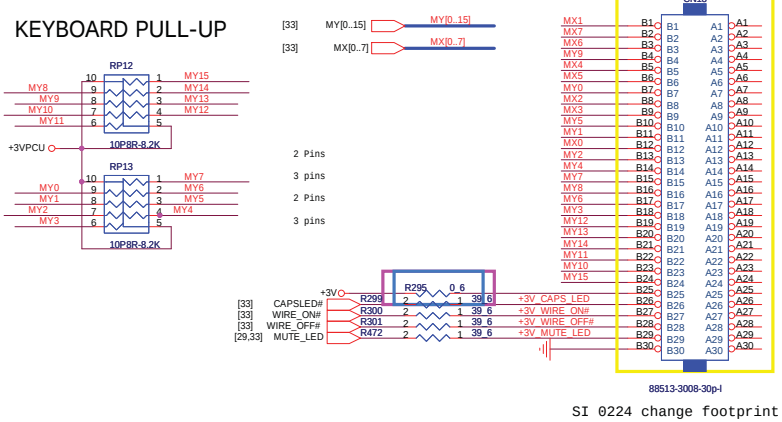


Change R181 to no stuff as internal pull high

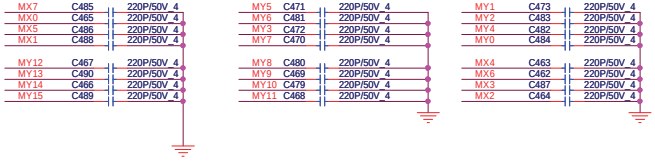
Pin 12: Low	38hex
Pin 12: unconnected/floating	3Ahex

Key Board CONN

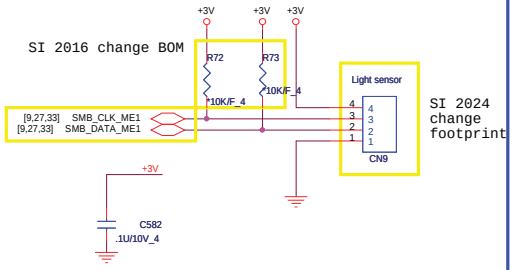
KEYBOARD PULL-UP



SI 0224 change footprint

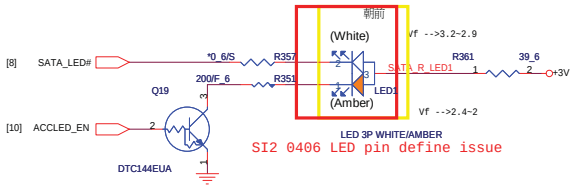


Ambient Light Sensor



LED

SI0210 white for HDD active
Amber for HDD locked



SI2 0406 LED pin define issue

[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,32,33,34,37,40]
[8,13,15,25,33,34,35,36,38,39,40,41,42]
+3V
+3VPCU

PROJECT : SP7
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	BT/TP/PW BN/Key CON/Acc/LED/ALS	1A
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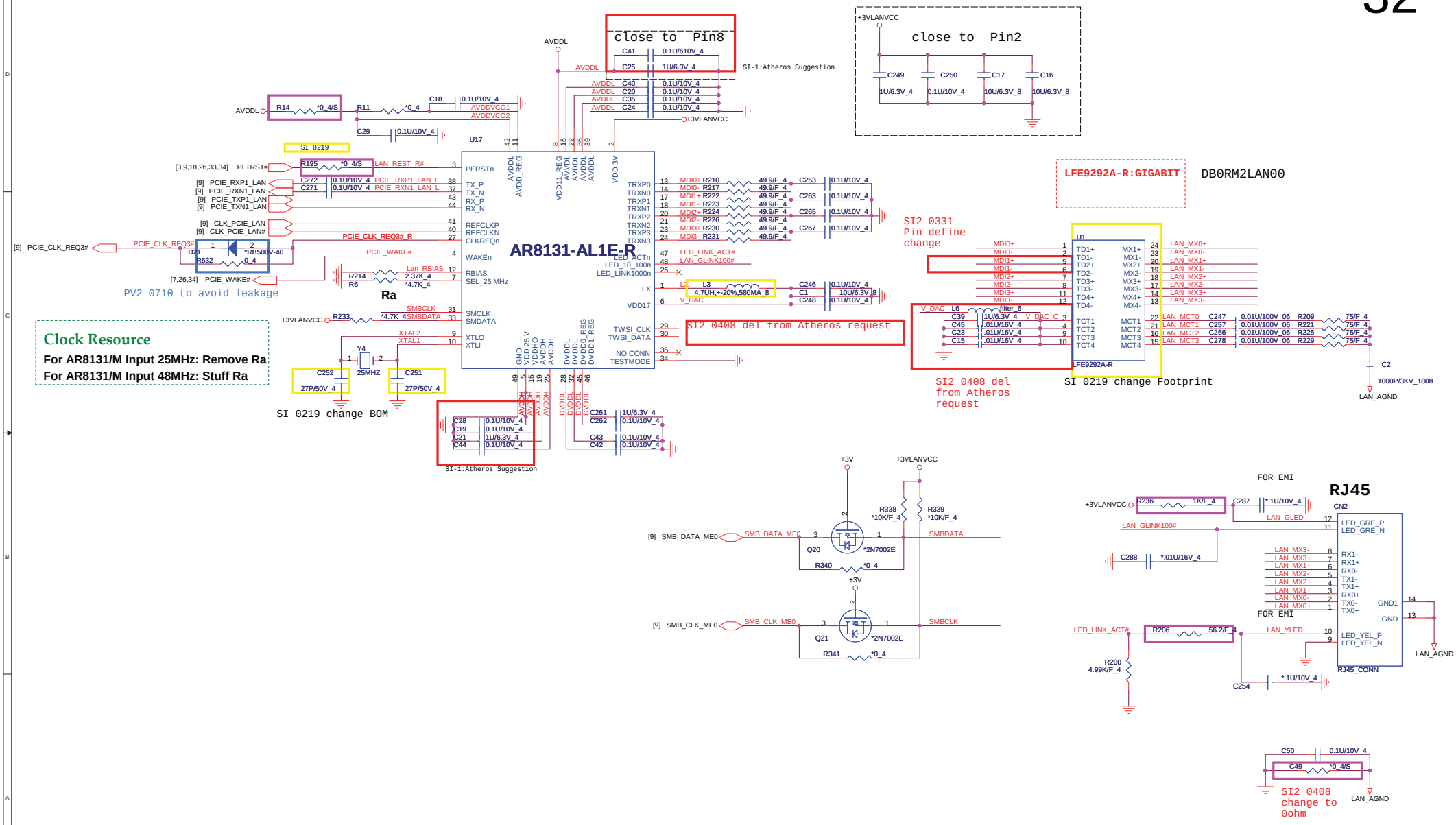
close to Pin8
close to Pin2
AR8131-AL1E-R
LFE9292A-R:GIGABIT
DB0RM2LAN00
SI 0331 Pin define change
SI2 0408 del from Atheros request
SI2 0408 del from Atheros request
SI 0219 change Footprint
SI 0219 change BOM
PV2 0710 to avoid leakage
Ra
Clock Resource
For AR8131/M Input 25MHz: Remove Ra
For AR8131/M Input 48MHz: Stuff Ra
RJ45
FOR EMI
FOR EMI
SI2 0408 change to 0ohm
SI-1:Atheros Suggestion
SI-1:Atheros Suggestion
PROJECT : SP7
Quanta Computer Inc.
NB5
Block Diagram
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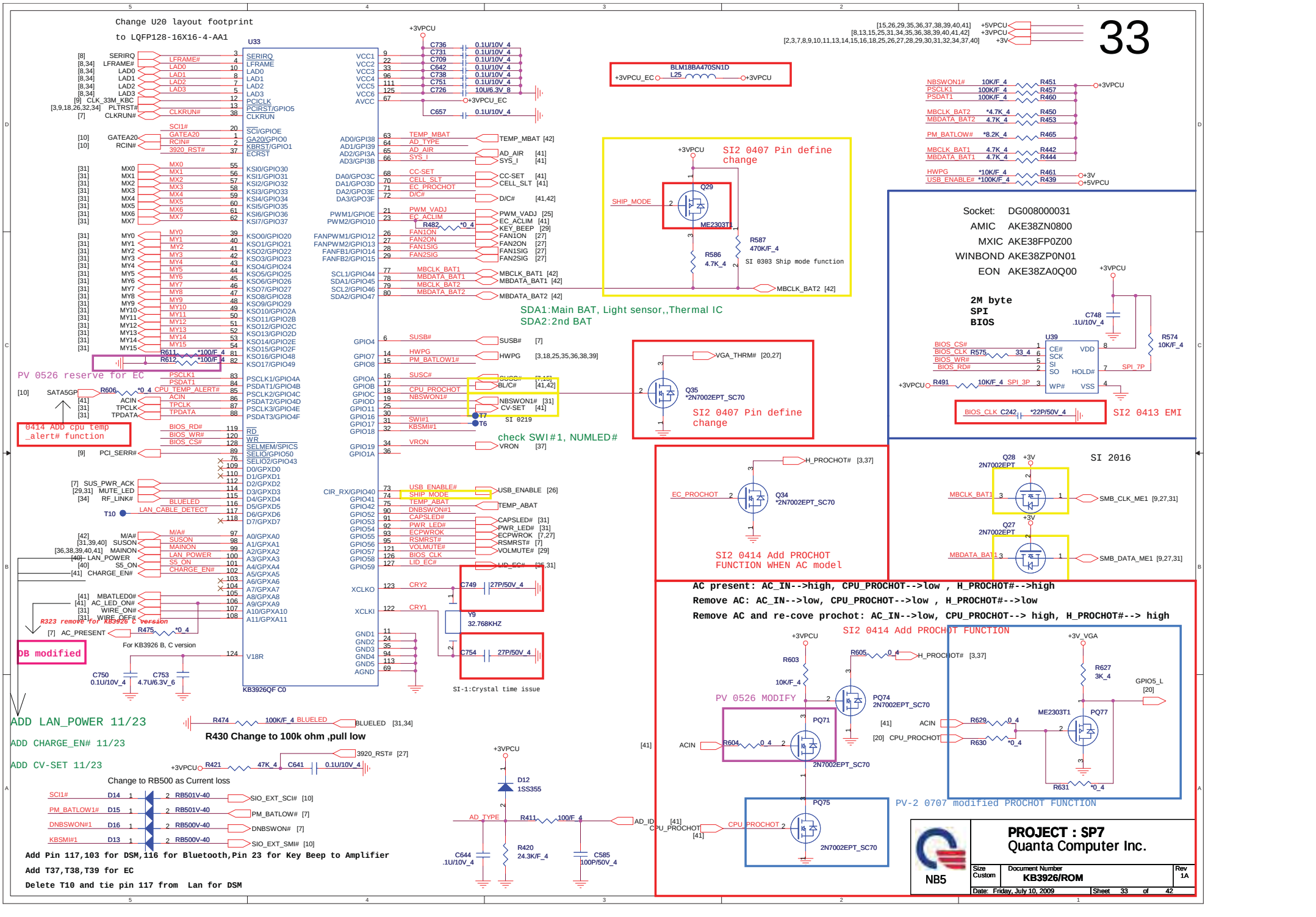
33
Change U20 layout footprint
to LQFP128-16X16-4-AA1
U33
KB3926QF C0
PV 0526 reserve for EC
0414 ADD cpu temp
_alert# function
SI2 0407 Pin define
change
SDA1:Main BAT, Light sensor,,Thermal IC
SDA2:2nd BAT
check SWI#1, NUMLED#
SI 0219
SI-1:Crystal time issue
SI2 0407 Pin define
change
SI2 0414 Add PROCHOT
FUNCTION WHEN AC model
SI 2016
SI2 0413 EMI
Socket: DG008000031
AMIC AKE38ZN0800
MXIC AKE38FP0Z00
WINBOND AKE38ZP0N01
EON AKE38ZA0Q00
2M byte
SPI
BIOS
AC present: AC_IN-->high, CPU_PROCHOT-->low , H_PROCHOT#-->high
Remove AC: AC_IN-->low, CPU_PROCHOT-->low , H_PROCHOT#-->low
Remove AC and re-cove prochot: AC_IN-->low, CPU_PROCHOT--> high, H_PROCHOT#--> high
SI2 0414 Add PROCHOT FUNCTION
PV 0526 MODIFY
PV-2 0707 modified PROCHOT FUNCTION
DB modified
ADD LAN_POWER 11/23
ADD CHARGE_EN# 11/23
ADD CV-SET 11/23
R430 Change to 100k ohm ,pull low
Change to RB500 as Current loss
Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier
Add T37,T38,T39 for EC
Delete T10 and tie pin 117 from Lan for DSM
PROJECT : SP7
Quanta Computer Inc.
NB5
KB3926/ROM
Size Custom
Rev 1A
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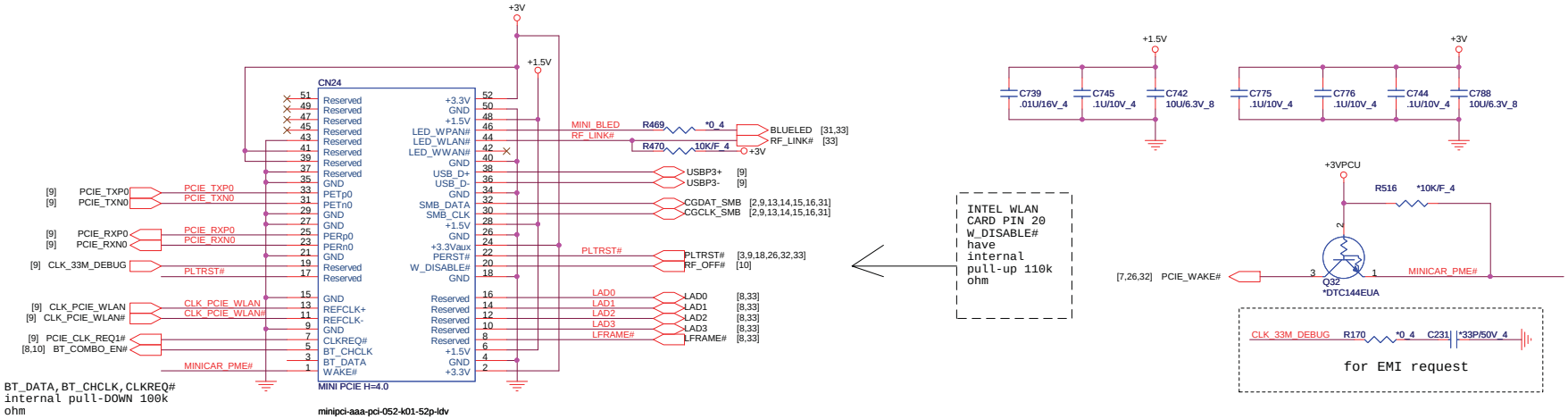
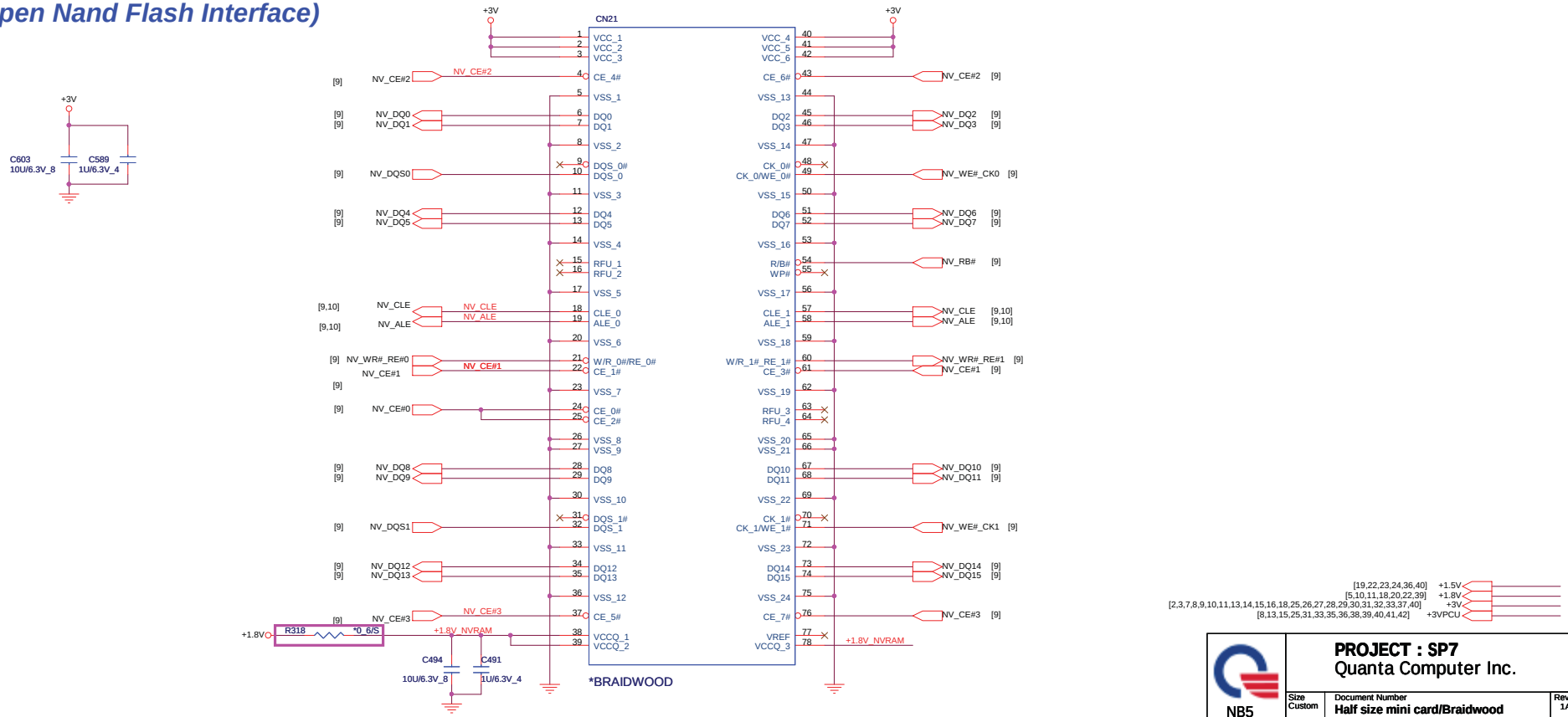
Half size mini card(802.11a/b/g/n)



Braidwood(Open Nand Flash Interface)



Size: Custom	Document Number: Half size mini card/Braidwood
Rev: 1A	
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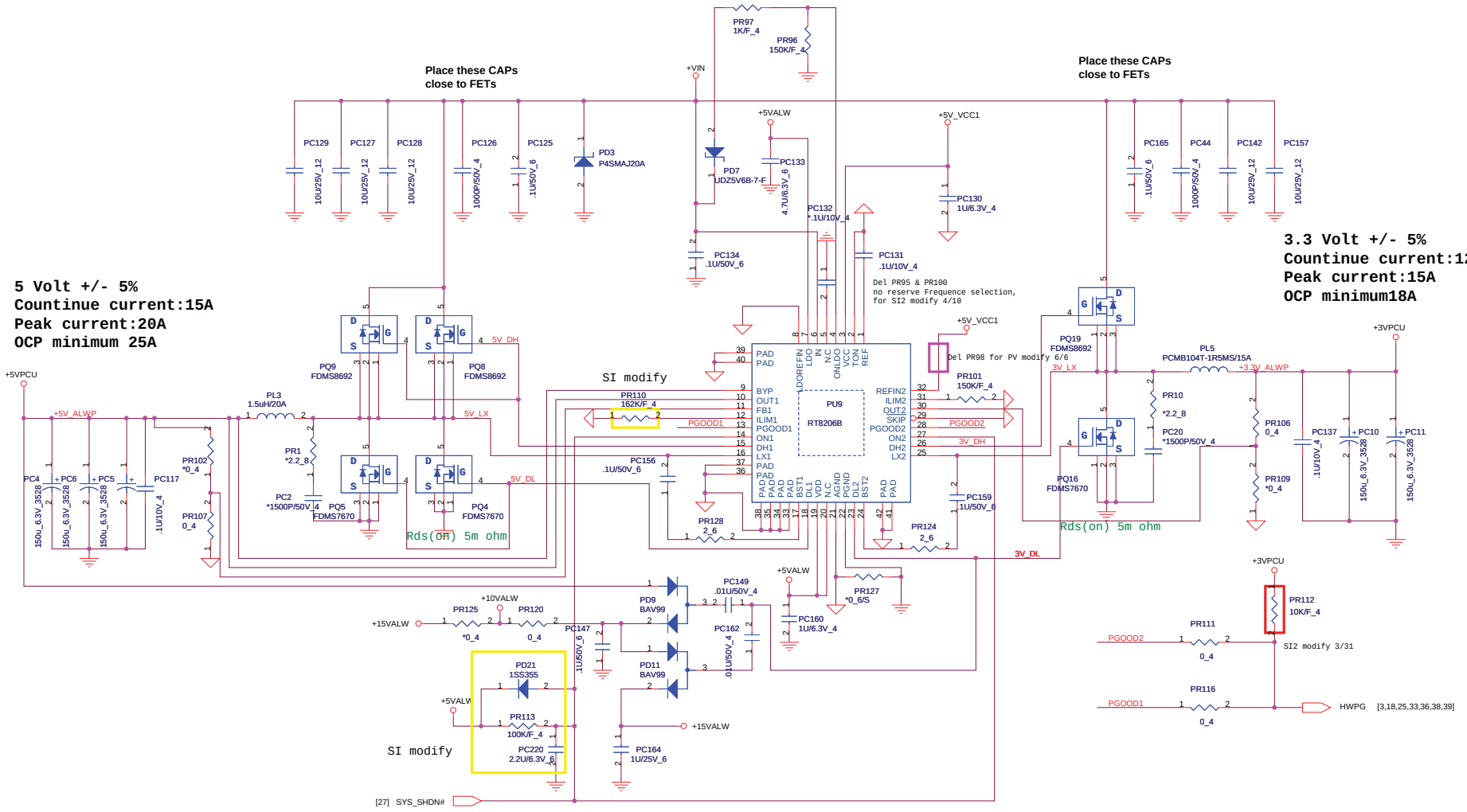
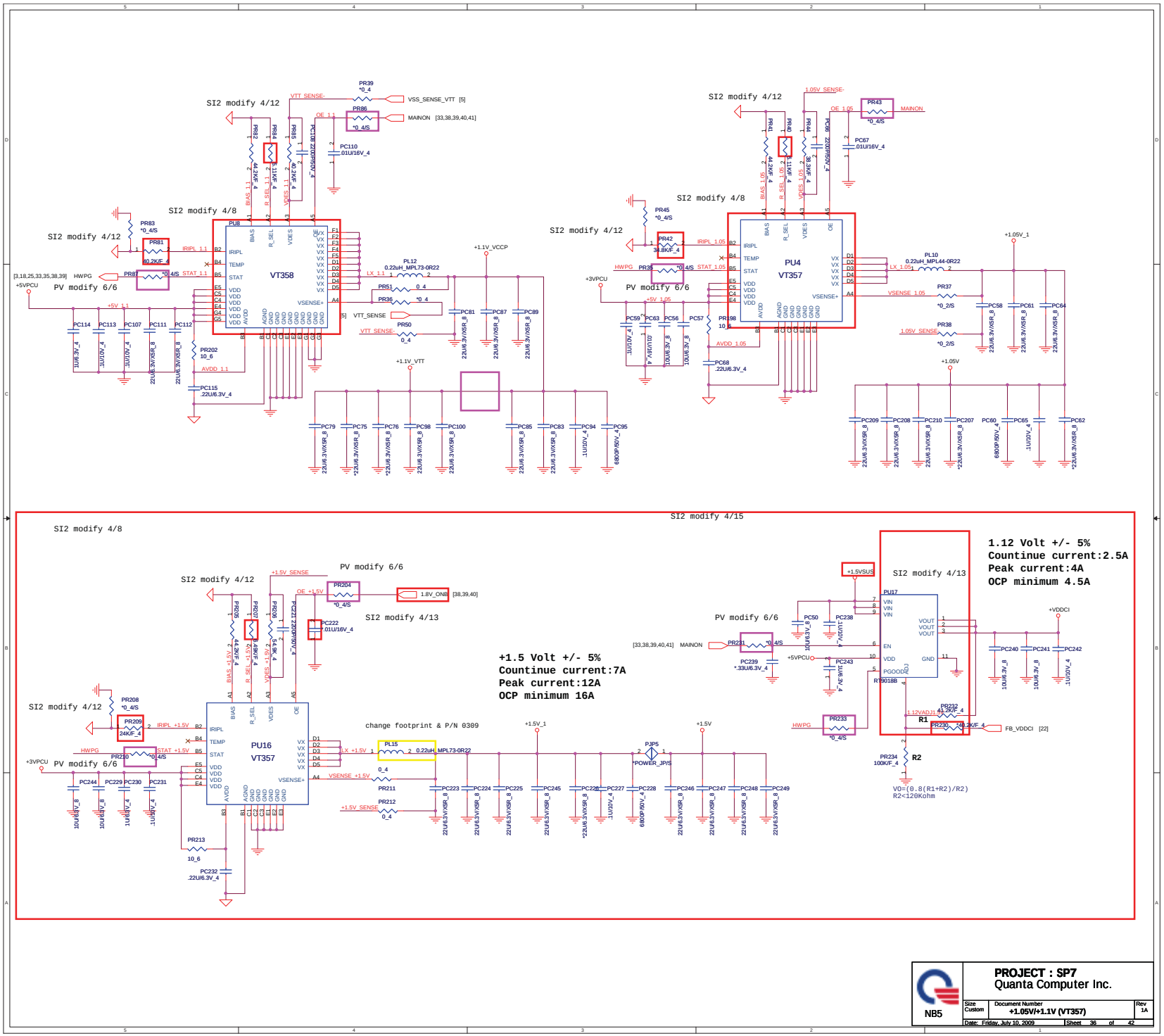
PROJECT : SP7
Quanta Computer Inc.
NB5

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW



NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 1A
Date: Friday, July 10, 2009	Sheet 35 of 42	


SI2 modify 4/12
SI2 modify 4/8
PU8
VT358
PV modify 6/6
SI2 modify 4/12
PU4
VT357
SI2 modify 4/8
PV modify 6/6
SI2 modify 4/15
SI2 modify 4/8
SI2 modify 4/12
PV modify 6/6
SI2 modify 4/13
SI2 modify 4/12
SI2 modify 4/13
PV modify 6/6
PU16
VT357
change footprint & P/N 0309
PU17
R19018B
1.12 Volt +/- 5%
Countinue current:2.5A
Peak current:4A
OCP minimum 4.5A
+1.5 Volt +/- 5%
Countinue current:7A
Peak current:12A
OCP minimum 16A
V0=(0.8(R1+R2)/R2)
R2<120Kohm
PROJECT : SP7
Quanta Computer Inc.
NB5
Size Custom
Document Number
+1.05V/+1.1V (VT357)
Rev 1A
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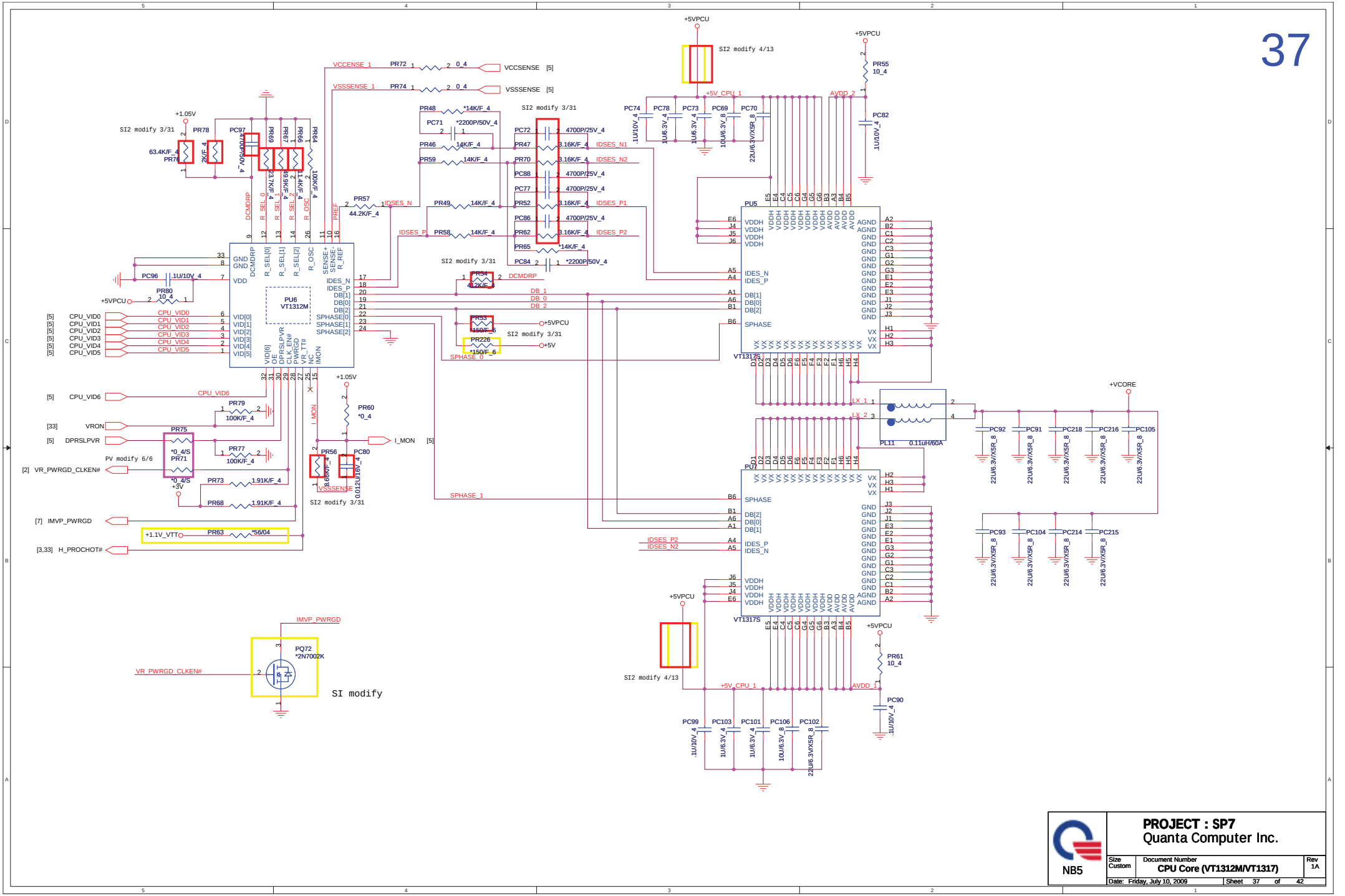

NB5	**PROJECT : SP7** Quanta Computer Inc.	
Size: Custom	Document Number: CPU Core (VT1312M/VT1317)	Rev: 1A
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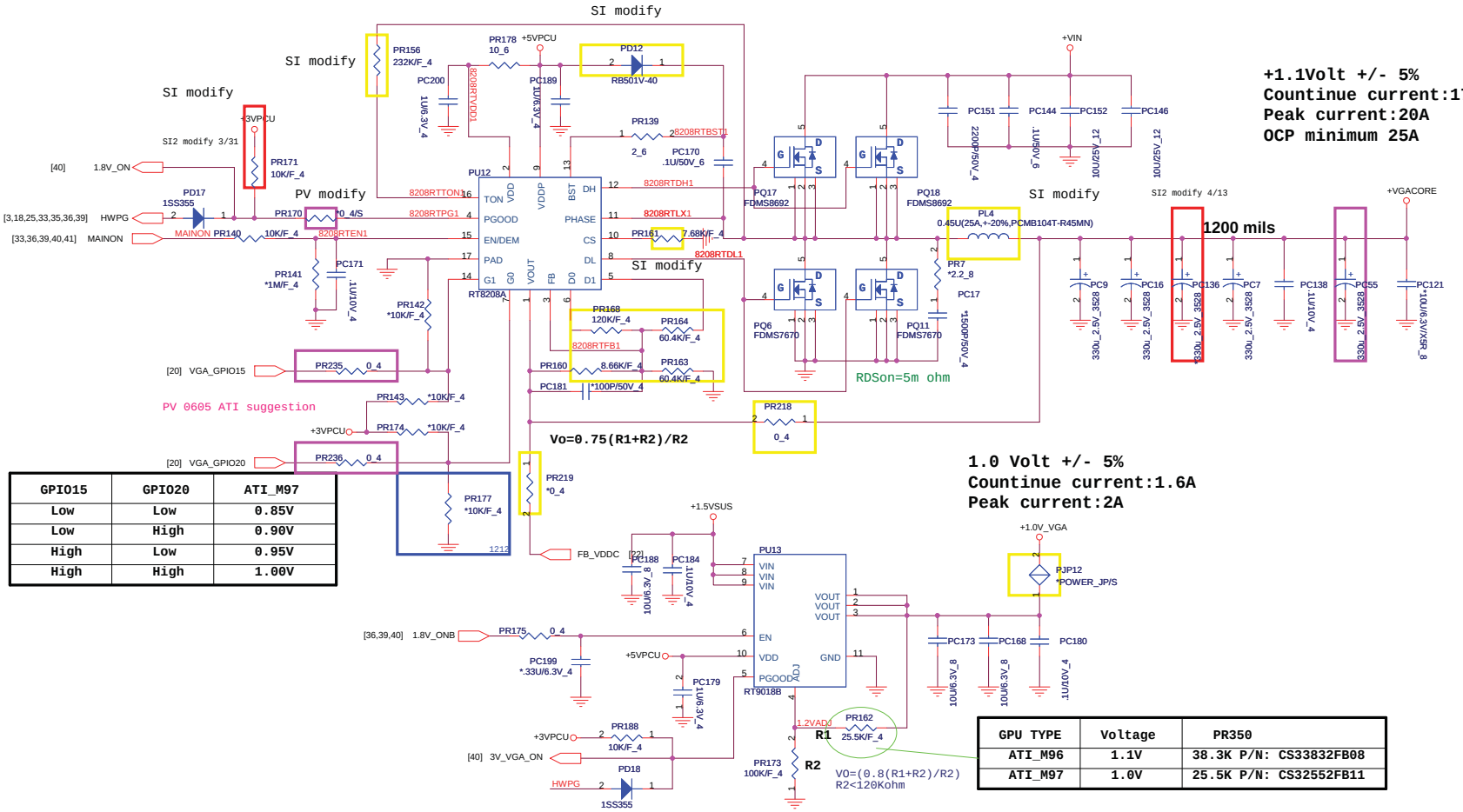
VGA Core & VCC1.1



GPIO15	GPIO20	ATI_M97
Low	Low	0.85V
Low	High	0.90V
High	Low	0.95V
High	High	1.00V

GPU TYPE	Voltage	PR350
ATI_M96	1.1V	38.3K P/N: CS33832FB08
ATI_M97	1.0V	25.5K P/N: CS32552FB11

NB5

PROJECT : SP7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA Core (RT8208)	1A

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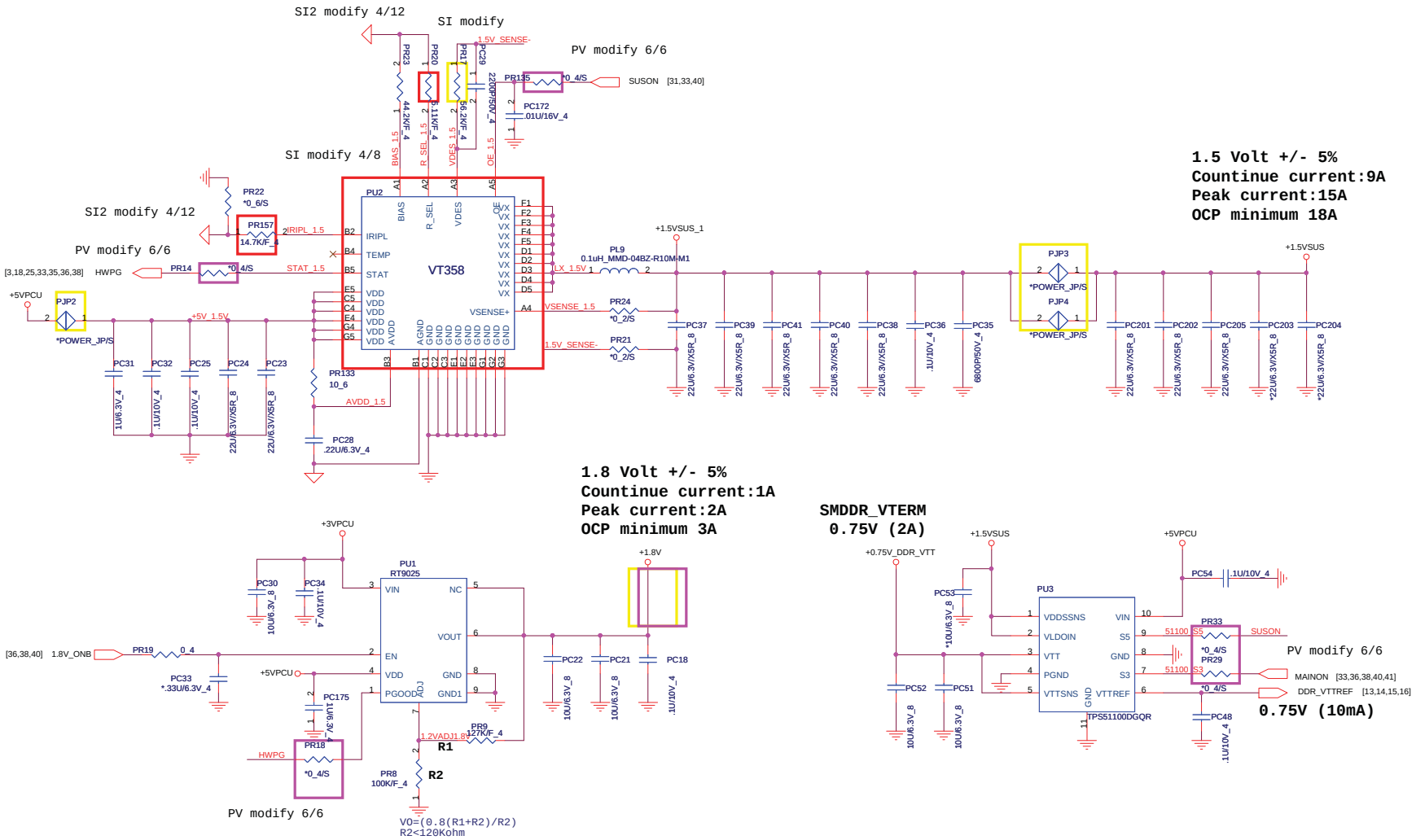

NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3/1.8V (VT356/VT357)	Rev: 1A
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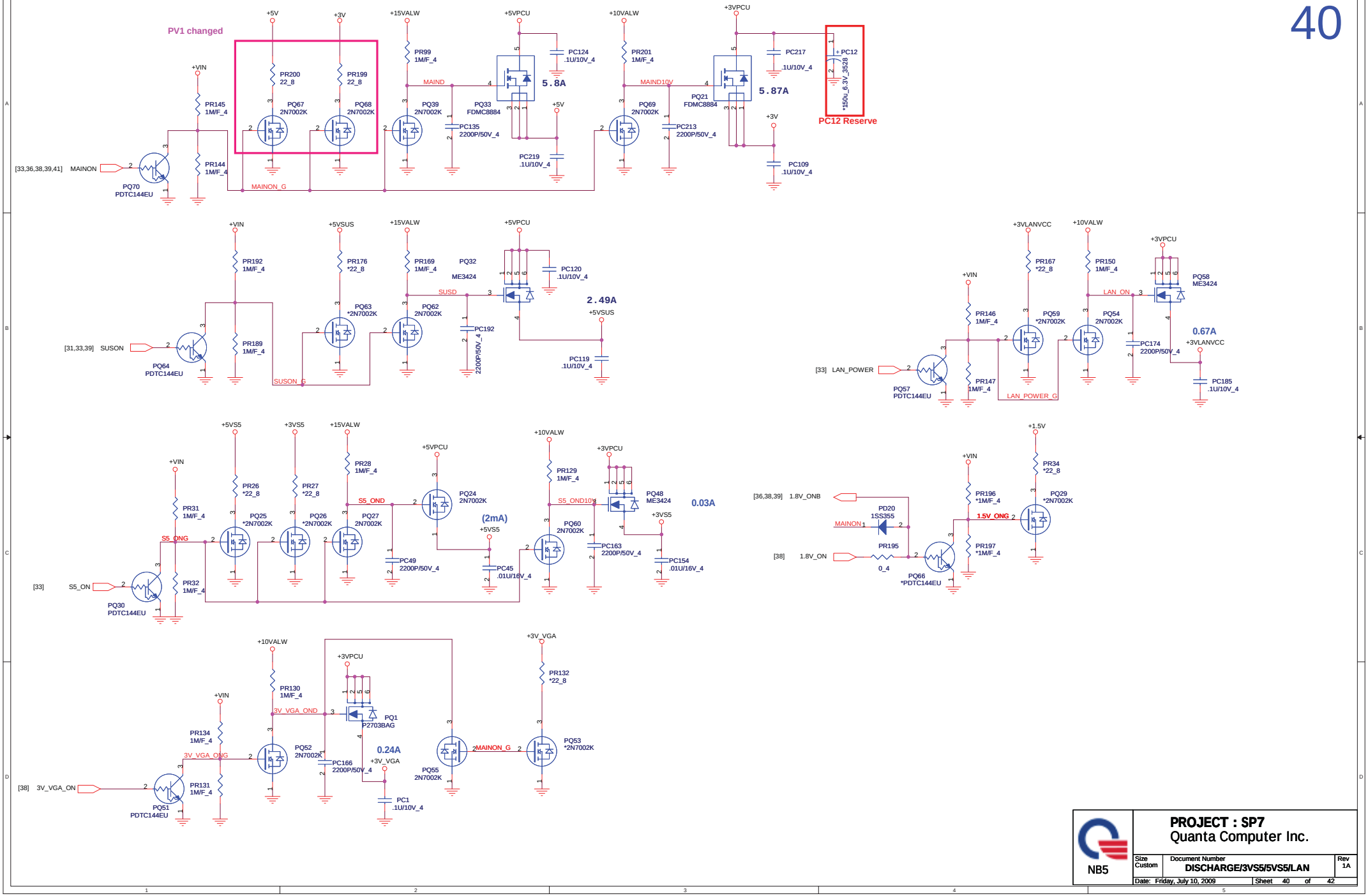

NB5	**PROJECT : SP7** Quanta Computer Inc.	
	Size: Custom Document Number: **DISCHARGE/3VS5/5VS5/LAN**	Rev: 1A
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TOP DC_JACK
65W/90W

41

SI2 modify 4/8

PV2 modify 7/7

SI2 modify 3/31

SI modify

PV 0526 MODIFY

Setting the Vin min to 12V For ACSET 2.4V

V ACLIM Setting ACSET=[(Iadaptor*3.3*Rsense)/0.1]

Charging Curret setting I_CHARGE=(Vsreset/ Vref)*(0.1/Rsns)

Battery Low = 8V

CELL_SLT = 1 -- 3 S (Cells = GND 3S)
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)

Input Current monitor V icm = 20 * (Vcsip - Vcsin)

SI-2 modify 4/15

SI-2 modify 4/16

NB5	PROJECT : SP7 Quanta Computer Inc.	
Size Custom	Document Number Charger (BQ24704)	Rev 1A
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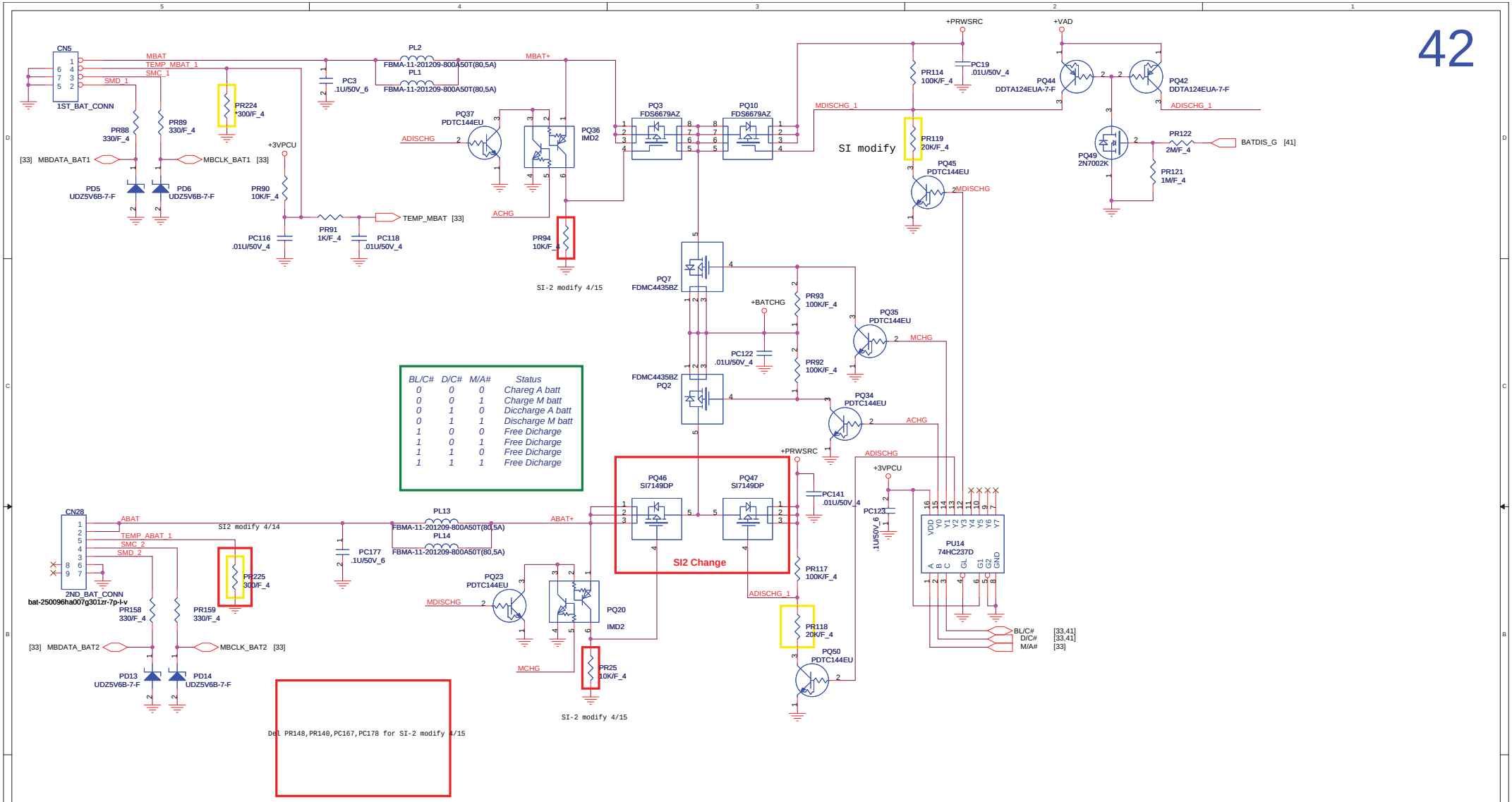

BL/C#	D/C#	M/A#	Status
0	0	0	Chareg A batt
0	0	1	Charge M batt
0	1	0	Diccharge A batt
0	1	1	Discharge M batt
1	0	0	Free Dicharge
1	0	1	Free Dicharge
1	1	0	Free Dicharge
1	1	1	Free Dicharge

NB5	PROJECT : SP7 Quanta Computer Inc.	
Size: Custom	Document Number: BATTERY SELECTOR	Rev: 1A
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