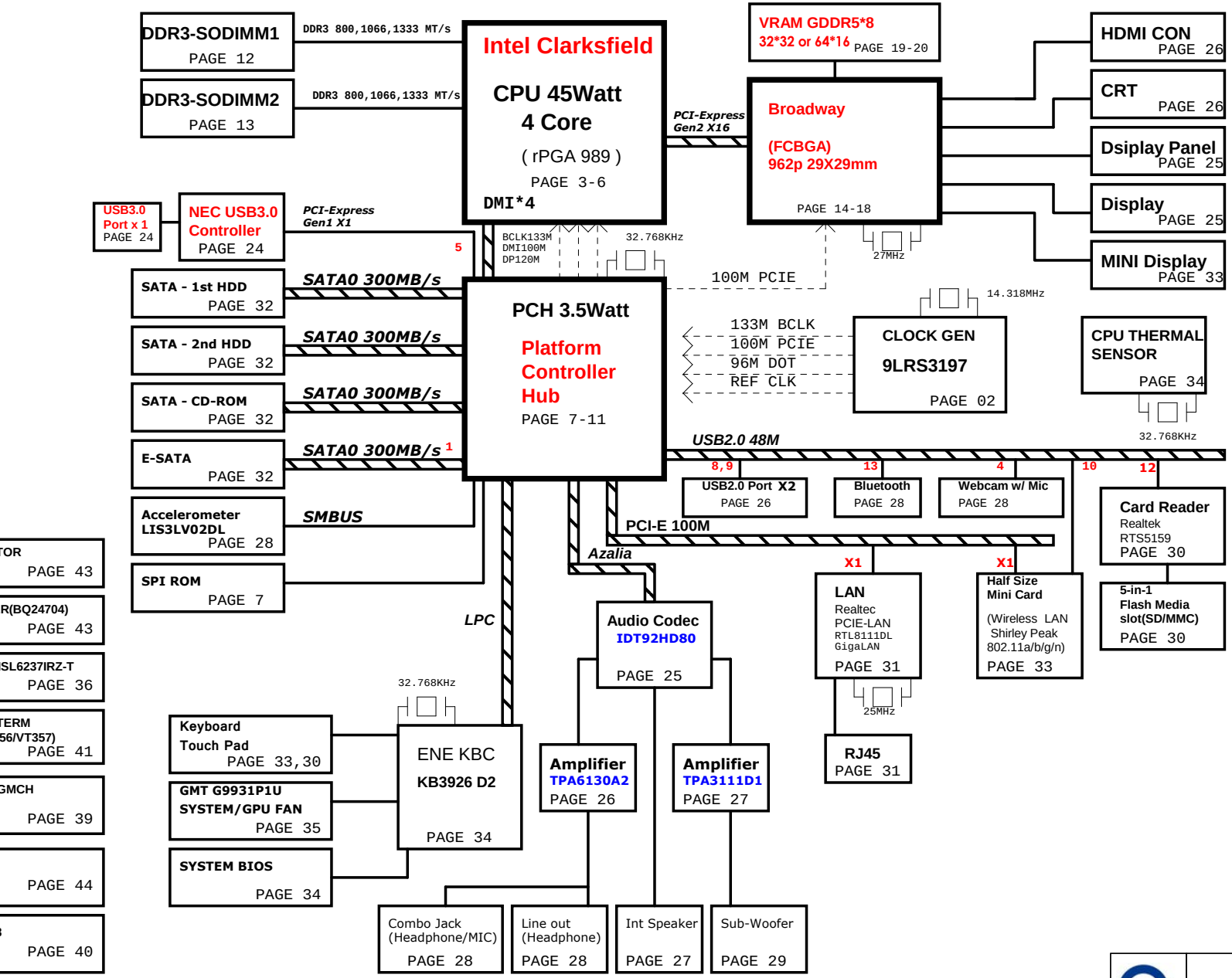
SP8 BLOCK DIAGRAM

01

PCB STACK UP

Discrete 6L

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(High)
LAYER 5 : SVCC
LAYER 6 : Bottom



BATTERY SELECTOR PAGE 43

SYSTEM CHARGER(BQ24704) PAGE 43

SYSTEM POWER ISL6237IRZ-T PAGE 36

DDR III SMDDR_VTERM 1.8V/1.8VSUS(VT356/VT357) PAGE 41

VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 39

VDDCI RT8209A PAGE 44

VGACORE RT8208 PAGE 40

CPU CORE VT1312M/VT1317 PAGE 38

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	3A

NB5/RD2

Date: Thursday, August 05, 2010 Sheet 1 of 47

+1.05V 7,8,9,11,37,38
+1.5V 35,42
+3V 3,7,8,9,10,11,12,13,14,17,25,26,27,28,30,31,32,33,34,35,38,40,42

25mA
+1.05V L57 HCB1608KF-181T15_6 +VDDIO_CLK
C433 0.1U/10V_4
C815 0.1U/10V_4
C813 10U/6.3V_6S
C434 *10U/6.3V_8S
Place each 0.1uF cap close to pin

150mA
+3V L29 HCB1608KF-181T15_6 +VDDSE_CLK
C458 4.7U/6.3V_6
C447 0.1U/10V_4
C454 0.1U/10V_4
Place each 0.1uF cap close to pin

150mA
+3V L58 *HCB1608KF-181T15_6 +VDDCORE_CLK
+1.5V L28 HCB1608KF-181T15_6
C418 4.7U/6.3V_6
C427 0.1U/10V_4
C453 0.1U/10V_4
C818 0.1U/10V_4
Place each 0.1uF cap close to pin

change to power saving
CLK need change to +1.5V
support

SI Add C479 and C469 for EMI request

+VDDIO_CLK C479 0.1U/10V_4
+VDDCORE_CLK C469 0.1U/10V_4

U17
9LRS3197
QFN32
RTM875N-632-VB-GRT

+VDDSE_CLK → VDD_LCD, VDD_REF
+VDDCORE_CLK → VDD_USB, VDD_SRC, VDD_CPU
+VDDIO_CLK → VDD_CPU_IO, VDD_SRC_IO
8,12,13,28 CGDAT_SMB → SDATA
8,12,13,28 CGCLK_SMB → SCLK
+3V R261 10K/F_4
8 CLK_ICH_14M R267 33_4 CPU_SEL → CPU_STOP#, REF_0/CPU_SEL
C451 *10P/50V_4
CK_PWRGD_R → CK_PWRGD/PD#_3.3
XTAL_OUT, XTAL_IN → XOUT, XIN
VSS_SATA, VSS_USB, VSS_LCD

CPU-0 23 CLK_BUF_BCLK_P_R
CPU-0# 22 CLK_BUF_BCLK_N_R
CPU-1 20
CPU-1# 19
DOT96T_LPR 3 CLK_BUF_DREFCLK_R
DOT96C_LPR 4 CLK_BUF_DREFCLK#_R
SRC-1 13 CLK_BUF_PCIE_3GPLL_R
SRC-1# 14 CLK_BUF_PCIE_3GPLL#_R
SATA 10 CLK_BUF_DREFSSCLK_R
SATA# 11 CLK_BUF_DREFSSCLK#_R
27MHz_nonSS 6 CLK_VGA_27M_NOSS
27MHz_SS 7 CLK_VGA_27M_SS
GND 33, 26, 21, 12
VSS_REF, VSS_CPU, VSS_SRC

Place within 0.5" of C/G
RP2 4P2R-S-0 → CLK_BUF_BCLK_P 8, CLK_BUF_BCLK_N 8
RP6 4P2R-S-0 → CLK_BUF_DREFCLK 8, CLK_BUF_DREFCLK# 8
RP3 4P2R-S-0 → CLK_BUF_PCIE_3GPLL 8, CLK_BUF_PCIE_3GPLL# 8
RP5 4P2R-S-0 → CLK_BUF_DREFSSCLK 8, CLK_BUF_DREFSSCLK# 8
R273 33_4
R274 *33_4
27Mhz SS/NOSS option.
CLK_27M_NONSS 17

Place R8044 within 0.5" of C/G

Y5 14.318MHZ
XTAL_IN — C443 33P/50V_4
XTAL_OUT — C438 33P/50V_4

+3V R272 *10K/F_4 CPU_SEL
R270 10K/F_4

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

+3V R260 1K/F_4 CK_PWRGD_R
Q15 2N7002E
38 VR_PWRGD_CLKEN# R262 100K/F_4

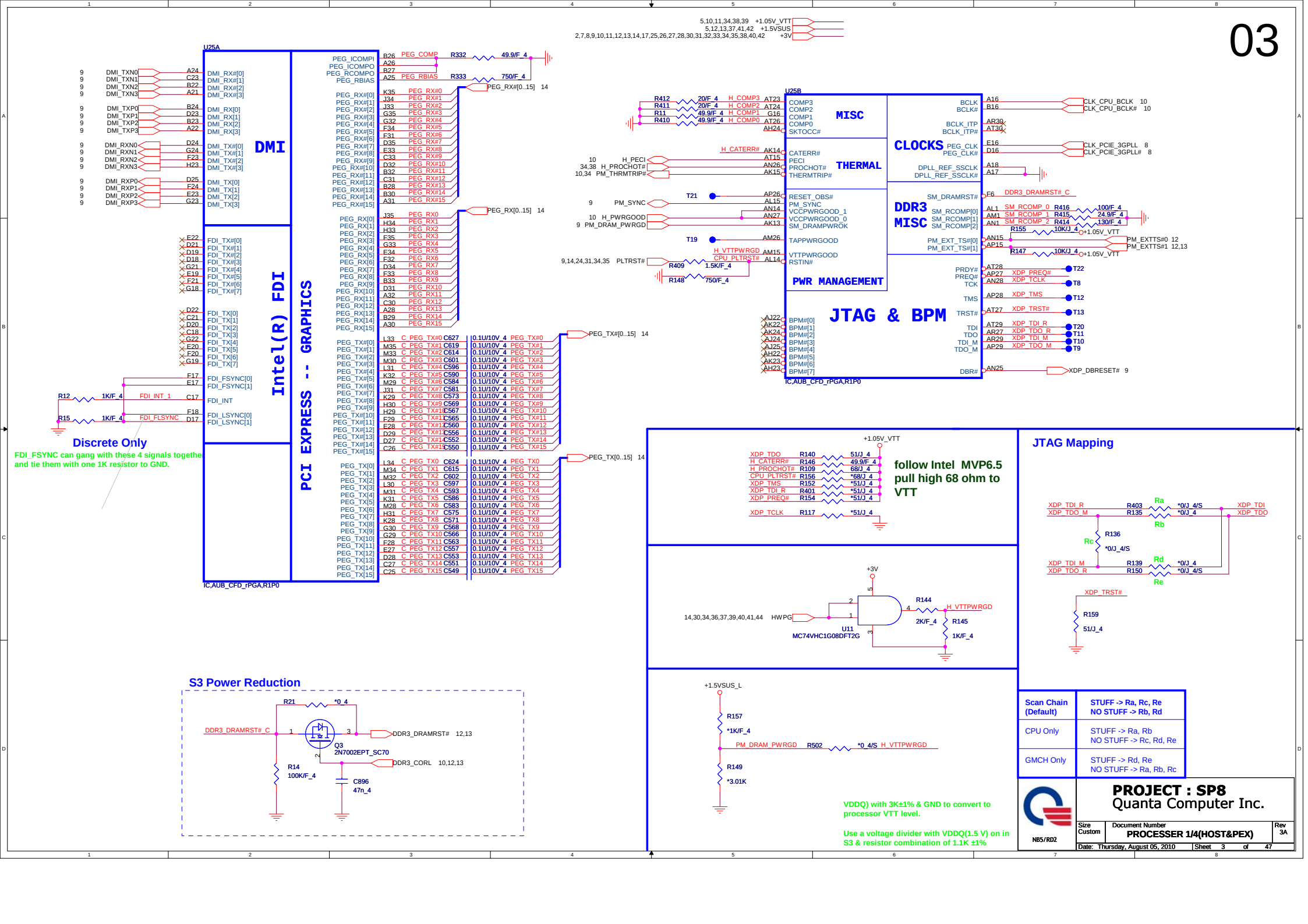
HOLDs

for GPU: H7, H18, H15, H17, H11, H16
for CPU: H8, H21, H14, H20, H13, H12, H5, H6

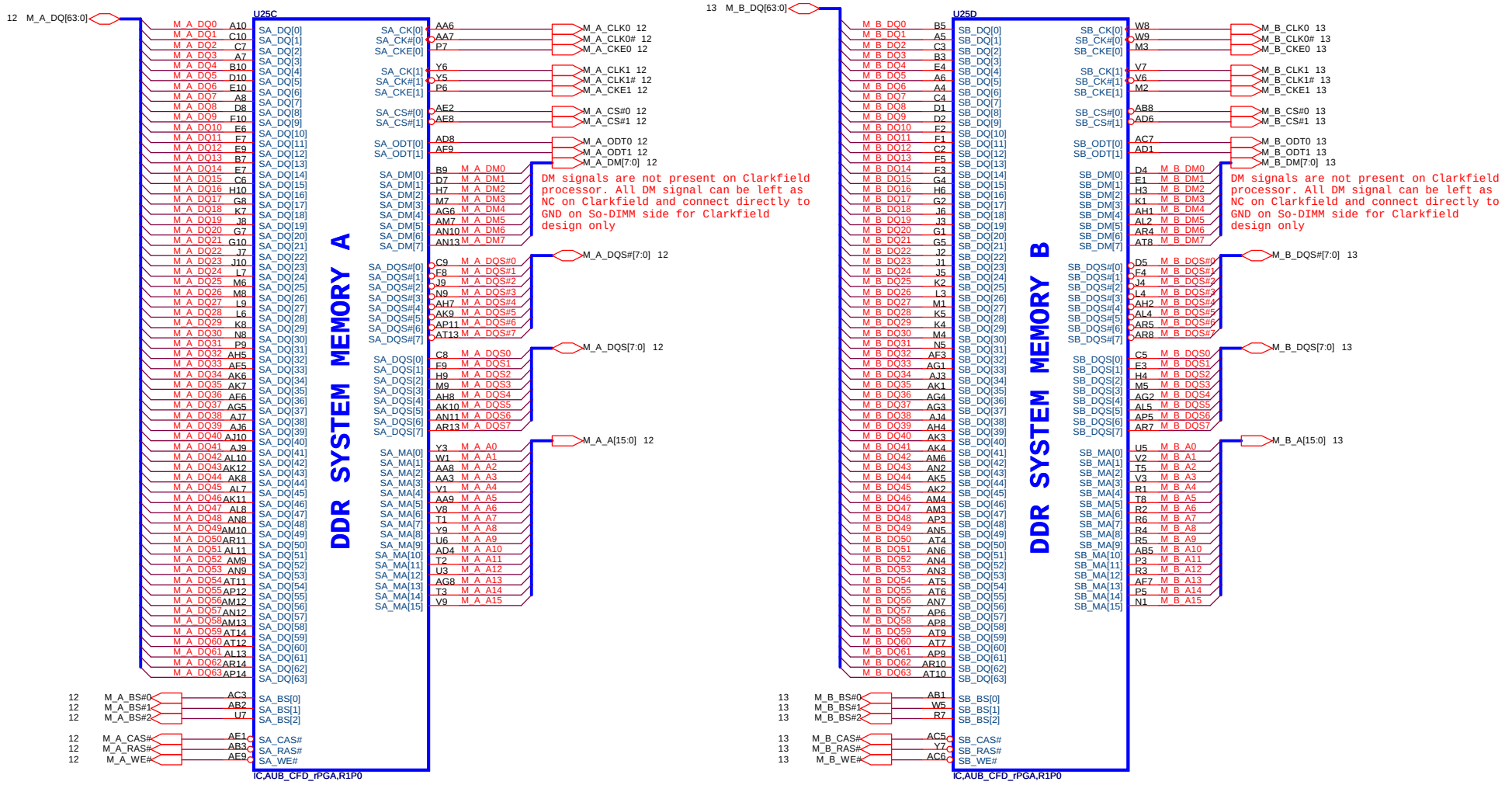
SI ME change Footprint: H9, H10
SI for ME change footprint: H1, H2, H3, H4, H19
SI add for PCH hole: H22, H23

*h-c236d118p2

NB5/RD2	PROJECT : SP8 Quanta Computer Inc.		
	Size: Custom	Document Number: Clock Gen(9LRS3197)/HOLES	Rev: 3A
	Date: Thursday, August 05, 2010	Sheet 2 of 47	


U25A
DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS
IC,AUB_CFD_rPGA,R1P0
U25B
MISC
THERMAL
CLOCKS
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
IC,AUB_CFD_rPGA,R1P0
Discrete Only
FDI_FSYNC can gang with these 4 signals together and tie them with one 1K resistor to GND.
follow Intel MVP6.5 pull high 68 ohm to VTT
JTAG Mapping
S3 Power Reduction
Q3
2N7002EPT_SC70
U11
MC74VHC1G08DFT2G
VDDQ) with 3K±1% & GND to convert to processor VTT level.
Use a voltage divider with VDDQ(1.5 V) on in S3 & resistor combination of 1.1K ±1%
Scan Chain (Default)
STUFF -> Ra, Rc, Re
NO STUFF -> Rb, Rd
CPU Only
STUFF -> Ra, Rb
NO STUFF -> Rc, Rd, Re
GMCH Only
STUFF -> Rd, Re
NO STUFF -> Ra, Rb, Rc
PROJECT : SP8
Quanta Computer Inc.
NB5/RD2
Size Custom
Document Number
PROCESSER 1/4(HOST&PEX)
Rev 3A
Date: Thursday, August 05, 2010
Sheet 3 of 47

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

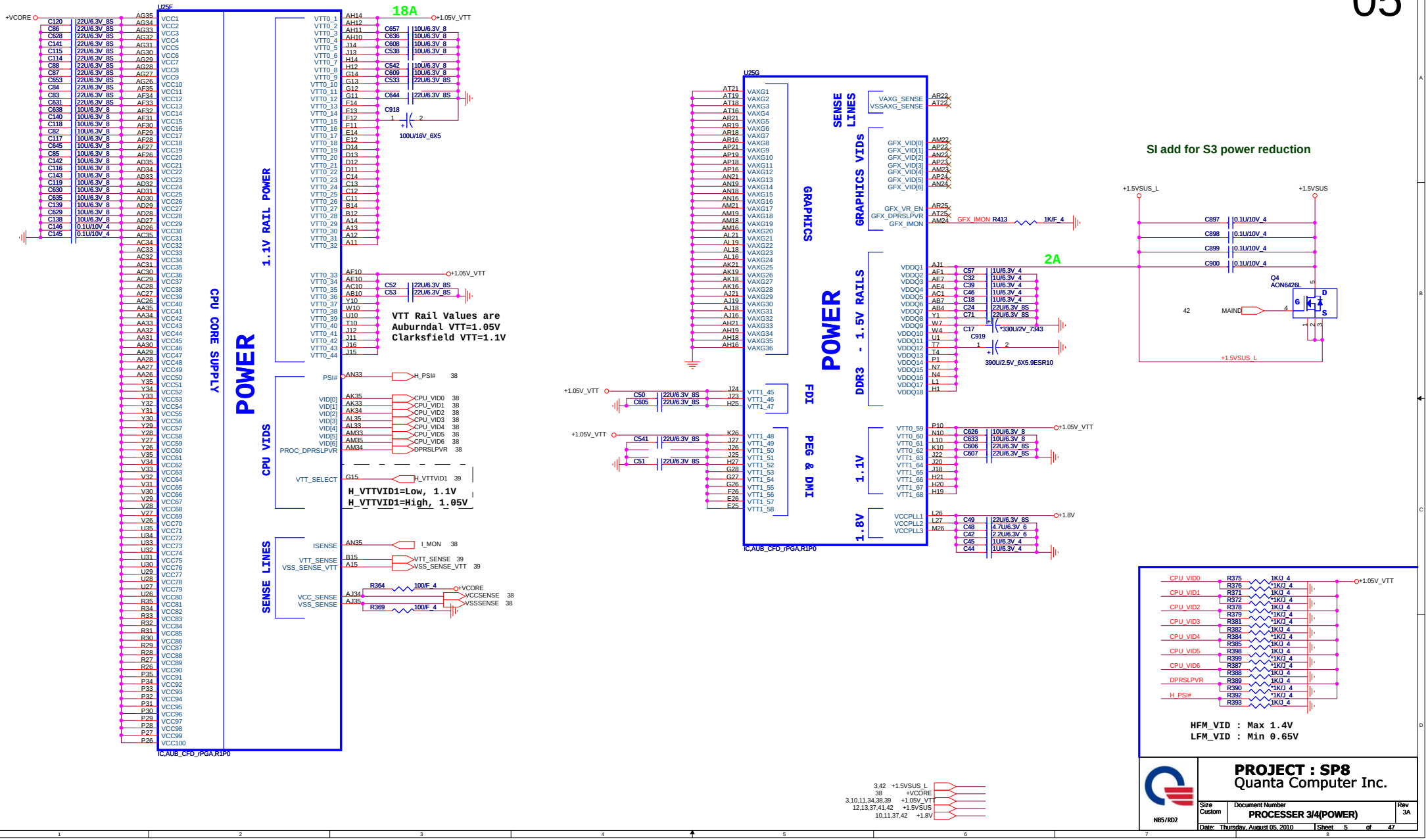


NB5/RD2

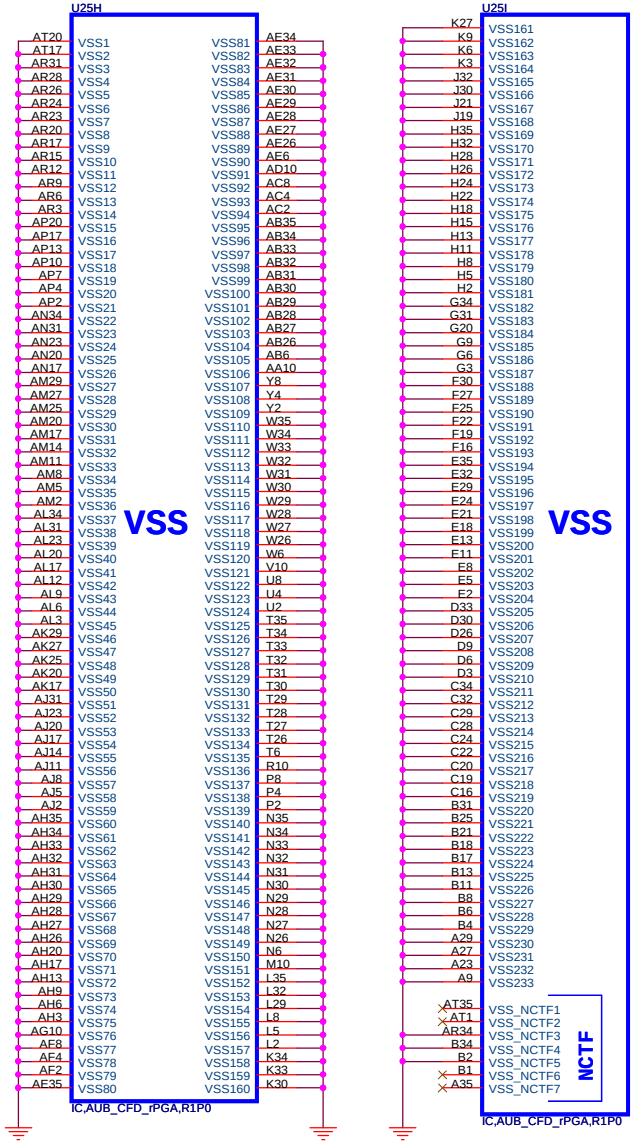
PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 2/4(DDR)	3A

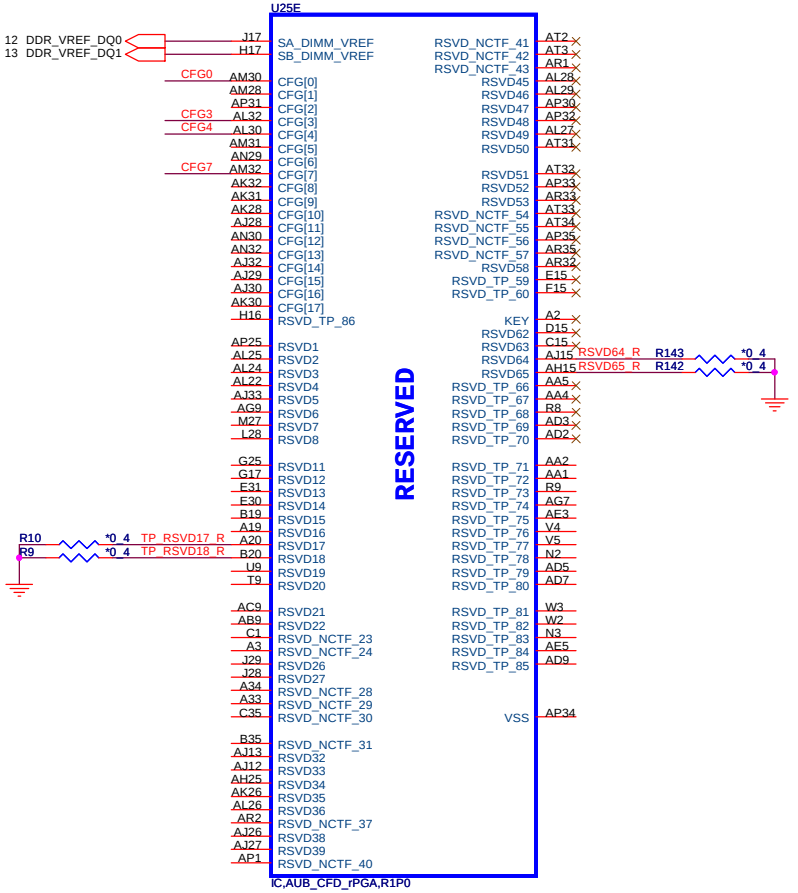
Date: Thursday, August 05, 2010 Sheet 4 of 47


U25F
POWER
CPU CORE SUPPLY
1.1V RAIL POWER
CPU VIDS
SENSE LINES
IC,AUB_CFD_rPGA,R1P0
18A
+VCORE
+1.05V_VTT
VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V
H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V
U25G
POWER
GRAPHICS
SENSE LINES
GRAPHICS VIDs
DDR3 - 1.5V RAILS
FDI
PEG & DMI
1.1V
1.8V
IC,AUB_CFD_rPGA,R1P0
2A
SI add for S3 power reduction
+1.5VSUS_L
+1.5VSUS
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
PROJECT : SP8
Quanta Computer Inc.
PROCESSER 3/4(POWER)
Size Custom
Rev 3A
Date: Thursday, August 05, 2010
Sheet 5 of 47
N85/RD2

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



For Discrete only

CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

PROJECT : SP8
Quanta Computer Inc.

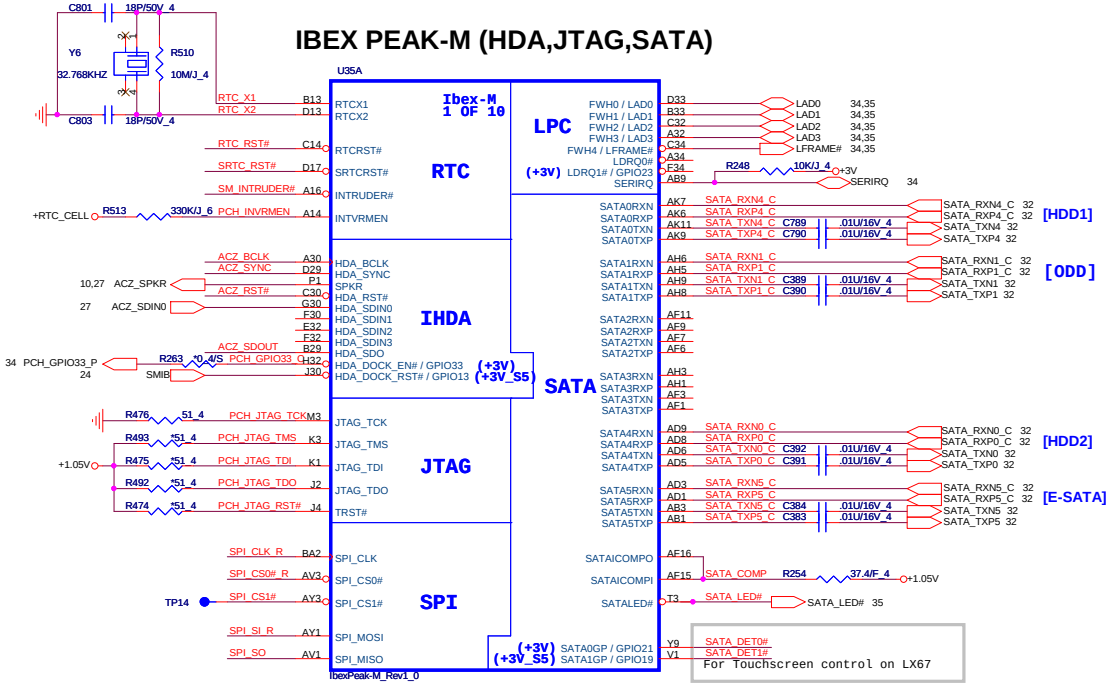
Size	Document Number	Rev
Custom	PROCESSER 4/4 (GND)	3A

NB5/RD2

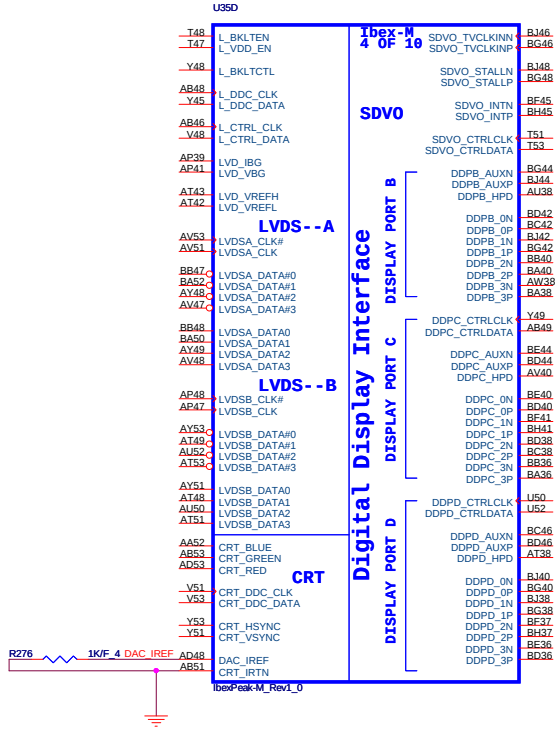
Date: Thursday, August 05, 2010 Sheet 6 of 47

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

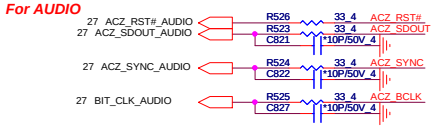


IBEX PEAK-M (LVDS,DDI)

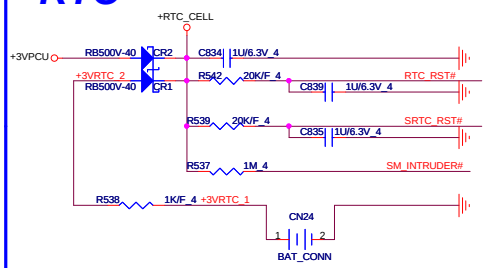


The SATALED# signal is open-collector
and requires a weak external pull-up
(8.2 k to 10 k) to +V3.3

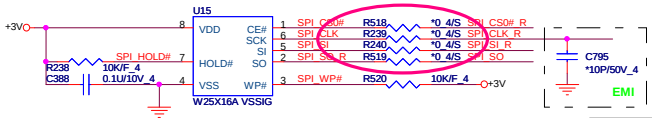
For AUDIO



RTC 1mA



4M byte SPI ROM



2,8,9,11,37,38 +1.05V
2,3,8,9,10,11,12,13,14,17,25,26,27,28,30,31,32,33,34,35,38,40,42 +3V
25,30,33,34,35,36,37,39,40,42,43 +3VPCU

Socket DG008000031
MXIC AKE39FP0Z00
WINBOND AKE391P0N00

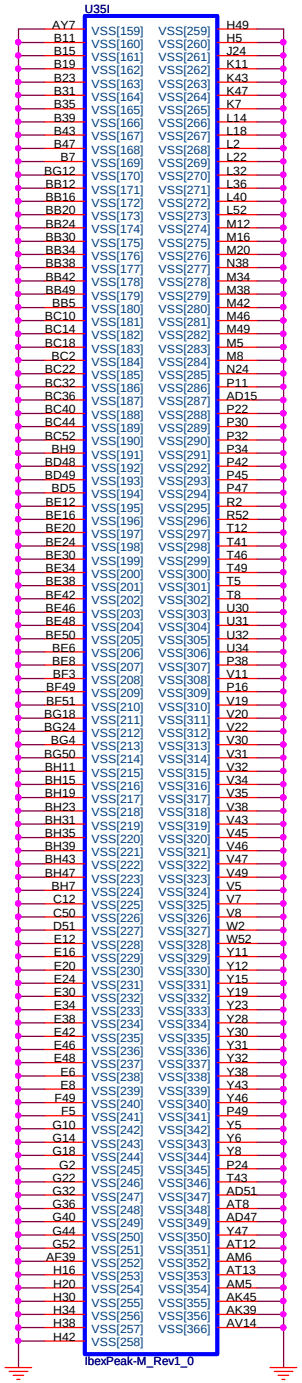
PROJECT : SP8
Quanta Computer Inc.

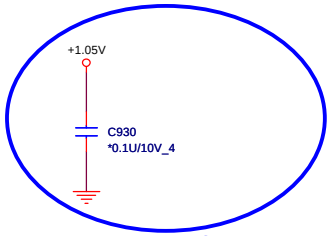
NB5/RD2

Size	Document Number	Rev
Custom	PCH 1/5 (SATA,HDA,LPC)	3A

Date: Thursday, August 05, 2010 Sheet 7 of 47

IBEX PEAK-M (GND)





SP81.1 SI for RF reserve

IBEX PEAK-M (PCI-E,SMBUS,CLK)

08

U35B

Ibex-M 2 OF 10

PCI-E*

[WLAN] [LAN] [USB3.0]

SMBus
(+3V_S5) SMBALERT# / GPIO11
SMBCLK
SMBDATA
(+3V_S5) SML0ALERT# / GPIO60
SML0CLK
SML0DATA
(+3V_S5) SML1ALERT# / GPIO74
(+3V_S5) SML1CLK / GPIO58
(+3V_S5) SML1DATA / GPIO75

Controller Link
CL_CLK1
CL_DATA1
CL_RST1#

PEG
(+3V_S5) PEG_A_CLKRQ# / GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P

From CLK BUFFER
CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_BCLK_N
CLKIN_BCLK_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N / CKSSCD_N
CLKIN_SATA_P / CKSSCD_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP

Clock Flex
(+3V) CLKOUTFLEX0 / GPIO64
(+3V) CLKOUTFLEX1 / GPIO65
(+3V) CLKOUTFLEX2 / GPIO66
(+3V) CLKOUTFLEX3 / GPIO67

Intel recommendation

IbexPeak-M_Rev1_0

+3VS5

CLK1_OE# R498 10K/J_4
CLK2_OE# R495 10K/J_4
PCIE_CLK_REQ0# R215 10K/J_4
PCIE_CLK_REQ3# R487 10K/J_4
PCIE_CLK_REQ4# R227 10K/J_4
PCIE_CLK_REQ8# R214 10K/J_4
PCIE_CLK_REQ5# R472 10K/J_4
PEG_CLKREQ# R491 10K/J_4

Q45 2N7002E
SMB_CLK_ME1 3 — MBCLK2 12,17,25,34
Q46 2N7002E
SMB_DATA_ME1 3 — MBDATA2 12,17,25,34
Q43 2N7002E
PDAT_SMB 3 — CGDAT_SMB 2,12,13,28
R485 10K/F_4
R486 10K/F_4
Q44 2N7002E
PCLK_SMB 3 — CGCLK_SMB 2,12,13,28

Q55 2N7002E
Q56 2N7002E
Q57 2N7002E
Q54 2N7002E
C543 0.1U/10V_4
C544 0.1U/10V_4
C547 0.1U/10V_4
AMP_SDA 28
AMP_SCL 28

SI for HP AMP

2,7,9,11,37,38 +1.05V
2,3,7,9,10,11,12,13,14,17,25,26,27,28,30,31,32,33,34,35,38,40,42 +3V
7,25,30,33,34,35,36,37,39,40,42,43 +3VPCU

XTAL25_IN — C843 *18P/50V_4
R540 *1M/F_4
Y7 *25MHZ
XTAL25_OUT — C838 *18P/50V_4

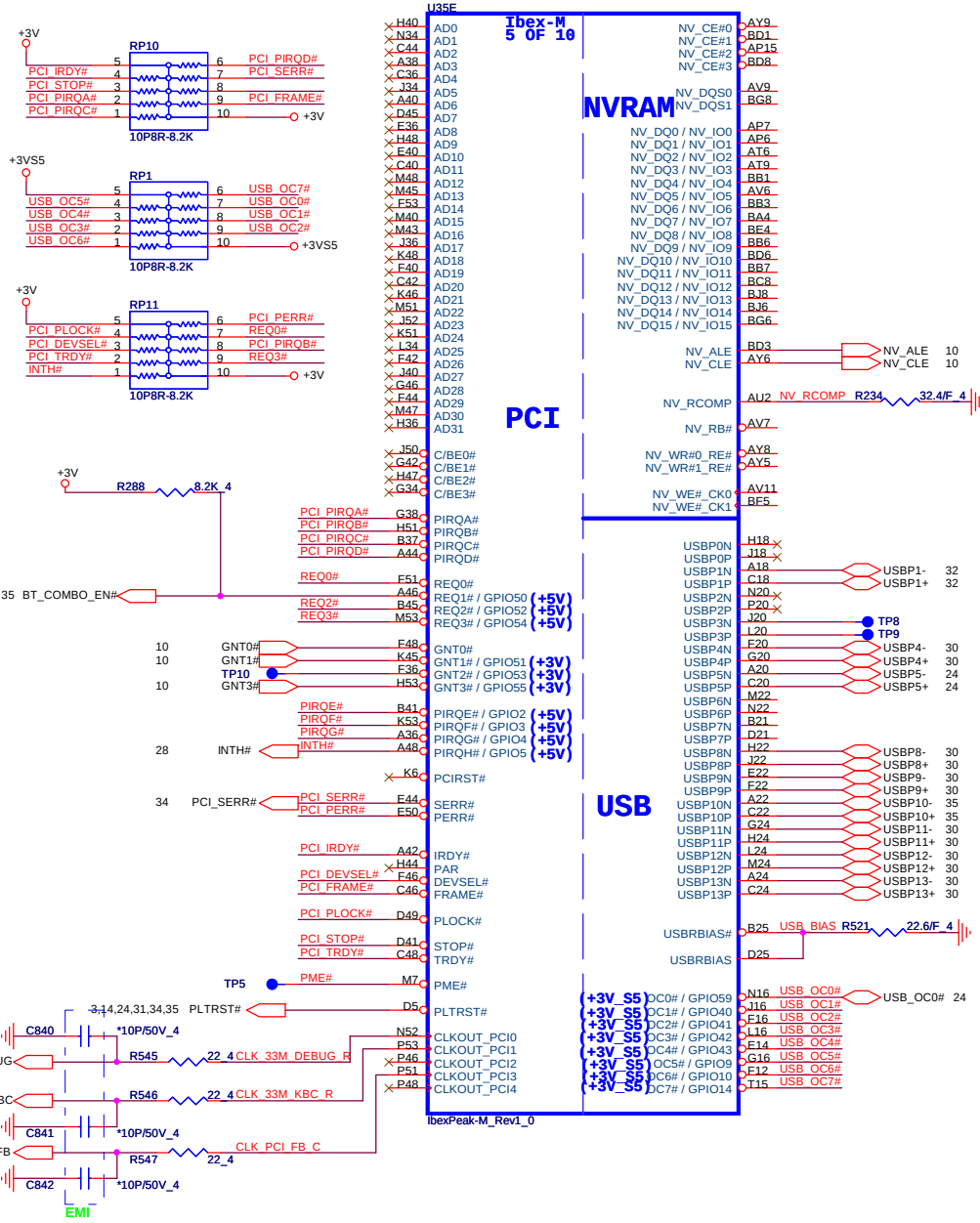
NB5/RD2

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/5 (PCIE, SMBUS, CK)	3A

Date: Thursday, August 05, 2010 Sheet 8 of 47

IBEX PEAK-M (PCI,USB,NVRAM)

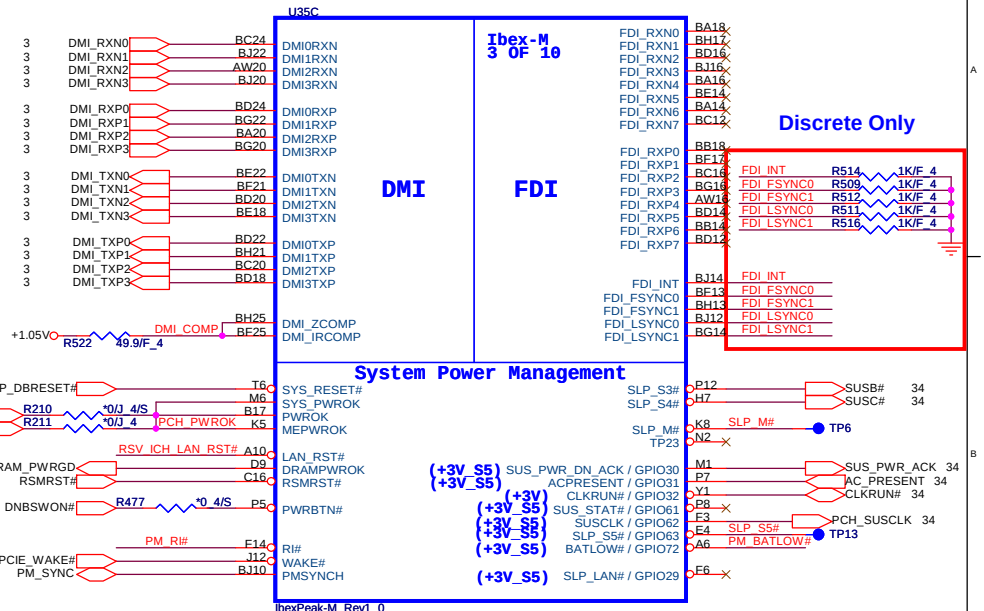


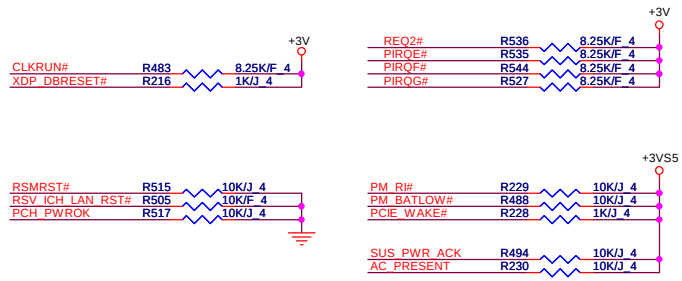
[E-SATA]
[Fingerprint]
[Touch screen]
[Webcam]
[USB 3.0 Co-layout]

[Right USB #1]
[Right USB #2]
[WLAN]
[Blue Tooth Front]
[Card Reaer]
[Blue Tooth LCD]

USB 3.0 OC#

IBEX PEAK-M (DMI,FDI,GPIO)





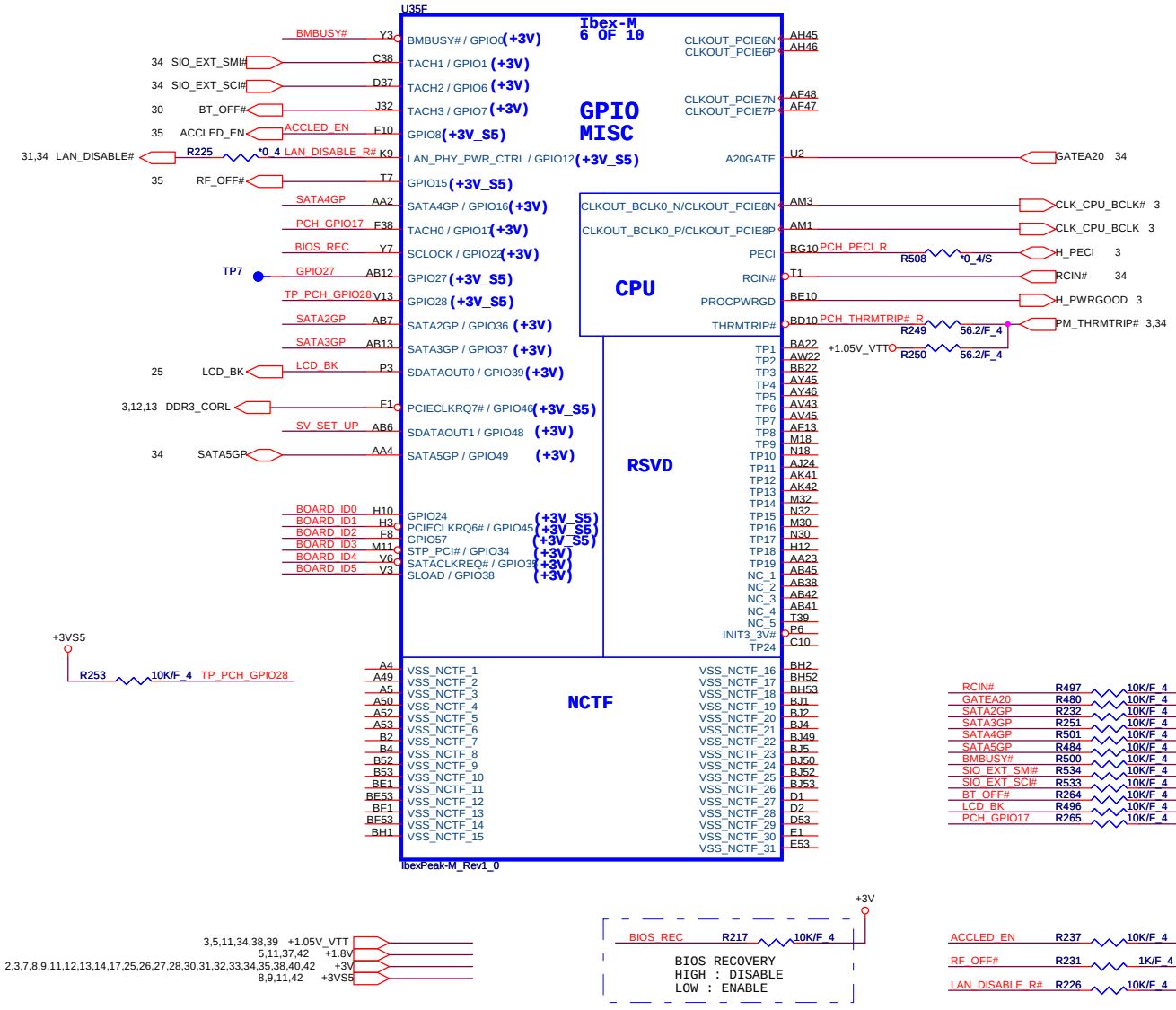
2,7,8,11,37,38 +1.05V
2,3,7,8,10,11,12,13,14,17,25,26,27,28,30,31,32,33,34,35,38,40,42 +3V
8,10,11,42 +3VS5

NB5/RD2

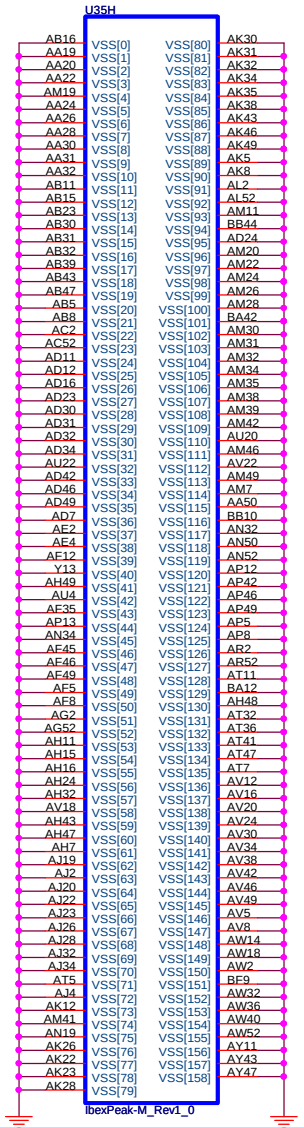
PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 3/5 (PCI,ONFI,USB,DMI)	3A
Date: Thursday, August 05, 2010	Sheet 9 of 47	

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



9 GNT3# R543 *10K_NC

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP R218 10K/F_4 +3V

SV_SET_UP	1-X High = Strong (Default)

9 GNT0# R269 *1K/F_4
9 GNT1# R268 *1K/F_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

9 NV_ALE R506 *1K/F_4 +1.8V
9 NV_CLE R507 *1K/F_4

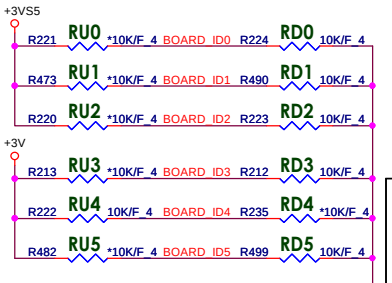
Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

BOARD ID SETTING

Board ID	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

Board ID	ID0 GPIO 24	ID1 GPIO 45	ID2 GPIO 57	ID3 GPIO 34	ID4 GPIO 35	ID5 GPIO 38
SP8	0	0			0	0
SP8 1.1	0	0			1	0
Discrete			0	0		
Reserve			0	0		
ROM Size				0= 4M 1= 2M		



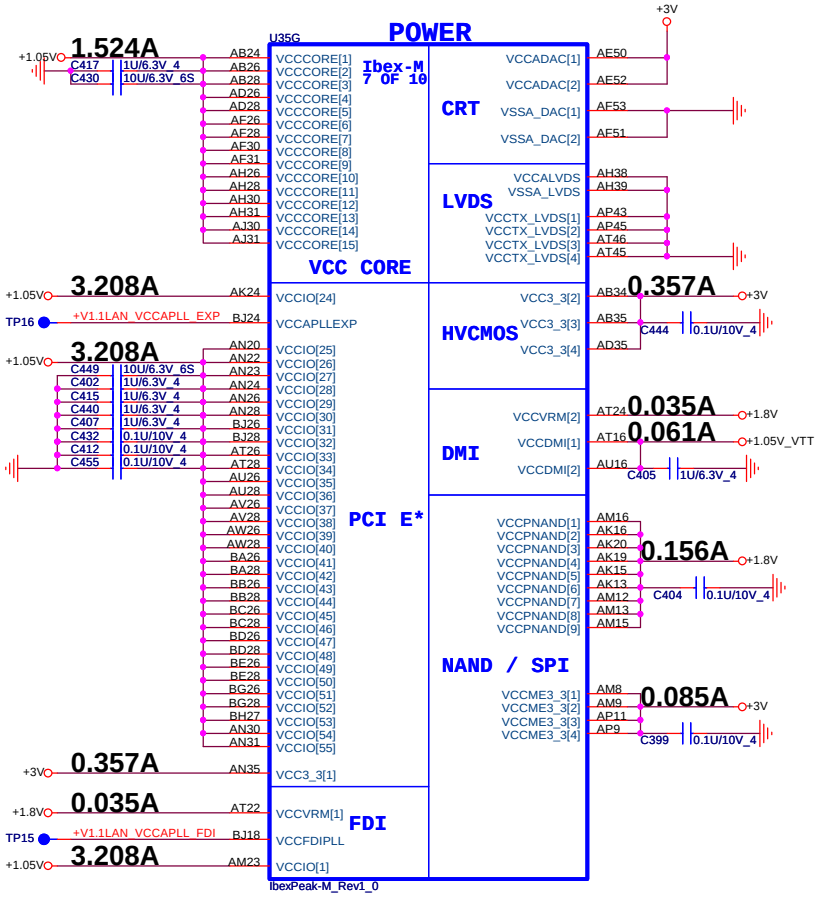
No Reboot Strap

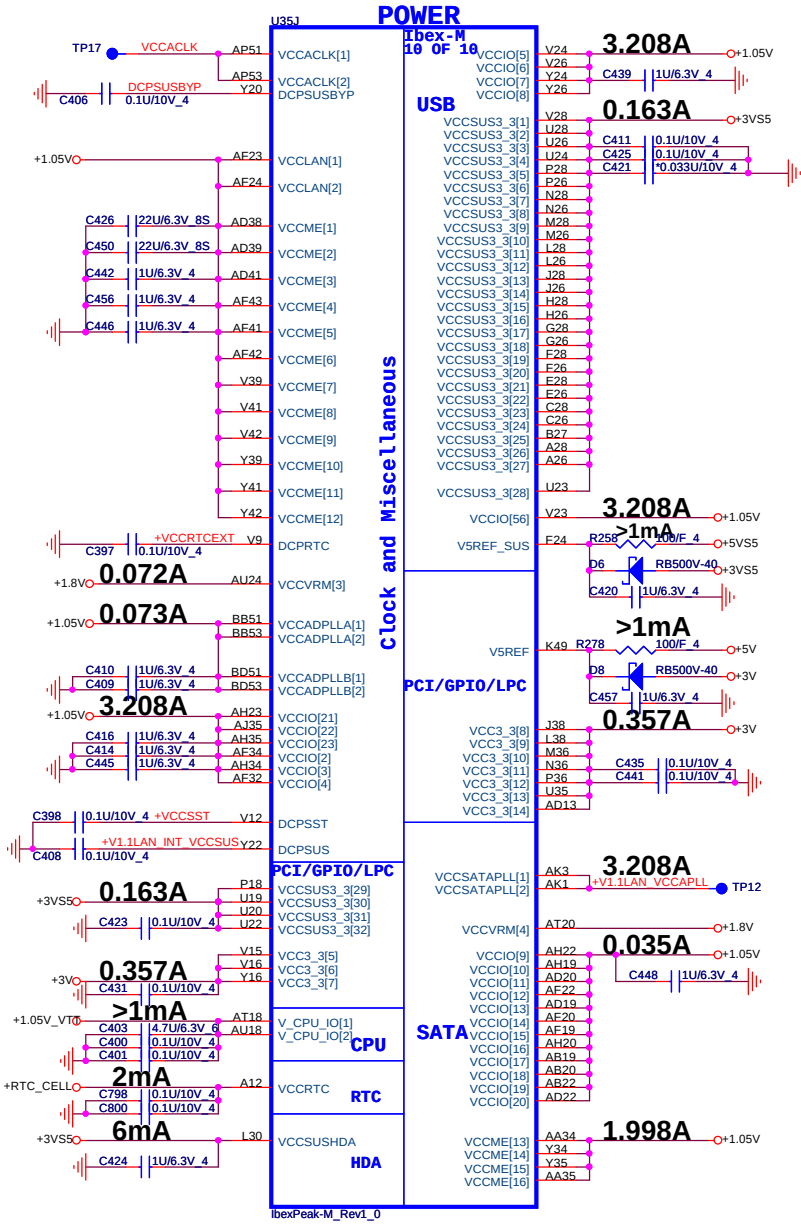
7,27 ACZ_SPKR R478 *1K/F_4 +3V

NB5/RD2

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/5 (GPIO & Strap)	3A
Date: Thursday, August 05, 2010	Sheet 10 of 47	





2,7,8,9,37,38 +1.05V
3,5,10,34,38,39 +1.05V_VTT
5,10,37,42 +1.8V
2,3,7,8,9,10,12,13,14,17,25,26,27,28,30,31,32,33,34,35,38,40,42 +3V
8,9,10,42 +3VS5
25,26,27,29,30,31,32,33,35,42 +5V
42 +5VS5

NB5/RD2

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	3A

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13,41 +0.75V_DDR_VTT
5,13,37,41,42 +1.5VSUS
2,3,7,8,9,10,11,13,14,17,25,26,27,28,30,31,32,33,34,35,38,40,42 +3V
7,25,30,33,34,35,36,37,39,40,42,43 +3VPCU
24,30,32,34,36,37,38,39,40,41,42,43,44 +5VPCU

SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30

JDIM2A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM1

4 M_A_A[15:0]
M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12/BC#
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15

4 M_A_BS#0 109 BA0
4 M_A_BS#1 108 BA1
4 M_A_BS#2 79 BA2
4 M_A_CS#0 114 S0#
4 M_A_CS#1 121 S1#
4 M_A_CLK0 101 CK0
4 M_A_CLK0# 103 CK0#
4 M_A_CLK1 102 CK1
4 M_A_CLK1# 104 CK1#
4 M_A_CKE0 73 CKE0
4 M_A_CKE1 74 CKE1
4 M_A_CAS# 115 CAS#
4 M_A_RAS# 110 RAS#
4 M_A_WE# 113 WE#
R406 10K/F_4 DIMM0_SA0 197 SA0
R420 10K/F_4 DIMM0_SA1 201 SA1
2,8,13,28 CGCLK_SMB 202 SCL
2,8,13,28 CGDAT_SMB 200 SDA

4 M_A_ODT0 116 ODT0
4 M_A_ODT1 120 ODT1
4 M_A_DM[7:0]
M_A_DM0 11 DM0
M_A_DM1 28 DM1
M_A_DM2 46 DM2
M_A_DM3 63 DM3
M_A_DM4 136 DM4
M_A_DM5 153 DM5
M_A_DM6 170 DM6
M_A_DM7 187 DM7

4 M_A_DQS[7:0]
M_A_DQS0 12 DQS0
M_A_DQS1 29 DQS1
M_A_DQS2 47 DQS2
M_A_DQS3 64 DQS3
M_A_DQS4 137 DQS4
M_A_DQS5 154 DQS5
M_A_DQS6 171 DQS6
M_A_DQS7 188 DQS7

4 M_A_DQS#[7:0]
M_A_DQS#0 10 DQS#0
M_A_DQS#1 27 DQS#1
M_A_DQS#2 45 DQS#2
M_A_DQS#3 62 DQS#3
M_A_DQS#4 135 DQS#4
M_A_DQS#5 152 DQS#5
M_A_DQS#6 169 DQS#6
M_A_DQS#7 186 DQS#7

M_A_DQ[63:0] 4

DQ0 5 M_A_DQ0
DQ1 7 M_A_DQ1
DQ2 15 M_A_DQ2
DQ3 17 M_A_DQ3
DQ4 4 M_A_DQ4
DQ5 6 M_A_DQ5
DQ6 16 M_A_DQ6
DQ7 18 M_A_DQ7
DQ8 21 M_A_DQ8
DQ9 23 M_A_DQ9
DQ10 33 M_A_DQ10
DQ11 35 M_A_DQ11
DQ12 22 M_A_DQ12
DQ13 24 M_A_DQ13
DQ14 34 M_A_DQ14
DQ15 36 M_A_DQ15
DQ16 39 M_A_DQ16
DQ17 41 M_A_DQ17
DQ18 51 M_A_DQ18
DQ19 53 M_A_DQ19
DQ20 40 M_A_DQ20
DQ21 42 M_A_DQ21
DQ22 50 M_A_DQ22
DQ23 52 M_A_DQ23
DQ24 57 M_A_DQ24
DQ25 59 M_A_DQ25
DQ26 67 M_A_DQ26
DQ27 69 M_A_DQ27
DQ28 56 M_A_DQ28
DQ29 58 M_A_DQ29
DQ30 68 M_A_DQ30
DQ31 70 M_A_DQ31
DQ32 129 M_A_DQ32
DQ33 131 M_A_DQ33
DQ34 141 M_A_DQ34
DQ35 143 M_A_DQ35
DQ36 130 M_A_DQ36
DQ37 132 M_A_DQ37
DQ38 140 M_A_DQ38
DQ39 142 M_A_DQ39
DQ40 147 M_A_DQ40
DQ41 149 M_A_DQ41
DQ42 157 M_A_DQ42
DQ43 159 M_A_DQ43
DQ44 146 M_A_DQ44
DQ45 148 M_A_DQ45
DQ46 158 M_A_DQ46
DQ47 160 M_A_DQ47
DQ48 163 M_A_DQ48
DQ49 165 M_A_DQ49
DQ50 175 M_A_DQ50
DQ51 177 M_A_DQ51
DQ52 164 M_A_DQ52
DQ53 166 M_A_DQ53
DQ54 174 M_A_DQ54
DQ55 176 M_A_DQ55
DQ56 181 M_A_DQ56
DQ57 183 M_A_DQ57
DQ58 191 M_A_DQ58
DQ59 193 M_A_DQ59
DQ60 180 M_A_DQ60
DQ61 182 M_A_DQ61
DQ62 192 M_A_DQ62
DQ63 194 M_A_DQ63

JDIM2B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM1

+1.5VSUS
VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

+3V
VDDSPD 199

NC1 77
NC2 122
NCTEST 125

3 PM_EXTTS#0 EVENT# 198 PM_EXTTS#0
3,13 DDR3_DRAMRST# RESET# 30
+1.5VSUS R8 1K/F_4

6 DDR_VREF_DQ0 R327 *0_4 VREF_DQ 1 SMDDR_VREF_DQ0
VREF_CA 126 SMDDR_VREF_DIMM
R13 100K/F_4

VSS1 2
VSS2 3
VSS3 8
VSS4 9
VSS5 13
VSS6 14
VSS7 19
VSS8 20
VSS9 25
VSS10 26
VSS11 31
VSS12 32
VSS13 37
VSS14 38
VSS15 43

VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 172
VSS44 173
VSS45 178
VSS46 179
VSS47 184
VSS48 185
VSS49 189
VSS50 190
VSS51 195
VSS52 196

VTT1 203 +0.75V_DDR_VTT
VTT2 204

GND 205
GND 206

C132 470P/50V_4 R95 *0_4/S SMDDR_VREF_DIMM 13
R97 *10K/F_4_NC R90 *10K/F_4_NC DDR_VTTREF 41
+1.5VSUS

Place these Caps near So-Dimm0.

+1.5VSUS
C72 10U/6.3V_6S
C34 10U/6.3V_6S
C25 10U/6.3V_6S
C109 10U/6.3V_6S
C105 10U/6.3V_6S
C122 10U/6.3V_6S
C27 0.1U/10V_4
C94 0.1U/10V_4
C40 0.1U/10V_4
C75 0.1U/10V_4
C112 0.1U/10V_4
C160 *8.2P/50V_4
C164 *8.2P/50V_4
C173 *8.2P/50V_4
C228 *6.8P/50V_4
C229 *6.8P/50V_4

PV for RF solution

+3V
C694 2.2U/6.3V_6
C695 *0.1U/10V_4

+0.75V_DDR_VTT
C719 1U/6.3V_4
C727 1U/6.3V_4
C726 1U/6.3V_4
C714 1U/6.3V_4
C723 *10U/6.3V_8
C725 *10U/6.3V_8
C722 10U/6.3V_6S

SMDDR_VREF_DQ0
C6 0.1U/10V_4
C8 2.2U/6.3V_6

SMDDR_VREF_DIMM
C153 0.1U/10V_4
C147 2.2U/6.3V_6

Place these U8008 near So-Dimm0(JDIM8000)

U23
8,17,25,34 MBCLK2 MBCLK2 8 SCLK VCC 1 C555 0.01U/25V_4 +3V
8,17,25,34 MBDATA2 MBDATA2 7 SDA DXP 2 DDR_THERMDA
3 PM_EXTTS#0 PM_EXTTS#0 6 ALERT# DXN 3 Q29
3,13 PM_EXTTS#1 PM_EXTTS#1 4 OVERT# GND 5 C554 2200P/50V_4 2 3 MMBT3904-7-F
DDR_THERMDC
G780P81U
ADDRESS: 98H

S3 Power Reduction

+1.5VSUS
R7 1K/F_4
DDR_VREF_DQ0 1 3 SMDDR_VREF_DQ0
3,10,13 DDR3_CORL 2 Q2 AP2302GN
R6 1K/F_4
C4 0.1U/10V_4

NB5/RD2

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0	3A

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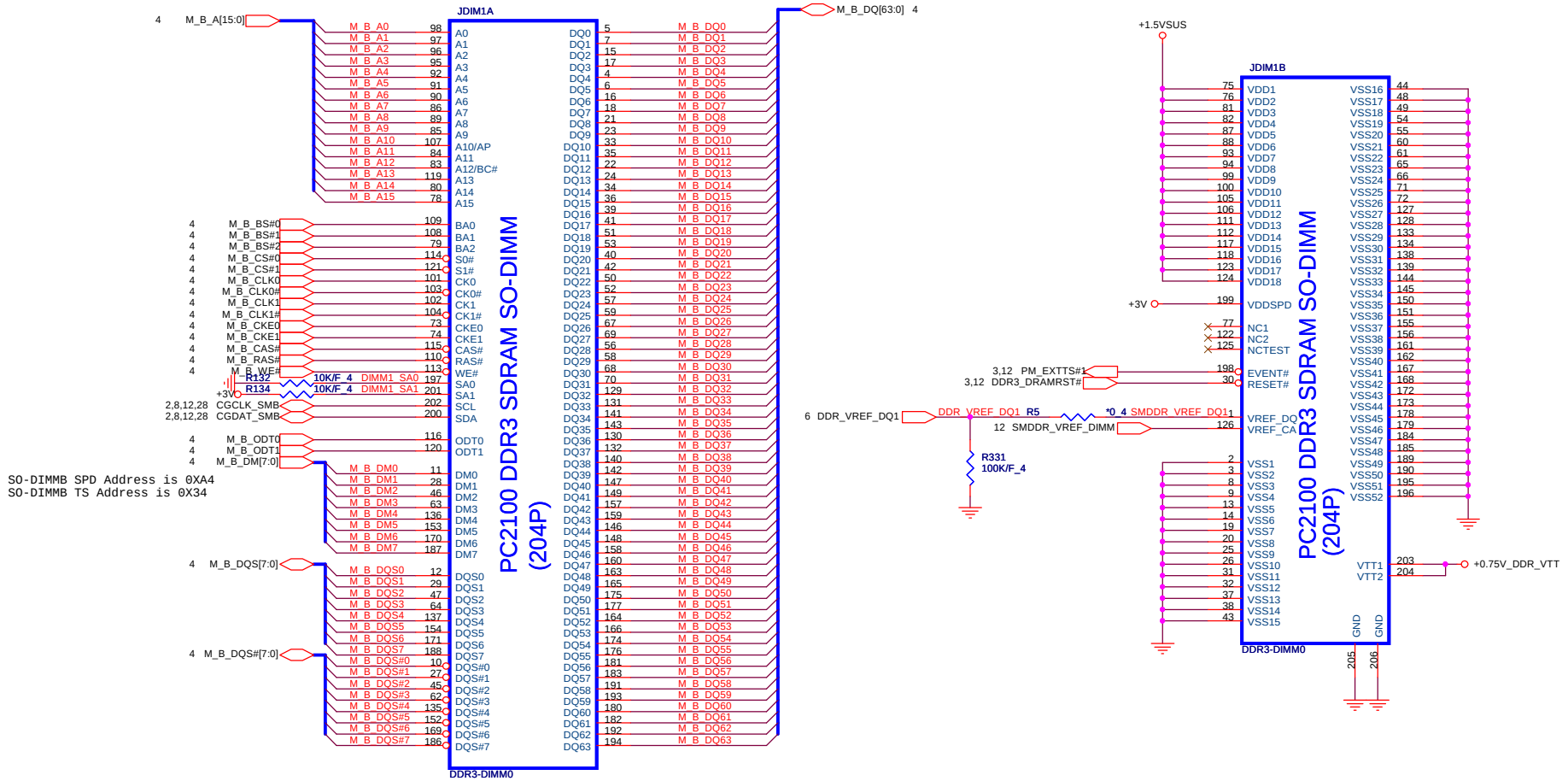
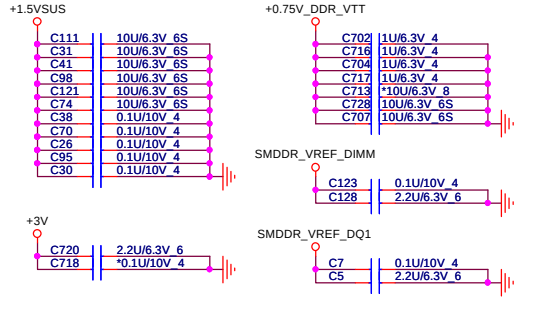
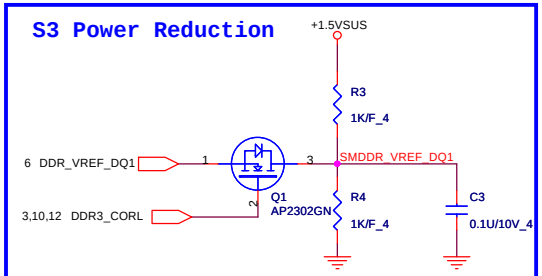
12,41 +0.75V_DDR_VTT
5,12,37,41,42 +1.5VSUS
2,3,7,8,9,10,11,12,14,17,25,26,27,28,30,31,32,33,34,35,38,40,42 +3V
7,25,30,33,34,35,36,37,39,40,42,43 +3VPCU
24,30,32,34,36,37,38,39,40,41,42,43,44 +5VPCU



Place these Caps near So-Dimm1



S3 Power Reduction



PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1	3A
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NB5/RD2

16,18,41 +1.0V_VGA
5,10,11,37,42 +1.8V
2,3,7,8,9,10,11,12,13,17,25,26,27,28,30,31,32,33,34,35,38,40,42 +3V

U27A

PCI EXPRESS INTERFACE

3 PEG_TX15	PEG_TX15 AA38	PCIE_RX0P	PCIE_TX0P	Y33	C_PEG_RXP15 C213 .1U/10V_4	PEG_RX15 3
3 PEG_TX#15	PEG_TX#15 Y37	PCIE_RX0N	PCIE_TX0N	Y32	C_PEG_RXN15 C201 .1U/10V_4	PEG_RX#15 3
3 PEG_TX14	PEG_TX14 Y35	PCIE_RX1P	PCIE_TX1P	W33	C_PEG_RXP14 C226 .1U/10V_4	PEG_RX14 3
3 PEG_TX#14	PEG_TX#14 W36	PCIE_RX1N	PCIE_TX1N	W32	C_PEG_RXN14 C231 .1U/10V_4	PEG_RX#14 3
3 PEG_TX13	PEG_TX13 W38	PCIE_RX2P	PCIE_TX2P	U33	C_PEG_RXP13 C236 .1U/10V_4	PEG_RX13 3
3 PEG_TX#13	PEG_TX#13 V37	PCIE_RX2N	PCIE_TX2N	U32	C_PEG_RXN13 C243 .1U/10V_4	PEG_RX#13 3
3 PEG_TX12	PEG_TX12 V35	PCIE_RX3P	PCIE_TX3P	U30	C_PEG_RXP12 C223 .1U/10V_4	PEG_RX12 3
3 PEG_TX#12	PEG_TX#12 U36	PCIE_RX3N	PCIE_TX3N	U29	C_PEG_RXN12 C217 .1U/10V_4	PEG_RX#12 3
3 PEG_TX11	PEG_TX11 U38	PCIE_RX4P	PCIE_TX4P	T33	C_PEG_RXP11 C256 .1U/10V_4	PEG_RX11 3
3 PEG_TX#11	PEG_TX#11 T37	PCIE_RX4N	PCIE_TX4N	T32	C_PEG_RXN11 C266 .1U/10V_4	PEG_RX#11 3
3 PEG_TX10	PEG_TX10 T35	PCIE_RX5P	PCIE_TX5P	T30	C_PEG_RXP10 C253 .1U/10V_4	PEG_RX10 3
3 PEG_TX#10	PEG_TX#10 R36	PCIE_RX5N	PCIE_TX5N	T29	C_PEG_RXN10 C246 .1U/10V_4	PEG_RX#10 3
3 PEG_TX9	PEG_TX9 R38	PCIE_RX6P	PCIE_TX6P	P33	C_PEG_RXP9 C269 .1U/10V_4	PEG_RX9 3
3 PEG_TX#9	PEG_TX#9 P37	PCIE_RX6N	PCIE_TX6N	P32	C_PEG_RXN9 C272 .1U/10V_4	PEG_RX#9 3
3 PEG_TX8	PEG_TX8 P35	PCIE_RX7P	PCIE_TX7P	P30	C_PEG_RXP8 C275 .1U/10V_4	PEG_RX8 3
3 PEG_TX#8	PEG_TX#8 N36	PCIE_RX7N	PCIE_TX7N	P29	C_PEG_RXN8 C288 .1U/10V_4	PEG_RX#8 3
3 PEG_TX7	PEG_TX7 N38	PCIE_RX8P	PCIE_TX8P	N33	C_PEG_RXP7 C295 0.1U/10V_4	PEG_RX7 3
3 PEG_TX#7	PEG_TX#7 M37	PCIE_RX8N	PCIE_TX8N	N32	C_PEG_RXN7 C294 0.1U/10V_4	PEG_RX#7 3
3 PEG_TX6	PEG_TX6 M35	PCIE_RX9P	PCIE_TX9P	N30	C_PEG_RXP6 C291 0.1U/10V_4	PEG_RX6 3
3 PEG_TX#6	PEG_TX#6 L36	PCIE_RX9N	PCIE_TX9N	N29	C_PEG_RXN6 C293 0.1U/10V_4	PEG_RX#6 3
3 PEG_TX5	PEG_TX5 L38	PCIE_RX10P	PCIE_TX10P	L33	C_PEG_RXP5 C296 0.1U/10V_4	PEG_RX5 3
3 PEG_TX#5	PEG_TX#5 K37	PCIE_RX10N	PCIE_TX10N	L32	C_PEG_RXN5 C297 0.1U/10V_4	PEG_RX#5 3
3 PEG_TX4	PEG_TX4 K35	PCIE_RX11P	PCIE_TX11P	L30	C_PEG_RXP4 C298 0.1U/10V_4	PEG_RX4 3
3 PEG_TX#4	PEG_TX#4 J36	PCIE_RX11N	PCIE_TX11N	L29	C_PEG_RXN4 C299 0.1U/10V_4	PEG_RX#4 3
3 PEG_TX3	PEG_TX3 J38	PCIE_RX12P	PCIE_TX12P	K33	C_PEG_RXP3 C300 0.1U/10V_4	PEG_RX3 3
3 PEG_TX#3	PEG_TX#3 H37	PCIE_RX12N	PCIE_TX12N	K32	C_PEG_RXN3 C301 0.1U/10V_4	PEG_RX#3 3
3 PEG_TX2	PEG_TX2 H35	PCIE_RX13P	PCIE_TX13P	J33	C_PEG_RXP2 C302 0.1U/10V_4	PEG_RX2 3
3 PEG_TX#2	PEG_TX#2 G36	PCIE_RX13N	PCIE_TX13N	J32	C_PEG_RXN2 C303 0.1U/10V_4	PEG_RX#2 3
3 PEG_TX1	PEG_TX1 G38	PCIE_RX14P	PCIE_TX14P	K30	C_PEG_RXP1 C307 0.1U/10V_4	PEG_RX1 3
3 PEG_TX#1	PEG_TX#1 F37	PCIE_RX14N	PCIE_TX14N	K29	C_PEG_RXN1 C306 0.1U/10V_4	PEG_RX#1 3
3 PEG_TX0	PEG_TX0 E35	PCIE_RX15P	PCIE_TX15P	H33	C_PEG_RXP0 C304 0.1U/10V_4	PEG_RX0 3
3 PEG_TX#0	PEG_TX#0 E37	PCIE_RX15N	PCIE_TX15N	H32	C_PEG_RXN0 C305 0.1U/10V_4	PEG_RX#0 3

CLOCK

8 CLK_PCIE_VGA — CLK_PCIE_VGA AB35 — PCIE_REFCLKP
8 CLK_PCIE_VGA# — CLK_PCIE_VGA# AA36 — PCIE_REFCLKN

AJ21 NC#1
AK21 NC#2
PWRGOOD_BUF — AH16 PWRGOOD

3,9,24,31,34,35 PLTRST# — AA30 PERSTB

CALIBRATION

PCIE_CALRP — Y30 PCIE_CALRP — R128 1.27K/F_4
PCIE_CALRN — Y29 PCIE_CALRN — R127 2K/F_4 — +1.0V_VGA

Broadway

U27H

DP C/D POWER

+1.8V_DPC_VDD18	AP20 AP21	DPC_VDD18#1 DPC_VDD18#2
+1.0V_DPC_VDD10	AP13 AT13	DPC_VDD10#1 DPC_VDD10#2
	AN17 AP16 AP17 AW14 AW16	DPC_VSSR#1 DPC_VSSR#2 DPC_VSSR#3 DPC_VSSR#4 DPC_VSSR#5
+1.8V_DPC_VDD18	AP22 AP23	DPD_VDD18#1 DPD_VDD18#2
+1.0V_DPC_VDD10	AP14 AP15	DPD_VDD10#1 DPD_VDD10#2
	AN19 AP18 AW20 AW22	DPD_VSSR#1 DPD_VSSR#2 DPD_VSSR#3 DPD_VSSR#4 DPD_VSSR#5
R29 150/F_4 DPCD_CALR	AW18	DPCD_CALR

DP A/B POWER

AN24 AP24	DPA_VDD18#1 DPA_VDD18#2
AP31 AP32	DPA_VDD10#1 DPA_VDD10#2
AN27 AP27 AP28 AW24 AW26	DPA_VSSR#1 DPA_VSSR#2 DPA_VSSR#3 DPA_VSSR#4 DPA_VSSR#5
AP25 AP26	DPB_VDD18#1 DPB_VDD18#2
AN33 AP33	DPB_VDD10#1 DPB_VDD10#2
AN29 AP29 AP30 AW30 AW32	DPB_VSSR#1 DPB_VSSR#2 DPB_VSSR#3 DPB_VSSR#4 DPB_VSSR#5
AW28 DPAB_CALR R352 150/F_4	DPAB_CALR

DP E/F POWER

+1.8V_DPE_VDD18 AH34 AJ34	DPE_VDD18#1 DPE_VDD18#2
+1.0V_DPE_VDD10 AL33 AM33	DPE_VDD10#1 DPE_VDD10#2
AN34 AP39 AR39 AU37	DPE_VSSR#1 DPE_VSSR#2 DPE_VSSR#3 DPE_VSSR#4
+1.8V_DPE_VDD18 AF34 AG34	DPF_VDD18#1 DPF_VDD18#2
+1.0V_DPE_VDD10 AK33 AK34	DPF_VDD10#1 DPF_VDD10#2
AF39 AH39 AK39 AL34 AM34	DPF_VSSR#1 DPF_VSSR#2 DPF_VSSR#3 DPF_VSSR#4 DPF_VSSR#5
R356 150/F_4 DPEF_CALR AM39	DPEF_CALR

DP PLL POWER

AU28 AV27	DPA_PVDD DPA_PVSS
AV29 AR28	DPB_PVDD DPB_PVSS
AU18 AV17	DPC_PVDD DPC_PVSS
AV19 AR18	DPD_PVDD DPD_PVSS
AM37 AN38	DPE_PVDD DPE_PVSS
AL38 AM35	DPF_PVDD DPF_PVSS

Broadway

+1.8V_DPA_VDD18 — (DPA/B_VDD10 : 1.0V@115mA+115mA) — +1.0V_VGA
+1.0V_DPA_VDD10 — HCB1608KF-181T15_6 L12 — C97 10U/6.3V_8, C108 1U/6.3V_4, C107 .1U/10V_4

+1.8V_DPA_VDD18

AMD 0821

+1.8V_VGA

(DPB_PVDD : 1.8V@20mA) — +1.8V_DPB_PVDD — HCB1608KF-181T15_6 L48 — C616 10U/6.3V_8, C622 1U/6.3V_4, C621 .1U/10V_4

(DPC_PVDD:1.8V@20mA) — +1.8V_DPC_PVDD — HCB1608KF-181T15_6 L44 — C576 10U/6.3V_8, C587 .1U/10V_4, C585 1U/6.3V_4

(DPD_PVDD:1.8V@20mA) — +1.8V_DPD_PVDD — HCB1608KF-181T15_6 L47 — C604 10U/6.3V_8, C620 .1U/10V_4, C618 1U/6.3V_4

(DPE/F_PVDD1.8V@20mA+20mA) — +1.8V_DPE_PVDD — HCB1608KF-181T15_6 L50 — C641 10U/6.3V_8, C640 .1U/10V_4, C639 .1U/10V_4

(DPE/F_VDD18 : 1.8V@200mA+200mA) — +1.8V_DPE_VDD18 — HCB1608KF-181T15_6 L17 — C135 10U/6.3V_8, C137 1U/6.3V_4, C136 .1U/10V_4

(DPE/F_VDD10 : 1.0V@115mA+115mA) — +1.0V_DPE_VDD10 — HCB1608KF-181T15_6 L13 — C99 10U/6.3V_8, C102 1U/6.3V_4, C101 .1U/10V_4

(DPA/B_VDD18 : 1.8V@200mA+200mA) — +1.8V_DPA_VDD18 — HCB1608KF-181T15_6 L46 — C591 10U/6.3V_8, C599 1U/6.3V_4, C610 .1U/10V_4

(DPC/D_VDD10 : 1.0V@115mA+115mA) — +1.0V_DPC_VDD10 — HCB1608KF-181T15_6 L59 — C329 10U/6.3V_8, C78 1U/6.3V_4, C92 .1U/10V_4

(DPC/D_VDD18 : 1.8V@200mA+200mA) — +1.8V_DPC_VDD18 — HCB1608KF-181T15_6 L60 — C598 10U/6.3V_8, C588 1U/6.3V_4, C589 .1U/10V_4

+3V
3,30,34,36,37,39,40,41,44 HWPG
U3 *MC74VHC1G08DFT2G
R36 4 *10K_4
PWRGOOD_BUF
R35 12K_4

For future ASIC, if PWRGOOD_BUF is not requred it should be pulled to ground.

NB5/RD2

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M97-M2 (PCIE I/F) 1/5	3A

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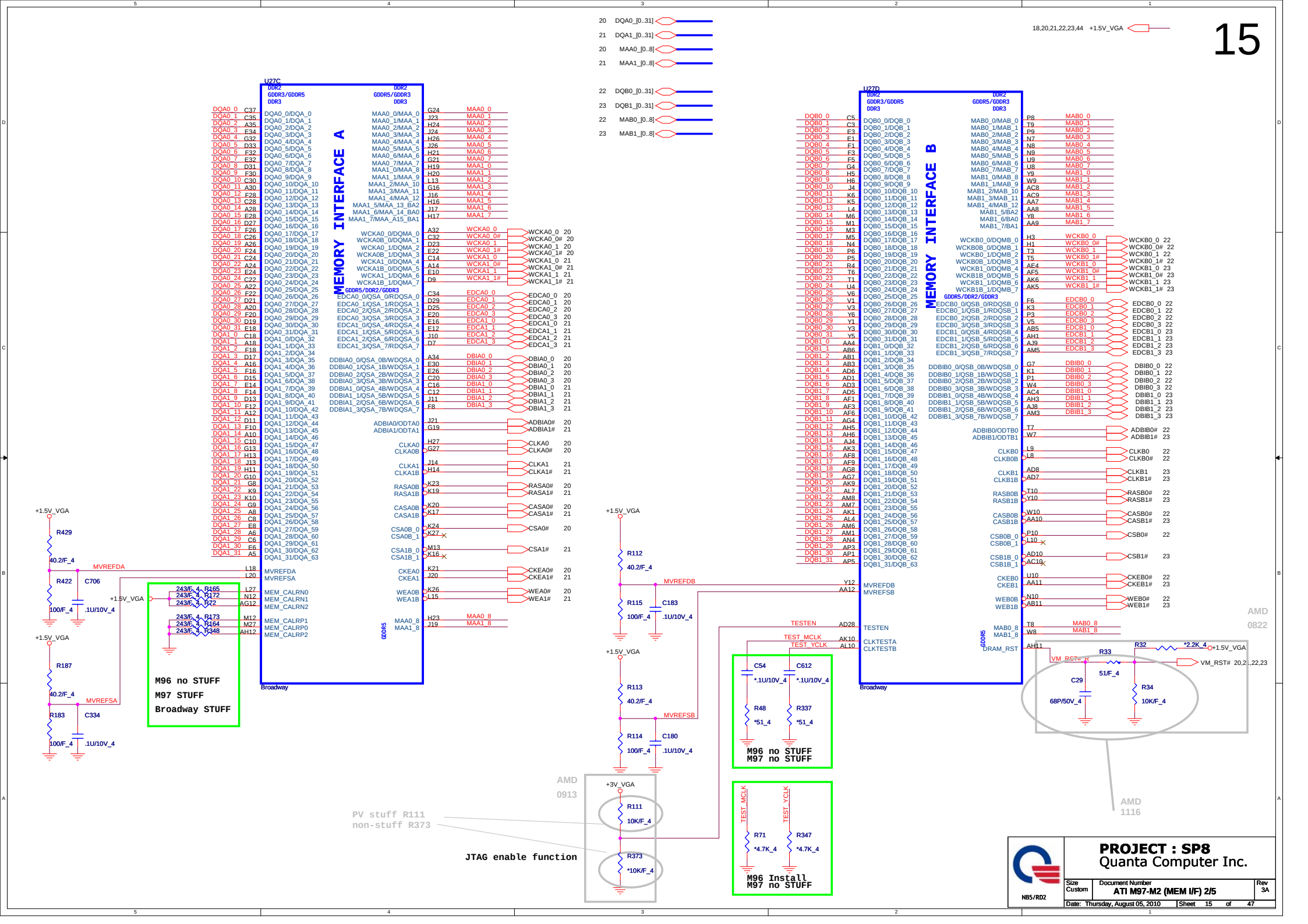
U27C
MEMORY INTERFACE A
Broadway
U27D
MEMORY INTERFACE B
Broadway
M96 no STUFF
M97 STUFF
Broadway STUFF
M96 no STUFF
M97 no STUFF
M96 Install
M97 no STUFF
PV stuff R111
non-stuff R373
JTAG enable function
AMD 0913
AMD 0822
AMD 1116
PROJECT : SP8
Quanta Computer Inc.
ATI M97-M2 (MEM I/F) 2/5
Rev 3A
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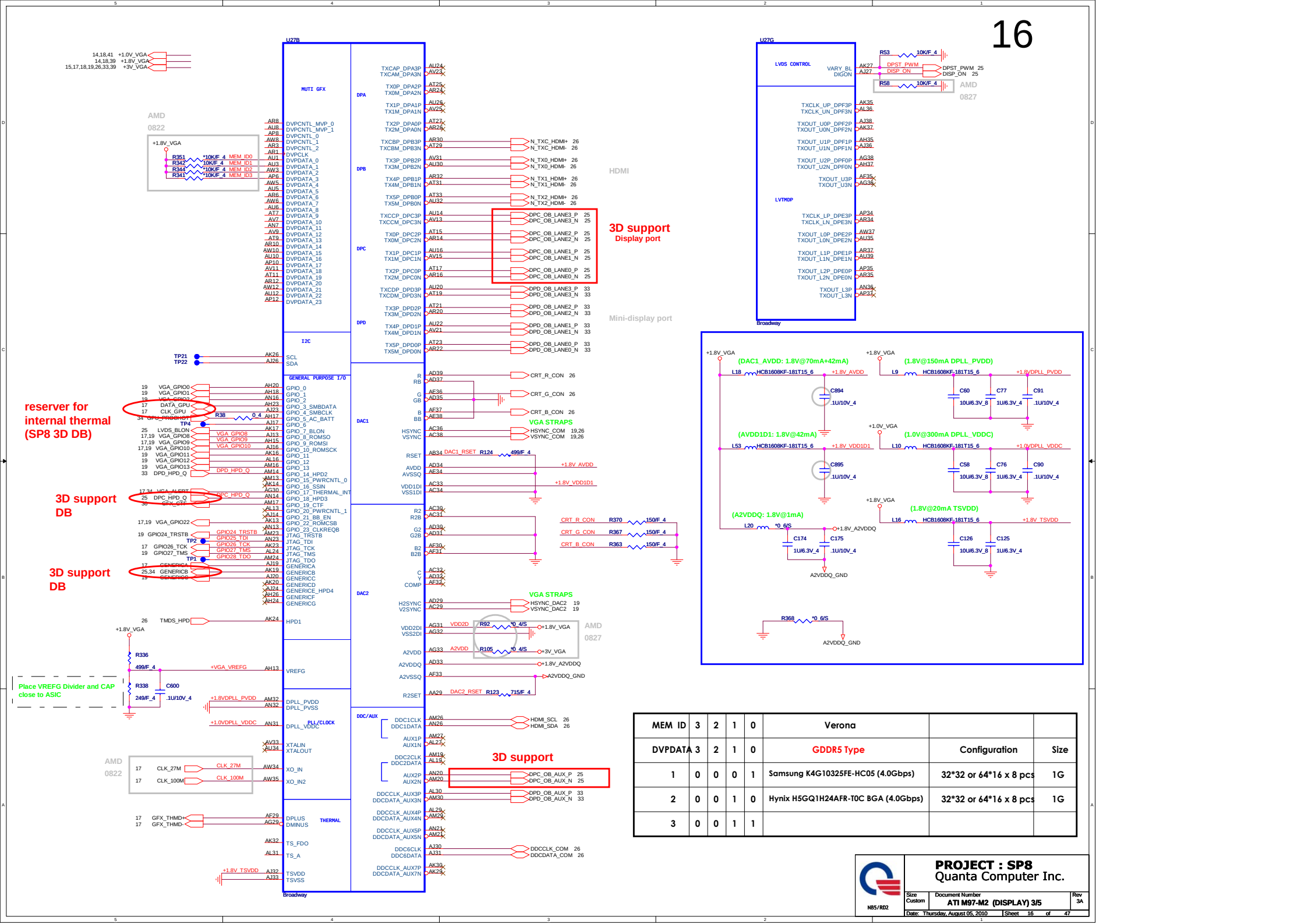

MEM ID	3	2	1	0	Verona		
DVPDATA	3	2	1	0	GDDR5 Type	Configuration	Size
1	0	0	0	1	Samsung K4G10325FE-HC05 (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
2	0	0	1	0	Hynix H5GQ1H24AFR-T0C BGA (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
3	0	0	1	1			

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M97-M2 (DISPLAY) 3/5	3A

NB5/RD2

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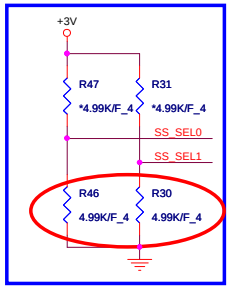
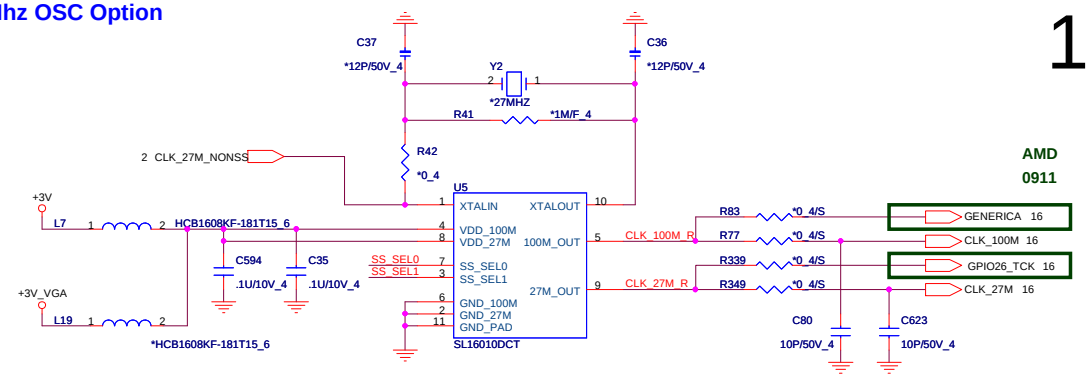
27MHz + 100Mhz OSC Option

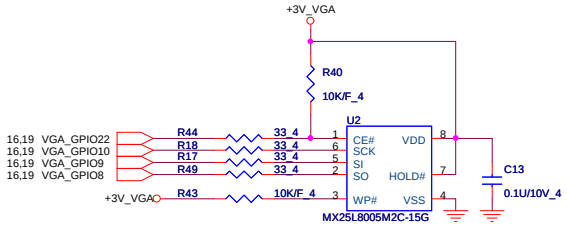


SP8 1.1 DB

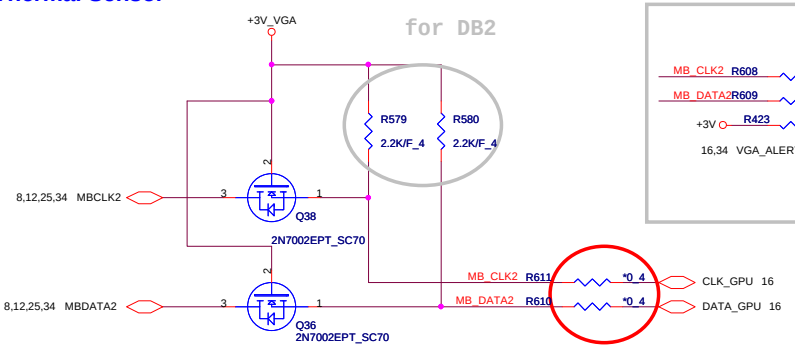


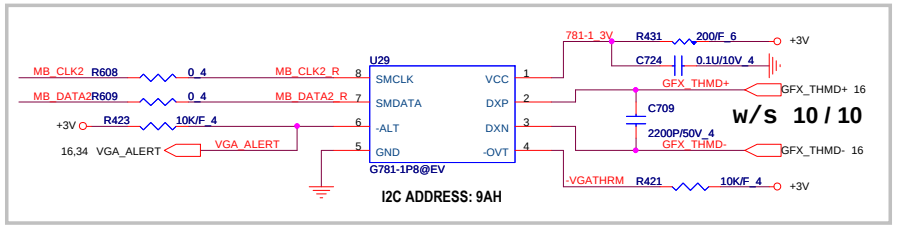
SS_SEL1	SS_SEL0	Spread Percent(%) SS_CLK (PIN 5)
LOW	LOW	Spread Off
LOW	Middle	-0.5%
LOW	High	-2.5%
Middle	LOW	-0.25%
Middle	Middle	-0.75%
Middle	High	-1.0%
High	LOW	-1.5%
High	Middle	-2.0%
High	High	-3.0%

Ext EEPROM



Thermal Sensor

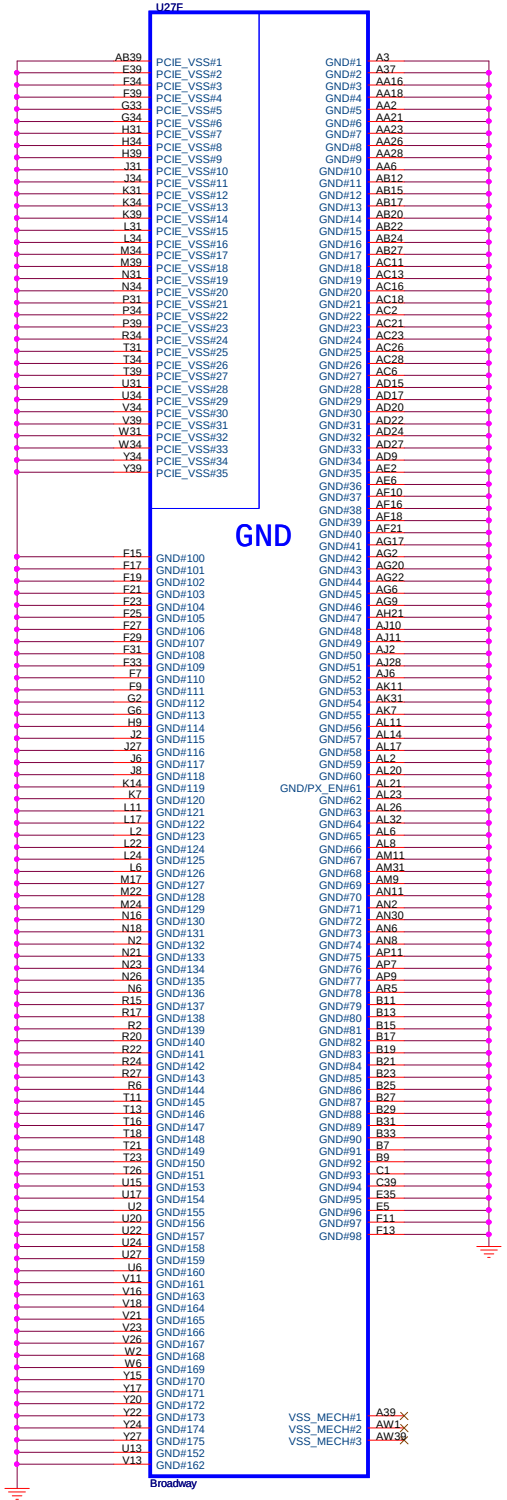


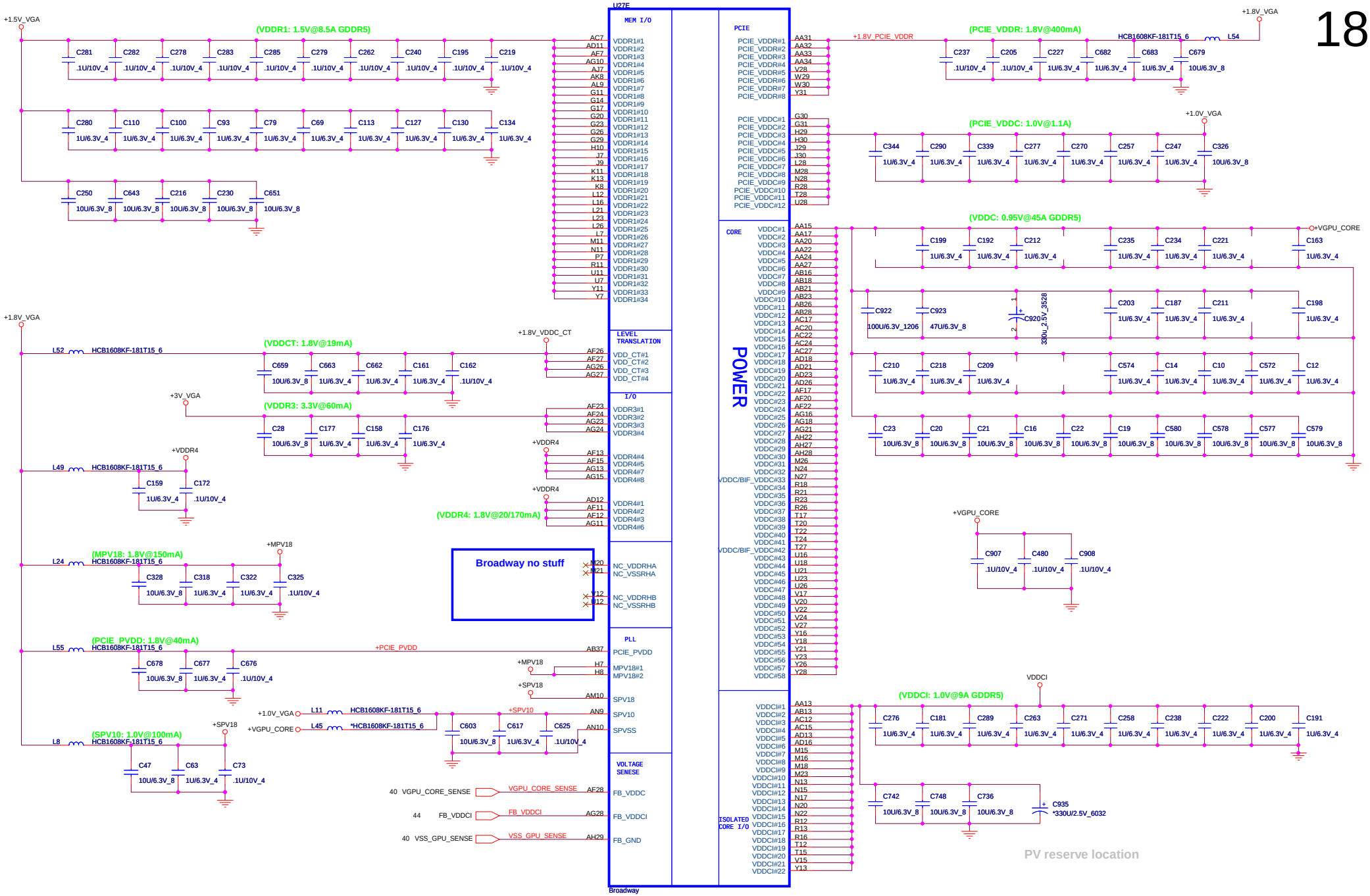


reserver for internal thermal SP8 1.1 DB

2,3,7,8,9,10,11,12,13,14,25,26,27,28,30,31,32,33,34,35,38,40,42 +3V

15,16,18,19,26,33,39 +3V_VGA




U27E
MEM I/O
PCIE
POWER
CORE
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENESE
ISOLATED CORE I/O
Broadway
+1.5V_VGA
(VDDR1: 1.5V@8.5A GDDR5)
+1.8V_VGA
+1.8V_PCIE_VDDR
(PCIE_VDDR: 1.8V@400mA)
HCB1608KF-181T15_6
L54
+1.0V_VGA
(PCIE_VDDC: 1.0V@1.1A)
(VDDC: 0.95V@45A GDDR5)
+VGPU_CORE
+1.8V_VDDC_CT
(VDDCT: 1.8V@19mA)
L52
+3V_VGA
(VDDR3: 3.3V@60mA)
+VDDR4
L49
(VDDR4: 1.8V@20/170mA)
Broadway no stuff
+MPV18
(MPV18: 1.8V@150mA)
L24
(PCIE_PVDD: 1.8V@40mA)
L55
+PCIE_PVDD
+SPV18
(SPV10: 1.0V@100mA)
L8
L11
L45
*HCB1608KF-181T15_6
+SPV10
+VGPU_CORE
VDDCI
(VDDCI: 1.0V@9A GDDR5)
PV reserve location
40 VGPU_CORE_SENSE
44 FB_VDDCI
40 VSS_GPU_SENSE
14,16,41 +1.0V_VGA
40 +VGPU_CORE
15,20,21,22,23,44 +1.5V_VGA
14,16,39 +1.8V_VGA
15,16,17,19,26,33,39 +3V_VGA
NB5/RD2
PROJECT : SP8
Quanta Computer Inc.
Size Custom
Document Number ATI M97-M2 (POWER) 5/5
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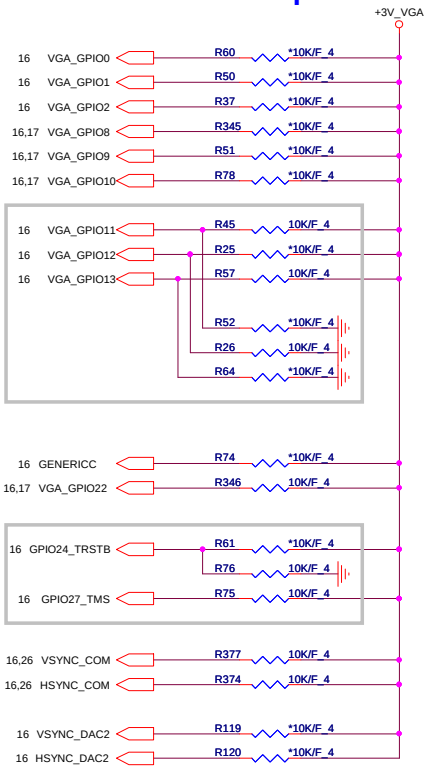
Straps



Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground — High logic voltage

Signal

Strap Name		Pin Straps Description	Default Value
TX_PWRS_ENB	GPIO0	GPIO[1:0]:Recommend to pulling up for PICE setting. GPIO_0:PCIE full TX output swing	
TX_DEEMPH_EN	GPIO1	GPIO_1:PCIE Transmitter DE-EMPHASIS enabled	
BIF_GEN2_EN	GPIO2	GPIO_2:System is using PCIE GEN1 can be let it NC(ASIC internal pull down) if Gen2 just pull up for PCIE 5GT/s support. (0=PCIE GNE1,2.5GT/s ; 1=PCIE GNE2,5GT/s)	
STRAP_BIF_CLK_PM_EN	GPIO8		
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11		
BIOS_ROM_EN	GPIO22	BIOS_ROM_EN(GPIO22)=1, then Config[2:0]=GPIO[13:12:11] defines the ROM type. (See table as below)	
AUDIO[0]	VSYNC		
AUD(1)	HSYNC		
VSYNC_DAC2	V2SYNC		
HSYNC_DAC2	H2SYNC		
	GENERICC		

Table 3-34 ROM Configurations

Manufacturer	Part Number	Size	CONFIG[2:0]
Atmel	AT25F512	512 kbit	001
	AT25F512A	512 kbit	010
	AT25F1024	1 Mbit	011
	AT25F1024A	1 Mbit	011
	AT25F2048	2 Mbit	011
	AT25F4096	4 Mbit	011
ST Microelectronics	M25P05A	512 kbit	100
	M25P10A	1 Mbit	101
	M25P20	2 Mbit	101
	M25P40	4 Mbit	101
	M25P80	8 Mbit	101
Silicon Storage Technology	SST25VF512	512 kbit	010
	SST25VF010	1 Mbit	011
	SST25VF020	2 Mbit	011
	SST25VF040	4 Mbit	011
Winbond Electronics Corporation	W45B512	512 kbit	110
	W45B012	1 Mbit	111
YMC	Y25LF05	512 kbit	010
	SA25C020	2 Mbit	011
PMC	Pm25LV512	512 kbit	100
	Pm25LV010	1 Mbit	101

Default

1GB GDDR5 : CHANNEL A-0 (64M x 16)

15 DQA0_[31..0]
15 MAA0_[8..0]

MF=1 Mirror

U30

U12

170-BALL SDRAM GDDR5

K4G52324FG

Change 1u to 2.2,for ATI Request 1212

15,18,21,22,23,44 +1.5V_VGA

PROJECT : SP8
Quanta Computer Inc.

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Custom	<Doc>	3A

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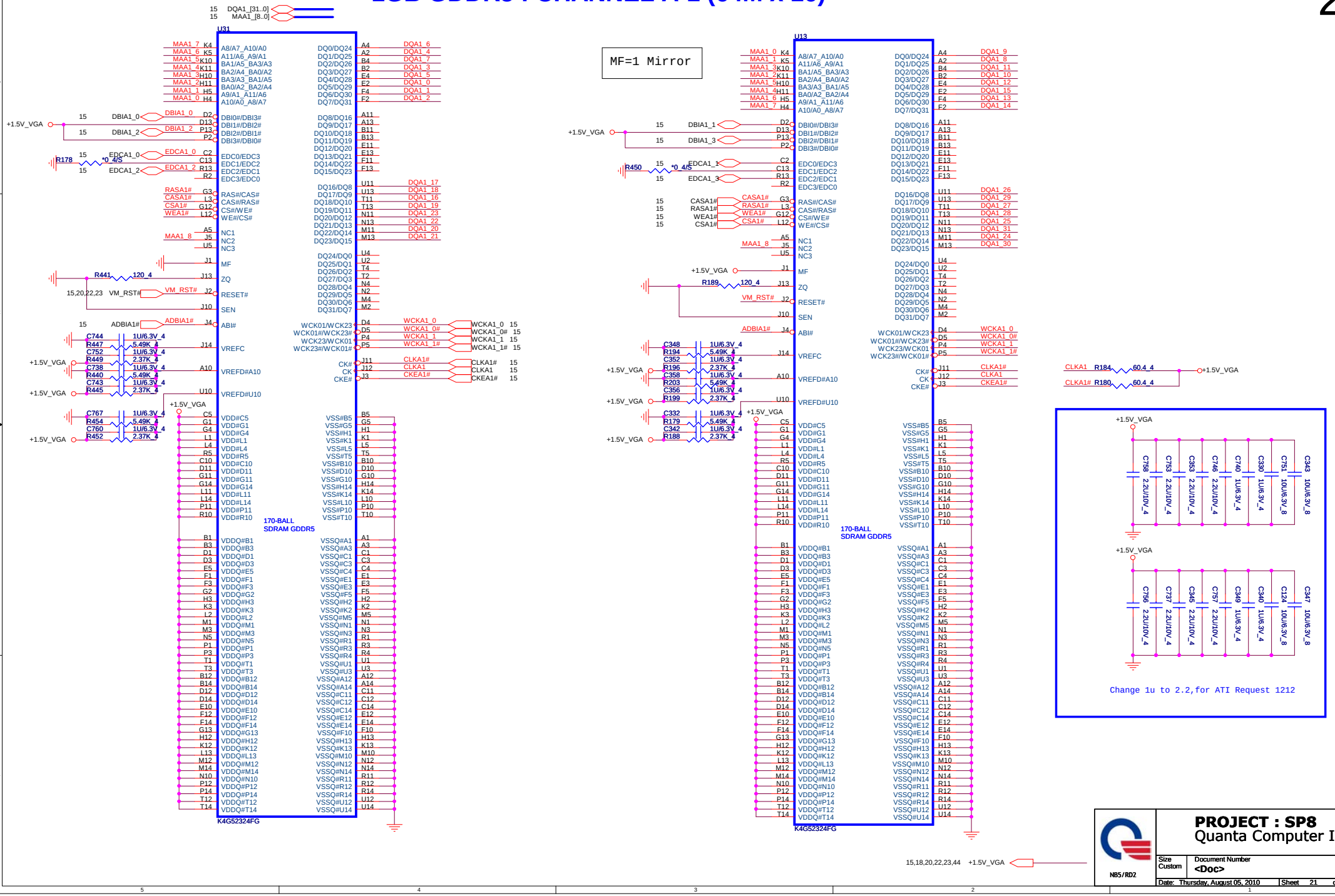
N85/RD2

1GB GDDR5 : CHANNEL A-1 (64M x 16)



1GB GDDR5 : CHANNEL B-0 (64M x 16)

15 DQB0_[0..31]
15 MAB0_[0..8]

MF=1 Mirror

U10

U28

170-BALL SDRAM GDDR5

K4G52324FG

Change 1u to 2.2,for ATI Request 1212

15,18,20,21,23,44 +1.5V_VGA

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Quanta Computer Inc.

NB5/RD2

Size: Custom | Document Number: <Doc> | Rev: 3A

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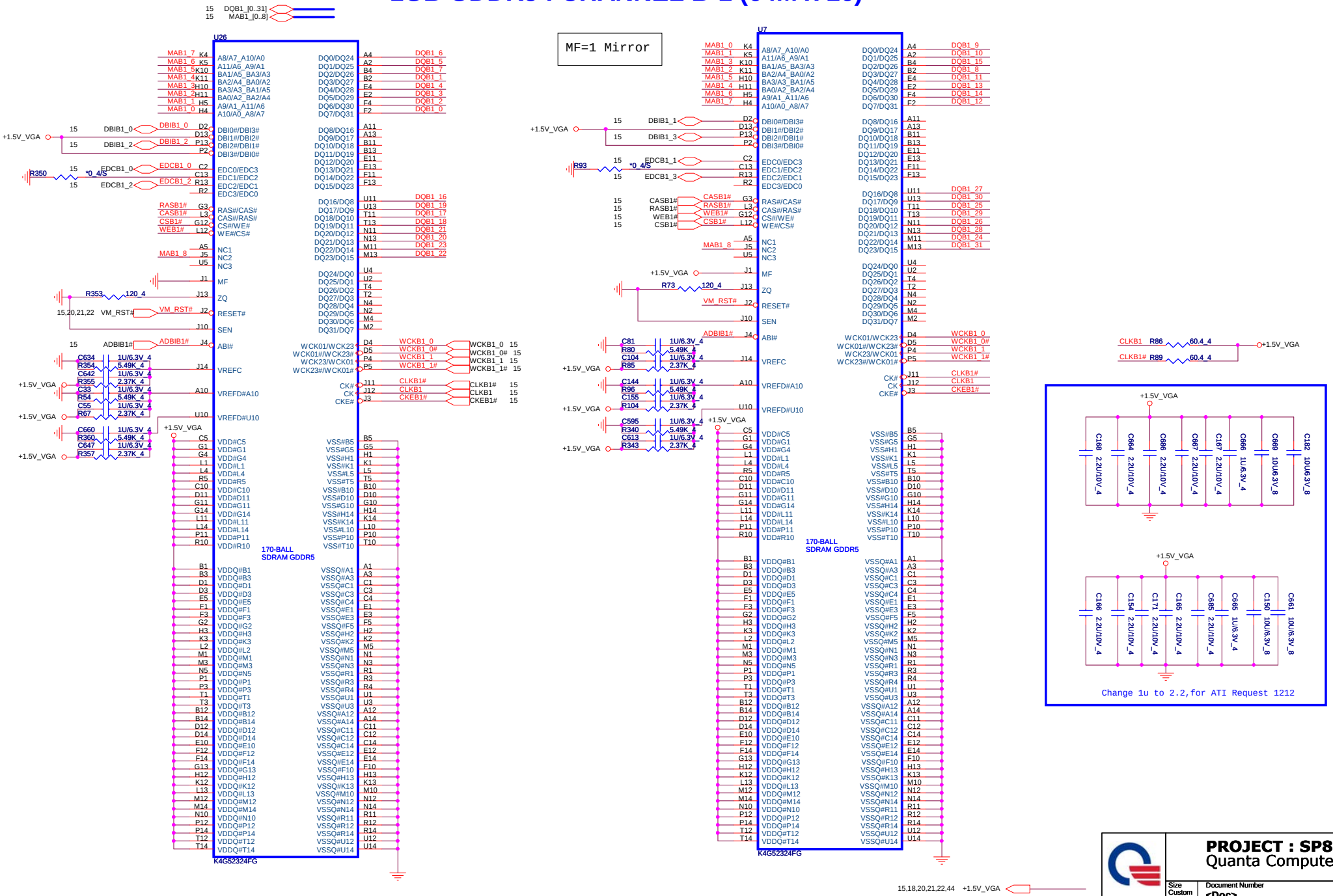
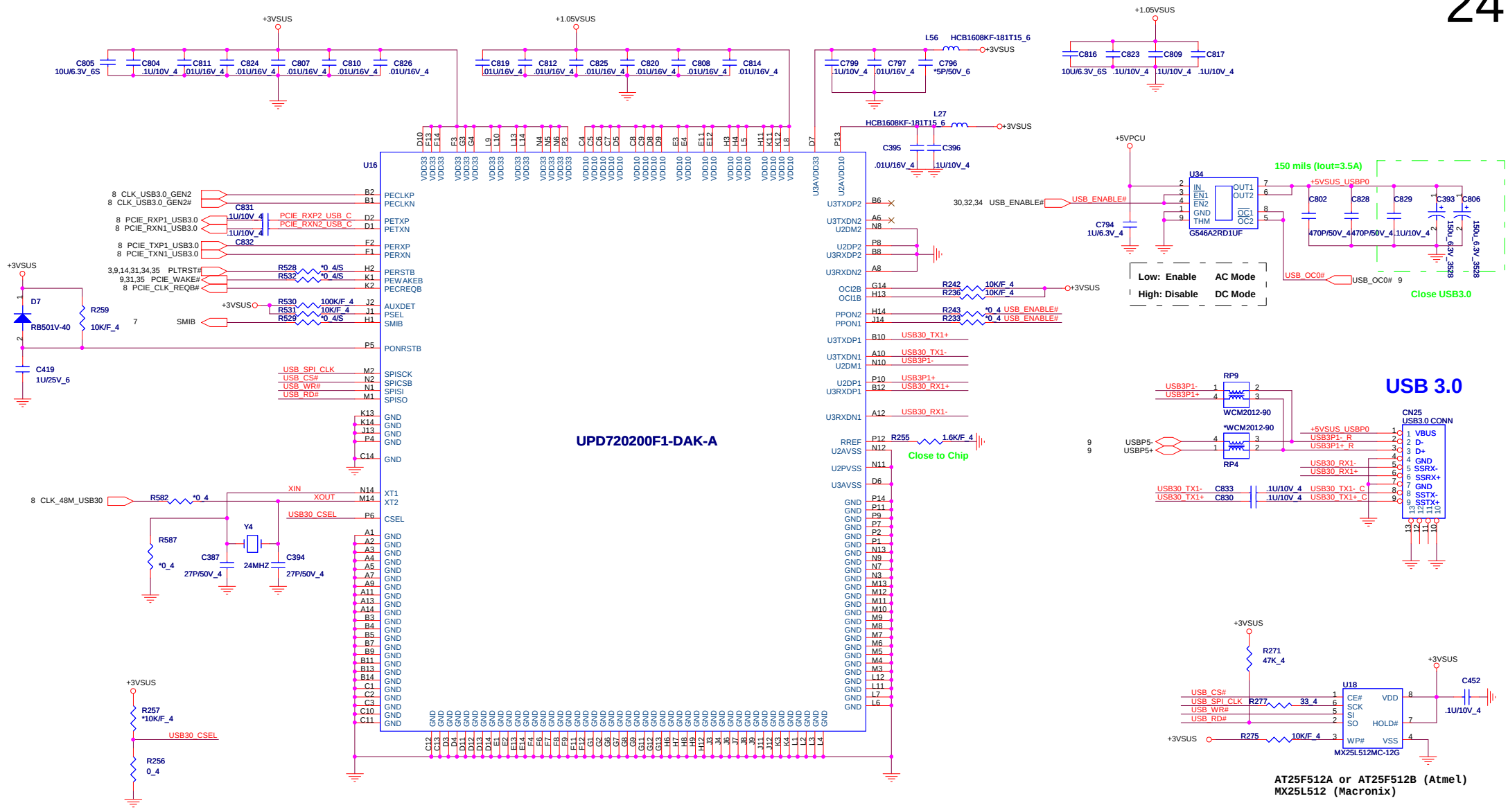
1GB GDDR5 : CHANNEL B-1 (64M x 16)

MF=1 Mirror




UPD720200F1-DAK-A
U16
+3VSUS
+1.05VSUS
+5VPCU
C805 10U/6.3V_6S
C804 .1U/10V_4
C811 .01U/16V_4
C824 .01U/16V_4
C807 .01U/16V_4
C810 .01U/16V_4
C826 .01U/16V_4
C819 .01U/16V_4
C812 .01U/16V_4
C825 .01U/16V_4
C820 .01U/16V_4
C808 .01U/16V_4
C814 .01U/16V_4
L56 HCB1608KF-181T15_6
C799 .1U/10V_4
C797 .01U/16V_4
C796 *5P/50V_6
C816 10U/6.3V_6S
C823 .1U/10V_4
C809 .1U/10V_4
C817 .1U/10V_4
L27 HCB1608KF-181T15_6
C395 .01U/16V_4
C396 1U/10V_4
U34
G546A2RD1UF
150 mils (Iout=3.5A)
+5VSUS_USBP0
C802 470P/50V_4
C828 470P/50V_4
C829 1U/10V_4
C393 150U_6.3V_3528
C806 150U_6.3V_3528
C794 1U/6.3V_4
USB_ENABLE#
USB_OC0#
Low: Enable AC Mode
High: Disable DC Mode
Close USB3.0
USB 3.0
RP9 WCM2012-90
*WCM2012-90
RP4
CN25 USB3.0 CONN
VBUS
D-
D+
GND
SSRX-
SSRX+
GND
SSTX-
SSTX+
USB3P1-
USB3P1+
USBP5-
USBP5+
USB30_RX1-
USB30_RX1+
USB30_TX1-
USB30_TX1+
C833 .1U/10V_4
C830 .1U/10V_4
D7 RB501V-40
R259 10K/F_4
C419 1U/25V_6
SMIB
PONRSTB
USB_SPI_CLK
USB_CS#
USB_WR#
USB_RD#
XIN
XOUT
USB30_CSEL
8 CLK_48M_USB30
R582 *0_4
R587 *0_4
Y4 24MHZ
C387 27P/50V_4
C394 27P/50V_4
R257 *10K/F_4
R256 0_4
R271 47K_4
R275 10K/F_4
U18 MX25L512MC-12G
C452 .1U/10V_4
AT25F512A or AT25F512B (Atmel)
MX25L512 (Macronix)
R255 1.6K/F_4
Close to Chip
R242 10K/F_4
R236 10K/F_4
R243 *0_4
R233 *0_4
R530 100K/F_4
R531 10K/F_4
R529 *0_4
R528 *0_4
R532 *0_4
C831 1U/10V_4
C832 1U/10V_4
PCIE_RXP2_USB_C
PCIE_RXN2_USB_C
Clock select signal
USB3.0_CSEL
High = External 48Mhz
Low = 24MHz X'tal
2,7,8,9,11,37,38 +1.05V
30,40,42 +3VSUS
30,32,34,36,37,38,39,40,41,42,43,44 +5VPCU
PROJECT : SP8
Quanta Computer Inc.
Size Custom
Document Number USB3.0
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N85/RD2

14.5v +12VALW
AO3404 ID current 5.8A
R330 330K_6
Q26 AO3404
+5V C540 .1U/10V_4
+5VSUS
R326 100K/F_4
Q27 2N7002E
C546 .027U/25V_6
LCDONG
LCDON#
Q28 DTC144EUA
16 DISP_ON
Q25 2N7002E
+5VLCD
R329 22_8
LCDDISCHG
L43 PBY201209T-4A/08
+5VLCD_CON
10W=2A
C558 *.01U/25V_4
C559 .1U/10V_4
C545 10U/6.3V_8
C548 22U/6.3V_8
C925 22U/6.3V_8

+3V
R616 100K/F_4
C_DPC_OB_AUX_N
C_DPC_OB_AUX_P
R617 100K/F_4

2,3,7,8,9,10,11,12,13,14,17,26,27,28,30,31,32,33,34,35,38,40,42 +3V
11,26,27,29,30,31,32,33,35,42 +5V
29,36,37,38,39,40,41,42,43,44 +VIN
7,30,33,34,35,36,37,39,40,42,43 +3VPCU

16 DPC_OB_AUX_N DPC_OB_AUX_N C522 .1U/10V_4 C_DPC_OB_AUX_N
16 DPC_OB_AUX_P DPC_OB_AUX_P C524 .1U/10V_4 C_DPC_OB_AUX_P
16 DPC_OB_LANE0_N DPC_OB_LANE0_N C528 .1U/10V_4 C_DPC_OB_LANE0_N
16 DPC_OB_LANE0_P DPC_OB_LANE0_P C525 .1U/10V_4 C_DPC_OB_LANE0_P
16 DPC_OB_LANE1_N DPC_OB_LANE1_N C530 .1U/10V_4 C_DPC_OB_LANE1_N
16 DPC_OB_LANE1_P DPC_OB_LANE1_P C529 .1U/10V_4 C_DPC_OB_LANE1_P
16 DPC_OB_LANE2_N DPC_OB_LANE2_N C532 .1U/10V_4 C_DPC_OB_LANE2_N
16 DPC_OB_LANE2_P DPC_OB_LANE2_P C531 .1U/10V_4 C_DPC_OB_LANE2_P
16 DPC_OB_LANE3_N DPC_OB_LANE3_N C537 .1U/10V_4 C_DPC_OB_LANE3_N
16 DPC_OB_LANE3_P DPC_OB_LANE3_P C536 .1U/10V_4 C_DPC_OB_LANE3_P
HGND
DPC_OB_HPD
BLON_CON
VADJ1
+LOGO_PWR1
CN5 LVD-A40SFYG+

+5V R318 75/F_6 C521 1000P/50V_4
+5VLCD_CON
PV change

+VIN
L42 FBM2125 HM330-T
+VIN_BLIGHT
C511 .1U/50V_6
C519 .01U/25V_4
C518 .1U/50V_6
C513 *10U/25V_12
10W

C910 .1U/50V_6
C911 .1U/50V_6
C912 .1U/50V_6
C913 .1U/50V_6
C914 .1U/50V_6
C915 *.1U/50V_6
C916 .1U/50V_6
C917 .1U/50V_6

R314 100K/F_4
C520 22P/50V_4
BLON_CON
PN_BLON
D13 RB500V-40
D12 RB500V-40
R313 47K_4 +3VPCU
16 LVDS_BLON R316 1K/F_4
LID_EC# 30,34
R315 10K/F_4
AMD 0822
10 LCD_BK
Q23 *DTC144EUA

Q51 *ME2303T1
R590 *150K/F_4
C906 *.1U/50V_6
C905 *.01U/25V_4
R592 *100K/F_4

+3V
DPC_OB_HPD_R
R602 150K/F_4
DPC_OB_HPD
16 DPC_HPD_Q
Q59 MMBT3904-7-F
R607 10K/F_4
R606 *348K/F_4
Close to Display Port Connector

DISPLAY

R621 0_8 HGND

34 PWM_VADJ R328 *0_4 VADJ1

PWM control

U41
LED_DRIVE
GENERICB_R
MBCLK2
P0.5 P0.3 P1.1_SCL VSS P1.0_SDA VDD P0.4 P0.2
PG-5V
VADJ1
PWM_IN
MBDATA2_R
R619 1K/F_4
*CY8C21123-24
PV change to 1K

Co-lay Crypress
SP8 1.1 DB

SP8 1.1 change
from 0402 to 0603
16 DPST_PWM DPST_PWM R325 1K/F_4 PWM_IN
C539 22P/50V_4
+3V
16,34 GENERICB R599 0_4 GENERICB_R
PWM_IN
R620 *0_6/S
TP18
C924 .01U/25V_4
U37
PG-5V
LED_DRIVE
VADJ1
VDD P0.7 P0.3 P0.1 P1.0_DAT VSS P1.1_SCL P1.3
MBDATA2_R
R615 0_4
MBDATA2 8,12,17,34
MBCLK2 8,12,17,34
PV change to 0Ω
CG7216
PV change
from Micro PIC16F505
to Cypress CG7216

+3V
R603 *10K/F_4 GENERICB_R
R604 *10K/F_4 PWM_IN
PV change for cypress Request

+5V
C933 .1U/10V_4
C934 .1U/10V_4
C936 .1U/10V_4
C937 .1U/10V_4
C938 .1U/10V_4
C939 .1U/10V_4
C940 .1U/10V_4
PV add for EMI solution

IR control

+5V
R430 *0_8/S
C928 .01U/25V_4
C927 .1U/10V_4
C926 10U/6.3V_8
PV change
PV change
from 0402 to 0805
R600 0_8
+IR_PWR 30
IR_LED 30
LED_DRIVE R319 200
34 LEDE_DRIVE R425 *200
Q53 AO3402
C931 1U/25V_6
PV add
reserve
SP8 1.1 DB
PV change
from 2N7002 to AO3402

N85/RD2
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Quanta Computer Inc.
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CRT

+5VCRT C561 1U/10V_4

F1 FUSE1A6V_POLY

+5V

40 mils

40 mils

SSM14 spec is 40V 1A

CN15

16 CRT_R_CON — CRT_R_CON — L51 BLM18BA470SN1D — CRT_R1

16 CRT_G_CON — CRT_G_CON — L15 BLM18BA470SN1D — CRT_G1

16 CRT_B_CON — CRT_B_CON — L14 BLM18BA470SN1D — CRT_B1

R362 150/F_4 R84 150/F_4 R79 150/F_4

C658 6.8P/50V_4 C106 6.8P/50V_4 C89 6.8P/50V_4

C632 6.8P/50V_4 C637 6.8P/50V_4 C646 6.8P/50V_4

+5V C43 1U/10V_4

16,19 VSYNC_COM — U4 M74VHC1GT125DF2G — CRTVSYNC_1

16,19 HSYNC_COM — U6 M74VHC1GT125DF2G — CRTHSYNC_1

R39 *0_4/S CRTVSYNC_2

R59 *0_4/S CRTHSYNC_2

R23 *0_4/S DDCCLK3

R27 *0_4/S DDCDAT3

C570 *470P/50V_4 C592 *47P/50V_4 C611 *47P/50V_4 C582 *470P/50V_4

+3V R334 10K/F_4

16 DDCCLK_COM — DDCCLK_COM — Q30 2N7002EPT — DDCCLK2

+3V R335 10K/F_4

16 DDCDATA_COM — DDCDATA_COM — Q31 2N7002EPT — DDCDAT2

R24 2.2K_4 R28 2.2K_4

D14 RB501V-40 +5VCRT +5V_CRT2

inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

+3V

D21 *BAV99W — CRT_R_CON

D20 *BAV99W — CRT_G_CON

D19 *BAV99W — CRT_B_CON

+5V

D15 *BAV99W — DDCCLK_COM

D16 *BAV99W — DDCDATA_COM

D18 *BAV99W — HSYNC_COM

D17 *BAV99W — VSYNC_COM

+5V 11,25,27,29,30,31,32,33,35,42

+3V 2,3,7,8,9,10,11,12,13,14,17,25,27,28,30,31,32,33,34,35,38,40,42

+3V_VGA 15,16,17,18,19,33,39

HDMI

Close to HDMI Connector

+5V_HDMVCC

+3V_VGA

D22 CH501H-40PT

R185 10K/F_4 R193 2.2K_4

16 HDMI_SCL — Q13 2N7002E — HDMI_SCLK

R191 *0_4

D23 CH501H-40PT

R200 10K/F_4 R195 2.2K_4

16 HDMI_SDA — Q14 2N7002E — HDMI_SDATA

R197 *0_4

+5V

Q42 2N7002E

R457 100K/F_4

R469 499/F_4 C_TX2_HDMI+

R467 499/F_4 C_TX2_HDMI-

R464 499/F_4 C_TX1_HDMI+

R463 499/F_4 C_TX1_HDMI-

R466 499/F_4 C_TX0_HDMI+

R465 499/F_4 C_TX0_HDMI-

R458 499/F_4 C_TXC_HDMI+

R456 499/F_4 C_TXC_HDMI-

Close to HDMI Connector

+3V_VGA

16 TMDS_HPD — Q41 MMBT3904-7-F — HDMI_DET_R

R442 150K/F_4 HDMI_DET

R444 10K/F_4

R446 *348K/F_4

16 N_TX2_HDMI+ — C371 .1U/10V_4 — C_TX2_HDMI+

16 N_TX2_HDMI- — C368 .1U/10V_4 — C_TX2_HDMI-

16 N_TX1_HDMI+ — C364 .1U/10V_4 — C_TX1_HDMI+

16 N_TX1_HDMI- — C362 .1U/10V_4 — C_TX1_HDMI-

16 N_TX0_HDMI+ — C367 .1U/10V_4 — C_TX0_HDMI+

16 N_TX0_HDMI- — C365 .1U/10V_4 — C_TX0_HDMI-

16 N_TXC_HDMI+ — C361 .1U/10V_4 — C_TXC_HDMI+

16 N_TXC_HDMI- — C360 .1U/10V_4 — C_TXC_HDMI-

CN21 HDMI CONN

SHELL1 SHELL3 SHELL4 SHELL2

D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET

HDMI_SCLK HDMI_SDATA +5V_HDMVCC HDMI_DET

F2 FUSE1A6V_POLY

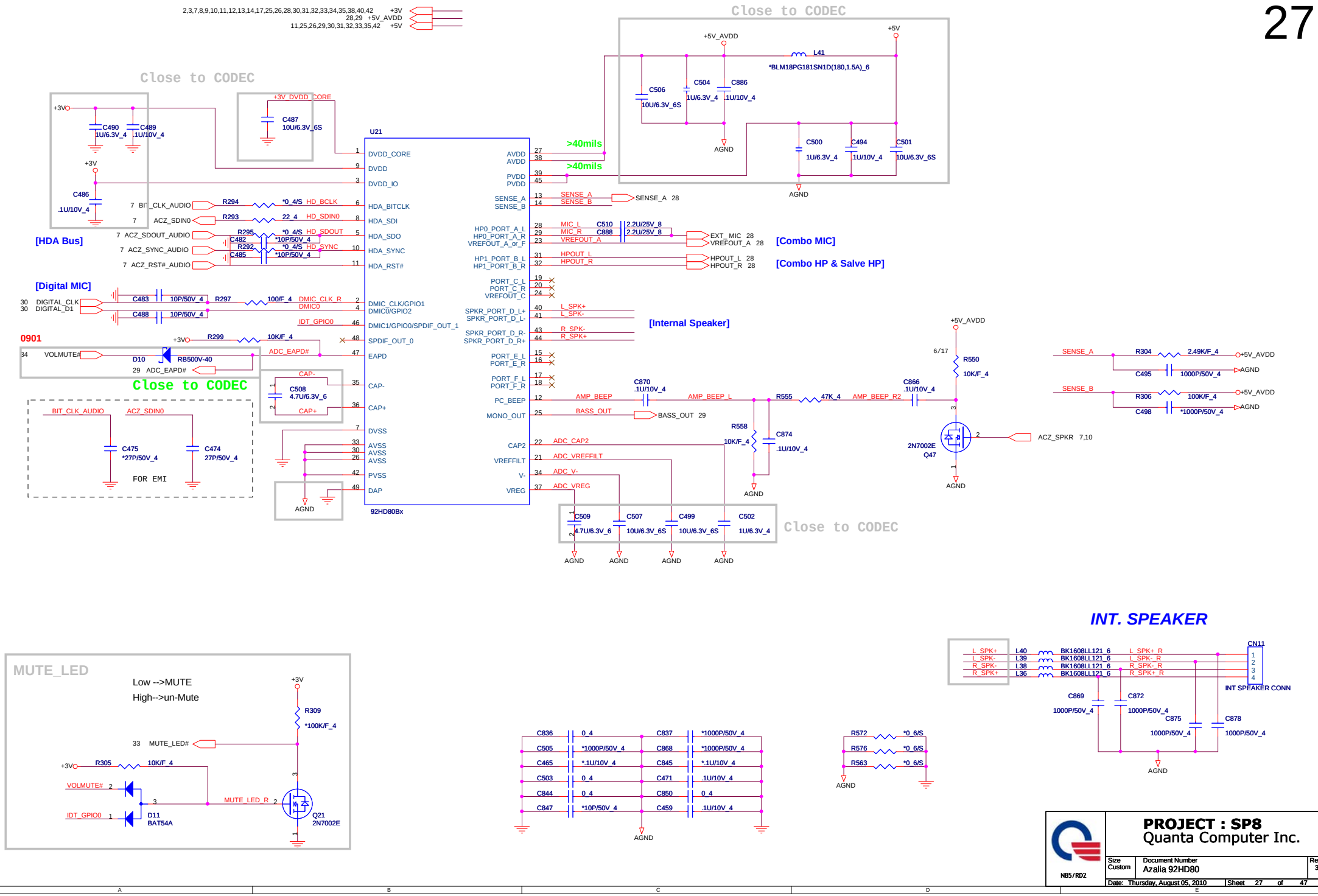
+5V C762 *0.1U/10V_4

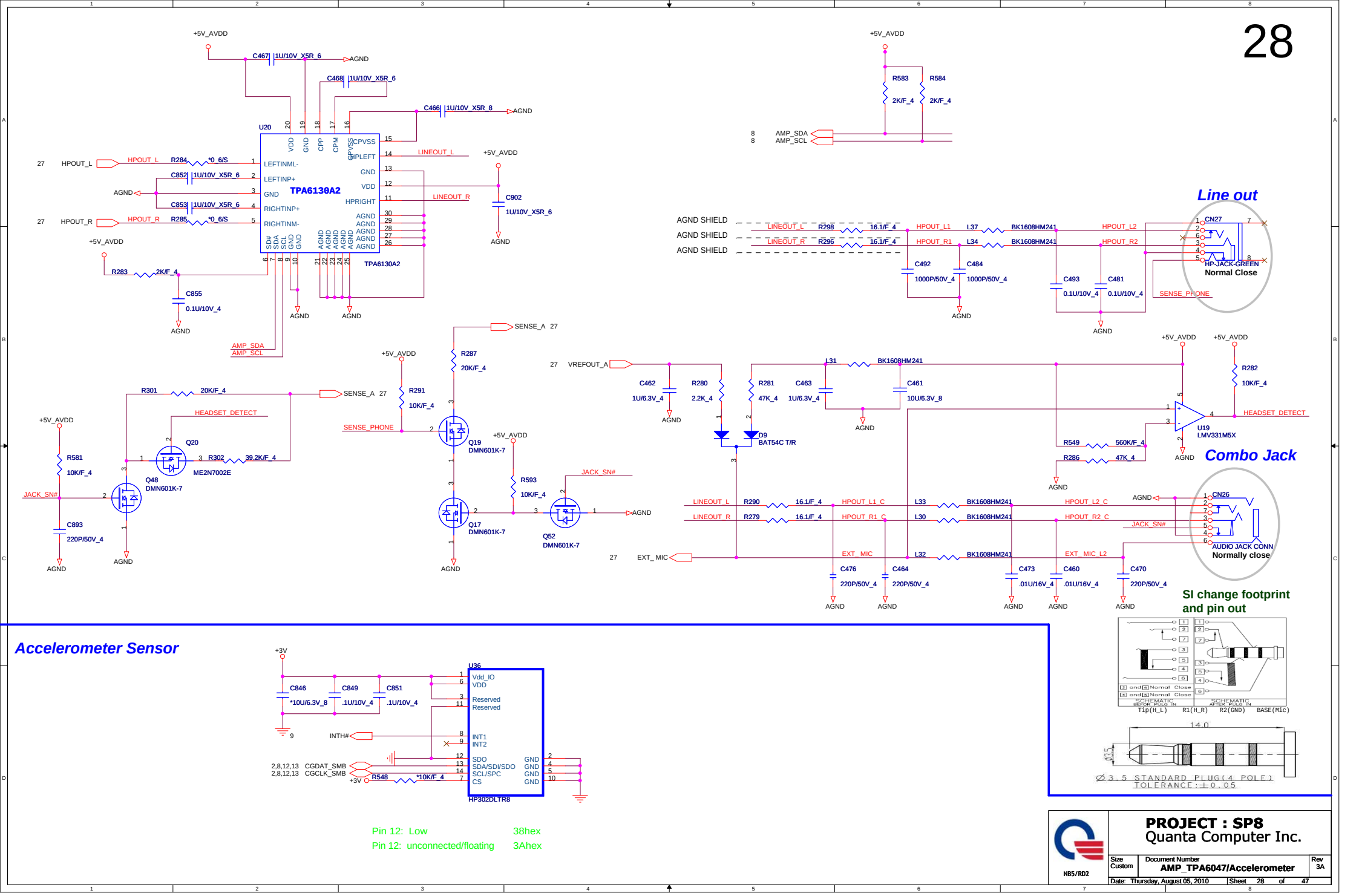
NB5/RD2

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Conn	3A

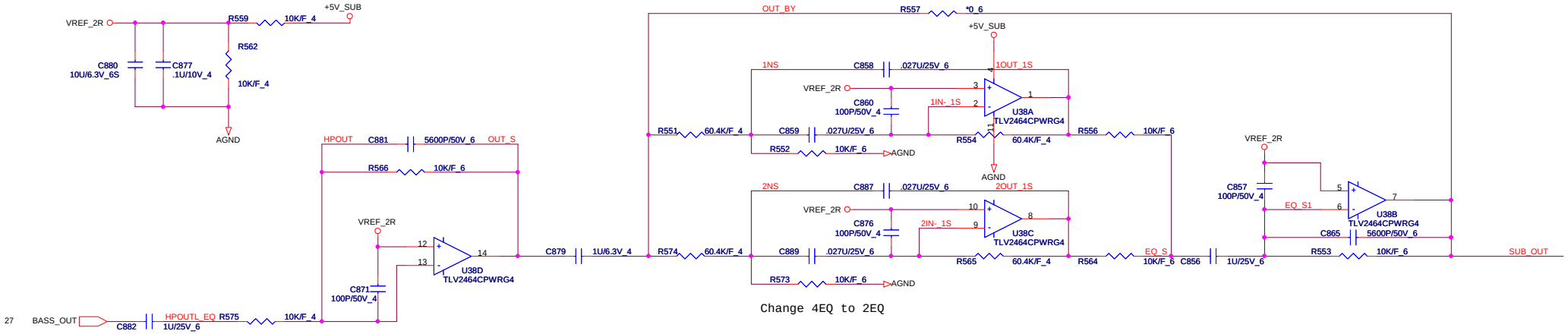
Date: Thursday, August 05, 2010 Sheet 26 of 47


Close to CODEC
Close to CODEC
Close to CODEC
Close to CODEC
U21
92HD80Bx
[HDA Bus]
[Digital MIC]
[Combo MIC]
[Combo HP & Salve HP]
[Internal Speaker]
0901
FOR EMI
MUTE_LED
Low -->MUTE
High-->un-Mute
INT. SPEAKER
INT SPEAKER CONN
PROJECT : SP8
Quanta Computer Inc.
Azalia 92HD80
Thursday, August 05, 2010

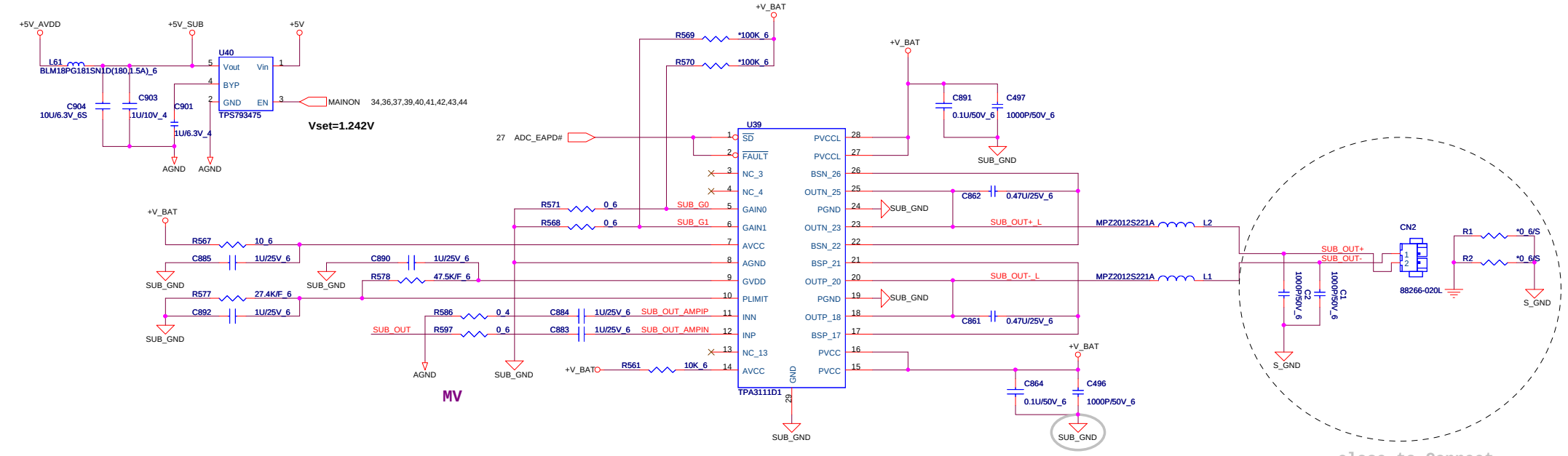


NB5/RD2	**PROJECT : SP8** Quanta Computer Inc.	
Size: Custom	Document Number: AMP_TPA6047/Accelerometer	Rev: 3A
Date: Thursday, August 05, 2010	Sheet 28 of 47	

SUBWOOFER



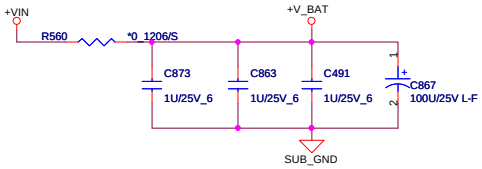
Change 4EQ to 2EQ



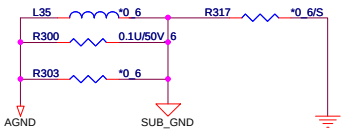
MV

close to Connect

Sub-Woofer power



GAIN1	GAIN0	dB
0	0	20
0	1	26
1	0	32
1	1	36



+3V 2,3,7,8,9,10,11,12,13,14,17,25,26,27,28,30,31,32,33,34,35,38,40,42
+5V_AVDD 27,28
+VIN 25,36,37,38,39,40,41,42,43,44

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SUBWOOFER (EQ & AMP.)	3A
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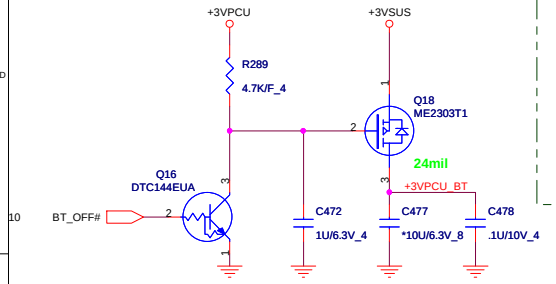
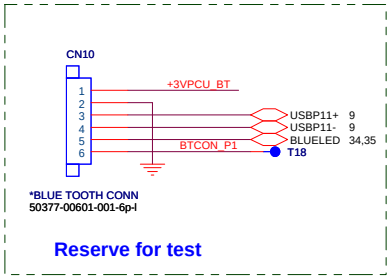
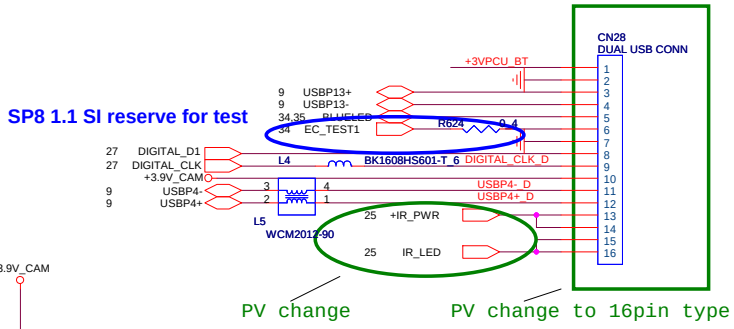
NB5/RD2

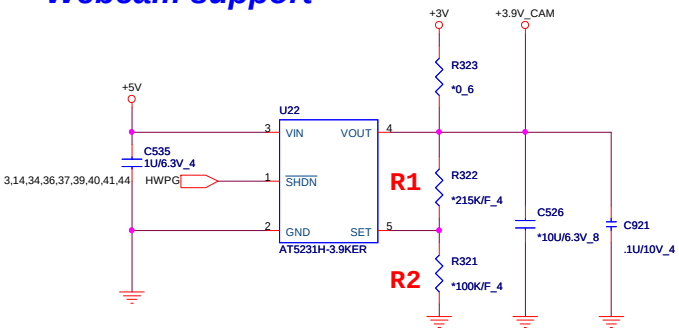
Bluetooth





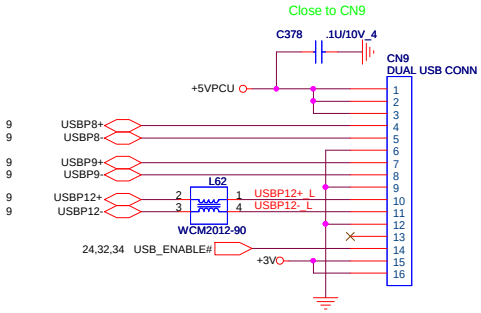


Webcam support

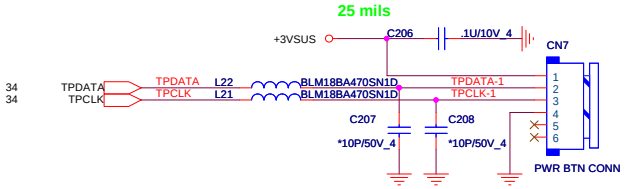


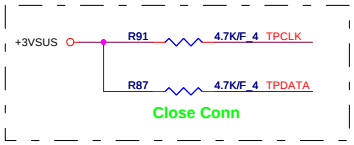
Vout=1.25(1+R1/R2)

Ext USB & Card Reader

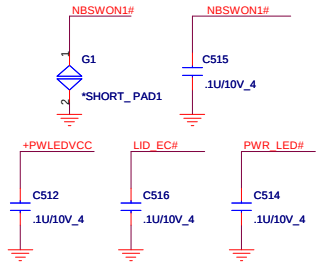


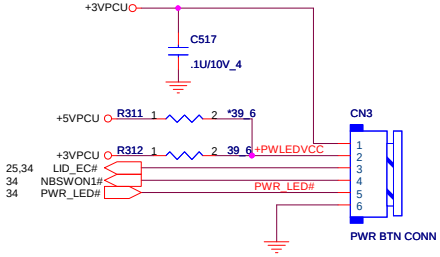
Touch Pad Botton





Power Botton





1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

NB5/RD2	**PROJECT : SP8** Quanta Computer Inc.		
	Size: Custom	Document Number: BT/WC/FT/Touchscreen	Rev: 3A
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T : Stuffed for RTL8111DL(10/100/1000)

for RTL8111DL use close Pin 44,45

+CTRL12DVDD — +CTRL12DVDD — C366 22U/6.3V_8 — C775 0.1U/10V_4

for RTL8111DL use

R468 *0_6/S short0603 — +3V_LAN

Remove R3571,R3573

R3571 and R3573 are used in RTL8111DL , remove R3573 if switching regulator is enable , Remove R3571 external power is used.

+3VLANVCC — R470 *0_8/S short0805 — +3V_LAN

C777 0.1U/10V_4 — C776 0.1U/10V_4 — C778 0.1U/10V_4 — C768 0.1U/10V_4

Close to PIN 1

AL08111DB00 RTL8111DL-GR

Y3 25MHZ — C376 33P/50V_4 — C370 33P/50V_4 — XTAL1 — XTAL2

+CTRL12DVDD — R204 2.49K/F_4 — LANRSET — ENSWREG

+3V_LAN — +DVDD12_LAN — +CTRL12A — LAN_TX# — +3V_LAN

U14 RTL8103EL/8111DL

AVDD33 MDIP0 MDIN0 NC/FB12 MDIP1 MDIN1 GND1 NC/MDIP2 NC/MDIN2 DVDD12/AVDD12 NC/MDIP3 NC/MDIN3

VCTRL12A/SROUT12 GND4 RSET VCTR12VDDSR NC/VDDSR NC/ENSWREG CKTAL2 CKTAL1 NC/AVDD33 NC/LV_PLL LED0 VDD33B

DVDD12B LED1/EESK LED2/EEDI LED3/EEDO EECS GND3 DVDD12A VDD33A ISOLATEB PERSTB LANWAKEB CLKREQB

DVDD12 GND2 HSIP HSIN REFCLK_P REFCLK_N EVDD12 HSOP HSON EGND NC/GPO NC/NC

MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- +DVDD12_LAN MDI3+ MDI3-

LAN_GLINK100# LAN_GLINK10# R207 3.6K_6 — +3V_LAN

EECS — T14

+DVDD12_LAN — +3V_LAN

ISOLATEB — PLTRST#_R# — R205 *0_4/S — PLTRST# 3,9,14,24,34,35

PCIE_WAKE# — PCIE_WAKE# 9,24,35

PCIE_CLK_REQ3# — PCIE_CLK_REQ3# 8

+DVDD12_LAN — EVDD12

8 PCIE_TXP1_LAN — PCIE_TXP6_LAN

8 PCIE_TXN1_LAN — PCIE_TXN6_LAN

8 CLK_PCIE_LAN — CLK_PCIE_LAN

8 CLK_PCIE_LAN# — CLK_PCIE_LAN#

PCIE_RXN1_LAN_L C374 0.1U/10V_4 — PCIE_RXN1_LAN 8

PCIE_RXP1_LAN_L C372 0.1U/10V_4 — PCIE_RXP1_LAN 8

+3V — R208 *1K/F_4 — ISOLATEB — R209 100_4 — LAN_DISABLE# 10,34

R206 15K/F_4 — *RB501V-40 D5

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

U32 NS892405

C766 .01U/16V_4 — V_DAC0 — MDI0+ — MDI0-

C765 .01U/16V_4 — V_DAC1 — MDI1+ — MDI1-

C764 .01U/16V_4 — V_DAC2 — MDI2+ — MDI2-

C763 .01U/16V_4 — V_DAC3 — MDI3+ — MDI3-

TCT1 TD1+ TD1- TCT2 TD2+ TD2- TCT3 TD3+ TD3- TCT4 TD4+ TD4-

MCT1 MX1+ MX1- MCT2 MX2+ MX2- MCT3 MX3+ MX3- MCT4 MX4+ MX4-

LAN_MCT0 — C734 0.01U/100V_0603 — R433 75/F_4 — LAN_MX0+ — LAN_MX0-

LAN_MCT1 — C733 0.01U/100V_0603 — R432 75/F_4 — LAN_MX1+ — LAN_MX1-

LAN_MCT2 — C732 0.01U/100V_0603 — R436 75/F_4 — LAN_MX2+ — LAN_MX2-

LAN_MCT3 — C731 0.01U/100V_0603 — R435 75/F_4 — LAN_MX3+ — LAN_MX3-

C323 1000P/3KV_1808

LAN_GLINK100# — LAN_TX# — LAN_White# — LAN_Amber# — Link

C381 *.01U/16V_4 — C375 *.01U/16V_4

NS892402:GIGABIT DB0AT9LAN05

>60mil — +CTRL12A — L25 4.7UH_8 — >60mil — +CTRL12A_L

Power trace Layout 寬度> 60mil

L23
RTL8111DL (Gaga lan) use 4.7uH
power choke A>600mA tolerance
±15%

C359 22U/6.3V_8 — C373 0.1U/10V_4

EVDD12 — Close to 8111DL DVDD12 pins-- 19

C363 1U/10V_4 — C380 1U/10V_4

+DVDD12_LAN

C773 0.1U/10V_4 — C369 0.1U/10V_4 — C379 0.1U/10V_4 — C779 0.1U/10V_4 — C774 0.1U/10V_4

Close to 8111DL DVDD12 pins-- 10, 13, 30, 36, 39.

PV Stuff for EMI solution

RJ45

+3V_LAN — R380 *30_4 — C674 .1U/10V_4 — LAN_White# — LAN_White

+5V — R596 100_4

CN17

LED_White_N LED_White_P

LAN_MX3- LAN_MX3+ LAN_MX1- LAN_MX2- LAN_MX2+ LAN_MX1+ LAN_MX0- LAN_MX0+

RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+ GND

FOR EMI

LAN_Amber# — LAN_Amber

+3V_LAN — R419 56_4 — C693 .1U/10V_4

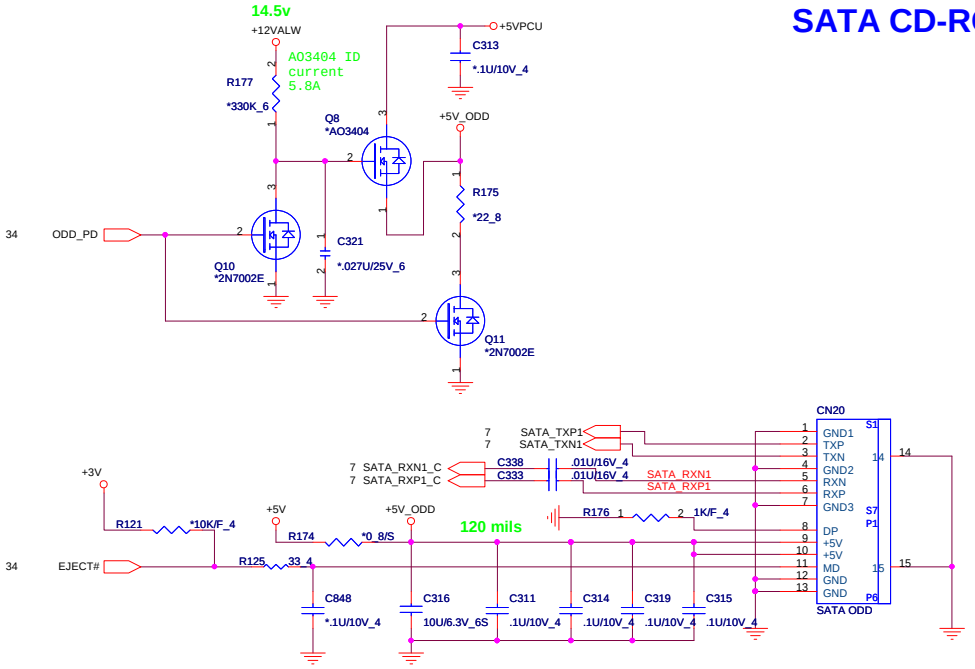
LED_Amber_N LED_Amber_P

RJ45_CONN

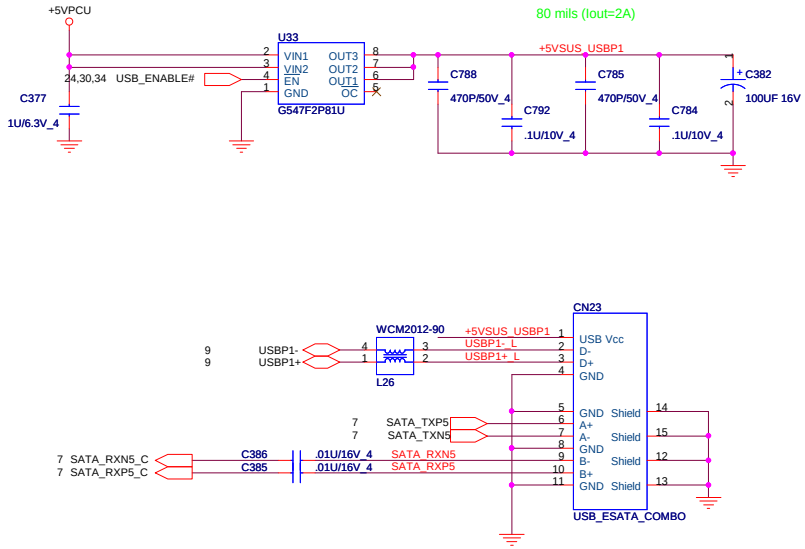
White is Link,Amber is active

PV Stuff for EMI solution

SATA CD-ROM

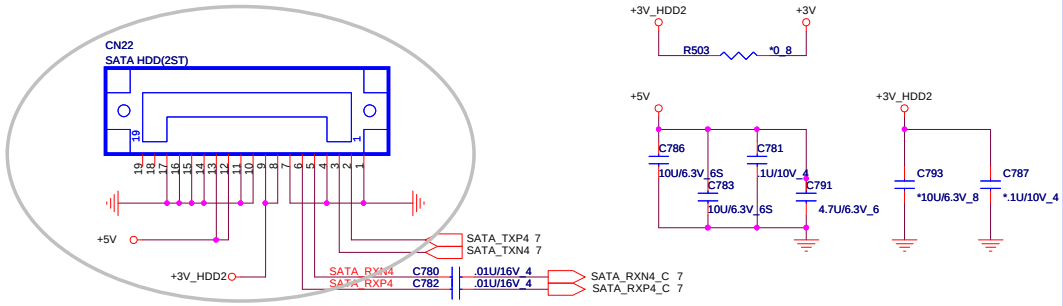


E-SATA



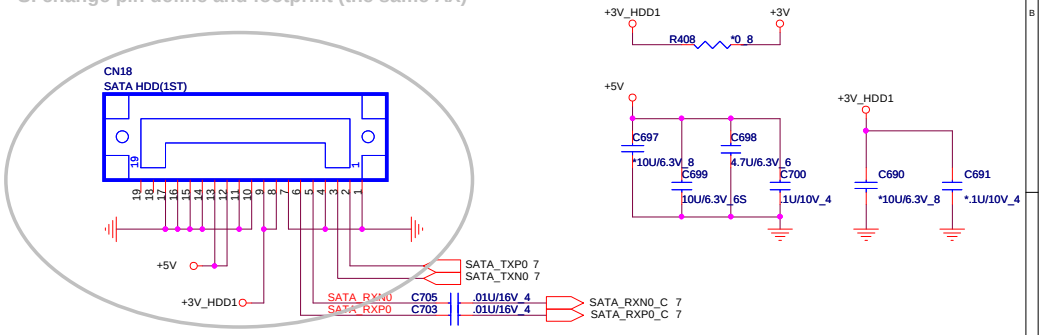
SATA HDD #1

SI change pin define and footprint (the same AX)



SATA HDD #2

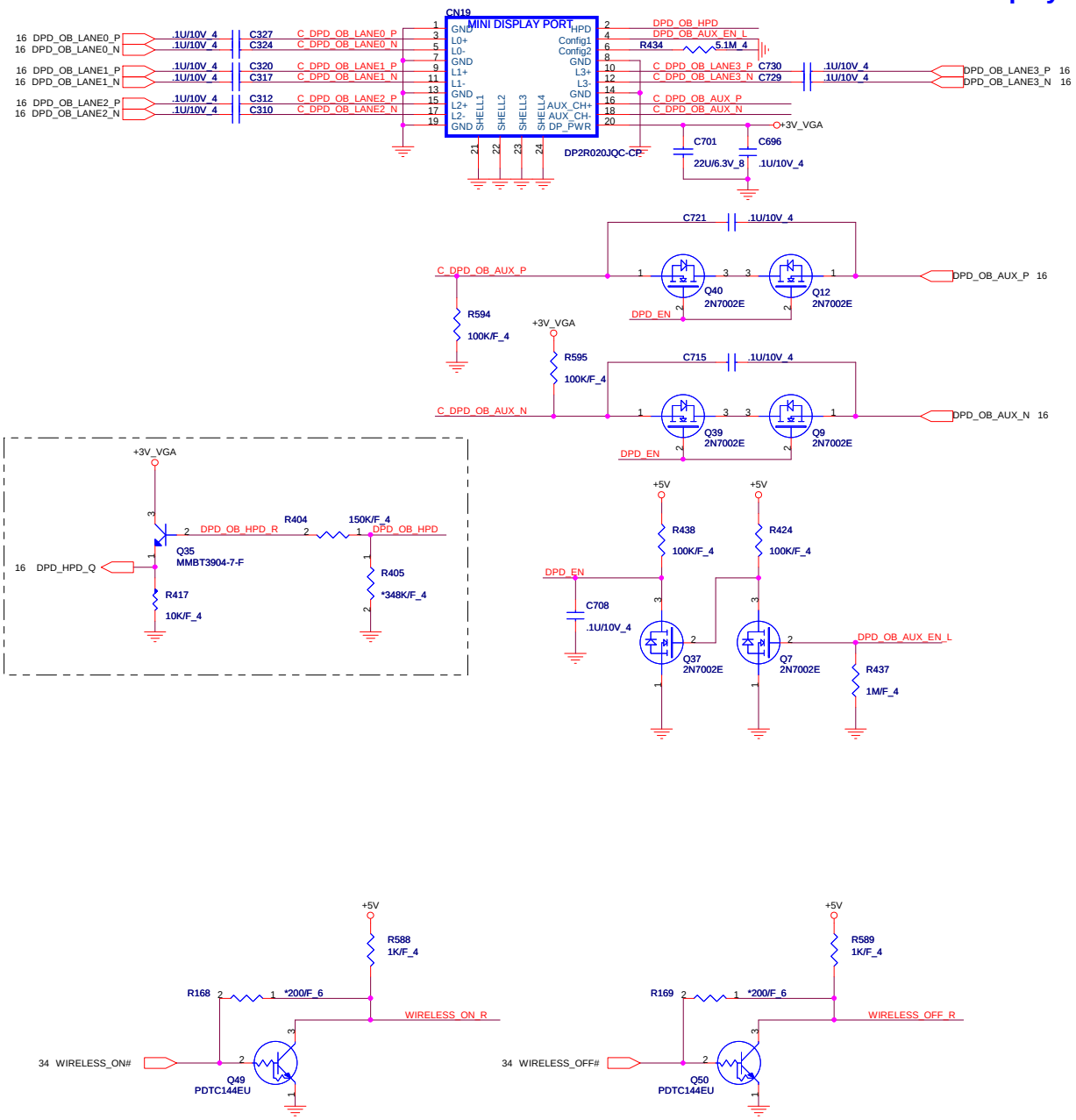
SI change pin define and footprint (the same AX)

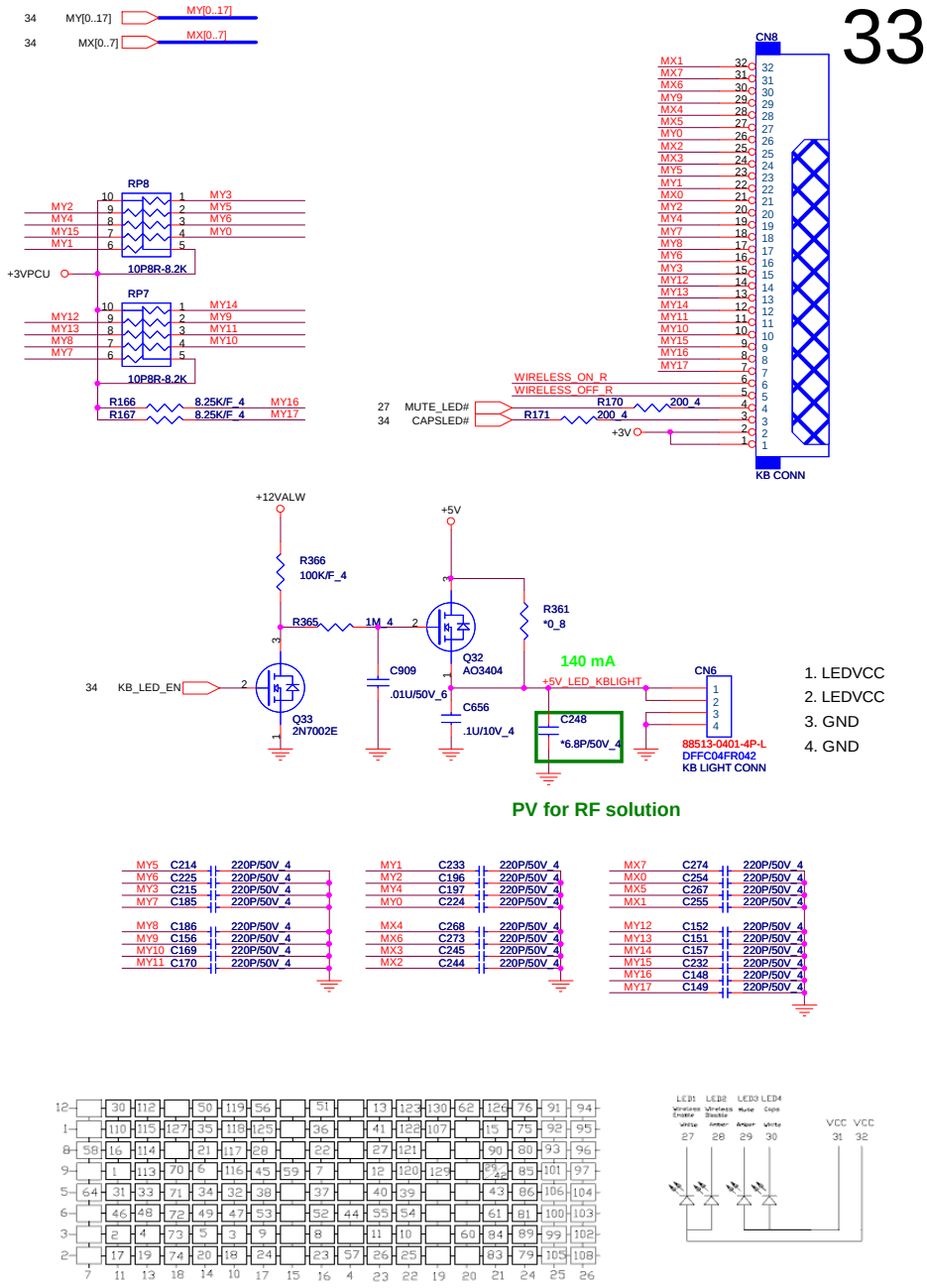


PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ODD/HDD/ONFI	3A
NB5/RD2	Date: Thursday, August 05, 2010	Sheet 32 of 47

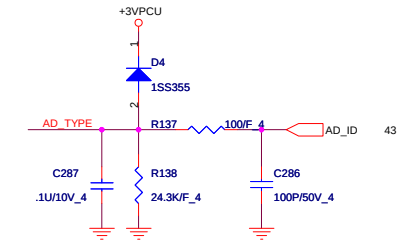
Mini Display





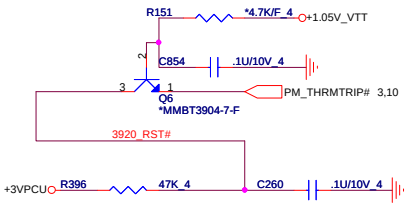
PROJECT : SP8	
Quanta Computer Inc.	
N85/RD2	
Size: Custom	Document Number: KB/LED/POWER CONN
Rev: 3A	
Date: Thursday, August 05, 2010	Sheet 33 of 47

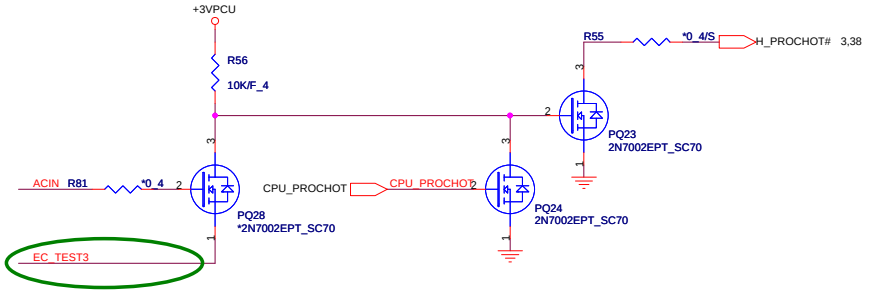
Adapter Type



R273
64.9K -->65W CS36492FB17
33.2K -->90W CS33322FB13
Change to 1SS355 as Current loss

Thermal Shutdown





for SP8 1.1 PV EC request

for SP8 1.1 SI

for SP8 1.1 PV

stuff for SP8 1.1 SI

[For Battery charge]

[For CPU thermal]

for SP8 3D DB

reserve for SP8 1.1 DB

CO-LAYOUT SP8 1.1 DB

For EMI

	GPIO41
SI	1
PV	0

Change to RB500 as Current loss

Hi ==> 120W

Low ==> 65W/90W

Adapter select for EC

PROJECT : SP8
Quanta Computer Inc.

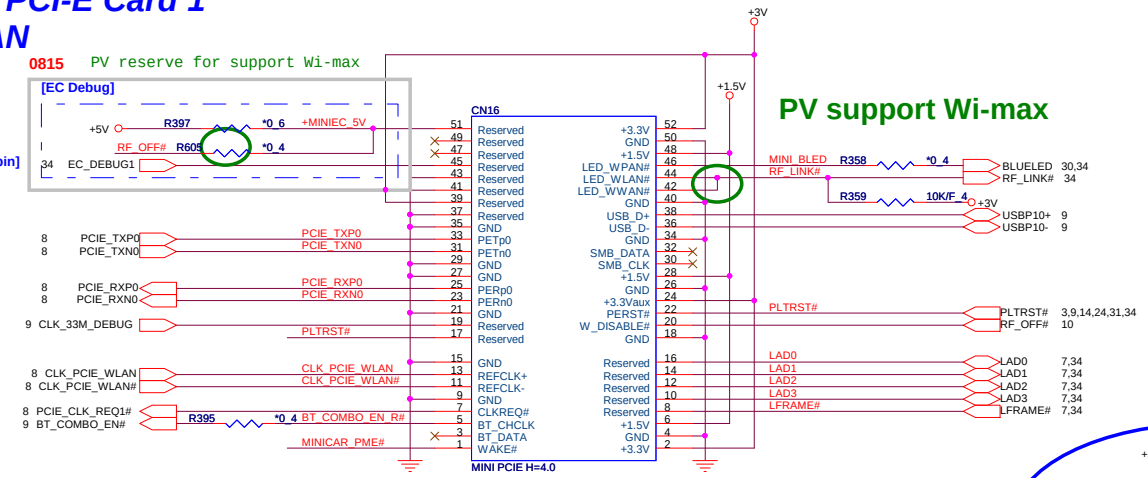
Size	Document Number	Rev
Custom	KB3926/ROM/TP	3A
NB5/RD2	Date: Thursday, August 05, 2010	Sheet 34 of 47

Mini PCI-E Card 1
WLAN

0815 PV reserve for support Wi-max

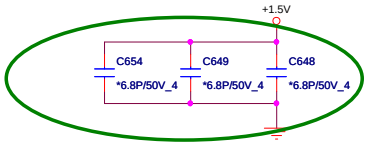
[EC Debug]

[EC Debug pin]

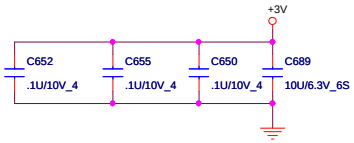


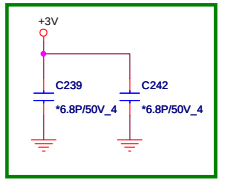
PV support Wi-max

BT_DATA,BT_CHCLK,CLKREQ#,W_DISABLE# pin has internal pull-Down 100k resister.

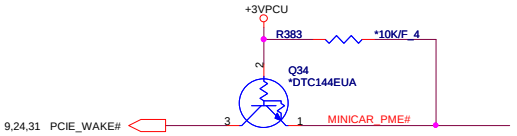


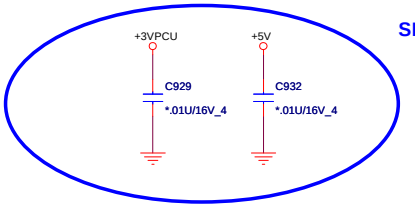
PV for RF solution



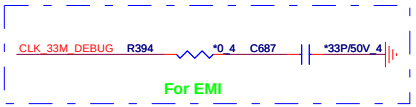


PV for RF solution

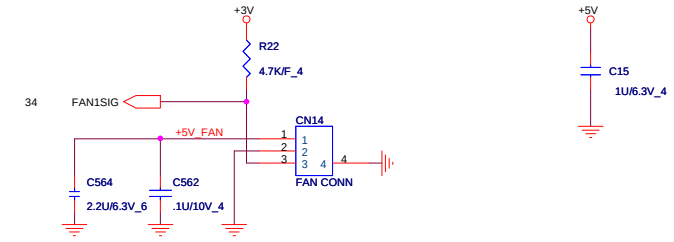




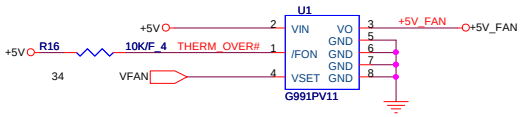
SP8 1.1 SI for RF reserve



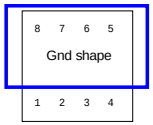
CPU FAN



FANPWR = 1.6*VSET 30 MIL

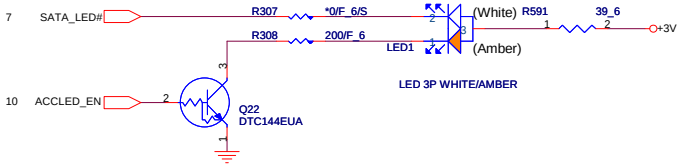


G995 layout notice



LED

朝前



LED 3P WHITE/AMBER

朝前

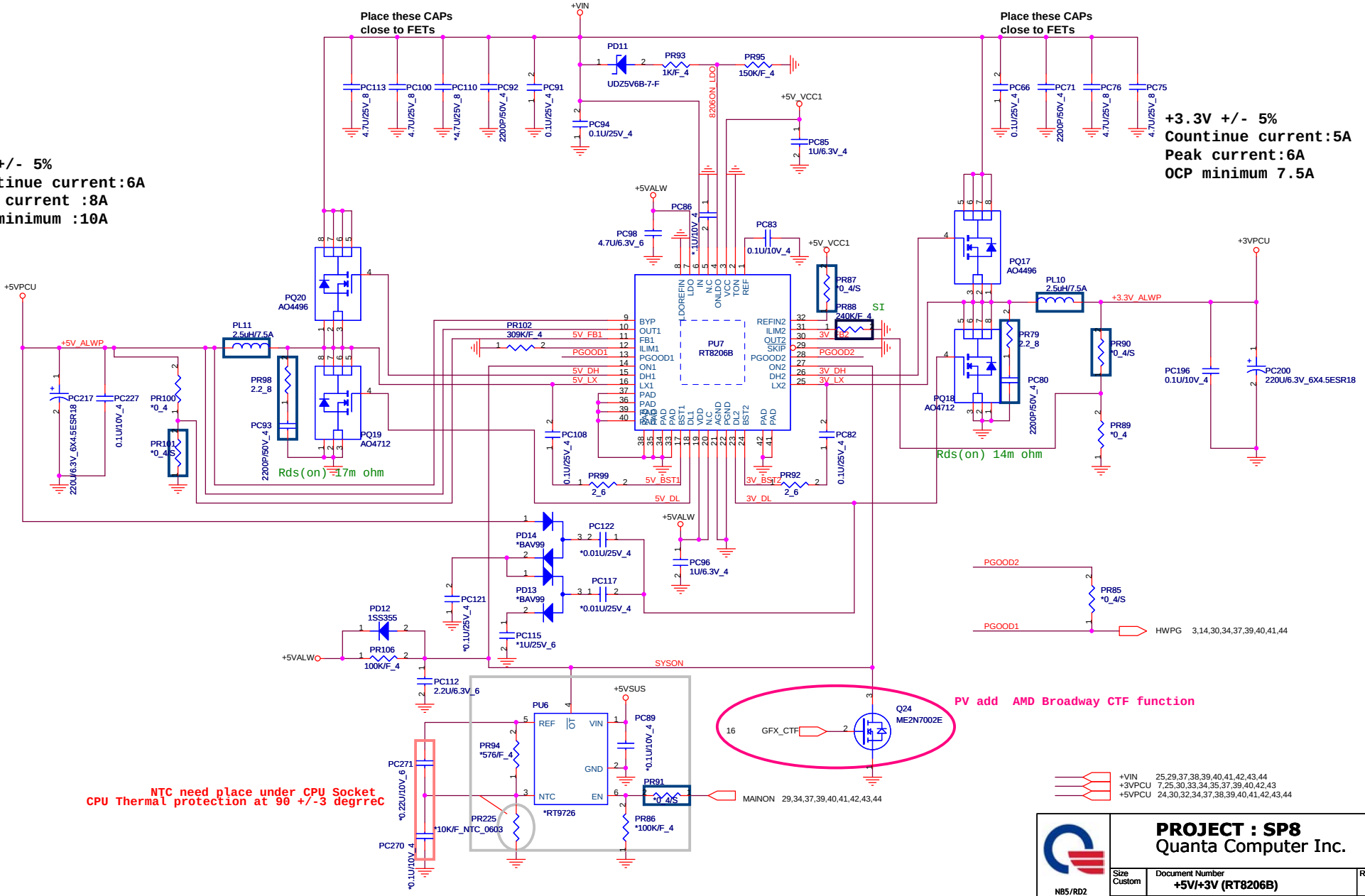
2P WHITE LED(Side-View)

NB5/RD2	PROJECT : SP8 Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCIE CONN X2	Rev: 3A
Date: Thursday, August 05, 2010	Sheet 35 of 47	

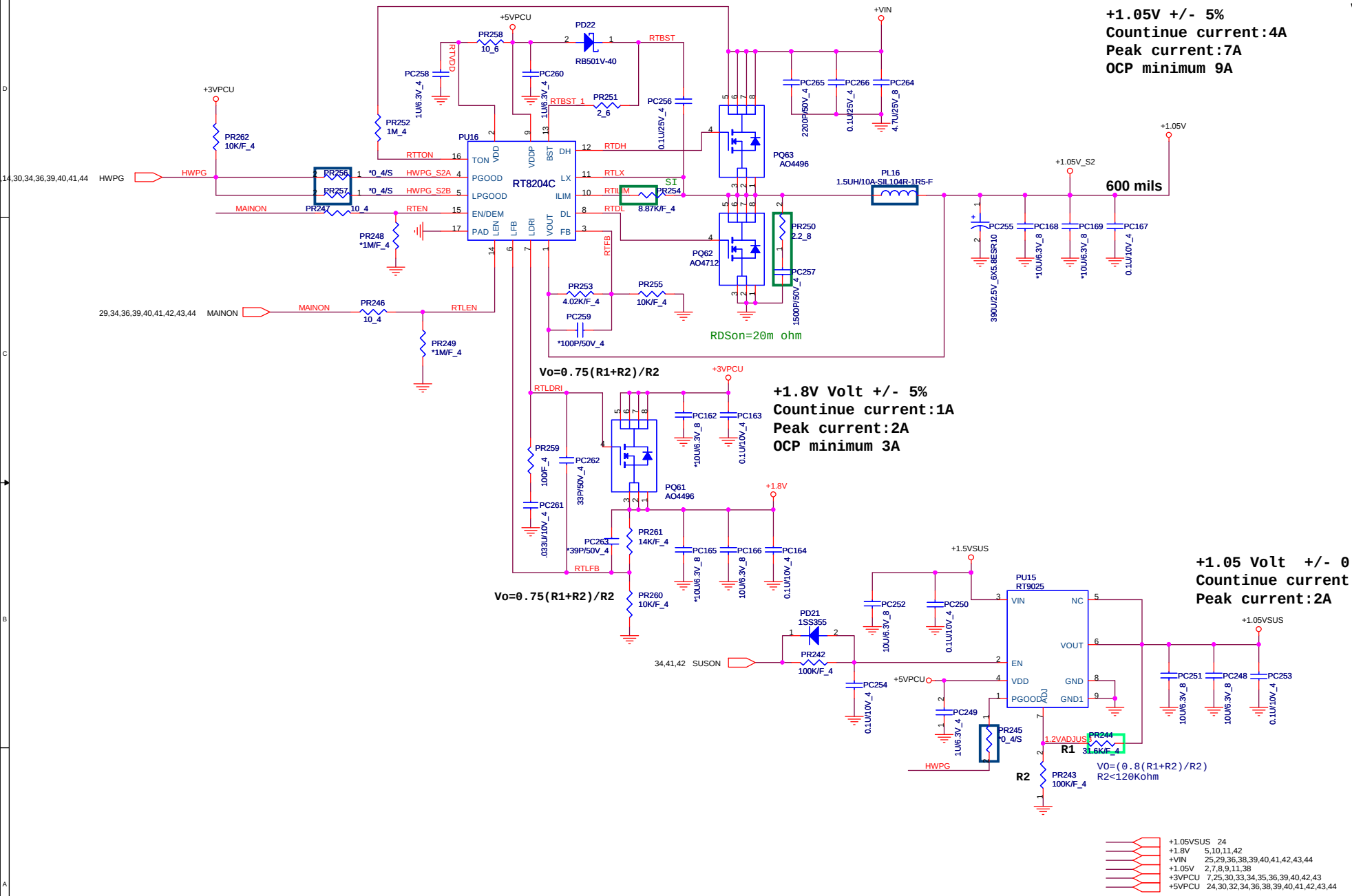
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

+5V +/- 5%
Countinue current:6A
Peak current :8A
OCP minimum :10A

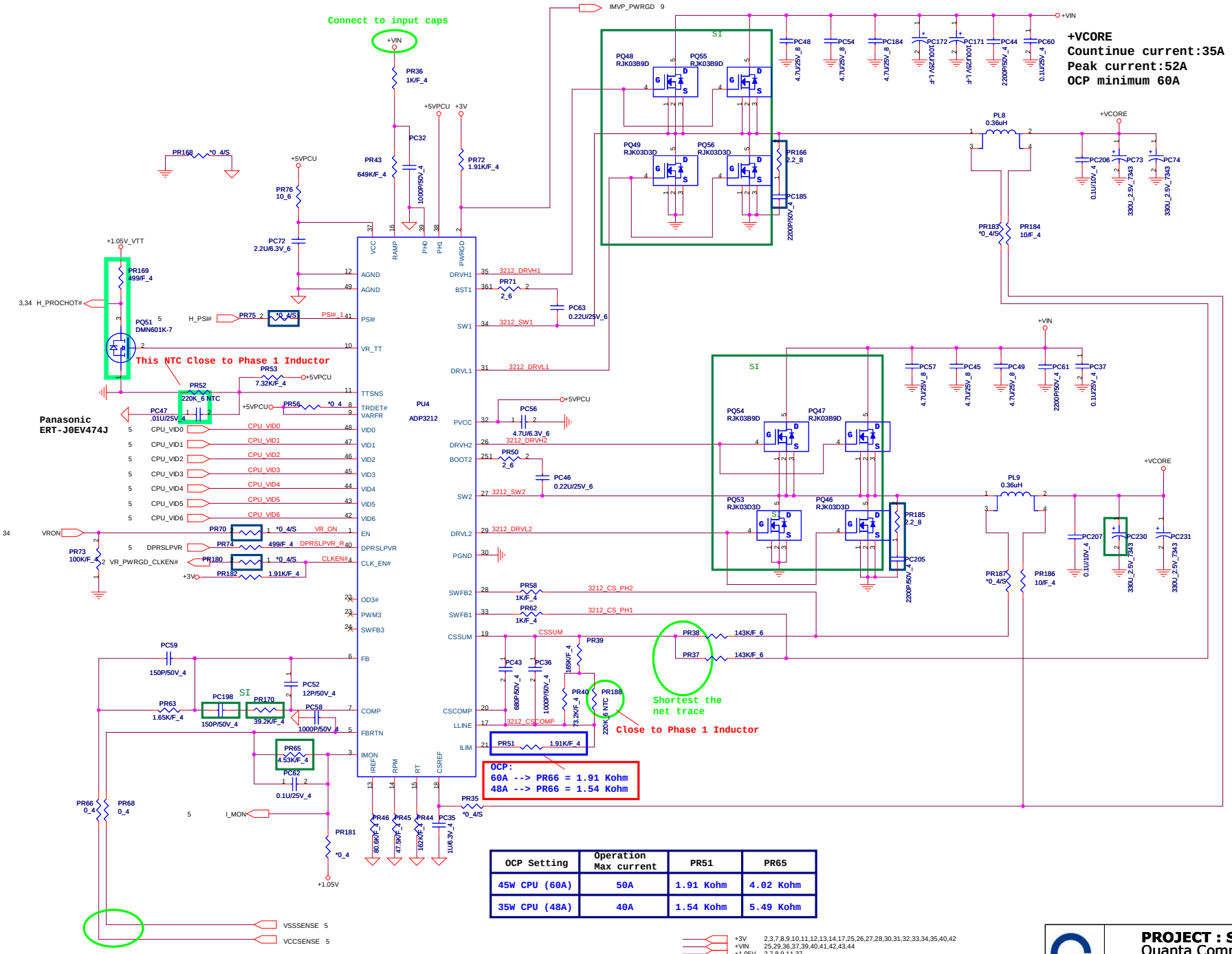
+3.3V +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum 7.5A



NB5/RD2	**PROJECT : SP8** Quanta Computer Inc.	
Size: Custom	Document Number: **+5V/+3V (RT8206B)**	Rev: 3A
Date: Thursday, August 05, 2010	Sheet 36 of 47	



PROJECT : SP8	Quanta Computer Inc.
NB5/RD2	
Size: Custom	Document Number: +1.05V/+1.8V (RT8204C)
Rev: 3A	
Date: Thursday, August 05, 2010	Sheet 37 of 47



OCP Setting	Operation Max current	PR51	PR65
45W CPU (60A)	50A	1.91 Kohm	4.02 Kohm
35W CPU (48A)	40A	1.54 Kohm	5.49 Kohm

+3V 2,3,7,8,9,10,11,12,13,14,17,25,26,27,28,30,31,32,33,34,35,40,42
+VIN 25,29,36,37,39,40,41,42,43,44
+1.05V 2,7,8,9,11,37
+5VPCU 24,30,32,34,36,37,39,40,41,42,43,44
+VCORE 5
+1.05V_VTT 3,5,10,11,34,39

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core (ADP3212)	3A

NB5/RD2

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H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

+VIN 25,29,36,37,38,40,41,42,43,44
+3VS5 8,9,10,11,42
+3VPCU 7,25,30,33,34,35,36,37,40,42,43
+5VPCU 24,30,32,34,36,37,38,40,41,42,43,44
+3V_VGA 15,16,17,18,19,26,33
+1.05V_VTT 3,5,10,11,34,38
+1.8V_VGA 14,16,18

+1.05V_VTT +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A

FOR SP8 1.1 SI

PU11 VT358
PR230 *0_4
PR174 0_4
PR175 40.2K/F_4
PR54 *0_4/S
PR176 44.2K/F_4
PR177 5.76K/F_4
PR178 40.2K/F_4
PC199 2200P/50V_4
PC55 0.1U/25V_4
PQ14 PMST3904
PR179 820K/F_4
PR64 1K/F_4
PR60 *100K/F_4
PR59 100K/F_4
PR67 0_4
PR55 *0_4/S
PL6 0.22uH_MPL73-0R22
PR171 10/F_4
PR172 10/F_4
PR173 10_6
PC197 0.22U/6.3V_4
PC195 1U/6.3V_4
PC193 0.1U/10V_4
PC194 0.1U/10V_4
PC191 10U/6.3V/X5R_8
PC192 10U/6.3V/X5R_8
PC204 0.1U/10V_4
PC186 10U/6.3V/X5R_8
PC187 10U/6.3V/X5R_8
PC203 680P/50V_4
PC190 10U/6.3V/X5R_8
PC188 10U/6.3V/X5R_8
PC189 10U/6.3V/X5R_8

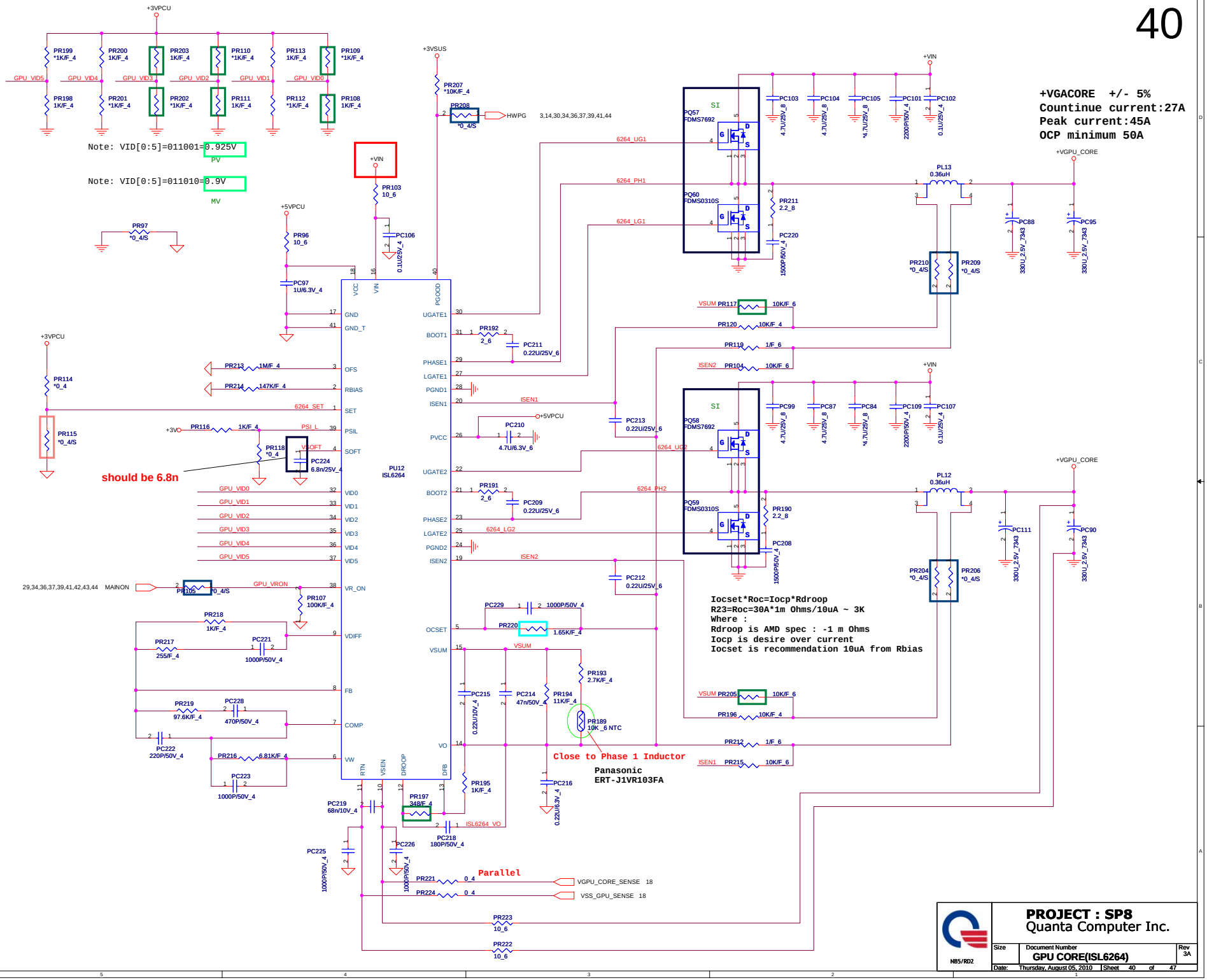
+1.8V +/- 5%
Countinue current:1.2A
Peak current:3A

PU8 RT9025
PR121 10K/F_4
PC118 0.1U/10V_4
PC114 10U/6.3V_8
PC119 0.33U/6.3V_4
PC120 1U/6.3V_4
PR130 127K/F_4
PR127 100K/F_4
PC125 10U/6.3V_8
PC123 10U/6.3V_8
PC126 0.1U/10V_4
R1
R2
VO=(0.8(R1+R2)/R2)
R2<120Kohm

PQ31 DTC144EUA
PR142 1M_4
PR138 1M_4
PR137 *22_8
PR147 *22_8
PQ32 *DMN601K-7
PQ36 *DMN601K-7
PR139 1M_4
PQ30 DMN601K-7
PQ33 ME3424D
PC135 0.1U/10V_4
PC139 *0.01U/25V_4
PC137 0.1U/10V_4
0.24A

Size Custom	Document Number +1.05V_VTT (VT358)	Rev 3A
NB5/RD2	Date: Thursday, August 05, 2010	Sheet 39 of 47

PROJECT : SP8
Quanta Computer Inc.


+VGACORE +/- 5%
Countinue current:27A
Peak current:45A
OCP minimum 50A
Note: VID[0:5]=011001=0.925V
PV
Note: VID[0:5]=011010=0.9V
MV
should be 6.8n
Iocset*Roc=Iocp*Rdroop
R23=Roc=30A*1m Ohms/10uA ~ 3K
Where :
Rdroop is AMD spec : -1 m Ohms
Iocp is desire over current
Iocset is recommendation 10uA from Rbias
Close to Phase 1 Inductor
Panasonic
ERT-J1VR103FA
Parallel
PU12
ISL6264
PROJECT : SP8
Quanta Computer Inc.
GPU CORE(ISL6264)
NB5/RD2
Date: Thursday, August 05, 2010
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+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

(VTT/2A)
+0.75V_DDR_VTT
(3mA)
12 DDR_VTTREF

PU5
RT8207AGQW
VTTGND
VTTSNS
GND
MODE
VTTREF
COMP
NC
VDDQSNS
VDDQSET
S3
S5
NC
GND
VLDOIN
VBST
DRVH
LL
DRVL
PGND
CS_GND
CS
V5IN
V5FILT
PGOOD
VTT

+1.5VSUS
+5VPCU
+VIN
+1.5VSUS_1
PC67 *10U/6.3V_8
PD9 *RB501V-40
PC64 0.1U/25V_4
PR69 2_6
PR78 *0_4/S
PC70 10U/6.3V_8
PC69 10U/6.3V_8
PC78 0.033U/10V_4
PR84 *0_4
PR81 619K/F_4
PC77 1U/6.3V_4
PR80 10_6
PC79 1U/6.3V_4
PR77 7.5K/F_4
PR82 10K/F_4
PR83 10K/F_4
PC81 *100P/50V_4
PC180 390U/2.5V_6X5.8ESR10
PC183 0.1U/10V_4
PC182 *2200P/50V_4
PR167 *2.2_8
PL7 CV-10L0MZ01/DC-10F0M102
PQ52 RJK03B9D
PQ45 RJK0303D
SI
PC38 0.1U/25V_4
PC41 4.7U/25V_8
PC40 4.7U/25V_8
PC39 2200P/50V_4

1116VBST
1116DRVH
1116LL
1116DRVL
1116CS
1116VDDQSET
1116TONSET
V5FILT
HWPG
SUSON
MAINON

need to stuff for S3 and PR263 change to 100K

PD23 1SS355
PR263 100K/F_4
PC267 0.1U/10V_4

+1.0V +/- 5%
Countinue current:1.7A
Peak current:3A

PU10 RT9025
VIN
NC
VOUT
EN
VDD
GND
PGOOD
GND1
ADJ
+1.0V_VGA
PC158 10U/6.3V_8
PC153 0.1U/10V_4
PR153 2.2K/F_4
PC155 0.1U/10V_4
PC152 1U/6.3V_4
PR152 *0_4/S
PR150 25.5K/F_4
PR149 100K/F_4
R1
R2
1.2VADJ1.0V
VO=(0.8(R1+R2)/R2)
R2<120Kohm
PC149 10U/6.3V_8
PC150 10U/6.3V_8
PC148 0.1U/10V_4

PROJECT : SP8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	3A

NB5/RD2

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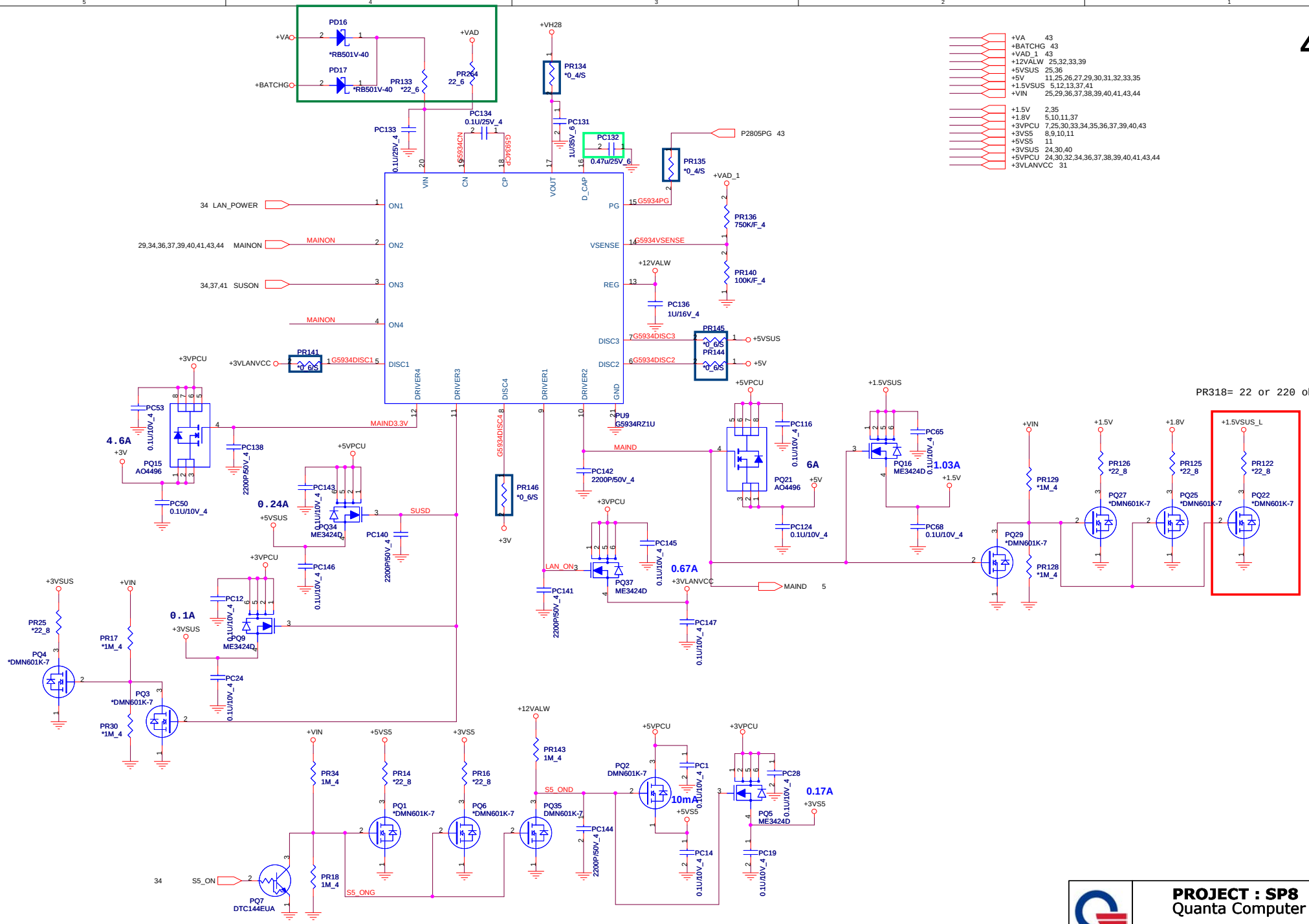
+VA 43
+BATCHG 43
+VAD_1 43
+12VALW 25,32,33,39
+5VSUS 25,36
+5V 11,25,26,27,29,30,31,32,33,35
+1.5VSUS 5,12,13,37,41
+VIN 25,29,36,37,38,39,40,41,43,44
+1.5V 2,35
+1.8V 5,10,11,37
+3VPCU 7,25,30,33,34,35,36,37,39,40,43
+3VS5 8,9,10,11
+5VS5 11
+3VSUS 24,30,40
+5PVCU 24,30,32,34,36,37,38,39,40,41,43,44
+3VLANVCC 31
PR318= 22 or 220 ohm ?
PROJECT : SP8
Quanta Computer Inc.
Dis-charge IC (P2806)
NB5/RD2
Size Custom
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TOP DC_JACK
65W/90W

PV reserve for EMI solution

PV EMI solution

SI EC change to SM bus1

MV

Place this cap close to EC

Place this cap close to EC

Place this cap close to EC

CN13 DC-IN CONN

PC273 *0.1U/25V_4

PU1 OZ8681

PU2 *P2805MF AQ

PU3 *SN74AHC1G14DBVR

PQ64 UMT1N

PQ44 P1003EVG

PQ42 AO4496

PQ43 AO4712

PQ10 PDTC144EU

PQ13 PDTC144EU

PQ11 PDTC144EU

PQ8 IMD2

PQ12 DMN601K-7

PD24 P4SMAJ20A

PD6 RB501V-40

PD10 P4SMAJ20A

PD18 MEK100-05-DPS

PD1 *1SS355

PD2 1SS355

PD3 UDZ5V6B-7-F

PD4 UDZ5V6B-7-F

PD5 1SS355

PD7 *1SS355

PD8 *1SS355

PD15 1SS355

PD25 1SS355

PD26 1SS355

PD27 RB501V-40

PQ50 P0603BDG

PL1 5A/08

PL2 10UH

PL3 5A/08

PL4 5A/08

PL5 5A/08

CN12 200045MR008G10JZR DFHD08MR095 bat-bp02083-b85b5-9h-8p-l-v

PC2 1U/10V_4

PC3 0.47U/10V_4

PC4 0.01U/25V_4

PC5 1U/10V_4

PC6 0.01U/25V_4

PC7 2.2U/10V_6

PC8 *0.1U/50V_6

PC9 *0.01U/25V_4

PC10 *100P/50V_4

PC11 *100P/50V_4

PC13 1U/25V_8

PC15 0.01U/25V_4

PC16 0.1U/50V_6

PC17 1U/10V_4

PC18 0.1U/10V_4

PC20 *0.1U/50V_6

PC21 *0.01U/25V_4

PC22 0.1U/25V_4

PC23 4.7U/25V_8

PC25 *1U/10V_4

PC26 4.7U/25V_8

PC27 *4.7U/6.3V_8

PC29 0.1U/25V_4

PC30 *10U/6.3V_8

PC31 0.22U/25V_8

PC33 0.1U/25V_4

PC34 *0.1U/25V_4

PC42 1000P/50V_4

PC51 1000P/50V_4

PC127 1U/10V_4

PC128 0.1U/10V_4

PC129 0.01U/25V_4

PC130 0.01U/25V_4

PC170 *2200P/50V_4

PC174 4.7U/25V_8

PC173 4.7U/25V_8

PC181 *4.7U/25V_8

PC178 *4.7U/25V_8

PC177 *4.7U/25V_8

PC175 0.1U/25V_4

PC176 0.1U/25V_4

PC179 0.1U/25V_4

PC201 0.1U/25V_4

PC202 0.1U/50V_6

PC272 *10U/25V_8

PR1 10/F_4

PR2 0_4

PR3 *3.3K/F_4

PR4 *1.3K/F_4

PR5 100K/F_4

PR6 100K/F_4

PR7 75K/F_4

PR8 12.4K/F_4

PR9 10/F_4

PR10 10/F_4

PR11 0_4

PR12 *0_4

PR13 *22_6

PR15 0_4

PR19 330_4

PR20 330_4

PR21 10K/F_4

PR22 1K/F_4

PR23 *0_4

PR24 2_6

PR25 *10K_6

PR26 *0_4

PR27 10_8

PR28 100_4

PR29 *0_4/S

PR31 *20K_6

PR32 *10K_6

PR33 *1M_4

PR41 150K/F_4

PR42 0_4

PR47 10K_6

PR48 *100/F_4

PR49 100/F_4

PR57 10K_6

PR124 *100K/F_4

PR127 1M_4

PR131 1M_4

PR132 10/F_4

PR159 *0_2/S

PR160 *2.2_8

PR161 RL3720WT-R020

PR162 *0_2/S

PR163 *0_2/S

PR164 RC2512-R010

PR165 *0_2/S

PR174 4.7U/25V_8

PR180 *4.7U/25V_8

PR181 *4.7U/25V_8

PR178 *4.7U/25V_8

PR177 *4.7U/25V_8

PR265 100K/F_4

PR266 *0_4/S

PR267 100K/F_4

PR268 10/F_4

PR269 1K_6

PR270 220K_4

PR271 220K_4

PR272 1M_4

PR273 1M_4

PR274 220K_6

+BATCHG

+VA

+VAD

+VAD_1

+VH28

+PRWSRC

+VIN

+3VPCU

+5VPCU

BATDIS_d_dod

BATDIS_G

ACOK_IN

ACOK#

ACIN

AC_LED_ON

AC_LED_ON# 34

MBATLED0

MBATLED0# 34

MAINON

29,34,36,37,39,40,41,42,44

AD_ID

AD_AIR 34

8681_ACAV

8681_VDDP

8681_VDDA

8681COMP

8681ICHP

8681ICHM

8681IACP

8681IACM

8681VDCM

8681HDR

8681LX

8681LDR

8681LR

8681B

DCIN

SYS_I 34

D/C# 34

D/C#_S6A

MBCLK 34

MBDATA 34

MBCLK

MBDATA

SCL

SDL

ACAV

VAC

COMP

GND

IAC

IACP

IACM

VDDA

VDDP

BST

HDR

LX

LDR

ICHP

ICHM

CSIP

CSIN

BATT+

SMD

SMC

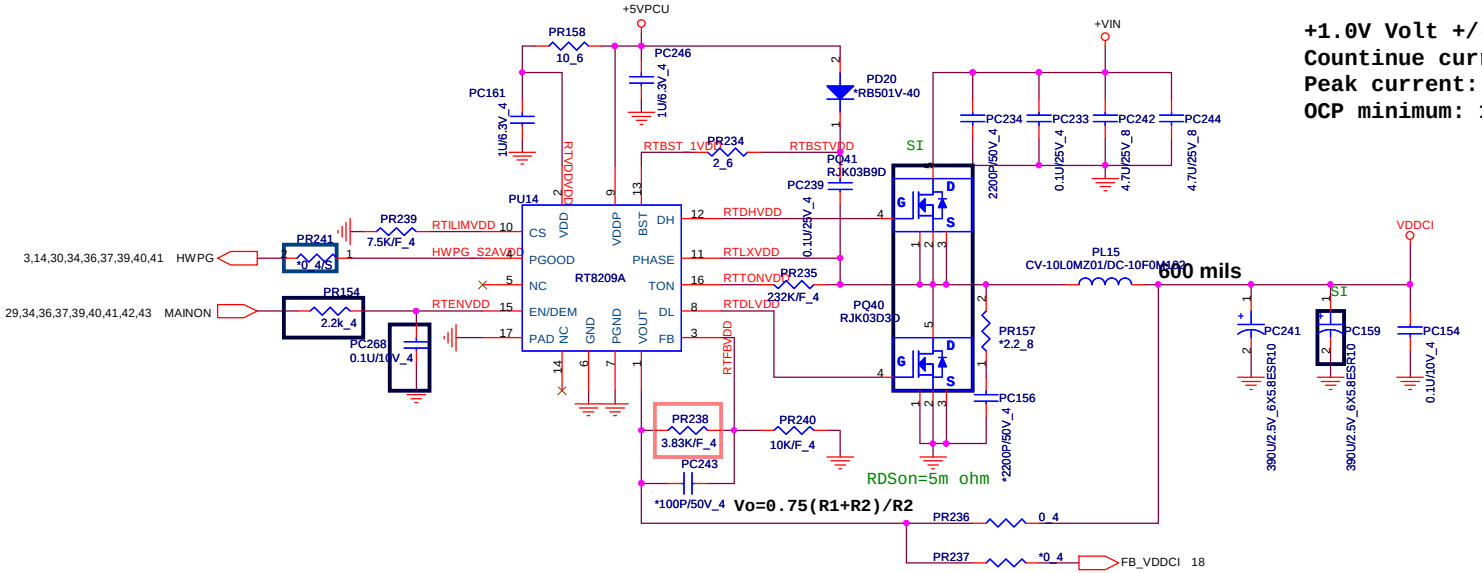
B_TEMP_MBAT

TEMP_MBAT 34

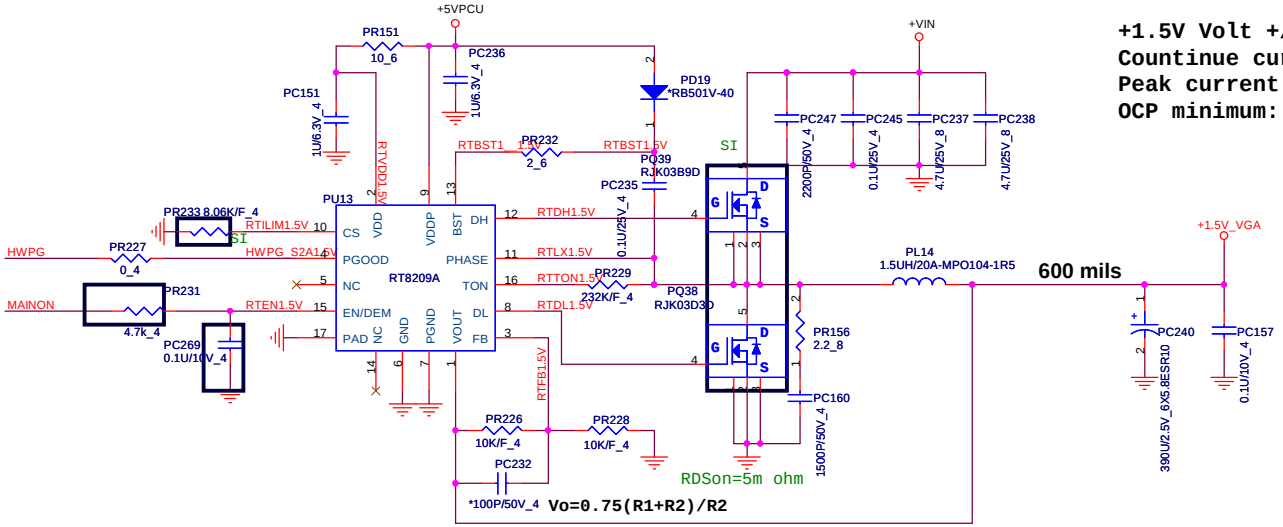
MBDATA 34

MBCLK 34

+VA 42
+VAD_1 42
+VH28 42
+BATCHG 42
+5VPCU 24,30,32,34,36,37,38,39,40,41,42,44



+1.0V Volt +/- 5%
Countinue current:9A
Peak current: 12A
OCP minimum: 15A



+1.5V Volt +/- 5%
Countinue current:9A
Peak current:12A
OCP minimum: 15A

NB5/RD2	**PROJECT : SP8** Quanta Computer Inc.	
Size Custom	Document Number **VGA Core/+1.8VGFX/1.0VGFX**	Rev 3A
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