Compal Confidential

Pixar AMD M/B LA-9851P Schematics Document

AMD Richland APU / Bolton FCH M3

Date : 2012-11-07

Version T0.1

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/11/07	Deciphered Date	2012/11/07	Title: SCHEMATIC, MB A9851

Size: B	Document Number: 4019NK	Rev: A
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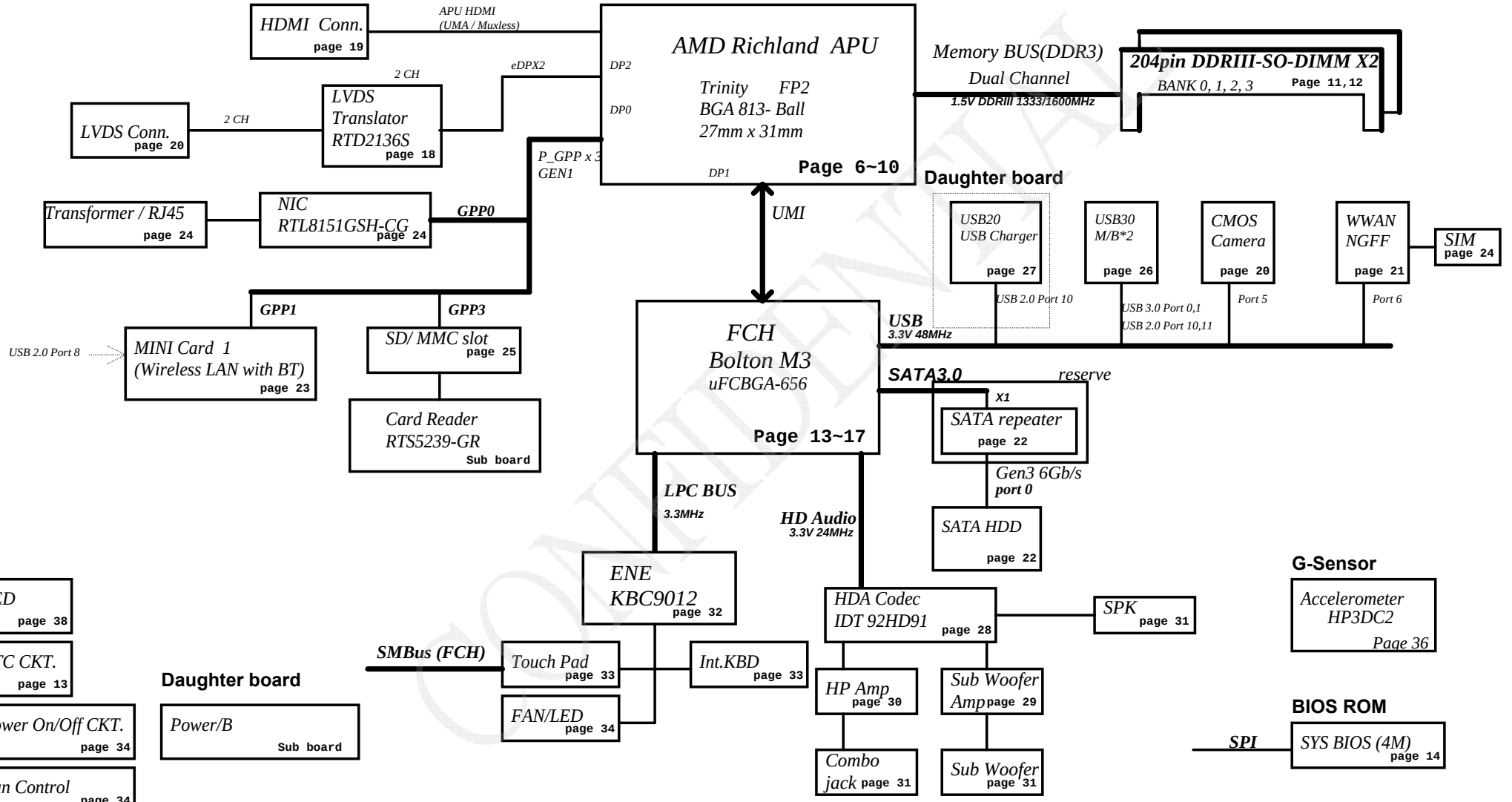
Model Name : VPU00 AMD

AMD Richland



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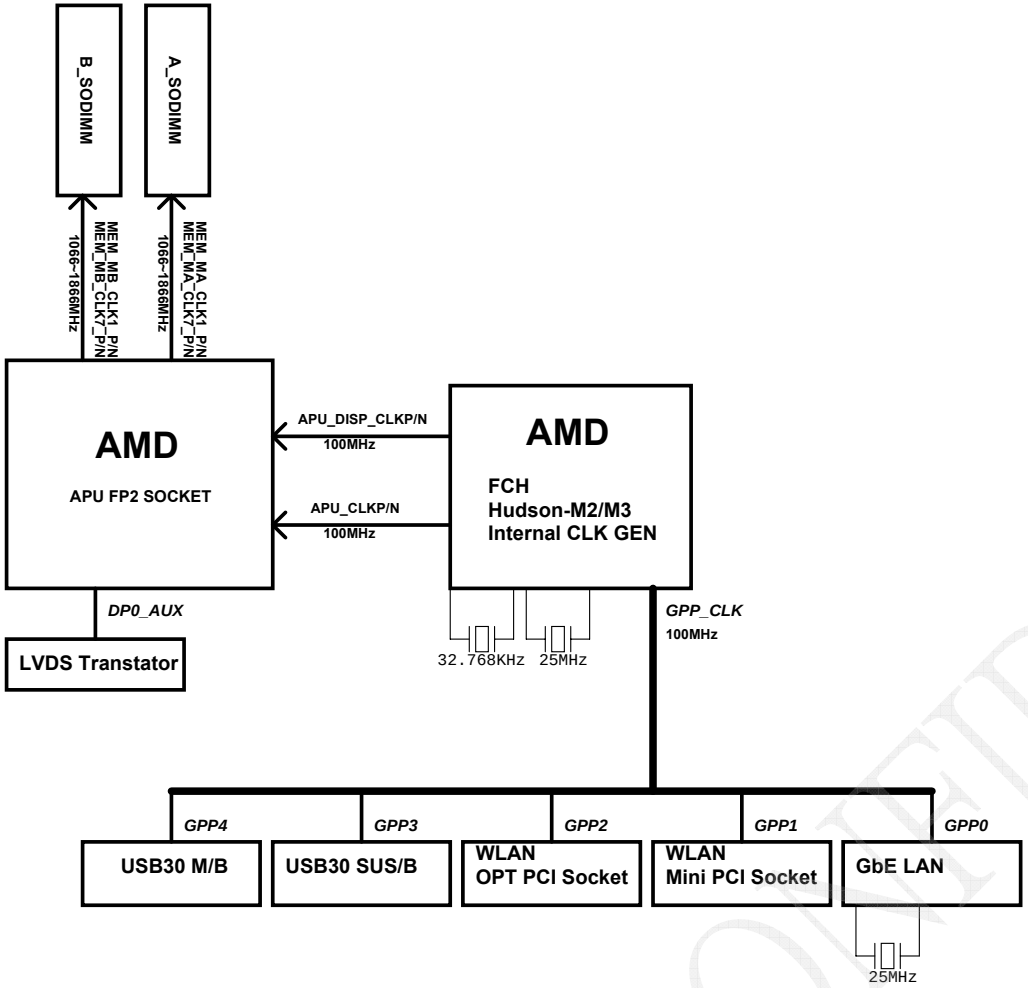
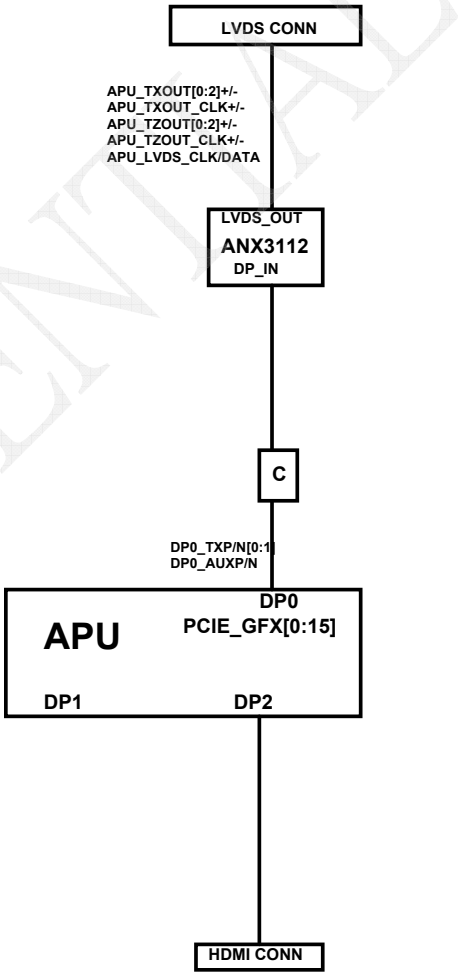
CLOCK DISTRIBUTION



DISPLAY OUTPUT



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

USB Port Table

USB 2.0	USB 1.1	Port	1 External USB Port
EHCI1	UHCI0	0	USB2.0 (left side)
		1	
	UHCI1	2	
		3	
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	BT
		9	
	UHCI5	10	USB2.0 (Right side)
		11	USB2.0 (Right side)
	UHCI6	12	
		13	

USB 3.0	Port	1 External USB Port
	0	USB3.0 (Right side)
	1	USB3.0 (Right side)
	2	
	3	

Audio Codec SSID

Platform	Platform ID
Evora 1.0 UMA	0x18DE

x = 1 is read cmd, x= 0 is writee cmd.

BOM Option Table

BOM Structure	Description

BOM Config

UMA V

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (GPU)	1001 101X b	9AH
SB-TSI (APU)	1001 100X b	98H
LVDS TR(RTD-2132S)	1010 100X b	A8H
VGA Internal Thermal	1000 001X b	82H

FCH SM Bus 0 address

Device	Address	HEX
DDR DIMM1	1101 000X b	90
DDR DIMM2	1101 001X b	94

FCH SM Bus 1 address

Device	Address	HEX

SMBUS Control Table

	SOURCE	BATT	Charger	HP Amp	MINI3	SODIMM	EC_SMB_CK2 EC_SMB_DA2	EC_SMB_CK1 EC_SMB_DA1	G-Sensor	TP
EC_SMB_CK1 EC_SMB_DA1	KB932	V	V						V	
EC_SMB_CK2 EC_SMB_DA2	KB932			V						
FCH_SCLK0 FCH_SDATA0	FCH					V				
FCH_SCLK1 FCH_SDATA1	FCH									V

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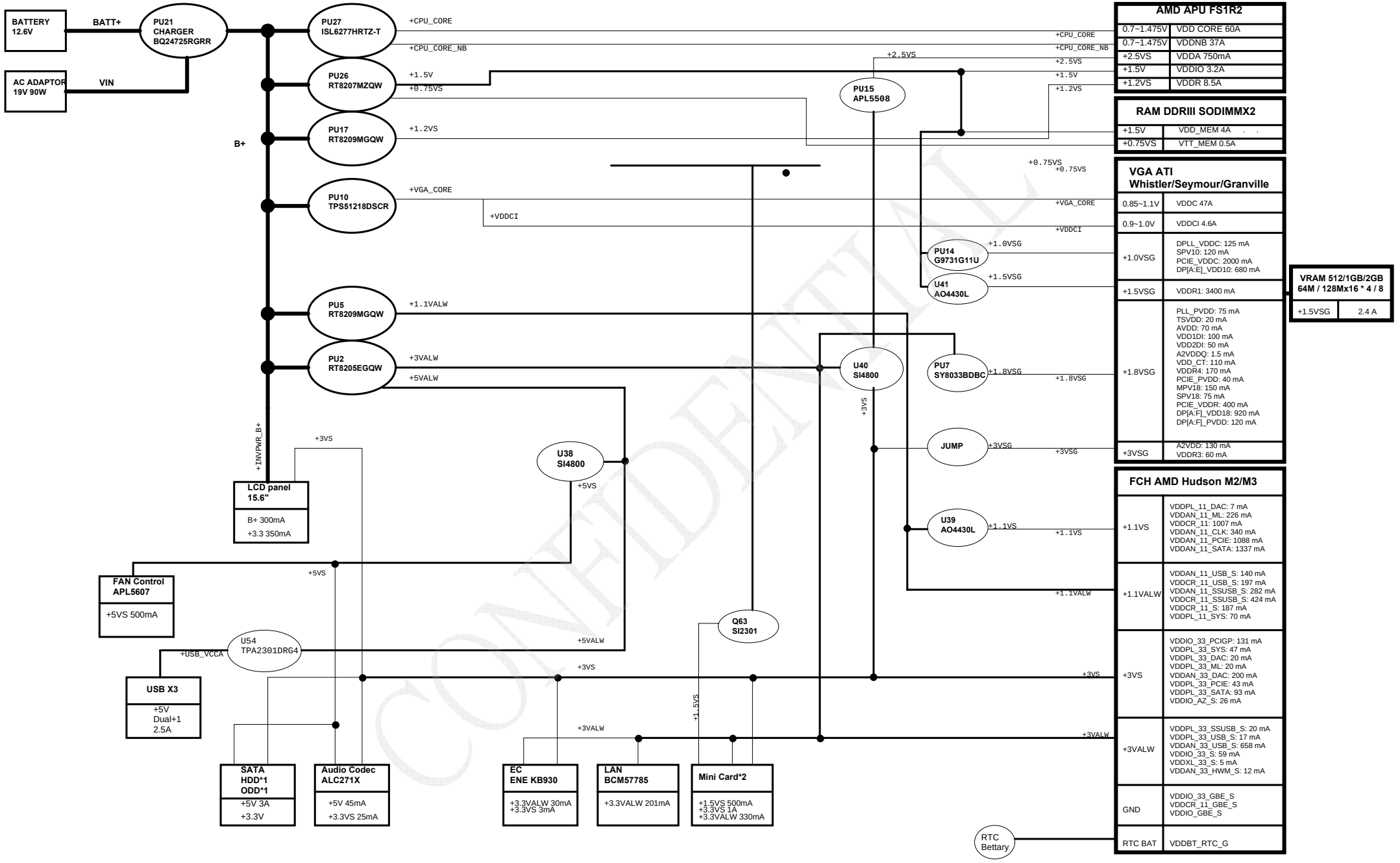

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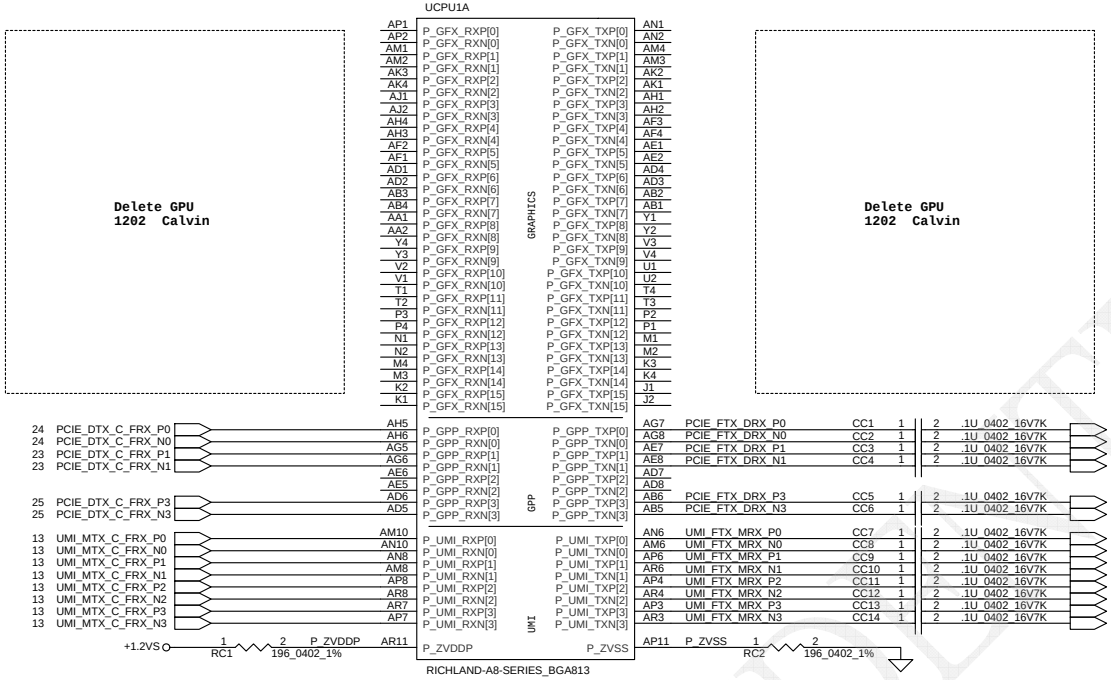
GPU

Delete GPU
1202 Calvin



Delete GPU
1202 Calvin

GPU

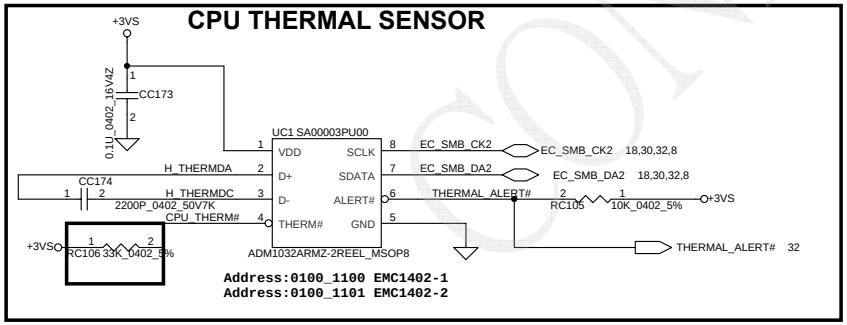
GLAN
WLAN
Card reader
UMI

10/4 Eric chagne back on RC1 & RC2.

P_ZVDDP W/S=8/12 mil, <3000mil

P_ZVSS W/S=8/12 mil, <3000mil

CPU THERMAL SENSOR



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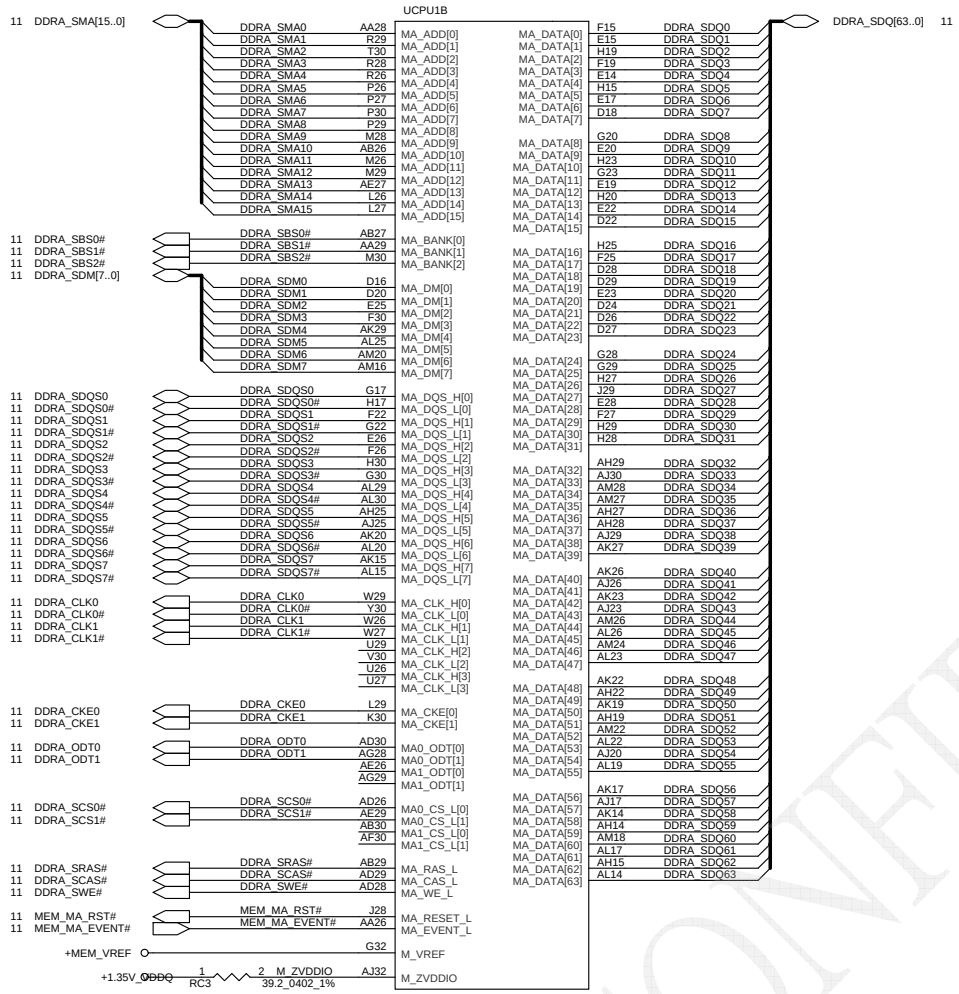
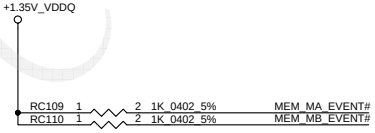
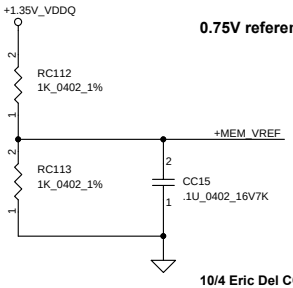


M_ZVDDIO W/S=8/12 mil, <1000mil

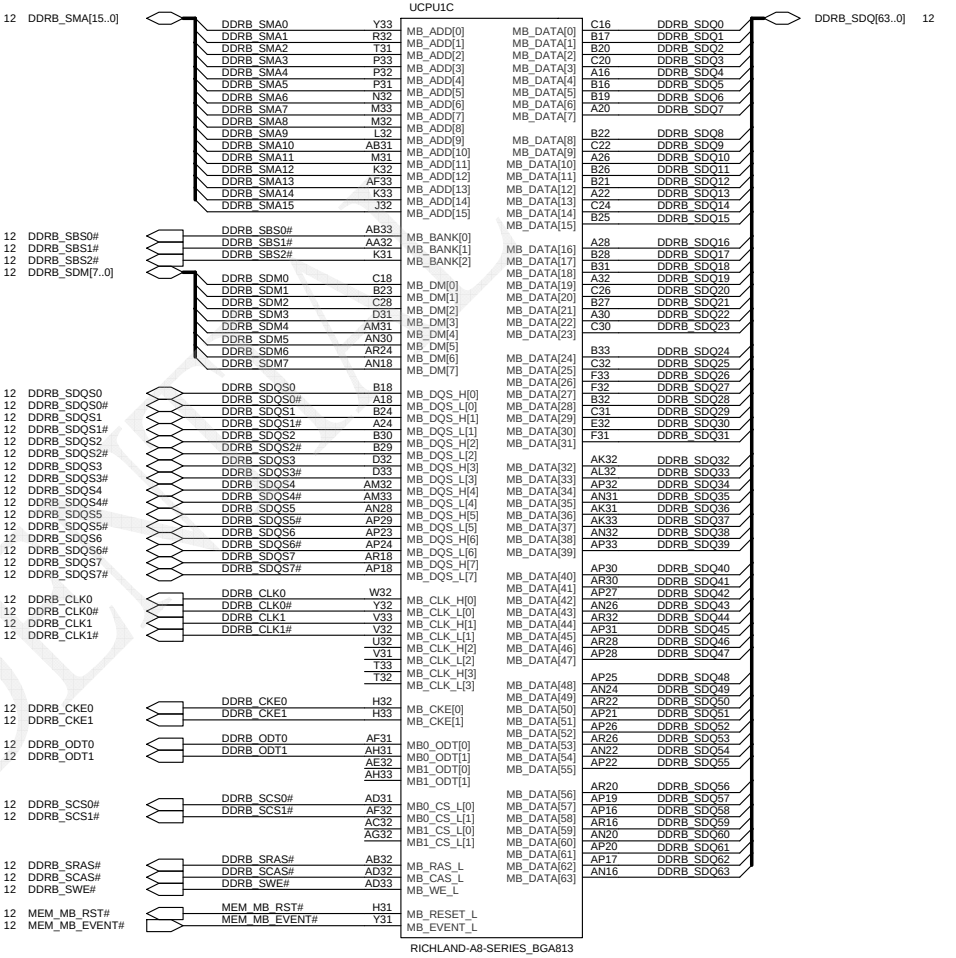


11/19 Eric change 4P2R to 8P4R.



10/4 Eric Del CC45.

+MEM_VREF 15mil
Close to JCPU1



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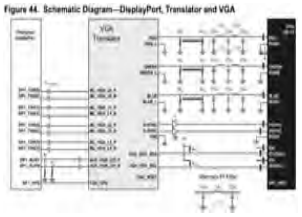

Close to APU (JCPU1)

Place near APU

To LVDS Translator

FHD eDP

UCPU1D

DISPLAY PORT 0

DISPLAY PORT 1

DISPLAY PORT 2

DISPLAY PORT MISC.

CLK

SER.

CTRL

JTAG

TEST

RSVD

SENSE

RICHLAND-A8-SERIES_BGA813

12/19 del CC141/CC142, RC10, RC11

To LVDS Translator

To HDMI

LVDS/eDP

HDMI

10/3 Eric Add DP_ENVDD control pin.

DP_AUX_ZVSS W/S=8/12 mil, <3000mil

10/27 add TP.

TEST35 change to PU for HDMI can not output 20110126

12/15 change to +1.5V

Close to Header

10/27 300 ohm??

Allow_STOP leakage issue

4/17 change to 0ohm new symbol

For ESD request close APU side

10/4 Eric Del.

10/4 Eric Del.

12/19 RF request

To HDMI

100MHz

100MHz NSS

SVI 2.0 (0 ohm at Power Side)

Check

SB-TSI (S5 Domain)

4/17 change to 0ohm new symbol

10/25 Eric aremovek H_PROCHOT# .

Internal PU when no use HDT

Route as differential with APU_VDD_RUN_FB_L

TC13 near APU.

CPU TSI interface level shift

When APU High -> MOS OFF (Vgs < 0.4V)

APU Low -> MOS ON (Vgs > 1.3V)

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

Vg = 1.607 V

Asserted as an input to force processor into HTC-active state

1/11 Eric mount RC25 for open drain needed.

2/29 remove RC42, add EC_THERM for power leakage issue

THERMTRIP shutdown temperature: 115 degree

Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately

HDT Debug conn

12/19 remove damping 0ohm.

12/15 change to +1.5V

12/27 Eric Del.

10/18 Eric change Level shift solution with Pagani AMD.

3/9 add QC5 for +5VS power leakage issue

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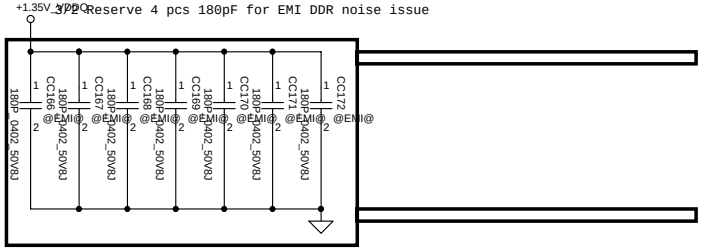
Power Name	Consumption
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	37A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.75A



On power team page

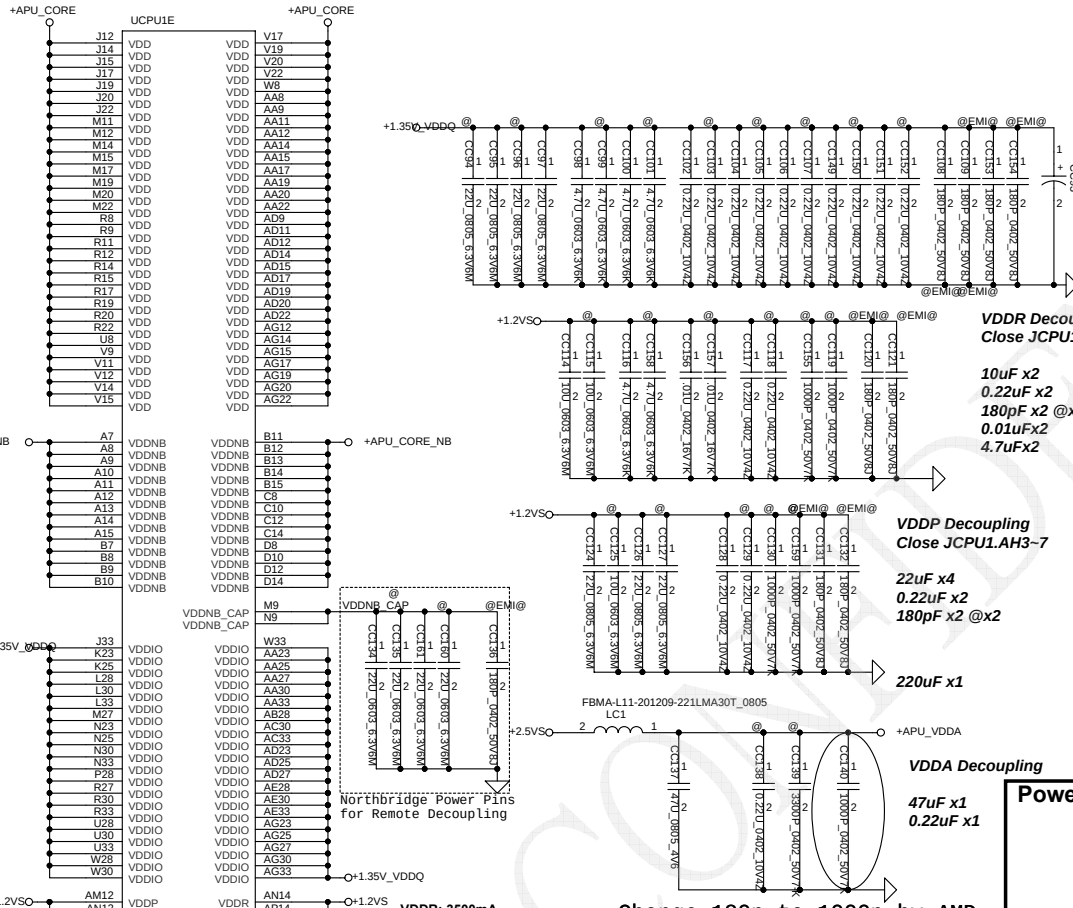
On power team page

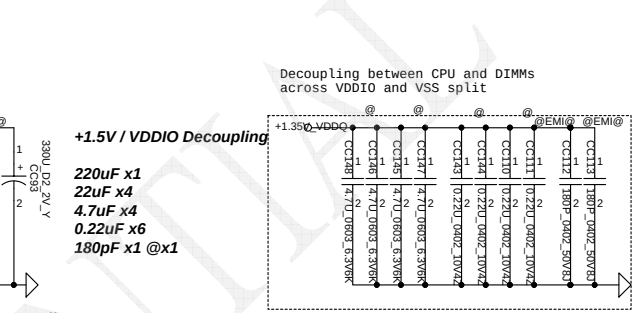
+APU_CORE Decoupling

330uF x 4 @ x1
22uF x 10
0.22uF x2
0.01uF x3
180pF x2 @ x1

+APU_CORE_NB Decoupling

330uF x2
22uF x2 @ x2
10uF x1
0.22uF x2
180pF x3





+1.5V / VDDIO Decoupling

220uF x1
22uF x4
4.7uF x4
0.22uF x6
180pF x1 @x1

VDDR Decoupling
Close JCPU1.AN14,AP14~15,AR14~15

10uF x2
0.22uF x2
180pF x2 @x2
0.01uFx2
4.7uFx2

VDDP Decoupling
Close JCPU1.AH3~7

22uF x4
0.22uF x2
180pF x2 @x2

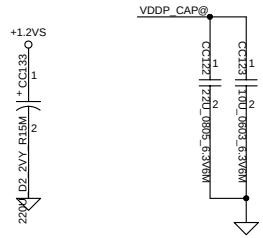
220uF x1

VDDA Decoupling

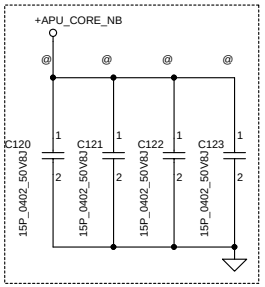
47uF x1
0.22uF x1

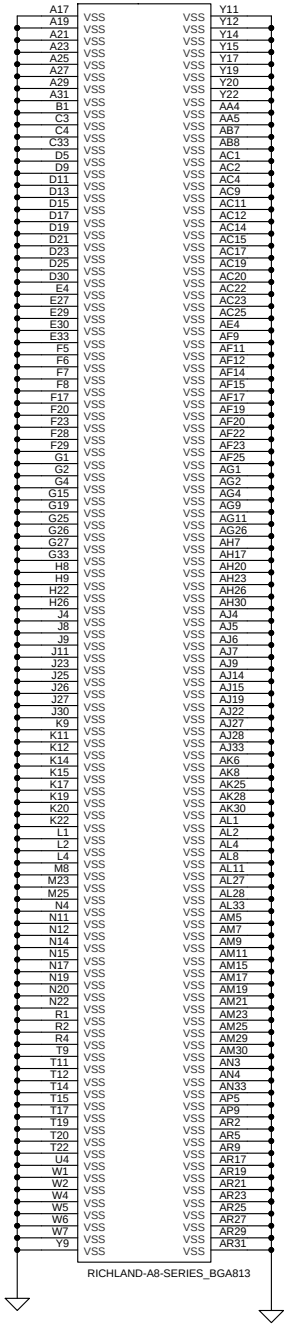
Change 180p to 1000p by AMD

Decoupling between CPU and DIMMs across VDDIO and VSS split

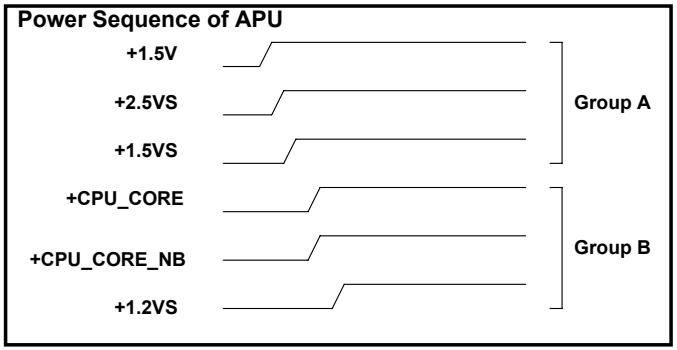


12/22 for RF request





Power Sequence of APU



Decoupling Caps.

Pop / @	330uF	220uF	47uF	22uF	10uF	4.7uF	0.22uF	0.01uF	3300pF	1nF	180pF
Pumori 2.0			0	19/11	7	5	17	3	1	1 / 1	13/3
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16

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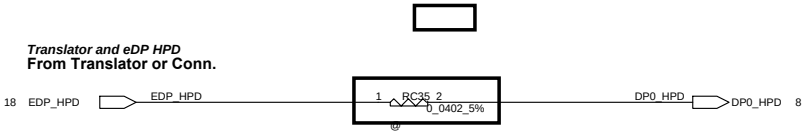
HPD

Del reserved NMOS

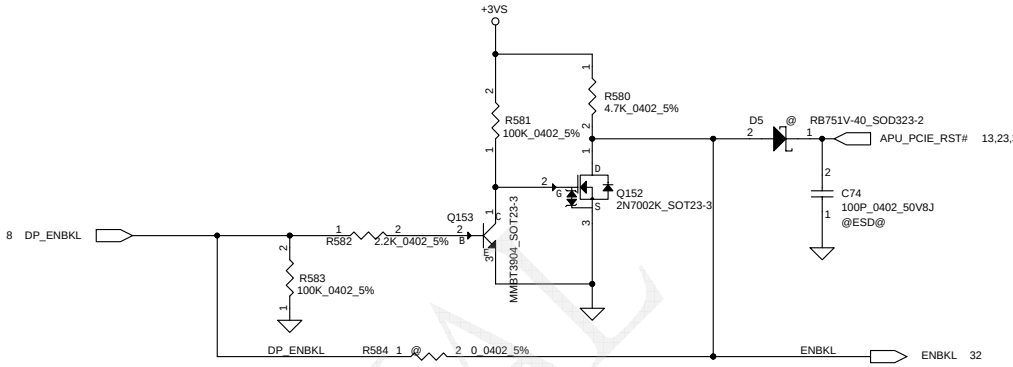


4/17 change to 0ohm new symbol

Del reserved NMOS

12/06 Del FCH_CRT_HPD

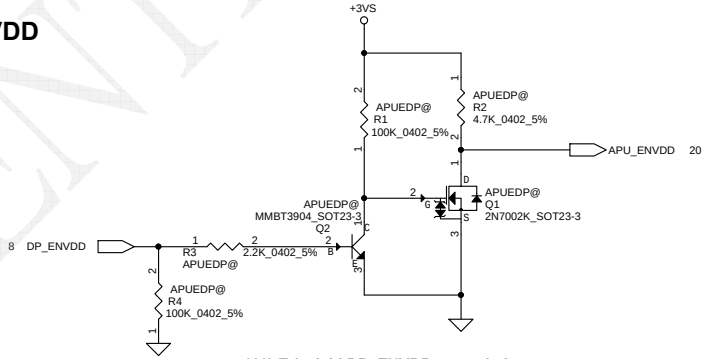
Panel ENBKL



11/13 Eric Add Panel EBBKL circuit.
Verify eDP on DB phase.

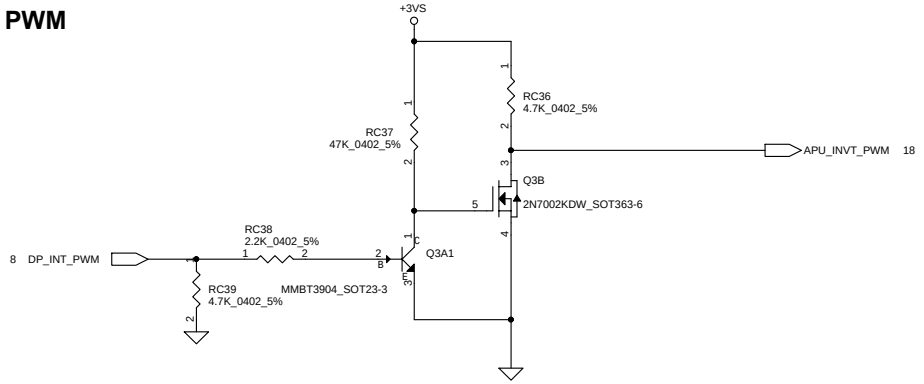
eDP Panel ENVDD

Panel ENVDD



10/3 Eric Add DP_ENVDD control pin.

Panel PWM



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All VREF traces should have 20 mil trace width

7 DDRA_SDQ[0..63] DDRA_SDQ[0..63]
7 DDRA_SDM[0..7] DDRA_SDM[0..7]
7 DDRA_SMA[0..15] DDRA_SMA[0..15]

+1.35V_VDDQ
RD10 1K_0402_1%
+V_DDR_REFA
RD11 1K_0402_1%

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

+0.675VS
CD3 1U_0402_6.3V6K
CD4 1U_0402_6.3V6K
CD5 1U_0402_6.3V6K
CD6 1U_0402_6.3V6K
CD7 10U_0603_6.3V6M
CD8 10U_0603_6.3V6M
CD9 10U_0603_6.3V6M

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.35V_VDDQ
CD12 10U_0603_6.3V6M
CD13 10U_0603_6.3V6M
CD14 10U_0603_6.3V6M
CD15 10U_0603_6.3V6M
CD16 10U_0603_6.3V6M
CD17 10U_0603_6.3V6M
CD18 0.1U_0402_16V7K
CD19 0.1U_0402_16V7K
CD20 0.1U_0402_16V7K
CD21 0.1U_0402_16V7K
@ CD22 47U 6.3V M B1 ESR70M

DDR3 SO-DIMM A

+1.35V_VDDQ
CD26 0.1U_0402_16V7K
CD27 0.1U_0402_16V7K
CD28 0.1U_0402_16V7K
CD25 0.1U_0402_16V7K

3/2 Reserve 4 pcs 180pF for EMI DDR noise issue

+1.35V_VDDQ
CD57 180P_0402_50V8J
CD58 180P_0402_50V8J
CD59 180P_0402_50V8J
CD60 180P_0402_50V8J

SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

+VREF_DQ 15mil

DDR3 SO-DIMM A

+V_DDR_REFA
CD1 0.1U_0402_16V7K
CD3 1000P_0603_50V7K
+1.35V_VDDQ
+1.35V_VDDQ
JDIMM1

		+V_DDR_REFA	1	VREF_DQ	VSS1	2	
			3	VSS2	DQ4	4	DDRA_SDQ4
		DDRA_SDQ0	5	DQ0	DQ5	6	DDRA_SDQ5
		DDRA_SDQ1	7	DQ1	VSS3	8	
			9	VSS4	DQS#0	10	DDRA_SDQS0#
		DDRA_SDM0	11	DM0	DQS0	12	DDRA_SDQS0
			13	VSS5	VSS6	14	
		DDRA_SDQ2	15	DQ2	DQ6	16	DDRA_SDQ6
		DDRA_SDQ3	17	DQ3	DQ7	18	DDRA_SDQ7
			19	VSS7	VSS8	20	
		DDRA_SDQ8	21	DQ8	DQ12	22	DDRA_SDQ12
		DDRA_SDQ9	23	DQ9	DQ13	24	DDRA_SDQ13
			25	VSS9	VSS10	26	
7	DDRA_SDQS1#	DDRA_SDQS1#	27	DQS#1	DM1	28	DDRA_SDM1
7	DDRA_SDQS1	DDRA_SDQS1	29	DQS1	RESET#	30	MEM_MA_RST#
			31	VSS11	VSS12	32	
		DDRA_SDQ10	33	DQ10	DQ14	34	DDRA_SDQ14
		DDRA_SDQ11	35	DQ11	DQ15	36	DDRA_SDQ15
			37	VSS13	VSS14	38	
		DDRA_SDQ16	39	DQ16	DQ20	40	DDRA_SDQ20
		DDRA_SDQ17	41	DQ17	DQ21	42	DDRA_SDQ21
			43	VSS15	VSS16	44	
7	DDRA_SDQS2#	DDRA_SDQS2#	45	DQS#2	DM2	46	DDRA_SDM2
7	DDRA_SDQS2	DDRA_SDQS2	47	DQS2	VSS17	48	
			49	VSS18	DQ22	50	DDRA_SDQ22
		DDRA_SDQ18	51	DQ18	DQ23	52	DDRA_SDQ23
		DDRA_SDQ19	53	DQ19	VSS19	54	
			55	VSS20	DQ28	56	DDRA_SDQ28
		DDRA_SDQ24	57	DQ24	DQ29	58	DDRA_SDQ29
		DDRA_SDQ25	59	DQ25	VSS21	60	
			61	VSS22	DQS#3	62	DDRA_SDQS3#
		DDRA_SDM3	63	DM3	DQS3	64	DDRA_SDQS3
			65	VSS23	VSS24	66	
		DDRA_SDQ26	67	DQ26	DQ30	68	DDRA_SDQ30
		DDRA_SDQ27	69	DQ27	DQ31	70	DDRA_SDQ31
			71	VSS25	VSS26	72	
7	DDRA_CKE0	DDRA_CKE0	73	CKE0	CKE1	74	DDRA_CKE1
			75	VDD1	VDD2	76	
7	DDRA_SBS2#	DDRA_SBS2#	77	NC1	A15	78	DDRA_SMA15
			79	BA2	A14	80	DDRA_SMA14
		DDRA_SMA12	81	VDD3	VDD4	82	
		DDRA_SMA9	83	A12/BC#	A11	84	DDRA_SMA11
			85	A9	A7	86	DDRA_SMA7
		DDRA_SMA8	87	VDD5	VDD6	88	
		DDRA_SMA5	89	A8	A6	90	DDRA_SMA6
			91	A5	A4	92	DDRA_SMA4
		DDRA_SMA3	93	VDD7	VDD8	94	
		DDRA_SMA1	95	A3	A2	96	DDRA_SMA2
			97	A1	A0	98	DDRA_SMA0
7	DDRA_CLK0	DDRA_CLK0	99	VDD9	VDD10	100	
7	DDRA_CLK0#	DDRA_CLK0#	101	CK0	CK1	102	DDRA_CLK1
			103	CK0#	CK1#	104	DDRA_CLK1#
		DDRA_SMA10	105	VDD11	VDD12	106	
		DDRA_SBS0#	107	A10/AP	BA1	108	DDRA_SBS1#
7	DDRA_SBS0#		109	BA0	RAS#	110	DDRA_SRAS#
		DDRA_SWE#	111	VDD13	VDD14	112	
7	DDRA_SWE#	DDRA_SCAS#	113	WE#	S0#	114	DDRA_SCS0#
7	DDRA_SCAS#		115	CAS#	ODT0	116	DDRA_ODT0
		DDRA_SMA13	117	VDD15	VDD16	118	
		DDRA_SCS1#	119	A13	ODT1	120	DDRA_ODT1
7	DDRA_SCS1#		121	S1#	NC2	122	
			123	VDD17	VDD18	124	
			125	NCTEST	VREF_CA	126	
		DDRA_SDQ32	127	VSS27	VSS28	128	
		DDRA_SDQ33	129	DQ32	DQ36	130	DDRA_SDQ36
			131	DQ33	DQ37	132	DDRA_SDQ37
		DDRA_SDQS4#	133	VSS29	VSS30	134	
7	DDRA_SDQS4#	DDRA_SDQS4	135	DQS#4	DM4	136	DDRA_SDM4
7	DDRA_SDQS4		137	DQS4	VSS31	138	
		DDRA_SDQ34	139	VSS32	DQ38	140	DDRA_SDQ38
		DDRA_SDQ35	141	DQ34	DQ39	142	DDRA_SDQ39
			143	VSS33	VSS34	144	
		DDRA_SDQ40	145	DQ35	DQ44	146	DDRA_SDQ44
		DDRA_SDQ41	147	VSS34	DQ45	148	DDRA_SDQ45
			149	DQ40	VSS35	150	
		DDRA_SDM5	151	DQ41	DQS#5	152	DDRA_SDQS5#
			153	VSS36	DQS5	154	DDRA_SDQS5
		DDRA_SDQ42	155	DM5	VSS38	156	
		DDRA_SDQ43	157	VSS37	DQ46	158	DDRA_SDQ46
			159	DQ42	DQ47	160	DDRA_SDQ47
		DDRA_SDQ48	161	DQ43	VSS40	162	
		DDRA_SDQ49	163	VSS39	DQ52	164	DDRA_SDQ52
			165	DQ48	DQ53	166	DDRA_SDQ53
		DDRA_SDQS6#	167	DQ49	VSS42	168	
7	DDRA_SDQS6#	DDRA_SDQS6	169	VSS41	DM6	170	DDRA_SDM6
7	DDRA_SDQS6		171	DQS#6	VSS43	172	
		DDRA_SDQ50	173	DQ56	DQ54	174	DDRA_SDQ54
		DDRA_SDQ51	175	VSS44	DQ55	176	DDRA_SDQ55
			177	DQ50	VSS45	178	
		DDRA_SDQ56	179	DQ51	DQ60	180	DDRA_SDQ60
		DDRA_SDQ57	181	VSS46	DQ61	182	DDRA_SDQ61
			183	DQ56	VSS47	184	
		DDRA_SDM7	185	DQ57	DQS#7	186	DDRA_SDQS7#
			187	VSS48	DQS7	188	DDRA_SDQS7
		DDRA_SDQ58	189	DM7	VSS50	190	
		DDRA_SDQ59	191	VSS49	DQ62	192	DDRA_SDQ62
			193	DQ58	DQ63	194	DDRA_SDQ63
			195	DQ59	VSS51	196	
		RD51 2_10K_0402_5%	197	SA0	EVENT#	198	MEM_MA_EVENT#
			199	VDDSPD	SDA	200	FCH_SDATA0 12,15
			201	SA1	SCL	202	FCH_SCLK0 12,15
			203	VTT1	VTT2	204	+0.675VS
			205	G1	G2	206	

LCN_DAN06-K4406-0102
CONN@

+3VS
CD23 2.2U_0603_6.3V6K
CD24 0.1U_0402_16V7K
RD6 0_0402_5%

+VREF_CB 15mil
+1.35V_VDDQ
RD12 1K_0402_1%
RD13 1K_0402_1%
+VREF_CA
CD10 0.1U_0402_16V7K
CD11 1000P_0603_50V7K

DDRA_CKE1 7
DDRA_SBS1# 7
DDRA_SRAS# 7
DDRA_SCS0# 7
DDRA_ODT0 7
DDRA_ODT1 7
DDRA_SDQS0# 7
DDRA_SDQS0 7
DDRA_SDQS3# 7
DDRA_SDQS3 7
DDRA_SDQS5# 7
DDRA_SDQS5 7
DDRA_SDQS7# 7
DDRA_SDQS7 7
MEM_MA_RST# 7
MEM_MA_EVENT# 7

DIMM_A REV H:4mm

<Address: 00>

Security Classification	Compal Secret Data		
Issued Date	2012/11/07	Deciphered Date	2012/11/07

Title	SCHEMATIC, MB A9851		
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DDR3 SO-DIMM B

All VREF traces should have 20 mil trace width

7 DDRB_SDQ[0..63] — DDRB_SDQ[0..63]
7 DDRB_SDM[0..7] — DDRB_SDM[0..7]
7 DDRB_SMA[0..15] — DDRB_SMA[0..15]

10/03 change to +V_DDR_REFB

+1.35V_VDDQ
RD14 1K_0402_1%
+V_DDR_REFB
RD15 1K_0402_1%

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

+0.675VS
CD34 1U_0402_6.3V6K
CD35 1U_0402_6.3V6K
CD54 1U_0402_6.3V6K
CD36 1U_0402_6.3V6K
CD53 10U_0603_6.3V6M
CD52 10U_0603_6.3V6M
CD39 10U_0603_6.3V6M

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.35V_VDDQ
CD37 10U_0603_6.3V6M
CD49 10U_0603_6.3V6M
CD45 10U_0603_6.3V6M
CD40 10U_0603_6.3V6M
CD42 10U_0603_6.3V6M
CD50 10U_0603_6.3V6M
CD44 0.1U_0402_16V7K
CD43 0.1U_0402_16V7K
CD47 0.1U_0402_16V7K
CD59 0.1U_0402_16V7K
CD36 47U 6.3V M B1 ESR70M

DDR3 SO-DIMM B

+1.35V_VDDQ
CD33 0.1U_0402_16V7K
CD34 0.1U_0402_16V7K
CD35 0.1U_0402_16V7K
CD32 0.1U_0402_16V7K

SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

+1.35V_VDDQ
CD61 180P_0402_50V8J
CD62 180P_0402_50V8J
CD63 180P_0402_50V8J
CD64 180P_0402_50V8J

3/2 Reserve 4 pcs 180pF for EMI DDR noise issue

10/05 change to PH.

+VREF_DQ 15mil
+V_DDR_REFB
CD50 0.1U_0402_16V7K
CD29 1000P_0603_50V7K
+1.35V_VDDQ

JDIMM2

VREF_DQ	1	2	VSS1
VSS2	3	4	DQ4
DQ0	5	6	DQ5
DQ1	7	8	VSS3
VSS4	9	10	DQS#0
DM0	11	12	DQS0
VSS5	13	14	VSS6
DQ2	15	16	DQ6
DQ3	17	18	DQ7
VSS7	19	20	VSS8
DQ8	21	22	DQ12
DQ9	23	24	DQ13
VSS9	25	26	VSS10
DQS#1	27	28	DM1
DQS1	29	30	RESET#
VSS11	31	32	VSS12
DQ10	33	34	DQ14
DQ11	35	36	DQ15
VSS13	37	38	VSS14
DQ16	39	40	DQ20
DQ17	41	42	DQ21
VSS15	43	44	VSS16
DQS#2	45	46	DM2
DQS2	47	48	VSS17
VSS18	49	50	DQ22
DQ18	51	52	DQ23
DQ19	53	54	VSS19
VSS20	55	56	DQ28
DQ24	57	58	DQ29
DQ25	59	60	VSS21
VSS22	61	62	DQS#3
DM3	63	64	DQS3
VSS23	65	66	VSS24
DQ26	67	68	DQ30
DQ27	69	70	DQ31
VSS25	71	72	VSS26
CKE0	73	74	CKE1
VDD1	75	76	VDD2
NC1	77	78	A15
BA2	79	80	A14
VDD3	81	82	VDD4
A12/BC#	83	84	A11
A9	85	86	A7
VDD5	87	88	VDD6
A8	89	90	A6
A5	91	92	A4
VDD7	93	94	VDD8
A3	95	96	A2
A1	97	98	A0
VDD9	99	100	VDD10
CK0	101	102	CK1
CK0#	103	104	CK1#
VDD11	105	106	VDD12
A10/AP	107	108	BA1
BA0	109	110	RAS#
VDD13	111	112	VDD14
WE#	113	114	S0#
CAS#	115	116	ODT0
VDD15	117	118	VDD16
A13	119	120	ODT1
S1#	121	122	NC2
VDD17	123	124	VDD18
NCTEST	125	126	VREF_CA
VSS27	127	128	VSS28
DQ32	129	130	DQ36
DQ33	131	132	DQ37
VSS29	133	134	VSS30
DQS#4	135	136	DM4
DQS4	137	138	VSS31
VSS32	139	140	DQ38
DQ34	141	142	DQ39
DQ35	143	144	VSS33
VSS34	145	146	DQ44
DQ40	147	148	DQ45
DQ41	149	150	VSS35
VSS36	151	152	DQS#5
DM5	153	154	DQS5
VSS37	155	156	VSS38
DQ42	157	158	DQ46
DQ43	159	160	DQ47
VSS39	161	162	VSS40
DQ48	163	164	DQ52
DQ49	165	166	DQ53
VSS41	167	168	VSS42
DQS#6	169	170	DM6
DQS6	171	172	VSS43
VSS44	173	174	DQ54
DQ50	175	176	DQ55
DQ51	177	178	VSS45
VSS46	179	180	DQ60
DQ56	181	182	DQ61
DQ57	183	184	VSS47
VSS48	185	186	DQS#7
DM7	187	188	DQS7
VSS49	189	190	VSS50
DQ58	191	192	DQ62
DQ59	193	194	DQ63
VSS51	195	196	VSS52
SA0	197	198	EVENT#
VDDSPD	199	200	SDA
SA1	201	202	SCL
VTT1	203	204	VTT2
G1	205	206	G2

LCN_DAN06-K4406-0102
CONN@

DDRB_SDQ0 DDRB_SDQ1 DDRB_SDM0 DDRB_SDQ2 DDRB_SDQ3 DDRB_SDQ8 DDRB_SDQ9 DDRB_SDQS1# DDRB_SDQS1 DDRB_SDQ10 DDRB_SDQ11 DDRB_SDQ16 DDRB_SDQ17 DDRB_SDQS2# DDRB_SDQS2 DDRB_SDQ18 DDRB_SDQ19 DDRB_SDQ24 DDRB_SDQ25 DDRB_SDM3 DDRB_SDQ26 DDRB_SDQ27 DDRB_SDQ32 DDRB_SDQ33 DDRB_SDQS4# DDRB_SDQS4 DDRB_SDQ34 DDRB_SDQ35 DDRB_SDQ40 DDRB_SDQ41 DDRB_SDM5 DDRB_SDQ42 DDRB_SDQ43 DDRB_SDQ48 DDRB_SDQ49 DDRB_SDQS6# DDRB_SDQS6 DDRB_SDQ50 DDRB_SDQ51 DDRB_SDQ56 DDRB_SDQ57 DDRB_SDM7 DDRB_SDQ58 DDRB_SDQ59

DDRB_SDQ4 DDRB_SDQ5 DDRB_SDQS0# DDRB_SDQS0 DDRB_SDQ6 DDRB_SDQ7 DDRB_SDQ12 DDRB_SDQ13 DDRB_SDM1 MEM_MB_RST# DDRB_SDQ14 DDRB_SDQ15 DDRB_SDQ20 DDRB_SDQ21 DDRB_SDM2 DDRB_SDQ22 DDRB_SDQ23 DDRB_SDQ28 DDRB_SDQ29 DDRB_SDQS3# DDRB_SDQS3 DDRB_SDQ30 DDRB_SDQ31 DDRB_CKE1 DDRB_SMA15 DDRB_SMA14 DDRB_SMA11 DDRB_SMA7 DDRB_SMA6 DDRB_SMA4 DDRB_SMA2 DDRB_SMA0 DDRB_CLK1 DDRB_CLK1# DDRB_SBS1# DDRB_SRAS# DDRB_SCS0# DDRB_ODT0 DDRB_ODT1 DDRB_SDQ36 DDRB_SDQ37 DDRB_SDM4 DDRB_SDQ38 DDRB_SDQ39 DDRB_SDQ44 DDRB_SDQ45 DDRB_SDQS5# DDRB_SDQS5 DDRB_SDQ46 DDRB_SDQ47 DDRB_SDQ52 DDRB_SDQ53 DDRB_SDM6 DDRB_SDQ54 DDRB_SDQ55 DDRB_SDQ60 DDRB_SDQ61 DDRB_SDQS7# DDRB_SDQS7 DDRB_SDQ62 DDRB_SDQ63 MEM_MB_EVENT# FCH_SDATA0 11,15 FCH_SCLK0 11,15 +0.675VS

7 DDRB_CKE0 — DDRB_CKE1 — DDRB_CKE1 7
7 DDRB_SBS2#
7 DDRB_CLK0 — DDRB_CLK1 7
7 DDRB_CLK0# — DDRB_CLK1# 7
7 DDRB_SBS0# — DDRB_SBS1# 7
7 DDRB_SWE# — DDRB_SCS0# 7
7 DDRB_SCAS# — DDRB_ODT0 7
7 DDRB_SCS1# — DDRB_ODT1 7
7 DDRB_SDQS4# — DDRB_SDQS4 7
7 DDRB_SDQS6# — DDRB_SDQS6 7
7 DDRB_SDQS0# — DDRB_SDQS0 7
7 DDRB_SDQS1# — DDRB_SDQS1 7
7 DDRB_SDQS2# — DDRB_SDQS2 7
7 DDRB_SDQS3# — DDRB_SDQS3 7
7 DDRB_SDQS5# — DDRB_SDQS5 7
7 DDRB_SDQS7# — DDRB_SDQS7 7
MEM_MB_RST# 7
MEM_MB_EVENT# 7
FCH_SDATA0 11,15
FCH_SCLK0 11,15

+3VS
RD71 2_10K_0402_5%
@ RD9 0_0402_5%
CD31 2.2U_0603_6.3V6K
CD38 0.1U_0402_16V7K

+VREF_CB 15mil
+1.35V_VDDQ
RD16 1K_0402_1%
+VREF_CB
RD17 1K_0402_1%
CD55 0.1U_0402_16V7K
CD30 1000P_0603_50V7K

01/15 update DDR address 10 to 01 for common design

DIMM_B REV H:8mm
Standard
<Address: 01>

Security Classification	Compal Secret Data		
Issued Date	2012/11/07	Deciphered Date	2012/11/07

Compal Electronics, Inc.

Title: SCHEMATIC, MB A9851

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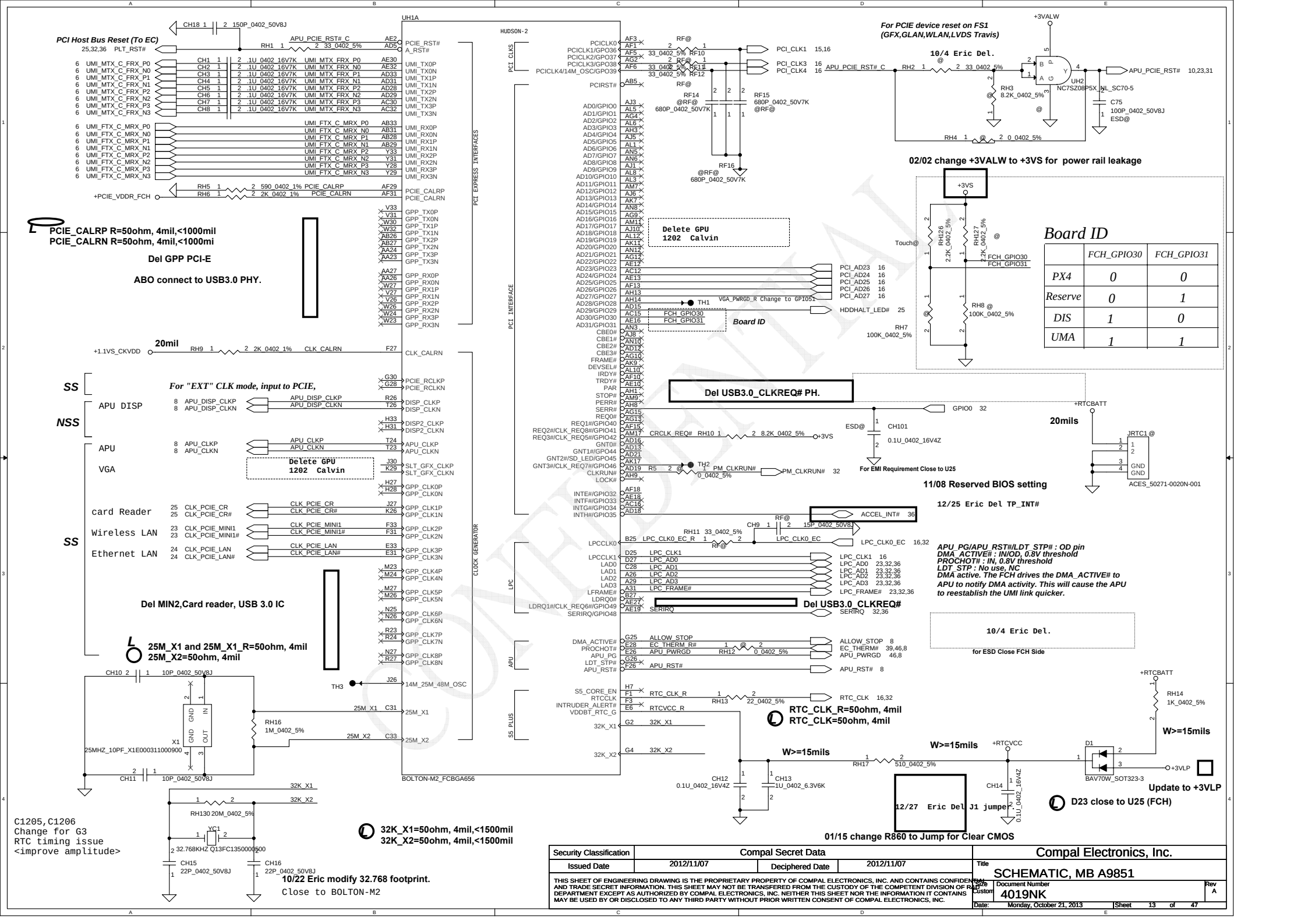

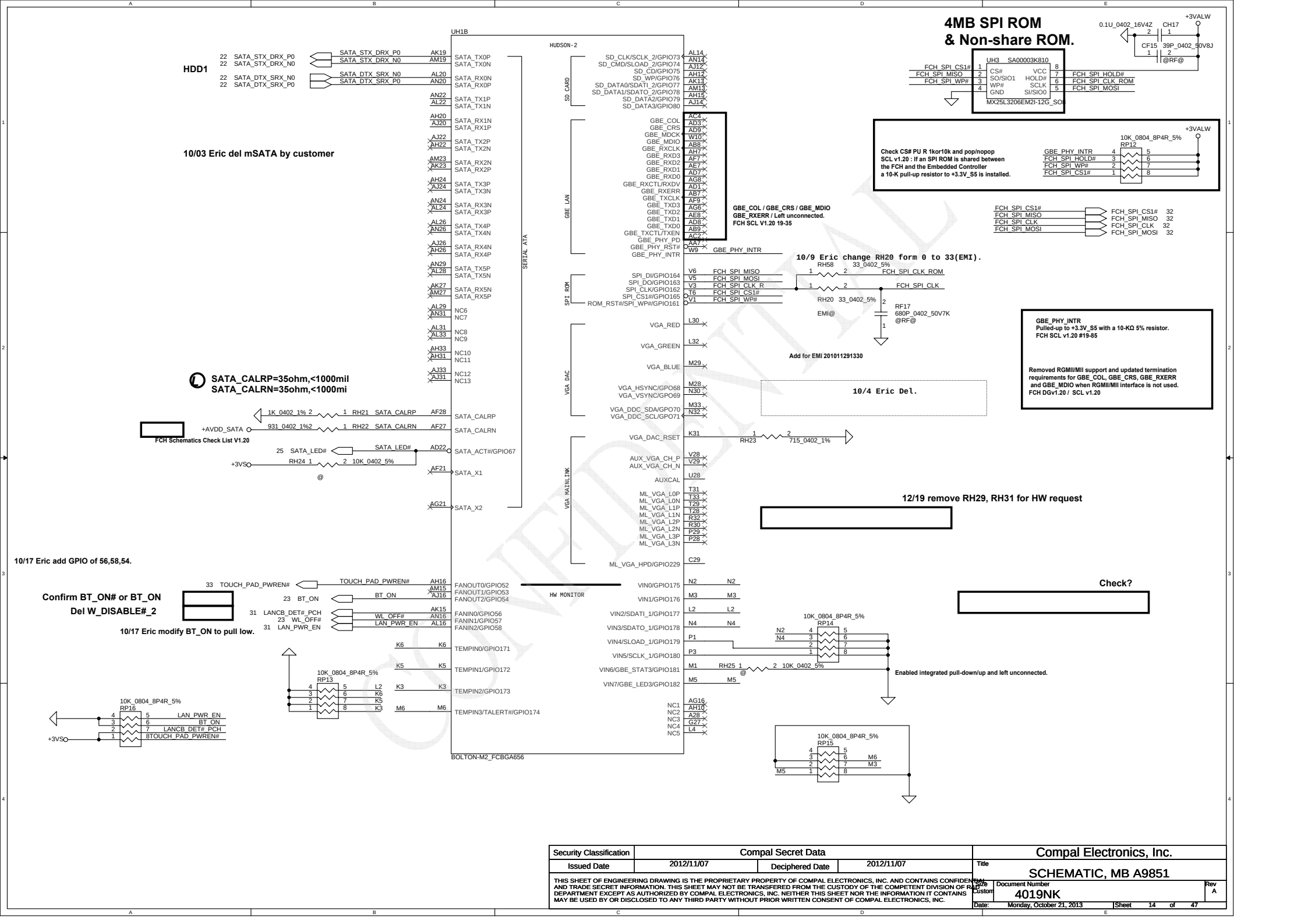

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/11/07	Deciphered Date 2012/11/07	Title: SCHEMATIC, MB A9851
Size: Custom	Document Number: 4019NK		Rev: A
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FCH_PCIE_RST# IS FOR PCIE DEVICES ON Hudson-M2/M3

02/22 Add SUS_STAT#

Check with BIOS

THERMTRIP:
Need level shift from +3VALW to +1.5V
Note: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.

SM bus 0-->S0 PWR domain
SM bus 1-->S5 PWR domain

FCH GEVENT (S5 domain) with isolation circuit to avoid leakage

H_THERMTRIP#
C72 100P_0402_50V8J ESD@

Del ODD_DA#

RH27 10K_0402_5% @ 1CARD_DET_FCH +3VALW

Confirm CR det or not.

+3VS RH57 10K_0402_5% WWAN_OFF# +3VALW

100K_0804_8P4R_5% RP18 USB_OC1# 8USB_OC0#

For FCH internal debug use

RH32 2.2K_0402_5% TEST0
RH33 2.2K_0402_5% TEST1
RH34 2.2K_0402_5% TEST2

+3VS +3VALW RH128 2.2K_0402_5% LAN_CLKREQ# MINI1_CLKREQ#

+3VS RH129 2.2K_0402_5% LAN_CLKREQ#

Del MINI2_CLKREQ# PH.

RH35 @ 8.2K_0402_5% EC_RSMRST#
RH36 @ 2.2K_0402_5% HDA_BITCLK
RH37 @ 10K_0402_5% HDA_SDIN0
RH38 @ 10K_0402_5% HDA_SDIN1
RH39 @ 10K_0402_5% HDA_SDIN2
RH40 @ 10K_0402_5% HDA_SDIN3
RH41 @ 10K_0402_5%

10/4 Eric Del.

UH1D

HUDSON-2

PCIE_RST2#/PCI_PME#/GEVENT4#
R#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
LPC_PD#/GEVENTS#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
RSMRST#
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_ISS#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#/VGA_PD
GBE_LED0/GPIO183
SPI_HOLD#/GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
PS2_CS2#/GBE_STAT2/GPIO166
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226

BOLTON-M2_FCBGA656

ACPI / WAKE UP EVENTS
GPIO
USB OC
HD AUDIO
USB 2.0
USB 1.1
USB MISC
USB 3.0
EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USBSS_CALRP
USBSS_CALRN
USB_SS_TX3P
USB_SS_TX3N
USB_SS_RX3P
USB_SS_RX3N
USB_SS_TX2P
USB_SS_TX2N
USB_SS_RX2P
USB_SS_RX2N
USB_SS_TX1P
USB_SS_TX1N
USB_SS_RX1P
USB_SS_RX1N
USB_SS_TX0P
USB_SS_TX0N
USB_SS_RX0P
USB_SS_RX0N
SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208

Hudson-M2/M3 OHCI CTL DEV 20, Fn 5 <Disable CTL>

Hudson-M2 EHCI CTL DEV 22, Fn 2 <Disable CTL of M2>
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0

USB 2.0 port(Left-2)
USB 2.0 port(Left-1)/ Charger
Del USB port 9
Hudson-M2/M3 EHCI CTL DEV 19, Fn 2
Mini1-WLAN
Del USB port 7
01/30 Eric del WWAM for USB 6.
Camera
Touch
Hudson-M2/M3 EHCI CTL DEV 18, Fn 2 <Support Wakeup>
USB 2.0 / To IO Board. 10/29 change from 2 to 1.
USBSS_CALRP=35ohm,<1000mil
USBSS_CALRN=35ohm,<1000mi
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0
USB 3.0 port(Left-2)
USB 3.0 port(Left-1)
For PCIE device reset on FS1 (GFX,GLAN,WLAN,LVDS Travis)

PC_BEEP use.

10/18 Eric Add SATA_ODD/PCH_AUDIO control pin.

Del SIMB output

33ohm termination resistor at CODEC side

Change GPIO fellow Pumori

Del FCH_GPIO187

10/5 Eric modify for EMI requirement

12/20 Del DDR3L_EN

RH65 close to PCH

Del FCH_GPIO187 R57 R55

11/20 Eric add test point from TH8 ~ TH26.

12/06 Del VGA_PWRGD

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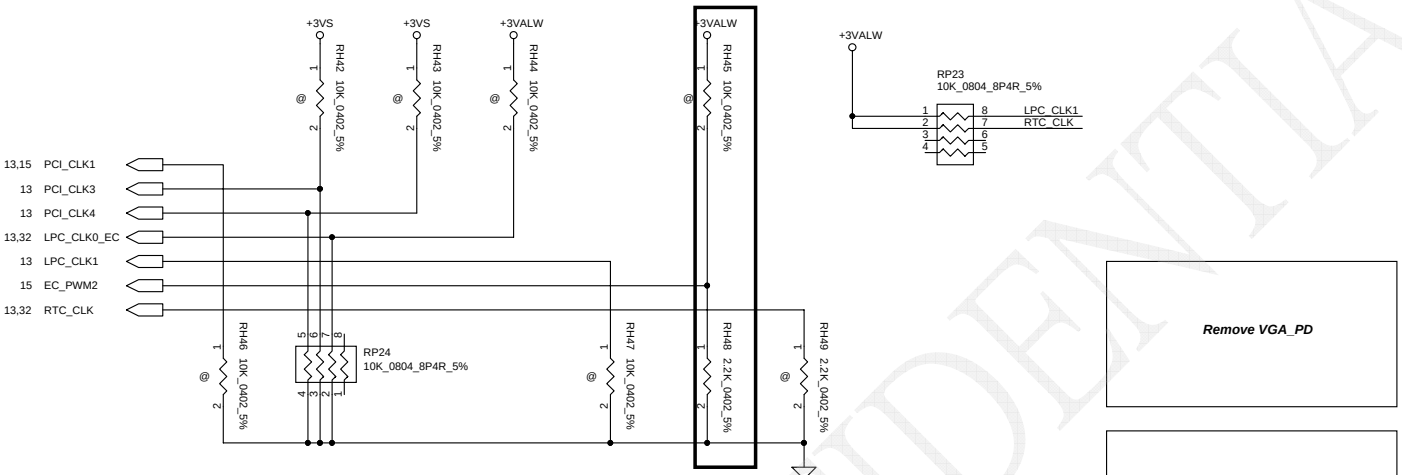
STRAP PINS

Change to SPI

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



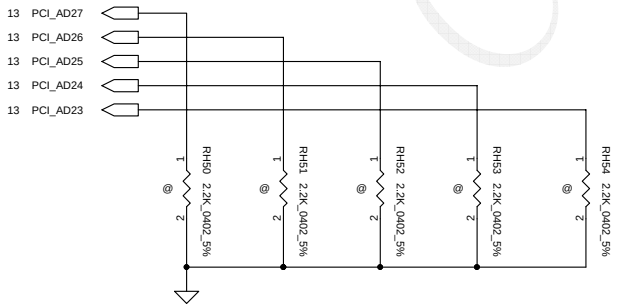
Remove VGA_PD

Remove VGA_PD

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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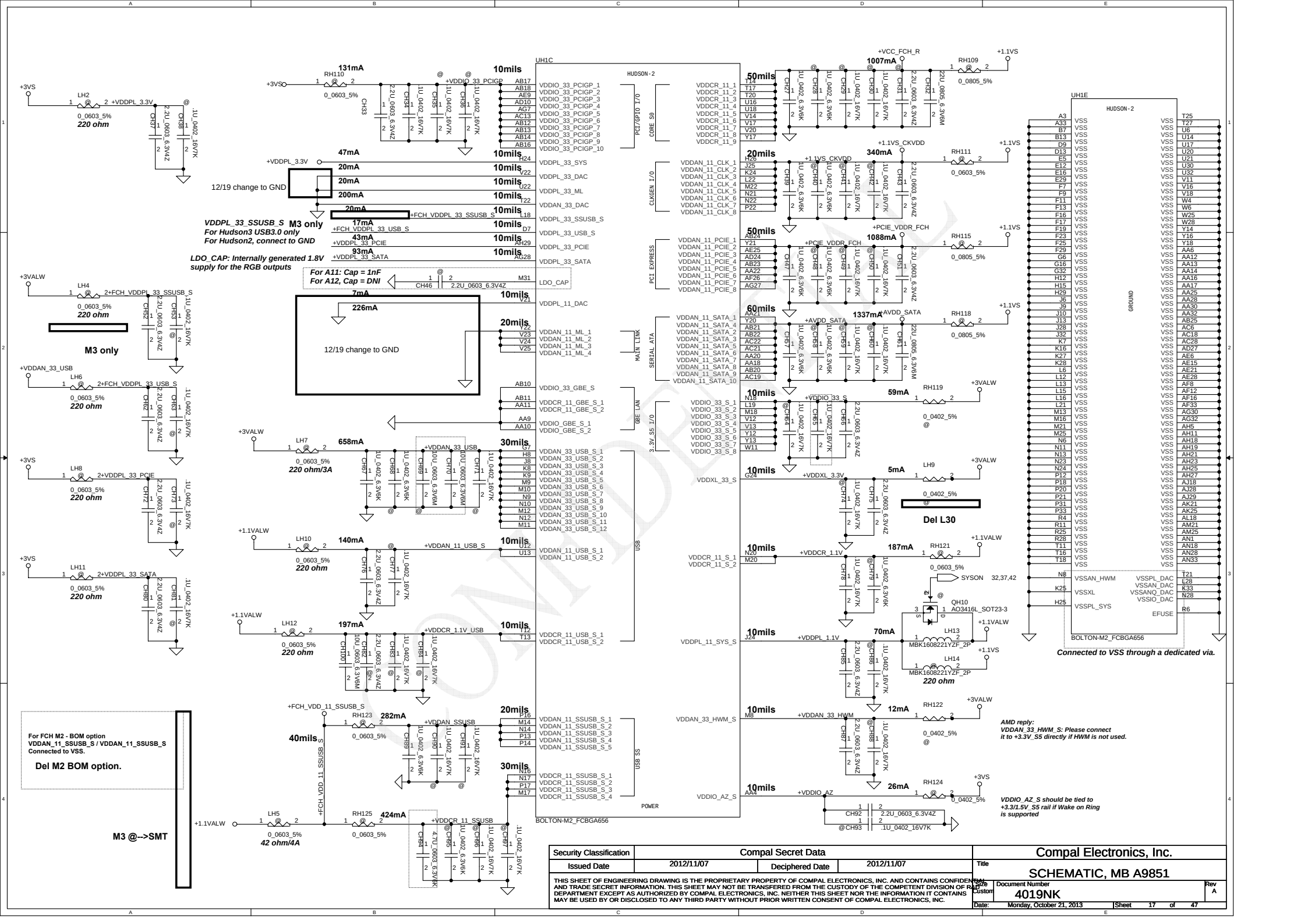

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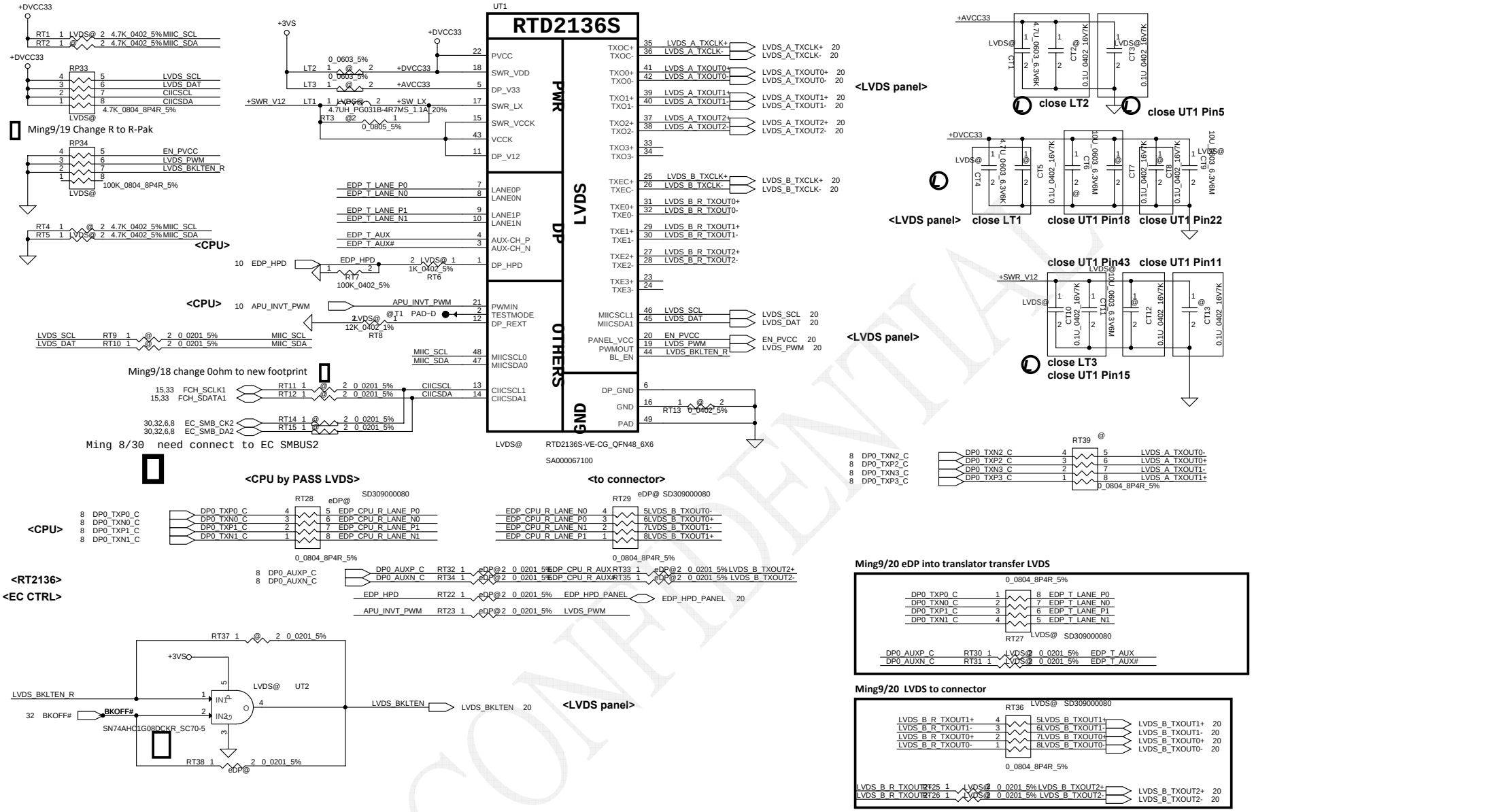

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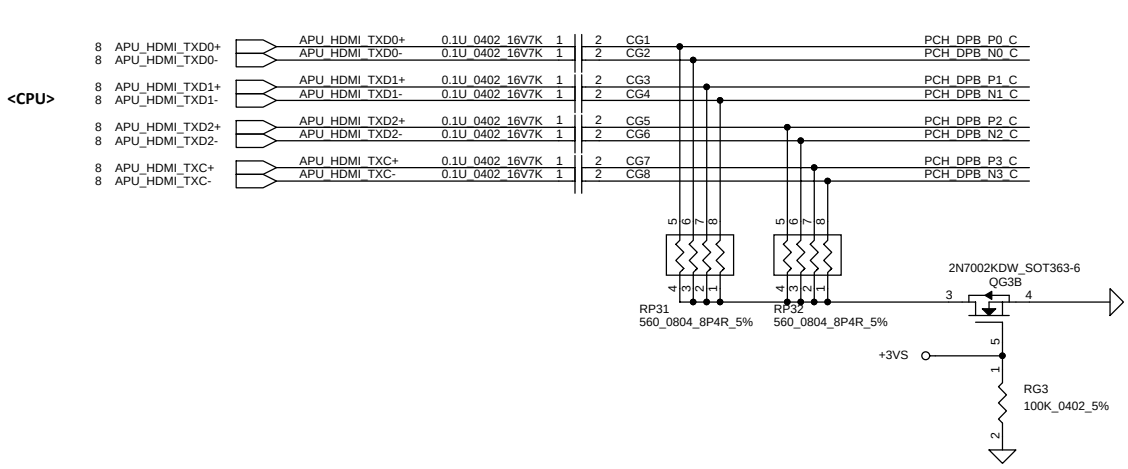
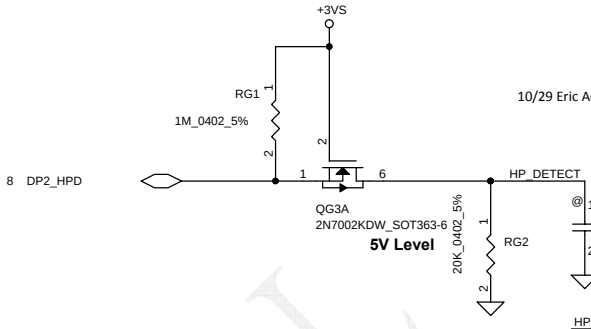
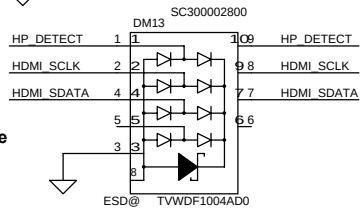
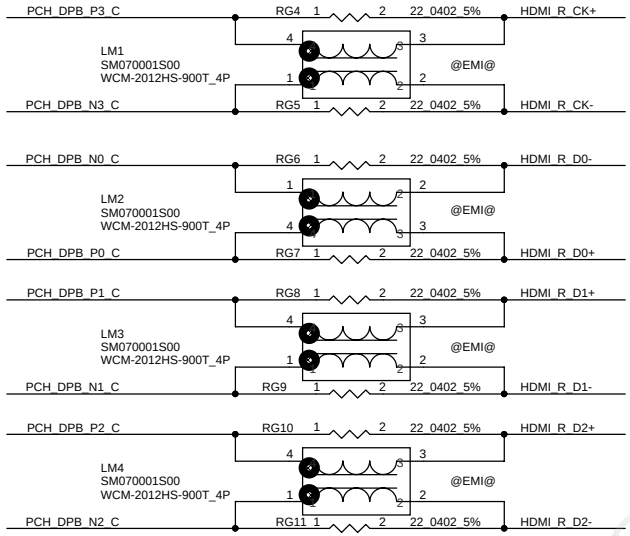


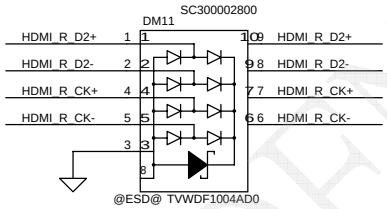


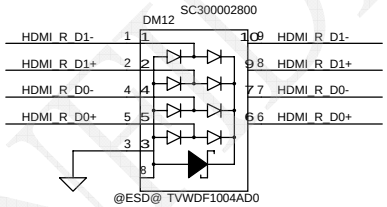
10/29 Eric Add ESD solution on HDMI_HPT

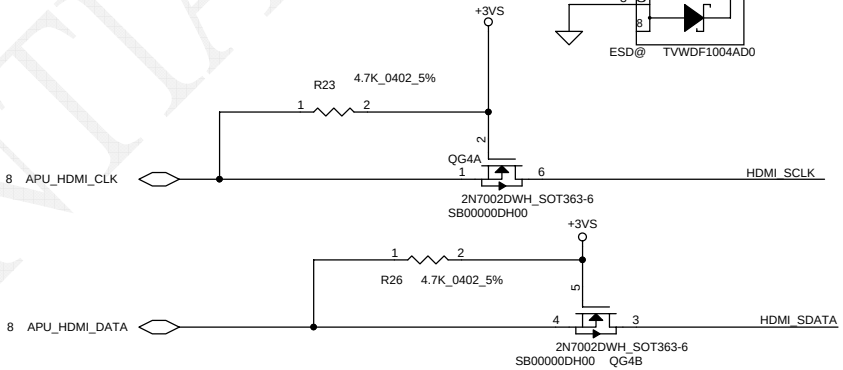


9/11 remove RG58/RG62 for doublle PU to CPU side

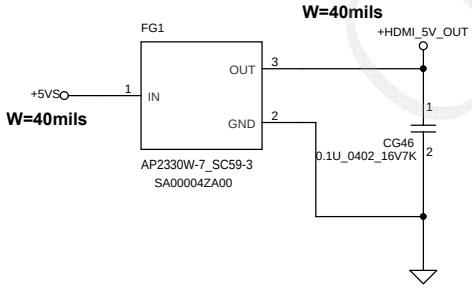






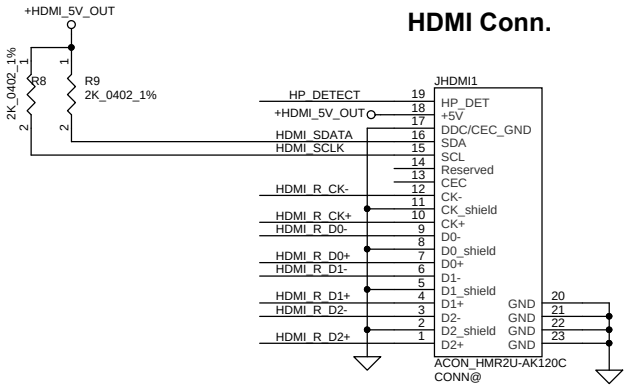


5V PULL UP IN CONNECTER SIDE



10/9 Eric Remvoe CM2 ~ CM9 for EMI requirement.

HDMI Conn.



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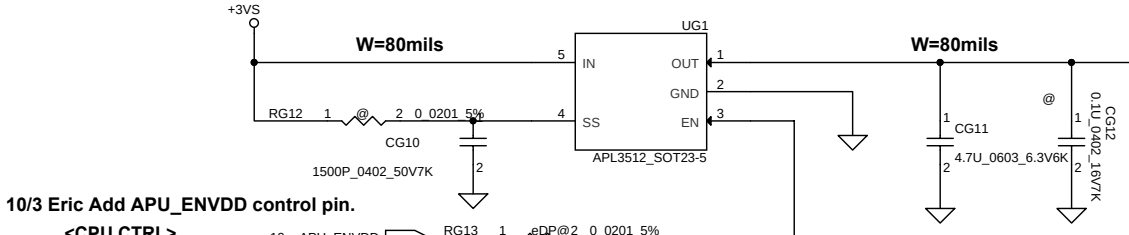
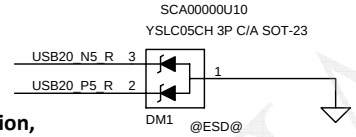


W=60mils W=60mils

10/20 Del LG1.

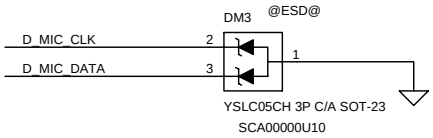
10/4 Eric Del.

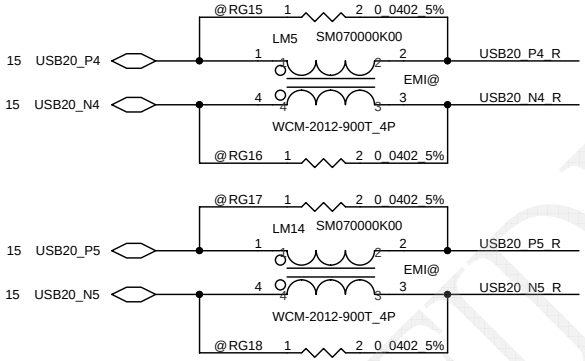
SM010014520 3000ma
220ohm@100mhz
DCR 0.04

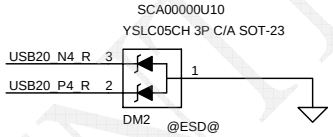


9/26 Eric remove common chock for touch screen portion, ask key part to add in touch IC side.

Put CF11 near webcam connector.







<LVDS>

<DB>eDP-->Dual LVDS

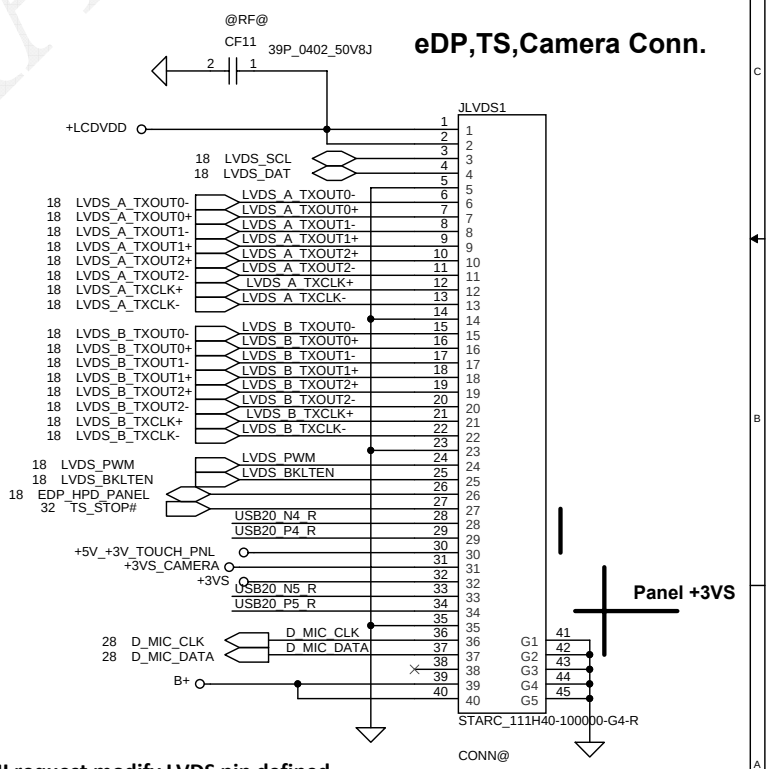
8/30 colay eDP use

<USB Touch panel>

<Touch panel>

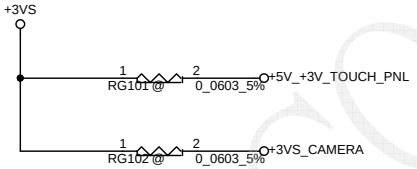
<Camara and DMIC>

<Camera>



9/6 by EMI request modify LVDS pin defined

10/3 Eric Del power switch of +3VS_CAMERA & +5V_+3V_TOUCH_PNL.



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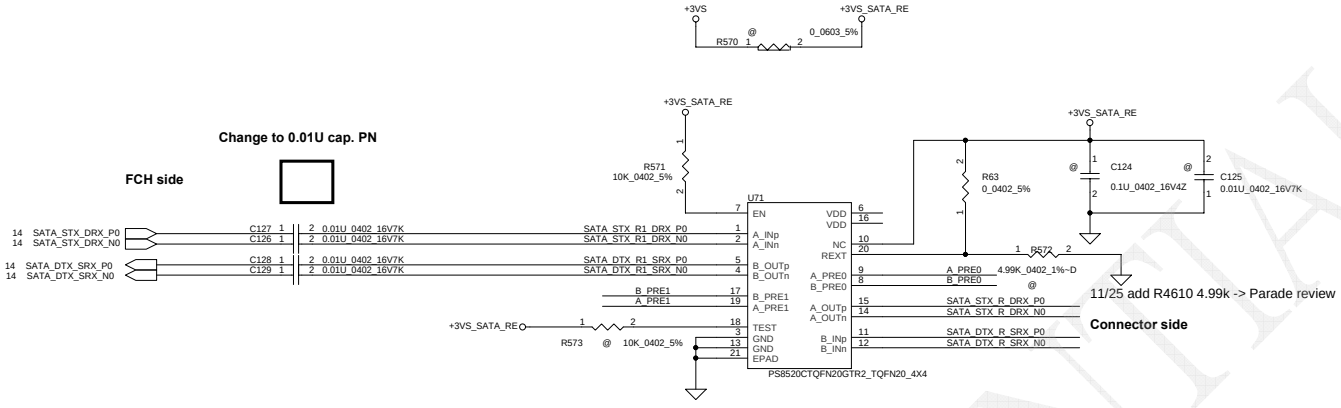
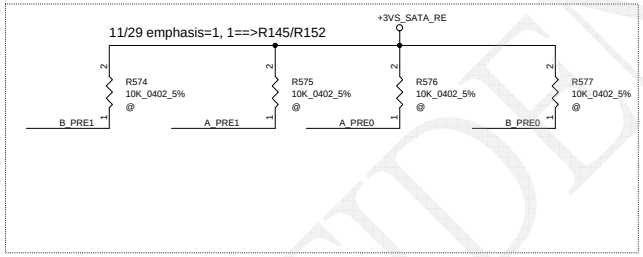
mSATA Conn.

10/03 Eric Del mSATA by customer

Reserve SATA Redriver

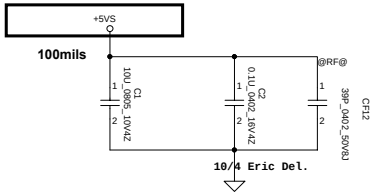




Need Vendor check value

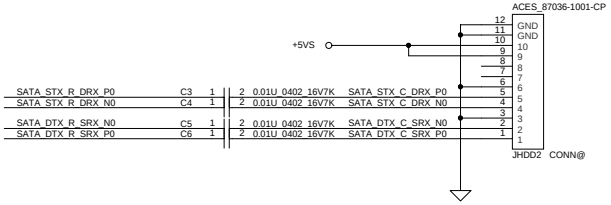
SATA0 (HDD)

02/22 Eric remvoe SATA power 0 ohm to +5VS.



02/22 Eric remvoe SATA 0 ohm co-lay.

<DB>Change to 10 Pin **2.5" HDD Conn.**



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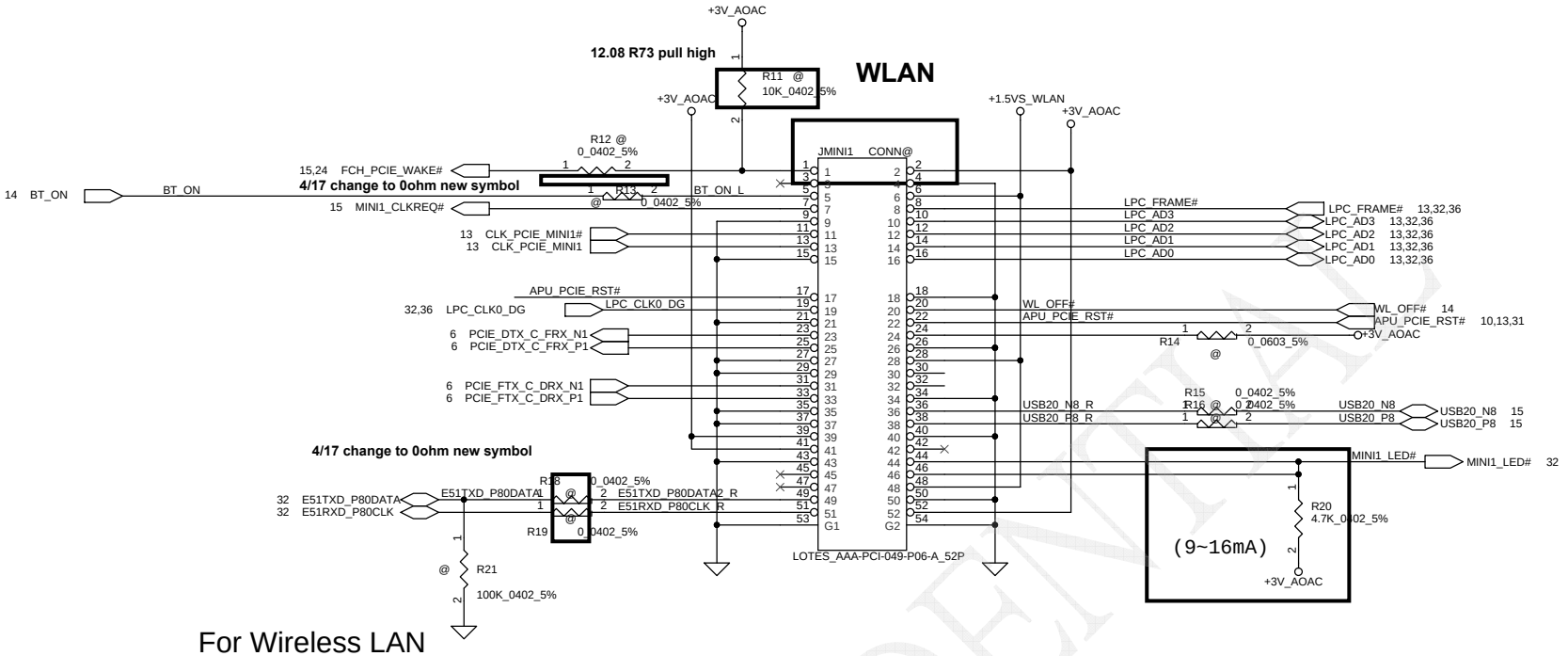
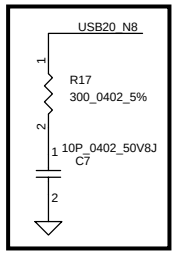
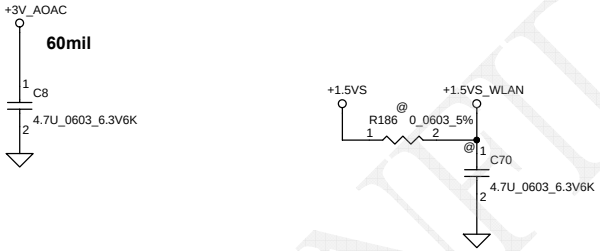


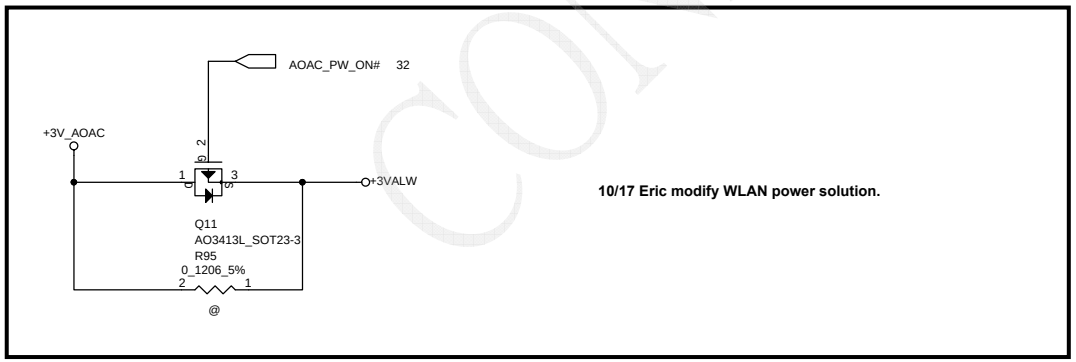
12/21 for AMD issue workaround



For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



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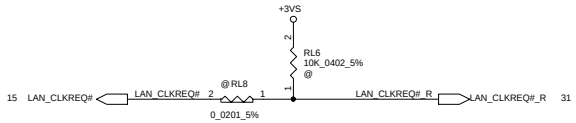
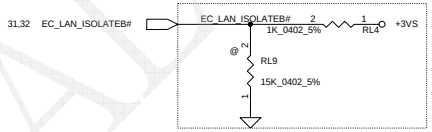
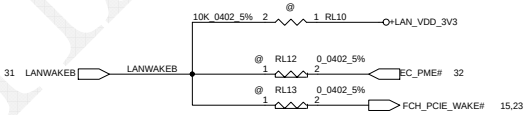




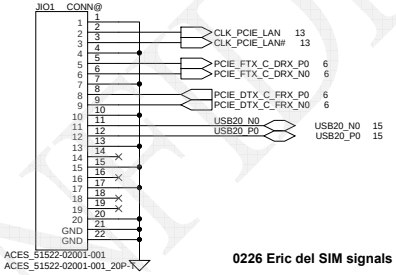
10/19 Eric del @ of RL10 for pull high, Del FCH_PCIE_WAKE# net, short RL12.



LED

<DB>Change to subboard.

20 Pin FFC



0226 Eric del SIM signals for remove WWAN.

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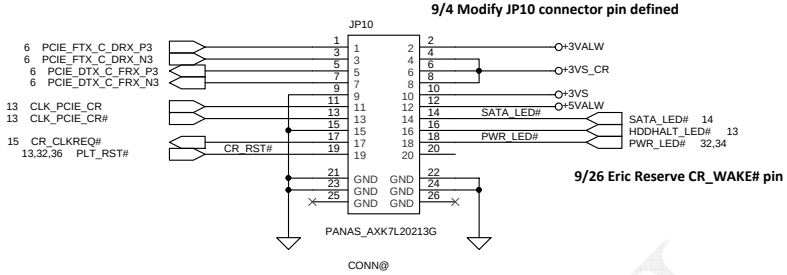
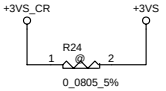
Card reader conn

9/4 Modify JP10 connector pin defined



9/26 Eric Reserve CR_WAKE# pin



10/4 Eric Reserve R212 for card reader power rail.

<CPU>

10/4 Eric Del +3VS_CR power rail from power switch

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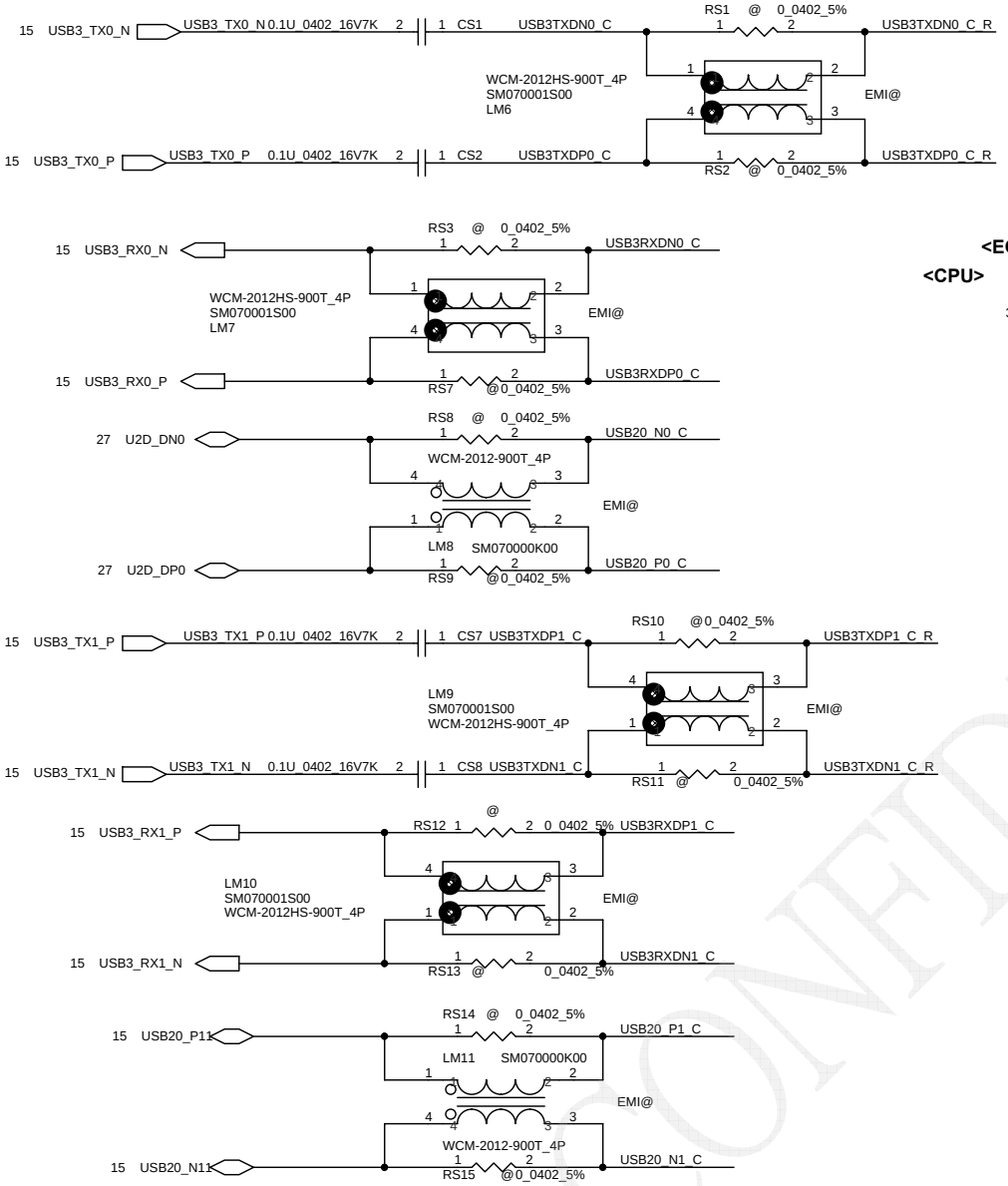
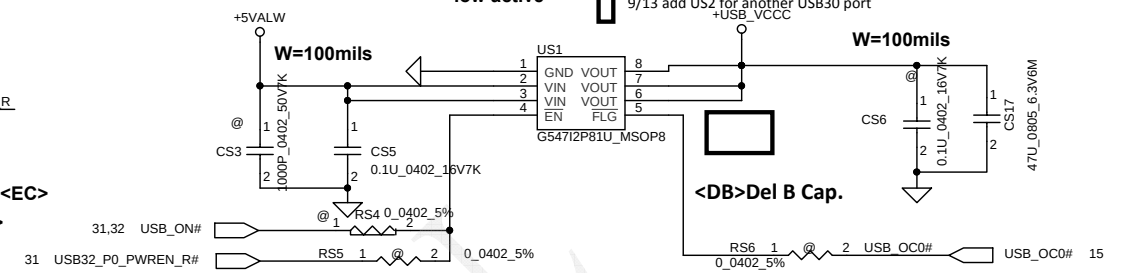


<EC>

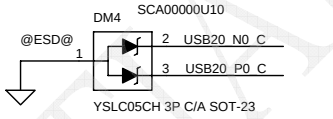
<CPU>

USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active

9/13 add US2 for another USB30 port



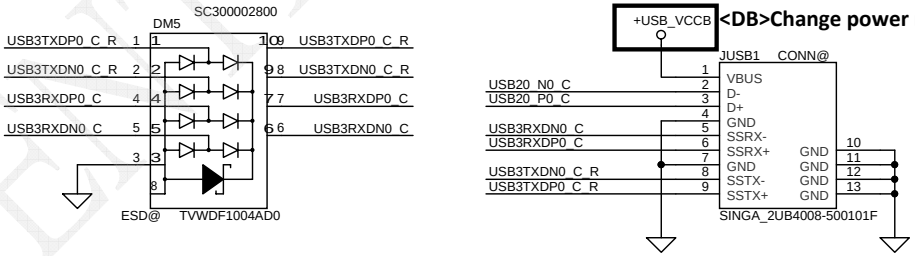
9/26 Eric change CS14 form 150uF to 47uF.

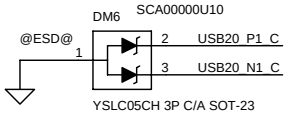


<DB>Update footprint to DC233008M10.

USB2.0/USB3.0 port 1

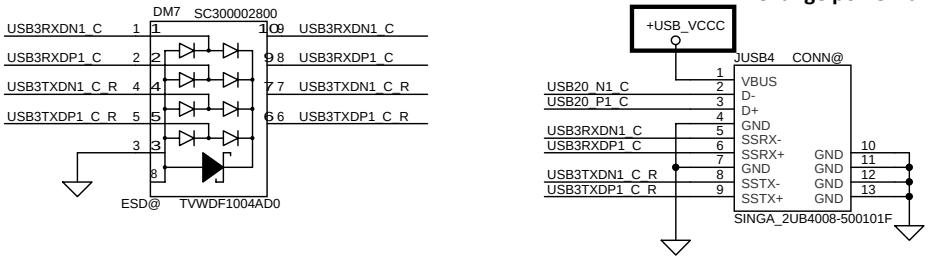
<DB>Change power rail to U18.





USB2.0/USB3.0 port 2

<DB>Change power rail to U18.



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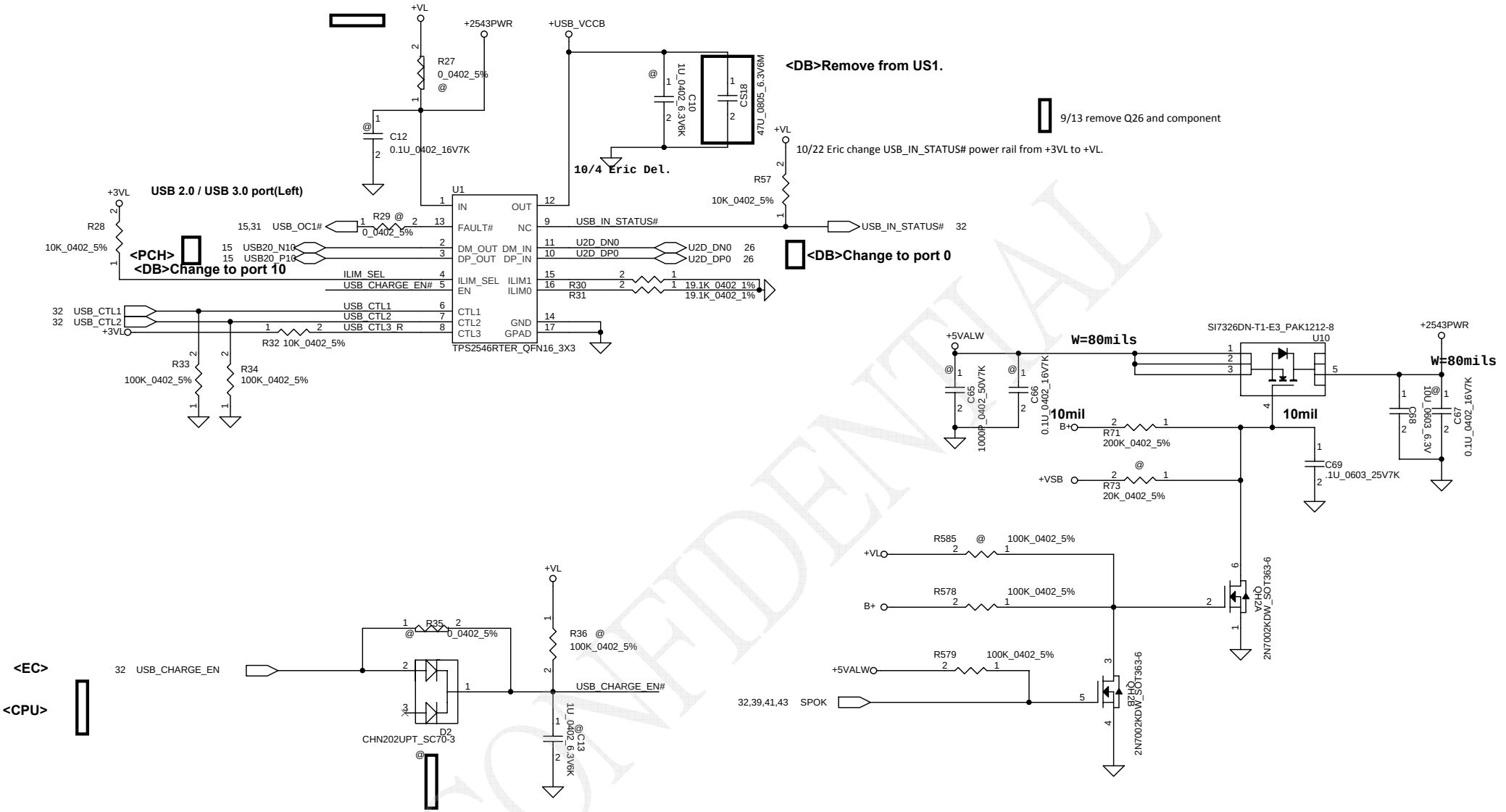

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Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

DVDD_IO should match
with HDA Bus level(optional for 3.3V signaling or 1.5V signaling)

Place AVDD ,PVDD,and DVDD capacitor close to Codec

RB3 Bead Max I=200mA

RB1 Bead Max I=3000mA

11/06 Beads close to UB1.

92HD91B2X5NLGXWCX8_QFN48_7X7

Place C208 close to Codec

Place C209,C210,CA87,CA89 close to Codec

Ext MIC

HP Jack

Internal SPKR

PLACE CLOSE TO U1 PIN 13

If Sense_A total length is greater than 6 inches, chagne C12 to 0.1uF

PLACE CLOSE TO U1 PIN 14

If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

Place need close UB3

9/17 add RF solution

change PN(SA000059J10) for 92HD91B2X5NLGXWCX8

10/17 Eric Del +5VALW to +5VS_AUDIO.

Audio power

Audio power

SB Beep

9/18 add reserve CB28, CB29 and stuff CB25,CB22,CB21 0.1uF

10/9 Eric Add EMI@ solution for CB31, CB35 & CB36 form EMI requirement.

Check HP LDO PN

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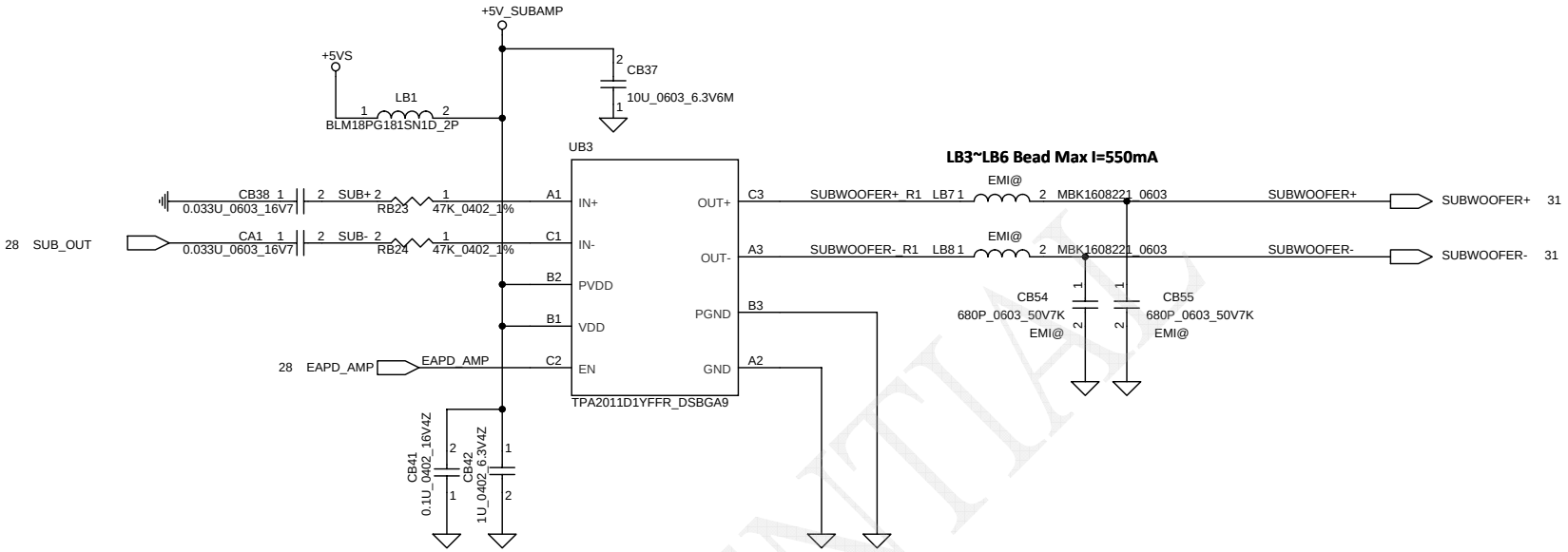
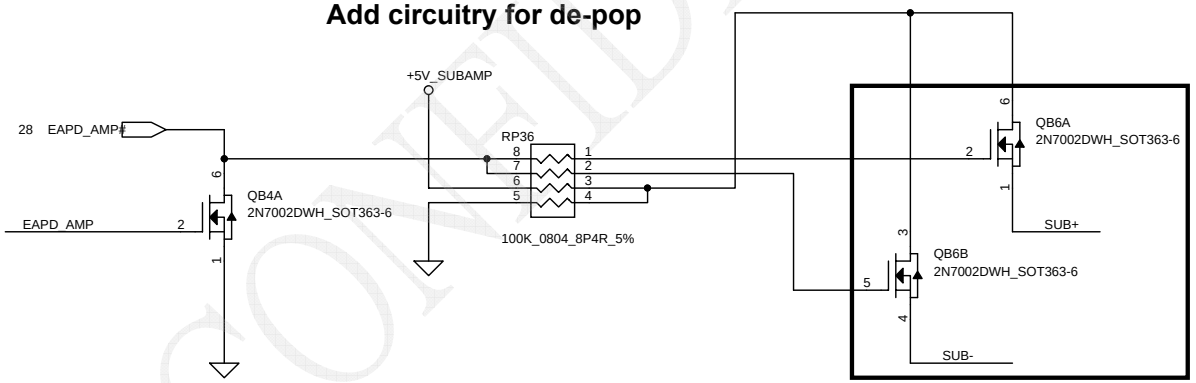
Subwoofer AMP TPA2011 = HPA01086YFFR

DB> TPA2012 Change to TPA2011



Add circuitry for de-pop



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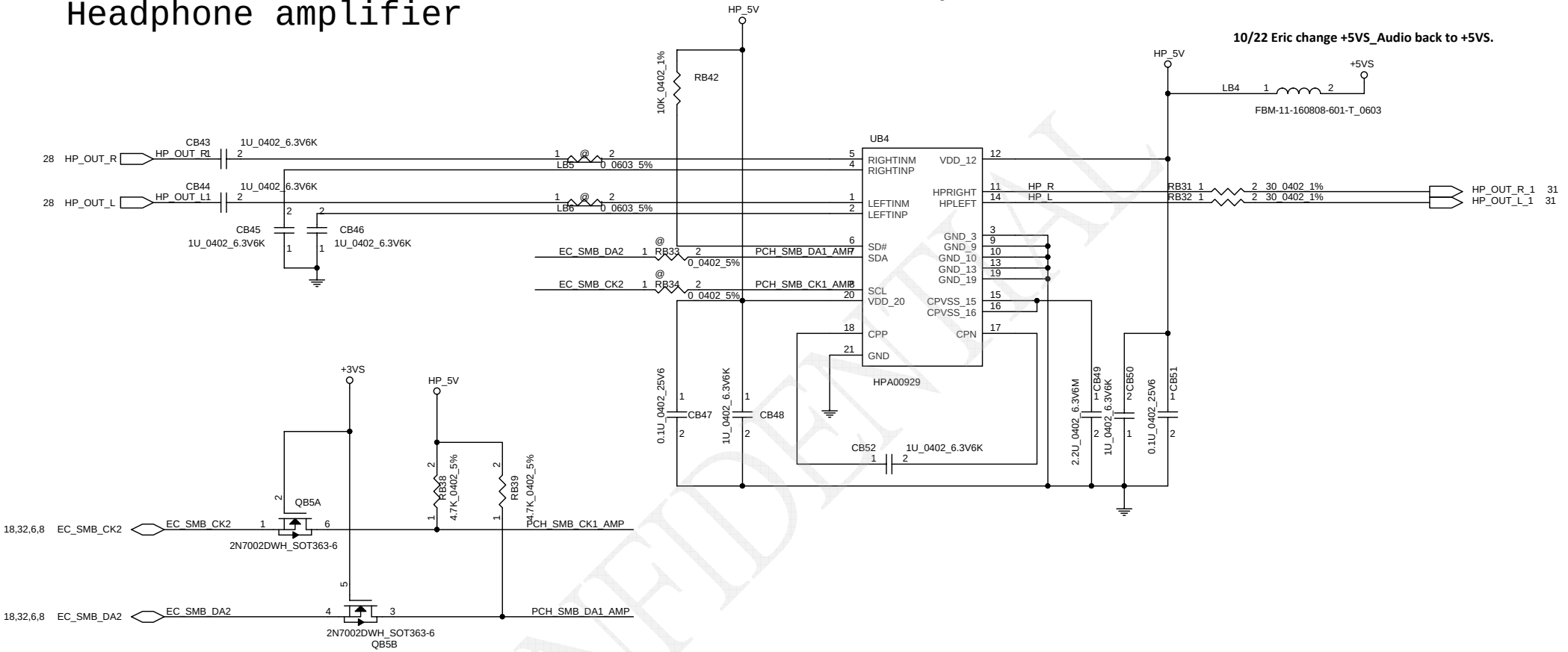
Headphone AMP TPA6130A2 = HPA00929

DB> HPA01196 Change to HPA00929

Headphone amplifier

10/22 Eric change +5VS_Audio back to +5VS.



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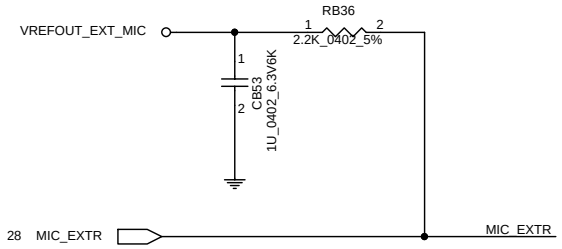
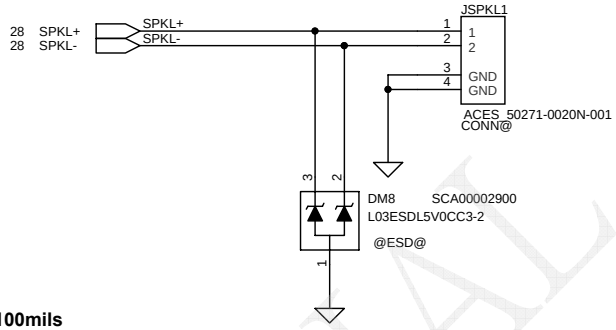
Ext. Mic

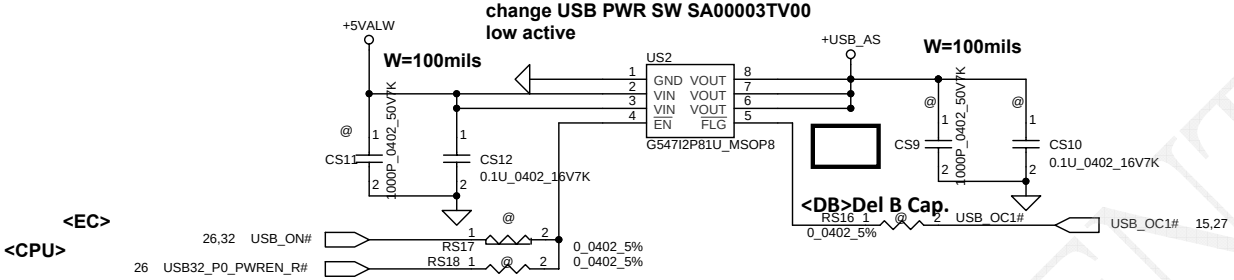


Front Speaker Connector 1

SPK conn



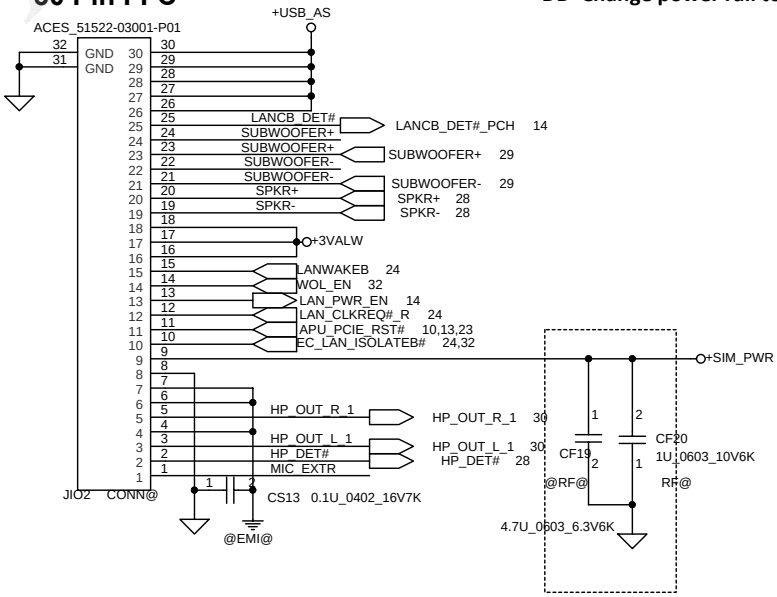
USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active



Headphone and Mic conn

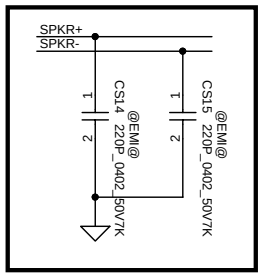
30 Pin FFC

<DB>Change power rail to US1.



10/30 RF add, near JIO1 connector.

11/06 EMI Cap close to JIO2.



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<db0>

Ming9/3 change to 8.2KK for DB phase board ID

	DB	SI	PV	MV
Board ID Rk13	0 K ohm	12K ohm	15K ohm	20K ohm
Project ID RK11	56k ohm	56k ohm	56k ohm	56k ohm

<DB>Add RK57

<DB>KBC 9012

Ming9/3 change Board ID to 8.2K for CS DB phase

Board ID control

<DB>Del HDMI_PWR_PD
<DB> add DGPU_GC6_EN on Pin M2
Ming8/28 remove DGPU_GC6_EN for UMA only

Ming 8/30 remove MINI1_LED#

MINI1_LED# NonCS only

<DB>Add PM_CLKRUN# and RK59

10/24 Eric modify SMBUS1 power rail to +3VALW_EC.

Ming9/18 change 0ohm to new footprint

Ming 9/3 add ADP_ID for power

Ming9/18 change 0ohm to new footprint

<PWR>
<HW>
Ming 9/4 add WWAN_OFF# to GPIO3D
Ming 9/3 remove LANCB_DET# EC and RK55
Ming 9/3 remove TP_ON_OFF_LED#
Eric 9/25 Add WWAN_OFF# to GPIO3D

Add LANCB_DET#_EC

EAPD:NonCS only

Ming 8/30 remove EAPD

Ming9/13 remove EC_SMI# for EC request

10/15 Eric remove SUSACK#.

<DB>Del EC SPI signal
EC suggest does not use as GPIO

<DB>Del EC SPI ROM
<DB> add VGA_THRMTRIP# on Pin J2
<DB> add FB_CLAMP_TGL_REQ# on Pin K2
<DB> add DGPU_HOLD_RST# on Pin M1
<DB> add GPU_THERMAL_DET# on Pin N2
Ming8/28 remove GPU GPIO for UMA only
Ming 9/13 remove PM_BATLOW#

Ming9/13 add KSO16/ KSO17 for KB request

Ming9/18 change 0ohm to new footprint

10/16 Eric change vgate from pin97 to pin 74.

10/18 Eric Add AOAC_PW_ON.

Add EC_LAN_ISOLATEB#

2/22 Eric Add SPOK to EC N7.

Add PROC_DETECT#

Ming9/3 remove PROC_DETECT#
change PM_SLP_SUS# to GPIO15

10/3 Eric Del ENBKL control pin.

10/16 Eric Change VR_ON to 108.

<DB>Remove @ 32.768KHz 'XTAL

<DB>Pin117 NC-->NMI_DBG#

<DB>RK56 10K-->100K

<DB>Remove JFW1

<DB>RK50 10K-->100K

10/4 Eric Del.

10/4 Eric Del.

20mil

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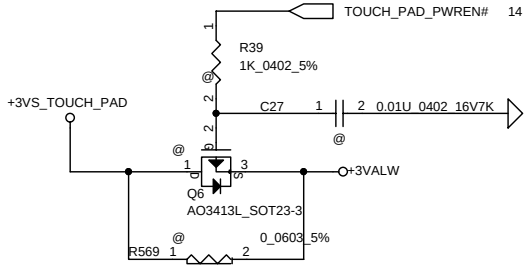
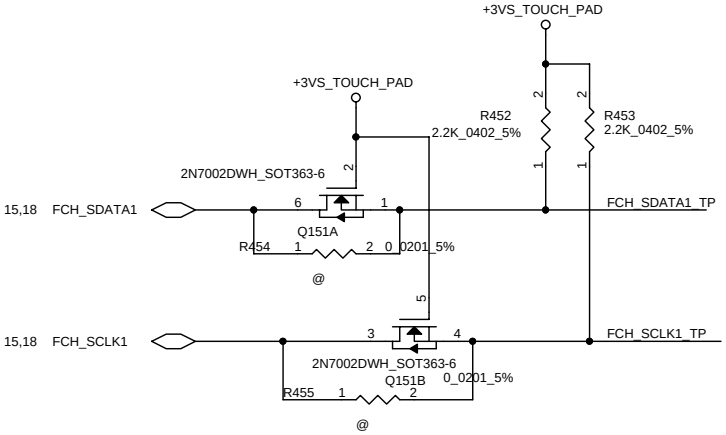


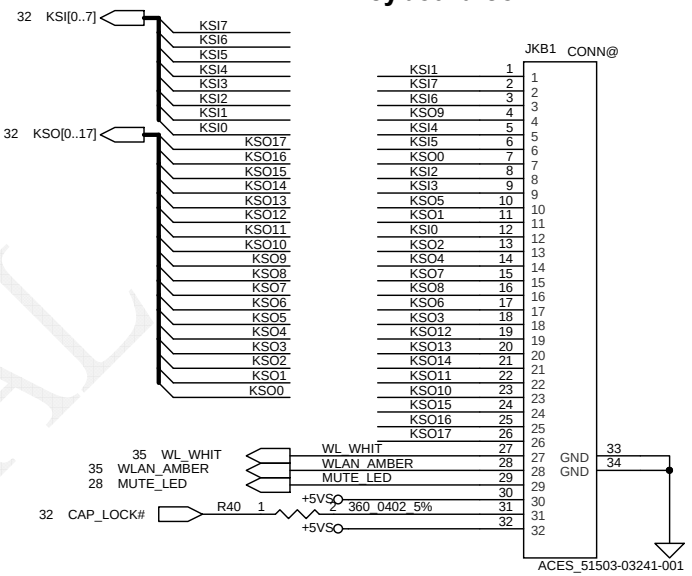


Touch pad conn

10/29 Del all KB caps.

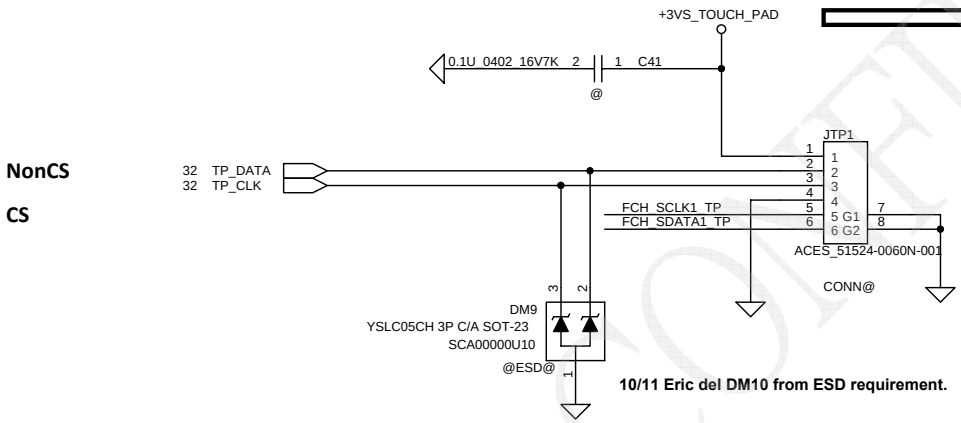
EMI reserve

Keyboard conn



Keyboard backlight Conn

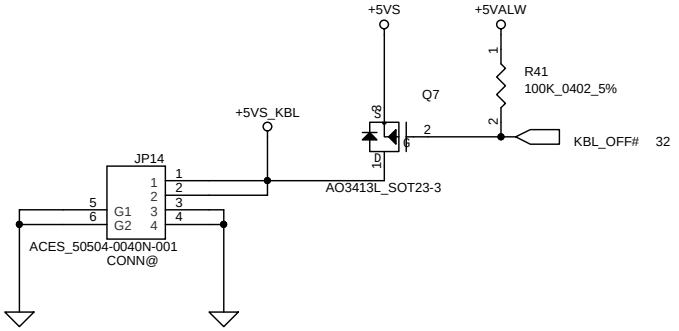
<DB>Check footprint and Touch PAD spec



NonCS

CS

10/11 Eric del DM10 from ESD requirement.



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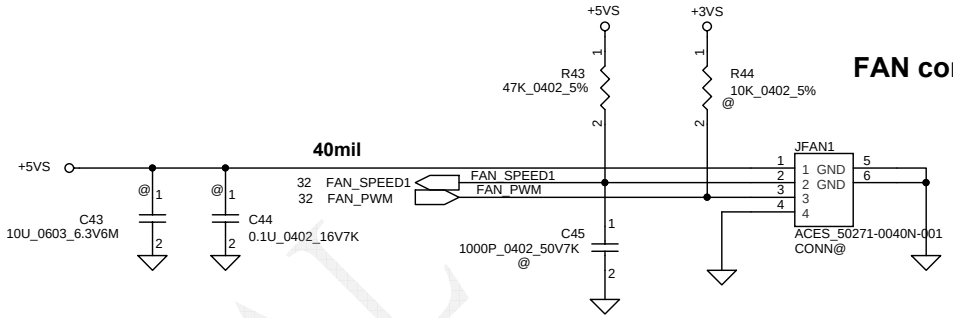
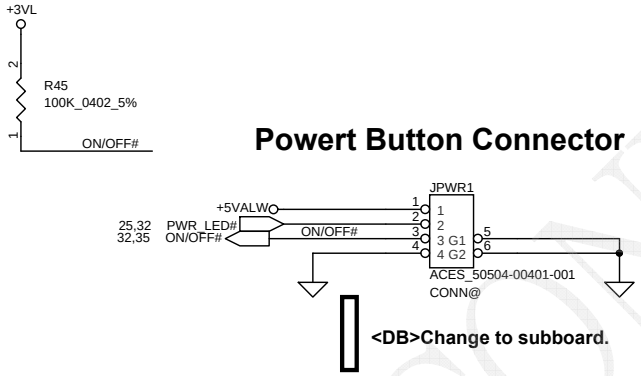
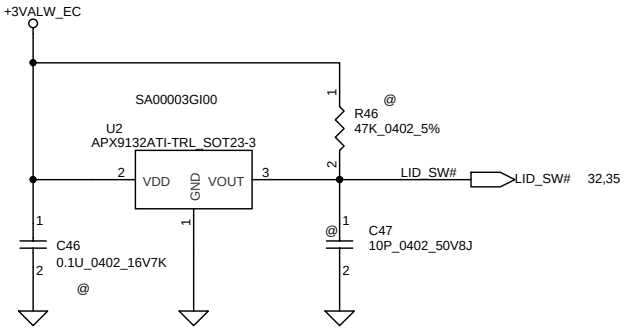
FAN conn



Powert Button Connector



Lid Switch (Hall Effect Sensor)



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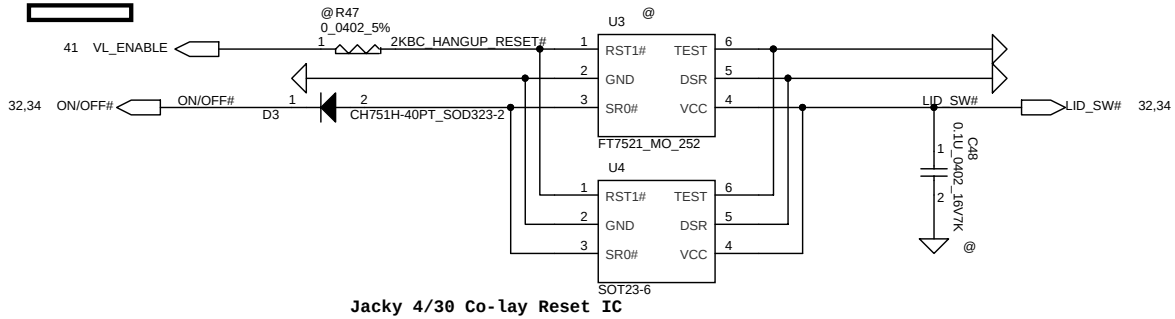
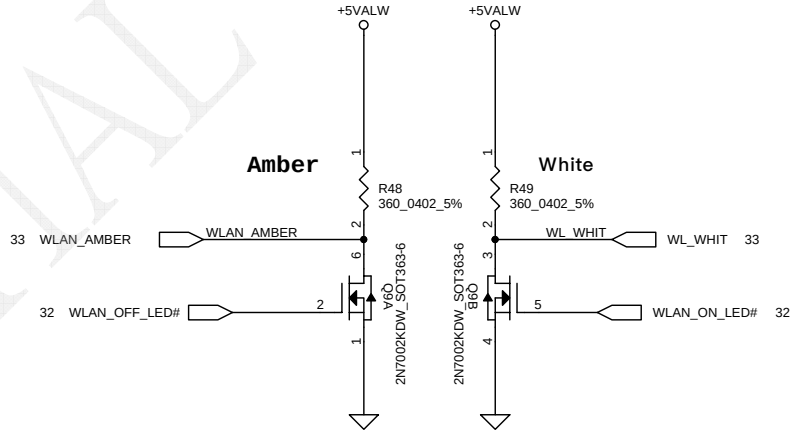
Reset IC

<DB> RST1# connect to ENM



Jacky 4/30 Co-lay Reset IC



CPU

H1 H_3P3 HOLEA
H2 H_3P3 HOLEA
H3 H_3P3 HOLEA
H4 H_3P3 HOLEA

PAD1
MB_SUP_BRK_25X5
HOLEA

Card reader

H7 H_3P3 HOLEA
H8 H_3P3 HOLEA

PCB
ZZZ1
LA-9851P
DA6000Y8000

H13 H_2P8 HOLEA
H5 H_2P8 HOLEA
H6 H_2P8 HOLEA
H16 H_2P8 HOLEA
H10 H_2P8 HOLEA

FD1 FIDUCIAL_C40M80
FD2 FIDUCIAL_C40M80
FD3 FIDUCIAL_C40M80
FD4 FIDUCIAL_C40M80

H15 H_3P0X2P5 HOLEA
WWAN
H9 H_2P8 HOLEA
H11 H_3P3 HOLEA
H12 H_3P3 HOLEA
WLAN

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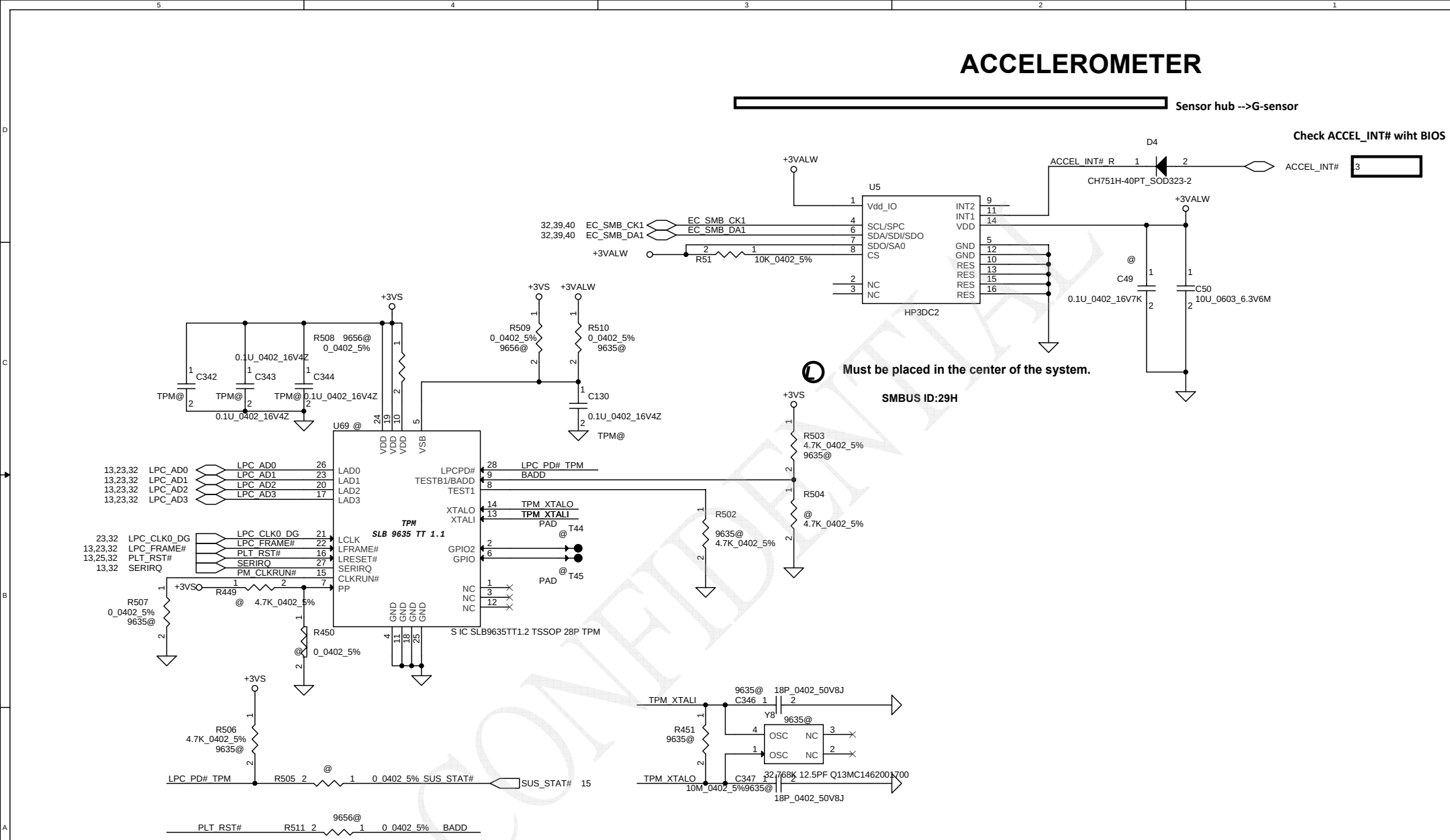
ACCELEROMETER



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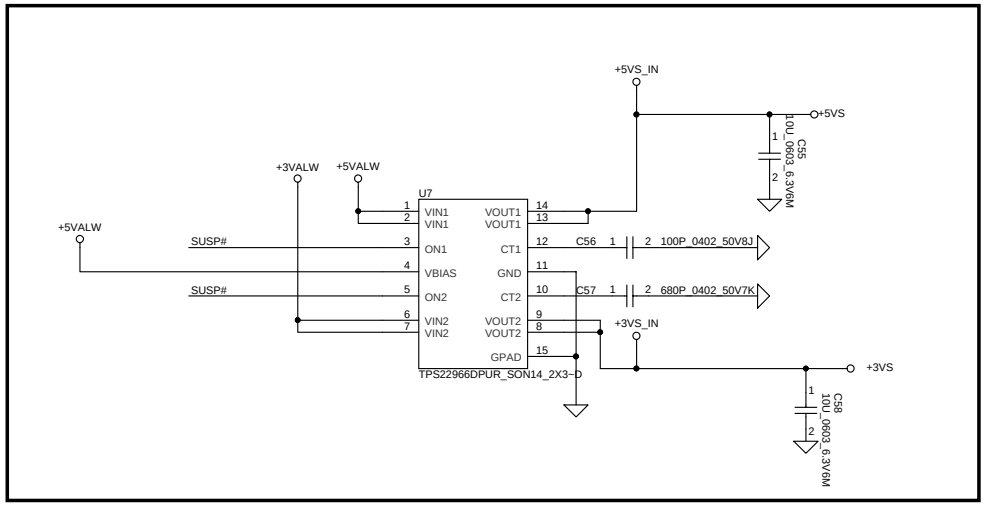
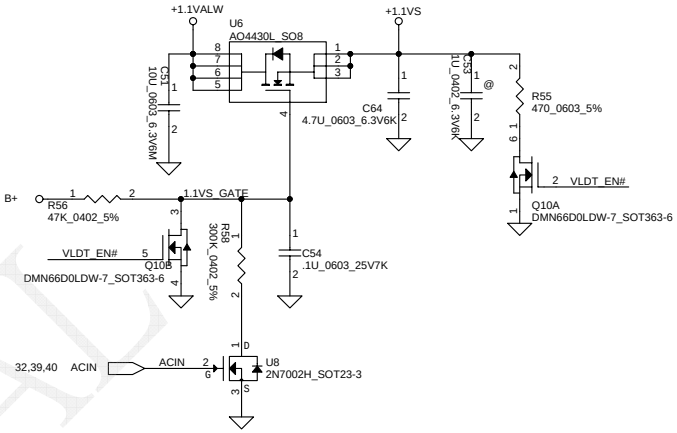
3/6 Co-lay 3VS/5VS low switch circuit

Each 250pF on CAP_MOS1 (2) will make
Slew Rate(uS/V) increase of 100uS/V

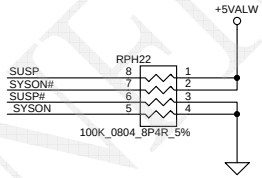


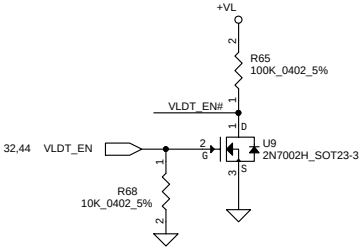
+1.1VALW TO +1.1VS (1.1A)

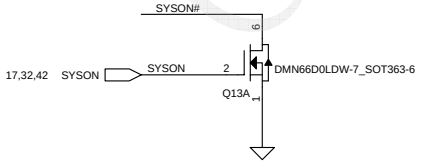


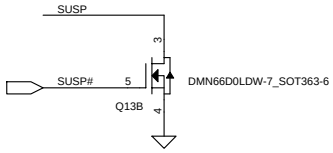
+1.5VTO +1.5V_PCIE

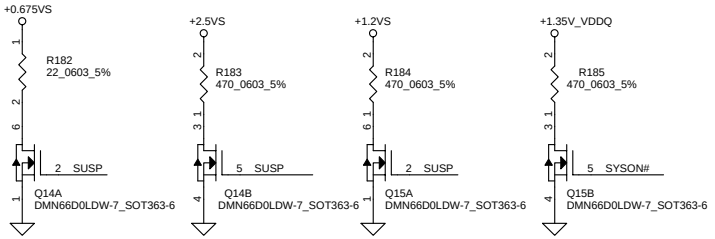
10/17 Eric Del +1.5V to +1.5V_PCIE.

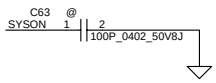












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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Version
1	23	Del short pad of R22	1/7		For Port80 issue	0.2
2	32	Change RK33 from 0 ohm to 12k ohm.	1/7		For SI phase board ID requirement	0.2
3	27	Add R578	1/7		For USB charger port requirement	0.2
4	13	Add CH101	1/7		For ESD requirement	0.2
5	23	Del R76, Q150, R370 and C73	1/7		For EC control directly	0.2
6	15	Change RF9 from 680pF to 15pF	1/7		For FIX EA issue	0.2
7	13	Add CH18	1/7		For FIX PLT_RST# noise	0.2
8	32	Del RK35	1/7		For EM1 no requirement	0.2
9	26	Add RK37	1/7		For support WOL in DC S5 mode	0.2
10	41	Change jump net name +3VLP to +3VL	1/7		For connection between PWR and HW	0.2
11	41	Change net name VL to +VL	1/7		For connection between PWR and HW	0.2
12	44	Change net name SUSP# to VLDT_EN for 1.2V EN	1/7		For connection between PWR and HW	0.2
13	39	Reserve PC9, PC10, PC13, PR13, PR14, PR16, PR18, PQ2, PQ4	1/7		For charger IC +VSB circuit	0.2
14	40	Change net name +3VALW to +3VL	1/7		For correct cell selection in S5	0.2
15	40	Change PR111 from 0 ohm to 2.2 ohm.	1/7		For EM1 request	0.2
16	40	Mount PC110, PC108, PR113, PC120	1/7		For EM1 request	0.2
17	40	Add PC136 0805 10uF	1/7		For EM1 request	0.2
18	39	Reserve PR29, PR31, PR32, PR33	1/7		For AC LED circuit	0.2
19	39	Reserve PQ6, PU4A, PU4B, PD8, PR19, PR20, PR21, PR22, PC22, PC23	1/7		For One Shot circuit	0.2
20	39	Reserve PR23	1/7		For Hysteresis resistor	0.2
21	39	Change net name H_PROCHOT#_EC to EC_THERM	1/7		For correction	0.2
22	41	Change PR302 from 30k ohm to 30.9k ohm	1/7		For USB port load issue	0.2
SI2		SI2	SI2		SI2	
1	21	Remove WWAN portion.	1/30		For HP requirement.	0.4
2	32	Change RK33 to 20K ohm from 15kohm.	1/30		For EC requirement.	0.4
3	45	Change PWM IC from ISL62771 to ISL6277A	1/30		For Power +APU_CORE_NB two pahse requirement.	0.4
4	45	Add one more phase for CORE NB and Use Dual-N MOSFET for each phase.	1/30		For Power requirement.	0.4
PV		PV				
1	32	Change RK33 from 20k ohm to 27k ohm.	3/03		For PV phase board ID requirement	0.5
2	36	Reserve TPM circuit	3/03		For HP requirement.	0.5
3	22	Remove R60, R61, R62 and R63.	3/03		Remove SATA co-lay.	0.5
4	43	Add PR1106.	3/03		For EC Fix code requirement.	0.5
5	22	Remove R69.	3/03		Remove +5V_HDD 0hm.	0.5
6	46	Modify +CPU_CORE_NB to two phase soluiton.	3/03		For PWR requirement.	0.5
7	32	Add C71, C73.	3/03		For ESD requirement.	0.5
8	15	Add C72.	3/03		For ESD requirement.	0.5
9	15	Reserve C74.	3/03		For ESD requirement.	0.5
10	13	Add C75.	3/03		For ESD requirement.	0.5
11	24	Move Lan chip to sub board.	3/03		For HW requirement.	0.5
12	41	Reserve PR318	3/03		For EM1 requirement.	0.5
MV		MV				
1	40	Add PC137	4/09		For PWR requirement.	1.0
2		change PR151, PR318, PR412, PR1106, PR1203, PRG4, PRG8, PRG10. PRG22, PRG23, PRG28, PRZ9, PRZ12, PRZ20, PRZ33, PRZ44 from 0 ohm to short pad	4/11		For PWR requirement.	1.0

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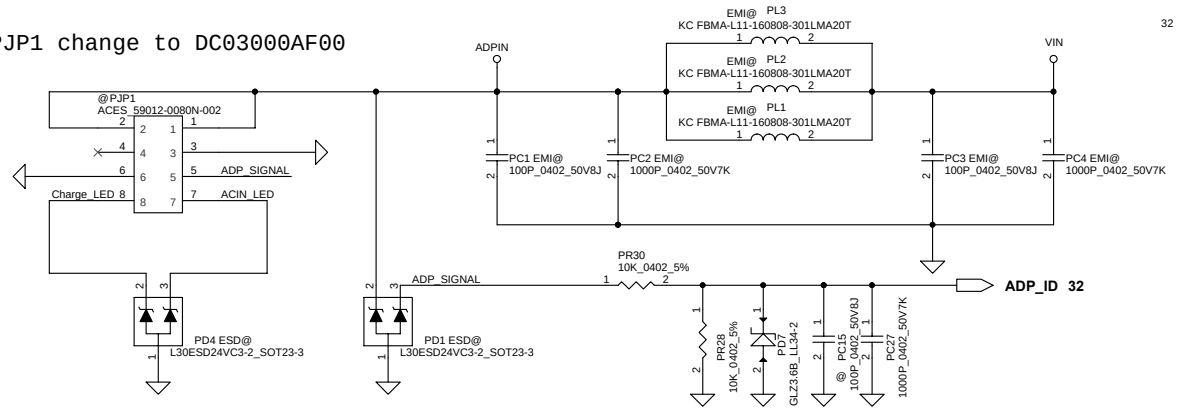
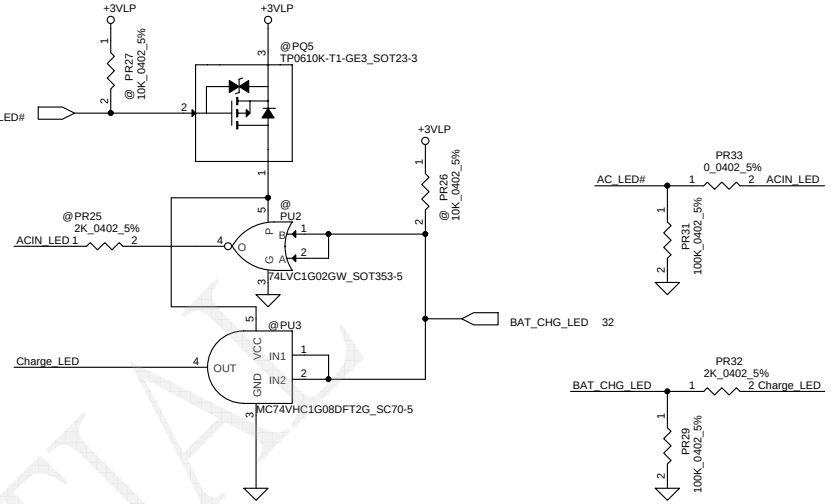
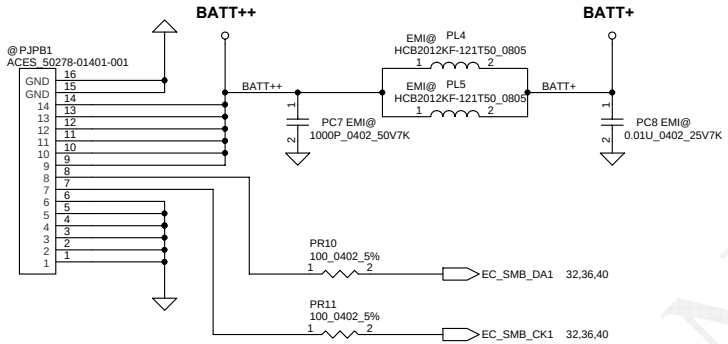
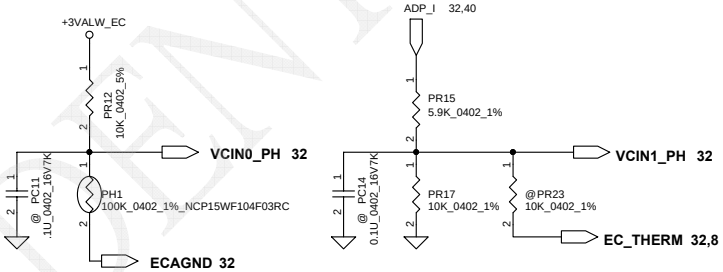
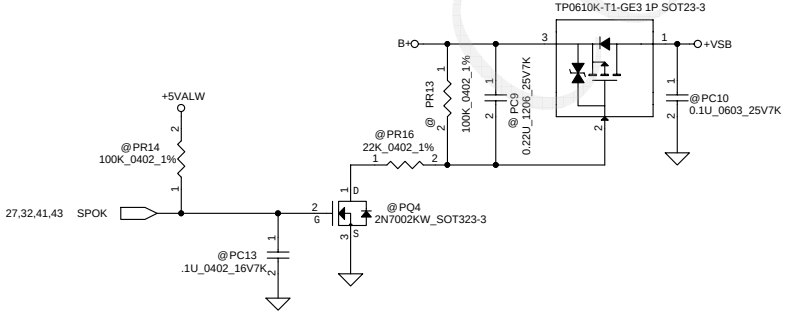
PJP1 change to DC03000AF00

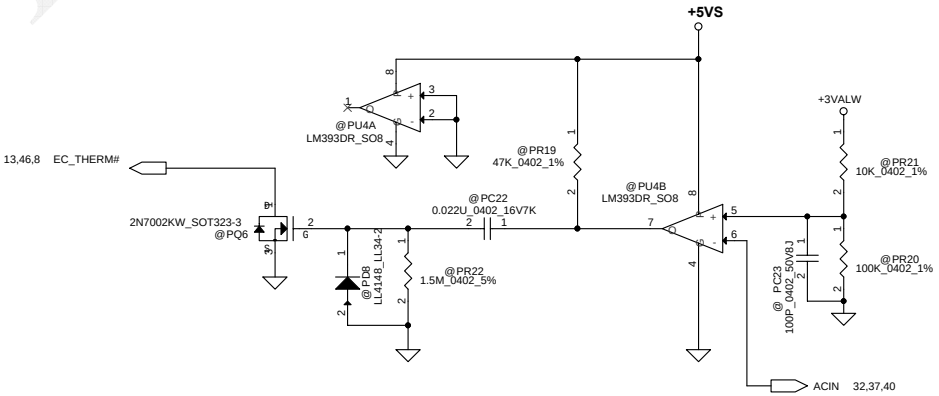












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Size	Document Number	Rev
Custom	4019NK	A

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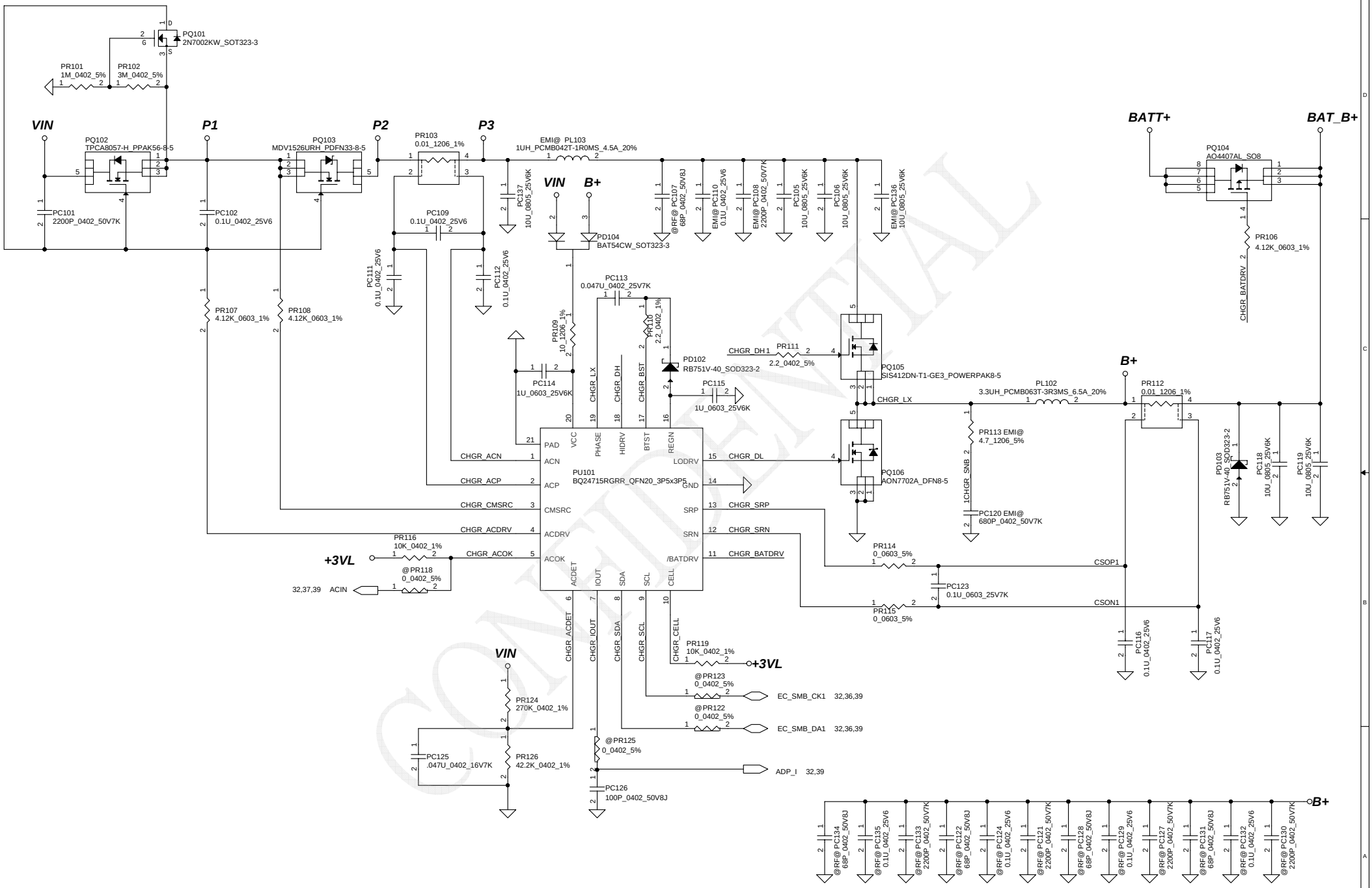

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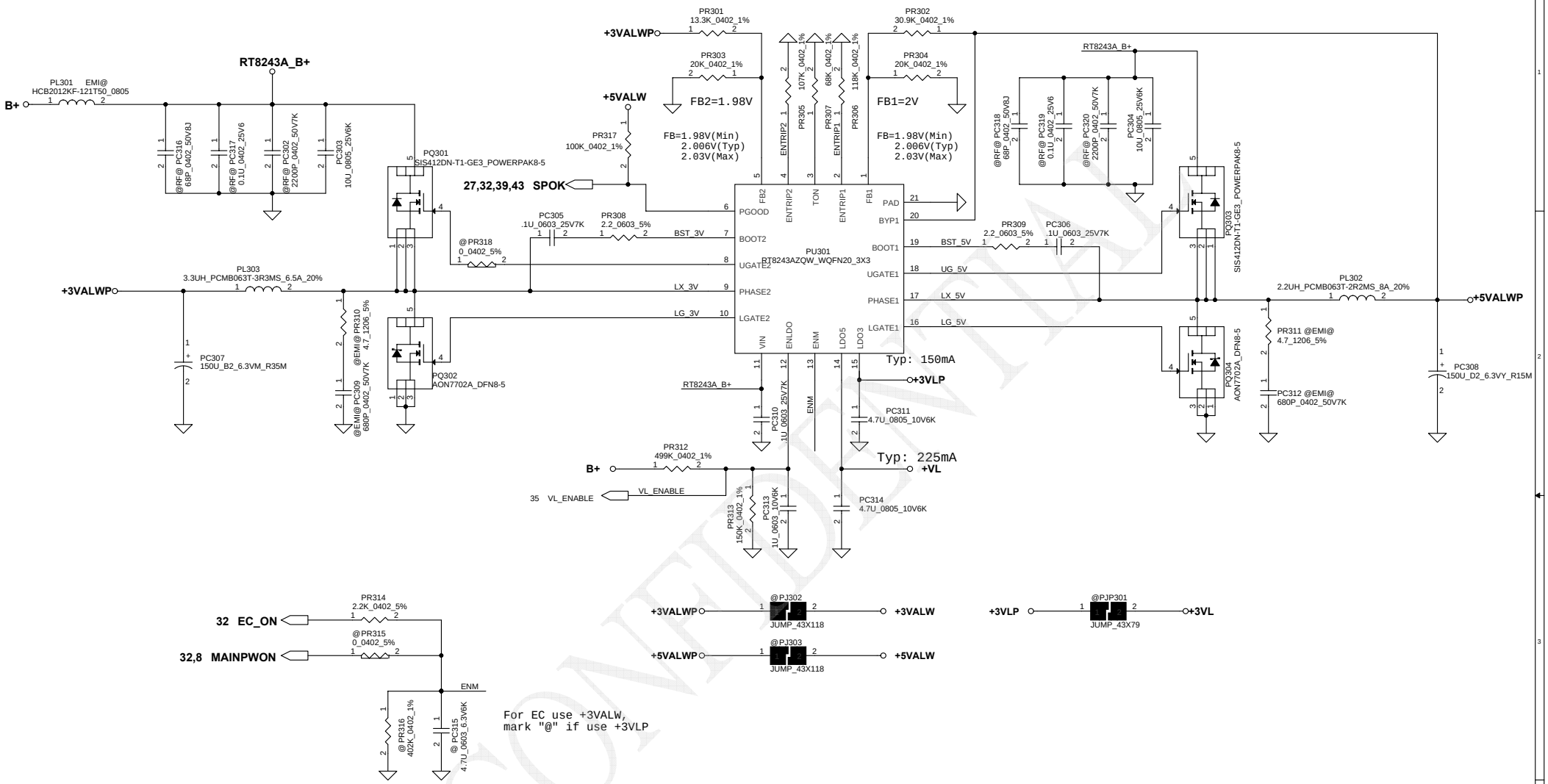

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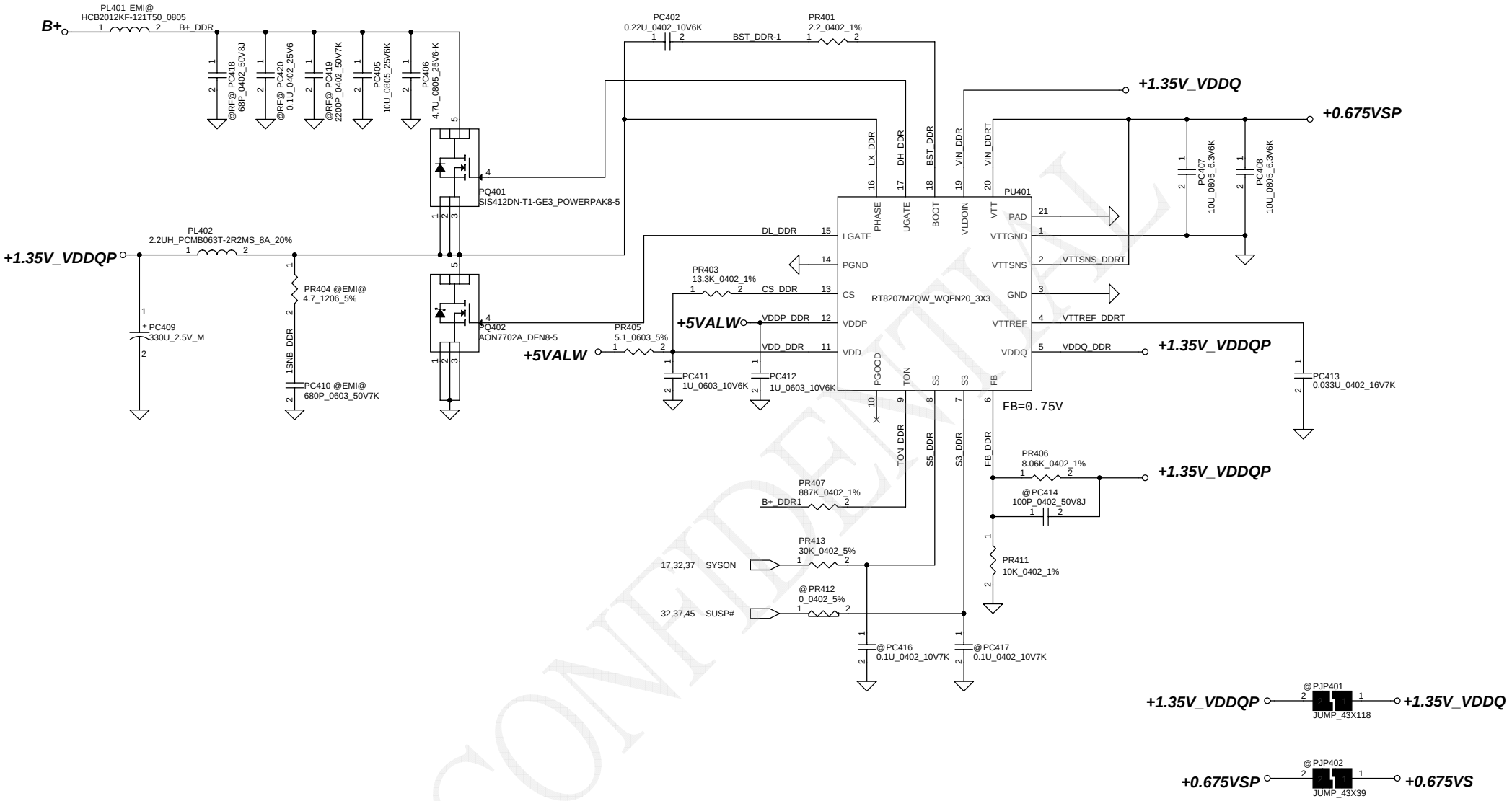

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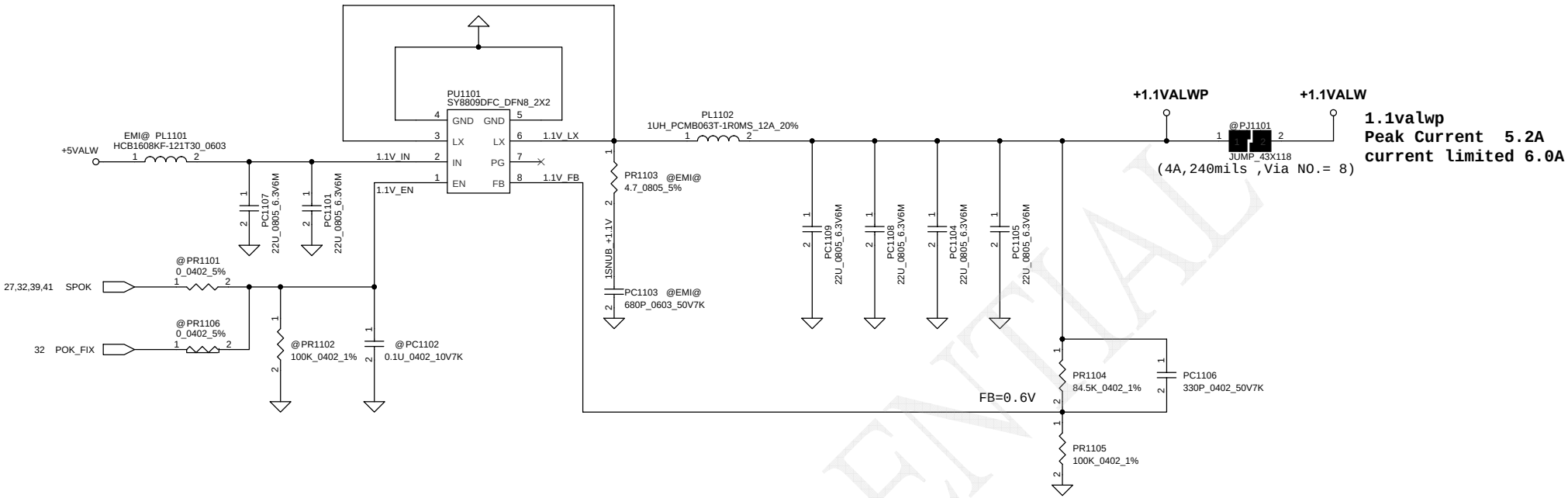

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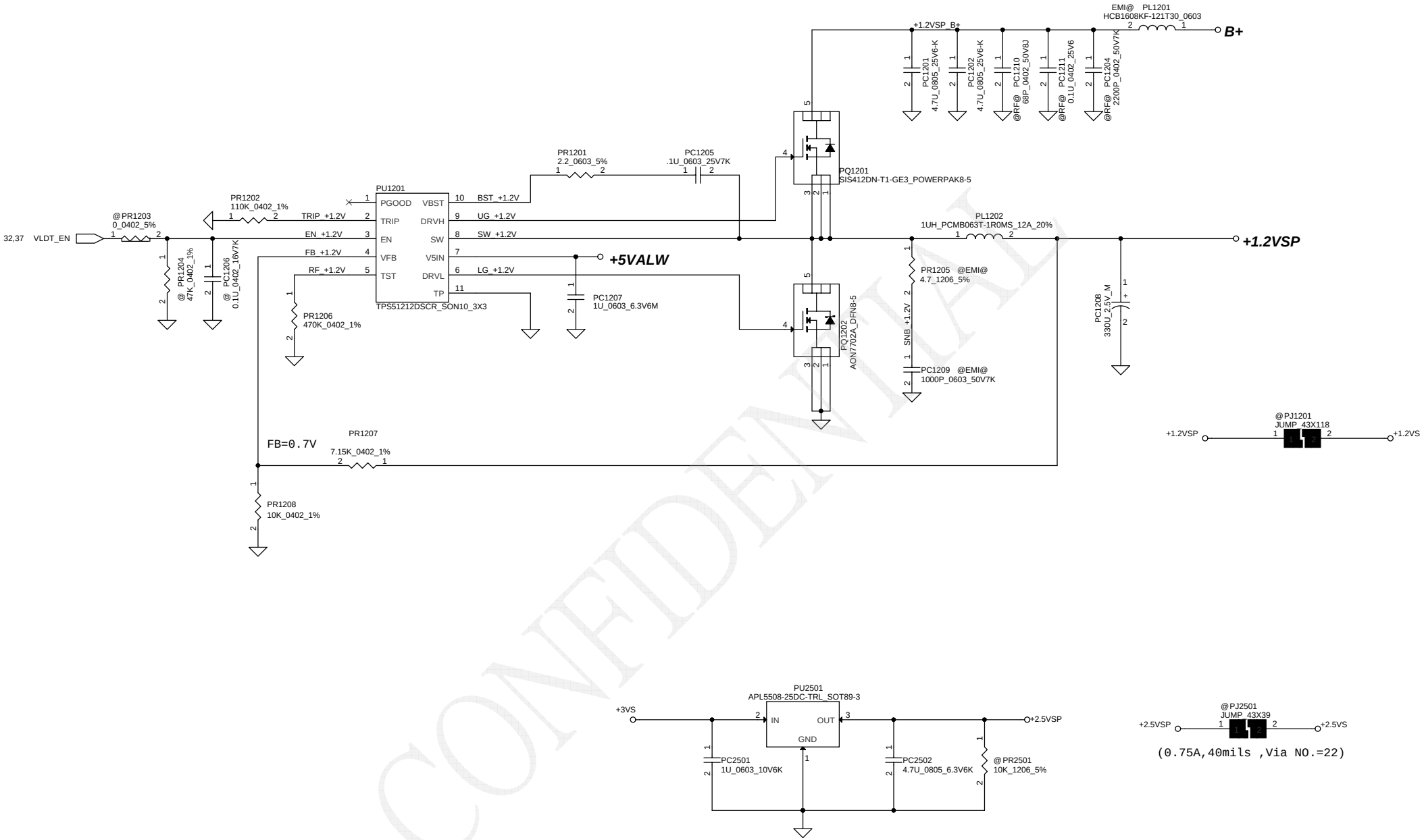

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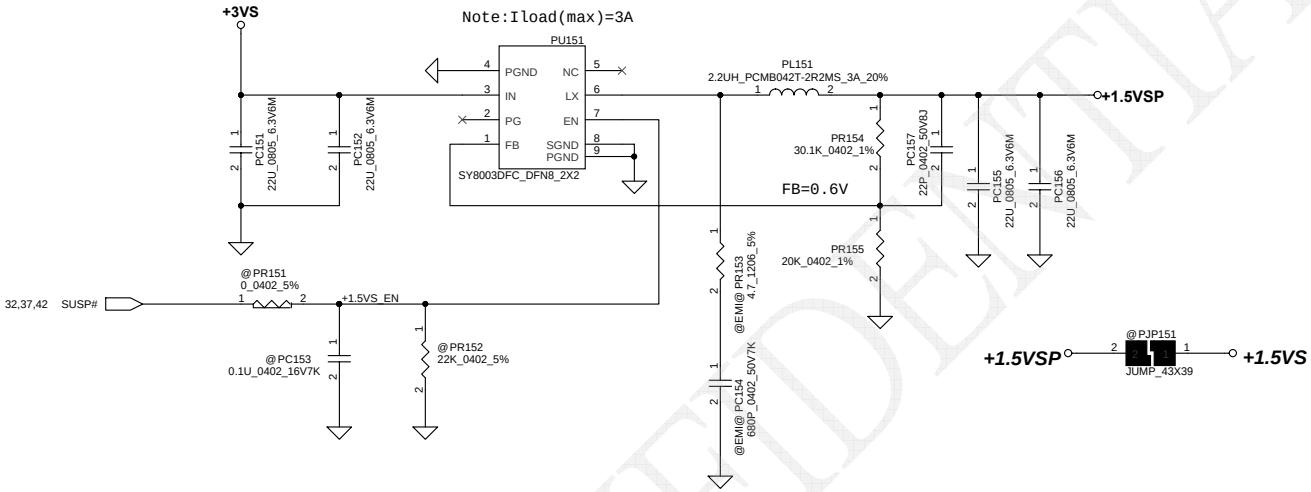

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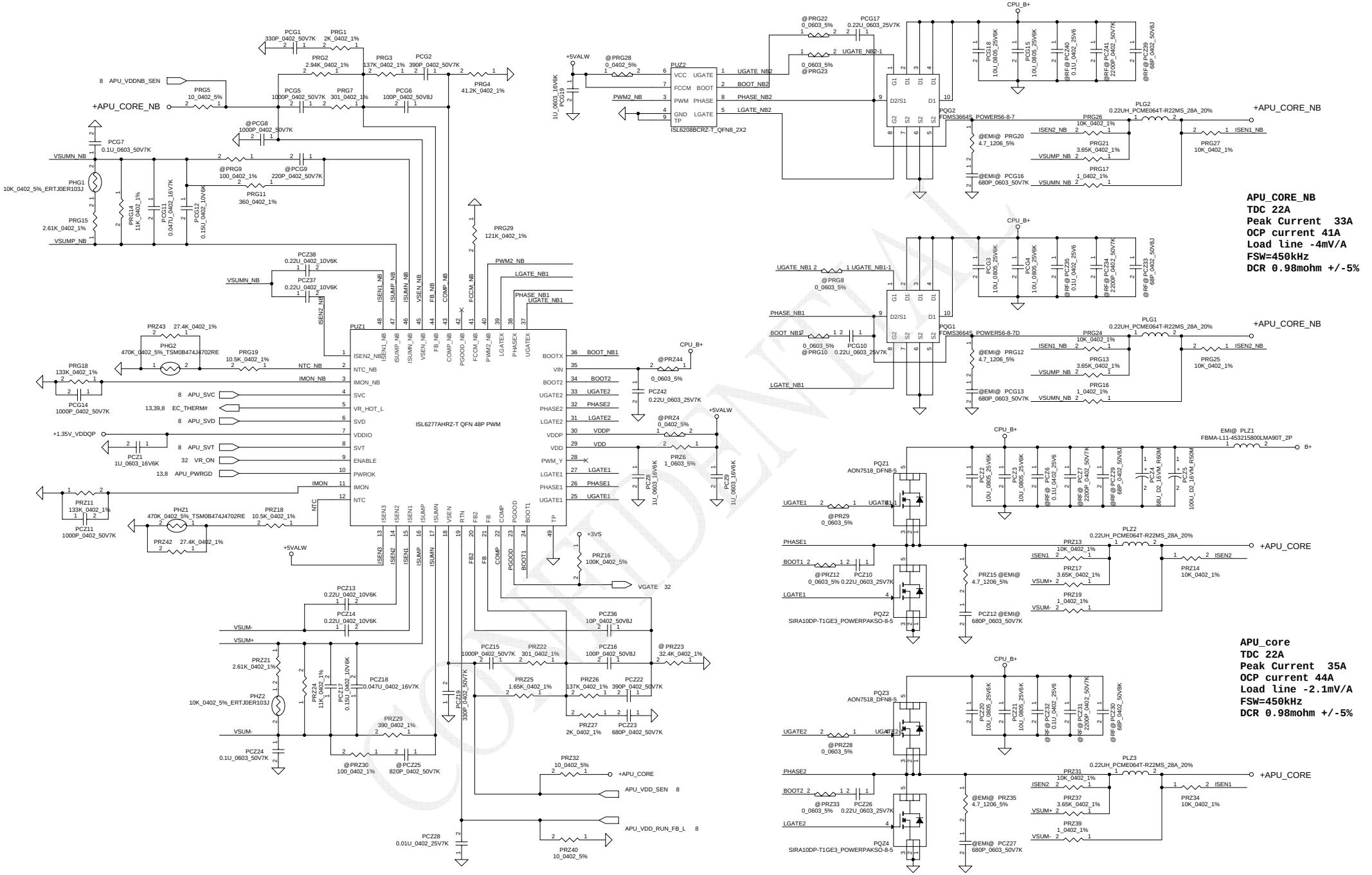

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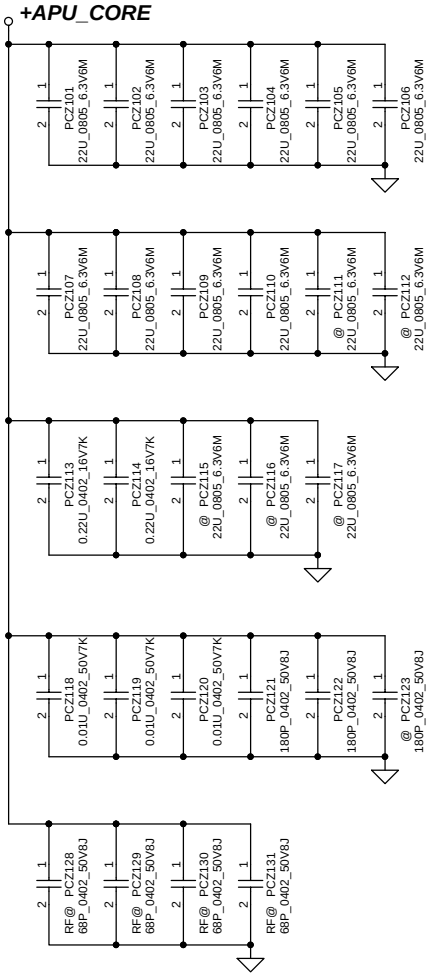

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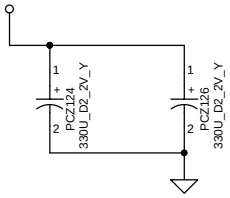

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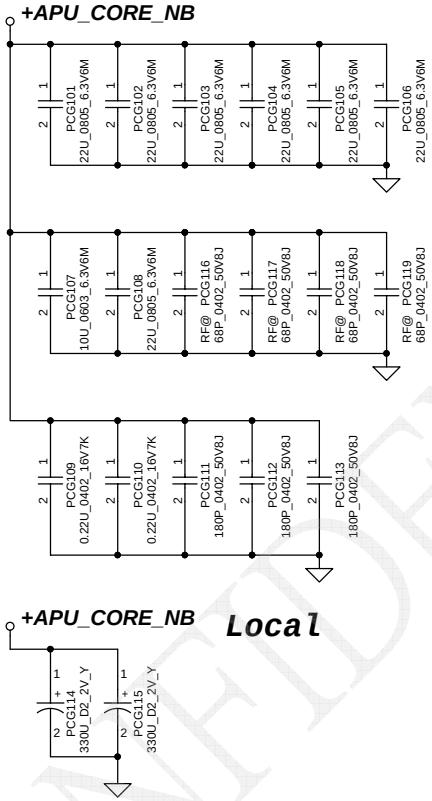

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