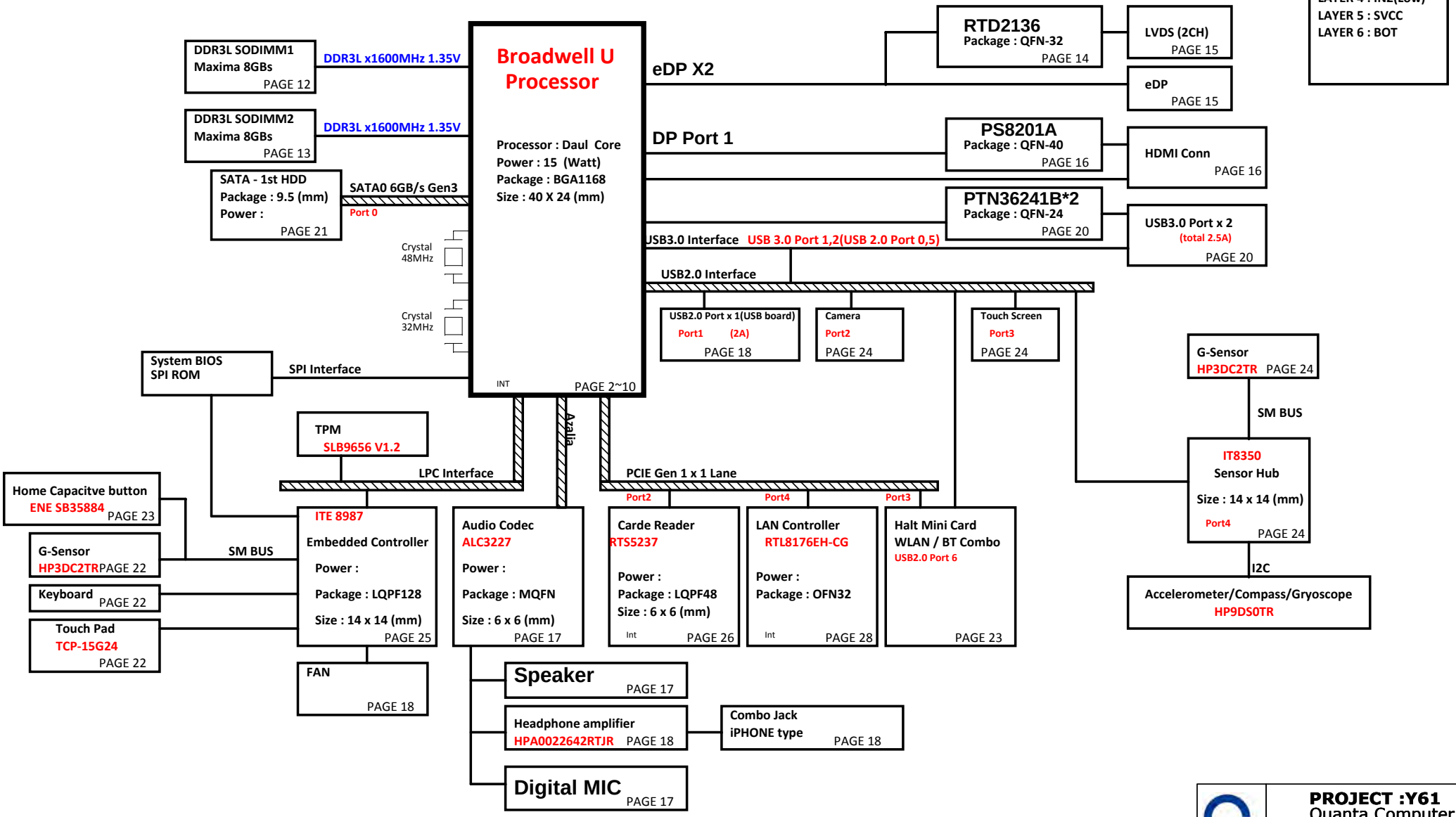
13"/15"
Y61 Intel Cresent Bay ULT Platform Block Diagram

PCB 6L STACK UP

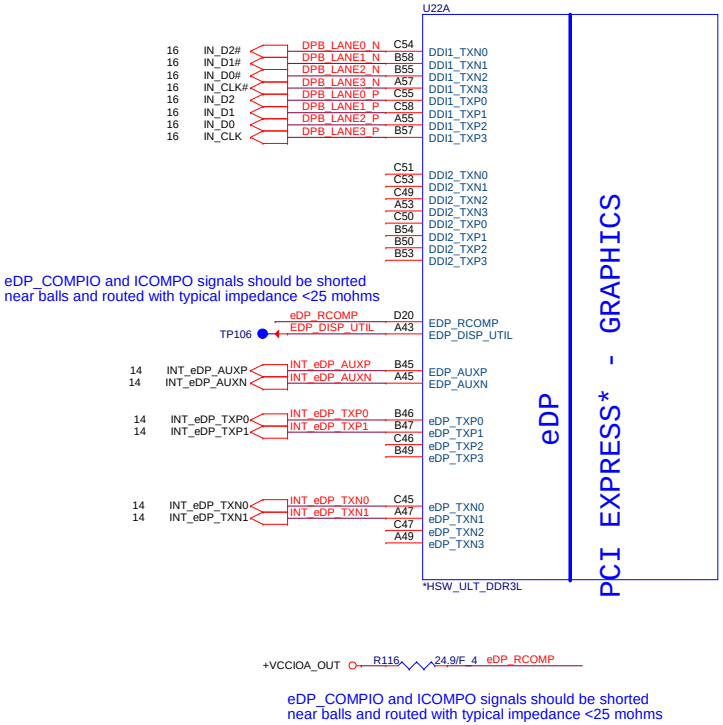
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A
Date: Monday, April 21, 2014	Sheet 1 of 32	

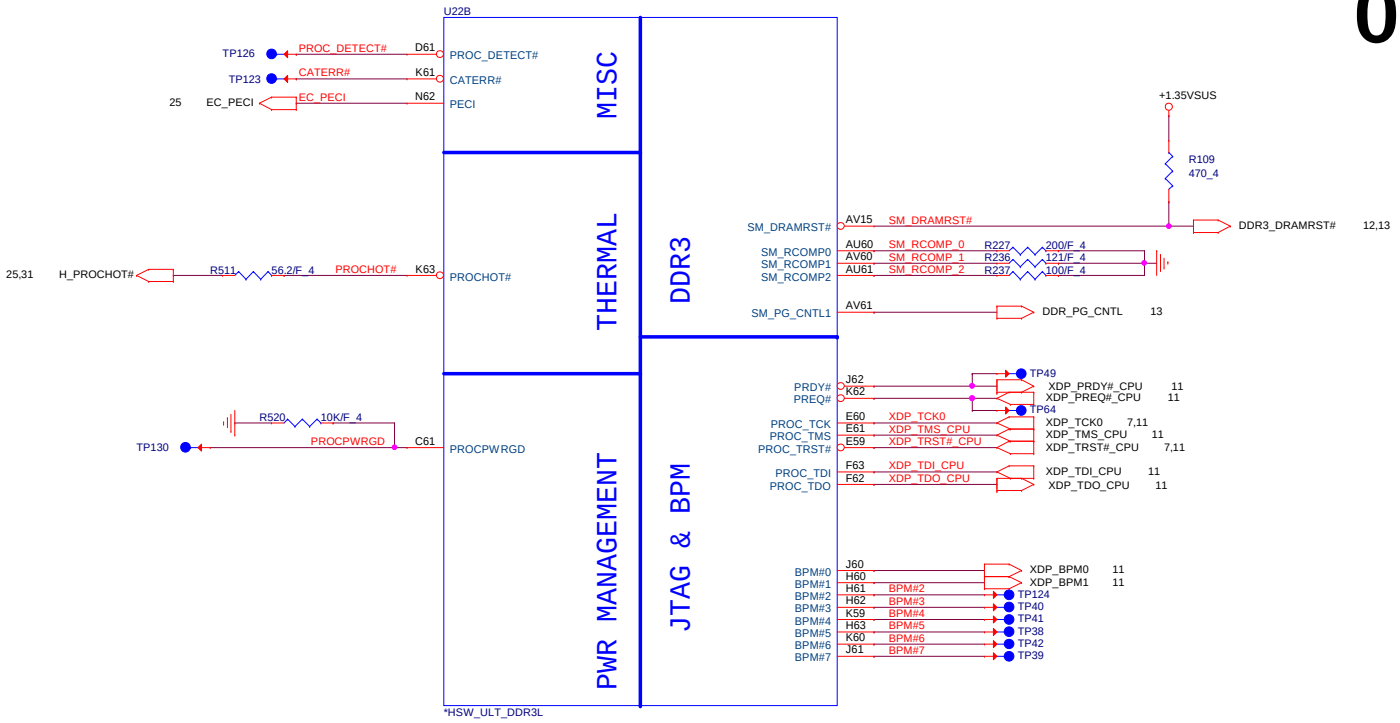
ICT



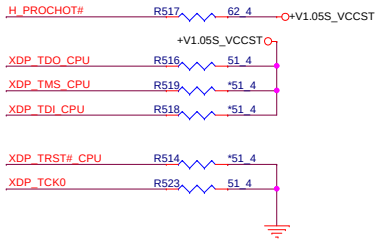
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+VCCIOA_OUT R116 24.9/F_4 eDP_RCOMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



Processor pull-up (CPU)

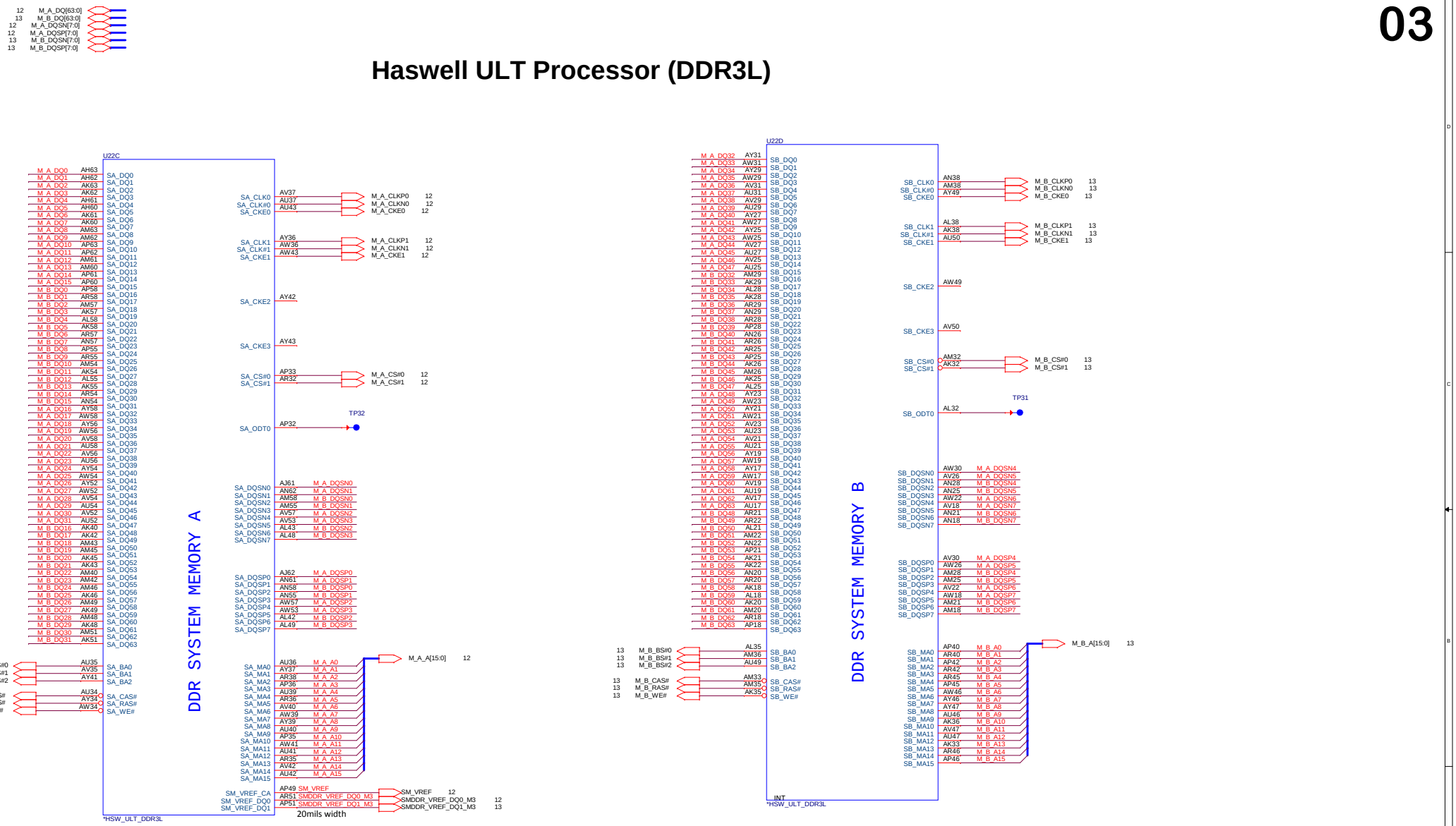


PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 1/9(eDP/DDI)	1A

Date: Monday, April 21, 2014 Sheet 2 of 32

Haswell ULT Processor (DDR3L)



PROJECT :Y61 Quanta Computer Inc.		
Size: Custom	Document Number: ULT 2/9 (DDR3 I/F)	Rev: 1A
Date: Monday, April 21, 2014	Sheet 3 of 32	

POWER

32A

+VCC_CORE

1.4A

+1.35VSUS

Close to CPU

Direct tie to CPU VCC/VSS-Ball

U22F

HSW ULT POWER

*HSW_ULT_DDR3L

U22E

RESERVED

*HSW_ULT_DDR3L

CFG0-19 need Reserve TP

Layout note: need routing together and ALERT need between CLK and DATA.

SVID ALERT

SVID CLK

SVID DATA

IO Thrm Protect

For 65 degree, 1.8v limit, (SW)

For 75 degree, 1.2v limit, (HW)

PV change to shortpad

PV reserve for RF request

100- ±1% pull-up to VCC near processor.

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R508 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R272 1K_4

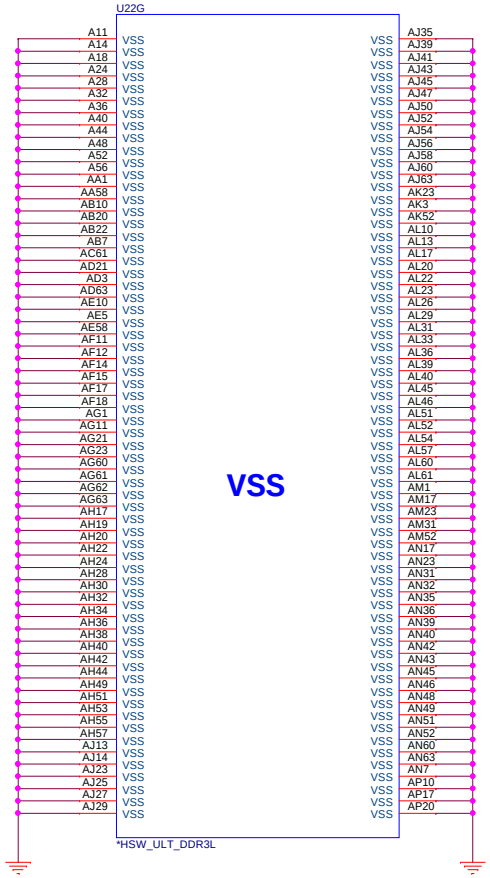
+VCCIOA_OUT 2
+VCCIO_OUT 6

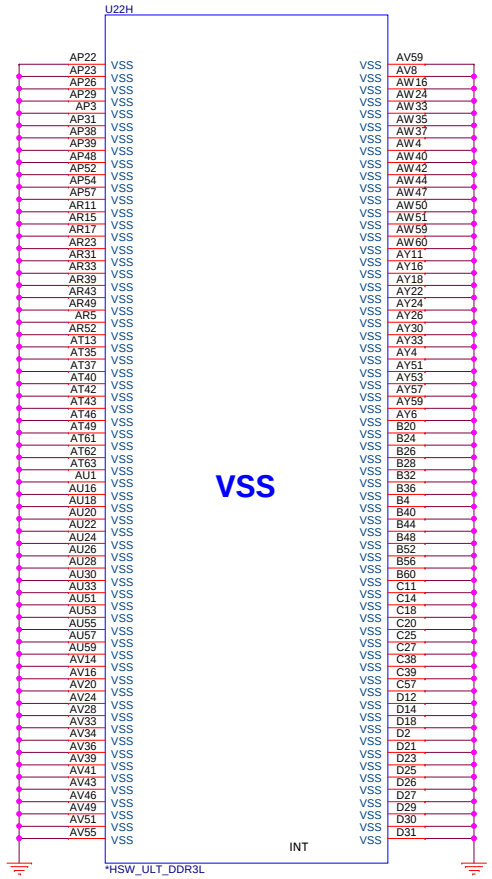
+1.35VSUS 2,12,13,29
+1.05V 7,10,11,25,30,32
+VCC_CORE 31

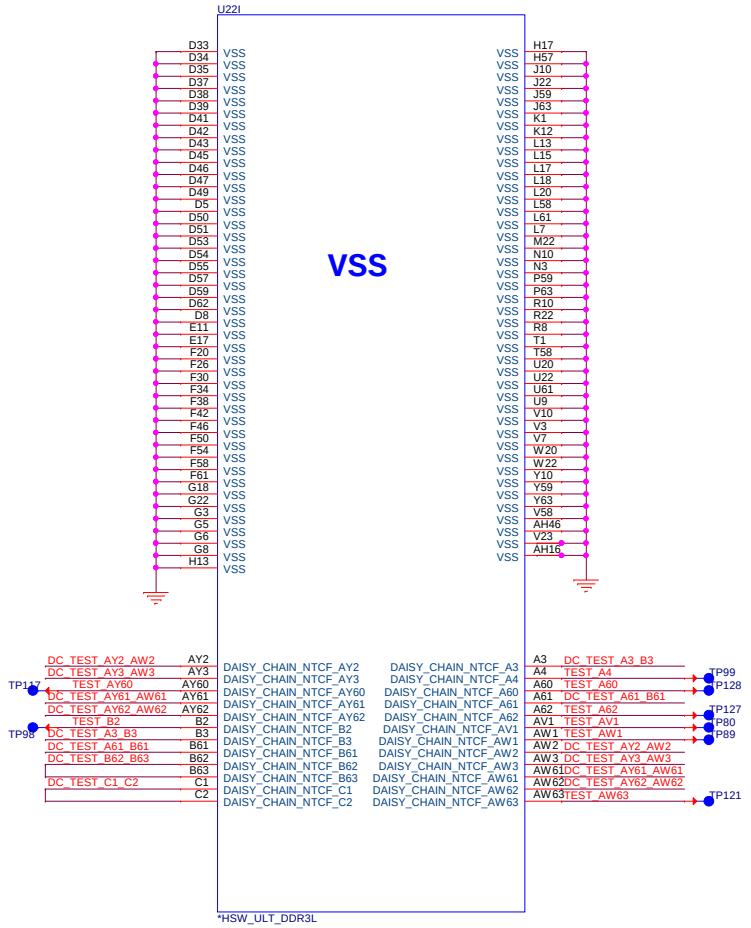
PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	04 – ULT 3/9 (POWER-1)	1A

Date: Monday, April 21, 2014 | Sheet 4 of 32



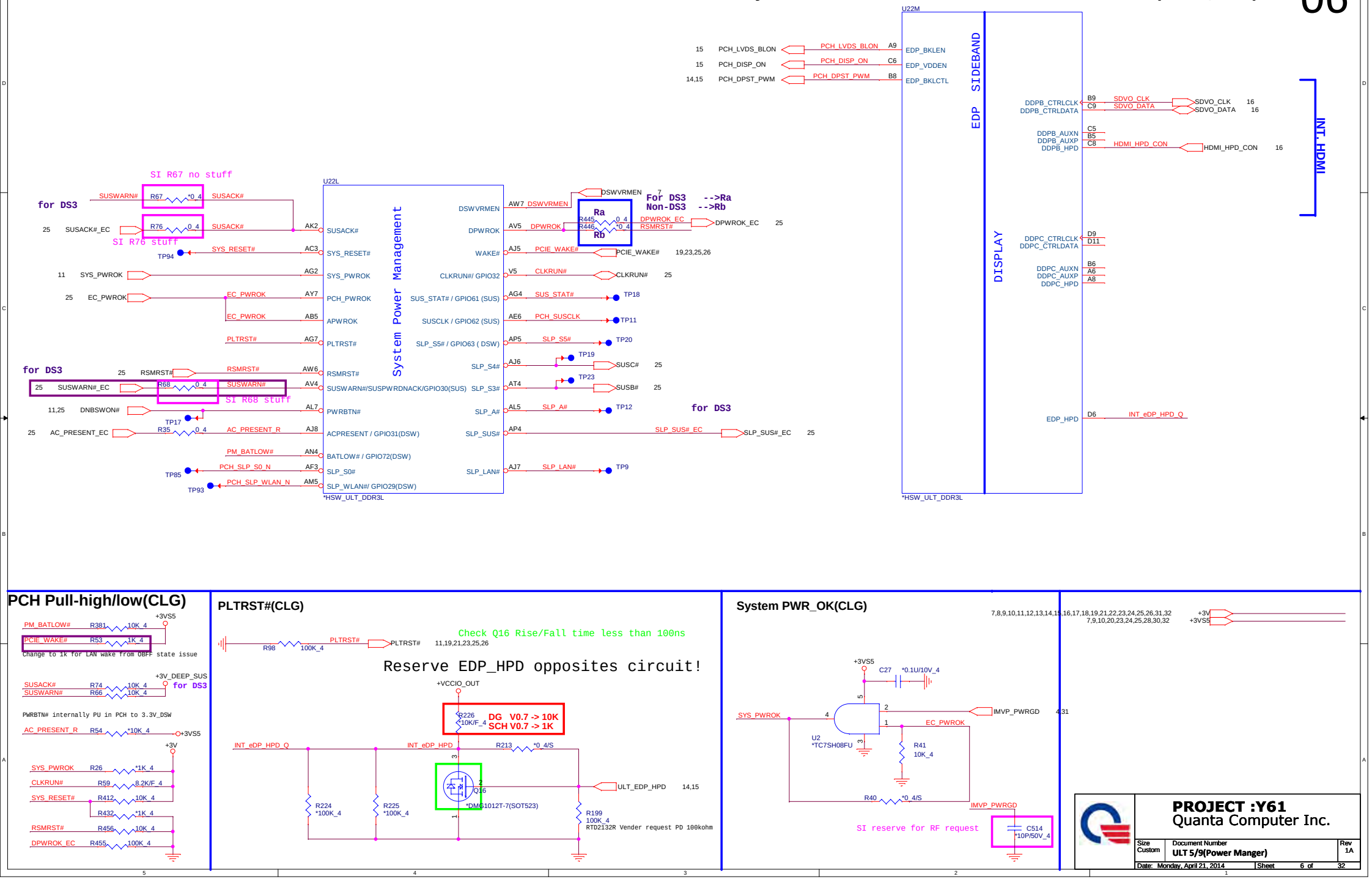




PROJECT :Y61 Quanta Computer Inc.		
Size: Custom	Document Number: ULT 4/9 (RSV,GND)	Rev: 1A
Date: Monday, April 21, 2014	Sheet 5 of 32	

Lynx Point-LP Platform Controller Hub (LVDS,DDI)

06

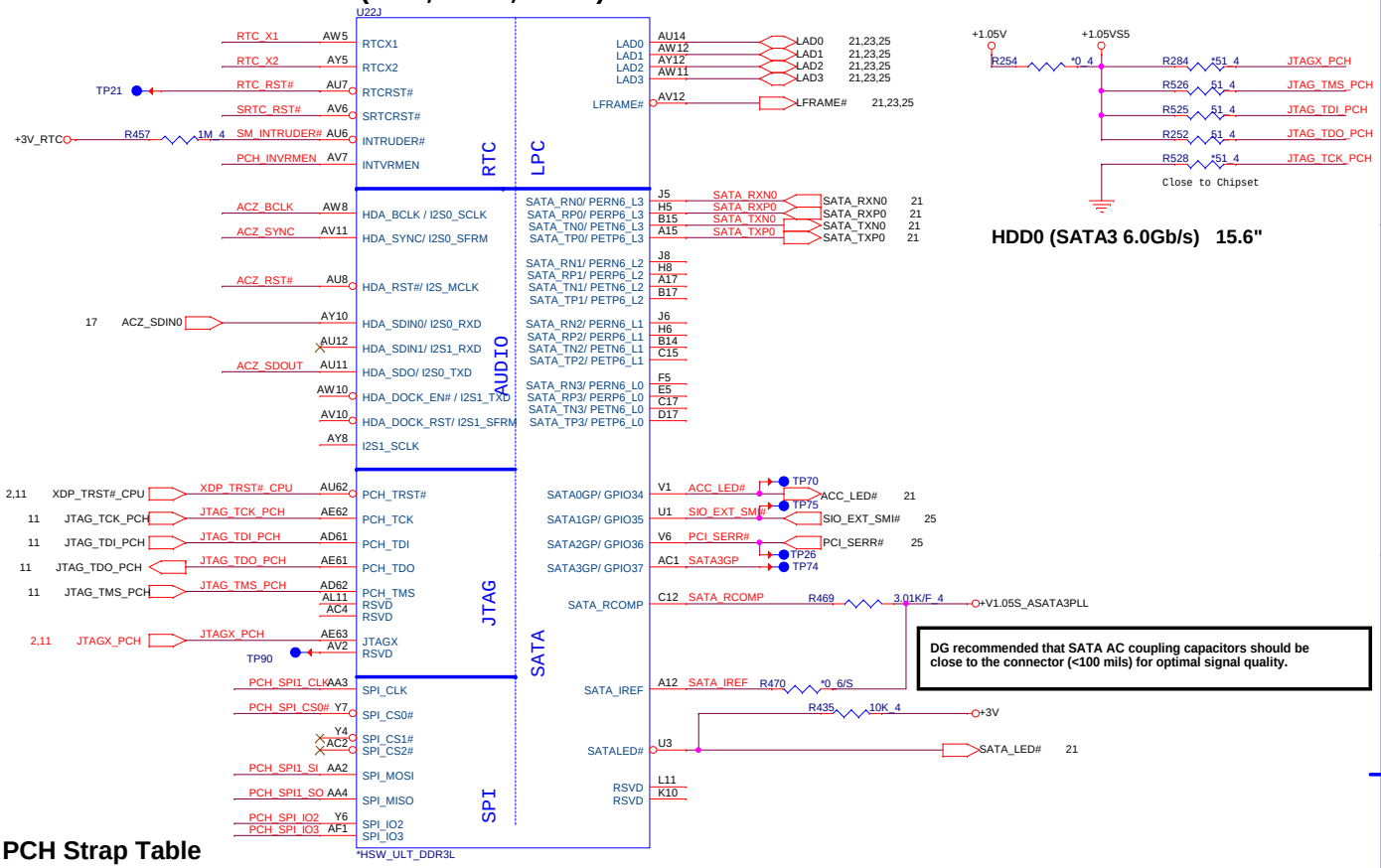


PCH Pull-high/low(CLG)

PLTRST#(CLG)

System PWR_OK(CLG)

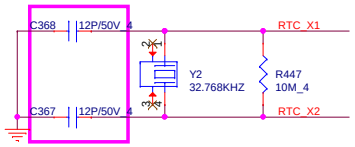
Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)



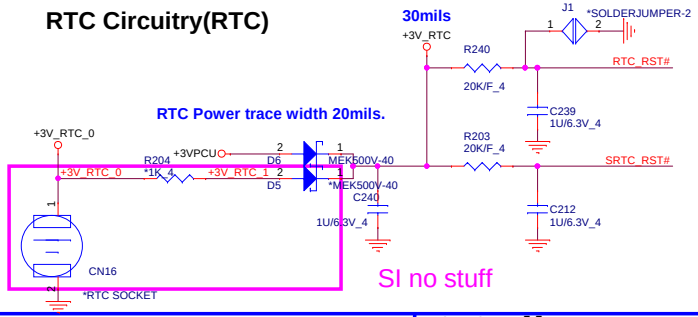
HDD0 (SATA3 6.0Gb/s) 15.6"

RTC Clock 32.768KHz

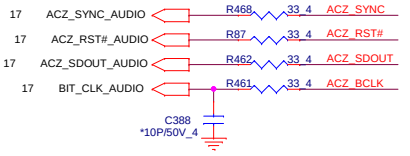
SI change to 12pF



RTC Circuitry(RTC)

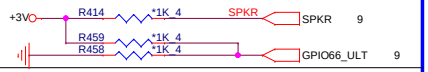
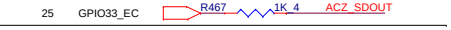
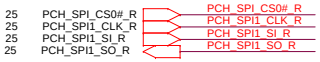


HDA Bus(CLG)



GPIO Pull UP

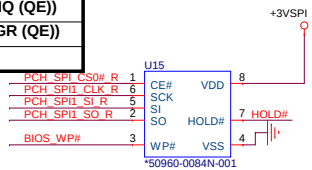
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overridden	
GSPI0_MOSI /GPIO86	Boot BIOS Selection	PWROK	GNT0# 1 = LPC; GNT0# 0 = SPI(Default)	
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality	
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	
				

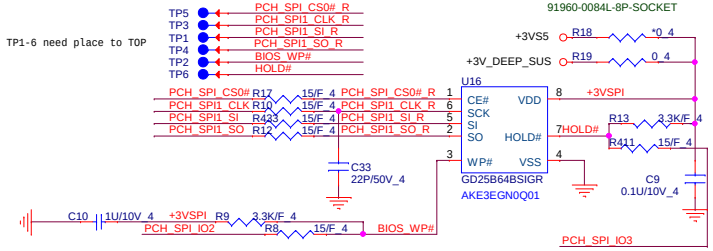
DG recommended that SATA AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP (QE))
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ (QE))
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR (QE))
Socket		DFHS08FS023

4M SPI ROM Socket



PCH SPI ROM(CLG)



+3V 6,8,9,10,11,12,13,14,15,16,17,18,19,21,22,23,24,25,26,31,32
+5V 16,17,18,21,22,23,32
+1.05V 4,10,11,25,30,32
+3VS5 6,9,10,20,23,24,25,28,30,32
+3VPCU 4,22,23,25,27,28
+3V_RTC 10,27
+V1.05S_ASATA3PLL 10

25 PCH_SPI_CS0#_R → PCH_SPI_CS0#_R
25 PCH_SPI1_CLK_R → PCH_SPI1_CLK_R
25 PCH_SPI1_SI_R → PCH_SPI1_SI_R
25 PCH_SPI1_SO_R → PCH_SPI1_SO_R

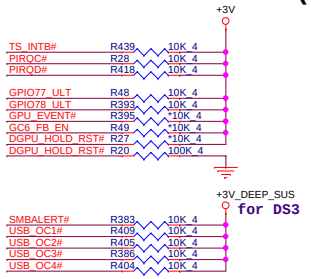
PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 6/9(SATA/HDA)	1A
Date: Monday, April 21, 2014	Sheet 7 of 32	

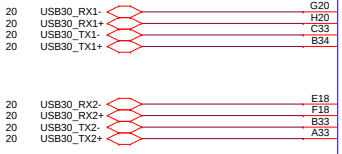
Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)

08

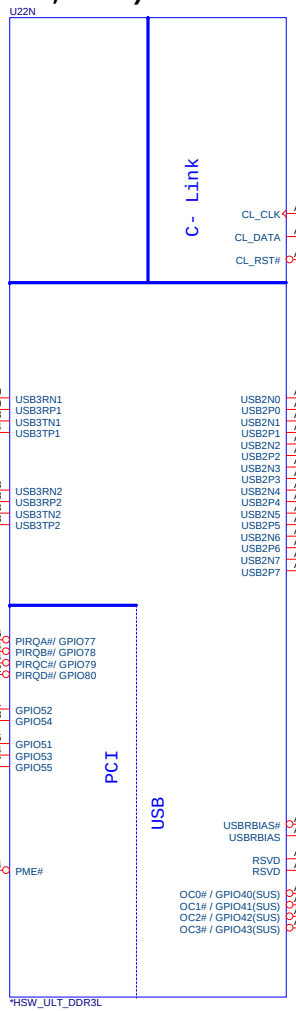
PCI/USBOC# Pull-up(CLG)



USB3.0

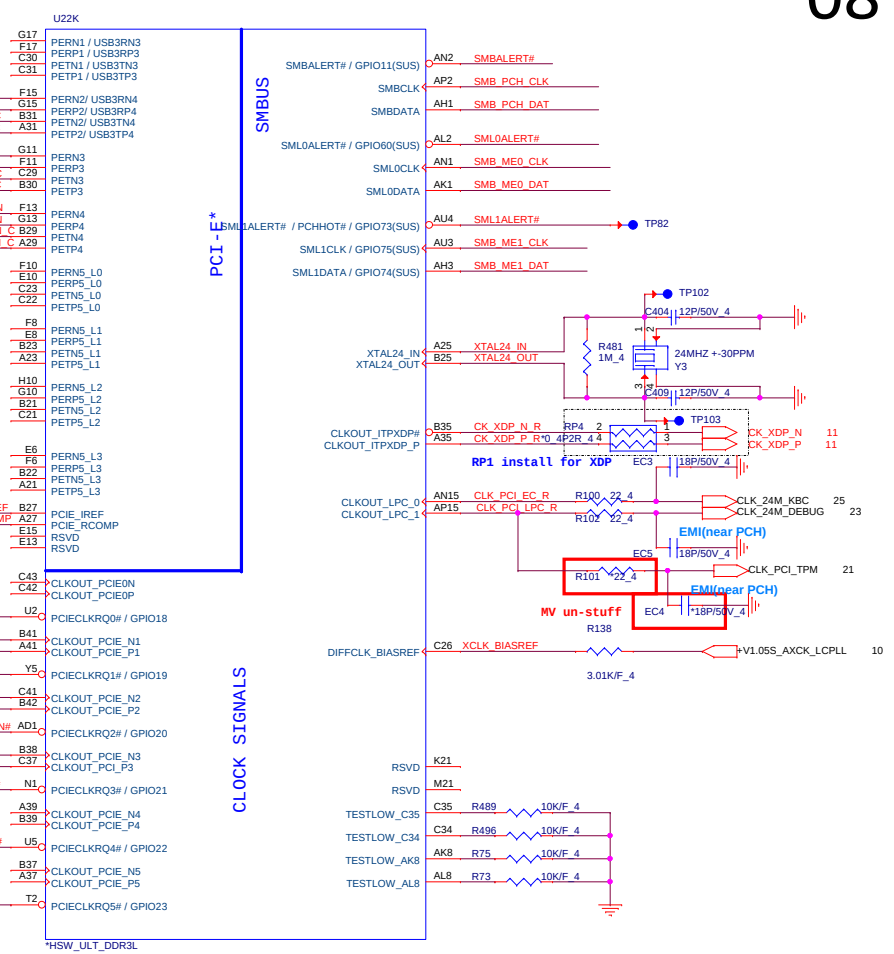


U22N



*HSW_ULT_DDR3L

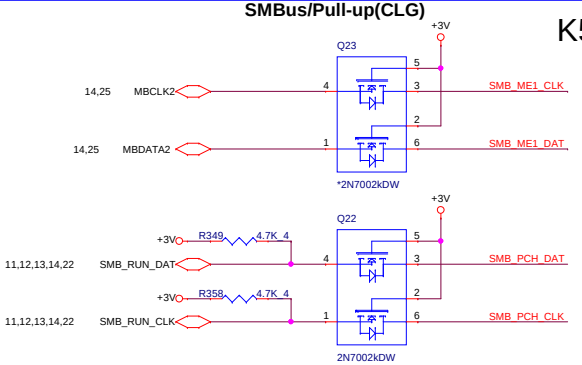
U22K



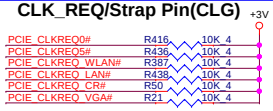
*HSW_ULT_DDR3L

SMBus/Pull-up(CLG)

K501UB

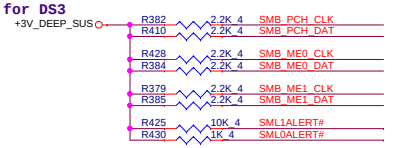


CLK_REQ/Strap Pin(CLG)



6,7,9,10,11,12,13,14,15,16,17,18,19,21,22,23,24,25,26,31,32 +3V
6,7,9,10,11 +3V_DEEP_SUS

SMBus/Pull-up(CLG)



PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 7/9 (PCIE/USB/CLK)	1A
Date: Monday, April 21, 2014	Sheet 8 of 32	

Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA) Haswell (GPIO)

09

PV change to shortpad

U22O

GPIO

SERIAL IO

CPU/MISC

*HSW_ULT_DDR3L

GPIO Pull-up/Pull-down(CLG)

+3V_DEEP_SUS

+3V

+3VS5

Close to EC

+V1.05S_VCCST

PM_THRMTRIP# R180 1K_4

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
13" clamshell wo/TS	0	0	0	0	0	1
13" convertible w/TS	0	0	0	0	1	0
15" convertible w/TS+ Giga NIC	0	0	0	0	1	1
13" clamshell w/TS (Reserve)	0	0	0	0	0	0
13" convertible wo/TS (Reserve)	0	0	0	0	0	0
15" convertible w/TS (Reserve)	0	0	0	0	0	0

R63 *10K_4 BOARD_ID0 R51 10K_4 +3V_DEEP_SUS

R427 *10K_4 BOARD_ID1 R406 10K_4

R24 10K_4 BOARD_ID2 R25 *10K_4

R39 10K_4 BOARD_ID3 R38 *10K_4

R34 10K_4 BOARD_ID4 R52 *10K_4

R61 10K_4 BOARD_ID5 R32 *10K_4

6,7,8,10,11,12,13,14,15,16,17,18,19,21,22,23,24,25,26,31,32 +3V

6,7,10,20,23,24,25,28,30,32 +3VS5

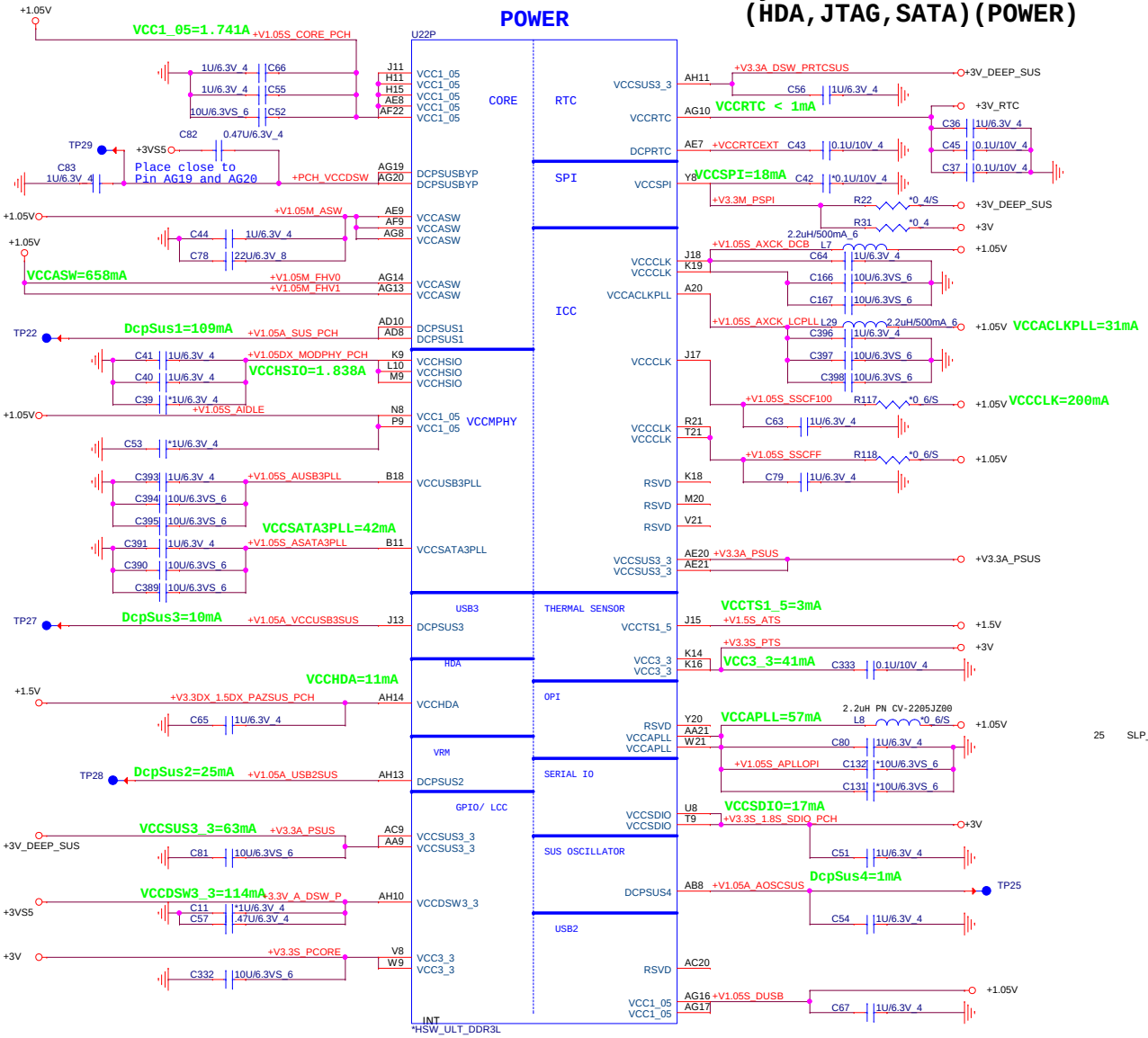
PROJECT :Y61
Quanta Computer Inc.

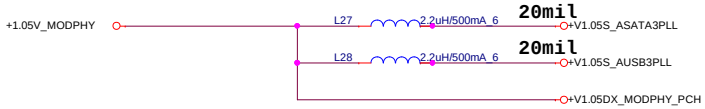
Size	Document Number	Rev
Custom	ULT 8/9 (GPIO/MISC)	1A

Date: Monday, April 21, 2014 Sheet 9 of 32

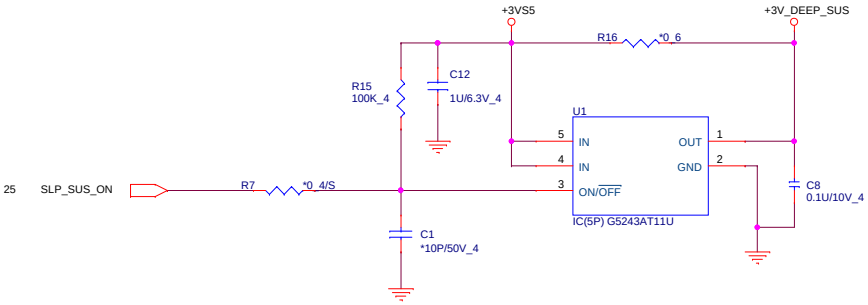
Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)(POWER)

POWER





for DS3

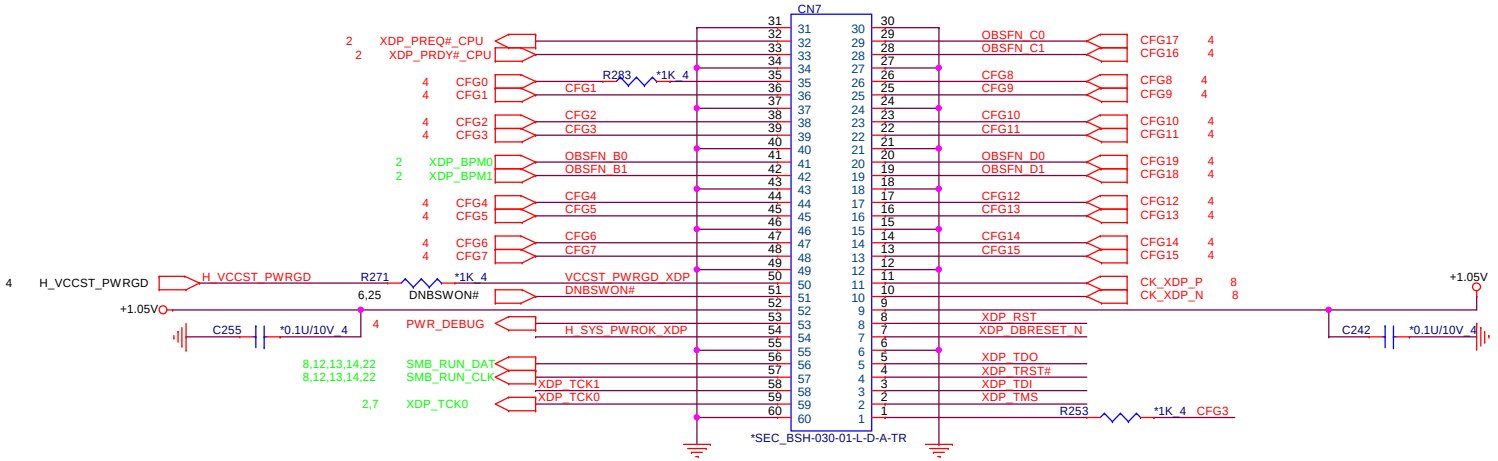


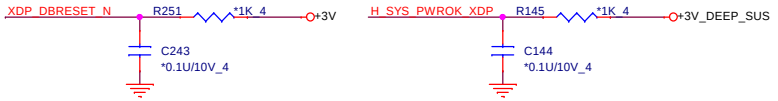
6,7,8,9,11,12,13,14,15,16,17,18,19,21,22,23,24,25,26,31,32	+3V
16,17,18,21,22,23,32	+5V
4,7,11,25,30,32	+1.05V
6,7,9,20,23,24,25,28,30,32	+3VS5
13,18,20,28,29,30,31,32	+5VS5
8	+V1.05S_AUSB3PLL
7	+V1.05S_ASATA3PLL
8	+V1.05S_AXCK_LCPLL
7,27	+3V_RTC
2,4,12,13,29	+1.35VSUS

PROJECT :Y61
Quanta Computer Inc.

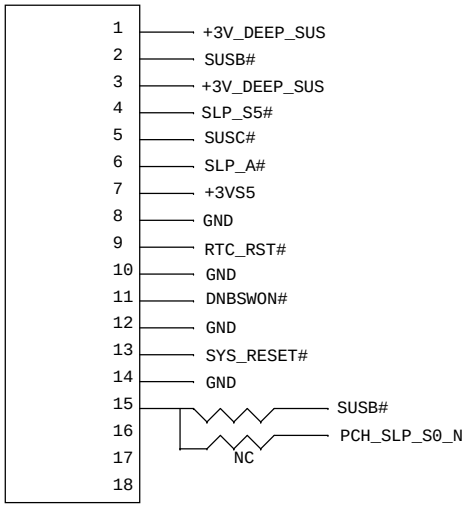
Size	Document Number	Rev
Custom	ULT 9/9(POWER-2)	1A

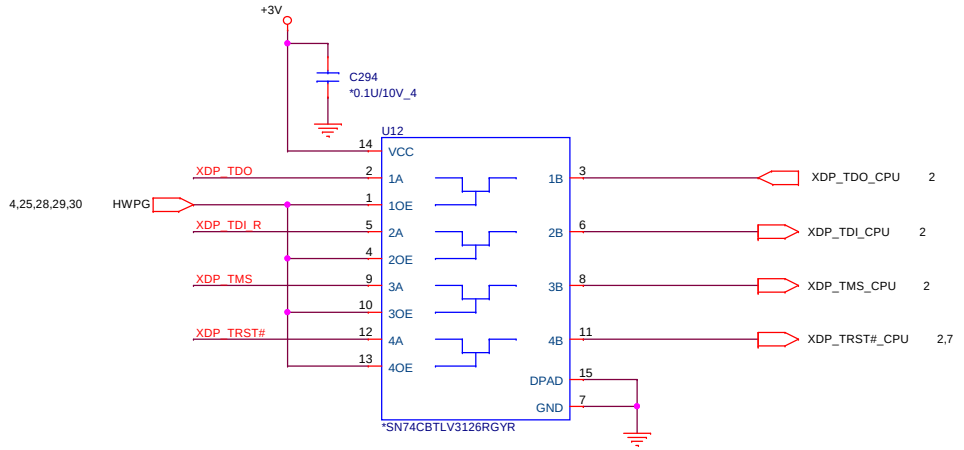
Date: Monday, April 21, 2014 Sheet 10of 32

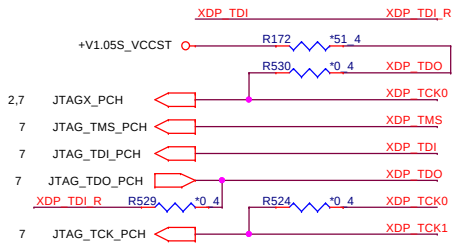


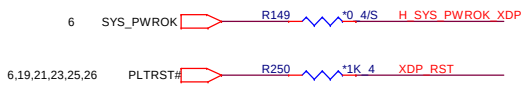


APS





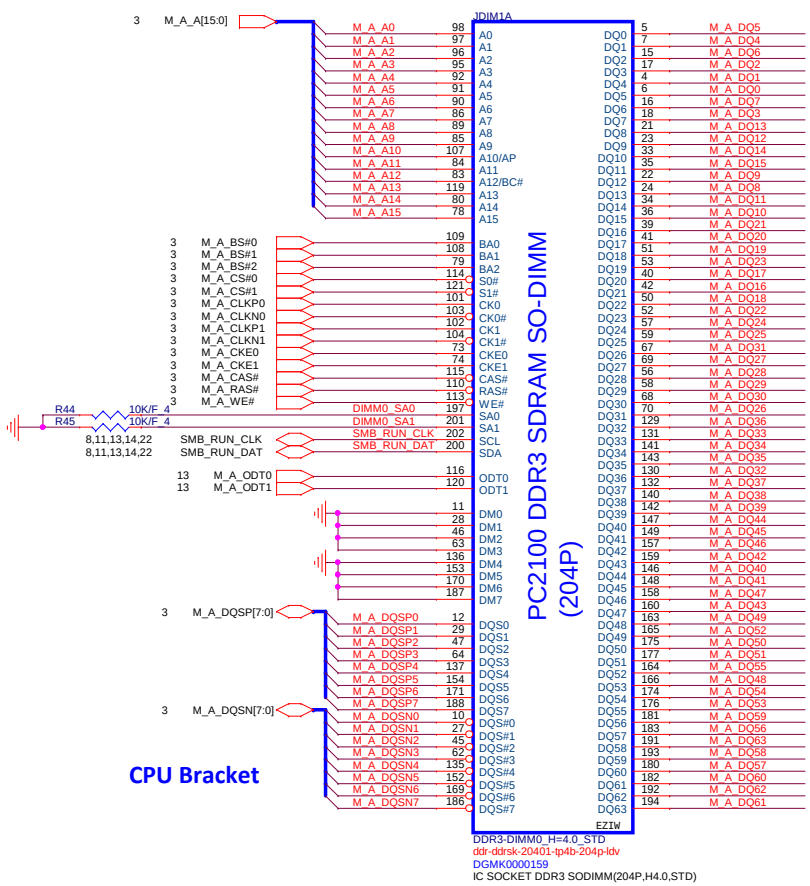


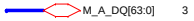


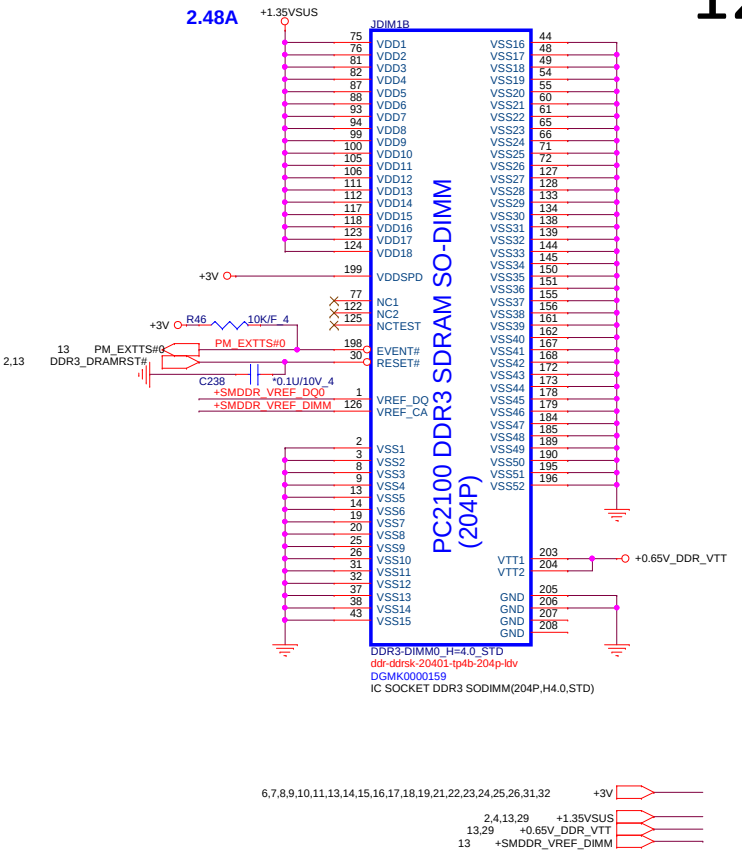
PROJECT :Y61
Quanta Computer Inc.
ULT

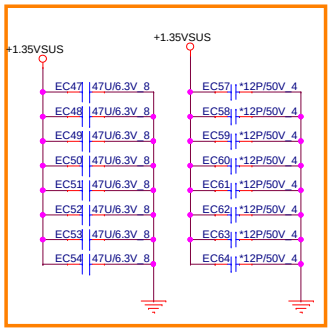
Size	Document Number	Rev
	HSW XDP & APS	1A

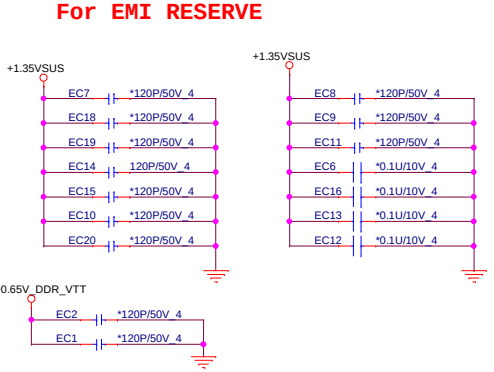
Date: Monday, April 21, 2014 | Sheet 11 of 32

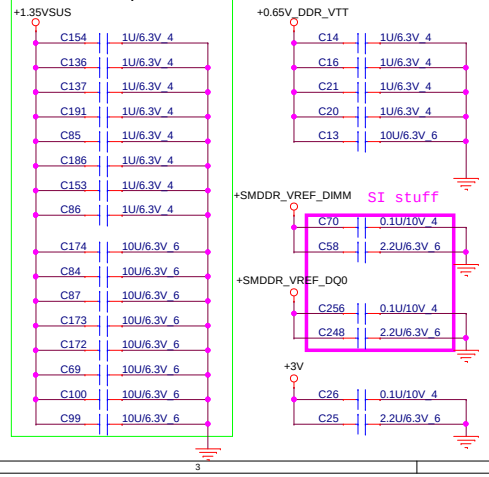


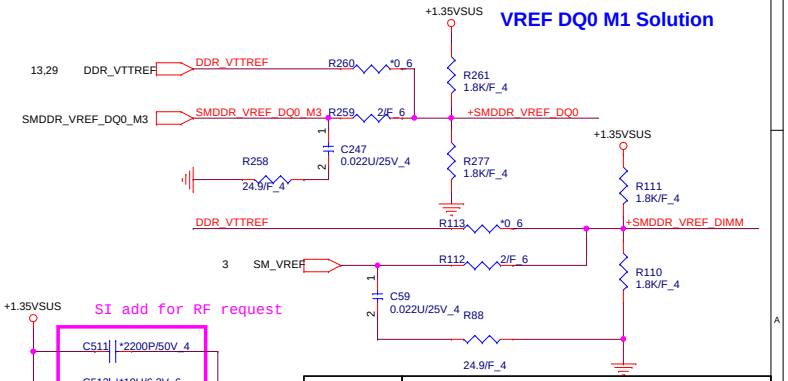






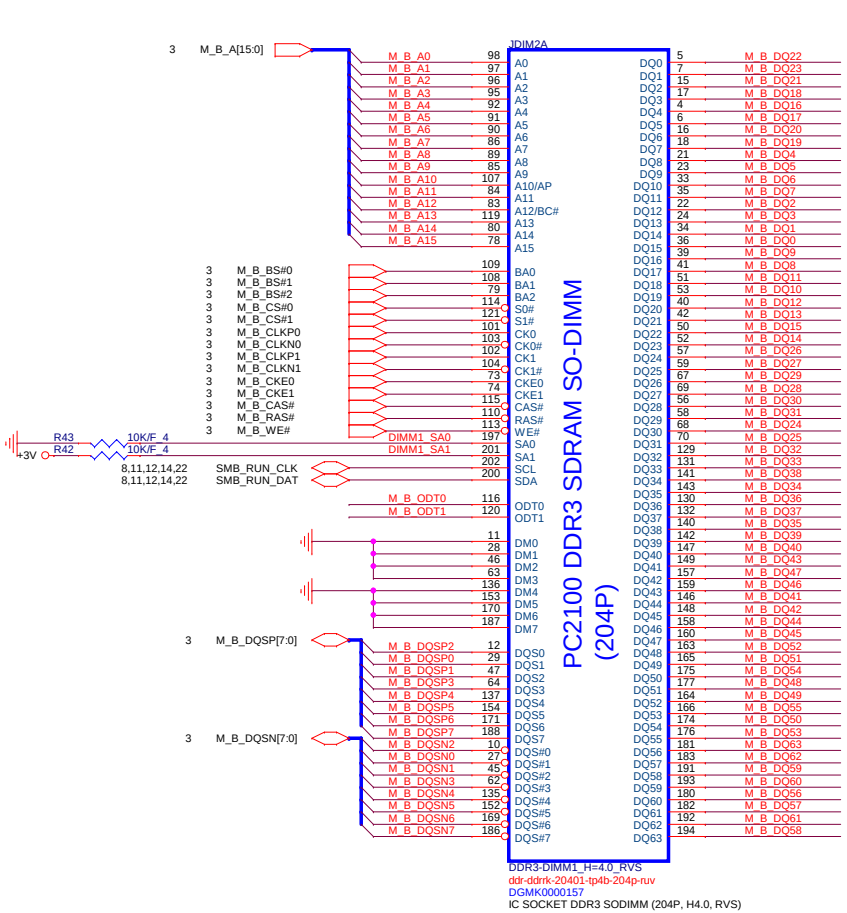


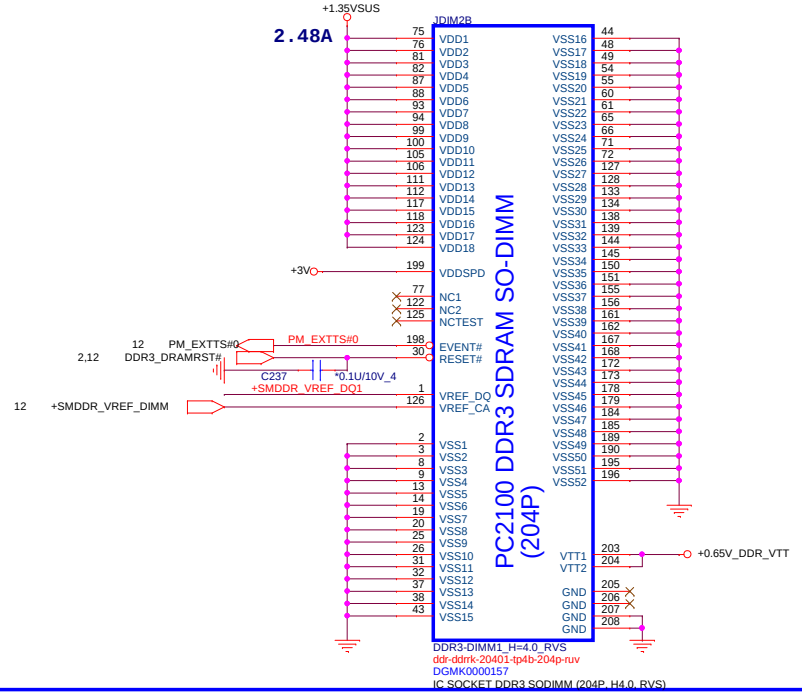


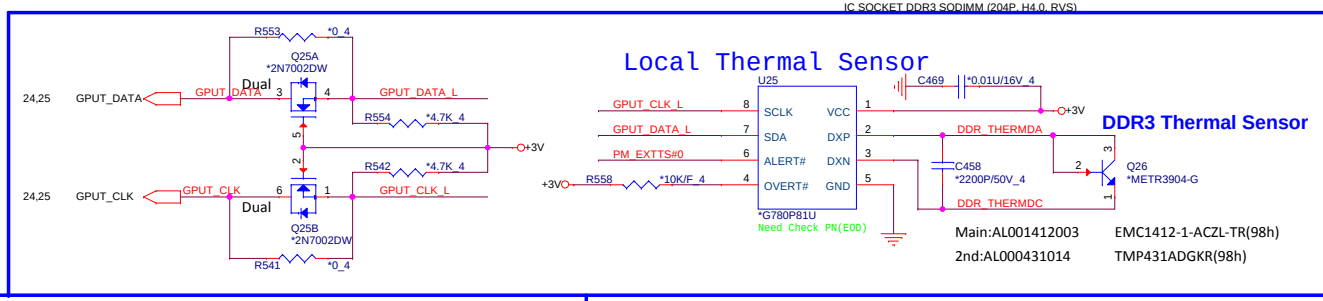


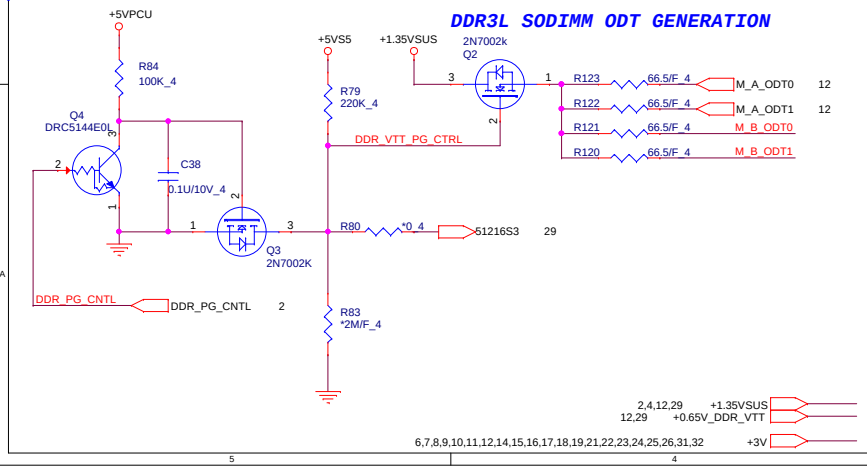
PROJECT :Y61
Quanta Computer Inc.

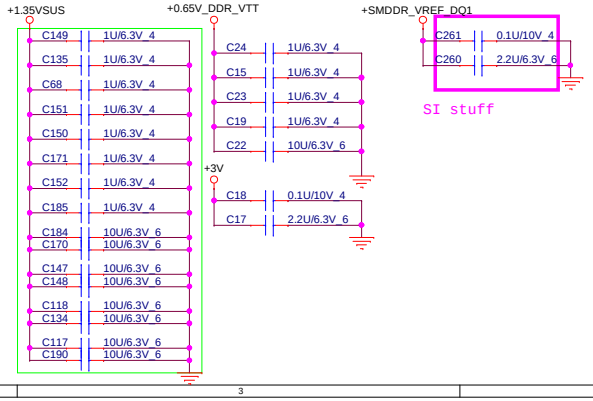
Size	Document Number	Rev
Custom	DDR3 DIMM0-STD(4.0H)	1A
Date: Monday, April 21, 2014	Sheet 12of 32	

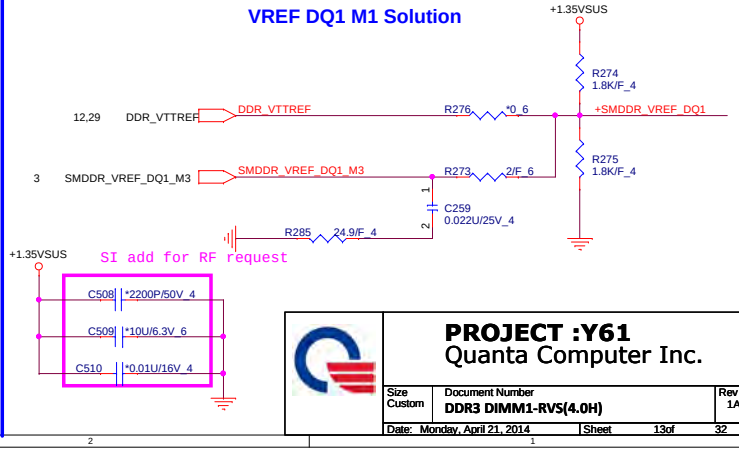










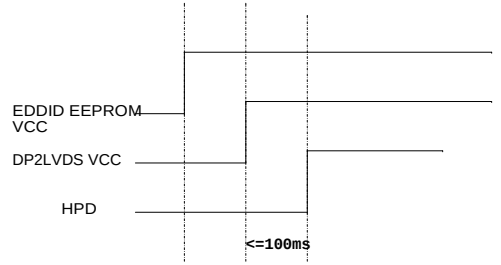


PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS(4.0H)	1A
Date: Monday, April 21, 2014	Sheet 13of 32	

RTD2136 Dual Channel only

RTD2136S Power Up Sequence 14



Reserve for co layout EDP CON, EDP only please stuff

Pine 18: keep 80 Mile Trace

RTD2136N

Reserve

PV Add TP

PV remove EEPROM

For EDP: unstuff Ra

Default PV change to shortpad

RTD2136R
R376;R365: NA
R375;R374: Stuff

keep 80 Mile Trace

L10: need use CV-4709MN00 for Vendor suggestion

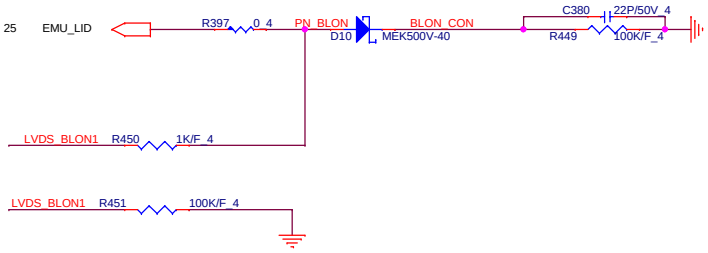
SWR MODE	LDO MODE
Stuff L22	Stuff R372

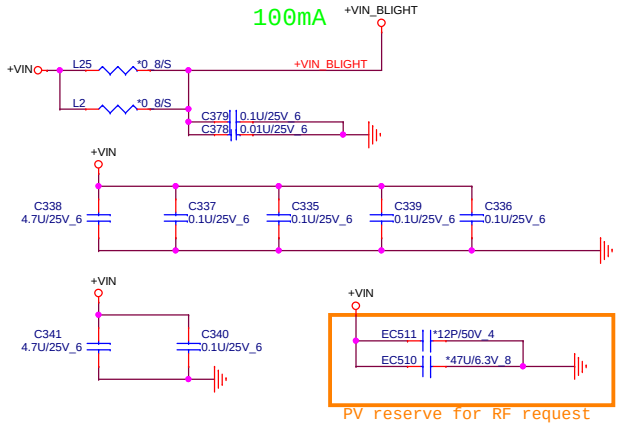
PROJECT :Y61
Quanta Computer Inc.

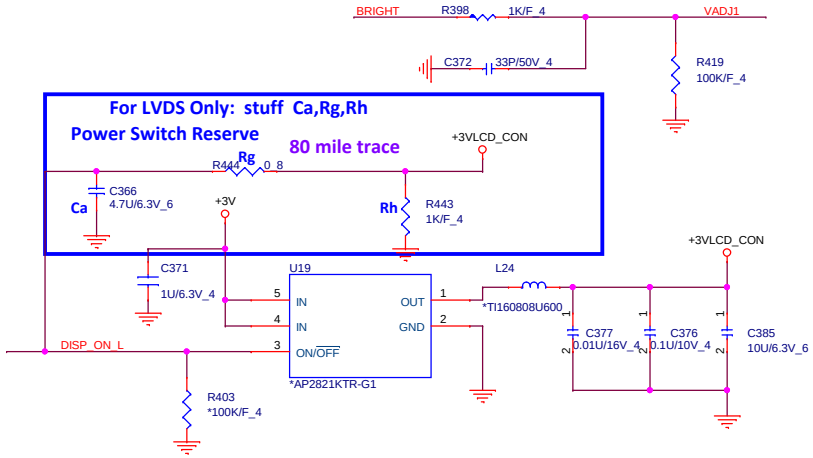
Size	Document Number	Rev
Custom	RTD2136	1A

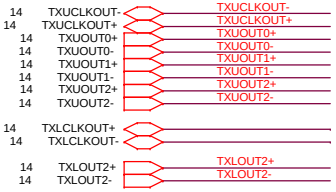
Date: Monday, April 21, 2014 Sheet 14 of 32

LID Switch



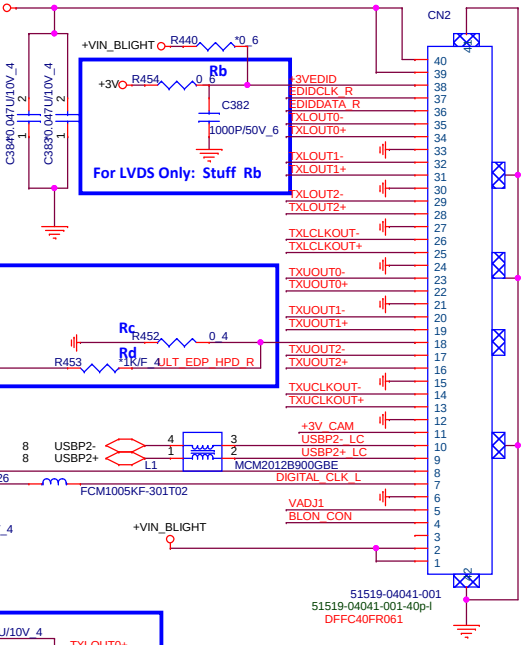


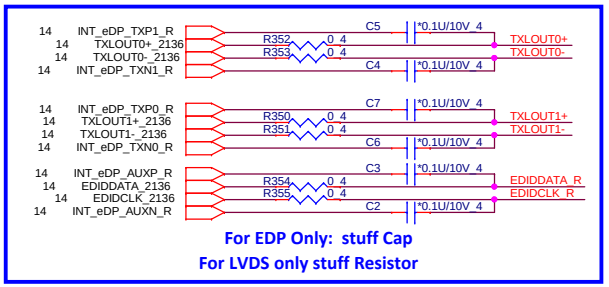


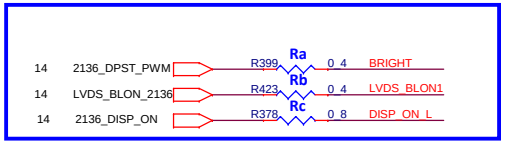


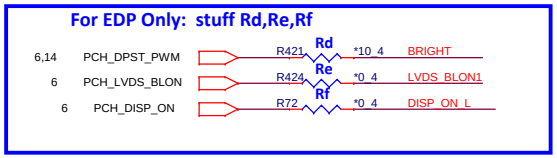
LVDS Conn.

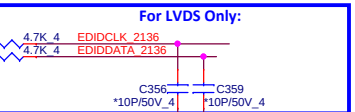
15

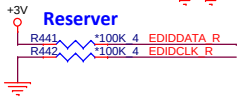


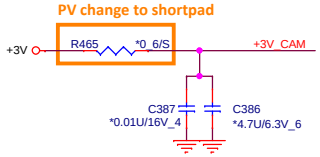


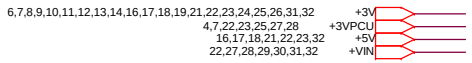








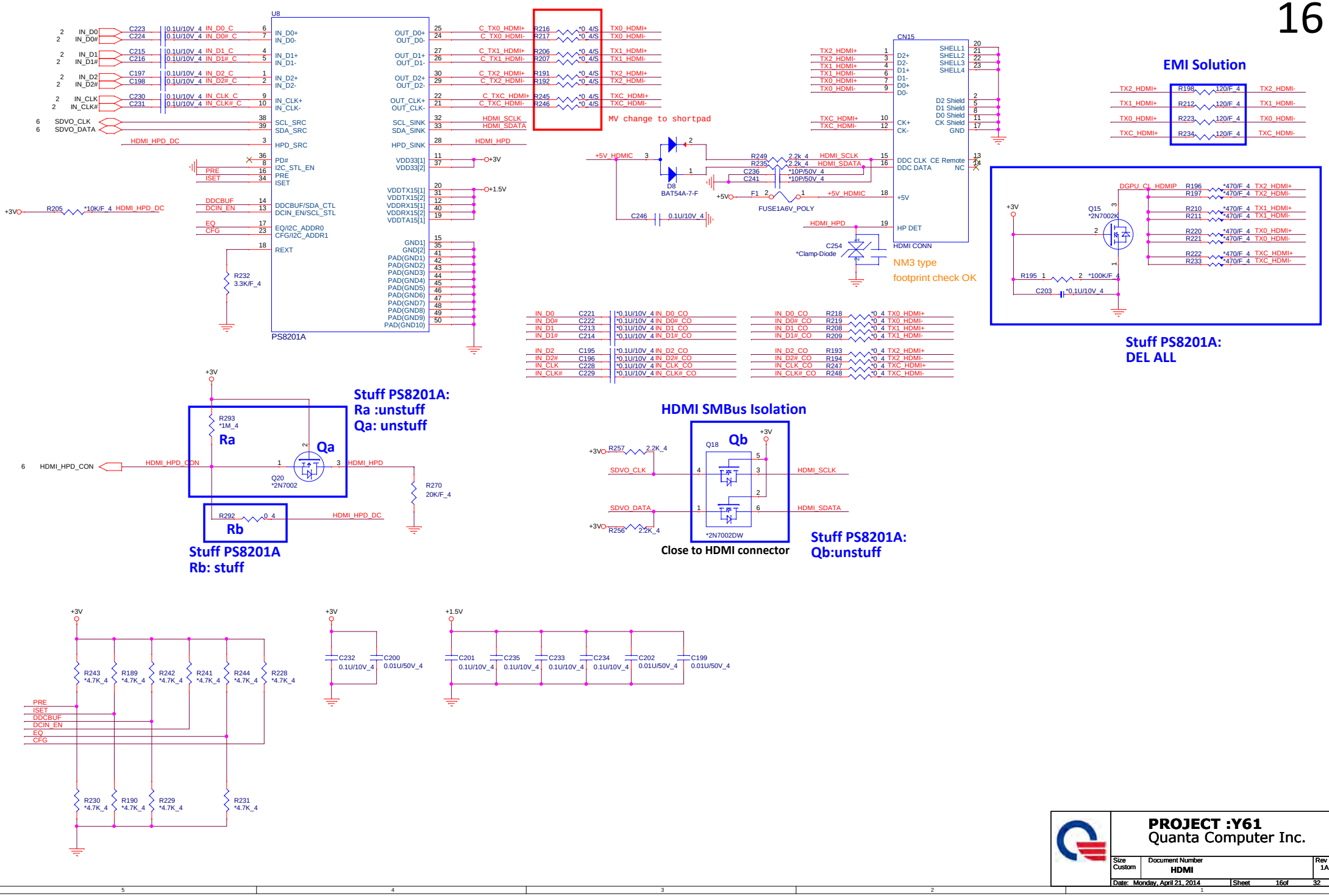




PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A

Date: Monday, April 21, 2014 Sheet 15 of 32


U8
PS8201A
MV change to shortpad
CN15
HDMI CONN
NM3 type
footprint check OK
EMI Solution
Stuff PS8201A:
DEL ALL
Stuff PS8201A:
Ra :unstuff
Qa: unstuff
Stuff PS8201A
Rb: stuff
HDMI SMBus Isolation
Qb
Close to HDMI connector
Stuff PS8201A:
Qb:unstuff
PROJECT :Y61
Quanta Computer Inc.
HDMI
Monday, April 21, 2014
16of 32

Close to PIN1

>40mils trace

Close to PIN26

Close to PIN40

Close to PIN27,39

Close to PIN28

Close to PIN7

Close to Pin 9

Close to Pin 34,35,36

Close to Pin 41

Close to Pin 46

Close to codec

Speaker 4 ohm: 40mils

Layout concern

Close to codec

Close to CODEC

place to near U10013 or under U10013

check value

Check layout mount location

TO Audio Jack MIC

TO Internal Speakers

for intel HSW ULT

PV change to shortpad

PV change from 0R for EMI solution

PV add for EMI solution

Digital MIC

U27

ALC3227 x QFN48

Analog

Digital

Vset=1.242V

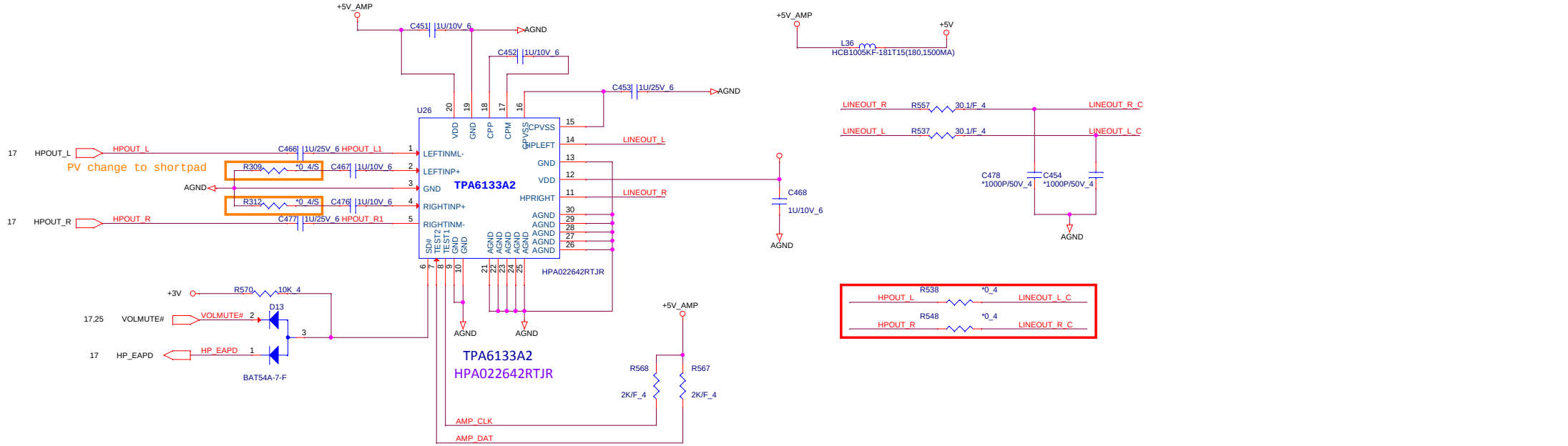
FOR EMI

PROJECT :Y61
Quanta Computer Inc.

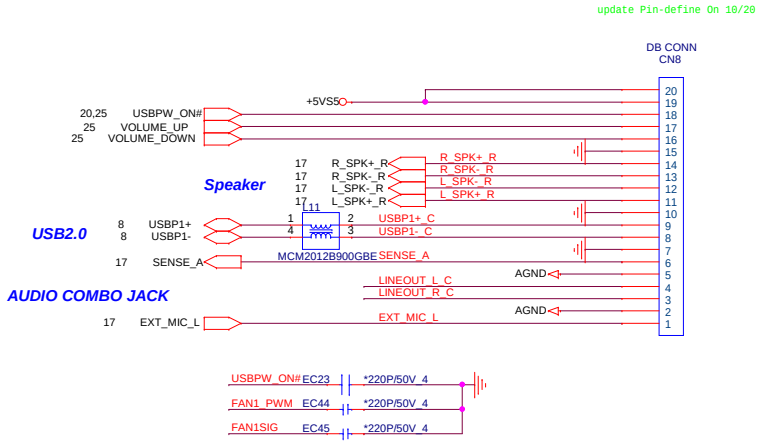
Size	Document Number	Rev
Custom	Azalia ALC 3227	1A

Date: Monday, April 21, 2014 Sheet 17 of 32

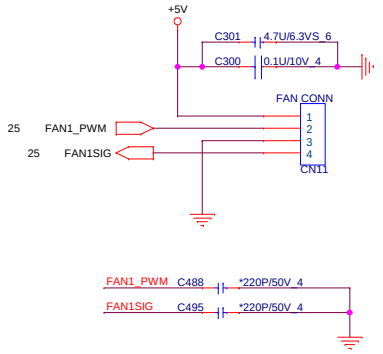
Head Phone out



Audio Board



FAN



6,7,8,9,10,11,12,13,14,15,16,17,19,21,22,23,24,25,26,31,32 +3V
16,17,21,22,23,32 +5V
13,20,28,29,30,31,32 +5VS5

PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Audio/AMP HPA022642RTJR	1A
Date: Monday, April 21, 2014	Sheet 18 of 32	

For EMI 0 ~ 22 ohm

LAN_XTAL1 — R165 10/F_4 — XTAL1

Y1 25MHZ +-10PPM

C176 10P/50V_4

C177 10P/50V_4

XTAL2

Trace<30 mil
Width > 60 mil

Power trace Layout 寬度> 60mil

>60mil

+1.05V_LAN_REGOUT — 4.7UH,+-20%,650MA_1210 La L30 — >60mil

R162 *0_8

Cb C125 4.7U/6.3V_6

Ca C126 0.1U/10V_4

Close to Choke La

SWR mode need stuff Ca & Cb

For GbE
* Place Cc,Cd,Ce,Cf close to each VDD10 pin-- 3, 8, 22, 30
For 10/100
* Place Cc , Cd close to each VDD10 pin-- 8, 30 only,

Cc C406 0.1U/10V_4

Cd C156 0.1U/10V_4

Ce C411 0.1U/10V_4

Cf C157 0.1U/10V_4

+1.05V_LAN

Cg C158 *1U/6.3V_4

C128 0.1U/10V_4

C399 1U/6.3V_4 Cf

C127 *0.1U/10V_4

Place Cg & C621 close to each VDD10 pin22

*RTL8166EH Cg & C621 close pin30

For GbE
* Place Cg close to each VDD10 pin-- 22 (reserve)

+1.05V_LAN

R486 2.49K/F_4 LANRSET

+3V_LAN

LAN_AMBLED# — TP34

R164 Ra 0_4 LAN_WLED#

R163 Rb *0_4

LED1:
FOR GIGA 8161: Stuff Ra, DEL Rb
FOR 10/100 8176: Stuff Rb,DEL Ra

U6

Please add 9 GND VIAs connection with thermal PAD

RTL8176EH

RTL8176EH-CG

MDI0+ MDI0- VDD10 MDI1+ MDI1- MDI2+ MDI2- VDD10

MDIP0 MDIN0 AVDD10(NC) MDIP1 MDIN1 MDIP2(NC) MDIN2(NC) AVDD10

REGOUT(NC) VDDREG(VDD33) DVDD10(NC) LANWAKEB ISOLATEB PERSTB HSON HSOP

+1.05V_LAN_REGOUT +3V_LAN +1.05V_LAN PCIE_WAKE# ISOLATEB

PCIE_RXN4_LAN_L PCIE_RXP4_LAN_L — C108 0.1U/10V_4 — C109 0.1U/10V_4

PLTRST# 6,11,21,23,25,26
PCIE_RXN4_LAN 8
PCIE_RXP4_LAN 8

FOR GIGA: 8161GSH: AL008161004

FOR 10/100: 8176EH: AL008176000

MDI3+ MDI3-

CLK_PCIE_LANN CLK_PCIE_LANP PCIE_TXN4_LAN PCIE_TXP4_LAN

CLK_PCIE_LANN 8
CLK_PCIE_LANP 8
PCIE_TXN4_LAN 8
PCIE_TXP4_LAN 8

+3V_LAN

8 PCIE_CLKREQ_LAN# — PCIE_CLKREQ_LAN# R134 *0_4/S — LAN_CLKRQ

+3V

R478 1K_4

ISOLATEB

R482 15K/F_4

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

10/100 only

U20

MDI1-_1 MDI1+_1 LAN_MCT2 MDI0-_1 MDI0+_1 LAN_MCT1

TD+ TD- CT RD+ RD- CT

TX+ CMT TX- RX- CT RX+

MDI1- V_DAC MDI1+ MDI0+ V_DAC MDI0-

*NS681684

For 10/100
* Stuff Ca and Ce only, close to each VDD33 pin-- 23, 32
For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32

BOT: TST1284R LF DB0EL5LAN00

+3V_LAN

+3VLANVCC

Reserve for Reltek FAE request.

C93 0.1U/10V_4 Ca

C159 0.1U/10V_4 Cb

C140 *0.1U/10V_4 Ce

C412 *4.7U/6.3V_6

C94 *4.7U/6.3V_6

close to each VDD33 pin-- 11, 32

Place Cc and Cd close to each VDD33 pin-- 23

C160 4.7U/6.3V_6 Cc

C413 0.1U/10V_4 Cd

For GIGA :
Stuff Cc ,Cd
For 10/100:
NA: Cc, Cd

Remove For Not Using SWR mode

6,7,8,9,10,11,12,13,14,15,16,17,18,21,22,23,24,25,26,31,32 — 32 — +3V +3VLANVCC

For 10/100
* Place Cf close to each VDD10 pin-- 30 (reserve)

U21

MDI2+ MDI2- MDI3- MDI3+ MDI0+ MDI0- MDI1+ MDI1-

TD1+ TD1- TD2+ TD2- TD3+ TD3- TD4+ TD4-

MX1+ MX1- MX2+ MX2- MX3+ MX3- MX4+ MX4-

MDI2+_1 MDI2-_1 MDI3-_1 MDI3+_1 MDI0+_1 MDI0-_1 MDI1+_1 MDI1-_1

V_DAC V_DAC V_DAC V_DAC

TCT1 TCT2 TCT3 TCT4

MCT1 MCT2 MCT3 MCT4

LAN_MCT1 75_4 R158
LAN_MCT2 75_4 R136
LAN_MCT3 75_4 R159
LAN_MCT4 75_4 R143

C95 0.01U/25V_4

NS892407

C392 10P/3KV_1808

For GiGA
BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00

For 10/100
BOT: TST1284R LF DB0EL5LAN00

LAN conn

RJ45 CN14

LAN_AMBLED LAN_AMBLED# (Amber)

LED_AMBER_P LED_AMBER_N

MDI3- MDI3+ MDI1- MDI2+ MDI1+ MDI0- MDI0+

RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+

GND1 GND

LAN_WLED LAN_WLED# (White)

LED_WHITE_P LED_WHITE_N

RJ45_CONN

R466 *0_6/S

R490 *0_6/S

SI change footprint to rj45-2rj3060-128111f-12p

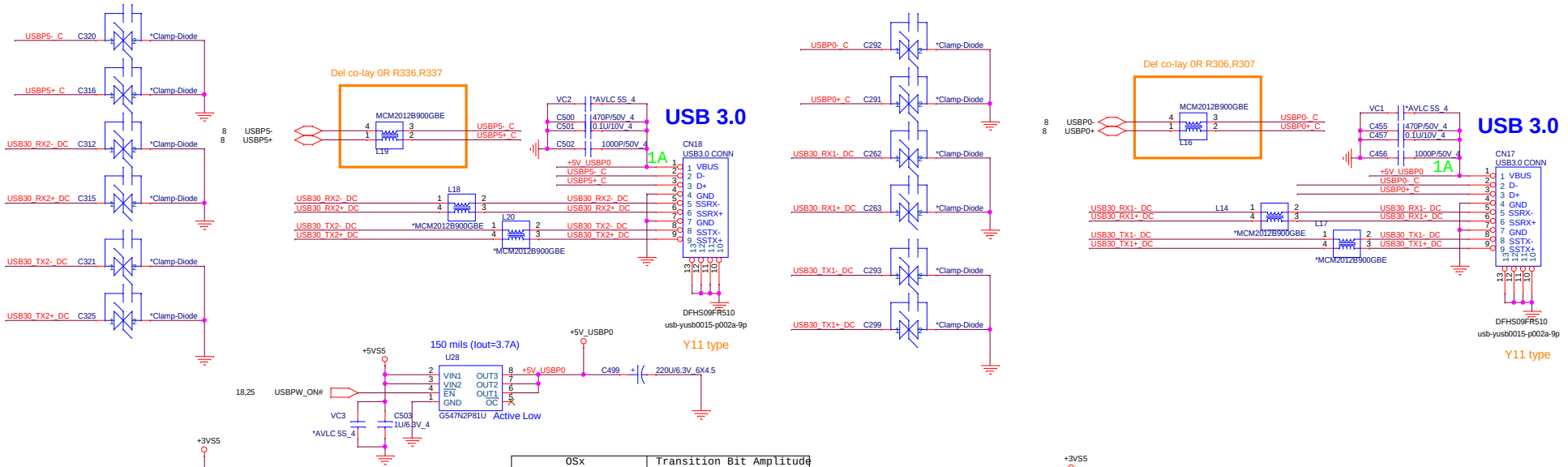
+3VLANVCC — R115 330_4 — C77 1000P/50V_4 — LAN_AMBLED

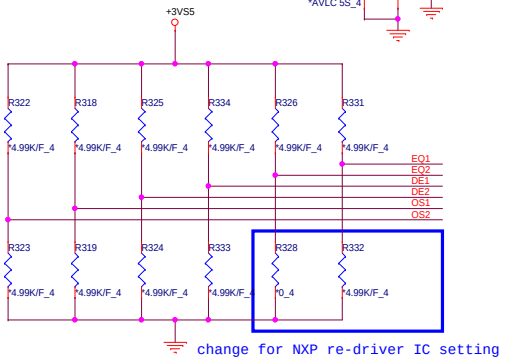
+3VLANVCC — R166 330_4 — LAN_WLED — C161 1000P/50V_4

PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL 8161/RJ45	1A
Date: Monday, April 21, 2014	Sheet 19 of 32	

USB 2.0/3.0 Combo





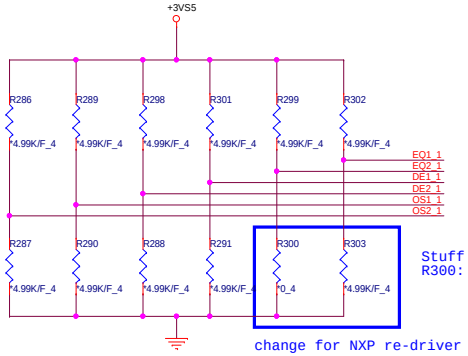
OSx	Transition Bit Amplitude
NC(default)	1000
0	870
1	1085

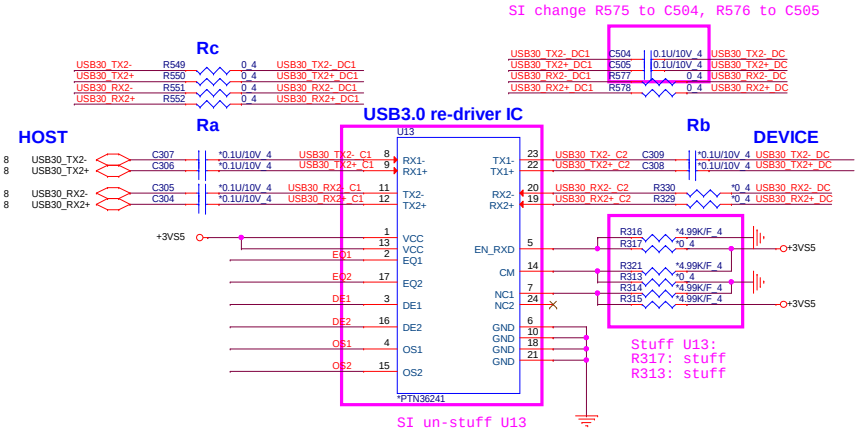
EQx	Equalization dB
NC(default)	0
0	7
1	15

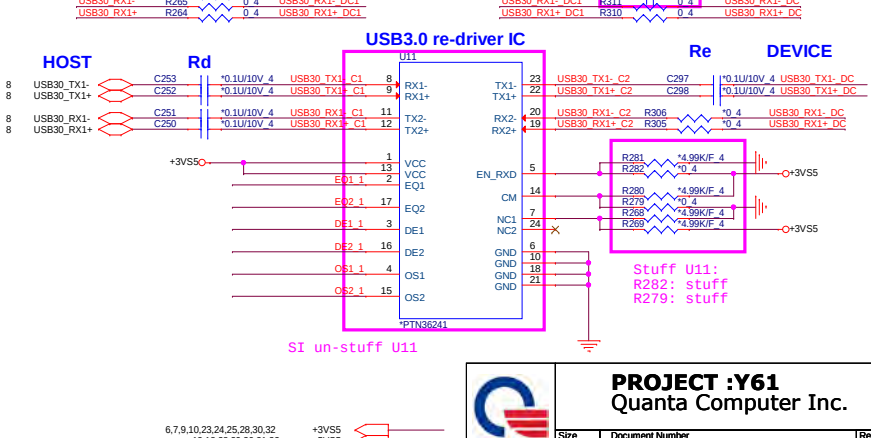
DEx	OSx=NC	OSx=0	OSx=1
NC	-3.5dB	-2.2dB	-4.4dB
0	-6.0dB	-5.2dB	-6.0dB
1	-8.5dB	-8.9dB	-7.6dB

EN_RXD	DEVICE FUNCTION
1(default)	Normal operating mode
0	Sleep mode

CM	DEVICE FUNCTION
0(default)	Normal operating mode
1	Compliance mode







6,7,9,10,23,24,25,28,30,32 +3VS5
13,18,28,29,30,31,32 +5VS5
4,7,22,23,25,27,28 +3VPCU

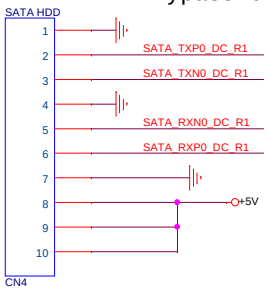
PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB 3.0	1A

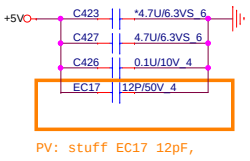
Date: Monday, April 21, 2014 Sheet 20 of 32

SATA HDD Connector(Cable type)

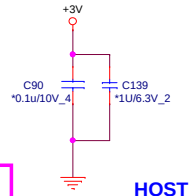
Bypass CAP close conn



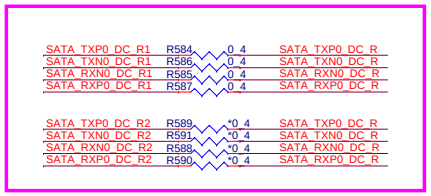
footprint check OK



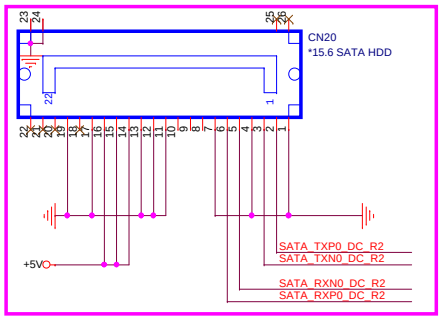
PV: stuff EC17 12pF,



SI add for co-lay use

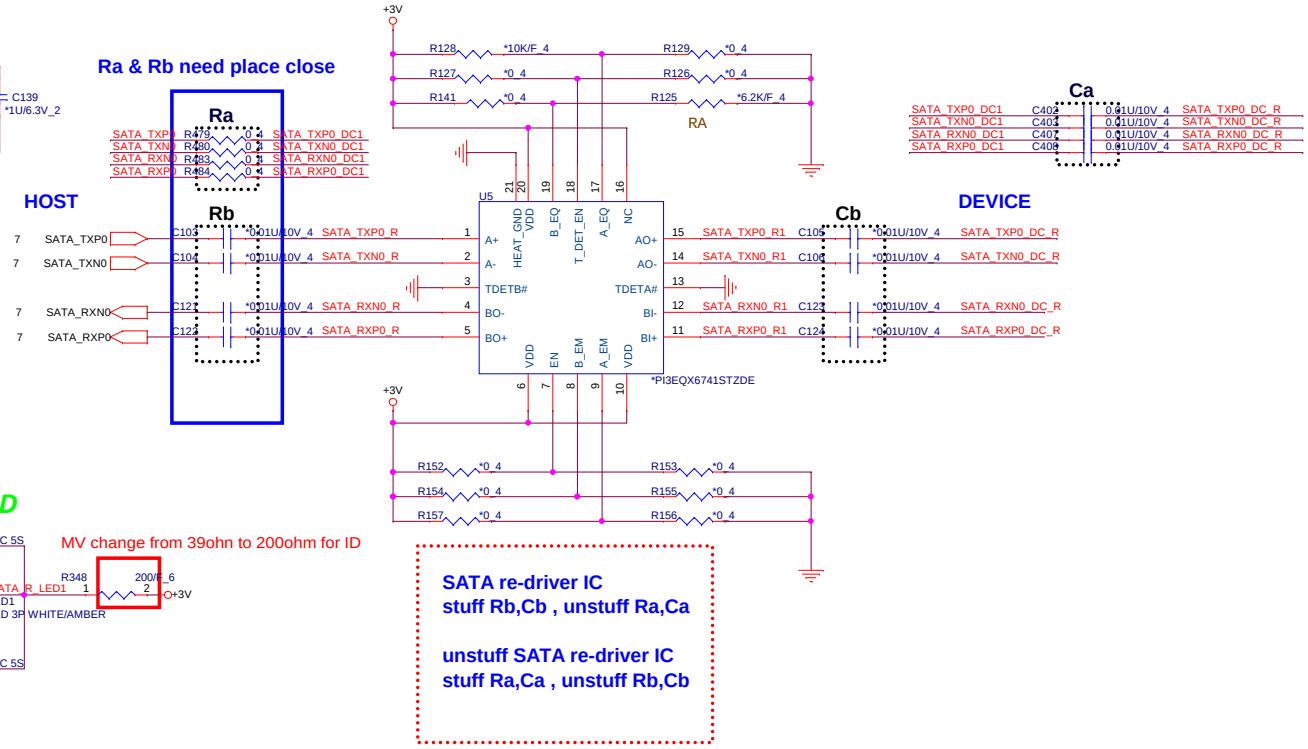


SI-co-lay SATA HDD Connector



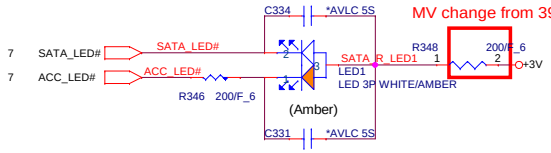
SATA Re-driver

Ra & Rb need place close



SATA LED

MV change from 39ohn to 200ohm for ID



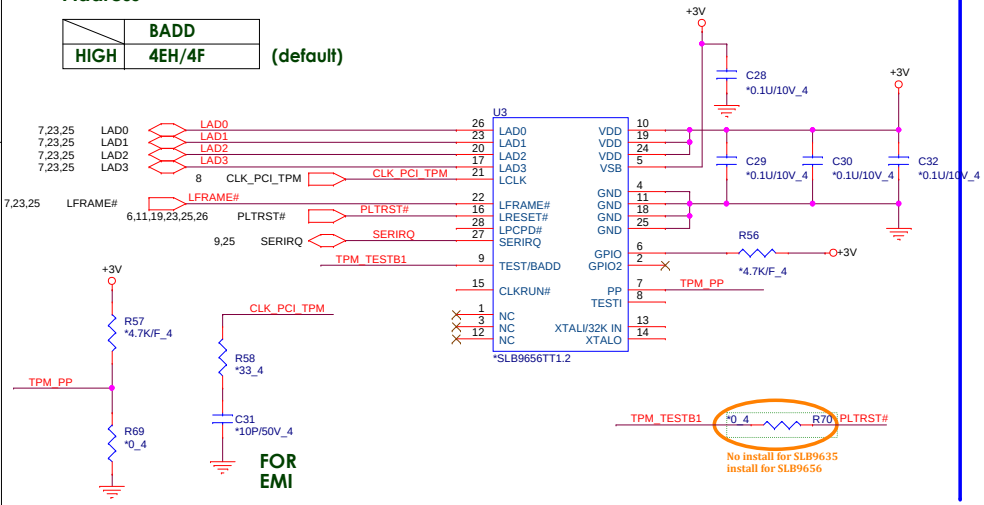
SATA re-driver IC
stuff Rb,Cb , unstuff Ra,Ca

unstuff SATA re-driver IC
stuff Ra,Ca , unstuff Rb,Cb

TPM (1.2)

Address

	BADD
HIGH	4EH/4F (default)



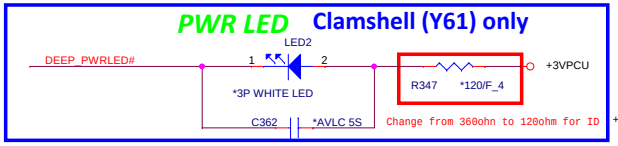
6,7,8,9,10,11,12,13,14,15,16,17,18,19,22,23,24,25,26,31,32 +3V
16,17,18,22,23,32 +5V
4,7,22,23,25,27,28 +3VPCU
27 BATT+

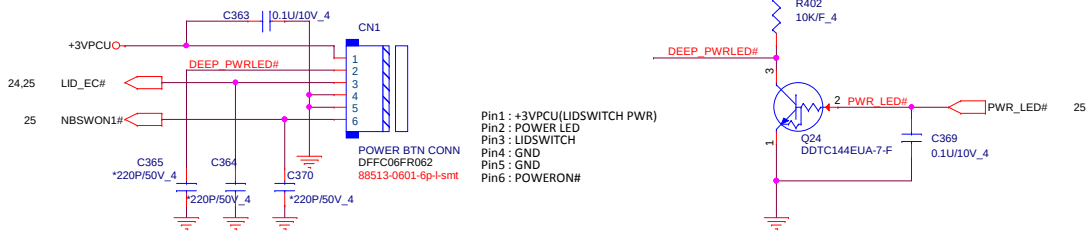
PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/mSATA/FAN/LED	1A
Date: Monday, April 21, 2014	Sheet 21of 32	

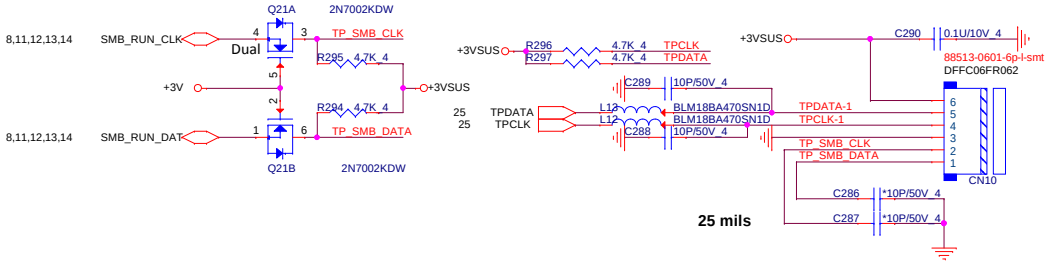
Power Botton Connector

PWR LED Clamshell (Y61) only

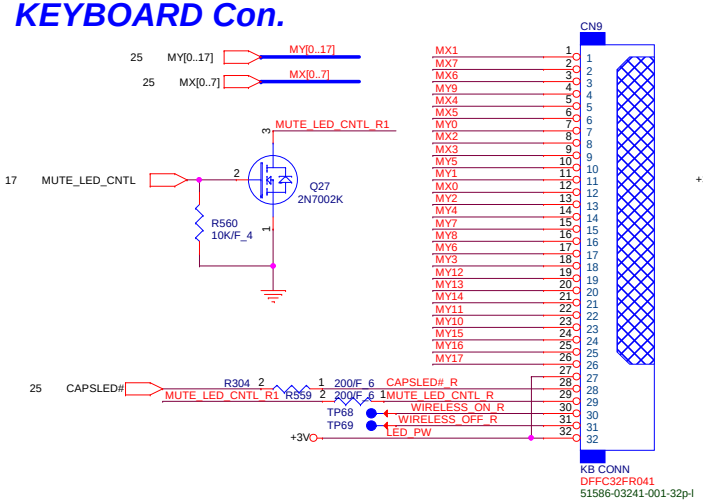




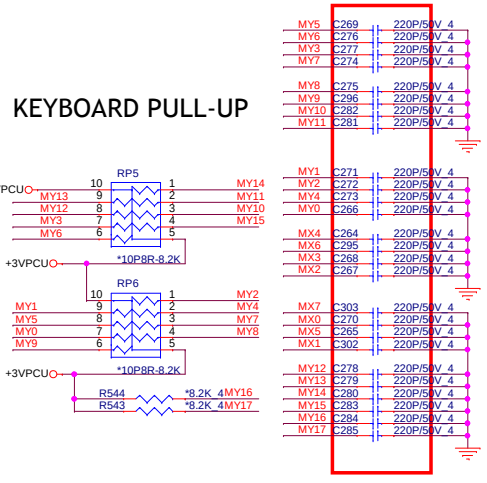
Touch Pad Connector



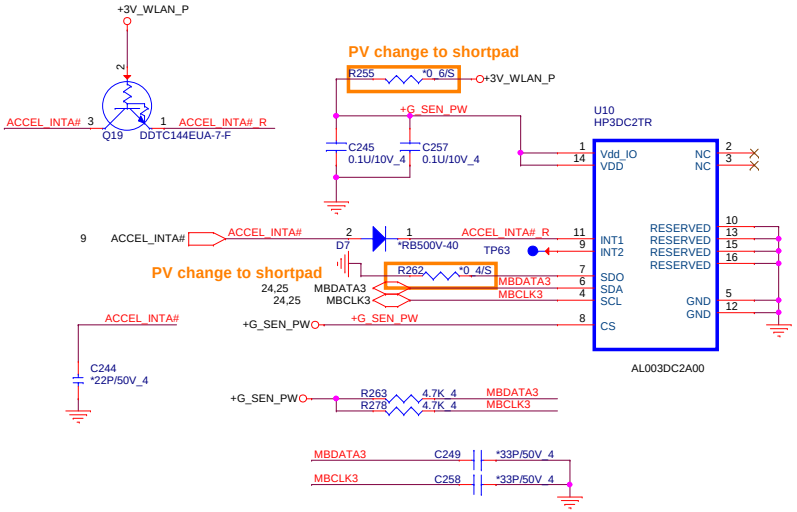
KEYBOARD Con.



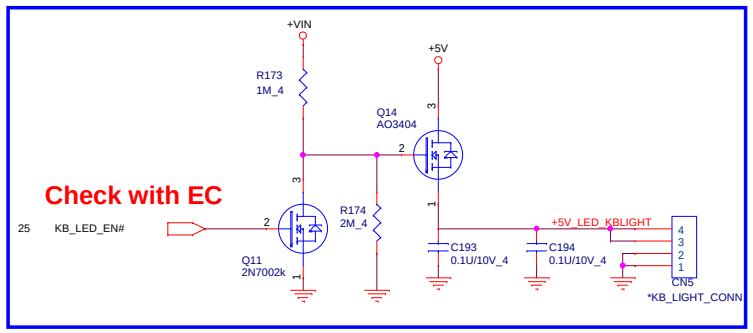
KEYBOARD PULL-UP



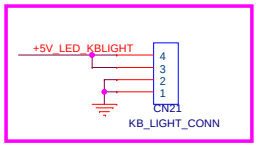
Accelerometer Sensor



15" KB backlight only



Co-lay

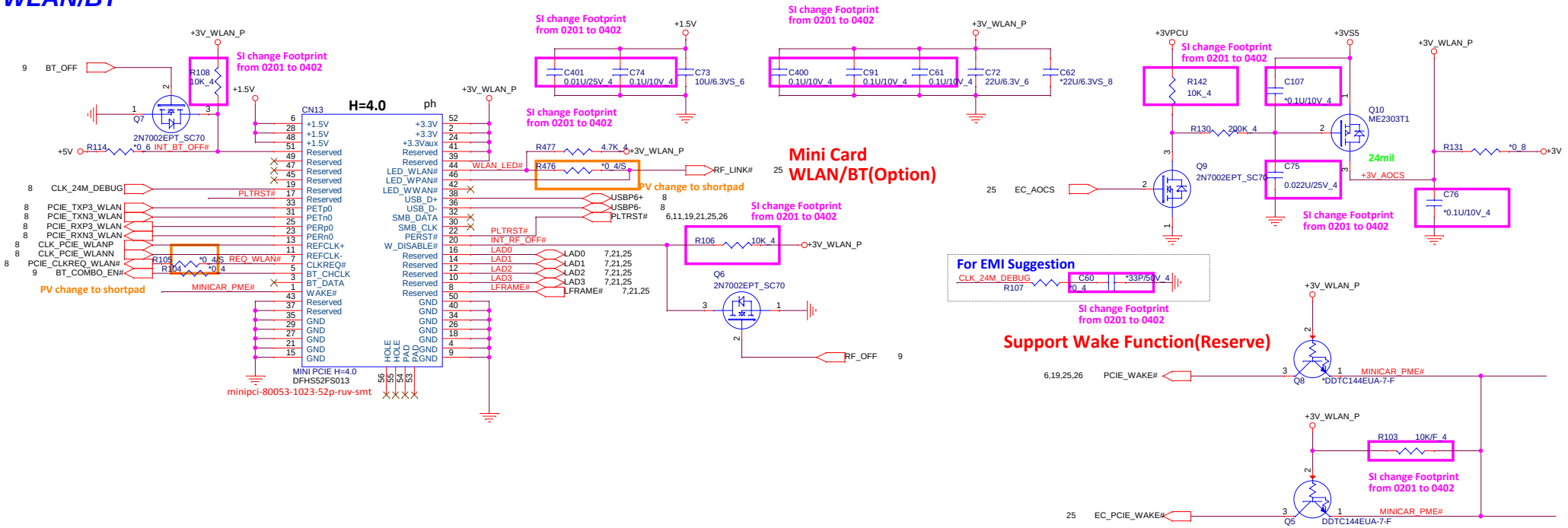


6,7,8,9,10,11,12,13,14,15,16,17,18,19,21,23,24,25,26,31,32 +3V
16,17,18,21,23,32 +5V
4,7,23,25,27,28 +3VPCU

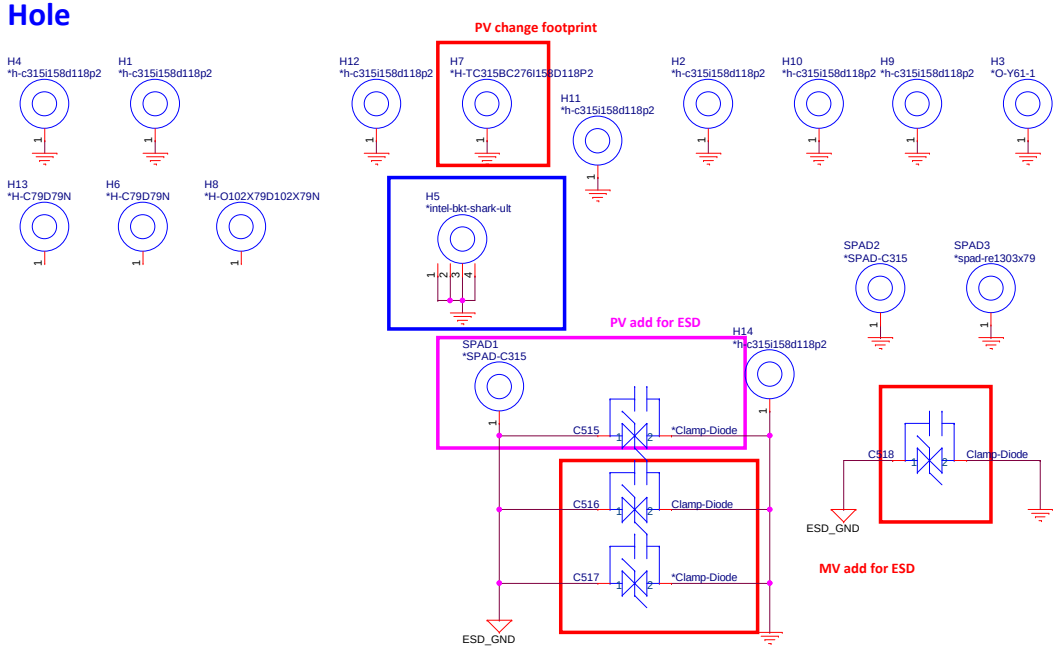
PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PB/TP/KB/FAN/EMI Cap	1A
Date: Monday, April 21, 2014	Sheet 22 of 32	

WLAN/BT



Hole



PROJECT :	Y61
Quanta Computer Inc.	
Size: Custom	Document Number: WLAN/G-Sensor/G-CLK/TS
Rev:	1A
Date: Monday, April 21, 2014	Sheet 23of 32

Accelerometer Sensor

Put it on MB side

U9 HP3DC2TR

C226 10U/6.3V_6, C225 0.1U/10V_4

ACC_INT, TP37, SMDAT4, SMCLK4

Vdd_IO, VDD, NC, NC, RESERVED, RESERVED, RESERVED, RESERVED, INT1, INT2, SDO, SDA, SCL, GND, GND, CS

Close to U9

Q17A *2N7002DW (Dual)

22,25 MBDATA3 — SMDAT4 — R238 *4.7K_4 — +3V

To EC SMBUS

22,25 MBCLK3 — SMCLK4 — R239 *4.7K_4 — +3V

Q17B *2N7002DW (Dual)

To Sensor Hub SMBUS: SMDAT4_L, SMCLK4_L — R184 0_4, R215 0_4 — SMDAT4, SMCLK4

Note: Place all capacitors close to IT8350.

C431 0.1U/10V_4, C432 0.1U/10V_4, C421 0.1U/10V_4, C211 0.1U/10V_4, C187 0.1U/10V_4

20MIL: +3V — R177 *0_6 — L9 BLM15PX181SN1D — AVCC; C419 1000P/50V_4, C418 0.1U/10V_4; L32 BLM15PX181SN1D — IT8350_AGND

20MIL

20MIL 10MIL (For PLL Power): +3V — +3VPLL — L10 BLM15PX181SN1D — +3V; C227 0.1U/10V_4 — AVCC

SMCLK0 R499 4.7K_4, SMDAT0 R500 4.7K_4, SMCLK2 R502 4.7K_4, SMDAT2 R503 4.7K_4, SMCLK4 R202 4.7K_4, SMDAT4 R183 4.7K_4

To APU: 9 ACCEL_INTH# — R488 *0_4 — ACC_INT

U23 IT8350E_LQFP-48

VSTBY (4, 16, 23, 36, 1), VSTBY(PLL) (7), AVCC (33)

IT8350E LQFP-48

Reserved SMBus channel 0 for debugging & updating FW

Reserved

SMbus channel 4 for connecting the Sensor (G-sensor)

SM BUS: SMCLK0/GPB3, SMDAT0/GPB4, SMCLK2/GPF6, SMDAT2/GPF7, SMCLK4/GPE0, SMDAT4/GPE7 — SMCLK0, SMDAT0, SMCLK2, SMDAT2, SMCLK4_L, SMDAT4_L — TP115, TP116

R504 100K_4, D11 RB500V-40, WRST# 11 — WRST#; C434 1U/6.3V_4X

FSPI: FSCE#/GPG3, FMOSI/GPG4, FMISO/GPG5, FSCK/GPG7

PWM: PWM0/GPA0, PWM1/GPA1, PWM4/SMCLK5/GPA4, PWM5/SMDAT5/GPA5, PWM6/SSCK/GPA6 — LID_EC# 22,25

R491 1.5K_4 — USBP4+

USB for Host

8 USBP4- / 8 USBP4+ — L33 *MCM2012B900GBE — USBP4-, USBP4+ — GPH5/ID5/DM, GPH6/ID6/DP

SI short L33

USB

UART: RXD/SIN0/GPB0, TXD/SOUT0/GPB1 — RXD, TXD — TP112, TP113

Reserved TX/RX for debugging

if no use ADC function, please pull down to GND

SMINTx for sensor interrupt

GPI0 R495 4.7K_4, SMINT0 R494 *4.7K_4, SMINT1 R185 *4.7K_4, SMINT2 R186 *4.7K_4, SMINT3 R492 *4.7K_4, GPI5 R171 4.7K_4

A/D: ADC0/GPI0, ADC1/SMINT0/GPI1, ADC2/SMINT1/GPI2, ADC3/SMINT2/GPI3, ADC4/SMINT3/GPI4, ADC5/GPI5

GPI0 R169 *0_4/S GYRO_DRDY — COOL SENSE 25

SMINT1 R175 *0_4/S GYRO_INT

SMINT2 R176 *0_4/S AE_INT

SMINT3 R493 *0_4/S ACC_INT

GPI5 R170 *0_4/S — DISABLE KB 25

PV change to shortpad

GPG2 can't floating

SSPI: SSCE0#/GPG2, KSO17/SMISO/GPC5, KSO16/SMOSI/GPC3 — GPIOG2, GPIOC5, GPIOC3 — TP105, TP109

R187 +3V — *100K_4; R188 100K_4

GPG2 Pull High Enable mirror function.

GPG2 Pull Low Disable mirror function.

For Home button IC update fw 25 HOME_BUTTON_Flash_EN#

3 IN 1-Sensor connector to HOME IC

25 HOME_BUTTON_INT#

25 HOME_BUTTON_LED — R135 200/F_6

CN3

Touch screen 25 TS_ON

+3V_HOME, TS_ON, USBP3-, USBP3+, AE_INT, GYRO_DRDY, GYRO_INT

C92 0.1U/10V_4 SMD FPC 20P

+3V — R473 0_4 — +3V_HOME; +3VS5 — R472 *0_4

13,25 GPUT_DATA, 13,25 GPUT_CLK

SMDAT4, SMCLK4

CLOCK: CK32KE/GPJ7, CK32K/GPJ6 — CK32KE, CK32K — 32.768KHZ_10 Y4; C429 10P/50V_4, C430 10P/50V_4

External crystal is must be item when USB func. is used !

VSS (5, 24, 35), VCORE (10), AVSS (34)

C433 0.1U/10V_4 — IT8350_AGND

8 USBP3- / 8 USBP3+ — L4 *MCM2012B900GBE

SI short L4

SI co-lay 6 pin TS CON

*HOUSING 6P — +3V_HOME, TS_ON, USBP3-, USBP3+ — CN22

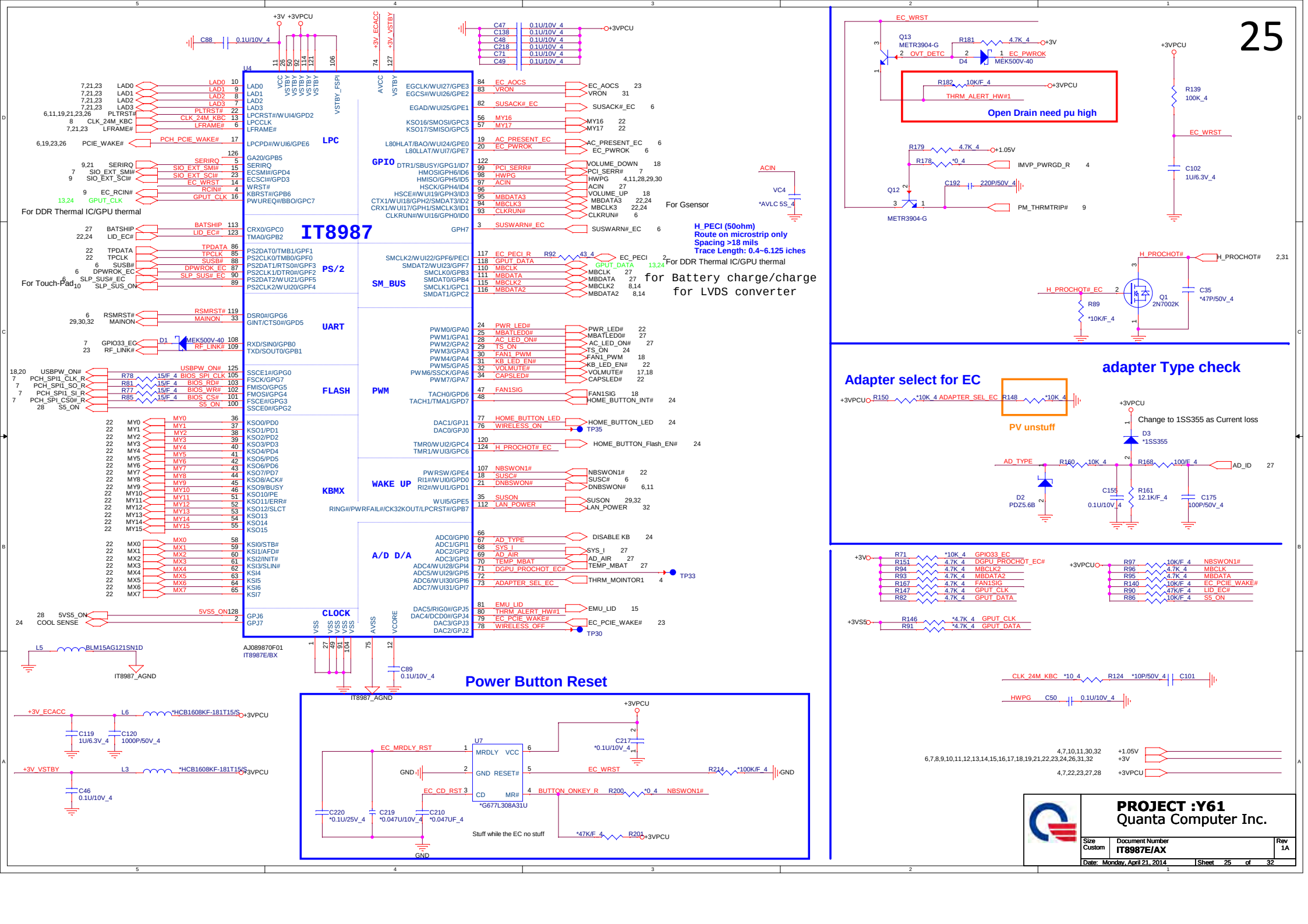
L31 *BLM18BA470SN1D/S — IT8350_AGND

32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ITE8350/HP9DS0/HP3DC2	1A

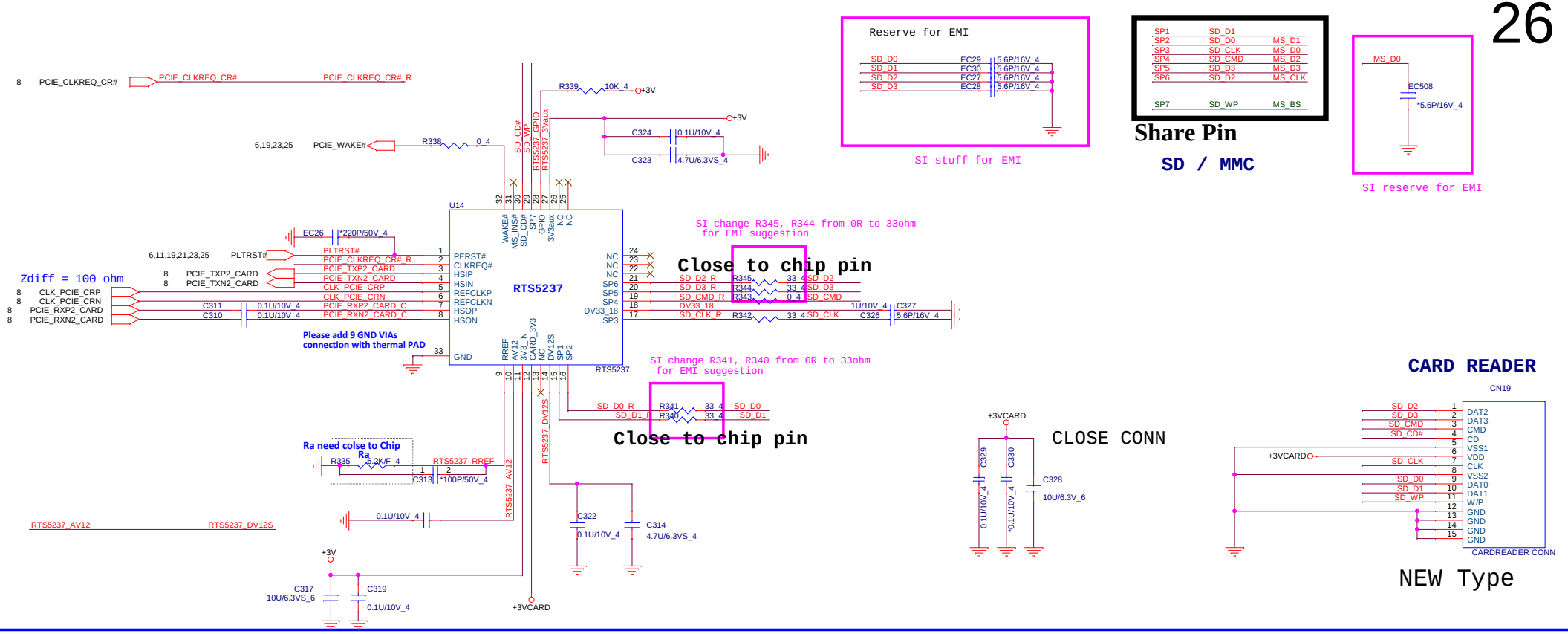
Date: Monday, April 21, 2014 | Sheet 24 of 32



PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	IT8987E/AX	1A

Date: Monday, April 21, 2014 Sheet 25 of 32



PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CR RTS5237 & HOLE	1A

Date: Monday, April 21, 2014 Sheet 26 of 32

DC_JACK/65W

Place this ZVS close to Diode away +VIN

Do Not add test pad on BATDIS_G signal

EMI request for ISN

Place this cap close to EC

15.6"

Place this ZVS close to Far-Far away +VIN

EMI request for ISN

ACDET=13V

MIN. BATV=7.2V

Setting MAX Icharge to 5A

Place this cap close to EC

Place this cap close to EC

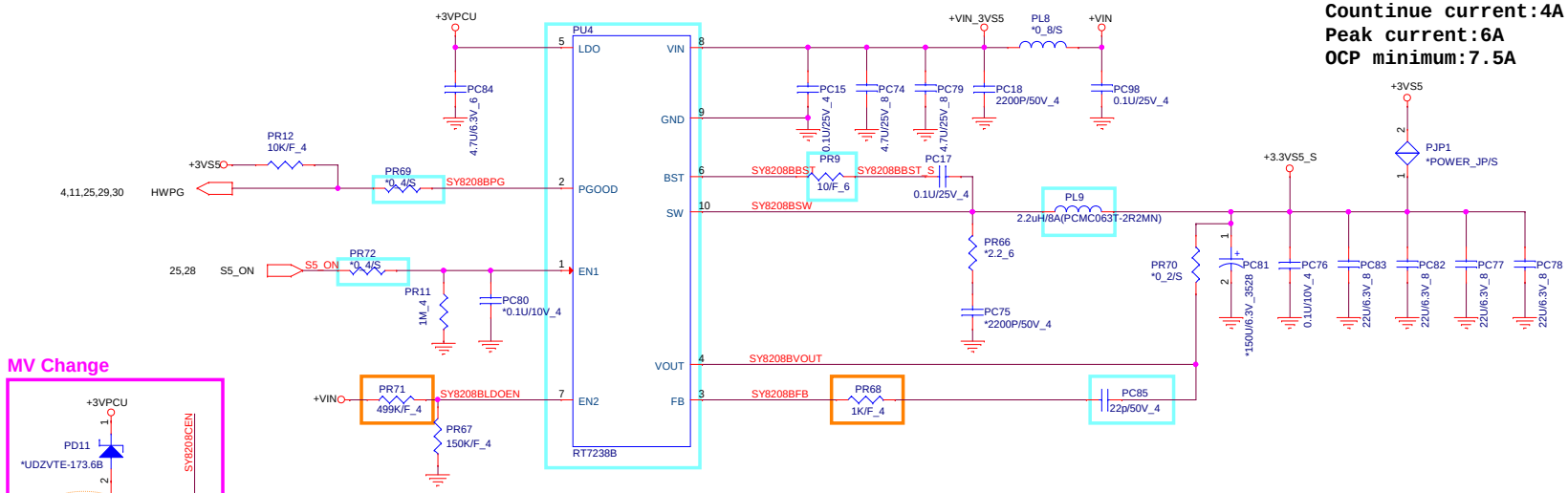
PU8 BQ24738H

+3VPCU 4,7,22,23,25,28
+5VPCU 13,28
BATT+
+PRWSRC

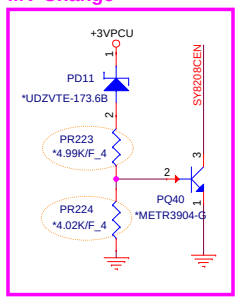
DC/DC +3VS5/+5VS5

+3VS5 6,7,9,10,20,23,24,25,30,32
+5VS5 13,18,20,29,30,31,32

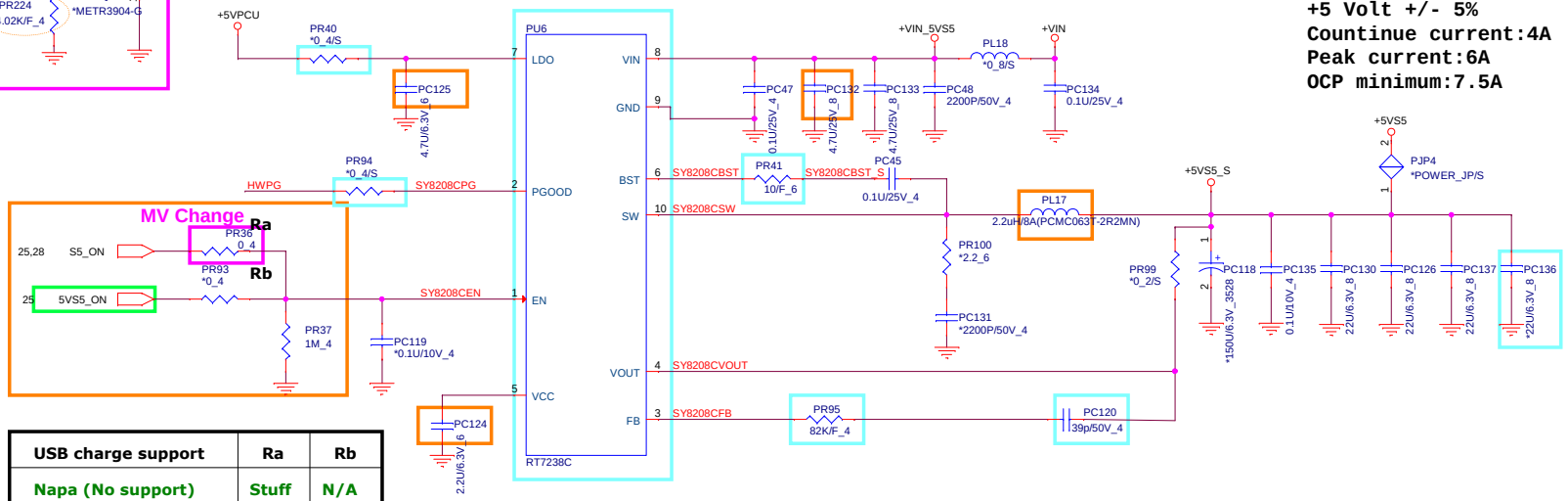
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



MV Change



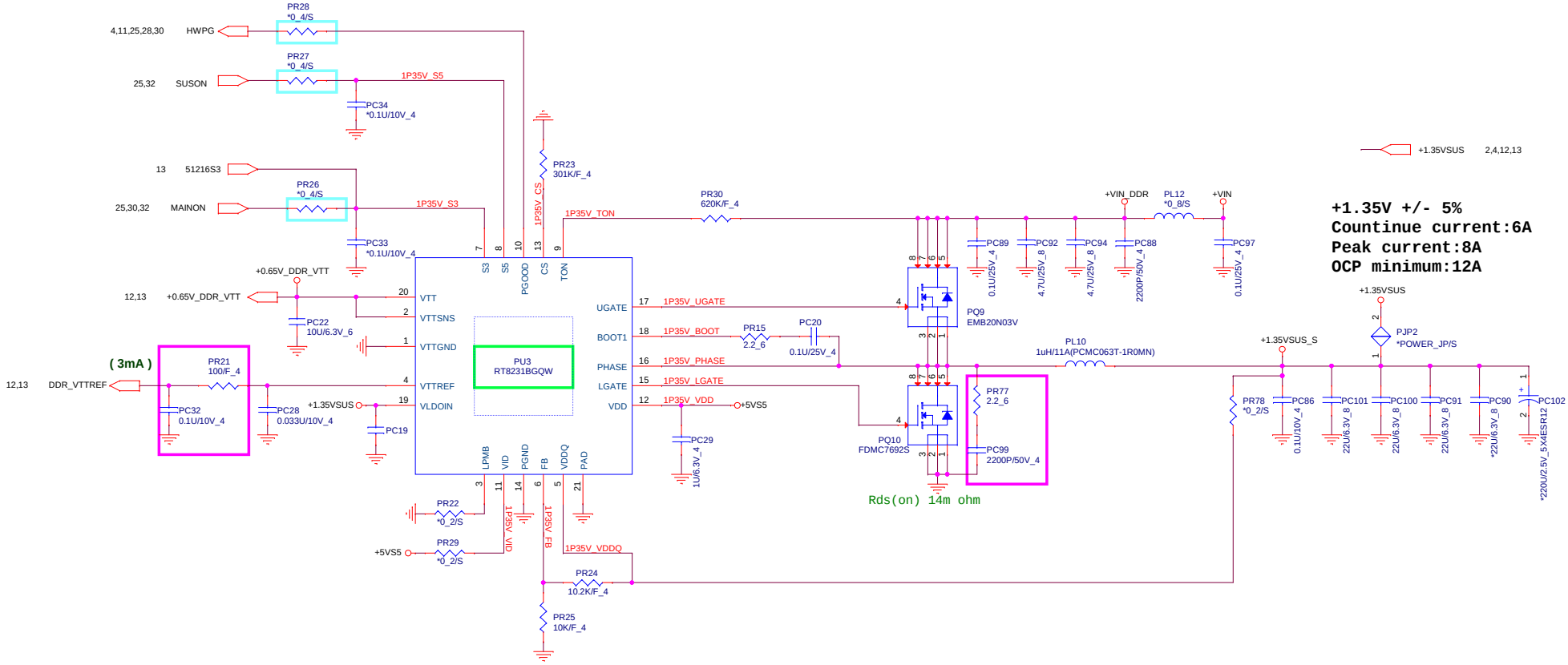
+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



USB charge support	Ra	Rb
Napa (No support)	Stuff	N/A
Whisky (Support)	N/A	Stuff

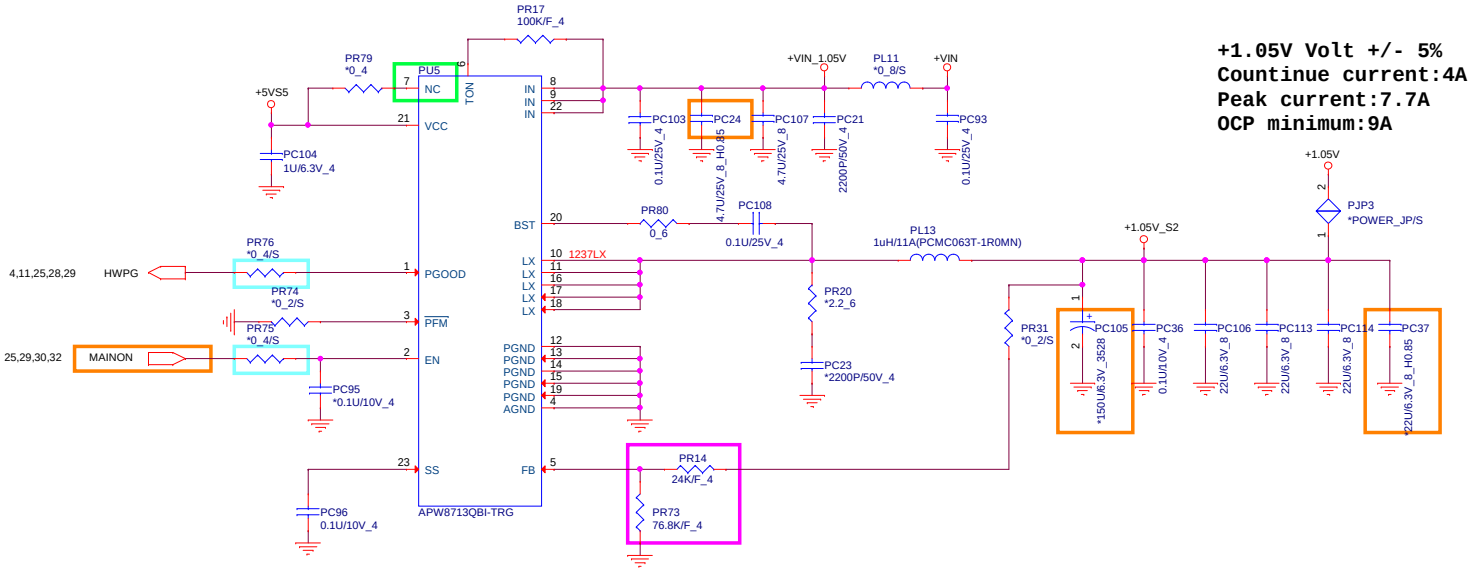
PROJECT :NAPA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A
Date: Monday, April 21, 2014	Sheet 28 of 32	

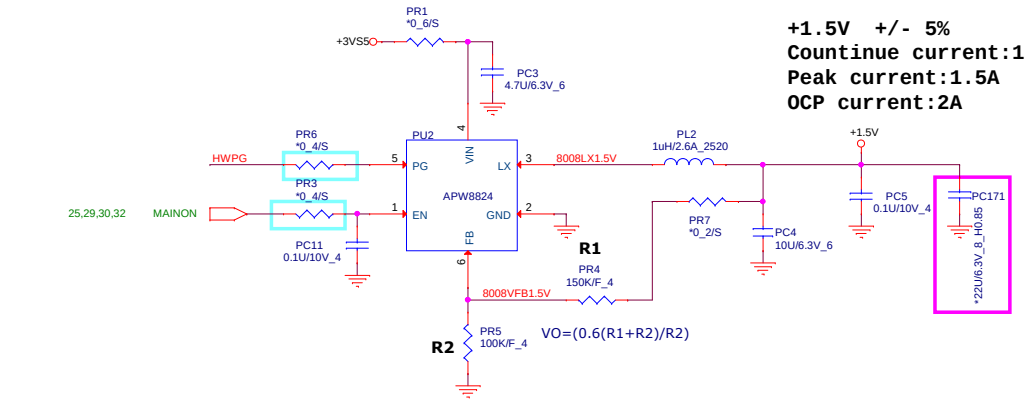


Size Custom	Document Number DDR3 (RT8231B)		Rev 1A
Date: Monday, April 21, 2014		Sheet 29 of 32	

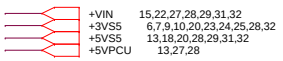
PROJECT :NAPA
Quanta Computer Inc.



+1.05V Volt +/- 5%
Countinue current:4A
Peak current:7.7A
OCP minimum:9A



+1.5V +/- 5%
Countinue current:1.3A
Peak current:1.5A
OCP current:2A

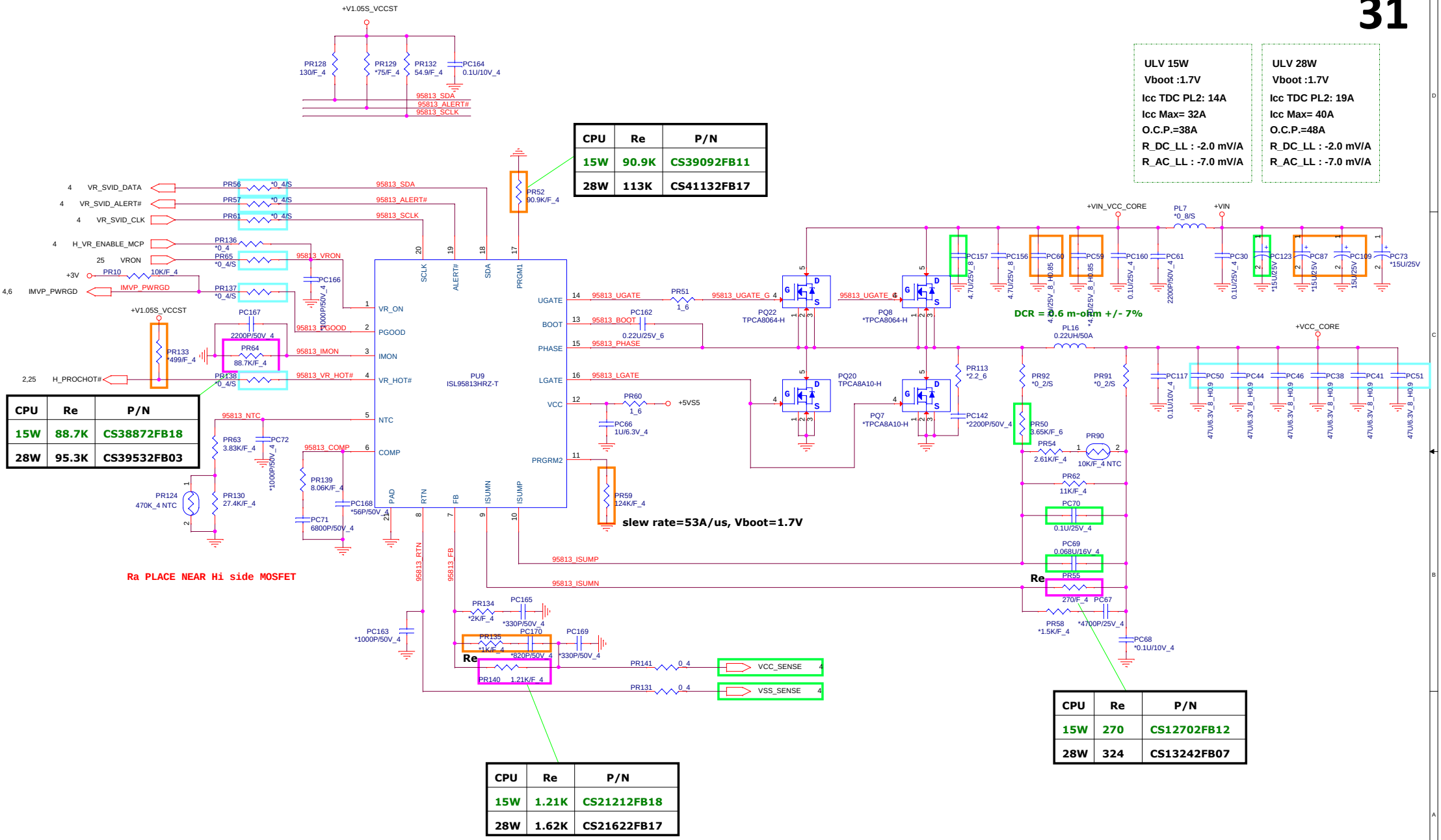


PROJECT :NAPA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V (APW8713)/1.5V	1A
Date: Monday, April 21, 2014	Sheet 30 of 32	

ULV 15W
Vboot :1.7V
Icc TDC PL2: 14A
Icc Max= 32A
O.C.P.=38A
R_DC_LL : -2.0 mV/A
R_AC_LL : -7.0 mV/A

ULV 28W
Vboot :1.7V
Icc TDC PL2: 19A
Icc Max= 40A
O.C.P.=48A
R_DC_LL : -2.0 mV/A
R_AC_LL : -7.0 mV/A



CPU	Re	P/N
15W	90.9K	CS39092FB11
28W	113K	CS41132FB17

CPU	Re	P/N
15W	88.7K	CS38872FB18
28W	95.3K	CS39532FB03

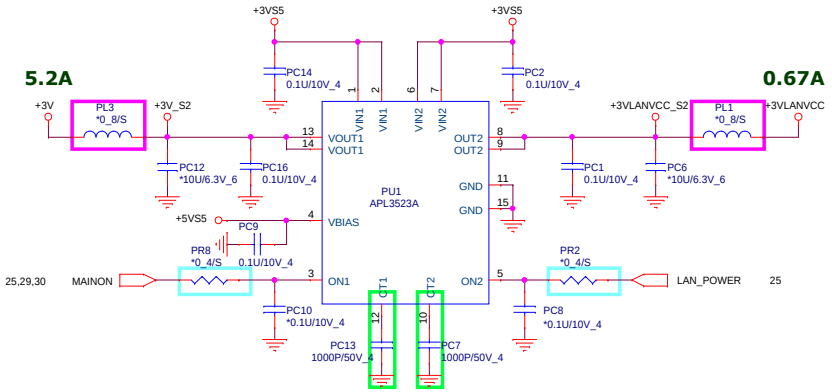
CPU	Re	P/N
15W	270	CS12702FB12
28W	324	CS13242FB07

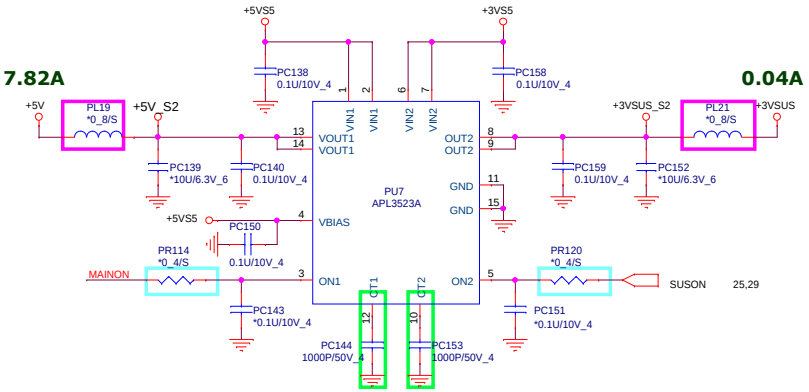
CPU	Re	P/N
15W	1.21K	CS21212FB18
28W	1.62K	CS21622FB17

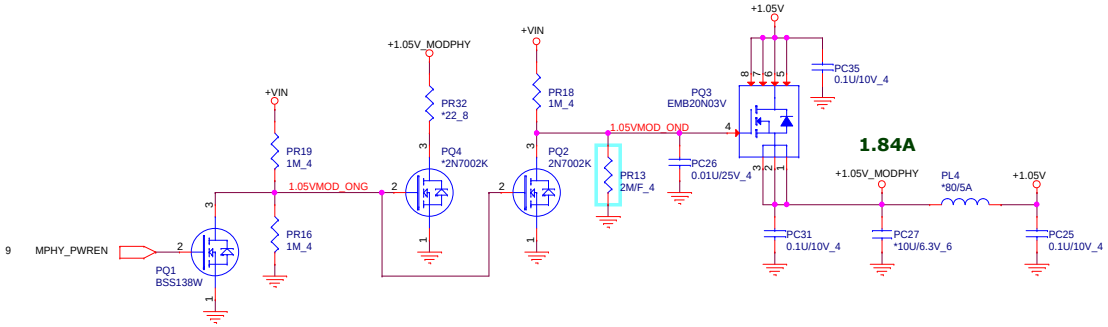
PROJECT :NAPA
Quanta Computer Inc.

Size	Document Number	Rev
	CPU_CORE(ISL95813) 15W	1A

Date: Monday, April 21, 2014 Sheet 31 of 32







6,7,8,9,10,11,12,13,14,15,16,17,18,19,21,22,23,24,25,26,31 +3V
16,17,18,21,22,23 +5V
15,22,27,28,29,30,31 +VIN
6,7,9,10,20,23,24,25,28,30 +3VS5
13,18,20,28,29,30,31 +5VS5
19 +3VLANVCC

PROJECT :NAPA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Load switch IC (APL3523A)	1A
Date: Monday, April 21, 2014	Sheet 32 of 32	