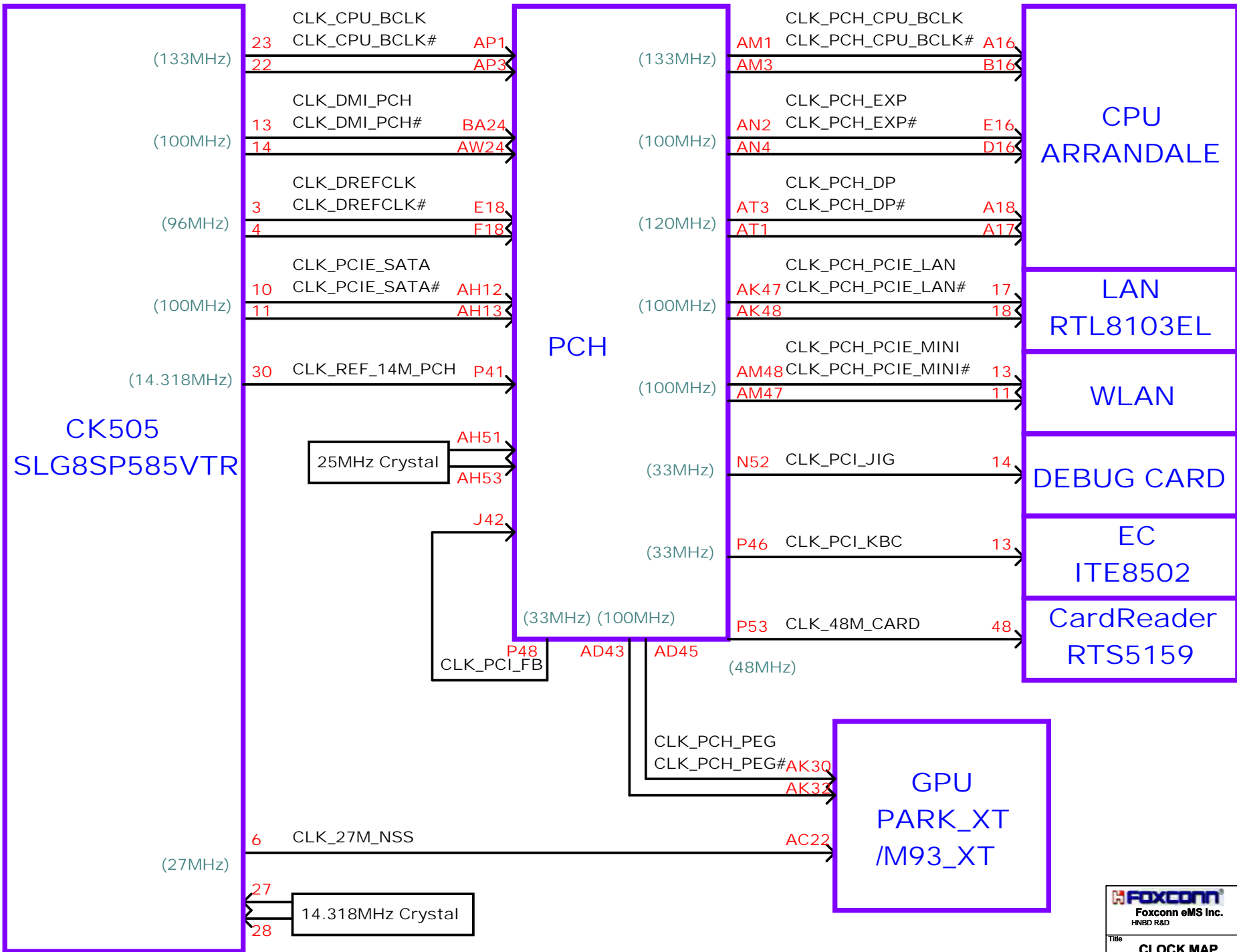


01 -- COVER SHEET	21 -- VGA_S3 (DDR3) 3/5
02 -- SYSTEM BLOCK DIAGRAM	22 -- VGA_S3 (DP) 4/5
03 -- CLOCK MAP	23 -- VGA_S3 (POWER) 5/5
04 -- POWER MAP	24 -- VRAM (DDR3)
05 -- POWER SEQUENCY DIAGRAM	25 -- EC+KBC (IT8502E)
06 -- POWER SEQUENCY TIMING	26 -- CODEC/JACK/SPEAKER/MIC
07 -- SMBUS MAP	27 -- LAN (RTL8103EL)/CLOCK GEN
08 -- Calpella (DMI,PEG,FDI)	28 -- Card Reader
09 -- Calpella (CLK,MISC,JTAG)	29 -- WLAN/BT/MDC/USB/MOUNTING
10 -- Calpella (DDR3)	30 -- LVDS/CRT/Webcam
11 -- Calpella (POWER/GND)	31 -- HDMI
12 -- Calpella (GRAPHIC POWER)	32 -- DCIN/Battery/OCP/FAN
13 -- PCH (HDA,JTAG,SATA)	33 -- PWR_Charger MAX8731AETI
14 -- PCH (PCI-E,SMBUS,CLK)	34 -- 5V/3.3V SN0608098RHBT
15 -- PCH (DMI,FDI,GPIO,LVDS)	35 -- Vcore MAX17030
16 -- PCH (PCI,USB,NVRAM,GPIO)	36 -- 1.1V VTT/+V1.05RUN
17 -- PCH (POWER)	37 -- 1.5VDDR3+0.75V+V1.8RUN
18 -- DDR3(SO-DIMM_0&1)	38 -- PWR_Others power plane
19 -- VGA (PCI-E/STRAP) 1/5	39 -- CPU VREG & Decoupling
20 -- VGA_S3 (IO) 2/5	40 -- ATVDD/+VPCIE


P. Leader	Check by	Design by

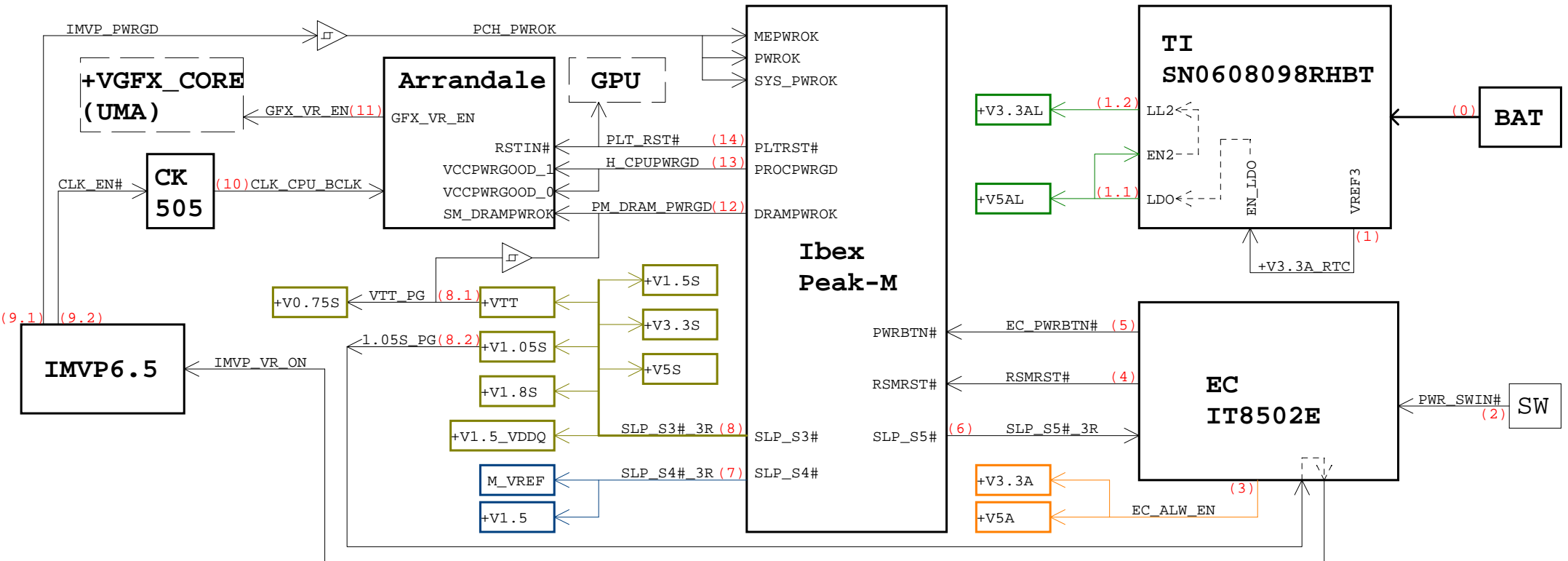
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Title Index Page		
Size Custom	Document Number STAR (Federer)	Rev 1.0
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SCH Page	Change Request Description	Notes
25,33~40	modify the power short pad to "POWER_OPENPAD_1P9X2P4"	SMD performance issue
15	Add RS74,RS77,RS79 for all SG sku	Fix VGA port auto detect function
39	Change PR944 from 1K to 1.5K	Fix power load line test issue
13	Del PCH SPI ROM connector circuitry	Del unnecessary functon parts
25	Del EC SPI ROM connector circuitry	Del unnecessary functon parts
25	Del debug connector	Del unnecessary functon part
25	SKU ID modify to MV phase	MV Phase ID
13	32.768KHZ crystal change to CL:7PF	RTC Clock tuning
25	32.768KHZ crystal change to CL:7PF	RTC Clock tuning
30	VGA connector change part number to halide free type	ROHS issue
29	MDC connector change part number to halide free type	ROHS issue
29	Mini-PCIE connector change part number to halide free type	ROHS issue
30	LVDS connector change part number to halide free type	ROHS issue
13	SATA connector change part number to halide free type	ROHS issue
30	Modify backlight PWM control path	Del unnecessary parts
18	Modify the DDR3 footprint	Co-lay for DDR3 connector
25	Del D110	Del unnecessary functon parts
25,30	Del RB28 and Add RI54	For 17" keyboard num lock LED
38	add PC775	Add for GPU M93 platform
38	add PC776	Add for VGA wave issue
35	Change VCORE VDD power source from +V5A to +V5S	Modify for V-BOOT
38	Change PR769 pull high power source from +12A to +V5A	Modify for GPU power sequence
29	Modify the HOLE1006 footprint	update footprint
40	modify all VDDCORE circuitry	modify VDDCORE circuitry
26	modify UA3 pin2 Analogy GND to Digital GND	Analogy GND change to Digital GND
32	add 2 pcs 2N7002 and swap EC_CHAR_LED#_A & EC_AC_LED#_A	Modify LED control and brightness
32	modify HEADER10 pin1 power source from +V5A to +V3.3AL	modify LED control and brightness
33~37	PC547 22uF_X5R_25V to 10uF_X5R_25V*2	modify for acoustic
	PC504 4.7uF_X5R_25V to 10uF_X5R_25V	
	PC813 4.7uF_X5R_25V to 10uF_X5R_25V	
	PC825, PC812 to 10uF_X5R_25V (NI)	
	PC826 to 10uF_X5R_25V (NI)	
	PC824, PC828, PC829 4.7uF_X5R_25V to 10uF_X5R_25V"	
32	RH1002 change to 1.3Kohm	modify LED control and brightness
27	RL13 change to 2.7Kohm"	modify LED control and brightness
32	ADD QB11	Thermal shutdown
19	ADD RG457, RG458	Add for power leakage issue
35	Del DB14	Thermal shutdown issue

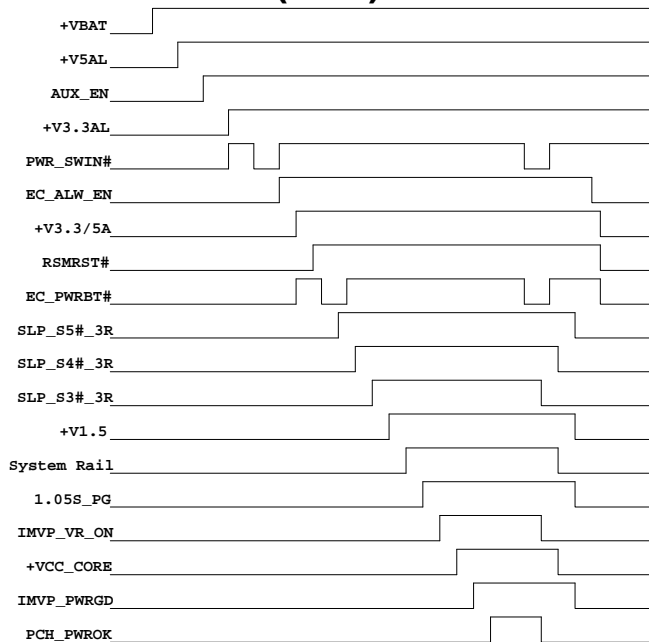
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		phone: +886-2-2799-6111	
History			
Size	Document Number	Rev	
Custom	STAR (Federer)	1.0	
Page Modified: Thursday, March 18, 2010 17:28:23 (UTC+8GMT) Sheet 4 of 40			



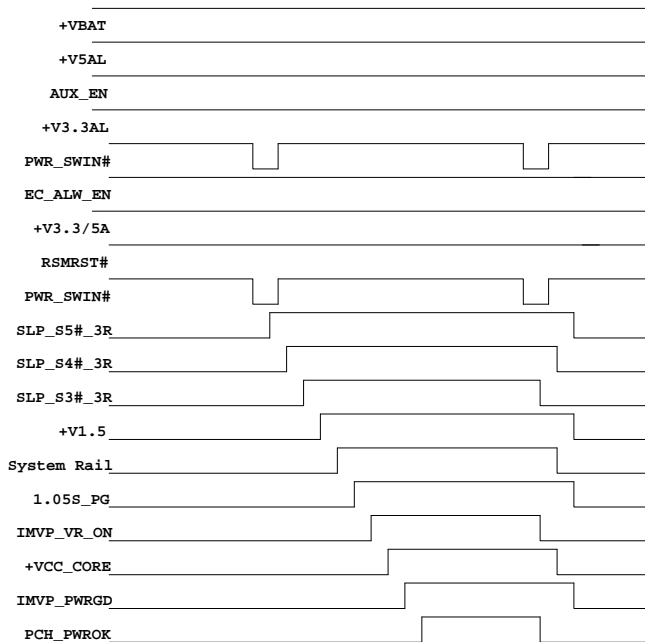
	Source Rail	EN	PG	Power Status				Remark
				S0	S3	AC S4/S5	DC S4/S5	
+VBAT	+VBAT	+V3.3A_RTC		V	V	V	V	
+V5AL	+VBAT	+V5AL		V	V	V	V	
+V3.3AL	+VBAT	+V5AL		V	V	V	V	
+V5A	+VBAT	EC_ALW_EN		V	V	V		
+V3.3A	+V3.3AL	EC_ALW_EN		V	V	V		
+V1.5	+VBAT	SLP_S4#_3R		V	V			
+V0.75S	+V1.5	VTT_PG		V				
+V1.5S	+V1.5	RUN_ON_LOAD		V				
+V1.5_VDDQ	+V1.5	RUN_ON_LOAD		V				
+VCC_CORE	+VBAT	IMVP_VR_ON	IMVP_PWRGD	V				
+VTT	+VBAT	SLP_S3#_3R	VTT_PG	V				
+VGFX_CORE	+VBAT	GFX_VR_EN		V				
+V1.8S	+VBAT	SLP_S3#_3R		V				
+V1.05S	+VBAT	SLP_S3#_3R	1.05S_PG	V				
+V5S	+V5A	RUN_ON_LOAD		V				
+V3.3S	+V3.3A	RUN_ON_LOAD		V				
+VDD_CORE	+VBAT	SLP_S3#_3R		V				
+V3.3S Delay	+V3.3S	+V1.8S		V				
+VPCIE	+V1.5S	SLP_S3#_3R		V				

POWER SEQUENCE TIMING

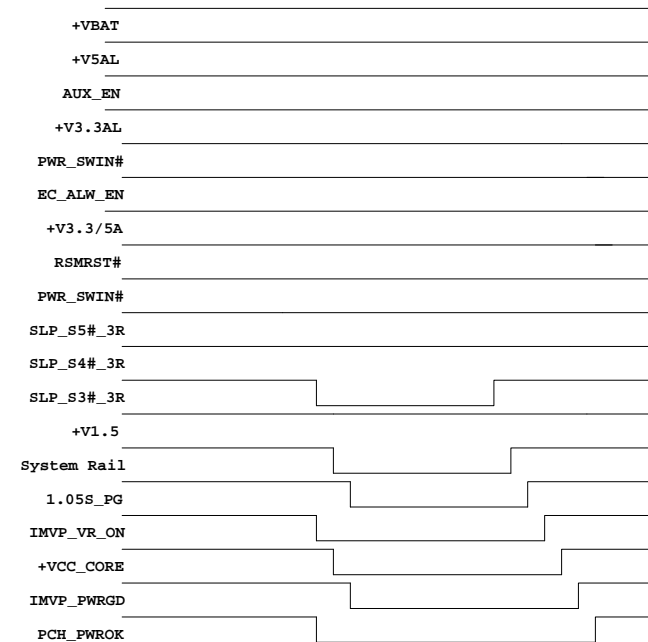
G3(OFF)->S0->S5



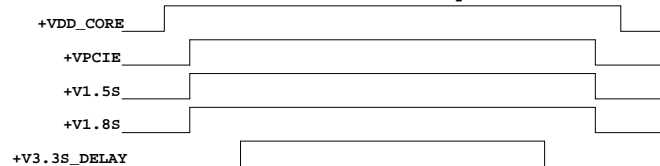
S5->S0->S5



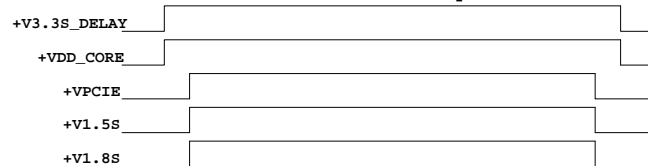
S0->S3->S0



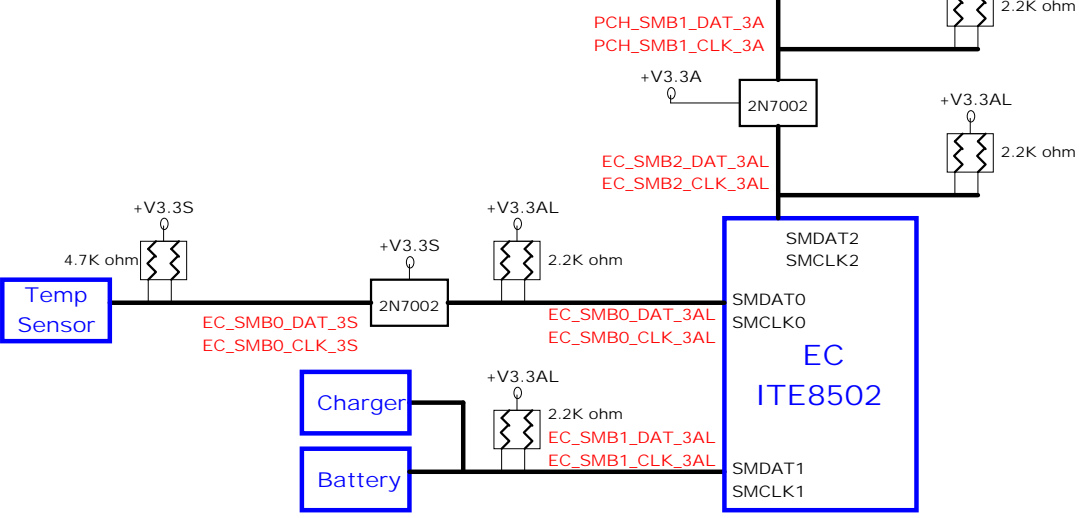
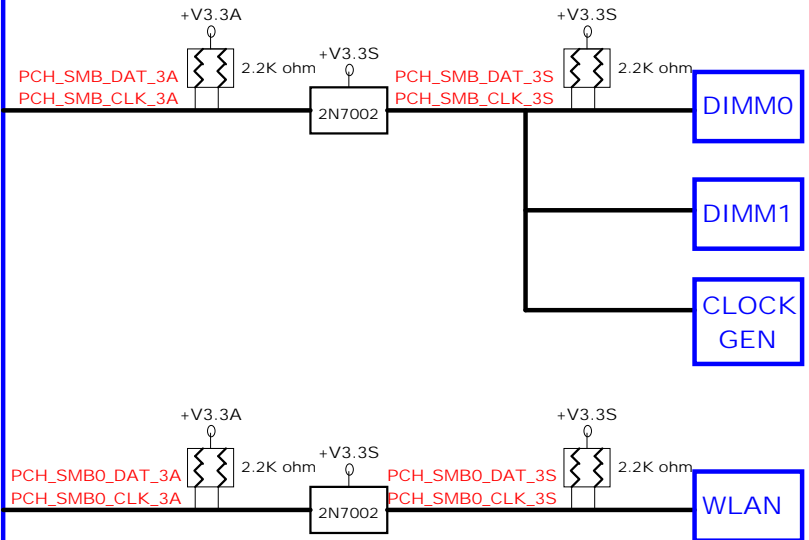
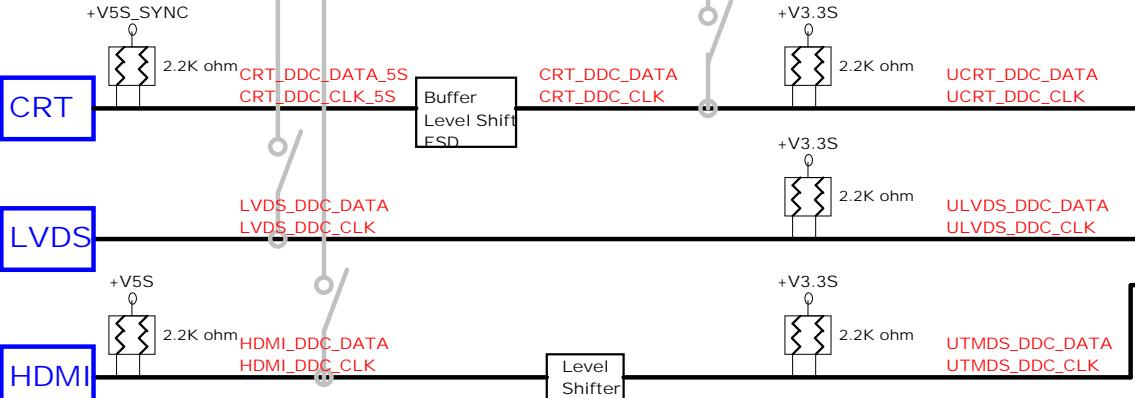
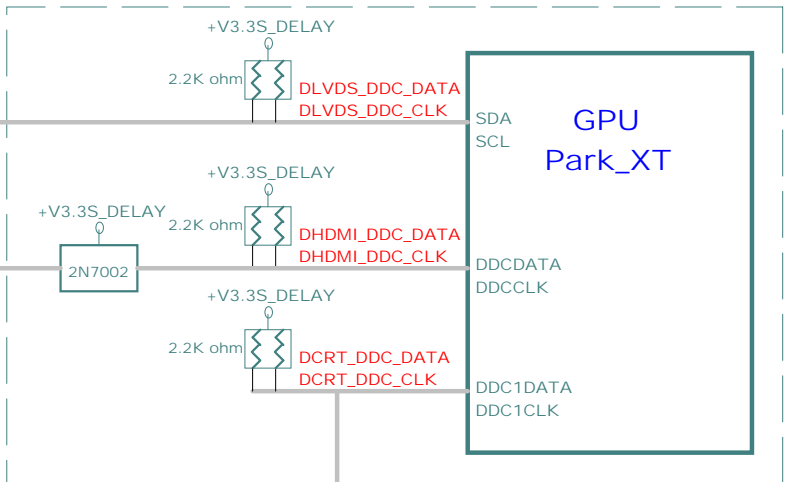
GPU_M93 Sequence

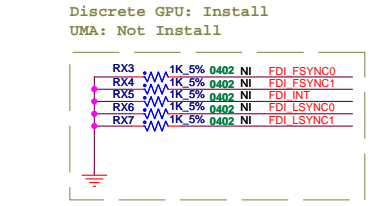
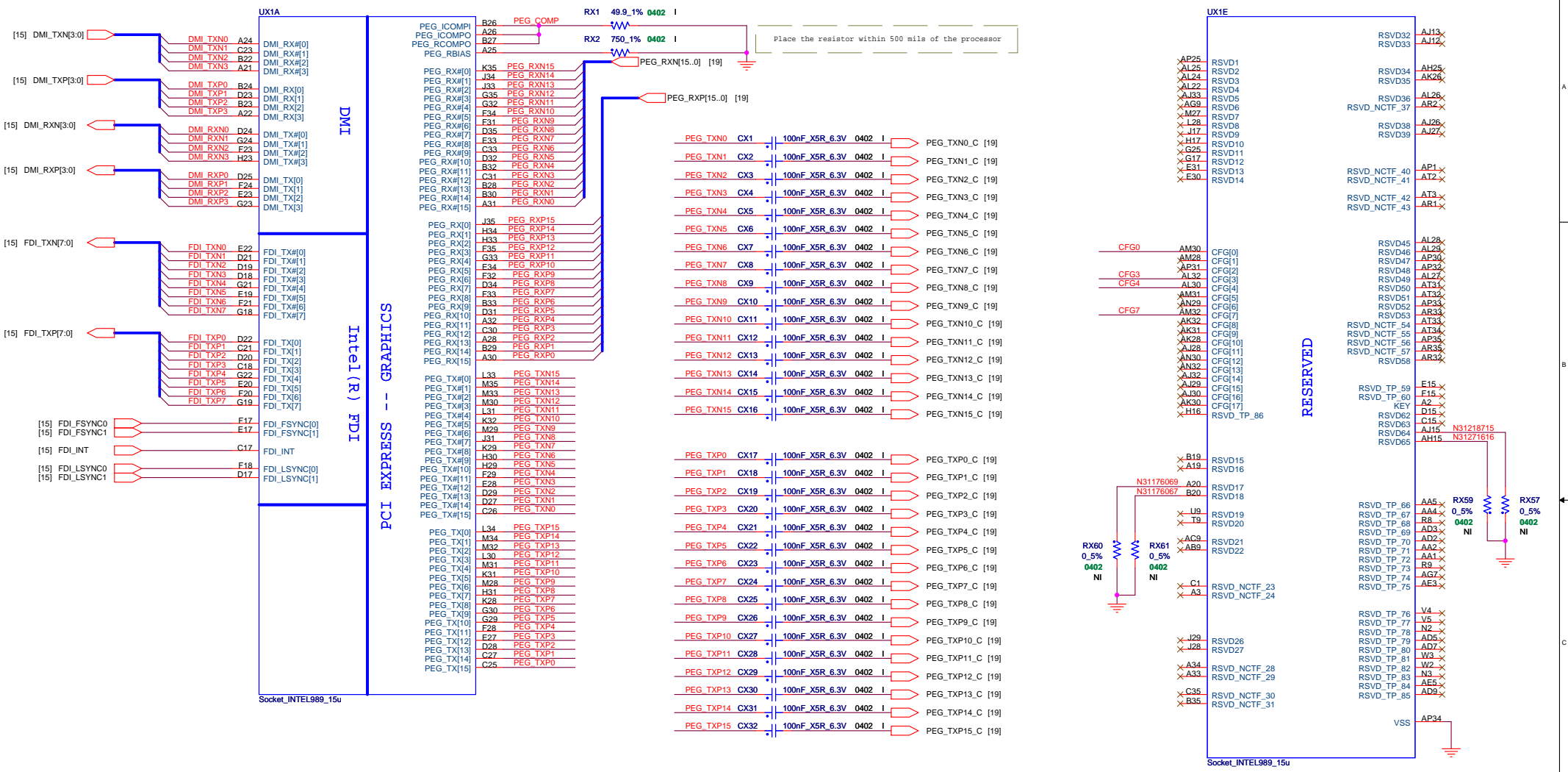


GPU_Park Sequence



Switchable GPU





CFG4 Display Port Presence
1 : Disabled ; No Physical Display Port attached to Embedded Display Port
0 : Enable ; An external Display Port device is connected to the Embedded Display Port

CFG7 Reserved - Temporarily used for early Clarksfield samples.
Clarksfield (only for early samples pre-E31) - Connect to GND with 3.01K Ohm/5% resistor

PCI Express Configuration Select
CFG0 1 : Single PEG
0 : Bifurcation enabled

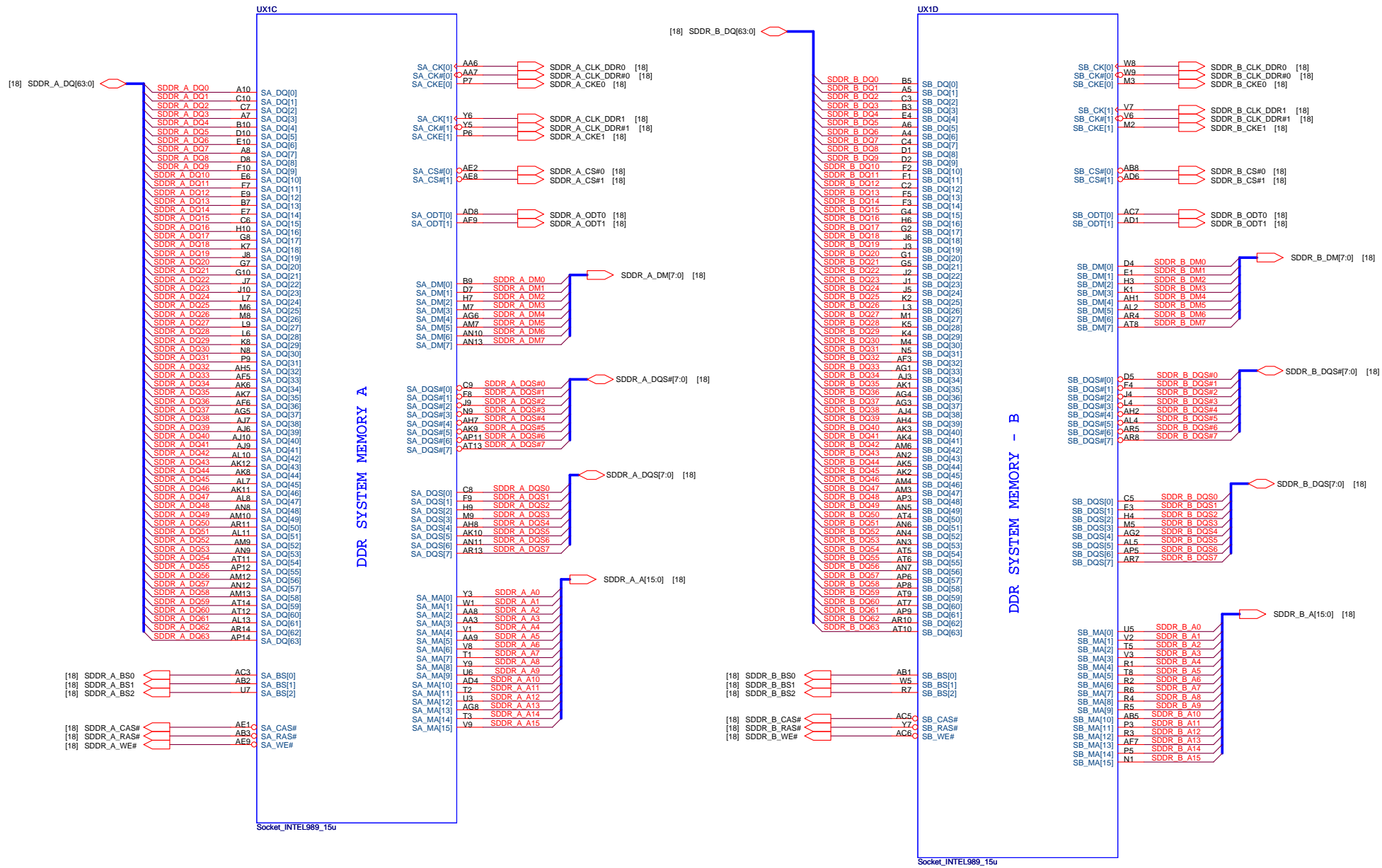
CFG3 PCI Express Static Lane Reversal
CFG3 1 : Normal Operation
0 : Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

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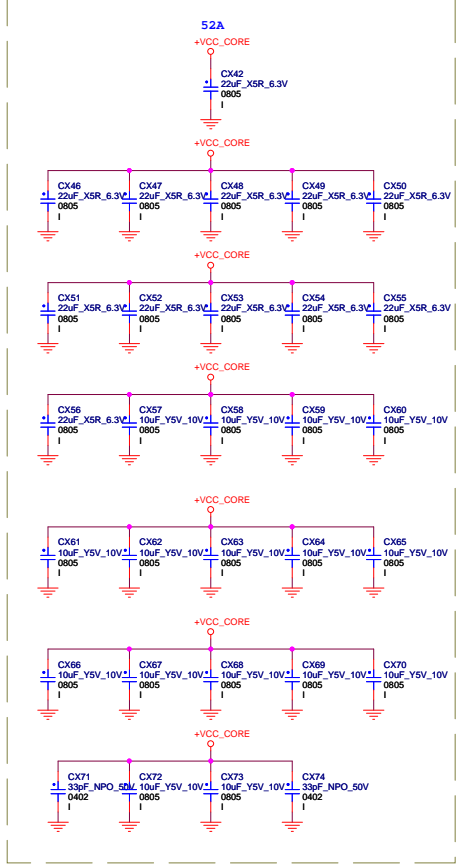
Title: **Calpella (DMI,PEG,FDI)**

Size: Document Number
Custom **STAR (Federer)** Rev: 1.0

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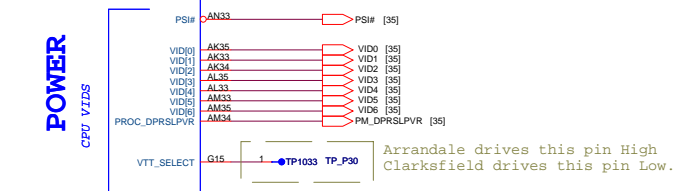
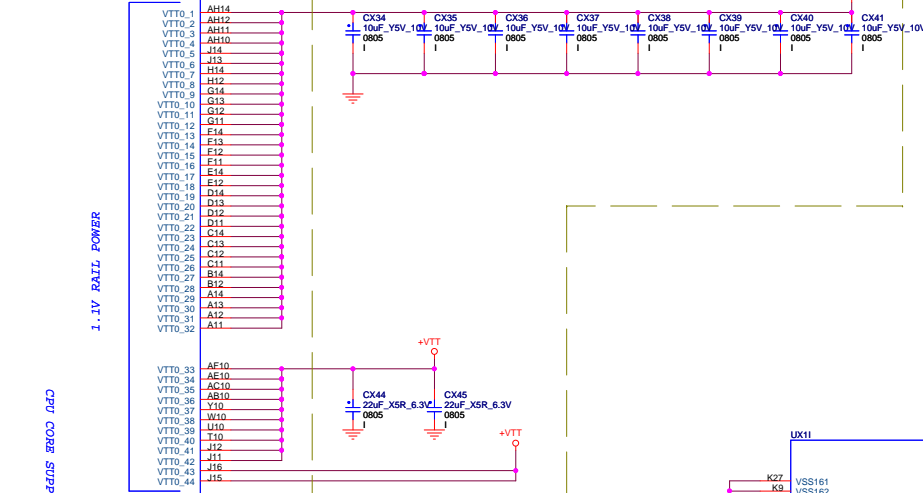
FOR VCC: 12x 0805 22 µF inside cavity, 7x 0805 10 µF under cavity and 9 x 0805 10 µF between inductor and socket on top layer



Socket_INTEL989_15u

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AD35	VCC20
AD34	VCC21
AD33	VCC22
AD32	VCC23
AD31	VCC24
AD30	VCC25
AD29	VCC26
AD28	VCC27
AD27	VCC28
AD26	VCC29
AD25	VCC30
AD24	VCC31
AD23	VCC32
AD22	VCC33
AD21	VCC34
AD20	VCC35
AD19	VCC36
AD18	VCC37
AD17	VCC38
AD16	VCC39
AD15	VCC40
AD14	VCC41
AD13	VCC42
AD12	VCC43
AD11	VCC44
AD10	VCC45
AD09	VCC46
AD08	VCC47
AD07	VCC48
AD06	VCC49
AD05	VCC50
AD04	VCC51
AD03	VCC52
AD02	VCC53
AD01	VCC54
AD00	VCC55
Y31	VCC56
Y30	VCC57
Y29	VCC58
Y28	VCC59
Y27	VCC60
Y26	VCC61
Y25	VCC62
Y24	VCC63
Y23	VCC64
Y22	VCC65
Y21	VCC66
Y20	VCC67
Y19	VCC68
Y18	VCC69
Y17	VCC70
Y16	VCC71
Y15	VCC72
Y14	VCC73
Y13	VCC74
Y12	VCC75
Y11	VCC76
Y10	VCC77
Y09	VCC78
Y08	VCC79
Y07	VCC80
Y06	VCC81
Y05	VCC82
Y04	VCC83
Y03	VCC84
Y02	VCC85
Y01	VCC86
R30	VCC87
R29	VCC88
R28	VCC89
R27	VCC90
R26	VCC91
R25	VCC92
R24	VCC93
R23	VCC94
R22	VCC95
R21	VCC96
R20	VCC97
R19	VCC98
R18	VCC99
R17	VCC100

FOR VTT:
7x 0805 22 µF under cavity
8x 0805 10 µF edge caps



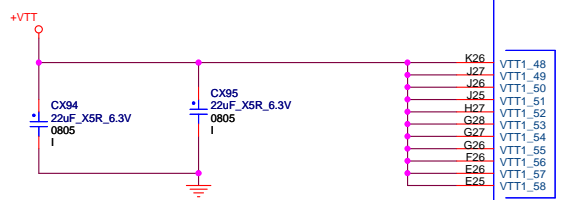
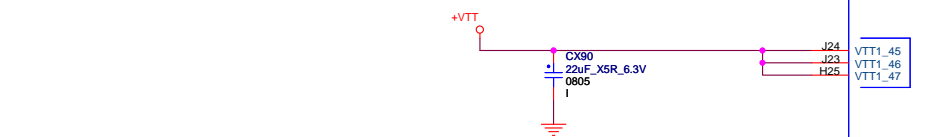
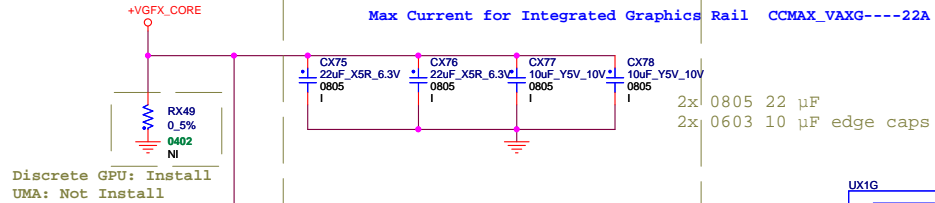
Socket_INTEL989_15u

K27	VSS161
K9	VSS162
K6	VSS163
VSS164	VSS164
J32	VSS165
J30	VSS166
J21	VSS167
J19	VSS168
H35	VSS169
H32	VSS170
H28	VSS171
H26	VSS172
H24	VSS173
H22	VSS174
H18	VSS175
H15	VSS176
H13	VSS177
H11	VSS178
H8	VSS179
H5	VSS180
G34	VSS181
G31	VSS182
G29	VSS183
G20	VSS184
G9	VSS185
G3	VSS186
F27	VSS187
F30	VSS188
F25	VSS189
F22	VSS190
F19	VSS191
F16	VSS192
E35	VSS193
E30	VSS194
E32	VSS195
E29	VSS196
E24	VSS197
E21	VSS198
E18	VSS199
E13	VSS200
E11	VSS201
E8	VSS202
E2	VSS203
D33	VSS204
D30	VSS205
D26	VSS206
D3	VSS207
D9	VSS208
D6	VSS209
D3	VSS210
C34	VSS211
C32	VSS212
C29	VSS213
C28	VSS214
C24	VSS215
C22	VSS216
C20	VSS217
C19	VSS218
C16	VSS219
B31	VSS220
B25	VSS221
B14	VSS222
B16	VSS223
B17	VSS224
B13	VSS225
B11	VSS226
B8	VSS227
B6	VSS228
B4	VSS229
A29	VSS230
A27	VSS231
A23	VSS232
A9	VSS233

Socket_INTEL989_15u

AT20	VSS1	AE34	VSS81
AT17	VSS2	AE33	VSS82
AR31	VSS3	AE32	VSS83
AR28	VSS4	AE31	VSS84
AR26	VSS5	AE30	VSS85
AR24	VSS6	AE29	VSS86
AR23	VSS7	AE28	VSS87
AR20	VSS8	AE27	VSS88
AR17	VSS9	AE26	VSS89
AR15	VSS10	AE25	VSS90
AR12	VSS11	AE24	VSS91
AR8	VSS12	AE23	VSS92
AR6	VSS13	AE22	VSS93
AR3	VSS14	AE21	VSS94
AP20	VSS15	AE20	VSS95
AP17	VSS16	AE19	VSS96
AP13	VSS17	AE18	VSS97
AP10	VSS18	AE17	VSS98
AP7	VSS19	AE16	VSS99
AN34	VSS20	AE15	VSS100
AN31	VSS21	AE14	VSS101
AN29	VSS22	AE13	VSS102
AN27	VSS23	AE12	VSS103
AN25	VSS24	AE11	VSS104
AN23	VSS25	AE10	VSS105
AN22	VSS26	AE9	VSS106
AN21	VSS27	AE8	VSS107
AN20	VSS28	AE7	VSS108
AN19	VSS29	AE6	VSS109
AN18	VSS30	AE5	VSS110
AN17	VSS31	AE4	VSS111
AN16	VSS32	AE3	VSS112
AN15	VSS33	AE2	VSS113
AN14	VSS34	AE1	VSS114
AN13	VSS35	AE0	VSS115
AM2	VSS36	AE-1	VSS116
AL34	VSS37	AE-2	VSS117
AL31	VSS38	AE-3	VSS118
AL23	VSS39	AE-4	VSS119
AL20	VSS40	AE-5	VSS120
AL17	VSS41	AE-6	VSS121
AL12	VSS42	AE-7	VSS122
AL9	VSS43	AE-8	VSS123
AL6	VSS44	AE-9	VSS124
AL3	VSS45	AE-10	VSS125
AK20	VSS46	AE-11	VSS126
AK27	VSS47	AE-12	VSS127
AK25	VSS48	AE-13	VSS128
AK20	VSS49	AE-14	VSS129
AK17	VSS50	AE-15	VSS130
AJ31	VSS51	AE-16	VSS131
AJ23	VSS52	AE-17	VSS132
AJ20	VSS53	AE-18	VSS133
AJ14	VSS54	AE-19	VSS134
AJ11	VSS55	AE-20	VSS135
AJ8	VSS56	AE-21	VSS136
AJ5	VSS57	AE-22	VSS137
AJ2	VSS58	AE-23	VSS138
AH34	VSS59	AE-24	VSS139
AH33	VSS60	AE-25	VSS140
AH32	VSS61	AE-26	VSS141
AH31	VSS62	AE-27	VSS142
AH30	VSS63	AE-28	VSS143
AH29	VSS64	AE-29	VSS144
AH28	VSS65	AE-30	VSS145
AH27	VSS66	AE-31	VSS146
AH26	VSS67	AE-32	VSS147
AH25	VSS68	AE-33	VSS148
AH24	VSS69	AE-34	VSS149
AH23	VSS70	AE-35	VSS150
AH22	VSS71	AE-36	VSS151
AH21	VSS72	AE-37	VSS152
AH20	VSS73	AE-38	VSS153
AH19	VSS74	AE-39	VSS154
AH18	VSS75	AE-40	VSS155
AH17	VSS76	AE-41	VSS156
AH16	VSS77	AE-42	VSS157
AH15	VSS78	AE-43	VSS158
AH14	VSS79	AE-44	VSS159
AH13	VSS80	AE-45	VSS160

+VTT0 → +VTT [9,12,16,17,27,35,36,39]
+VCC_CORE → +VCC_CORE [35]



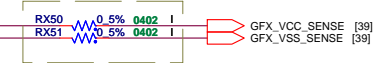
- UX16**
- AT21 VAXG1
 - AT19 VAXG2
 - AT18 VAXG3
 - AT16 VAXG4
 - AR21 VAXG5
 - AR19 VAXG6
 - AR18 VAXG7
 - AR16 VAXG8
 - AN19 VAXG9
 - AN18 VAXG10
 - AN16 VAXG11
 - AN21 VAXG12
 - AN19 VAXG13
 - AN18 VAXG14
 - AN16 VAXG15
 - AN18 VAXG16
 - AM21 VAXG17
 - AM19 VAXG18
 - AM18 VAXG19
 - AM16 VAXG20
 - AL21 VAXG21
 - AL19 VAXG22
 - AL18 VAXG23
 - AL16 VAXG24
 - AK21 VAXG25
 - AK19 VAXG26
 - AK18 VAXG27
 - AK16 VAXG28
 - AJ21 VAXG29
 - AJ19 VAXG30
 - AJ18 VAXG31
 - AJ16 VAXG32
 - AH19 VAXG33
 - AH18 VAXG34
 - AH16 VAXG35
 - AH16 VAXG36

- GRAPHICS**
- SENSE LINES**
- VAXG_SENSE
 - VSSAXG_SENSE
 - GFX_VID[0]
 - GFX_VID[1]
 - GFX_VID[2]
 - GFX_VID[3]
 - GFX_VID[4]
 - GFX_VID[5]
 - GFX_VID[6]
 - GFX_VR_EN
 - GFX_DPRSLPVR
 - GFX_IMON

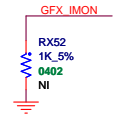
- POWER**
- DDR3 - 1.5V RAILS**
- VDDQ01
 - VDDQ02
 - VDDQ03
 - VDDQ04
 - VDDQ05
 - VDDQ06
 - VDDQ07
 - VDDQ08
 - VDDQ09
 - VDDQ10
 - VDDQ11
 - VDDQ12
 - VDDQ13
 - VDDQ14
 - VDDQ15
 - VDDQ16
 - VDDQ17
 - VDDQ18
- 1.1V**
- VTT1_63
 - VTT1_64
 - VTT1_65
 - VTT1_66
 - VTT1_67
 - VTT1_68
- 1.8V**
- VCCPLL1
 - VCCPLL2
 - VCCPLL3

- +VTT0 → +VTT [9,11,16,17,27,35,36,39]
- +VGFX_CORE0 → +VGFX_CORE [39]
- +V1.5_VDDQ0 → +V1.5_VDDQ [9,17,27,29,38]
- +V1.8S0 → +V1.8S [17,37,38]

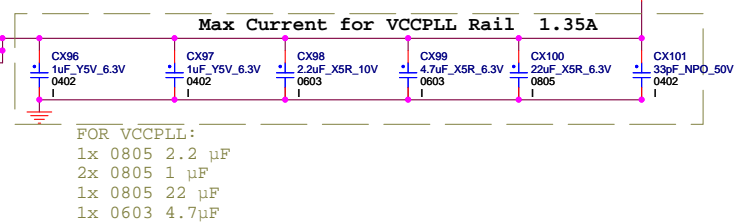
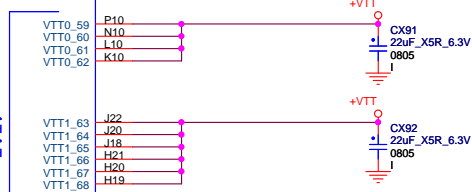
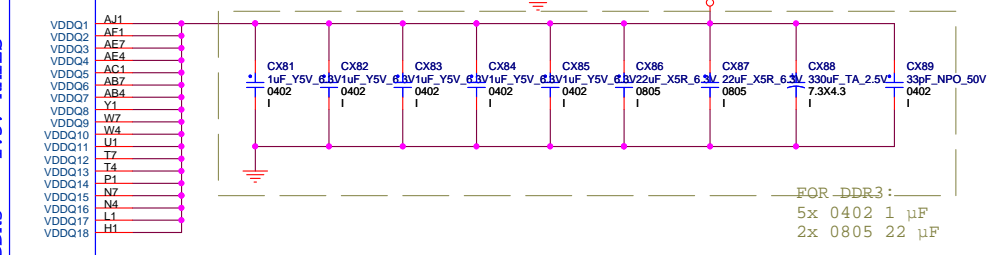
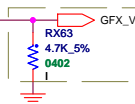
Discrete GPU: Not Install
UMA: Install



Discrete GPU: Install
UMA: Not Install



Discrete GPU: Not Install
UMA: Install



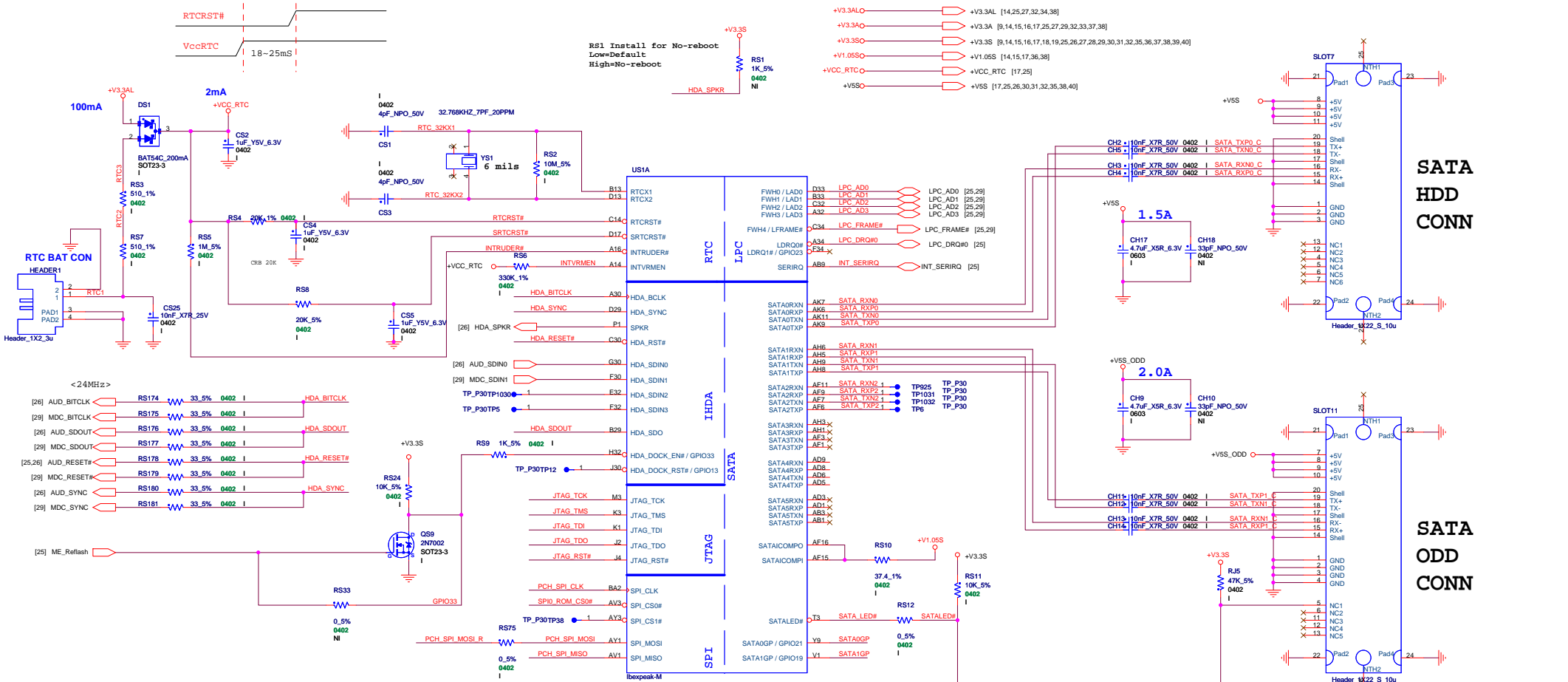
Socket_INTEL989_15u

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Foxconn eMS Inc.
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Title: **Calpella (GRAPHICS POWER)**

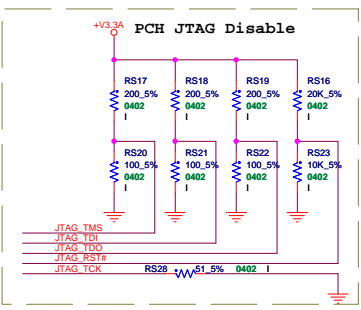
Size: Custom Document Number Rev: 1.0

Page Modified: Thursday, March 18, 2010 17:34:40 (UTC/GMT) Sheet 12 of 40

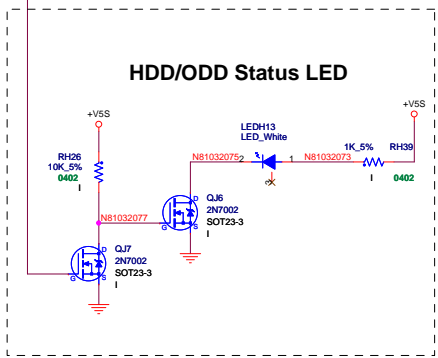
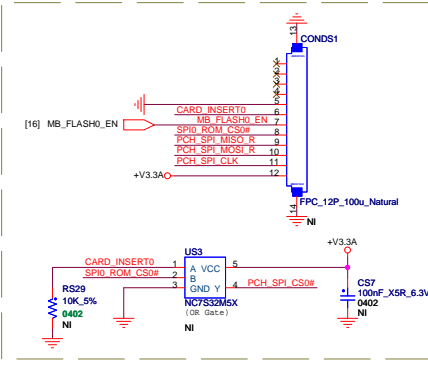


SATA HDD CONN

SATA ODD CONN

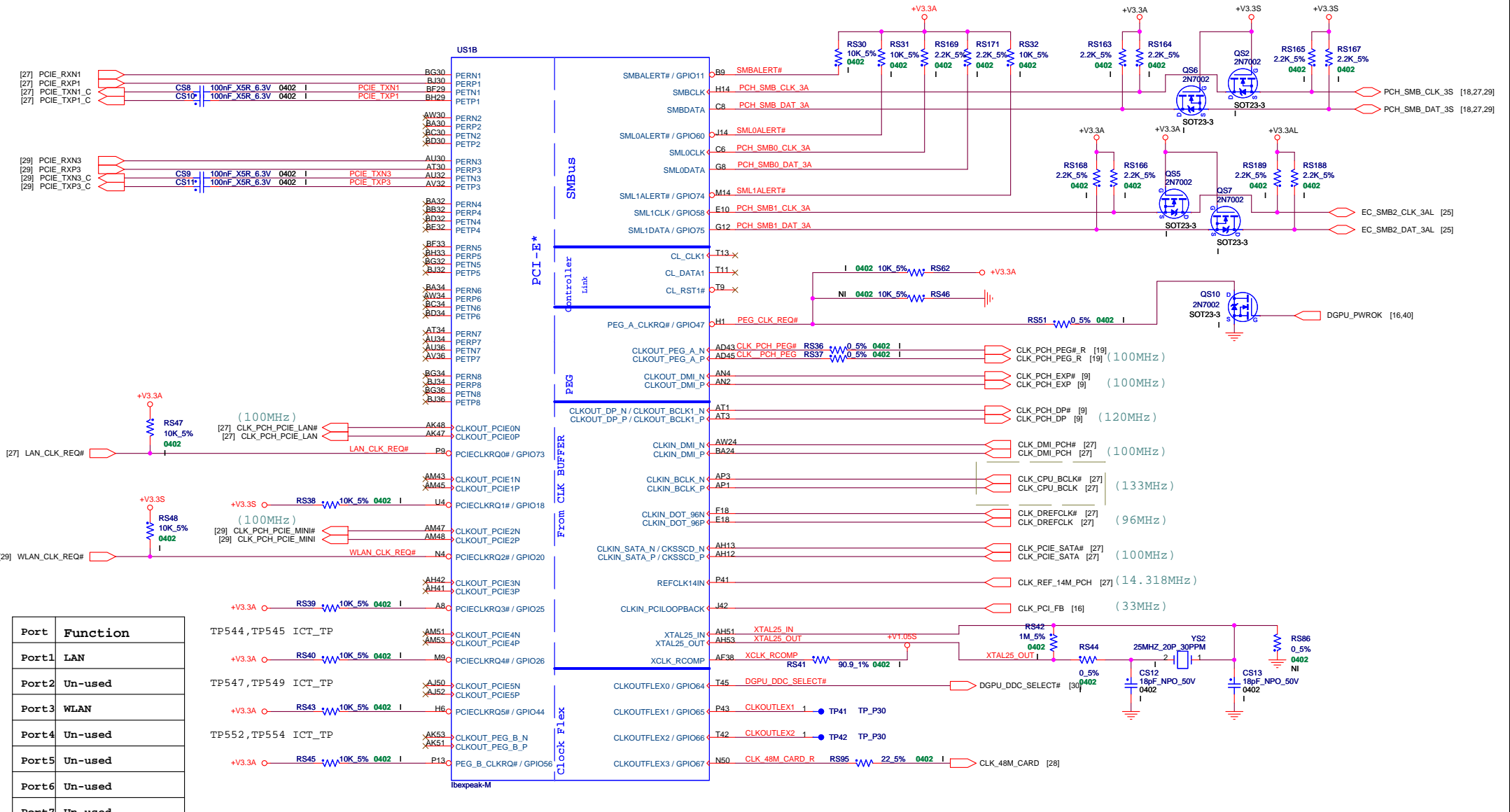


EXTERNAL SPI0 ROM INTERFACE (FOR US2)



Power pin current max. 1300 mA (less 2ms)

+V3.3AL [13,25,27,32,34,38]
 +V3.3A [9,13,15,16,17,25,27,29,32,33,37,38]
 +V3.3S [9,13,15,16,17,18,19,25,26,27,28,29,30,31,32,35,36,37,38,39,40]
 +V1.05S [13,15,17,36,38]

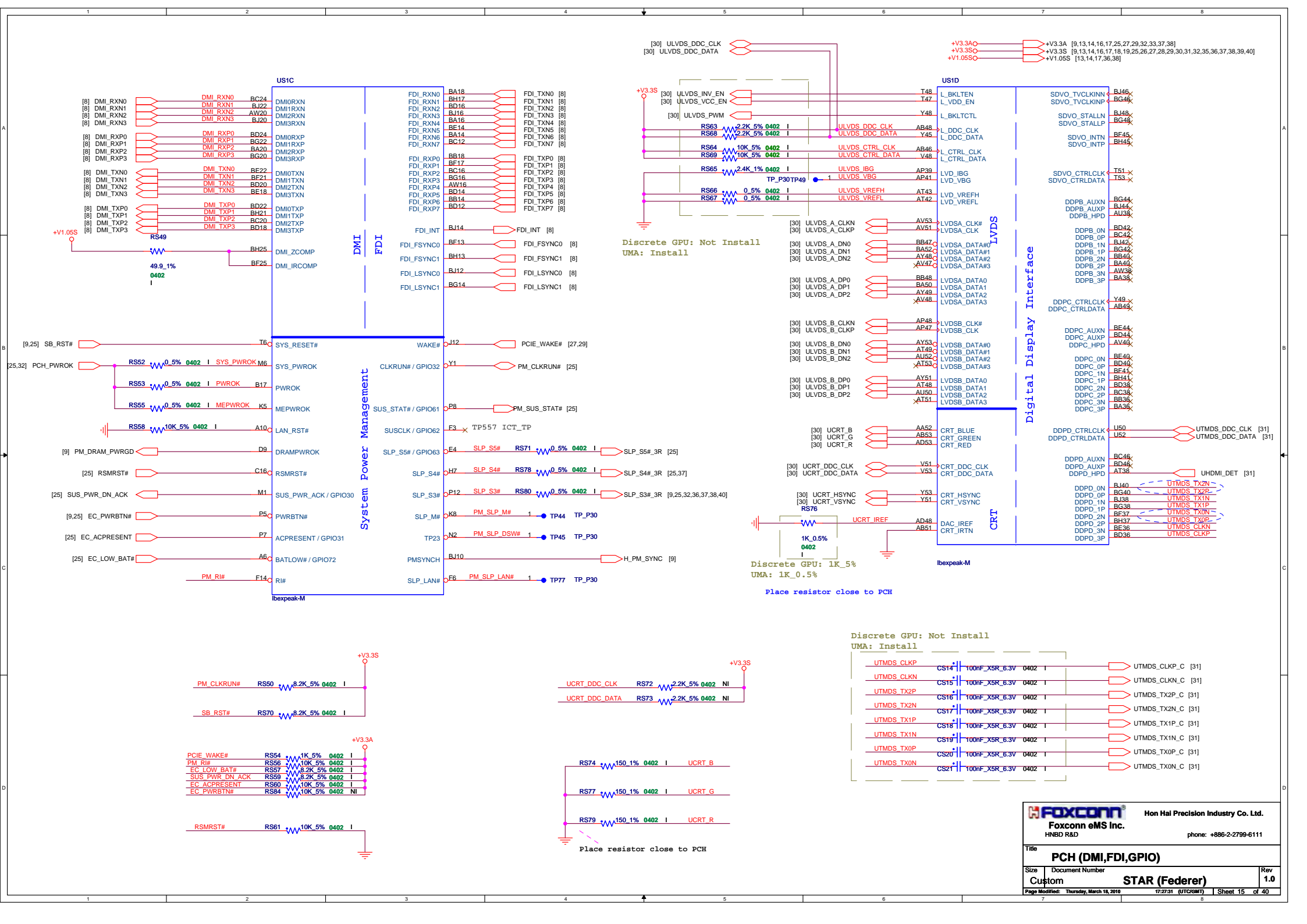


Port	Function
Port1	LAN
Port2	Un-used
Port3	WLAN
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used
Port8	Un-used

PCI-E Port Table

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Title: PCH (PCI-E,SMBUS,CLK)
 Size: Document Number
 Custom: STAR (Federer) Rev: 1.0
 Page Modified: Thursday, March 18, 2010 17:24:41 (UTC+8MT) Sheet 14 of 40



US1C

US1D

System Power Management

Digital Display Interface

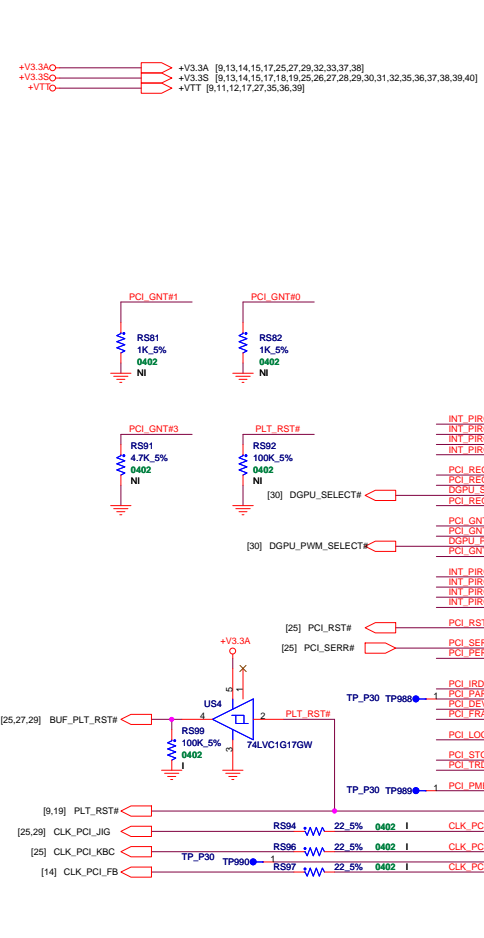
**Discrete GPU: Not Install
UMA: Install**

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Foxconn eMS Inc. HNBND R&D phone: +886-2-2799-6111

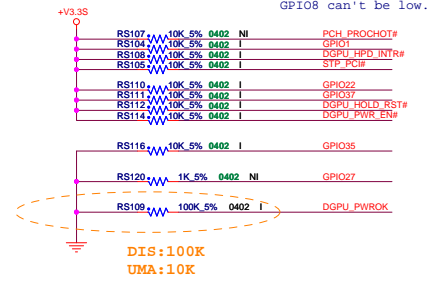
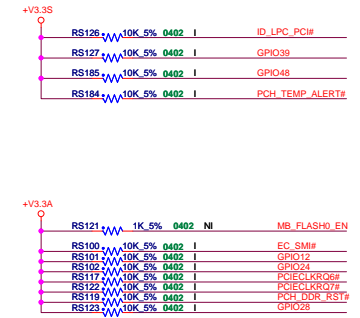
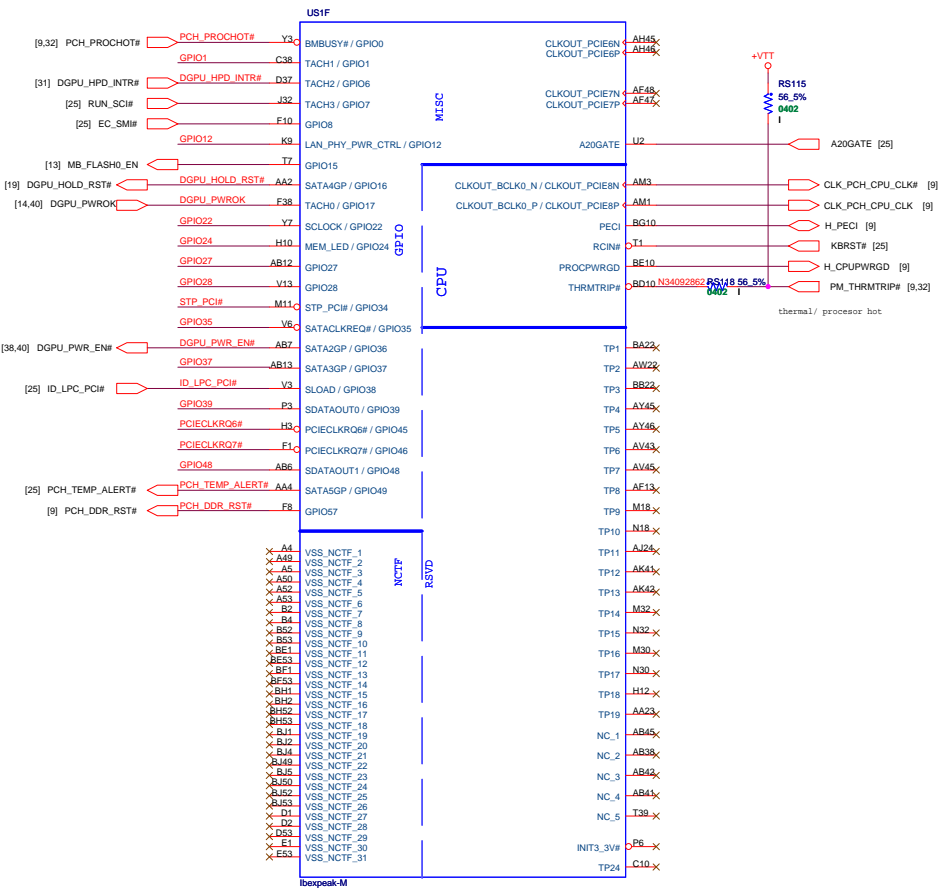
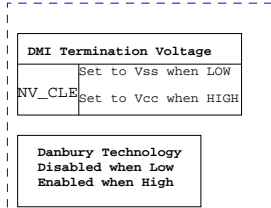
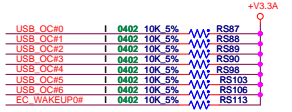
Title: **PCH (DMI,FDI,GPIO)**

Size: Document Number
 Custom **STAR (Federer)** Rev 1.0

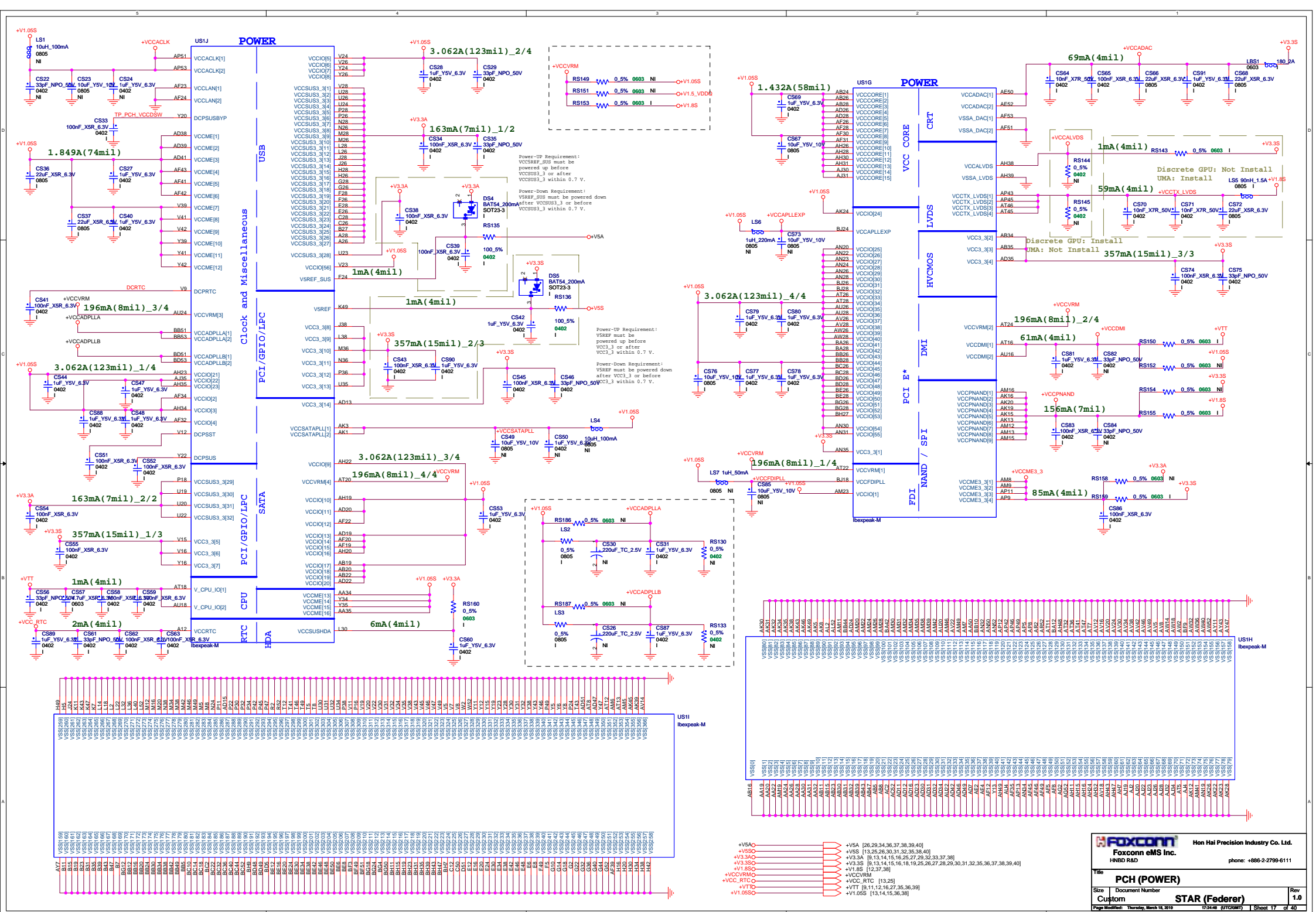
Page Modified: Thursday, March 18, 2010 17:27:31 (UTC+8GMT) Sheet 15 of 40



USB PORT	Function	OC pin
PORT-0	Ext. USB 0	
PORT-1	Ext. USB 1	
PORT-2	Ext. USB 2	
PORT-3		
PORT-4		
PORT-5		
PORT-6		
PORT-7		
PORT-8	Bluetooth	
PORT-9		
PORT-10	Camera	
PORT-11	WLAN/WiMAX	
PORT-12	Card reader	
PORT-13		



DVT Ask EC if we need to change GPIO pin.
GPIO8 can't be low.



3.062A(123mil)_2/4

Power-Up Requirement:
VSRFP must be powered up before VCC3_3 or after VCC3_3 within 0.7 V.

Power-Down Requirement:
VSRFP must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

3.062A(123mil)_4/4

Power-Up Requirement:
VSRFP must be powered up before VCC3_3 or after VCC3_3 within 0.7 V.

Power-Down Requirement:
VSRFP must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

3.062A(123mil)_3/4

Power-Up Requirement:
VSRFP must be powered up before VCC3_3 or after VCC3_3 within 0.7 V.

Power-Down Requirement:
VSRFP must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

1.96mA(8mil)_1/4

Power-Up Requirement:
VSRFP must be powered up before VCC3_3 or after VCC3_3 within 0.7 V.

Power-Down Requirement:
VSRFP must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

1.96mA(8mil)_2/4

Power-Up Requirement:
VSRFP must be powered up before VCC3_3 or after VCC3_3 within 0.7 V.

Power-Down Requirement:
VSRFP must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

1.96mA(8mil)_3/4

Power-Up Requirement:
VSRFP must be powered up before VCC3_3 or after VCC3_3 within 0.7 V.

Power-Down Requirement:
VSRFP must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

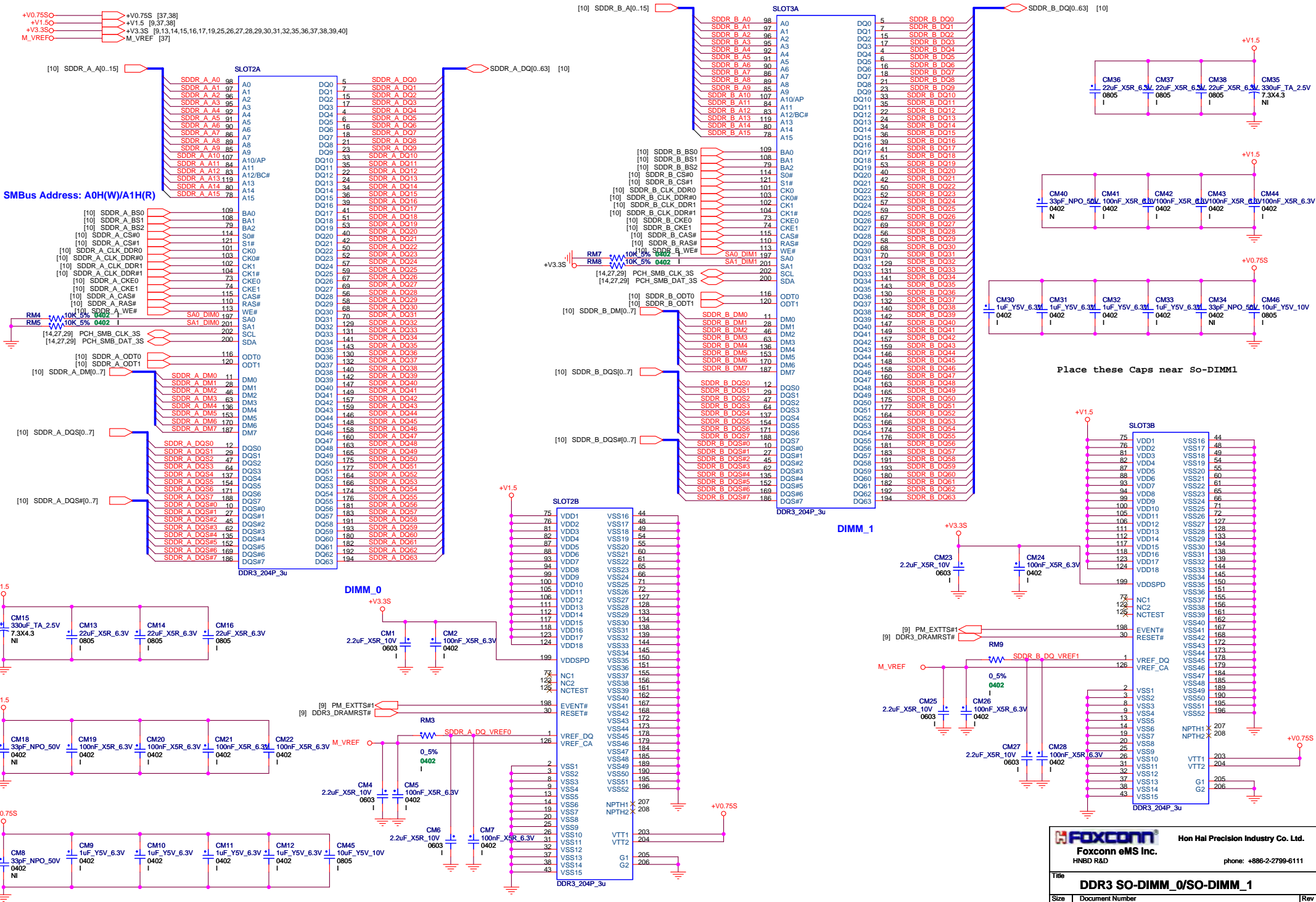
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File: **PCH (POWER)**

Size: Custom Document Number: STAR (Fedeer)

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- +V5A [26,29,34,36,37,38,39,40]
- +V5S [13,25,26,30,31,32,35,38,40]
- +V3.3A [9,13,14,15,16,25,27,29,32,33,37,38]
- +V3.3S [13,14,15,16,18,19,25,26,27,28,29,30,31,32,35,36,37,38,39,40]
- +V1.8S [12,37,38]
- +VCCVCRM [13,25]
- +VCC_RTC [13,25]
- +VTT [9,11,12,16,27,35,36,39]
- +V1.05SO [13,14,15,36,39]



SMBus Address: A0H(W)/A1H(R)

Place these Caps near So-DIMM1

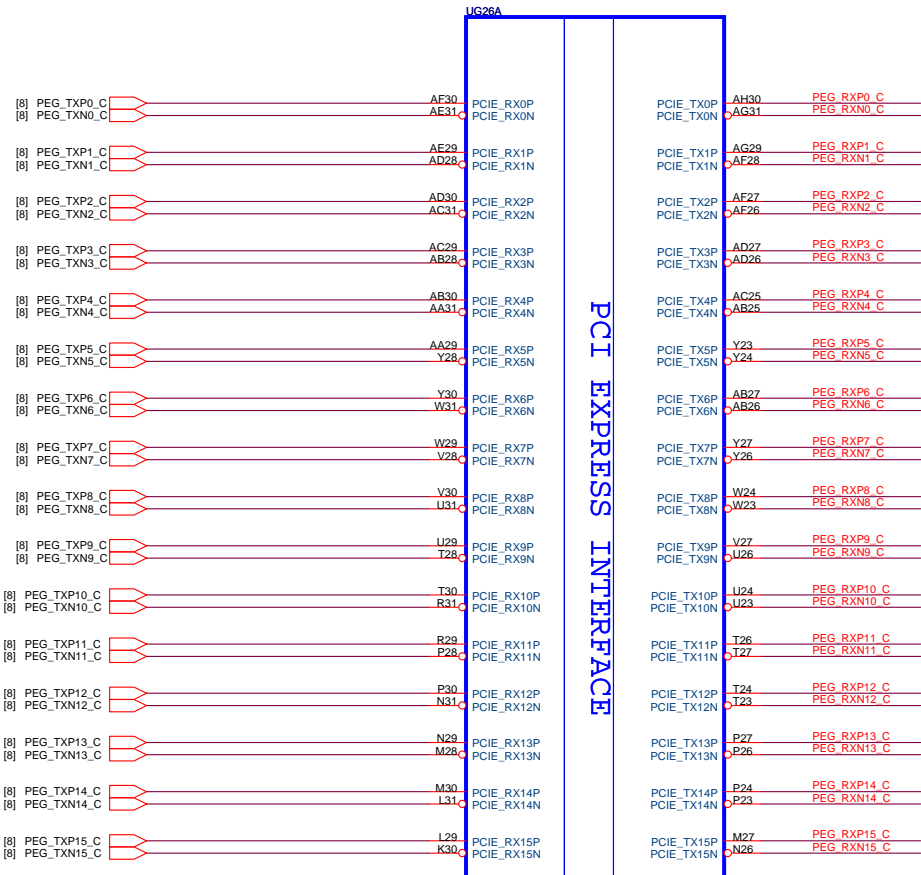
Place between two SO-DIMM

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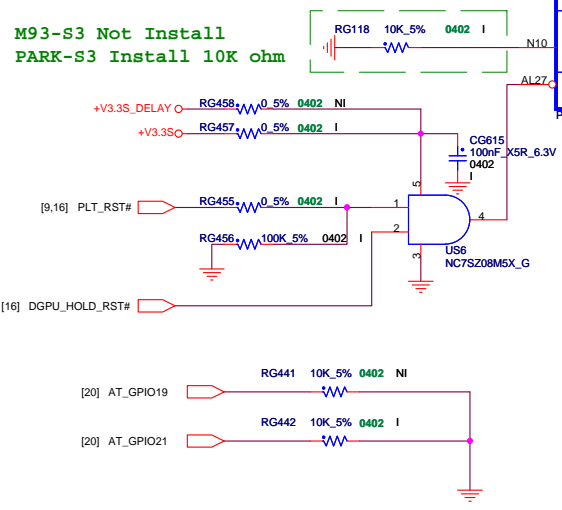
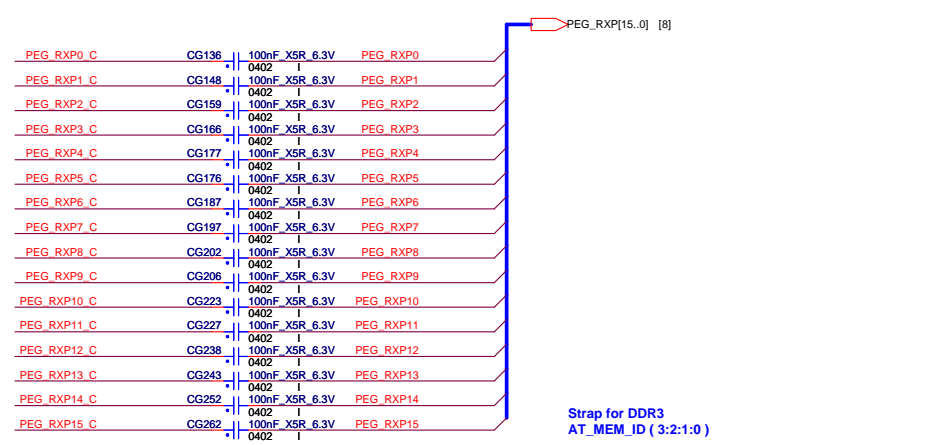
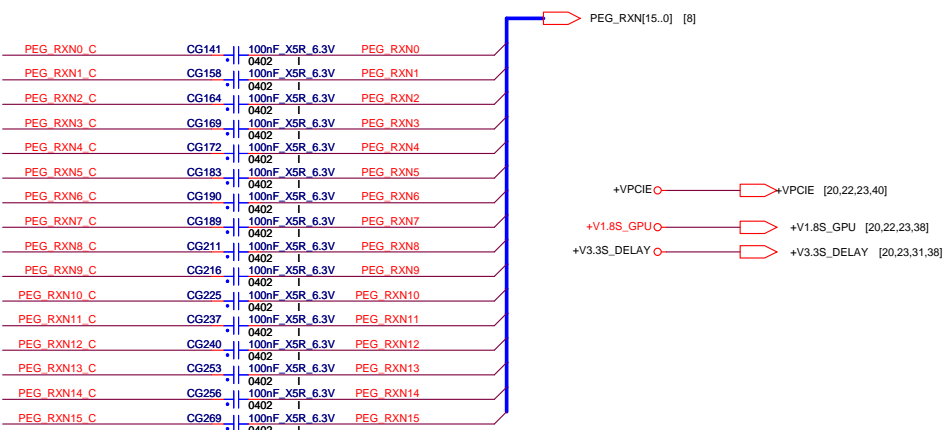
Title: **DDR3 SO-DIMM_0/DO-DIMM_1**

Size: Document Number
 Custom **STAR (Federer)** Rev 1.0

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PCI EXPRESS INTERFACE



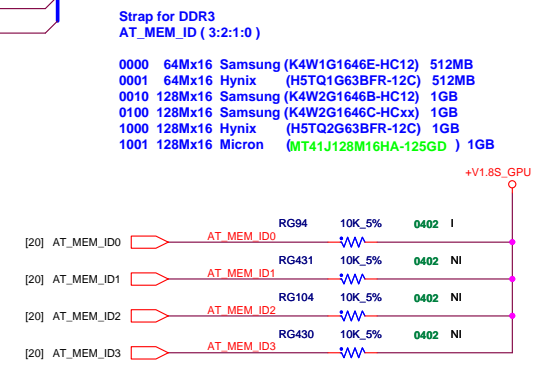
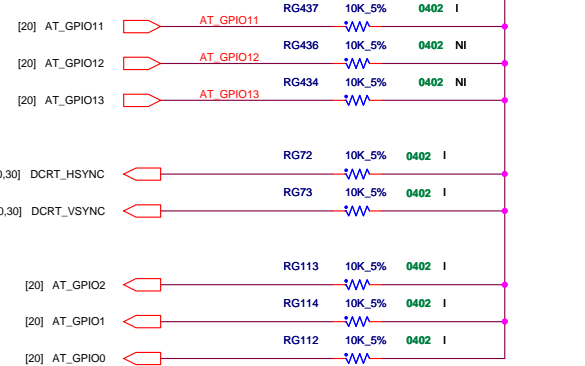
If no ROM attached, GPIO[13:12:11] ; CONFIG(2:0) controls the memory aperture size.

Reserved	011
512MB	001

HSYNC , VSYNC
AUD[1] , AUD[0]

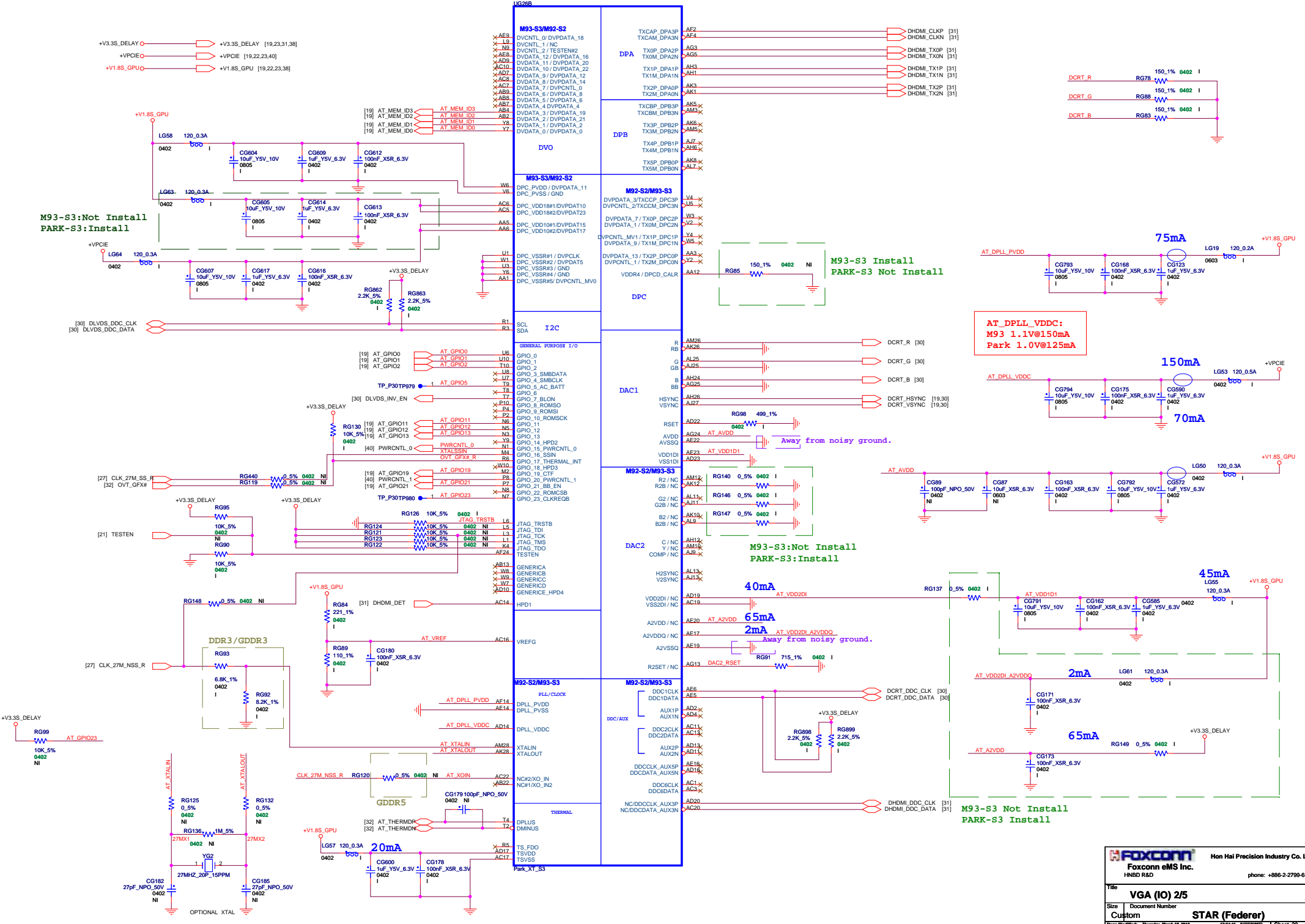
0,0 No audio function
0,1 Audio for DisplayPort and HDMI if dongle is detected
1,0 Audio for DisplayPort only
1,1 Audio for both DisplayPort and HDMI

GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2 : PCIE GEN2 ENABLED



- Strap for DDR3
AT_MEM_ID (3:2:1:0)
- 0000 64Mx16 Samsung (K4W1G1646E-HC12) 512MB
 - 0001 64Mx16 Hynix (H5TQ1G63BFR-12C) 512MB
 - 0010 128Mx16 Samsung (K4W2G1646B-HC12) 1GB
 - 0100 128Mx16 Samsung (K4W2G1646C-HCxx) 1GB
 - 1000 128Mx16 Hynix (H5TQ2G63BFR-12C) 1GB
 - 1001 128Mx16 Micron (MT41J128M16HA-125GD) 1GB

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VGA (PCI-E/STRAP) 1/5			
Size	Document Number		Rev
Custom	STAR (Federer)		1.0
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M93-S3:Not Install
PARK-S3: Install

M93-S3 Install
PARK-S3 Not Install

M93-S3:Not Install
PARK-S3: Install

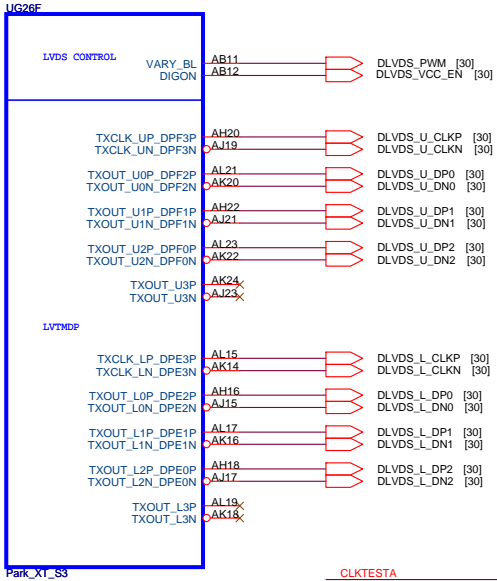
M93-S3 Not Install
PARK-S3 Install

AT_DPLL_VDDC:
M93 1.1V@150mA
Park 1.0V@125mA

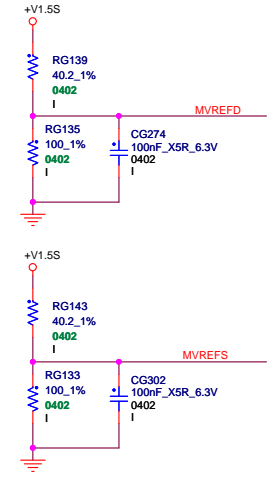


+V1.5S [23,24,38,40]

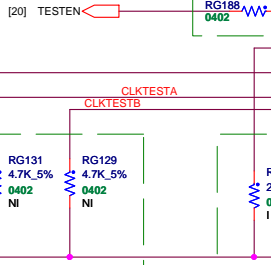
	M93_XT_S3	Park_XT_S3
RG139	100_1%	40.2_1%
MVREFD	0.75V	1.07V
RG143	100_1%	40.2_1%
MVREFS	0.75V	1.07V



PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



M93-S3 No Install
PARK-S3 Install

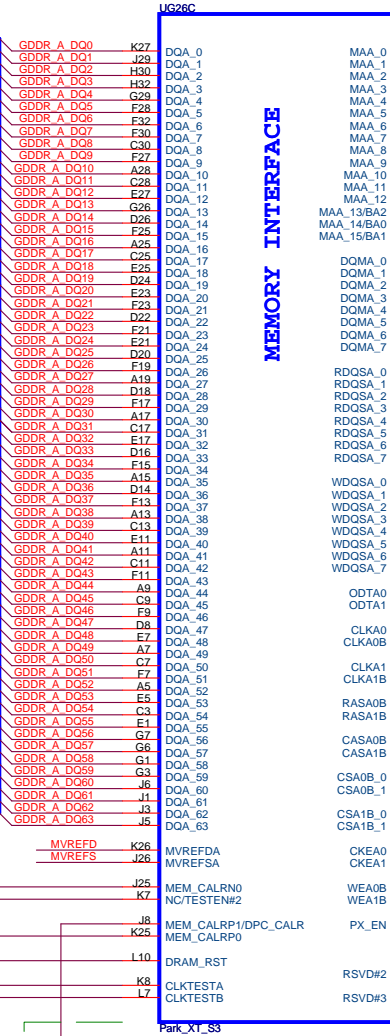


M93-S3 Install
PARK-S3 Not Install

M93-S3 Not Install
PARK-S3 Install

M93-S3 Install 240 ohm
PARK-S3 Install 150 ohm

	M93-S3	PARK-S3
RG141	DNI	10K
RG142	0R	680R
RG145	2.2K	DNI
CG781	2.2nF	68pF



MEMORY INTERFACE

M93-S3 No Install
PARK-S3 Install

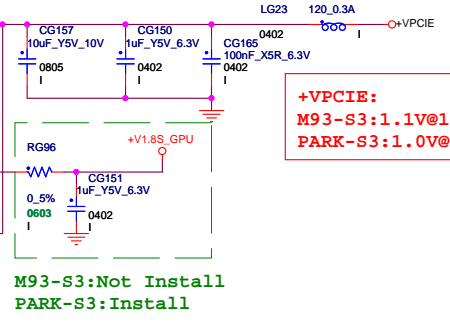
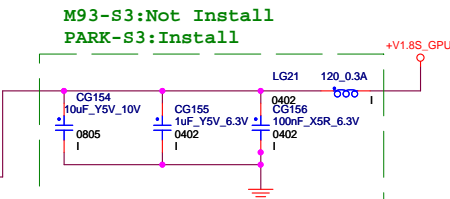
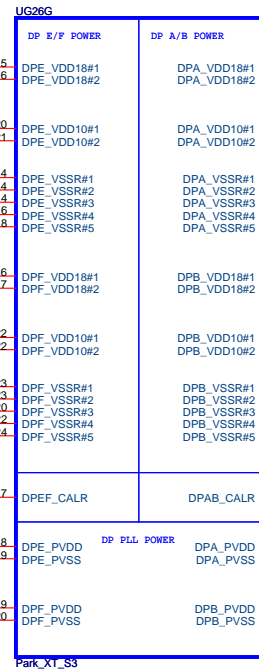
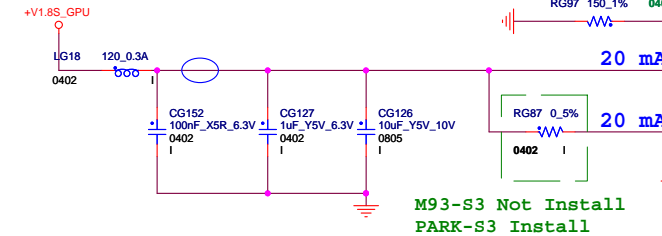
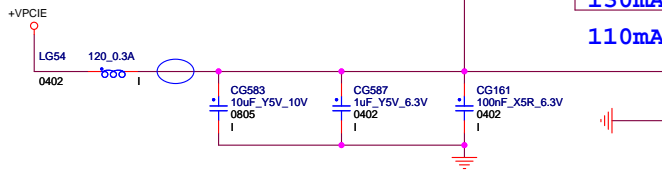
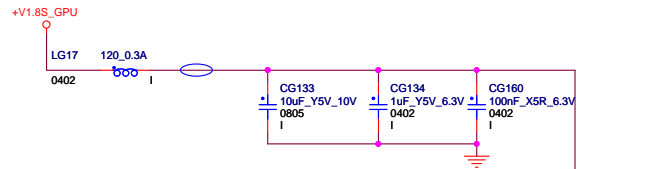
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Title: **VGA (DDR3) 3/5**

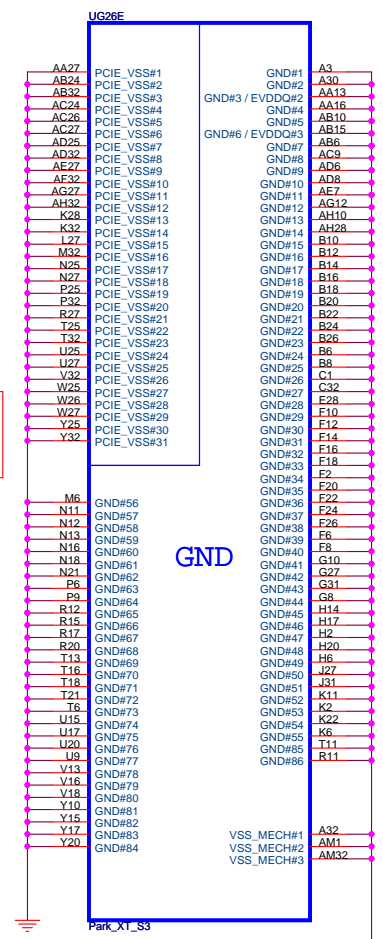
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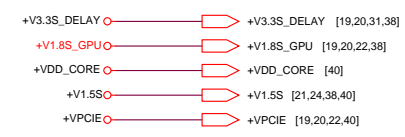
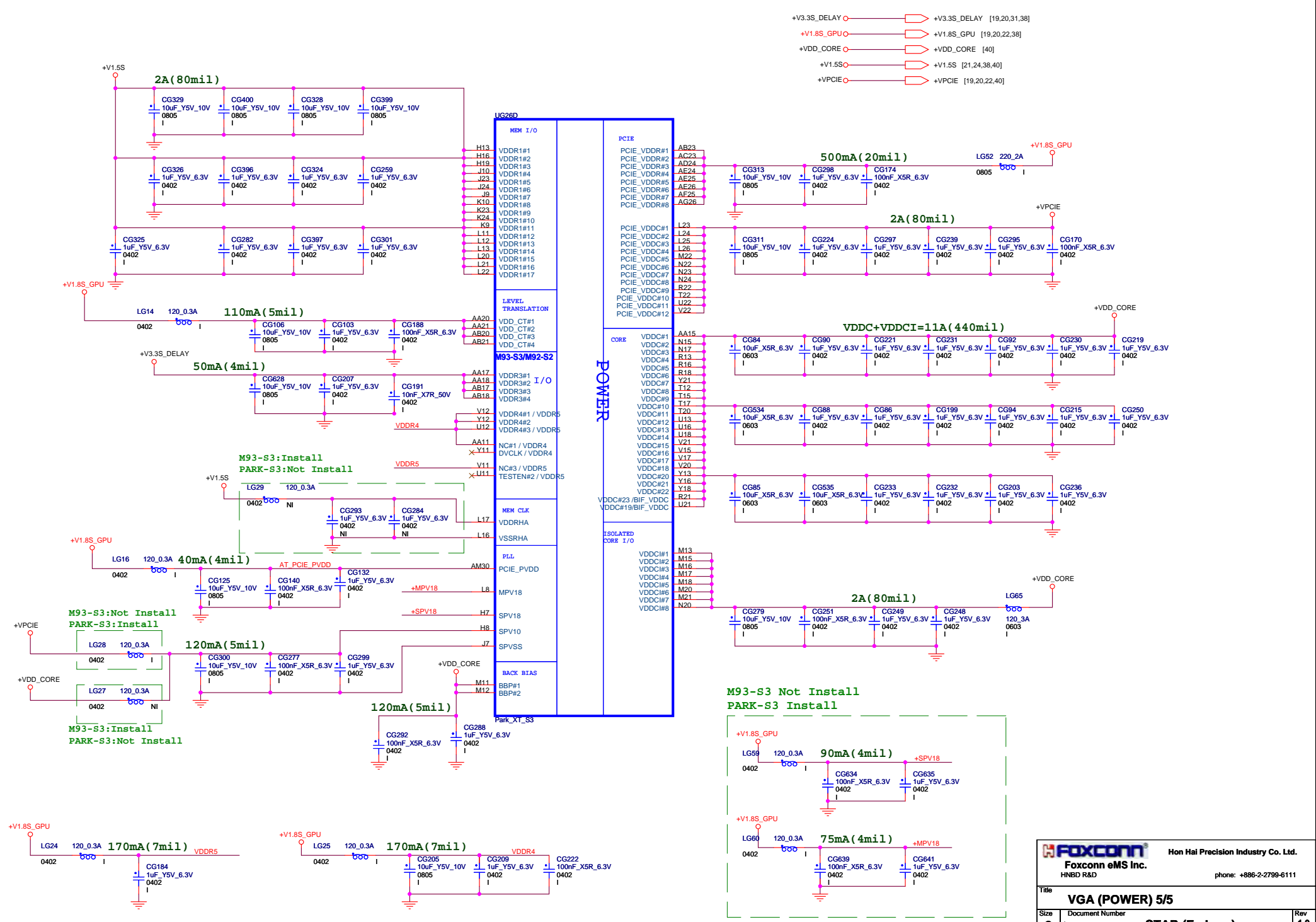
Rev: **1.0**
STAR (Federer)

+VPCIE [19,20,23,40]
 +V1.8S_GPU [19,20,23,38]

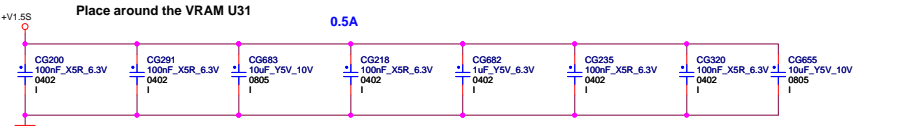
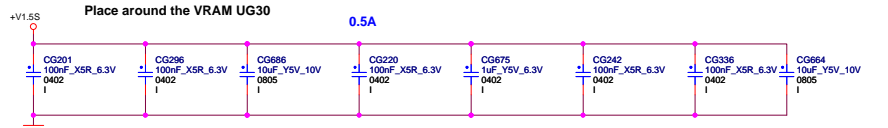
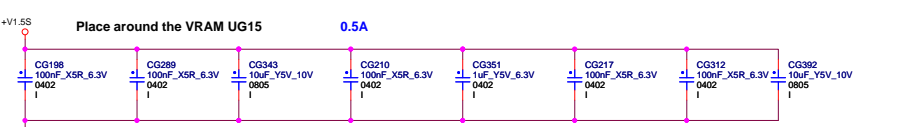
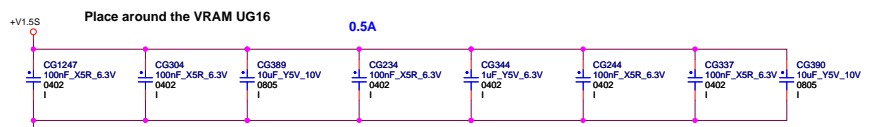
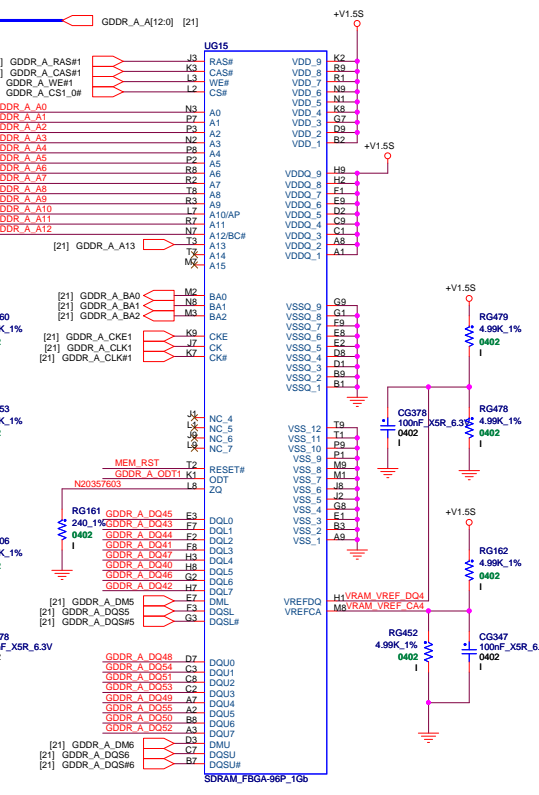
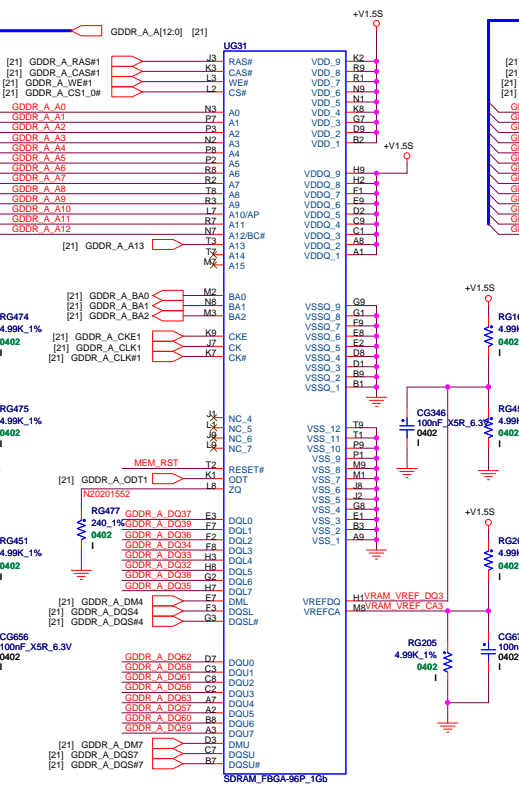
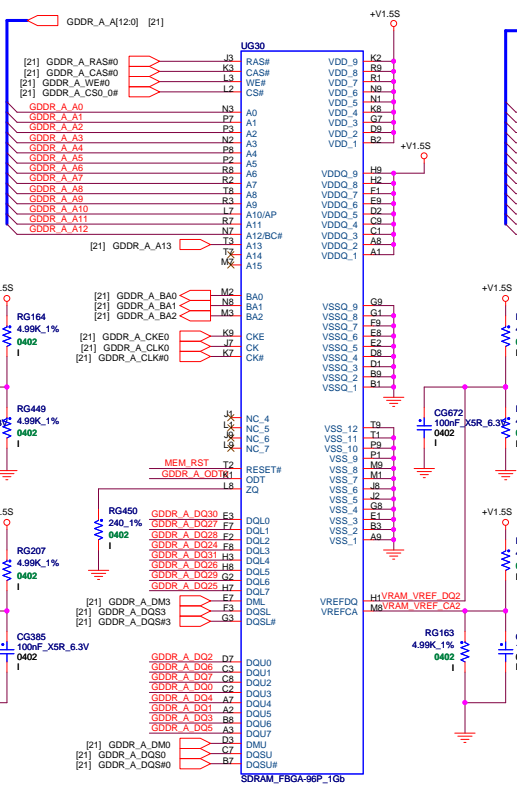
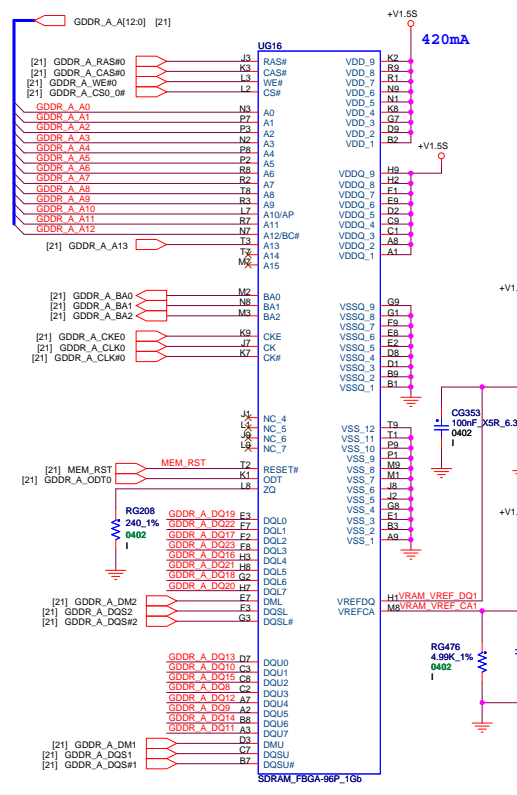


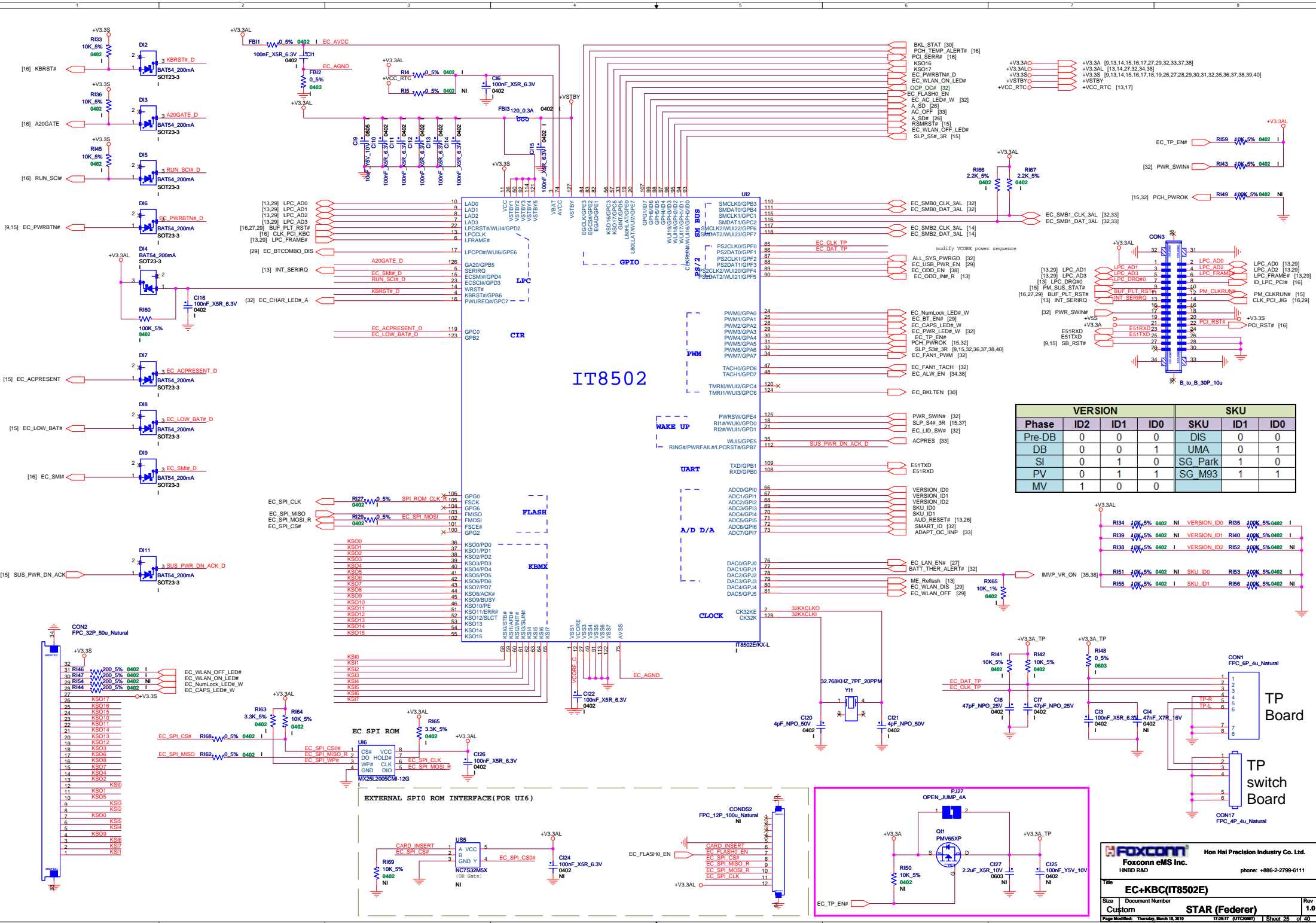
+VPCIE:
 M93-S3:1.1V@110mA
 PARK-S3:1.0V@200mA





+V1.5S [21,23,38,40]

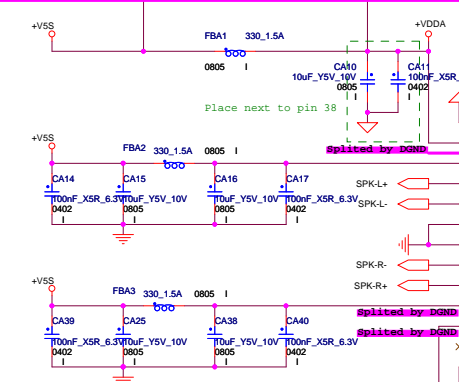
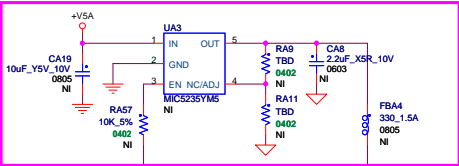




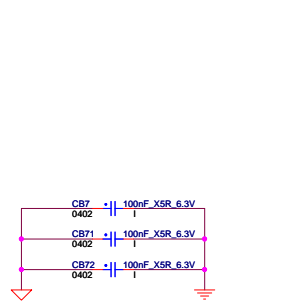
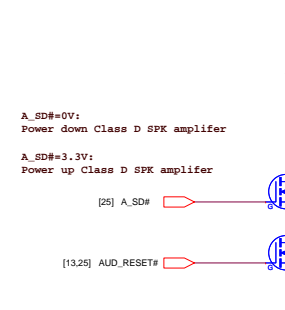
Phase	VERSION			SKU		
	ID2	ID1	ID0	SKU ID1	ID1	ID0
Pre-DB	0	0	0	DIS	0	0
DB	0	0	1	UMA	0	1
SI	0	1	0	SG Park	1	0
PV	0	1	1	SG M93	1	1
MV	1	0	0			

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Reserved LDO circuitry for +VDDA power source



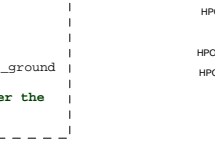
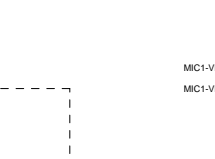
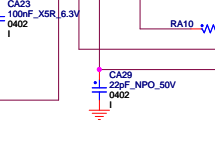
<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge



- +V3.3S
- +V5S
- +VDDA
- INT_MIC_REF

ALC270A-GR
(Viate Premium Version)
Thermal Pad
5 x 6 mm
9 Via Array

ANALOG
DIGITAL
(Include Thermal Pad)

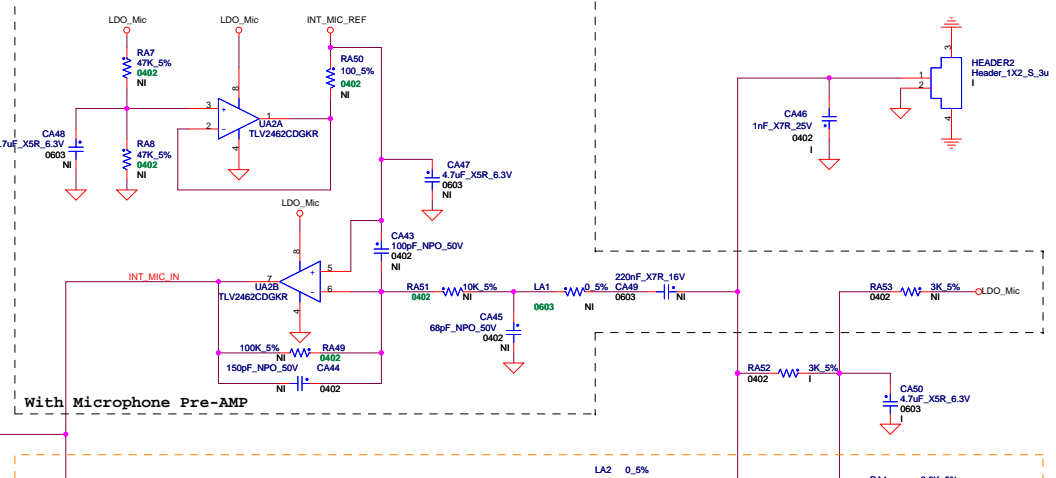


- +V3.3S
- +V5S
- +VDDA
- INT_MIC_REF

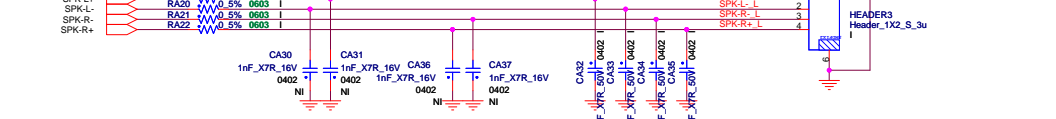
With Microphone Pre-AMP

Reserved for without Microphone Pre-AMP

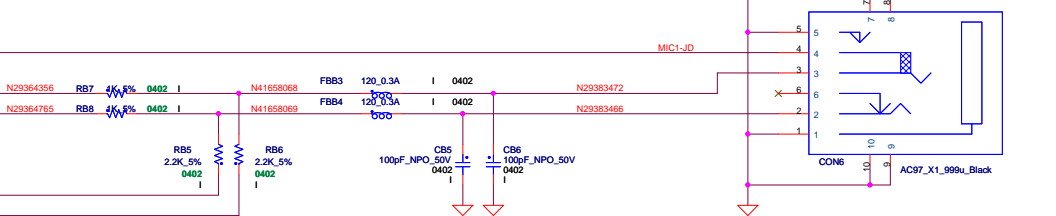
INTERNAL MICROPHONE



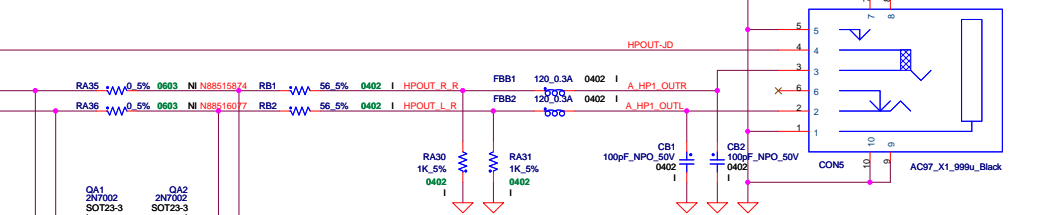
INTERNAL SPEAKER

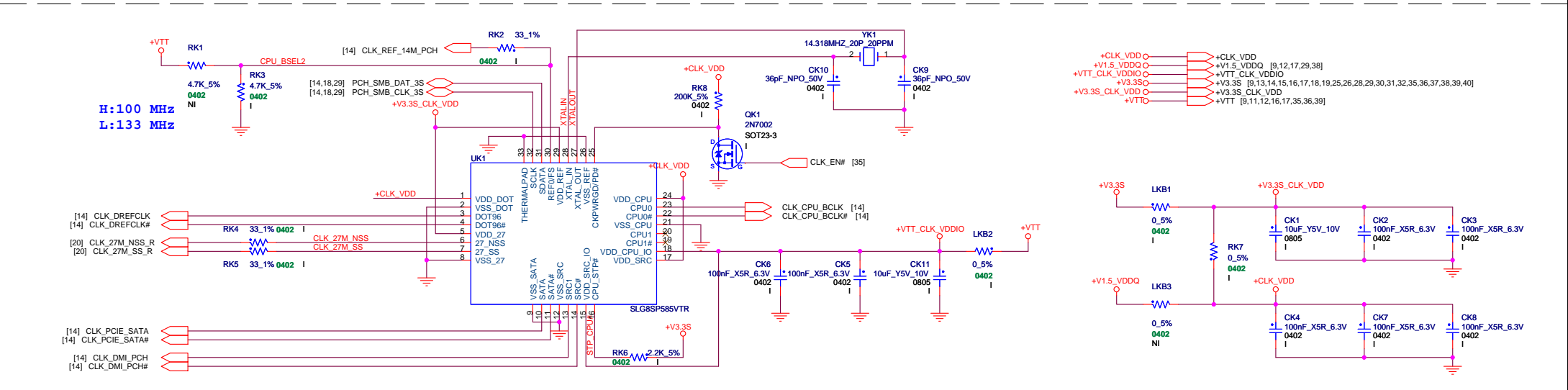
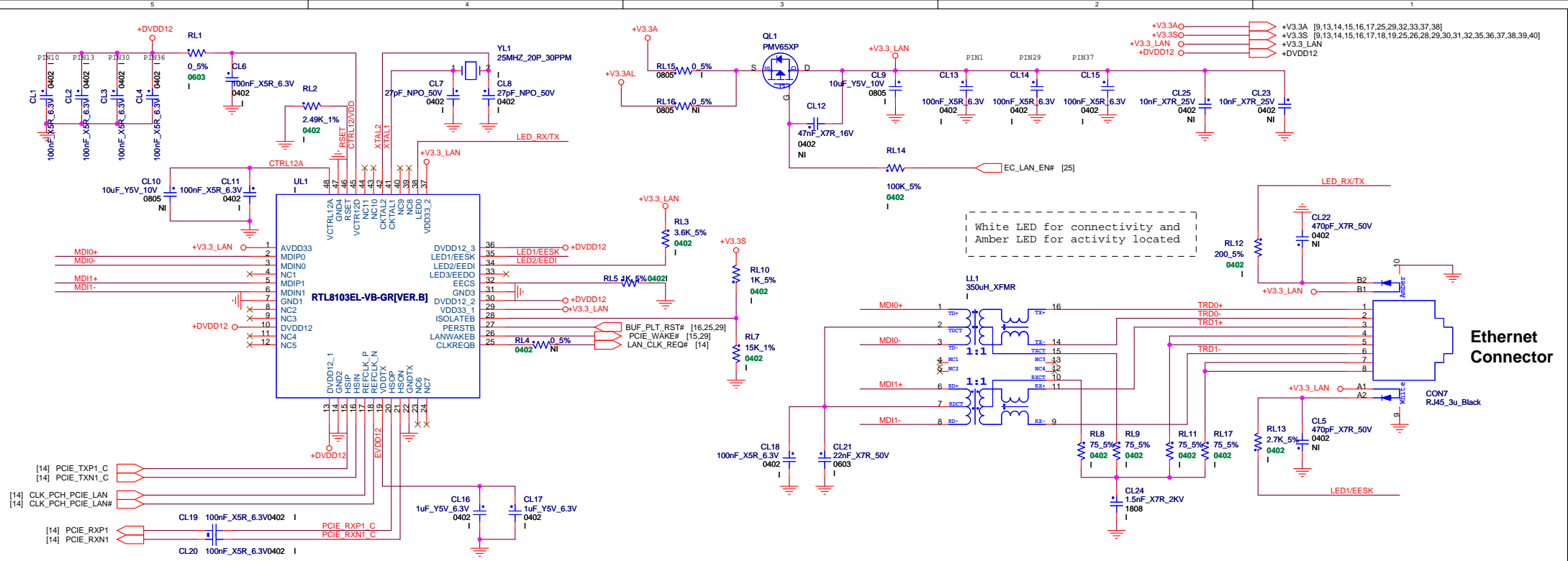


EXTERNAL MIC JACK



HEADPHONE Jack





FSP Table

FS	CPU (PCH-->CPU)	Power On	SRC (DMI) (PCH-->CPU)	SATA (PCH)	DOT96 (PCH)	27MHz (GPU)	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

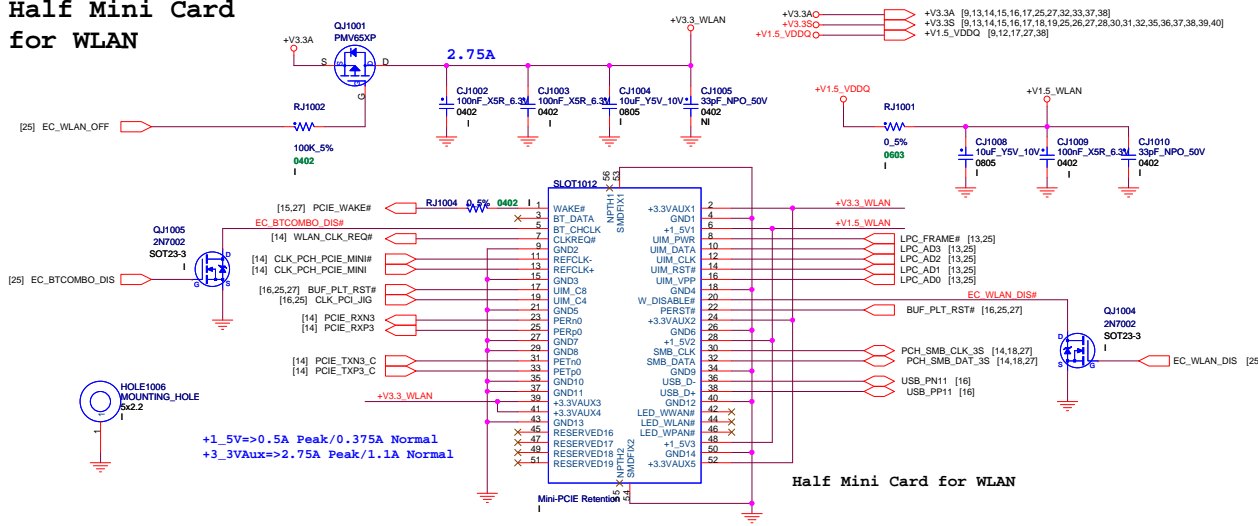
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Title: **LAN (RTL8103EL)CLOCK GEN**

Size: Document Number
 Custom **STAR (Federer)** Rev 1.0

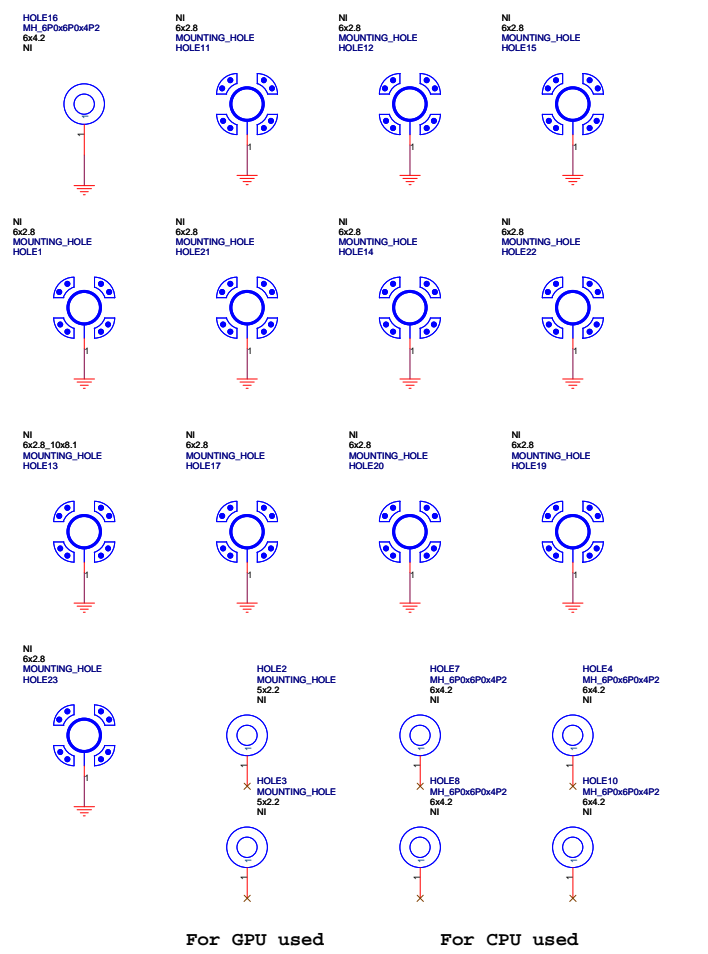
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Half Mini Card for WLAN

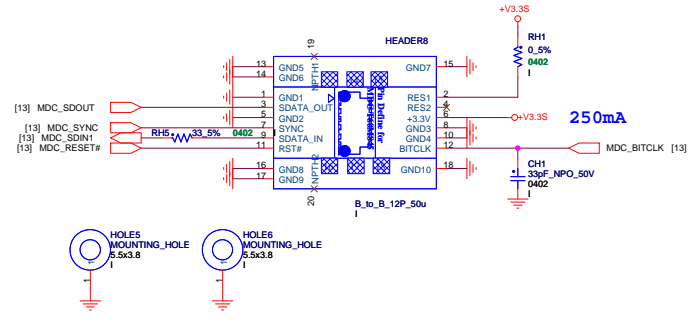


Half Mini Card for WLAN

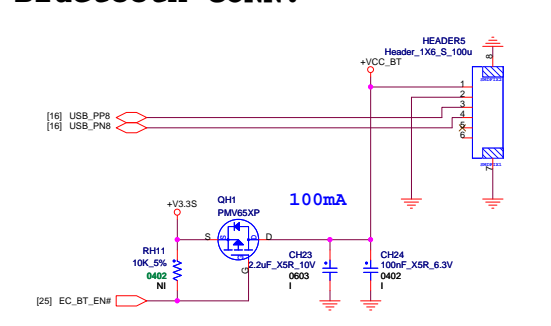
MOUNTING HOLE



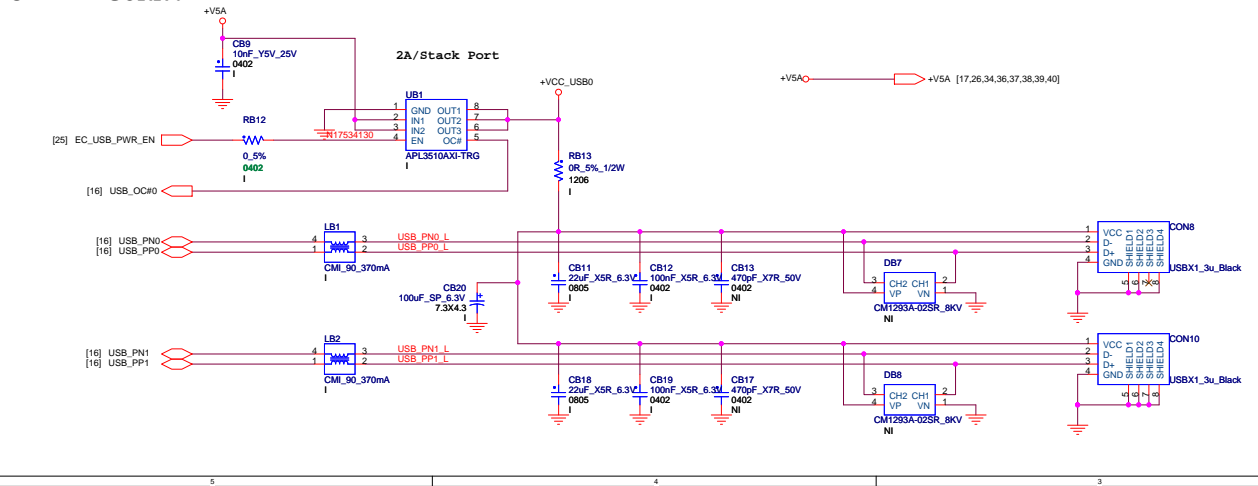
MDC CONN.



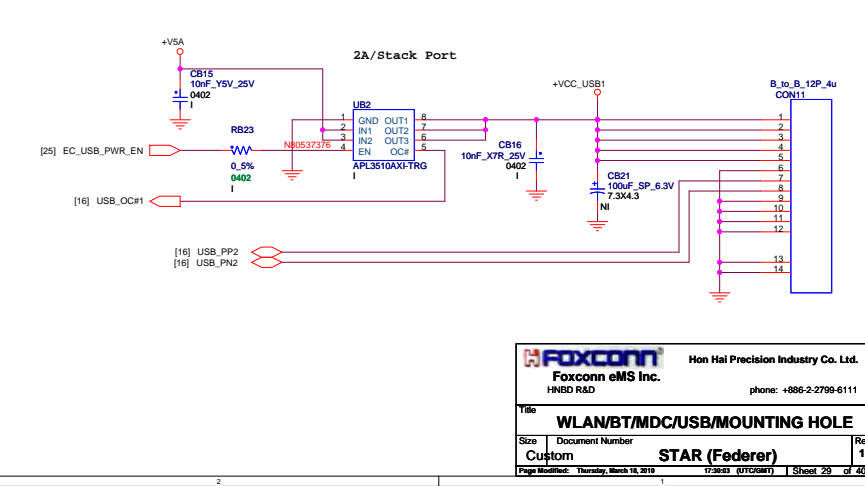
Bluetooth CONN.



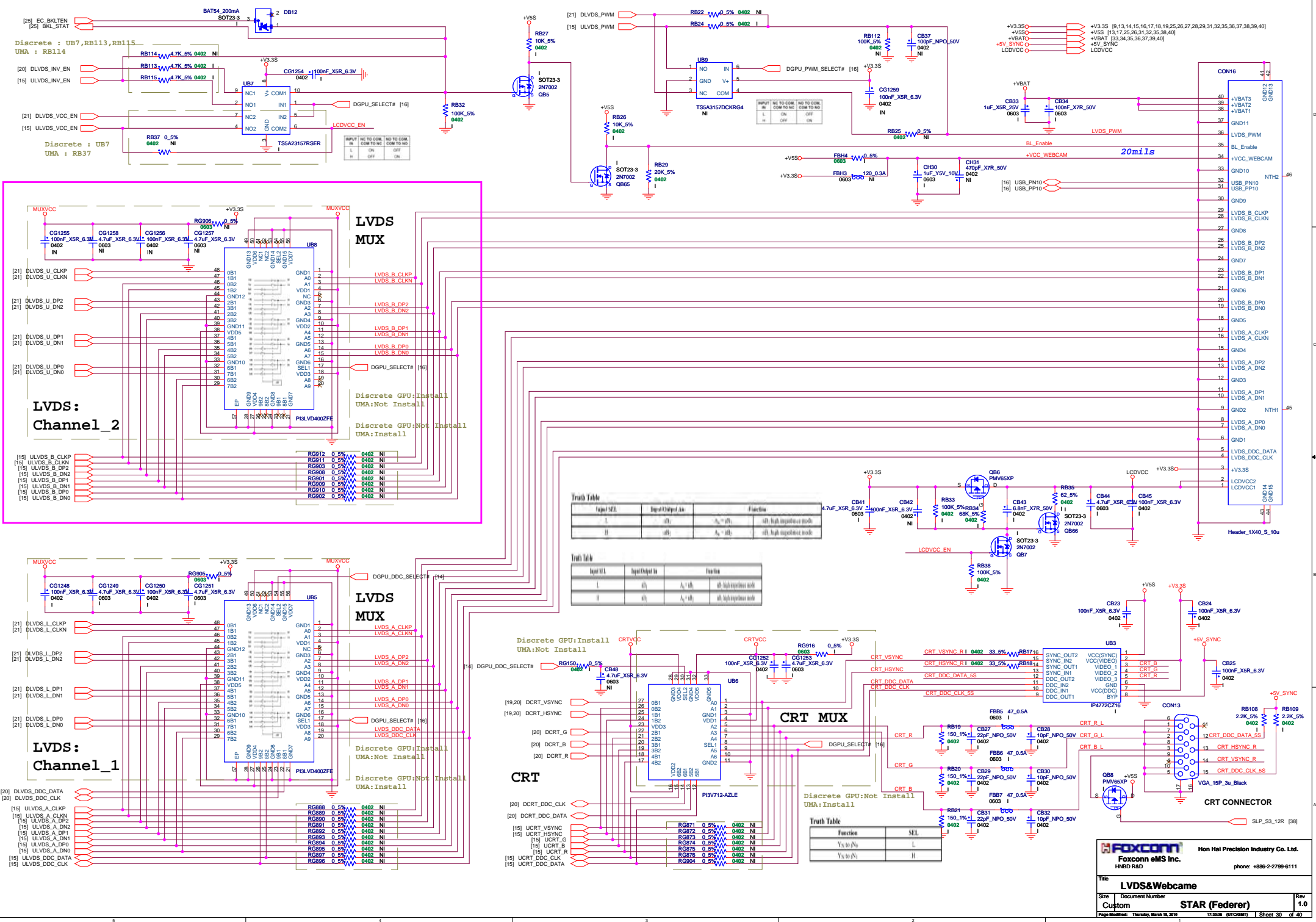
USBX2 CONN.



USBX1 CONN.



For GPU used For CPU used



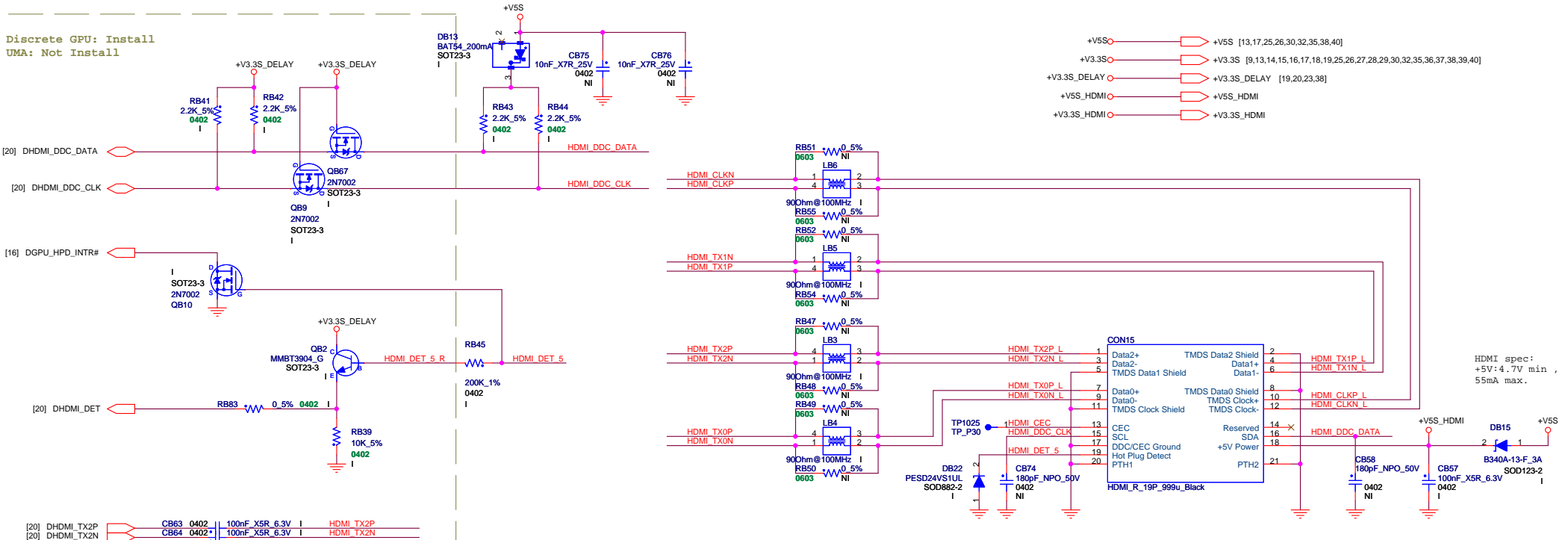
Input SEL	Input Output An	Function
I	oh	A _n = oh, oh, high impedance mode
II	ohh	A _n = ohh, ohh, high impedance mode

Input SEL	Input Output An	Function
I	oh	A _n = oh, oh, high impedance mode
II	ohh	A _n = ohh, ohh, high impedance mode

Function	SEL
Y to B	L
Y to R	II

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Discrete GPU: Install
UMA: Not Install

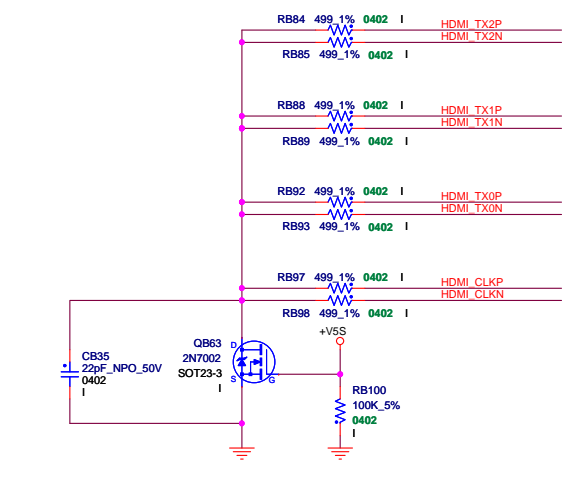
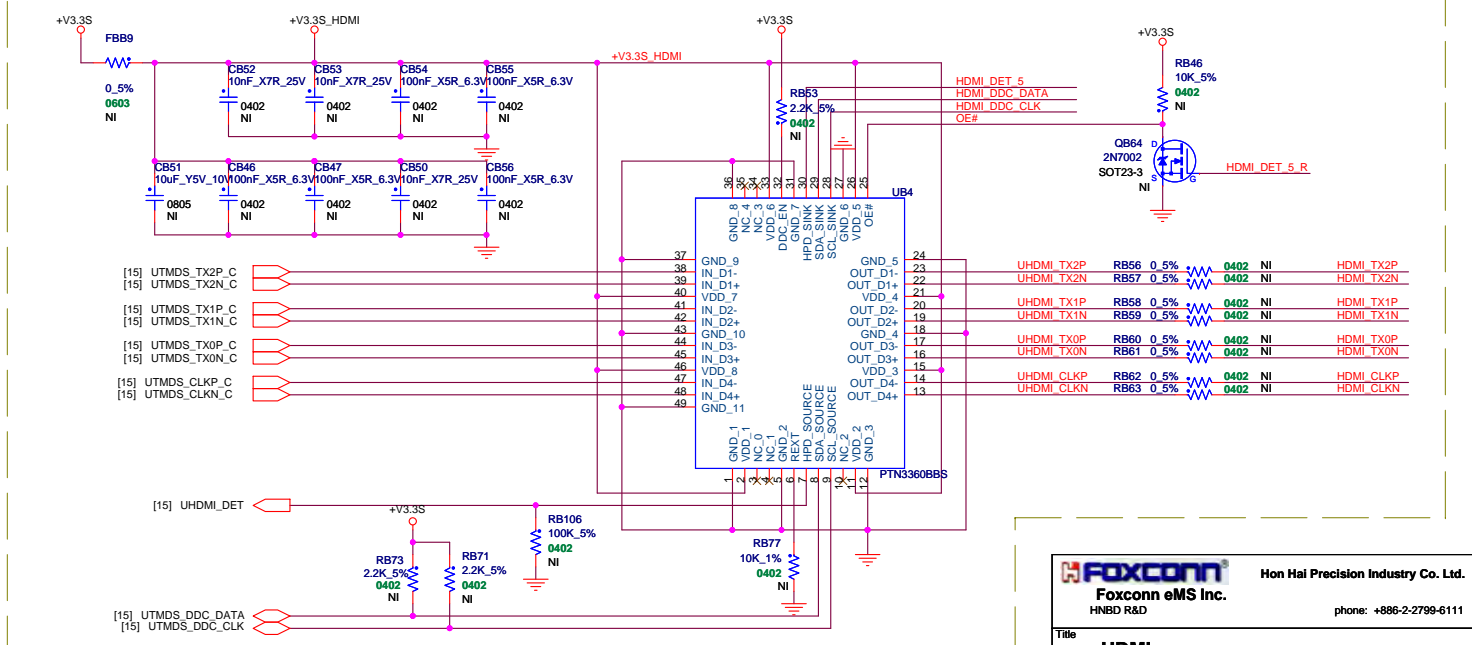


- +V5S [13,17,25,26,30,32,35,38,40]
- +V3.3S [9,13,14,15,16,17,18,19,25,26,27,28,29,30,32,35,36,37,38,39,40]
- +V3.3S_DELAY [19,20,23,38]
- +V5S_HDMI
- +V3.3S_HDMI

HDMI spec:
+5V: 4.7V min,
55mA max.

- [20] DHDMI_TX2P CB63 0402 100nF X5R 6.3V | HDMI TX2P
- [20] DHDMI_TX2N CB64 0402 100nF X5R 6.3V | HDMI TX2N
- [20] DHDMI_TX1P CB65 0402 100nF X5R 6.3V | HDMI TX1P
- [20] DHDMI_TX1N CB66 0402 100nF X5R 6.3V | HDMI TX1N
- [20] DHDMI_TX0P CB67 0402 100nF X5R 6.3V | HDMI TX0P
- [20] DHDMI_TX0N CB68 0402 100nF X5R 6.3V | HDMI TX0N
- [20] DHDMI_CLKP CB69 0402 100nF X5R 6.3V | HDMI CLKP
- [20] DHDMI_CLKN CB70 0402 100nF X5R 6.3V | HDMI CLKN

Discrete GPU: Not Install
UMA: Install



- [15] UTMDS_TX2P_C
- [15] UTMDS_TX2N_C
- [15] UTMDS_TX1P_C
- [15] UTMDS_TX1N_C
- [15] UTMDS_TX0P_C
- [15] UTMDS_TX0N_C
- [15] UTMDS_CLKP_C
- [15] UTMDS_CLKN_C
- [15] UHDMI_DET
- [15] UTMDS_DDC_DATA
- [15] UTMDS_DDC_CLK

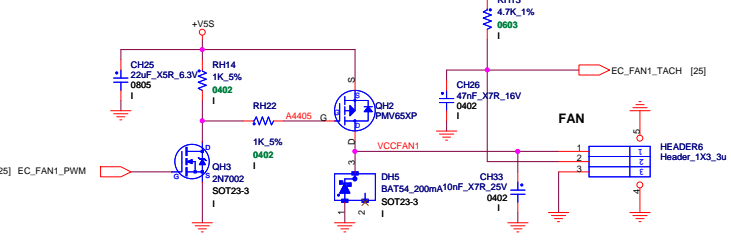
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Title: **HDMI**

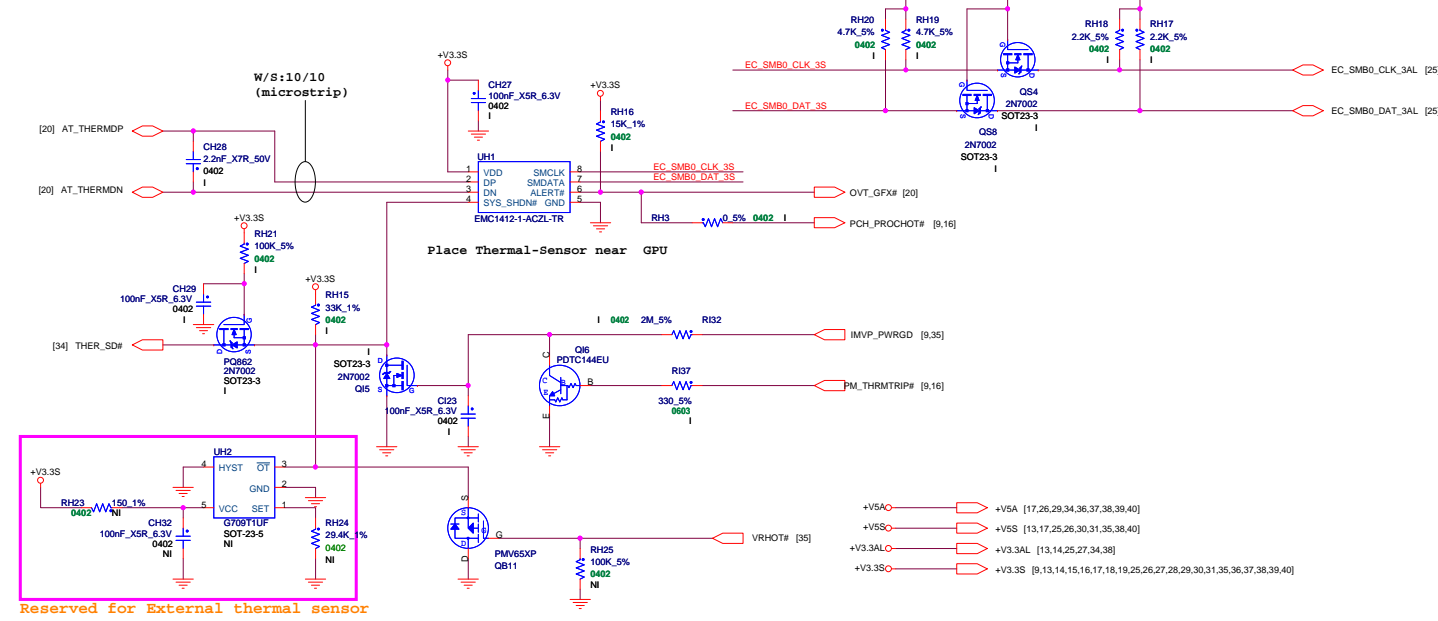
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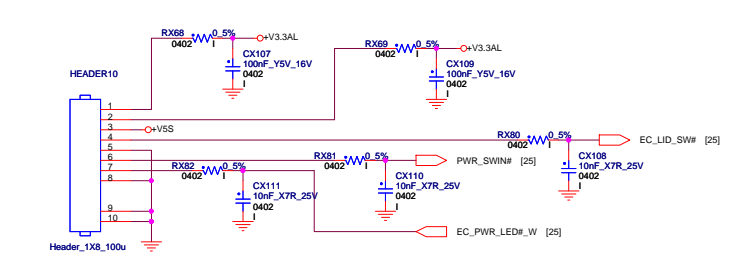
FAN CONNECTOR



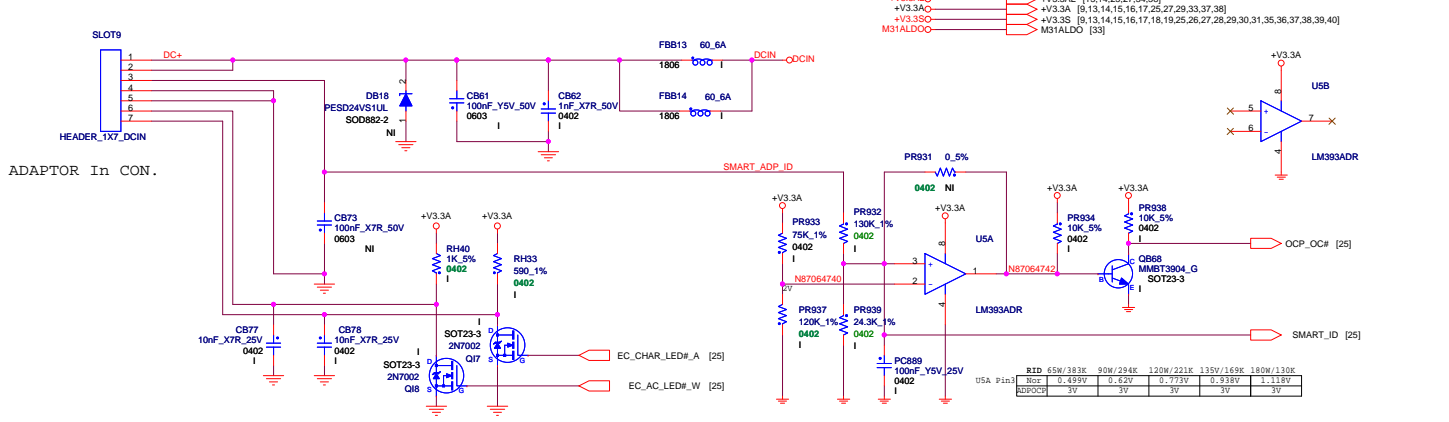
THERMAL SENSOR



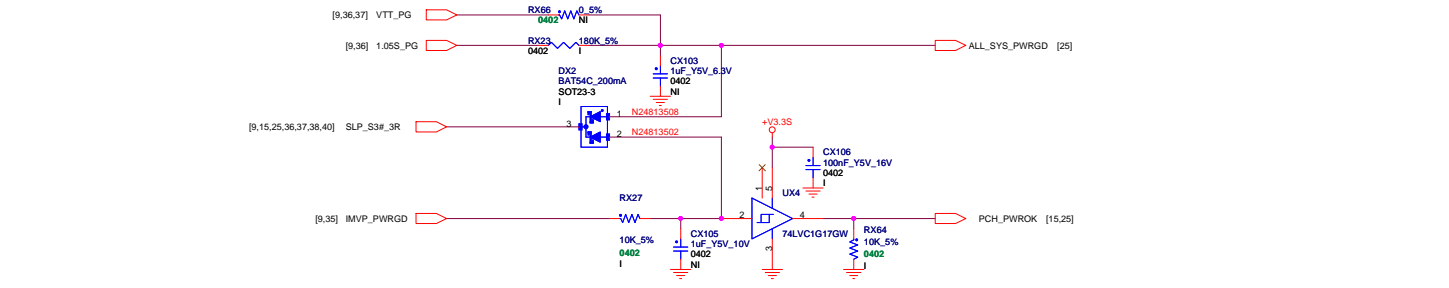
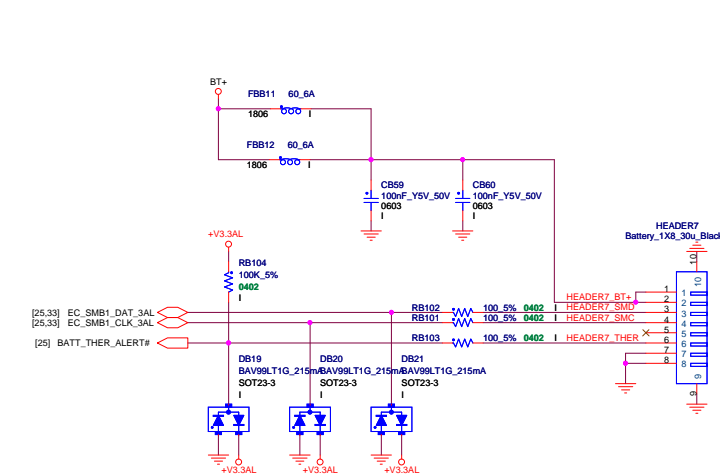
POWER BUTTON BOARD CONNECTOR



DC JACK Wire to Board Connector



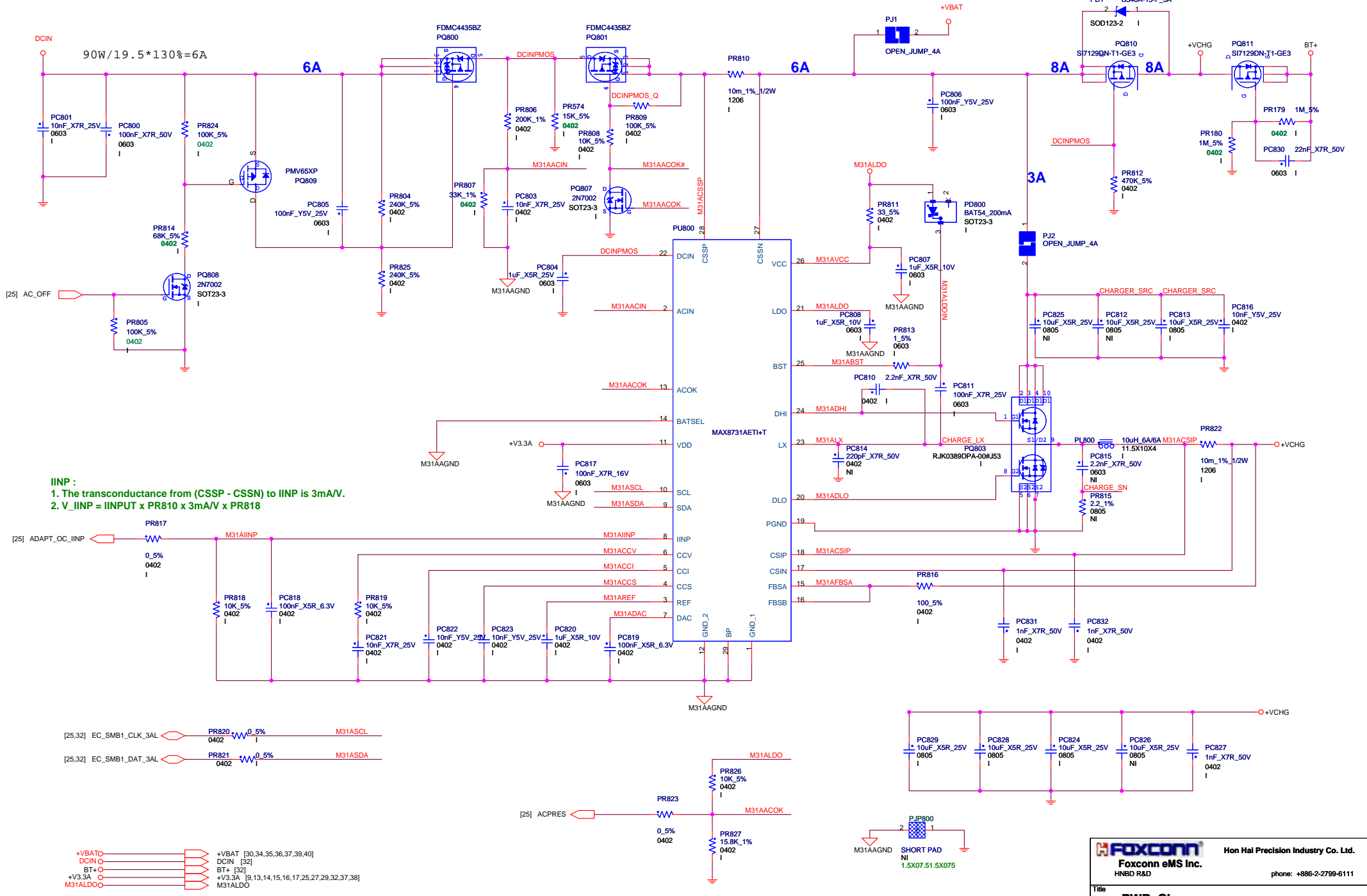
BATTERY CONNECTOR



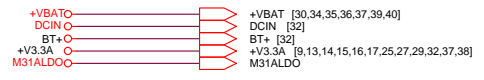
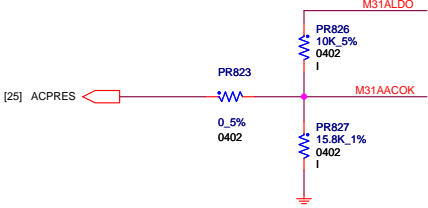
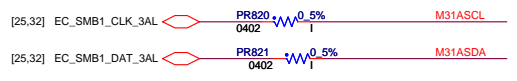
Pin No.	Symbol	Comments
1	BATT+	Batt+, Battery Positive Terminal
2	BATT+	Batt+, Battery Positive Terminal
3	SMD	SMBus data interface I/O pin.
4	SMC	SMBus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal

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DCIN/Battery/OC/P/FAN
 Size: Custom Document Number: STAR (Federer) Rev: 1.0
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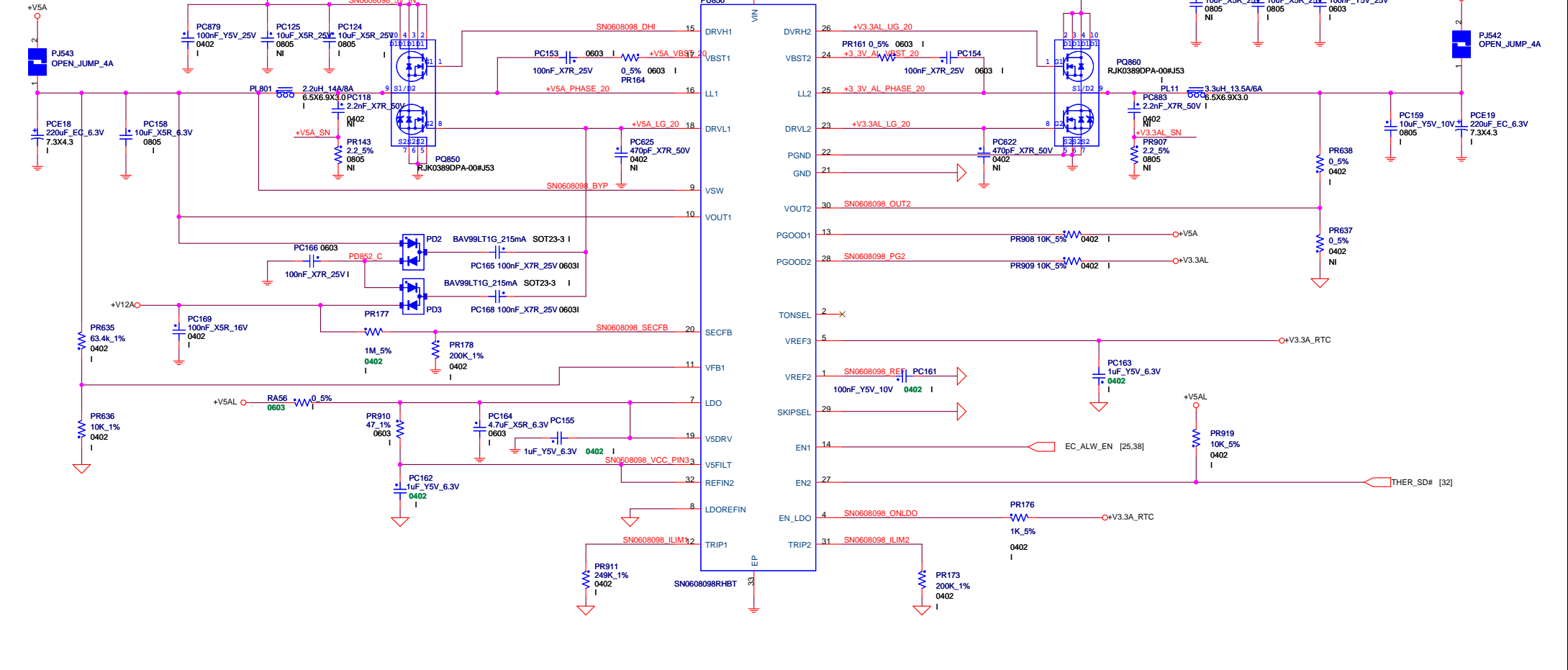
IINP :
 1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
 2. $V_IINP = IINPUT \times PR810 \times 3mA/V \times PR818$



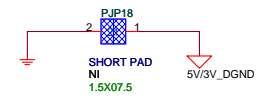
FOXCONN		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBD R&D	
		phone: +86-2-2799-6111	
Title PWR_Charger			
Size	Document Number	Rev	
Custom	STAR (Federer)	1.0	
Page Modified: Thursday, March 18, 2010		17:31:26 (UTC+0800)	
		Sheet 33 of 40	

+V5A/7A/5.6A

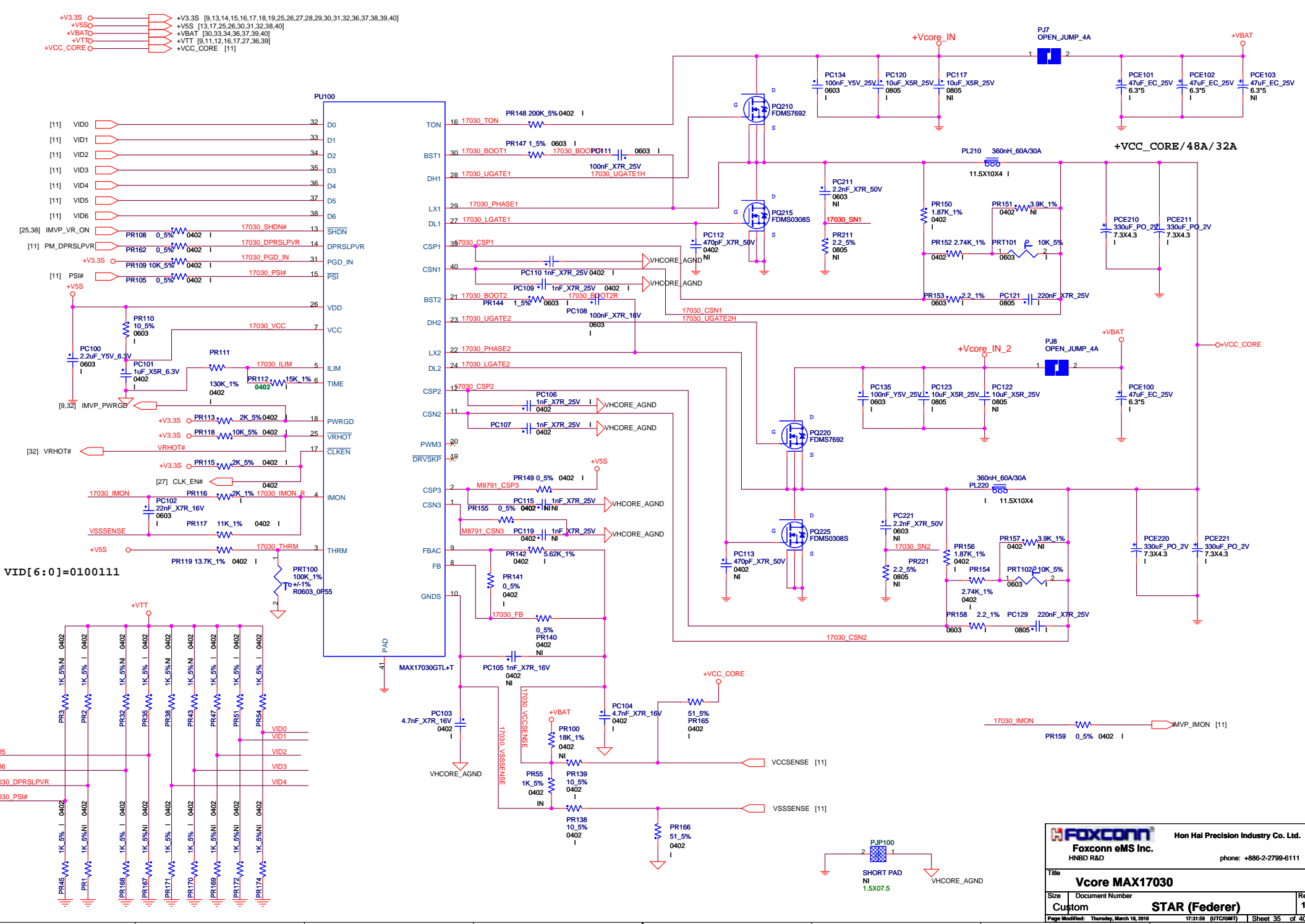
+V3.3A/6/4.8A



- +V3.3ALC [13,14,25,27,32,38]
- +V3.3A [9,13,14,15,16,17,25,27,29,32,33,37,38]
- +V3.3S [9,13,14,15,16,17,18,19,25,26,27,28,29,30,31,32,35,36,37,38,39,40]
- +VBAT [30,33,35,36,37,39,40]
- +V12A [38]
- +V5A [17,26,29,36,37,38,39,40]
- +V5AL [38]



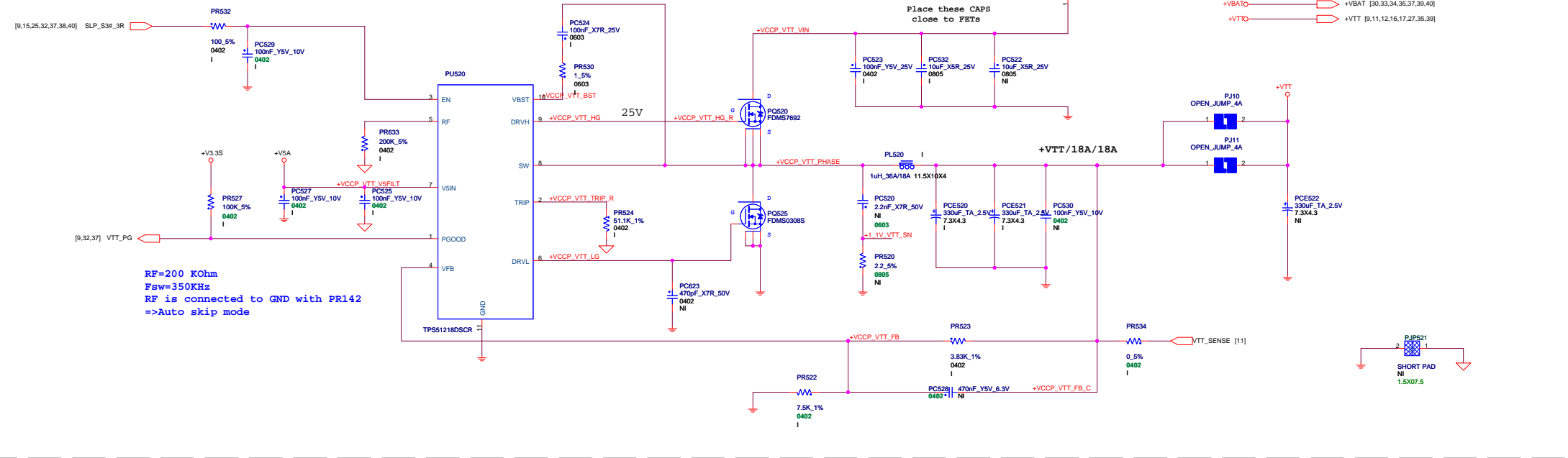
FOXCONN		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBD R&D	
		phone: +886-2-2799-6111	
Title			
5V/3.3V SN0608098RHBT			
Size	Document Number		Rev
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Page Modified: Thursday, March 18, 2010		17:31:43 (UTC/GMT)	
		Sheet 34 of 40	



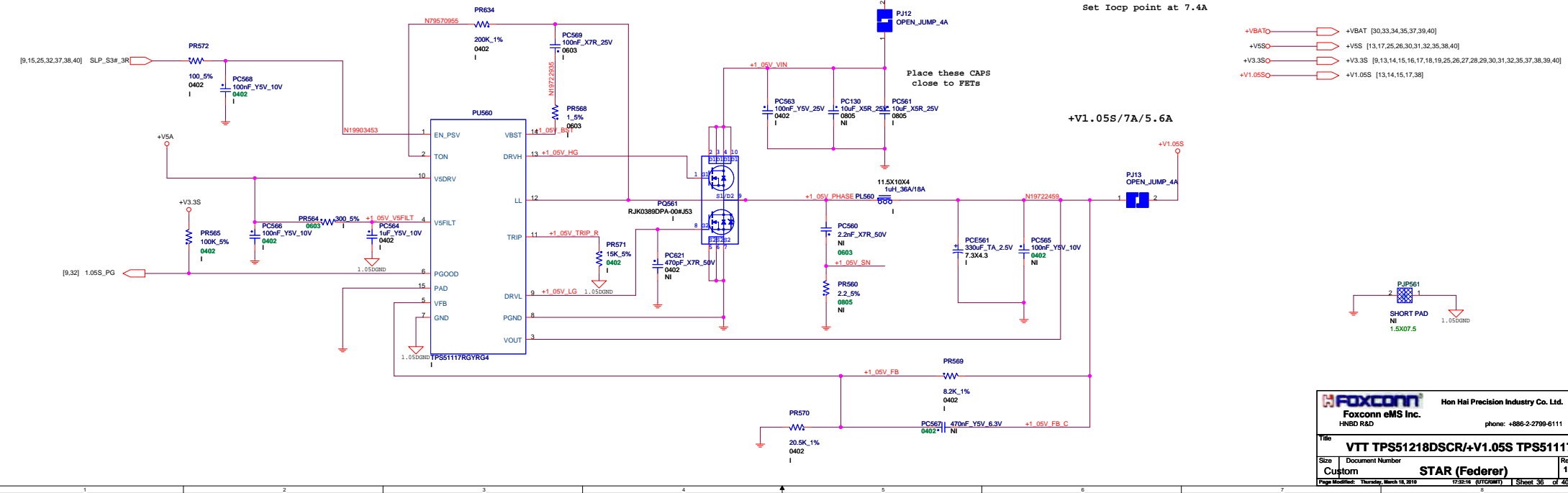
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		Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNBD R&D	
		phone: +886-2-2799-6111	
Title Vcore MAX17030			
Size Document Number Custom	STAR (Federer)		Rev 1.0
Page Modified: Thursday, March 18, 2010		17:31:59 (UTC/GMT) Sheet 35 of 40	

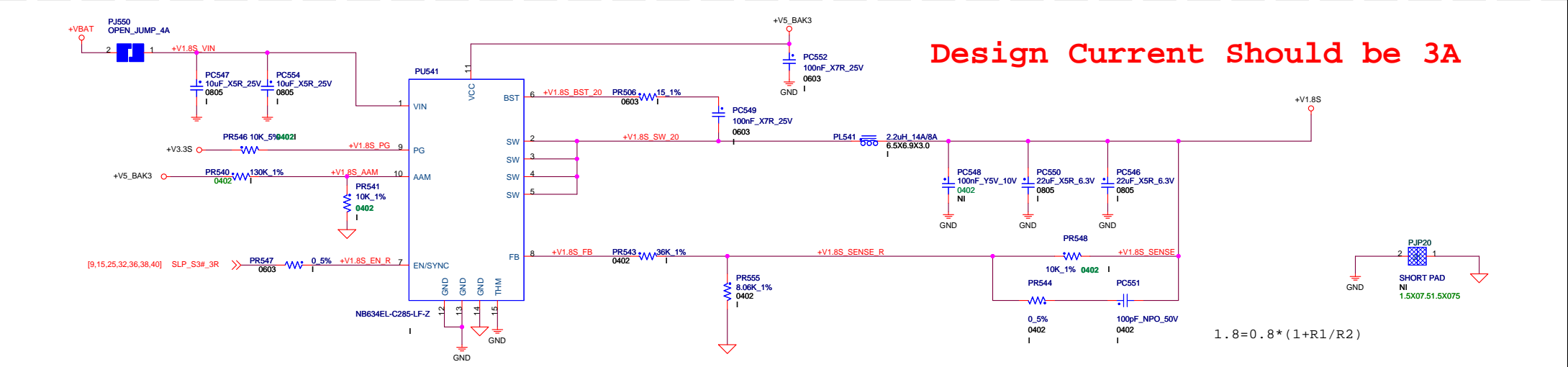
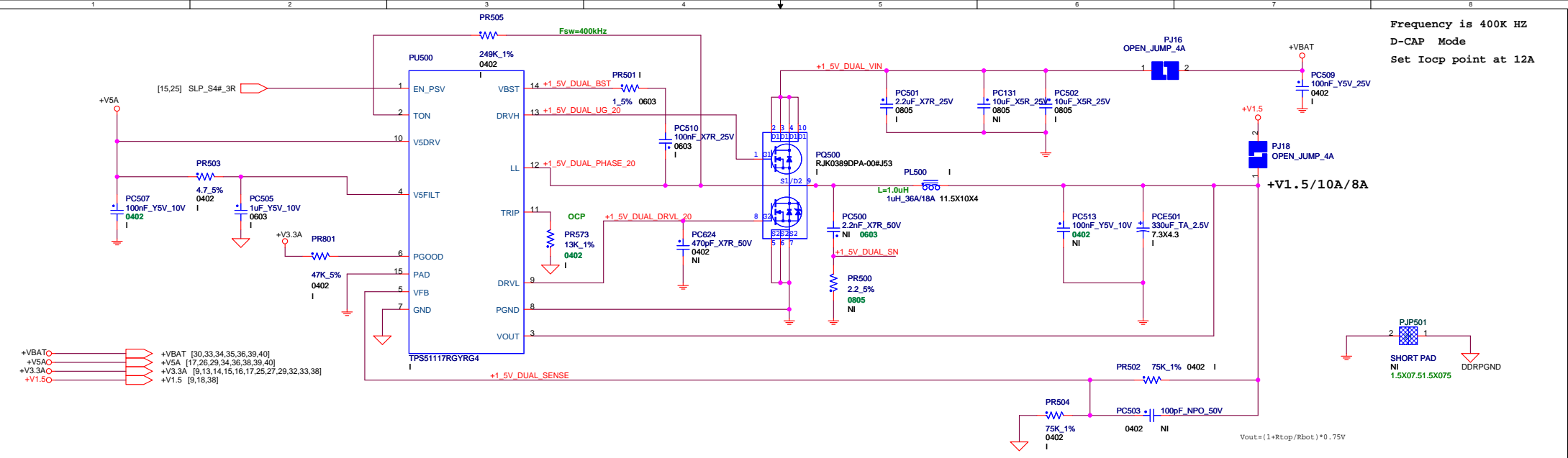
+VTT TPS51218



+V1.05S TPS51117

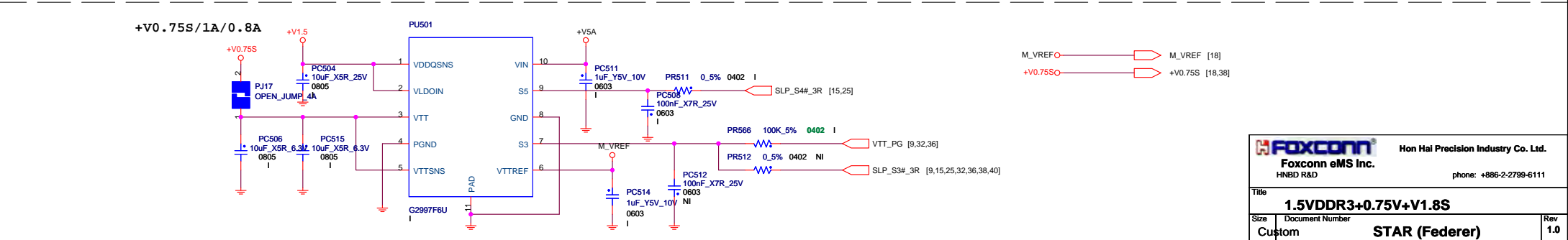


Frequency is 400K HZ
D-CAP Mode
Set Iocp point at 12A



Design Current Should be 3A

$$1.8 = 0.8 * (1 + R1/R2)$$

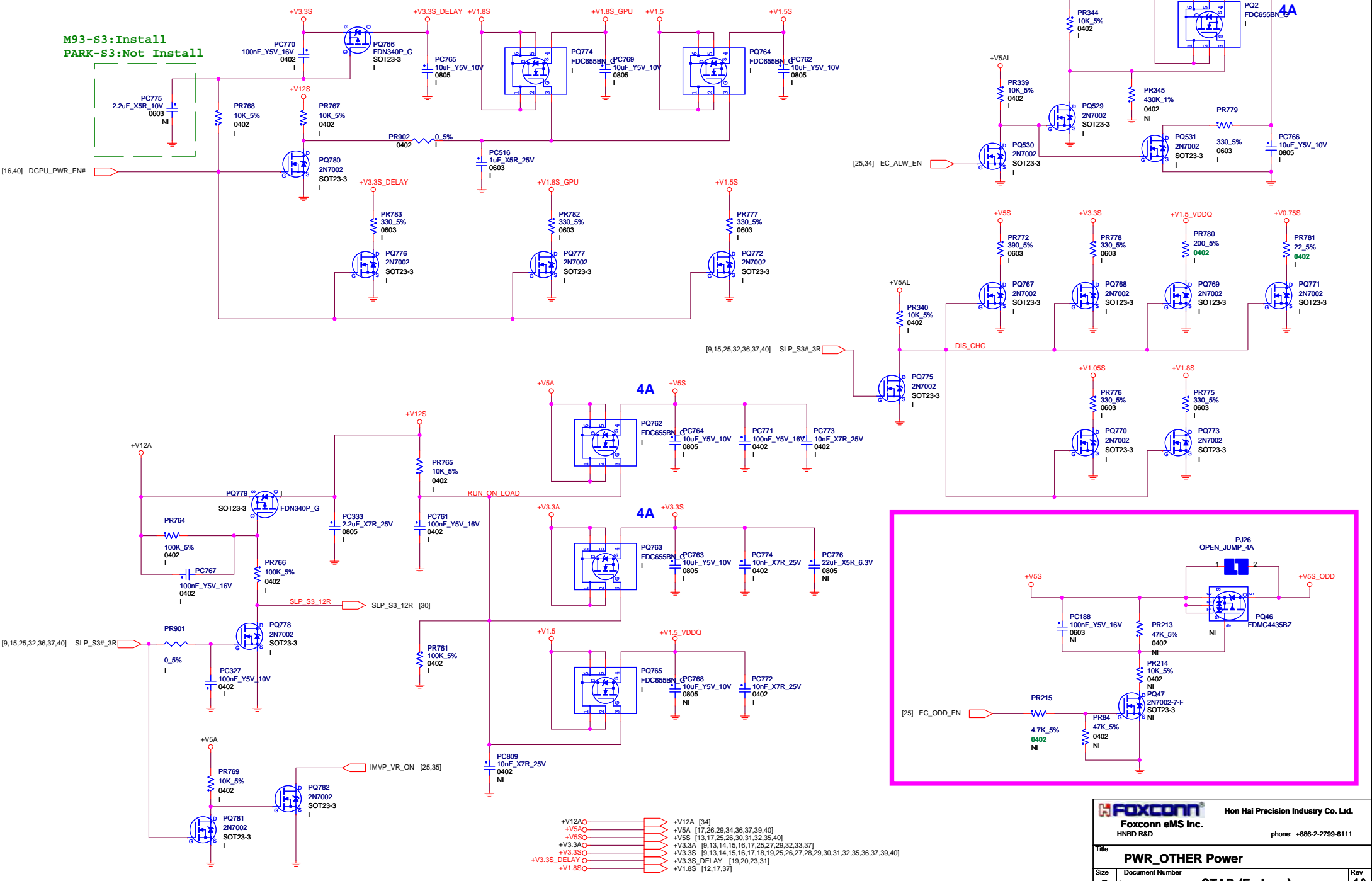


M93-S3:Install
PARK-S3:Not Install

+V3.3S_GPU

+V1.8S_GPU

+V1.5S_GPU



- +V12A [34]
- +V5A [17,26,29,34,36,37,39,40]
- +V5S [13,17,25,26,30,31,32,35,40]
- +V3.3A [9,13,14,15,16,17,25,27,29,32,33,37]
- +V3.3S [9,13,14,15,16,17,18,19,25,26,27,28,29,30,31,32,35,36,37,39,40]
- +V3.3S_DELAY [19,20,23,31]
- +V1.8S [12,17,37]

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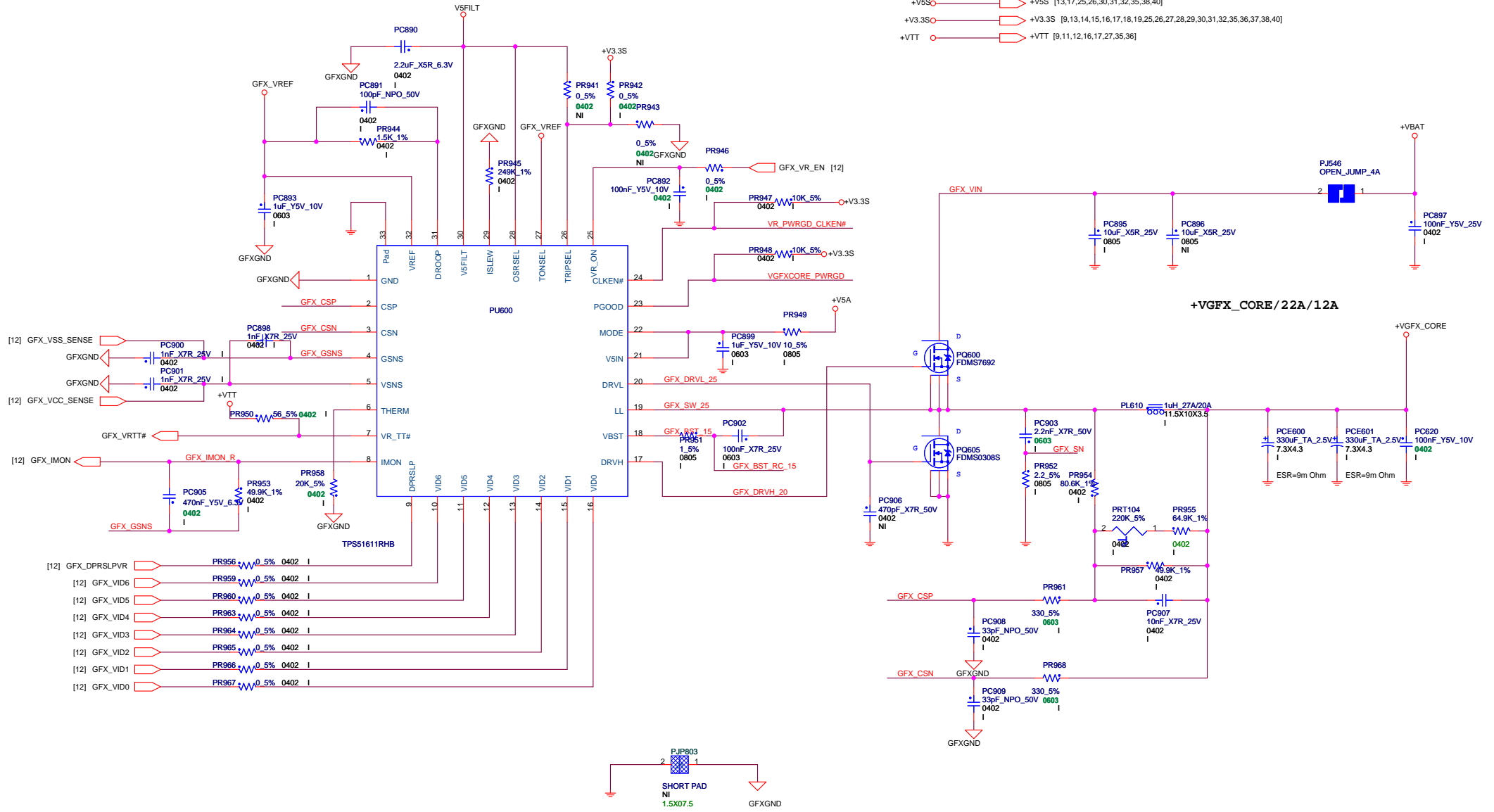
Title: **PWR_OTHER Power**

Size: Document Number
 Custom **STAR (Federer)** Rev: 1.0

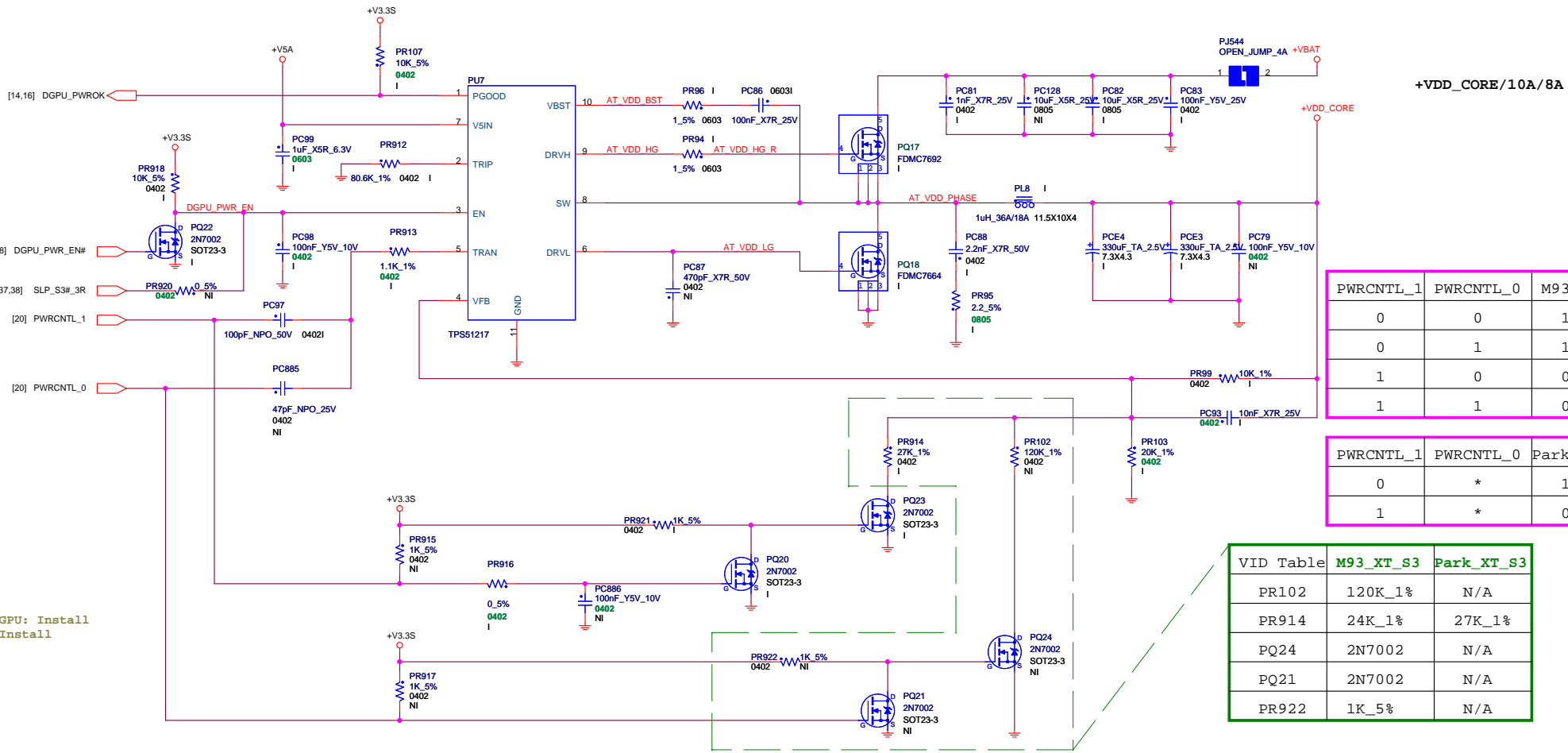
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+VGFXCORE

- +VBAT +VBAT [30,33,34,35,36,37,40]
- +VGFX_CORE +VGFX_CORE [12]
- +V5S +V5S [13,17,25,26,30,31,32,35,38,40]
- +V3.3S +V3.3S [9,13,14,15,16,17,18,19,25,26,27,28,29,30,31,32,35,36,37,38,40]
- +VTT +VTT [9,11,12,16,17,27,35,36]

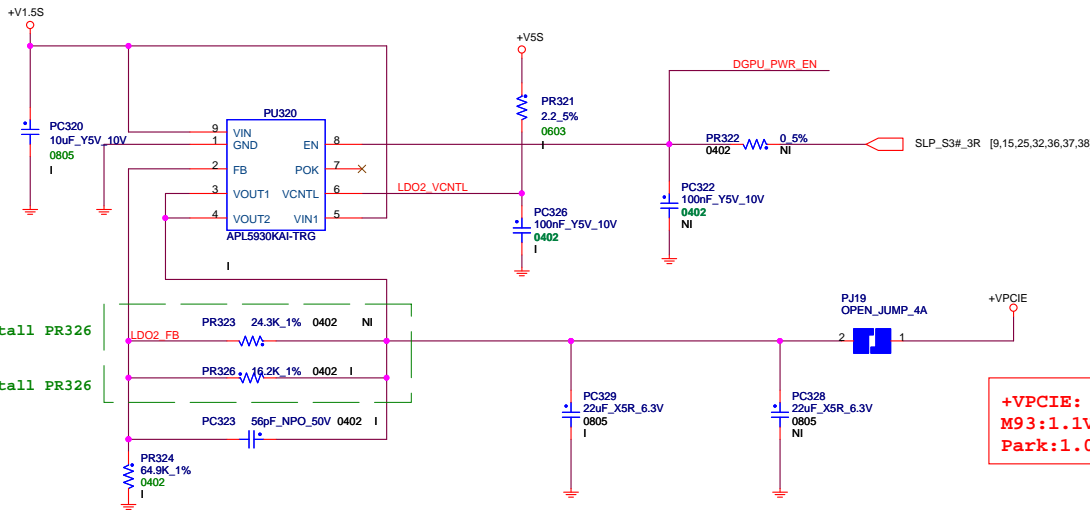


+VGFX_CORE/22A/12A



Discrete GPU: Install
UMA: Not Install

Discrete GPU: Install
UMA: Not Install



M93-S3:
Install PR323 and Not Install PR326

Park-S3 :
Not Install PR323 and Install PR326

+VPCIE:
M93: 1.1V@150mA
Park: 1.0V@125mA