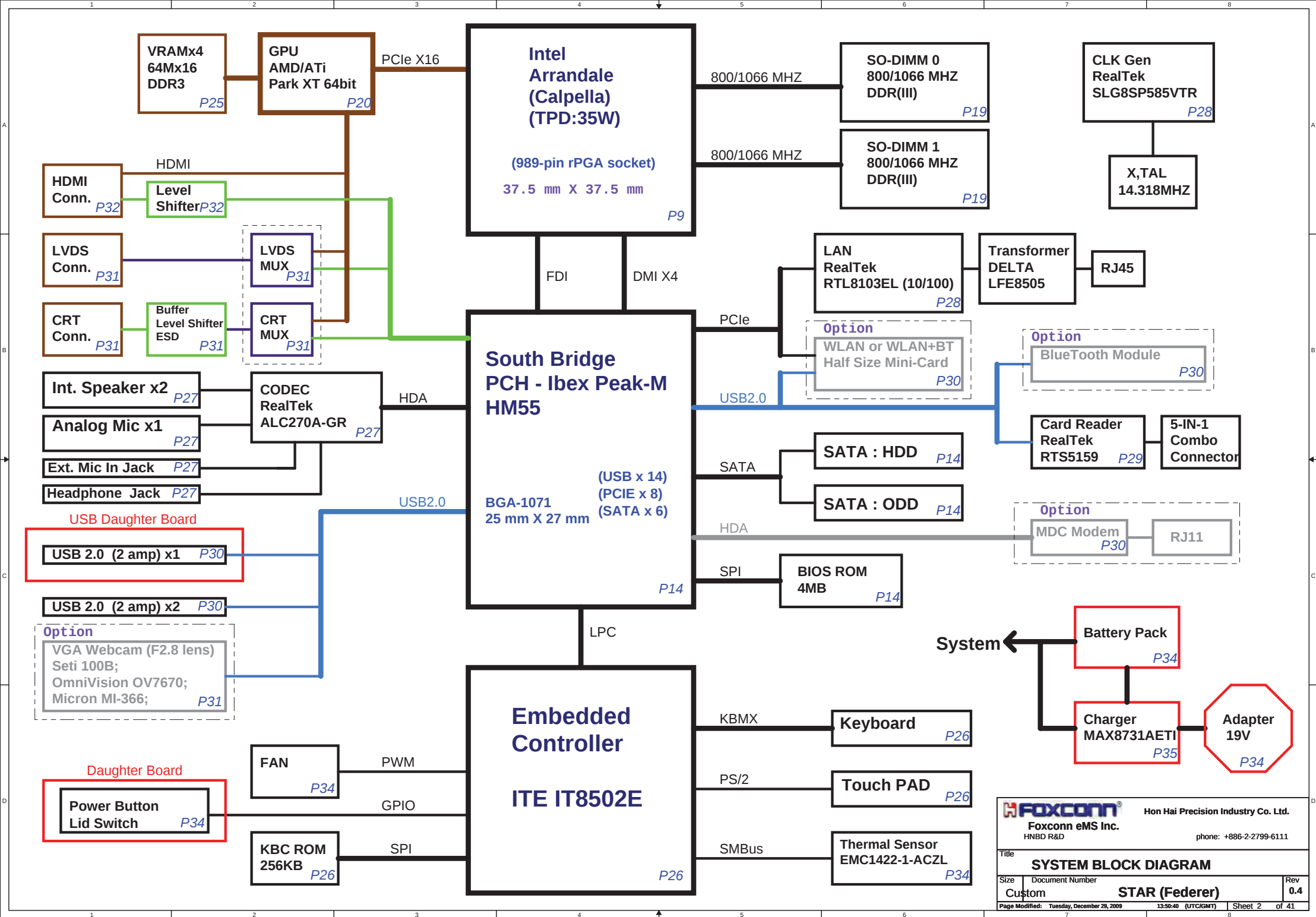
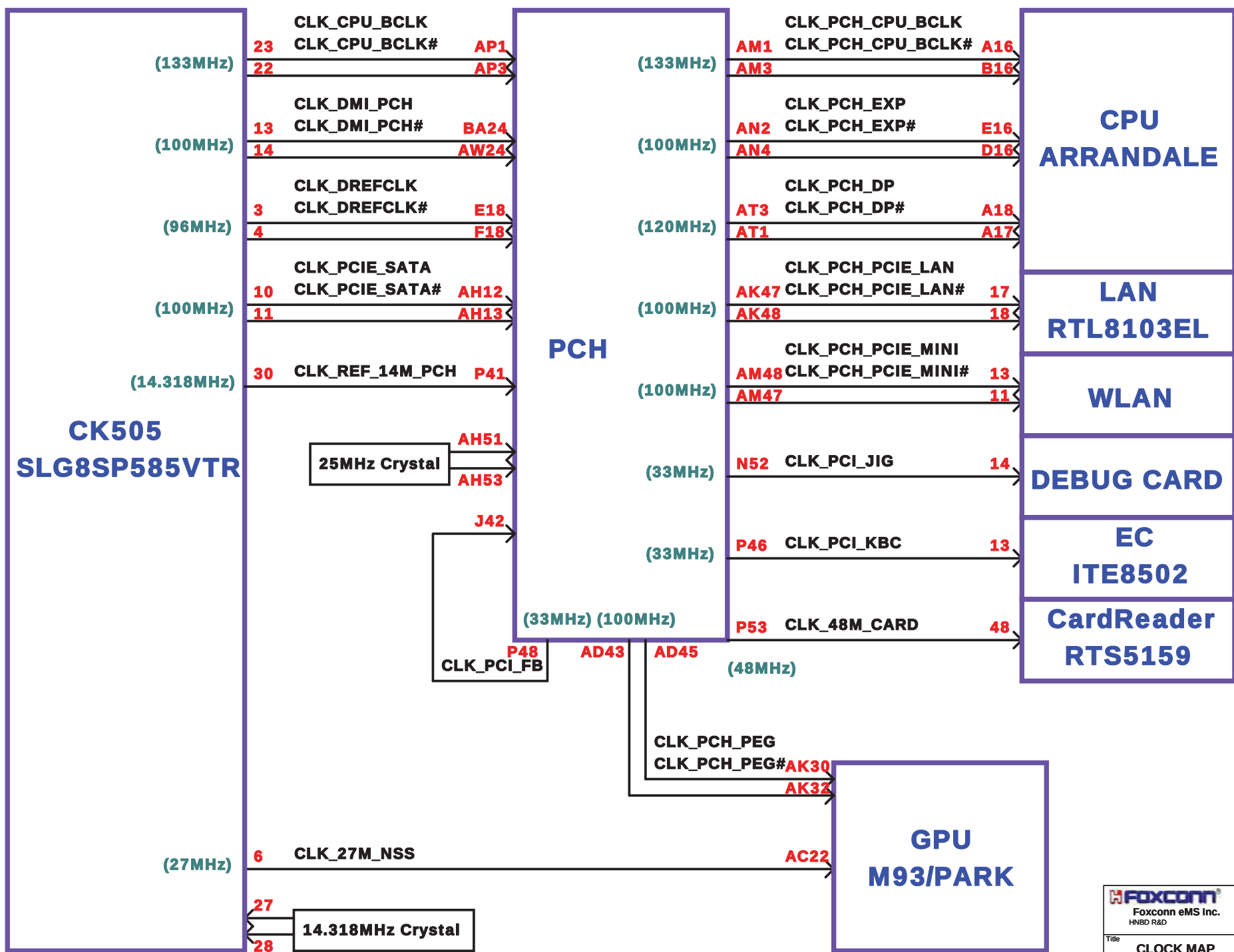


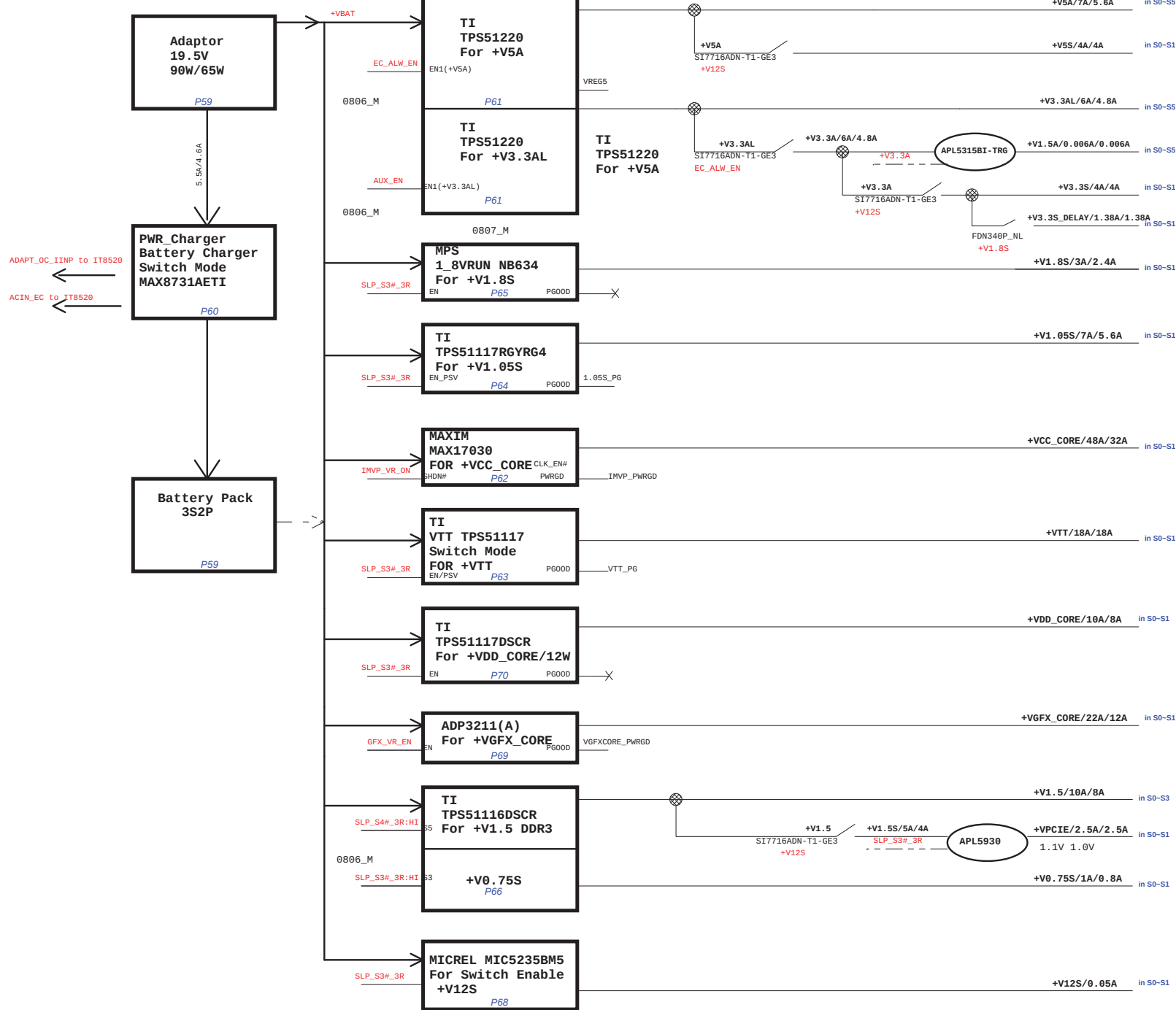
01	--	COVER SHEET	21	--	VGA_S3 (IO) 2/5
02	--	SYSTEM BLOCK DIAGRAM	22	--	VGA_S3 (DDR3) 3/5
03	--	CLOCK MAP	23	--	VGA_S3 (DP) 4/5
04	--	POWER MAP	24	--	VGA_S3 (POWER) 5/5
05	--	POWER SEQUENCY DIAGRAM	25	--	VRAM (DDR3)
06	--	POWER SEQUENCY TIMING	26	--	EC+KBC (IT8502E)
07	--	SMBUS MAP	27	--	CODEC/JACK/SPEAKER/MIC
08	--	RESET SIGNAL MAP	28	--	LAN (RTL8103EL)/CLOCK GEN
09	--	Calpella (DMI,PEG,FDI)	29	--	Card Reader
10	--	Calpella (CLK,MISC,JTAG)	30	--	WLAN/BT/MDC/USB/MOUNTING
11	--	Calpella (DDR3)	31	--	LVDS/CRT/Webcam
12	--	Calpella (POWER/GND)	32	--	HDMI
13	--	Calpella (GRAPHIC POWER)	33	--	DCIN/Battery/OCP/FAN
14	--	PCH (HDA,JTAG,SATA)	34	--	PWR_Charger MAX8731AETI
15	--	PCH (PCI-E,SMBUS,CLK)	35	--	5V/3.3V SN0608098RHB
16	--	PCH (DMI,FDI,GPIO,LVDS)	36	--	Vcore MAX17030
17	--	PCH (PCI,USB,NVRAM,GPIO)	37	--	1.1V VTT/+V1.05RUN
18	--	PCH (POWER)	38	--	1.5VDDR3+0.75V+V1.8RUN
19	--	DDR3(SO-DIMM_0&1)	39	--	PWR_Others power plane
20	--	VGA (PCI-E/STRAP) 1/5	40	--	CPU VREG & Decoupling
			41	--	ATVDD/+VPCIE

P. Leader	Check by	Design by

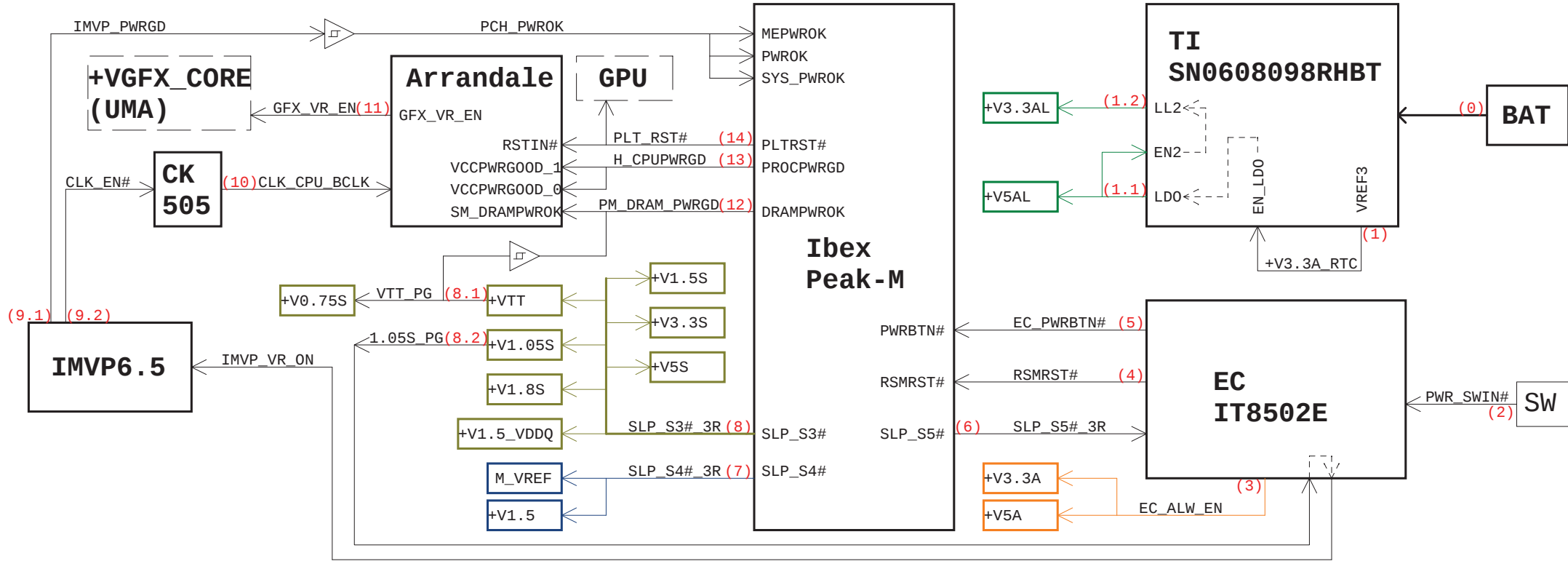
 Foxconn eMS Inc. HNBD R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111
Title		
Index Page		
Size	Document Number	Rev
Custom	STAR (Federer)	0.4
Page Modified: Tuesday, December 29, 2009 13:50:37 (UTC+GMT) Sheet 1 of 41		







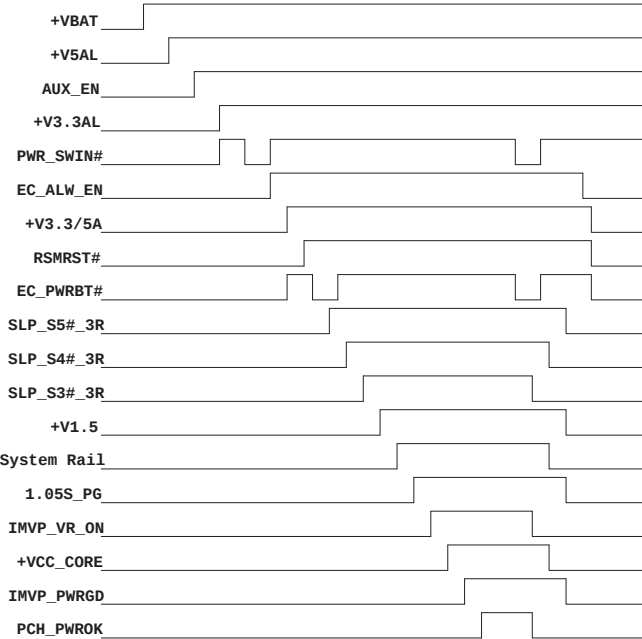
POWER SEQUENCY DIAGRAM



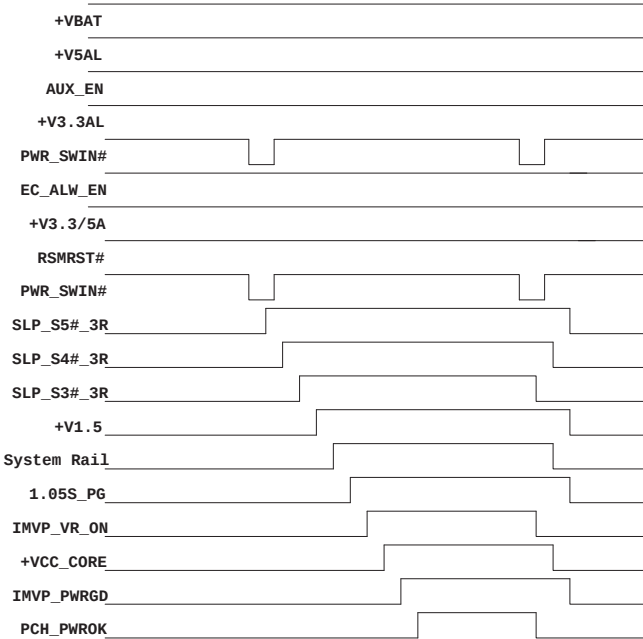
	Source Rail	EN	PG	Power Status				Remark
				S0	S3	AC S4/S5	DC S4/S5	
+VBAT				V	V	V	V	
+V5AL	+VBAT	+V3.3A_RTC		V	V	V	V	
+V3.3AL	+VBAT	+V5AL		V	V	V	V	
+V5A	+VBAT	EC_ALW_EN		V	V	V		
+V3.3A	+V3.3AL	EC_ALW_EN		V	V	V		
+V1.5	+VBAT	SLP_S4#_3R		V	V			
+V0.75S	+V1.5	VTT_PG		V				
+V1.5S	+V1.5	RUN_ON_LOAD		V				
+V1.5_VDDQ	+V1.5	RUN_ON_LOAD		V				
+VCC_CORE	+VBAT	IMVP_VR_ON	IMVP_PWRGD	V				
+VTT	+VBAT	SLP_S3#_3R	VTT_PG	V				
+VGFX_CORE	+VBAT	GFX_VR_EN		V				
+V1.8S	+VBAT	SLP_S3#_3R		V				
+V1.05S	+VBAT	SLP_S3#_3R	1.05S_PG	V				
+V5S	+V5A	RUN_ON_LOAD		V				
+V3.3S	+V3.3A	RUN_ON_LOAD		V				
+VDD_CORE	+VBAT	SLP_S3#_3R		V				
+V3.3S_Delay	+V3.3S	+V1.8S		V				
+VPCIE	+V1.5S	SLP_S3#_3R		V				

POWER SEQUENCE TIMING

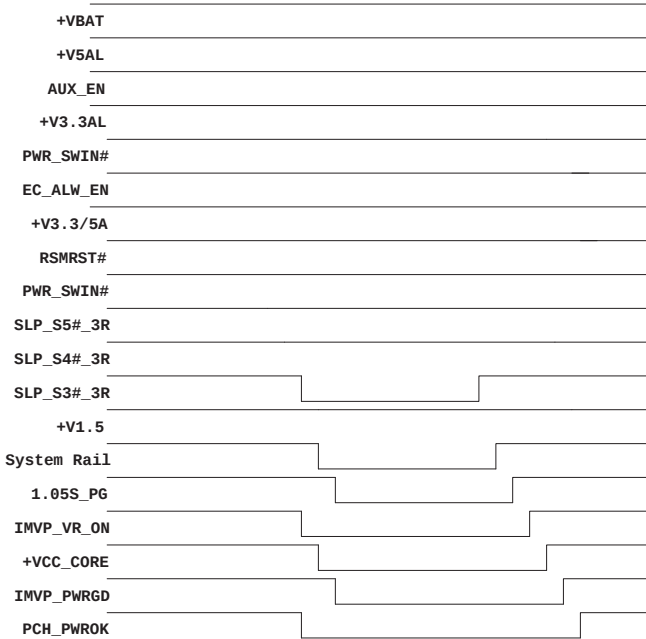
G3(OFF)->S0->S5



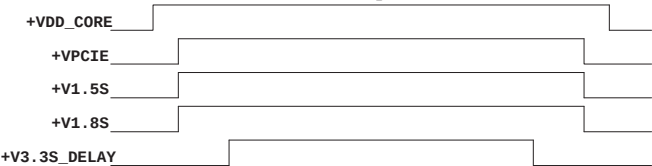
S5->S0->S5



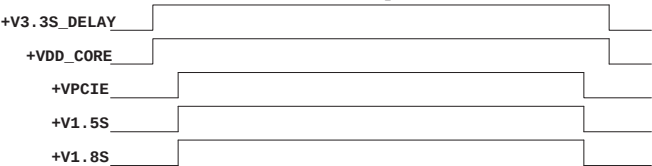
S0->S3->S0



M93 Sequence



Park Sequence



SMBUS&I2C MAP

Discrete
GPU

GPU
M93/Park
S3 Package

PCH

EC
ITE8502

DIMM0

DIMM1

CLOCK
GEN

WLAN

Temp
Sensor

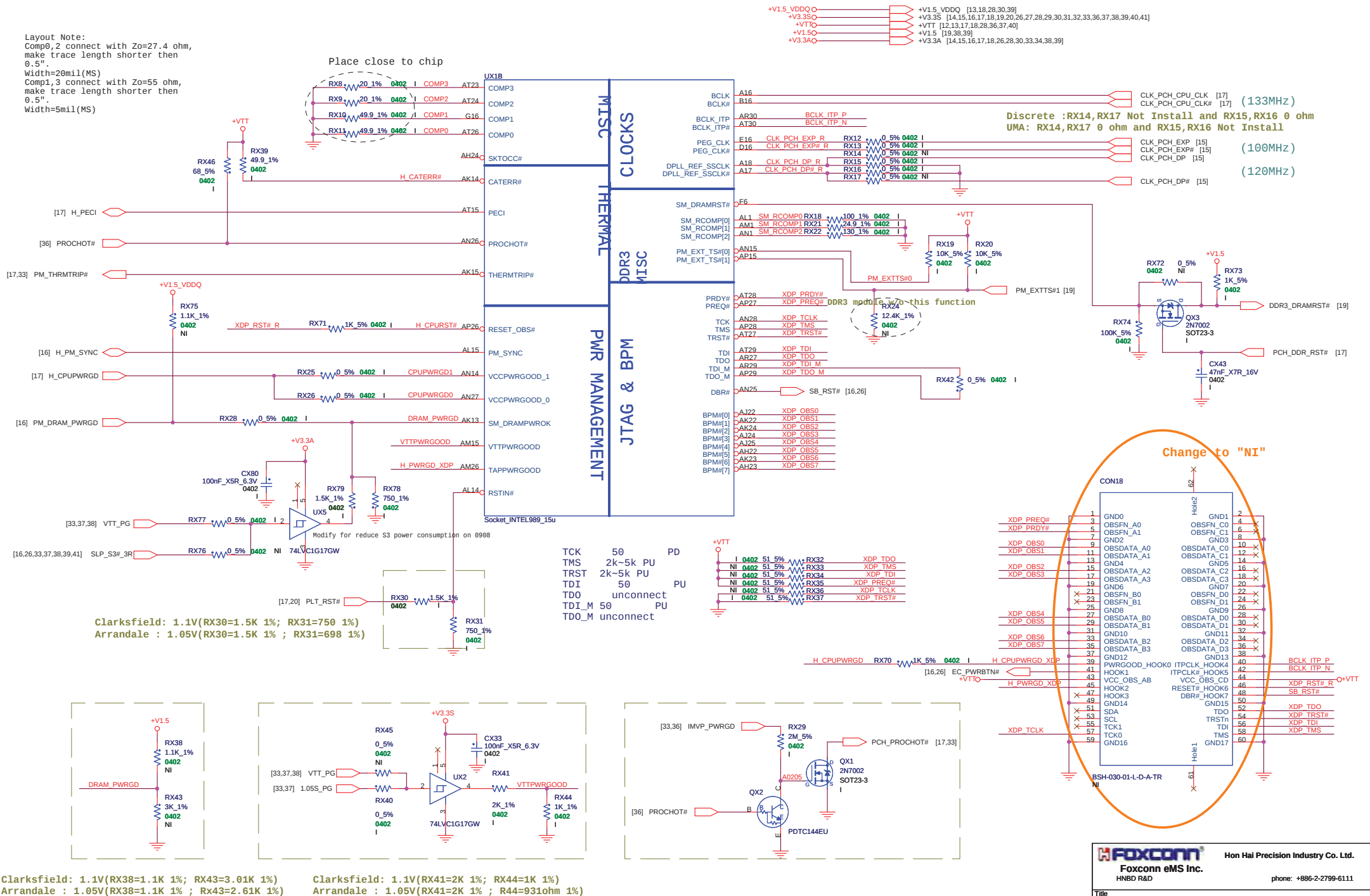
Charger

Battery

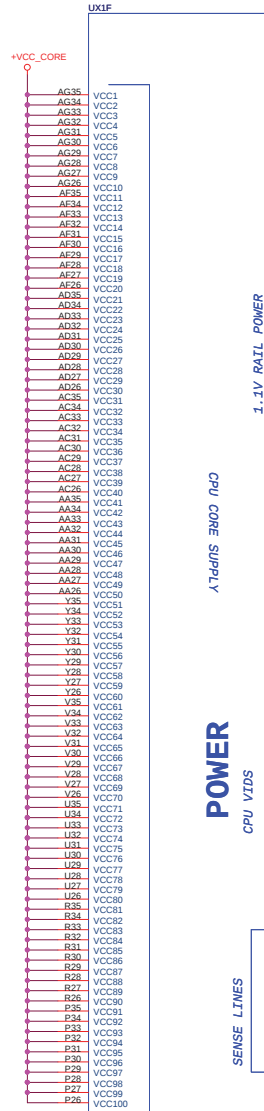
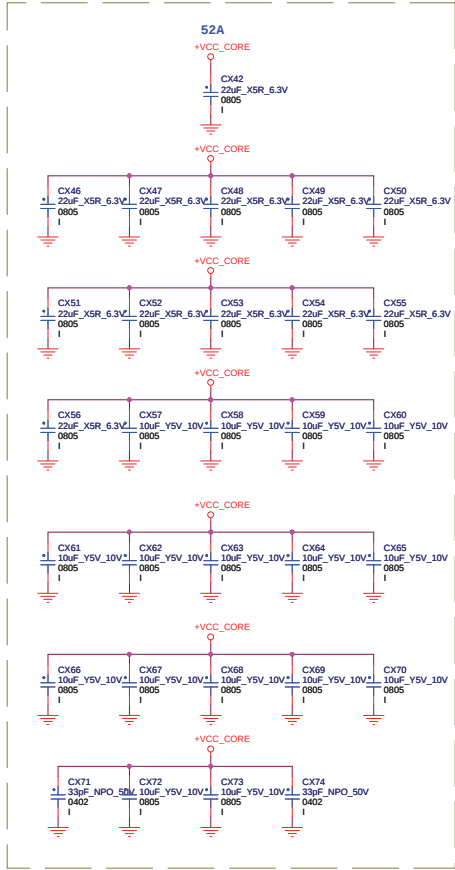
RESET SIGNAL MAP

Layout Note:
Comp0,2 connect with Zo=27.4 ohm,
make trace length shorter then
0.5".
Width=20mil(MS)
Comp1,3 connect with Zo=55 ohm,
make trace length shorter then
0.5".
Width=5mil(MS)

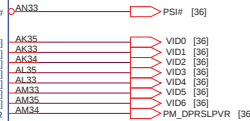
Place close to chip



FOR VCC:
12x 0805 22 μ F inside cavity,
7x 0805 10 μ F under cavity and 9 x 0805 10 μ F
between inductor and socket on top layer

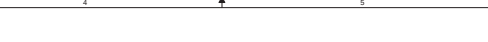
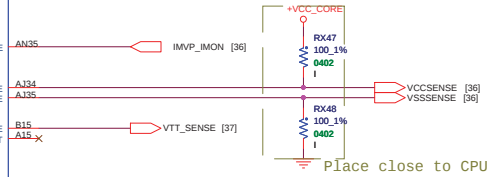


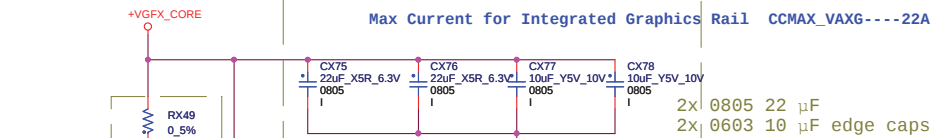
Socket_INTEL989_15u



Arrandale drives this pin High
Clarkfield drives this pin Low.

Place close to CPU





Discrete GPU: Not Install
UMA: Install

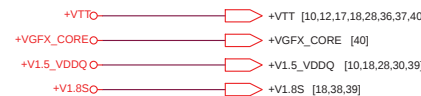
GRAPHICS

POWER

FDI

PEG & DMI

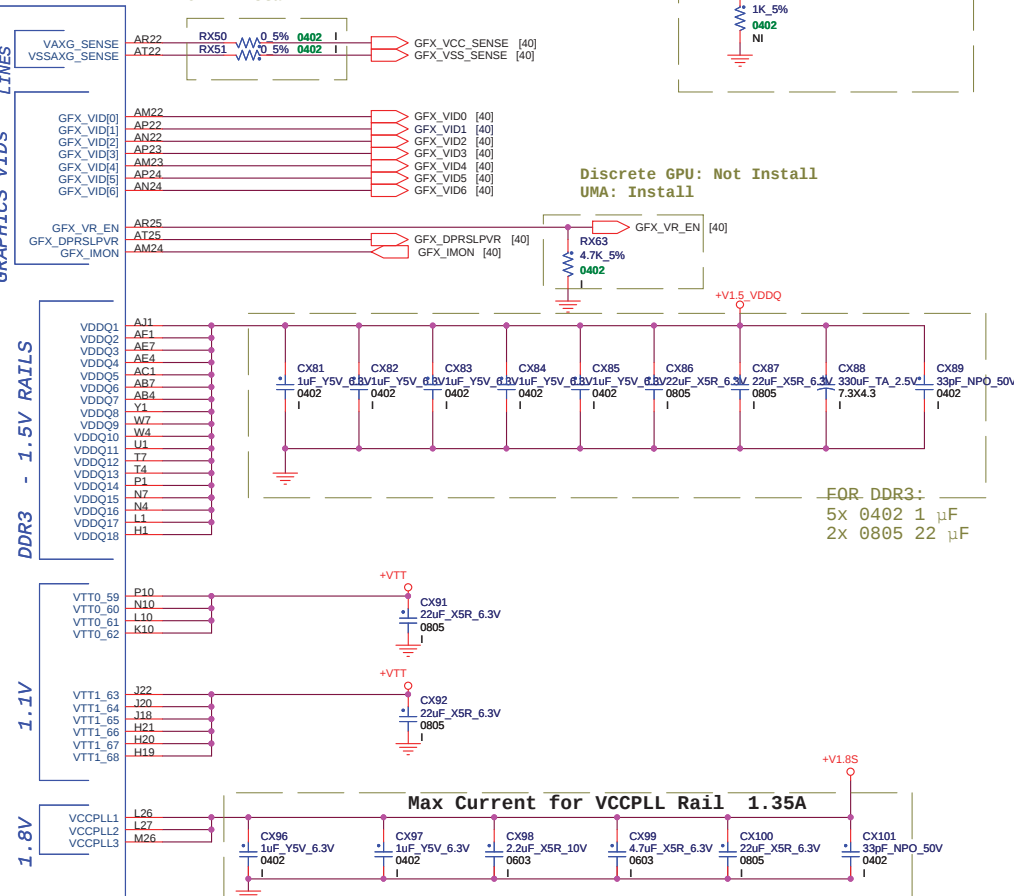
Socket_INTEL989_15u



Discrete GPU: Not Install
UMA: Install

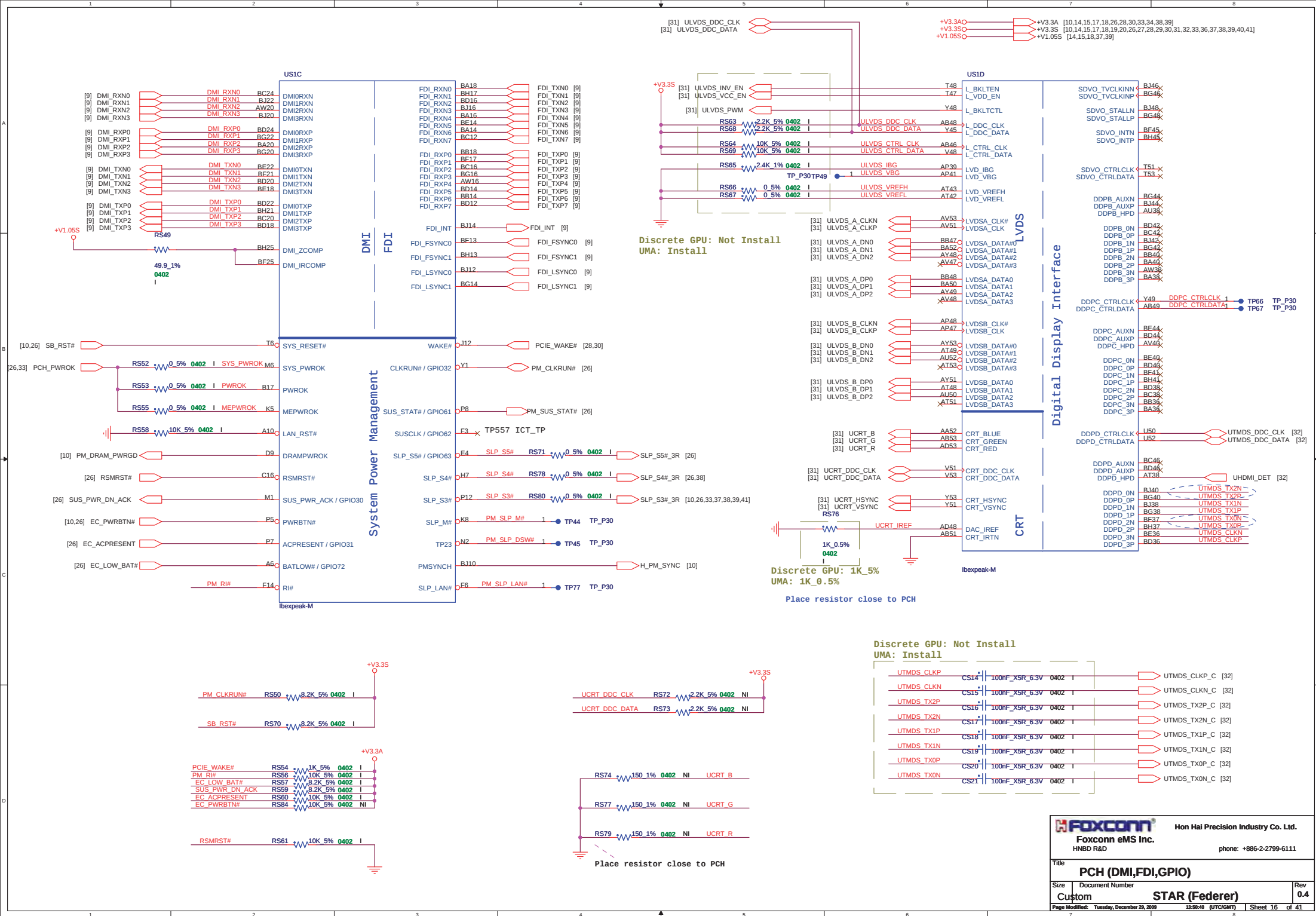
Discrete GPU: Install
UMA: Not Install

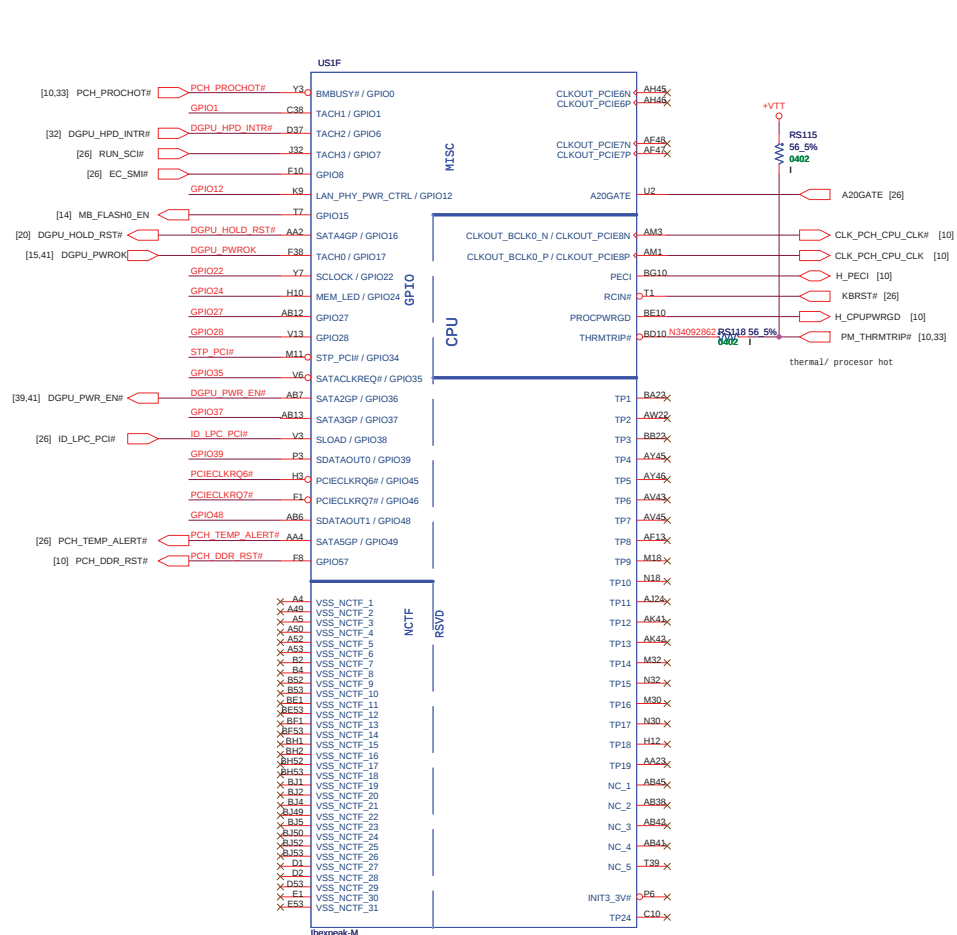
Discrete GPU: Not Install
UMA: Install



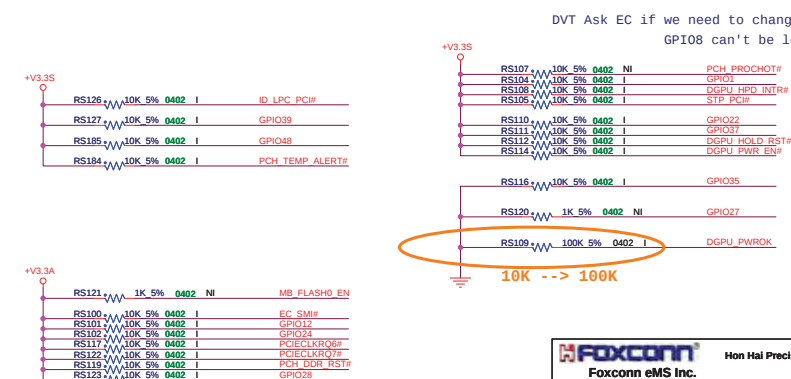
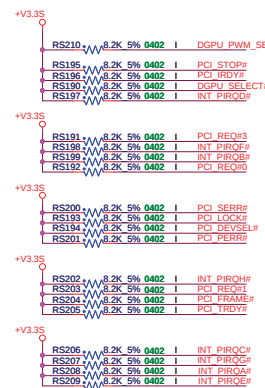
Port	Function
Port1	LAN
Port2	Un-used
Port3	WLAN
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used
Port8	Un-used

PCI-E Port Table

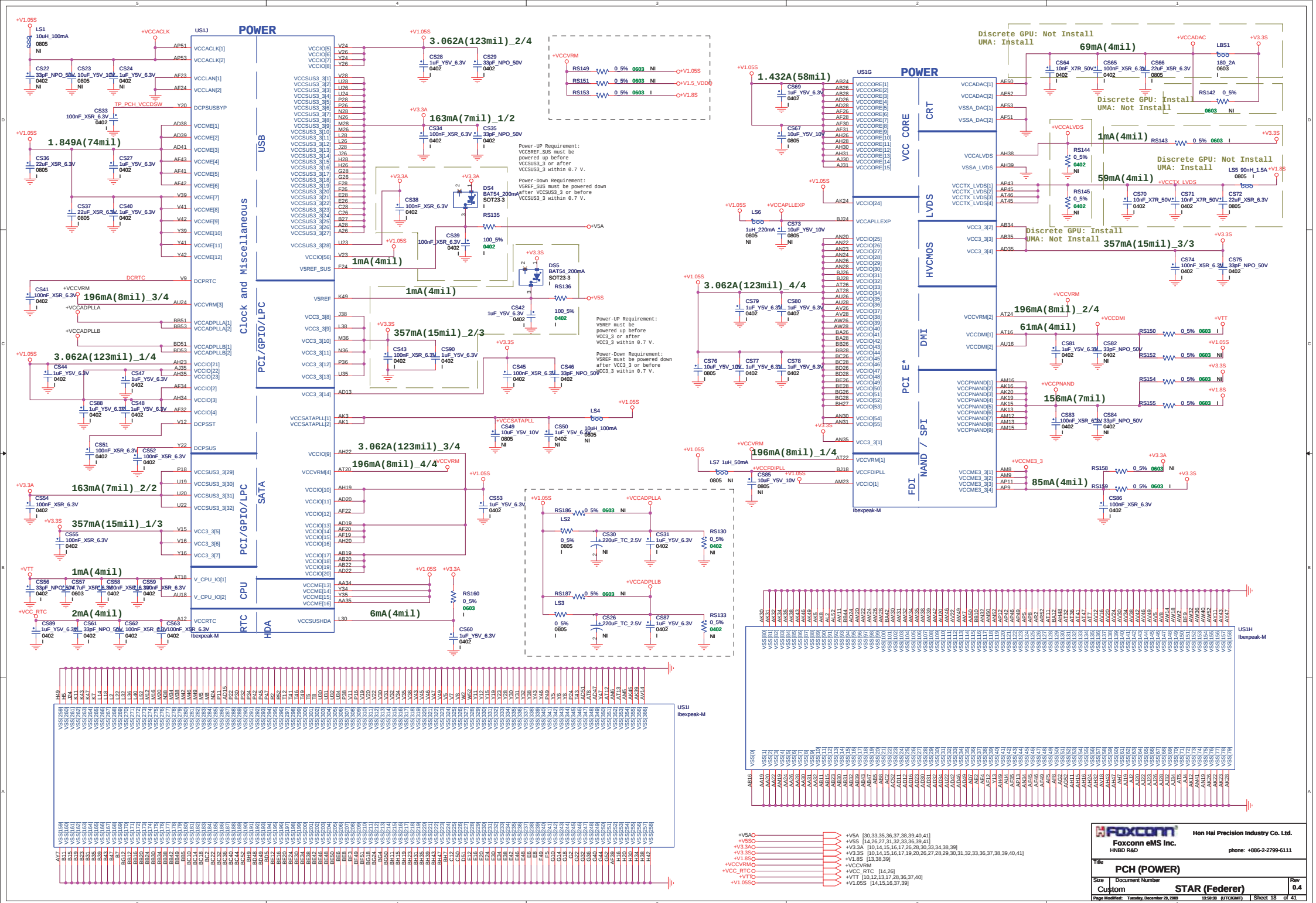


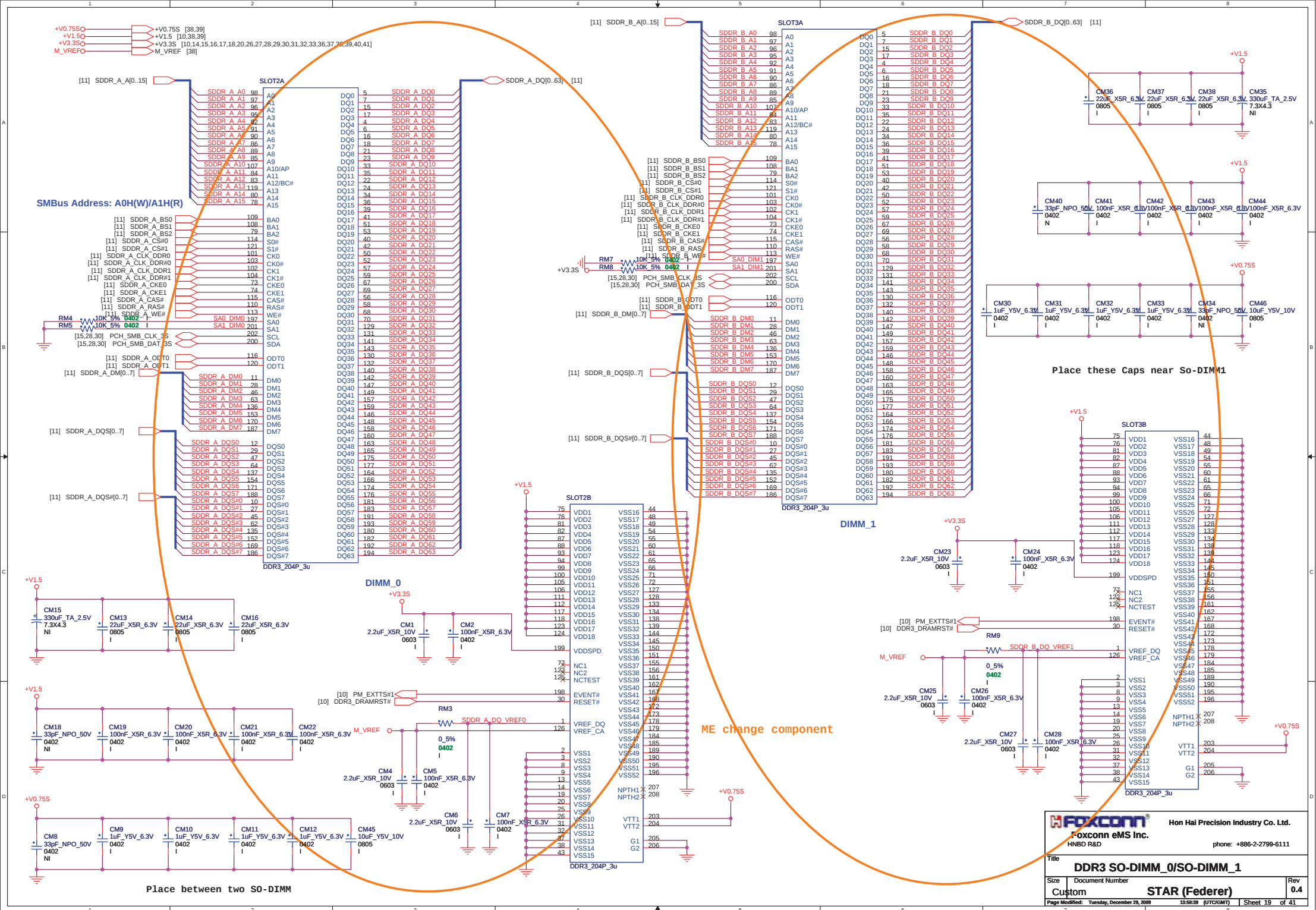


Device	Address	Size	Value	Device	Address	Size	Value
USB OC#0	0402	10K	5%	RS87			
USB OC#1	0402	10K	5%	RS88			
USB OC#2	0402	10K	5%	RS89			
USB OC#3	0402	10K	5%	RS90			
USB OC#4	0402	10K	5%	RS98			
USB OC#5	0402	10K	5%	RS103			
USB OC#6	0402	10K	5%	RS106			
EC WAKEUP#	0402	10K	5%	RS113			

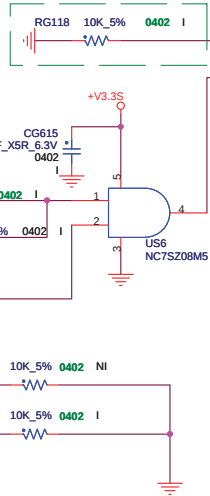


DVT Ask EC if we need to change GPIO pin.
GPIO8 can't be low.





M93-S3 Not Install
PARK-S3 Install 10K ohm



If no ROM attached, GPIO[13:12:11] ;
CONFIG(2:0)
controls the memory aperture size.

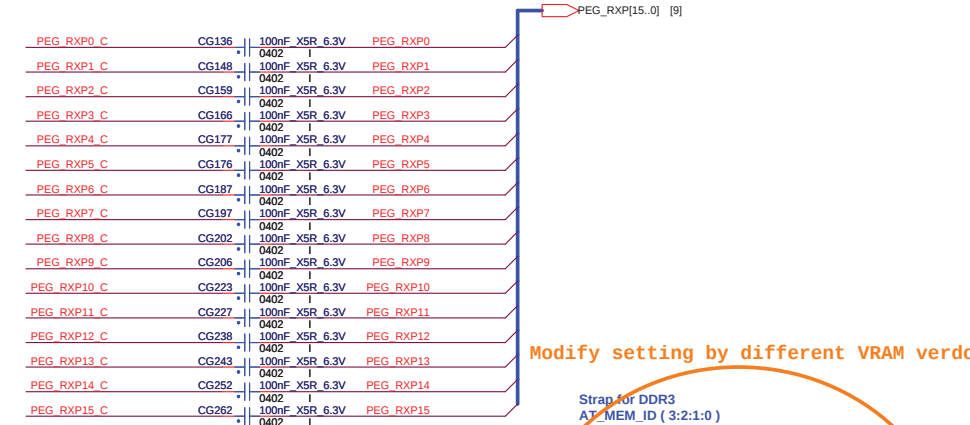
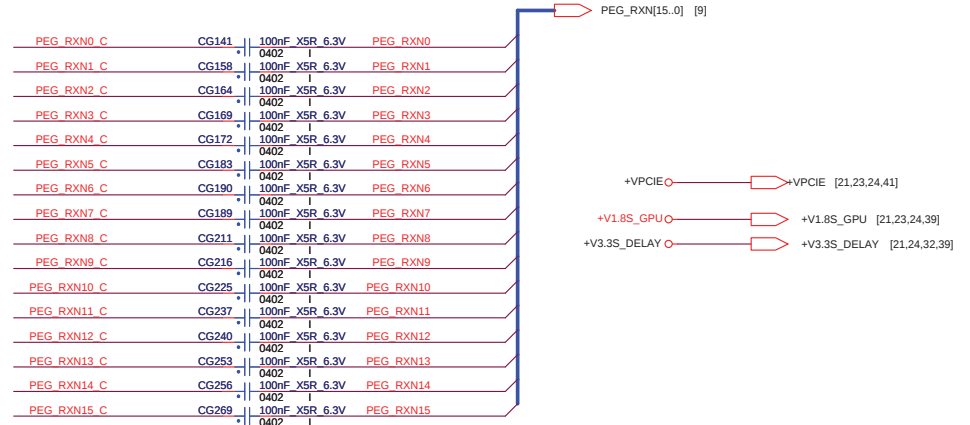
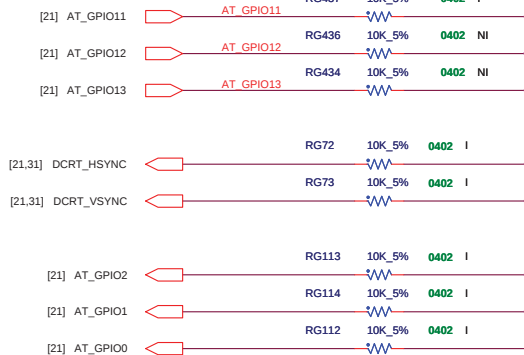
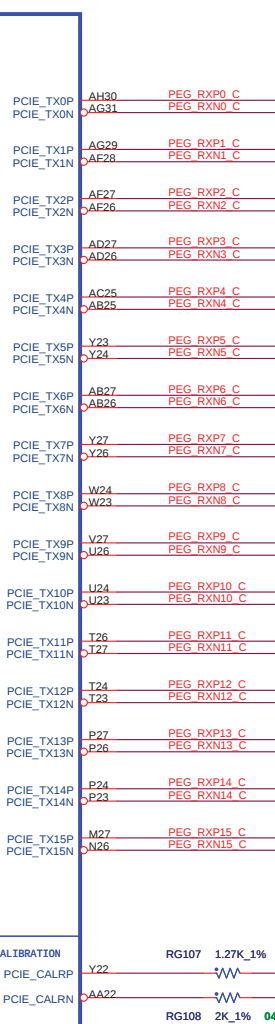
Reserved 011
512MB 001

HSYNC , VSYNC
AUD[1] , AUD[0]

0,0 No audio function
0,1 Audio for DisplayPort and HDMI if dongle is detected
1,0 Audio for DisplayPort only
1,1 Audio for both DisplayPort and HDMI

GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2 : PCIE GEN2 ENABLED

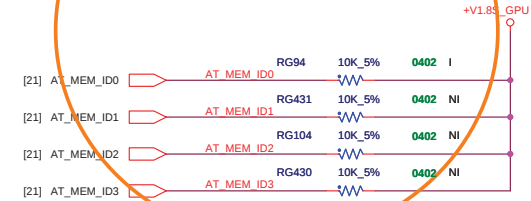
PCI EXPRESS INTERFACE



Modify setting by different VRAM vendor

Strap for DDR3
AT_MEM_ID (3:2:1:0)

0000	64Mx16	Samsung (K4W1G1646E-HC12)	512MB
0001	64Mx16	Hynix (H5TQ1G63BFR-12C)	512MB
0010	128Mx16	Samsung (K4W2G1646B-HC12)	1GB
0100	128Mx16	Samsung (K4W2G1646C-HCxx)	1GB
1000	128Mx16	Hynix (H5TQ2G63BFR-12C)	1GB
1001	128Mx16	Micron (MT41J128M16HA-12)	1GB



**Hon Hai Precision Industry Co. Ltd.**
Foxconn eMS Inc.
HNBD R&D
phone: +886-2-2799-6111

Title
VGA (PCI-E/STRAP) 1/5

Size
Document Number
Custom STAR (Federer)

Rev
0.4

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M93-S3:Not Install
PARK-S3:Install

Del NorFlash parts

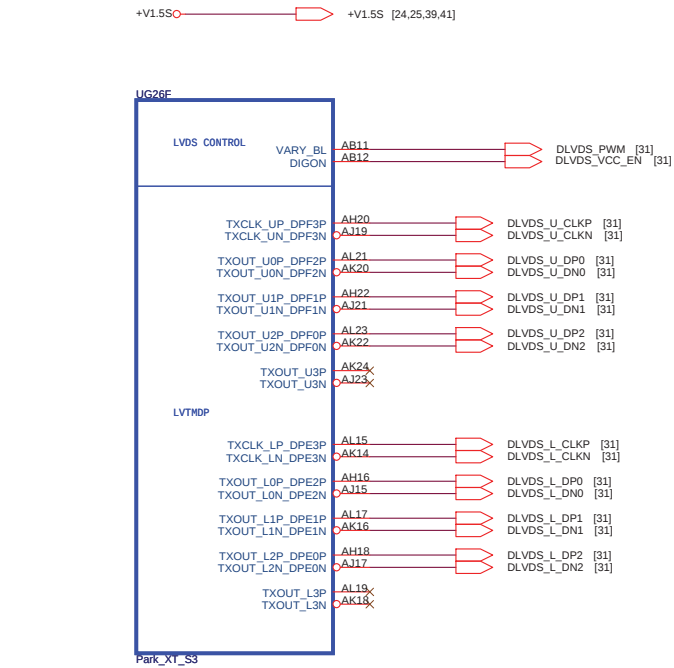
clock source change to clock gen.

M93-S3 Install
PARK-S3 Not Install

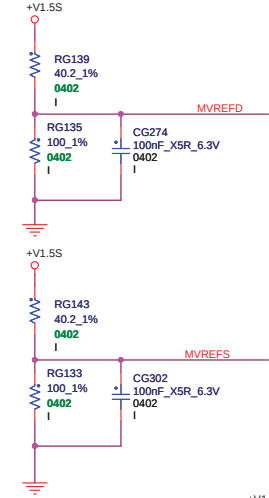
M93-S3:Not Install
PARK-S3:Install

AT_DPLL_VDDC:
M93 1.1V@150mA
Park 1.0V@125mA

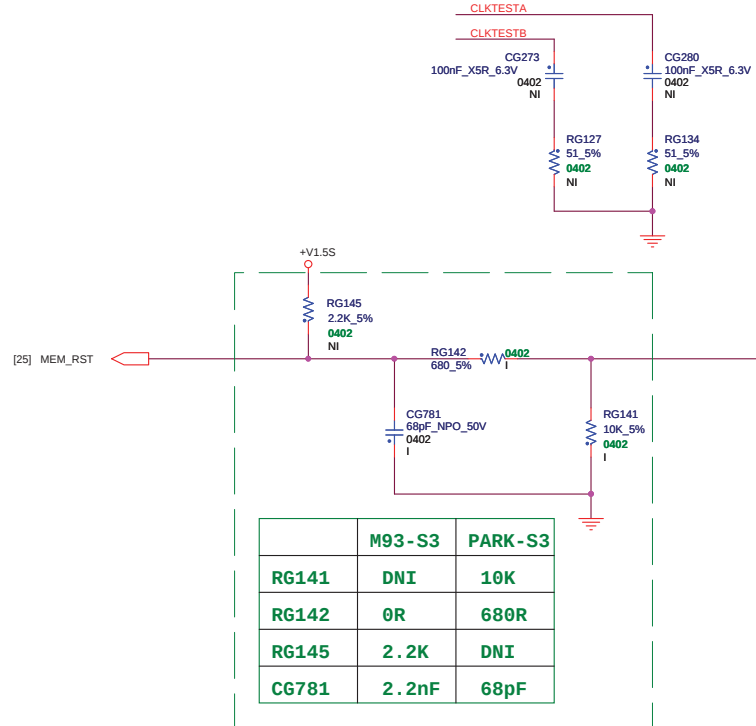
M93-S3 Not Install
PARK-S3 Install



PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC



M93-S3 No Install
PARK-S3 Install



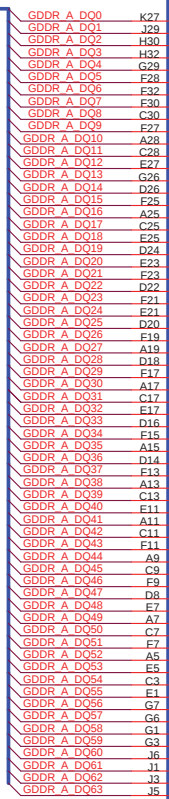
	M93-S3	PARK-S3
RG141	DNI	10K
RG142	0R	680R
RG145	2.2K	DNI
CG781	2.2nF	68pF

M93-S3 Install
PARK-S3 Not Install

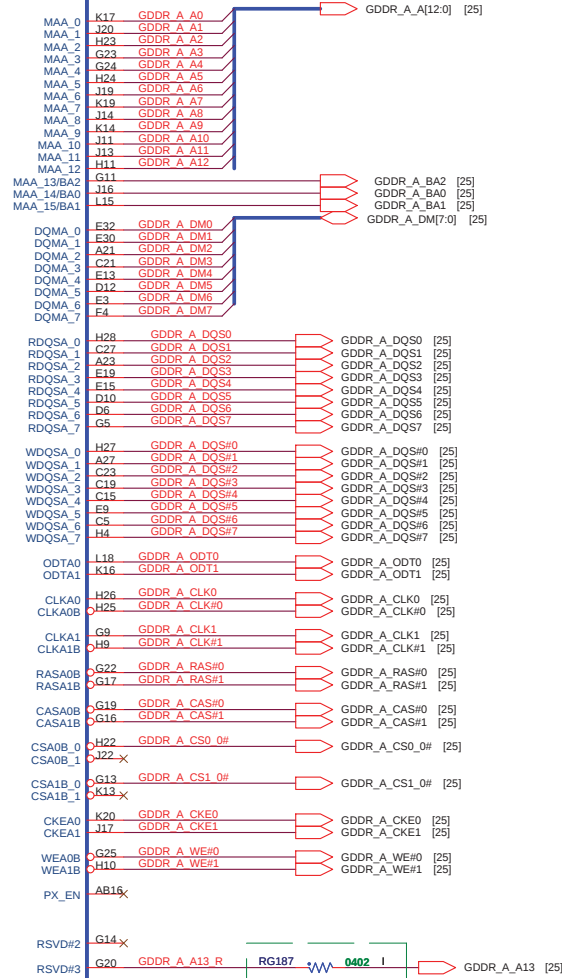
M93-S3 Not Install
PARK-S3 Install

M93-S3 Install 240 ohm
PARK-S3 Install 150 ohm

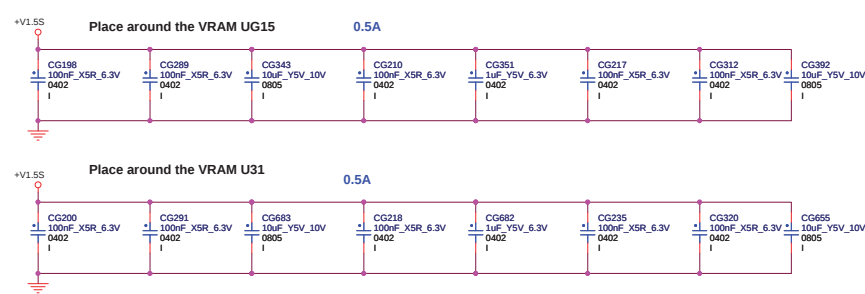
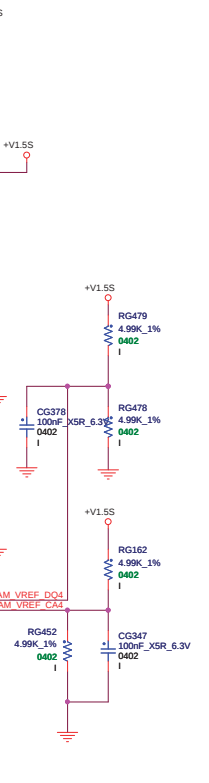
[25] GDDR_A_DQ[63:0]

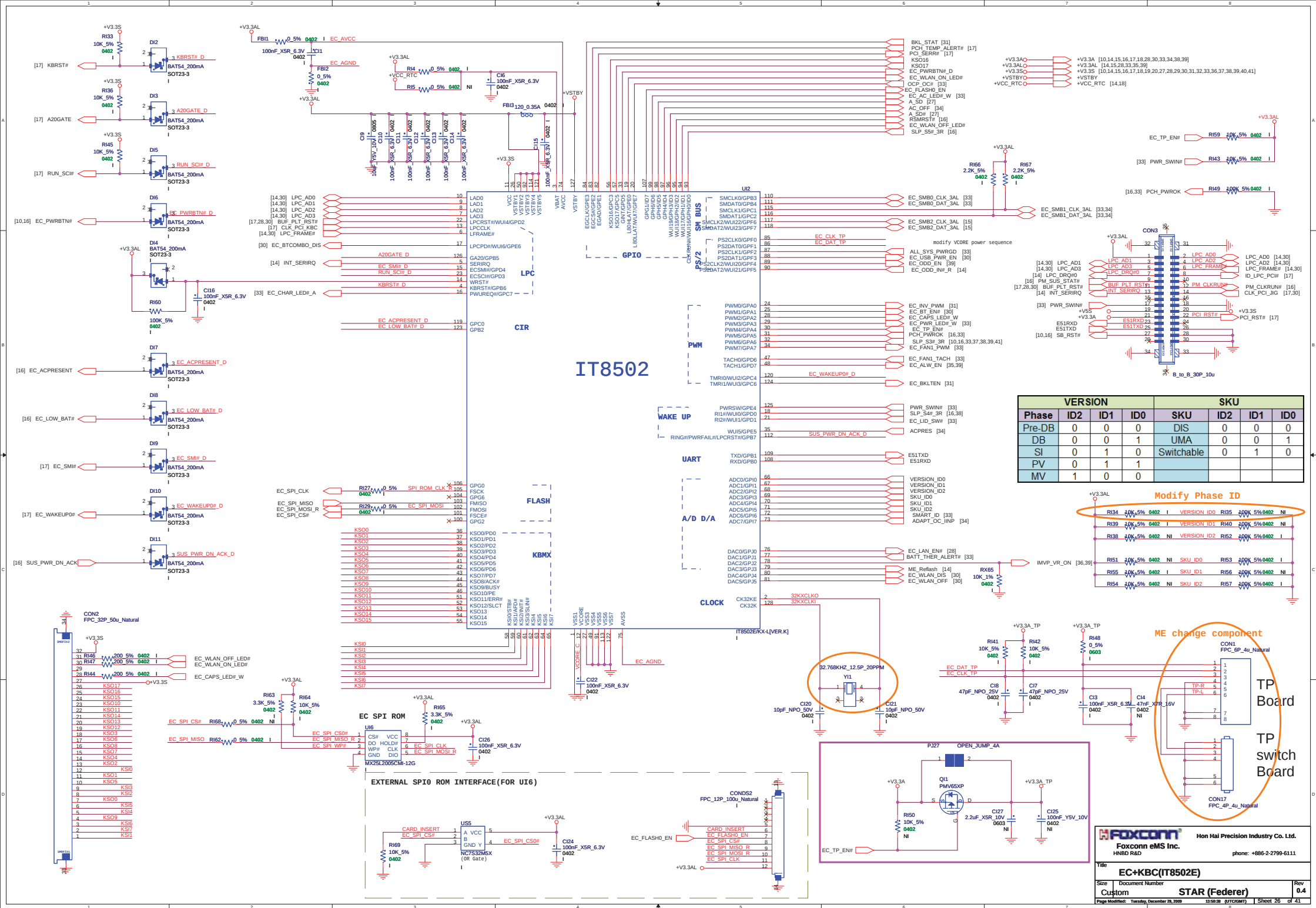


MEMORY INTERFACE

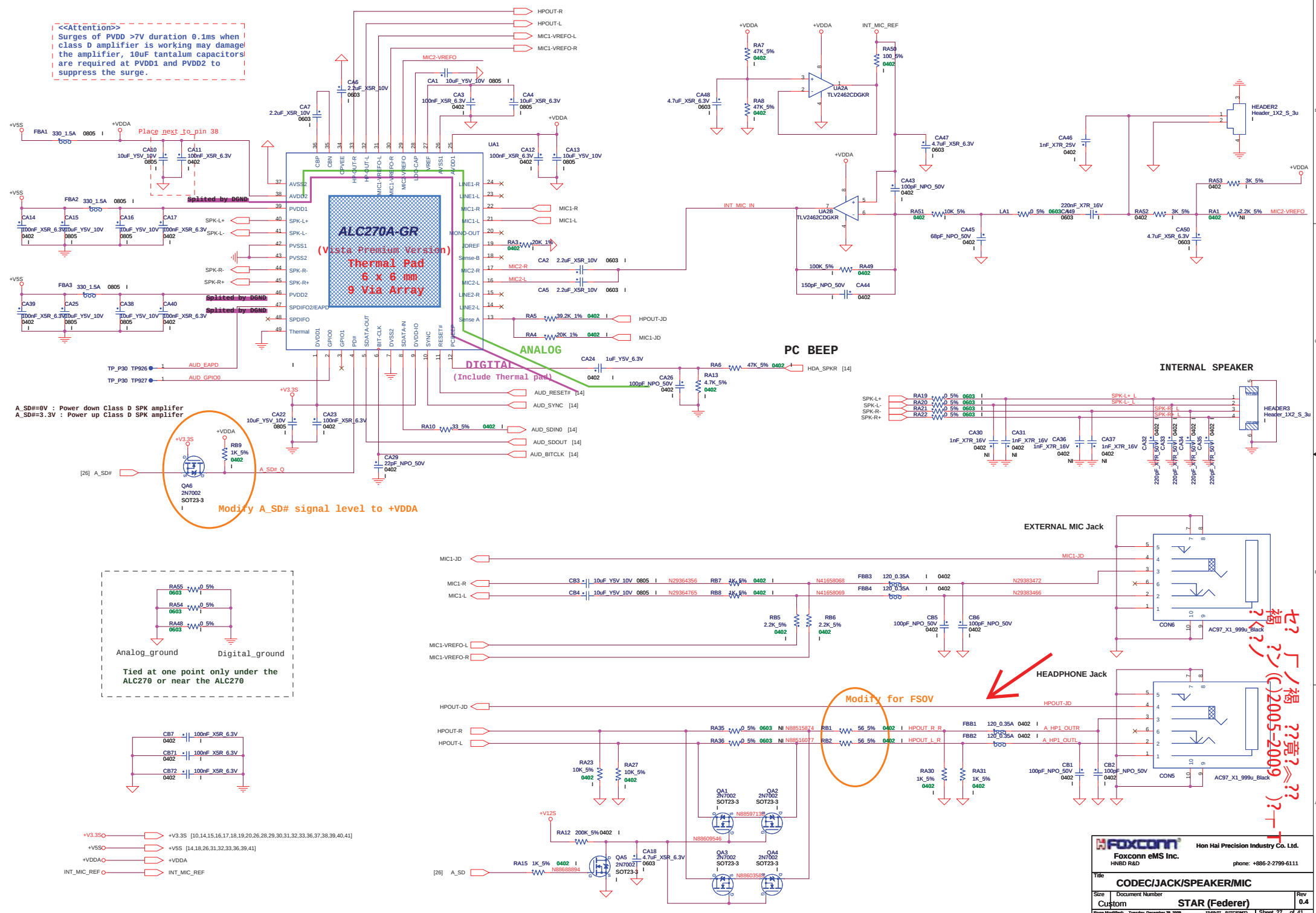


M93-S3 No Install
PARK-S3 Install

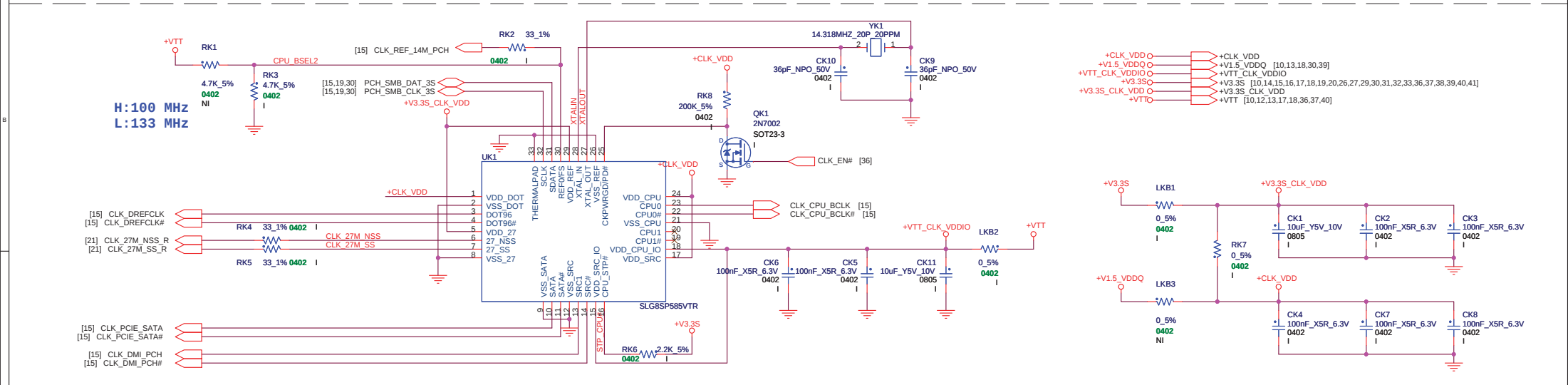
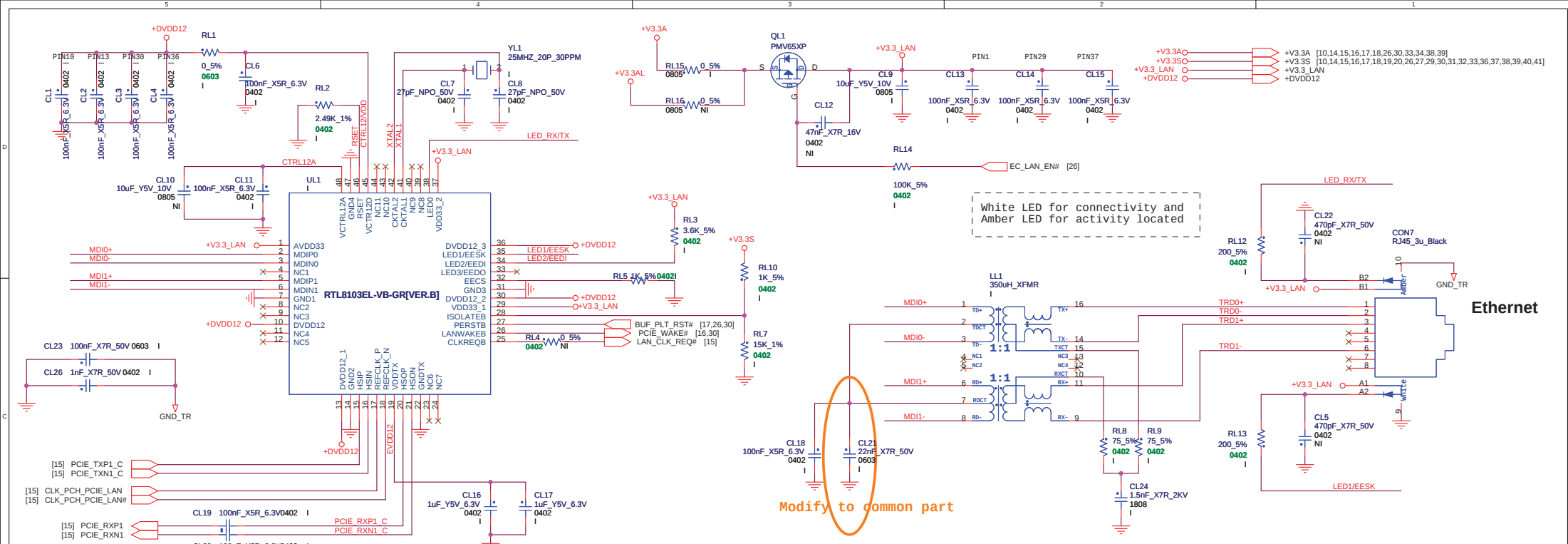




<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier. 40uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.



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FSP Table

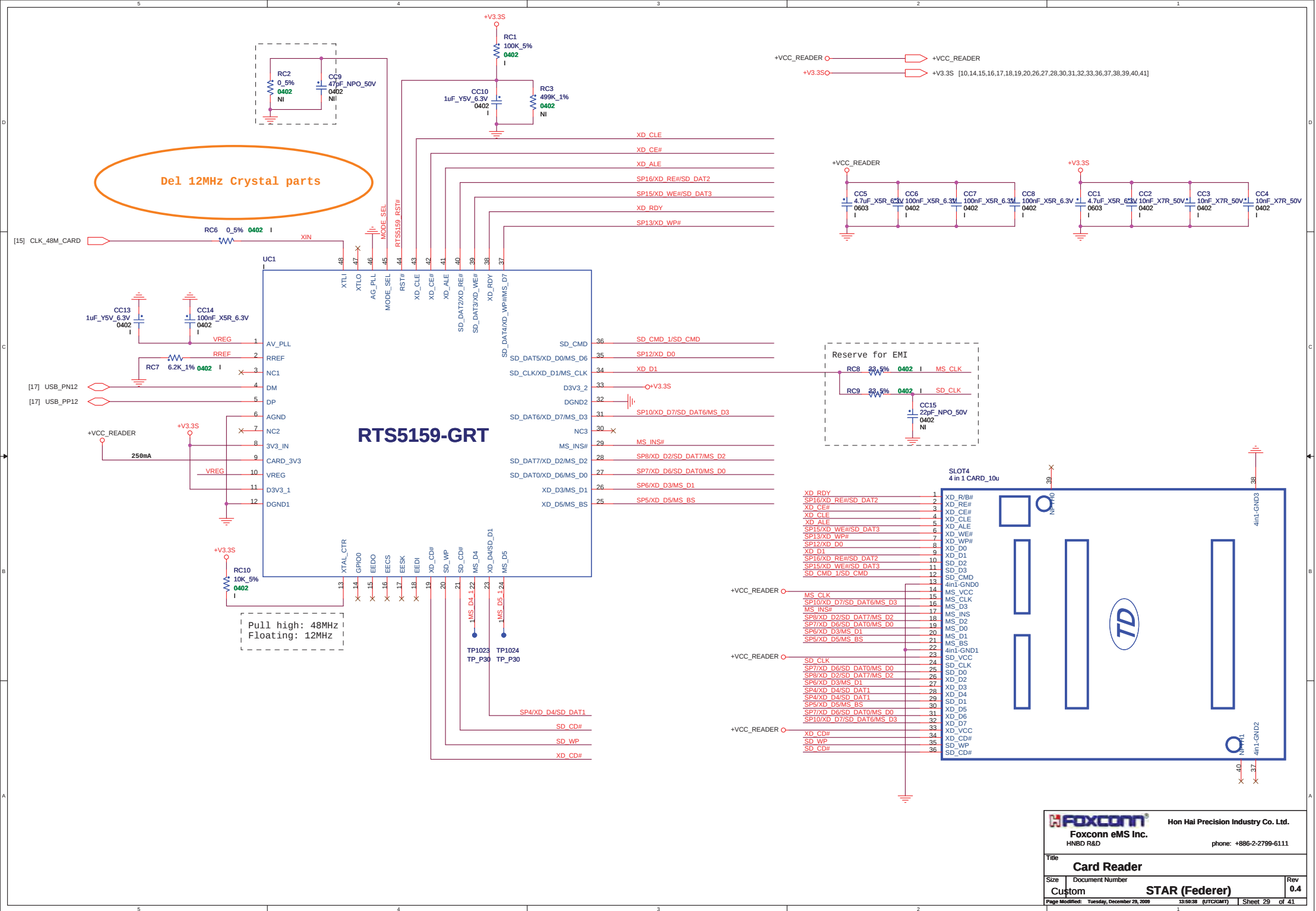
FS	CPU (PCH ->CPU)	Power On	SRC(DMI) (PCH ->CPU)	SATA (PCH)	DOT96 (PCH)	27MHz (GPU)	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

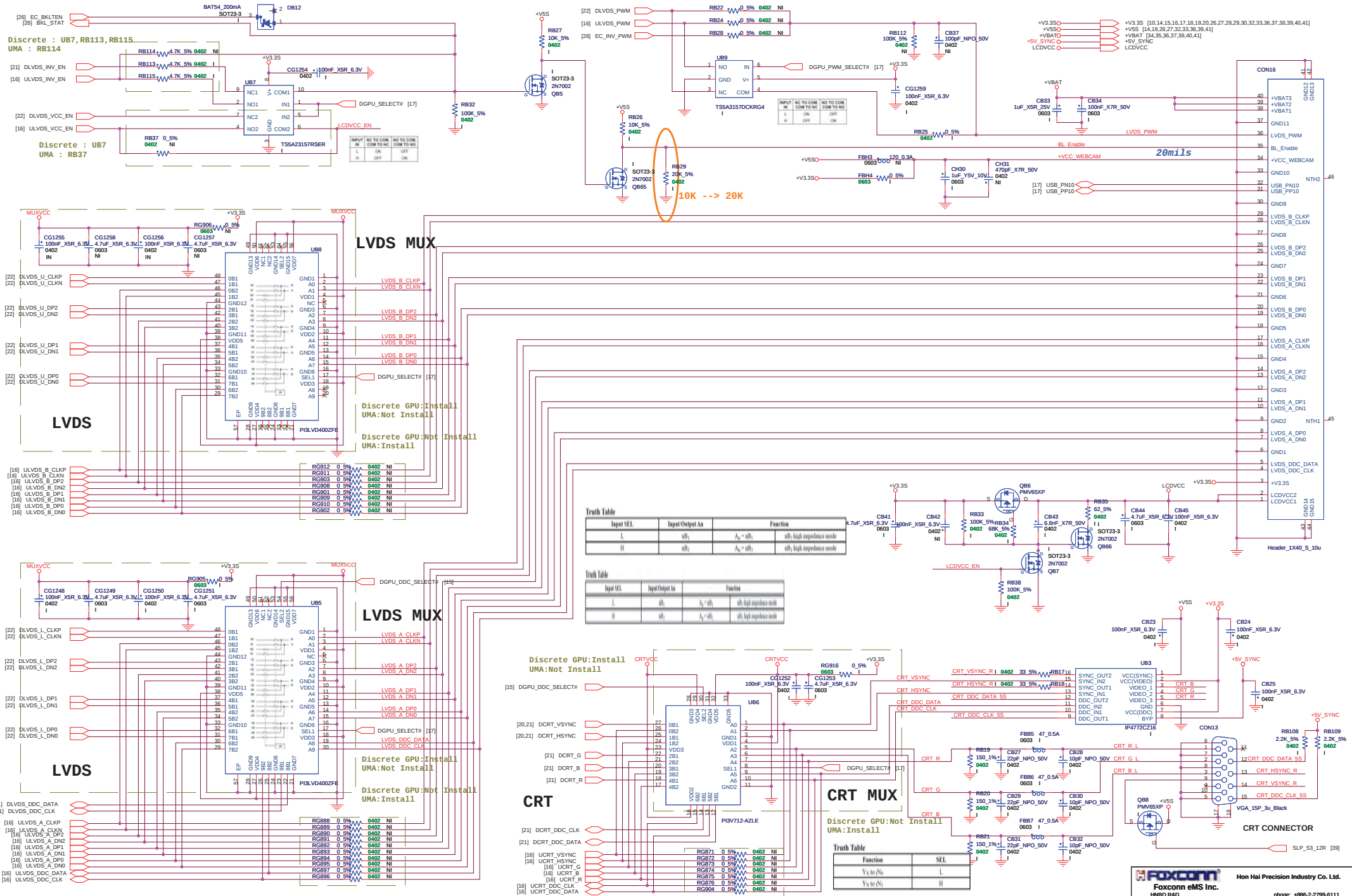
FOXCONN Hon Hai Precision Industry Co. Ltd.
Foxconn eMS Inc.
HNBD R&D phone: +886-2-2799-6111

Title **LAN (RTL8103EL)/CLOCK GEN**

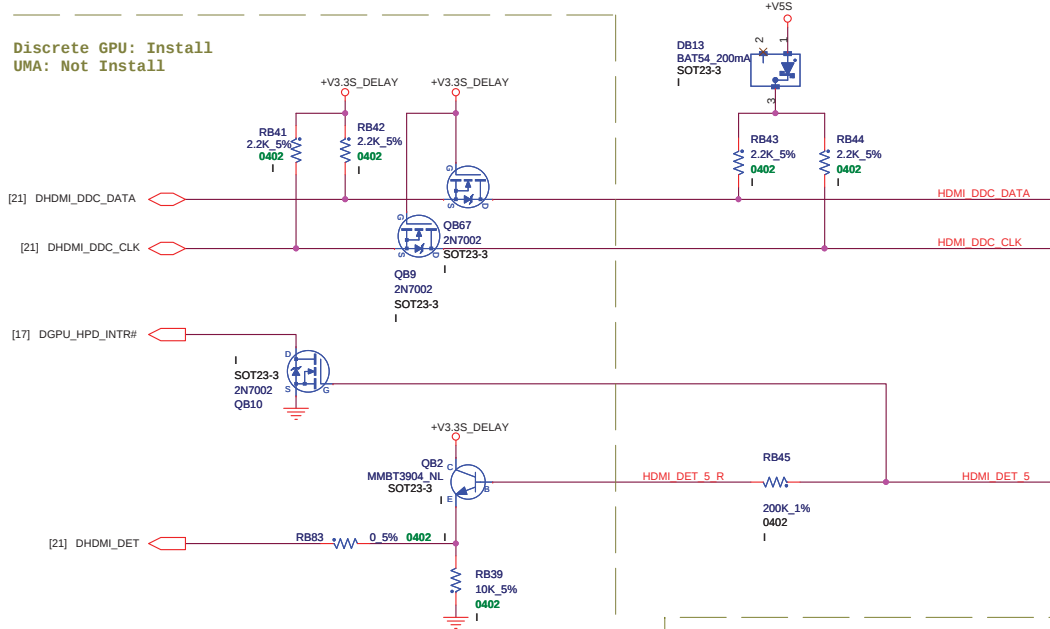
Size Document Number **Custom STAR (Federer)** Rev **0.4**

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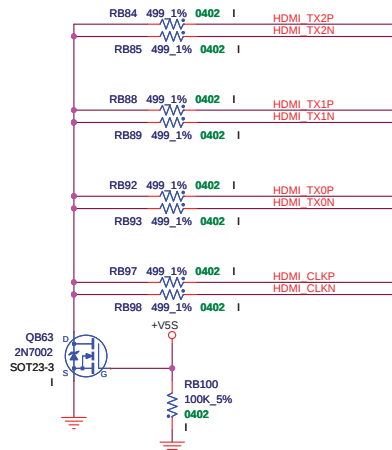




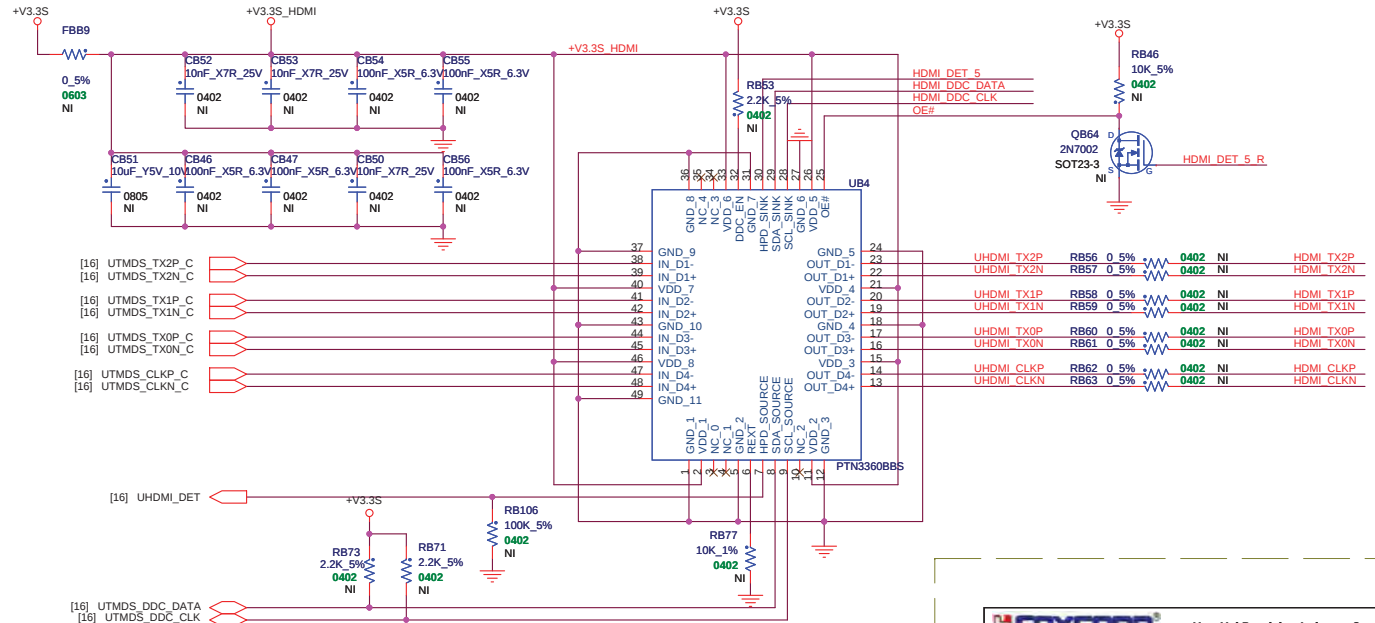
Discrete GPU: Install
UMA: Not Install



[21] DHDMI_TX2P	CB63 0402	100nF X5R 6.3V	I	HDMI TX2P
[21] DHDMI_TX2N	CB64 0402	100nF X5R 6.3V	I	HDMI TX2N
[21] DHDMI_TX1P	CB65 0402	100nF X5R 6.3V	I	HDMI TX1P
[21] DHDMI_TX1N	CB66 0402	100nF X5R 6.3V	I	HDMI TX1N
[21] DHDMI_TX0P	CB67 0402	100nF X5R 6.3V	I	HDMI TX0P
[21] DHDMI_TX0N	CB68 0402	100nF X5R 6.3V	I	HDMI TX0N
[21] DHDMI_CLKP	CB69 0402	100nF X5R 6.3V	I	HDMI CLKP
[21] DHDMI_CLKN	CB70 0402	100nF X5R 6.3V	I	HDMI CLKN

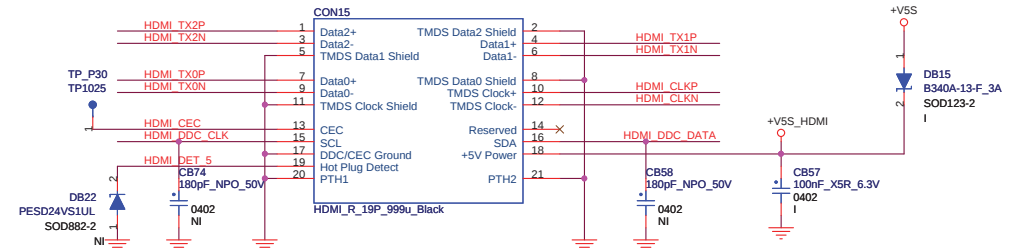


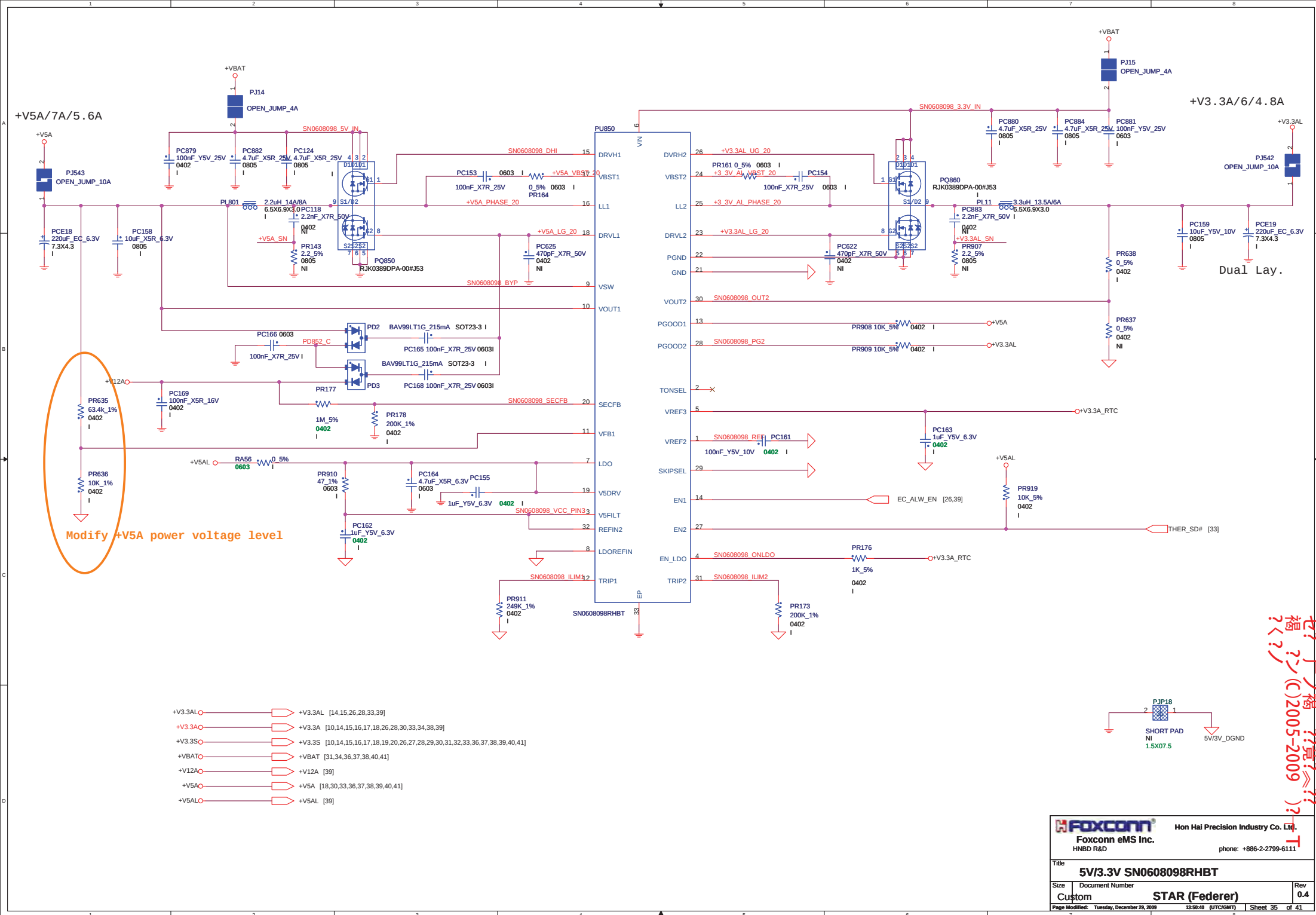
Discrete GPU:Not Install
UMA:Install



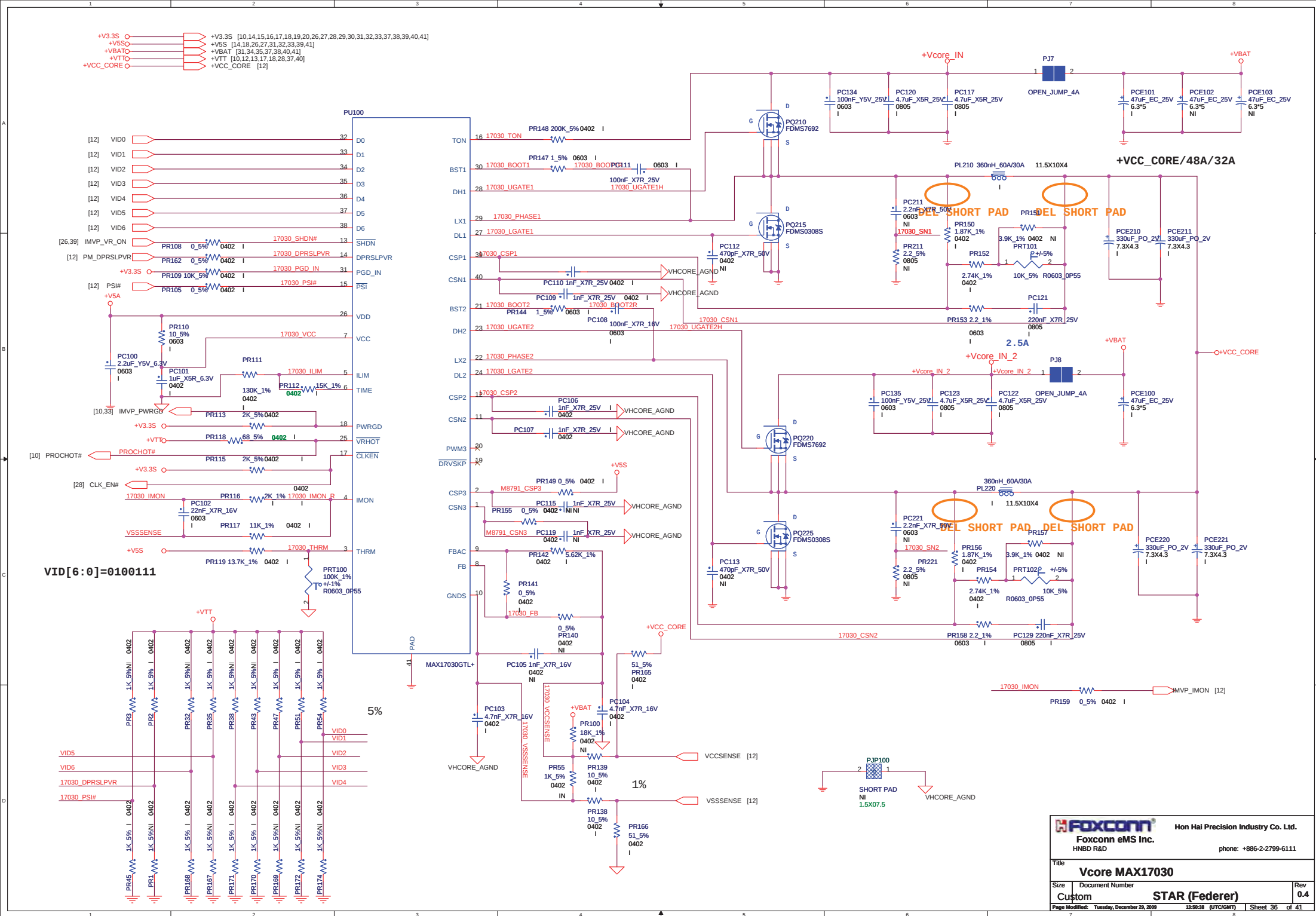
+V5S	→	+V5S [14,18,26,27,31,33,36,39,41]
+V3.3S	→	+V3.3S [10,14,15,16,17,18,19,20,26,27,28,29,30,31,33,36,37,38,39,40,41]
+V3.3S_DELAY	→	+V3.3S_DELAY [20,21,24,39]
+V5S_HDMI	→	+V5S_HDMI
+V3.3S_HDMI	→	+V3.3S_HDMI

HDMI spec: +5V:4.7V min , 55mA max.

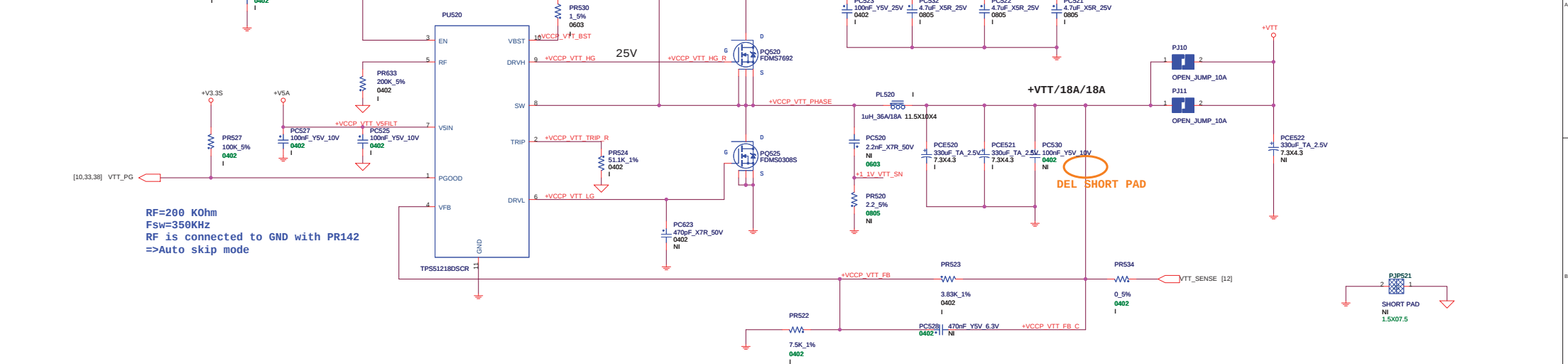




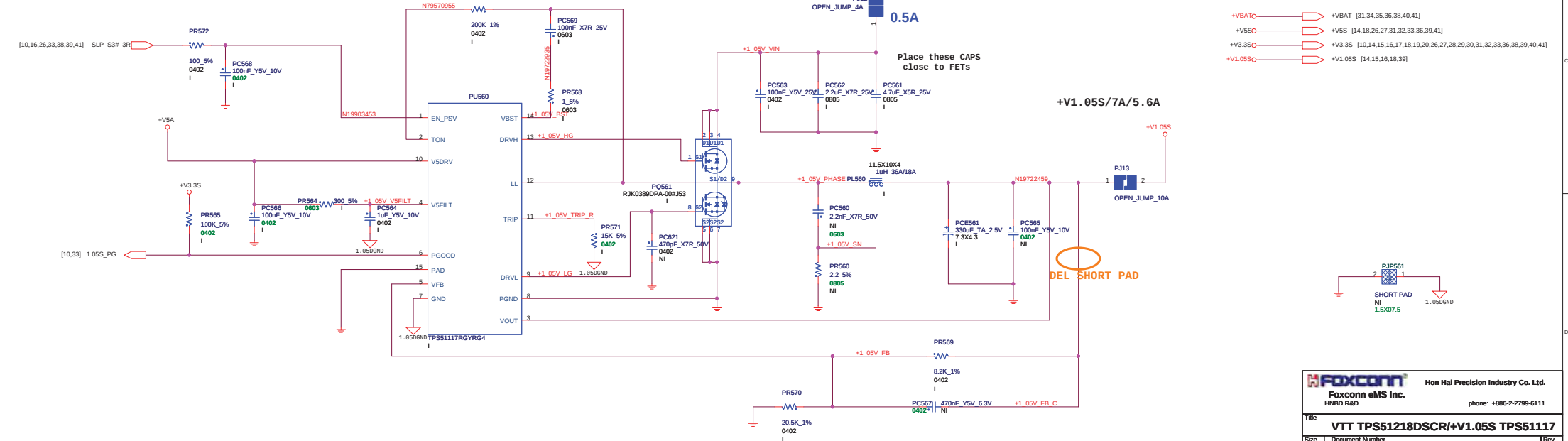
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褐? ? (C) 2005-2009 ?
? < ?



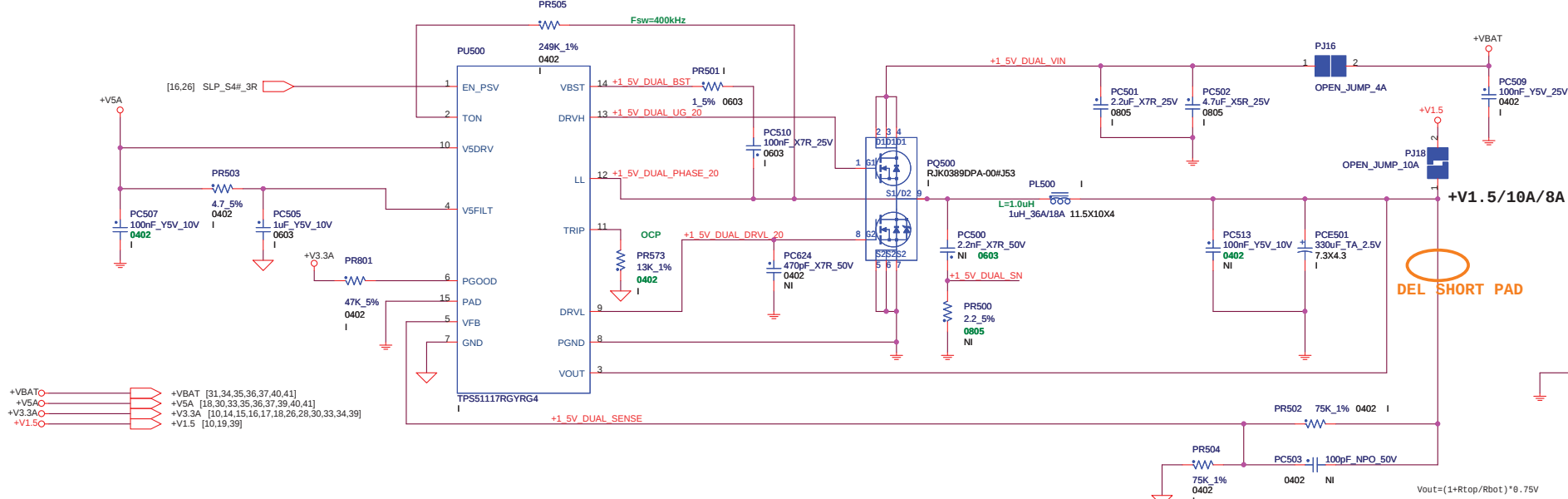
+VTT TPS51218



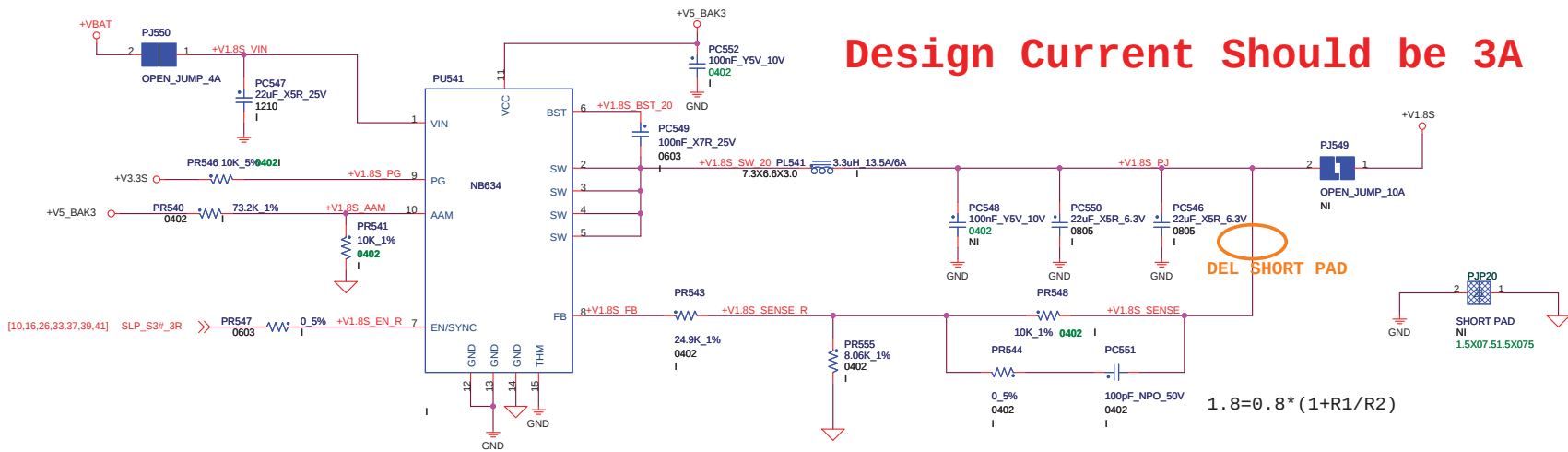
+V1.05S TPS51117



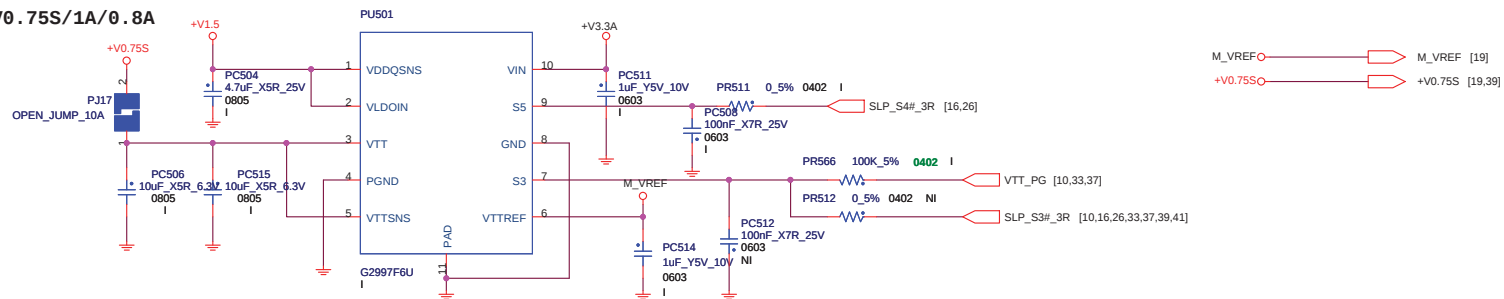
Frequency is 400K HZ
D-CAP Mode
Set Iocp point at 12A

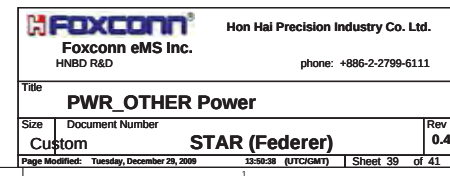


Design Current Should be 3A

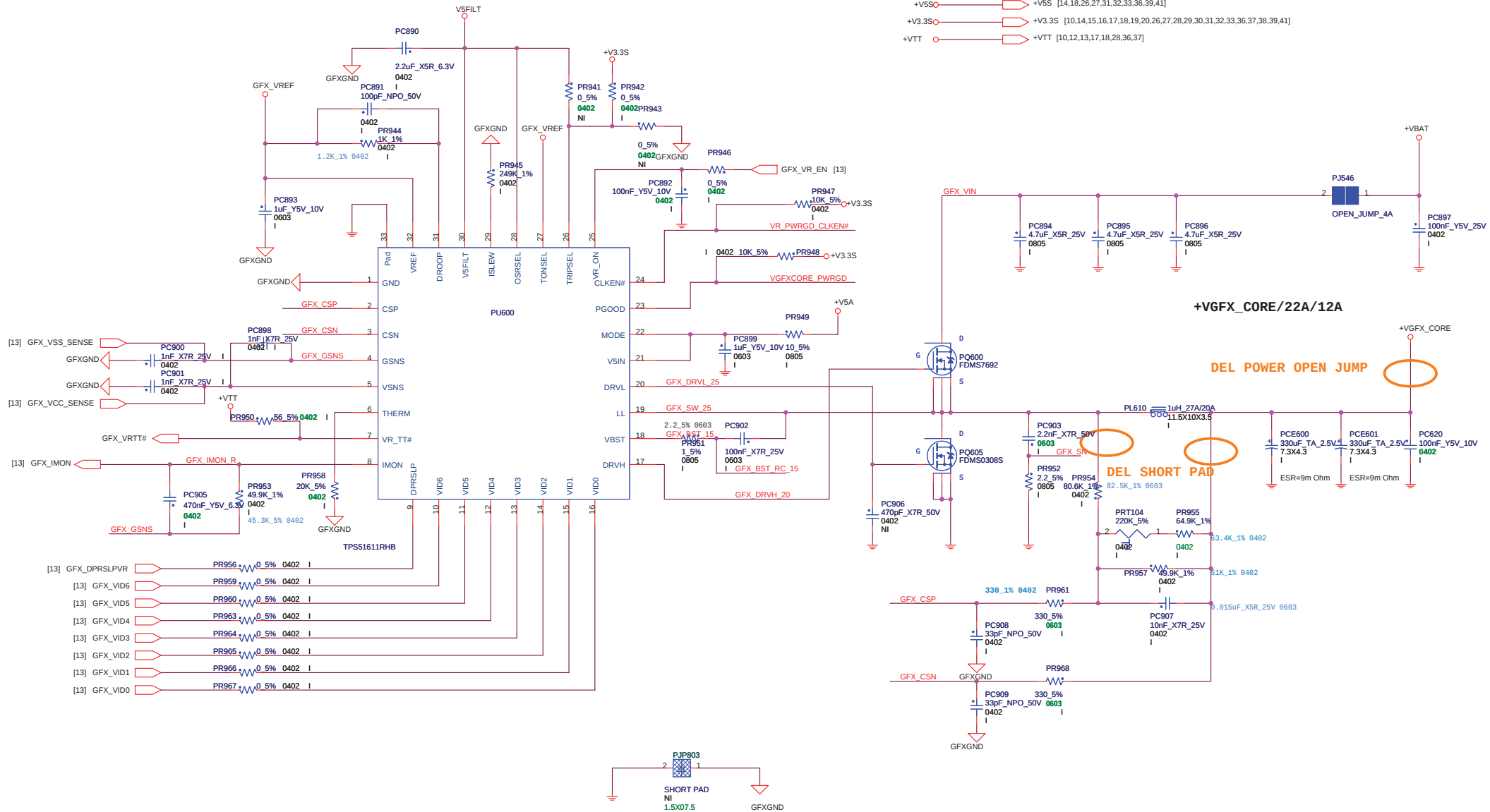


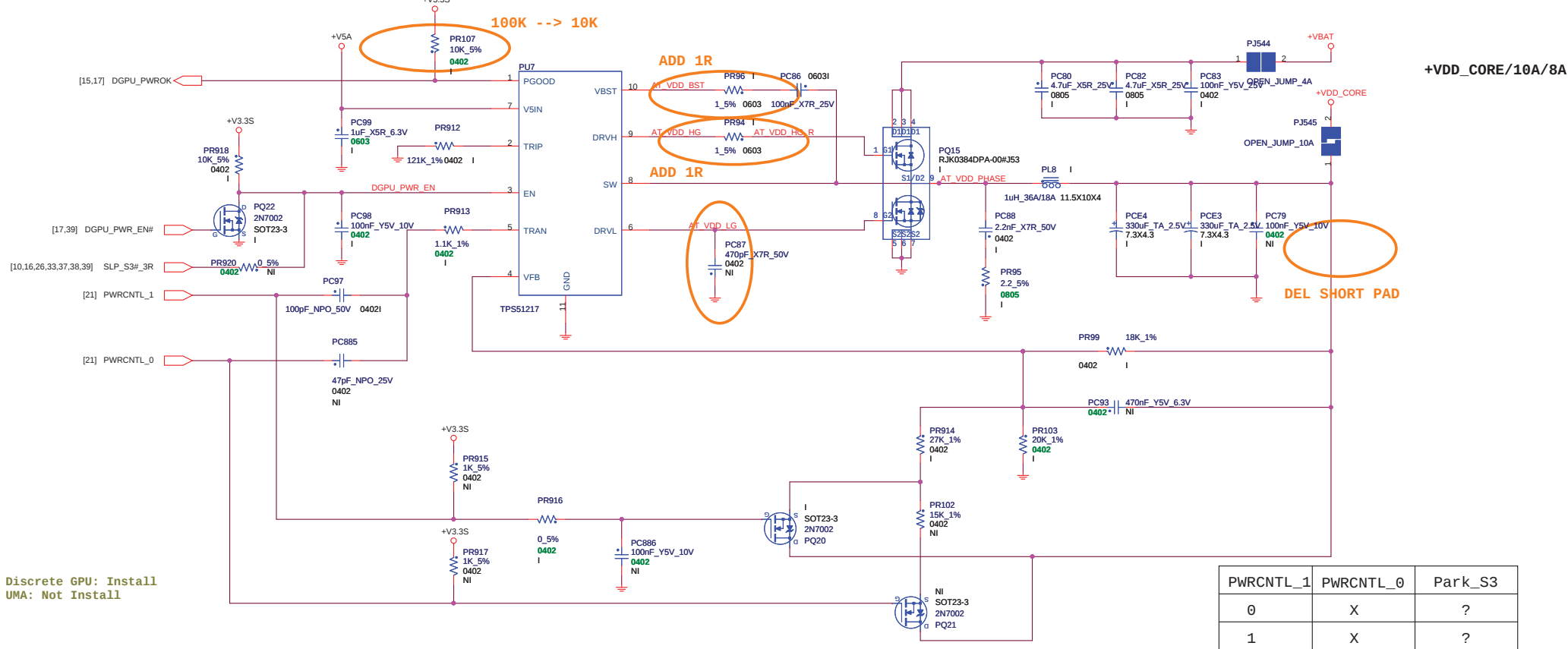
+V0.75S/1A/0.8A



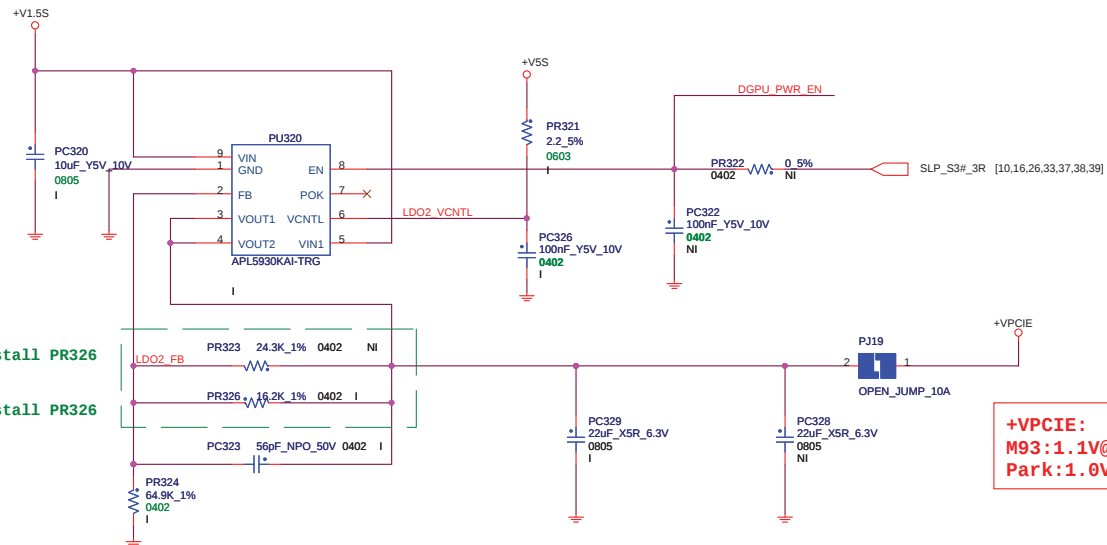


+VGFXCORE





Discrete GPU: Install
UMA: Not Install



- +VBAT [31,34,35,36,37,38,40]
- +V5A [18,30,33,35,36,37,38,39,40]
- +V5S [14,18,26,27,31,32,33,36,39]
- +V3.3S [10,14,15,16,17,18,19,20,26,27,28,29,30,31,32,33,36,37,38,39,40]
- +V1.5S [22,24,25,39]
- +VDD_CORE [24]
- +VPCIE [20,21,23,24]