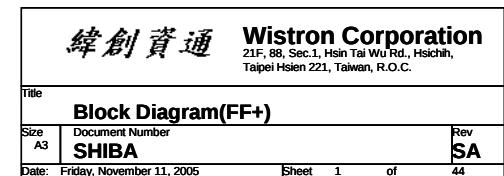
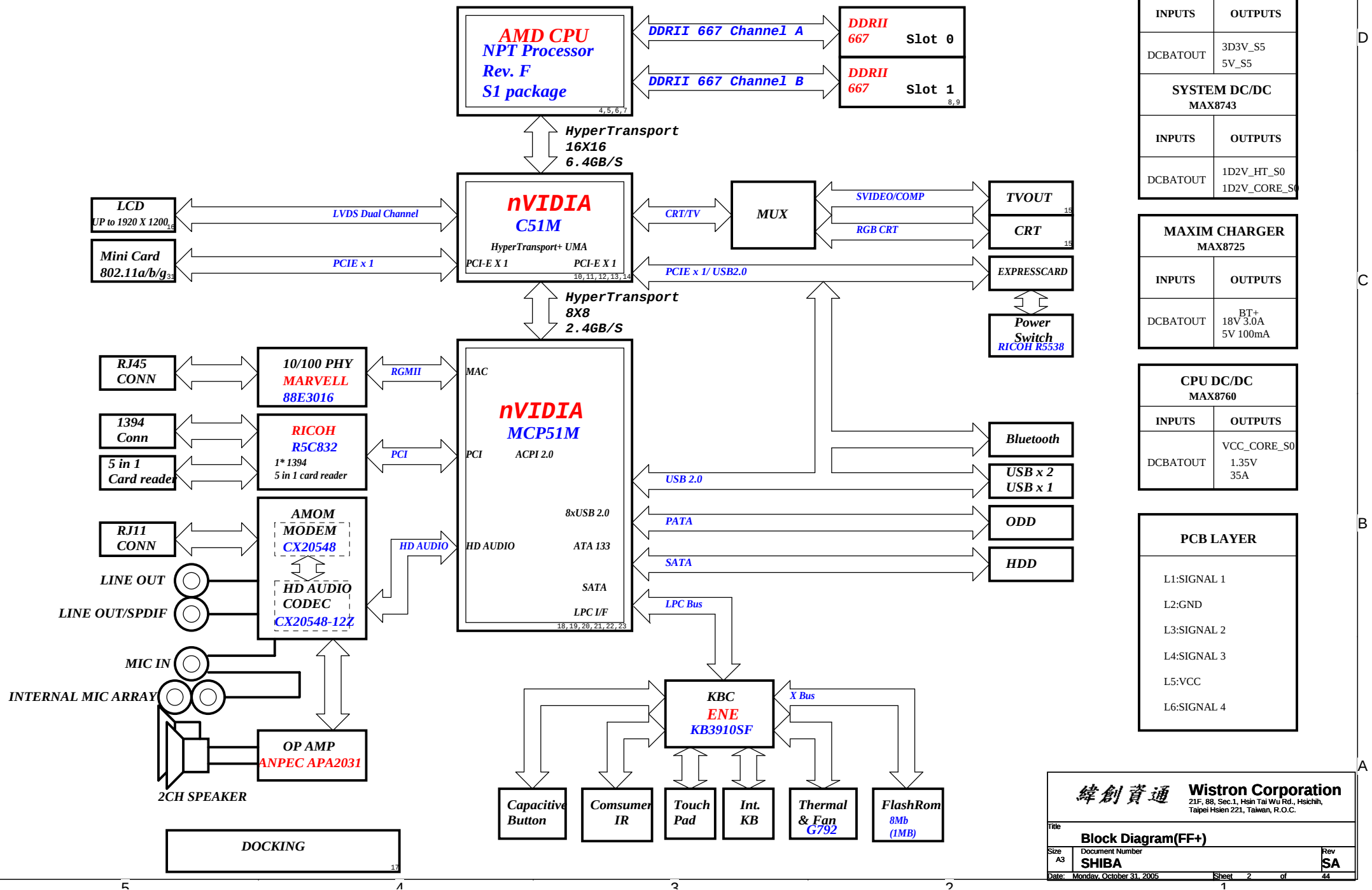


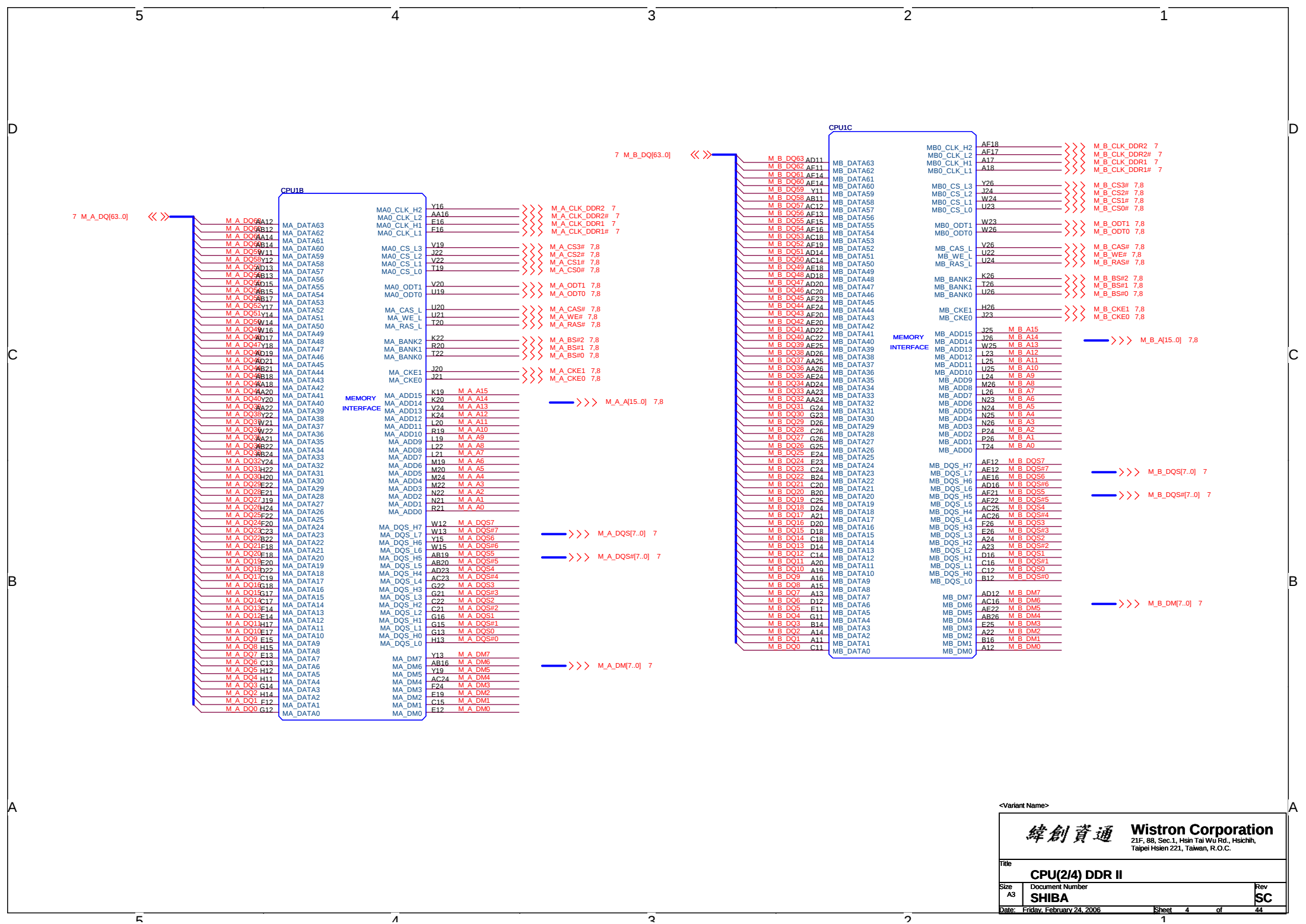
Project Code: 91.4F701.001
Project Name: Shiba
PCB Number: 05234

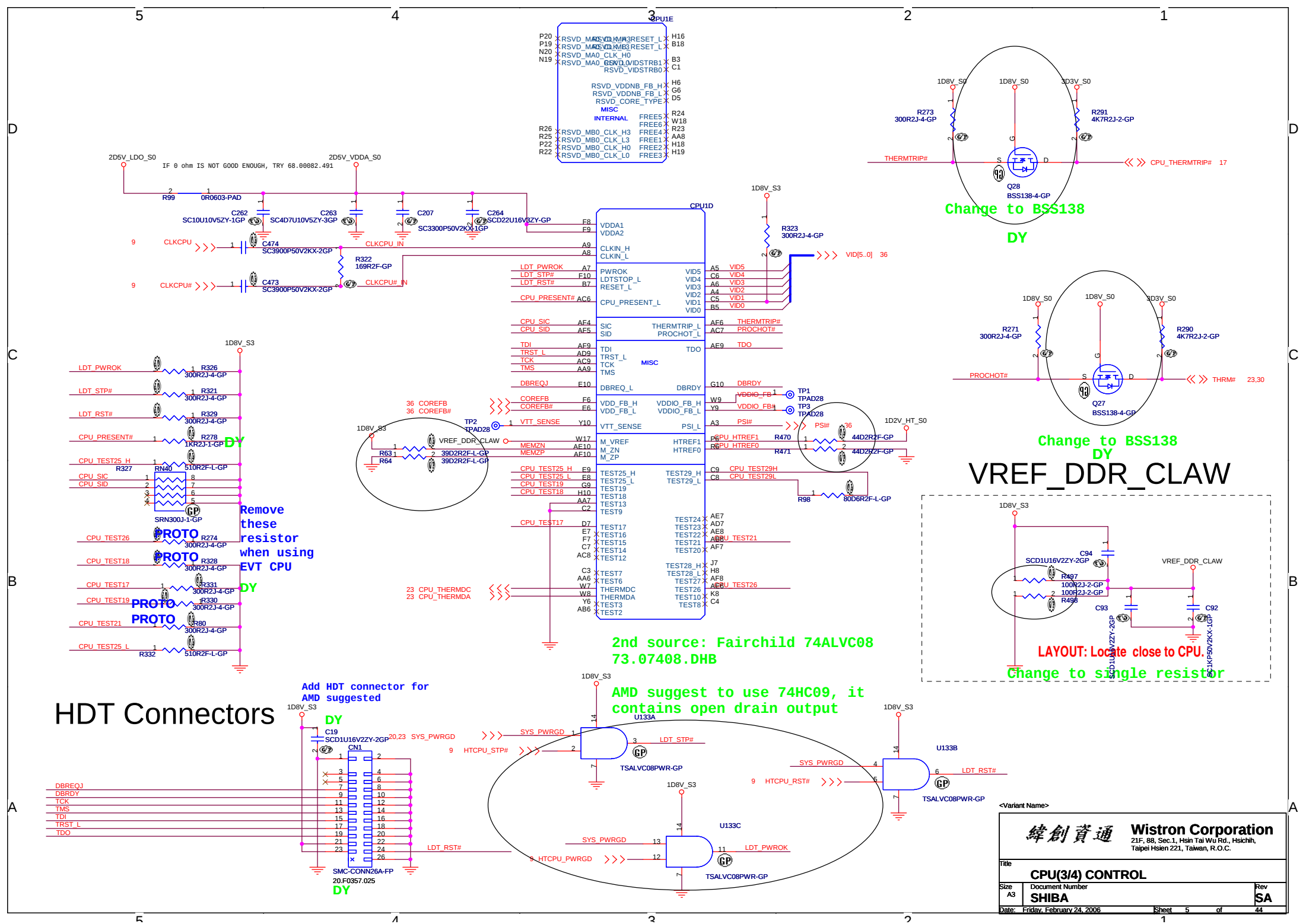


Shiba Block Diagram(DF)



SC





HDT Connectors

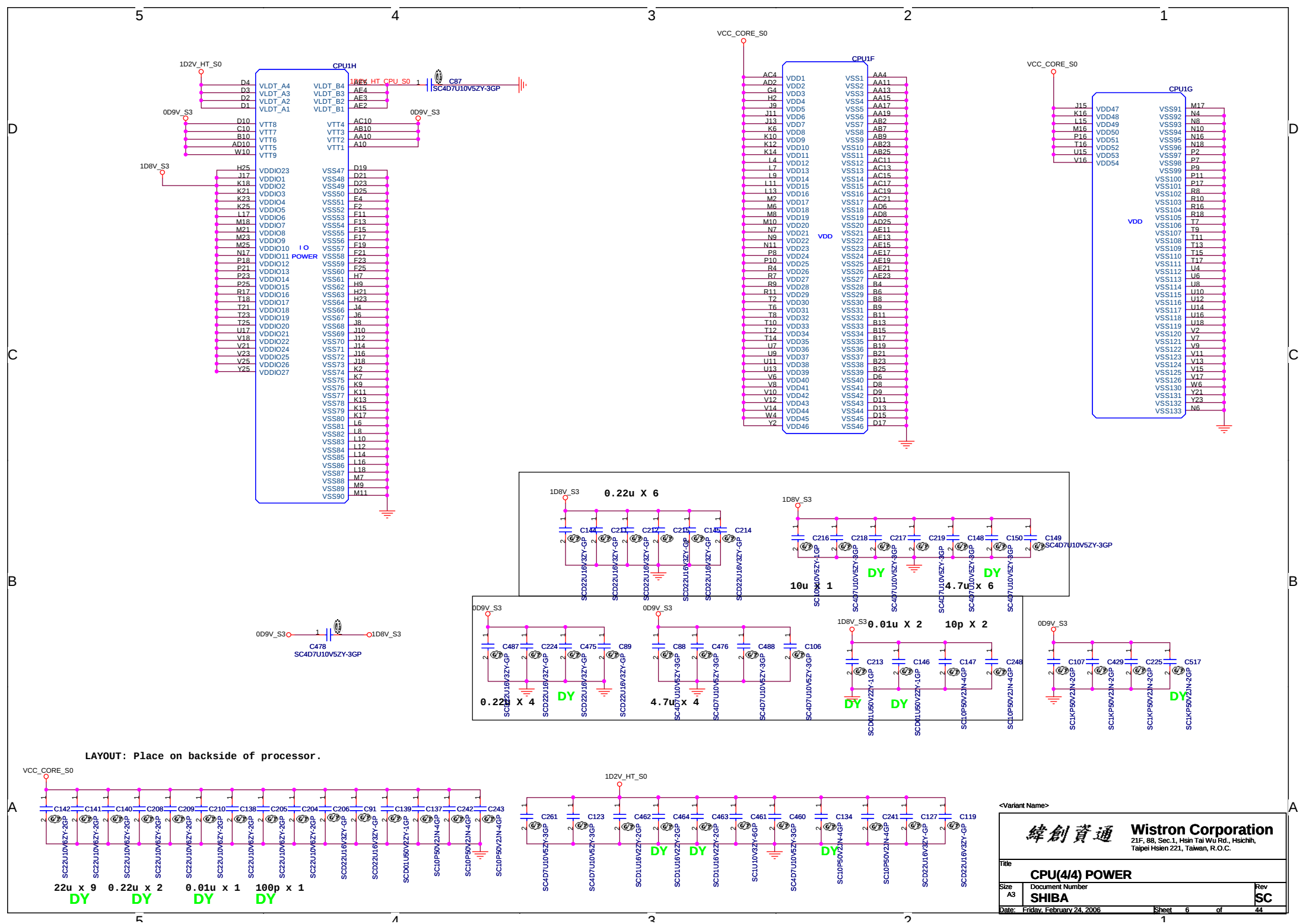
2nd source: Fairchild 74ALVC08
73.07408.DHB

AMD suggest to use 74HC09, it
contains open drain output

Change to BSS138
DY
VREF_DDR_CLAW

LAYOUT: Locate close to CPU.
Change to single resistor

<Variant Name>			
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU(3/4) CONTROL			
Size A3	Document Number SHIBA		Rev SA
Date: Friday, February 24, 2006	Sheet 5	of	44



LAYOUT: Place on backside of processor.

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd.,, Hsinchi,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU(4/4) POWER

Size

A3

Document Number

SHIBA

Rev

SC

Date

Friday, February 24, 2006

Sheet

6

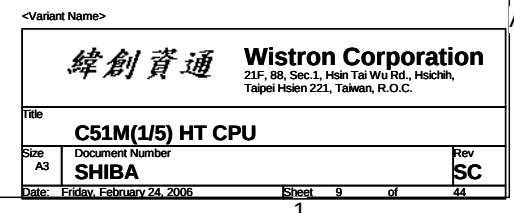
of

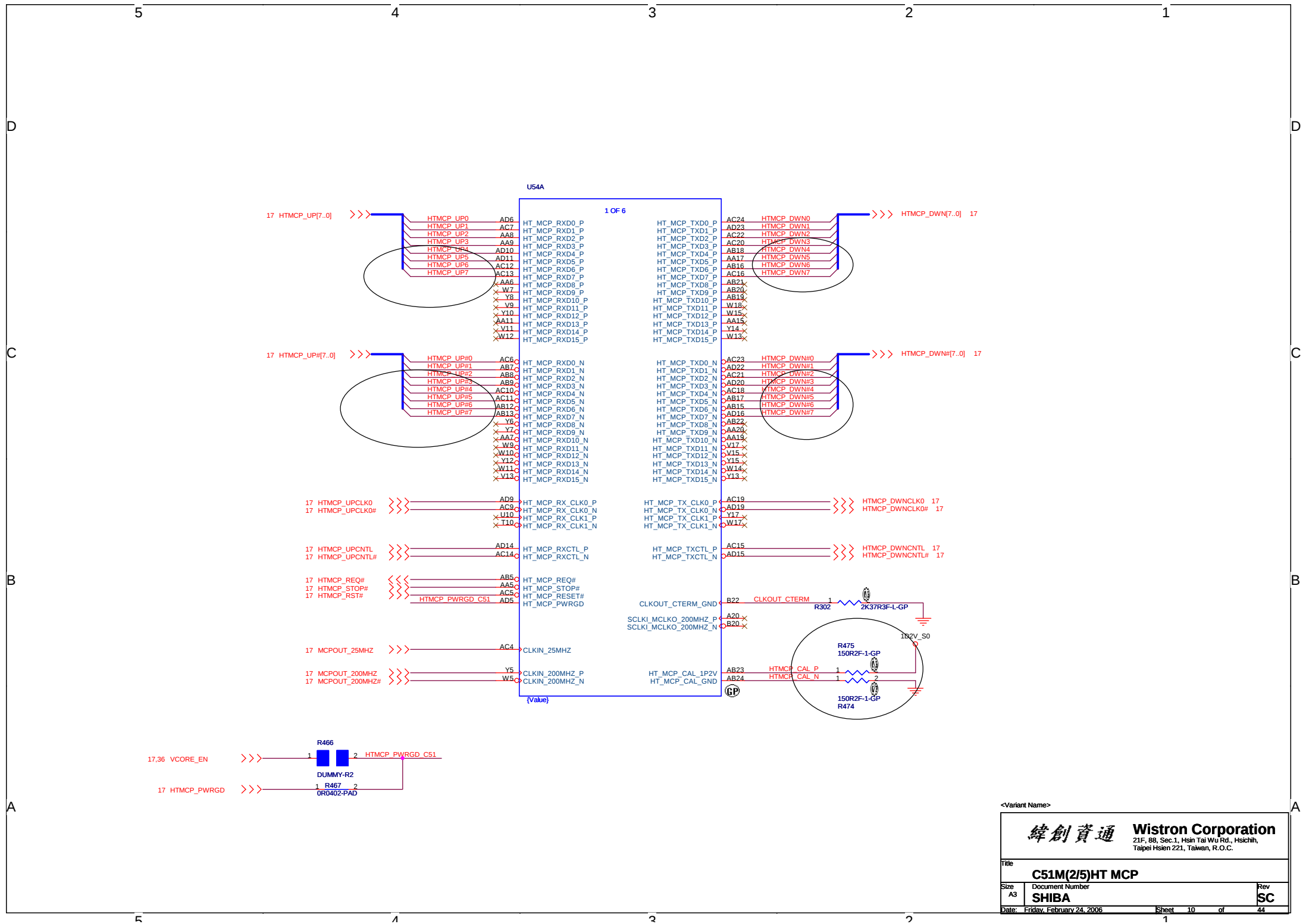
44

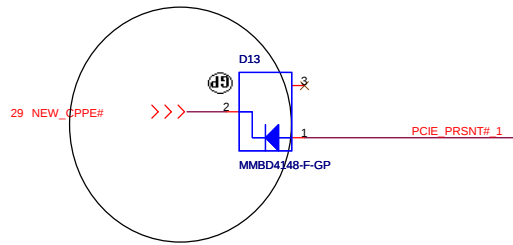


Place these Caps near PARALLEL TERMINATION

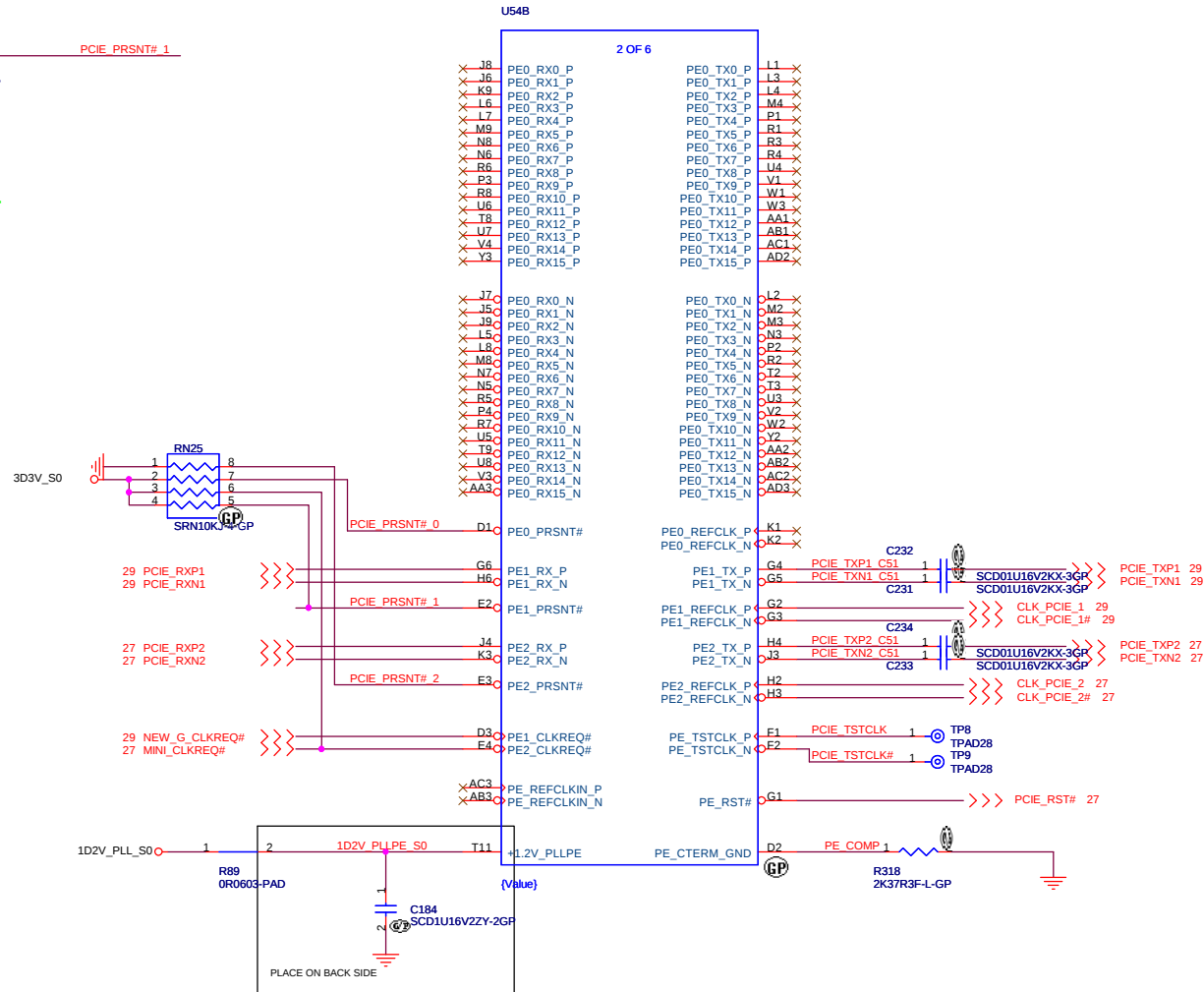
Rev
SA





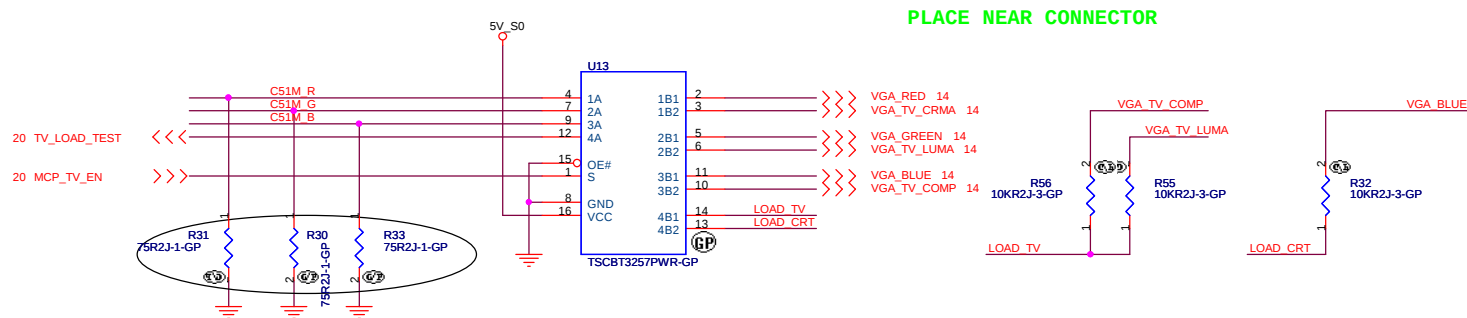
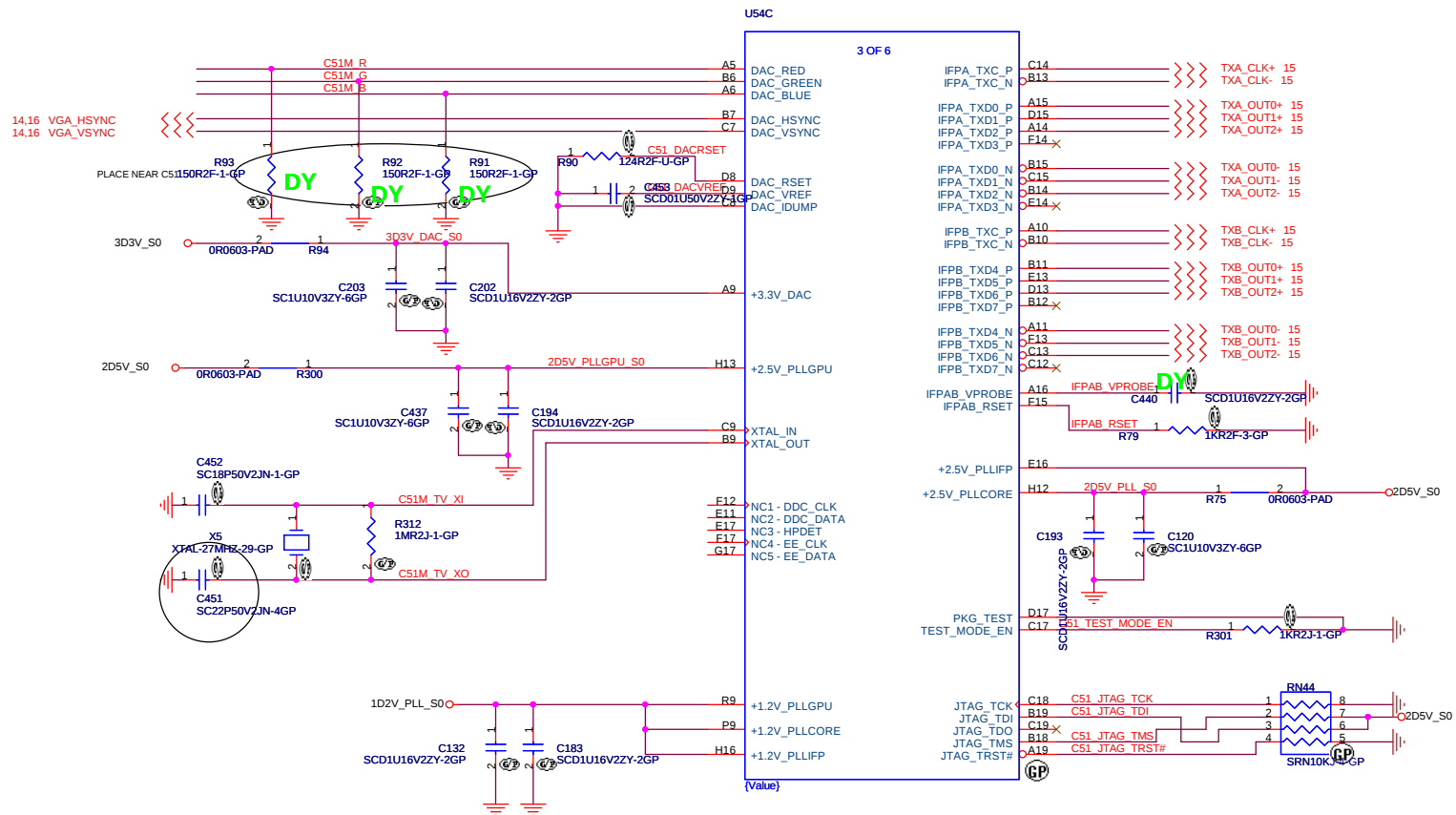


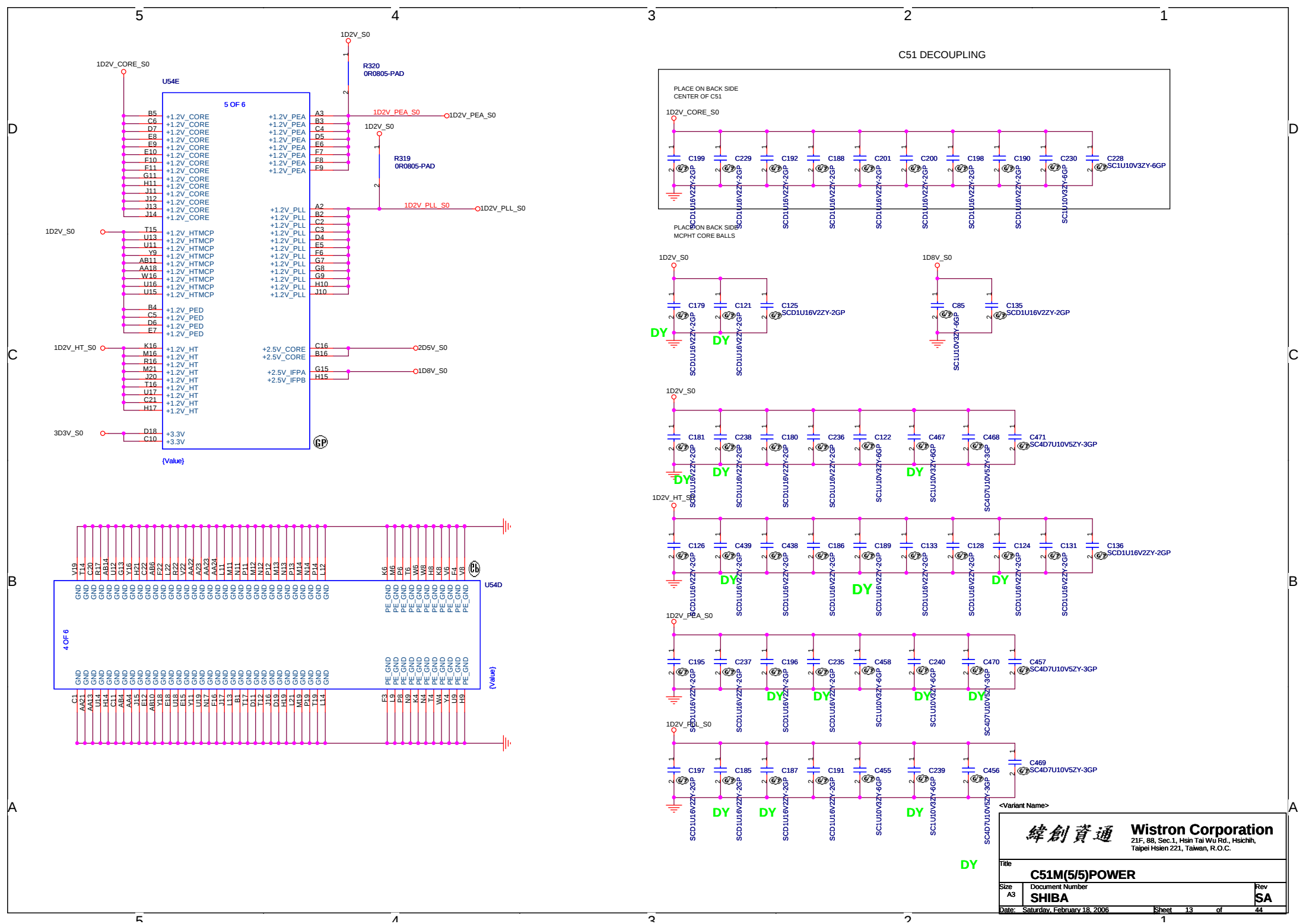
CHECK LEAKAGE CURRENT



<Variant Name>

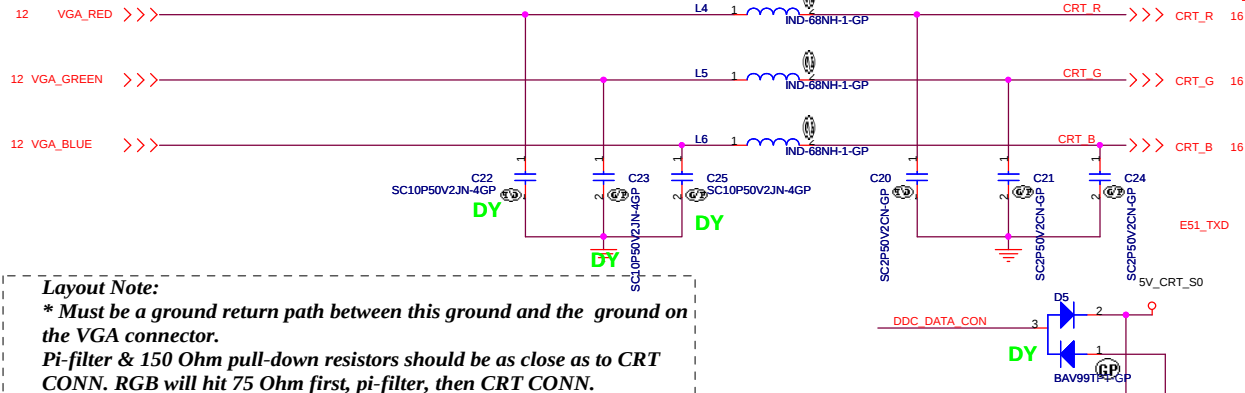
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title C51M(3/5)PCIE		
Size A3	Document Number SHIBA	Rev SA
Date: Monday, February 27, 2006 Sheet 11 of 44		



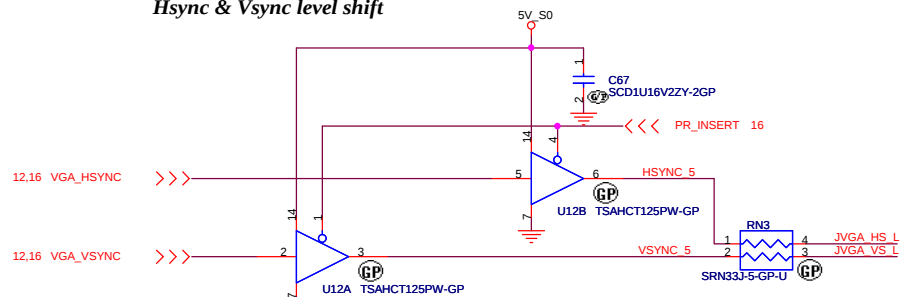


CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

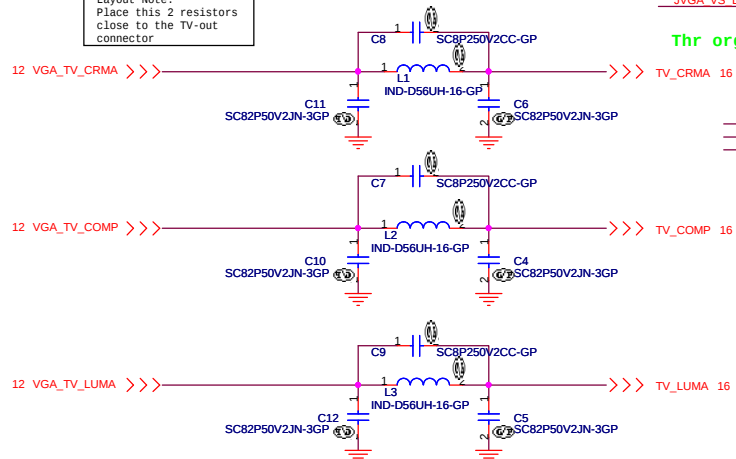


Hsync & Vsync level shift

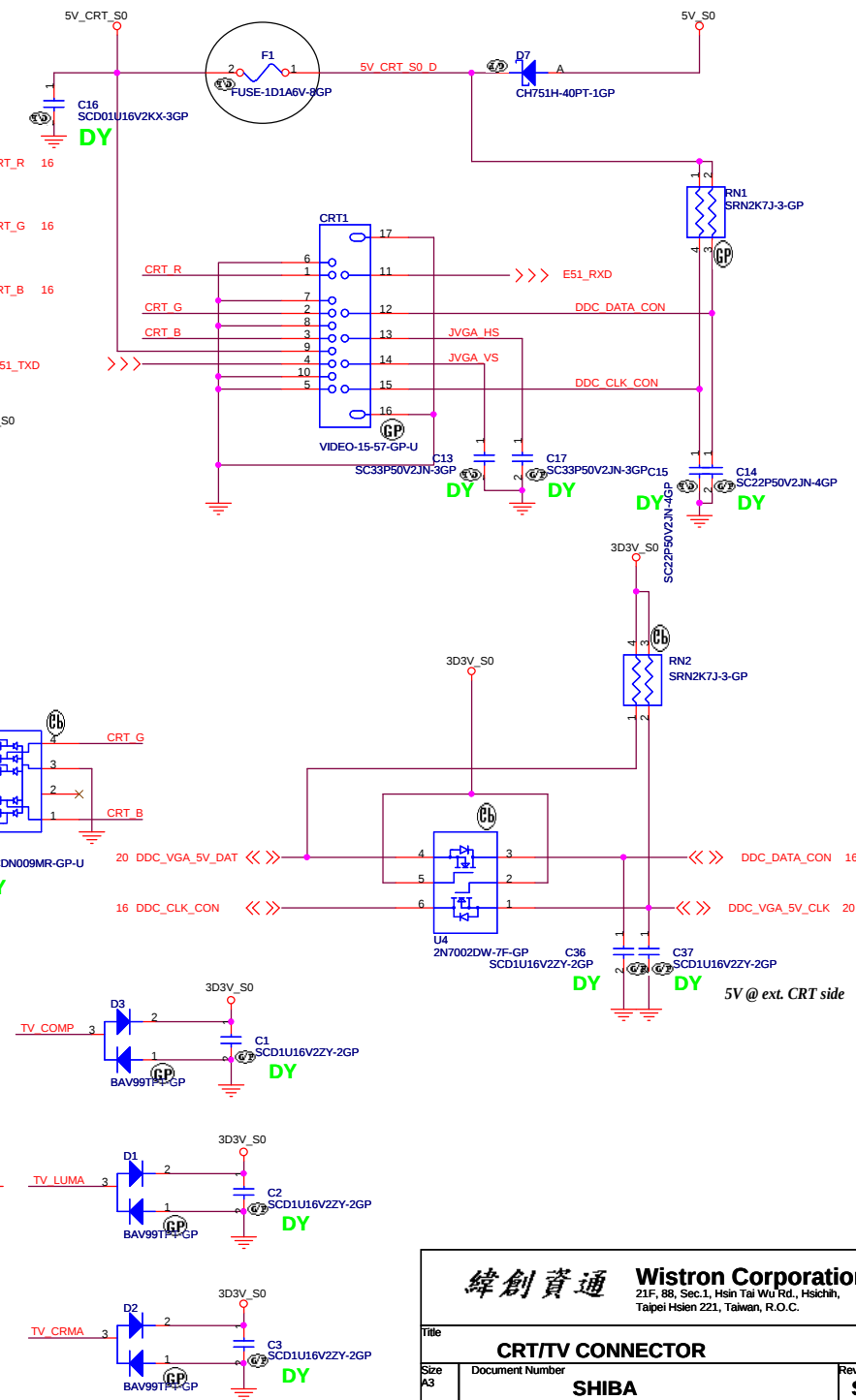
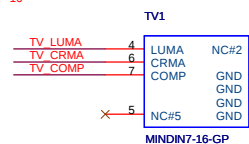


TV OUT CONN

Layout Note:
Place this 2 resistors
close to the TV-out
connector



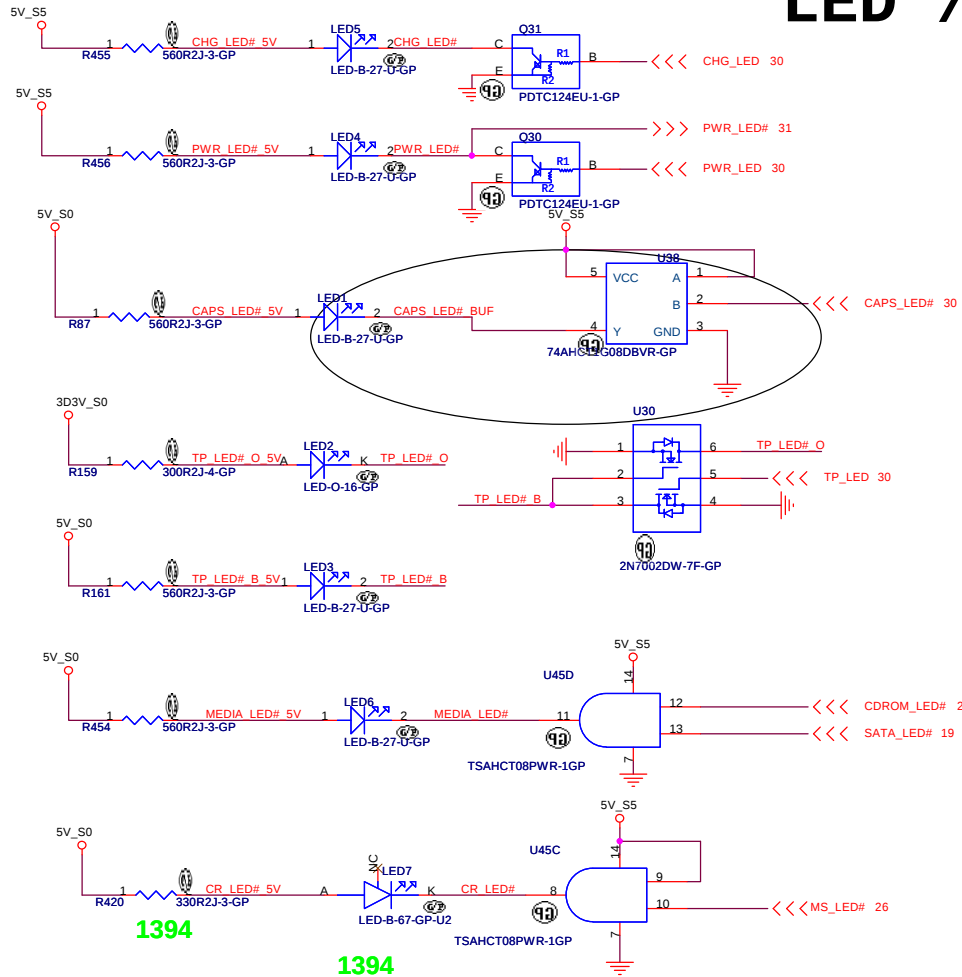
Thr org part is 68.2703N.10B



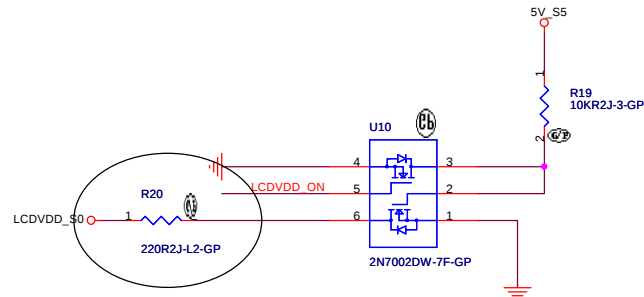
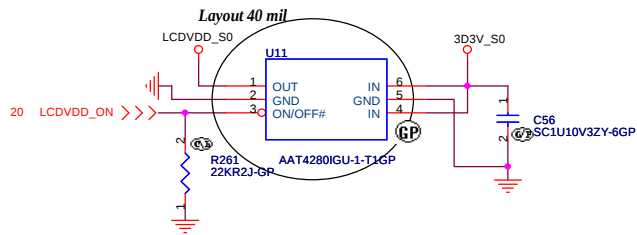
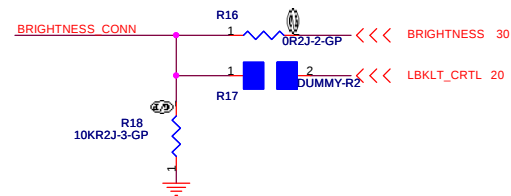
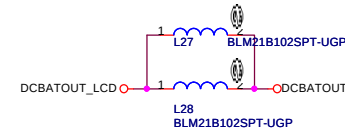
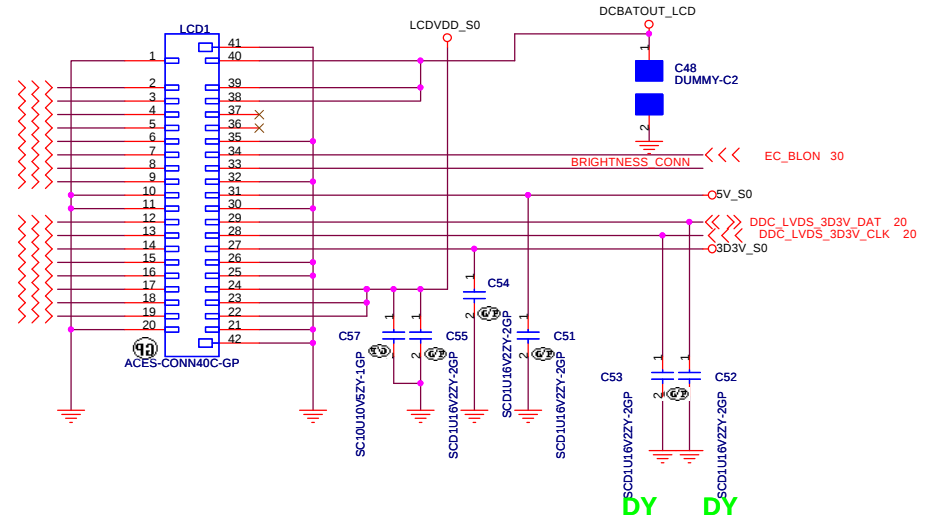
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

CRT/TV CONNECTOR		
Size A3	Document Number SHIBA	Rev SA
Date: Thursday, February 23, 2006	Sheet 14 of 44	

LED / INVERTER INTERFACE



12 TXB_OUT2+
12 TXB_OUT2-
12 TXB_OUT1+
12 TXB_OUT1-
12 TXB_OUT0+
12 TXB_OUT0-
12 TXB_CLK+
12 TXB_CLK-
12 TXA_OUT2+
12 TXA_OUT2-
12 TXA_OUT1+
12 TXA_OUT1-
12 TXA_OUT0+
12 TXA_OUT0-
12 TXA_CLK+
12 TXA_CLK-



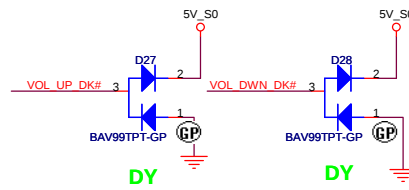
緯創資通

Wistron Corporation

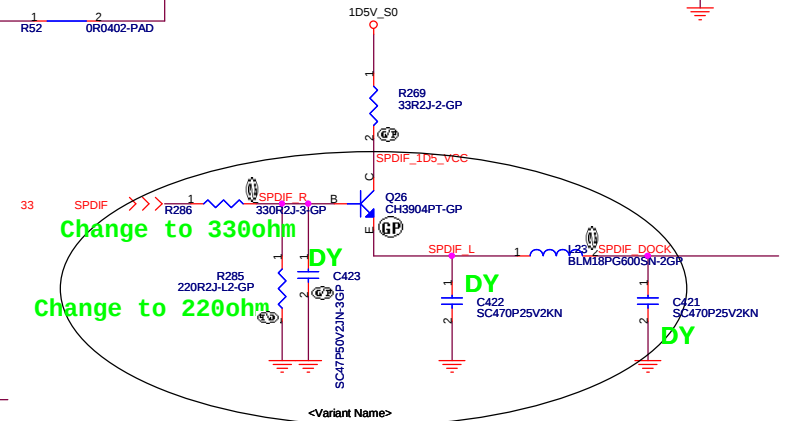
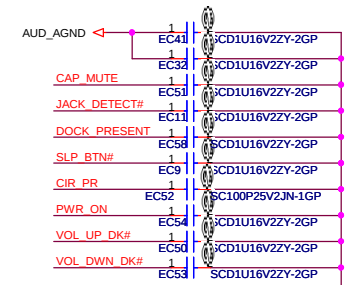
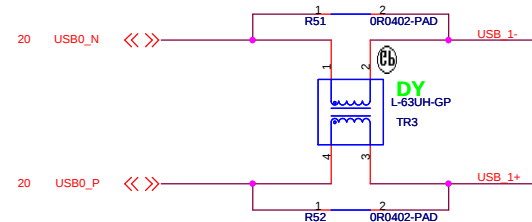
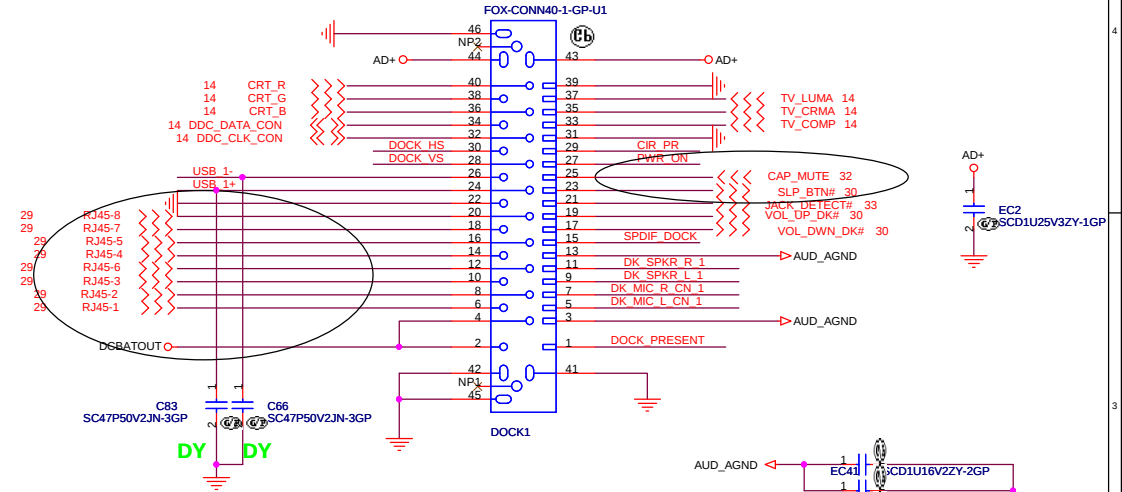
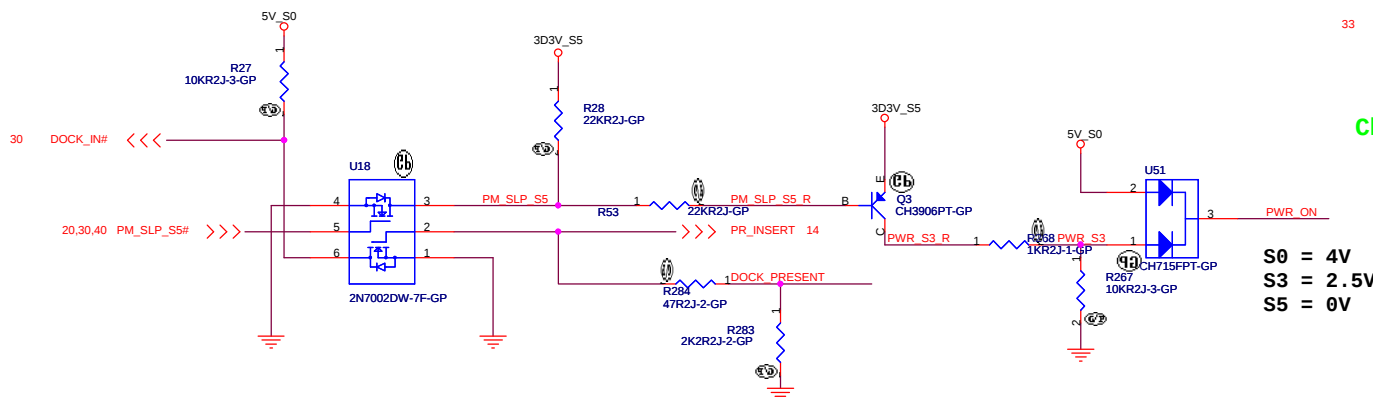
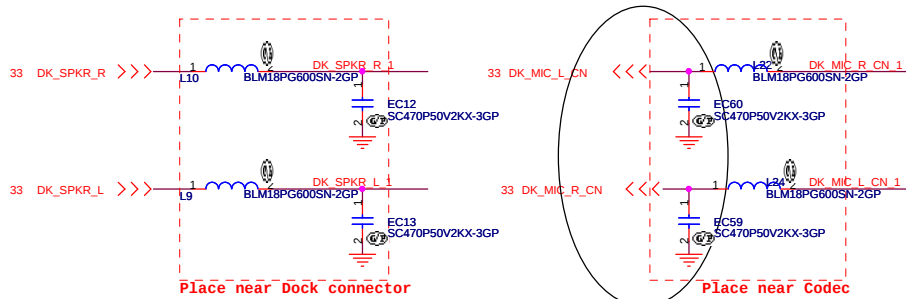
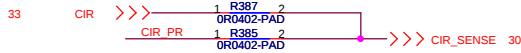
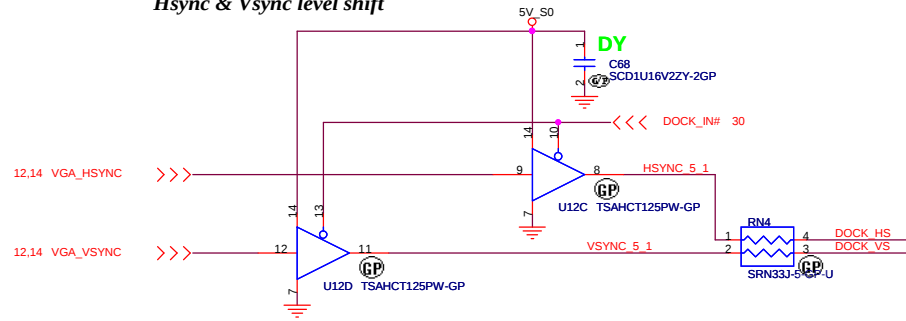
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LCD/Inverter Connector		
Size	Document Number	Rev
Custom	SHIBA	SA
Date: Friday, February 24, 2006		
Sheet 15 of 44		

Docking Connector



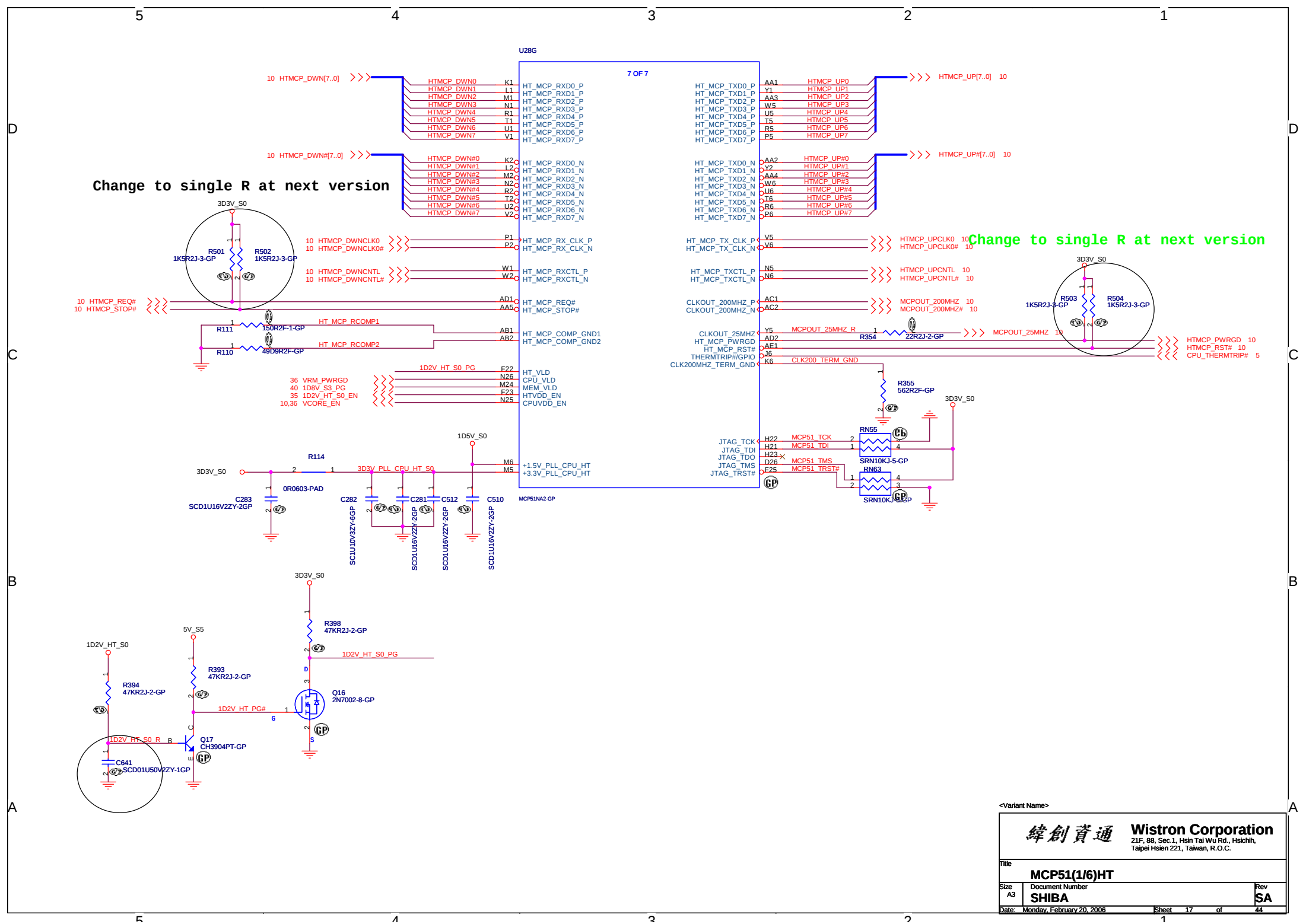
Hsync & Vsync level shift

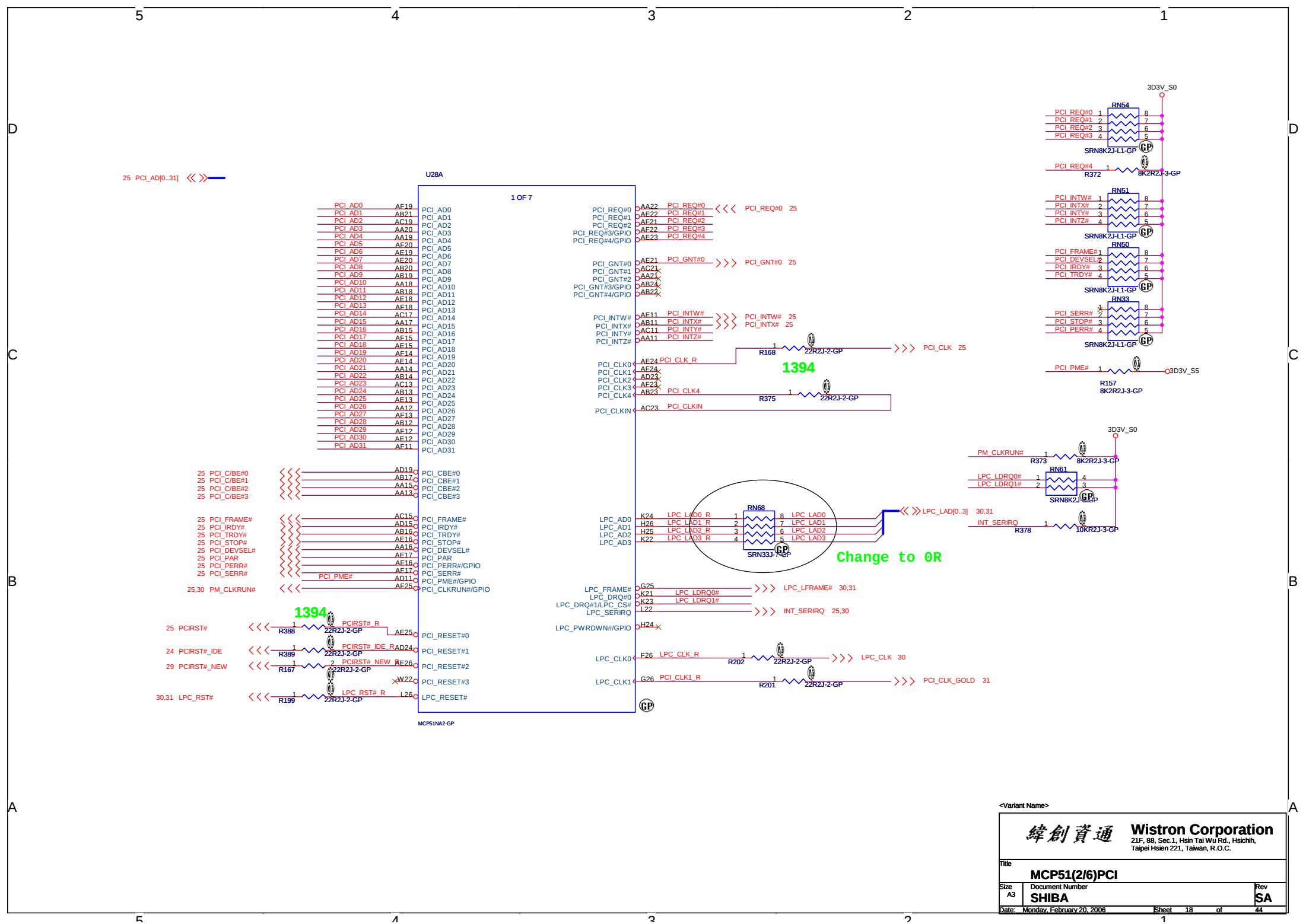


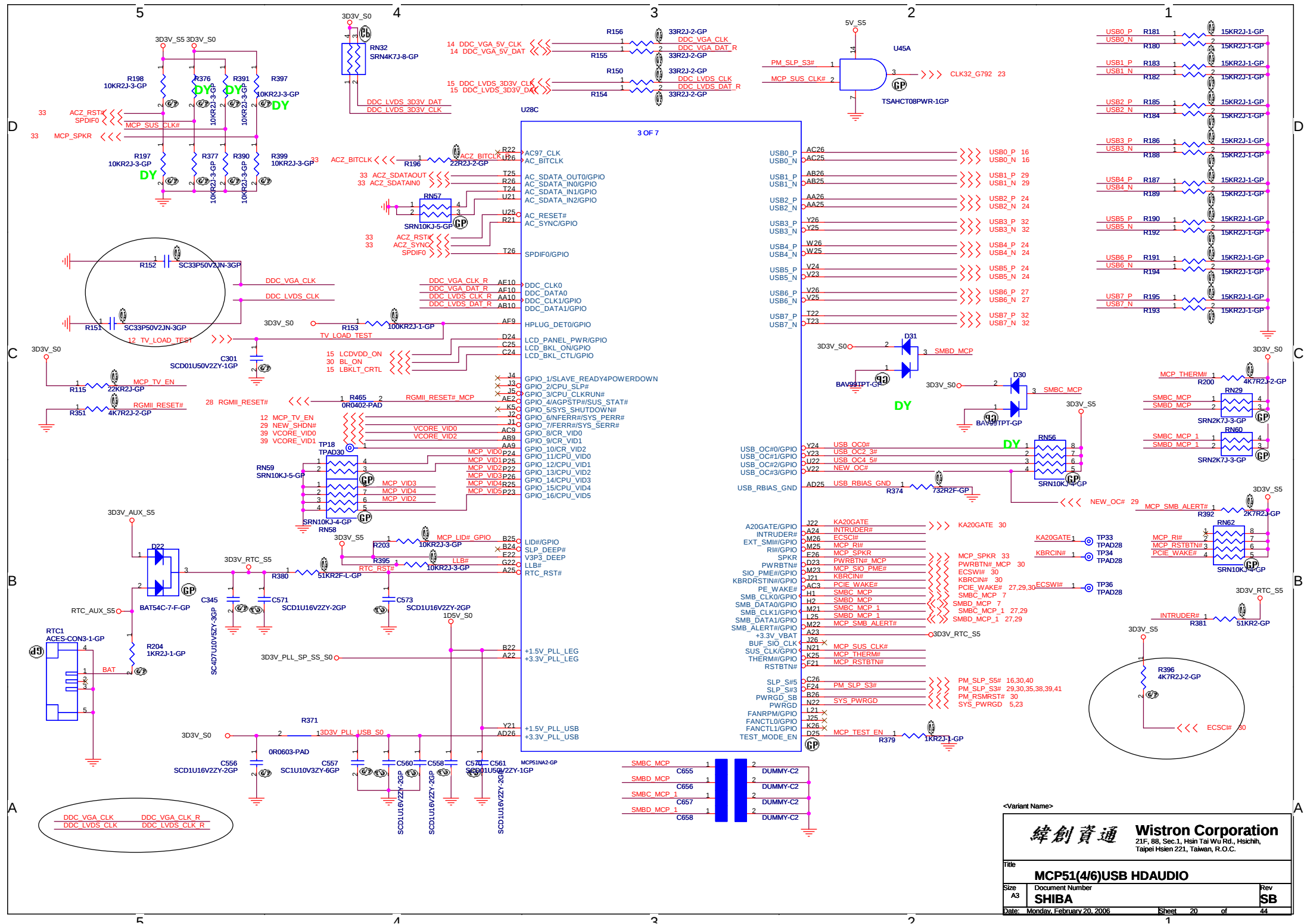
緯創資通 Wistron Corporation

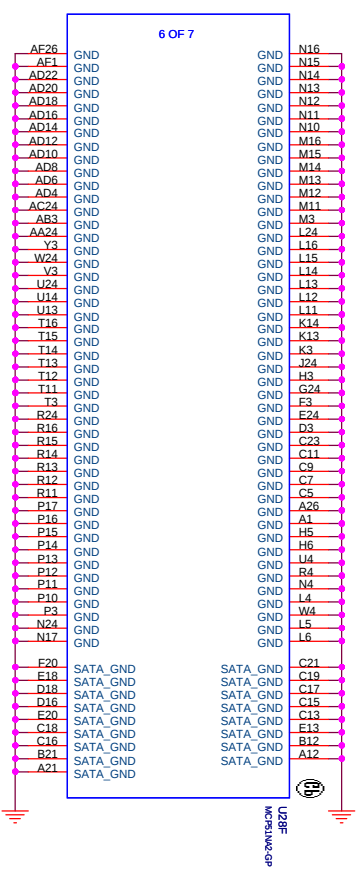
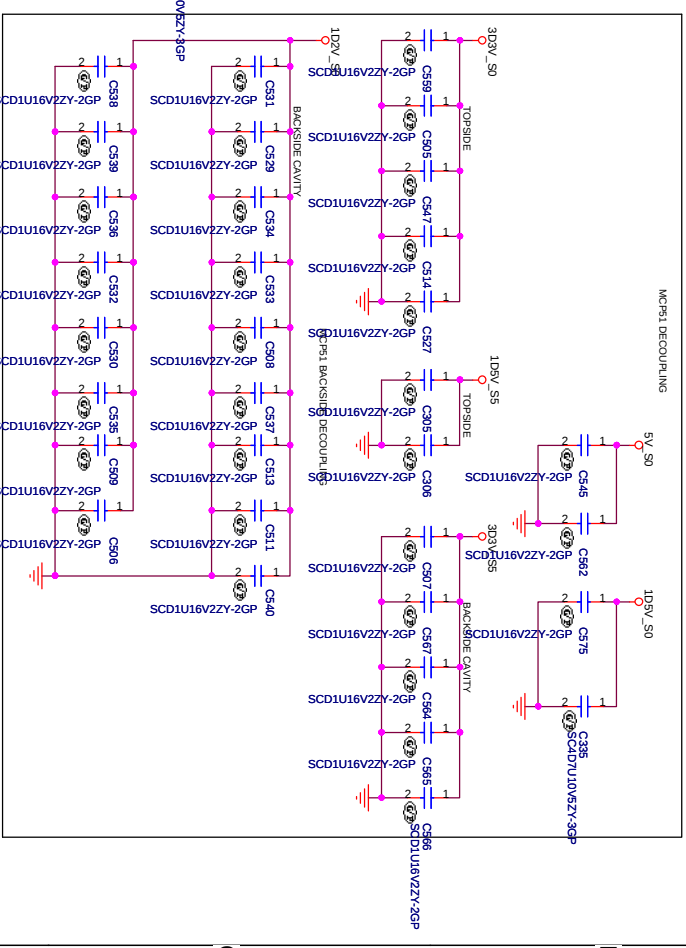
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

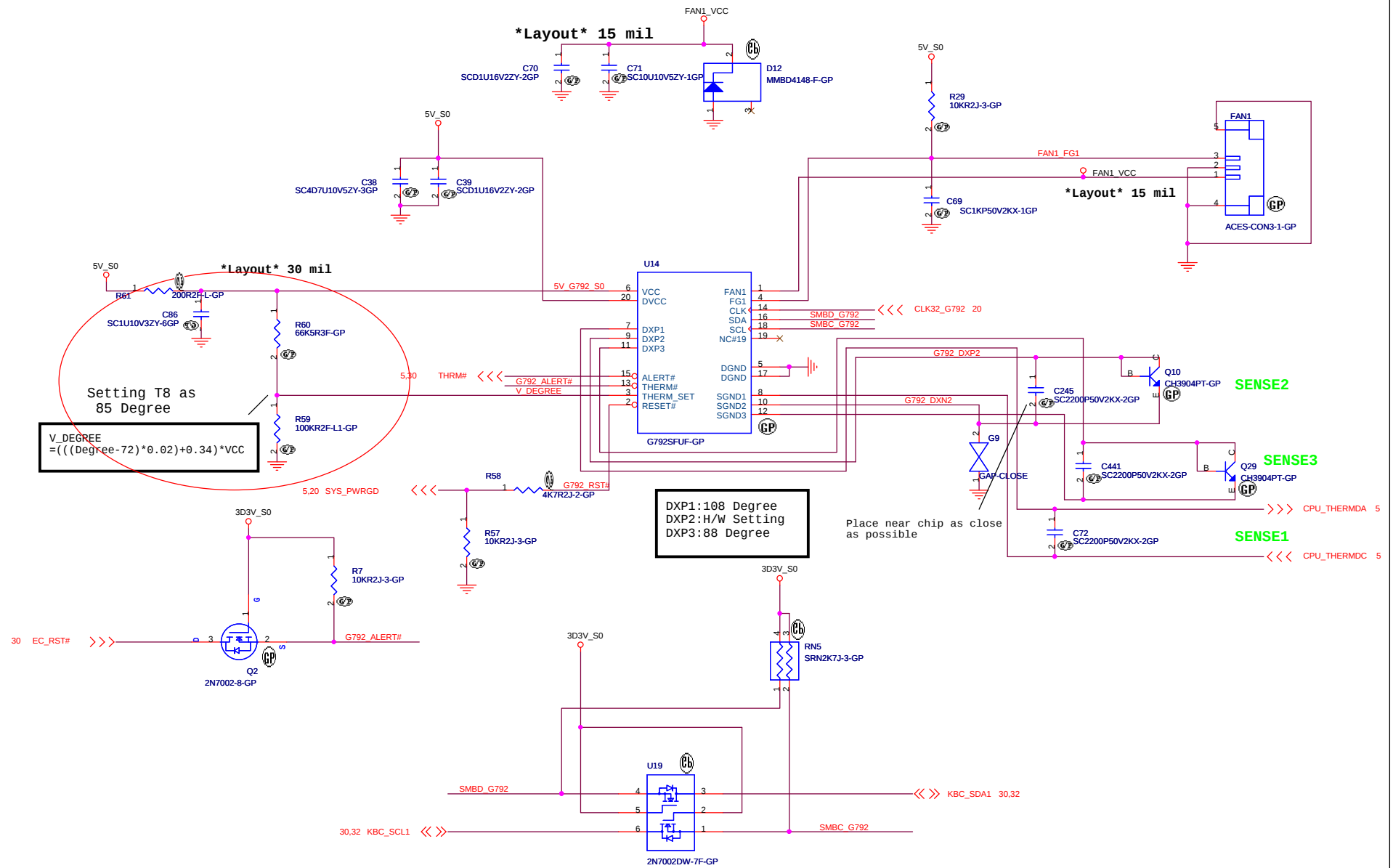
Board to board conn/ Docking			
Title	Document Number	Rev	SA
Size A3	SHIBA		
Date: Monday, February 27, 2006	Sheet 16 of 44		







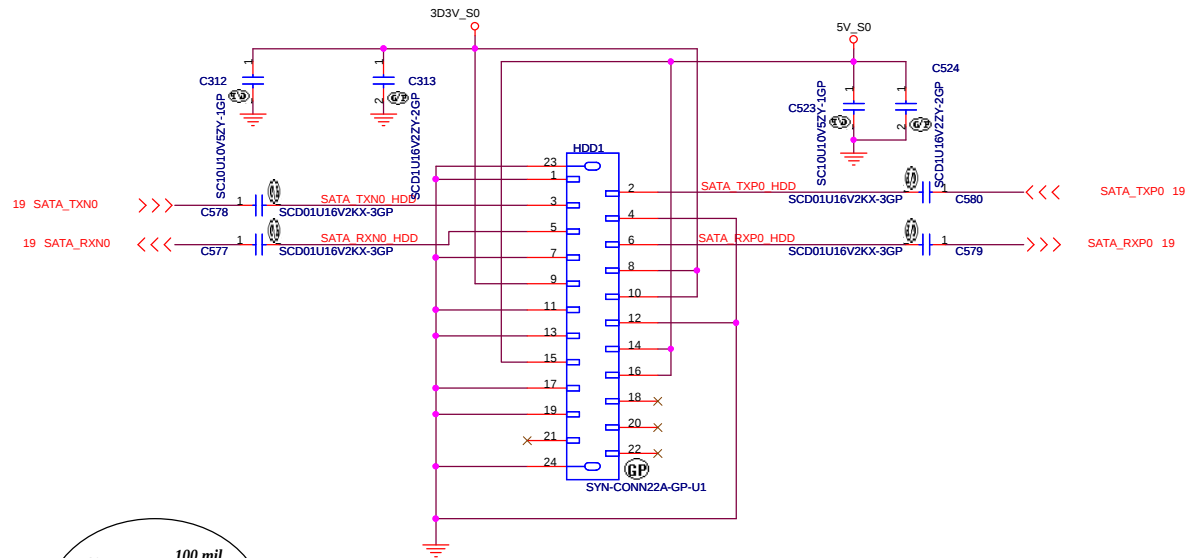




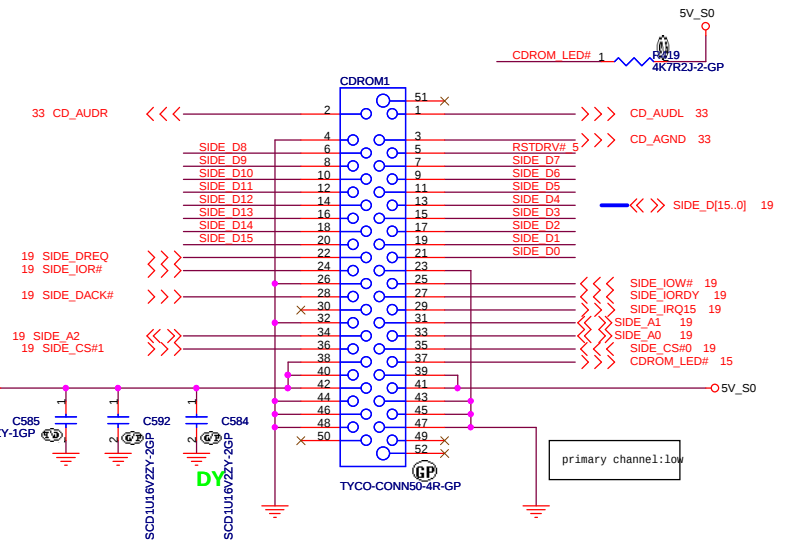
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Thermal/Fan Controller
Size	Document Number	Rev	
Custom		SA	
Date:	Monday, February 20, 2006	Sheet	23 of 44

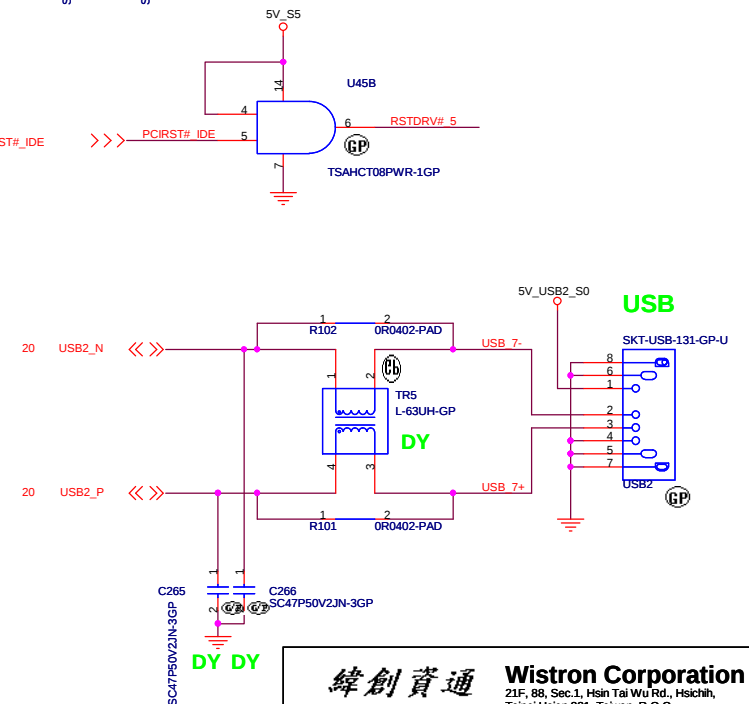
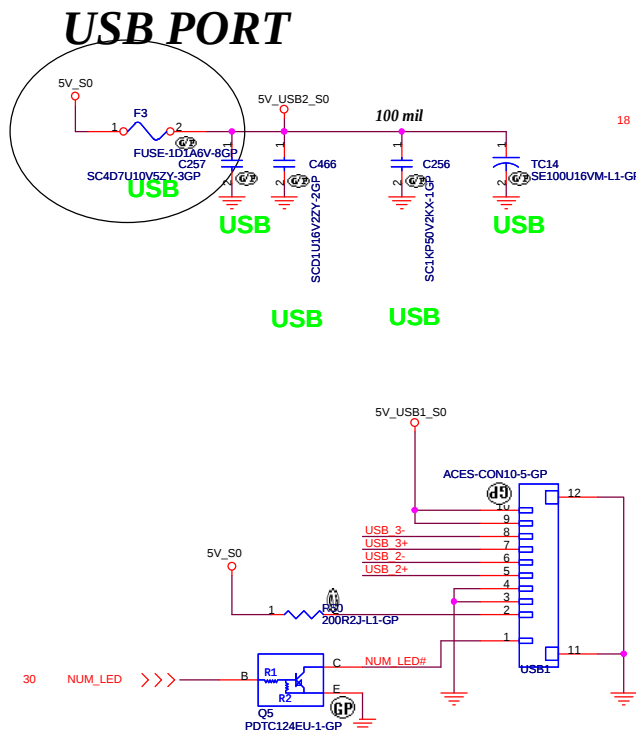
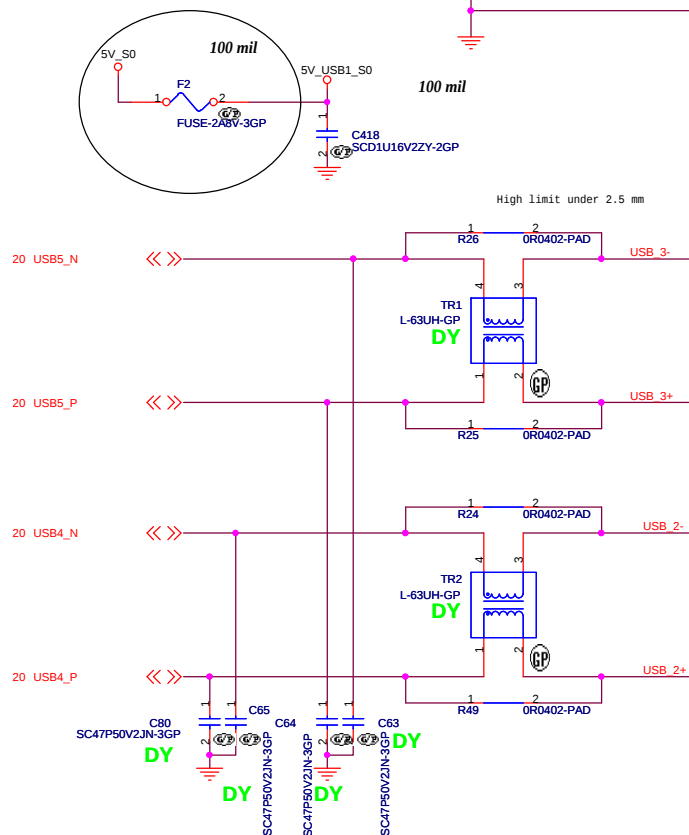
SATA HD Connector



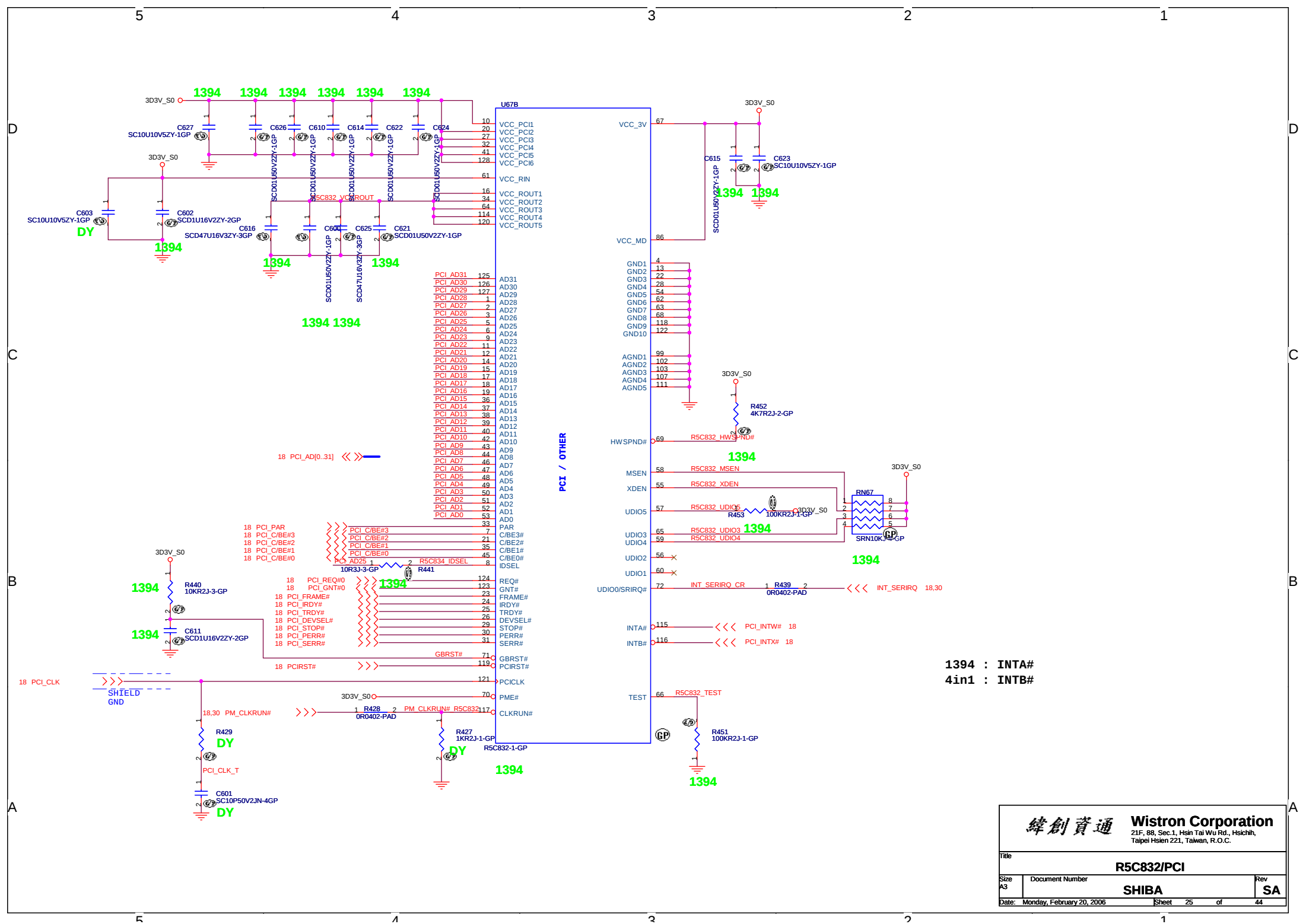
CD-ROM CONNECTOR



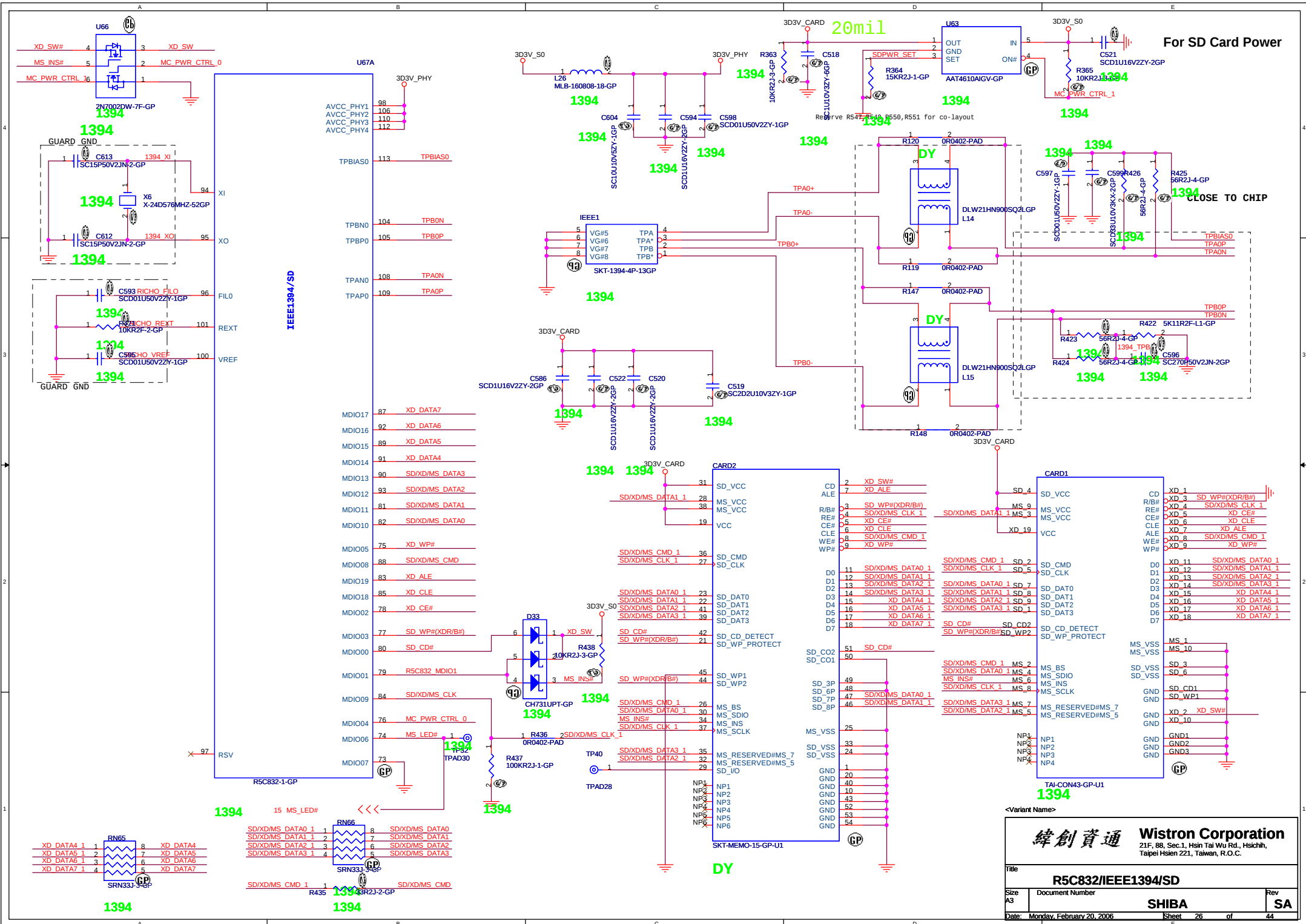
USB PORT



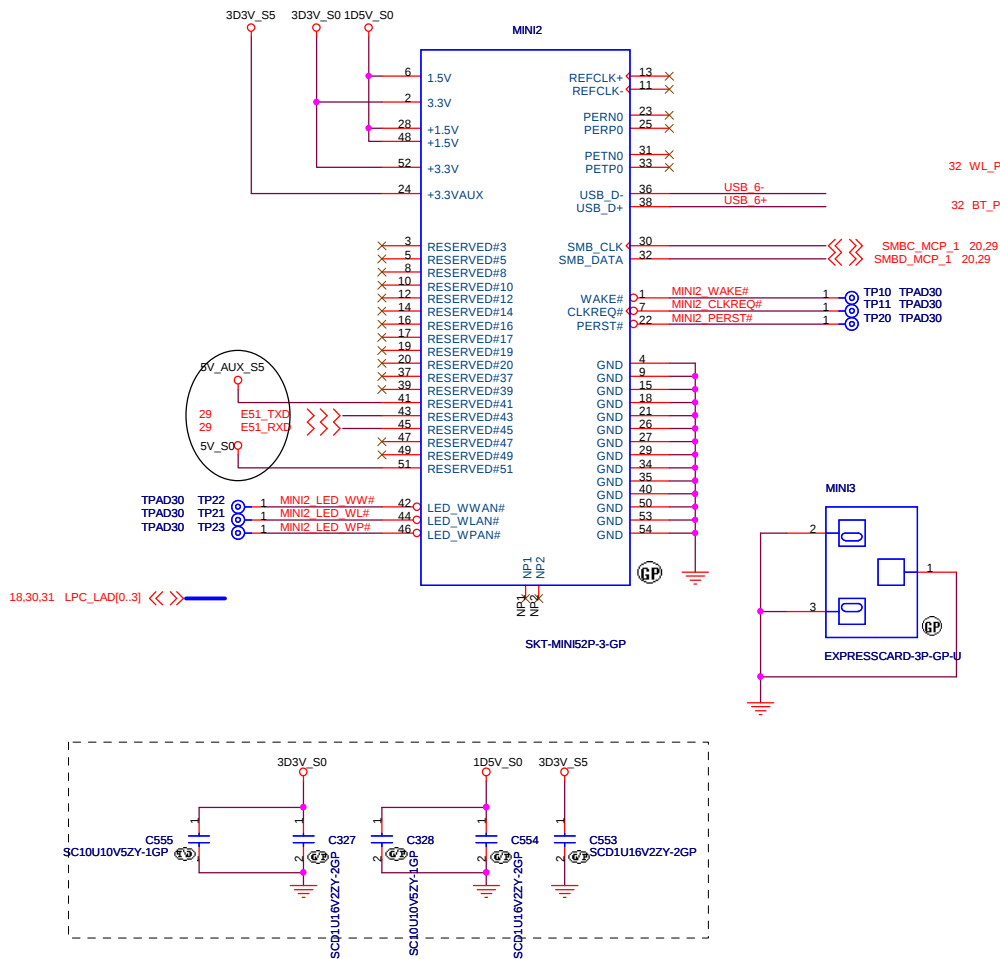
Title		HD/CDROM	
Size	Document Number	Rev	SA
A3	SHIBA		
Date:	Saturday, March 04, 2006	Sheet	24 of 44



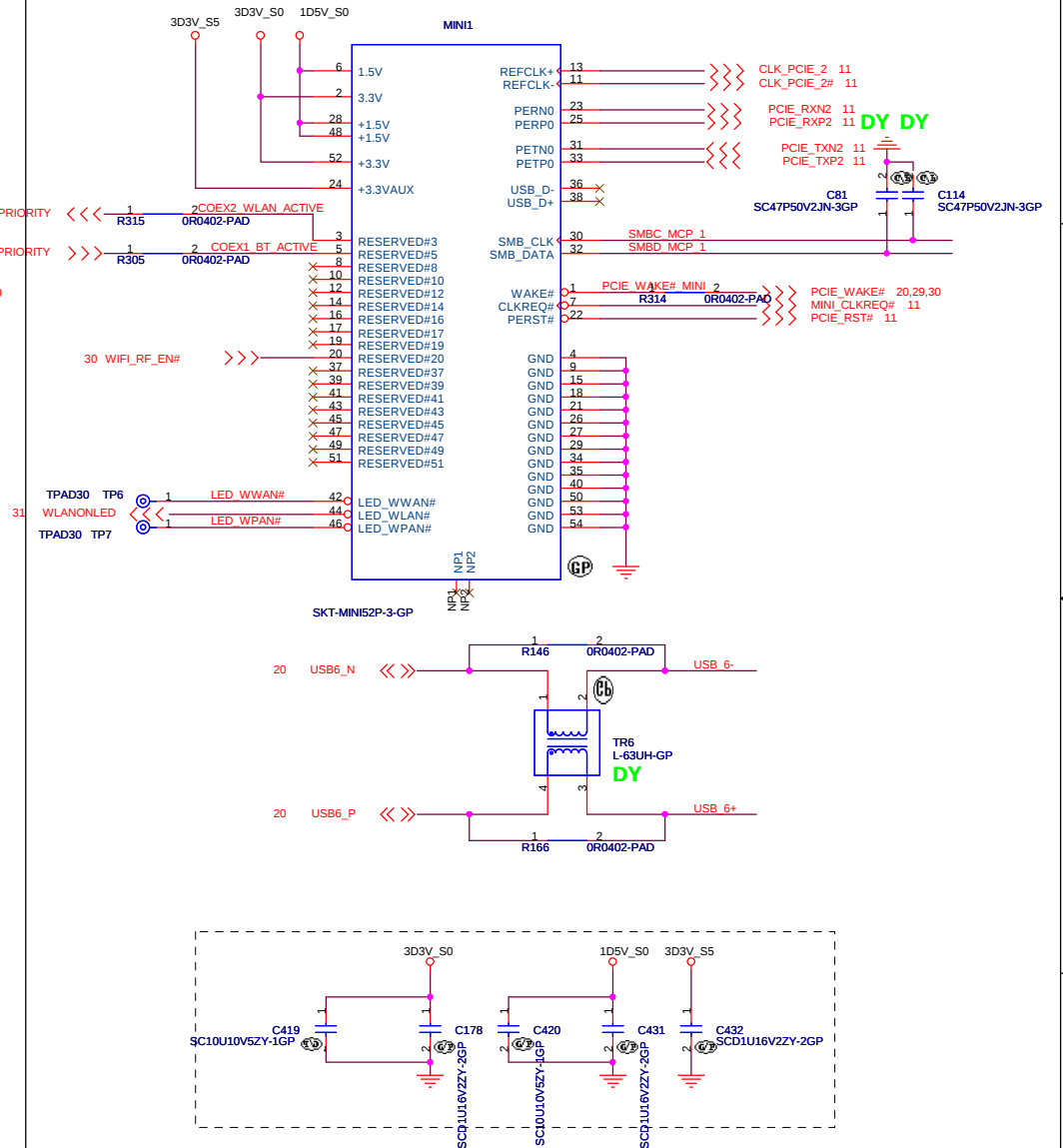
1394 : INTA#
4in1 : INTB#



Mini Card Connector 1



Mini Card Connector 2

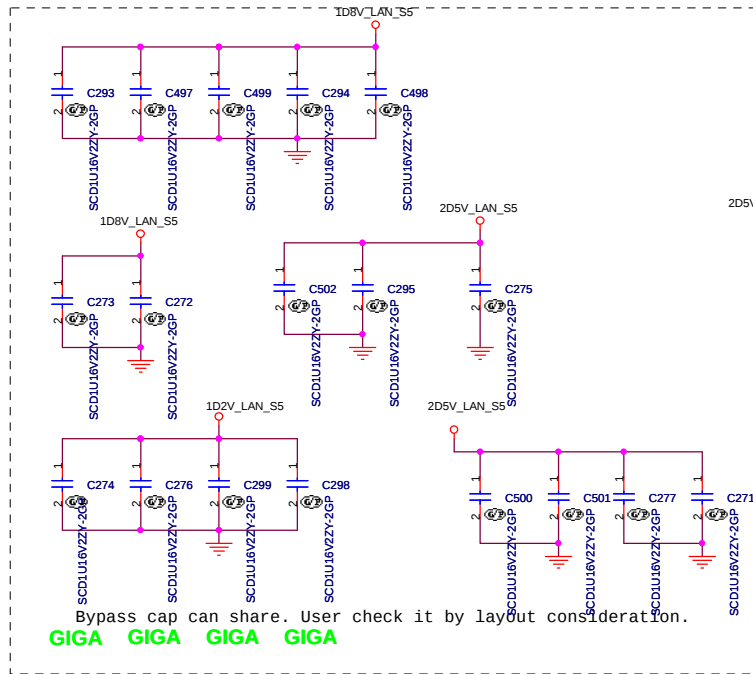
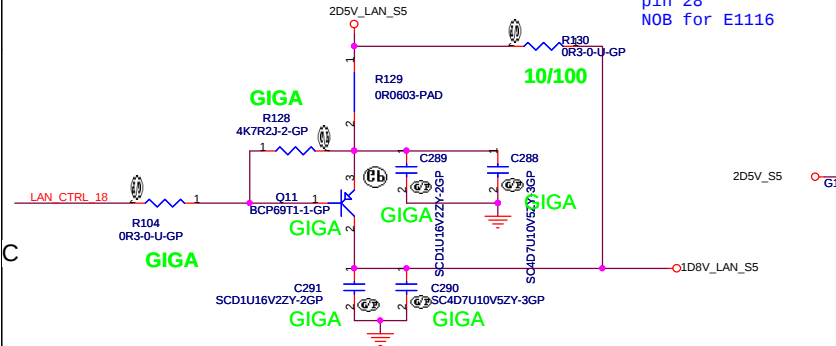


Hardware Configuration: See config_0:4

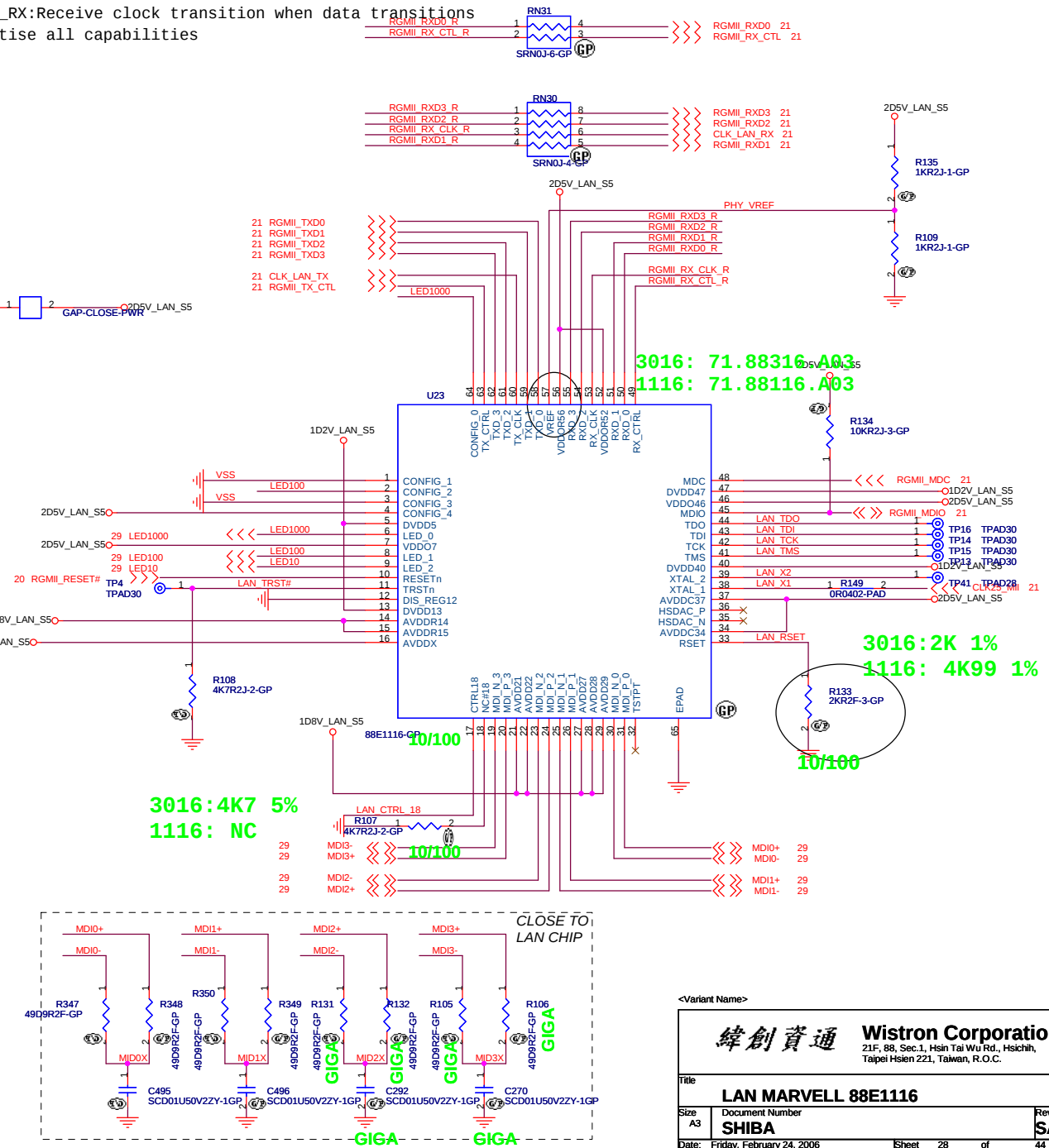
1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities

E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.

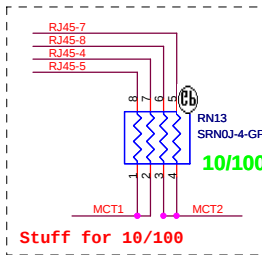
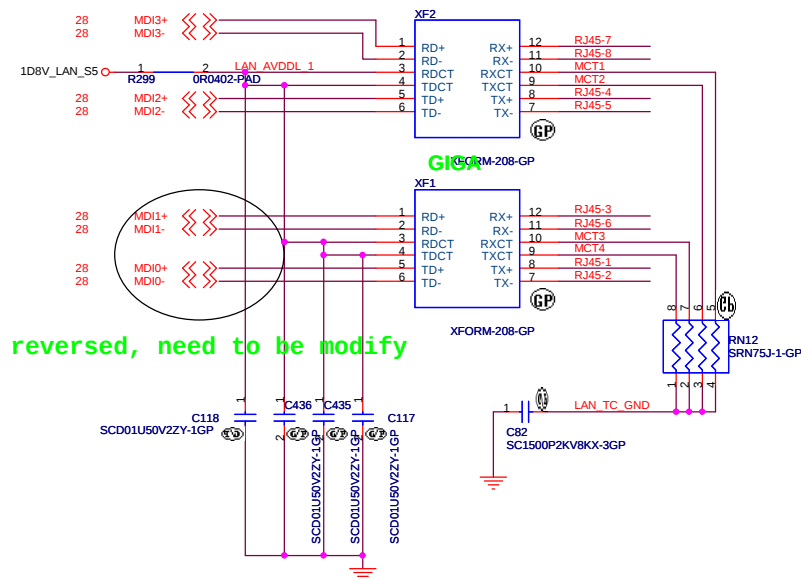
Put L10 for E3016 application since pin 28 NOB for E1116



Bypass cap can share. User check it by layout consideration.

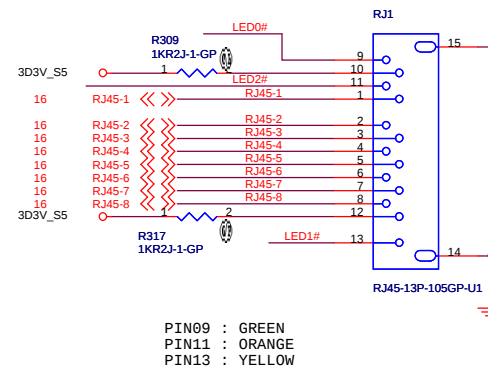


<Variant Name>		
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
LAN MARVELL 88E1116		
Size	Document Number	Rev
A3	SHIBA	SA
Date: Friday, February 24, 2006	Sheet 28 of 44	



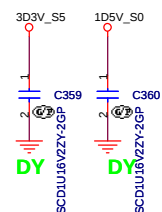
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

GREEN: LINK 10/100 Mbps
YELLOW: TX/RX ACTIVITY
ORANGE: LINK 1000Mbps

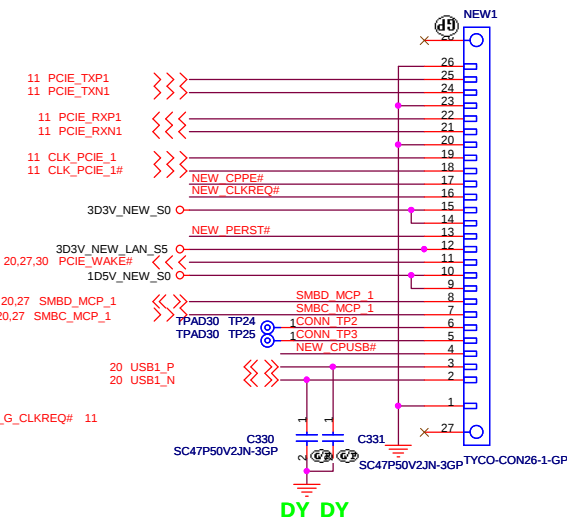
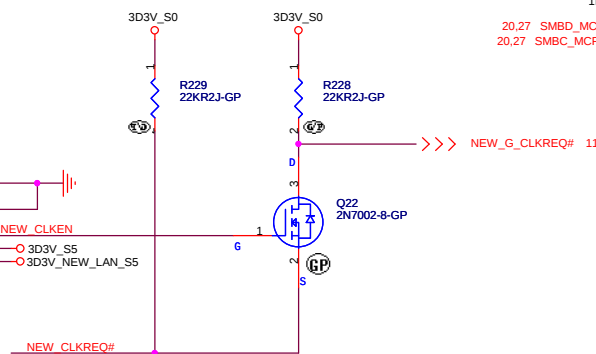
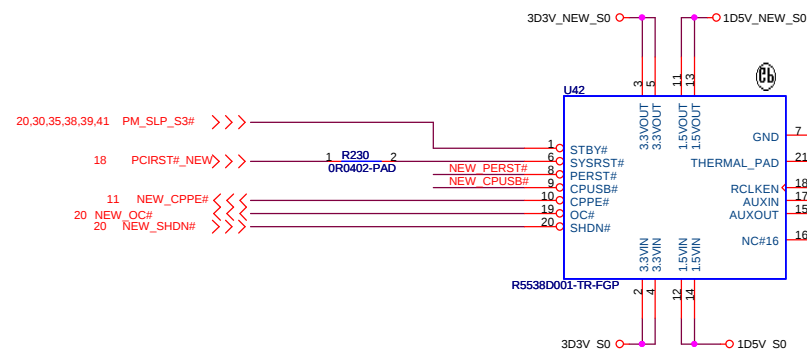
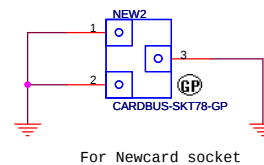
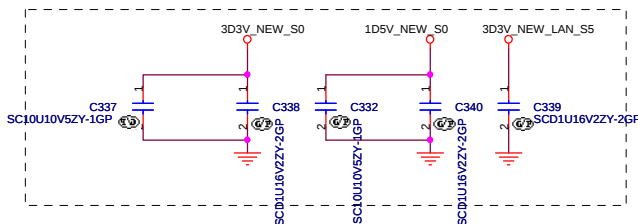


NEWCARD Connector

Place them Near to Chip



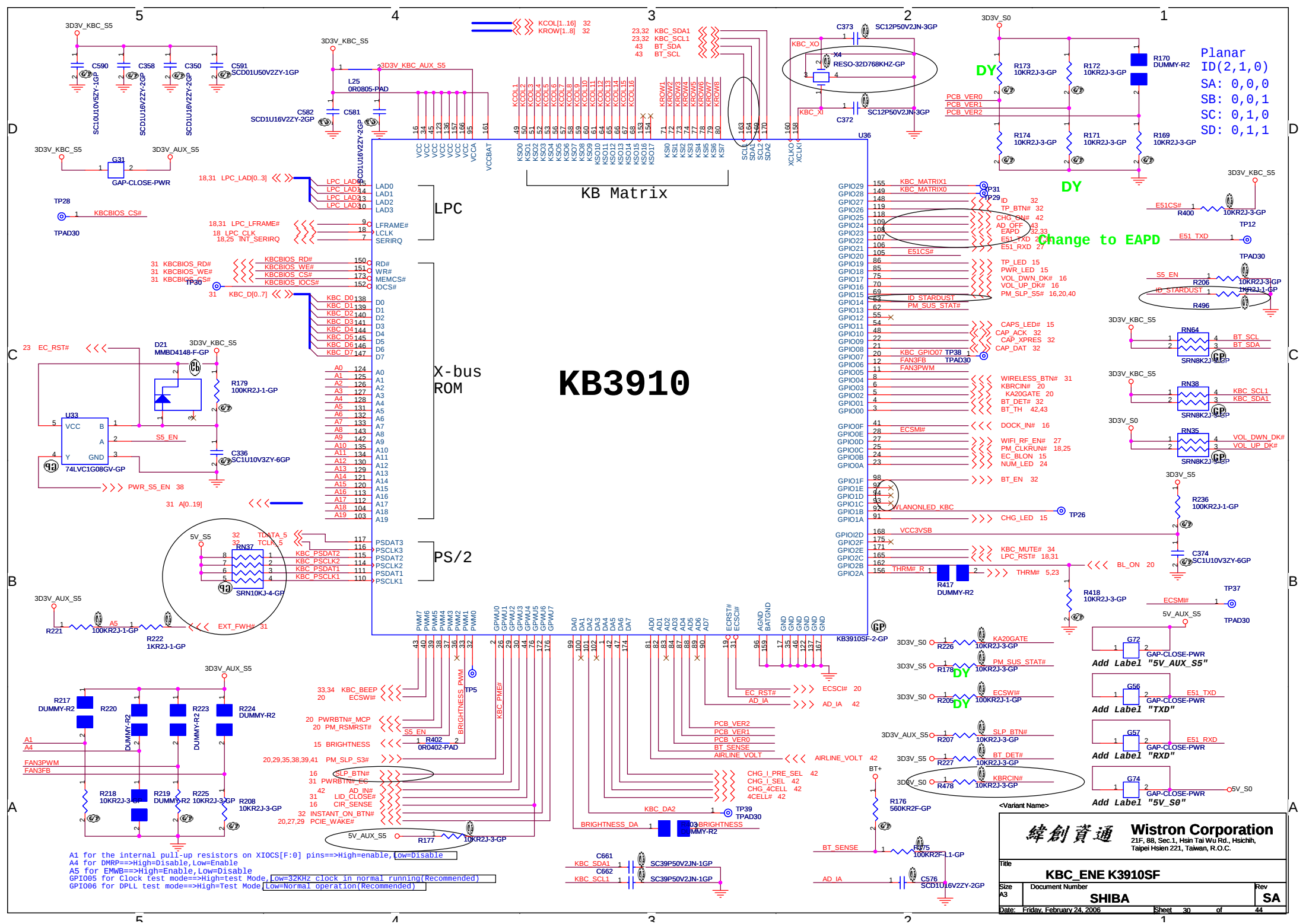
Place them Near to Connector



緯創資通

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title			New Card	
Size	Document Number	SHIBA		Rev
A3				SA
Date:	Monday, February 20, 2006	Sheet	29	of 44



Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1

KB Matrix

KB3910

X-bus
ROM

PS/2

Change to EAPD

緯創資通

Wistron Corporation

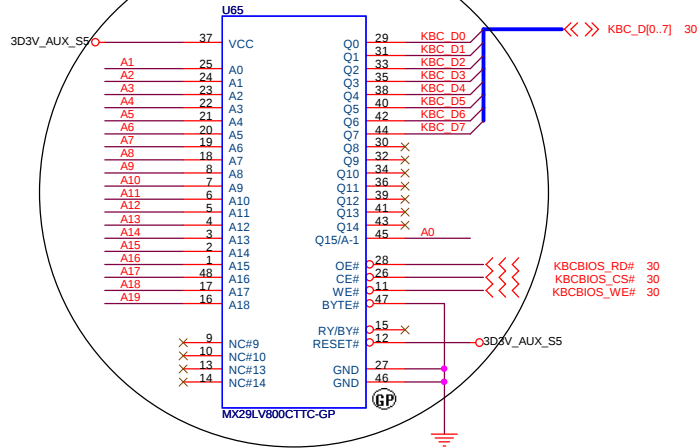
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			KBC_ENE K3910SF		
Size	Document Number				Rev
A3	SHIBA				SA
Date:	Friday, February 24, 2006	Sheet	30	of	44

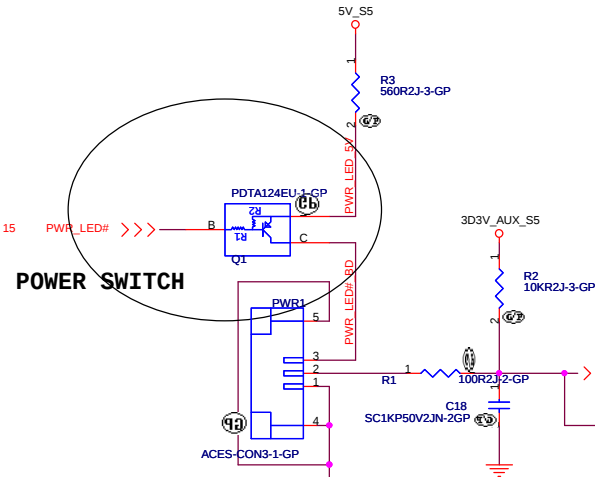
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable, Low=Disable
A4 for DMRP==>High=Disable, Low=Enable
A5 for EMWB==>High=Enable, Low=Disable
GP1085 for clock test mode==>High=Test Mode, Low=32KHz clock in normal running(Recommended)
GP1086 for DPLL test mode==>High=Test Mode(Low=Normal operation)(Recommended)

30 A[0..19]

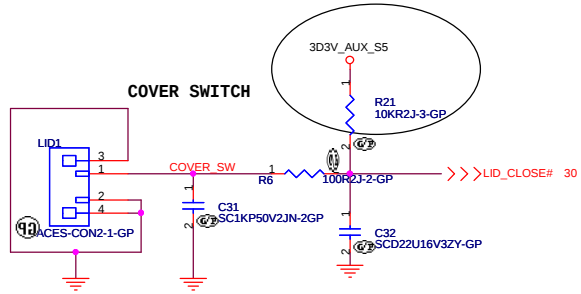
>>>



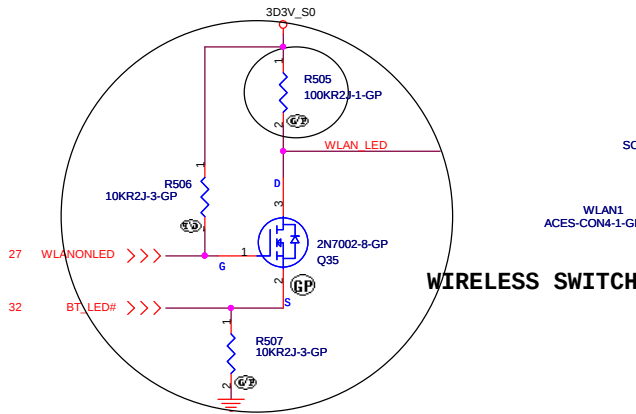
Change to MX29LV800CTTC
72.29800.0B9



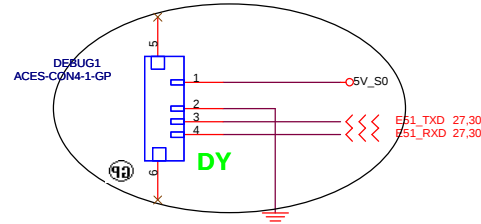
POWER SWITCH



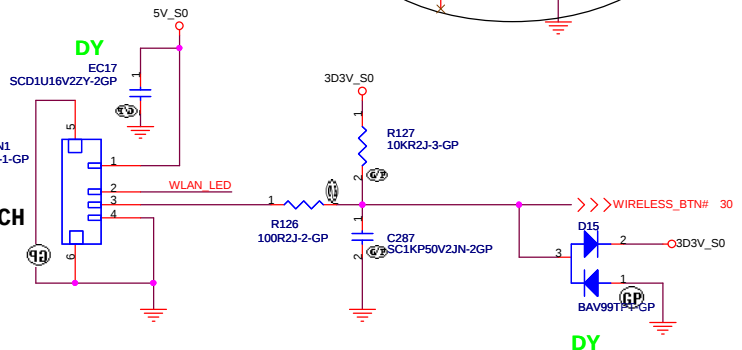
COVER SWITCH



WIRELESS SWITCH

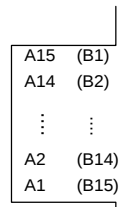


DY



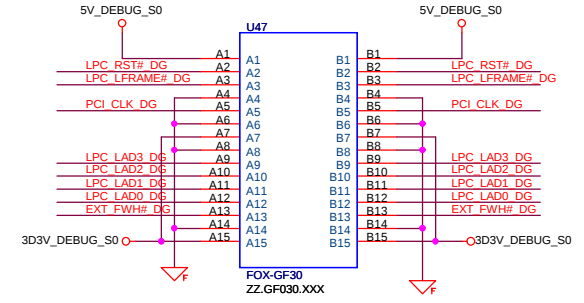
DY

TOP VIEW



(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD



>>> LPC_LAD[0..3] 18,30

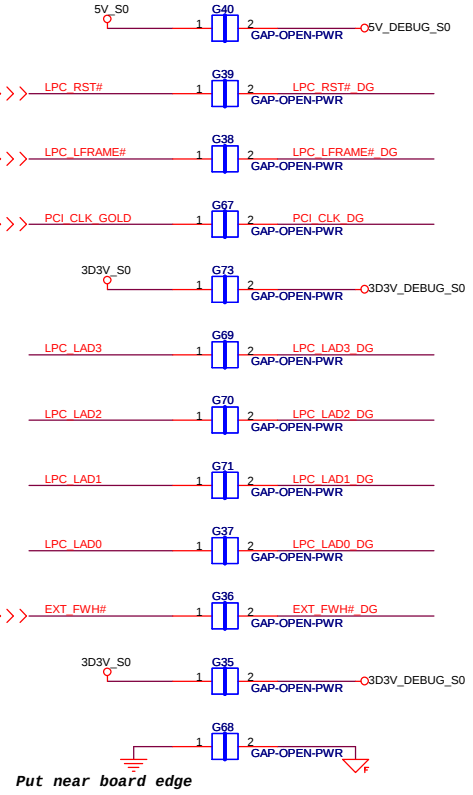
18,30 LPC_RST#

18,30 LPC_LFRAME#

18 PCI_CLK_GOLD

DY

30 EXT_FWH#



Put near board edge

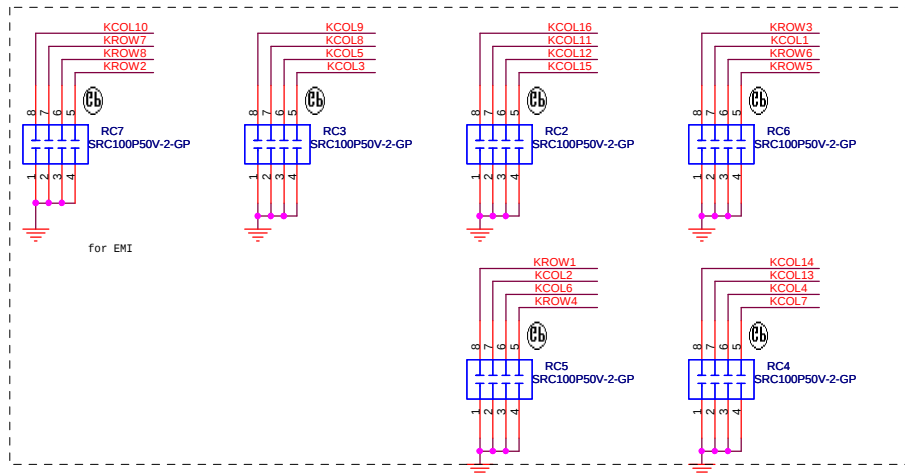
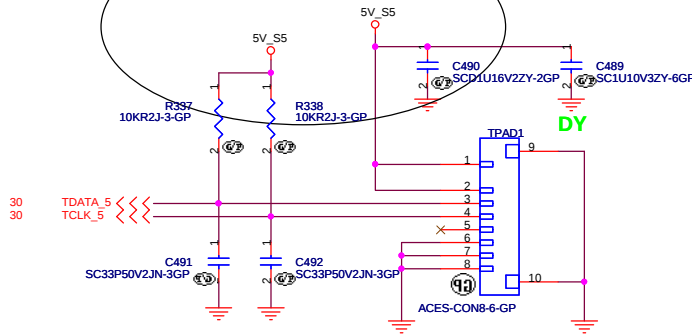
Internal KeyBoard Connector

30 KROW[1..8] <<< <<< <<<
30 KCOL[1..16] <<< <<< <<<

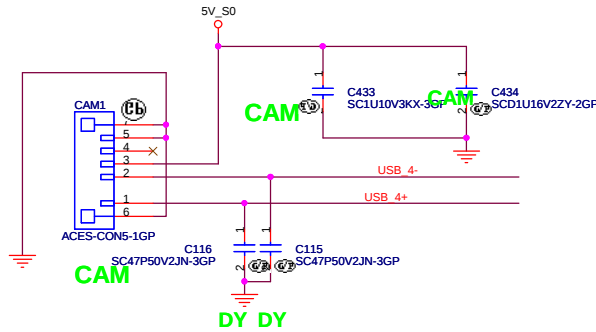
Keyboard matrix (from vendor)

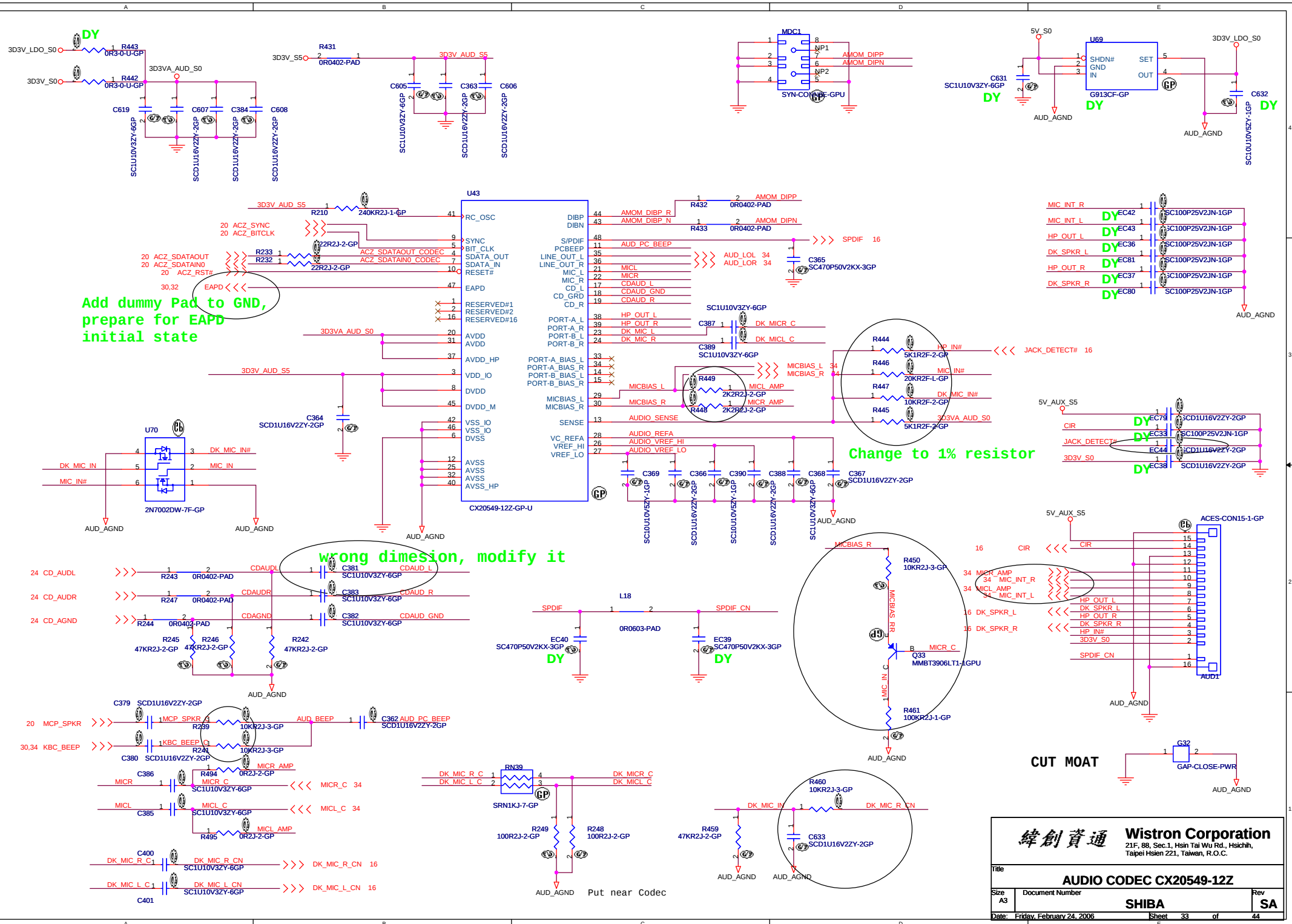
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

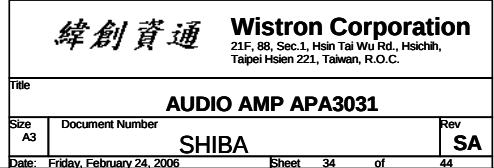
TouchPad Connector



CAMERA



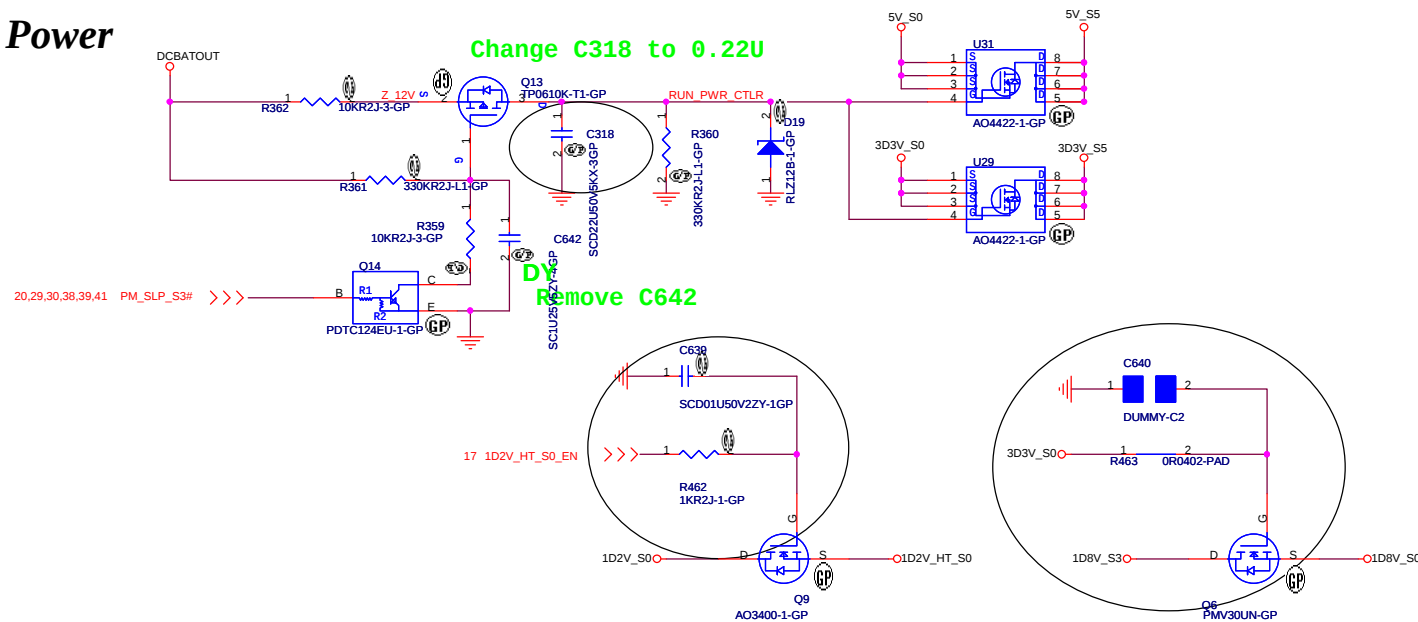




Suspend Power

Remove Dummy PAD

Run Power

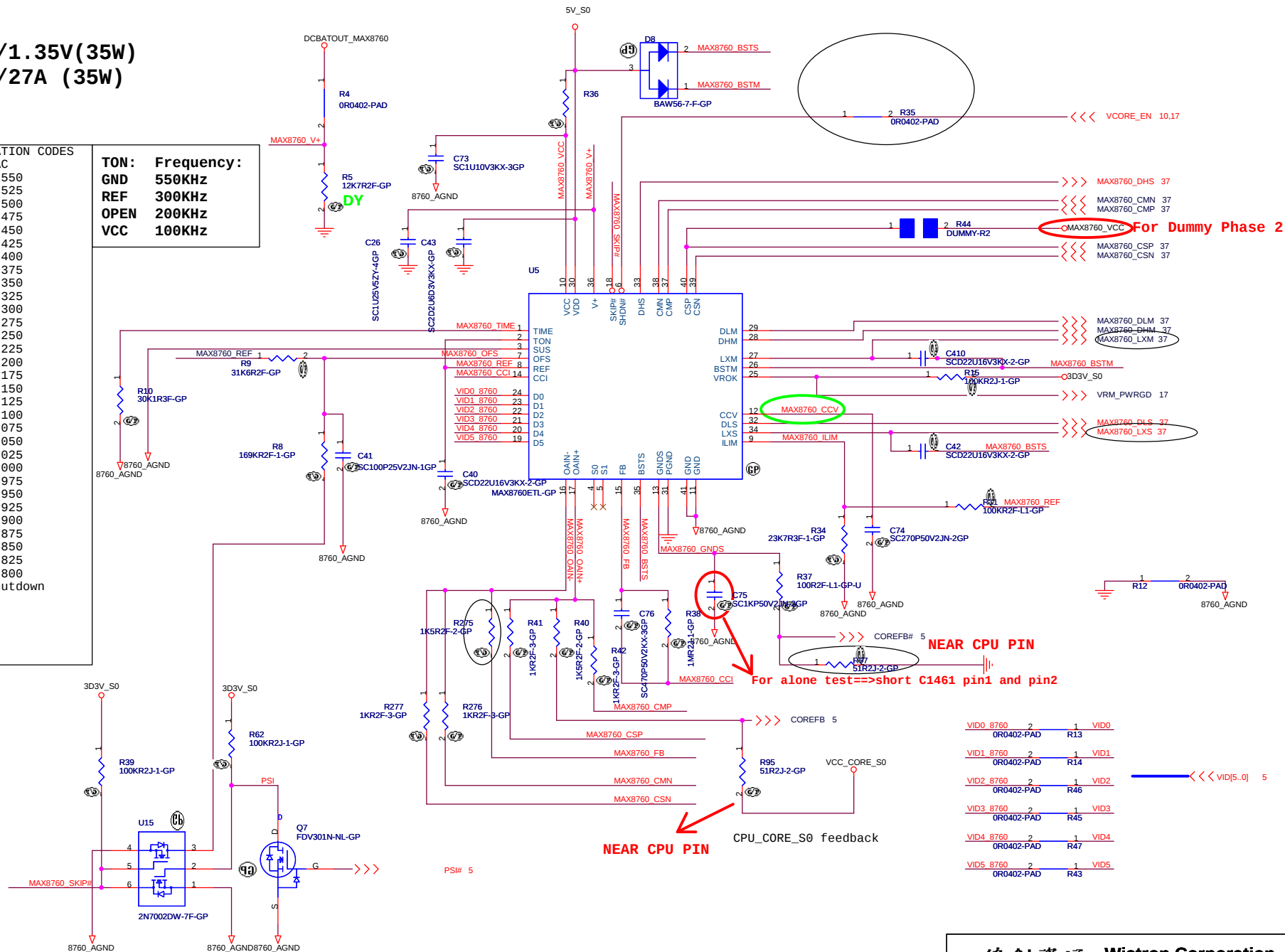


CPU_VCORE
VID=1.20V(25W)/1.35V(35W)
Iomax=21A(25W)/27A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

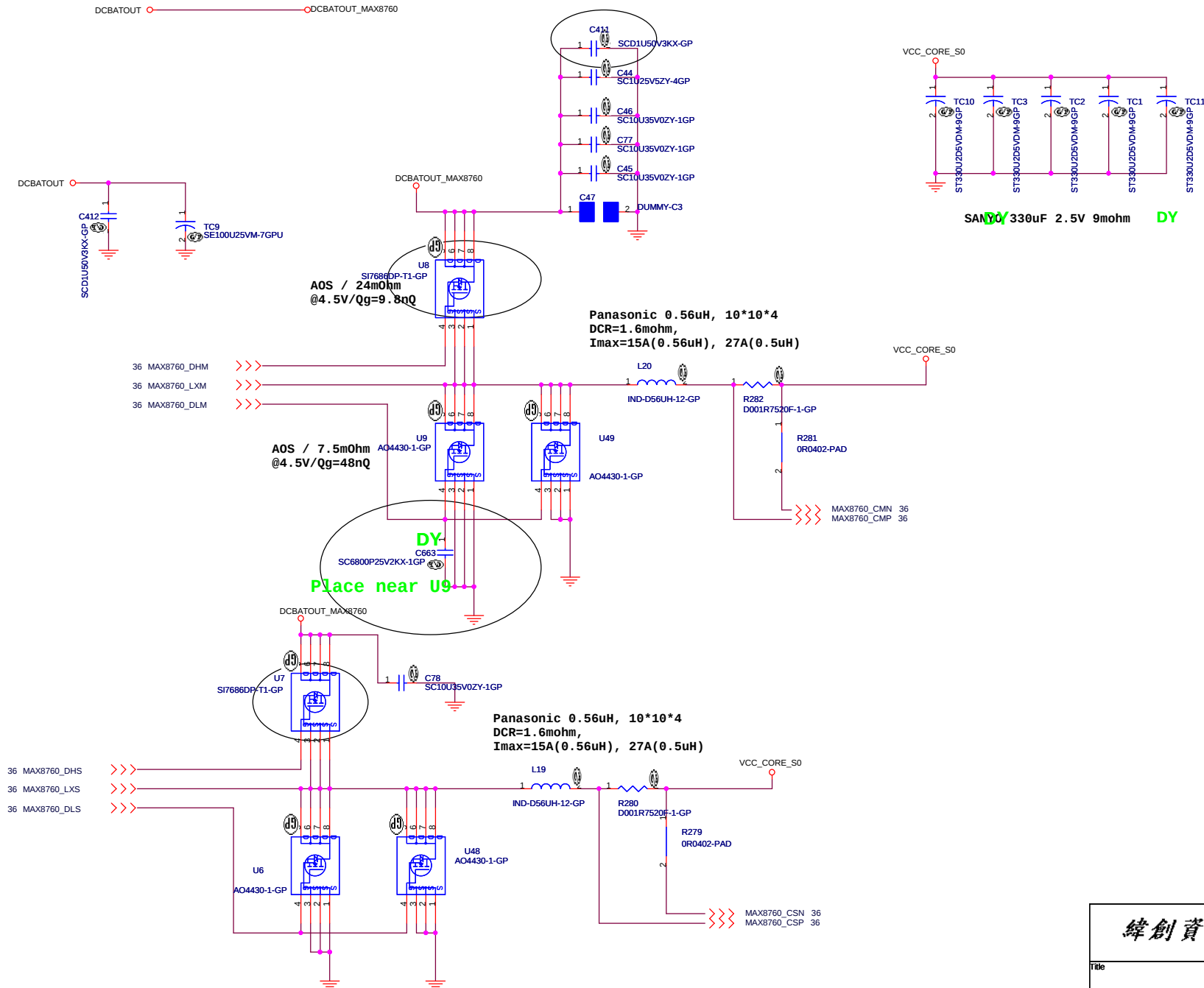
VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

TON: Frequency:
GND 550KHZ
REF 300KHZ
OPEN 200KHZ
VCC 100KHZ



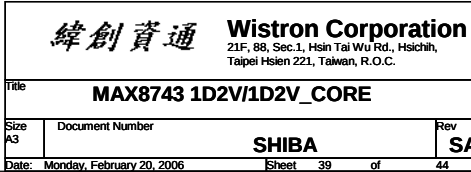
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title			CPU CORE MAX8760(1/2)		
Size	Document Number	SHIBA			Rev
A3					SA
Date:	Wednesday, February 22, 2006	Sheet	36	of	44

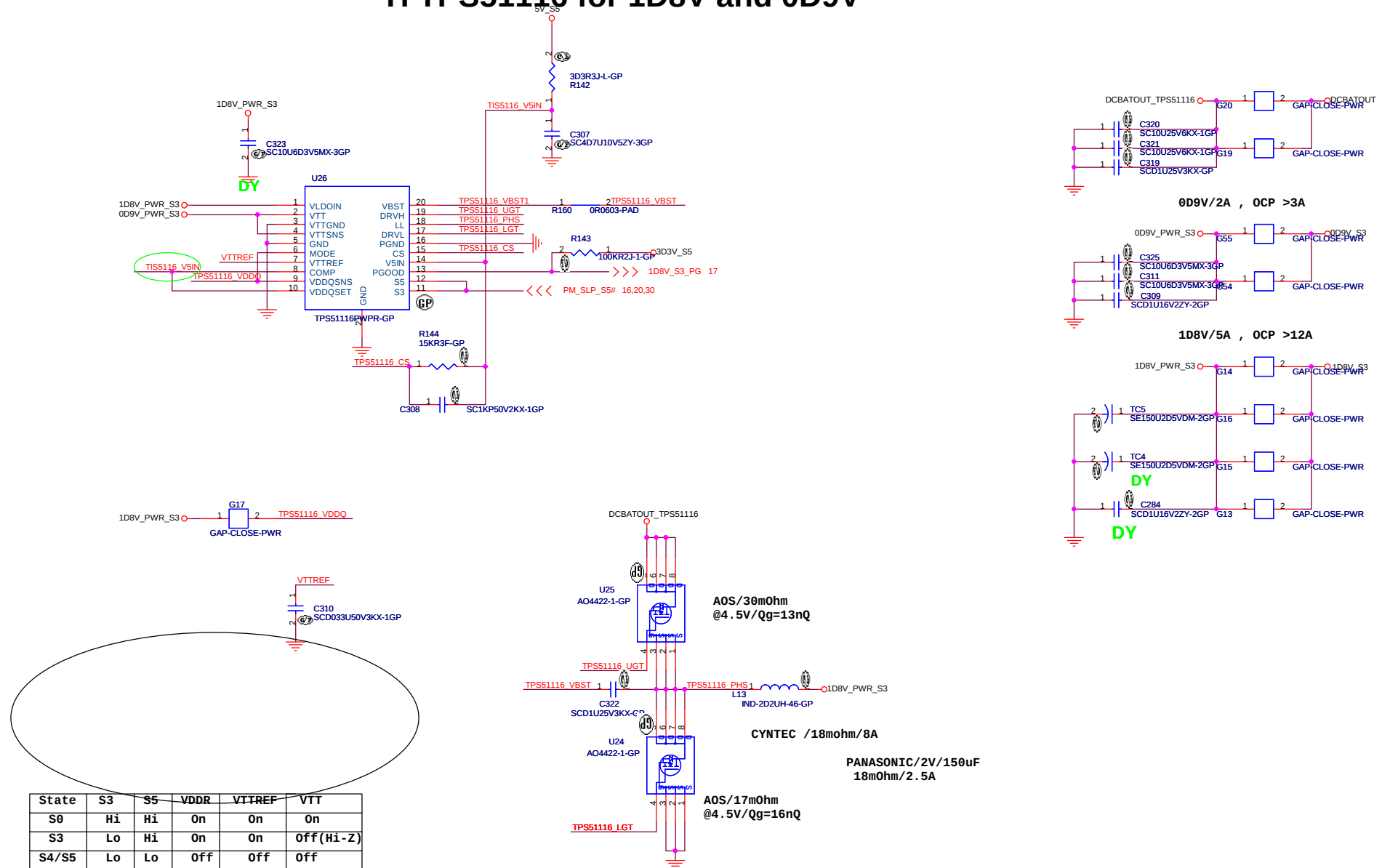


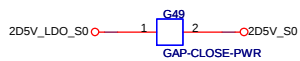
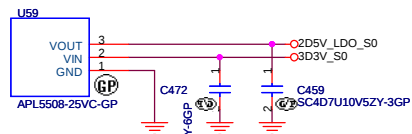
(Power Team)

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
CPU CORE MAX8760(2/2)			
Size	Document Number	Rev	
A3		SA	
Date: Wednesday, February 22, 2006		Sheet 37 of 44	



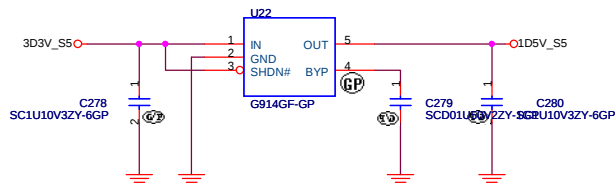
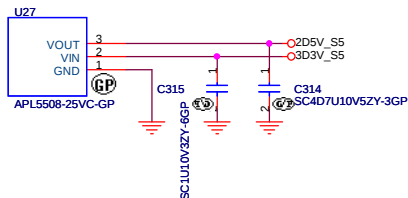
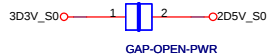
TI TPS51116 for 1D8V and 0D9V



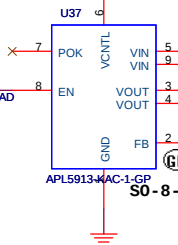
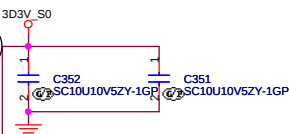
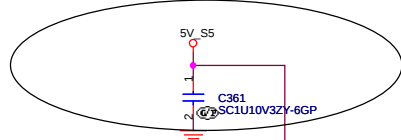


20,29,30,35,38,39 PM_SLP_S3#

G50



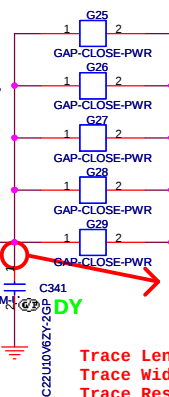
Change to S5 power plane



$$Vo=0.8*(1+(R1/R2))$$

KEMET
100uF, 4V, B2 Size, NTD:5.615
Iripple=1.1A, ESR=70mohm

Vo(cal.)=1.512V



Trace Length=3cm
Trace Width=5mils
Trace Resistance>80mohm

1D5V_S0
Iomax=1.3A
OCP=2.6A

2nd source : 74.00916.D3F

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
1D5V/2D5V/3D3V/5V_AUX		
Size	Document Number	Rev
A3	SHIBA	SA
Date:	Monday, February 20, 2006	Sheet 41 of 44

[illegible]

Title			
AD/BATT CONN			
Size A3	Document Number SHIBA	Rev SA	
Date: Thursday, February 23, 2006	Sheet 43	of	44

	FF	DF
CAMERA	○	×
LAN	10/100	10/100
1394/5 IN 1	○	×
EXTRA USB	○	×
MIC	○	×
CR LED	○	×

