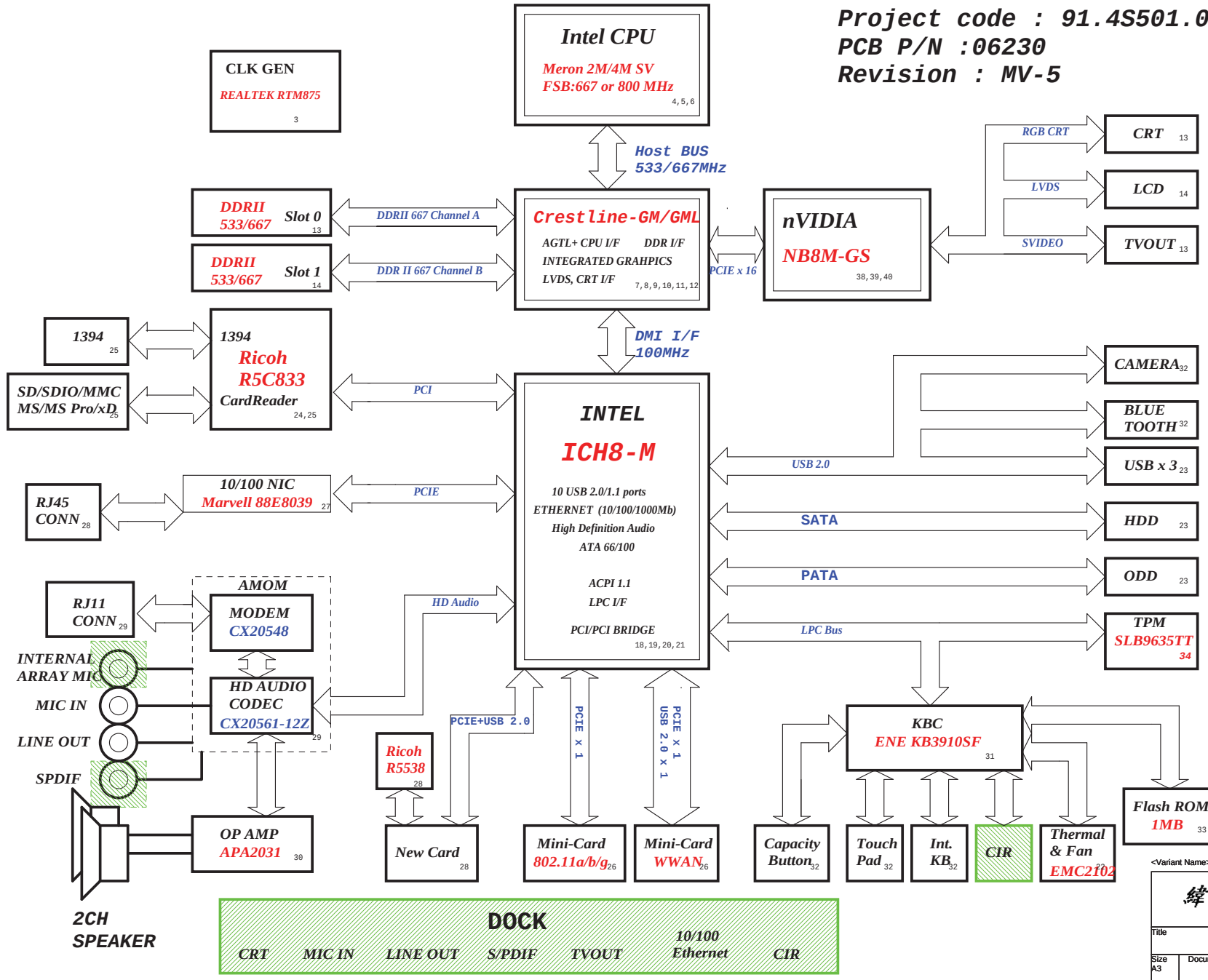
Viking-Discrete Block Diagram

Project code : 91.4S501.001
PCB P/N :06230
Revision : MV-5



SYSTEM DC/DC
TPS51120

INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC
MAX8743

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

SYSTEM DC/DC
FAN5234

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0 11A

MAXIM CHARGER
MAX8725

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC
MAX8736ETL

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: GND
L6: VCC
L7: Signal 4
L8: Signal 5
L9: GND
L10: Signal 5

<Variant Name>

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Title: Block Diagram

Size	Document Number	Rev
A3	Pamirs-Discrete	-5

Date: Wednesday, September 12, 2007 Sheet 1 of 47

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD/tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port config bit1

A16 swap override strap

PCI_GNT#3	
	low = A16 swap override enable
	high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

19,21 +RTCVCC → +RTCVCC
4,5,6,7,9,10,11,19,21,37,47 1D05V_S0 → 1D05V_S0
3,7,10,21,38 1D25V_S0 → 1D25V_S0
27 1D2V_LAN_S5 → 1D2V_LAN_S5
28 1D5V_NEW_S0 → 1D5V_NEW_S0
5,10,17,19,20,21,26,28,38,47 1D5V_S0 → 1D5V_S0
7,10,11,13,14,34,37,38 1D8V_S3 → 1D8V_S3
27,28 2D5V_LAN_S5 → 2D5V_LAN_S5
29,30 3D3V_AUD_S0 → 3D3V_AUD_S0
19,31,32,33,36,39,46 3D3V_AUX_S5 → 3D3V_AUX_S5
27,28 3D3V_LAN_S5 → 3D3V_LAN_S5
3,4,7,10,11,13,14,15,16,18,19,20,21,22,23,24,25,26,27,28,29,31,32,33,34,35,36,40,41,42,43,47 3D3V_S0 → 3D3V_S0
17,18,20,21,22,26,27,28,29,31,34,36,39,47 3D3V_S5 → 3D3V_S5
22,26,29,31,34,36 5V_AUX_S5 → 5V_AUX_S5
16,23,32,33,34,36,37,38 5V_S3 → 5V_S3
15,16,17,20,21,22,23,29,30,31,32,33,34,35,47 5V_S0 → 5V_S0
16,21,34,37,40 5V_S5 → 5V_S5
17,39,46,47 AD+ → AD+
16,17,34,35,36,37,39,40,47 DCBATOUT → DCBATOUT
13,14,38 DDR_VREF_S0 → DDR_VREF_S0
7,13,14,38 DDR_VREF_S3 → DDR_VREF_S3
22,31,33,39 KBC_3D3V_AUX → KBC_3D3V_AUX
16 LCDVDD_S0 → LCDVDD_S0
5,6,35 VCC_CORE_S0 → VCC_CORE_S0

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reversed	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

<Core Design>

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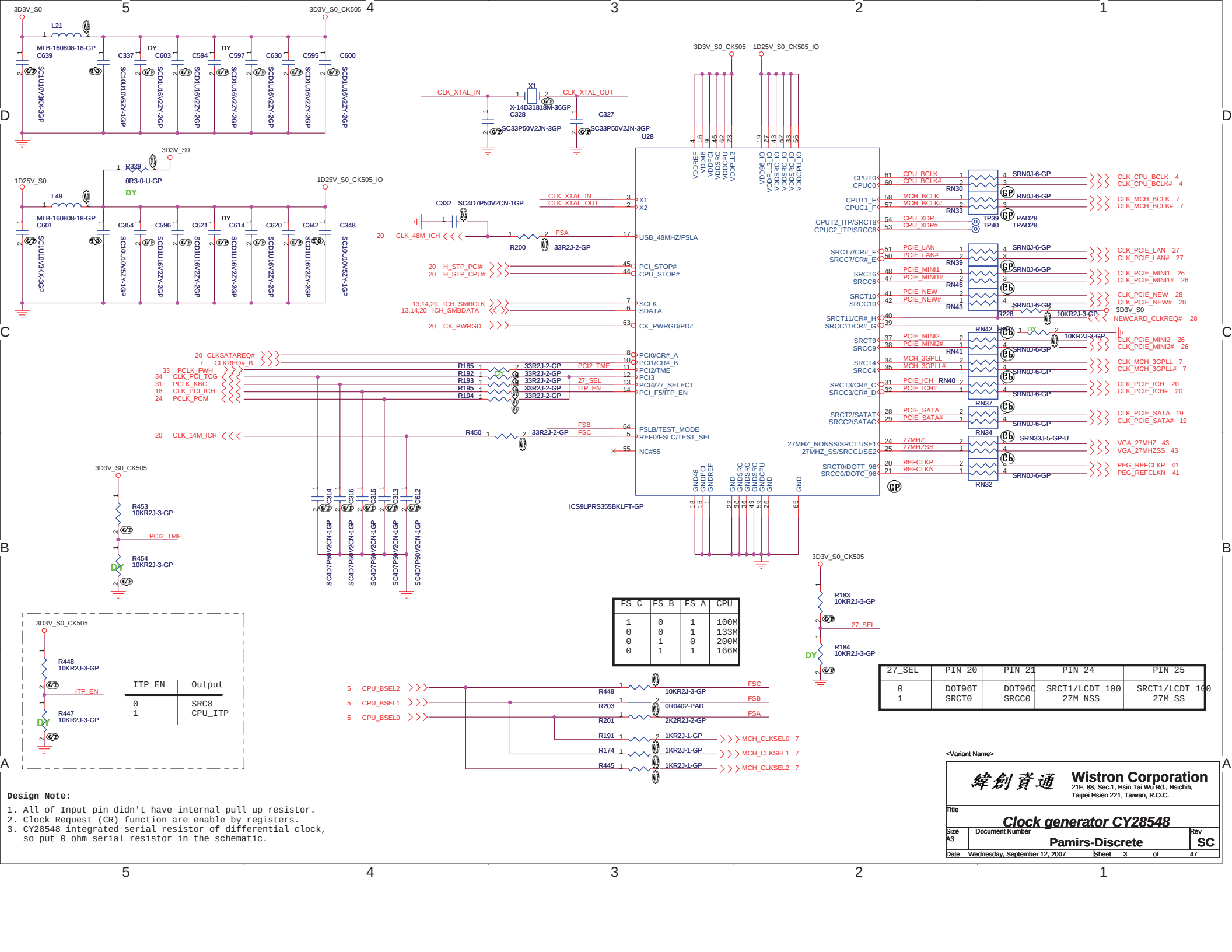

ITP_EN	Output
0	SRC8
1	CPU_ITP

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	200M
0	1	1	166M

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1	SRCT0	SRCC0	27M_NSS	27M_SS

Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

<Variant Name>

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Title: ***Clock generator CY28548***

Size	Document Number	Rev
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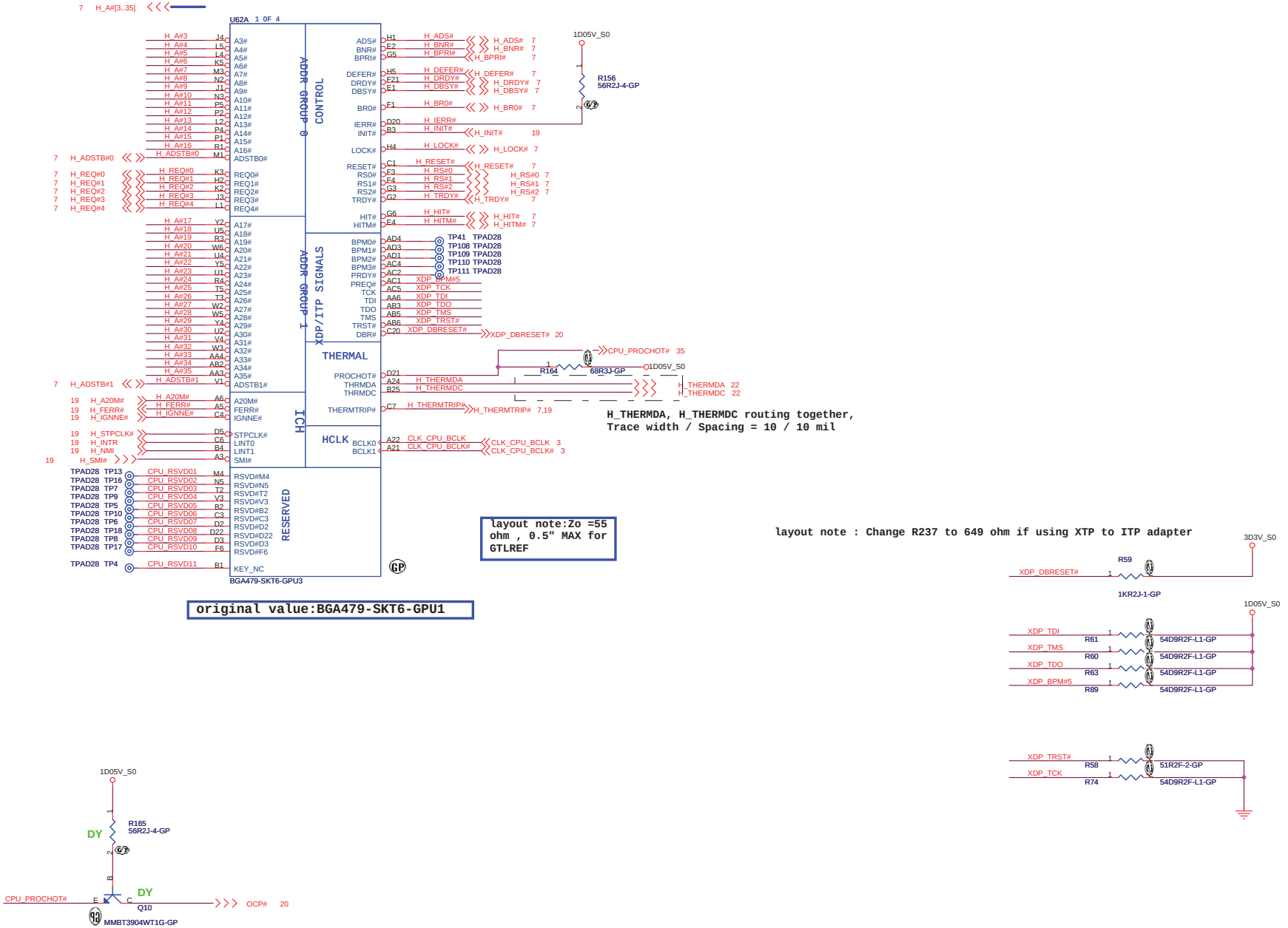

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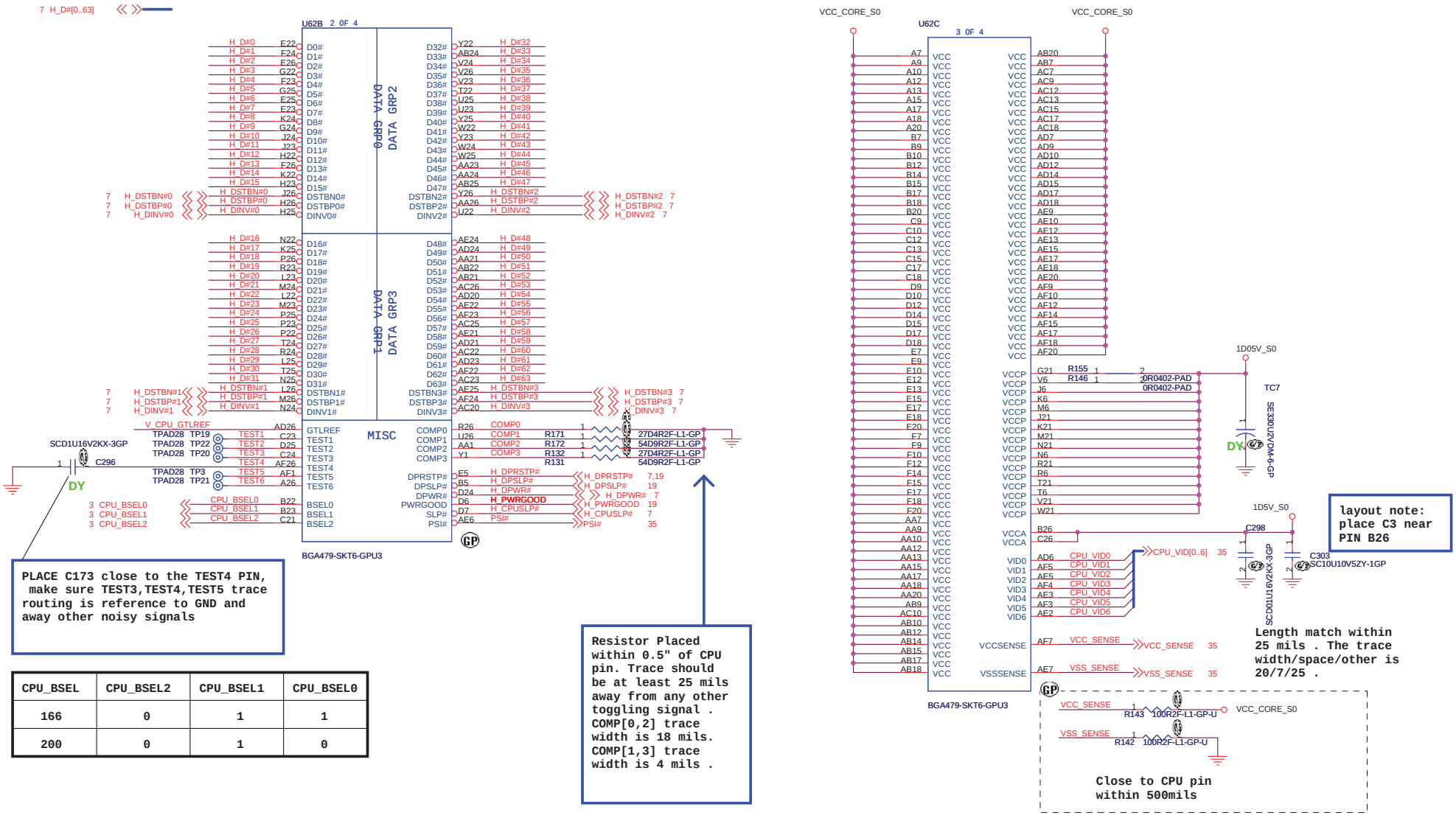
Title: Meron(1/3)-AGTL+/XDP

Size: Custom | Document Number: Pamirs-Discrete | Rev: SC

Date: Friday, September 14, 2007 | Sheet 4 of 47



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

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Title: Meron(2/3)-AGTL+/PWR

Size: A3 | Document Number: Pamirs-Discrete | Rev: SC

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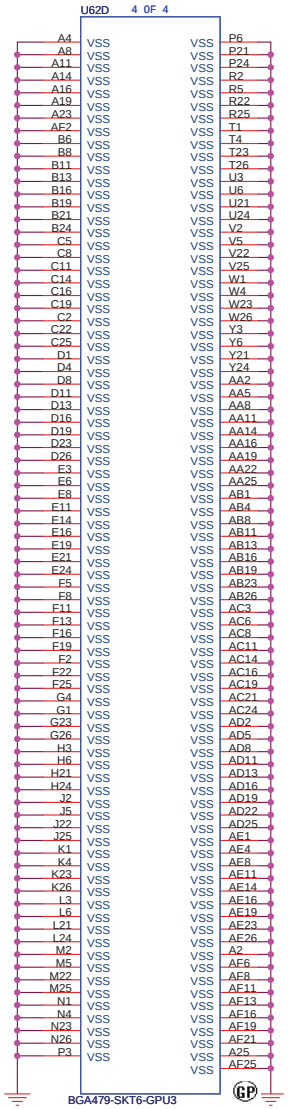
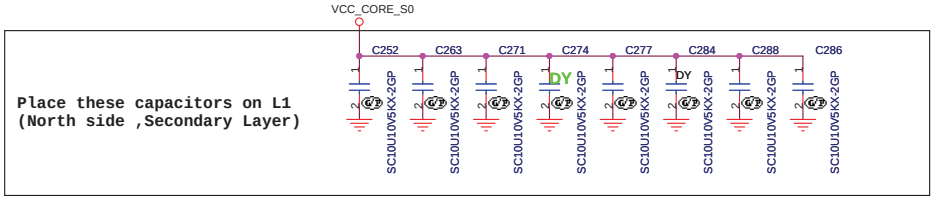
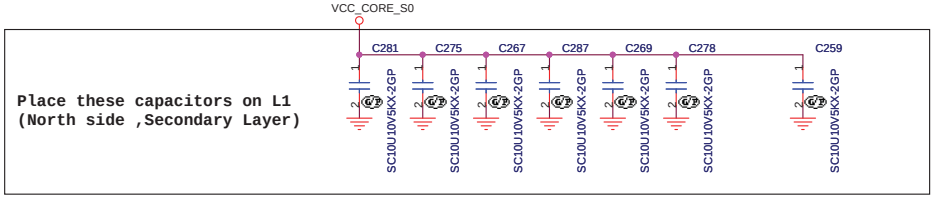
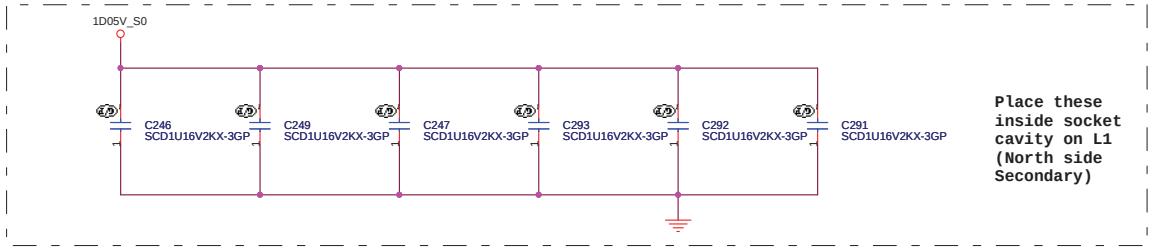






Mid Frequencd Decoupling



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Title: Meron(3/3)-GND&Bypass

Size: A3 | Document Number: Pamirs-Discrete | Rev: SC

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FOR Calero: 80.6 ohm
Crestline: 20 ohm

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

From Astro demo schematic

layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

Layout Note :
Place C151 within 100 mils of NB

Layout Note :
Place C153 near pin B3 of NB

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Title: CRESTLINE(1/6)-AGTL+/DMI/DDR2

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Custom	Pamirs-Discrete	SA

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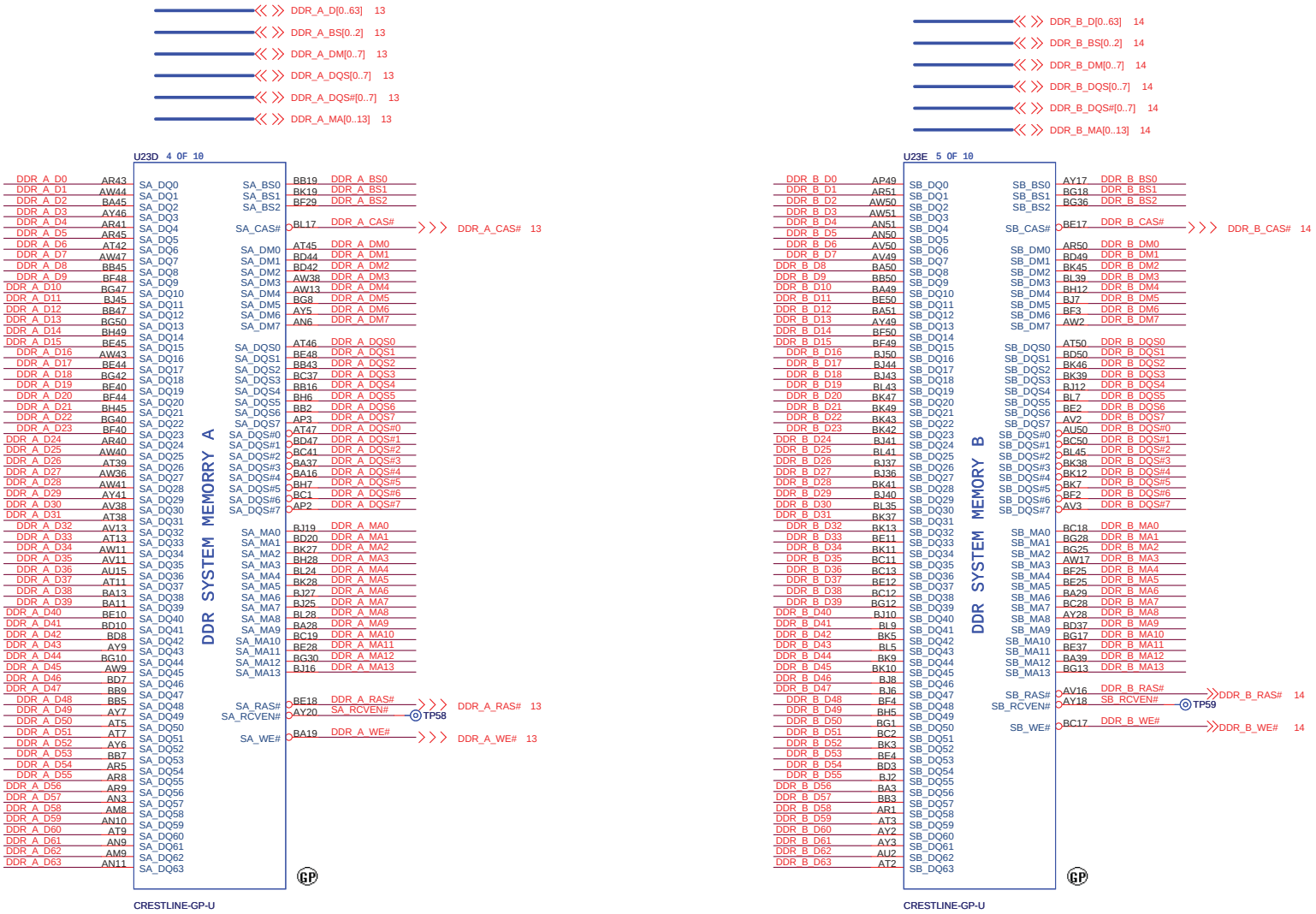

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Title
CRESTLINE(2/6)-DDR2 A/B CH

Size	Document Number	Rev
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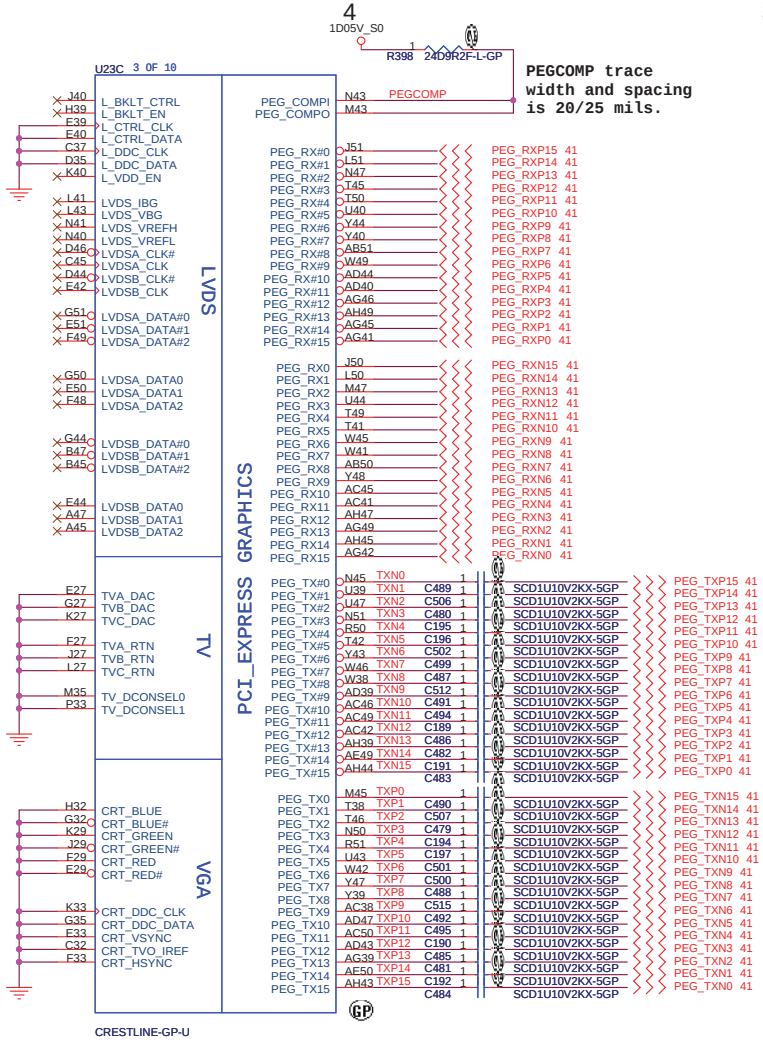

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

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Title: CRESTLINE(3/6)-VGA/LVDS/TV

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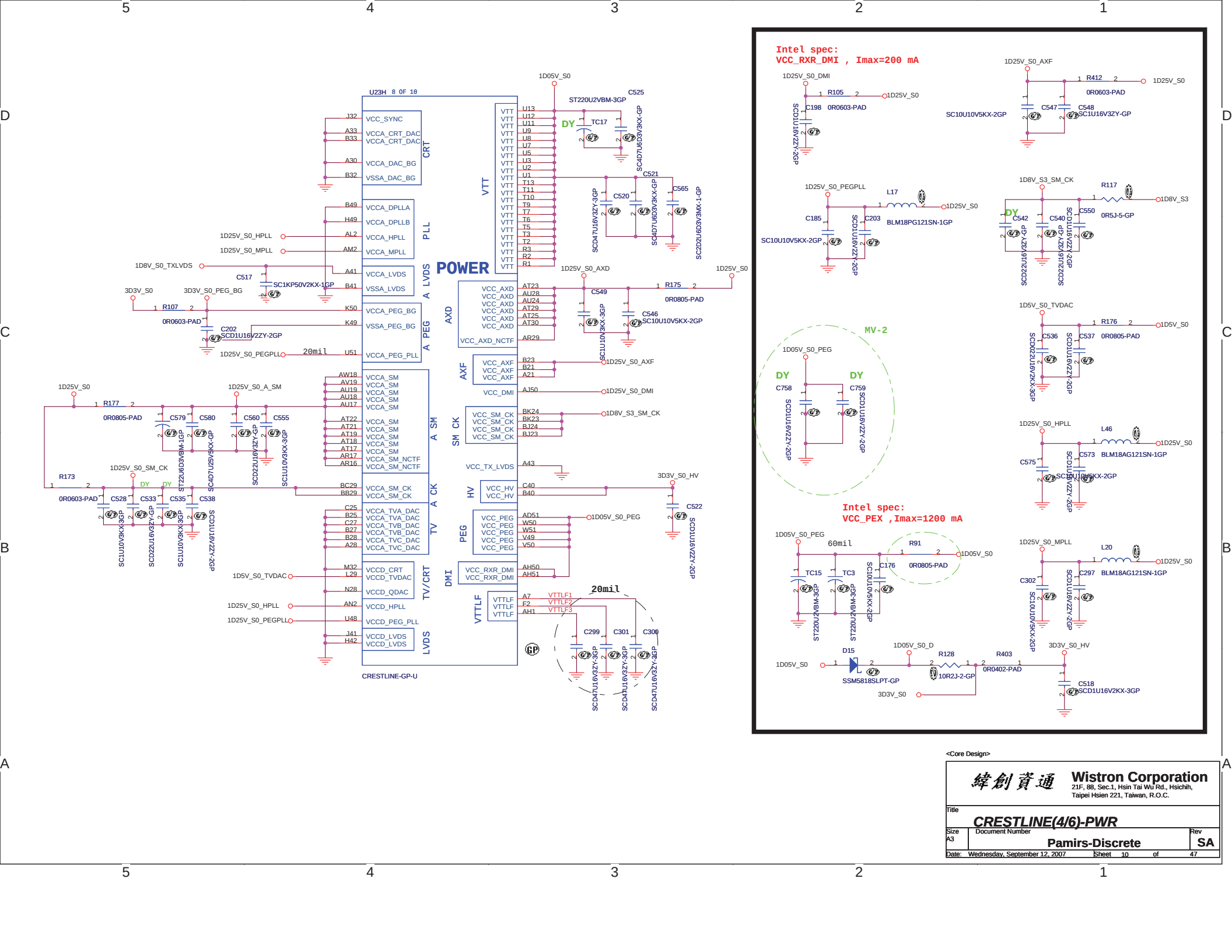

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Title: CRESTLINE(4/6)-PWR

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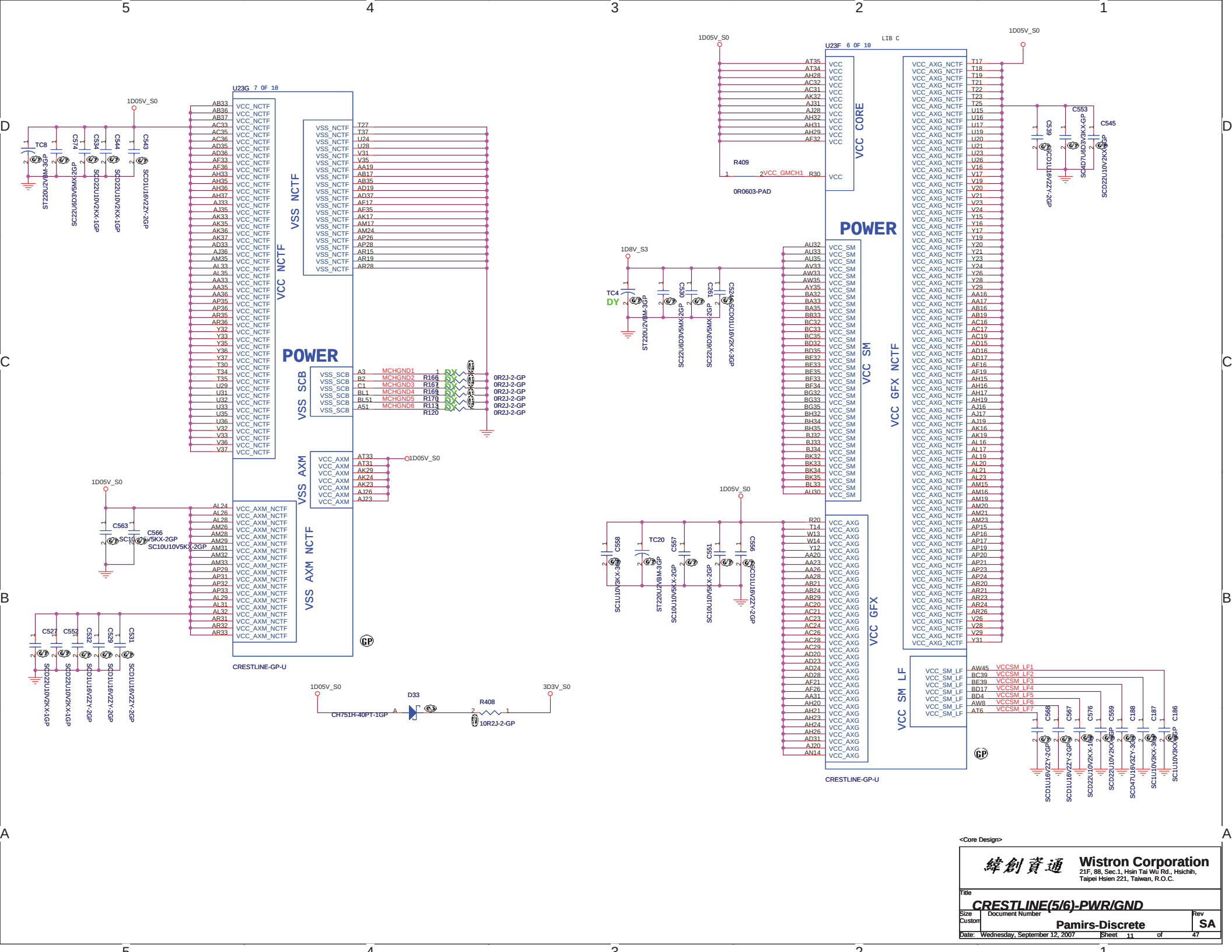
U23G 7 0F 10
POWER
VCC NCTF
VSS NCTF
VSS SCB
VSS AXM
VSS AXM NCTF
CRESTLINE-GP-U
U23F 6 0F 10
LIB C
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
CRESTLINE-GP-U
1D05V_S0
1D8V_S3
3D3V_S0
R409
0R0603-PAD
R408
D33
CH751H-40PT-1GP
0R2J-2-GP
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Title
CRESTLINE(5/6)-PWR/GND
Size Custom
Document Number
Pamirs-Discrete
Rev SA
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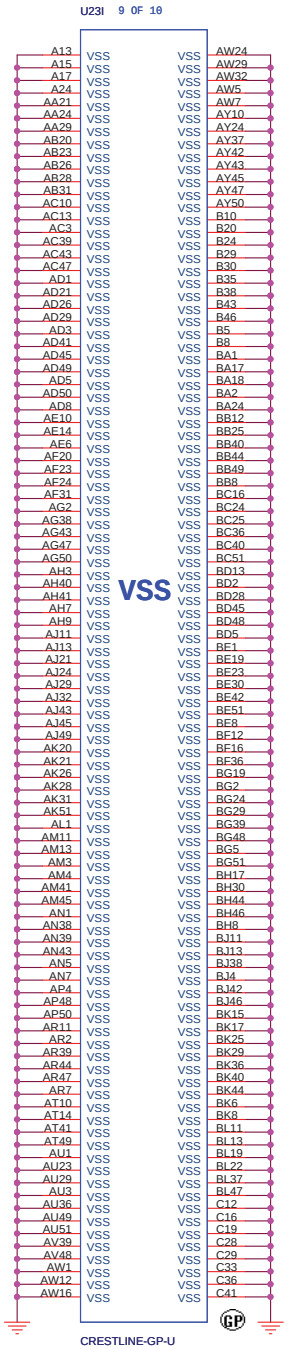

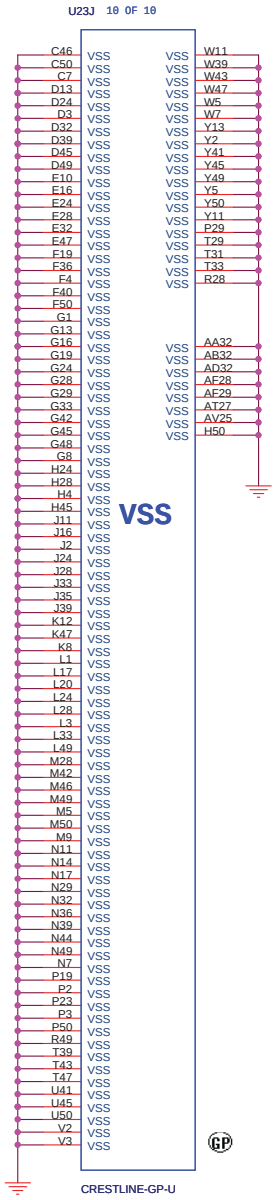

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Title
CRESTLINE(6/6)-PWR/GND

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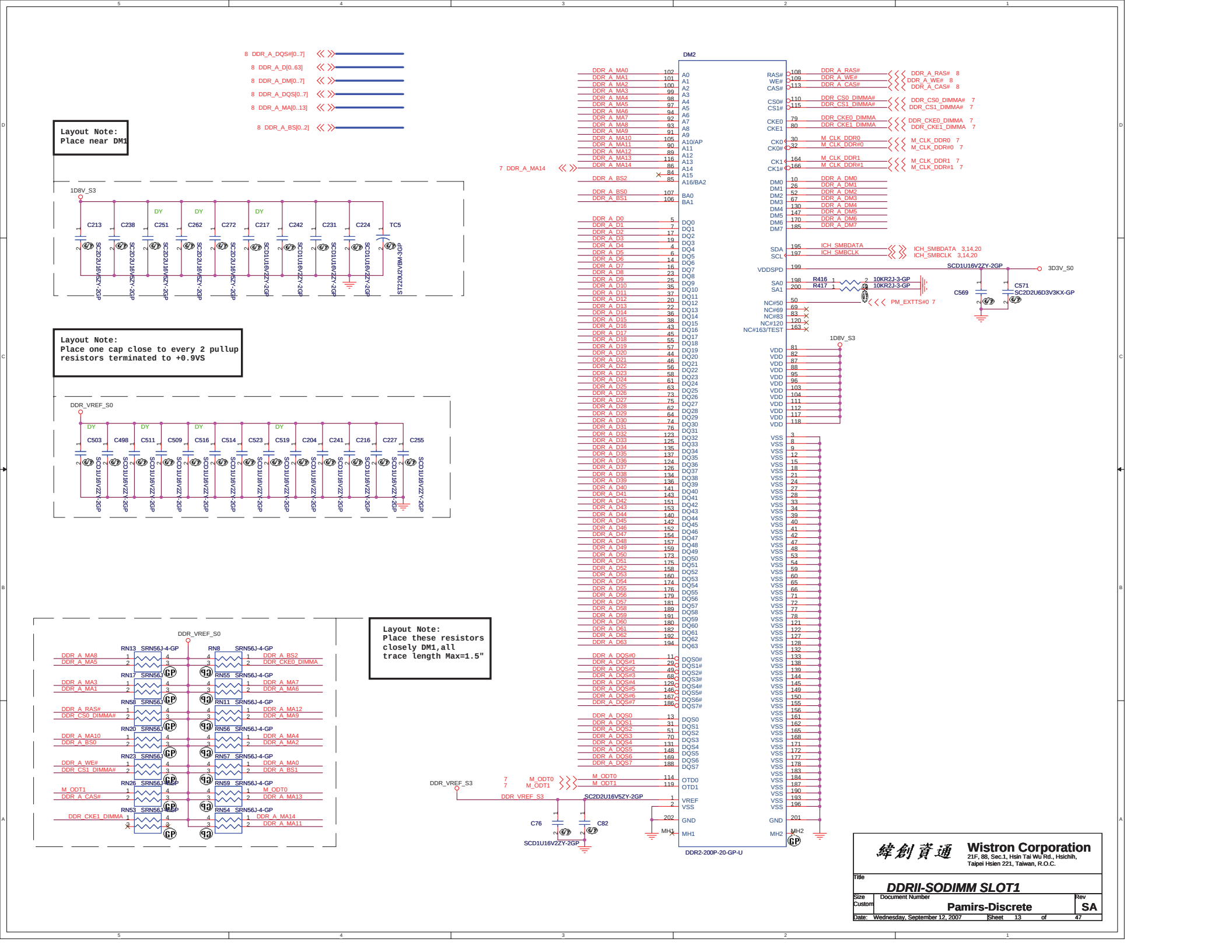

8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..13]
8 DDR_A_BS[0..2]
Layout Note:
Place near DM1
1D8V_S3
C213 C238 C251 C262 C272 C217 C242 C231 C224 TC5
DY
SC2D2U16VZY-2GP
ST220U2VBM-3GP
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
DDR_VREF_S0
C503 C498 C511 C509 C516 C514 C523 C519 C204 C241 C216 C227 C255
SCD1U16V2ZY-2GP
DDR_VREF_S0
RN13 SRN56J-4-GP
RN8 SRN56J-4-GP
RN17 SRN56J-4-GP
RN55 SRN56J-4-GP
RN58 SRN56J-4-GP
RN11 SRN56J-4-GP
RN20 SRN56J-4-GP
RN56 SRN56J-4-GP
RN23 SRN56J-4-GP
RN57 SRN56J-4-GP
RN26 SRN56J-4-GP
RN59 SRN56J-4-GP
RN53 SRN56J-4-GP
RN54 SRN56J-4-GP
DDR_A_MA8 DDR_A_MA5 DDR_A_MA3 DDR_A_MA1 DDR_A_RAS# DDR_CS0_DIMMA# DDR_A_MA10 DDR_A_BS0 DDR_A_WE# DDR_CS1_DIMMA# M_ODT1 DDR_A_CAS# DDR_CKE1_DIMMA
DDR_A_BS2 DDR_CKE0_DIMMA DDR_A_MA7 DDR_A_MA6 DDR_A_MA12 DDR_A_MA9 DDR_A_MA4 DDR_A_MA2 DDR_A_MA0 DDR_A_BS1 M_ODT0 DDR_A_MA13 DDR_A_MA14 DDR_A_MA11
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
DM2
DDR_A_MA0 DDR_A_MA1 DDR_A_MA2 DDR_A_MA3 DDR_A_MA4 DDR_A_MA5 DDR_A_MA6 DDR_A_MA7 DDR_A_MA8 DDR_A_MA9 DDR_A_MA10 DDR_A_MA11 DDR_A_MA12 DDR_A_MA13 DDR_A_MA14
DDR_A_BS2 DDR_A_BS0 DDR_A_BS1
DDR_A_D0 DDR_A_D1 DDR_A_D2 DDR_A_D3 DDR_A_D4 DDR_A_D5 DDR_A_D6 DDR_A_D7 DDR_A_D8 DDR_A_D9 DDR_A_D10 DDR_A_D11 DDR_A_D12 DDR_A_D13 DDR_A_D14 DDR_A_D15 DDR_A_D16 DDR_A_D17 DDR_A_D18 DDR_A_D19 DDR_A_D20 DDR_A_D21 DDR_A_D22 DDR_A_D23 DDR_A_D24 DDR_A_D25 DDR_A_D26 DDR_A_D27 DDR_A_D28 DDR_A_D29 DDR_A_D30 DDR_A_D31 DDR_A_D32 DDR_A_D33 DDR_A_D34 DDR_A_D35 DDR_A_D36 DDR_A_D37 DDR_A_D38 DDR_A_D39 DDR_A_D40 DDR_A_D41 DDR_A_D42 DDR_A_D43 DDR_A_D44 DDR_A_D45 DDR_A_D46 DDR_A_D47 DDR_A_D48 DDR_A_D49 DDR_A_D50 DDR_A_D51 DDR_A_D52 DDR_A_D53 DDR_A_D54 DDR_A_D55 DDR_A_D56 DDR_A_D57 DDR_A_D58 DDR_A_D59 DDR_A_D60 DDR_A_D61 DDR_A_D62 DDR_A_D63
DDR_A_DQS#0 DDR_A_DQS#1 DDR_A_DQS#2 DDR_A_DQS#3 DDR_A_DQS#4 DDR_A_DQS#5 DDR_A_DQS#6 DDR_A_DQS#7
DDR_A_DQS0 DDR_A_DQS1 DDR_A_DQS2 DDR_A_DQS3 DDR_A_DQS4 DDR_A_DQS5 DDR_A_DQS6 DDR_A_DQS7
M_ODT0 M_ODT1
DDR_VREF_S3
SC2D2U16V5ZY-2GP
C76 C82
SCD1U16V2ZY-2GP
MH1
DDR2-200P-20-GP-U
RAS# WE# CAS# CS0# CS1# CKE0 CKE1 CK0 CK0# CK1 CK1# DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
DDR_A_RAS# DDR_A_WE# DDR_A_CAS# DDR_CS0_DIMMA# DDR_CS1_DIMMA# DDR_CKE0_DIMMA DDR_CKE1_DIMMA M_CLK_DDR0 M_CLK_DDR0# M_CLK_DDR1 M_CLK_DDR1# DDR_A_DM0 DDR_A_DM1 DDR_A_DM2 DDR_A_DM3 DDR_A_DM4 DDR_A_DM5 DDR_A_DM6 DDR_A_DM7
SDA SCL
ICH_SMBDATA ICH_SMBCLK
VDDSPD
SA0 SA1
R416 R417 10KR2J-3-GP
PM_EXTTS#0
NC#50 NC#69 NC#83 NC#120 NC#163/TEST
C569 C571 SCD1U16V2ZY-2GP SC2D2U6D3V3KX-GP
3D3V_S0
1D8V_S3
VDD
VSS
GND
MH2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT1
Size Custom
Document Number
Pamirs-Discrete
Rev SA
Date: Wednesday, September 12, 2007
Sheet 13 of 47

8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]
8 DDR_B_BS[0..2]

Layout Note:
Place near DM2

1D8V_S3
DY C541 C508 C244 C497 C232 C513 DY C170 C221 DY C264
SCD1U16V2ZY-2GP

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

DDR_VREF_S0
DY C245 C256 C184 DY C207 C234 C265 C226 C235 C243 C237 C215 C183 DY C225
SCD1U16V2Z7-2GP

DDR_VREF_S0
RN18 SRN56J-4-GP: DDR_B_MA3, DDR_B_MA1
RN21 SRN56J-4-GP: DDR_B_MA10, DDR_B_BS0
RN19 SRN56J-4-GP: DDR_B_MA0, DDR_B_BS1
RN22 SRN56J-4-GP: DDR_CS2_DIMMB#, DDR_B_RAS#
RN24 SRN56J-4-GP: DDR_B_WE#, DDR_B_CAS#
RN27 SRN56J-4-GP: DDR_CS3_DIMMB#, M_ODT3
RN9 SRN56J-4-GP: DDR_B_MA14
RN10 SRN56J-4-GP: DDR_B_MA12, DDR_B_MA9
RN7 SRN56J-4-GP: DDR_CKE3_DIMMB, DDR_B_MA11
RN14 SRN56J-4-GP: DDR_B_MA5, DDR_B_MA8
RN12 SRN56J-4-GP: DDR_B_MA7, DDR_B_MA6
RN16 SRN56J-4-GP: DDR_B_MA4, DDR_B_MA2
RN25 SRN56J-4-GP: M_ODT2, DDR_B_MA13
RN6 SRN56J-4-GP: DDR_B_BS2, DDR_CKE2_DIMMB
SRN56J-4-GP

Layout Note:
Place these resistors closely DM2,all trace length Max=1.5"

DM1
7 DDR_B_MA14
DDR_B_MA0 102 A0
DDR_B_MA1 101 A1
DDR_B_MA2 100 A2
DDR_B_MA3 99 A3
DDR_B_MA4 98 A4
DDR_B_MA5 97 A5
DDR_B_MA6 94 A6
DDR_B_MA7 92 A7
DDR_B_MA8 93 A8
DDR_B_MA9 91 A9
DDR_B_MA10 105 A10/AP
DDR_B_MA11 90 A11
DDR_B_MA12 89 A12
DDR_B_MA13 116 A13
DDR_B_MA14 86 A14
84 A15
DDR_B_BS2 85 A16/BA2
DDR_B_BS0 107 BA0
DDR_B_BS1 106 BA1
DDR_B_D0 5 DQ0
DDR_B_D1 7 DQ1
DDR_B_D2 17 DQ2
DDR_B_D3 19 DQ3
DDR_B_D4 4 DQ4
DDR_B_D5 6 DQ5
DDR_B_D6 14 DQ6
DDR_B_D7 16 DQ7
DDR_B_D8 23 DQ8
DDR_B_D9 25 DQ9
DDR_B_D10 35 DQ10
DDR_B_D11 37 DQ11
DDR_B_D12 20 DQ12
DDR_B_D13 22 DQ13
DDR_B_D14 36 DQ14
DDR_B_D15 38 DQ15
DDR_B_D16 43 DQ16
DDR_B_D17 45 DQ17
DDR_B_D18 55 DQ18
DDR_B_D19 57 DQ19
DDR_B_D20 44 DQ20
DDR_B_D21 46 DQ21
DDR_B_D22 56 DQ22
DDR_B_D23 58 DQ23
DDR_B_D24 61 DQ24
DDR_B_D25 63 DQ25
DDR_B_D26 73 DQ26
DDR_B_D27 75 DQ27
DDR_B_D28 62 DQ28
DDR_B_D29 64 DQ29
DDR_B_D30 74 DQ30
DDR_B_D31 76 DQ31
DDR_B_D32 123 DQ32
DDR_B_D33 125 DQ33
DDR_B_D34 135 DQ34
DDR_B_D35 137 DQ35
DDR_B_D36 124 DQ36
DDR_B_D37 126 DQ37
DDR_B_D38 134 DQ38
DDR_B_D39 136 DQ39
DDR_B_D40 141 DQ40
DDR_B_D41 143 DQ41
DDR_B_D42 151 DQ42
DDR_B_D43 153 DQ43
DDR_B_D44 140 DQ44
DDR_B_D45 142 DQ45
DDR_B_D46 152 DQ46
DDR_B_D47 154 DQ47
DDR_B_D48 157 DQ48
DDR_B_D49 159 DQ49
DDR_B_D50 173 DQ50
DDR_B_D51 175 DQ51
DDR_B_D52 158 DQ52
DDR_B_D53 160 DQ53
DDR_B_D54 174 DQ54
DDR_B_D55 176 DQ55
DDR_B_D56 179 DQ56
DDR_B_D57 181 DQ57
DDR_B_D58 189 DQ58
DDR_B_D59 191 DQ59
DDR_B_D60 180 DQ60
DDR_B_D61 182 DQ61
DDR_B_D62 192 DQ62
DDR_B_D63 194 DQ63
DDR_B_DQS#0 11 DQS0#
DDR_B_DQS#1 29 DQS1#
DDR_B_DQS#2 49 DQS2#
DDR_B_DQS#3 68 DQS3#
DDR_B_DQS#4 129 DQS4#
DDR_B_DQS#5 146 DQS5#
DDR_B_DQS#6 167 DQS6#
DDR_B_DQS#7 186 DQS7#
DDR_B_DQS0 13 DQS0
DDR_B_DQS1 31 DQS1
DDR_B_DQS2 51 DQS2
DDR_B_DQS3 70 DQS3
DDR_B_DQS4 131 DQS4
DDR_B_DQS5 148 DQS5
DDR_B_DQS6 169 DQS6
DDR_B_DQS7 188 DQS7
M_ODT2 114 OTD0
M_ODT3 119 OTD1
1 VREF
2 VSS
202 GND
MH1
DDR2-200P-21-GP-U

RAS# 108 DDR_B_RAS# → DDR_B_RAS# 8
WE# 109 DDR_B_WE# → DDR_B_WE# 8
CAS# 113 DDR_B_CAS# → DDR_B_CAS# 8
CS0# 110 DDR_CS2_DIMMB# → DDR_CS2_DIMMB# 7
CS1# 115 DDR_CS3_DIMMB# → DDR_CS3_DIMMB# 7
CKE0 79 DDR_CKE2_DIMMB → DDR_CKE2_DIMMB 7
CKE1 80 DDR_CKE3_DIMMB → DDR_CKE3_DIMMB 7
CK0 30 M_CLK_DDR2 → M_CLK_DDR2 7
CK0# 32 M_CLK_DDR#2 → M_CLK_DDR#2 7
CK1 164 M_CLK_DDR3 → M_CLK_DDR3 7
CK1# 166 M_CLK_DDR#3 → M_CLK_DDR#3 7
DM0 10 DDR_B_DM0
DM1 26 DDR_B_DM1
DM2 52 DDR_B_DM2
DM3 67 DDR_B_DM3
DM4 130 DDR_B_DM4
DM5 147 DDR_B_DM5
DM6 170 DDR_B_DM6
DM7 185 DDR_B_DM7
SDA 195 ICH_SMBDATA → ICH_SMBDATA 3,13,20
SCL 197 ICH_SMBCLK → ICH_SMBCLK 3,13,20
VDDSPD 199 SCD1U16V2ZY-2GP → 3D3V_S0
SA0 198 R420 10KR2J-3-GP
SA1 200 R421 10KR2J-3-GP → 3D3V_S0
C577 SC2D2U6D3V3KX-GP
C578
50 PM_EXTTS#1 7
NC#50 69
NC#69
NC#83 83
NC#120 120
NC#163/TEST 163

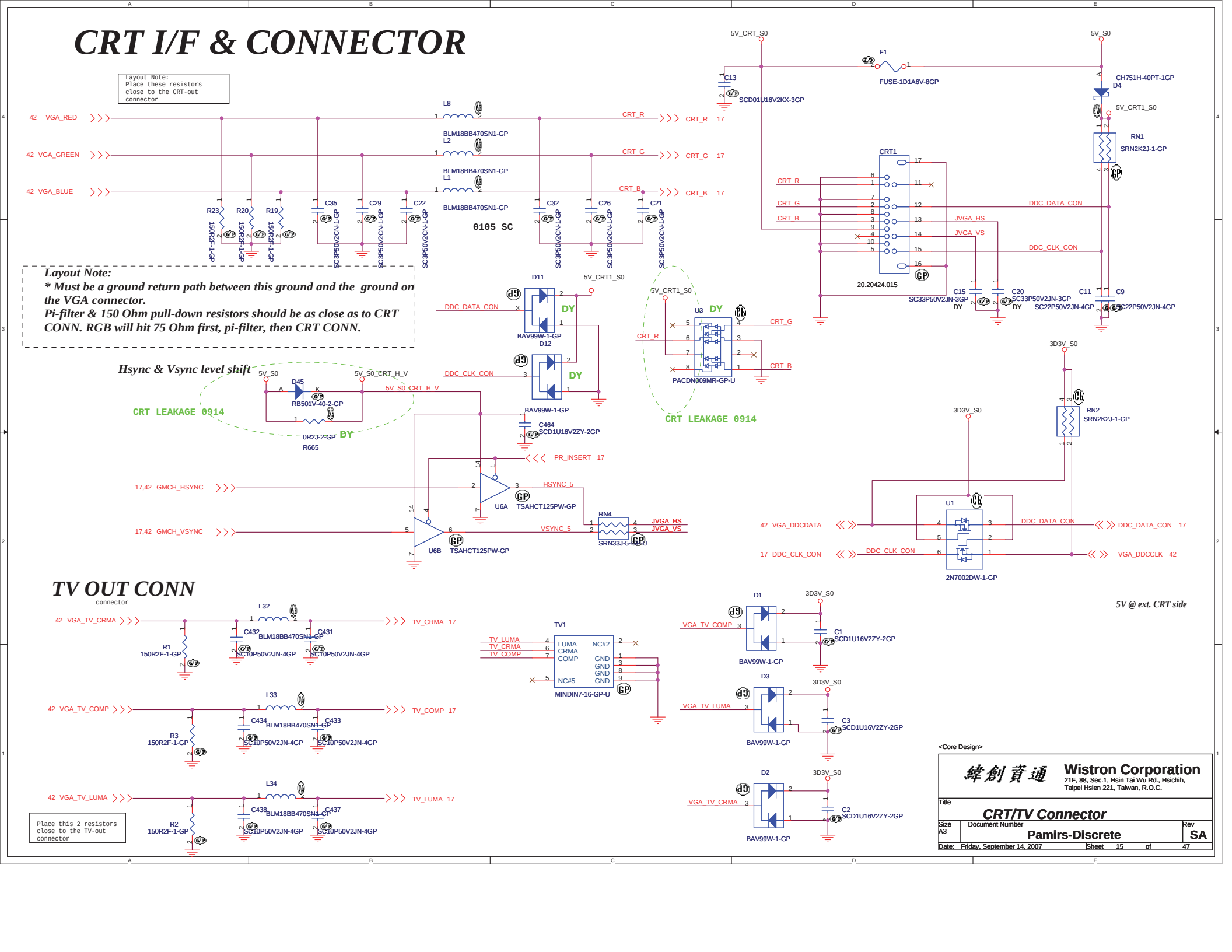
1D8V_S3
VDD 81 82 87 88 95 96 103 104 111 112 117 118

VSS 3 8 9 12 15 18 21 24 27 28 33 34 39 40 41 42 47 48 53 54 59 60 65 66 71 72 77 78 121 122 127 128 132 133 138 139 144 145 149 150 155 156 161 162 165 168 171 172 177 178 183 184 187 190 193 196
GND 201 MH2

DDR_VREF_S3
7 M_ODT2
7 M_ODT3
DDR_VREF_S3
SC2D2U16V5ZY-2GP
C71 C77
SCD1U16V2ZY-2GP

緯創資通	**Wistron Corporation**	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DDRII-SODIMM SLOT2***	
Size: Custom	Document Number: **Pamirs-Discrete**	Rev: **SA**
Date: Wednesday, September 12, 2007	Sheet 14 of 47	

CRT I/F & CONNECTOR



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

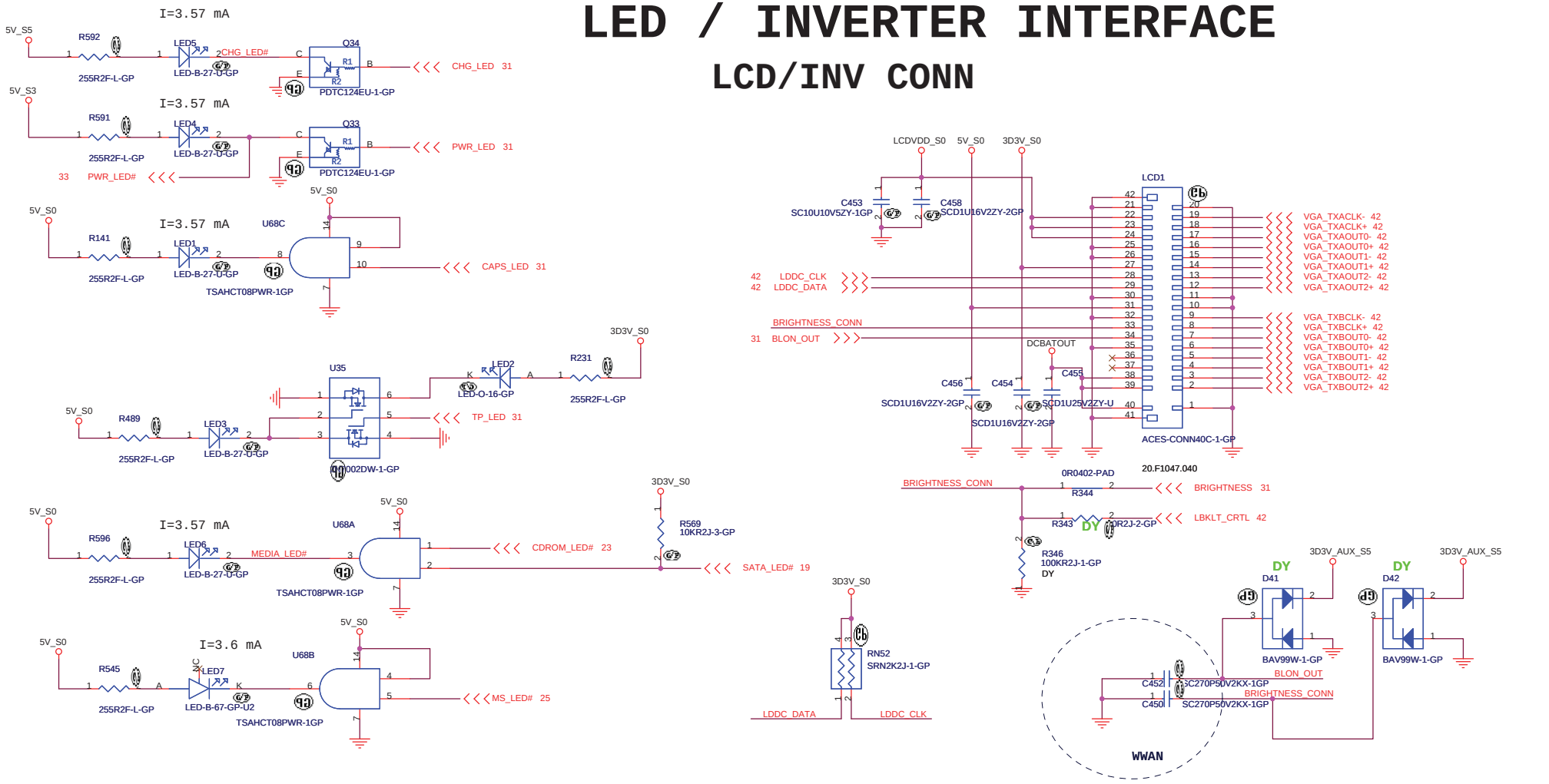
Title: CRT/TV Connector

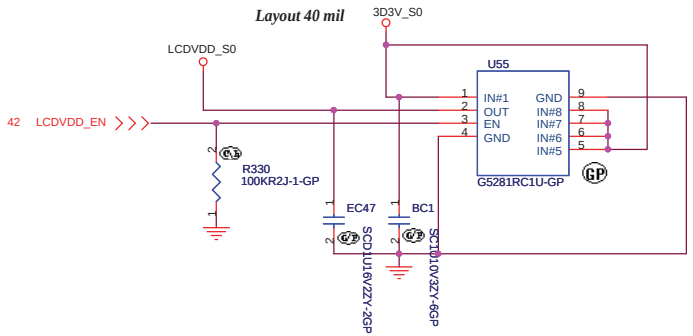
Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Friday, September 14, 2007 Sheet 15 of 47

LED / INVERTER INTERFACE

LCD/INV CONN





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD/Inverter Connector**

Size	Document Number	Rev
Custom	Pamirs-Discrete	SA

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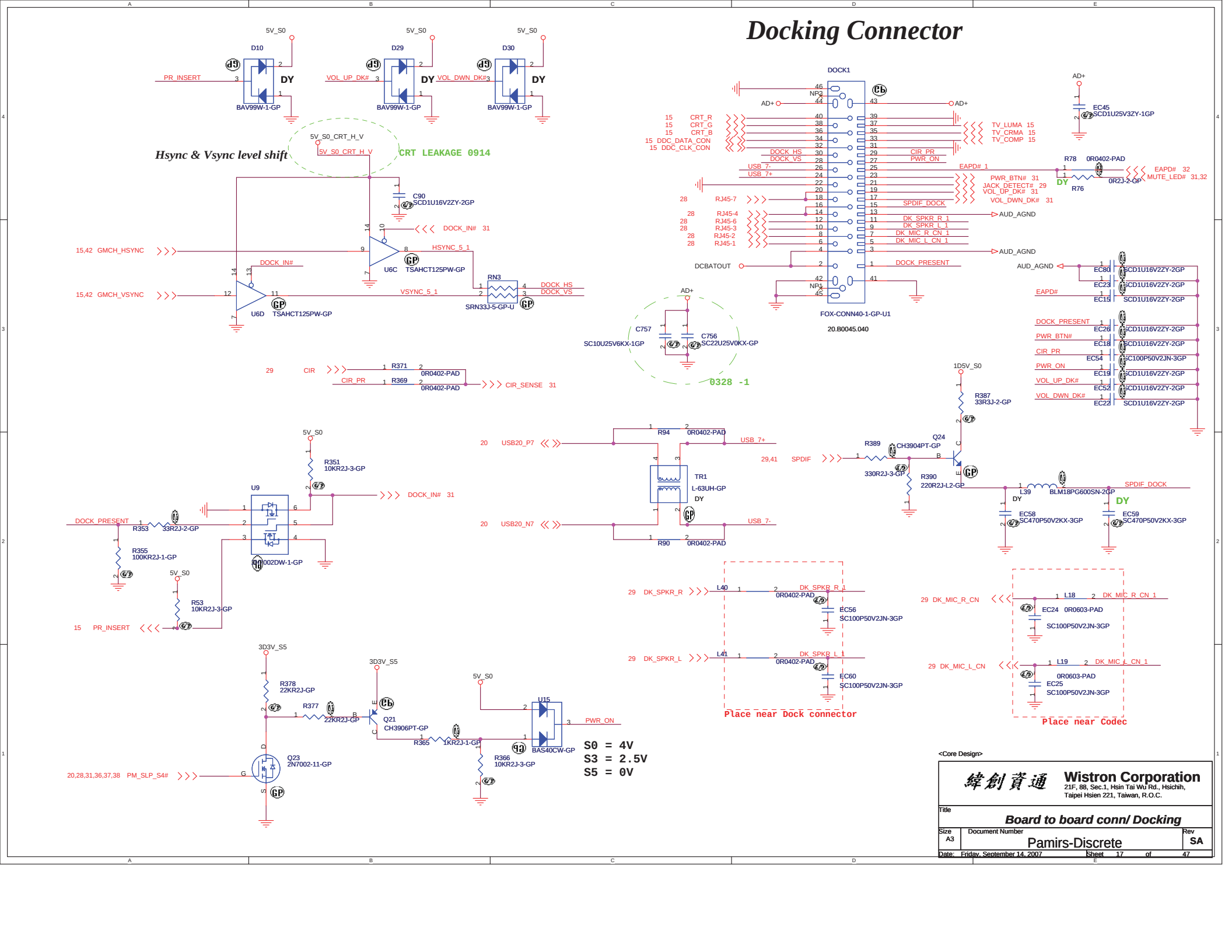
Docking Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Board to board conn/ Docking**

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

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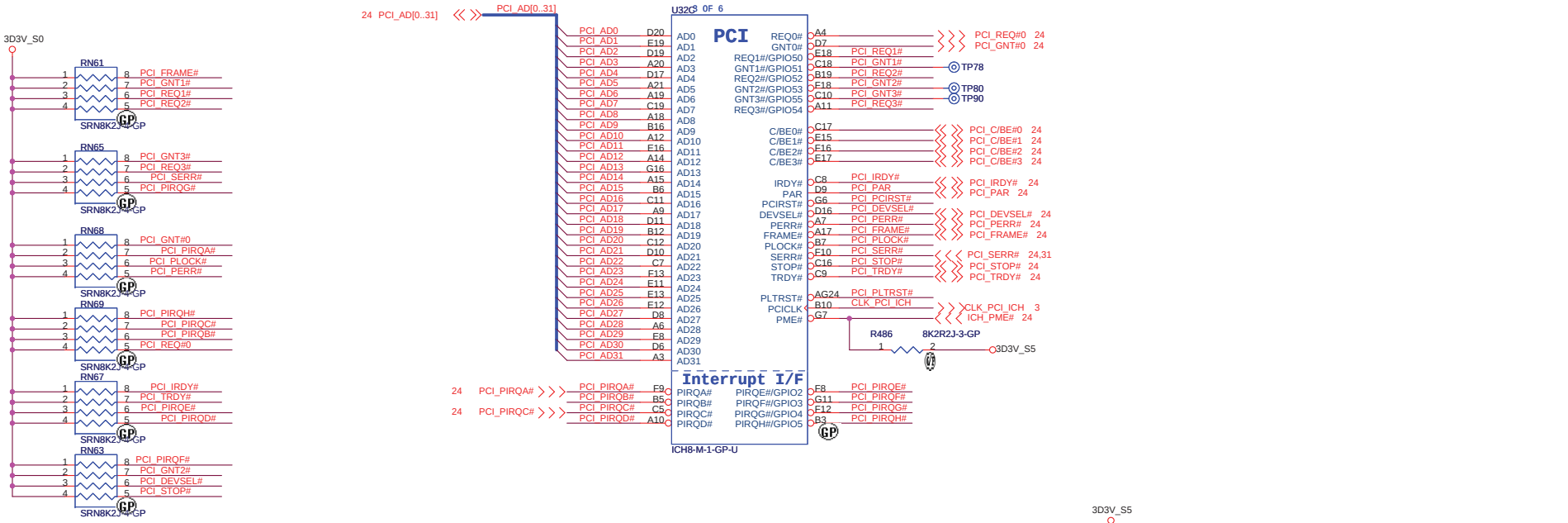
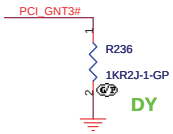
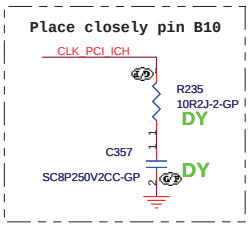
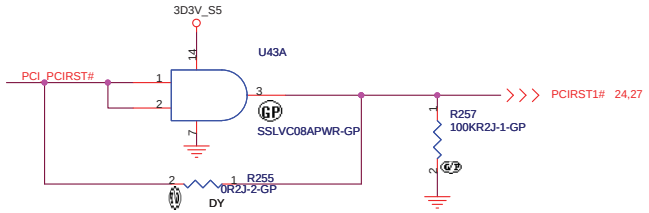


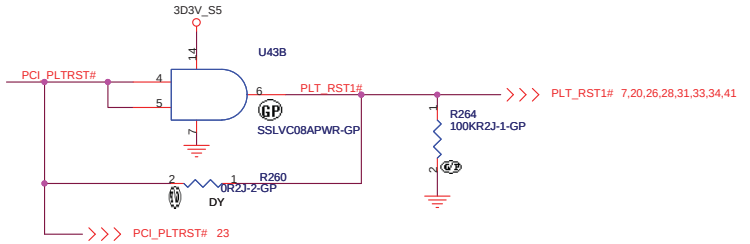


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *







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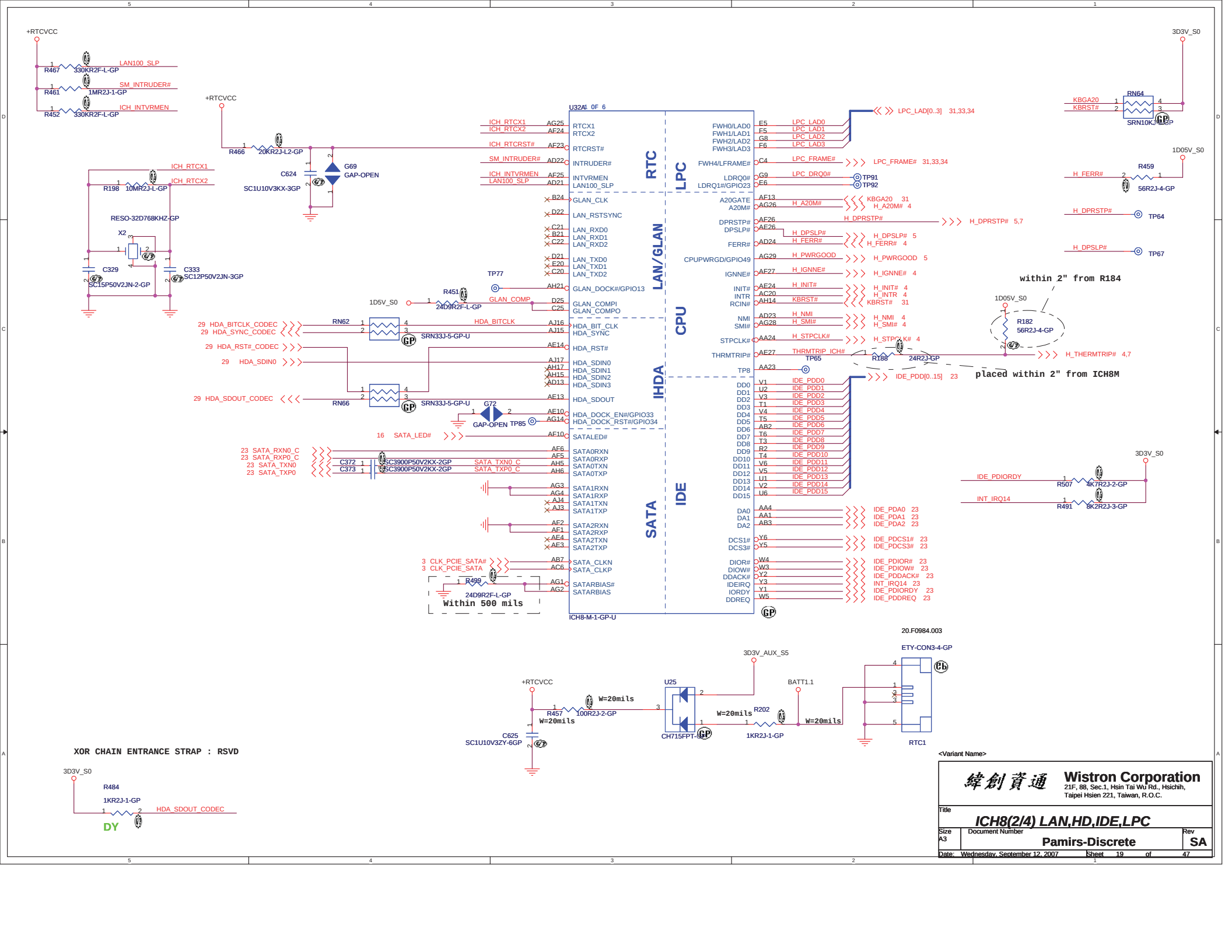
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ICH8(1/4)-PCI/INT	
Size A3	Document Number: Pamirs-Discrete	Rev SA
Date: Wednesday, September 12, 2007	Sheet 18 of 47	



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(2/4) LAN,HD,IDE,LPC

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

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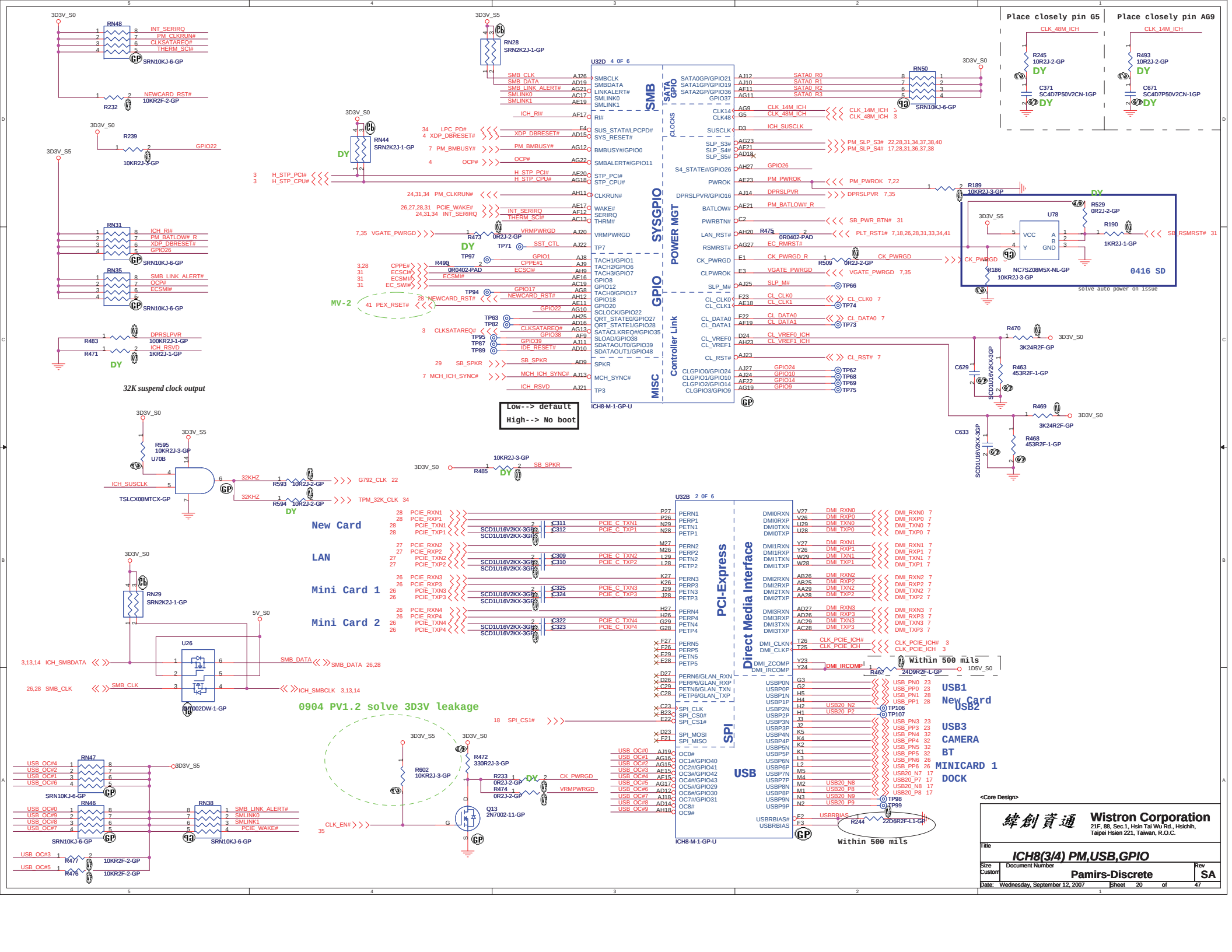
Place closely pin G5
Place closely pin AG9
U32D 4 OF 6
ICH8-M-1-GP-U
U32B 2 OF 6
SMB
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
SATA GPIO
CLOCKS
PCI-Express
Direct Media Interface
SPI
USB
Low--> default
High--> No boot
32K suspend clock output
0904 PV1.2 solve 3D3V leakage
New Card
LAN
Mini Card 1
Mini Card 2
USB1
New Card
USB2
USB3
CAMERA
BT
MINICARD 1
DOCK
0416 SD
solve auto power on issue
Within 500 mils
Within 500 mils
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH8(3/4) PM,USB,GPIO
Pamirs-Discrete
SA
Date: Wednesday, September 12, 2007
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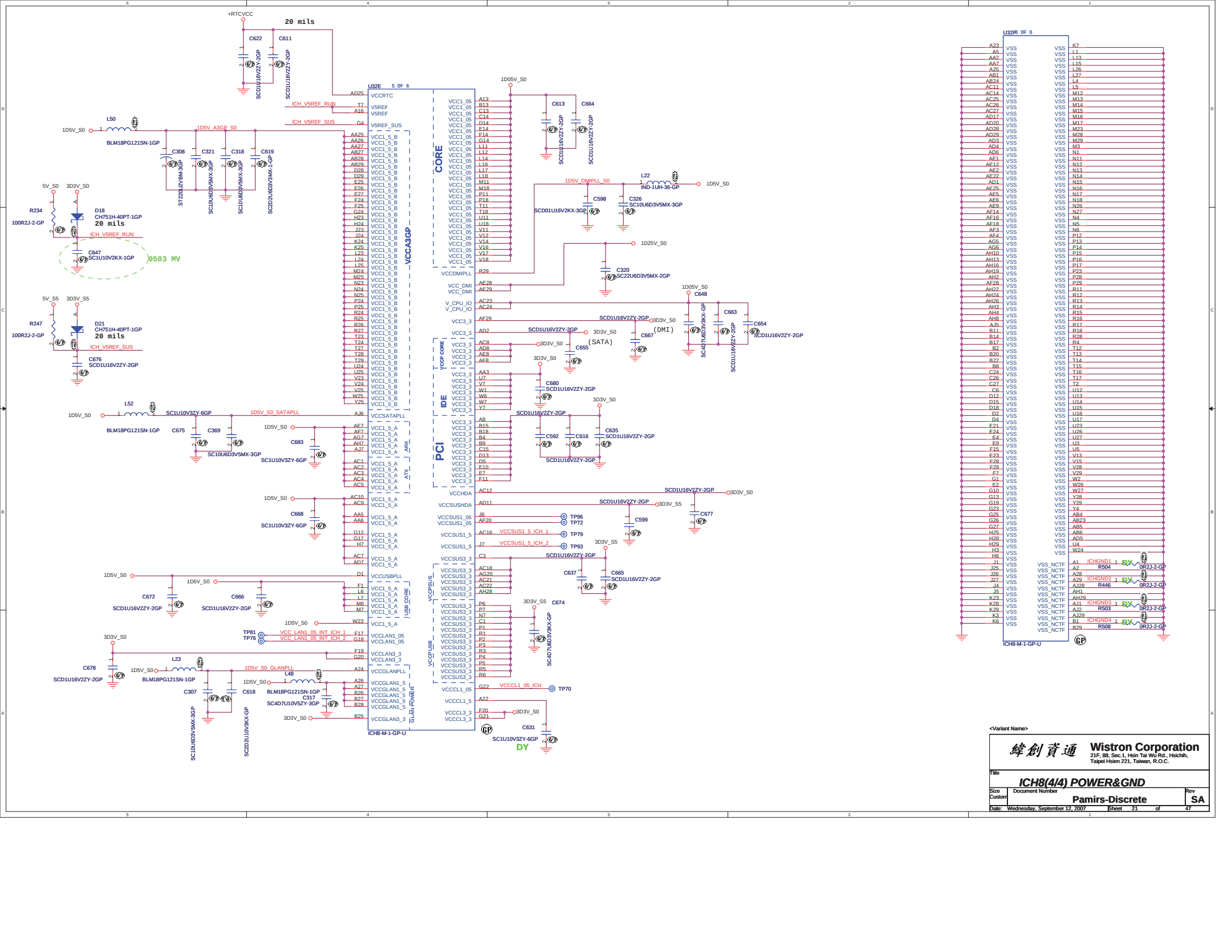
+RTCVCC
20 mils
C622
C611
SCD1U16V2ZY-2GP
U32E 5 OF 6
VCCRTC
VSREF
VSREF_SUS
ICH_V5REF_RUN
ICH_V5REF_SUS
L50
BLM18PG121SN-1GP
1D5V_S0
1D5V_A3GP_S0
C308
C321
C318
C619
ST220U2V6M-3GP
SC10U6D3V5MX-3GP
SC10U6D5V5MX-3GP
SC22U6D3V3MX-1GP
5V_S0
3D3V_S0
R234
100R2J-2-GP
D18
CH751H-40PT-1GP
20 mils
C647
SC1U10V2KX-1GP
0503 MV
5V_S5
3D3V_S5
R247
D21
C676
SCD1U16V2ZY-2GP
L52
SC1U10V3ZY-6GP
1D5V_S0_SATAPLL
C675
C369
C683
C668
C672
C666
C678
L23
1D5V_S0_GLANPLL
L48
C307
C618
C317
SC4D7U10V5ZY-3GP
SC10U6D3V5MX-3GP
SC2D2U10V3KX-GP
TP81
TP76
VCC_LAN1_05_INT_ICH_1
VCC_LAN1_05_INT_ICH_2
CORE
VCCA3GP
IDE
PCI
ATX
ARX
USB CORE
GLAN POWER
VCCP_CORE
VCCPSUS
VCCPUSB
ICH8-M-1-GP-U
1D05V_S0
C613
C664
SCD1U16V2ZY-2GP
L22
IND-1UH-36-GP
1D5V_DMIPLL_S0
C598
SCD01U16V2KX-3GP
C326
SC10U6D3V5MX-3GP
1D25V_S0
C320
SC22U6D3V5MX-2GP
C648
SC4D7U6D3V3KX-GP
C663
C654
SCD1U16V2ZY-2GP
3D3V_S0
(DMI)
(SATA)
C667
C655
C680
C592
C616
C635
SCD1U16V2ZY-2GP
C599
C677
TP96
TP72
TP79
TP93
VCCSUS1_5_ICH_1
VCCSUS1_5_ICH_2
3D3V_S5
C637
C665
C674
SC4D7U6D3V3KX-GP
TP70
VCCCL1_05_ICH
C631
SC1U10V3ZY-6GP
DY
U32F6 0F 6
VSS
VSS_NCTF
ICHGND1
ICHGND2
ICHGND3
ICHGND4
R504
R446
R503
R508
0R2J-2-GP
GP
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8(4/4) POWER&GND
Size
Custom
Document Number
Pamirs-Discrete
Rev
SA
Date: Wednesday, September 12, 2007
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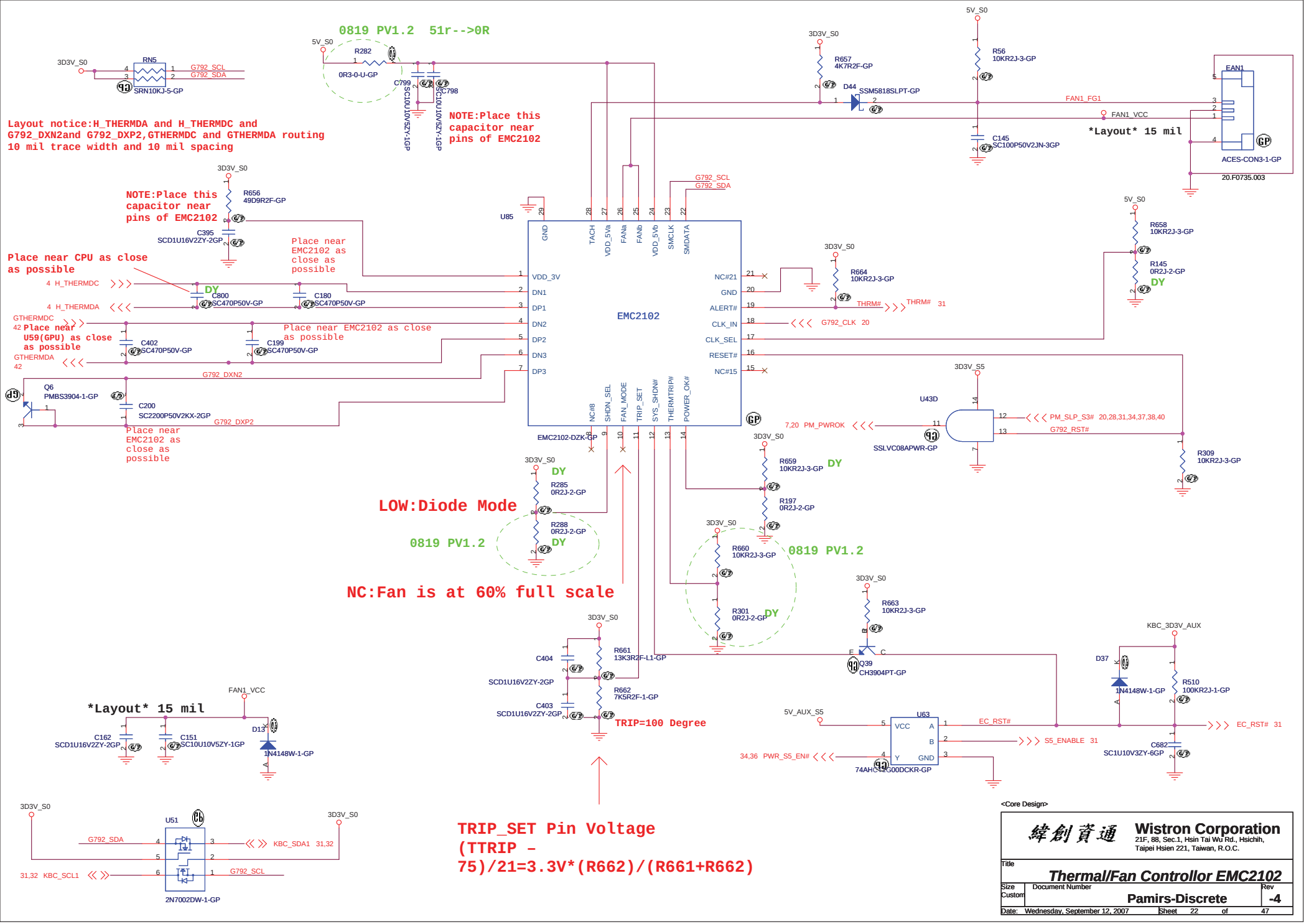

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size	Document Number	Rev
Custom	Pamirs-Discrete	-4

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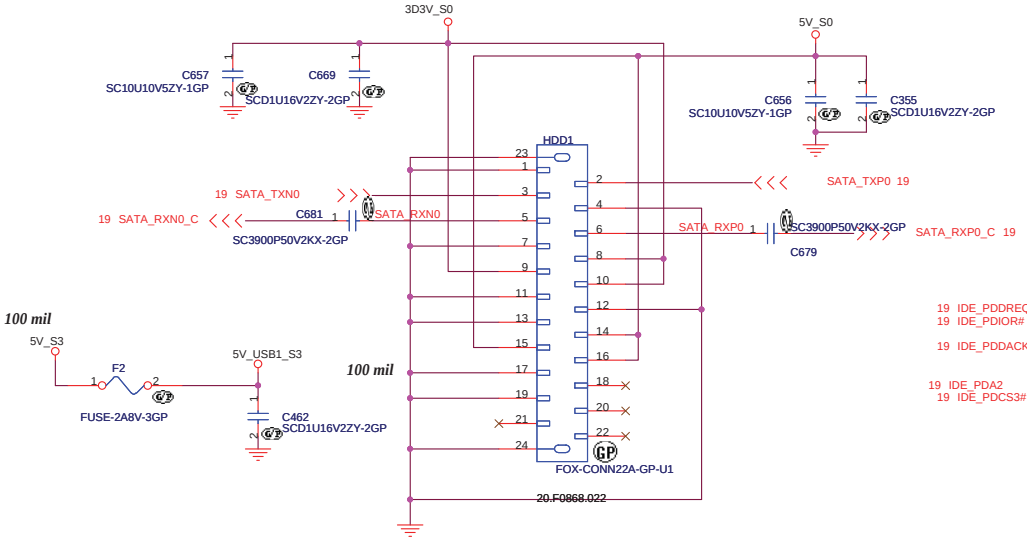
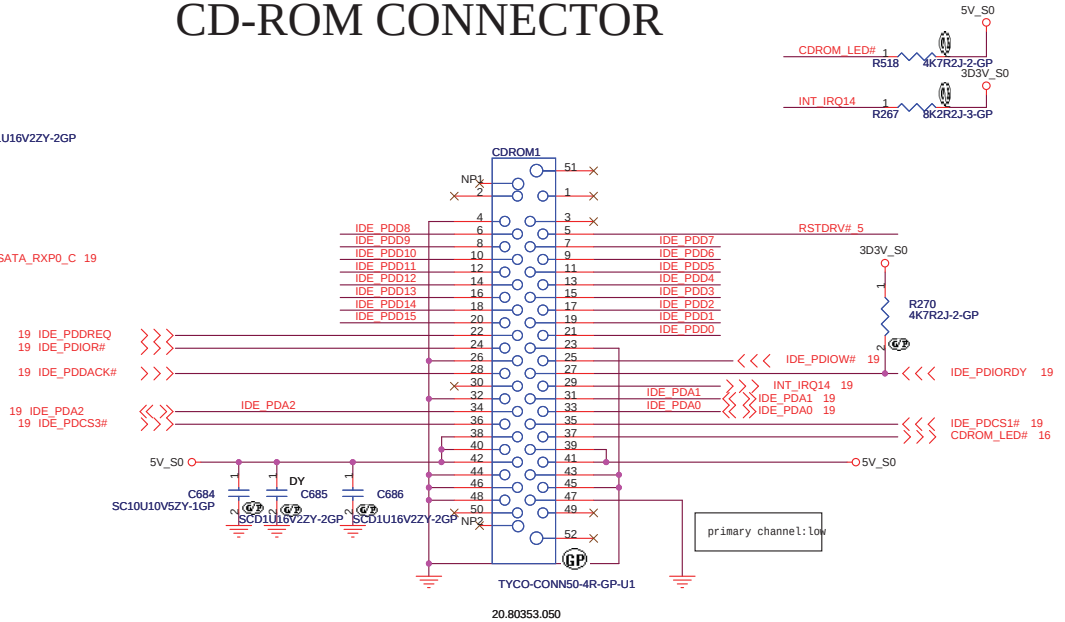
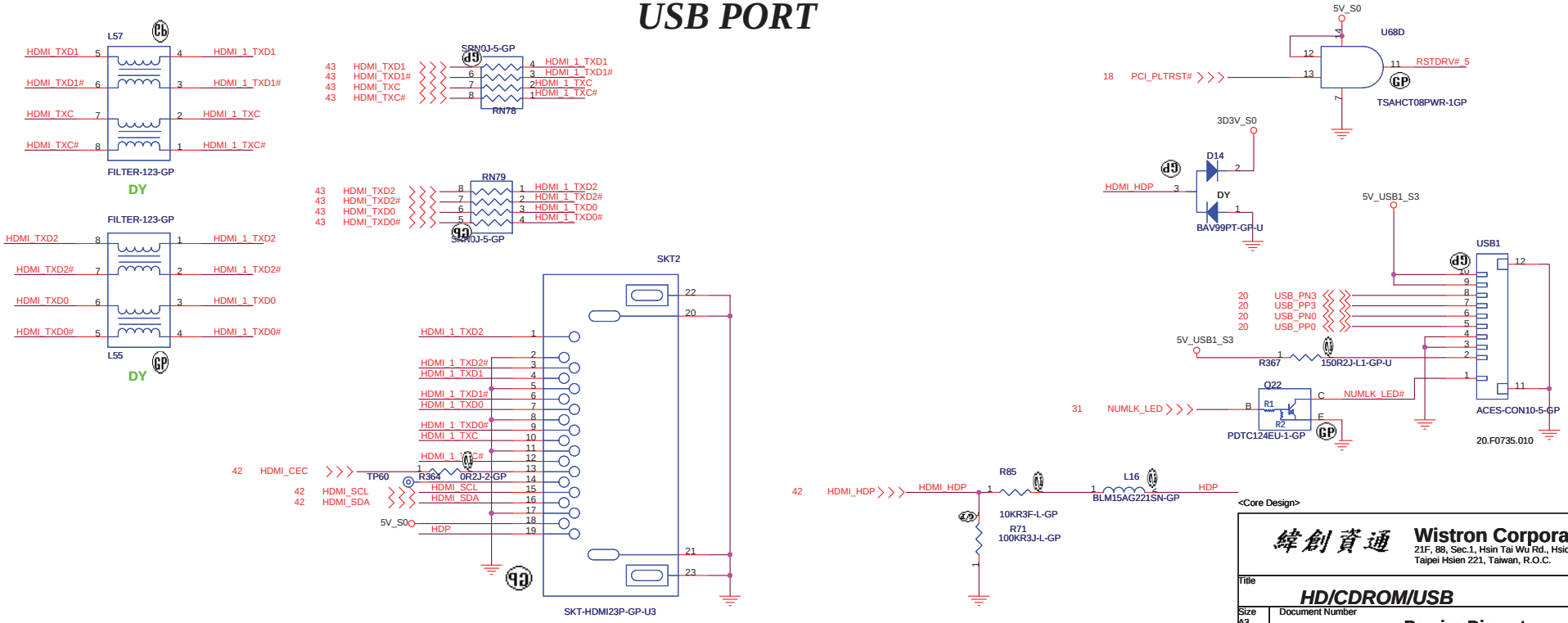
SATA HD Connector



CD-ROM CONNECTOR



USB PORT



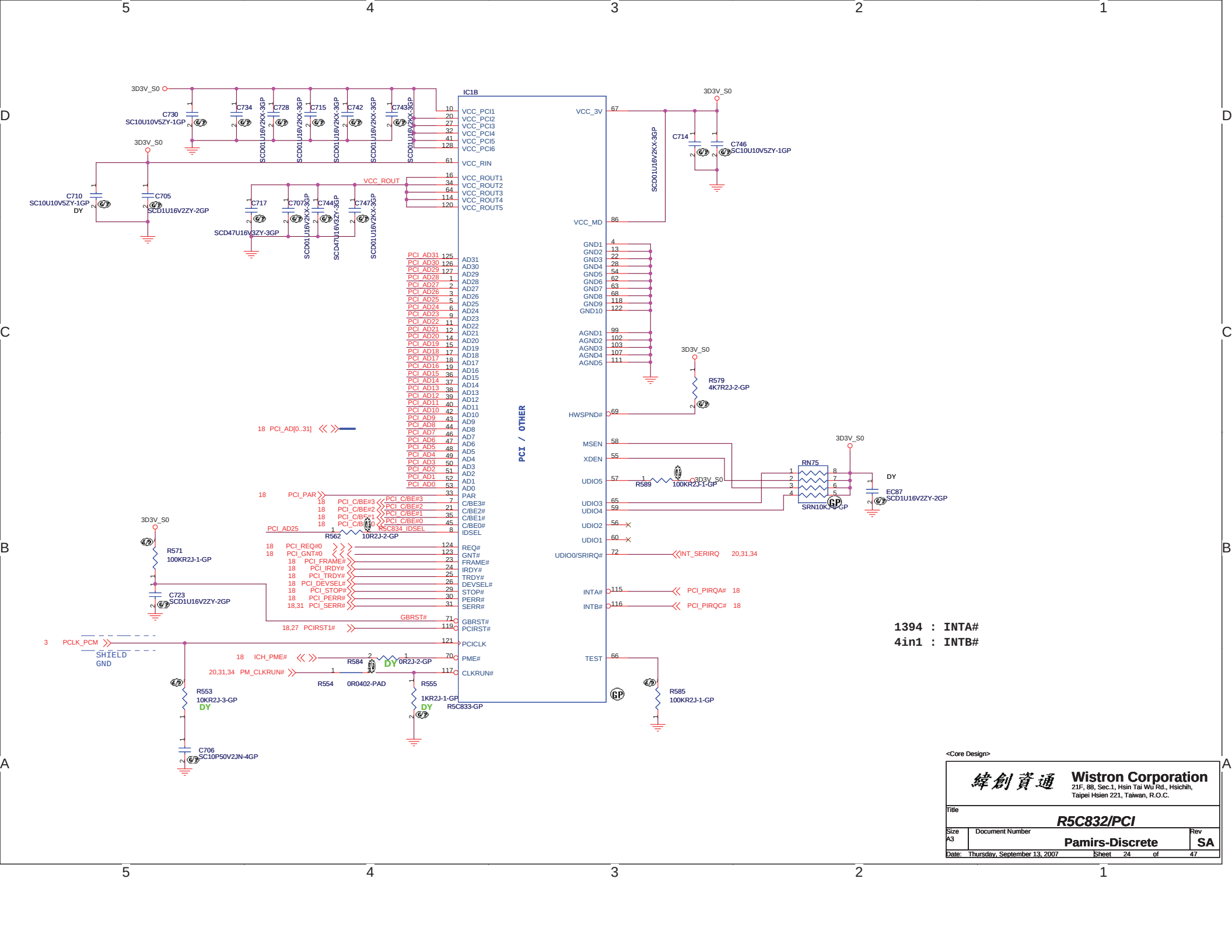
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HD/CDROM/USB**

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Wednesday, September 12, 2007 Sheet 23 of 47



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C832/PCI

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

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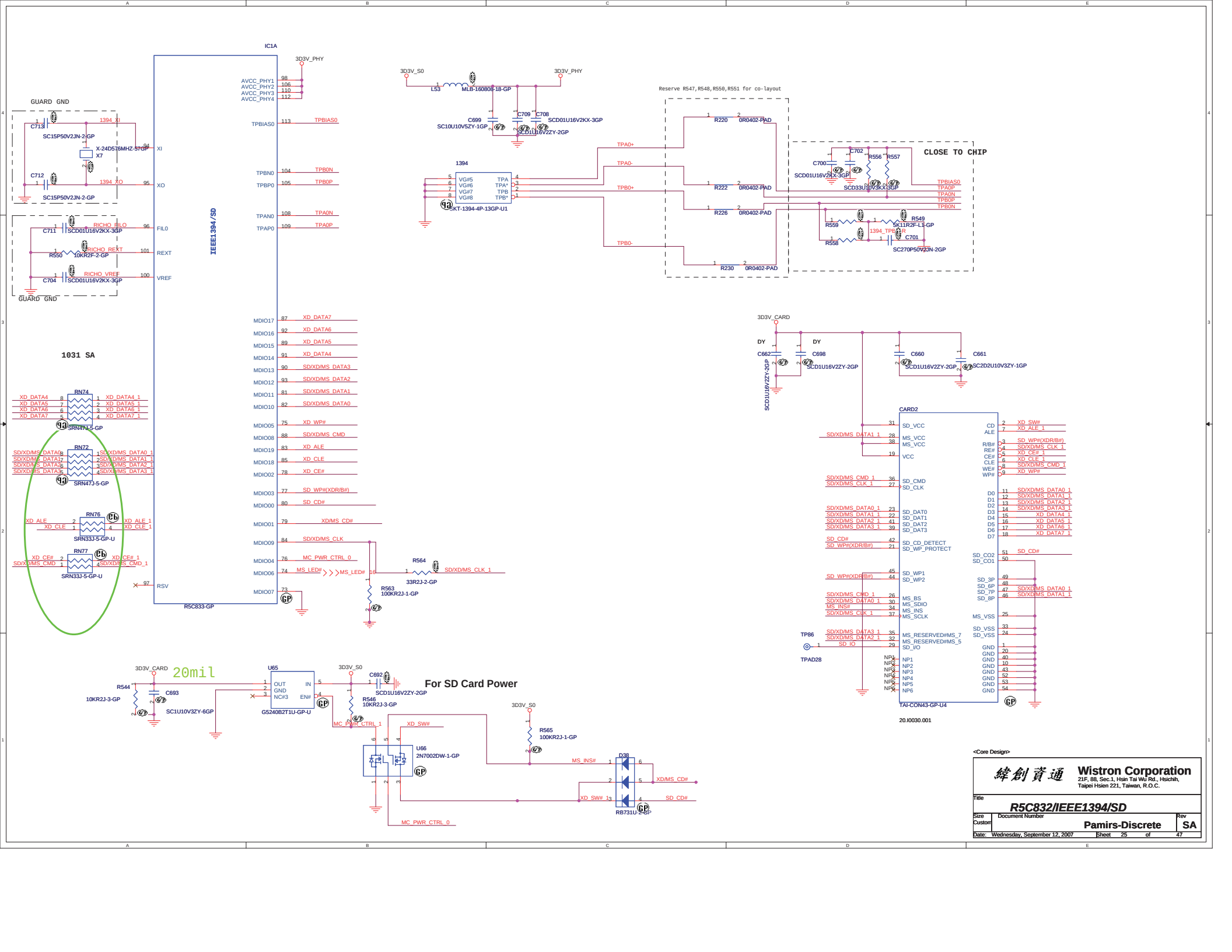
IC1A
R5C833-GP
IEEE1394/SD
1031 SA
GUARD GND
1394
SKT-1394-4P-13GP-U1
Reserve R547,R548,R550,R551 for co-layout
CLOSE TO CHIP
CARD2
TAI-CON43-GP-U4
20.I0030.001
U65
G5240B2T1U-GP-U
U66
2N7002DW-1-GP
D38
RB731U-2-GP
For SD Card Power
20mil
TPAD28
TP86
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
R5C832/IEEE1394/SD
Pamirs-Discrete
SA
Wednesday, September 12, 2007
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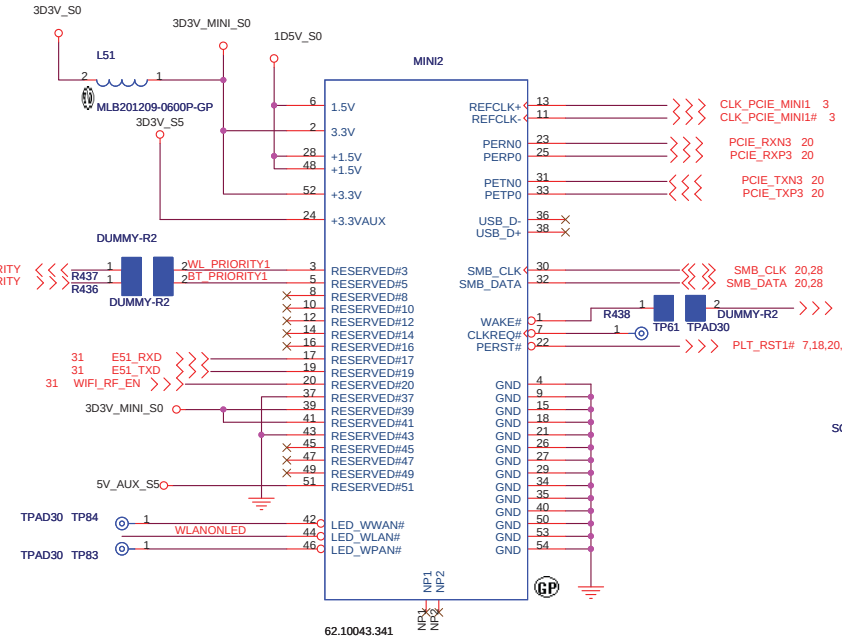
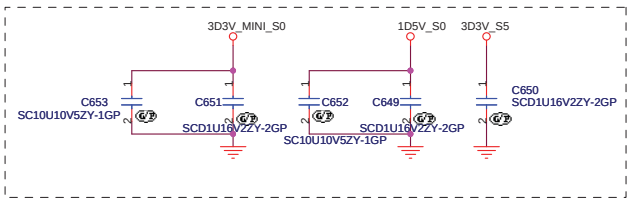
Mini Card Connector 2

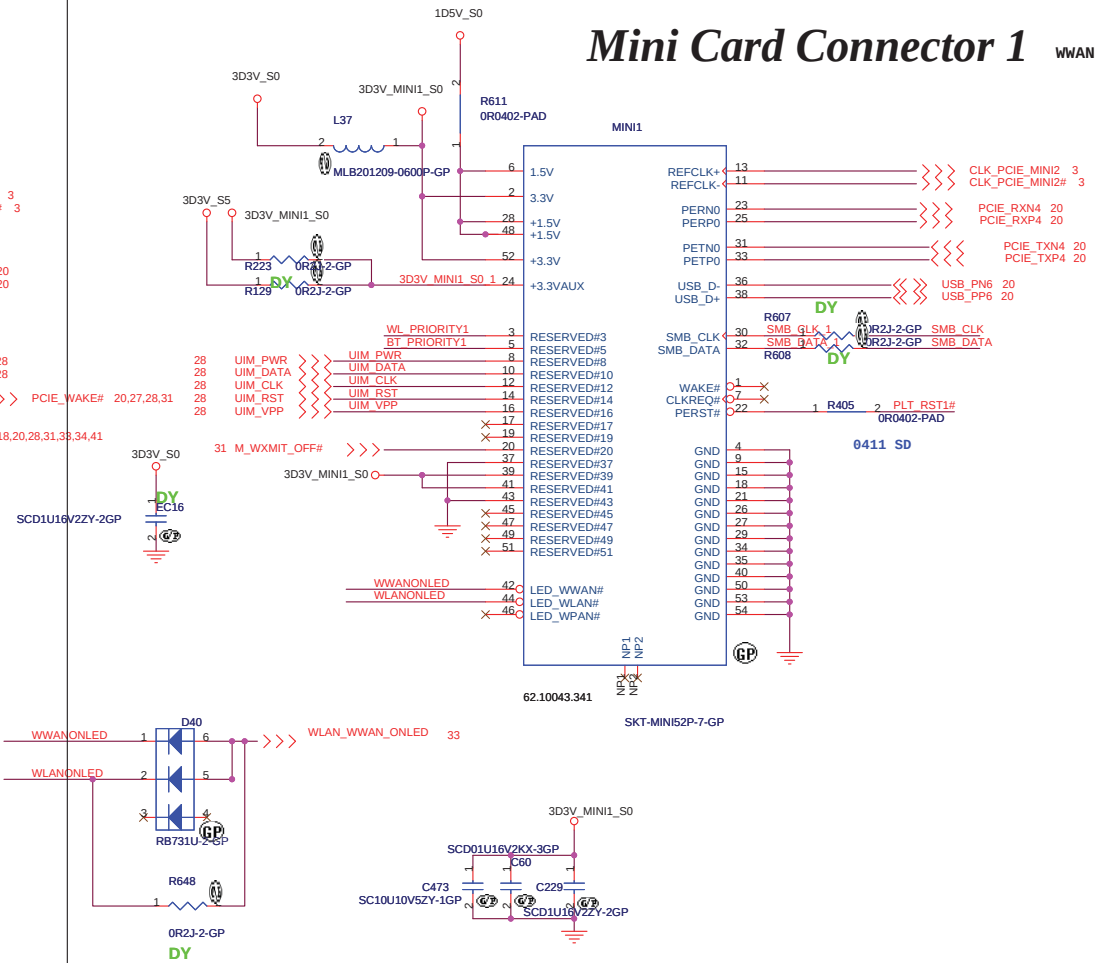
Wireless card





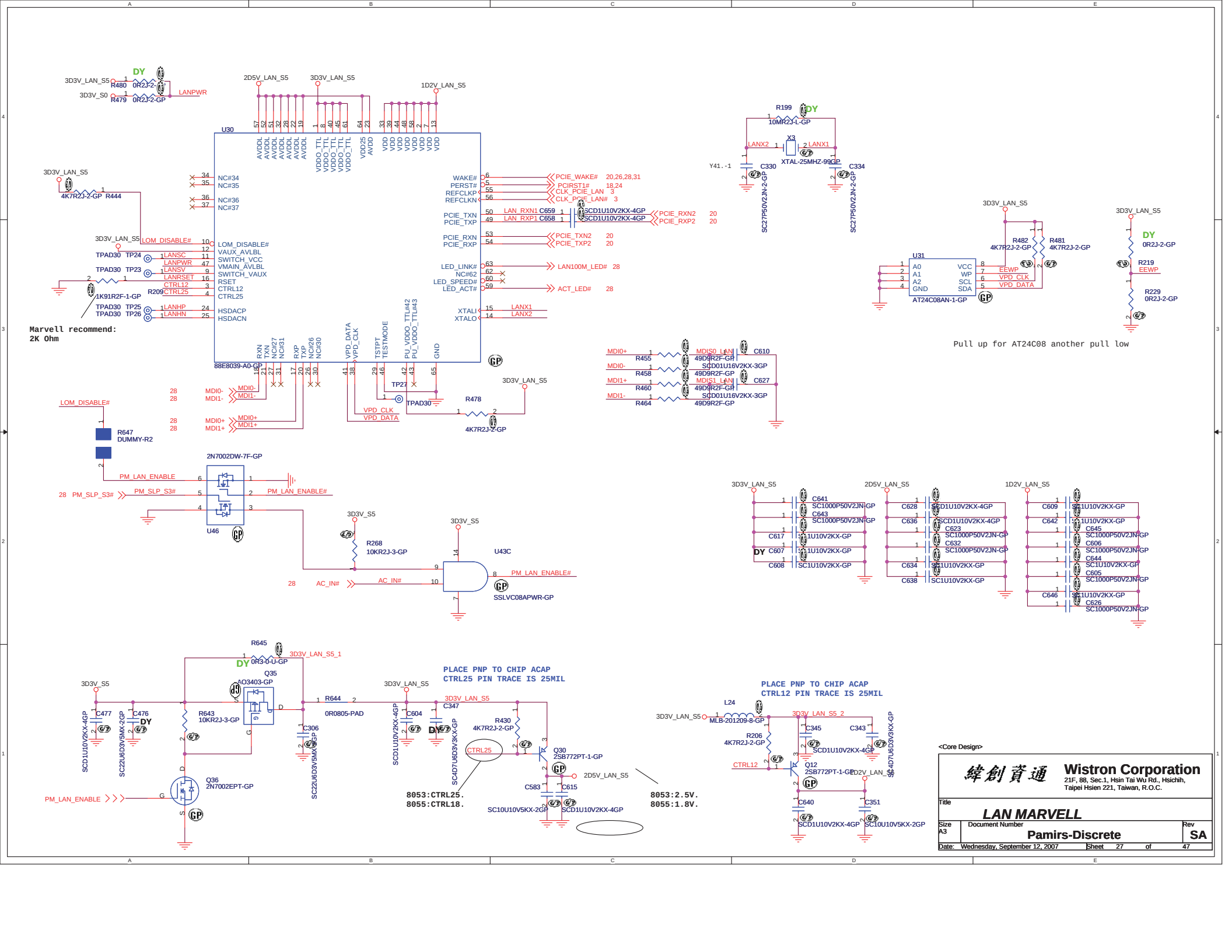
Mini Card Connector 1

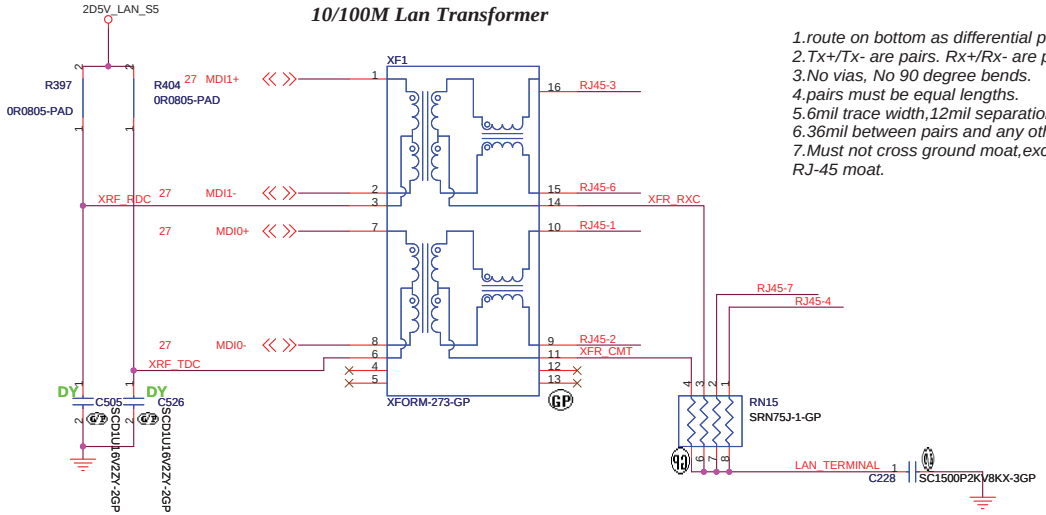
WWAN



<Core Design>

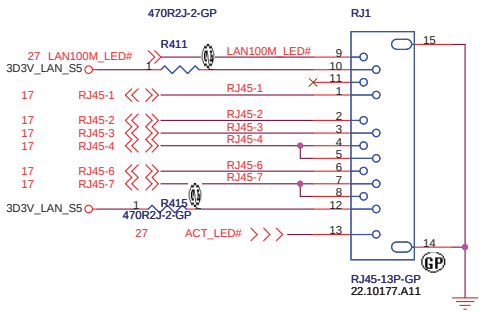
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINI CARD CONN .	
Size A3	Document Number: Pamirs-Discrete	Rev: SA
Date: Wednesday, September 12, 2007	Sheet 26 of 47	


U30
88E8039-A0-GP
Marvell recommend:
2K Ohm
Pull up for AT24C08 another pull low
U31
AT24C08AN-1-GP
U46
2N7002DW-7F-GP
U43C
SSLVC08APWR-GP
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
8053:CTRL25.
8055:CTRL18.
8053:2.5V.
8055:1.8V.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LAN MARVELL
Pamirs-Discrete
SA
Wednesday, September 12, 2007
27
47



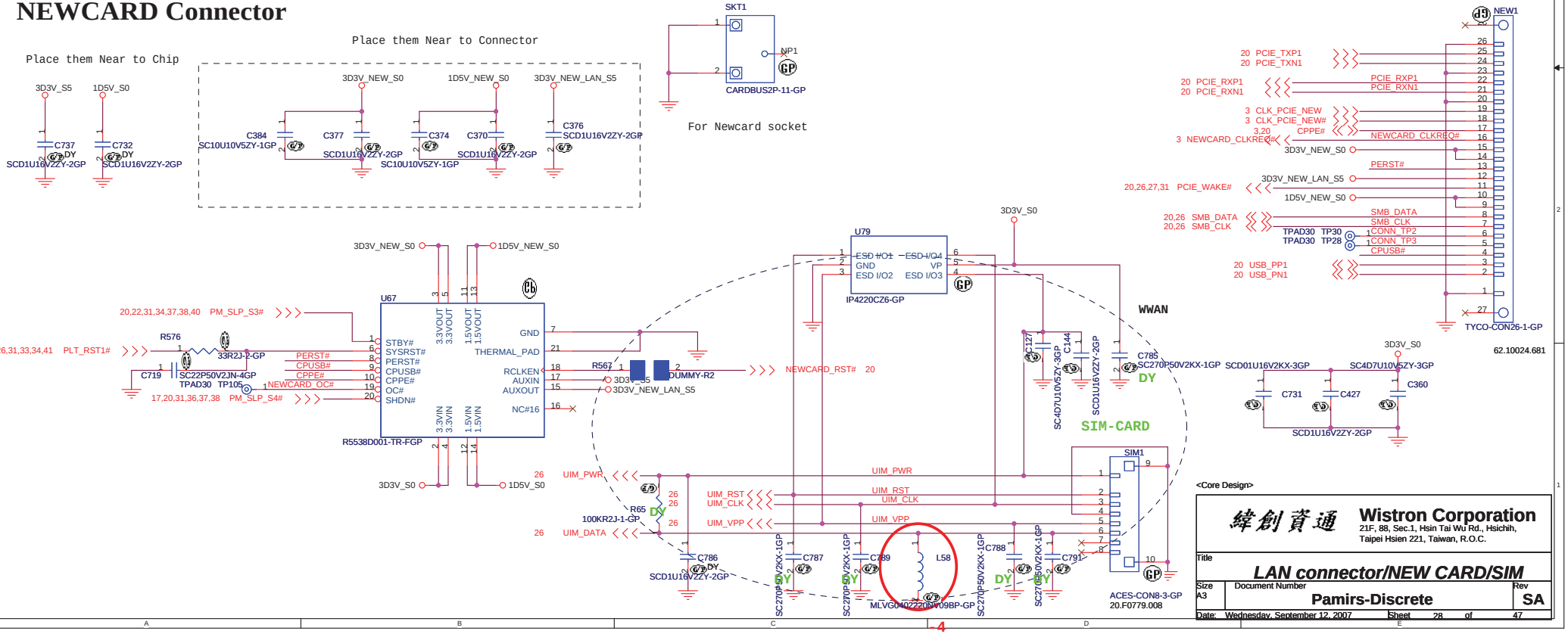
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW



Green : Link up
Blinking : TX/RX activity

NEWCARD Connector



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LAN connector/NEW CARD/SIM***	
Size A3	Document Number **Pamirs-Discrete**	Rev **SA**
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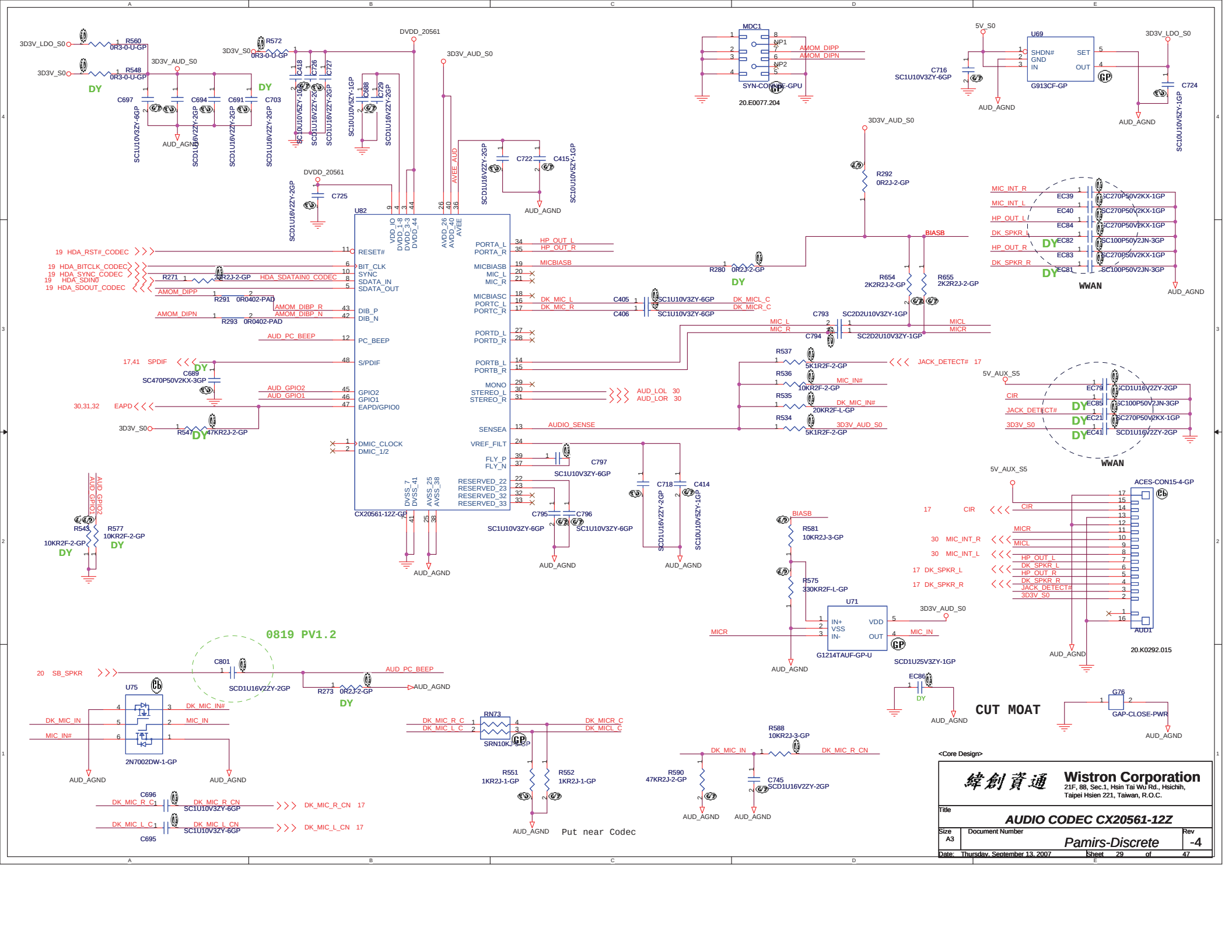
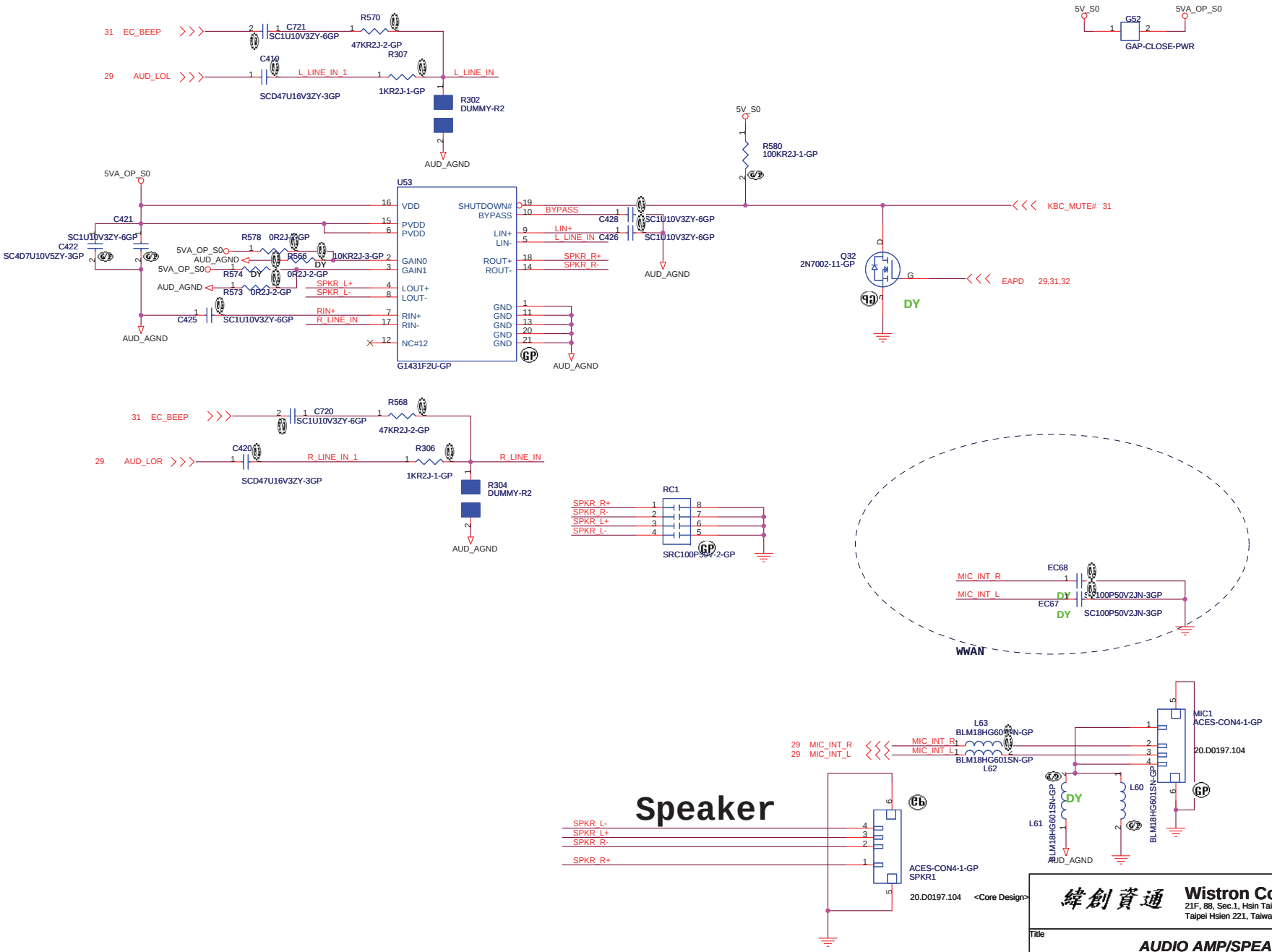
CLOSE TO TRANSFORMER


U82
CX20561-12Z-GP
U75
2N7002DW-1-GP
U71
G1214TAUF-GP-U
MDC1
SYN-CONN-GPU
20.E0077.204
U69
G913CF-GP
ACES-CON15-4-GP
AUD1
20.K0292.015
WWAN
WWAN
0819 PV1.2
CUT MOAT
Put near Codec
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO CODEC CX20561-12Z
Pamirs-Discrete
Size A3
Rev -4
Date: Thursday, September 13, 2007
Sheet 29 of 47

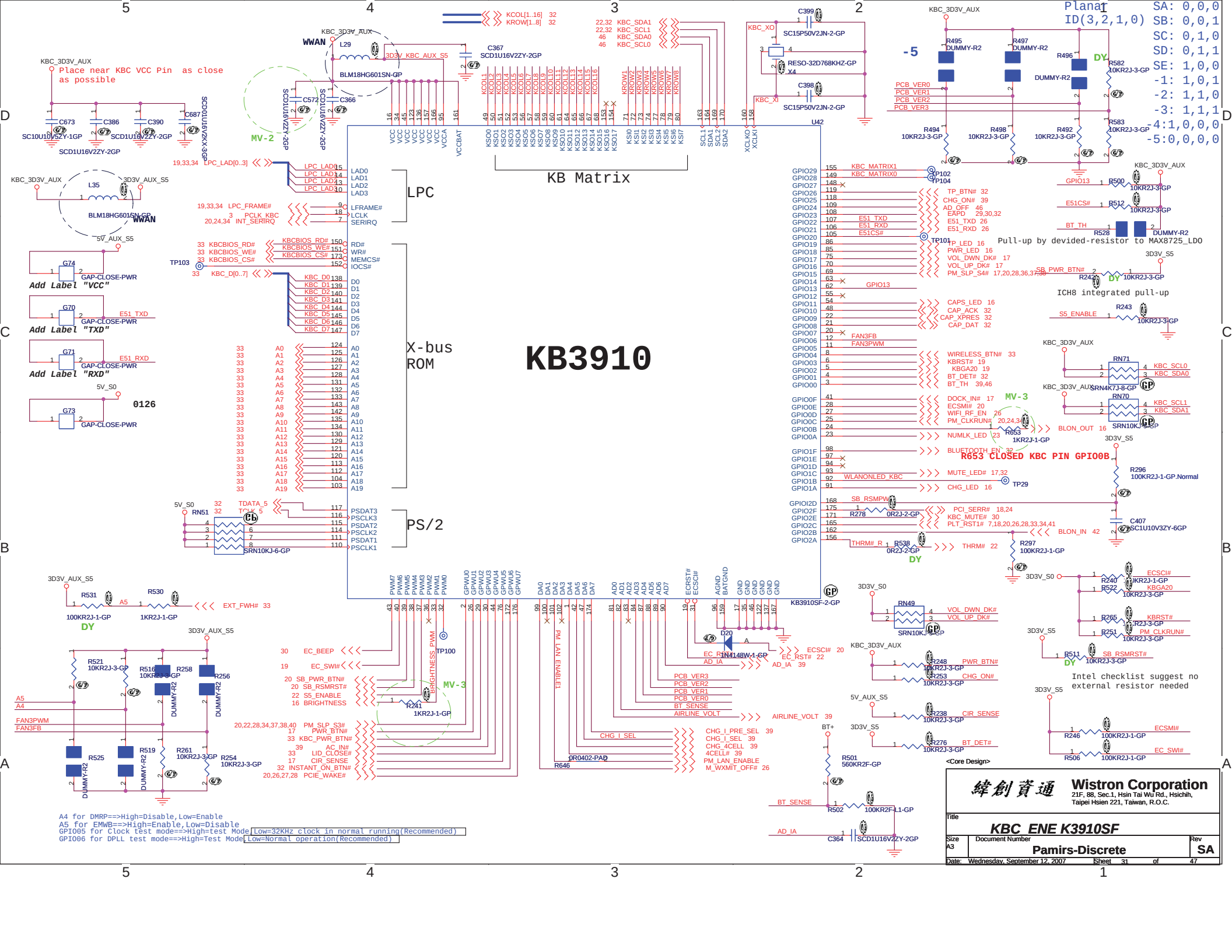


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP/SPEAKER

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Wednesday, September 12, 2007 Sheet 30 of 47


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
U42
KB3910SF-2-GP
Planar ID(3,2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
SE: 1,0,0
-1: 1,0,1
-2: 1,1,0
-3: 1,1,1
-4:1,0,0,0
-5:0,0,0,0
Place near KBC VCC Pin as close as possible
Add Label "VCC"
Add Label "TXD"
Add Label "RXD"
0126
Pull-up by devided-resistor to MAX8725_LDO
ICH8 integrated pull-up
R653 CLOSED KBC PIN GPIO0B
Intel checklist suggest no external resistor needed
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=Test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC_ENE K3910SF
Pamirs-Discrete
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CAMERA

Blue thumb

Internal KeyBoard Connector

31 KROW[1..8]
31 KCOL[1..16]

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

KB1
ETY-CON24-4-GP
20.K0201.024

CAM1
ACES-CON5-1GP
20.D0197.105

BT1
ACES-CON8-4-GP
20.F0772.008

Close to CN8

TouchPad Connector

TPAD1
FOX-CON4-12-GP
20.K0179.004

WWAN

TOUCH-PAD SWITCH

SW1
SW-TACT-68-GP-U1
62.40009.451

CAPACITY BUTTON

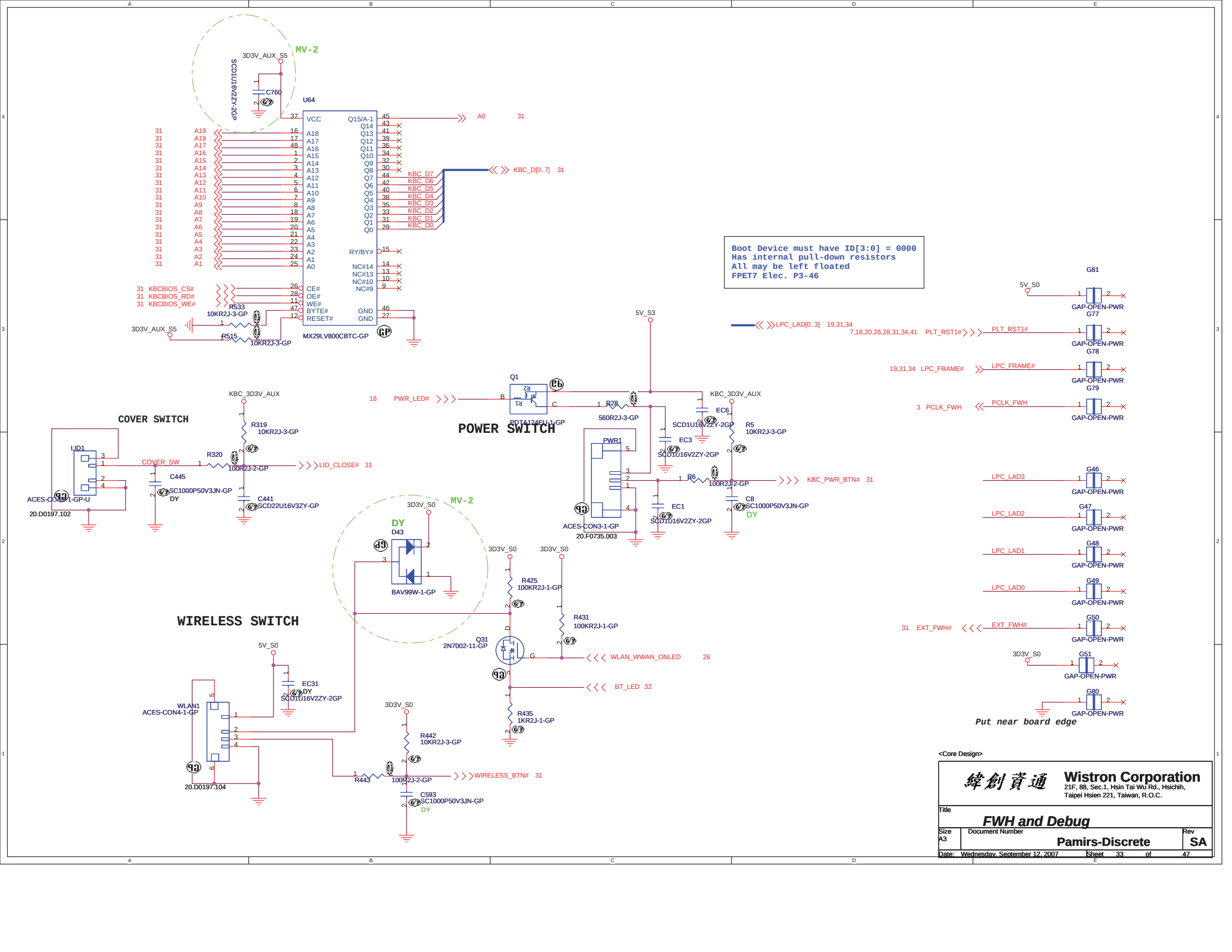
CAP1
ACES-CON12-4-GP
20.K0276.012

for EMI

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KeyBoard-CONN
Size: A3
Document Number: Pamirs-Discrete
Rev: SA
Date: Wednesday, September 12, 2007
Sheet 32 of 47


MV-2
3D3V_AUX_S5
SCD1U16V2ZY-2GP
C760
U64
MX29LV800CBTC-GP
A0 31
KBC_D[0..7] 31
KBC_D7
KBC_D6
KBC_D5
KBC_D4
KBC_D3
KBC_D2
KBC_D1
KBC_D0
31 KBCBIOS_CS#
31 KBCBIOS_RD#
31 KBCBIOS_WE#
R533
10KR2J-3-GP
R515
10KR2J-3-GP
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46
5V_S3
Q1
PDTA124EU-1-GP
16 PWR_LED#
R28
560R2J-3-GP
KBC_3D3V_AUX
EC6
SCD1U16V2ZY-2GP
EC3
SCD1U16V2ZY-2GP
R5
10KR2J-3-GP
PWR1
ACES-CON3-1-GP
20.F0735.003
R6
100R2J-2-GP
KBC_PWR_BTN# 31
EC1
SCD1U16V2ZY-2GP
C8
SC1000P50V3JN-GP
DY
POWER SWITCH
KBC_3D3V_AUX
COVER SWITCH
LID1
ACES-CON4-1-GP-U
20.D0197.102
COVER_SW
R319
10KR2J-3-GP
R320
100R2J-2-GP
LID_CLOSE# 31
C445
SC1000P50V3JN-GP
DY
C441
SCD22U16V3ZY-GP
MV-2
3D3V_S0
DY
D43
BAV99W-1-GP
WIRELESS SWITCH
3D3V_S0
3D3V_S0
R425
100KR2J-1-GP
R431
100KR2J-1-GP
Q31
2N7002-11-GP
WLAN_WWAN_ONLED 26
BT_LED 32
R435
1KR2J-1-GP
5V_S0
EC31
DY
SCD1U16V2ZY-2GP
WLAN1
ACES-CON4-1-GP
20.D0197.104
3D3V_S0
R442
10KR2J-3-GP
R443
100R2J-2-GP
WIRELESS_BTN# 31
C593
SC1000P50V3JN-GP
DY
LPC_LAD[0..3] 19,31,34
7,18,20,26,28,31,34,41 PLT_RST1#
19,31,34 LPC_FRAME#
3 PCLK_FWH
LPC_LAD3
LPC_LAD2
LPC_LAD1
LPC_LAD0
31 EXT_FWH#
5V_S0
3D3V_S0
G81
G77
G78
G79
G46
G47
G48
G49
G50
G51
G80
GAP-OPEN-PWR
Put near board edge
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
FWH and Debug
Size A3
Document Number
Pamirs-Discrete
Rev SA
Date: Wednesday, September 12, 2007
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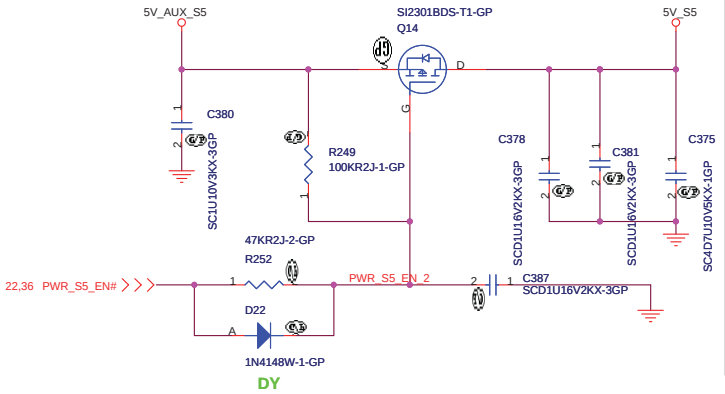
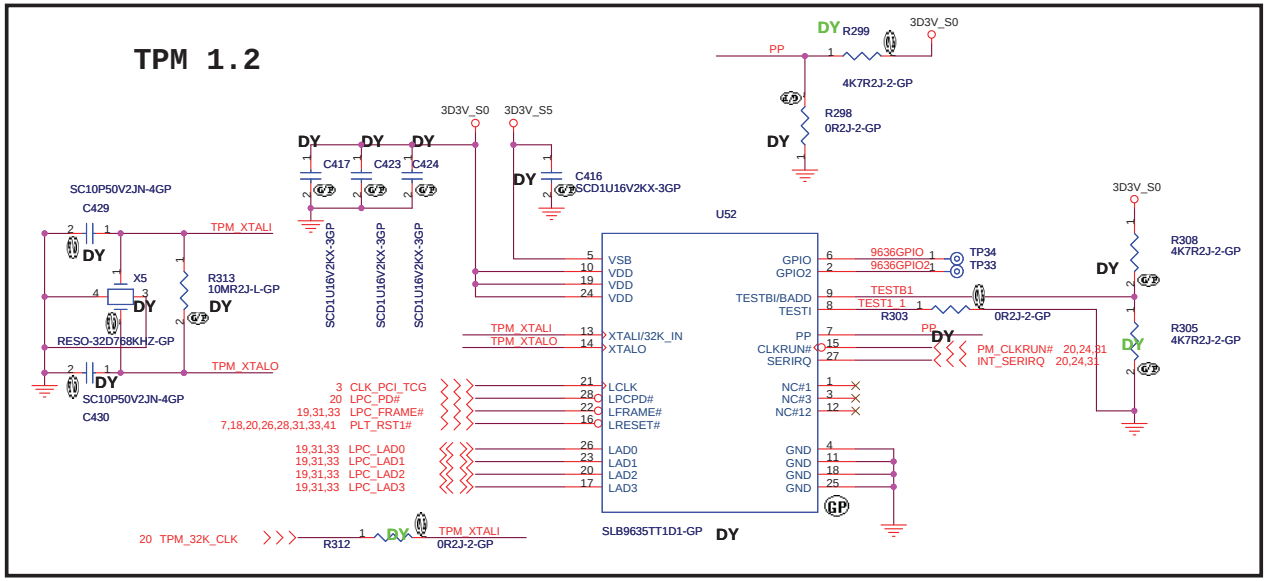
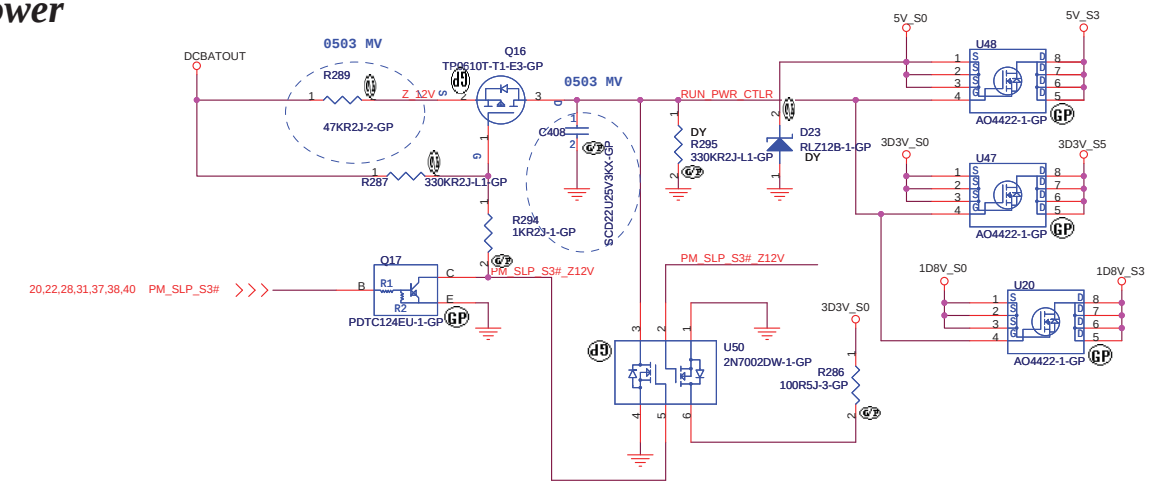
5V_AUX_S5 TO 5V_S5



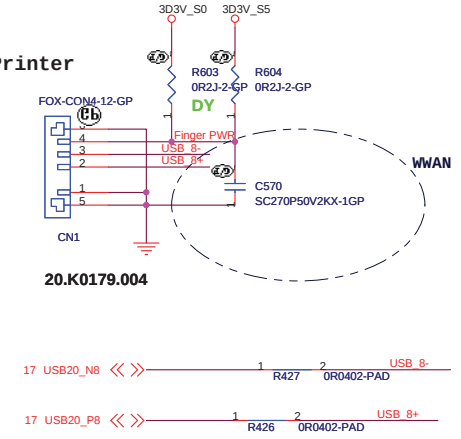
TPM 1.2



Run Power



Finger Printer



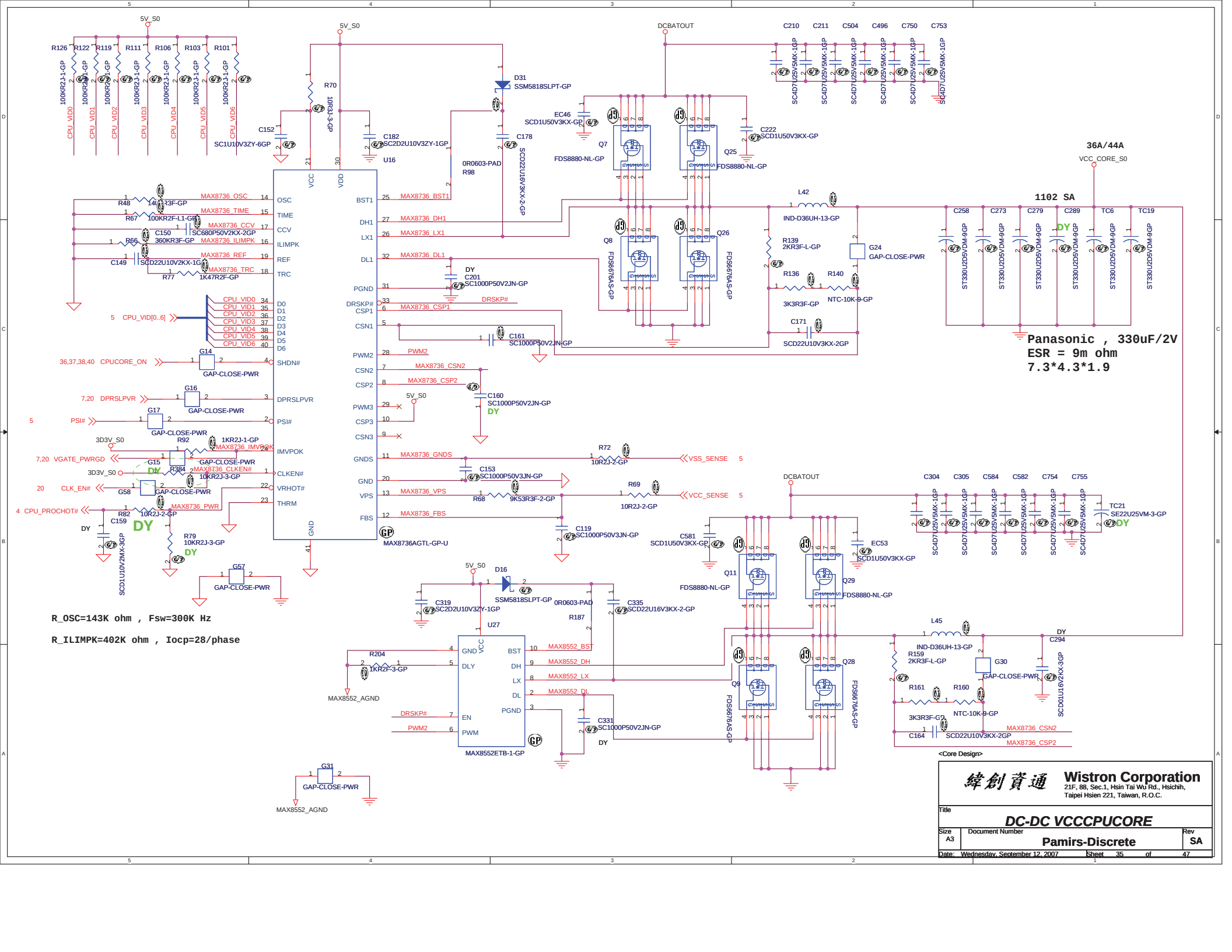
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PWRPLANE&RESETLOGIC**

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Wednesday, September 12, 2007 Sheet 34 of 47


5V_S0
DCBATOUT
MAX8736_OSC
MAX8736_TIME
MAX8736_CCV
MAX8736_ILIMPK
MAX8736_REF
MAX8736_TRC
CPU_VID[0..6]
CPUCORE_ON
DPRSLPVR
PSI#
VGATE_PWRGD
CLK_EN#
CPU_PROCHOT#
MAX8736_PWR
MAX8736_IMVPOK
MAX8736_CLKEN#
MAX8736_BST1
MAX8736_DH1
MAX8736_LX1
MAX8736_DL1
MAX8736_CSP1
MAX8736_CSN2
MAX8736_CSP2
MAX8736_GNDS
MAX8736_VPS
MAX8736_FBS
PWM2
DRSKP#
VSS_SENSE
VCC_SENSE
MAX8736AGTL-GP-U
MAX8552_BST
MAX8552_DH
MAX8552_LX
MAX8552_DL
MAX8552_AGND
MAX8552ETB-1-GP
36A/44A
VCC_CORE_S0
1102 SA
Panasonic , 330uF/2V
ESR = 9m ohm
7.3*4.3*1.9
R_OSC=143K ohm , Fsw=300K Hz
R_ILIMPK=402K ohm , Iocp=28/phase
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC-DC VCCCPUCORE
Size A3
Document Number
Pamirs-Discrete
Rev SA
Date: Wednesday, September 12, 2007
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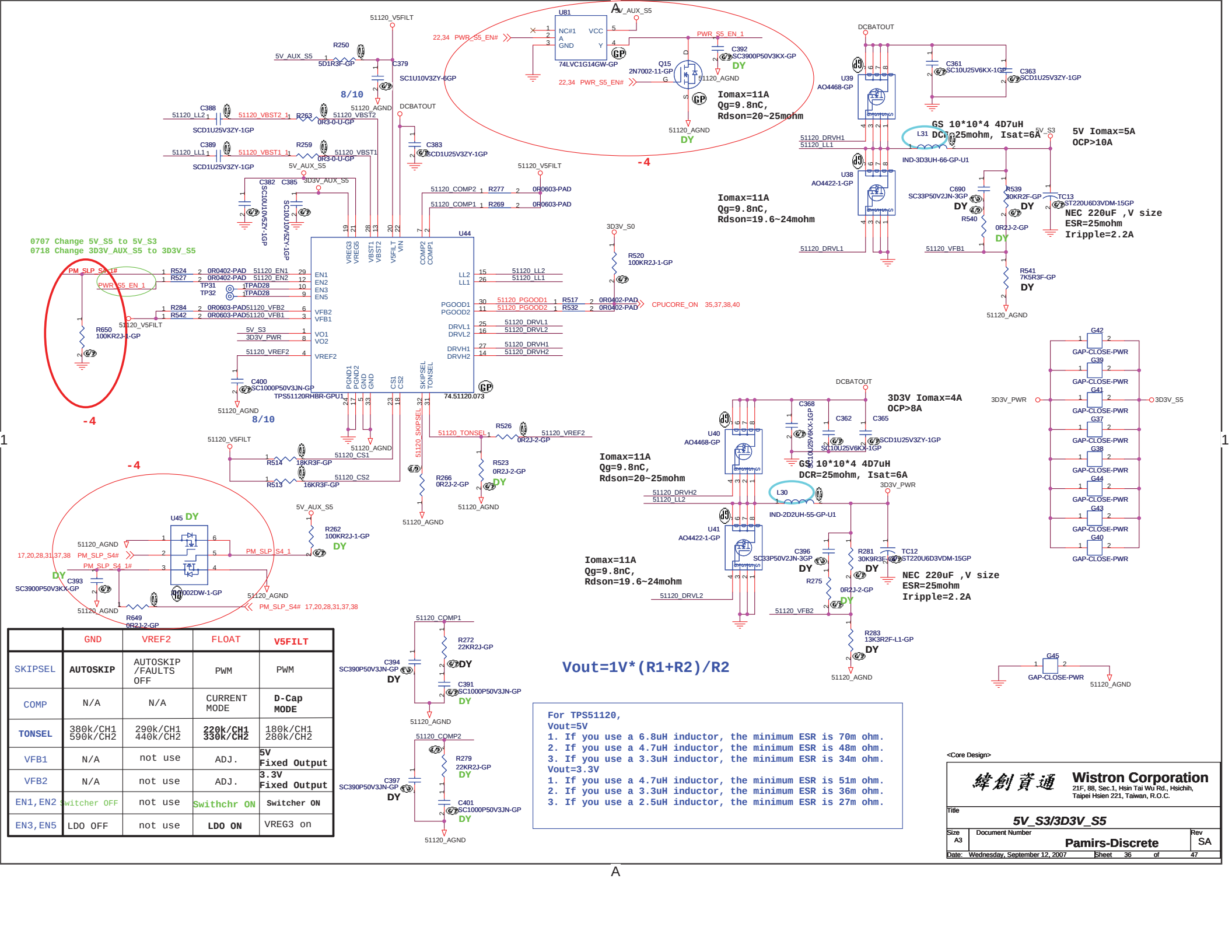


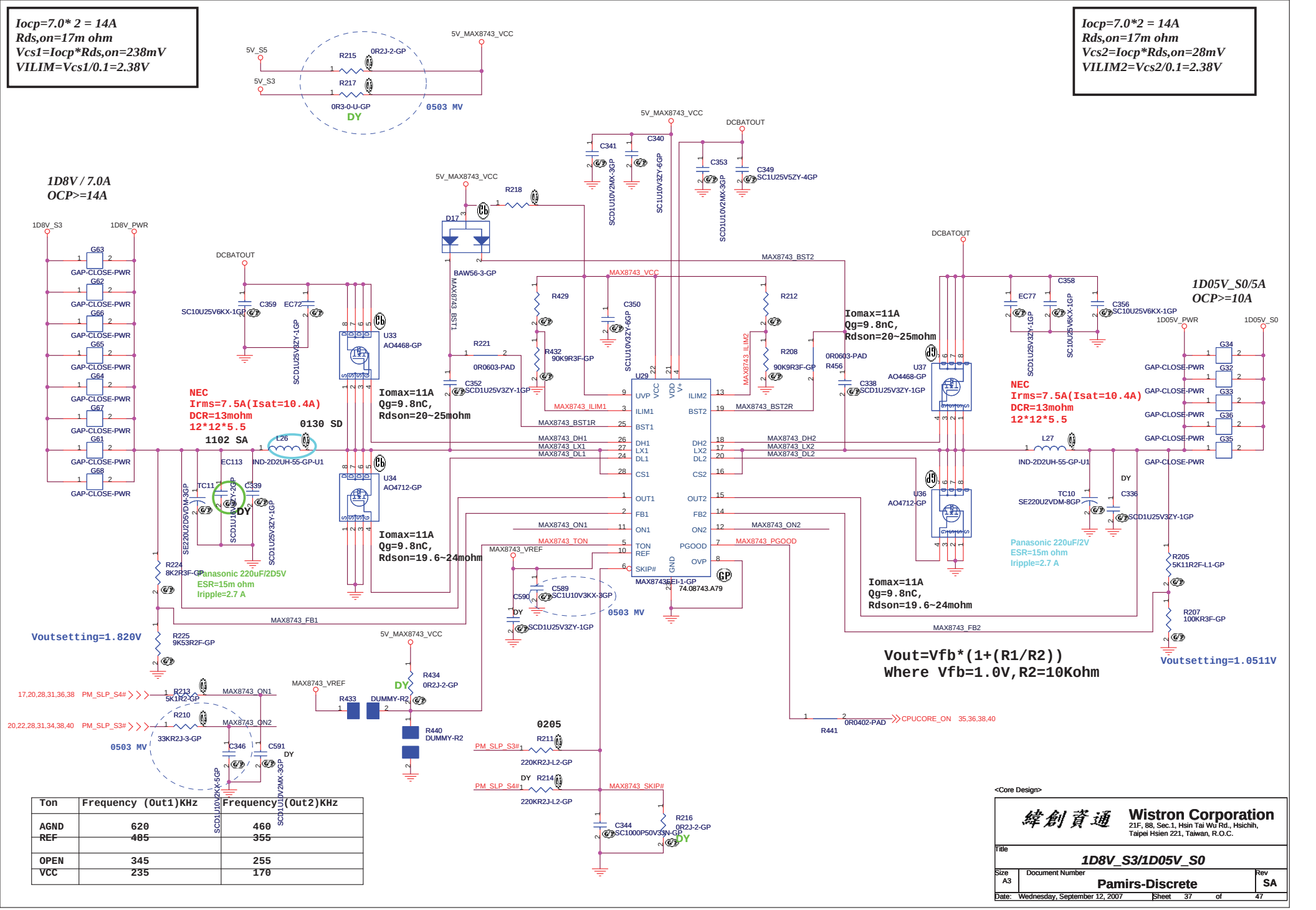
	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V_S3/3D3V_S5

Size: A3 | Document Number: Pamirs-Discrete | Rev: SA

Date: Wednesday, September 12, 2007 | Sheet 36 of 47



Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D8V_S3/1D05V_S0

Size: A3 | Document Number: Pamirs-Discrete | Rev: SA

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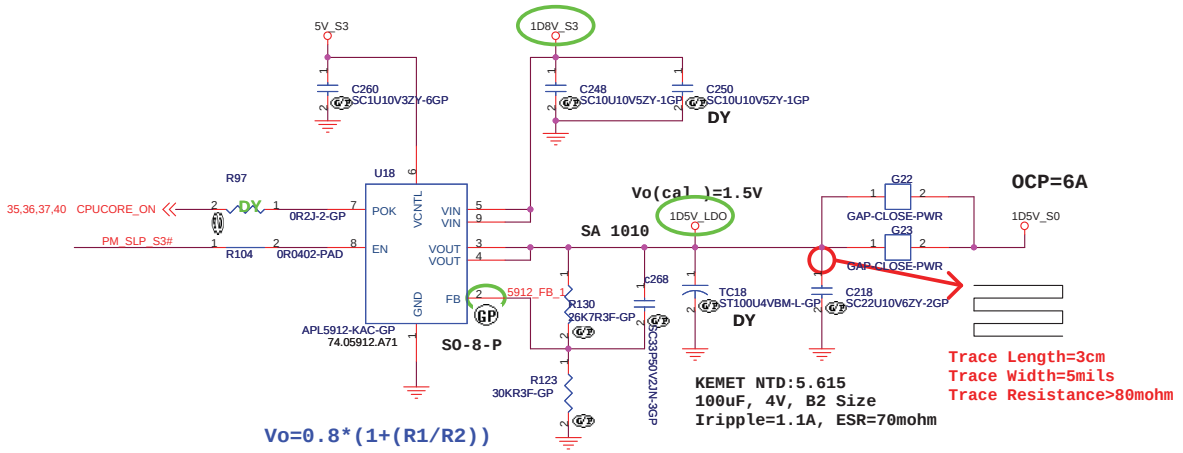

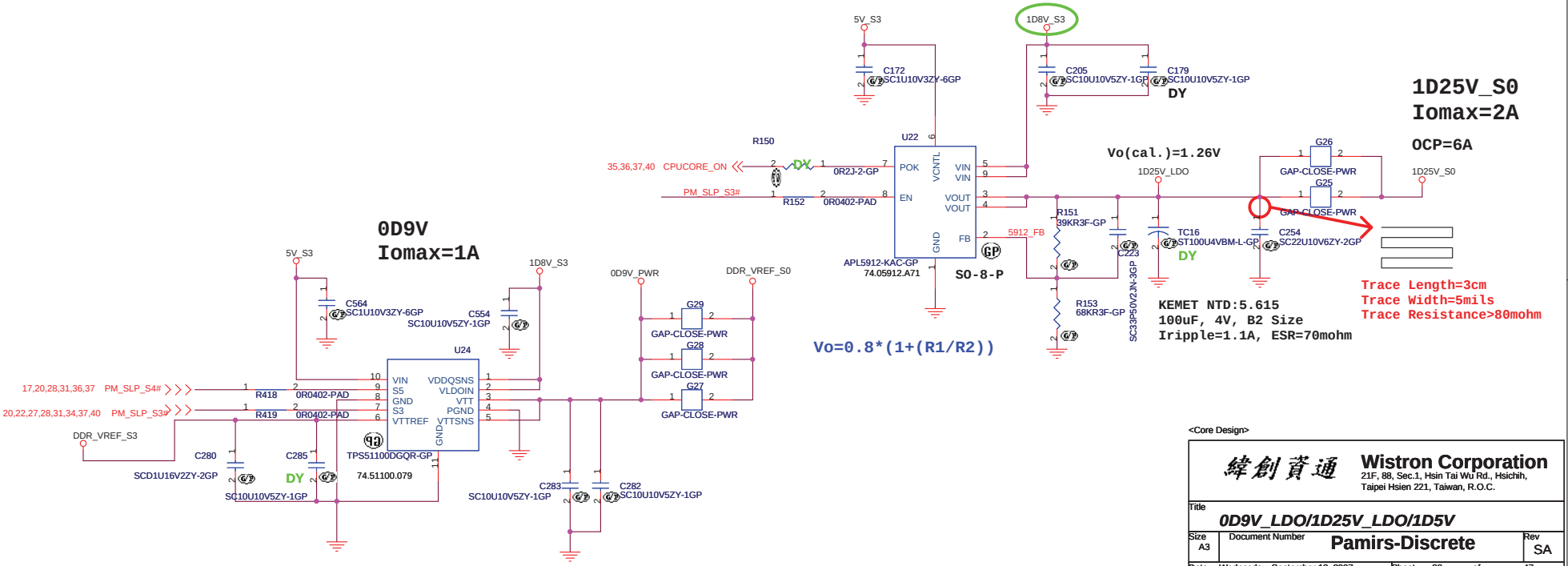

<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	0D9V_LDO/1D25V_LDO/1D5V	
Size A3	Document Number Pamirs-Discrete	Rev SA
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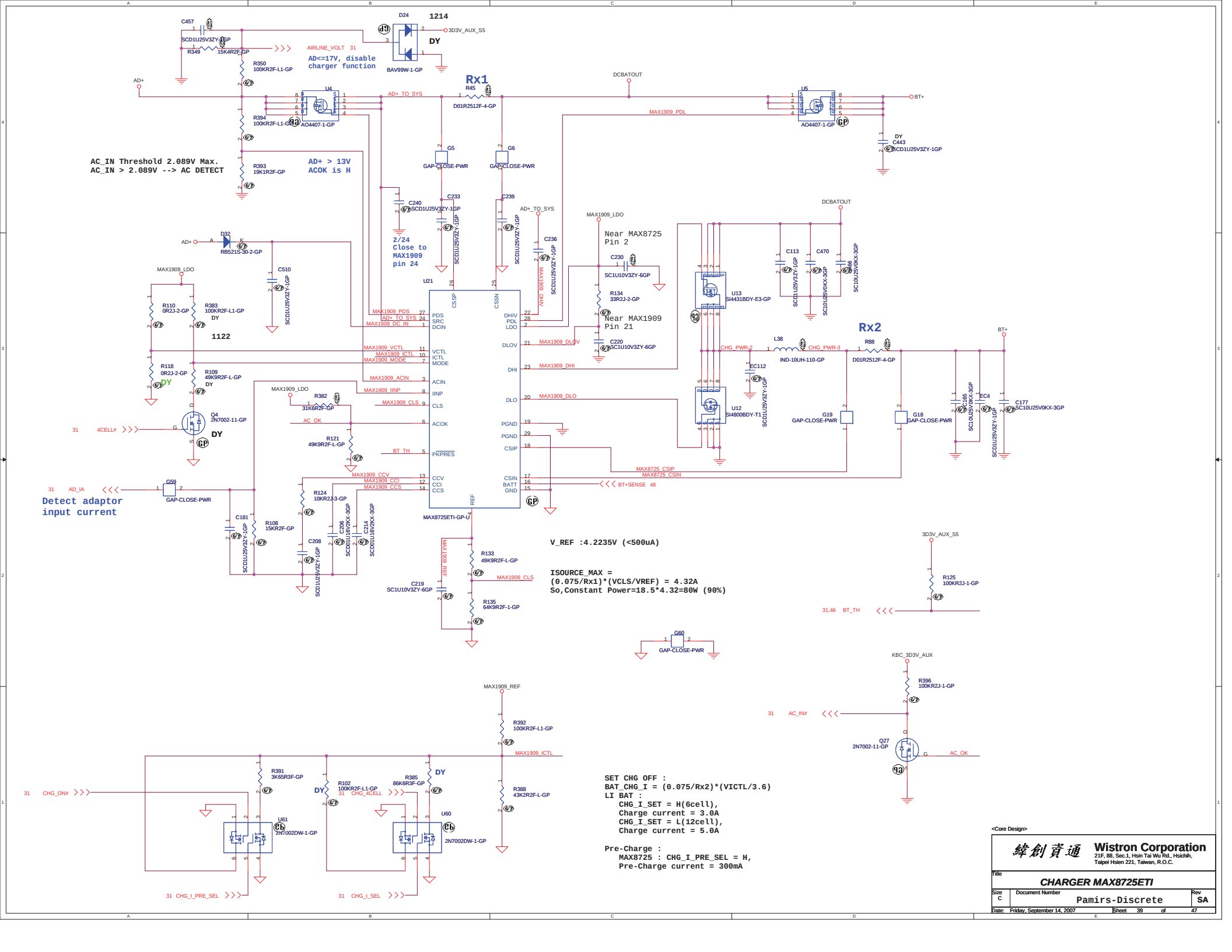
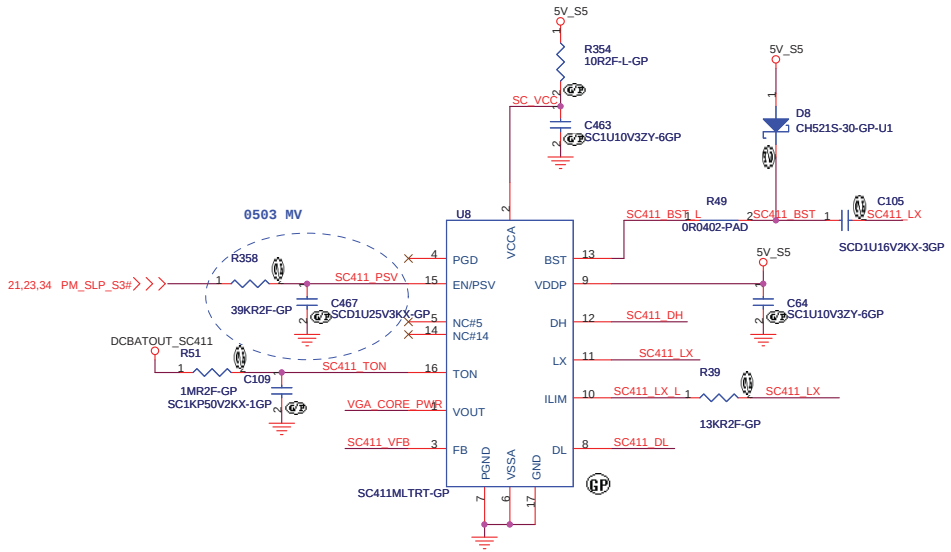
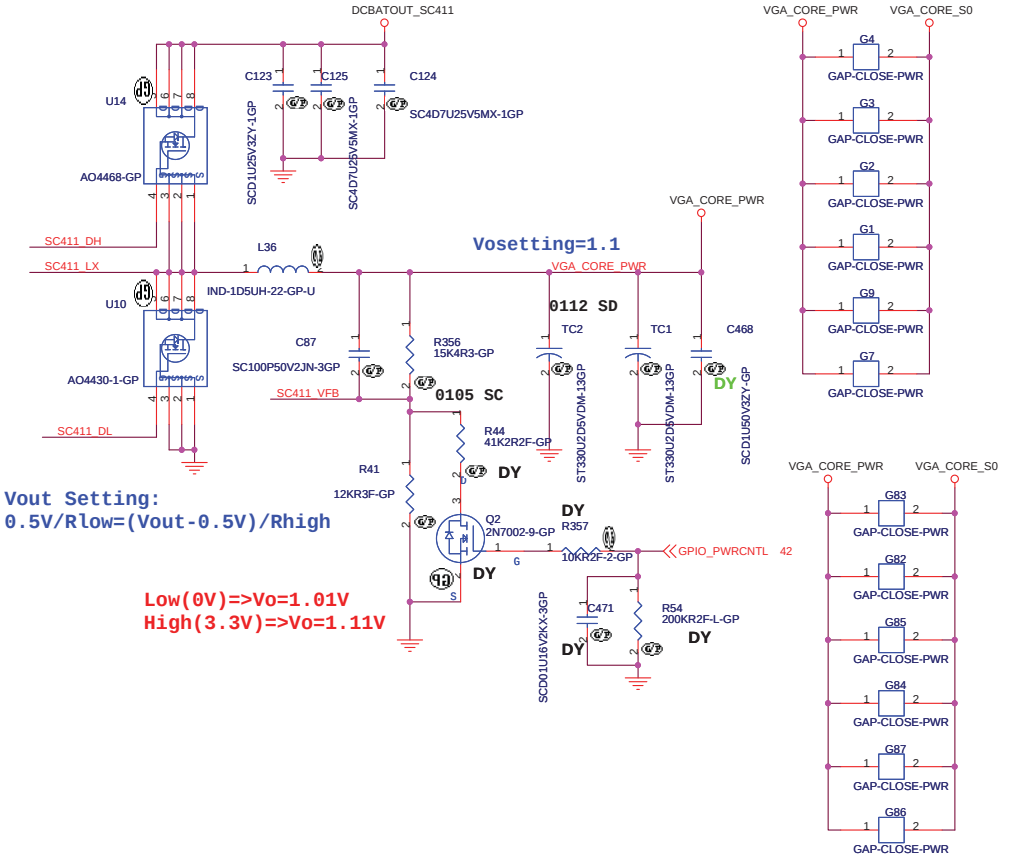
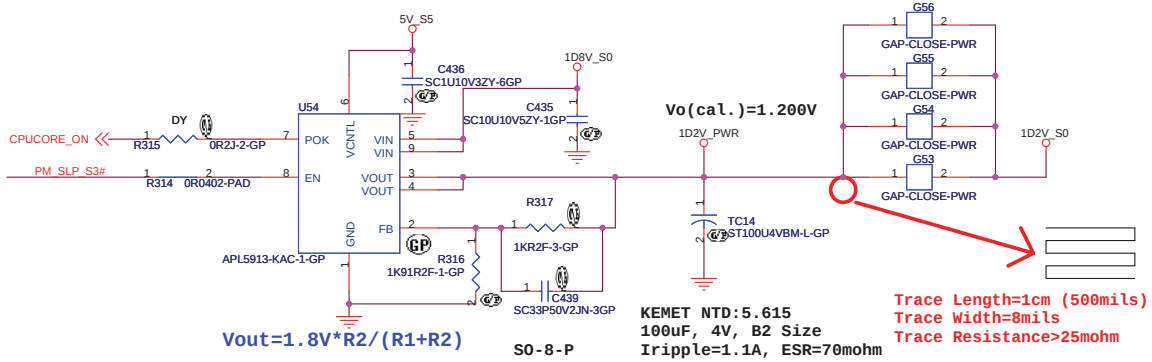
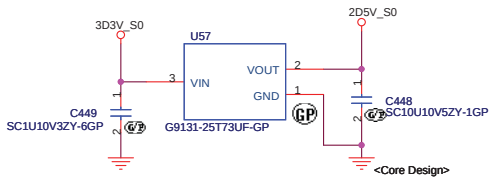
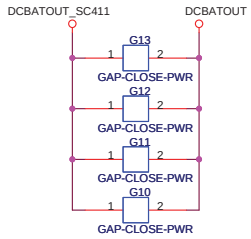

AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
AD+ > 13V
ACOK is H
AD<=17V, disable charger function
Rx1
Rx2
2/24
Close to MAX1909 pin 24
Near MAX8725 Pin 2
Near MAX1909 Pin 21
1214
1122
Detect adaptor input current
V_REF :4.2235V (<500uA)
ISOURCE_MAX =
(0.075/Rx1)*(VCLS/VREF) = 4.32A
So,Constant Power=18.5*4.32=80W (90%)
SET CHG OFF :
BAT_CHG_I = (0.075/Rx2)*(VICTL/3.6)
LI BAT :
CHG_I_SET = H(6cell),
Charge current = 3.0A
CHG_I_SET = L(12cell),
Charge current = 5.0A
Pre-Charge :
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 300mA
MAX8725ETI-GP-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8725ETI
Pamirs-Discrete
Friday, September 14, 2007
Sheet 39 of 47





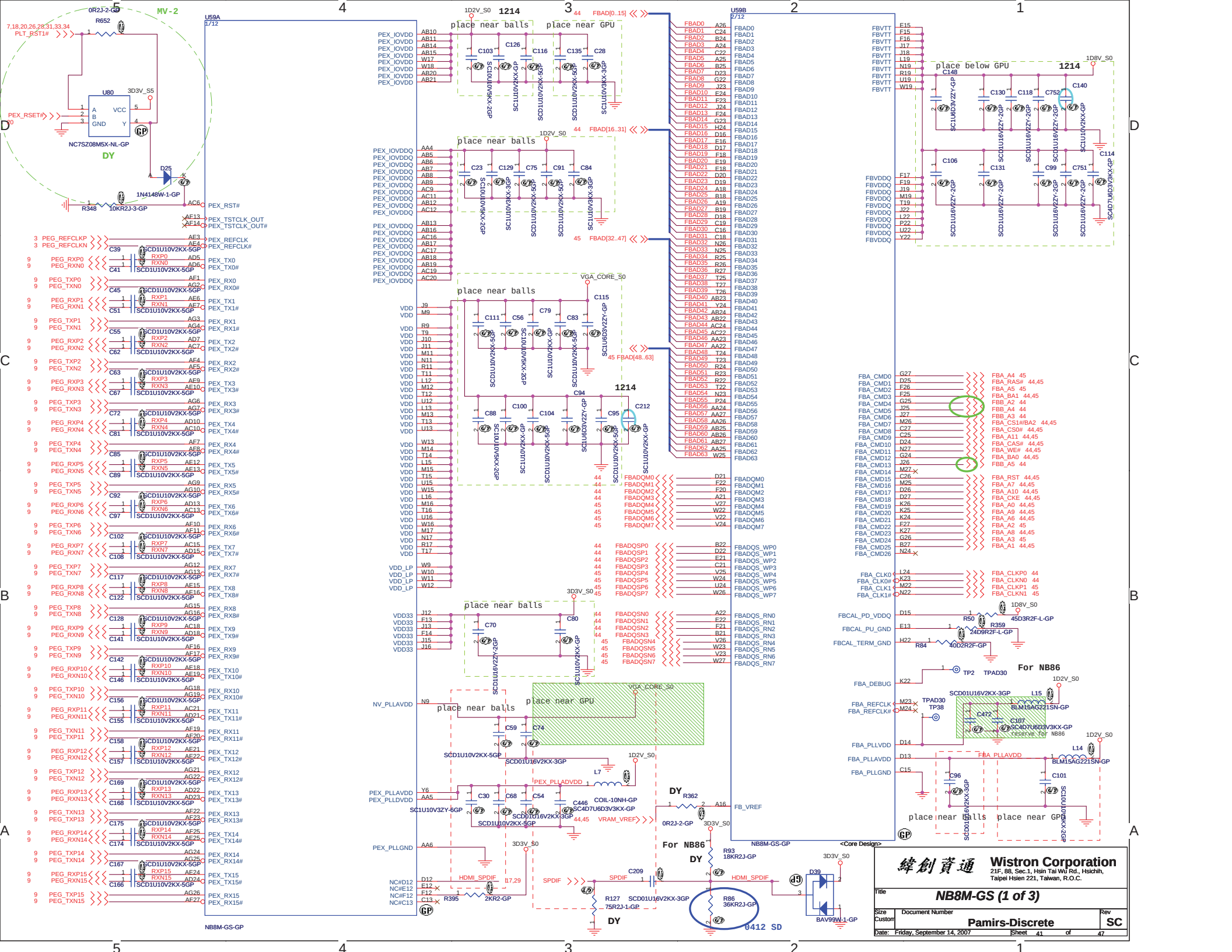






<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**VGA CORE 1V**	
Size A3	Document Number **Pamirs-Discrete**	Rev **SA**
Date: Wednesday, September 12, 2007	Sheet 40 of 47	


MV-2
DY
place near balls
place near GPU
place below GPU
1214
U59A
1/12
U59B
2/12
NB8M-GS-GP
<Core Design>
For NB86
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
NB8M-GS (1 of 3)
Pamirs-Discrete
Date: Friday, September 14, 2007
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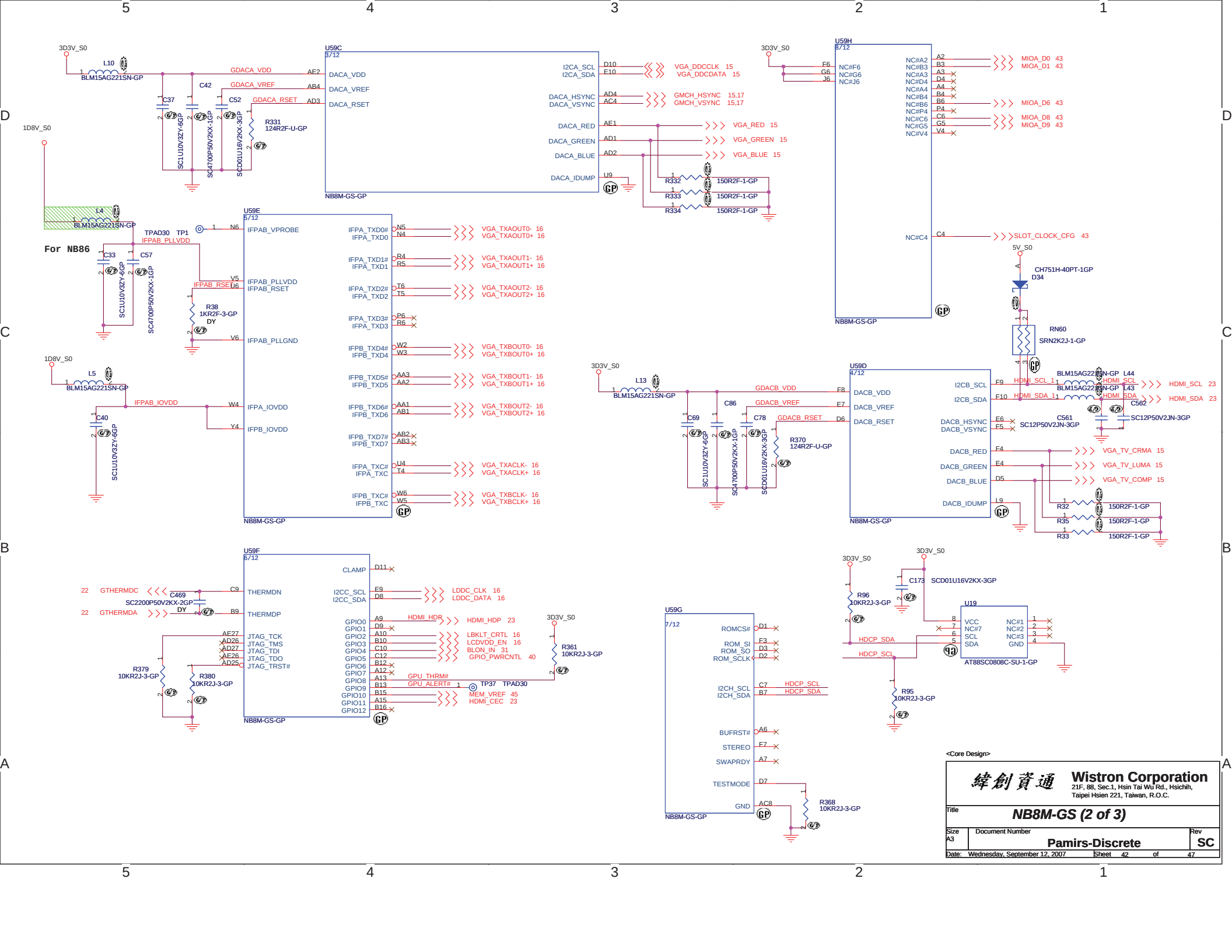
0412 SD


3D3V_S0
L10
BLM15AG221SN-GP
GDACA_VDD
C42
GDACA_VREF
C37
C52
GDACA_RSET
R331
124R2F-U-GP
SC1U10V3ZY-6GP
SC4700P50V2KX-1GP
SCD01U16V2KX-3GP
U59C
6/12
DACA_VDD
DACA_VREF
DACA_RSET
I2CA_SCL
I2CA_SDA
VGA_DDCCLK 15
VGA_DDCDATA 15
DACA_HSYNC
DACA_VSYNC
GMCH_HSYNC 15,17
GMCH_VSYNC 15,17
DACA_RED
DACA_GREEN
DACA_BLUE
DACA_IDUMP
VGA_RED 15
VGA_GREEN 15
VGA_BLUE 15
R332
R333
R334
150R2F-1-GP
NB8M-GS-GP
1D8V_S0
L4
BLM15AG221SN-GP
For NB86
TPAD30
TP1
IFPAB_PLLVDD
C33
C57
IFPAB_RSET
R38
1KR2F-3-GP
DY
U59E
6/12
IFPAB_VPROBE
IFPAB_PLLVDD
IFPAB_RSET
IFPAB_PLLGND
IFPA_IOVDD
IFPB_IOVDD
IFPA_TXD0#
IFPA_TXD0
IFPA_TXD1#
IFPA_TXD1
IFPA_TXD2#
IFPA_TXD2
IFPA_TXD3#
IFPA_TXD3
IFPB_TXD4#
IFPB_TXD4
IFPB_TXD5#
IFPB_TXD5
IFPB_TXD6#
IFPB_TXD6
IFPB_TXD7#
IFPB_TXD7
IFPA_TXC#
IFPA_TXC
IFPB_TXC#
IFPB_TXC
VGA_TXAOUT0- 16
VGA_TXAOUT0+ 16
VGA_TXAOUT1- 16
VGA_TXAOUT1+ 16
VGA_TXAOUT2- 16
VGA_TXAOUT2+ 16
VGA_TXBOUT0- 16
VGA_TXBOUT0+ 16
VGA_TXBOUT1- 16
VGA_TXBOUT1+ 16
VGA_TXBOUT2- 16
VGA_TXBOUT2+ 16
VGA_TXACLK- 16
VGA_TXACLK+ 16
VGA_TXBCLK- 16
VGA_TXBCLK+ 16
NB8M-GS-GP
1D8V_S0
L5
BLM15AG221SN-GP
IFPAB_IOVDD
C40
SC1U10V3ZY-6GP
U59H
8/12
NC#F6
NC#G6
NC#J6
NC#A2
NC#B3
NC#A3
NC#D4
NC#A4
NC#B4
NC#B6
NC#P4
NC#C6
NC#G5
NC#V4
MIOA_D0 43
MIOA_D1 43
MIOA_D6 43
MIOA_D8 43
MIOA_D9 43
NB8M-GS-GP
NC#C4
C4
SLOT_CLOCK_CFG 43
5V_S0
CH751H-40PT-1GP
D34
RN60
SRN2K2J-1-GP
3D3V_S0
L13
BLM15AG221SN-GP
GDACB_VDD
C86
GDACB_VREF
C69
C78
GDACB_RSET
R370
124R2F-U-GP
SC4700P50V2KX-1GP
SCD01U16V2KX-3GP
U59D
4/12
DACB_VDD
DACB_VREF
DACB_RSET
I2CB_SCL
I2CB_SDA
DACB_HSYNC
DACB_VSYNC
DACB_RED
DACB_GREEN
DACB_BLUE
DACB_IDUMP
HDMI_SCL_1
HDMI_SDA_1
HDMI_SCL 23
HDMI_SDA 23
BLM15AG221SN-GP L44
BLM15AG221SN-GP L43
C562
C561
SC12P50V2JN-3GP
VGA_TV_CRMA 15
VGA_TV_LUMA 15
VGA_TV_COMP 15
R32
R35
R33
150R2F-1-GP
NB8M-GS-GP
U59F
6/12
CLAMP
I2CC_SCL
I2CC_SDA
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
LDDC_CLK 16
LDDC_DATA 16
HDMI_HDR
HDMI_HDP 23
LBKLT_CRTL 16
LCDVDD_EN 16
BLON_IN 31
GPIO_PWRCNTL 40
GPU_THRM#
GPU_ALERT#
TP37
TPAD30
MEM_VREF 45
HDMI_CEC 23
22 GTHERMDC
22 GTHERMDA
C469
SC2200P50V2KX-2GP
DY
THERMDN
THERMDP
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST#
R379
10KR2J-3-GP
R380
10KR2J-3-GP
R361
10KR2J-3-GP
NB8M-GS-GP
U59G
7/12
ROMCS#
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST#
STEREO
SWAPRDY
TESTMODE
GND
HDCP_SCL
HDCP_SDA
R368
10KR2J-3-GP
NB8M-GS-GP
3D3V_S0
C173
SCD01U16V2KX-3GP
R96
10KR2J-3-GP
HDCP_SDA
HDCP_SCL
R95
10KR2J-3-GP
U19
VCC
NC#7
SCL
SDA
NC#1
NC#2
NC#3
GND
AT88SC0808C-SU-1-GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB8M-GS (2 of 3)
Size
A3
Document Number
Pamirs-Discrete
Rev
SC
Date: Wednesday, September 12, 2007
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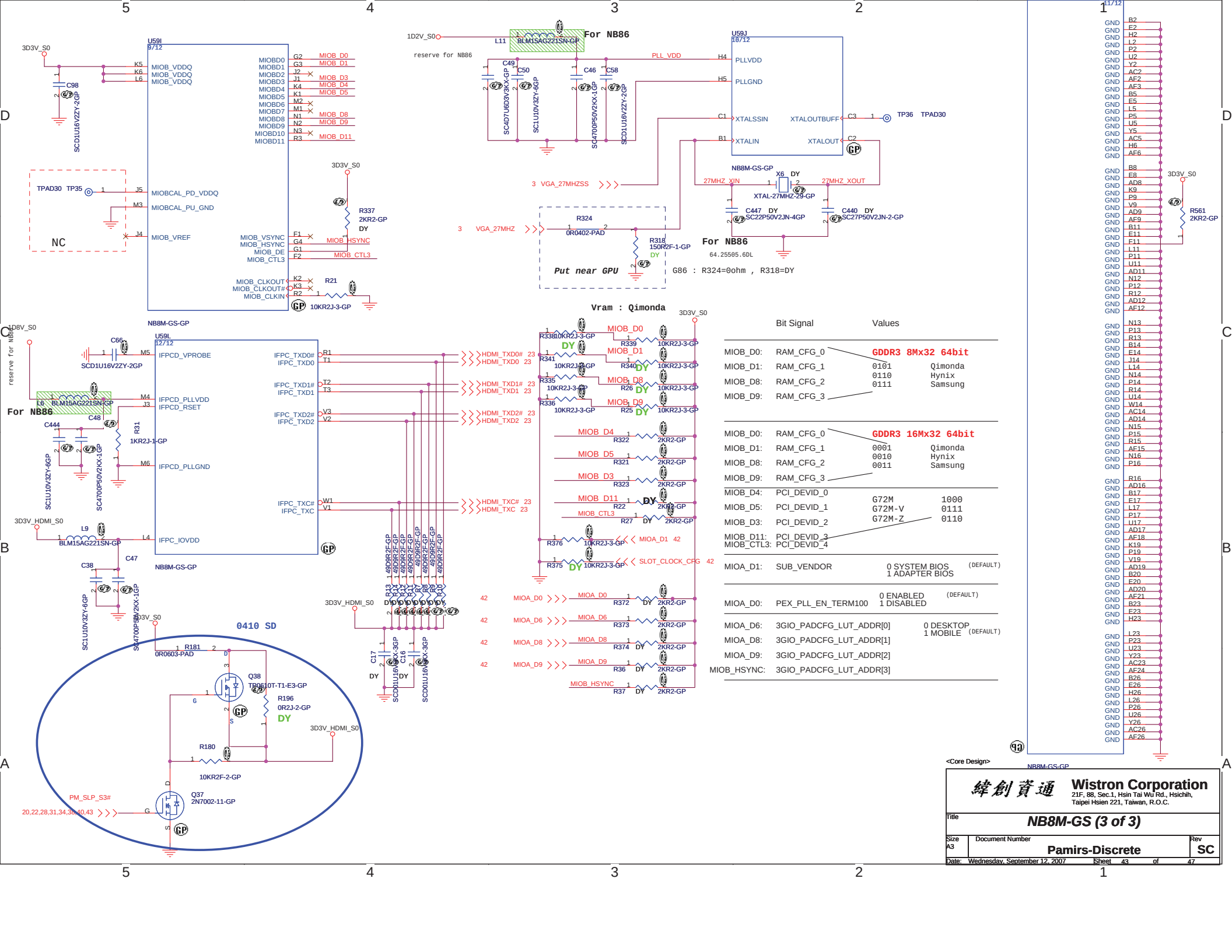
U59I 9/12
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MIOBD0
MIOBD1
MIOBD2
MIOBD3
MIOBD4
MIOBD5
MIOBD6
MIOBD7
MIOBD8
MIOBD9
MIOBD10
MIOBD11
MIOB_D0
MIOB_D1
MIOB_D3
MIOB_D4
MIOB_D5
MIOB_D8
MIOB_D9
MIOB_D11
MIOBCAL_PD_VDDQ
MIOBCAL_PU_GND
MIOB_VREF
NC
MIOB_VSYNC
MIOB_HSYNC
MIOB_DE
MIOB_CTL3
MIOB_CLKOUT
MIOB_CLKOUT#
MIOB_CLKIN
R337 2KR2-GP DY
R21 10KR2J-3-GP
For NB86
L11 BLM15AG221SN-GP
reserve for NB86
U59J 10/12
PLLVDD
PLLGND
XTALSSIN
XTALIN
XTALOUTBUFF
XTALOUT
TP36 TPAD30
NB8M-GS-GP
27MHZ_XIN
27MHZ_XOUT
X6 DY
XTAL-27MHZ-29-GP
C447 DY SC22P50V2JN-4GP
C440 DY SC27P50V2JN-2-GP
R324 0R0402-PAD
R318 150R2F-1-GP DY
Put near GPU
G86 : R324=0ohm , R318=DY
For NB86
64.25505.6DL
Vram : Qimonda
MIOB_D0 R338 10KR2J-3-GP DY
MIOB_D1 R339 10KR2J-3-GP
MIOB_D8 R340 10KR2J-3-GP DY
MIOB_D9 R341 10KR2J-3-GP
R335 10KR2J-3-GP
R336 10KR2J-3-GP
R26 10KR2J-3-GP DY
R25 10KR2J-3-GP DY
MIOB_D4 R322 2KR2-GP
MIOB_D5 R321 2KR2-GP
MIOB_D3 R323 2KR2-GP
MIOB_D11 R22 2KR2-GP DY
MIOB_CTL3 R27 DY 2KR2-GP
R376 10KR2J-3-GP MIOA_D1 42
R375 DY 10KR2J-3-GP SLOT_CLOCK_CFG 42
MIOA_D0 R372 DY 2KR2-GP
MIOA_D6 R373 2KR2-GP
MIOA_D8 R374 DY 2KR2-GP
MIOA_D9 R36 DY 2KR2-GP
MIOB_HSYNC R37 DY 2KR2-GP
NB8M-GS-GP
U59L 12/12
IFPCD_VPROBE
IFPCD_PLLVDD
IFPCD_RSET
IFPCD_PLLGND
IFPC_TXD0#
IFPC_TXD0
IFPC_TXD1#
IFPC_TXD1
IFPC_TXD2#
IFPC_TXD2
IFPC_TXC#
IFPC_TXC
IFPC_IOVDD
HDMI_TXD0# 23
HDMI_TXD0 23
HDMI_TXD1# 23
HDMI_TXD1 23
HDMI_TXD2# 23
HDMI_TXD2 23
HDMI_TXC# 23
HDMI_TXC 23
1KR2J-1-GP
BLM15AG221SN-GP
0410 SD
R181 0R0603-PAD
Q38 TP0610T-T1-E3-GP
R196 0R2J-2-GP DY
R180 10KR2F-2-GP
Q37 2N7002-11-GP
PM_SLP_S3#
20,22,28,31,34,35,40,43
Bit Signal Values
MIOB_D0: RAM_CFG_0 GDDR3 8Mx32 64bit
MIOB_D1: RAM_CFG_1 0101 Qimonda
MIOB_D8: RAM_CFG_2 0110 Hynix
MIOB_D9: RAM_CFG_3 0111 Samsung
MIOB_D0: RAM_CFG_0 GDDR3 16Mx32 64bit
MIOB_D1: RAM_CFG_1 0001 Qimonda
MIOB_D8: RAM_CFG_2 0010 Hynix
MIOB_D9: RAM_CFG_3 0011 Samsung
MIOB_D4: PCI_DEVID_0
MIOB_D5: PCI_DEVID_1 G72M 1000
MIOB_D3: PCI_DEVID_2 G72M-V 0111
MIOB_D11: PCI_DEVID_3 G72M-Z 0110
MIOB_CTL3: PCI_DEVID_4
MIOA_D1: SUB_VENDOR 0 SYSTEM BIOS (DEFAULT) 1 ADAPTER BIOS
MIOA_D0: PEX_PLL_EN_TERM100 0 ENABLED (DEFAULT) 1 DISABLED
MIOA_D6: 3GIO_PADCFG_LUT_ADDR[0] 0 DESKTOP 1 MOBILE (DEFAULT)
MIOA_D8: 3GIO_PADCFG_LUT_ADDR[1]
MIOA_D9: 3GIO_PADCFG_LUT_ADDR[2]
MIOB_HSYNC: 3GIO_PADCFG_LUT_ADDR[3]
11/12
GND
3D3V_S0
R561 2KR2-GP
<Core Design>
NB8M-GS-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB8M-GS (3 of 3)
Size A3
Document Number
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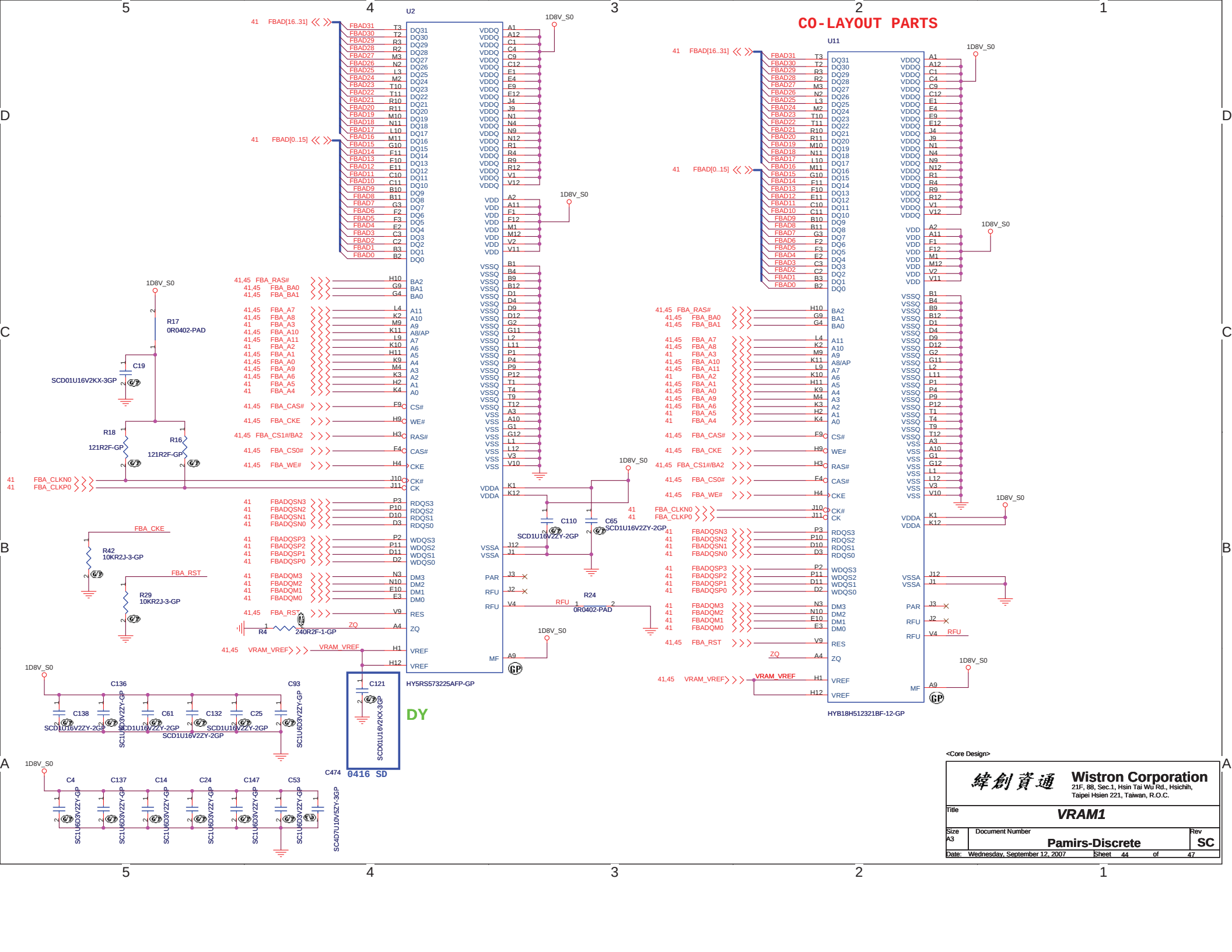
CO-LAYOUT PARTS
U2
U11
HY5RS573225AFP-GP
HYB18H512321BF-12-GP
DY
0416 SD
R17 0R0402-PAD
R18 121R2F-GP
R16 121R2F-GP
R42 10KR2J-3-GP
R29 10KR2J-3-GP
R4 240R2F-1-GP
R24 0R0402-PAD
C19 SCD01U16V2KX-3GP
C110 SCD1U16V2ZY-2GP
C65 SCD1U16V2ZY-2GP
C121 SCD01U16V2KX-3GP
C474
C136
C93
C138
C61
C132
C25
C4
C137
C14
C24
C147
C53
SC4D7U10V5ZY-3GP
1D8V_S0
VRAM_VREF
FBA_CKE
FBA_RST
ZQ
RFU
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM1
Size A3
Document Number
Pamirs-Discrete
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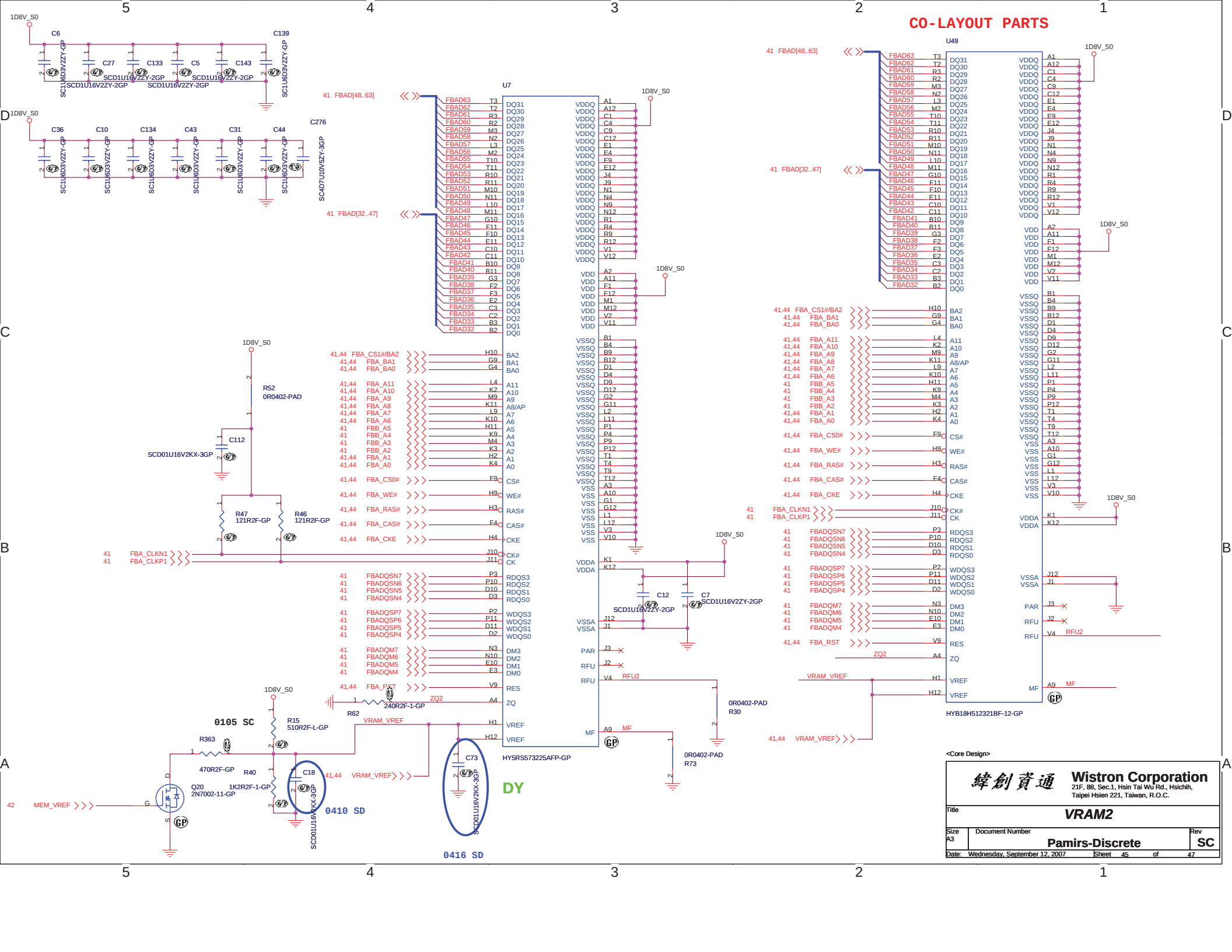
CO-LAYOUT PARTS
U7
U49
HY5RS573225AFP-GP
HYB18H512321BF-12-GP
1D8V_S0
C6
C139
C27
C133
C5
C143
SCD1U16V2ZY-2GP
SC1U6D3V2ZY-GP
C36
C10
C134
C43
C31
C44
C276
SC4D7U10V5ZY-3GP
R52
0R0402-PAD
C112
SCD01U16V2KX-3GP
R47
121R2F-GP
R46
121R2F-GP
R62
240R2F-1-GP
R15
510R2F-L-GP
0105 SC
R363
470R2F-GP
R40
1K2R2F-1-GP
Q20
2N7002-11-GP
C18
SCD01U16V2KX-3GP
0410 SD
C73
SCD01U16V2KX-3GP
0416 SD
DY
C12
C7
SCD1U16V2ZY-2GP
R30
R73
0R0402-PAD
ZQ2
VRAM_VREF
MEM_VREF
MF
RFU
RFU2
PAR
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM2
Size
A3
Document Number
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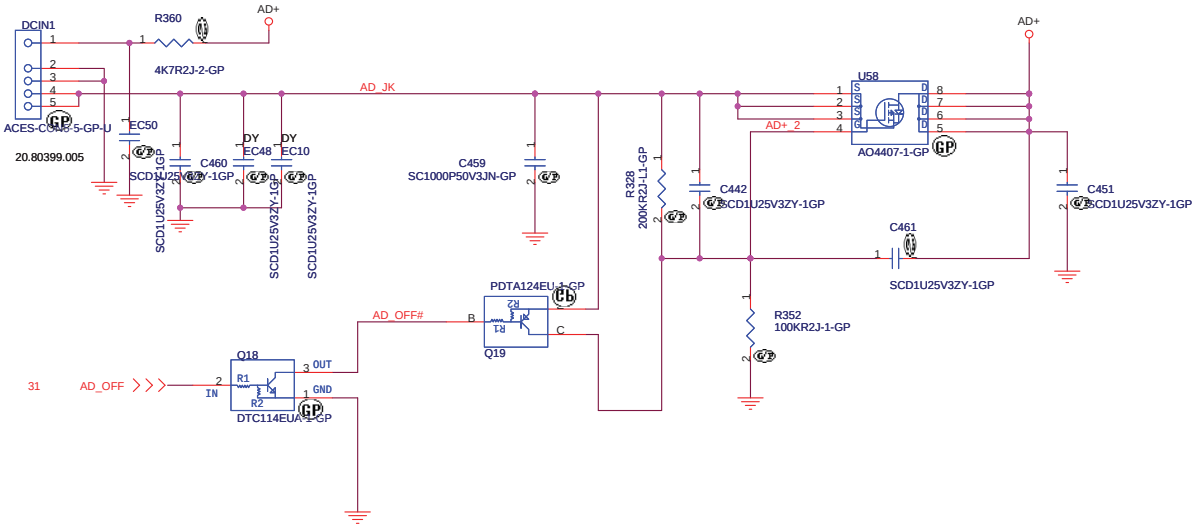
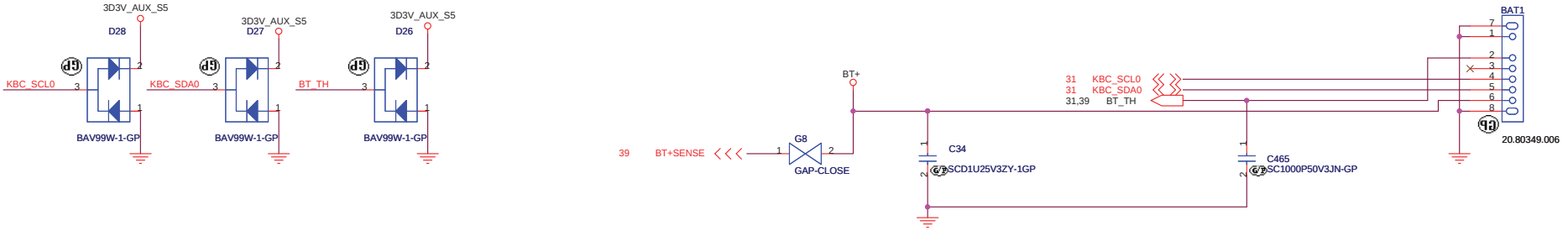
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

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Title: **AD/BATT CONN**

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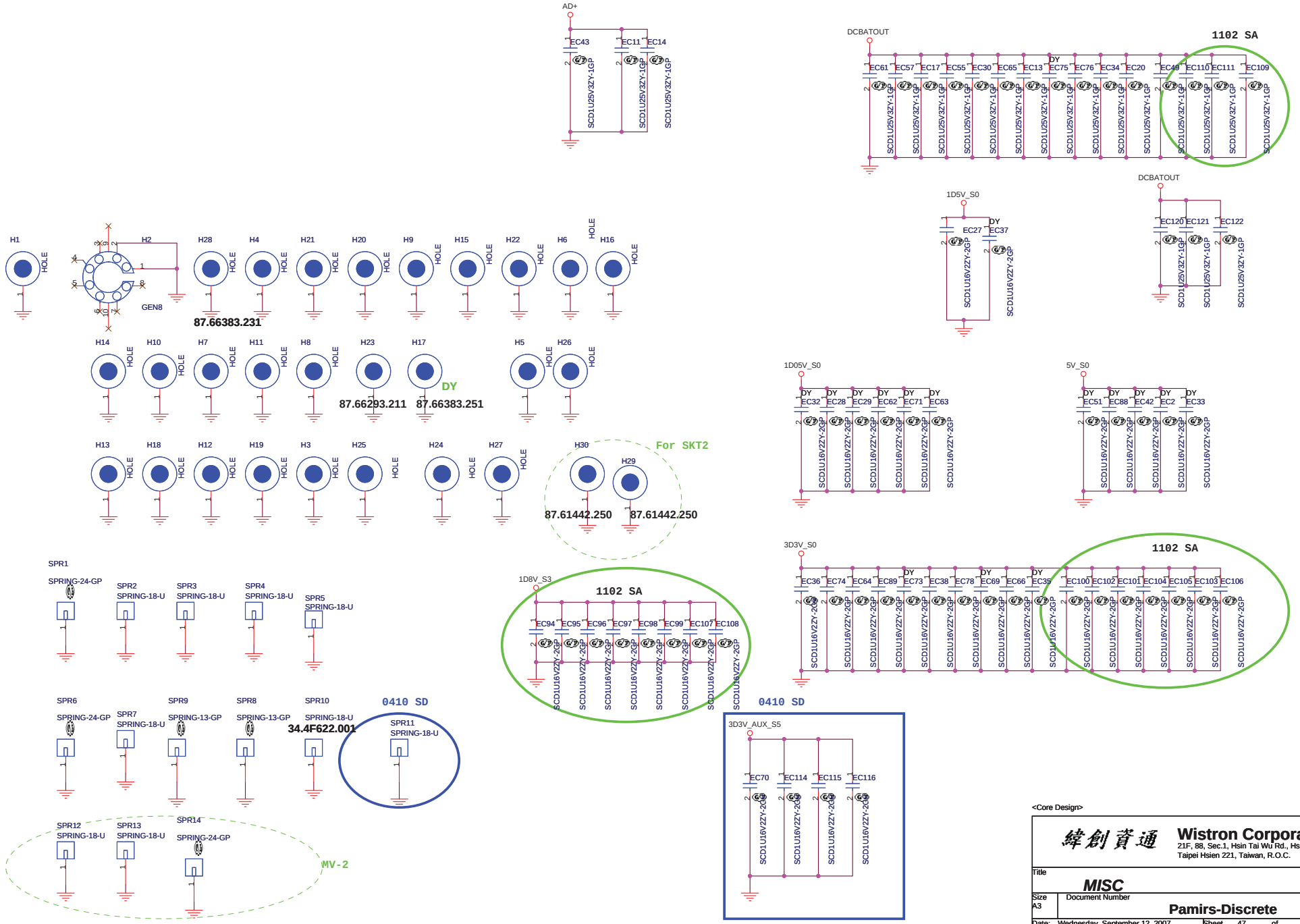

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **MISC**

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