

PCB STACK UP

6L Dis.

Jones/Cujo 2.0 (UP6/7) BLOCK DIAGRAM

01

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

Cable Docking
VGA
RJ-45
CIR/Pwr btn
SPDIF Out
Stereo MIC
Headphone Jack
USB Port
VOL Cntr
PAGE 32

SYSTEM POWER RT8206B
PAGE 35

VCCP +1.1VTT(RT8208A) AND PCH
1.05V(RT8204)
PAGE 36

CPU CORE ISL6251A
PAGE 41

VGACORE(1.025V) RT8208A
PAGE 38

DDR III SMDRR_VTERM
1.5V/1.5VSUS(RT8207)
PAGE 39

SYSTEM CHARGER(ISL6251AHAZ-T)
PAGE 40

Keyboard PAGE 31
Touch Pad PAGE 29
Capacitive Sense
SW PAGE 32

DDRIII-SODIMM1
PAGE 12
DDRIII 800/1066 MT/s
1333MT/s CFD only
DDRIII-SODIMM2
PAGE 13
DDRIII 800/1066 MT/s
1333MT/s CFD only

SATA - HDD
PAGE 31
SATA0 150MB
SATA - CD-ROM
PAGE 31
SATA1 150MB
SATA - 2ndHDD
PAGE 31
SATA4 150MB
E-SATA
PAGE 30
SATA5 150MB
Accelerometer
LIS3LV02DL
PAGE 25
SMBUS

ENE KBC
KB3926 D2
PAGE 29
GMT G9931P1U
FAN
PAGE 32
SPI
PAGE 29

CPU
Auburndale 35W
Clarkfield 45W
PAGE 3-6

PCH
Ibex-M
PAGE 7-11

nVIDIA
N10M-GE 128 Bit
N10P-GE 969p
PAGE 14-20
HDMI CON
PAGE 22
CRT
PAGE 22
LCD CONN
PAGE 21

CLOCK GEN
9LRS3197
PAGE 2

Mini PCI-E Card x2
Express Card x1
Cable Docking x1

USB2.0
6,1,8,9 5 3 2
USB2.0 Ports X4
PAGE 30
BlueTooth
PAGE 30
Webcam
PAGE 30
Fingerprint
PAGE 30

PCI-E
X1 X1 X1 X1 X1
Mini PCI-E Card
WWAN/TV
PAGE 34
Mini PCI-E Card
Wireless LAN
PAGE 34
LAN
Realtek
RTL8111DL
GigaLAN
PAGE 27
Express Card
PAGE 31
JMICO 380
PAGE 23
IEEE1394
PAGE 23
Memory CardReader
PAGE 23

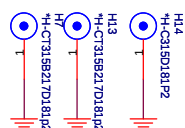
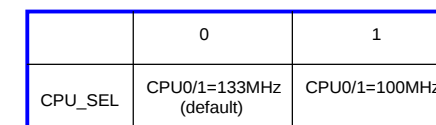
Azalia
Analog
IDT92HD75B3
PAGE 24
AUDIO Amplifier
TPA6047A4
PAGE 25
AUDIO Amplifier
TPA3007D1
PAGE 26

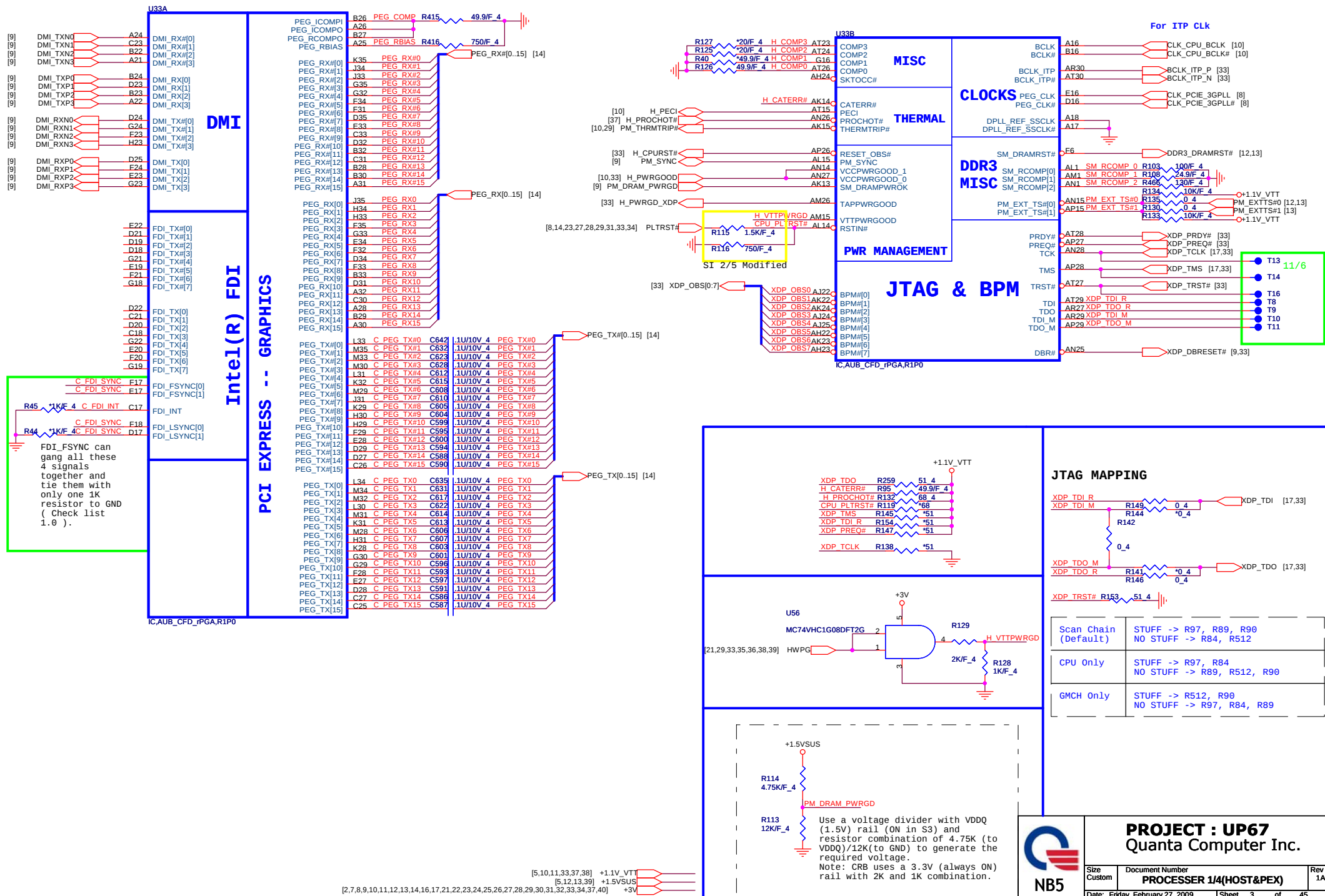
microphone
PAGE 24
Audio Jacks
(Phone/ MIC)
PAGE 24
Jack to Speaker
PAGE 25
Jack to Sub-Woofer
PAGE 26



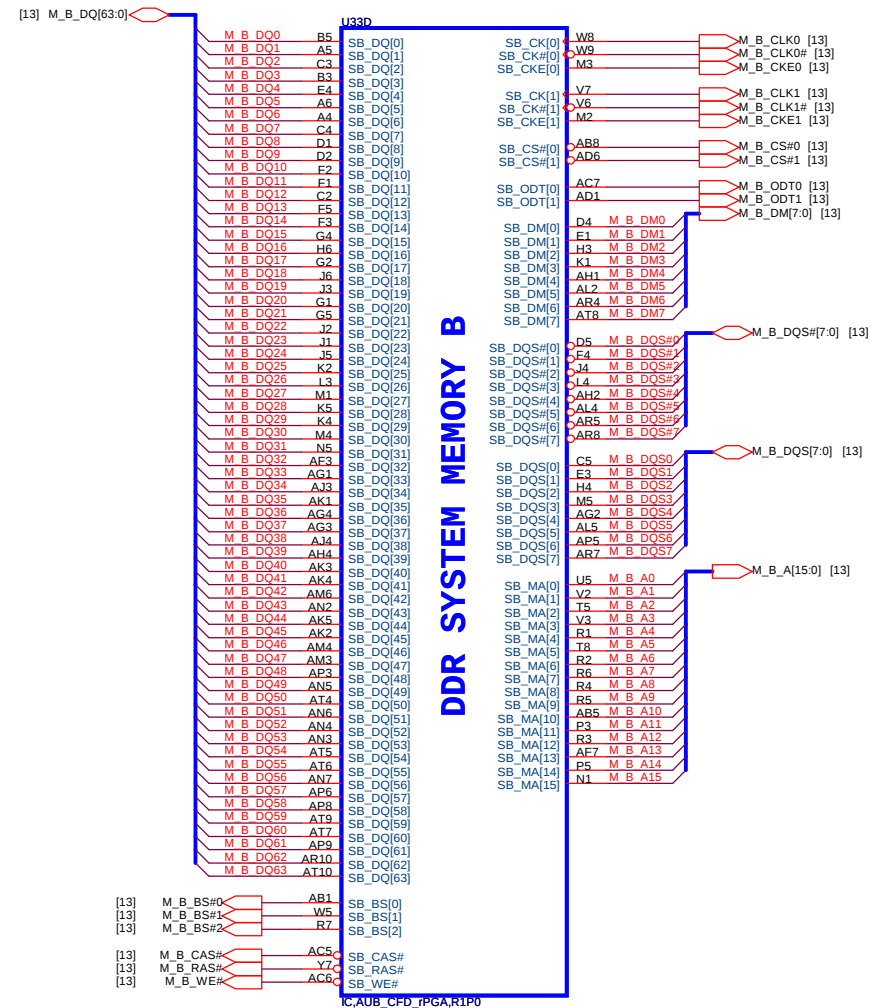
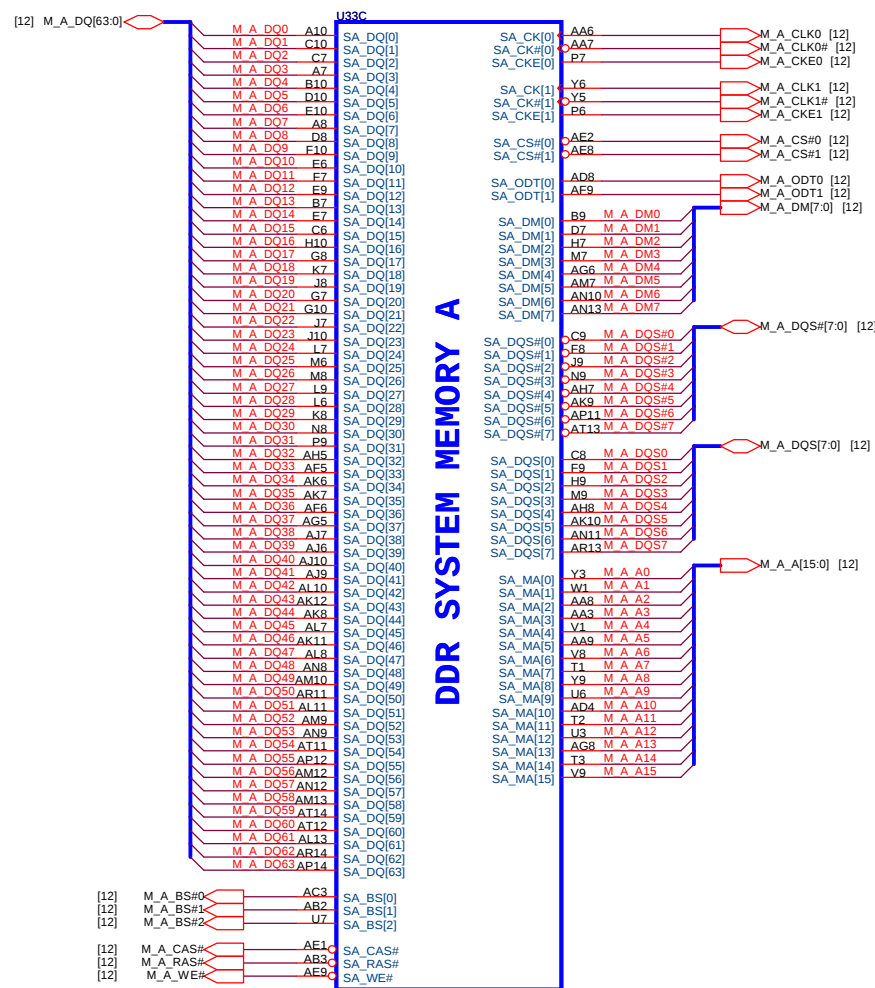
PROJECT : UP67
Quanta Computer Inc.

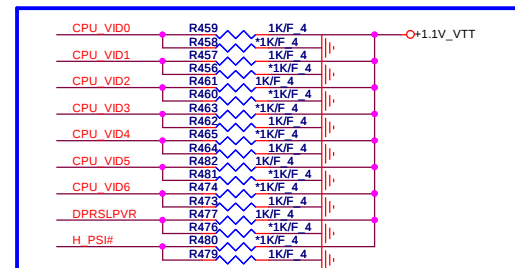
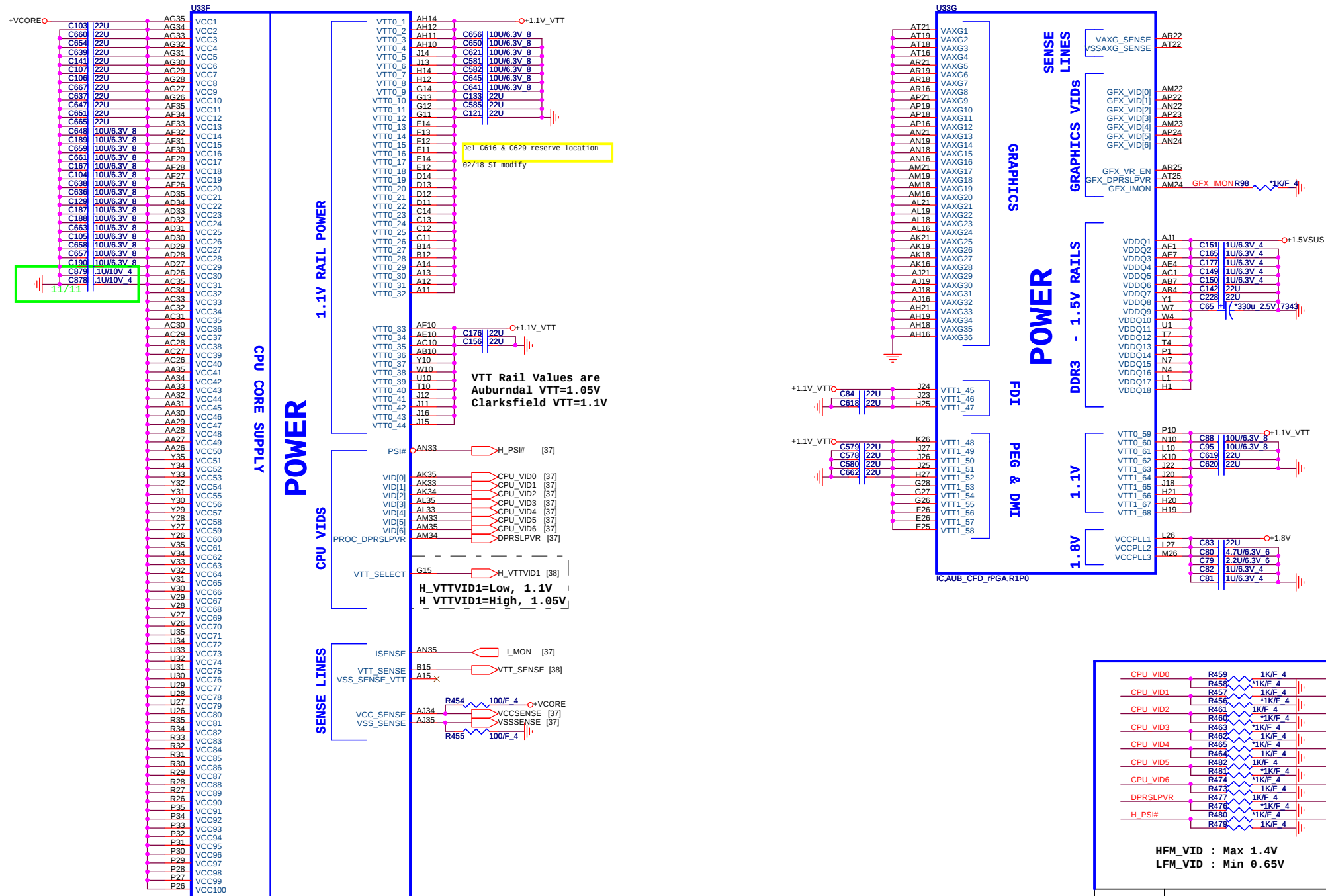
Size Custom Document Number BLOCK DIAGRAM Rev 1A
Date: Friday, February 27, 2009 Sheet 1 of 45





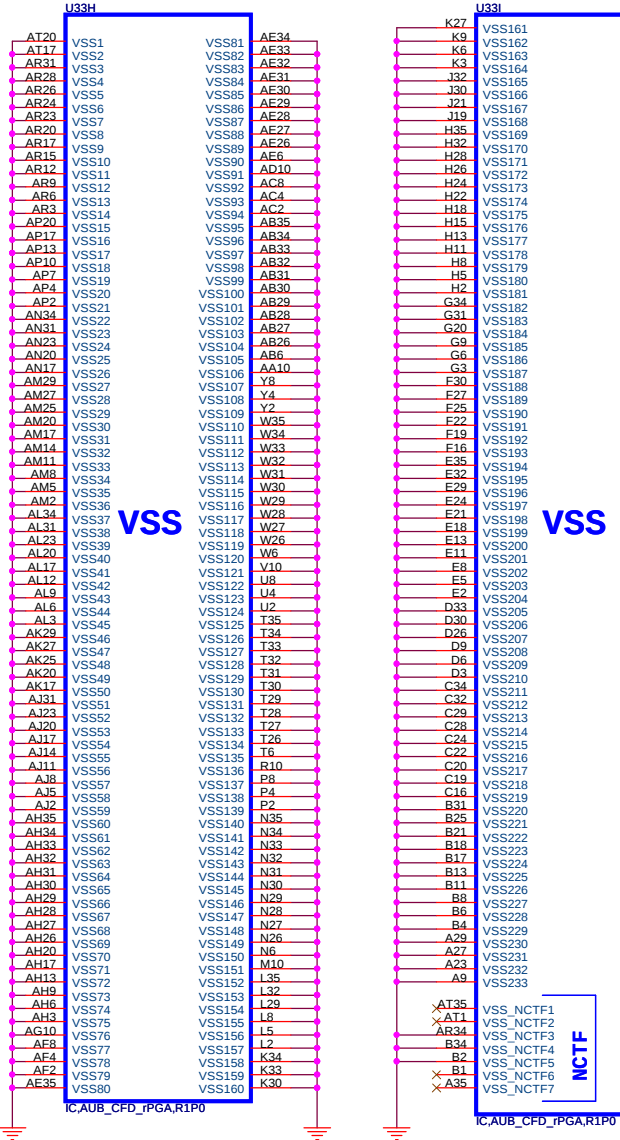
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



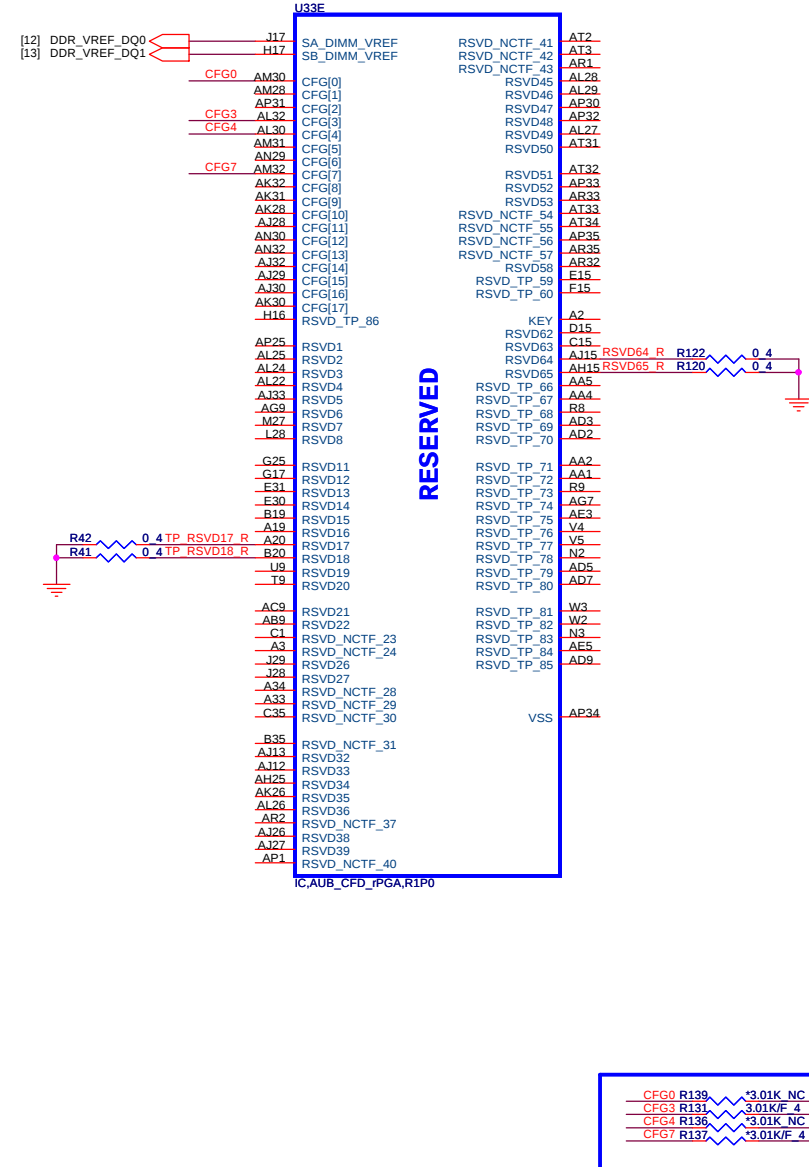


HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

CFG0 R139 3.01K NC

CFG3 R131 3.01K/F 4

CFG4 R136 3.01K NC

CFG7 R137 3.01K/F 4

CFG[1:0] - PCI_Epress Configuration Select

* 11= 1 x 16 PEG

* 10= 2 x 8 PEG

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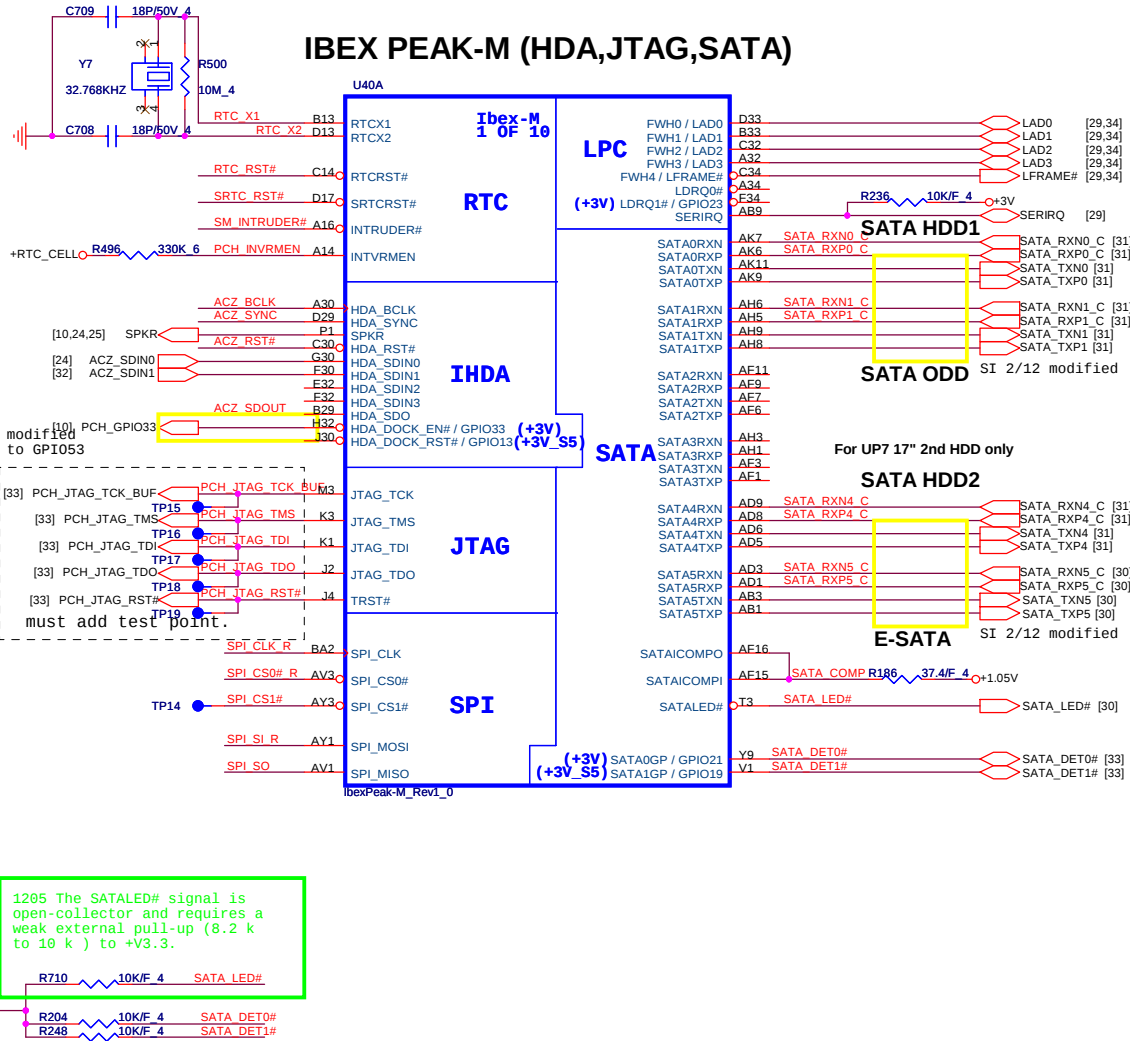
NB5

Size Custom Document Number **PROCESSOR 4/4(GND)** Rev 1A

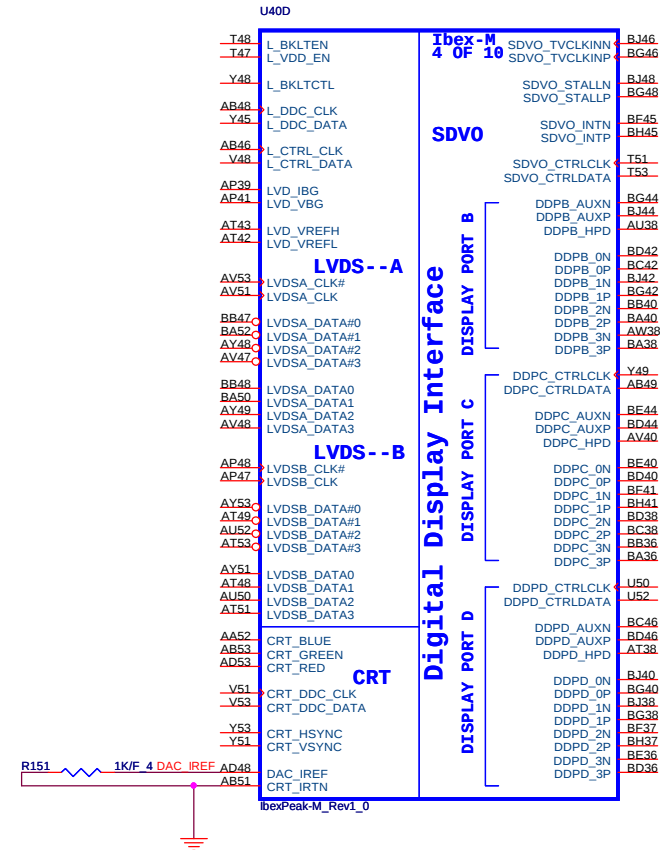
Date: Friday, February 27, 2009 I Sheet 6 of 45

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRS

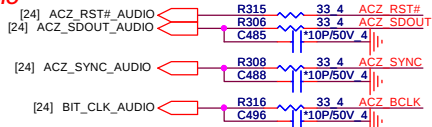
IBEX PEAK-M (HDA,JTAG,SATA)



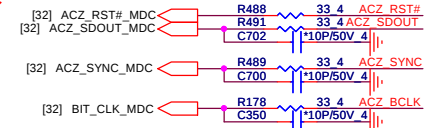
IBEX PEAK-M (LVDS,DDI)



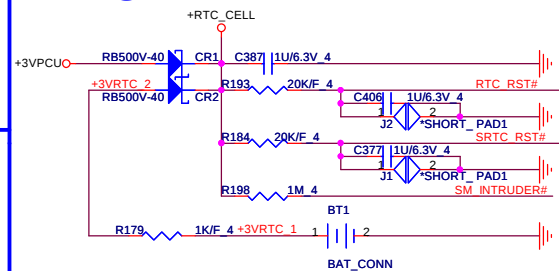
For AUDIO



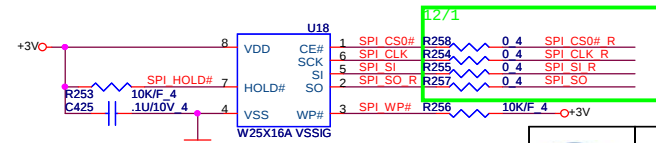
For MDC



RTC



2M byte SPI ROM for ME & Bios



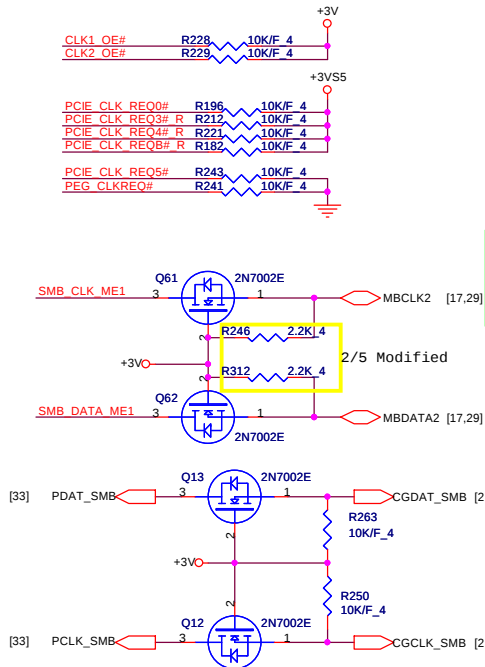
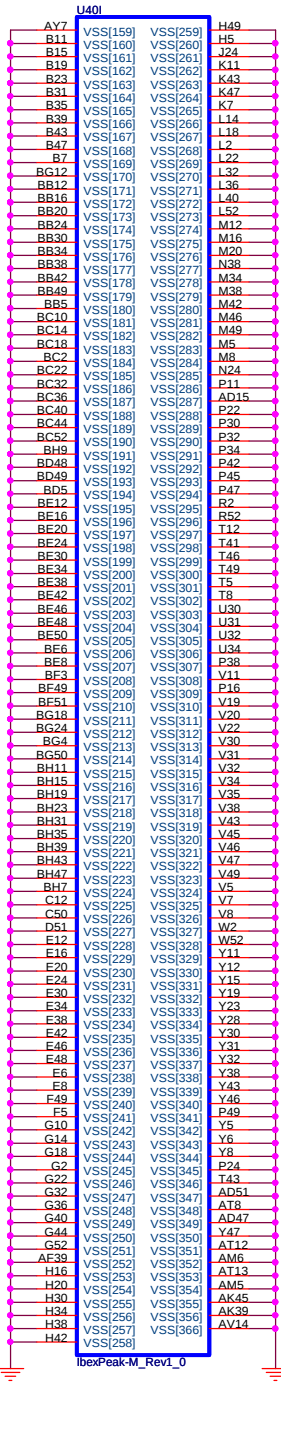
Socket: DG008000031
MXIC AKE38FP0Z00
WINBOND AKE38ZP0N01
SI 2/17 modified



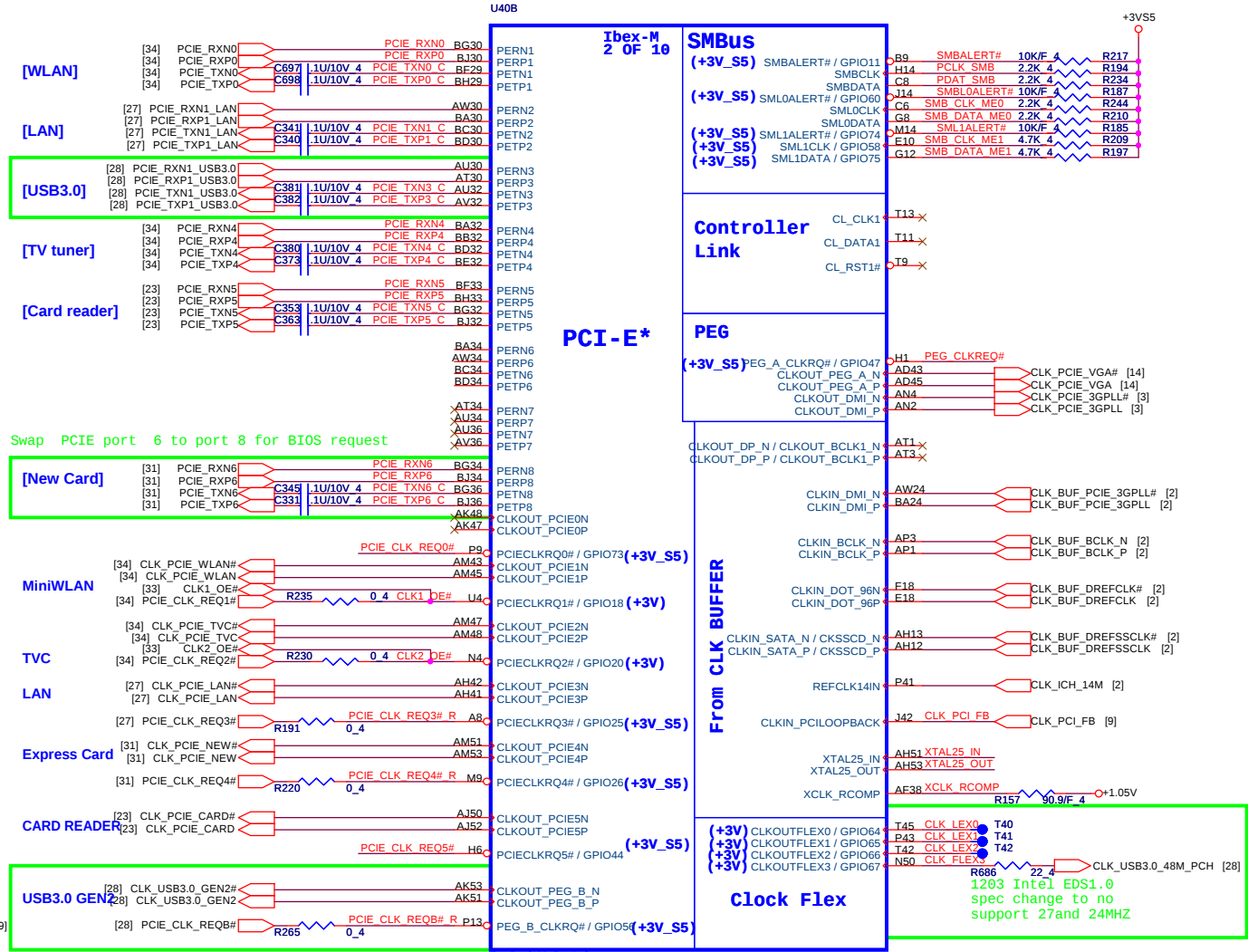
PROJECT : UP67
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Size	Document Number	Rev
Custom	PCH 2/6 (SATA,HDA,LPC)	1A
Date: Friday, February 27, 2009	Sheet 7 of 45	

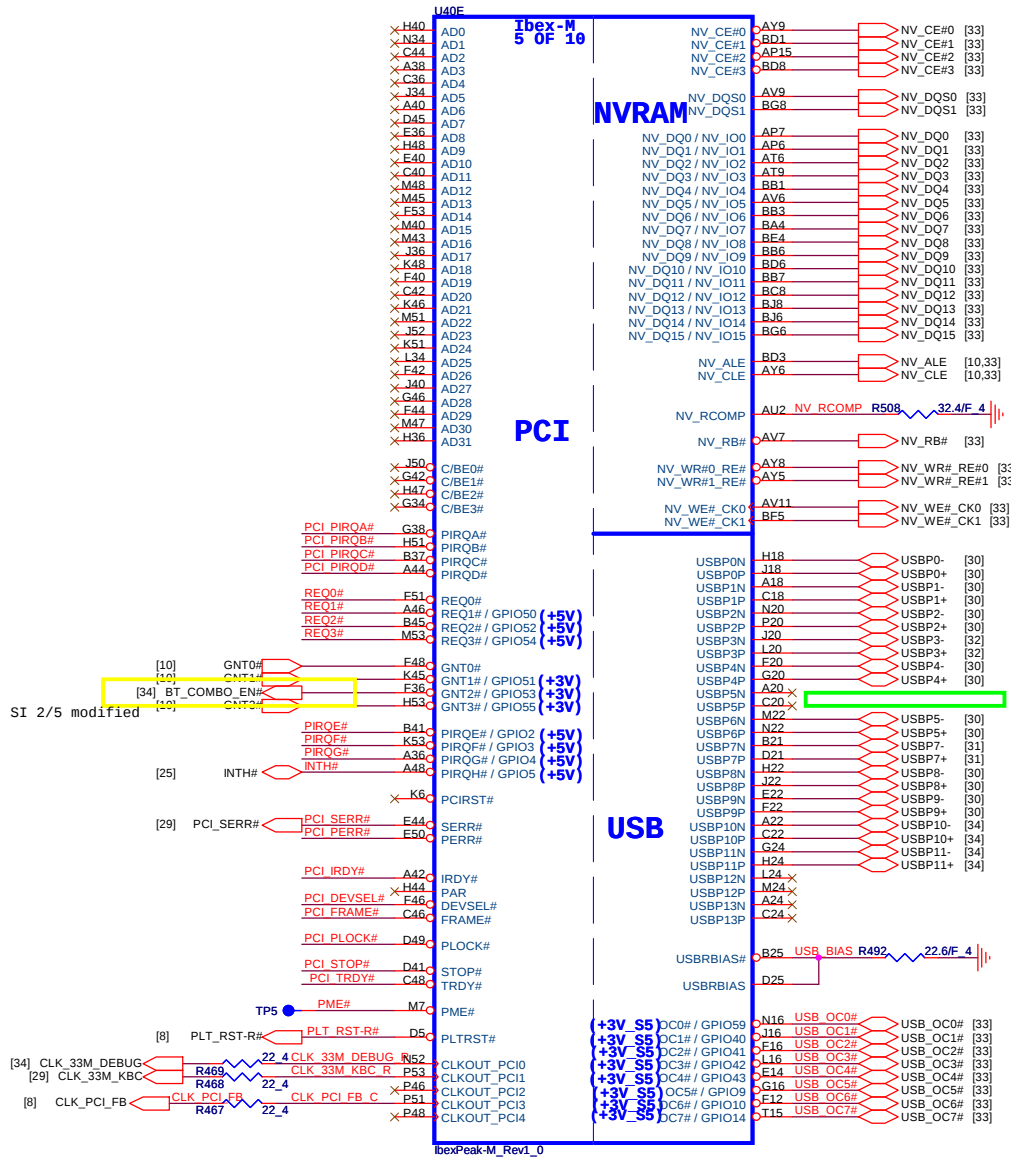
IBEX PEAK-M (GND)



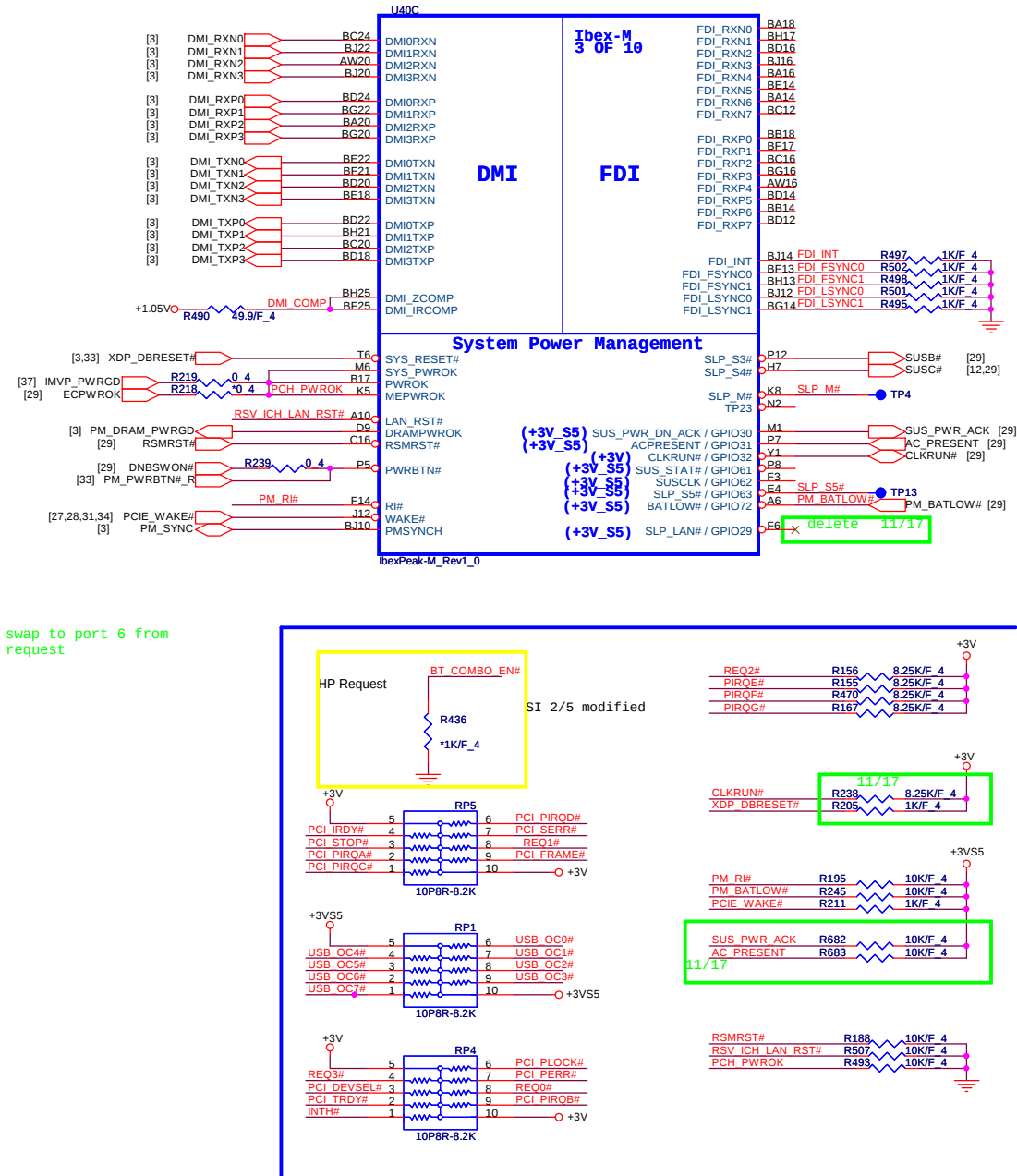
IBEX PEAK-M (PCI-E,SMBUS,CLK)



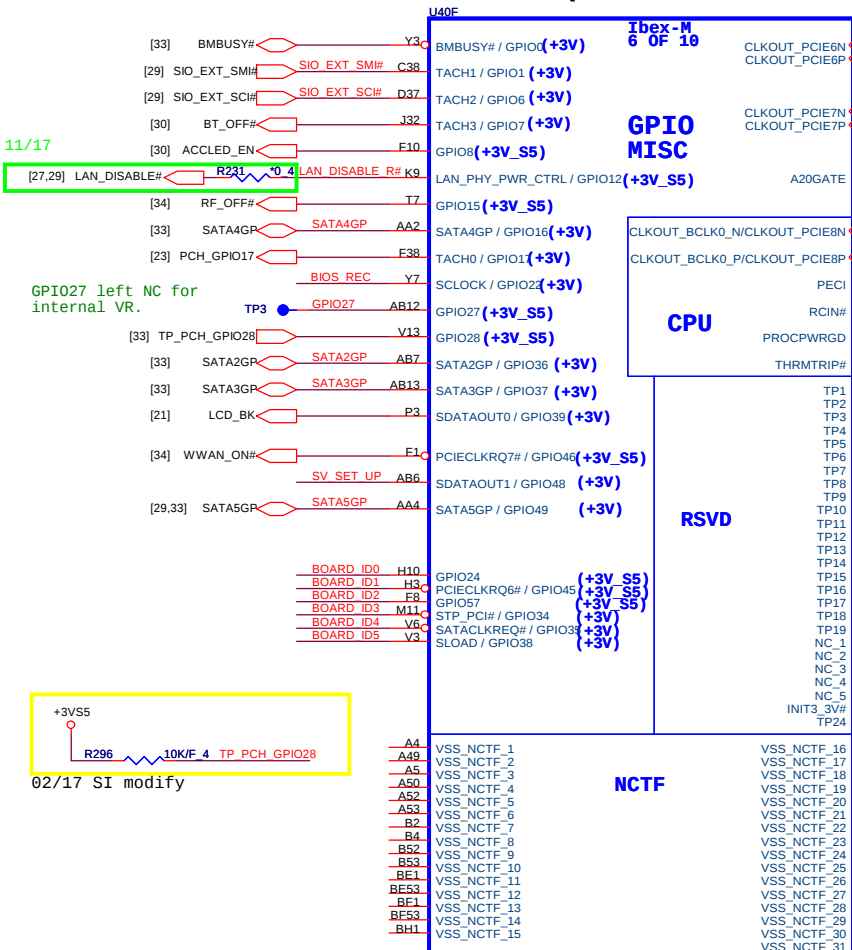
IBEX PEAK-M (PCI,USB,NVRAM)



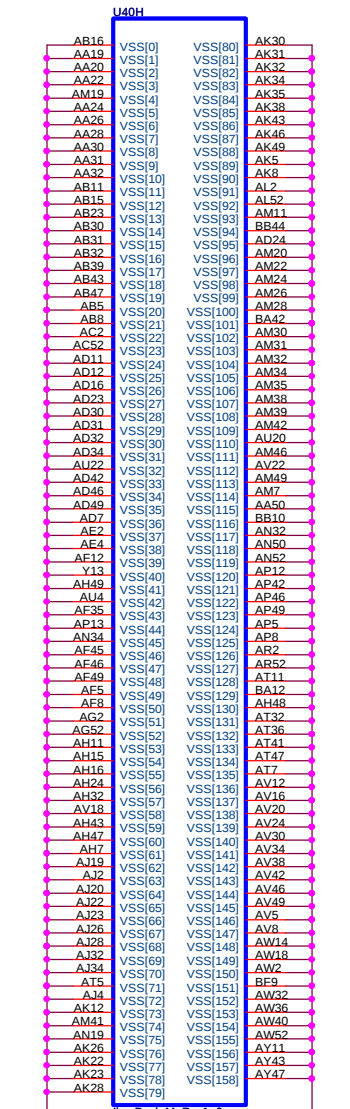
IBEX PEAK-M (DMI,FDI,GPIO)



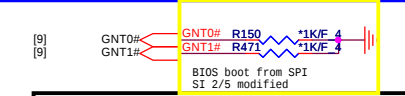
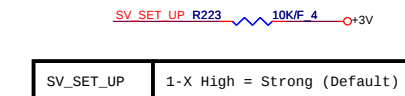
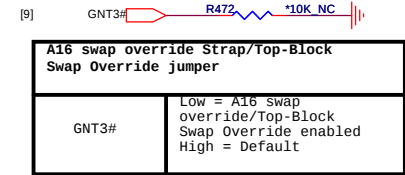
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



10

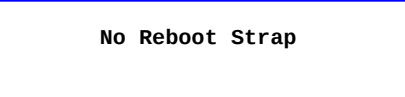


Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

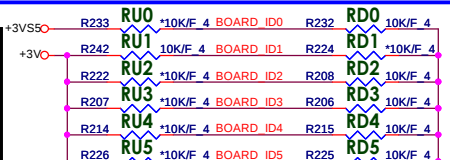
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH



BOARD ID SETTING

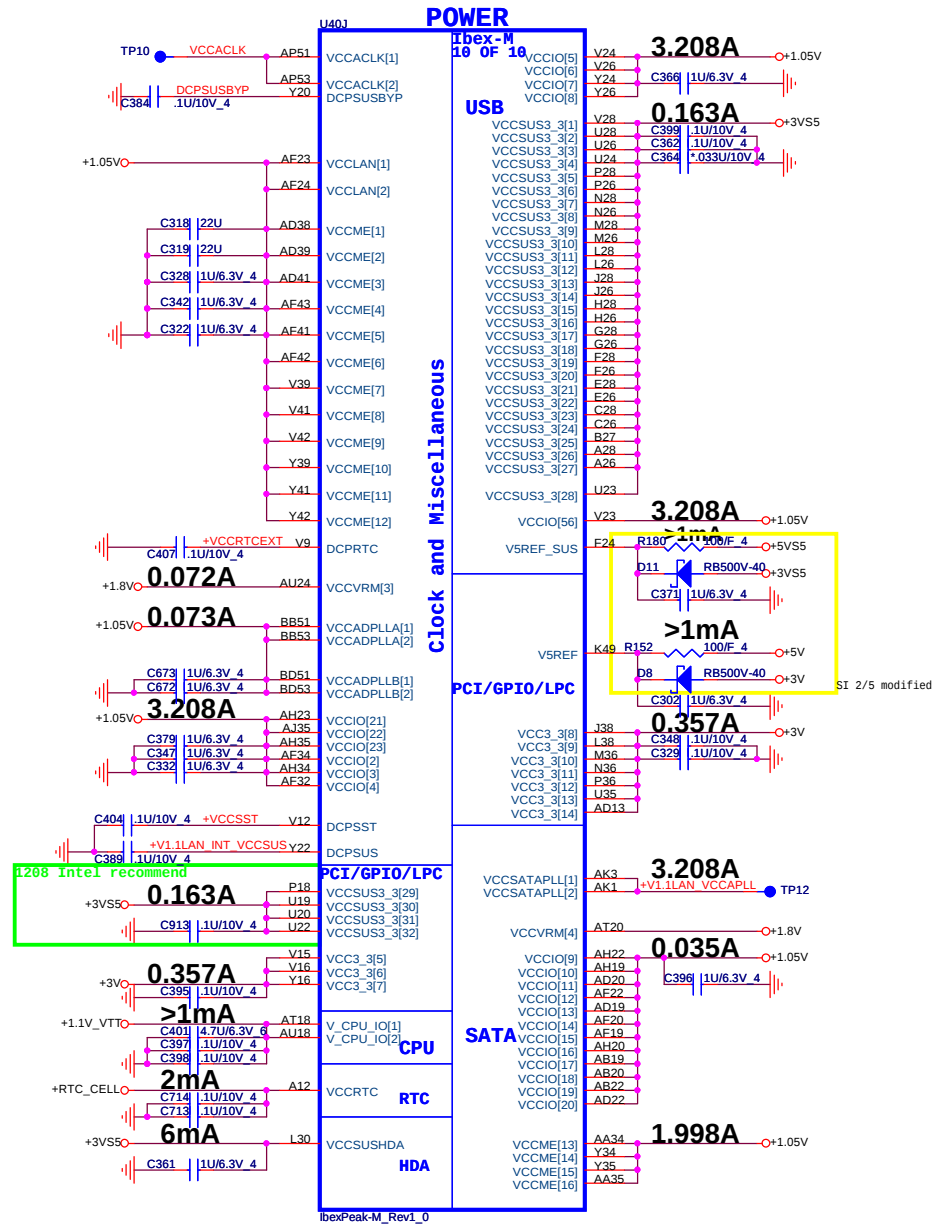
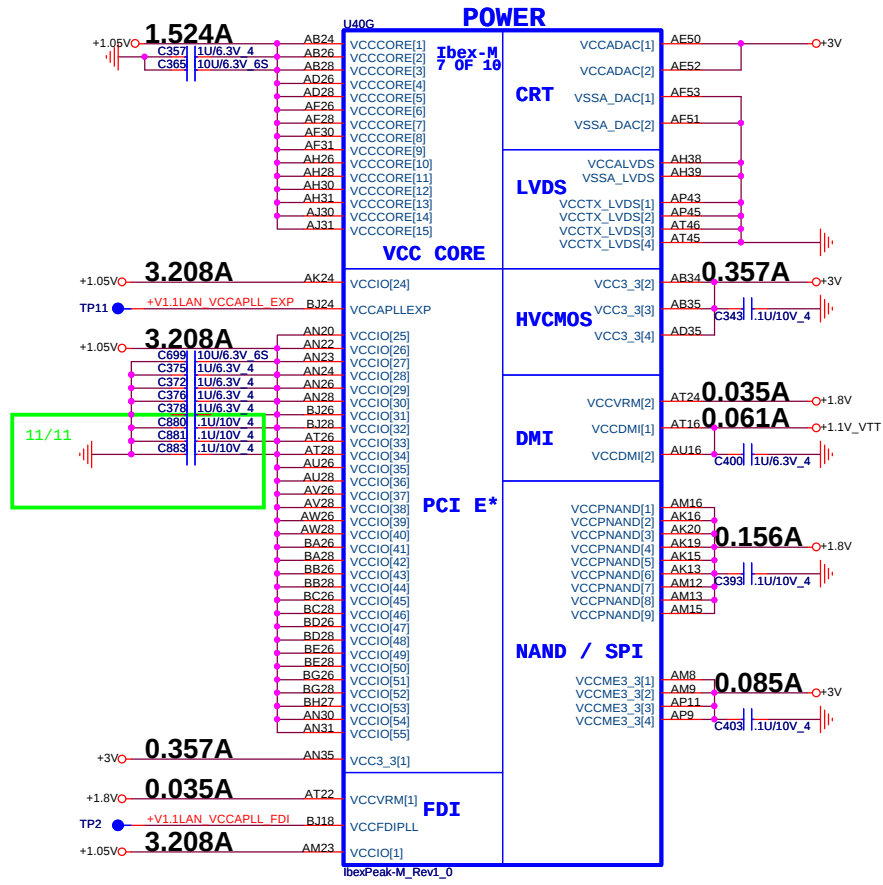
Board ID	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UP6/7	0=UP6 1=UP7					
UMA/Dis.		0=UMA 1=Dis.				
Project name			0=Jones/Cujo 2.0 (Clarkfield) 1=Jones/Cujo 2.1 (Auburndale UMA)			
ROM Size				0= 2M 1= 4M		



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Size	Document Number	Rev
Custom	PCH 4/6 (GPIO & Strap)	1A
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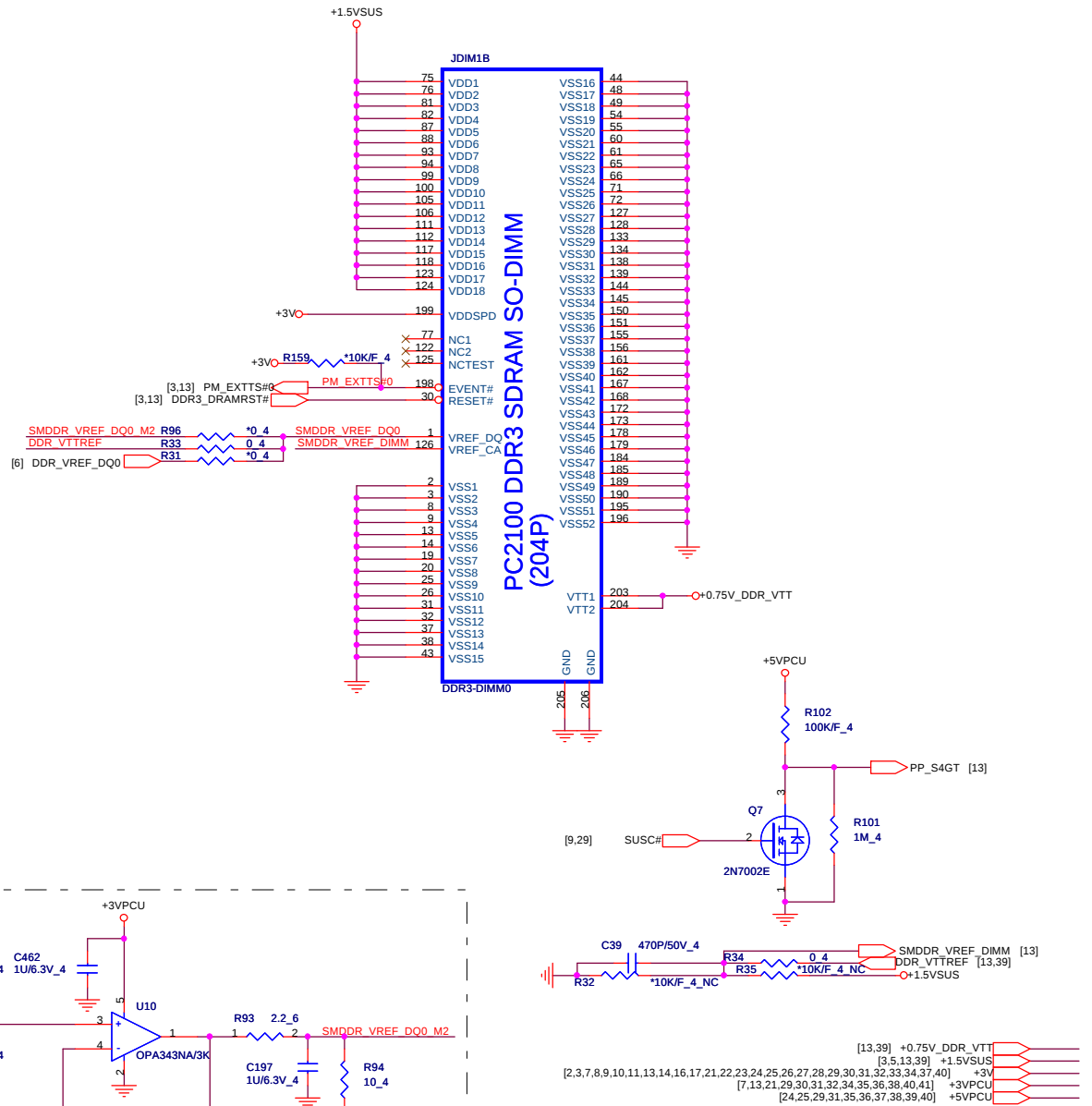
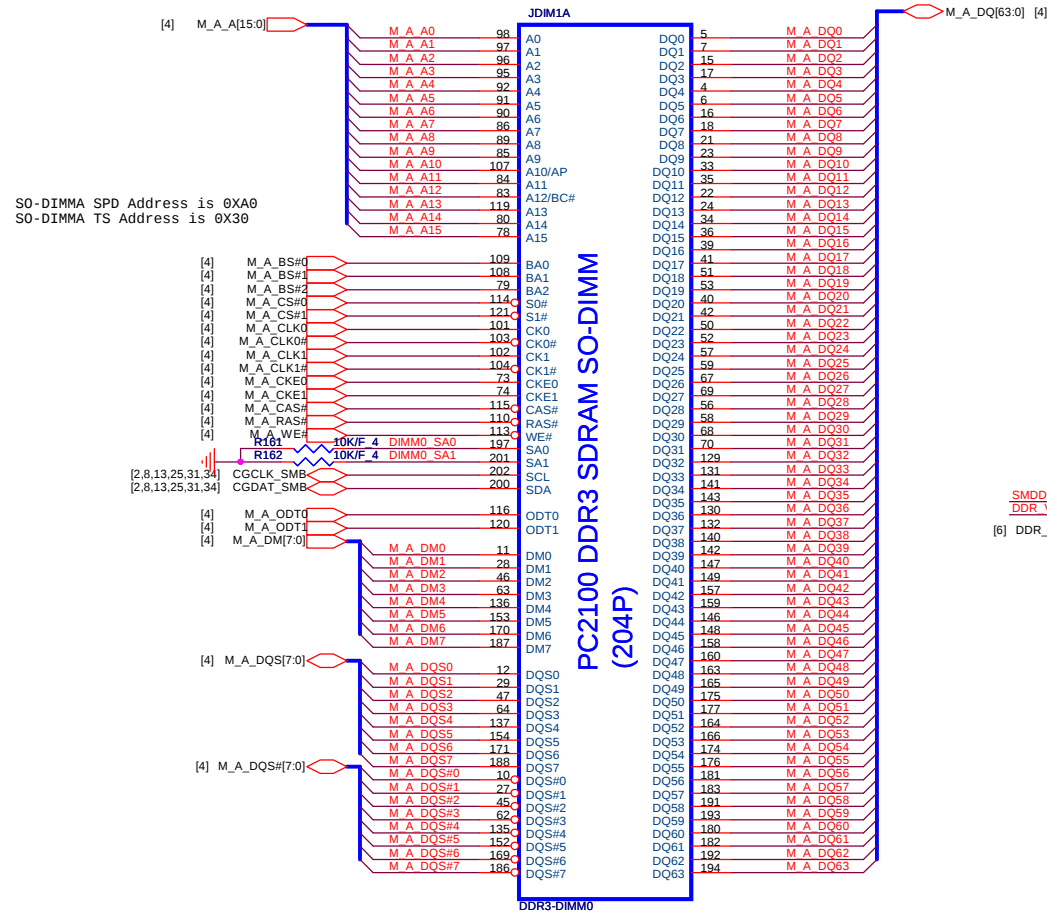


[2,7,8,9,14,15,16,28,29,33,36]	+1.05V
[3,5,10,33,37,38]	+1.1V_VTT
[5,10,16,33,36,40]	+1.8V
[2,3,7,8,9,10,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40]	+3V
[8,9,10,31,33,40]	+3VSS
[21,22,24,25,30,31,32,34,40]	+5V
[40]	+5VSS

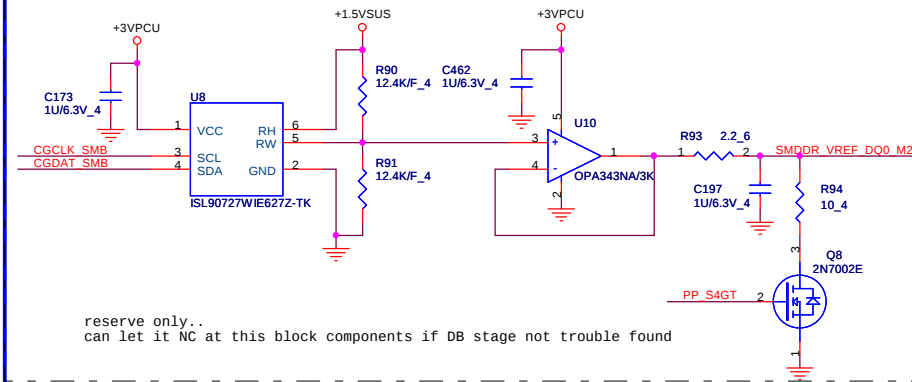
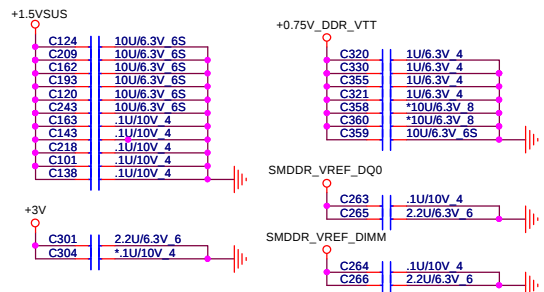


PROJECT : UP67
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Size Custom	Document Number PCH 5/6 (POWER)	Rev 1A
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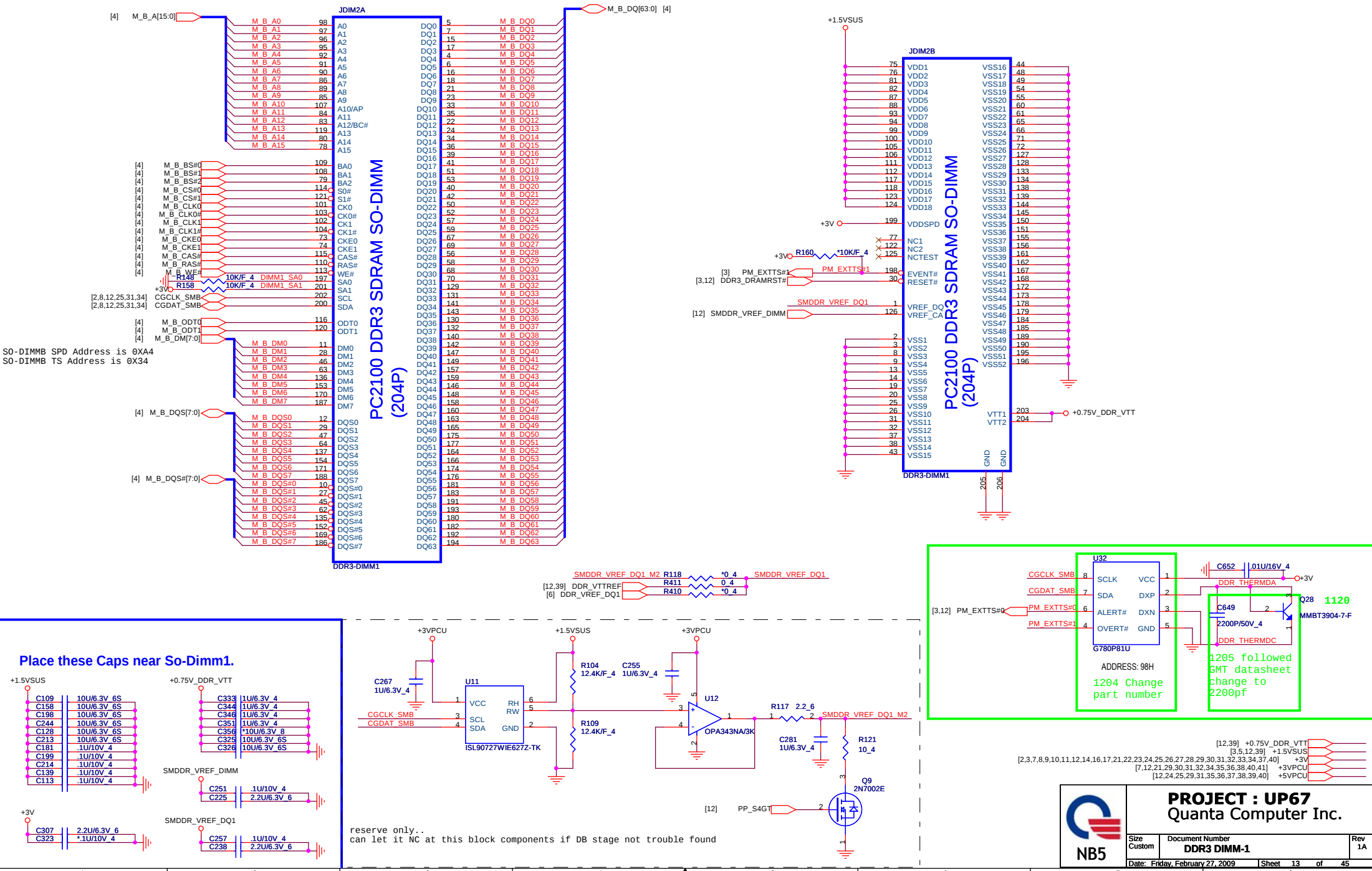


Place these Caps near So-Dimm0.

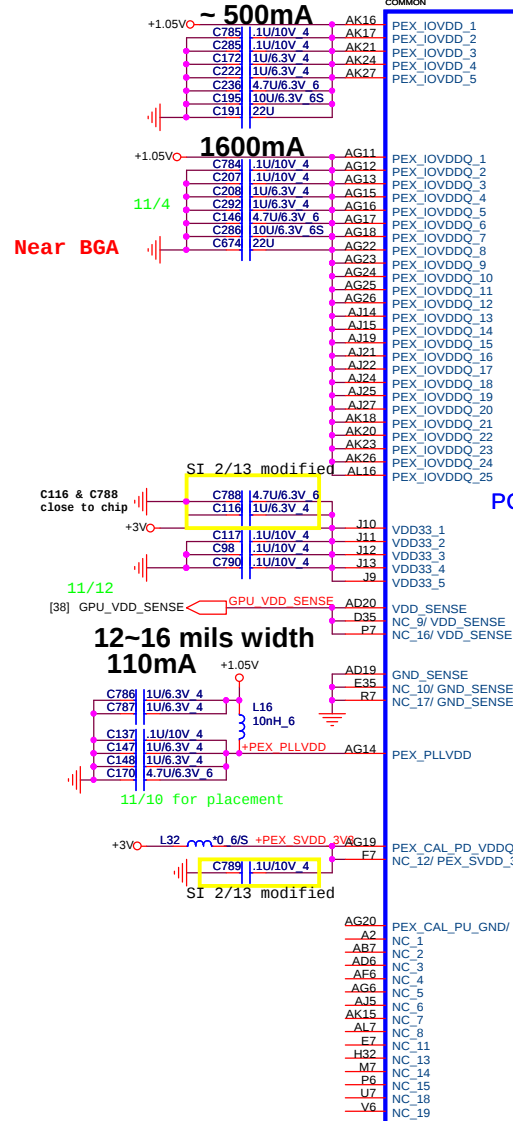


PROJECT : UP67
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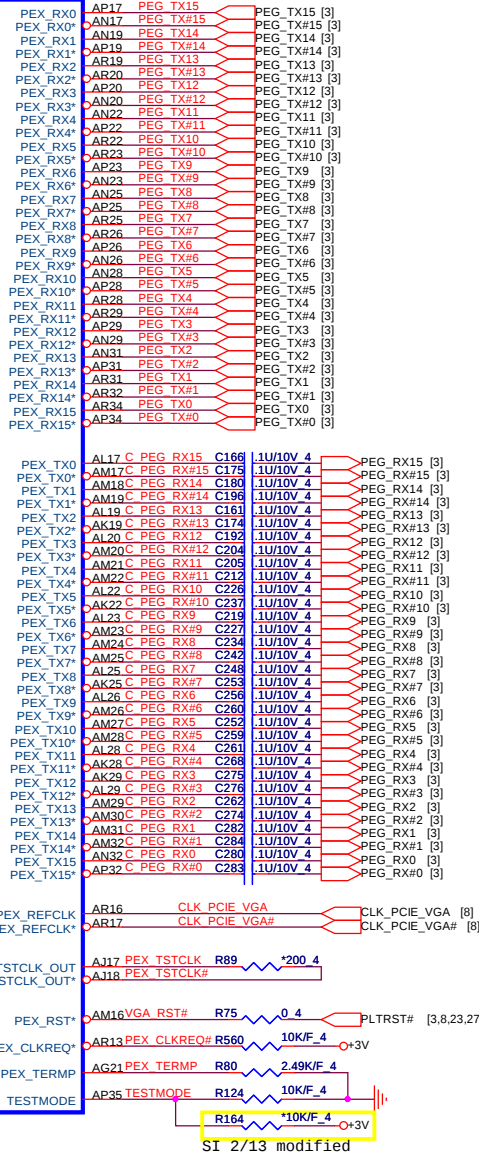
Size	Document Number	Rev
Custom	DDR3 DIMM-0	1A
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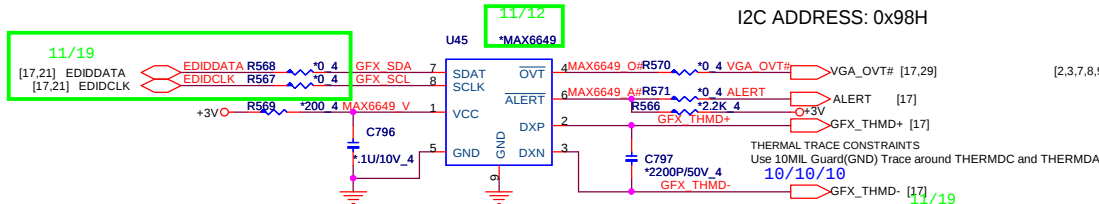
PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A



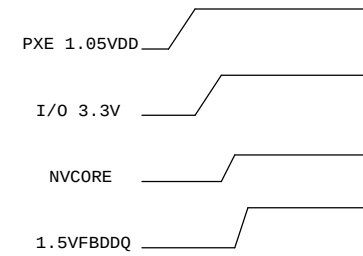
PCI EXPRESS



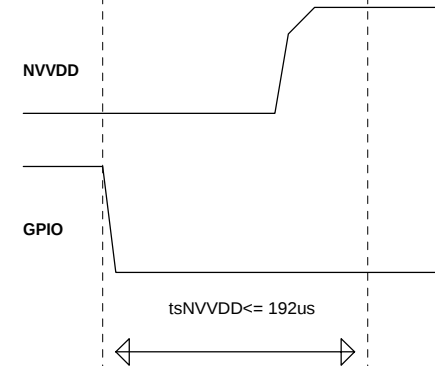
VGA Thermal Circuit



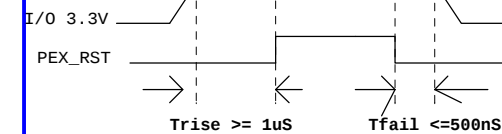
power up sequence



NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time



PEX_RST timing



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Size	Document Number	Rev
Custom	N10X (PCIE I/F) 1/5	1A
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U35B

BGA669-NVIDIA-NB9P-GS
COMMON12/02 modify
package for N10

[19] FBA_CMD0 V32 FBA_CMD0
[19] FBA_CMD1 W31 FBA_CMD1
[19] FBA_CMD2 Y32 FBA_CMD2
[19] FBA_CMD3 AB35 FBA_CMD3
[19] FBA_CMD4 AB34 FBA_CMD4
[19] FBA_CMD5 W35 FBA_CMD5
[19] FBA_CMD6 W33 FBA_CMD6
[19] FBA_CMD7 W30 FBA_CMD7
[19] FBA_CMD8 T34 FBA_CMD8
[19] FBA_CMD9 T35 FBA_CMD9
[19] FBA_CMD10 T35 FBA_CMD10
[19] FBA_CMD11 AB31 FBA_CMD11
[19] FBA_CMD12 Y30 FBA_CMD12
[19] FBA_CMD13 Y32 FBA_CMD13
[19] FBA_CMD14 AA30 FBA_CMD14
[19] FBA_CMD15 AA32 FBA_CMD15
[19] FBA_CMD16 Y33 FBA_CMD16
[19] FBA_CMD17 U32 FBA_CMD17
[19] FBA_CMD18 Y31 FBA_CMD18
[19] FBA_CMD19 U34 FBA_CMD19
[19] FBA_CMD20 Y35 FBA_CMD20
[19] FBA_CMD21 W34 FBA_CMD21
[19] FBA_CMD22 Y30 FBA_CMD22
[19] FBA_CMD23 U35 FBA_CMD23
[19] FBA_CMD24 U30 FBA_CMD24
[19] FBA_CMD25 U33 FBA_CMD25
[19] FBA_CMD26 AB30 FBA_CMD26
[19] FBA_CMD27 AB33 FBA_CMD27
[19] FBA_CMD28 T33 FBA_CMD28
[19] FBA_CMD29 W29 FBA_CMD29
[19] FBA_CMD30 FBA_CMD30

12/02 modify
package for N10

VMA_DM0 P32 FBA_DQM0
VMA_DM1 H34 FBA_DQM1
VMA_DM2 J30 FBA_DQM2
VMA_DM3 P30 FBA_DQM3
VMA_DM4 AF32 FBA_DQM4
VMA_DM5 AL32 FBA_DQM5
VMA_DM6 AL34 FBA_DQM6
VMA_DM7 AF35 FBA_DQM7
VMA_DQS0 L34 FBA_DQS_WP0
VMA_DQS1 H35 FBA_DQS_WP1
VMA_DQS2 J32 FBA_DQS_WP2
VMA_DQS3 N31 FBA_DQS_WP3
VMA_DQS4 AE31 FBA_DQS_WP4
VMA_DQS5 AJ32 FBA_DQS_WP5
VMA_DQS6 AL34 FBA_DQS_WP6
VMA_DQS7 AC33 FBA_DQS_WP7
VMA_RDQS0 L35 FBA_DQS_RN0
VMA_RDQS1 G35 FBA_DQS_RN1
VMA_RDQS2 H31 FBA_DQS_RN2
VMA_RDQS3 N32 FBA_DQS_RN3
VMA_RDQS4 AD32 FBA_DQS_RN4
VMA_RDQS5 AJ31 FBA_DQS_RN5
VMA_RDQS6 AJ35 FBA_DQS_RN6
VMA_RDQS7 AC34 FBA_DQS_RN7

P29 FBA_WCK0
R29 FBA_WCK0_N
L28 FBA_WCK1
M29 FBA_WCK1_N
AG29 FBA_WCK2
AH29 FBA_WCK2_N
AD29 FBA_WCK3
AE29 FBA_WCK3_N

+1.5V

MEMORY I/F A

FBA_CLK0 T32 VMA_CLK0
FBA_CLK0# T31 VMA_CLK0#
FBA_CLK1 AC31 VMA_CLK1
FBA_CLK1# AC30 VMA_CLK1#

FB_VREF

J27 +FB_VREF1 R105 +1K/F 4 +1.5V
C230 1U/10V 4

15mils width

For Debug only
FBA_DEBUG T30 FBA_DEBUG R110 +10K/F 4 +1.5V

15mils width

FB_DLLAVDD0 AG27 +FB_PLLAVDD L17 PB1Y60808T-301Y-N 6 +1.05V
FB_PLLAVDD0 AE27 C254 4.7U/6.3V 6 SI 2/13 modified
C171 1U/6.3V 4

Memory clk spread :
down 1.25% (
30-33KHZ)
use internal Vref, ext
divider no stuff

+1.5V

C145 0.01U/16V 4
C246 0.01U/16V 4
C687 0.01U/16V 4
C250 0.01U/16V 4
C258 1U/10V 4
C223 1U/10V 4
C653 1U/10V 4
C391 0.047U/16V 4
C655 0.047U/16V 4
C303 0.047U/16V 4
C800 4.7U/6.3V 6
C801 4.7U/6.3V 6

SI 2/13 modified

U35C

BGA669-NVIDIA-NB9P-GS
COMMON12/02 modify
package for N10

[20] FBC_CMD0 C17 FBC_CMD0
[20] FBC_CMD1 D18 FBC_CMD1
[20] FBC_CMD2 F21 FBC_CMD2
[20] FBC_CMD3 A23 FBC_CMD3
[20] FBC_CMD4 D21 FBC_CMD4
[20] FBC_CMD5 B23 FBC_CMD5
[20] FBC_CMD6 E20 FBC_CMD6
[20] FBC_CMD7 C21 FBC_CMD7
[20] FBC_CMD8 F20 FBC_CMD8
[20] FBC_CMD9 F19 FBC_CMD9
[20] FBC_CMD10 F23 FBC_CMD10
[20] FBC_CMD11 A22 FBC_CMD11
[20] FBC_CMD12 C22 FBC_CMD12
[20] FBC_CMD13 B17 FBC_CMD13
[20] FBC_CMD14 F24 FBC_CMD14
[20] FBC_CMD15 C25 FBC_CMD15
[20] FBC_CMD16 E22 FBC_CMD16
[20] FBC_CMD17 C20 FBC_CMD17
[20] FBC_CMD18 B22 FBC_CMD18
[20] FBC_CMD19 A19 FBC_CMD19
[20] FBC_CMD20 D22 FBC_CMD20
[20] FBC_CMD21 D22 FBC_CMD21
[20] FBC_CMD22 E19 FBC_CMD22
[20] FBC_CMD23 D19 FBC_CMD23
[20] FBC_CMD24 F18 FBC_CMD24
[20] FBC_CMD25 C19 FBC_CMD25
[20] FBC_CMD26 F22 FBC_CMD26
[20] FBC_CMD27 C23 FBC_CMD27
[20] FBC_CMD28 B20 FBC_CMD28
[20] FBC_CMD29 A20 FBC_CMD29
[20] FBC_CMD30 FBC_CMD30

12/02 modify
package for N10

VMC_DM0 A16 FBC_DQM0
VMC_DM1 D10 FBC_DQM1
VMC_DM2 F11 FBC_DQM2
VMC_DM3 D15 FBC_DQM3
VMC_DM4 D27 FBC_DQM4
VMC_DM5 D34 FBC_DQM5
VMC_DM6 A34 FBC_DQM6
VMC_DM7 D28 FBC_DQM7

VMC_WDQS0 C14 FBC_DQS_WP0
VMC_WDQS1 A10 FBC_DQS_WP1
VMC_WDQS2 E10 FBC_DQS_WP2
VMC_WDQS3 D14 FBC_DQS_WP3
VMC_WDQS4 F26 FBC_DQS_WP4
VMC_WDQS5 D32 FBC_DQS_WP5
VMC_WDQS6 A32 FBC_DQS_WP6
VMC_WDQS7 B26 FBC_DQS_WP7

VMC_RDQS0 B14 FBC_DQS_RN0
VMC_RDQS1 B10 FBC_DQS_RN1
VMC_RDQS2 D9 FBC_DQS_RN2
VMC_RDQS3 E14 FBC_DQS_RN3
VMC_RDQS4 F26 FBC_DQS_RN4
VMC_RDQS5 A31 FBC_DQS_RN5
VMC_RDQS6 A31 FBC_DQS_RN6
VMC_RDQS7 A26 FBC_DQS_RN7

G14 FBC_WCK0
G15 FBC_WCK0_N
G11 FBC_WCK1
G12 FBC_WCK1_N
G27 FBC_WCK2
G28 FBC_WCK2_N
G24 FBC_WCK3
G25 FBC_WCK3_N

+1.5V

N27 FBVDDQ_28
P27 FBVDDQ_29
R27 FBVDDQ_30
T27 FBVDDQ_31
U27 FBVDDQ_32
V27 FBVDDQ_33
W27 FBVDDQ_34
Y27 FBVDDQ_35
Y27 FBVDDQ_36
Y27 FBVDDQ_37
Y27 FBVDDQ_38

MEMORY I/F C

FB_CAL_PD_VDDQ K27 FB_CAL_PD_VDDQ R98 40.2/F 4 +1.5V

FB_CAL_PU_GND L27 FB_CAL_PU_GND R100 40.2/F 4

FB_CAL_TERM_GND M27 FB_CAL_TERM_GND R107 40.2/F 4 12/16 Modified

FBC_DEBUG G19 FBC_DEBUG R92 10K/F 4 +1.5V

NC/FB_DLLAVDD1 J19

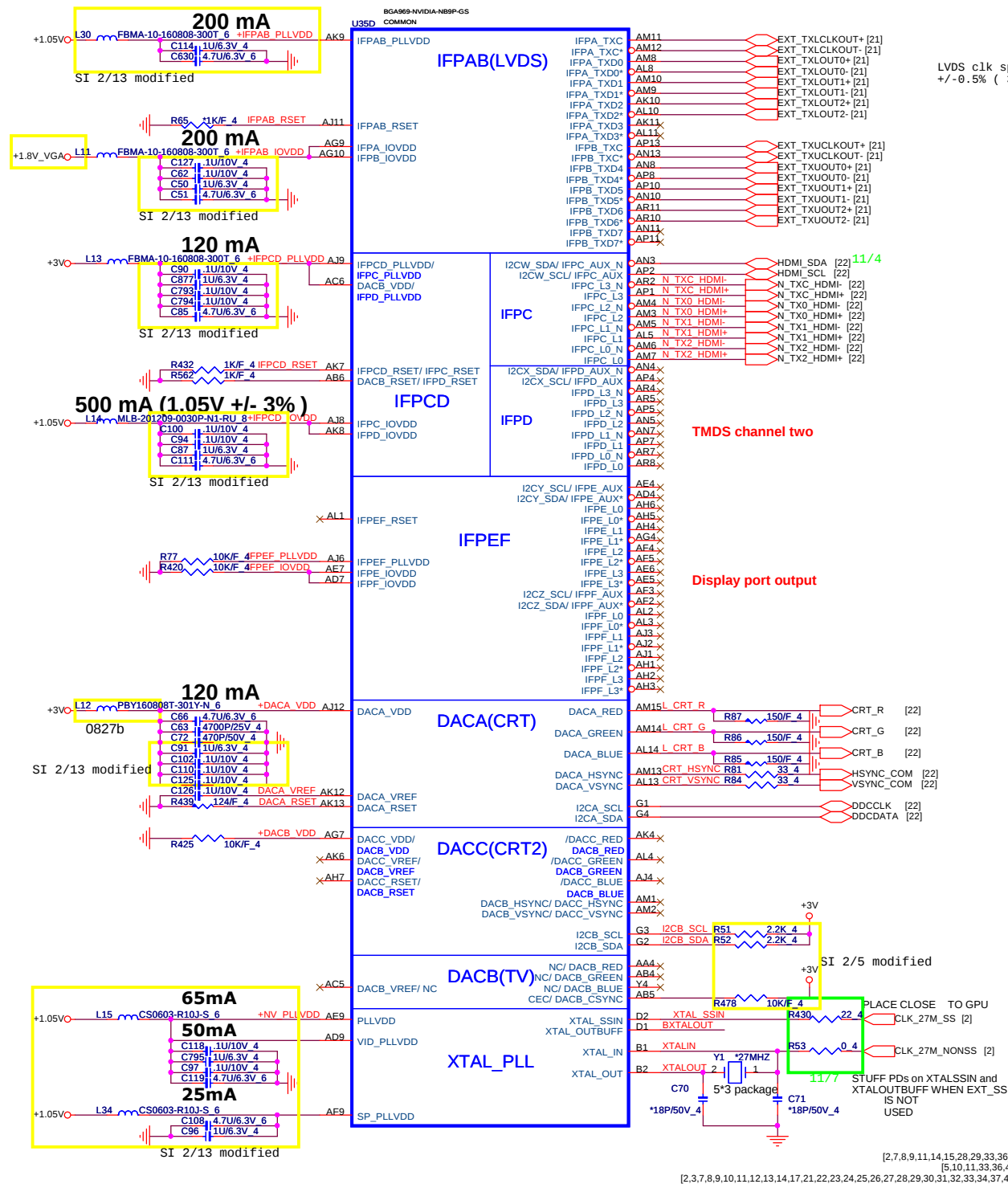
NC/FB_PLLAVDD1 J18

R92 no stuff



PROJECT : UP67
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Size	Document Number	Rev
Custom	N10X (MEMORY I/F) 2/5	1A
Date: Friday, February 27, 2009 Sheet 15 of 45		



LVDS clk spread : Center
+/-0.5% (30~33KHZ)

TMD5 channel two

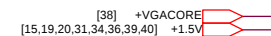
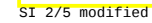
Display port output

PLACE CLOSE TO GPU

$\frac{XTAL_SSIN}{BXTALOUT}$ R431 $\frac{*10K/F}{10K/F}$ 4
 R55 4

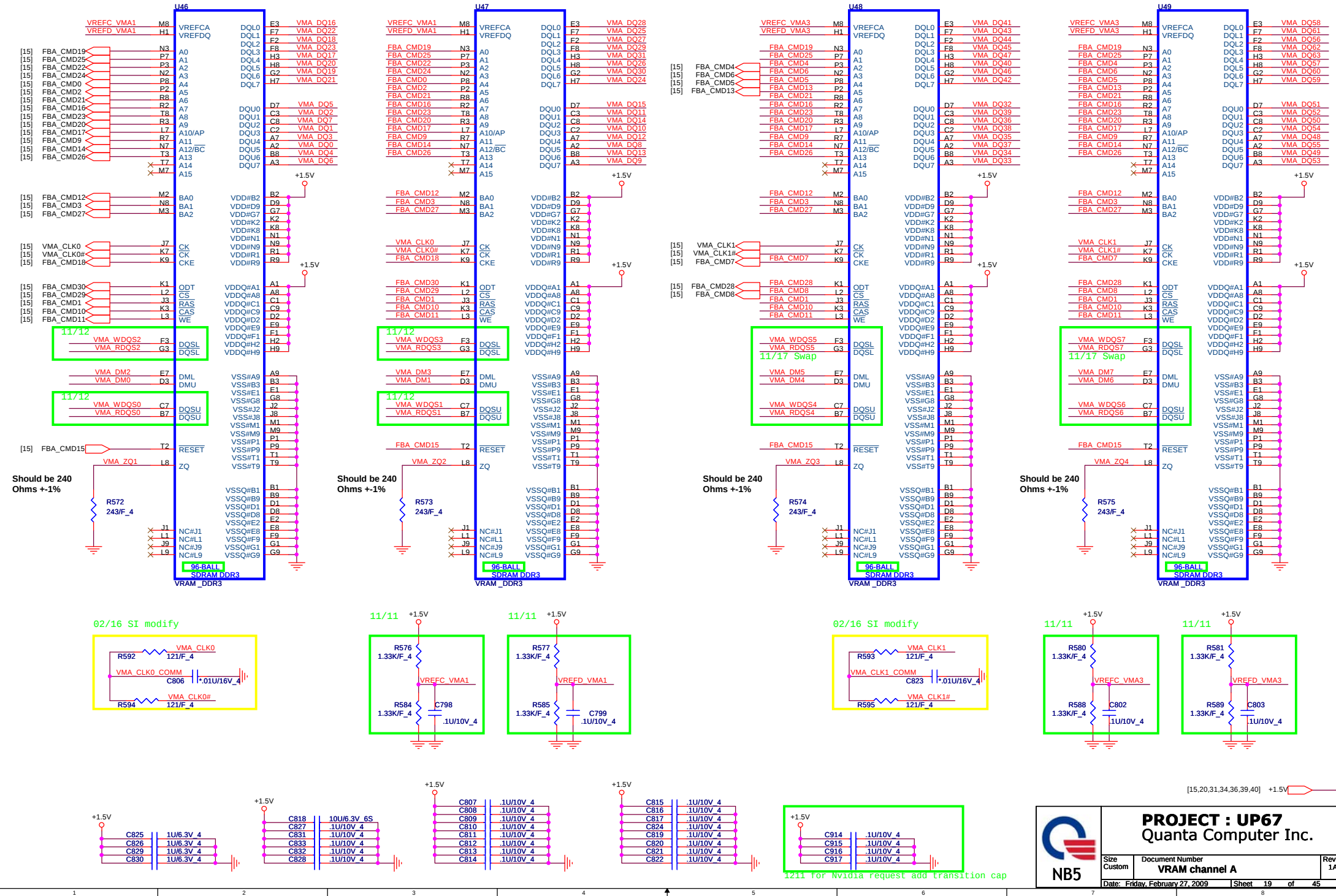
11/4

10 kΩ pull-down only if no spread chip used.



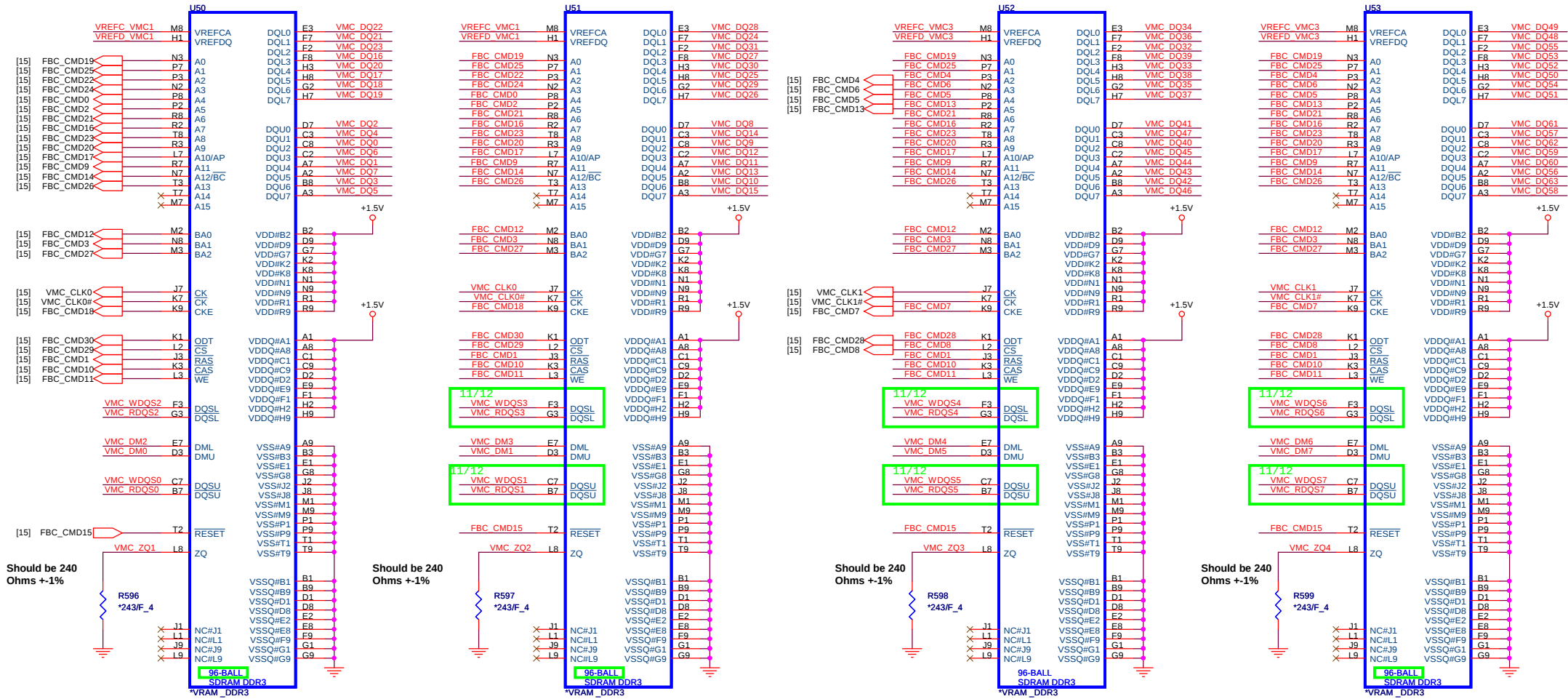
[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

CHANNEL A: 256MB/512MB DDR3



CHANNEL B: 256MB/512MB DDR3

[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]

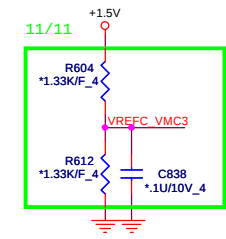
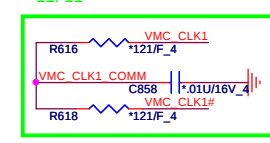
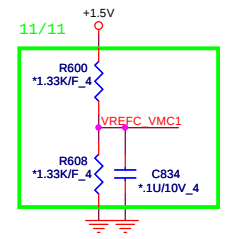
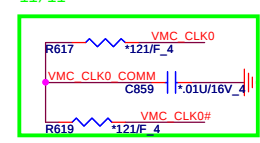


Should be 240 Ohms +-1%

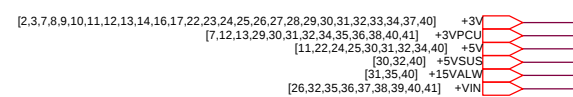
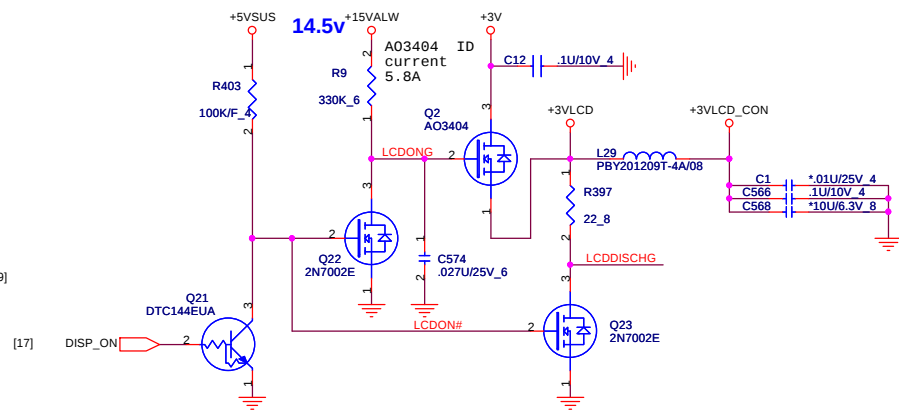
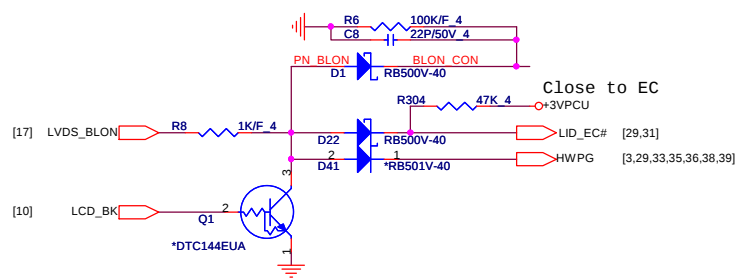
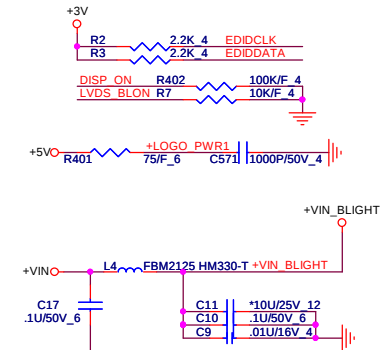
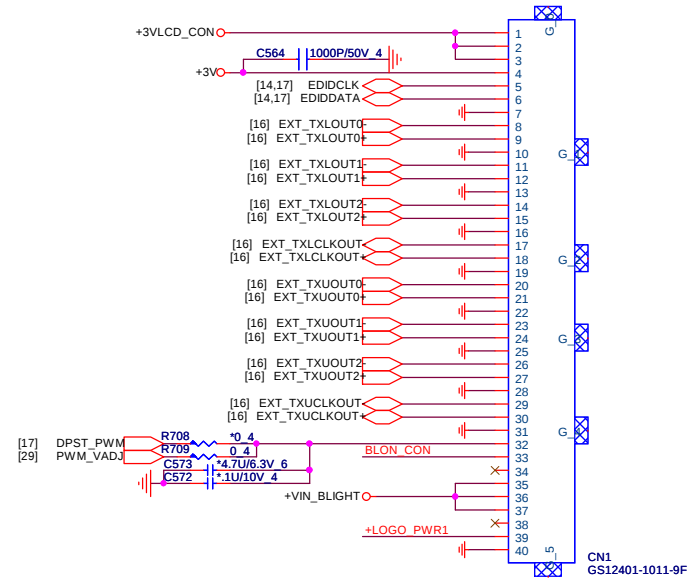
Should be 240 Ohms +-1%

Should be 240 Ohms +-1%

Should be 240 Ohms +-1%



[15,19,31,34,36,39,40] +1.5V

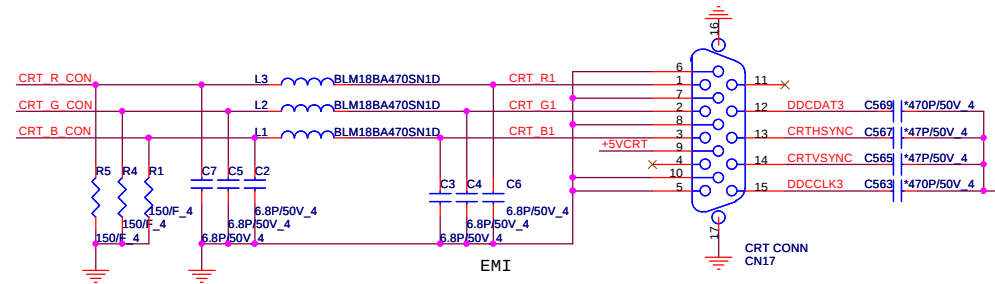
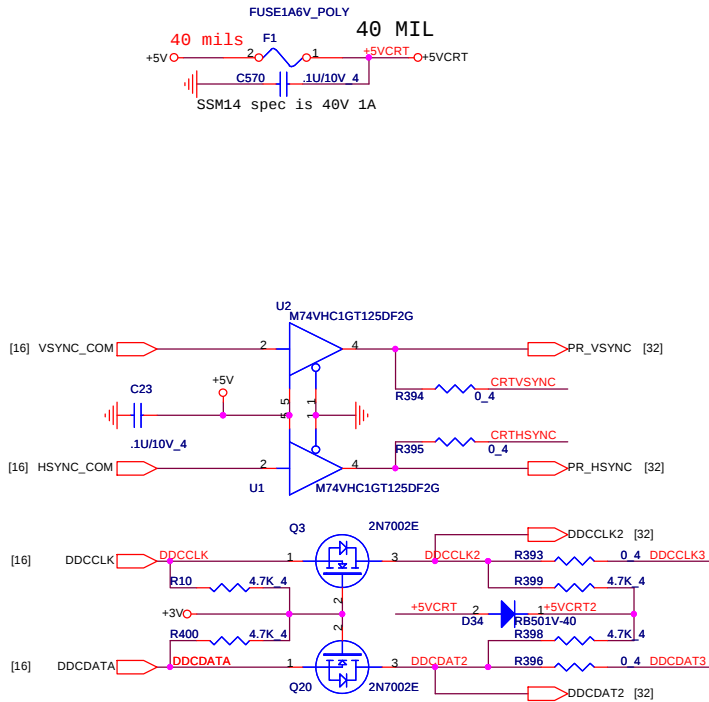


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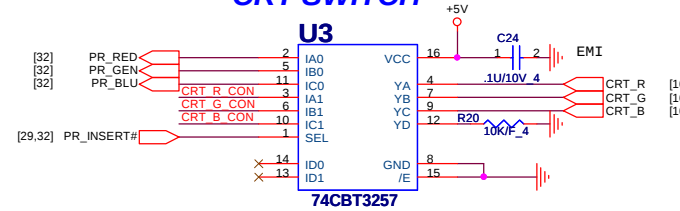
Size	Document Number	Rev
Custom	LCD CONN/LID function	1A

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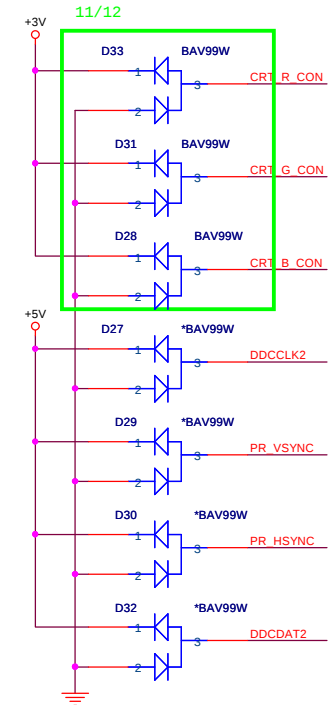
CRT PORT



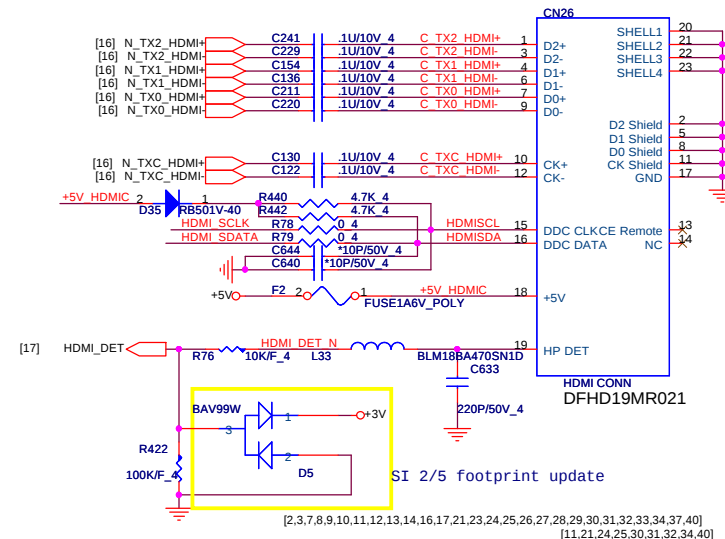
CRT SWITCH



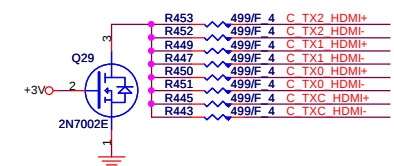
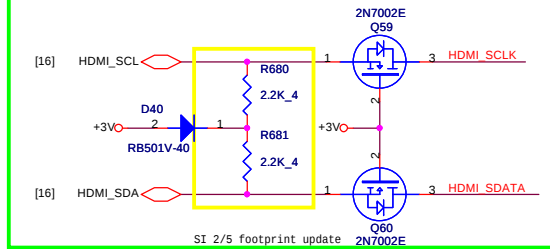
inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect



HDMI PORT

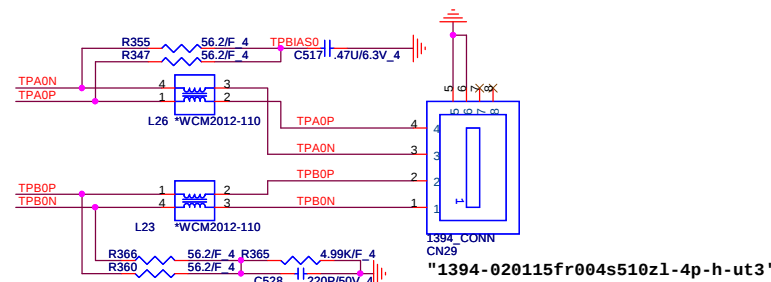
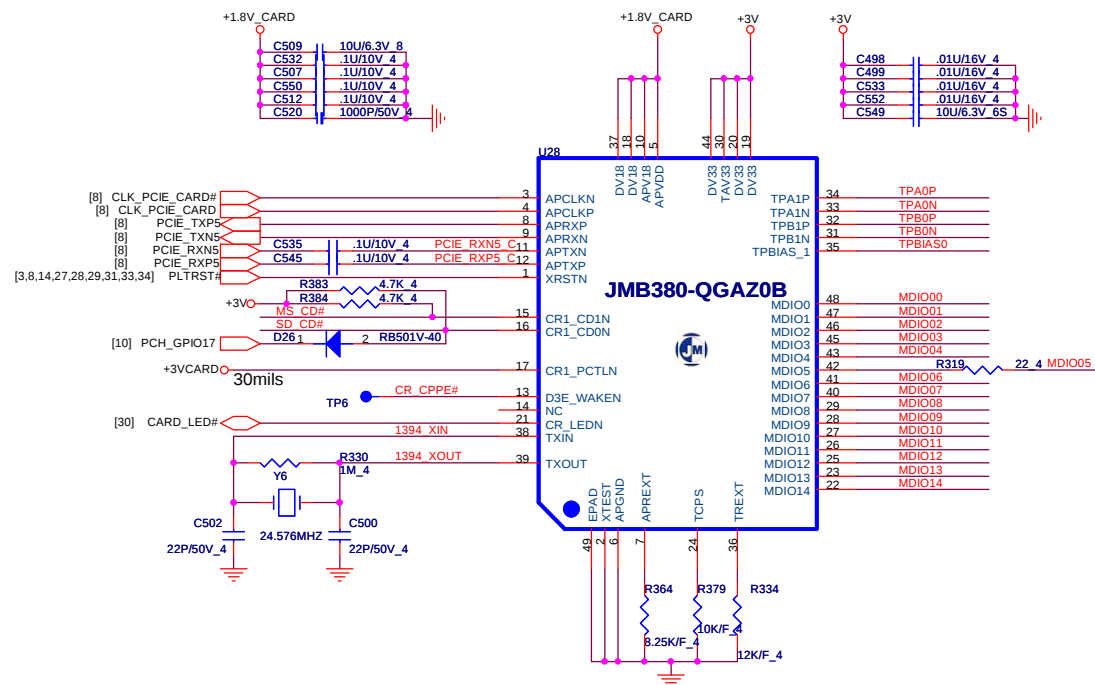


11/17 add level shift



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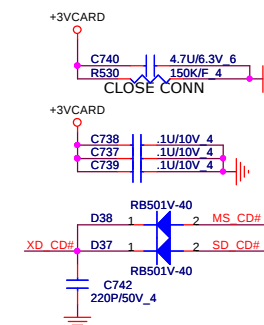
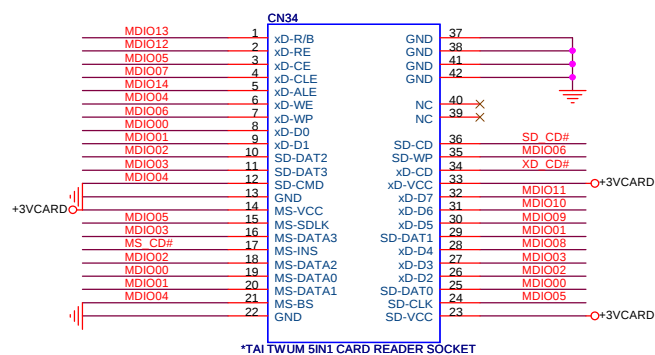
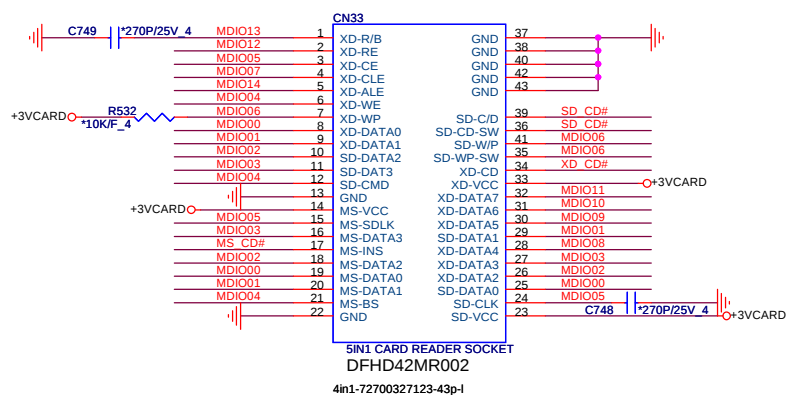
Size	Document Number	Rev
Custom	CRT/HDMI Conn	1A
Date: Friday, February 27, 2009	Sheet 22 of 45	



JMB 380 Note:

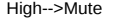
	SD/MMC	MS	XD
MDI00	SD DAT0	MS D0	XD D0
MDI01	SD DAT1	MS D1	XD D1
MDI02	SD DAT2	MS D2	XD D2
MDI03	SD DAT3	MS D3	XD D3
MDI04	SD CMD	MS BS	XD WE#
MDI05	SD CLK	MS SCLK	XD CE#
MDI06	SD WP		XD WP#
MDI07			XD CLE
MDI08	SD DAT4		XD D4
MDI09	SD DAT5		XD D5
MDI10	SD DAT6		XD D6
MDI11	SD DAT7		XD D7
MDI12			XD RE#
MDI13			XD R/B#
MDI14			XD ALE
CR1_LED0	SD1 LED#	MS1 LED#	XD LED#
CR1_TFLN	SD1 PCTL#	MS1 PCTL#	XD TFLN#
CR1_CD0	SD1 CD#		XD CV#
CR1_CD1		MS1 CD#	XD CD#

5 IN1 CARD READER
XD, MMC/SD, MS/MSP

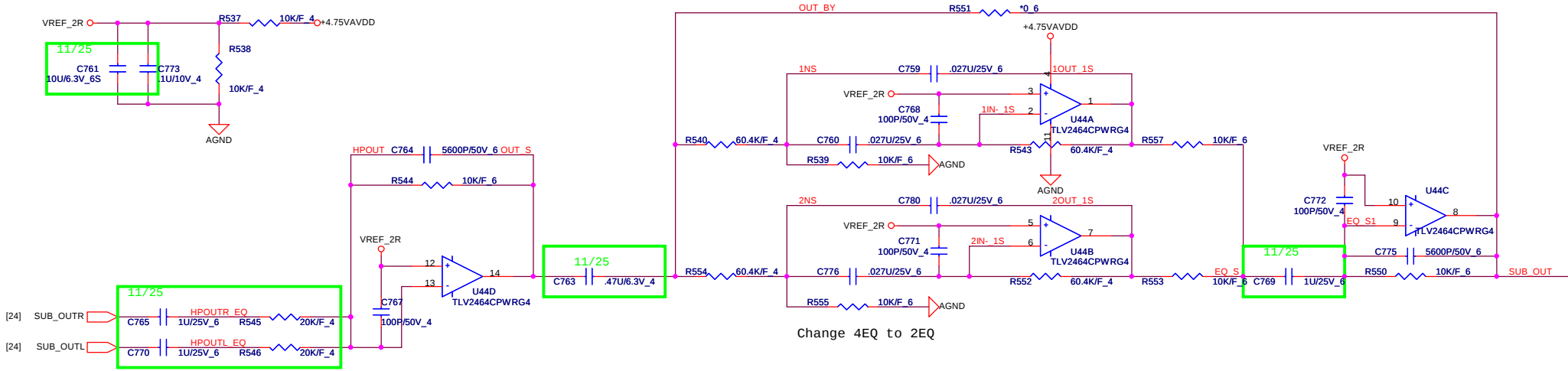




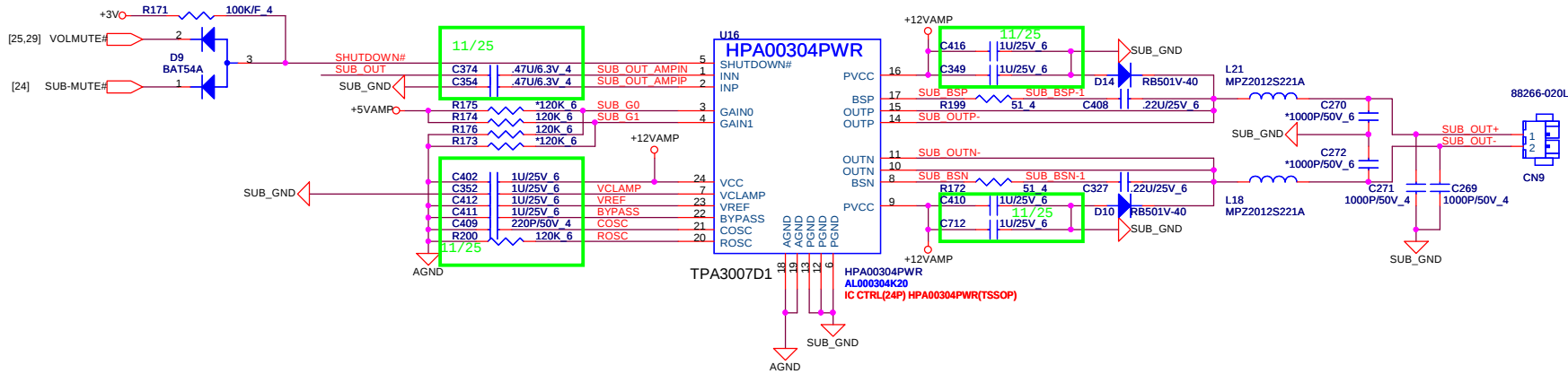
25



[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,26,27,28,29,30,31,32,33,34,37,40] +3V
[11,21,22,24,30,31,32,34,40] +5V
[24,26] +4.75VAVDD
[26] +5VAMP

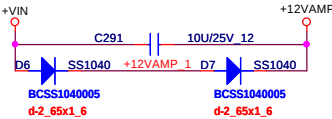


MODEL	UP7
R316	60.4K/F_6
R319	60.4K/F_6
R330	60.4K/F_6
R314	60.4K/F_6
C509	0.027U/25V_6
C510	0.027U/25V_6
C529	0.027U/25V_6
C543	0.027U/25V_6

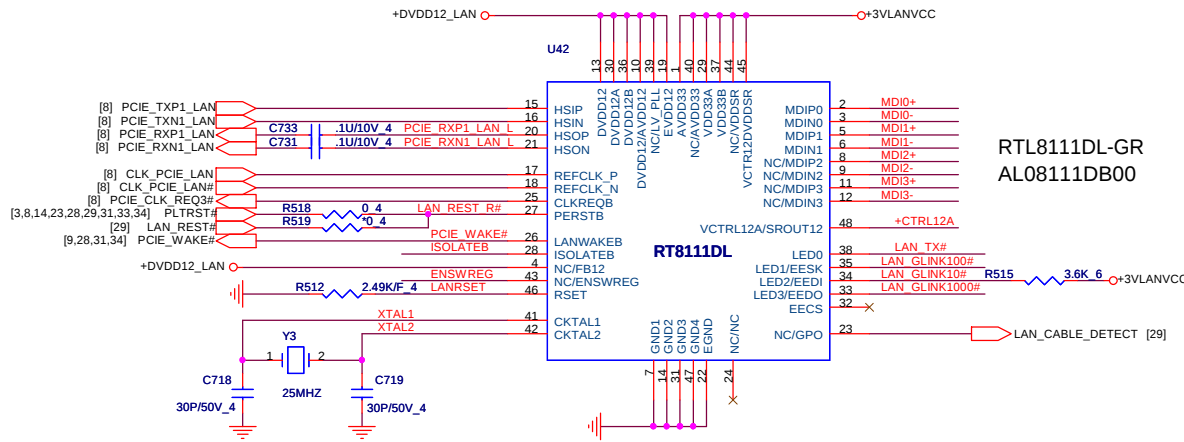


Sub-Woofer power

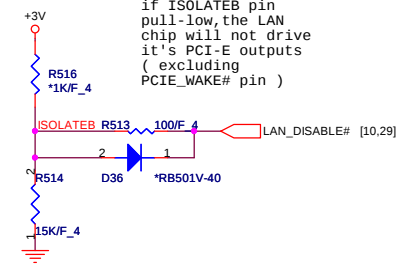
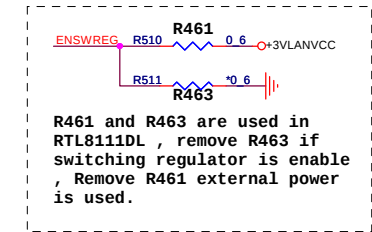
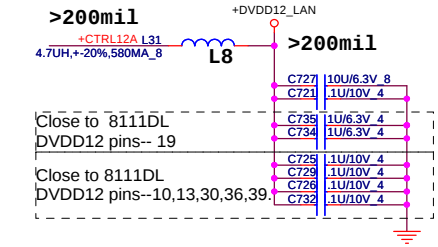
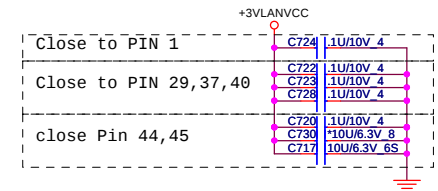
GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36



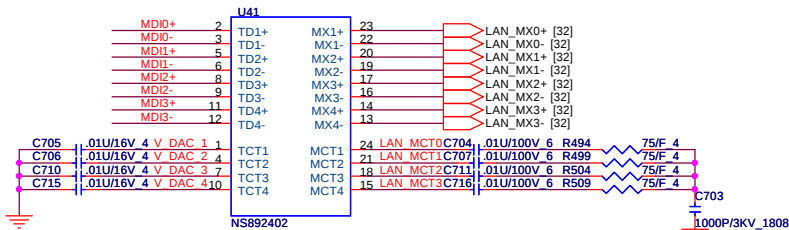
[24,25] +4.75VAVDD
[25] +5VAMP
[21,32,35,36,37,38,39,40,41] +VIN
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,27,28,29,30,31,32,33,34,37,40] +3V



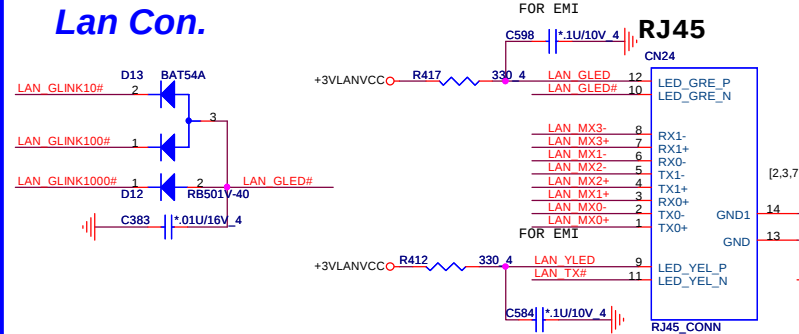
RTL8111DL-GR
AL08111DB00

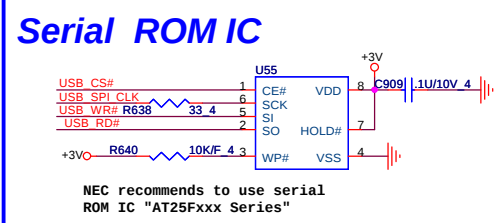
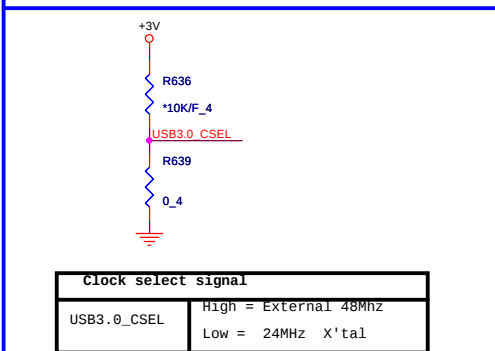
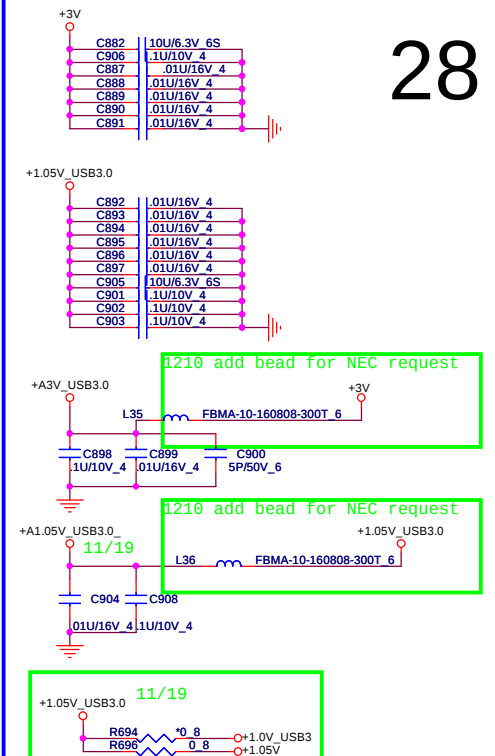
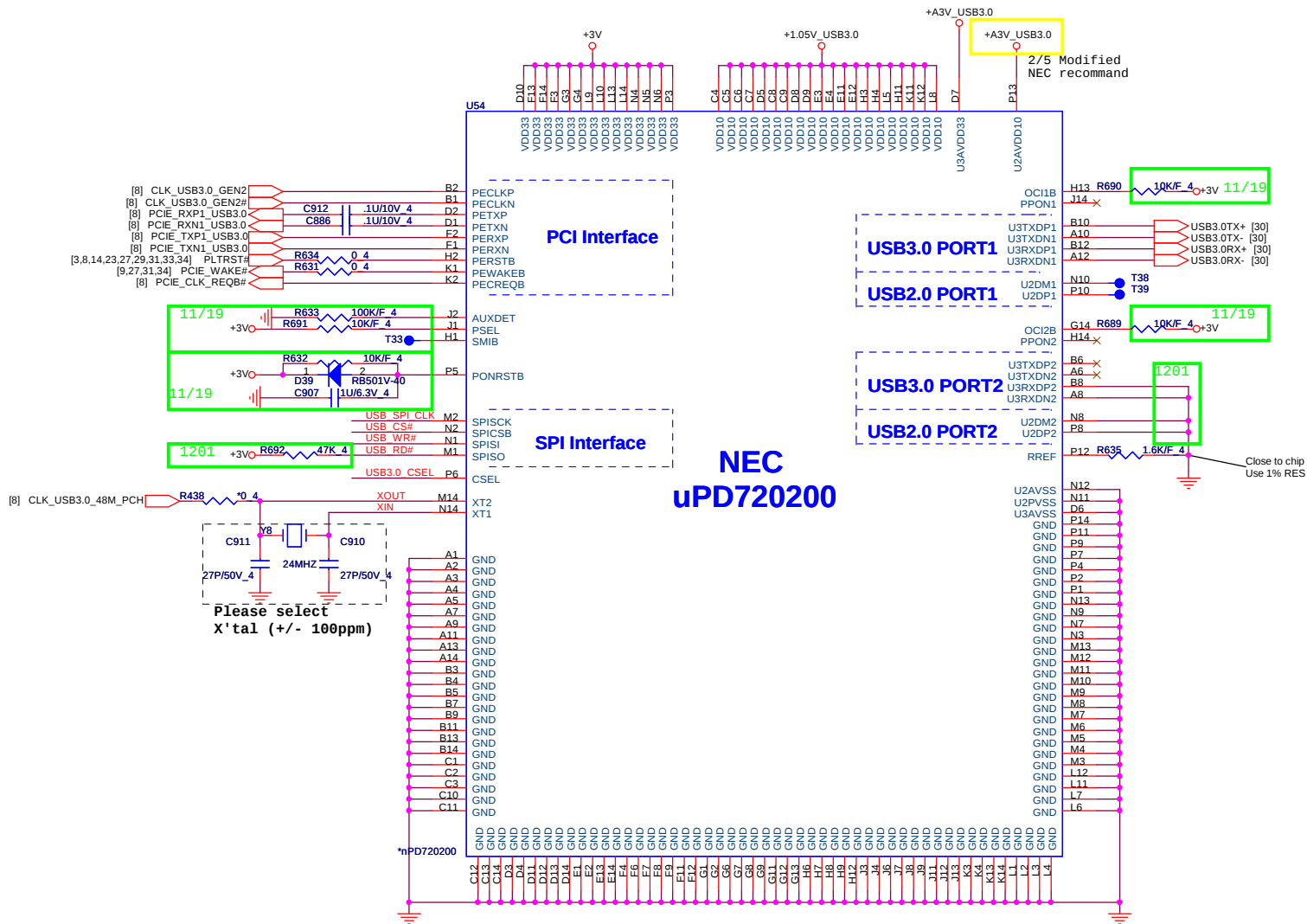


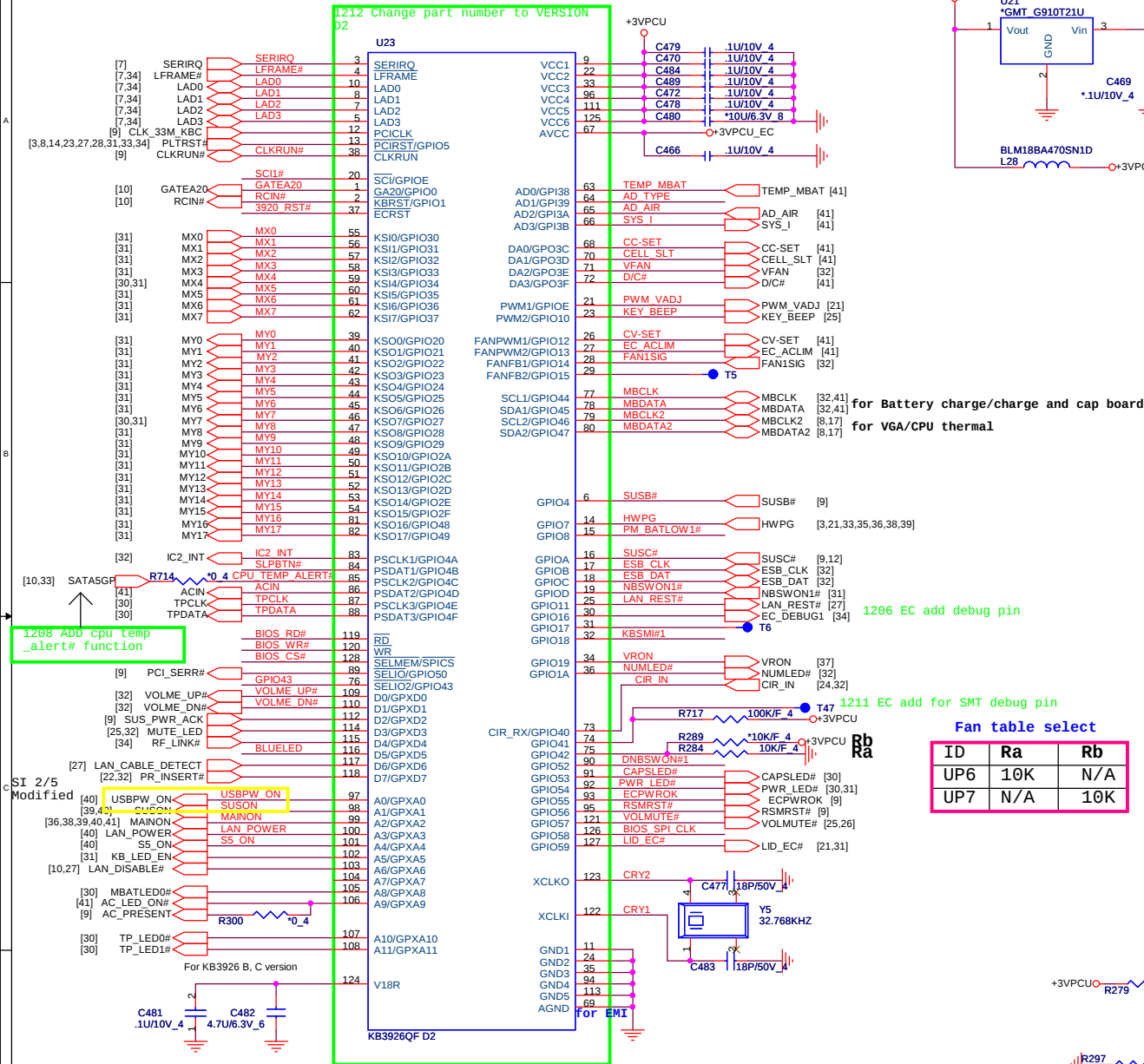
Transformer for 10/100/1000



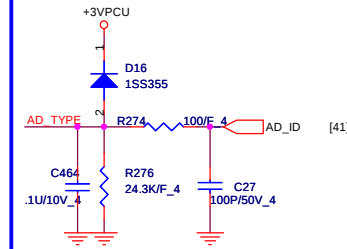
Lan Con.







adapter Type check



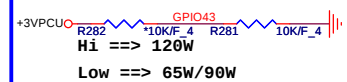
R273

64.9K -->65W CS36492FB17

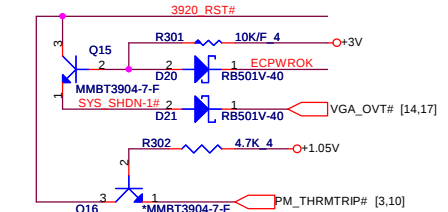
33.2K -->90W CS33322FB13

Change to 1SS355 as Current loss

adapter select for EC



thermal shutdown circuit



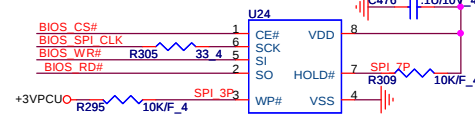
512K byte SPI EC ROM

Socket: DG008000031

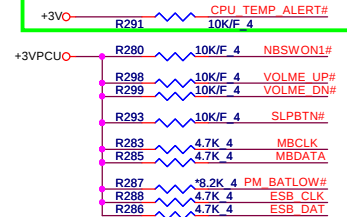
MXIC AKE3KZP0001

WINBOND AKE37ZN0N00

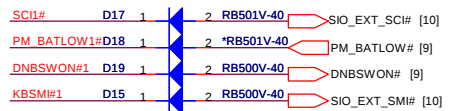
AMIT AKE38ZN0800



1208 ADD cpu temp _alert# function



Change to RB501 as Current loss



Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier

Delete T10 and tie pin 117 from Lan for DSM

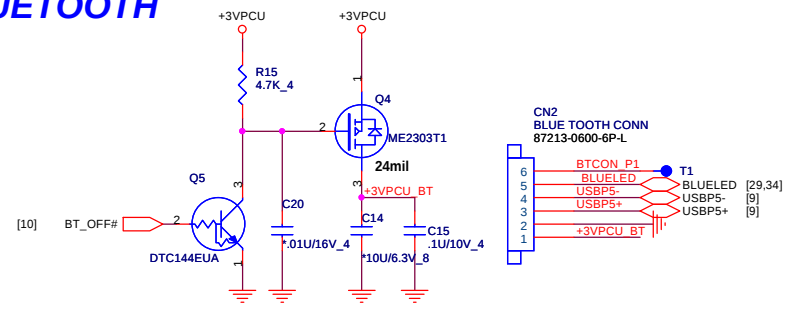


PROJECT : UP67
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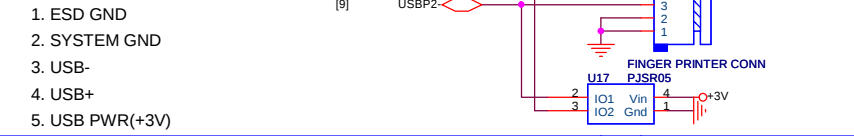
Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A
Date:	Friday, February 27, 2009	Sheet 29 of 45

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[7,12,13,21,30,31,32,34,35,36,38,40,41]
[12,24,25,31,35,36,37,38,39,40]

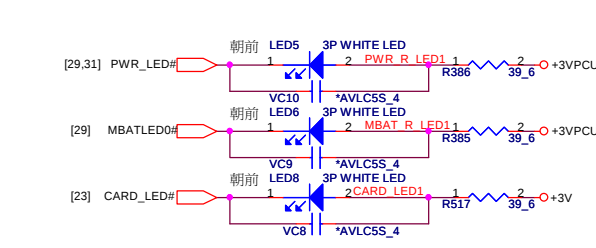
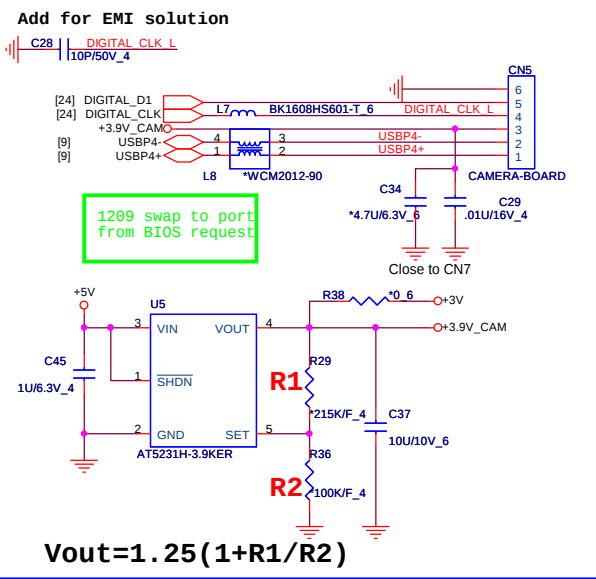
BLUETOOTH



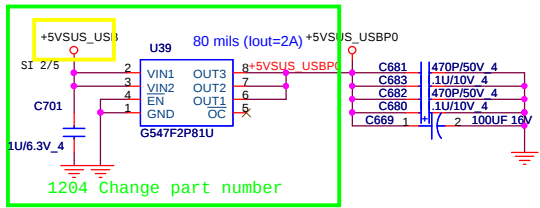
USB fingerprint CON



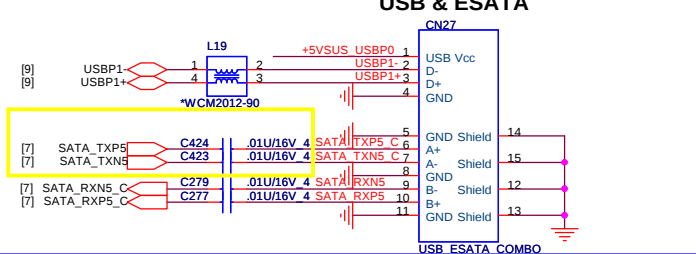
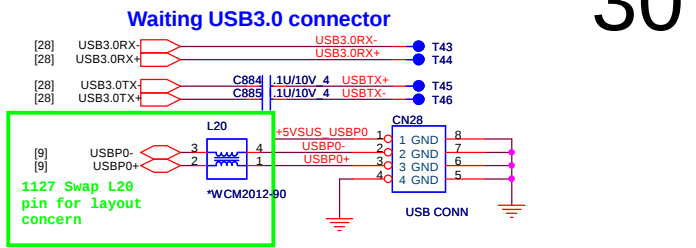
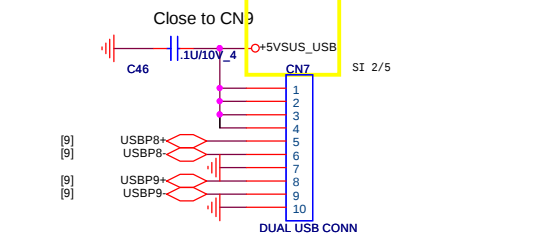
USB CAMERA /DIGITAL MIC CONNECT



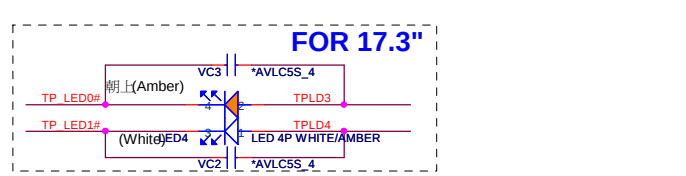
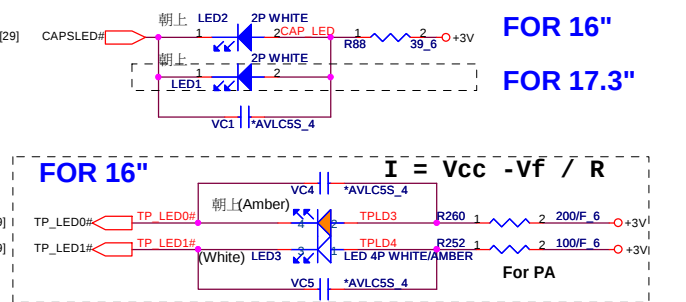
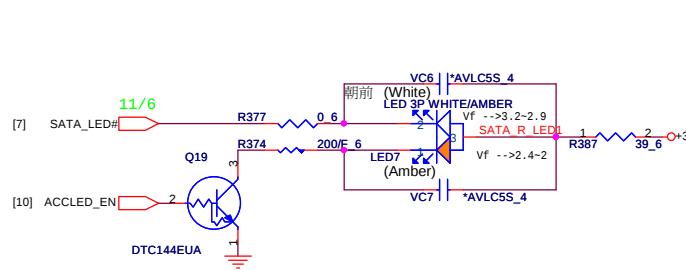
LEFT SIDE USBX1 and E-SATA/USB COMBO



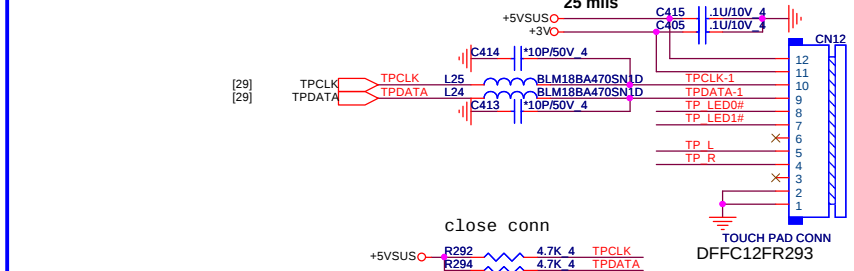
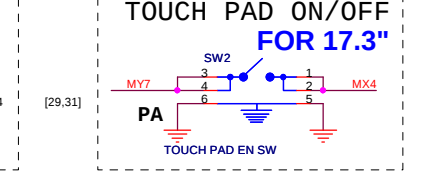
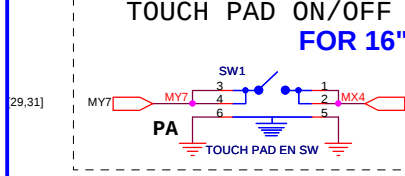
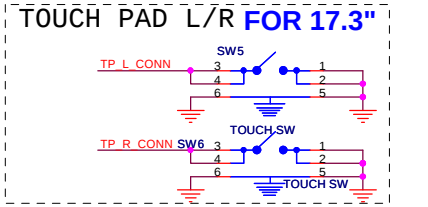
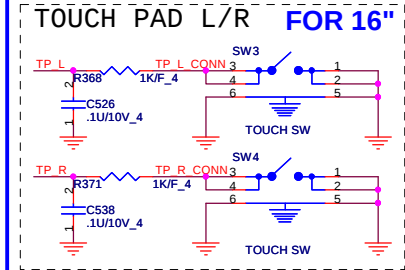
RIGHT SIDE USBX2



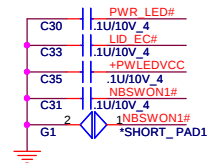
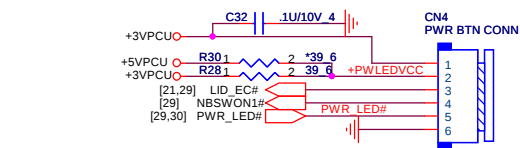
LED



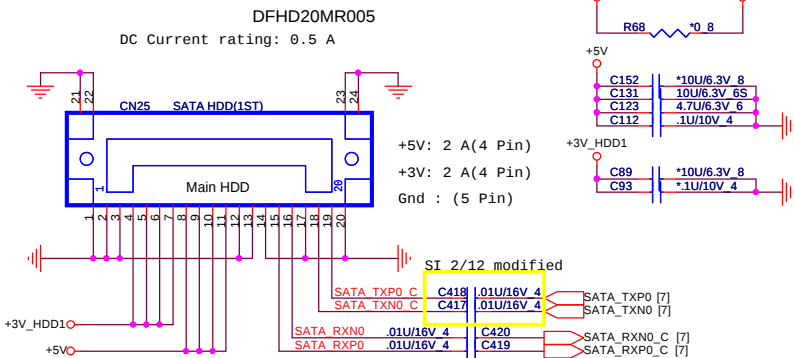
TOUCH PAD CONNECTOR & ON/OFF BOTTOM



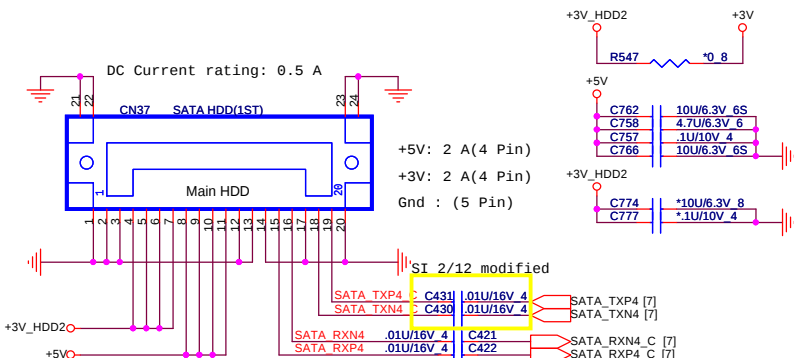
POWER BOTTON CONNECT



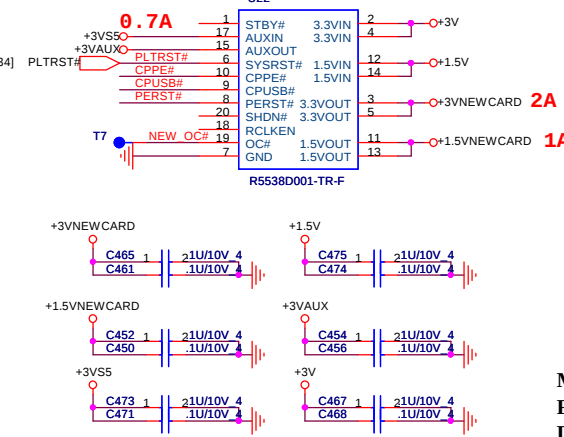
SATA HDD CONNECTOR



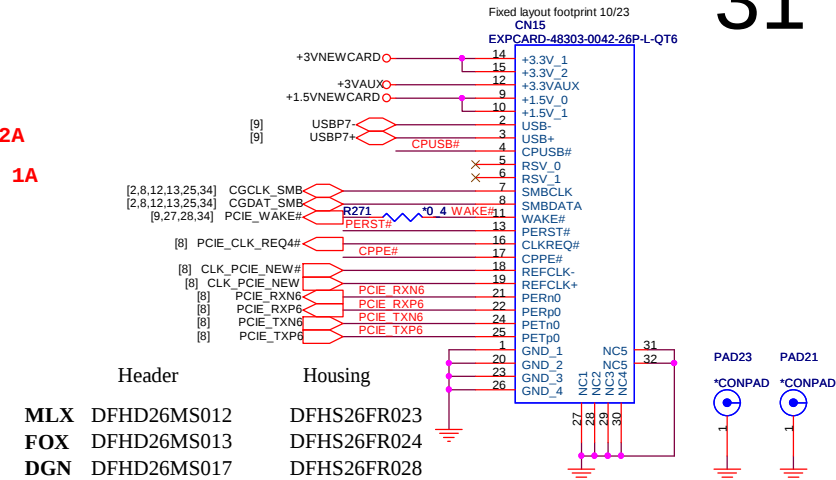
SATA_2 CONNECTOR



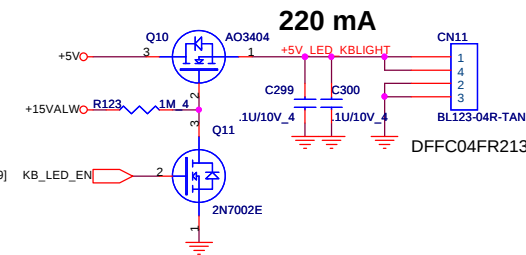
NEWCARD



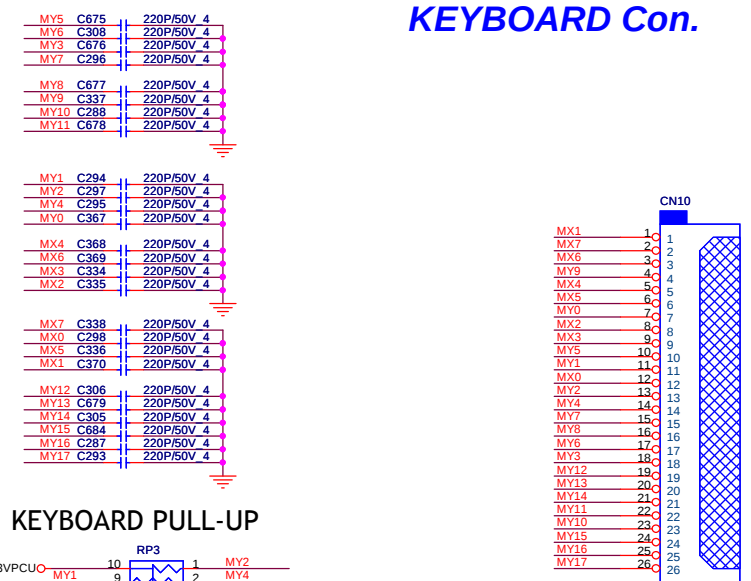
NEWCARD (PCIEXPRESS*1 + USB*1)



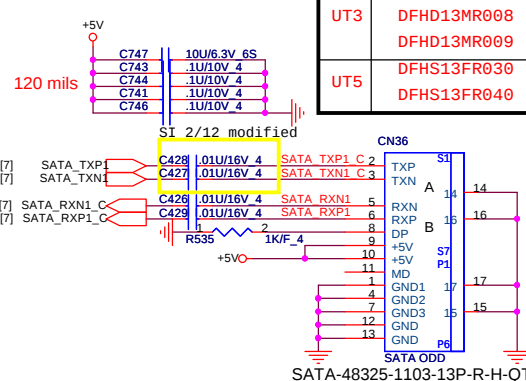
Backlight Keyboard Con.



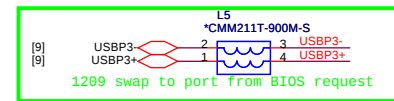
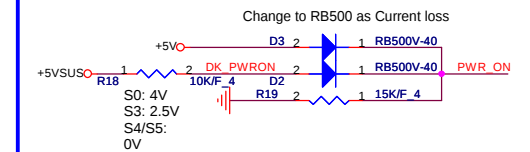
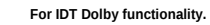
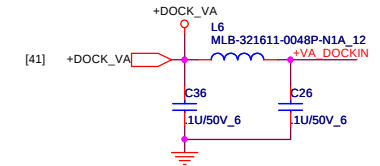
KEYBOARD Con.



SATA CD-ROM



32



[22] PR_GEN

[22] PR_RED

[22] PR_BLU

R16 R11 R13 C22 C13 C19

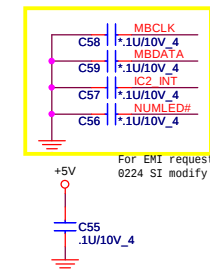
150F_4 150F_4 150F_4 6.8P/50V_4 6.8P/50V_4 6.8P/50V_4

R14 BLM18BA470SN1D CRT GDK C18 6.8P/50V_4

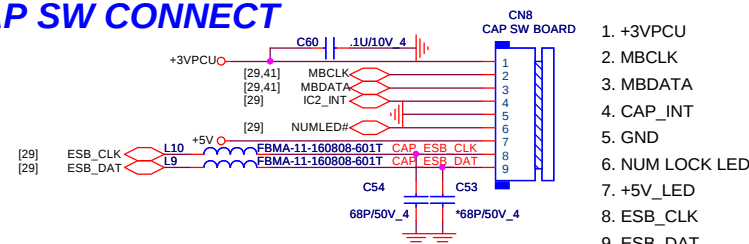
R12 BLM18BA470SN1D CRT RDK C16 6.8P/50V_4

R17 BLM18BA470SN1D CRT BDK C21 6.8P/50V_4

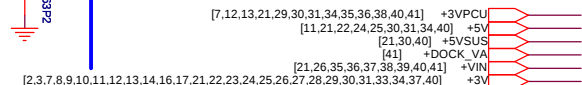
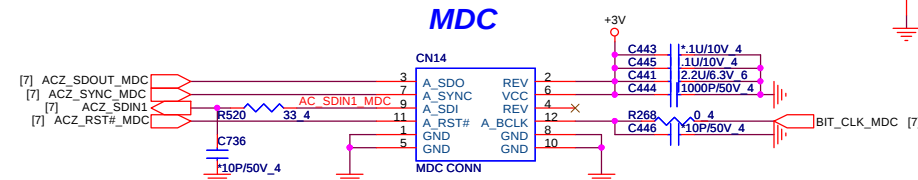
1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V_LED
8. ESB_CLK
9. ESB_DAT



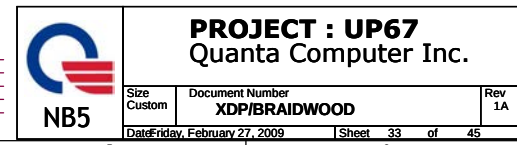
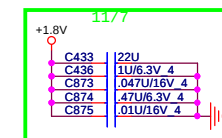
30 MIL



MDC

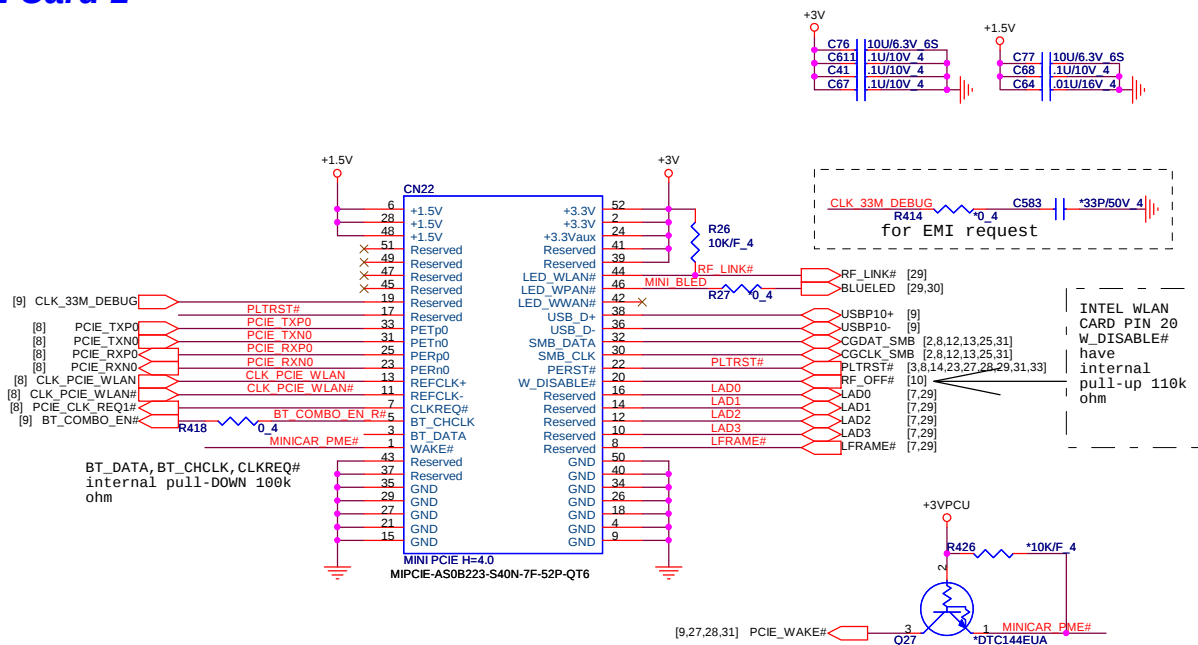


Size Custom	Document Number DOCKING/FAN/CAP/MDC	Rev 1A
Date: Monday, March 02, 2009		Sheet 32 of 45

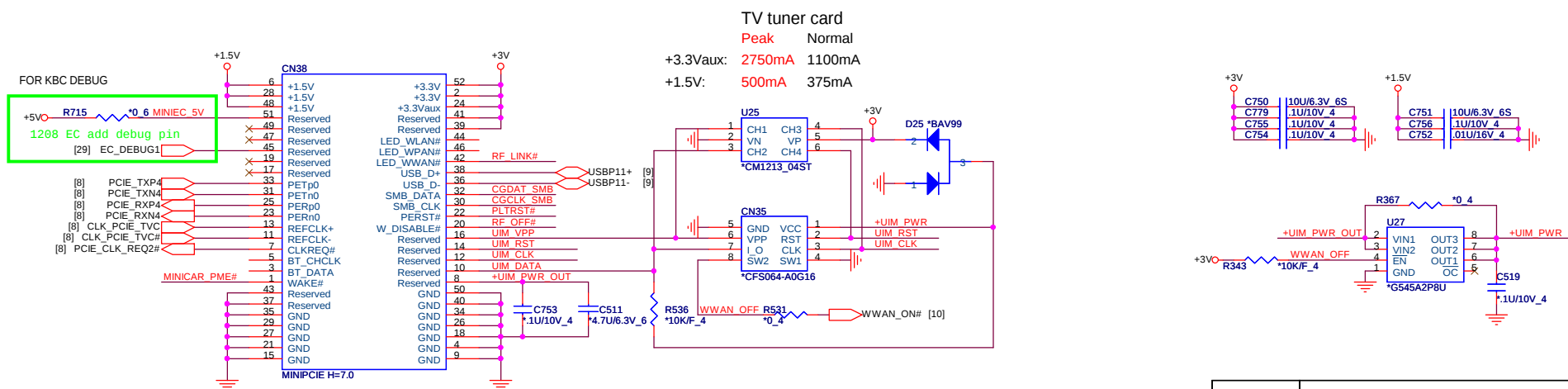


Mini PCI-E Card 1 WLAN

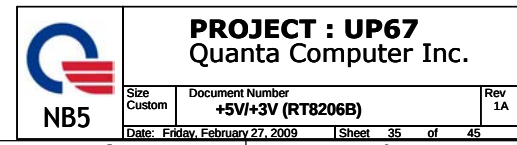
34

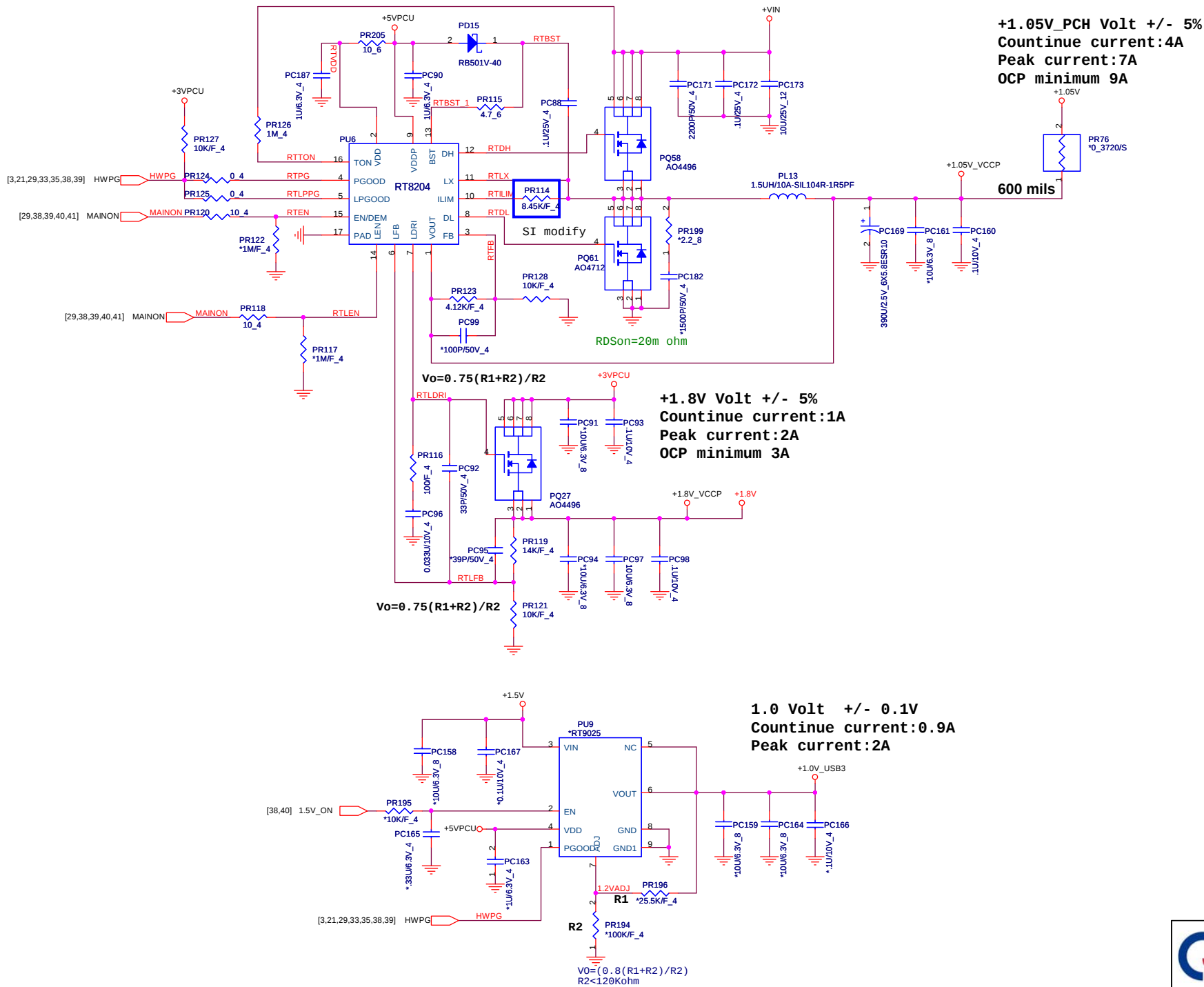


Mini PCI-E Card 2 TV Tuner or WWAN



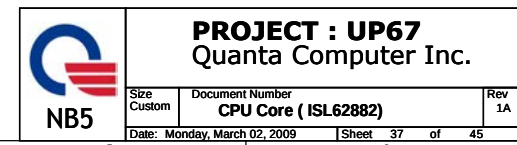
[15,19,20,31,36,39,40] +1.5V
[2,3,7,8,9,10,11,12,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40] +3V
[7,12,13,21,29,30,31,32,35,36,38,40,41] +3VPCU
[11,21,22,24,25,30,31,32,40] +5V





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 Quanta Computer Inc.

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Custom	+5V/+3V (RT8206B)	1A
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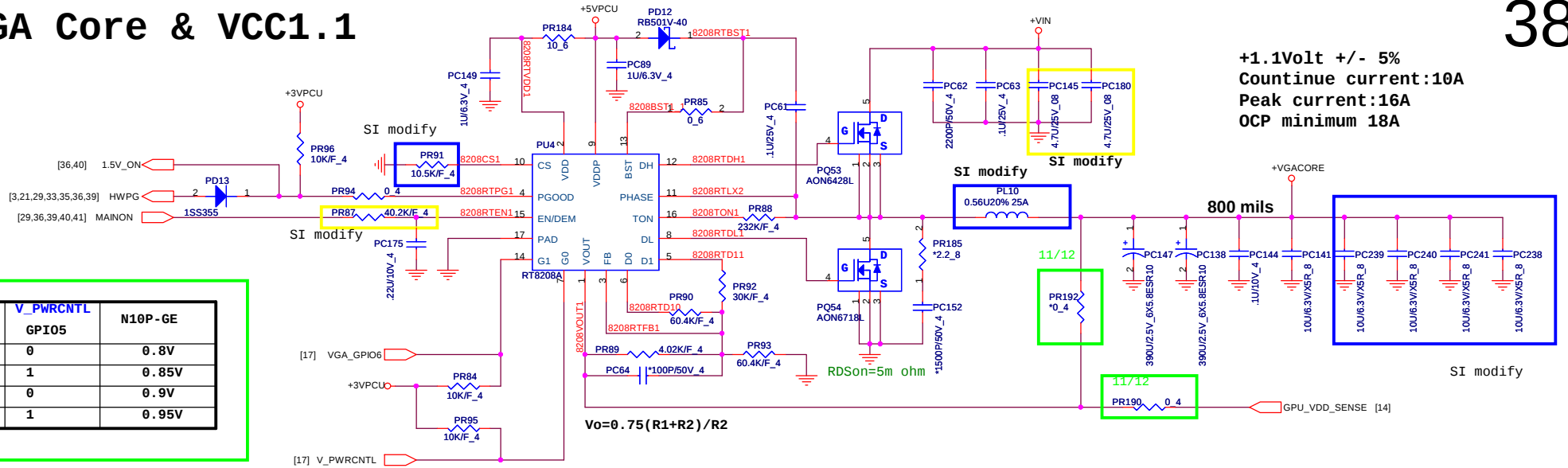


VGA Core & VCC1.1

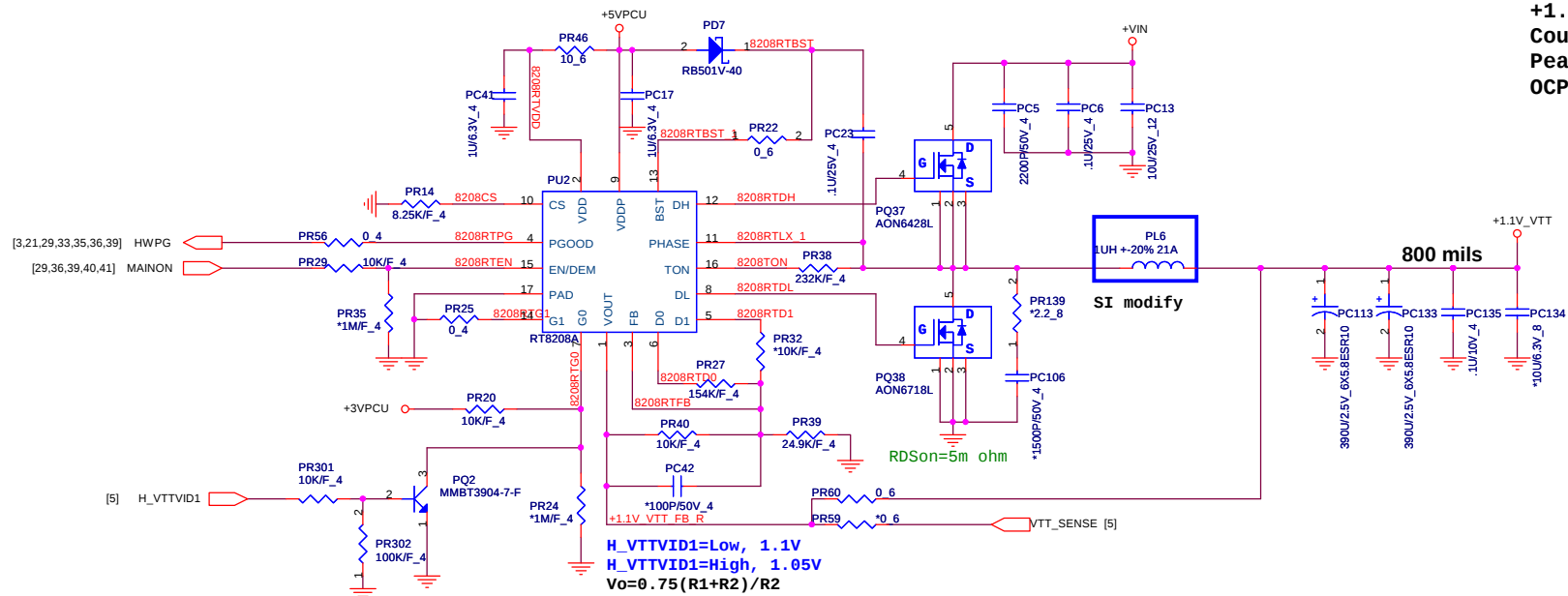
38

11/13

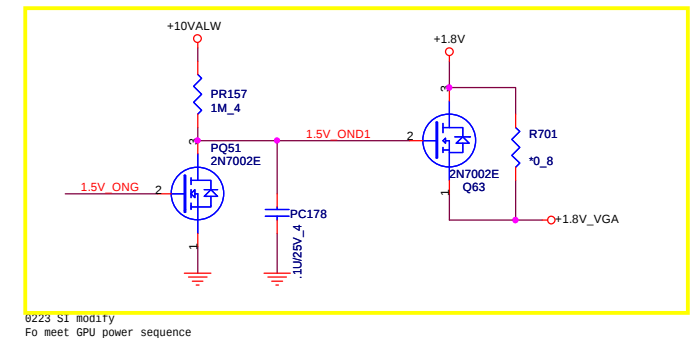
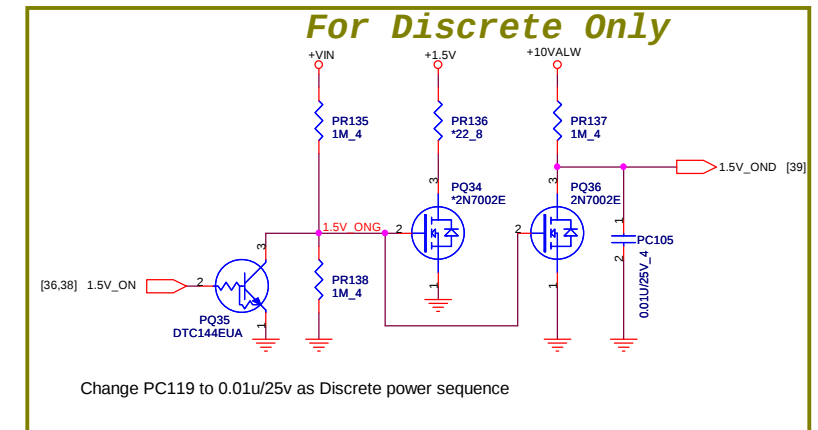
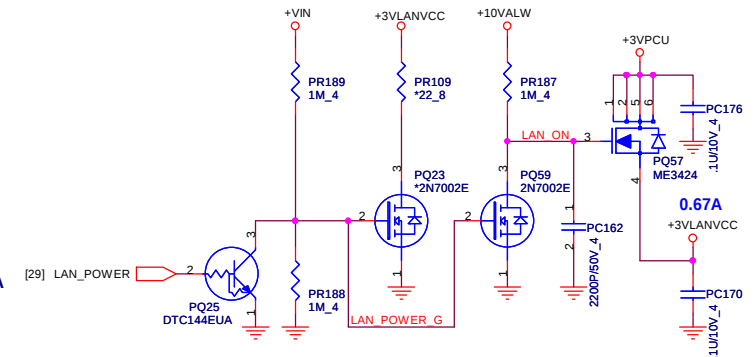
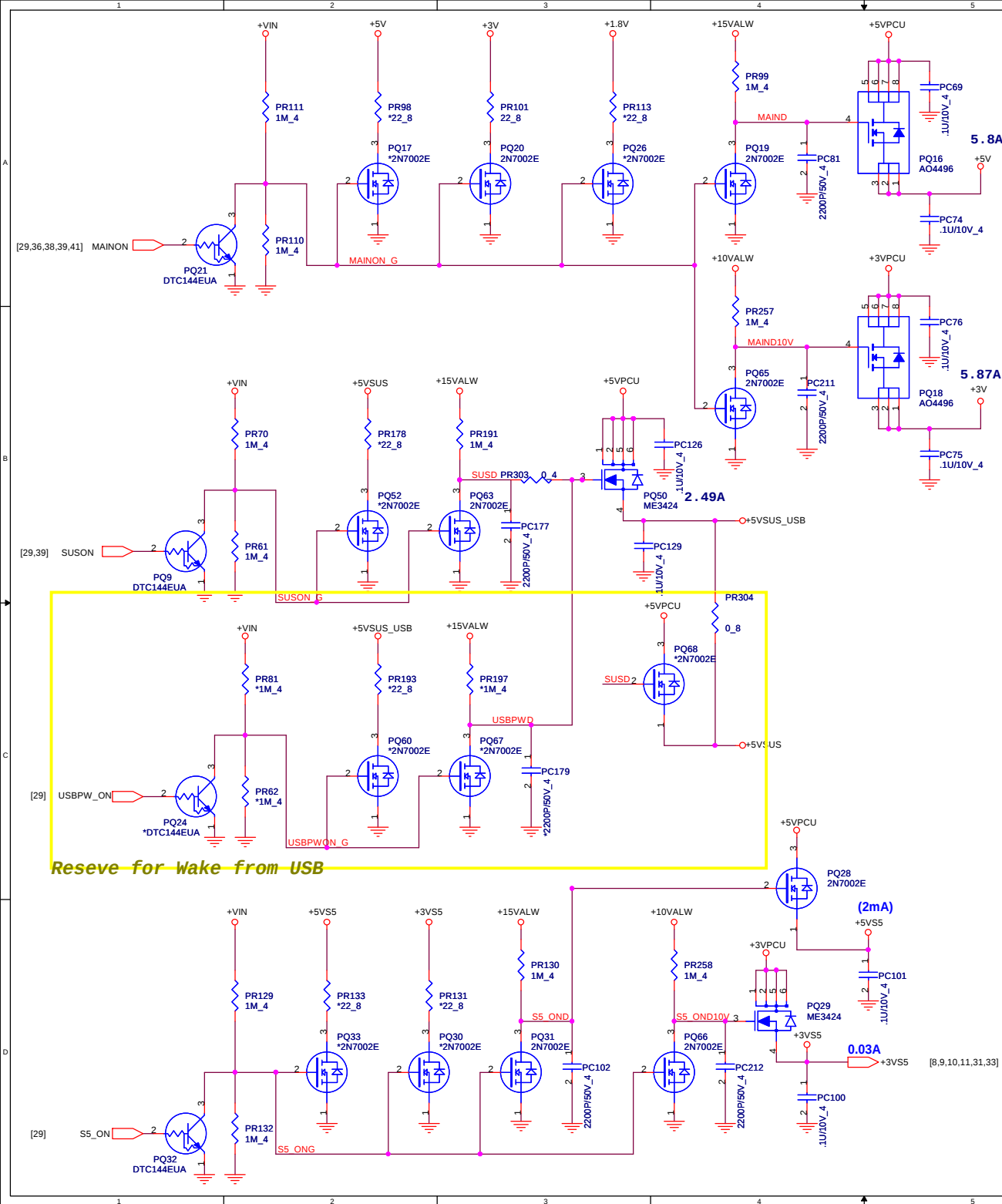
VGA_GPIO6	V_PWRCNTL	N10P-GE
0	0	0.8V
0	1	0.85V
1	0	0.9V
1	1	0.95V



+1.1Volt +/- 5%
Countinue current:10A
Peak current:16A
OCP minimum 18A



+1.1V_PCH Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A

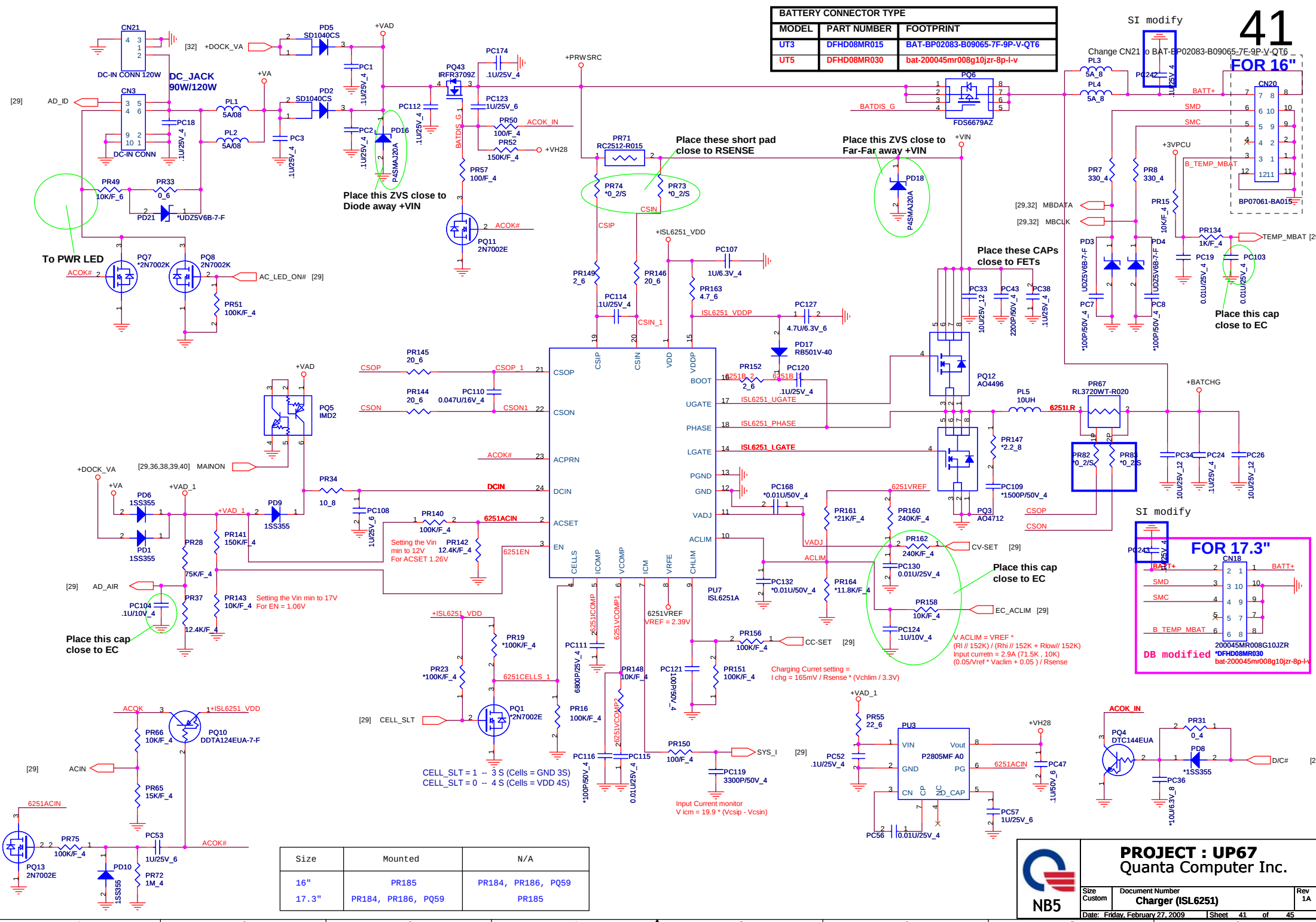


BATTERY CONNECTOR TYPE		
MODEL	PART NUMBER	FOOTPRINT
UT3	DFHD08MR015	BAT-BP02083-B09065-7F-9P-V-QT6
UT5	DFHD08MR030	bat-200045mr008g10jzr-8p-l-v

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FOR 16"

FOR 17.3"



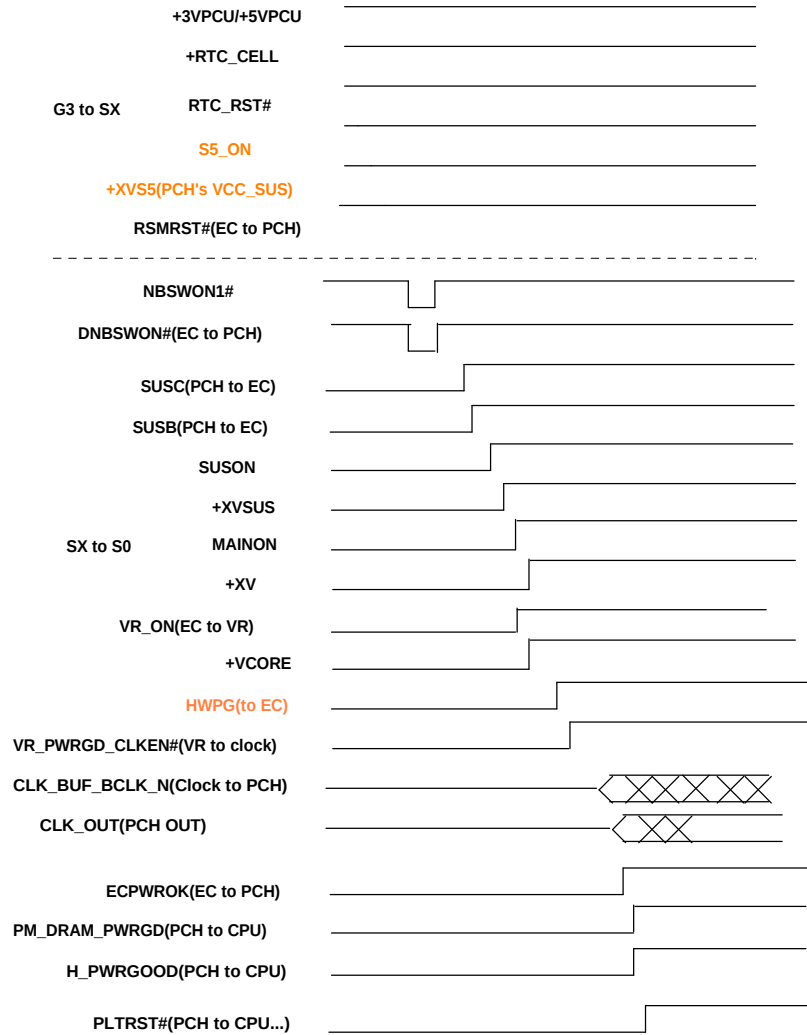
Size	Mounted	N/A
16"	PR185	PR184, PR186, PQ59
17.3"	PR184, PR186, PQ59	PR185

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Quanta Computer Inc.

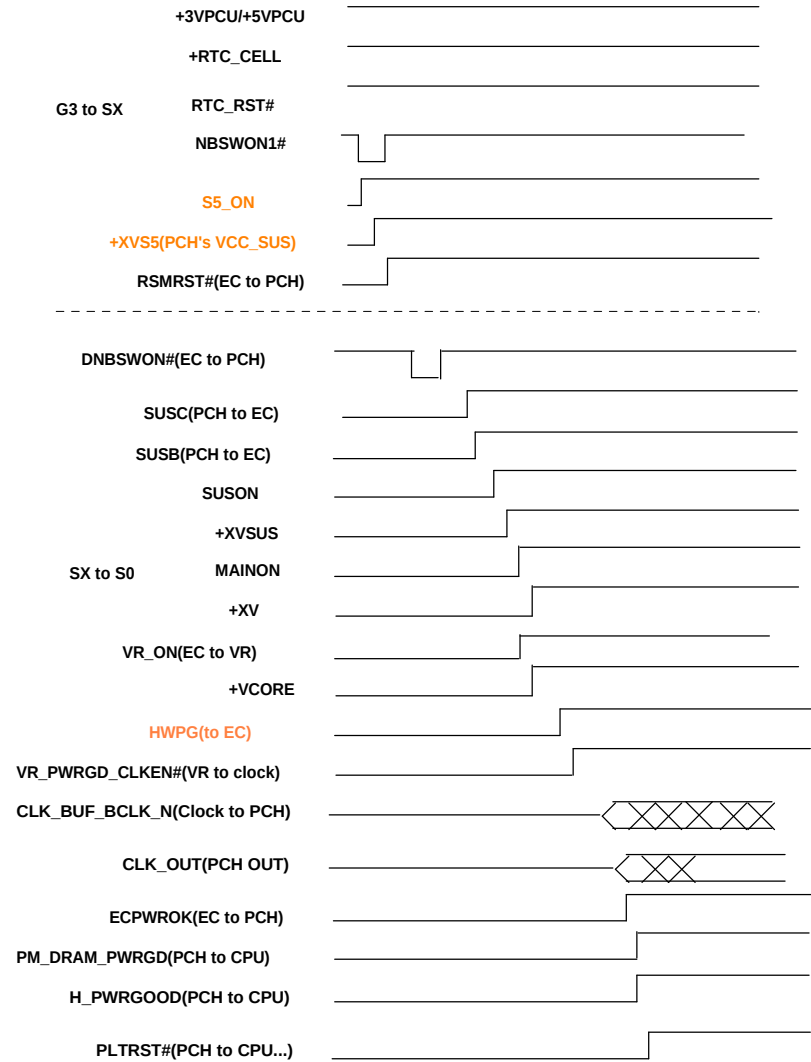
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Power up sequence

LAN/RTC WAKE UP ENABLE.



LAN/RTC WAKE UP DISABLE.



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