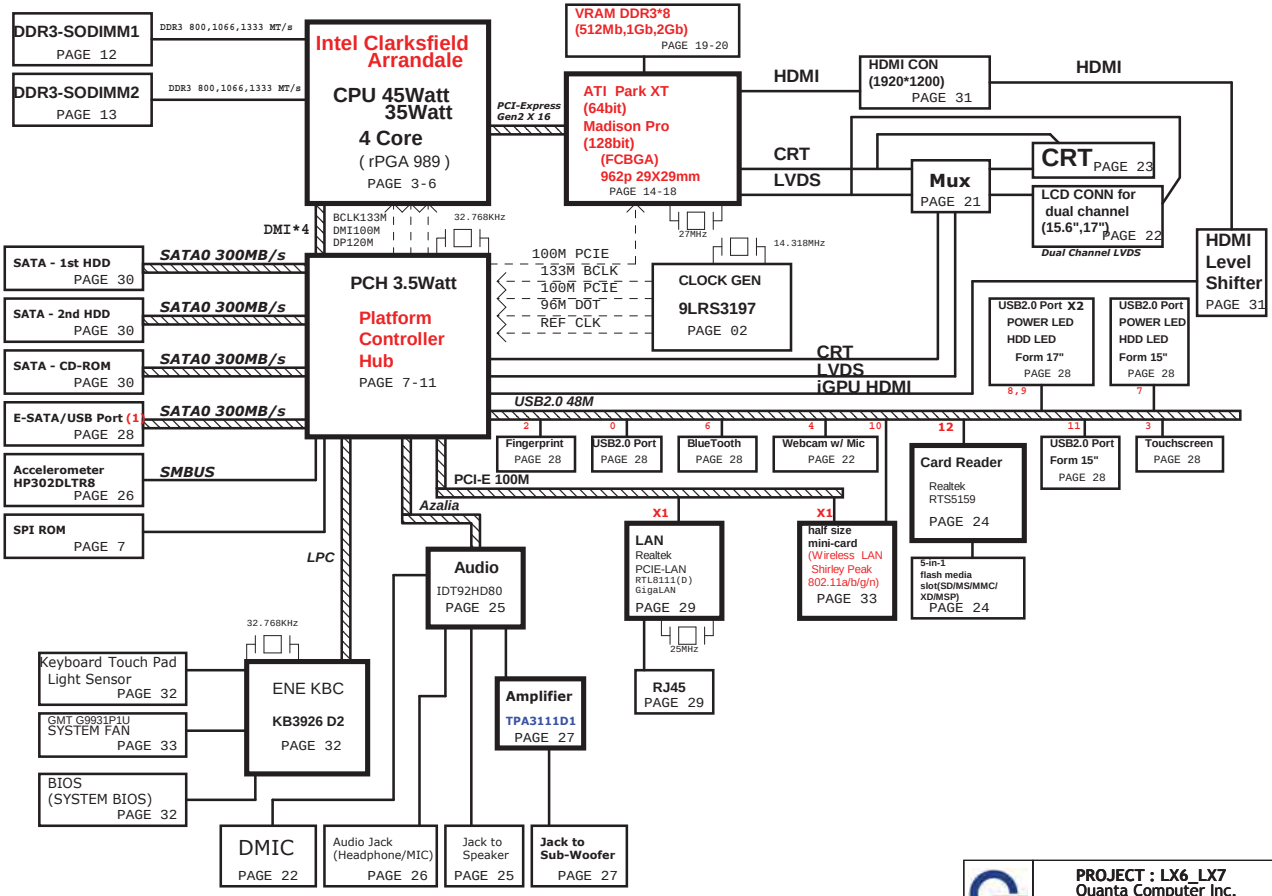
LX6/7 (Liverpool) BLOCK DIAGRAM

01

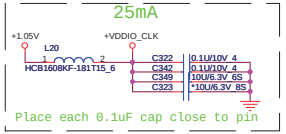
PCB STACK UP

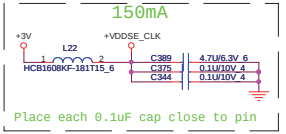
6L Dis.

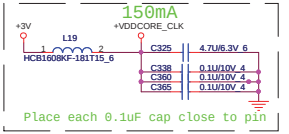
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

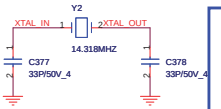


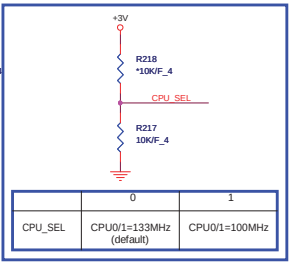
NB5	PROJECT : LX6_LX7 Quanta Computer Inc.	
Size: Custom	Document Number: BLOCK DIAGRAM	Rev: 1A
Date: Tuesday, February 02, 2010	Sheet 1 of 44	

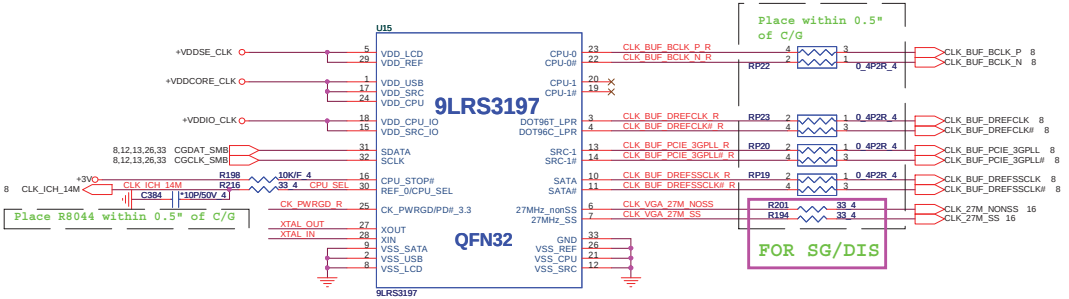


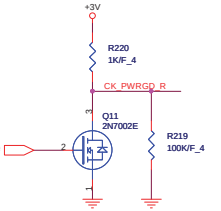






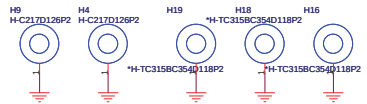




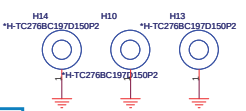


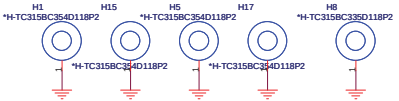
+1.05V 7,8,9,11,36,37,43
+1.5V 33,41
+3V 3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40,41

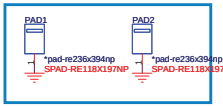
HOLE



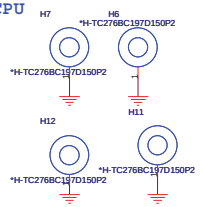
GPU

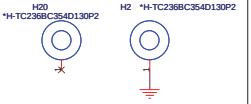






CPU





NB5

PROJECT : LX6_LX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Gen(9LRS3197)/HOLES	1A

Date: Tuesday, February 02, 2010 Sheet 2 of 44

	DIS	SG/UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

03

U25A

DMI_TXN0 A24 DMI_RX#[0]
DMI_TXN1 C23 DMI_RX#[1]
DMI_TXN2 B22 DMI_RX#[2]
DMI_TXN3 A21 DMI_RX#[3]
DMI_TXP0 B24 DMI_RX[0]
DMI_TXP1 D23 DMI_RX[1]
DMI_TXP2 B23 DMI_RX[2]
DMI_TXP3 A22 DMI_RX[3]
DMI_RXN0 D24 DMI_TX#[0]
DMI_RXN1 G24 DMI_TX#[1]
DMI_RXN2 F23 DMI_TX#[2]
DMI_RXN3 H23 DMI_TX#[3]
DMI_RXP0 D25 DMI_TX[0]
DMI_RXP1 E24 DMI_TX[1]
DMI_RXP2 E23 DMI_TX[2]
DMI_RXP3 G23 DMI_TX[3]

DMI

2.7GT/s data rate

FDI_TXN[7:0] → FDI_TXN0 E22 … FDI_TXN7 G18 → FDI_TX#[0] … FDI_TX#[7]
FDI_TXP[7:0] → FDI_TXP0 D22 … FDI_TXP7 G22 → FDI_TX[0] … FDI_TX[7]
FDI_FSYNC0 F17 → FDI_FSYNC[0]
FDI_FSYNC1 E17 → FDI_FSYNC[1]
FDI_INT C17 → FDI_INT
FDI_LSYNC0 F18 → FDI_LSYNC[0]
FDI_LSYNC1 D17 → FDI_LSYNC[1]

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI B26 PEG_COMP R270 49.9/F_4
PEG_ICOMPO A26
PEG_RCOMPO B27
PEG_RBIAS A25 PEG_RBIAS R269 750/F_4
PEG_RX#[0..15] 14

PEG_RX#0 K35 … PEG_RX#15 A31
PEG_RX[0..15] 14
PEG_RX0 J35 … PEG_RX15 A30

PEG_TX#0 L33 … PEG_TX#15 C26
PEG_TX#[0..15] 14
C_PEG_TX#0 … C_PEG_TX#15
0.1U/10V_4 C538 … C552
PEG_TX#0 … PEG_TX#15

PEG_TX0 L34 … PEG_TX15 C25
PEG_TX[0..15] 14
C_PEG_TX0 … C_PEG_TX15
0.1U/10V_4 C534 … C549
PEG_TX0 … PEG_TX15

FOR SG/DIS
MV Modify

IC_AUB_CFD_rPGA_R1P0

U25B

COMP3 AT23
COMP2 AT24
COMP1 G16
COMP0 AT26
SKTOCC# AH24
MISC

H_CATERR# AK14 → CATERR#
10 H_PECI AT15 → PECI
32,37 H_PROCHOT# AN26 → PROCHOT#
10,32 PM_THRMTRIP# AK15 → THERMTRIP#
THERMAL

R400 20/F_4 H_COMP3
R401 20/F_4 H_COMP2
R24 49.9/F_4 H_COMP1
R405 49.9/F_4 H_COMP0

BCLK A16 BCLK#
BCLK_ITP AP30 BCLK_ITP#
E16 PEG_CLK
D16 PEG_CLK#
CLOCKS

CLK_CPU_BCLK 10
CLK_CPU_BCLK# 10
CLK_PCIE_3GPLL 8
CLK_PCIE_3GPLL# 8
R274 *0.4
DREFSSCLK_R
Ra
R273 0 4P2R_4
DREFSSCLK 8
DREFSSCLK# 8
Rb
R272 *0.4
DREFSSCLK# R
DDR3_DRAMRST# C
DDR3_DRAMRST#_C 12

DPLL_REF_SSCLK
DPLL_REF_SSCLK#

SM_DRAMRST# F6
DDR3 MISC

SM_RCOMP_0 AL1 R396 100/F_4
SM_RCOMP_1 AM1 R397 24.9/F_4
SM_RCOMP_2 AN1 R398 130/F_4
SM_RCOMP[1] R426 10K/J_4
SM_RCOMP[2] R427 *0/short_4 +1.05V_VTT
PM_EXT_TS#[0] AN15 PM_EXT_TS#0 R424 *0/short_4 PM_EXTTS#0 12
PM_EXT_TS#[1] AP15 PM_EXT_TS#1 R425 10K/J_4 PM_EXTTS#1 12,13
+1.05V_VTT

C301 *0.1U/10V_4
T4 AP26
9 PM_SYNC AL15
10 H_PWRGOOD AN27
9 PM_DRAM_PWRGD AK13
T5 AM26
H_VTTPWRGD AM15
9,29,32,33,34 PLTRST# CPU_PLTRST# AL14
R108 1.5K/F_4
R107 750/F_4

PRDY# AT28 T20
PREQ# AP27 XDP_PREQ#
TCK AN28 XDP_TCLK T6
TMS AP28 XDP_TMS T8
TRST# AT27 XDP_TRST# T19
TDI AT29 XDP_TDI_R T9
TDO AR27 XDP_TDO_R T11
TDI_M AR29 XDP_TDI_M T10
TDO_M AP29 XDP_TDO_M T7
DBR# AN25 XDP_DBRESET# 9

JTAG & BPM

BPM#[0] AJ22
BPM#[1] AK22
BPM#[2] AK24
BPM#[3] AJ24
BPM#[4] AJ25
BPM#[5] AH22
BPM#[6] AK23
BPM#[7] AH23

PWR MANAGEMENT

IC_AUB_CFD_rPGA_R1P0

FOR DIS ONLY

R28 1K/F_4 FDI_INT
R25 *0_4 FDI_FSYNC0
R26 *0_4 FDI_FSYNC1
R27 *0_4 FDI_LSYNC0
R21 1K/F_4 FDI_LSYNC1

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

SI Del R416,R393,R407,R406,R395,Q31,Q30,Q32

U30
MC74VHC1G08DFT2G
+3V
HWPG 2 1 4 HWPG_1
R421 2K/F_4
H_VTTPWRGD
R417 1K/F_4

+1.05V_VTT
XDP_TDO_R R97 51/F_4
H_CATERR# R76 49.9/F_4
H_PROCHOT# R86 56.2/F_4
CPU_PLTRST# R109 *68/J_4
XDP_TMS R94 *51/J_4
XDP_TDI_R R93 *51/J_4
XDP_PREQ# R95 *51/J_4
XDP_TCLK R91 *51/J_4
C1006 100P/50V_4
H_PROCHOT#
MV Add

JTAG MAPPING
XDP_TRST#
R394 51/F_4

MV Change
SI2 Modidy
U45
*MC74VHC1G08DFT2G
+3VS5
32,35,36,38,39,40,43 HWPG
+1.5VSUS_L
R422 *1.1K/F_4
R423 *3K/F_4
PM_DRAM_PWRGD
R662 *1.5K/F_4
R663 1.5K/F_4
R664 750/F_4
HWPG_1

Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

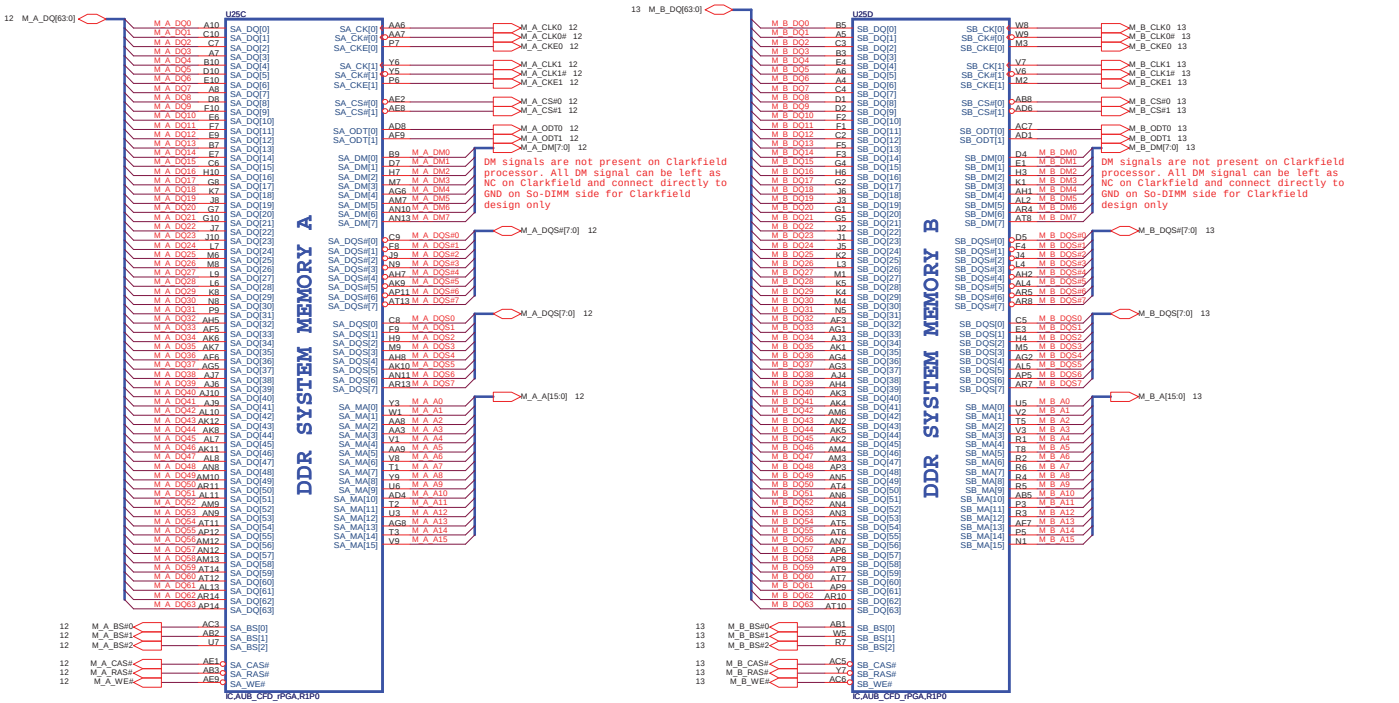
+3V 2,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40,41
+1.05V_VTT 5,10,11,32,37,38,43
+1.5VSUS_L 5,41
+3VS5 8,9,10,11,41

NB5

PROJECT : LX6_LX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 1/4(HOST&PEX)	1A
Date: Tuesday, February 02, 2010	Sheet 3 of 44	

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



18A

	DIS	SG/UMA
Rc	NA	470
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

	DIS	SG/UMA
Ra	0 ohm	NA
Rb	NA	STUFF

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

2A

SI Del BOM

SI2 Add

PV Add

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

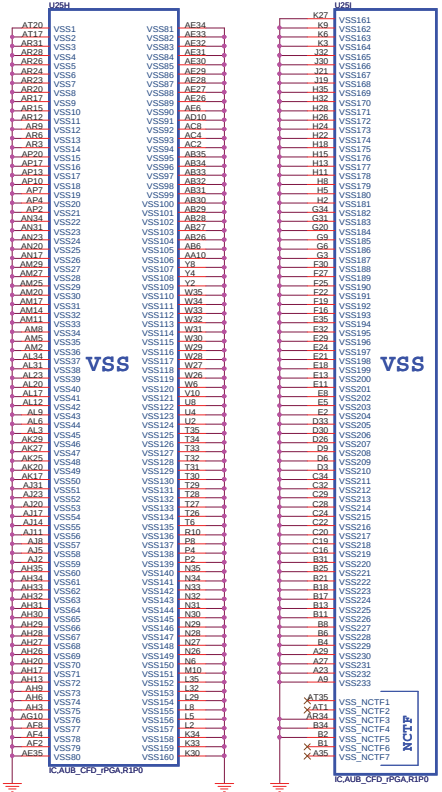
PROJECT : LX6_LX7
Quanta Computer Inc.

NB5

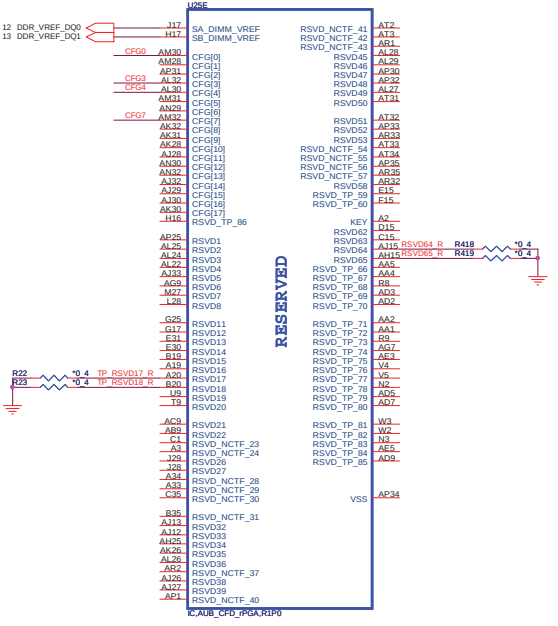
Size: Custom | Document Number: PROCESSER 3/4(POWER) | Rev: 1A

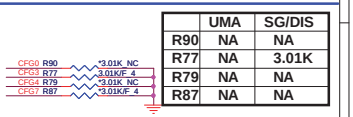
Date: Tuesday, February 02, 2010 | Sheet 5 of 44

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)





	UMA	SG/DIS
R90	NA	NA
R77	NA	3.01K
R79	NA	NA
R87	NA	NA

CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

NB5

PROJECT : LX6_LX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 4/4 (GND)	1A

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INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

UMA CRT,LVDS&HDMI signals

IBEX PEAK-M (LVDS,DDI)

SI Add

SI2 ADD

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

PV Change to Short Pad

UMA HDMI signals

RTC 1mA

4M byte SPI ROM

PV change short pad

For AUDIO

Socket: DG008000031
MXIC AKE39FP0Z00
WINBOND AKE391P0N00

PROJECT : LX6_LX7
Quanta Computer Inc.
NB5
Size: Custom
Document Number: PCH 1/5 (SATA,HDA,LPC)
Rev: 1A
Date: Tuesday, February 02, 2010
Sheet 7 of 44

IBEX PEAK-M (GND)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

U37J

AY2	VSS[159]	VSS[259]
B11	VSS[160]	VSS[260]
B15	VSS[161]	VSS[261]
B19	VSS[162]	VSS[262]
B23	VSS[163]	VSS[263]
B31	VSS[164]	VSS[264]
B35	VSS[165]	VSS[265]
B39	VSS[166]	VSS[266]
B43	VSS[167]	VSS[267]
B47	VSS[168]	VSS[268]
B7	VSS[169]	VSS[269]
BG12	VSS[170]	VSS[270]
BB12	VSS[171]	VSS[271]
BB16	VSS[172]	VSS[272]
BB20	VSS[173]	VSS[273]
BB24	VSS[174]	VSS[274]
BB30	VSS[175]	VSS[275]
BB34	VSS[176]	VSS[276]
BB38	VSS[177]	VSS[277]
BB42	VSS[178]	VSS[278]
BB46	VSS[179]	VSS[279]
BB5	VSS[180]	VSS[280]
BC10	VSS[181]	VSS[281]
BC14	VSS[182]	VSS[282]
BC18	VSS[183]	VSS[283]
BC2	VSS[184]	VSS[284]
BC22	VSS[185]	VSS[285]
BC32	VSS[186]	VSS[286]
BC36	VSS[187]	VSS[287]
BC40	VSS[188]	VSS[288]
BC44	VSS[189]	VSS[289]
BC52	VSS[190]	VSS[290]
BH9	VSS[191]	VSS[291]
BD48	VSS[192]	VSS[292]
BD49	VSS[193]	VSS[293]
BD5	VSS[194]	VSS[294]
BE12	VSS[195]	VSS[295]
BE16	VSS[196]	VSS[296]
BE20	VSS[197]	VSS[297]
BE24	VSS[198]	VSS[298]
BE30	VSS[199]	VSS[299]
BE34	VSS[200]	VSS[300]
BE38	VSS[201]	VSS[301]
BE42	VSS[202]	VSS[302]
BE46	VSS[203]	VSS[303]
BE48	VSS[204]	VSS[304]
BE50	VSS[205]	VSS[305]
BE6	VSS[206]	VSS[306]
BE8	VSS[207]	VSS[307]
BF3	VSS[208]	VSS[308]
BF49	VSS[209]	VSS[309]
BF51	VSS[210]	VSS[310]
BG18	VSS[211]	VSS[311]
BG24	VSS[212]	VSS[312]
BG4	VSS[213]	VSS[313]
BG50	VSS[214]	VSS[314]
BH11	VSS[215]	VSS[315]
BH15	VSS[216]	VSS[316]
BH19	VSS[217]	VSS[317]
BH23	VSS[218]	VSS[318]
BH31	VSS[219]	VSS[319]
BH35	VSS[220]	VSS[320]
BH39	VSS[221]	VSS[321]
BH43	VSS[222]	VSS[322]
BH47	VSS[223]	VSS[323]
BH7	VSS[224]	VSS[324]
C12	VSS[225]	VSS[325]
C50	VSS[226]	VSS[326]
D51	VSS[227]	VSS[327]
E12	VSS[228]	VSS[328]
E16	VSS[229]	VSS[329]
E20	VSS[230]	VSS[330]
E24	VSS[231]	VSS[331]
E30	VSS[232]	VSS[332]
E34	VSS[233]	VSS[333]
E38	VSS[234]	VSS[334]
E42	VSS[235]	VSS[335]
E46	VSS[236]	VSS[336]
E48	VSS[237]	VSS[337]
E6	VSS[238]	VSS[338]
E8	VSS[239]	VSS[339]
F45	VSS[240]	VSS[340]
F5	VSS[241]	VSS[341]
G10	VSS[242]	VSS[342]
G14	VSS[243]	VSS[343]
G18	VSS[244]	VSS[344]
G2	VSS[245]	VSS[345]
G22	VSS[246]	VSS[346]
G32	VSS[247]	VSS[347]
G36	VSS[248]	VSS[348]
G40	VSS[249]	VSS[349]
G44	VSS[250]	VSS[350]
G52	VSS[251]	VSS[351]
AF39	VSS[252]	VSS[352]
H16	VSS[253]	VSS[353]
H20	VSS[254]	VSS[354]
H30	VSS[255]	VSS[355]
H34	VSS[256]	VSS[356]
H38	VSS[257]	VSS[366]
H42	VSS[258]	

H49		
H5		
J24		
K11		
K43		
K47		
K7		
L14		
L18		
L2		
L22		
L32		
L36		
L40		
L52		
M12		
M16		
M20		
N38		
M34		
M38		
M42		
M46		
M49		
M5		
M8		
N24		
P11		
AD15		
P22		
P30		
P32		
P34		
P42		
P45		
P47		
R2		
R52		
T12		
T41		
T46		
T49		
T5		
T8		
U30		
U31		
U32		
U34		
P38		
V11		
P16		
V19		
V20		
V22		
V30		
V31		
V32		
V34		
V35		
V38		
V43		
V45		
V46		
V47		
V49		
V5		
V7		
V8		
W2		
W52		
Y11		
Y12		
Y15		
Y16		
Y23		
Y28		
Y30		
Y31		
Y32		
Y36		
Y43		
V46		
P49		
Y5		
Y6		
Y8		
P24		
T43		
AD51		
AT8		
AD47		
Y47		
AT12		
AM6		
AT13		
AM5		
AK45		
AK39		
AV14		

IbexPeak-M_Rev1_0

U37B

[WLAN]

33 PCIE_RXN0 — PCIE_RXN0 BG30
33 PCIE_RXP0 — PCIE_RXP0 BJ30
33 PCIE_TXN0 — C334 0.1U/10V_4 — PCIE_TXN0_C BF29
33 PCIE_TXP0 — C340 0.1U/10V_4 — PCIE_TXP0_C BH29

[LAN]

29 PCIE_RXN1_LAN — PCIE_RXN1_LAN AW30
29 PCIE_RXP1_LAN — PCIE_RXP1_LAN BA30
29 PCIE_TXN1_LAN — C350 0.1U/10V_4 — PCIE_TXN1_C BC30
29 PCIE_TXP1_LAN — C343 0.1U/10V_4 — PCIE_TXP1_C BD30

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8

T22 BF33
T23 BH33
T24 BG32
T25 BJ32

AU30 AT30 AU32 AV32
BA32 BB32 BD32 BE32
BC34 BD34 AT34 AU34 AU36 AV36
BG34 BJ34 BG36 BJ36 AK48 AK47

PCI-E*

SMBus
(+3V_S5) SMBALERT# / GPIO11
SMBCLK
SMBDATA
(+3V_S5) SMLOALERT# / GPIO60
SMLOCLK
SMLODATA
(+3V_S5) SMLIALERT# / GPIO74
(+3V_S5) SMLICLK / GPIO58
(+3V_S5) SMLIDATA / GPIO75

+3VS5
B9 SMBALERT# 10K/F_4 R489
H14 PCLK_SMB 2.2K_4 R166
C8 PDAT_SMB 2.2K_4 R486
J14 SMBLDALERT# 10K/F_4 R172
C6 SMB_CLK_ME0 2.2K_4 R478
G8 SMB_DATA_ME0 2.2K_4 R463
M14 SMB_LALERT# 10K/F_4 R177
E10 SMB_CLK_ME1 4.7K_4 R148
G12 SMB_DATA_ME1 4.7K_4 R161

Controller Link
CL_CLK1 T13
CL_DATA1 T11
CL_RST1# T9

PEG
(+3V_S5) PEG_A_CLKRQ# / GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P

H1 PEG_CLKREQ#
AD43 CLK_PCIE_VGA# 14
AD45 CLK_PCIE_VGA 14
AN4 CLK_PCIE_3GPLL# 3
AN2 CLK_PCIE_3GPLL 3

CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P
AT1 DREFSSCLK# 3
AT3 DREFSSCLK 3

From CLK BUFFER

CLKIN_DMI_N AW24 CLK_BUF_PCIE_3GPLL# 2
CLKIN_DMI_P BA24 CLK_BUF_PCIE_3GPLL 2
CLKIN_BCLK_N AP3 CLK_BUF_BCLK_N 2
CLKIN_BCLK_P AP1 CLK_BUF_BCLK_P 2
CLKIN_DOT_96N F18 CLK_BUF_DREFCLK# 2
CLKIN_DOT_96P E18 CLK_BUF_DREFCLK 2
CLKIN_SATA_N / CKSSCD_N AH13 CLK_BUF_DREFSSCLK# 2
CLKIN_SATA_P / CKSSCD_P AH12 CLK_BUF_DREFSSCLK 2
REFCLK14IN P41 CLK_ICH_14M 2
C794 *5.6P/50V_4
CLKIN_PCILOOPBACK J42 CLK_PCI_FB 9
XTAL25_IN AH51 XTAL25_IN
XTAL25_OUT AH53 XTAL25_OUT
R530 *0_4 DIS only
XCLK_RCOMP AF38 XCLK_RCOMP
R210 90.9/F_4 +1.05V

(+3V) CLKOUTFLEX0 / GPIO64
(+3V) CLKOUTFLEX1 / GPIO65
(+3V) CLKOUTFLEX2 / GPIO66
(+3V) CLKOUTFLEX3 / GPIO67
Clock Flex
T45 CLK_FLEX0
P43 CLK_FLEX1
T42 CLK_FLEX2
N50 CLK_FLEX3
T15 T13 T14
R536 22_4 CLK_48M_CR 24

PCIE_CLK_REQ0# P9
PCIECLKRQ0# / GPIO73 (+3V_S5)
CLKOUT_PCIE1N AM45
CLKOUT_PCIE1P
MiniWLAN
33 CLK_PCIE_WLAN# — AM43
33 CLK_PCIE_WLAN — CLKOUT_PCIE1N
33 CLK1_OE# — CLKOUT_PCIE1P
33 PCIE_CLK_REQ1# — U4
PCIECLKRQ1# / GPIO18 (+3V)
AM47 AM48 CLKOUT_PCIE2N CLKOUT_PCIE2P
CLK2_OE# N4
PCIECLKRQ2# / GPIO20 (+3V)
LAN
29 CLK_PCIE_LAN# — AH42
29 CLK_PCIE_LAN — AH41
29 PCIE_CLK_REQ3# — A8
PCIECLKRQ3# / GPIO25 (+3V_S5)
AM51 AM53 CLKOUT_PCIE4N CLKOUT_PCIE4P
PCIE_CLK_REQ4# M9
PCIECLKRQ4# / GPIO26 (+3V_S5)
AJ50 AJ52 CLKOUT_PCIE5N CLKOUT_PCIE5P
PCIE_CLK_REQ5# H6
PCIECLKRQ5# / GPIO44 (+3V_S5)
AK53 AK51 CLKOUT_PEG_B_N CLKOUT_PEG_B_P
PCIE_CLK_REQB# R_P13
PEG_B_CLKRQ# / GPIO56 (+3V_S5)

IbexPeak-M_Rev1_0

CLK1_OE# R446 10K/J_4 +3V
CLK2_OE# R471 10K/J_4
+3VS5
PCIE_CLK_REQ0# R164 10K/J_4
PCIE_CLK_REQ3# R487 10K/J_4
PCIE_CLK_REQ4# R141 10K/J_4
PCIE_CLK_REQB# R R170 10K/J_4
PCIE_CLK_REQ5# R462 10K/J_4
PEG_CLKREQ# R474 10K/J_4

SMB_CLK_ME1 — Q37 2N7002E — MBCLK2 12,17,32
+3V
SMB_DATA_ME1 — Q39 2N7002E — MBDATA2 12,17,32

PDAT_SMB — Q9 2N7002E — CGDAT_SMB 2,12,13,26,33
R162 10K/F_4
+3V
R159 10K/F_4
PCLK_SMB — Q8 2N7002E — CGCLK_SMB 2,12,13,26,33

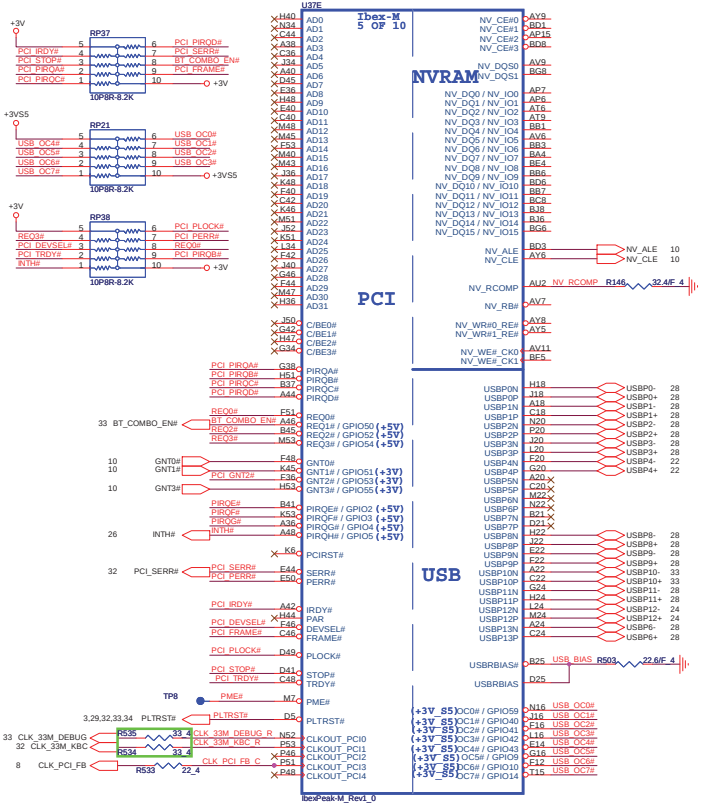
2,7,9,11,36,37,43 +1.05V
3,9,10,11,41 +3VS5
2,3,7,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40,41 +3V

FOR UMA/SG
PV Change to 27P
XTAL25_IN — C750 27P/50V_4
R531 1M/F_4 — Y6 25MHZ
XTAL25_OUT — C751 27P/50V_4
SI Change footprint

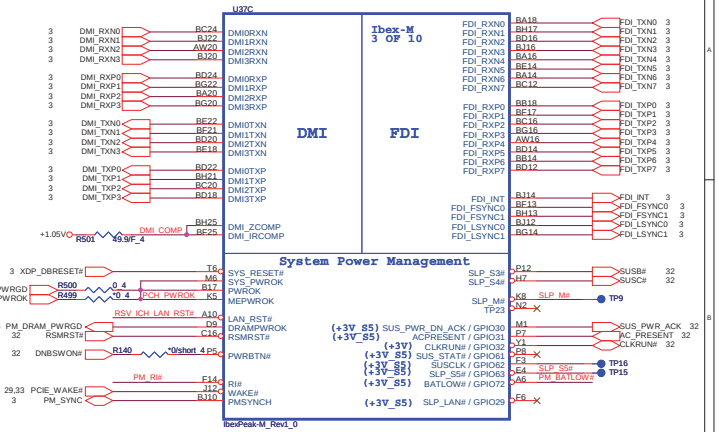
SI Del L21

PROJECT : LX6_LX7
Quanta Computer Inc.
NB5
Size: Custom
Document Number: PCH 2/5 (PCIE, SMBUS, CK)
Rev: 1A
Date: Tuesday, February 02, 2010
Sheet 8 of 44

IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (DMI,FDI,GPIO)



Left_USB
E-Sata
Fingerprint
Touchscreen
Webcam

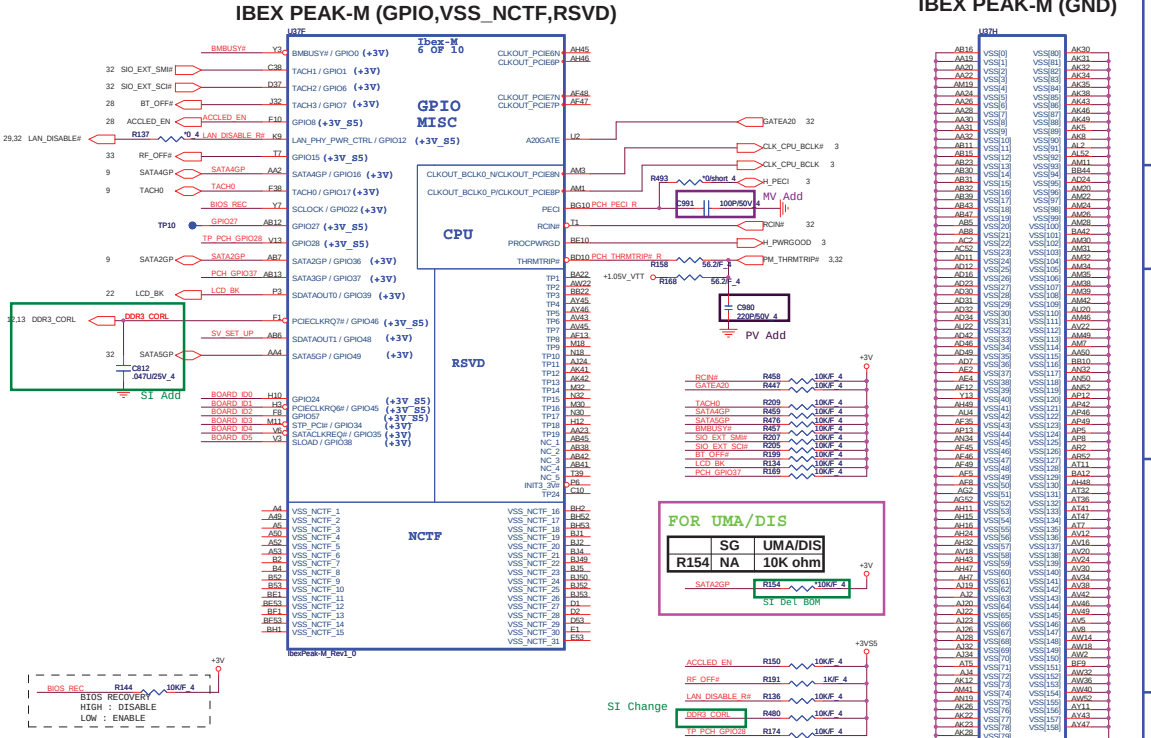
Right_USB 17"/SATA LED
Right_USB 15"/SATA LED
WLAN
Right_USB 15"
Card Reaer
Blue tooth

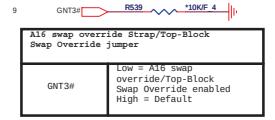
FOR SG ONLY

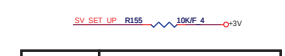
DGPU_SELECT#	R515 0_4	REQ2#	
EDID_SELECT#	R532 0_4	REQ3#	
PWM_SELECT#	R202 0_4	PCI GNT2#	
DGPU_PWR_EN	R163 0_4	SATA2GP	SATA2GP 10
DGPU_PWROK	R204 0_4	TACH0	TACH0 10
DGPU_HOLD_RST#	R461 0_4	SATA4GP	SATA4GP 10

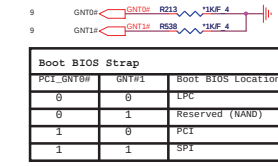
2,7,8,11,36,37,43	+1.05V
2,3,7,8,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40,41	+3V
3,8,10,11,41	+3VS5

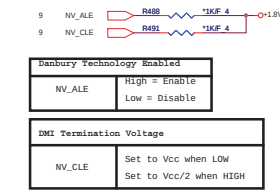
PROJECT :	LX6_LX7
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: PCH 3/5 (PCI,ONFI,USB,DMI)
Rev: 1A	
Date: Tuesday, February 02, 2010	Sheet 9 of 44







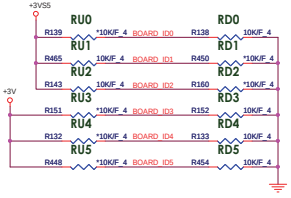




BOARD ID SETTING

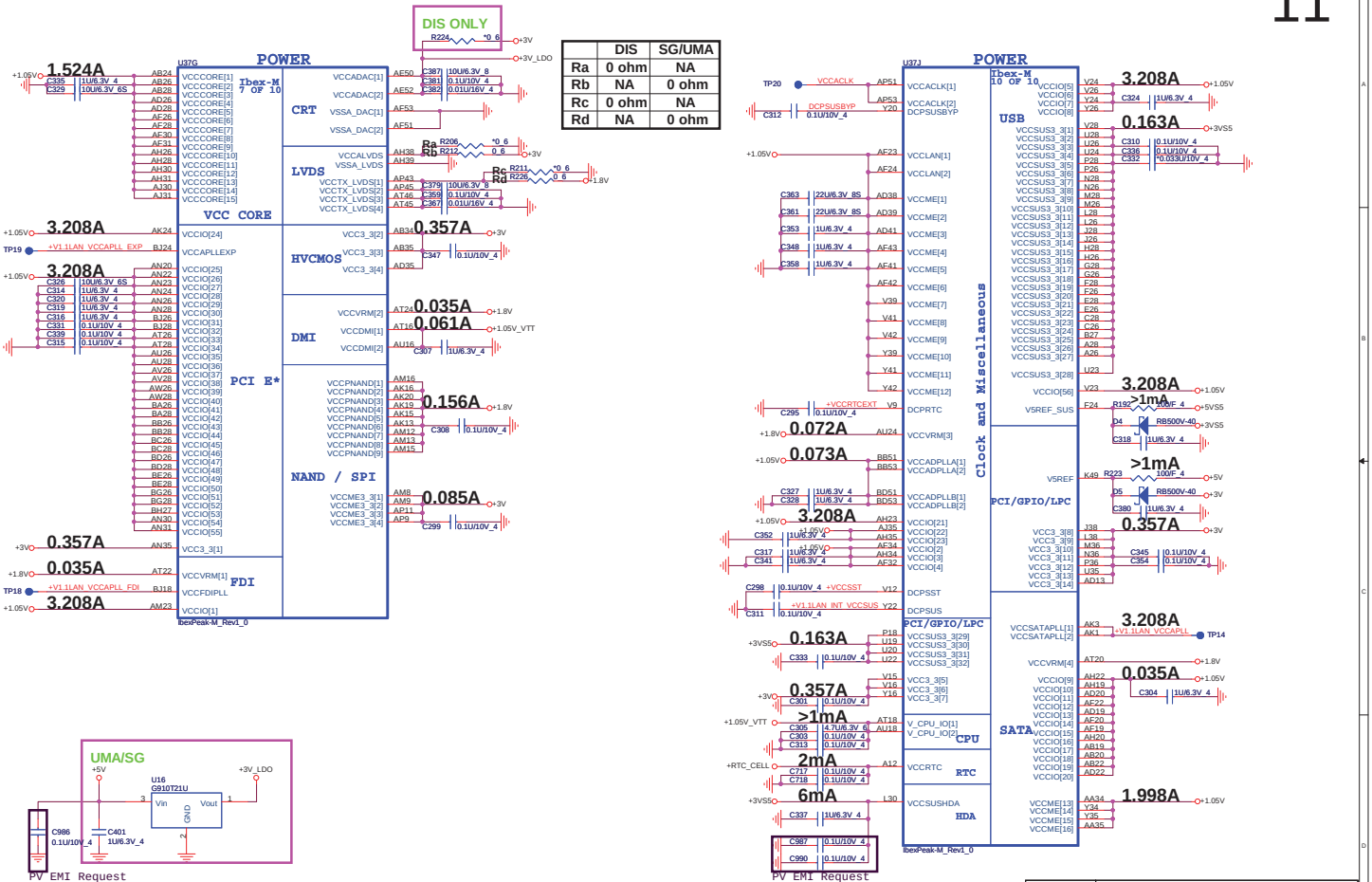
Board ID	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
LX6	0	1				
LX7	1	0				
Discrete			0	0		
UMA			0	1		
SG			1	0		
LX7_No Subwoofer	1	1				

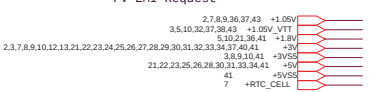


+3V 2,3,7,8,9,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40,41
+1.8V 5,11,21,36,41
+3VS5 3,8,9,11,41
+1.05V_VTT 3,5,11,32,37,38,43

PROJECT : LX6_LX7
Quanta Computer Inc.
NB5
Size: Custom
Document Number: PCH 4/5 (GPIO & Strap)
Rev: 1A
Date: Tuesday, February 02, 2010
Sheet 10 of 44



	DIS	SG/UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

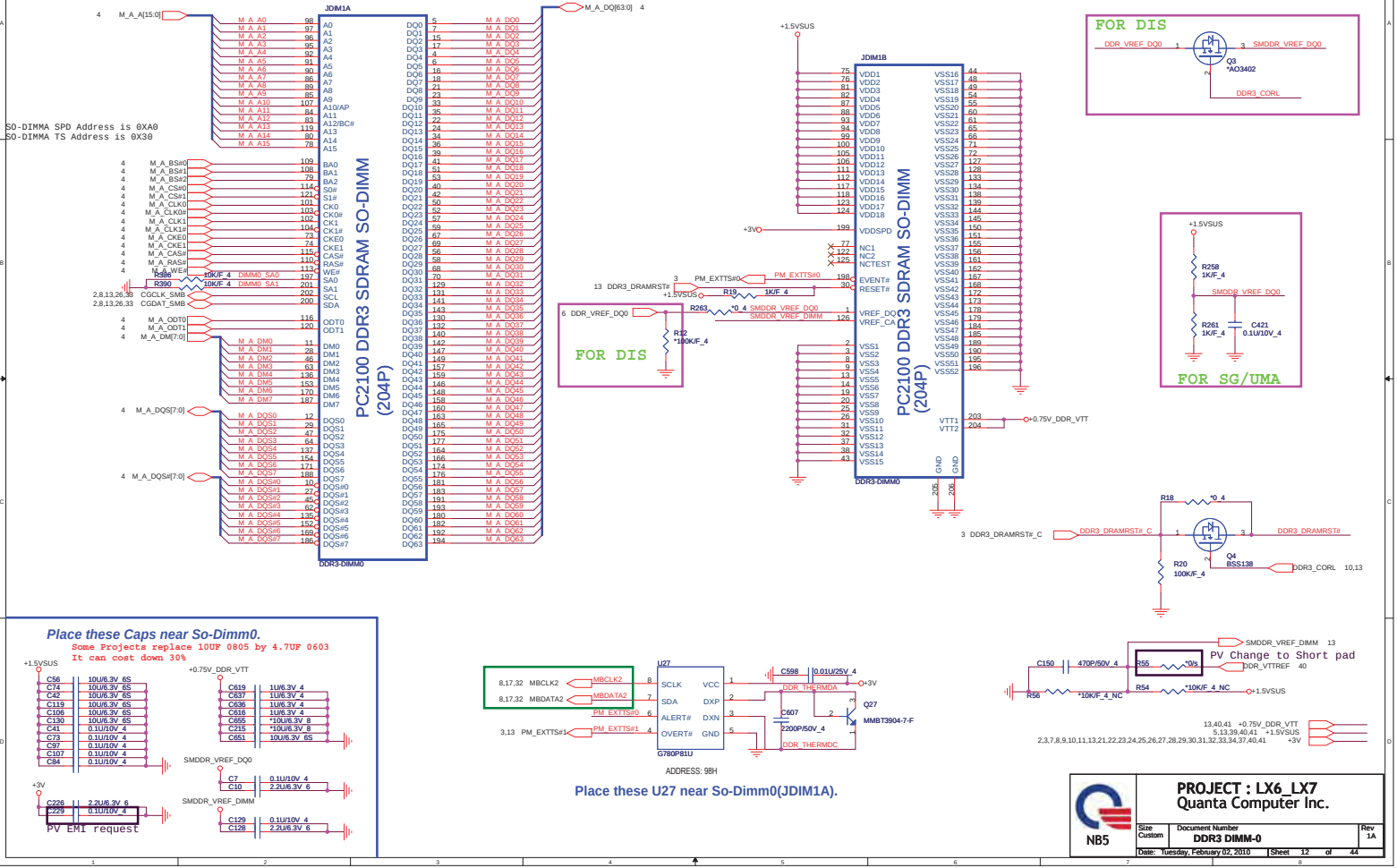


NB5

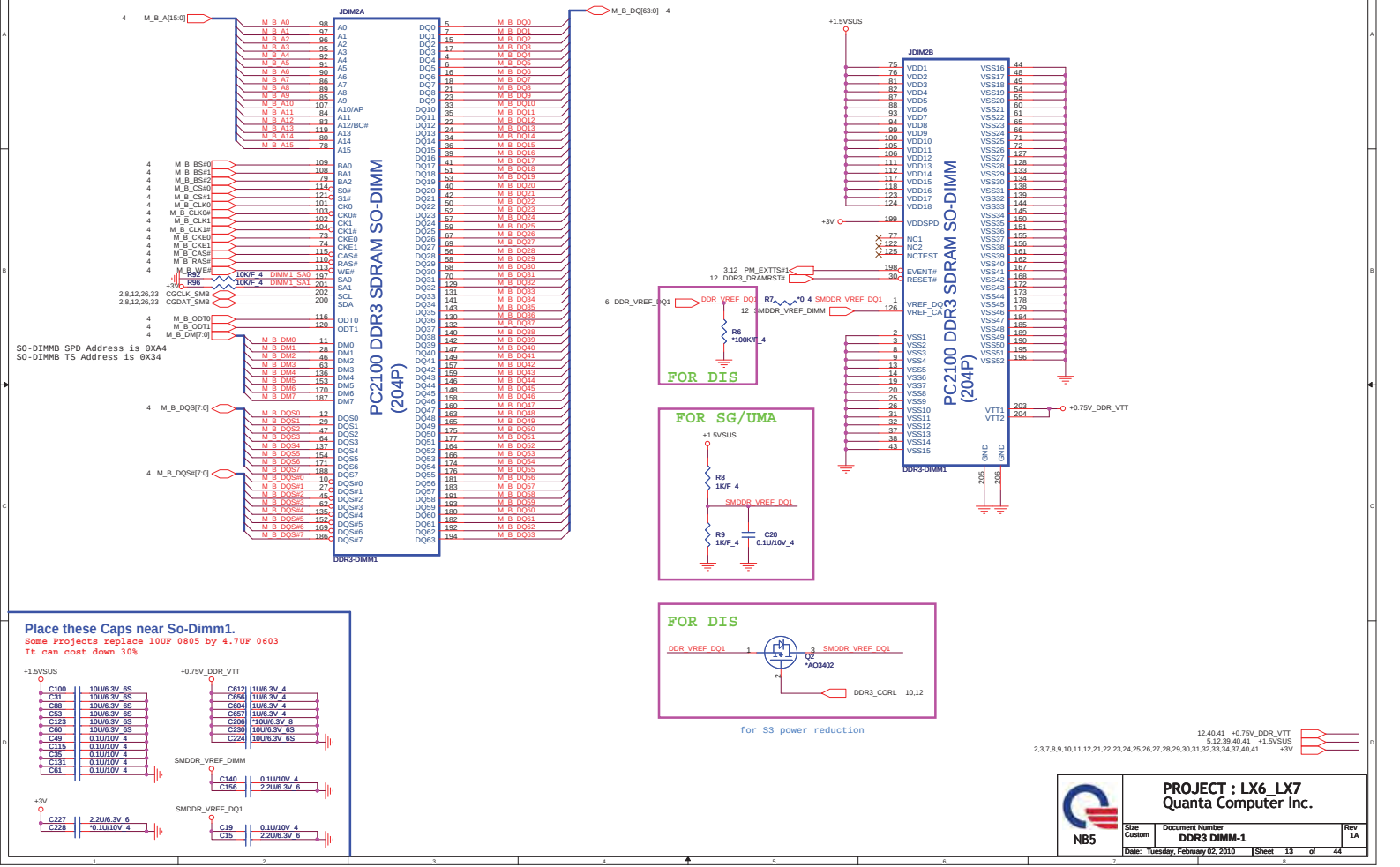
PROJECT : LX6_LX7
Quanta Computer Inc.

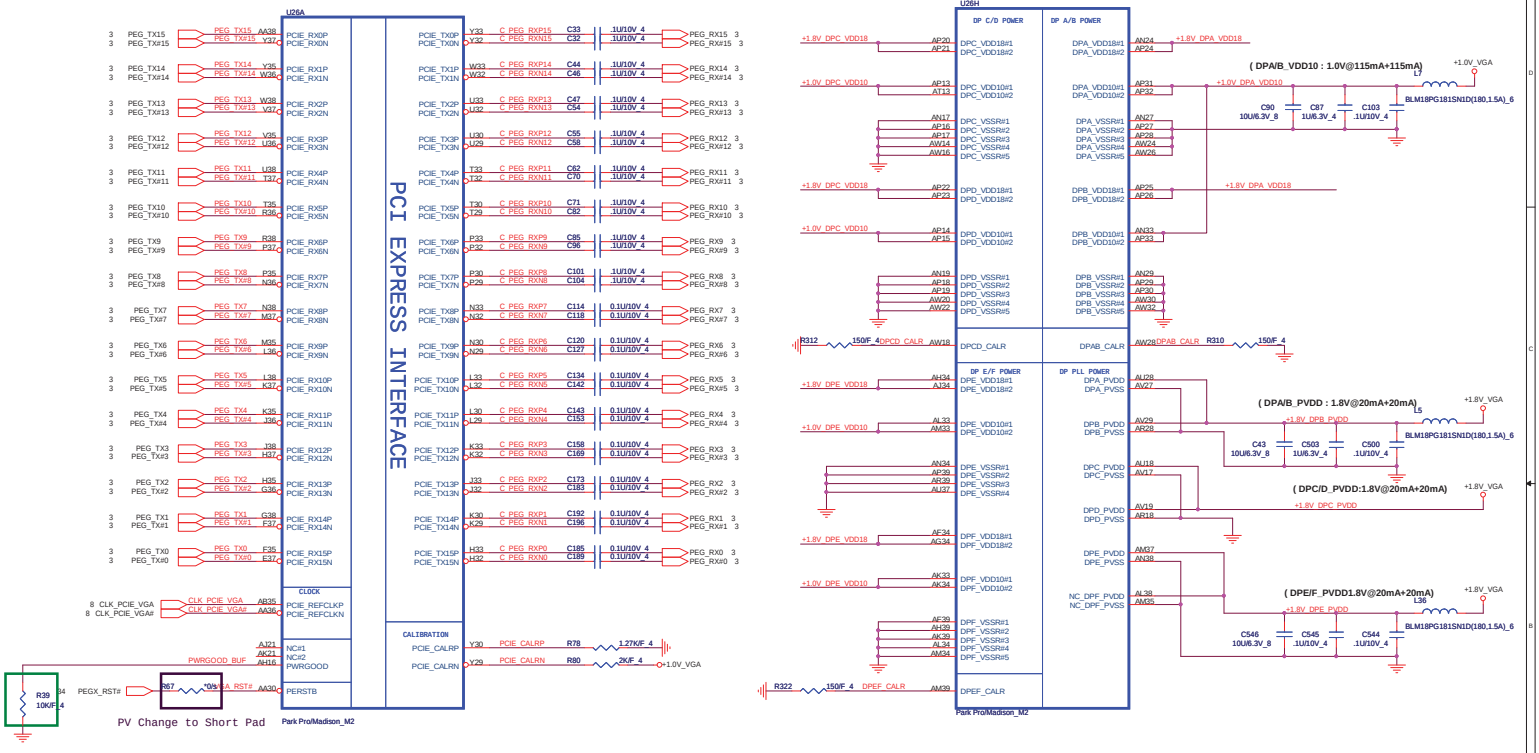
Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	1A

Date: Tuesday, February 02, 2010 Sheet 11 of 44

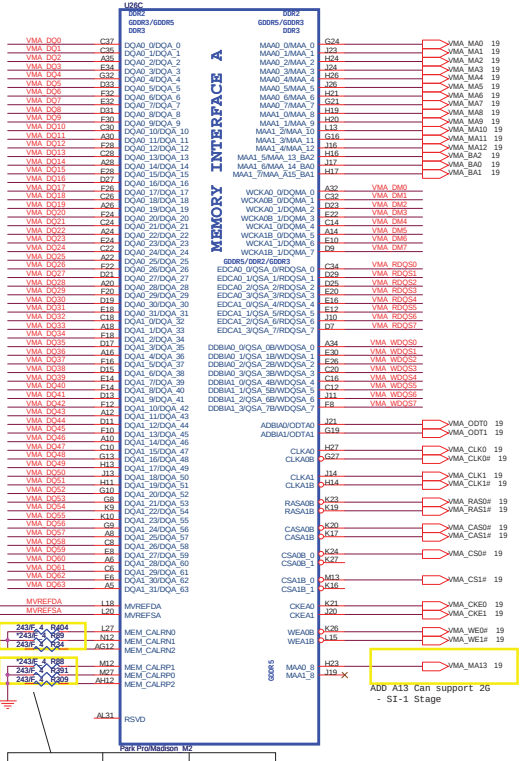


PROJECT : LX6_LX7		
Quanta Computer Inc.		
NB5	Size: Custom	Document Number: DDR3 DIMM-0
	Rev: 1A	
Date: Tuesday, February 02, 2010	Sheet 12 of 44	

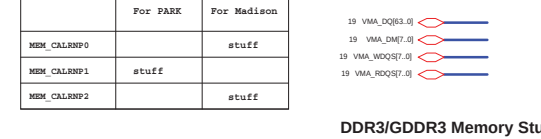

JDIM2A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1
SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34
FOR DIS
FOR SG/UMA
FOR DIS
for S3 power reduction
Place these Caps near So-Dimm1.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%
PROJECT : LX6_LX7
Quanta Computer Inc.
NB5
DDR3 DIMM-1
Date: Tuesday, February 02, 2010
Sheet 13 of 44

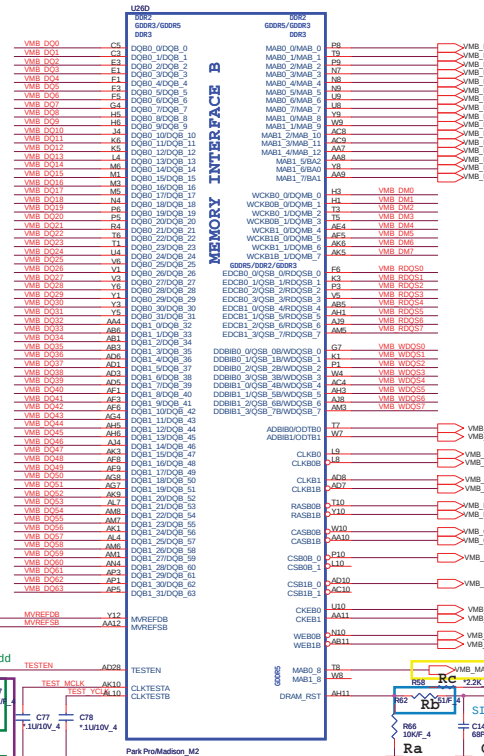


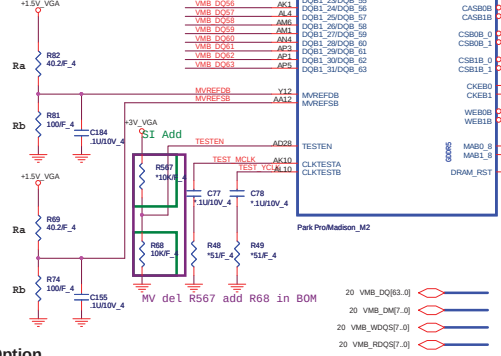
PROJECT : LX6_LX7	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: ATI M97-M2 (PCIE I/F) 1/5; Rev: 1A
Date: Tuesday, February 02, 2010	Sheet 14 of 44



	For PARK	For Madison
MEM_CALRNP0		stuff
MEM_CALRNP1	stuff	
MEM_CALRNP2		stuff







Designator		For Mannhatton
Ra		10K
Rb		51R
Rc		DNI
Ca		68pF

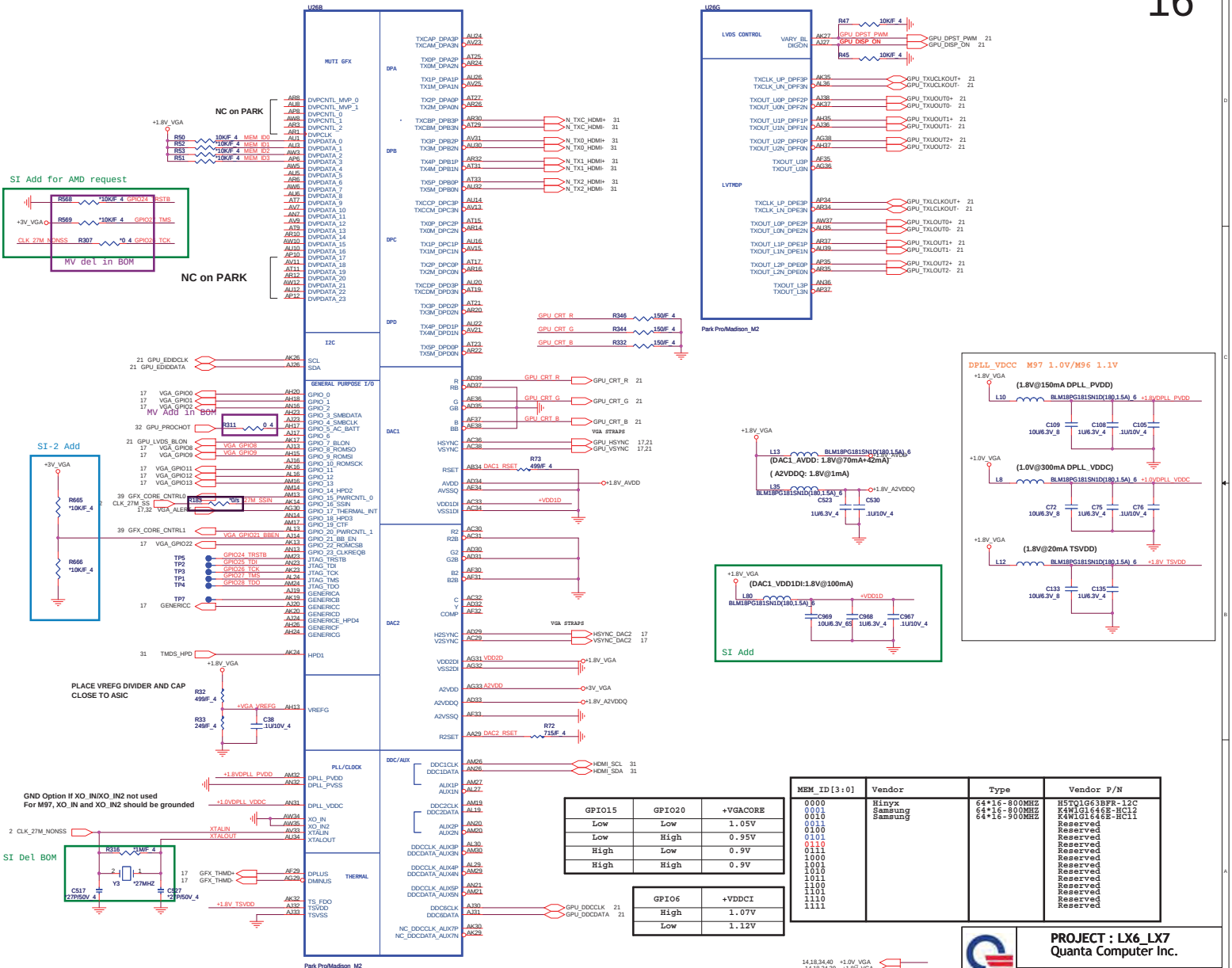
DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

NB5

PROJECT : LX6_LX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M97-M2 (MEM I/F) 2/5	1A
Date: Tuesday, February 02, 2010	Sheet 15 of 44	



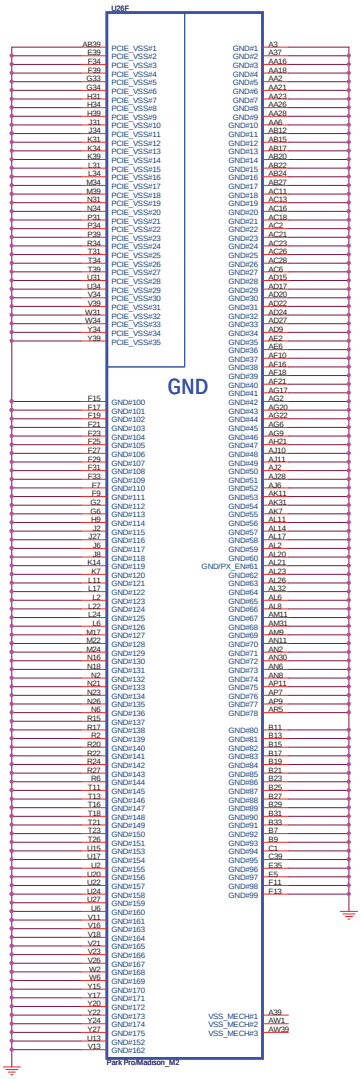
GPIO15	GPIO20	+VGACORE
Low	Low	1.05V
Low	High	0.95V
High	Low	0.9V
High	High	0.9V

GPIO6	+VDDCI
High	1.07V
Low	1.12V

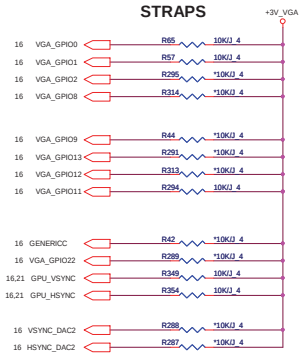
MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hinyx	64*16-800MHZ	H5TQ1G63BFR-12C
0001	Samsung	64*16-800MHZ	K4W1G1646E-HC12
0010	Samsung	64*16-900MHZ	K4W1G1646E-HC11
0011			Reserved
0100			Reserved
0101			Reserved
0110			Reserved
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved

14,18,34,40 +1.0V_VGA
14,18,34,39 +1.8V_VGA
15,17,18,31,34,39 +3V_VGA

PROJECT : LX6_LX7
Quanta Computer Inc.
NB5
Size: Custom
Document Number: ATI M97-M2 (DISPLAY) 3/5
Rev: 1A
Date: Tuesday, February 02, 2010
Sheet 16 of 44



STRAPS



Memory Aperture size fix 256M

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

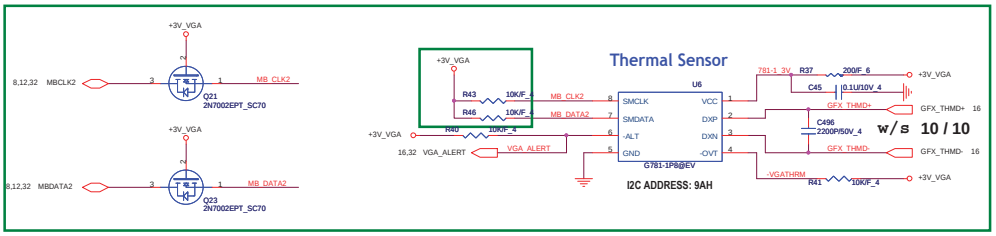
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC

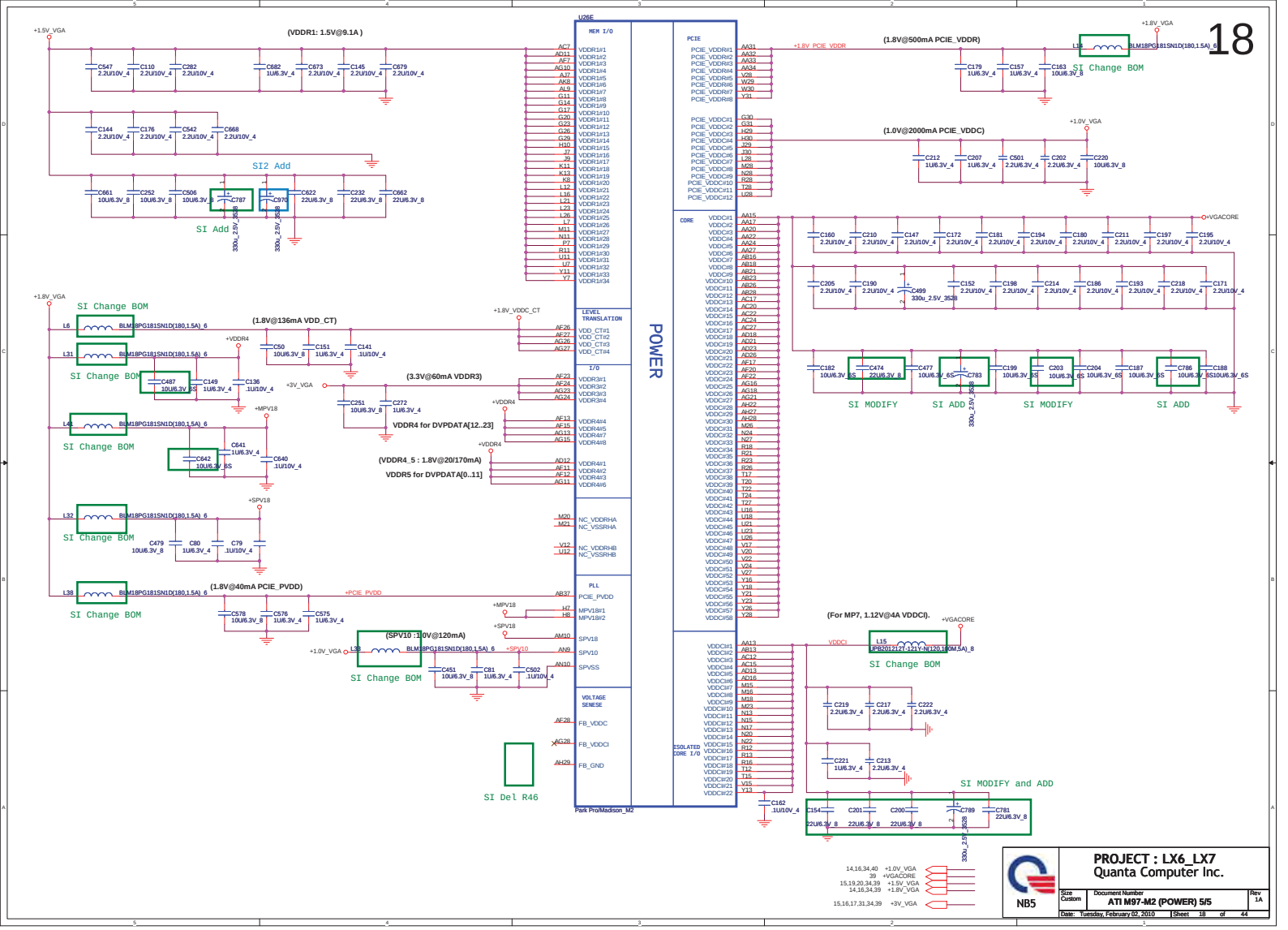
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN



15,16,18,31,34,39 +3V_VGA

PROJECT : LX6_LX7
Quanta Computer Inc.
NB5
Size: Custom
Document Number: ATI M97(GND&Str&Ther)4/5
Rev: 1A
Date: Tuesday, February 02, 2010
Sheet 17 of 44



PROJECT : LX6_LX7
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	ATI M97-M2 (POWER) 5/5	1A

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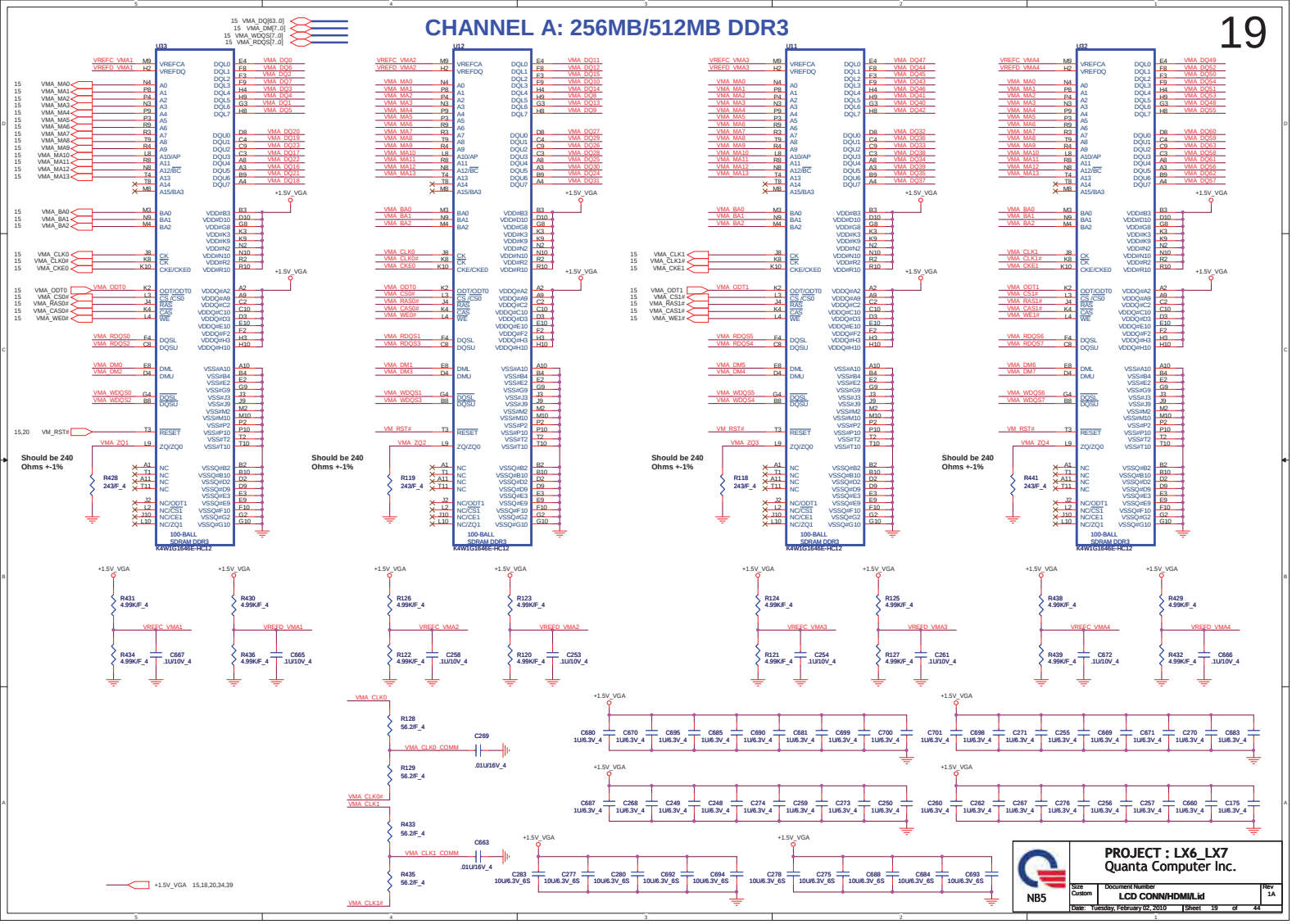
CHANNEL A: 256MB/512MB DDR3



PROJECT : LX6_LX7
Quanta Computer Inc.
NB5
Size: Custom
Document Number: LCD CONN/HDMI/Lid
Rev: 1A
Date: Tuesday, February 02, 2010
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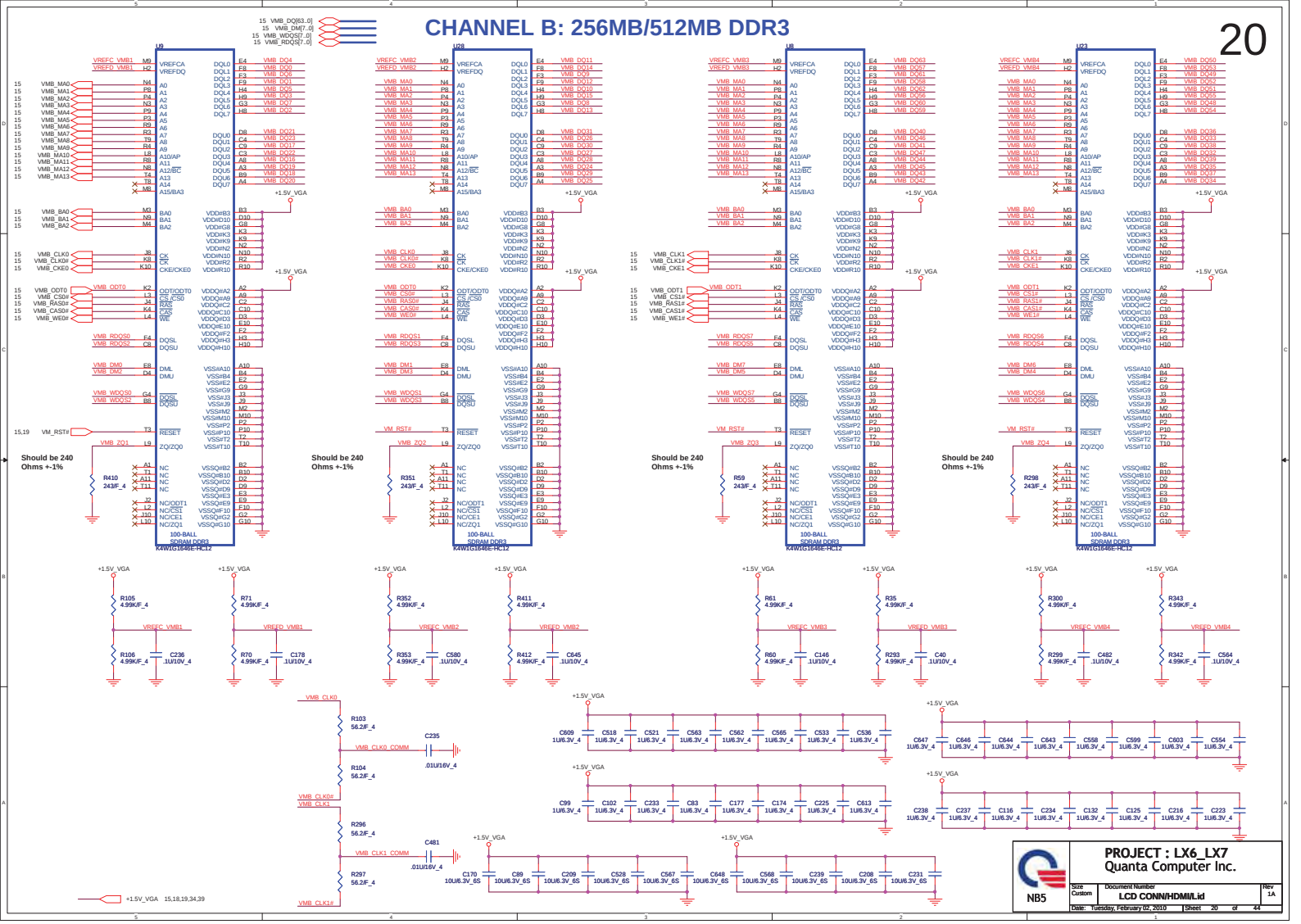
CHANNEL B: 256MB/512MB DDR3



NB5	PROJECT : LX6_LX7 Quanta Computer Inc.		
Size: Custom	Document Number: LCD CONN/HDMI/Lid		Rev: 1A
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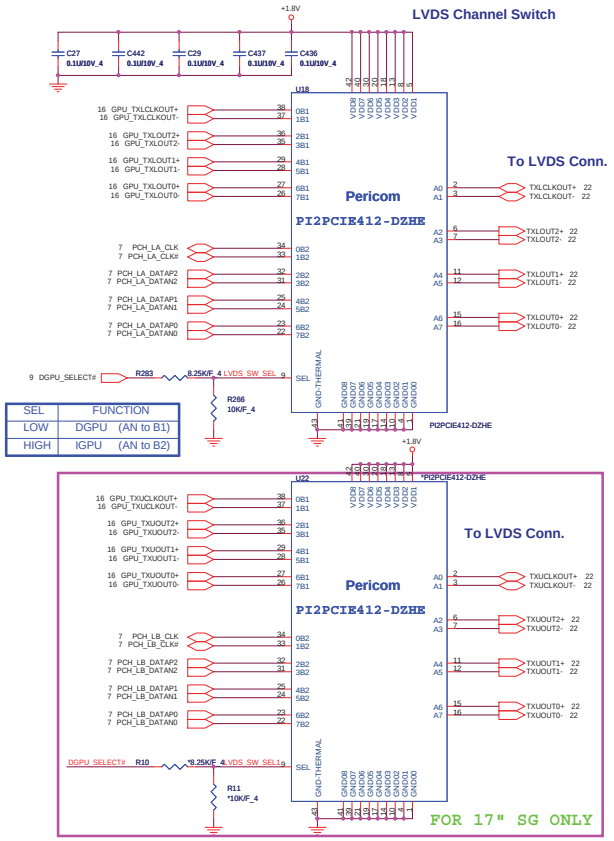
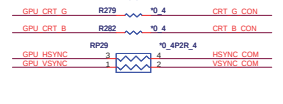
LVDS Channel Switch



SEL	FUNCTION
LOW	DGPU (AN to B1)
HIGH	IGPU (AN to B2)

FOR DIS ONLY

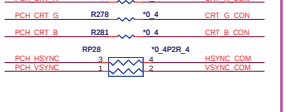
OPTION SIGNAL FROM NB to CRT for DIS



OPTION SIGNAL FROM NB to CRT for DIS

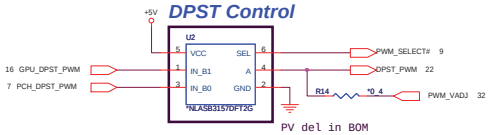
FOR UMA ONLY

OPTION SIGNAL FROM NB to CRT for UMA



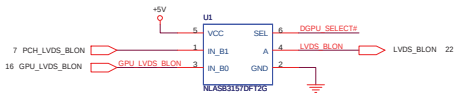
OPTION SIGNAL FROM NB to CRT for UMA

DPST Control

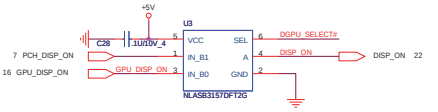


PV del in BOM

SEL	FUNCTION(COM)
LOW	IN_B0 to A
HIGH	IN_B1 to A

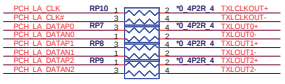


LCDVcc control

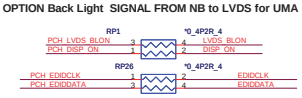


FOR UMA ONLY

OPTION SIGNAL FROM NB to LVDS for UMA

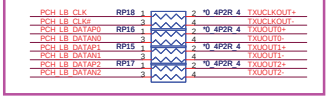


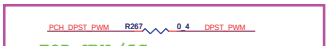
OPTION Back Light SIGNAL FROM NB to LVDS for UMA



OPTION SIGNAL FROM NB to LVDS for UMA

FOR 17"UMA ONLY



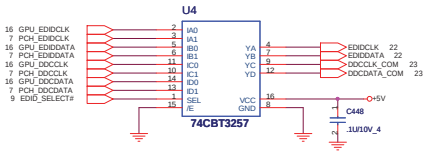


FOR UMA/SG

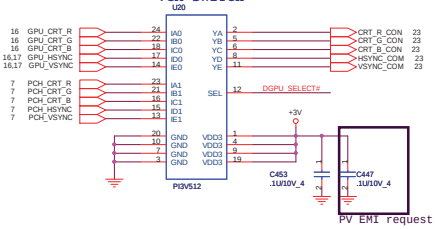
FOR DIS ONLY

LVDS/CRT DDC Switch

SEL	FUNCTION(COM)
LOW	IN_B1 to A
HIGH	IN_B2 to A



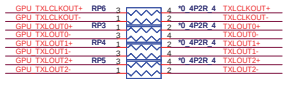
VGA SWITCH



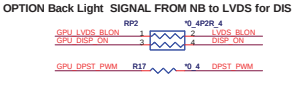
PV EMI request

FOR DIS ONLY

OPTION SIGNAL FROM NB to LVDS for DIS



OPTION Back Light SIGNAL FROM NB to LVDS for DIS



OPTION SIGNAL FROM NB to LVDS for DIS

FOR 17"DIS ONLY

NB5

PROJECT : LX6_LX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SWITCHABLE	1A

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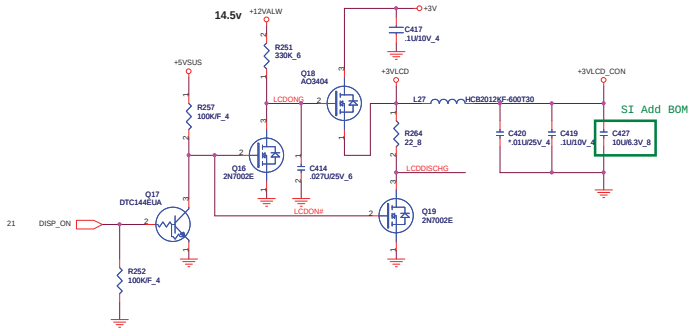

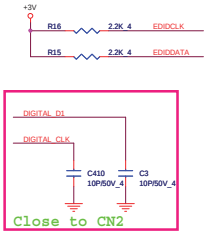

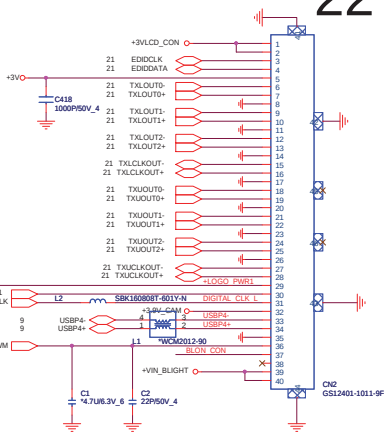

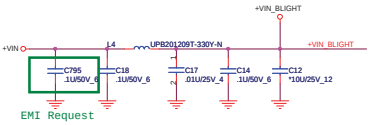

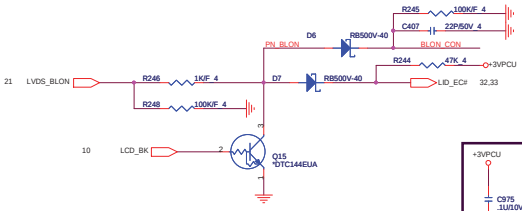

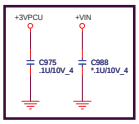

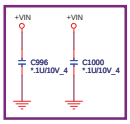

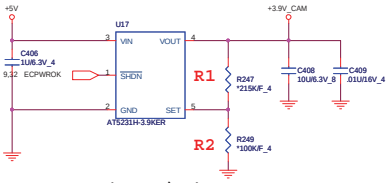

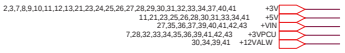

NB5

PROJECT : LX6_LX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID function	1A
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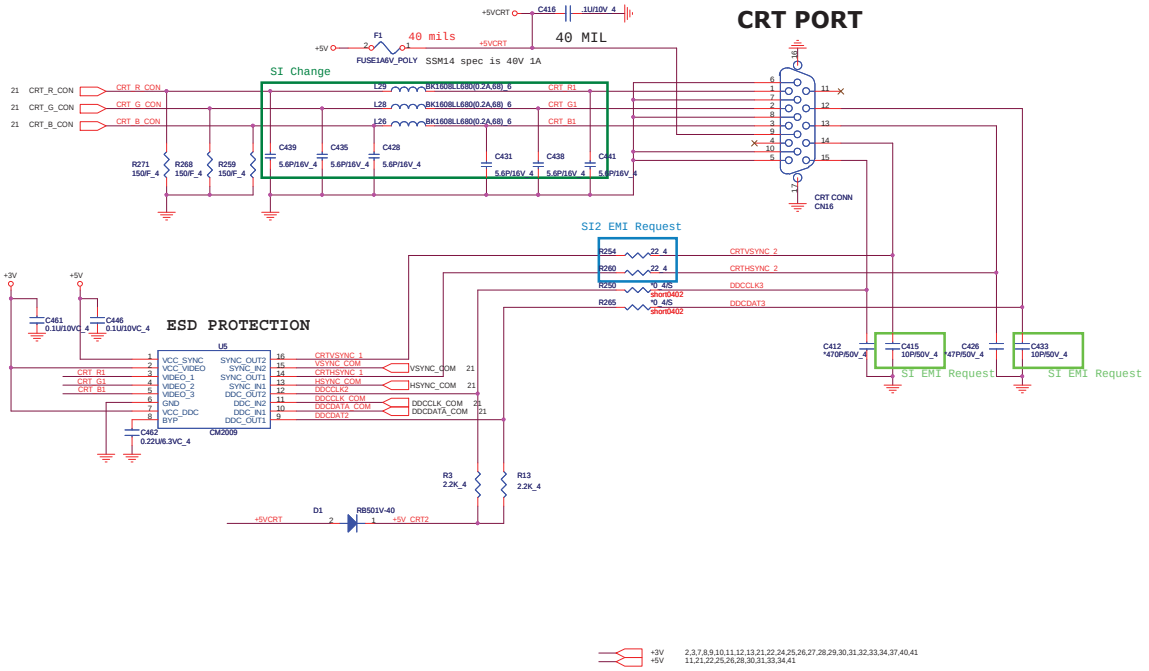
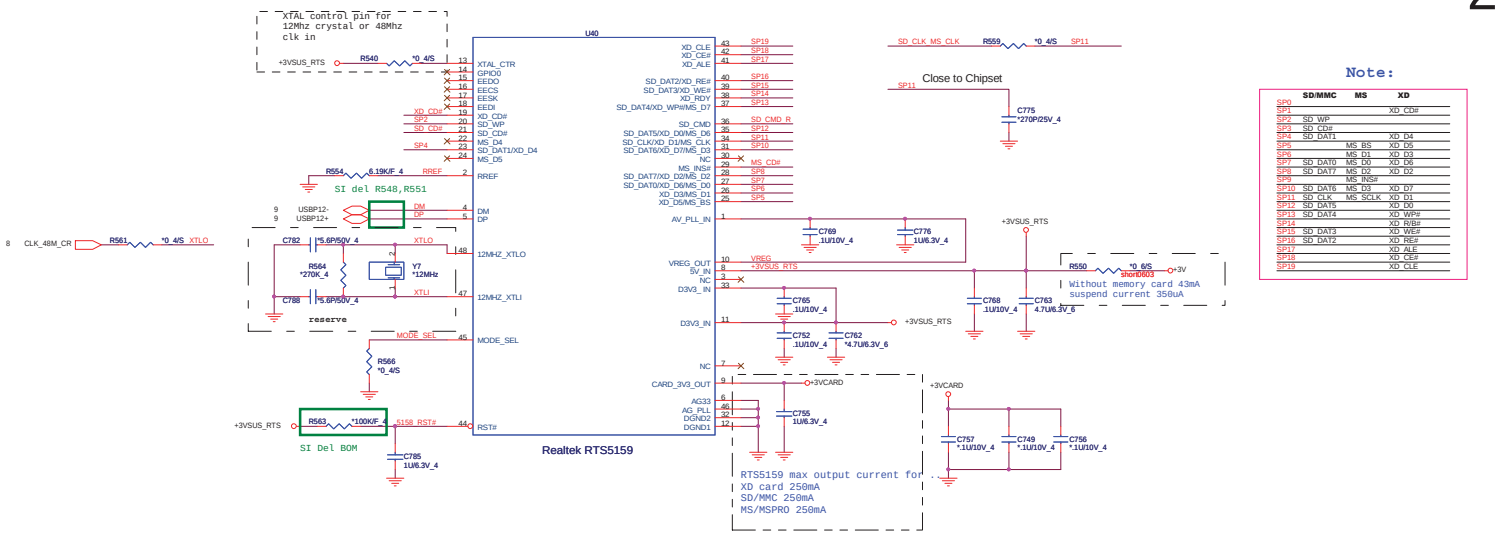
CRT PORT



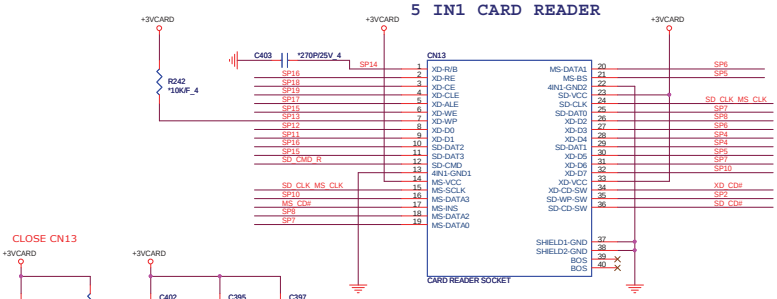
NB5	PROJECT : LX6_LX7 Quanta Computer Inc.		
	Size: Custom	Document Number: CRT/HDMI Conn	Rev: 1A
	Date: Tuesday, February 02, 2010	Sheet 23 of 44	



Note:

	SD/MMC	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

XD,MMC/SD,MS/MSP
5 IN1 CARD READER



5 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/xD Cards

+3V 2,3,7,8,9,10,11,12,13,21,22,23,25,26,27,28,29,30,31,32,33,34,37,40,41

NB5

PROJECT : LX6_LX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5159 & CR SOCKET	1A

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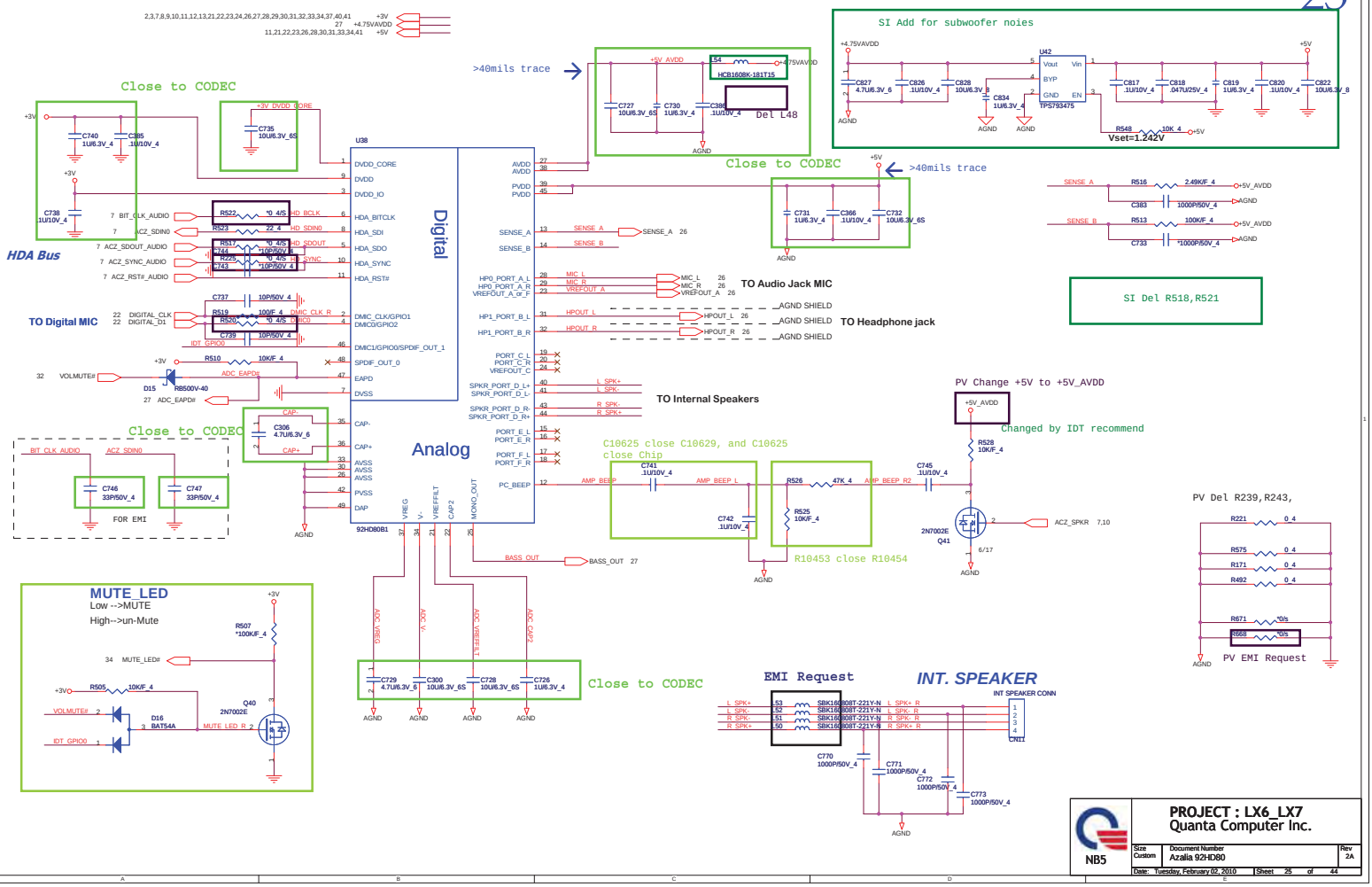

NB5	PROJECT : LX6_LX7 Quanta Computer Inc.		
	Size: Custom	Document Number: Azalia 92HD80	Rev: 2A
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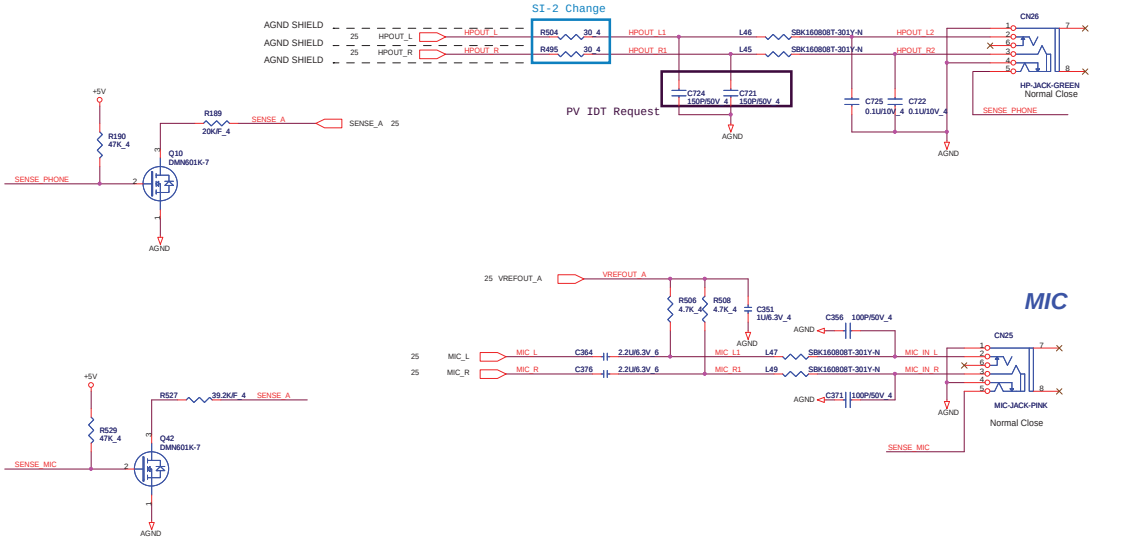
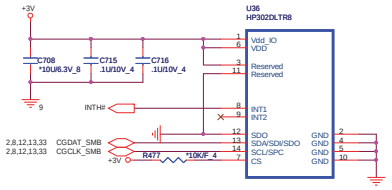
Line out



MIC

Accelerometer Sensor

SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



Pin 12: Low 38hex

Pin 12: unconnected/floating 3Ahex

NB5	PROJECT : LX6_LX7 Quanta Computer Inc.	
Size: Custom	Document Number: Audio Jack/Accelerometer	Rev: 1A
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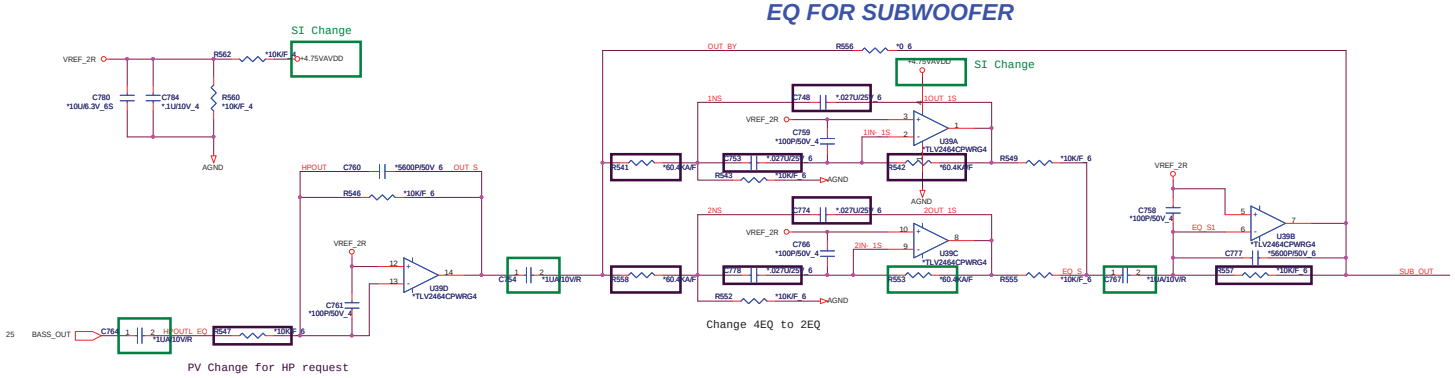
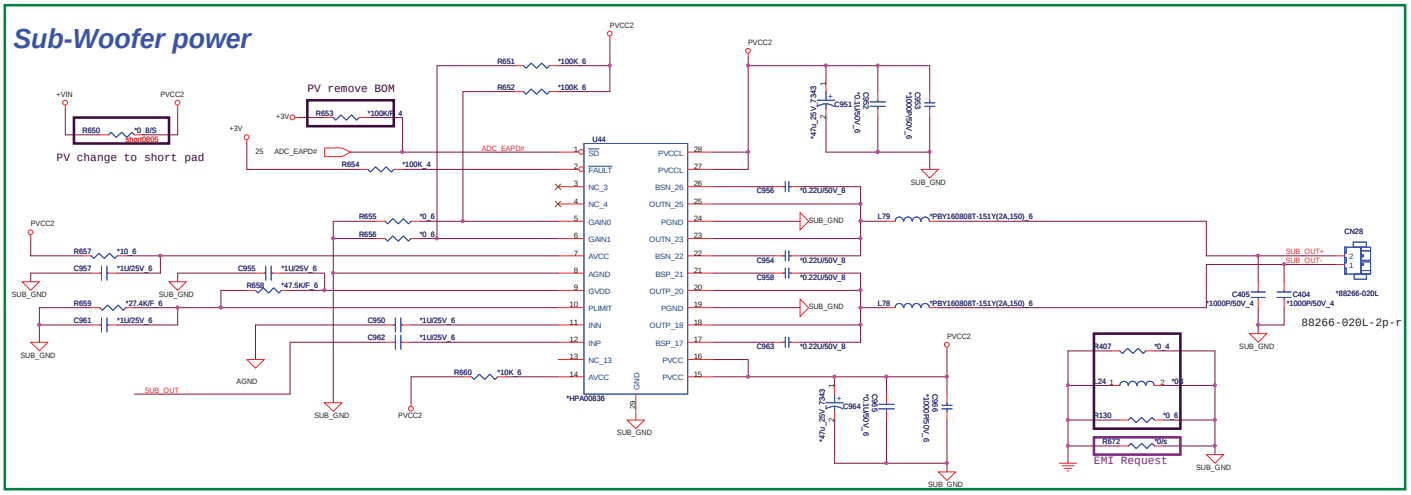
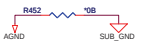
EQ FOR SUBWOOFER



Sub-Woofer power



PV Del R574,R241,R240



GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

+3V 2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,28,29,30,31,32,33,34,37,40,41
+4.75VAVDD 25
+VIN 22,35,36,37,39,40,41,42,43

PROJECT :	LX6_LX7
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: SUBWOOFER (EQ & AMP.)
Rev: 1A	
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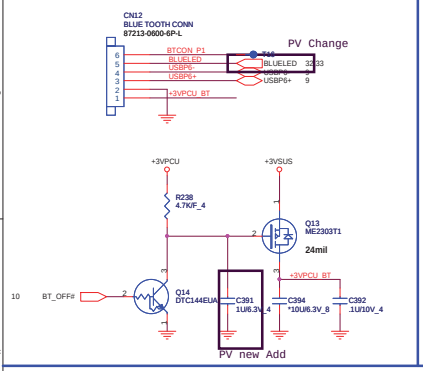
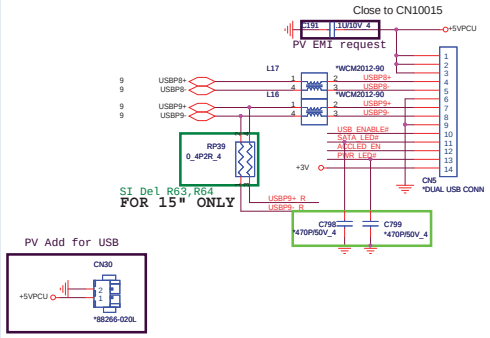
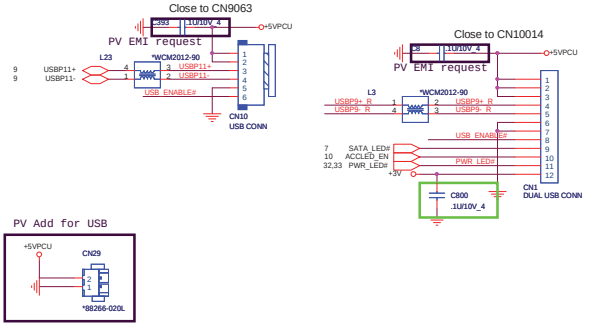
BLUETOOTH



RIGHT SIDE USBX2 for 17"

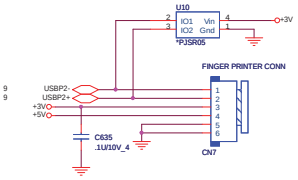


RIGHT SIDE USB for 15"

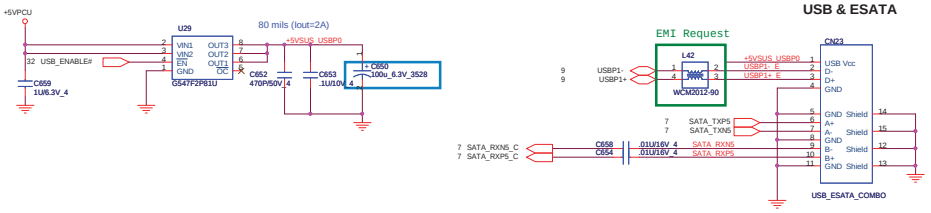


USB fingerprint CON

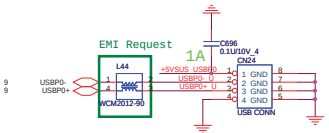
1. USBP2-
2. USBP2+
3. +3V
4. +5V
5. SYSTEM GND
6. SYSTEM GND



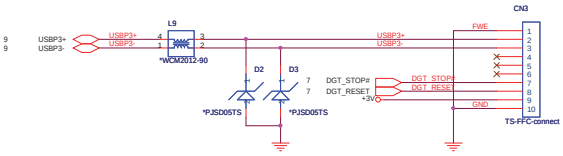
E-SATA



LEFT USB PORT



Touch screen for 15"



PROJECT :	LX6_LX7
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: BT/WC/FT/Touchscreen
Rev: 1A	
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T : Stuffed for RTL8111DL(10/100/1000)

for RTL8111DL use Close Pin 44,45

SI del R452

Remove R3571,R3573

R3571 and R3573 are used in RTL8111DL , remove R3573 if switching regulator is enable , Remove R3571 external power is used.

SI del R130

Close to PIN 1

AL08111DB00 RTL8111DL-GR

RTL8111DL-VB-GR

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

NS892402:GIGABIT

Power trace Layout 寬度> 60mil

>60mil

>60mil

L23
RTL8111DL (Gaga lan) use 4.7uH power choke A>600mA tolerance ±15%

Close to 8111DL DVDD12 pins-- 19

Close to 8111DL DVDD12 pins-- 10, 13, 30, 36, 39.

RJ45

FOR EMI

Link

PROJECT : LX6_LX7
Quanta Computer Inc.

NB5

Size: Custom | Document Number: 8103E/RJ45 | Rev: 1A

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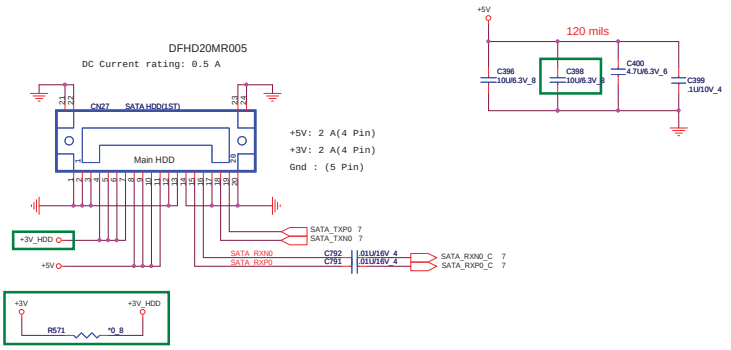
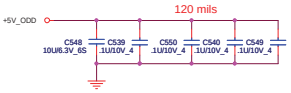
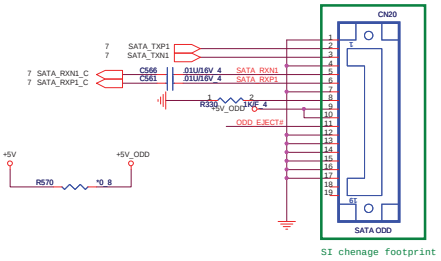
SATA HDD CONNECTOR



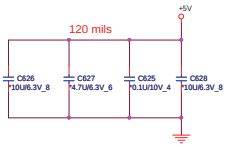
SATA CD-ROM

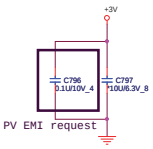


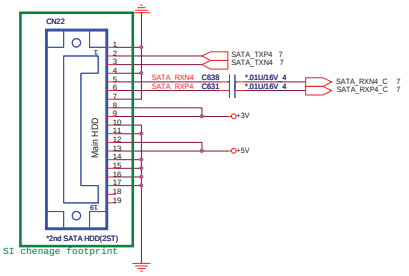


SI chenage footprint

SATA_2 CONNECTOR FOR 17.3"

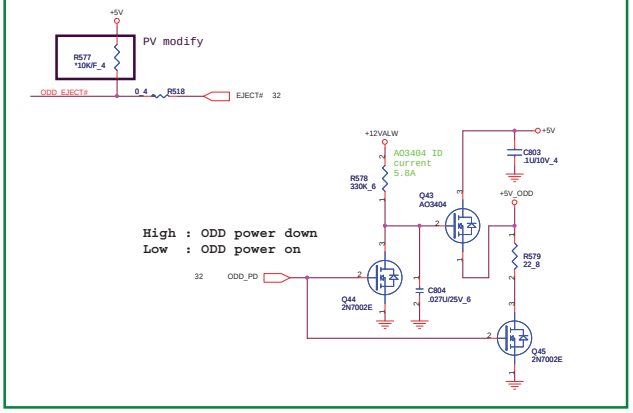






SI chenage footprint

SI Add



+3V 2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,31,32,33,34,37,40,41
+5V 11,21,22,23,25,26,28,31,33,34,41
+12VALW 22,34,39,41

NB5

PROJECT : LX6_LX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ODD/HDD/ANT	1A

Date: Tuesday, February 02, 2010 Sheet 30 of 44

For UMA HDMI function

for UMA

SI EMI Request

MV Del R181,R182

U14

POWER

*PS8101

CONTROL

GND

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCL/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

for UMA

Close to HDMI(CN21) Connector

for SG/DIS

Close to HDMI(CN21) Connector

Signals		PDT	CHR	PIM
PC1	Ra	NC	4.7K	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	1.2K	4.7K
PC1	Re	NC	NC	4.7K
HDMI_OE#	Rf	NC	4.7K	NC
PC0	Rg	4.7K	4.7K	4.7K

Vendor:PDT P/N:AL008101000
Vendor:CHR P/N:AL007318002
Vendor:PIM P/N:ALP411LS004

U14
for UMA

PV EMI Request

for Dis/SG

Close to HDMI(CN21) Connector

SI Del Q29,R378,R413,R415

MV Change

MV Del R670,R669

PV Change to short pad

PV Del R374,R368,R378 BOM

for UMA/DIS/SG

MV EMI Request

DFHD19MR021

PROJECT : LX6_LX7
Quanta Computer Inc.
NB5
KB/POWER CONN
Size: Custom
Rev: 1A
Date: Tuesday, February 02, 2010
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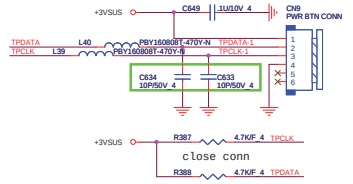
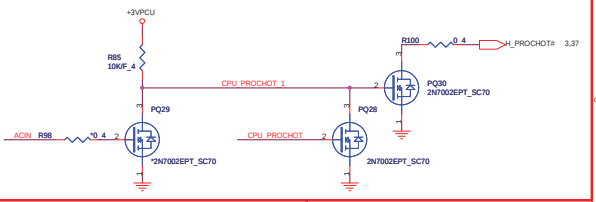
TOUCH PAD CONNECTOR & ON/OFF BOTTOM

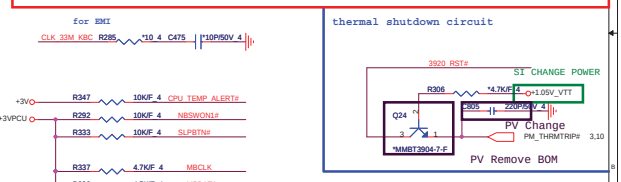


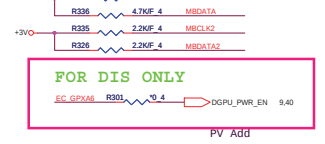
AC present: AC_IN-->high, CPU_PROCHOT-->low , H_PROCHOT#-->high

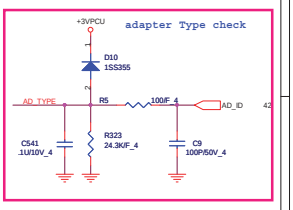
Remove AC: AC_IN-->low, CPU_PROCHOT-->low , H_PROCHOT#-->low

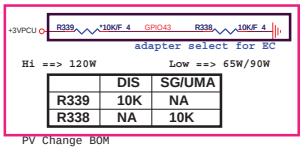
Remove AC and re-cove prochot: AC_IN-->low, CPU_PROCHOT--> high, H_PROCHOT#--> high





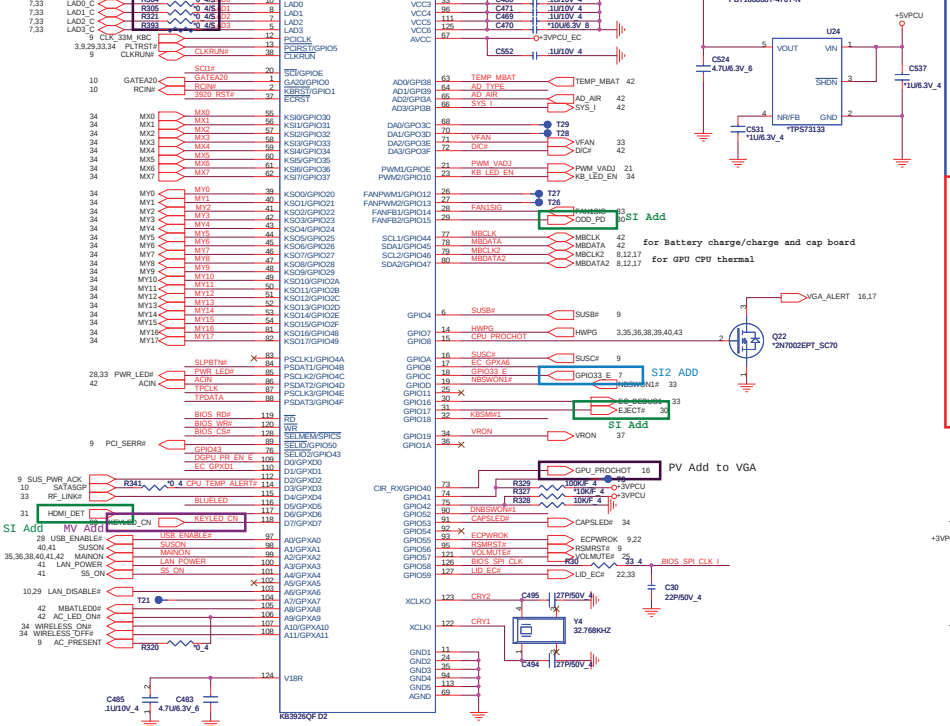


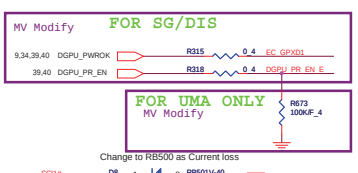


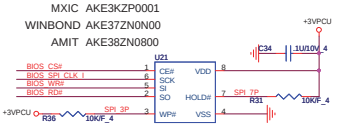


	DIS	SG/UMA
R339	10K	NA
R338	NA	10K

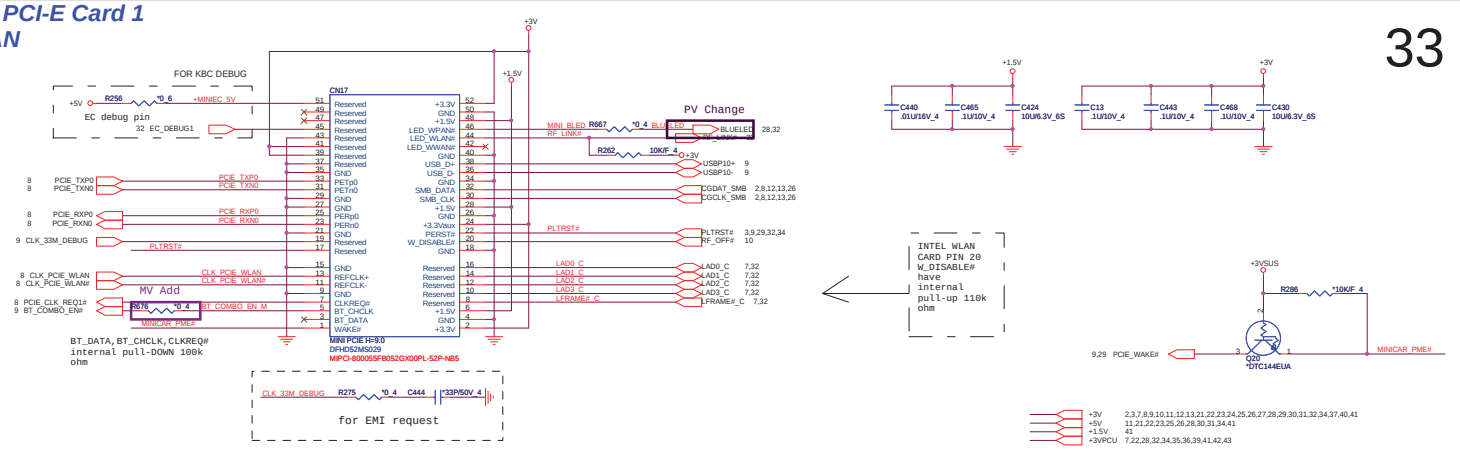
PV Change BOM



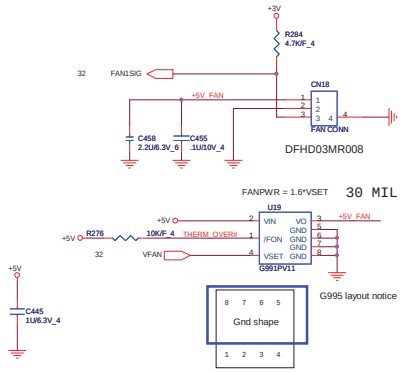




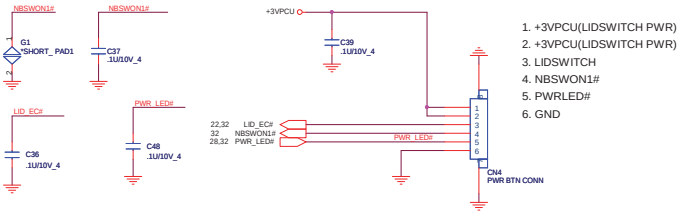
Mini PCI-E Card 1
WLAN



CPU FAN



POWER BOTTON CONNECT



1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. NBSWON1#
5. PWRLED#
6. GND

NB5	PROJECT : LX6_LX7 Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCIE CONN/FAN	Rev: 1A
Date: Tuesday, February 02, 2010	Sheet 33 of 44	

KEYBOARD PULL-UP

clear ABS 758 resin for key cap.
7 LEDs for 15.4" (total LED current 140mA)
11 LEDs for 17" (Total LED current 220mA)

SI Add

PV Change BOM

MV Add

KB backlight for 15"

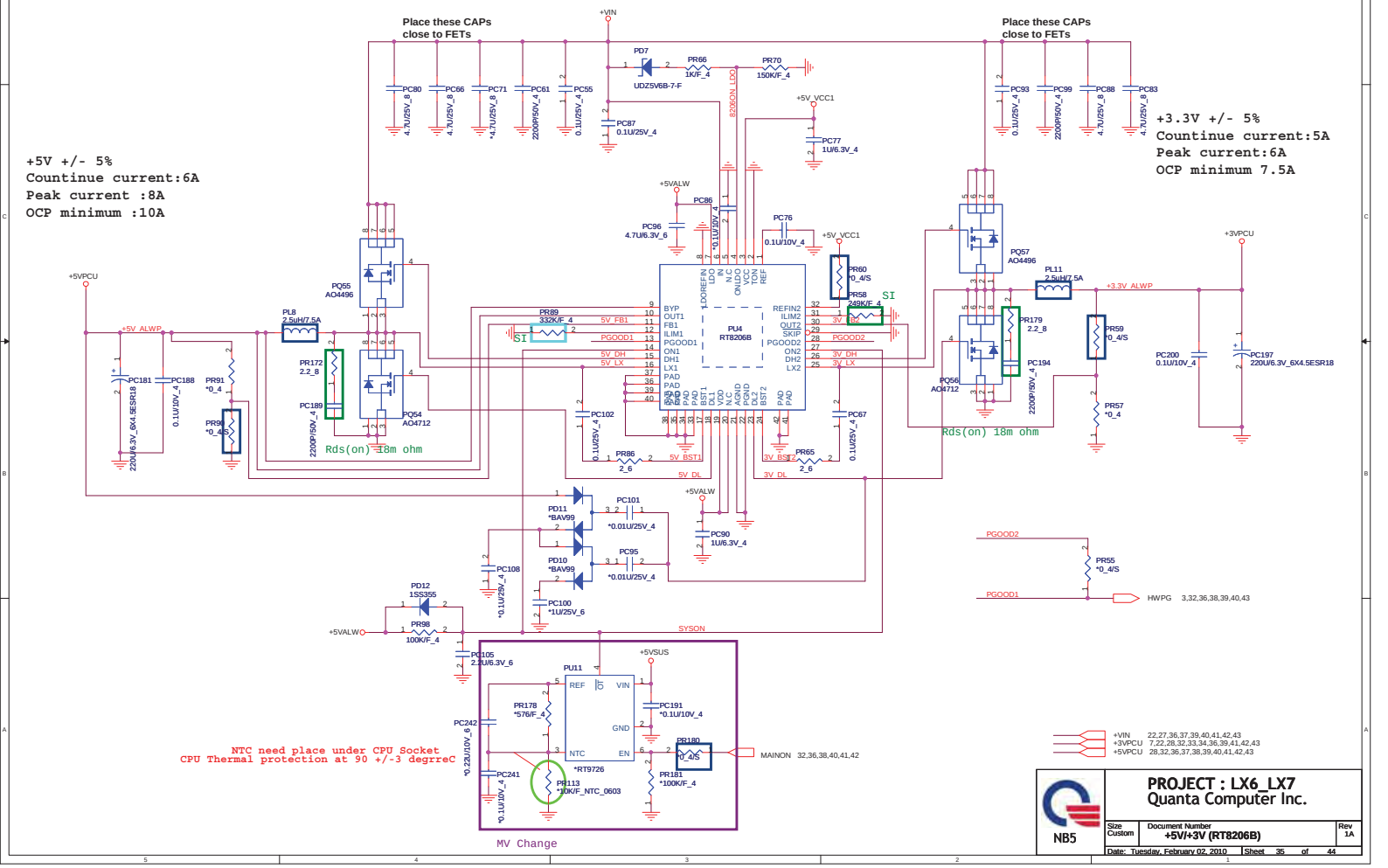
140 mA

4.LEDVCC
3. LEDVCC
2. GND
1. GND

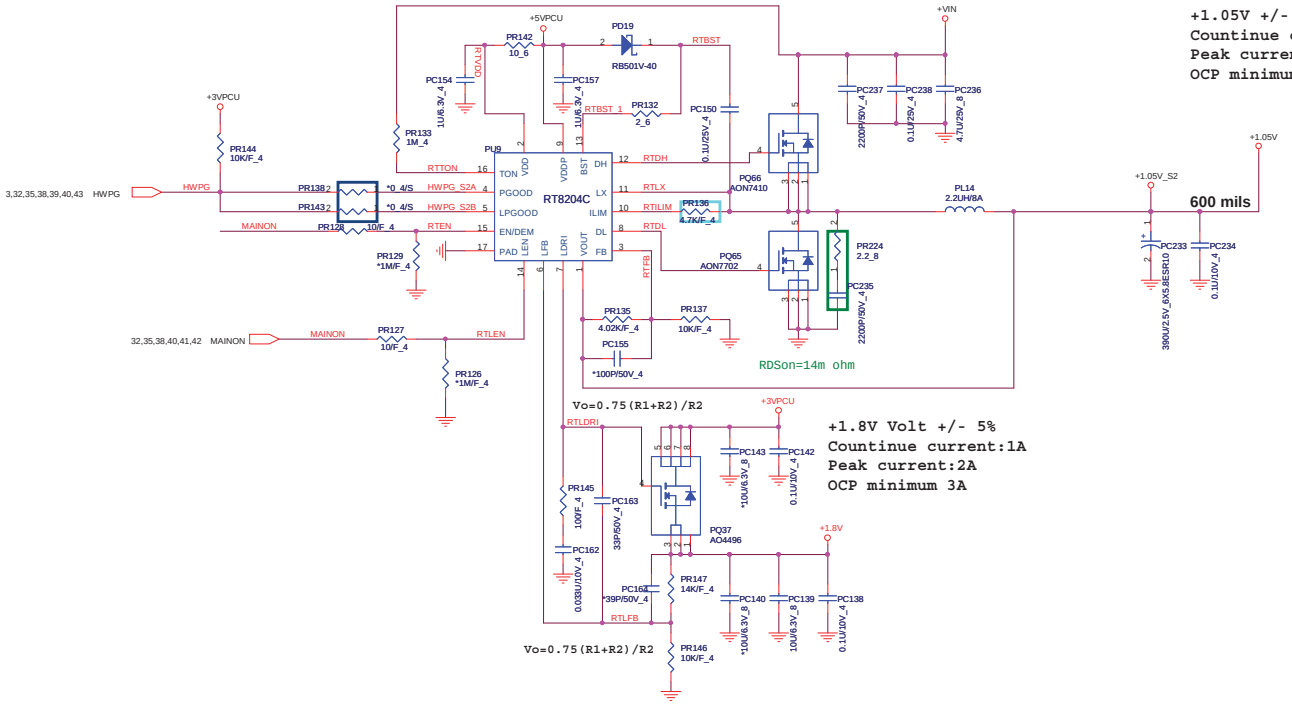
FOR DIS ONLY

FOR SG ONLY

NB5	PROJECT : LX6_LX7 Quanta Computer Inc.
Size: Custom	Document Number: KB
Rev: 1A	
Date: Tuesday, February 02, 2010	Sheet 34 of 44



NB5	PROJECT : LX6_LX7 Quanta Computer Inc.	
Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 1A
Date: Tuesday, February 02, 2010	Sheet 35 of 44	



+1.8V	5,10,11,21,41
+VIN	22,27,35,37,39,40,41,42,43
+1.05V	2,7,8,9,11,37,43
+3VPCU	7,22,28,32,33,34,35,39,41,42,43
+5VPCU	28,32,35,37,38,39,40,41,42,43

PROJECT : LX6_LX7
Quanta Computer Inc.

NB5	Size: Custom	Document Number: +1.05V/+1.8V (RT8204C)
	Date: Tuesday, February 02, 2010	Sheet 36 of 44

Rev 1A

	DIS (Clarksfild)	SG/UMA (Arburndle)
不上件		PQ45 PQ46 PQ43 PQ44
PR14	1.91k(OCP=63A) (CS21912FB13)	1.69k(OCP=55A) (CS21692FB01)
PR34	4.7k (CS24702FB10)	4.87k (CS24872FB07)

+VCORE
Countinue current:24A
Peak current:40A
OCP minimum 48A

Connect to input caps

This NTC Close to Phase 1 Inductor

Panasonic
ERT-J0EV474J

Shortest the net trace

Close to Phase 1 Inductor

OCP:
60A --> PR66 = 1.91 Kohm
48A --> PR66 = 1.69 Kohm

+3V 2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,40,41
+VIN 22,27,35,36,39,40,41,42,43
+1.05V 2,7,8,9,11,36,43
+5VPCU 28,32,35,36,38,39,40,41,42,43
+VCORE 5
+1.05V_VTT 3,5,10,11,32,38,43

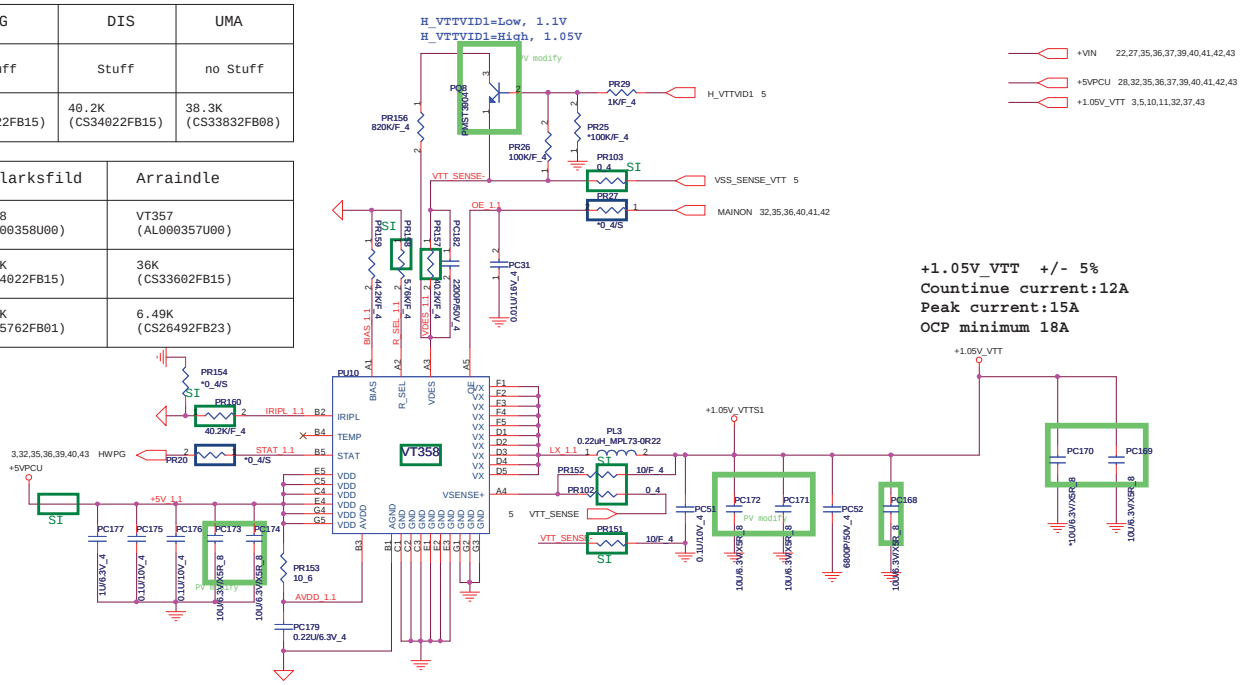
NB5

PROJECT : LX6_LX7
Quanta Computer Inc.

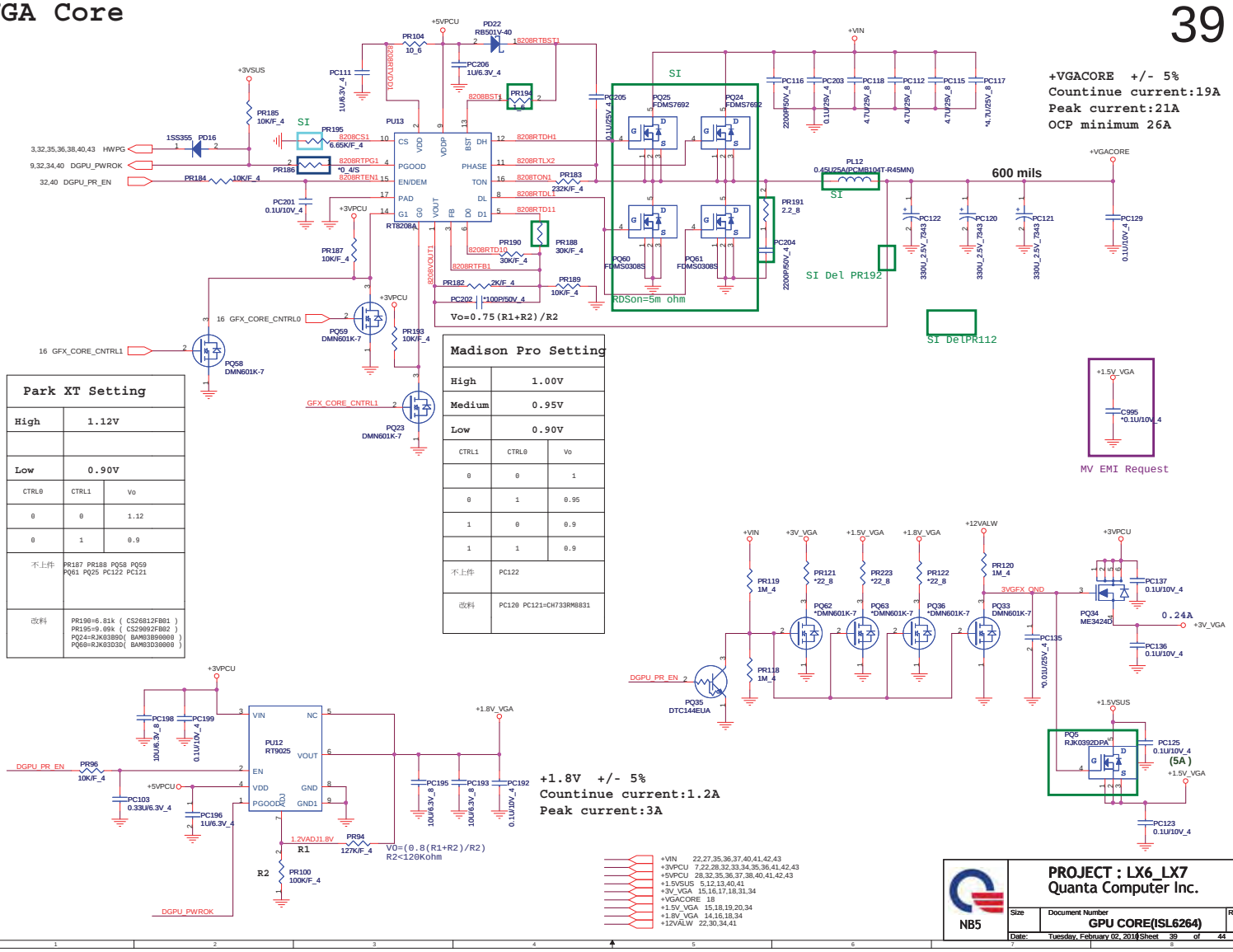
Size: Custom | Document Number: CPU Core (ADP3212) | Rev: 1A
Date: Tuesday, February 02, 2010 | Sheet 37 of 44

	SG	DIS	UMA
PR156 PR26 PR29 PQ8	Stuff	Stuff	no Stuff
PR157	40.2K (CS34022FB15)	40.2K (CS34022FB15)	38.3K (CS33832FB08)

	Clarksfild	Arraindle
PU10	VT358 (AL000358U00)	VT357 (AL000357U00)
PR160	40.2K (CS34022FB15)	36K (CS33602FB15)
PR158	5.76K (CS25762FB01)	6.49K (CS26492FB23)



VGA Core



Park XT Setting

High	1.12V	
Low	0.90V	
CTRL0	CTRL1	Vo
0	0	1.12
0	1	0.9
不上件	PR187 PR188 PQ58 PQ59 PQ61 PQ25 PC122 PC121	
改料	PR190=6.81k (CS26812FB01) PR195=9.09k (CS29092FB02) PQ24=RJK03B9D(BAM03B90000) PQ60=RJK03D3D(BAM03D30000)	

Madison Pro Setting

High	1.00V	
Medium	0.95V	
Low	0.90V	
CTRL1	CTRL0	Vo
0	0	1
0	1	0.95
1	0	0.9
1	1	0.9
不上件	PC122	
改料	PC120 PC121=CH733RM8831	

+VIN 22,27,35,36,37,40,41,42,43
+3VPCU 7,22,28,32,33,34,35,36,41,42,43
+5VPCU 28,32,35,36,37,38,40,41,42,43
+1.5VSUS 5,12,13,40,41
+3V_VGA 15,16,17,18,31,34
+VGACORE 18
+1.5V_VGA 15,18,19,20,34
+1.8V_VGA 14,16,18,34
+12VALW 22,30,34,41

NB5	PROJECT : LX6_LX7 Quanta Computer Inc.		
	Size	Document Number GPU CORE(ISL6264)	Rev 1A
	Date: Tuesday, February 02, 2016	Sheet 39 of 44	

+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

(VTT/2A)
+0.75V_DDR_VTT
PC56 10U/6.3V_8
PC57 10U/6.3V_8
+1.5VSUS_1
PR61 *0_4/S
(3mA)
12 DDR_VTTREF
PC70 0.033U/10V_4
PU3 RT8207AGQW
VTTGND VTTSNS GND MODE VTTREF COMP NC VDDQSNS VDDQSET S3 S5 NC
GND VTT VLDOIN VBST DRVH LL DRVL PGND CS_GND CS V5IN V5FILT PGOOD
+1.5VSUS
+5VPCU
PC53 *10U/6.3V_8
PD4 RB501V-40
PC50 0.1U/25V_4
PR39 2_6
1116VBST
1116DRVH
1116LL
1116DRVL
1116CS
V5FILT
PR75 *0_4
1116VDDQSET
PR56 7.5K/F_4
32,41 SUSON
+VIN
PR74 619K/F_4
1116TONSET
HWPG
HWPG 3,32,35,36,38,39,43
PC73 1U/6.3V_4
PR68 10_6
+5VPCU
PC69 1U/6.3V_4
SI2 Change
36,38,41,42 MAINON
PD9 RB501V-40
PR81 100K/F_4
100k
PC91 0.1U/10V_4
PQ49 RJK03B9D
PQ41 RJK03D3D
SI
PC23 0.1U/25V_4
PC20 4.7U/25V_8
PC21 4.7U/25V_8
PC22 2200P/50V_4
+VIN
PL4 1U18A(PCMB103T-1R0MS)
PR168 2.2_8
PC185 2200P/50V_4
+1.5VSUS_1
+1.5VSUS
PC18 330U_2.5V_7343
PC45 0.1U/10V_4
PR73 10.5K/F_4
PC84 *100P/50V_4
MV Change
PR72 10K/F_4

SG & Discrete Only

+1.0V +/- 5%
Countinue current:1.7A
Peak current:3A

+1.5VSUS
+1.0V_VGA
PC126 10U/6.3V_8
PC210 0.1U/10V_4
PU7 RT9025
VIN NC VOUT EN VDD GND PGOOD ADJ GND1
9,32 DGPU_PWR_EN
PR339 *0_4/S
DGPU_PR_EN 32,39
+5VPCU
PC124 *0.33U/6.3V_4
PC211 1U/6.3V_4
1.2VADJ1.0V
PR115 25.5K/F_4
R1
9,32,34,39 DGPU_PWROK
PR114 *0_4/S
R2
PR116 100K/F_4
VO=(0.8(R1+R2)/R2)
R2<120Kohm
PC128 10U/6.3V_8
PC127 10U/6.3V_8
PC130 0.1U/10V_4

+3V
C977 *0.1U/10V_4
PV EMI Request

+3V
+5VPCU
C999 *0.1U/10V_4
C1002 *0.1U/10V_4
MV EMI Request

+3V 2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,41
+VIN 22,27,35,36,37,39,41,42,43
+5VPCU 28,32,35,36,37,38,39,41,42,43
+1.5VSUS 5,12,13,39,41
+1.0V_VGA 14,16,18,34
+0.75V_DDR_VTT 12,13,41

NB5
PROJECT : LX6_LX7
Quanta Computer Inc.
Size Custom
Document Number DDR3 (RT8207)
Rev 1A
Date: Tuesday, February 02, 2010
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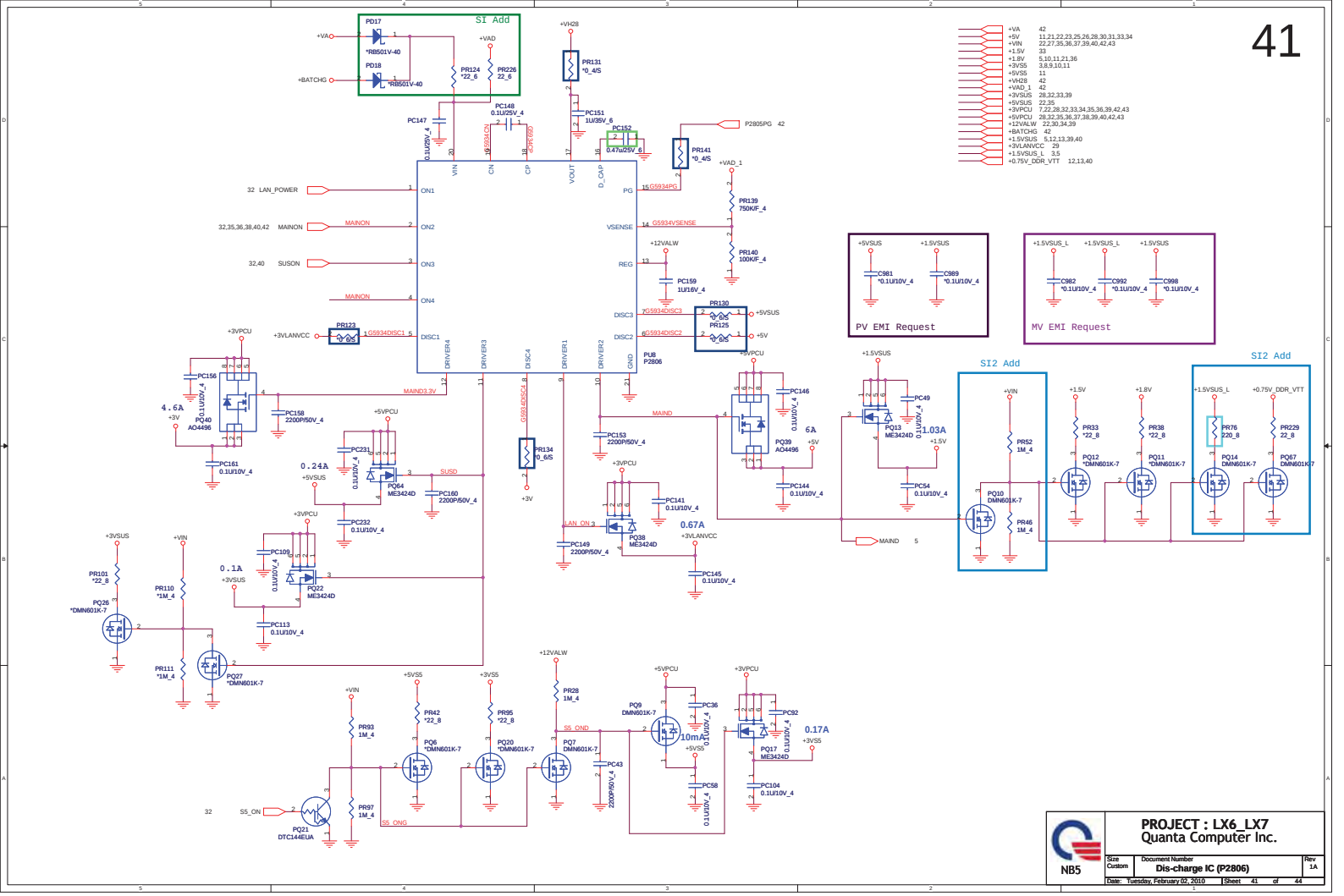
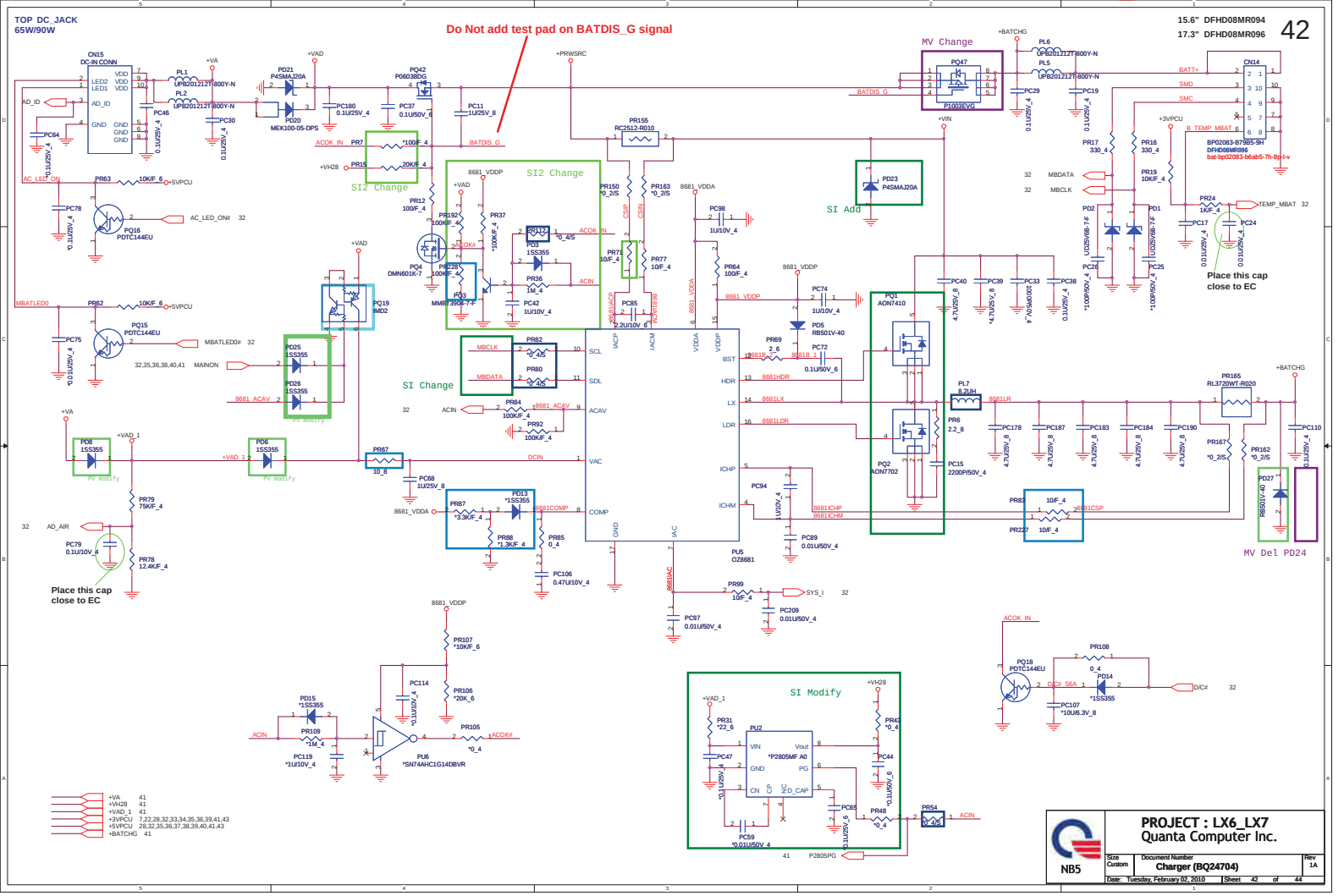


PROJECT :	LX6_LX7
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Dis-charge IC (P2806)
Rev: 1A	
Date: Tuesday, February 02, 2010	Sheet 41 of 44


TOP DC_JACK
65W/90W
Do Not add test pad on BATDIS_G signal
15.6" DFHD08MR094
17.3" DFHD08MR096
42
MV Change
SI2 Change
SI Change
SI Add
SI Modify
Place this cap close to EC
Place this cap close to EC
MV Del PD24
PROJECT : LX6_LX7
Quanta Computer Inc.
NB5
Charger (BQ24704)
Tuesday, February 02, 2010

+VGACORE_IGPU 5
+VIN 22,27,35,36,37,39,40,41,42
+5VPCU 28,32,35,36,37,38,39,40,41,42
+1.05V 2,7,8,9,11,36,37
+3VPCU 7,22,28,32,33,34,35,36,39,41,42
+1.05V_VTT 3,5,10,11,32,37,38

+VGA_UMA +/- 5%
Countinue current:12A
Peak current:18A
OCP minimum 22A

PR117 *0_4/S

8152VCCGFX +5VPCU
PR207 10_6
PC221 1U/6.3V_4
PC220 1U/6.3V_4

+VIN
PR209 10_6
PC222 0.1U/25V_4
PR206 120K/F_4
8152TONGFX

PV EMI Request
PC223 2200P/50V_4
PC226 0.1U/25V_4
PC133 4.7U/25V_8
C983 *0.1U/25V_4
PC134 4.7U/25V_8

PU14 RT8152C

VCC PVDD TON UGATE BOOT PHASE LGATE ISEN ISEN_N CMSET VSEN FB COMP RGND SOFT CM

VID0 VID1 VID2 VID3 VID4 VID5 VID6 DPRSLPVR VRON CLKEN PGOOD VRTT NTC OCSET

5 GFXVR_VID_0 GFXVR_VID_0 31
5 GFXVR_VID_1 GFXVR_VID_1 30
5 GFXVR_VID_2 GFXVR_VID_2 29
5 GFXVR_VID_3 GFXVR_VID_3 28
5 GFXVR_VID_4 GFXVR_VID_4 27
5 GFXVR_VID_5 GFXVR_VID_5 26
5 GFXVR_VID_6 GFXVR_VID_6 25

5 GFXVR_DPRSLPVR PR214 *0_4/S 8152DPRSLPVRGFX 3
5 GFXVR_EN PR212 *0_4/S GFXVR_EN_R 4
+3VPCU PR208 10K/F_4 6
3,32,35,36,38,39,40 HWPG PR210 *0_4/S 8152PGOODGFX 5
+1.05V PR220 10K/F_4 8152VRTTGFX 32
8152NTCGFX 1
8152VCCGFX PR219 10K/F_4 PR218 2.2K/F_4 PR217 4.64K/F_4 8152OCSETGFX 2
PR222 10K/F_NTC_0603
PR215 6.98K/F_4

Place this R close to Inductor

8152UGATEGFX 23
8152BOOTGFX 24
PR216 2_6
PC227 0.1U/25V_4
8152PHASEGFX 22
8152LGATEGFX 20

SI
PQ31 RJK03B9D
PQ32 RJK0389D
PC228 2200P/50V_4
PR221 2.2_8
PR204 3.74K/F_4
PR203 *6.65K/F_4
PC218 0.1U/25V_4
PL13 0.56U25A(PCMC104T-R56MN)

+VGACORE_IGPU_1 +VGACORE_IGPU
800 mils
SI Delete
PC131 330U_2.5V_7343
PC132 330U_2.5V_7343
PC224 0.1U/10V_4

RDSon=5m ohm

8152ISENGFX 16
8152ISEN_NGFX 15
PC212 0.1U/25V_4
PC213 *56p/50V_4
PR201 12K/F_4
8152CMSETGFX 11
8152VSENGFX 12
8152FBGFX 13
PC214 *0.1U/25V_4
PC216 56PF/50V_4
PR198 14K/F_4
PR199 10K/F_4
PR197 10K/F_NTC_0603
PC215 82PF/50V_4
PR225 100/F_4
SI ADD
+VGACORE_IGPU
VCC_AXG_SENSE 5
VSS_AXG_SENSE 5
8152COMPGFX 14
PR202 56K/F_4
SI
PR205 100/F_4
PC219 5600p/25V_4
8152SOFTGFX 8
8152CMGFX 10
GFXVR_IMON 5
PR200 86.6K/F_4
PC217 0.01U/25V_4

Place this R close to Inductor

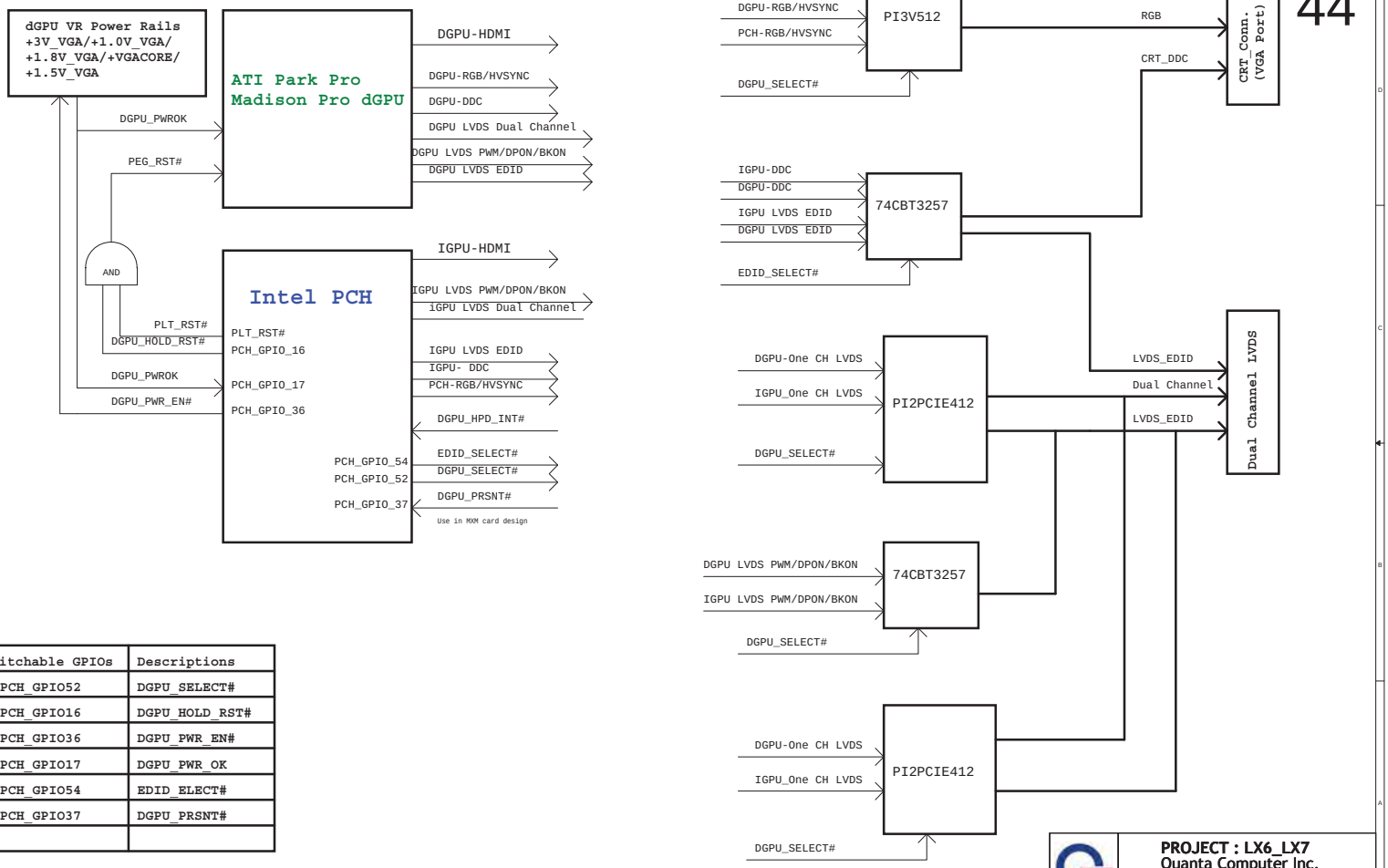
GND PAD PAD PAD PAD PAD PAD PAD PAD PAD PAD PAD PAD PGND
18 33 35 34 36 37 38 39 40 41 42 21

MV Change

+1.05V_VTT
PR213 *1K/F_4
GFXVR_EN_R
PR211 *1K/F_4

+1.05V_VTT +1.05V_VTT
C994 *0.1U/10V_4
C993 *0.1U/10V_4
MV EMI Request

PROJECT : LX6_LX7
Quanta Computer Inc.
NB5
Size Custom
Document Number UMA GPU CORE (RT8152C)
Rev 1A
Date: Tuesday, February 02, 2010 Sheet 43 of 44



Switchable GPIOs	Descriptions
PCH_GPIO52	DGPU_SELECT#
PCH_GPIO16	DGPU_HOLD_RST#
PCH_GPIO36	DGPU_PWR_EN#
PCH_GPIO17	DGPU_PWR_OK
PCH_GPIO54	EDID_ELECT#
PCH_GPIO37	DGPU_PRSNT#

NB5

PROJECT : LX6_LX7
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