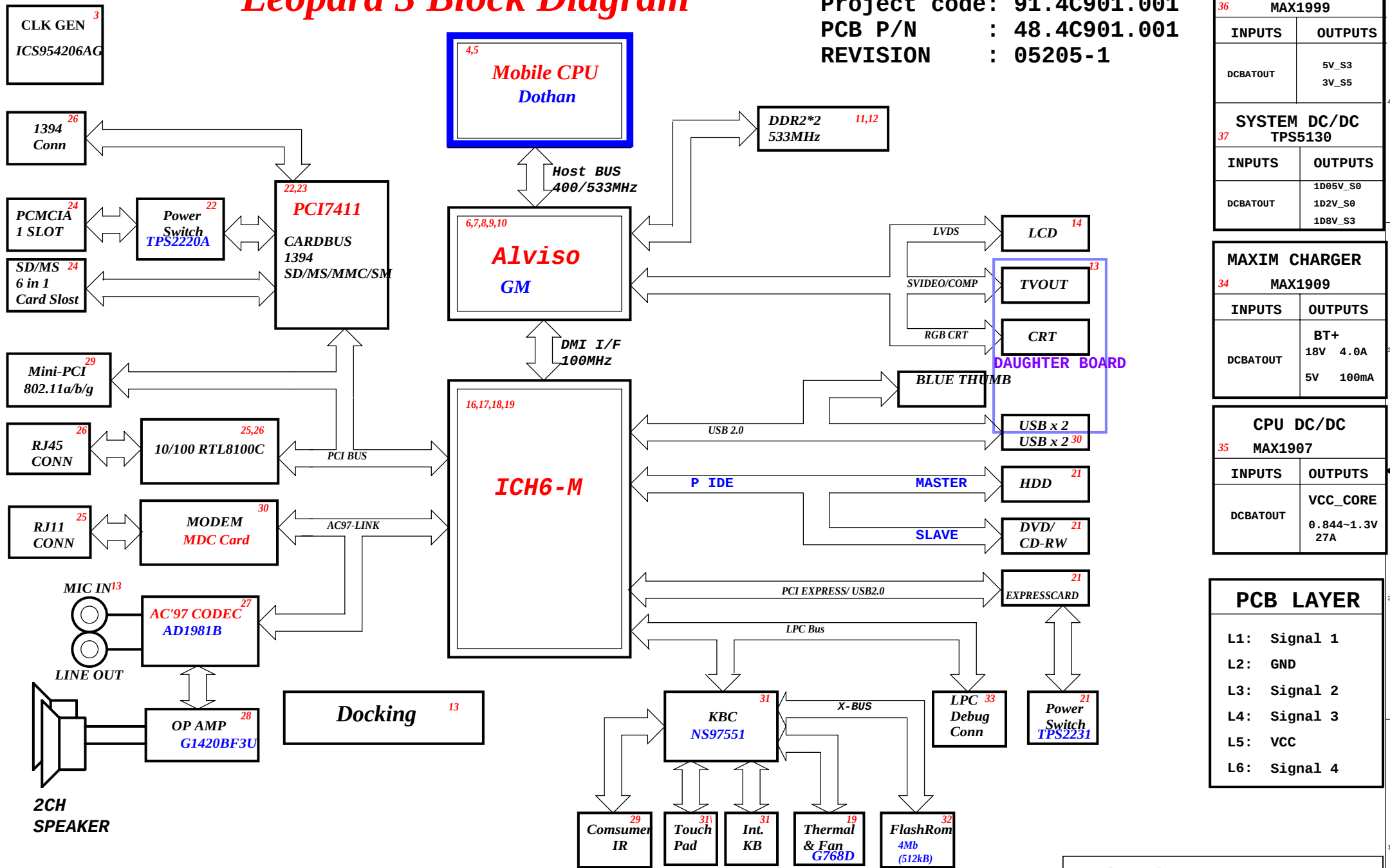


Leopard 3 Block Diagram

Project code: 91.4C901.001
PCB P/N : 48.4C901.001
REVISION : 05205-1



SYSTEM DC/DC MAX1999	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5
SYSTEM DC/DC TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 1D8V_S3
MAXIM CHARGER MAX1909	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA
CPU DC/DC MAX1907	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

ICH6-M Integrated Pull-up
and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDRQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series
Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

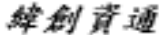
Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
5V_S3= 5 Voltage suspend to RAM(S3 state)
5V_S5= 5 Voltage soft off(S5 state)
3D3V_S0= 3.3 Voltage power up on system work(S0 state)
3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
3D3V_S5= 3.3 Voltage soft off(S5 state)
LVDDR_1D8V= 1.8 Voltage power up on system work(S0 state)
1D8V_S3= 1.8Voltage suspend to RAM(S3 state)
2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S5= 1.5 Voltage soft off(S5 state)
DDR_VREF_S3= 0.9 Voltage suspend to RAM(S3 state)
0D9V_S0= 1.25 Voltage power up on system work(S0 state)
1D2_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
1D05V_S0= 1.05 Voltage power up on system work(S0 state)
CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0#/GNT0#
Cardbus Controller TI7411	AD22	(CARBUS)P_INTG# (1394)P_INTF# (CARD READER)P_INTG#	REQ1#/GNT1#
LAN	AD23	P_INTE#	REQ2#/GNT2#
Blue Thumb	AD24		



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

ITP

Size
A3

Document Number

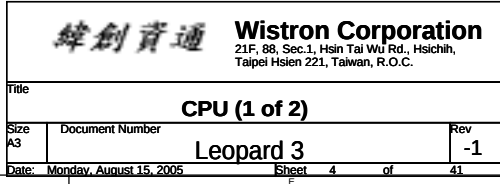
Leopard 3

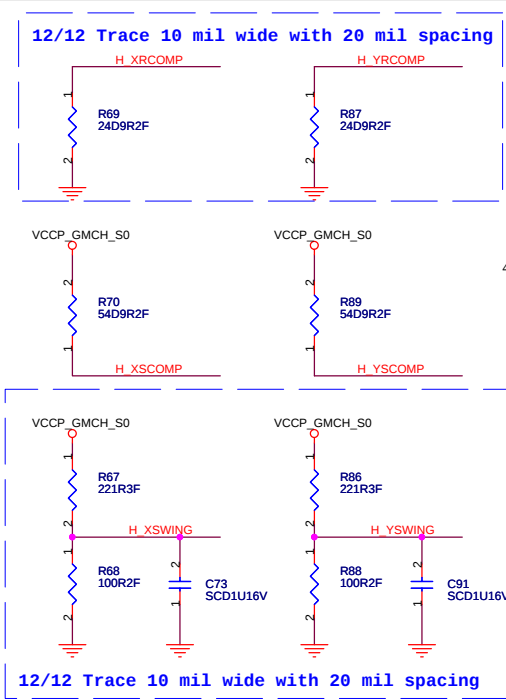
Rev
-1

Date: Tuesday, July 12, 2005

Sheet 2 of 41

F



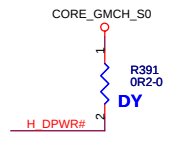
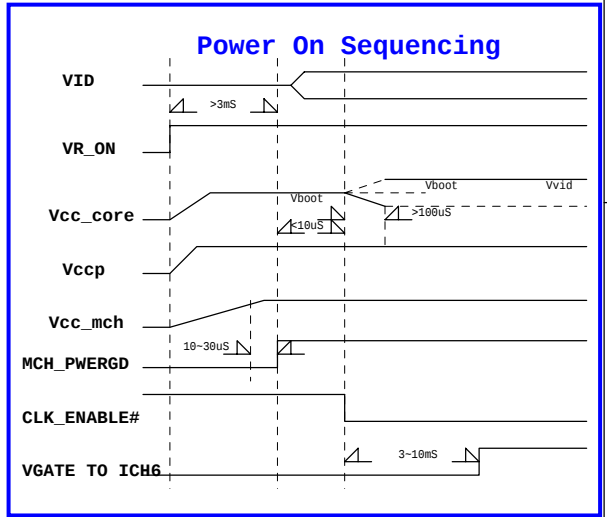
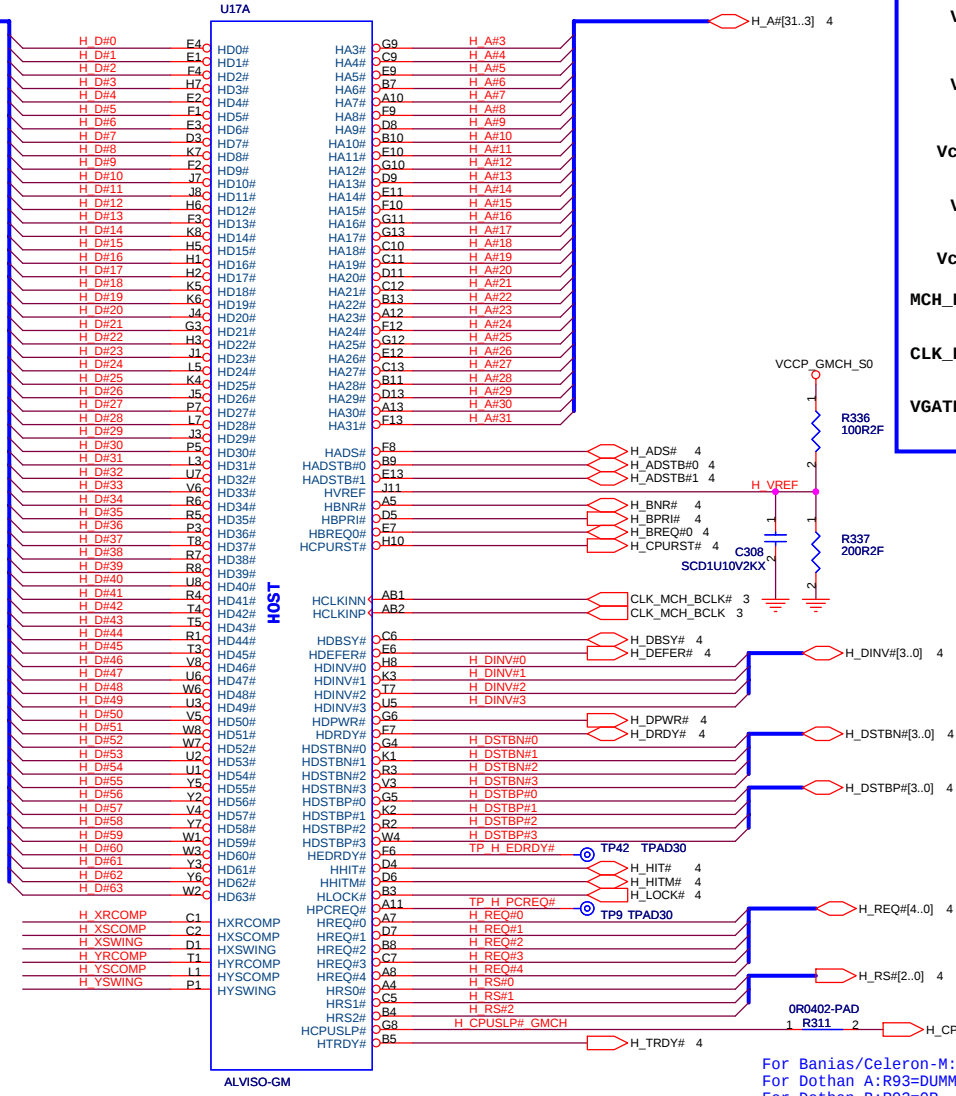


Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

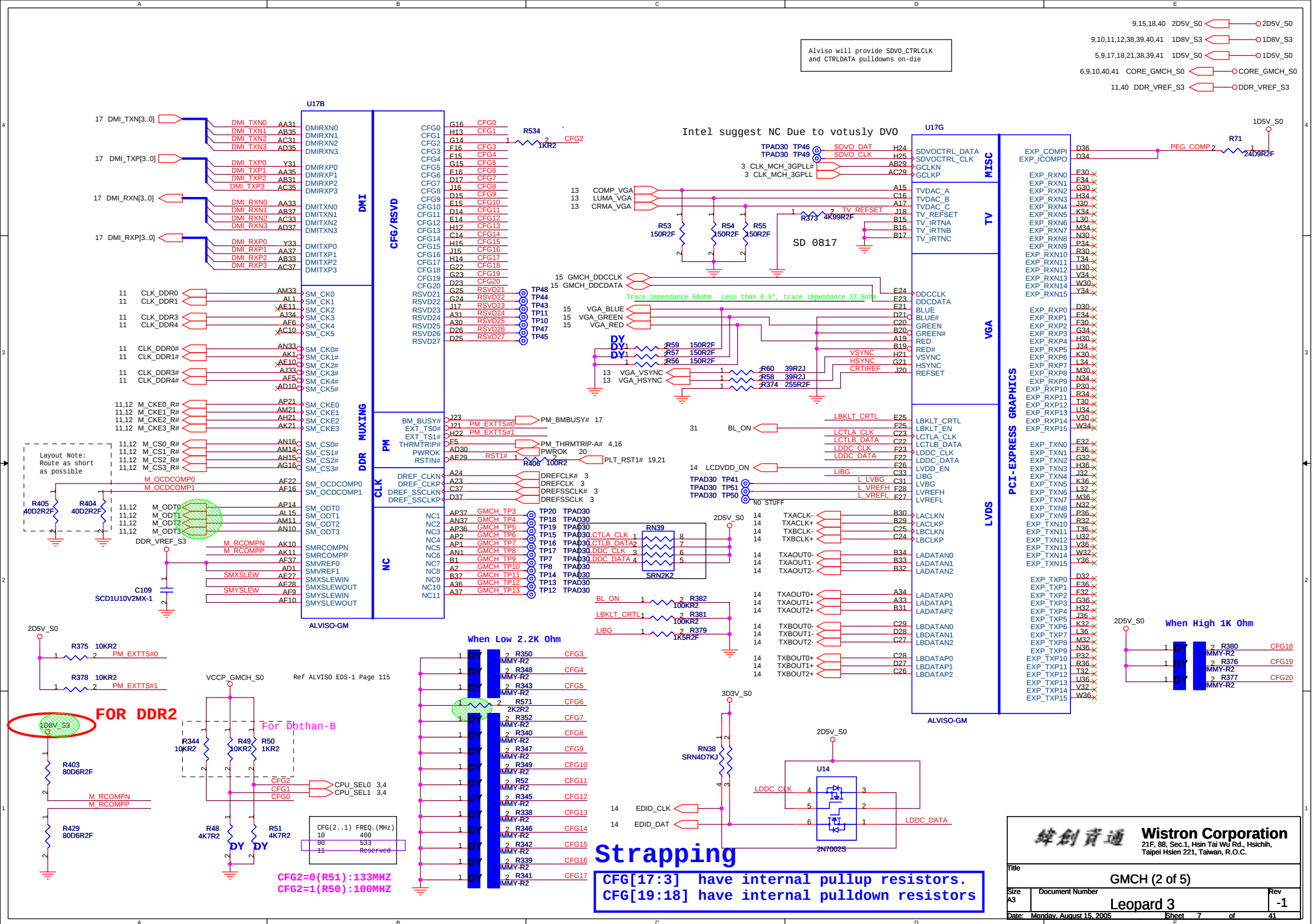
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 101 = FSB400 others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	0 = DDR2 1 = DDR1 (Default)
CFG7	CPU Strap	0 = Reserved 1 = Dothan (Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes 1 = Normal (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reserved	
CFG18	GMCH core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reserved	
SDV0CTRL_DATA	SDVO Present	0 = No SDVO device present(Default) 1= SDVO device present

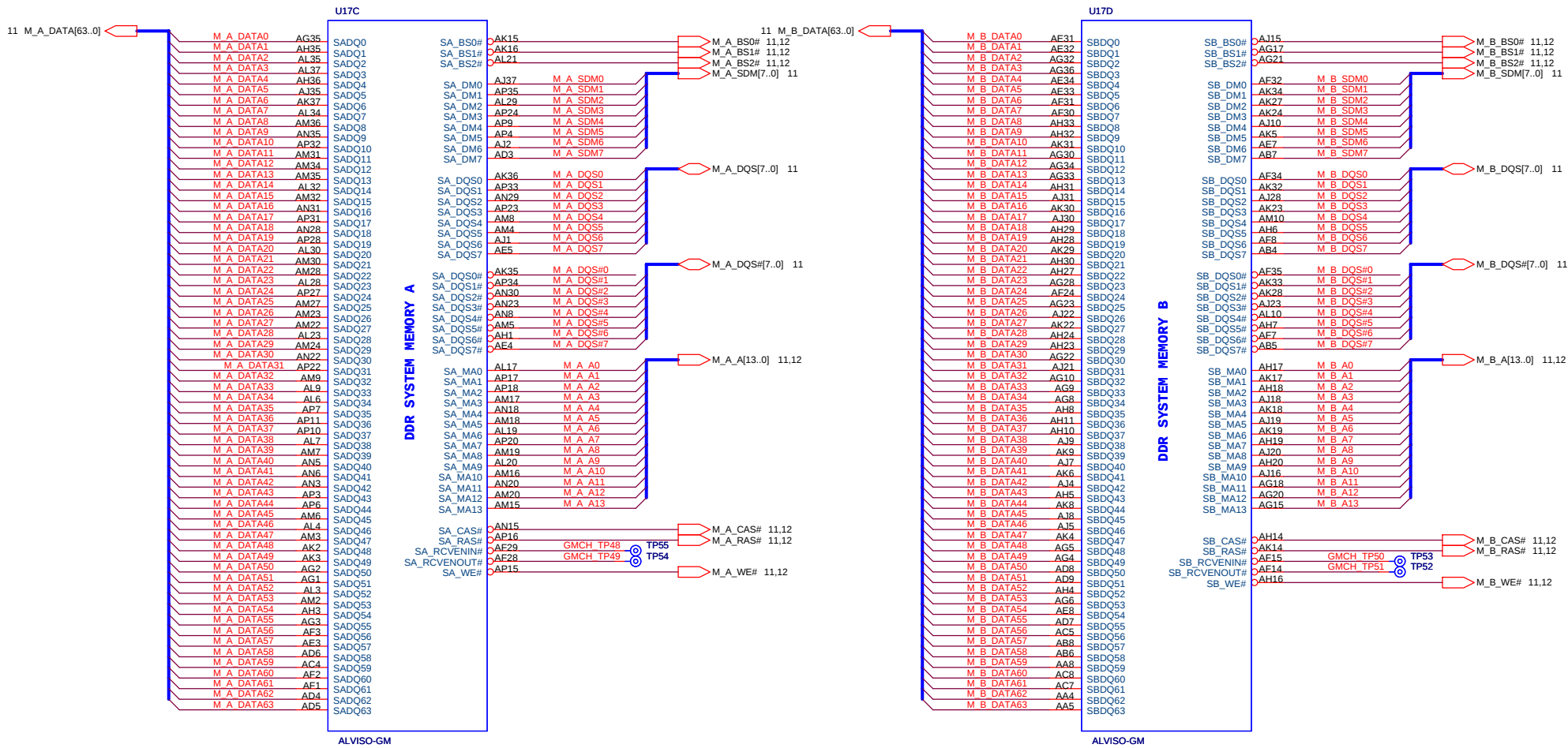
NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK in signal.

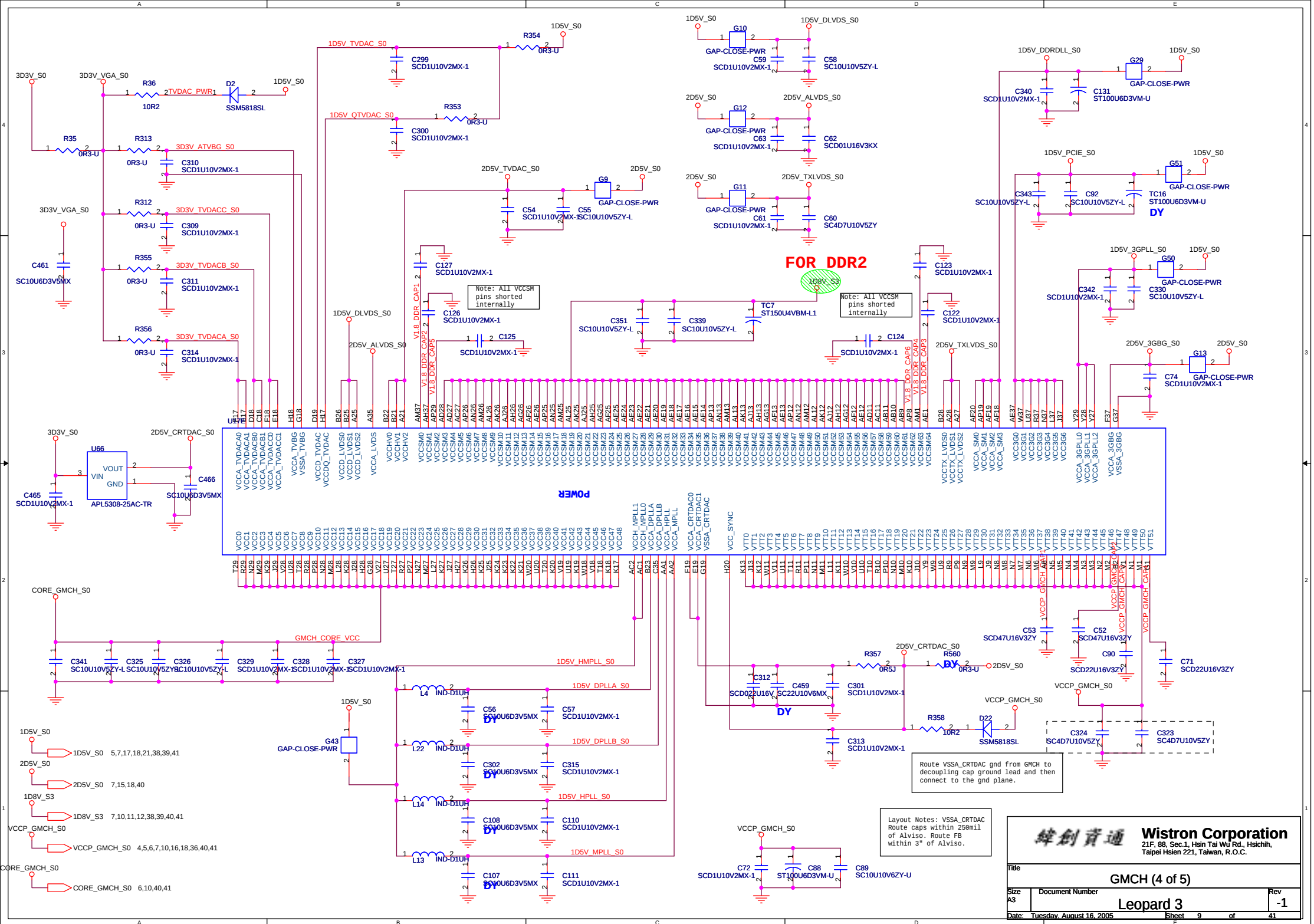


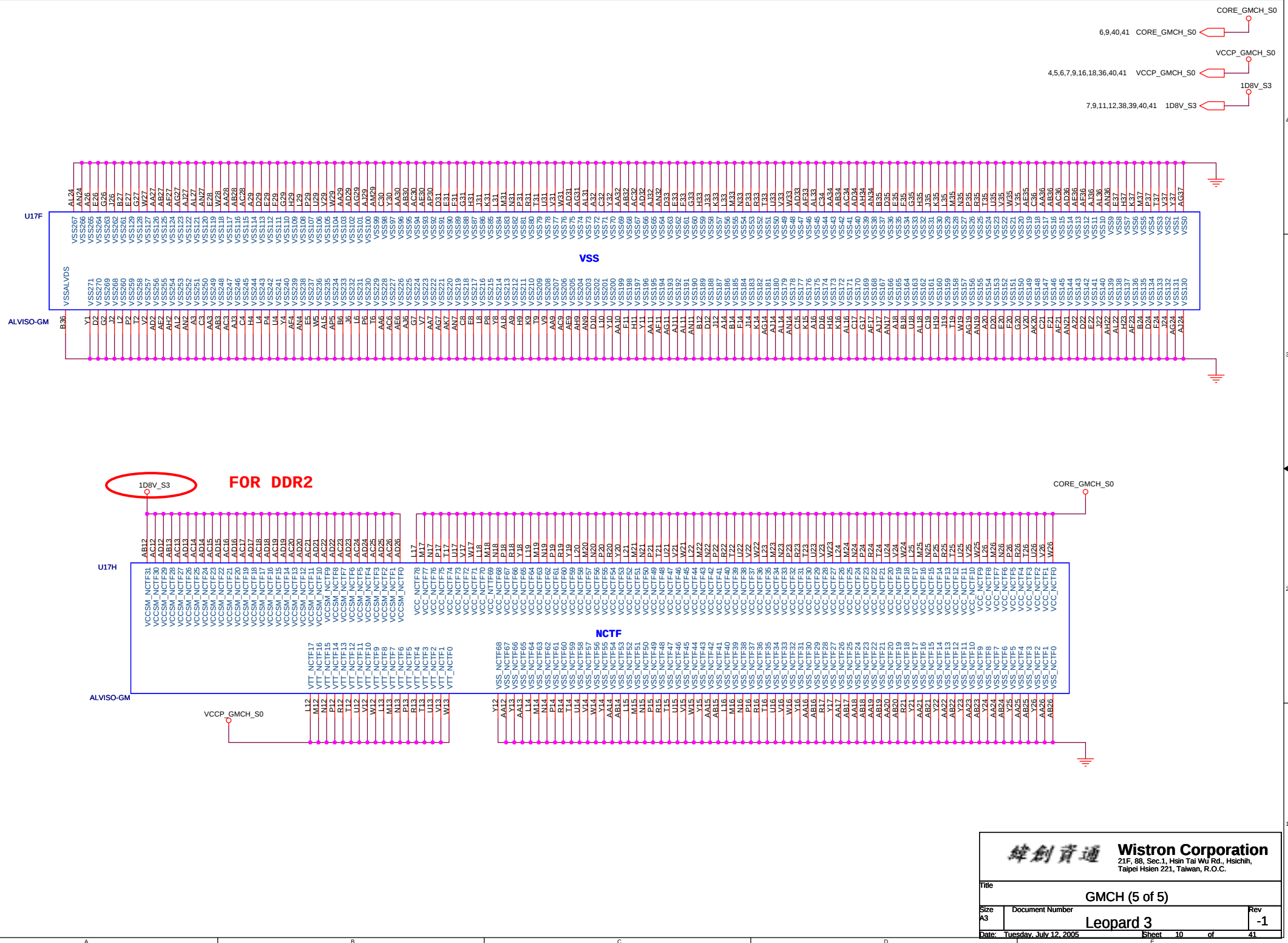
For Banias/Celeron-M:R93=DUMMY
For Dothan A:R93=DUMMY
For Dothan B:R93=0R

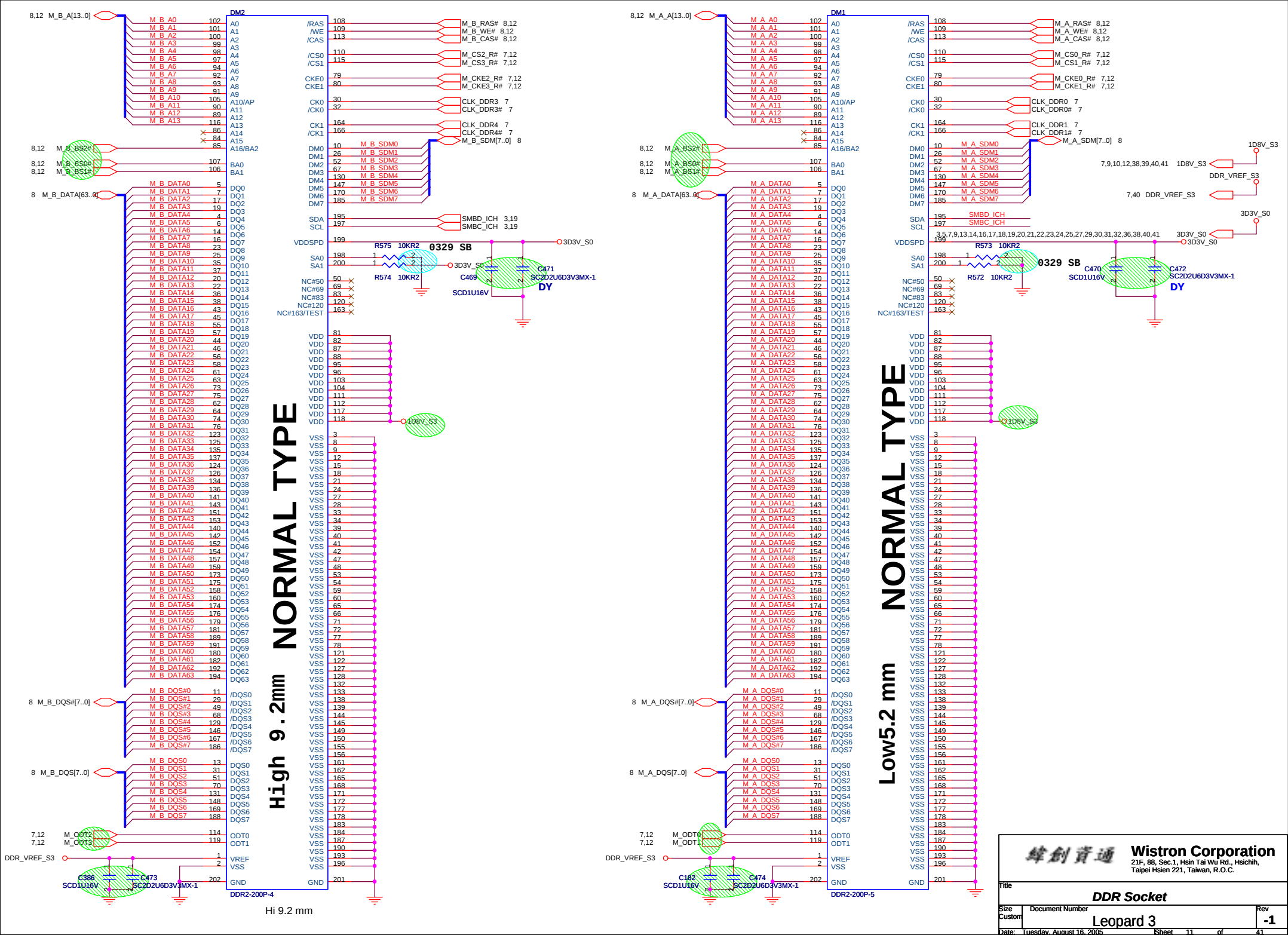
ALVISO-GM:71.0GMCH.08U
ALVISO-PM:71.0GMCH.0BU
ALVISO-GML:71.0GMCH.0JU

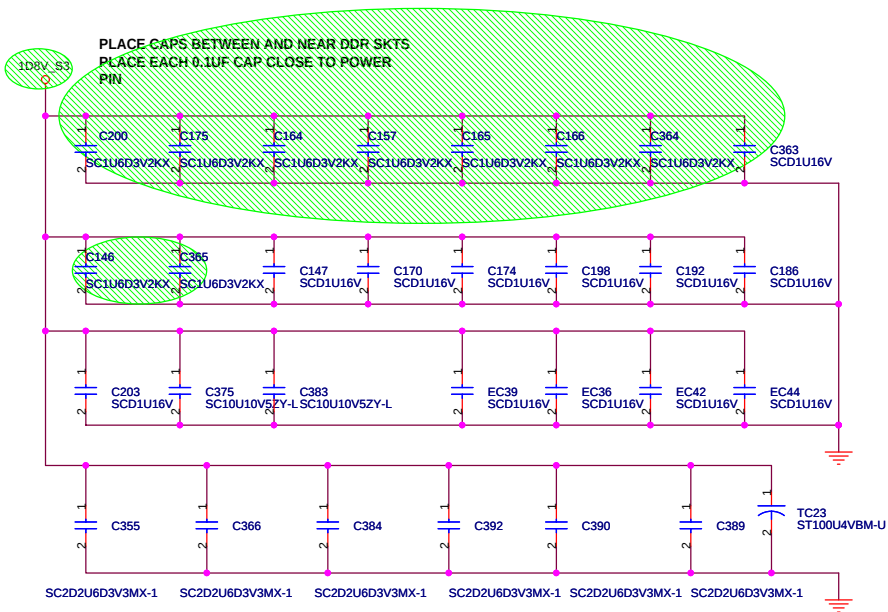




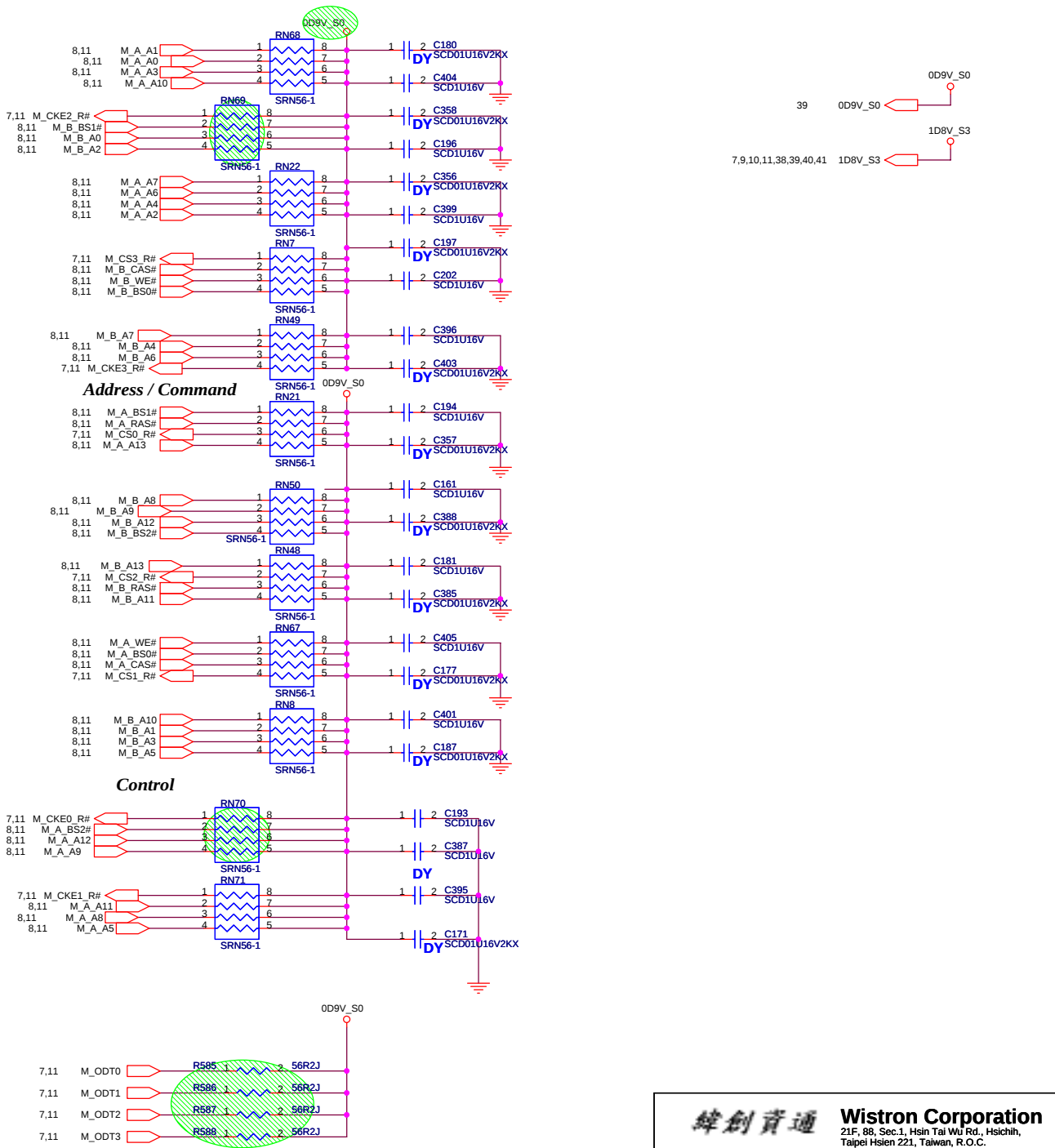
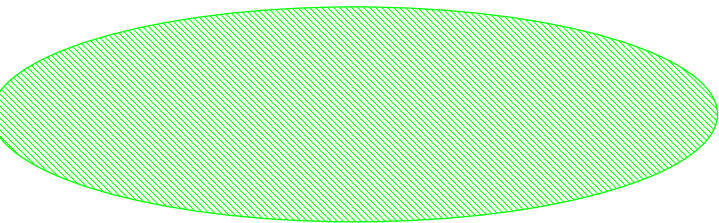




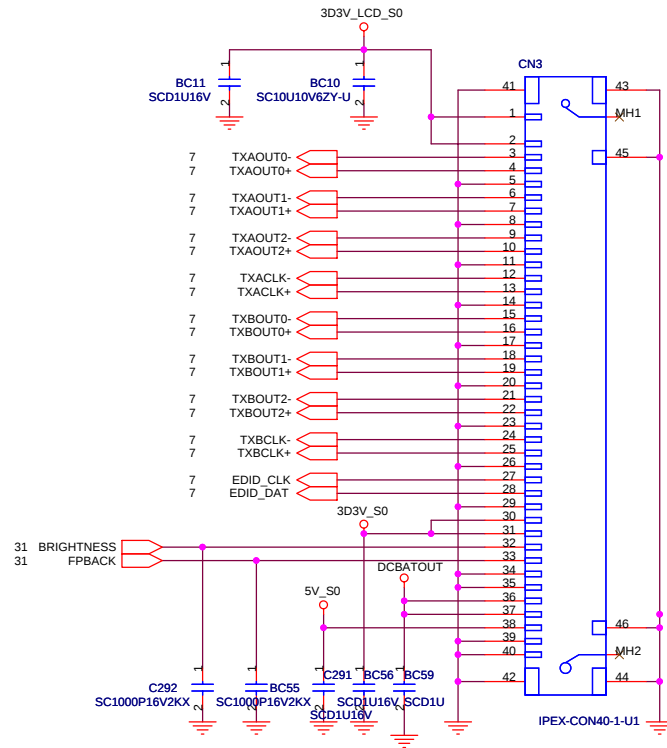




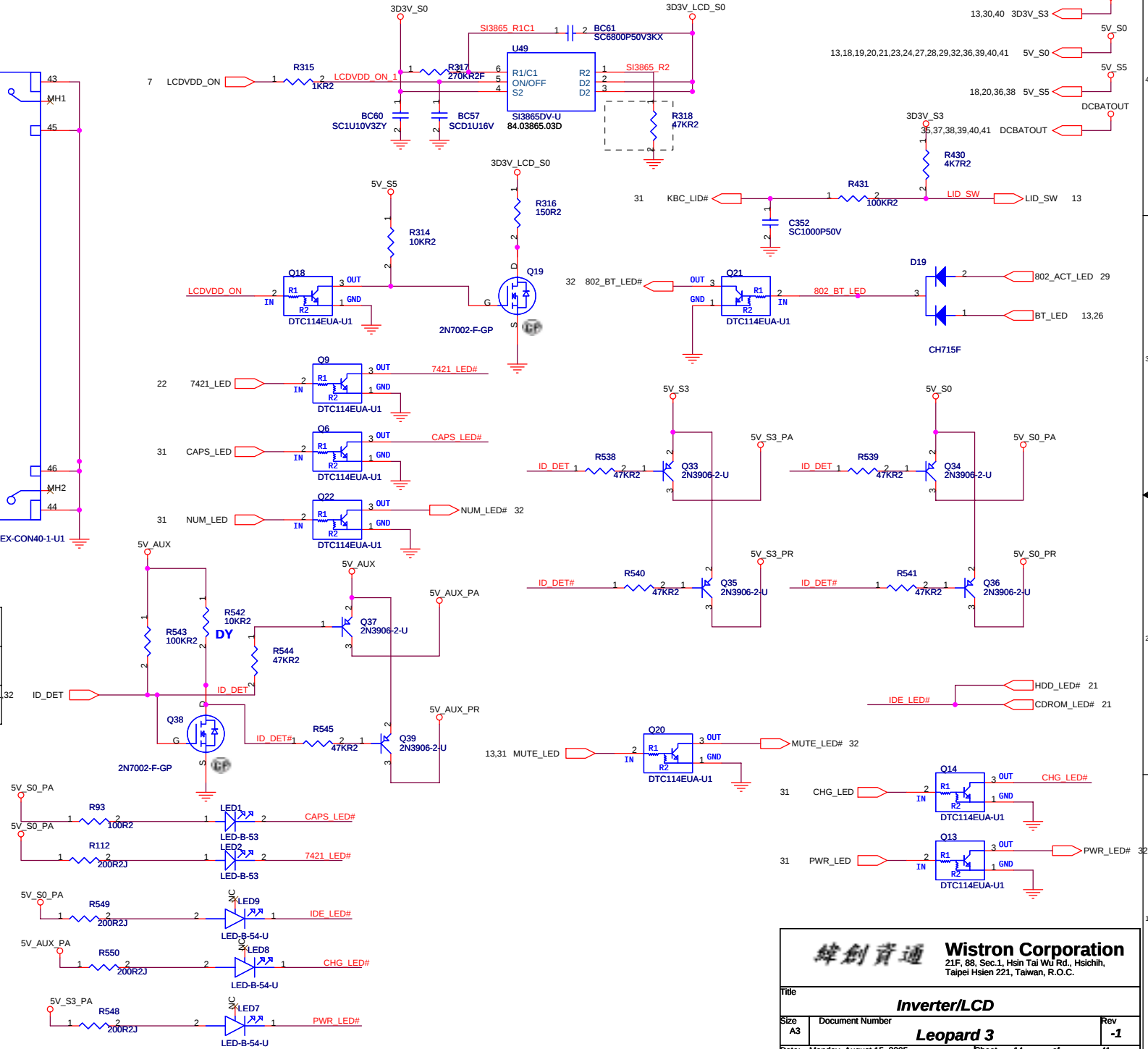
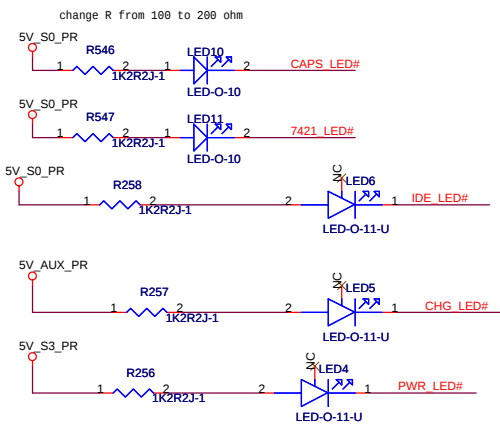
For 1GB Memory



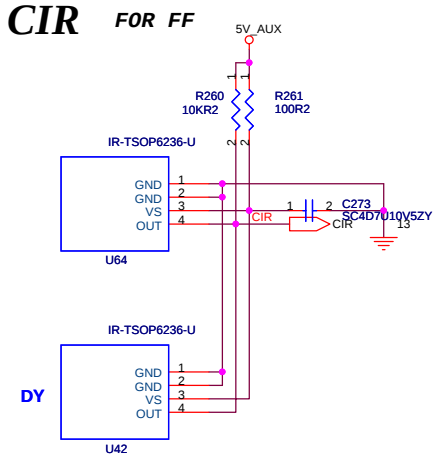
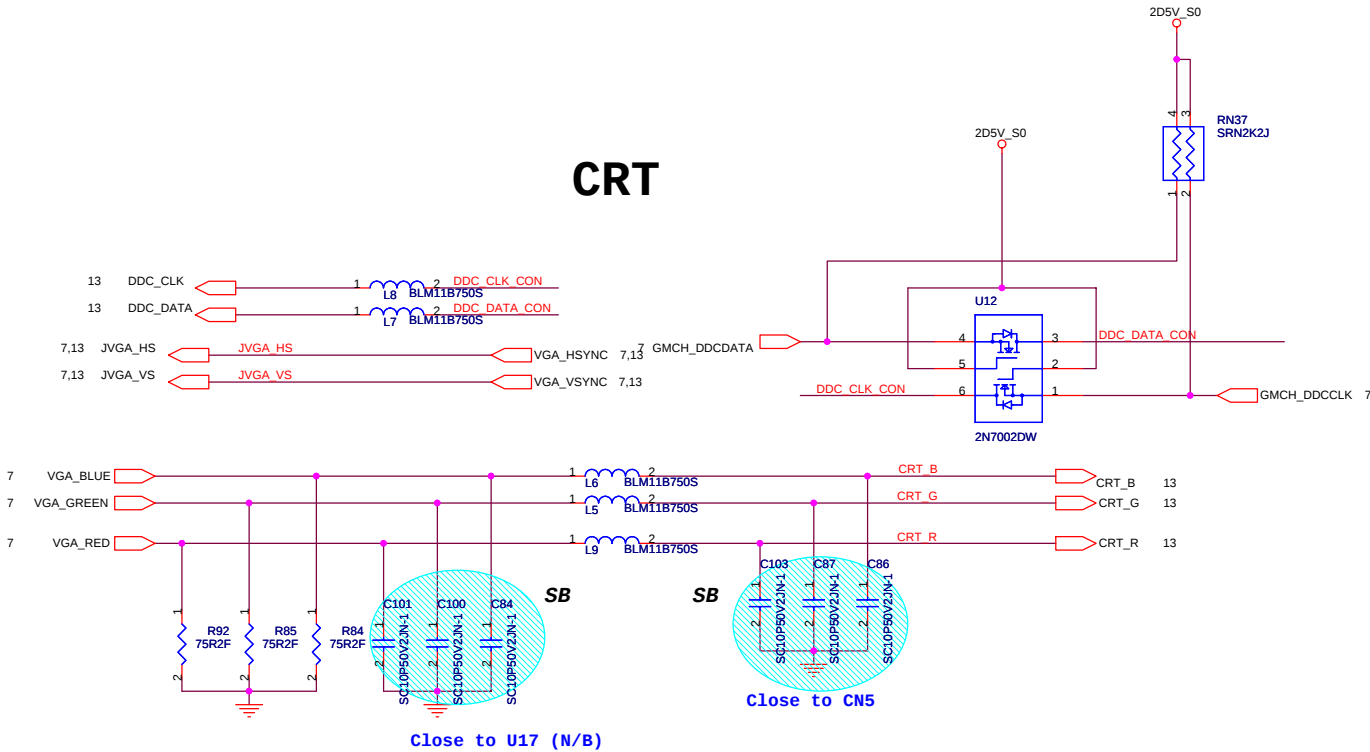
INVERTER/LCD

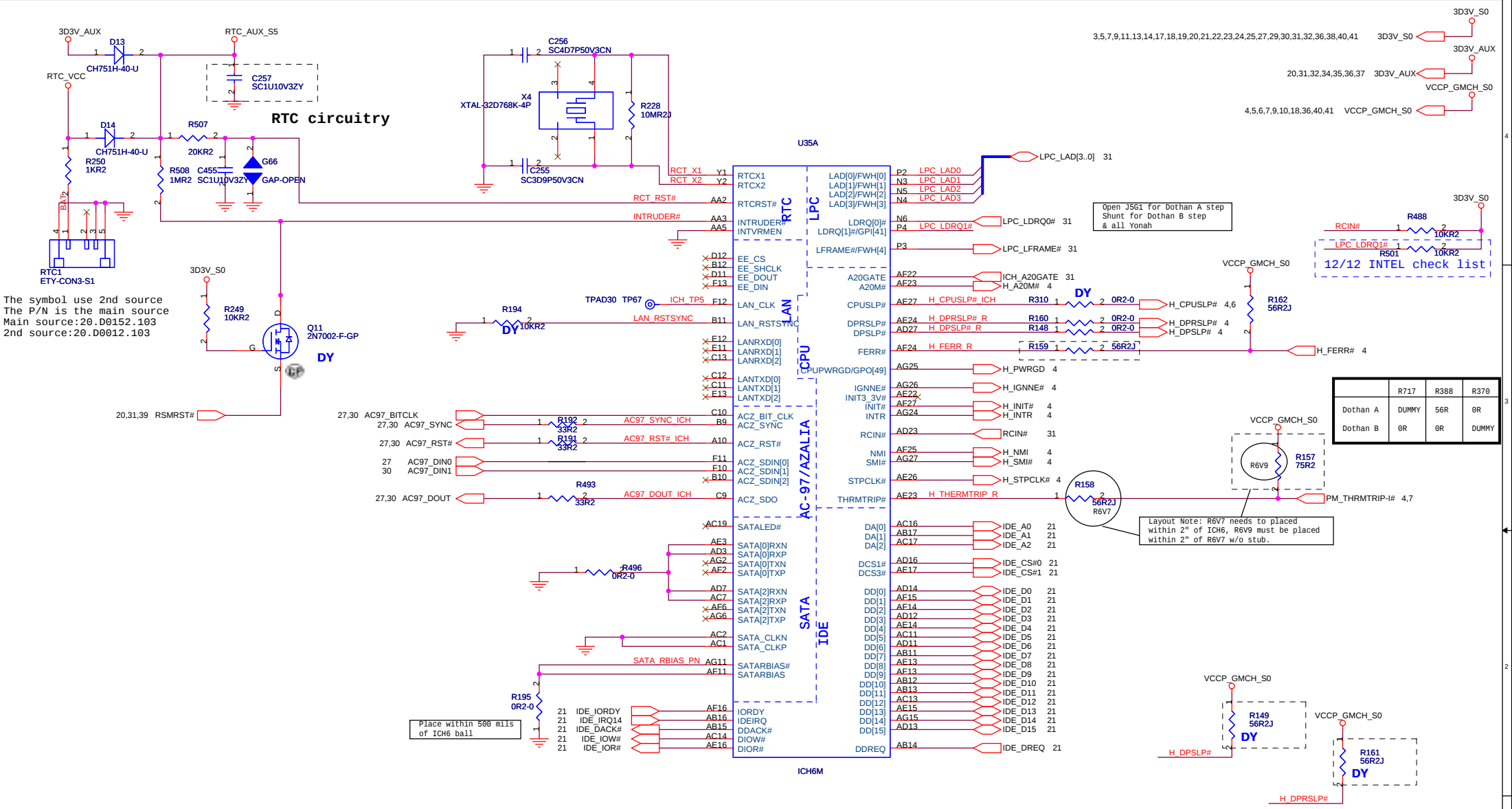


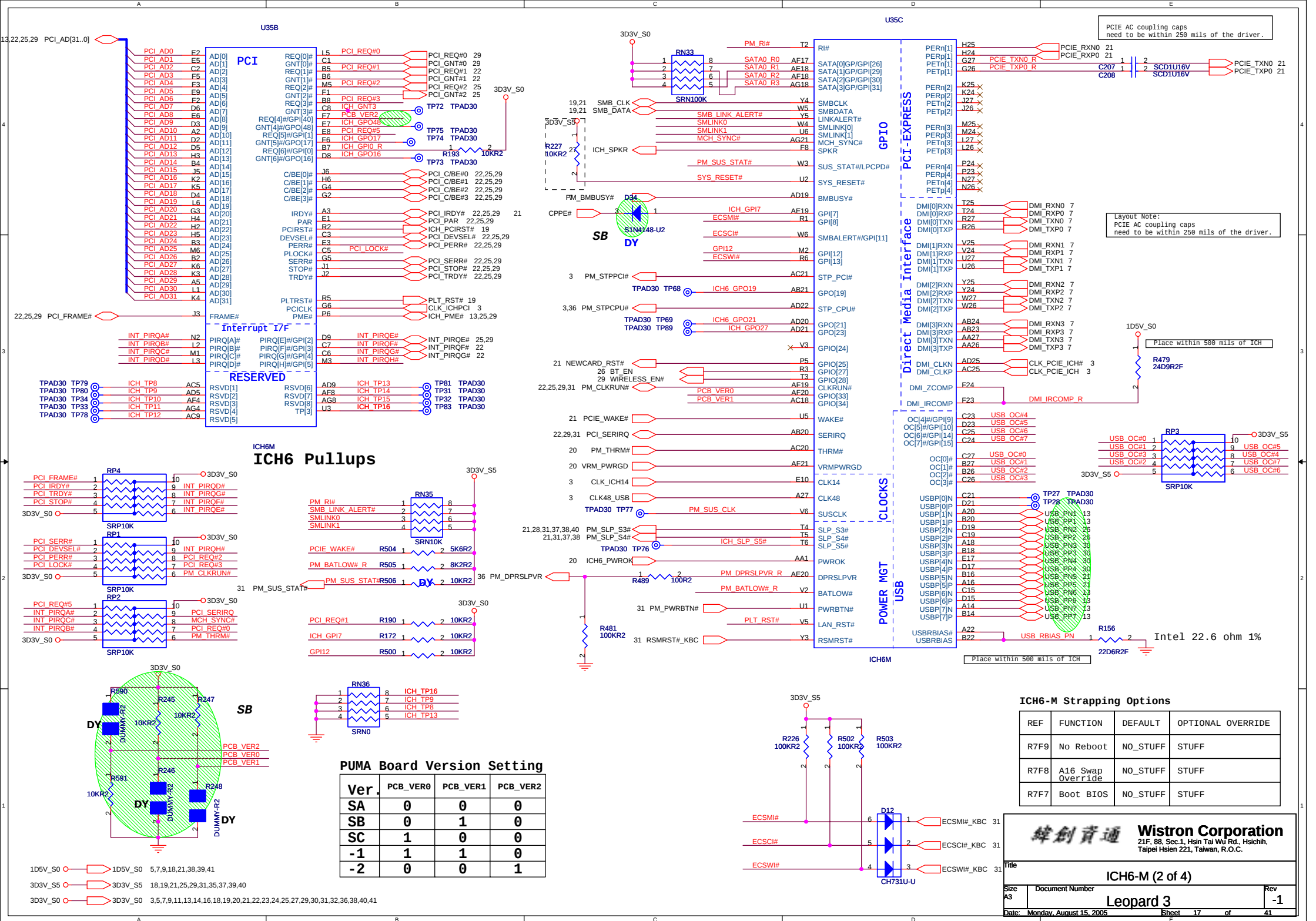
		PWR	CHR	HDD	IR	CAPS	7421
PR Botton		Amber LED4	Amber LED5	Amber LED6	U42	Amber LED1	Amber LED2
PA Top		Blue LED8	Blue LED7	Blue LED9	U64	Blue LED1	Blue LED2



PA & PR diffent parts		
	PA	PR
LED1	83.00190.Y70	83.00190.W70
LED2	83.00190.Y70	83.00190.W70
LED4	Dummy	83.00110.D70
LED5	Dummy	83.00110.D70
LED6	Dummy	83.00110.D70
LED7	83.00110.E70	Dummy
LED8	83.00110.E70	Dummy
LED9	83.00110.E70	Dummy
U64	56.15006.001	Dummy
U42	Dummy	56.15006.001
R256	63.20134.1D1	63.12234.1D1
R257	63.20134.1D1	63.12234.1D1
R258	63.20134.1D1	63.12234.1D1
R93	63.20134.1D1	63.12234.1D1
R112	63.20134.1D1	63.12234.1D1
CBUS1	21.H0088.001	21.H0088.001
R176	63.10334.1D1	Dummy
R177	Dummy	63.10334.1D1







Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27

Layout Note:
IDE decoupling

Layout Note:
PCI decoupling

Place within 100
mils of ICH
near pin AG5

Place within 100
mils of ICH
near pin AG9

Place within 100
mils of ICH

Place within 100
mils of ICH
near E26, E27

Place within 100
mils of ICH
pin AG10

Intel dummy

Place within 100
mils of ICH
pin A13

Place within 100
mils of ICH
pin V7

U35E

PCIE
VCC1_5_B
AA22 VCC1_5_B
AA23 VCC1_5_B
AA24 VCC1_5_B
AA25 VCC1_5_B
AB25 VCC1_5_B
AB26 VCC1_5_B
AB27 VCC1_5_B
F25 VCC1_5_B
F26 VCC1_5_B
F27 VCC1_5_B
G22 VCC1_5_B
G23 VCC1_5_B
G24 VCC1_5_B
G25 VCC1_5_B
H21 VCC1_5_B
H22 VCC1_5_B
J21 VCC1_5_B
J22 VCC1_5_B
K21 VCC1_5_B
K22 VCC1_5_B
L21 VCC1_5_B
L22 VCC1_5_B
M21 VCC1_5_B
M22 VCC1_5_B
N21 VCC1_5_B
N22 VCC1_5_B
N23 VCC1_5_B
N24 VCC1_5_B
N25 VCC1_5_B
P21 VCC1_5_B
P26 VCC1_5_B
P27 VCC1_5_B
R21 VCC1_5_B
R22 VCC1_5_B
T21 VCC1_5_B
T22 VCC1_5_B
U21 VCC1_5_B
U22 VCC1_5_B
V21 VCC1_5_B
V22 VCC1_5_B
W21 VCC1_5_B
W22 VCC1_5_B
Y21 VCC1_5_B
Y22 VCC1_5_B

SATA
VCC1_5_A
AA6 VCC1_5_A
AB4 VCC1_5_A
AB5 VCC1_5_A
AB6 VCC1_5_A
AC4 VCC1_5_A
AD4 VCC1_5_A
AE4 VCC1_5_A
AE5 VCC1_5_A
AG5 VCC1_5_A
AA7 VCC1_5_A
AA8 VCC1_5_A
AA9 VCC1_5_A
AB8 VCC1_5_A
AC8 VCC1_5_A
AD8 VCC1_5_A
AE8 VCC1_5_A
AE9 VCC1_5_A
AG9 VCC1_5_A

ICH6M
VCCSUS3_3
A11 VCCSUS3_3
U4 VCCSUS3_3
V1 VCCSUS3_3
V7 VCCSUS3_3
V2 VCCSUS3_3
Y7 VCCSUS3_3
A17 VCCSUS3_3
B17 VCCSUS3_3
C17 VCCSUS3_3
F18 VCCSUS3_3
G17 VCCSUS3_3
G18 VCCSUS3_3

ICH6M
VCCSUS3_3
A11 VCCSUS3_3
U4 VCCSUS3_3
V1 VCCSUS3_3
V7 VCCSUS3_3
V2 VCCSUS3_3
Y7 VCCSUS3_3
A17 VCCSUS3_3
B17 VCCSUS3_3
C17 VCCSUS3_3
F18 VCCSUS3_3
G17 VCCSUS3_3
G18 VCCSUS3_3

CORE
VCC1_5_A
F9 VCC1_5_A
U17 VCC1_5_A
U16 VCC1_5_A
U14 VCC1_5_A
U12 VCC1_5_A
U11 VCC1_5_A
T17 VCC1_5_A
T11 VCC1_5_A
P17 VCC1_5_A
P11 VCC1_5_A
M17 VCC1_5_A
M11 VCC1_5_A
L17 VCC1_5_A
L16 VCC1_5_A
L14 VCC1_5_A
L12 VCC1_5_A
L11 VCC1_5_A
AA21 VCC1_5_A
AA20 VCC1_5_A
AA19 VCC1_5_A

IDE
VCC3_3
AA10 VCC3_3
AG19 VCC3_3
AG16 VCC3_3
AG13 VCC3_3
AD17 VCC3_3
AC15 VCC3_3
AA17 VCC3_3
AA15 VCC3_3
AA14 VCC3_3
VCC3_3

PCI
VCC3_3
M7 VCC3_3
L7 VCC3_3
L4 VCC3_3
J7 VCC3_3
H7 VCC3_3
E4 VCC3_3
B1 VCC3_3
A6 VCC3_3

USB
VCCSUS1_5
VCCSUS1_5
G19 VCCSUS1_5
G20 VCC1_5_A
E20 VCC1_5_A
E24 VCC1_5_A
E23 VCC1_5_A
E22 VCC1_5_A
E21 VCC1_5_A
E20 VCC1_5_A
D27 VCC1_5_A
D26 VCC1_5_A
D25 VCC1_5_A
D24 VCC1_5_A

PCI/IDE
VCC2_5
VCC2_5
AB18 VCC2_5
P7 VCC2_5

ICH6M
VCCSUS3_3
A11 VCCSUS3_3
U4 VCCSUS3_3
V1 VCCSUS3_3
V7 VCCSUS3_3
V2 VCCSUS3_3
Y7 VCCSUS3_3
A17 VCCSUS3_3
B17 VCCSUS3_3
C17 VCCSUS3_3
F18 VCCSUS3_3
G17 VCCSUS3_3
G18 VCCSUS3_3

ICH6M
VCCSUS3_3
A11 VCCSUS3_3
U4 VCCSUS3_3
V1 VCCSUS3_3
V7 VCCSUS3_3
V2 VCCSUS3_3
Y7 VCCSUS3_3
A17 VCCSUS3_3
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F18 VCCSUS3_3
G17 VCCSUS3_3
G18 VCCSUS3_3

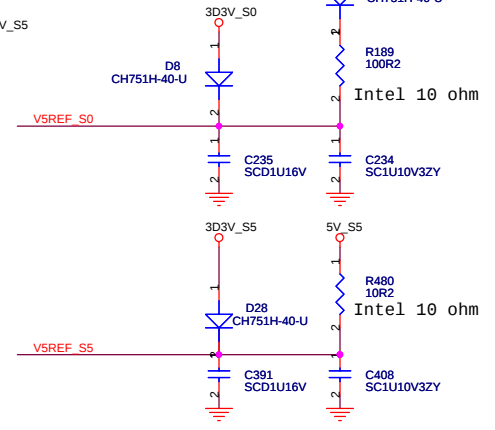
ICH6M
VCCSUS3_3
A11 VCCSUS3_3
U4 VCCSUS3_3
V1 VCCSUS3_3
V7 VCCSUS3_3
V2 VCCSUS3_3
Y7 VCCSUS3_3
A17 VCCSUS3_3
B17 VCCSUS3_3
C17 VCCSUS3_3
F18 VCCSUS3_3
G17 VCCSUS3_3
G18 VCCSUS3_3

1D5V_S0
3.5,7,9,11,13,14,16,17,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41
3D3V_S0
3D3V_S5
5V_S0
1D5V_S0
1D5V_S5
2D5V_S0
VCCP_GMCH_S0

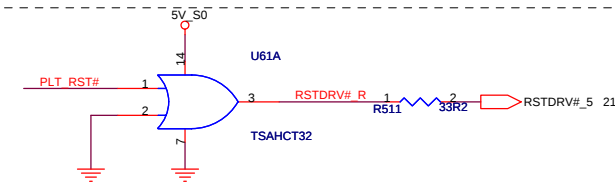
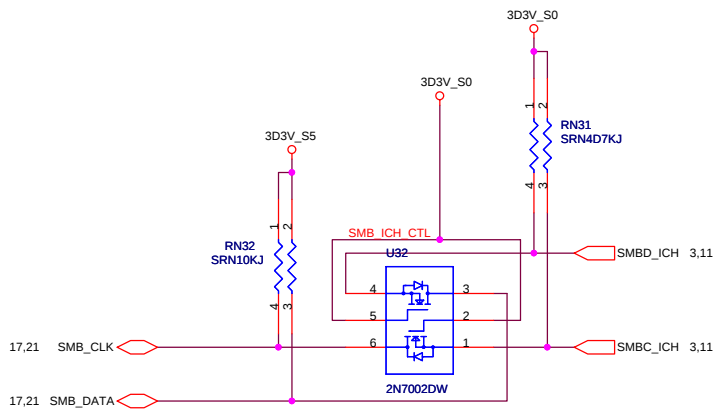
Layout Note:
Place near pin AA19

ALL NO_STUFF Caps do
not have layout
requirements but if
layout allows then place
next to ICH6

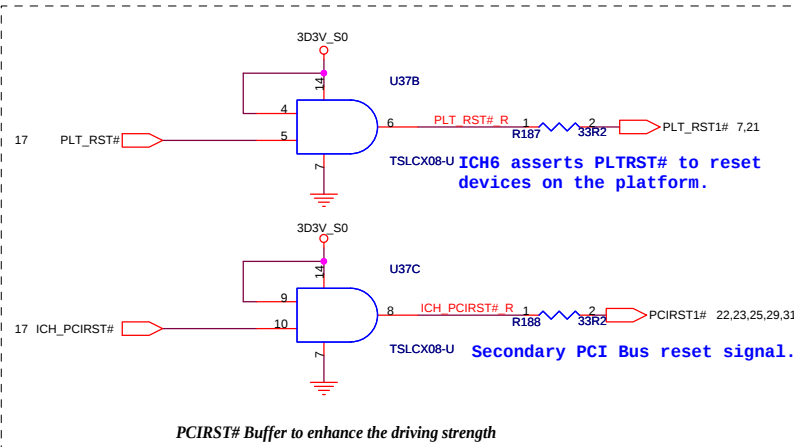
*Within a given well, 5VREF needs to be up before the
corresponding 3.3V rail



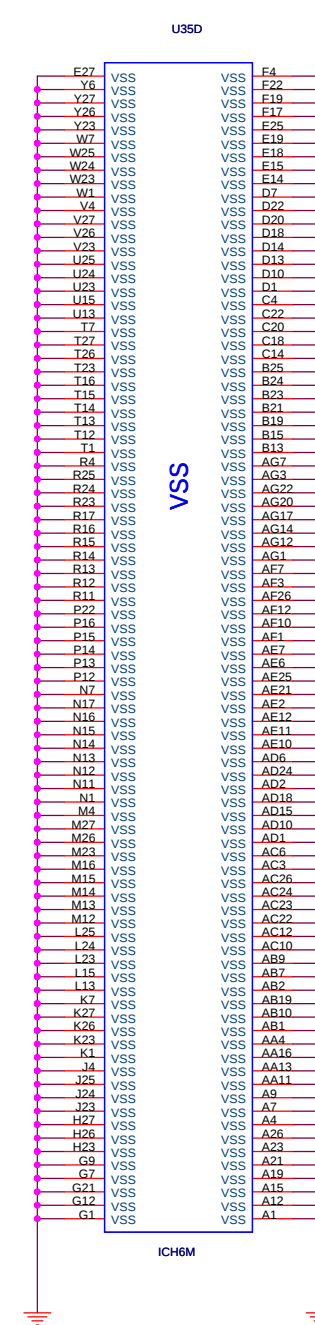
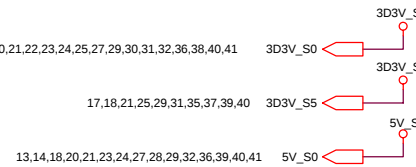
SMBUS(ICH6 ---> SODIMM,CLKGEN)

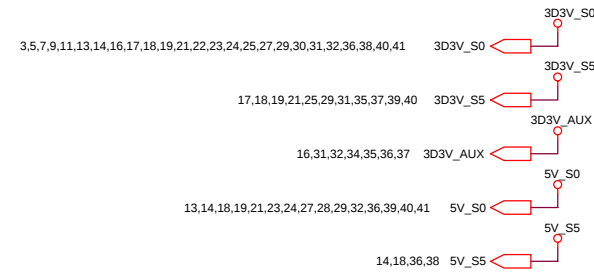
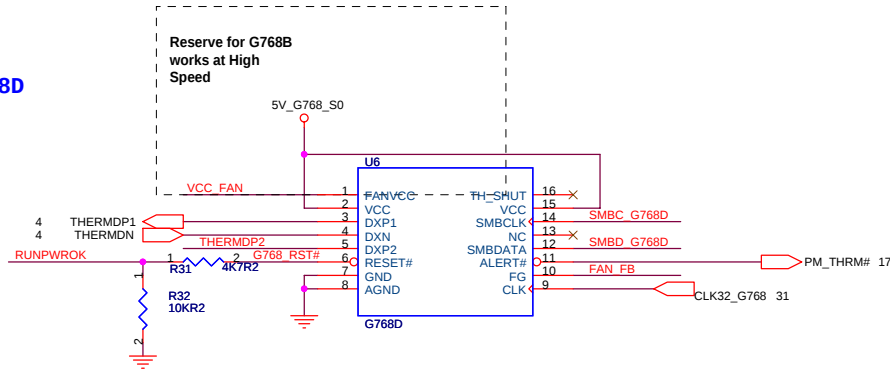
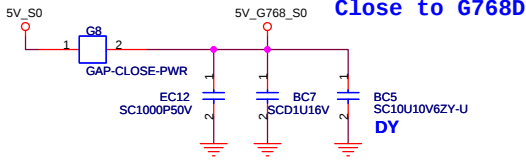


PCIRST# 3V to 5V level shift for HDD & CDROM

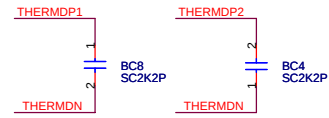
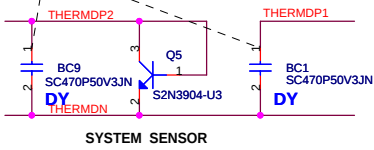


PCIRST# Buffer to enhance the driving strength



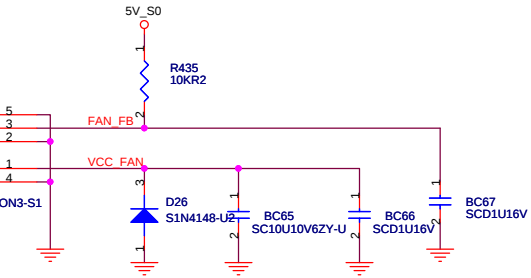


Put these two Caps near the thermal diode.

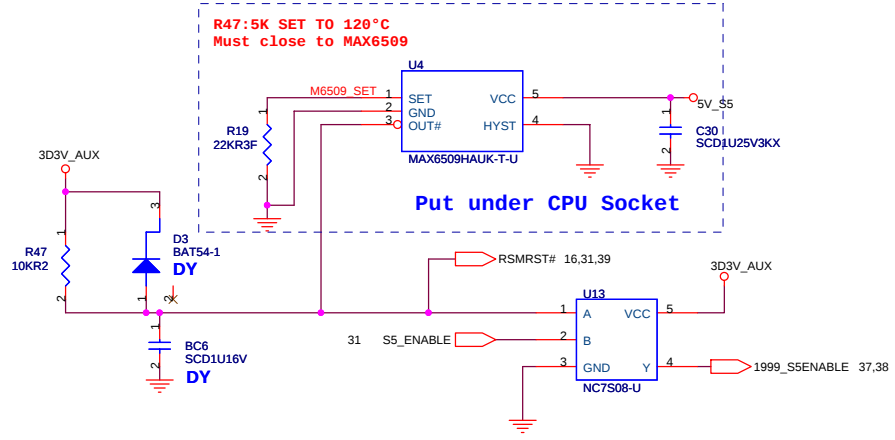
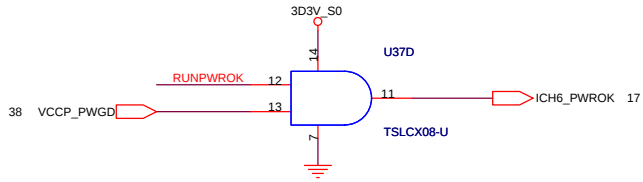
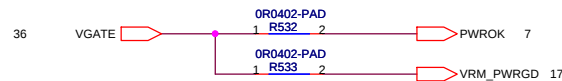
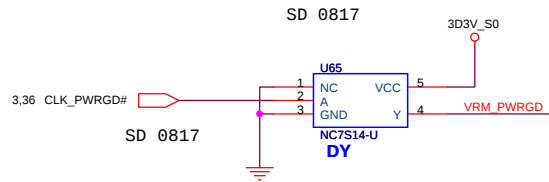


THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B

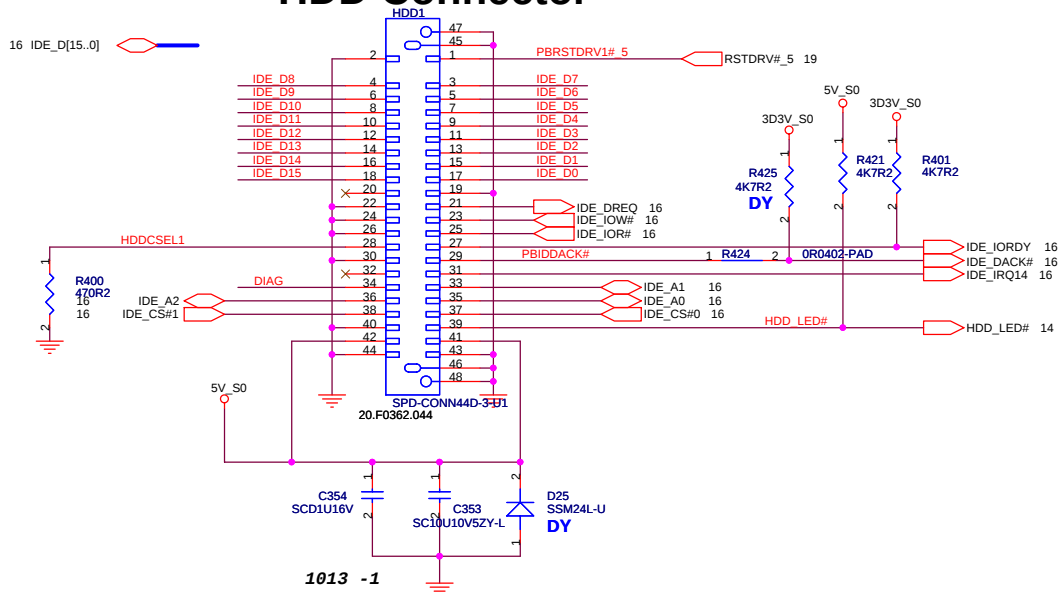
180 ms after VCC_G768 > 4.38v, p2, 7



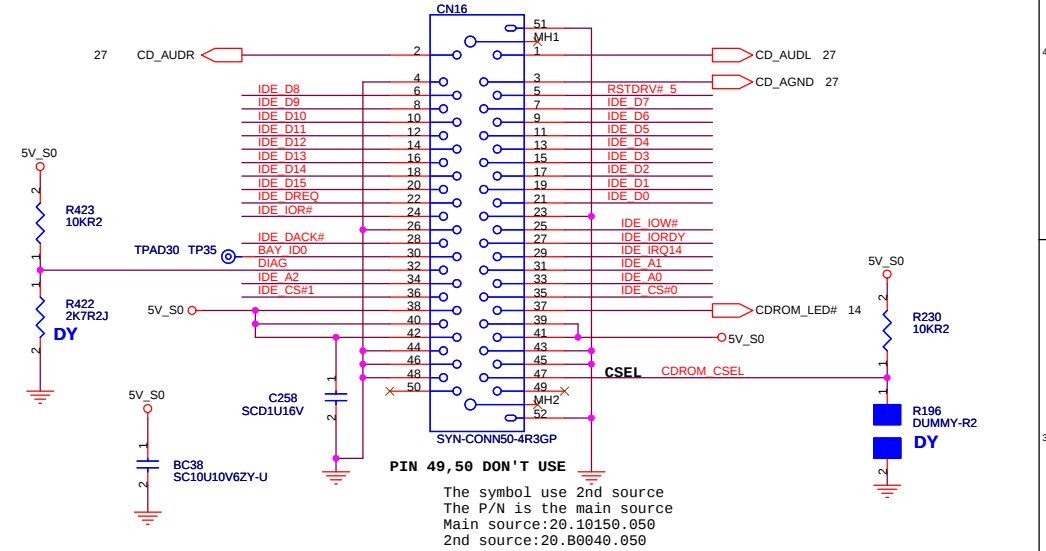
The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103



HDD Connector

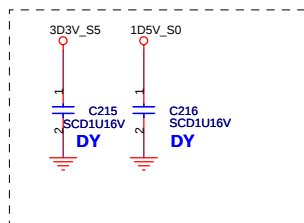


CDROM

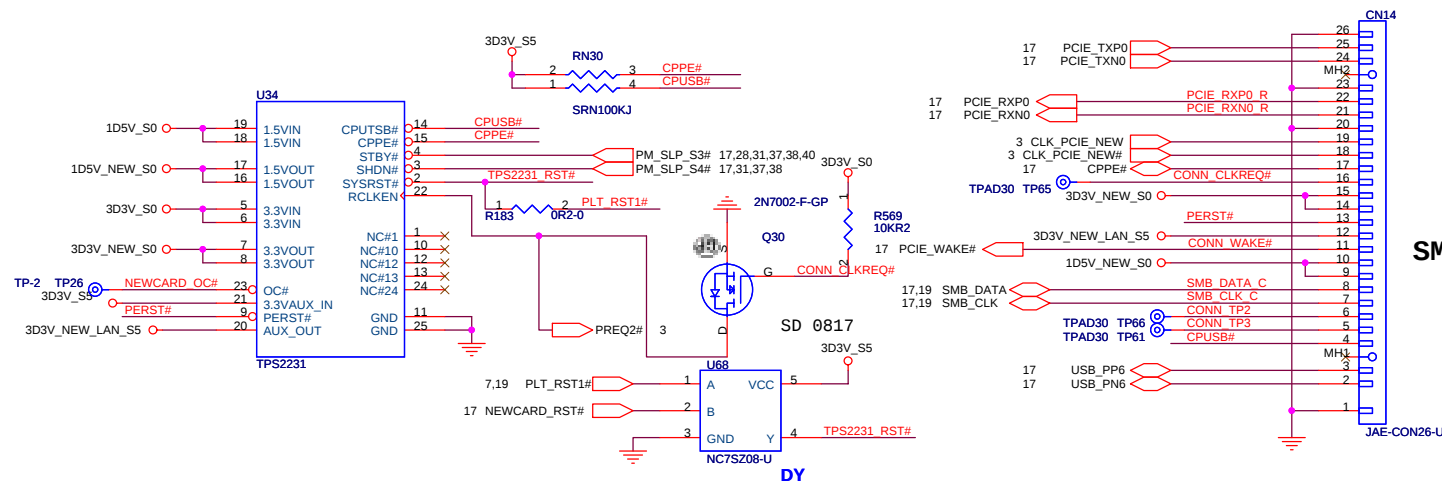
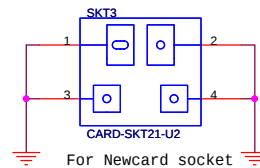
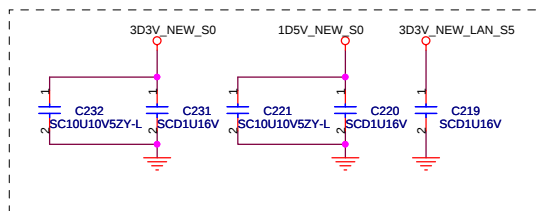


NEWCARD Connector

Place them Near to Chip

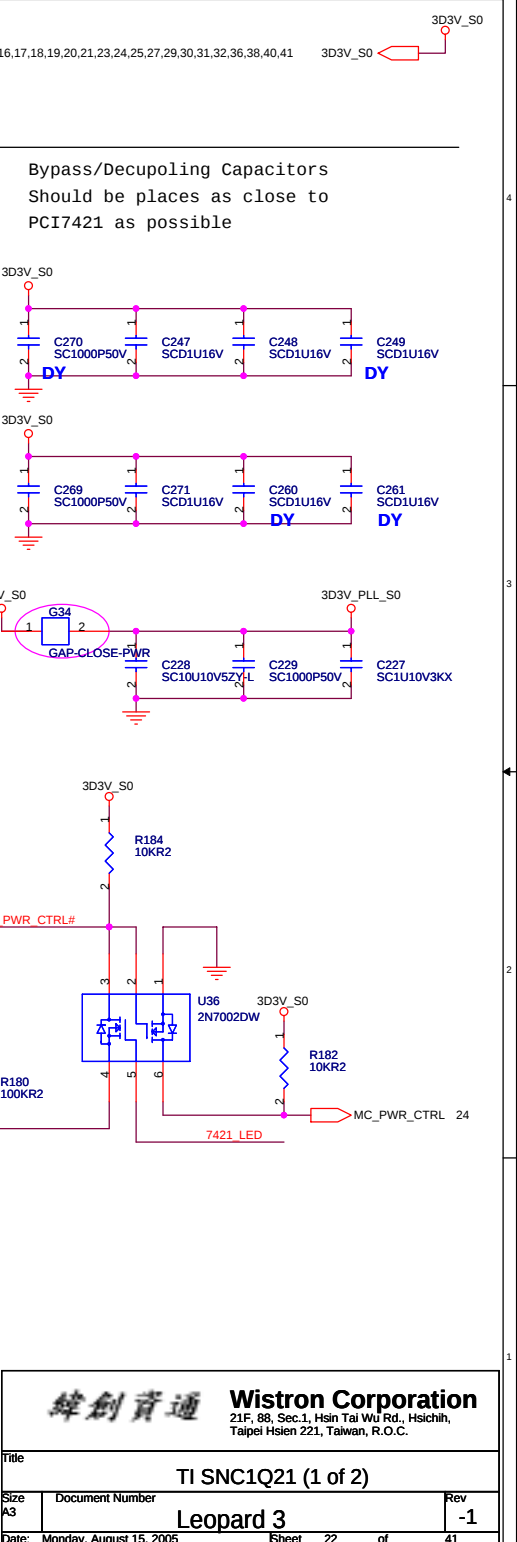
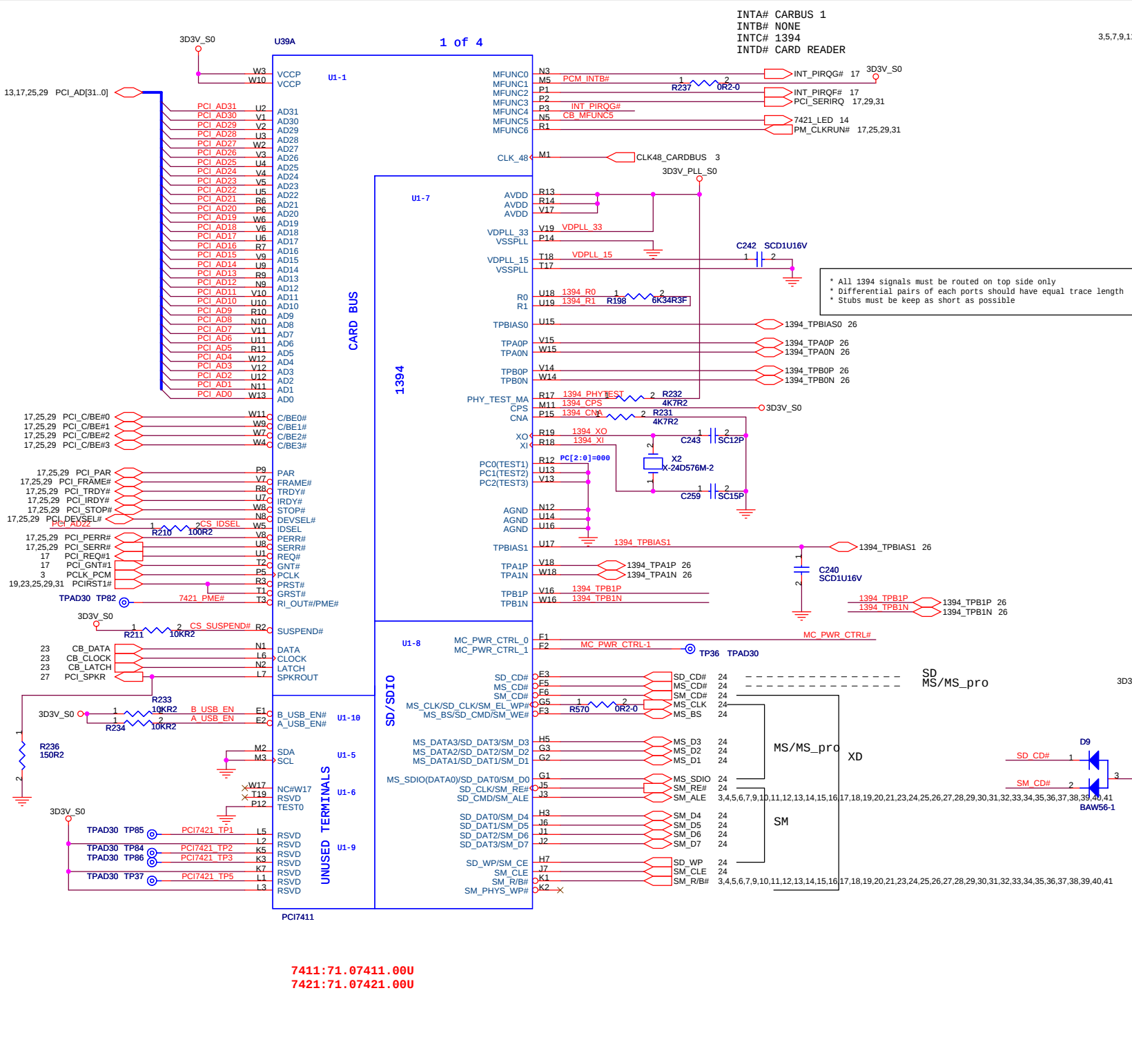


Place them Near to Connector

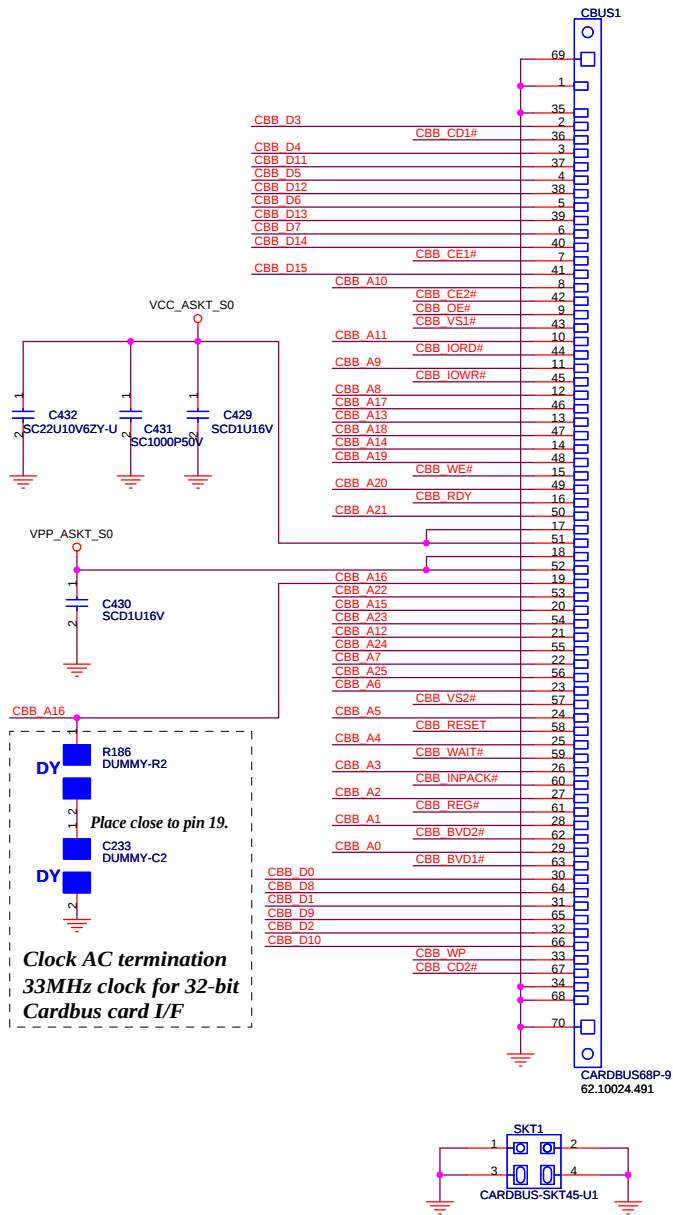


SMBUS (ICH6 - - NEWCARD, LAN)

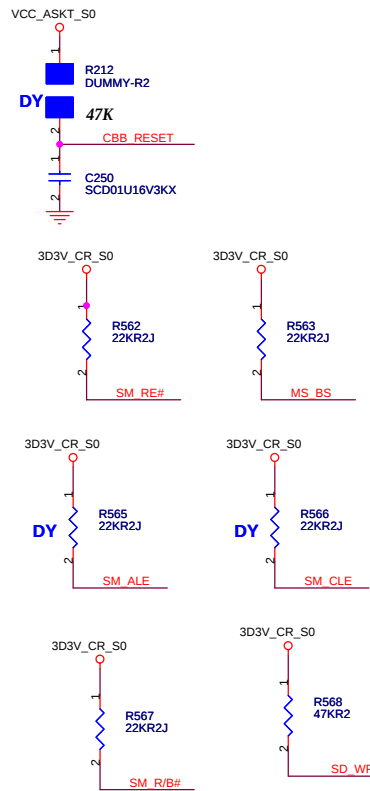
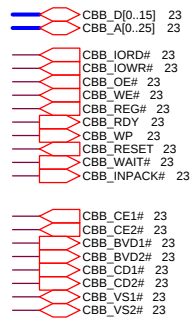




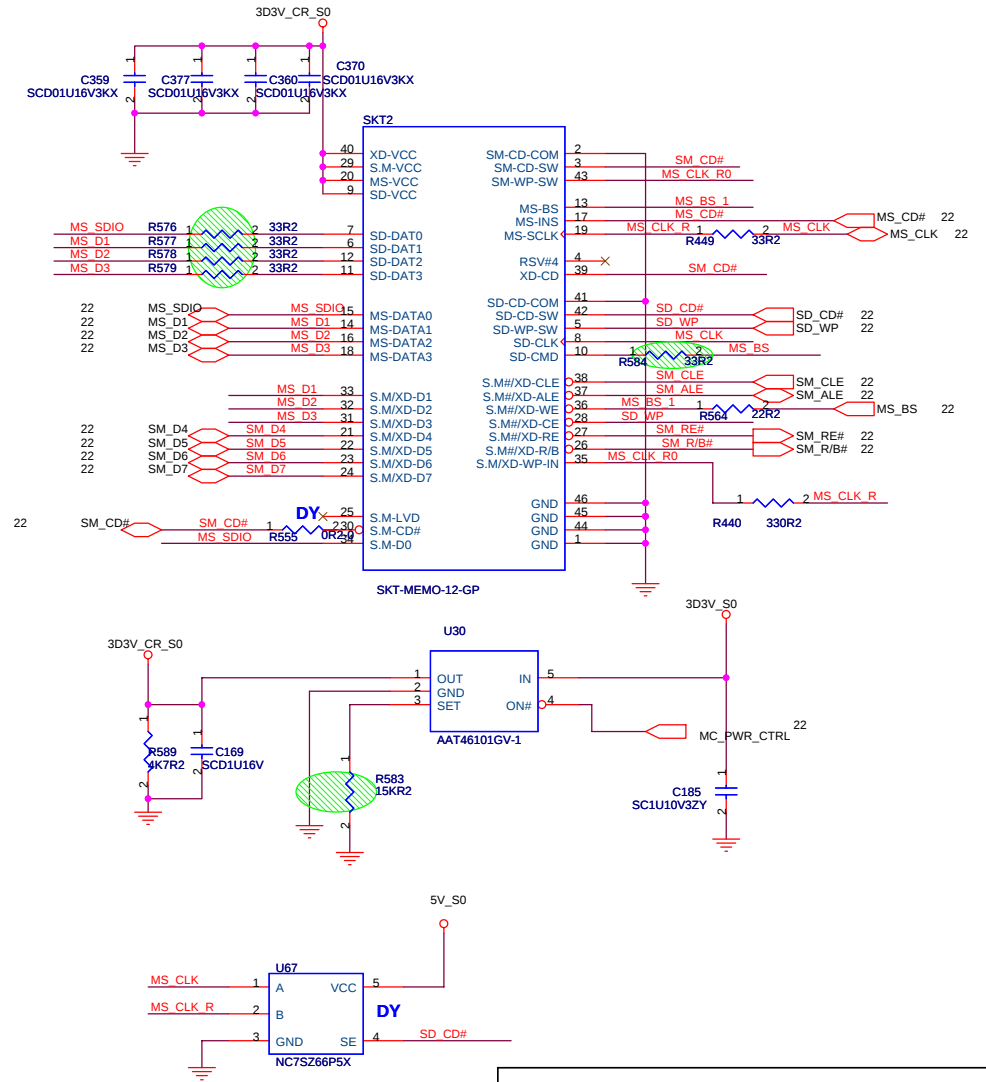
PCMCIA Socket



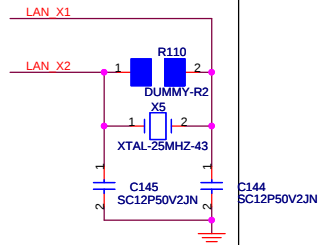
Cardbus I/F



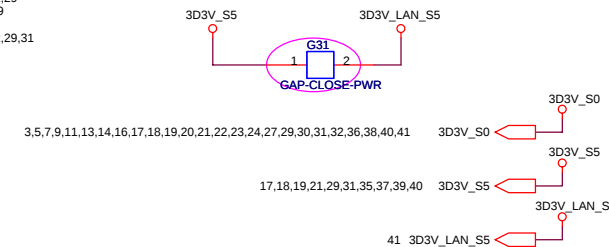
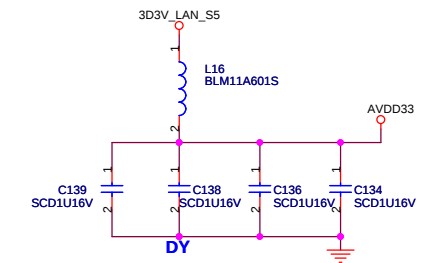
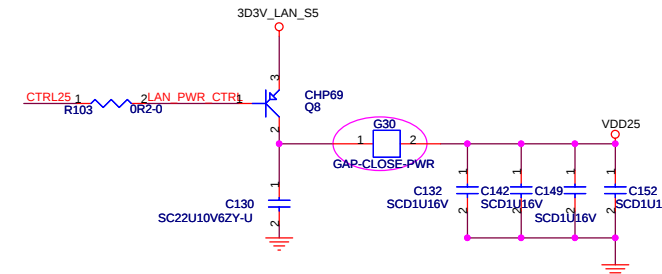
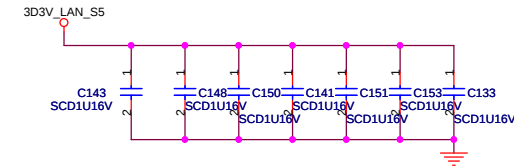
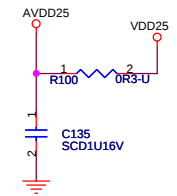
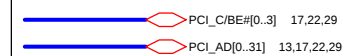
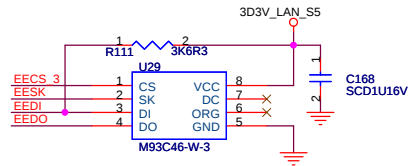
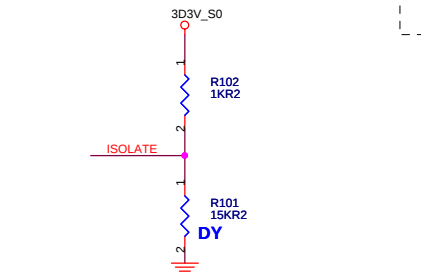
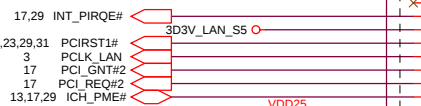
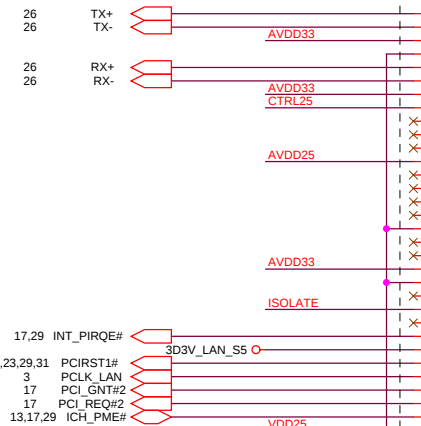
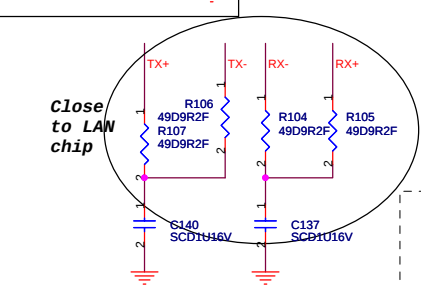
6 in 1 Connector



Close to RTL8100C
Pin121, Pin122

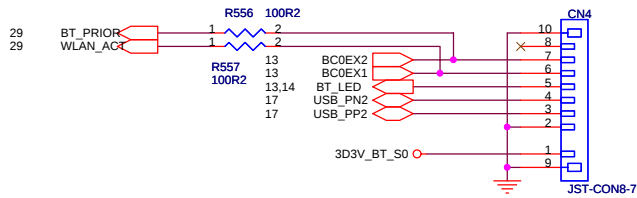


Close
to LAN
chip



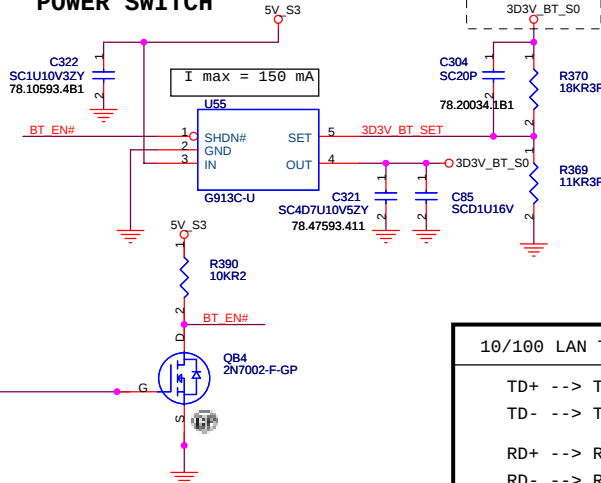
Blue thumb

Place on bottom side

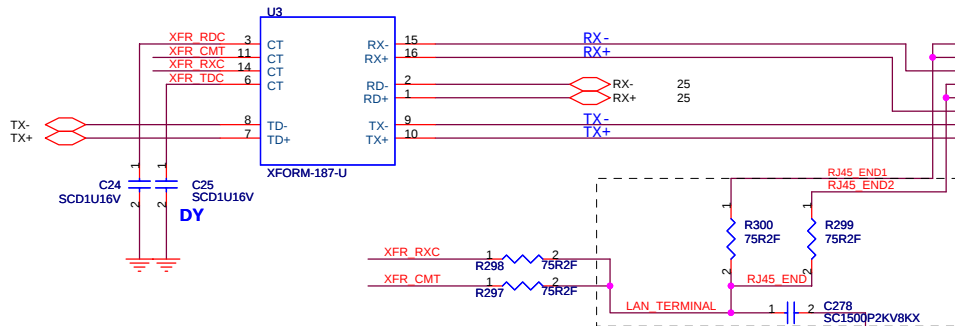


BC0EX2 connect to PCI_AD22 on main board.
BC0EX1 connect to ICH_PME# on main board.

POWER SWITCH

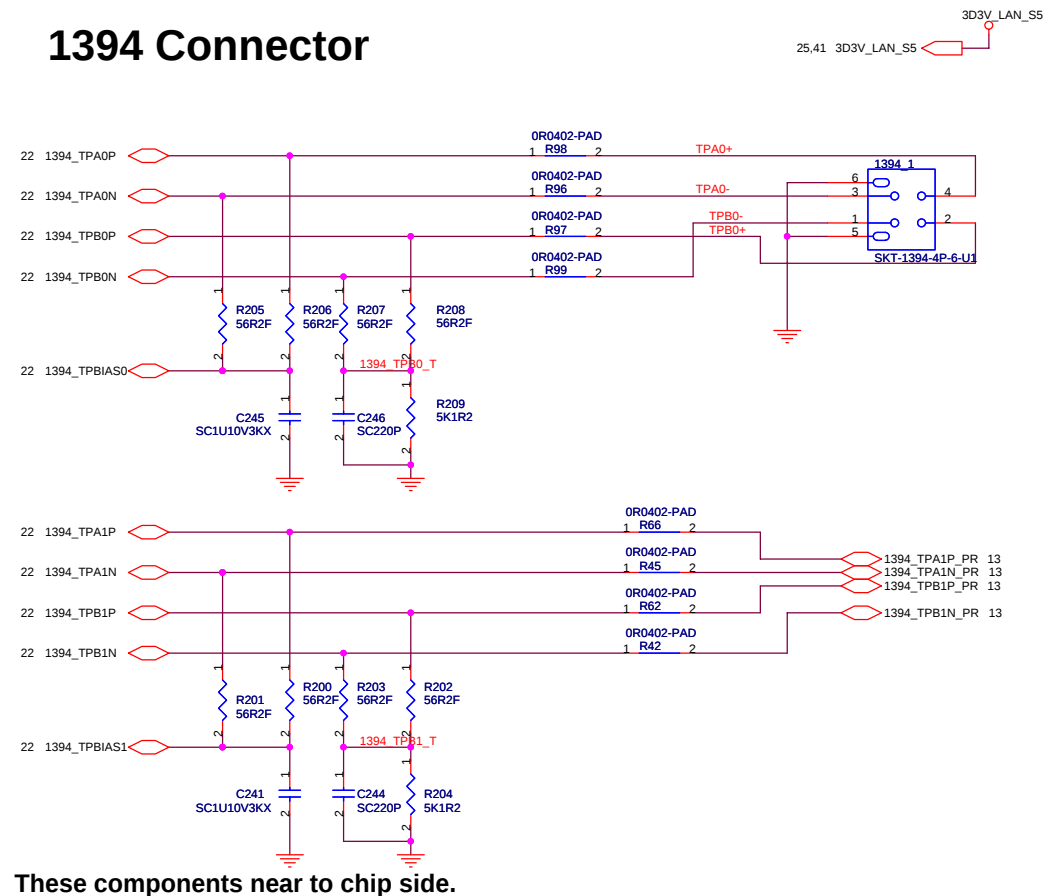


10/100M Lan Transformer



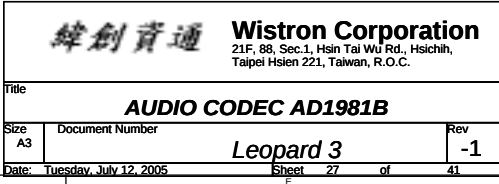
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

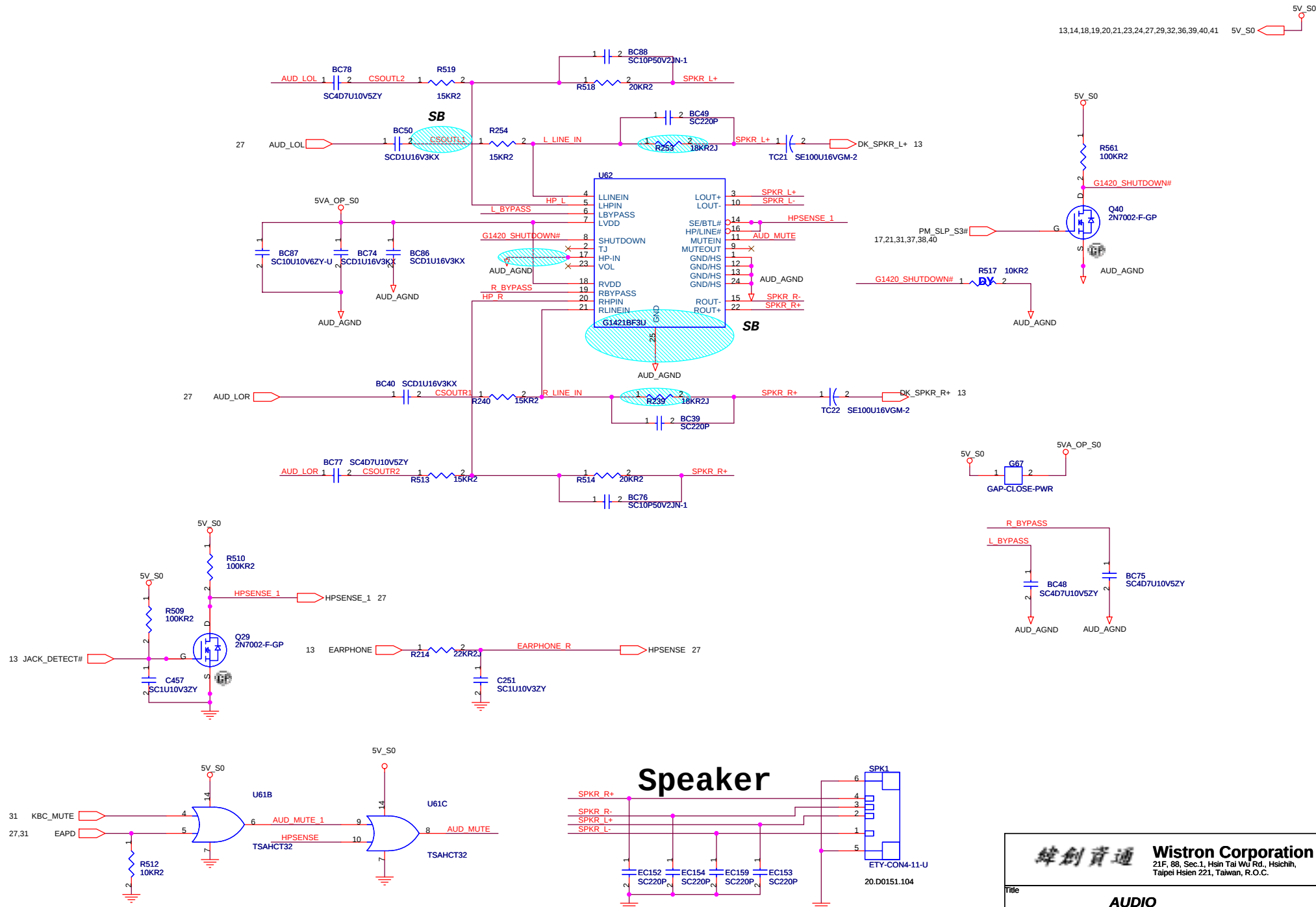
1394 Connector



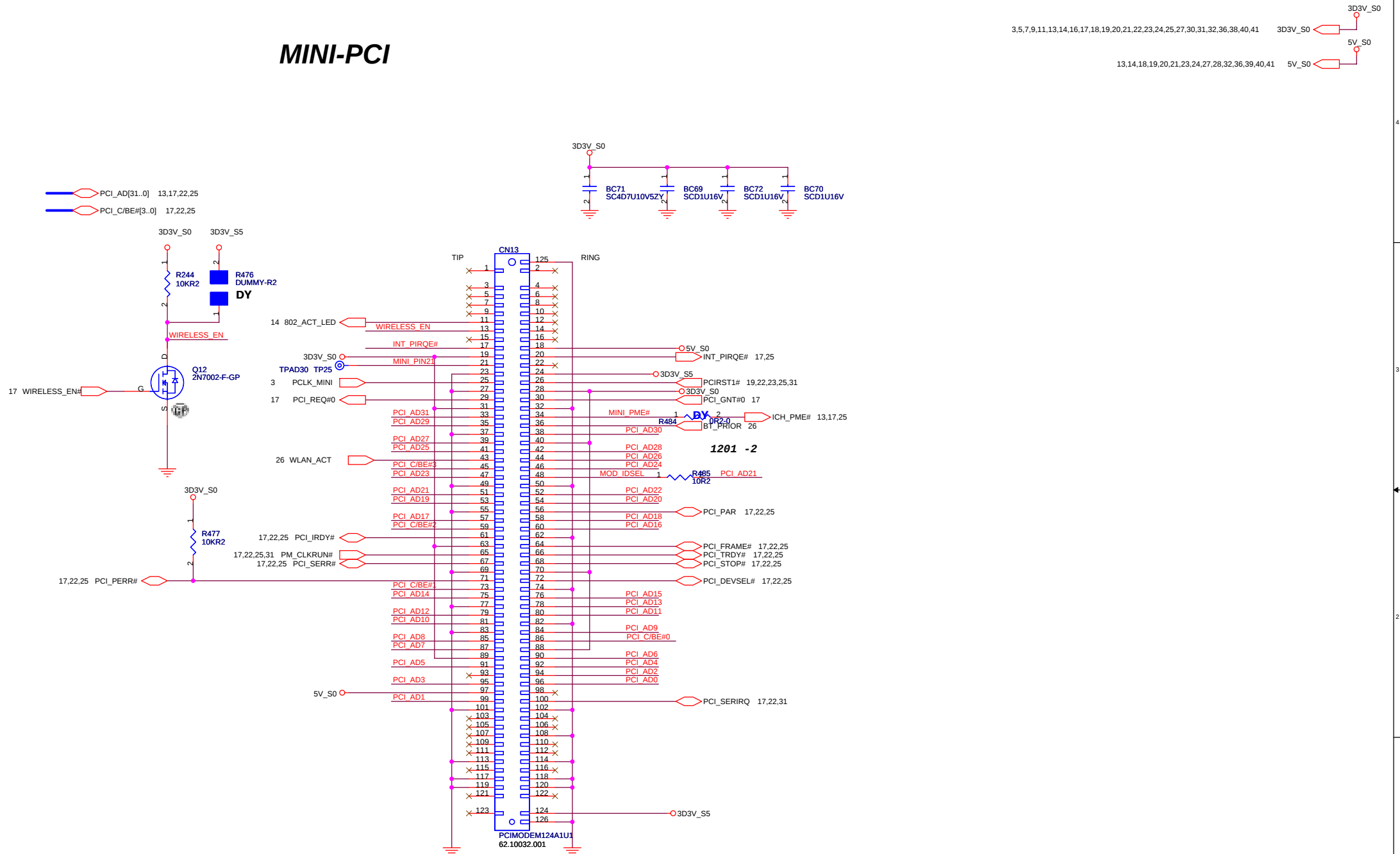
These components near to chip side.

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



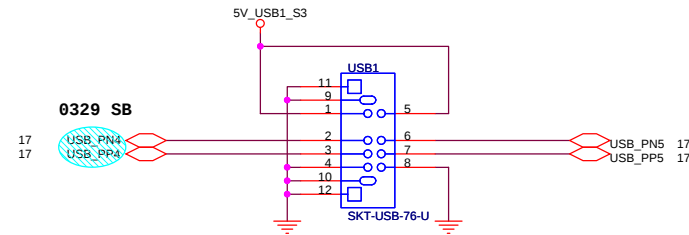
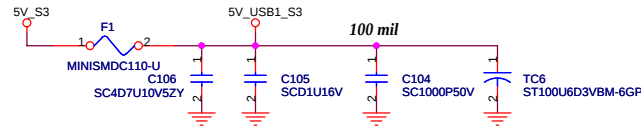


MINI-PCI

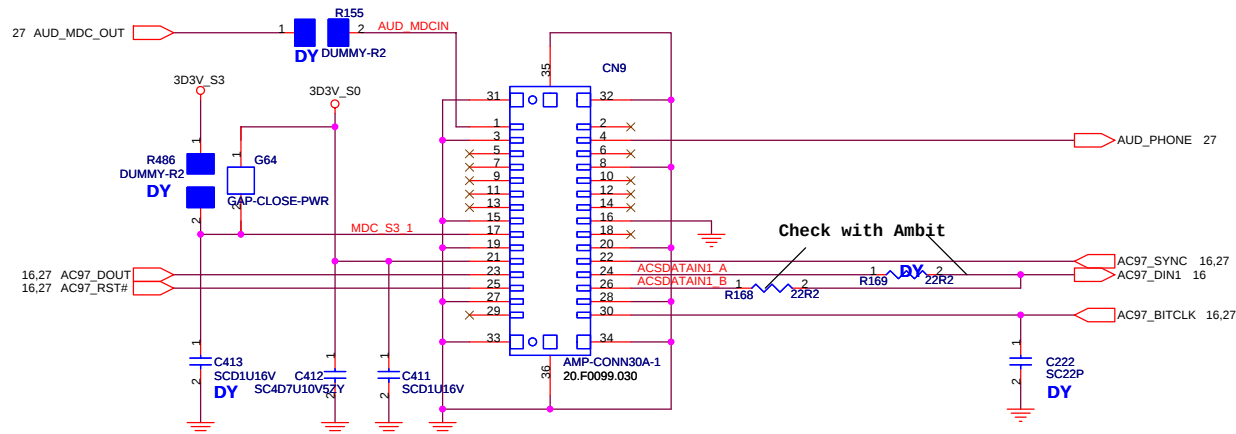


The symbol use 2nd source
The P/N is the main source
Main source:62.10032.001
2nd source:62.10032.031

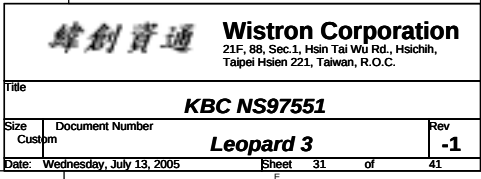
USB POWER



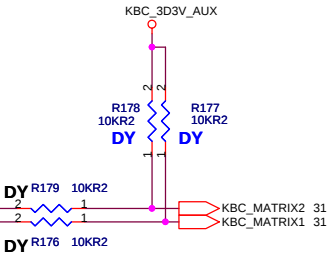
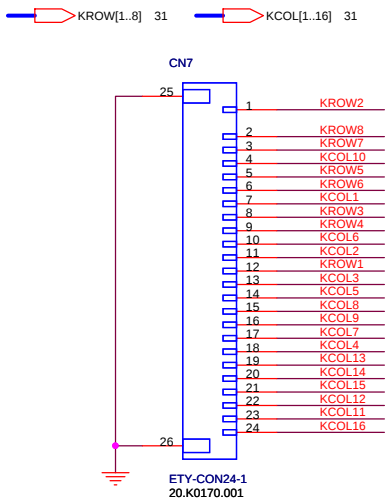
MDC Connector



 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
USB / MDC CONN.	
Size	Document Number
A3	
Date:	Rev
Tuesday, July 12, 2005	-1
Sheet 30 of 41	



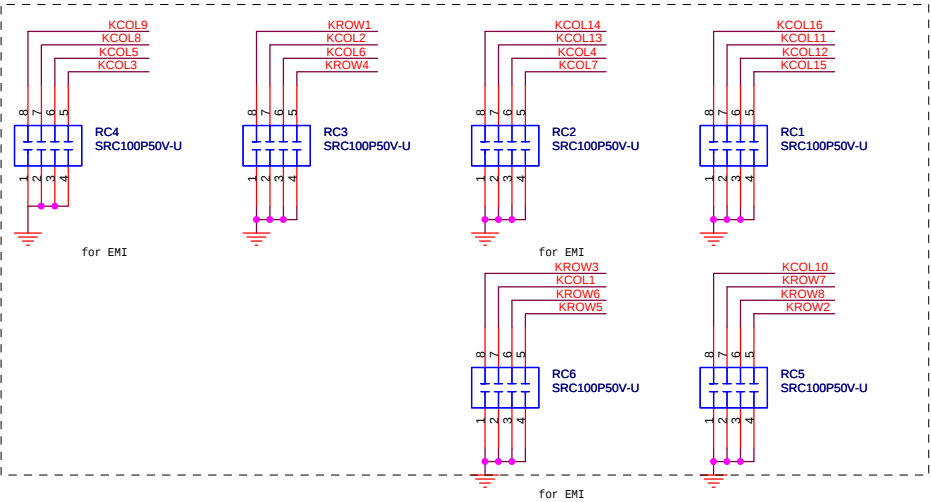
INTERNAL KEYBOARD CONNECTOR



the matrix table for PCB

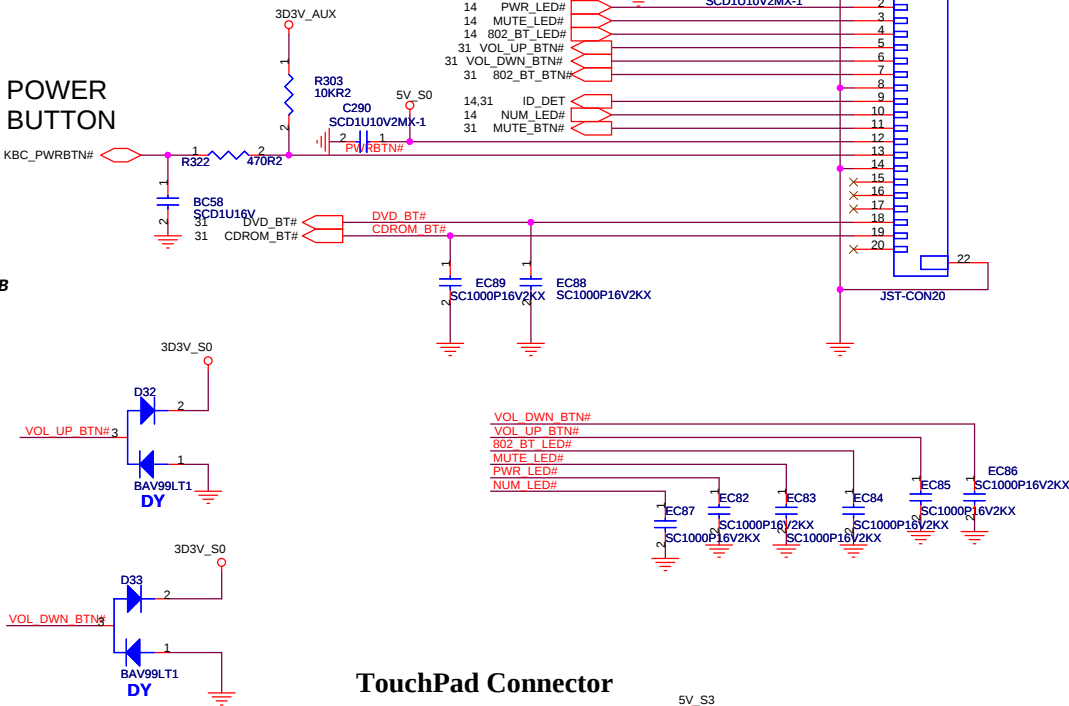
KBC_MATRIX2, KBC_MATRIX1		
PA	PR	
FF	00	01
DF	10	11

	NONE Quick Play	Quick Play
MATRIXID1#	0	1

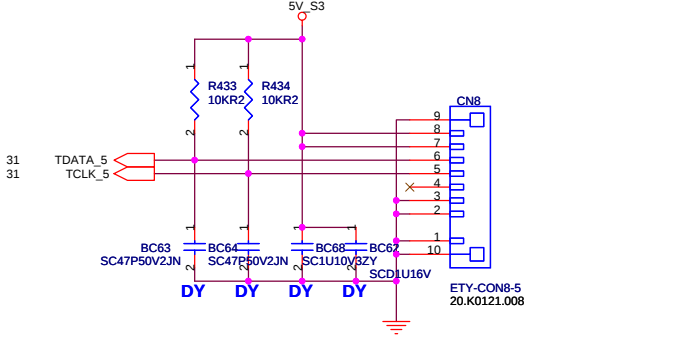


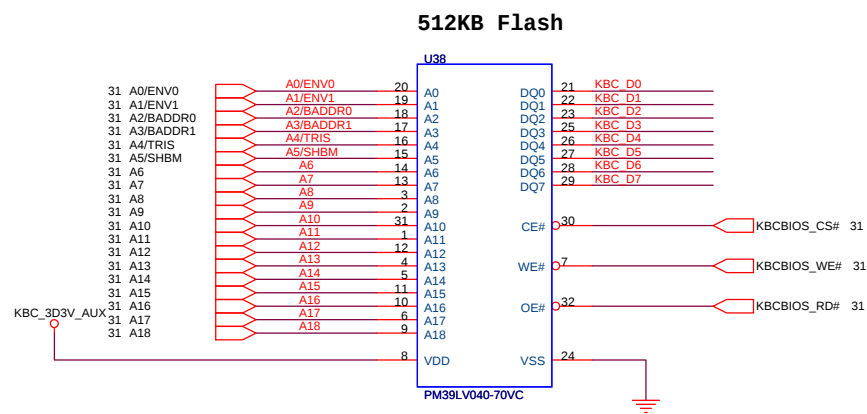
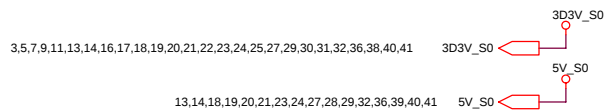
LAUNCH Board

POWER BUTTON



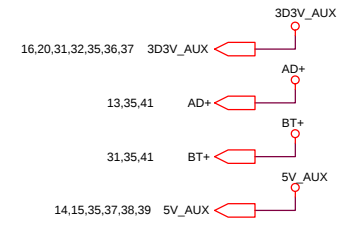
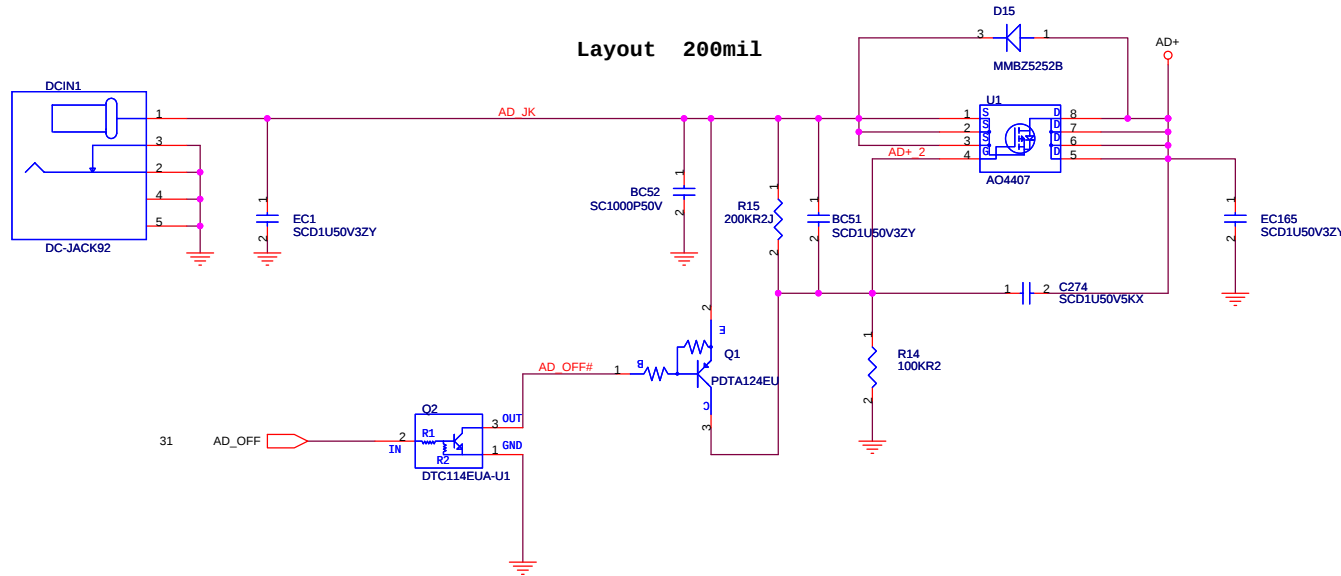
TouchPad Connector



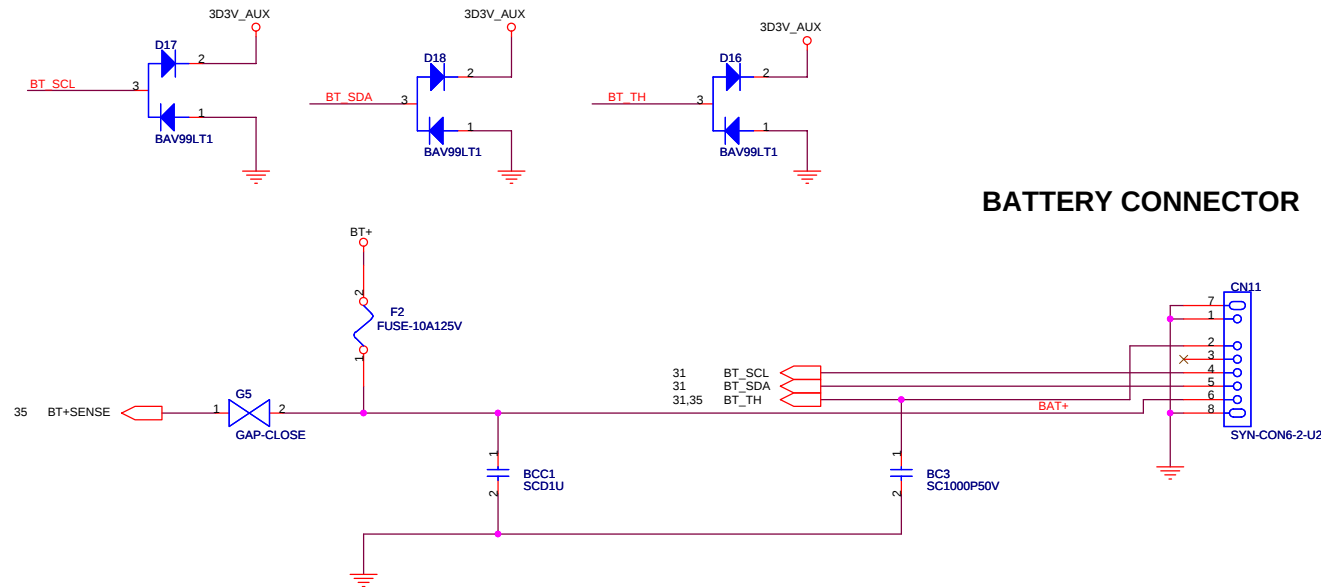


Adaptor in to generate DCBATOUT

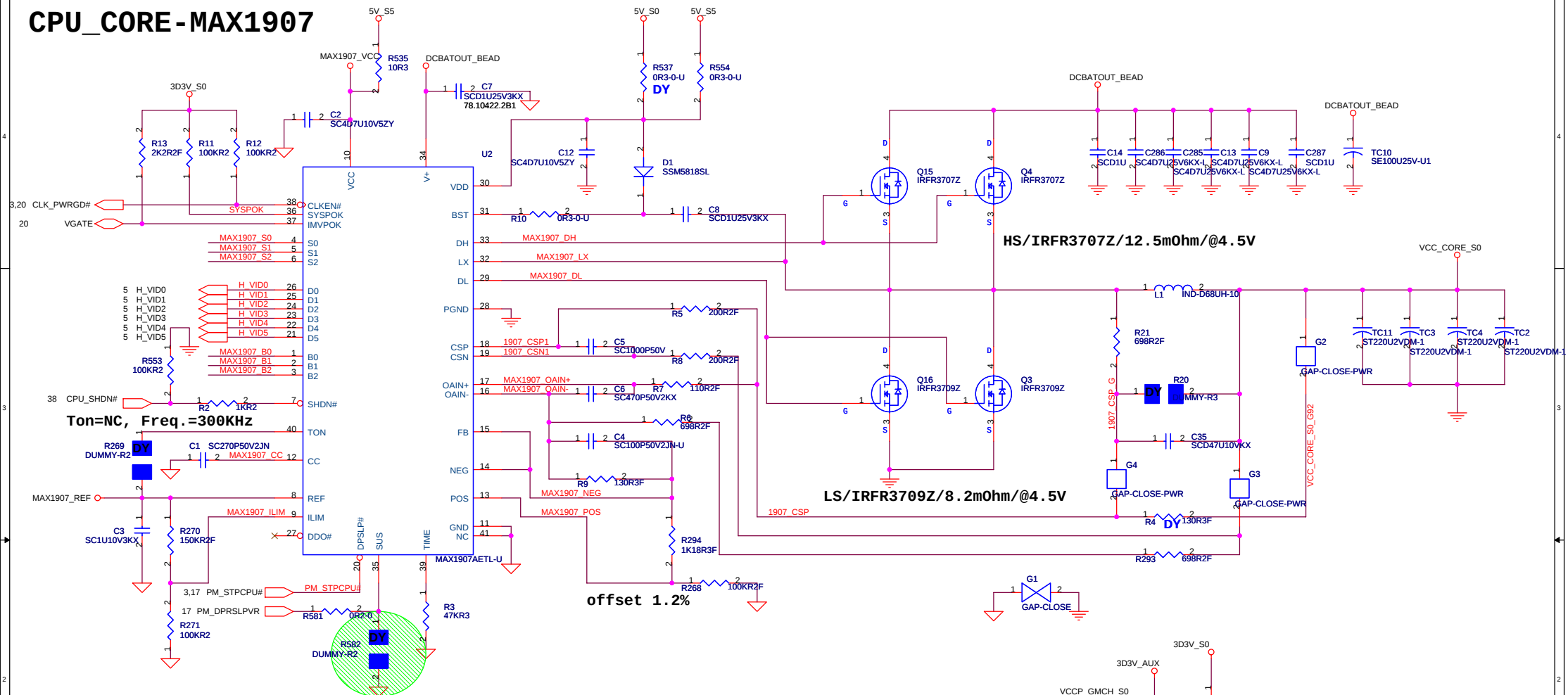
Layout 200mil



BATTERY CONNECTOR



CPU_CORE-MAX1907

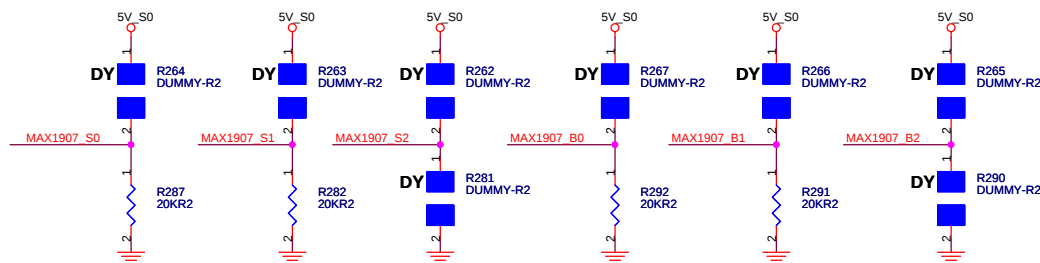
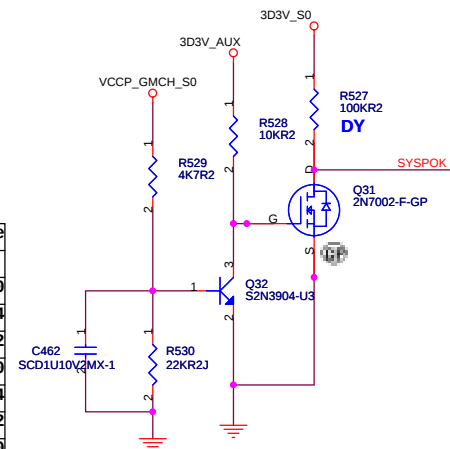


OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

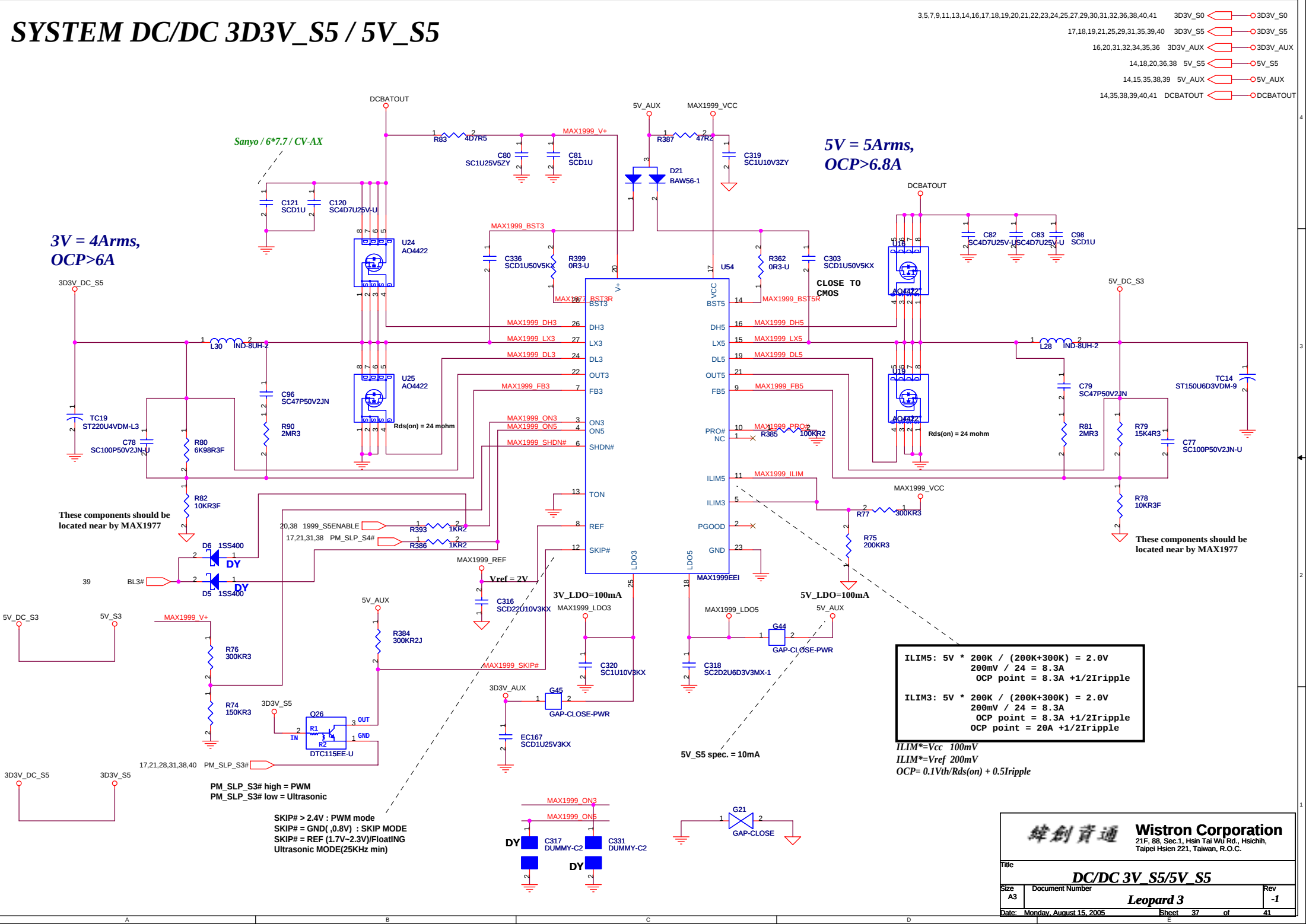
Deeper Sleep Voltage : 0.940V
, S0=L, S1=L, S2=open,

**Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open**

VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.346
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.266
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.186
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.106
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.026
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.946



SYSTEM DC/DC 3D3V_S5 / 5V_S5



5V = 5Arms,
OCP>6.8A

3V = 4Arms,
OCP>6A

These components should be
located near by MAX1977

These components should be
located near by MAX1977

$$ILIM5: 5V * 200K / (200K+300K) = 2.0V$$
$$200mV / 24 = 8.3A$$

OCP point = 8.3A +1/2Iripple

$$ILIM3: 5V * 200K / (200K+300K) = 2.0V$$
$$200mV / 24 = 8.3A$$

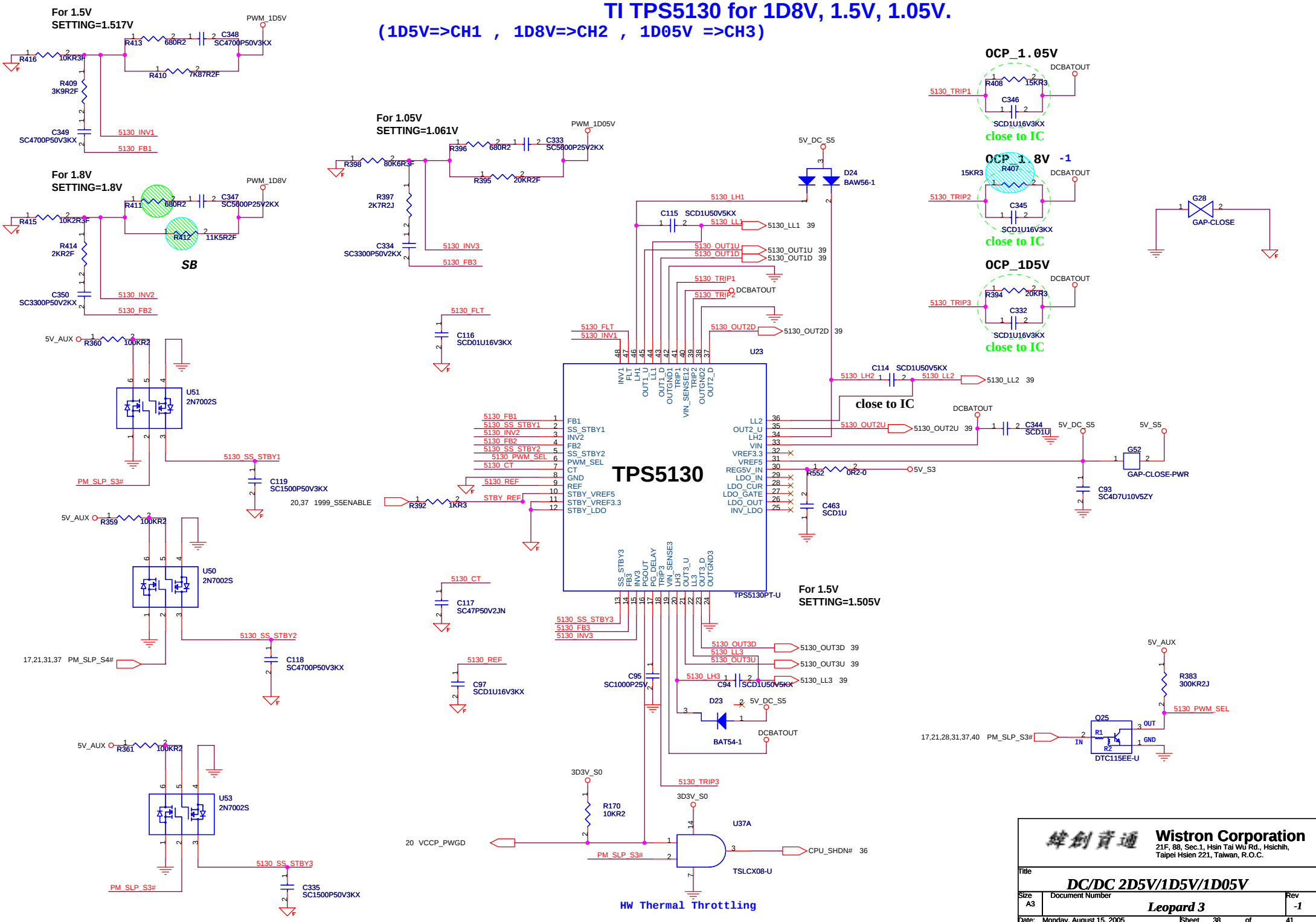
OCP point = 8.3A +1/2Iripple

OCP point = 20A +1/2Iripple

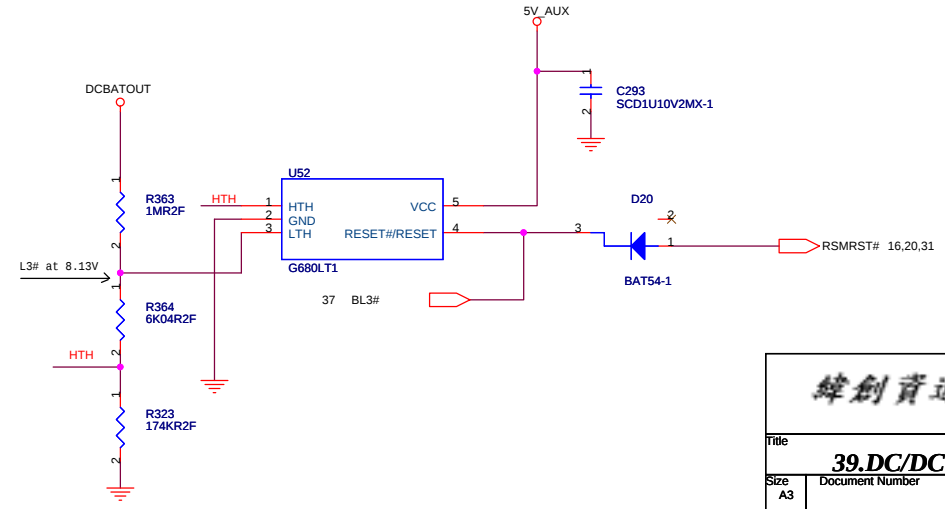
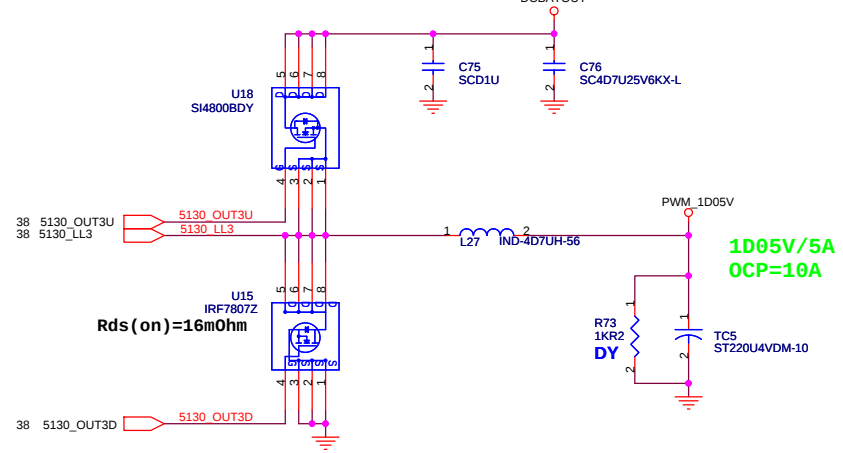
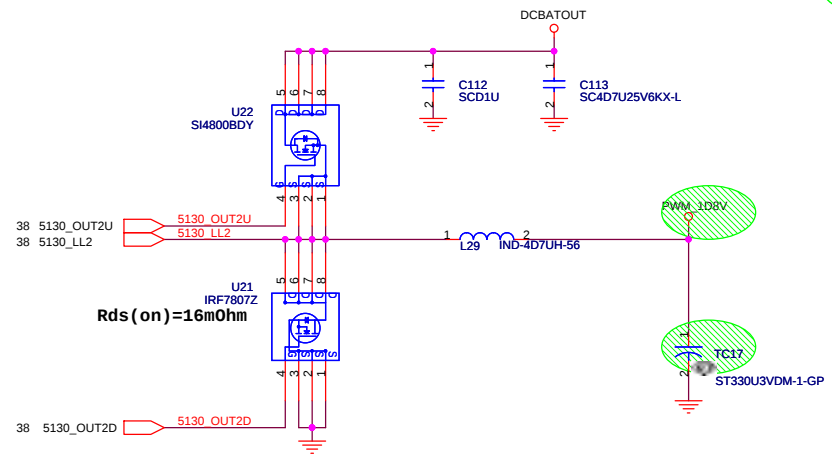
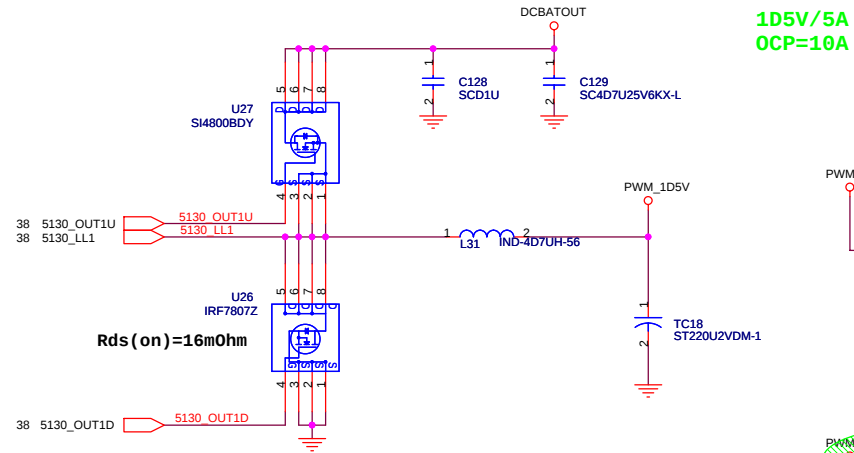
ILIM*=Vcc 100mV
ILIM*=Vref 200mV
OCP= 0.1Vth/Rds(on) + 0.5Iripple

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

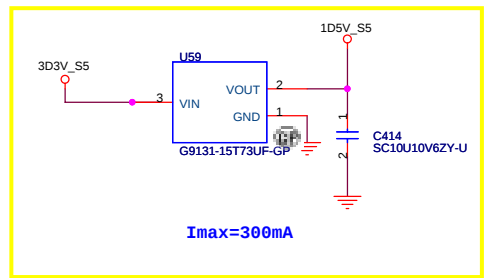
TI TPS5130 for 1D8V, 1.5V, 1.05V. (1D5V=>CH1 , 1D8V=>CH2 , 1D05V =>CH3)



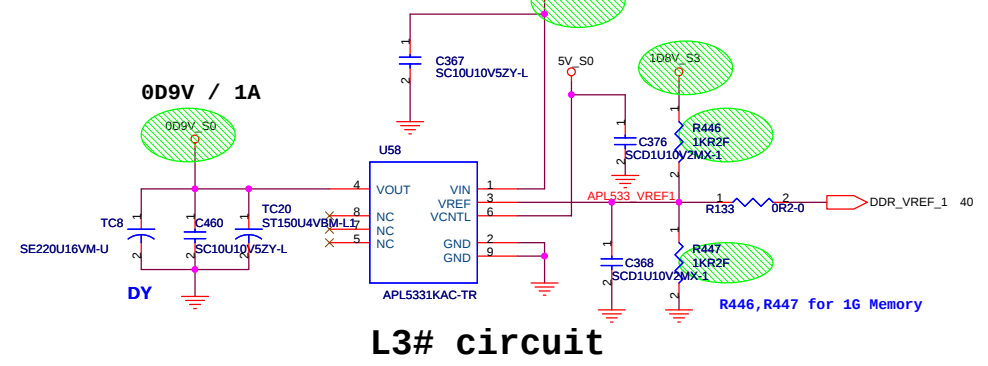
TI TPS5130 for 2.5V, 1.5V, 1.05V
(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)



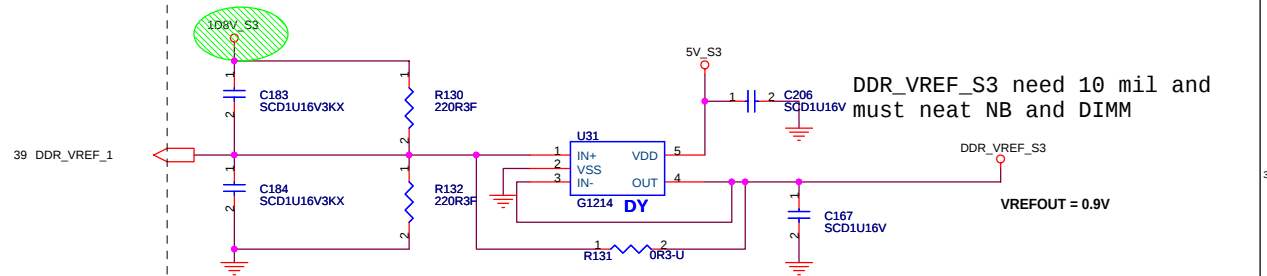
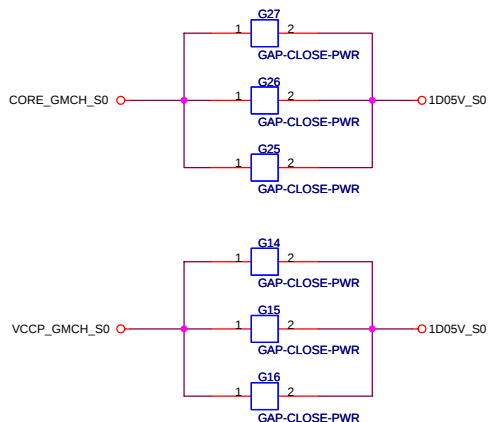
1.5V_S5 (For ICH6)



Power budget: 0D9V/2.2Apeak (For DDR2_VTT)

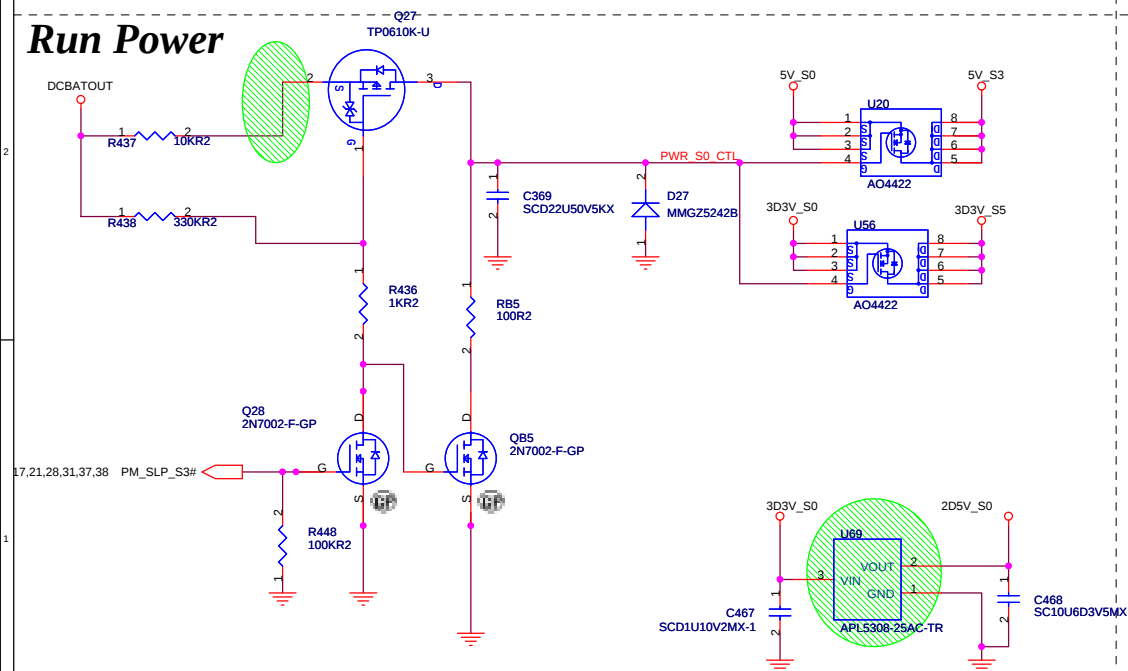


FOR GMCH Power



FOR DDR 2 Power

Run Power



Suspend Power

