

Leopard Block Diagram

Project code: 91.49Q01.001
PCB P/N : 48.49Q01.001
REVISION : 04221-2 DF

CLK GEN³
ICS954206AG

4,5
Mobile CPU
Celeron/Dothan

DDR1*2
333MHz^{11,12}

6,7,8,9,10
Alviso
GML

16,17,18,19
ICH6-M

22
PCI 1510
CARDBUS

23
PCMCIA
1 SLOT

22
Power
Switch
TPS2211A

28
Mini-PCI
802.11a/b/g

25
RJ45
CONN

24,25
10/100 RTL8100C

25
RJ11
CONN

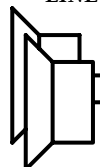
30
MODEM
MDC Card

MIC IN²⁸

26
AC'97 CODEC
AD1981B

LINE OUT

27
OP AMP
G1420B



2CH SPEAKER

Host BUS
400MHz

DMI I/F
100MHz

PCI BUS

AC97-LINK

LPC Bus

LVDS

LCD¹⁴

SVIDEO/COMP

TVOUT¹³

RGB CRT

CRT¹⁵

USB 2.0

USB x 2³⁰

P IDE

MASTER

HDD²¹

SLAVE

DVD/
CD-RW²¹

X-BUS

31
KBC
NS97551

32
Touch
Pad

32
Int.
KB

20
Thermal
& Fan
G768D

33
FlashRom
4Mb
(512kB)

SYSTEM DC/DC MAX1999 ³⁷	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC TPS5130 ^{38,39}	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 2D5V_S3

MAXIM CHARGER MAX8725 ³⁵	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC MAX1907 ³⁶	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

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Title	
Block Diagram	
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ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]/GPO[17], GNT[6]/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDRQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

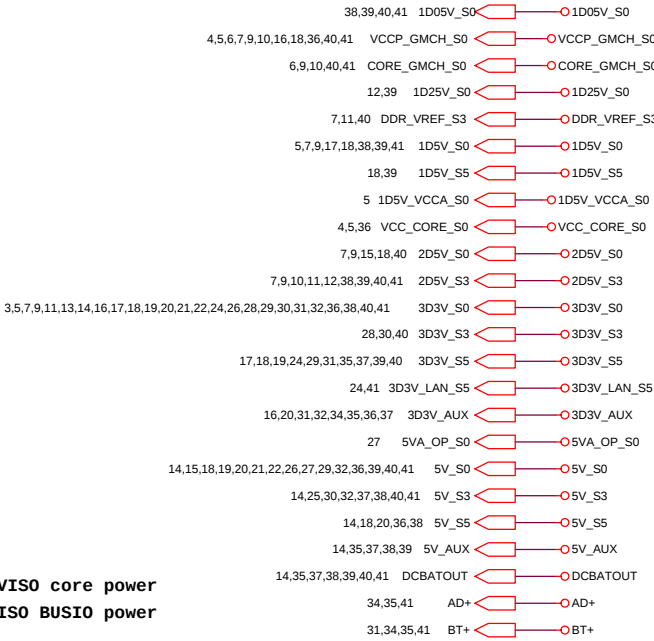
ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
5V_S3= 5 Voltage suspend to RAM(S3 state)
5V_S5= 5 Voltage soft off(S5 state)
3D3V_S0= 3.3 Voltage power up on system work(S0 state)
3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
3D3V_S5= 3.3 Voltage soft off(S5 state)
LVDDR_2D5V= 2.5 Voltage power up on system work(S0 state)
2D5V_S3= 2.5 Voltage suspend to RAM(S3 state)
2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S5= 1.5 Voltage soft off(S5 state)
DDR_VREF_S3= 1.25 Voltage suspend to RAM(S3 state)
1D25V_S0= 1.25 Voltage power up on system work(S0 state)
1D2_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
1D05V_S0= 1.05 Voltage power up on system work(S0 state)
CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power



PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0#/GNT0#
Cardbus Controller TI PCI1510	AD22	(CARBUS)P_INTG#	REQ1#/GNT1#
LAN	AD23	P_INTE#	REQ2#/GNT2#

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Title

ITP

Size
A3

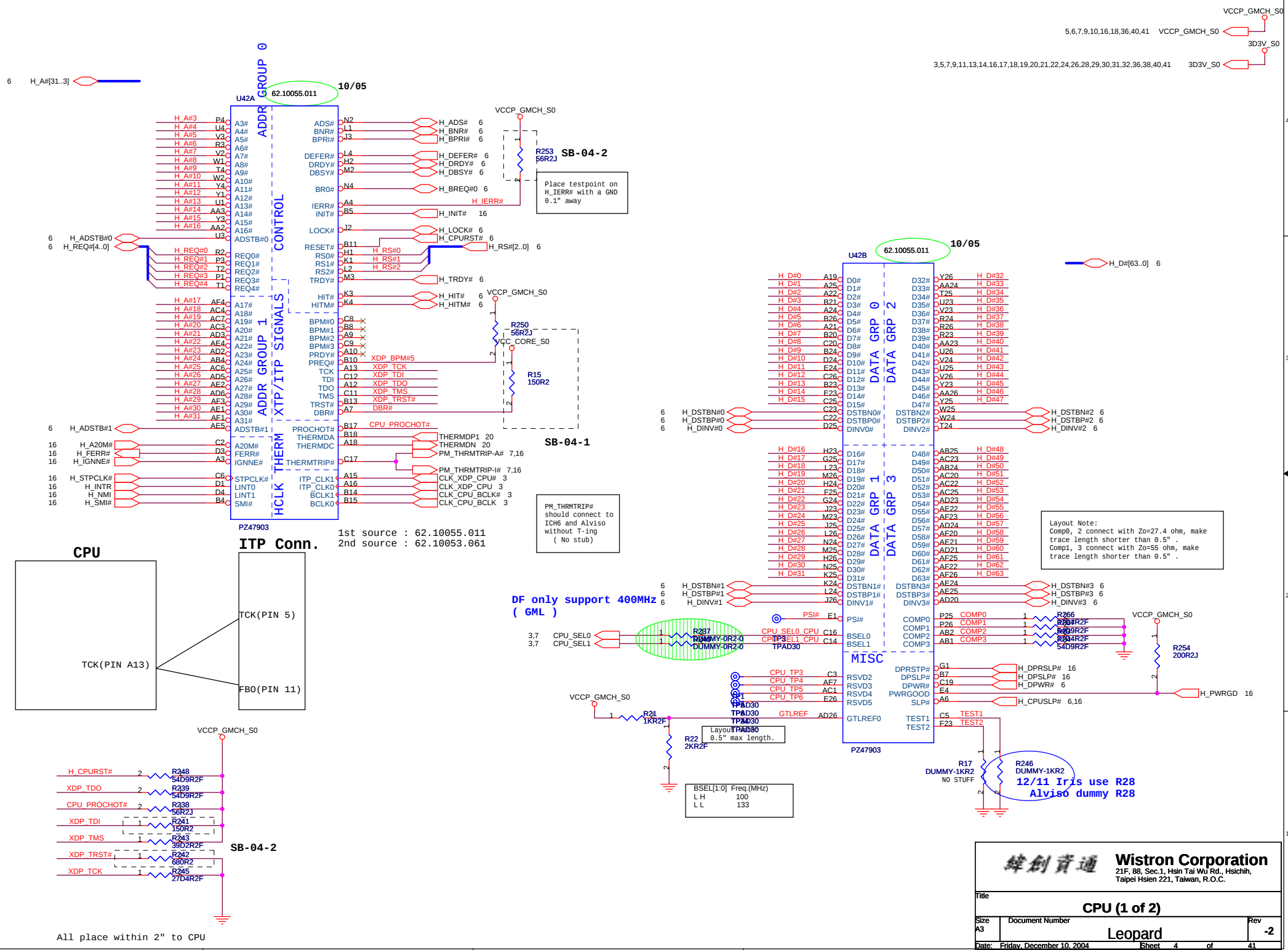
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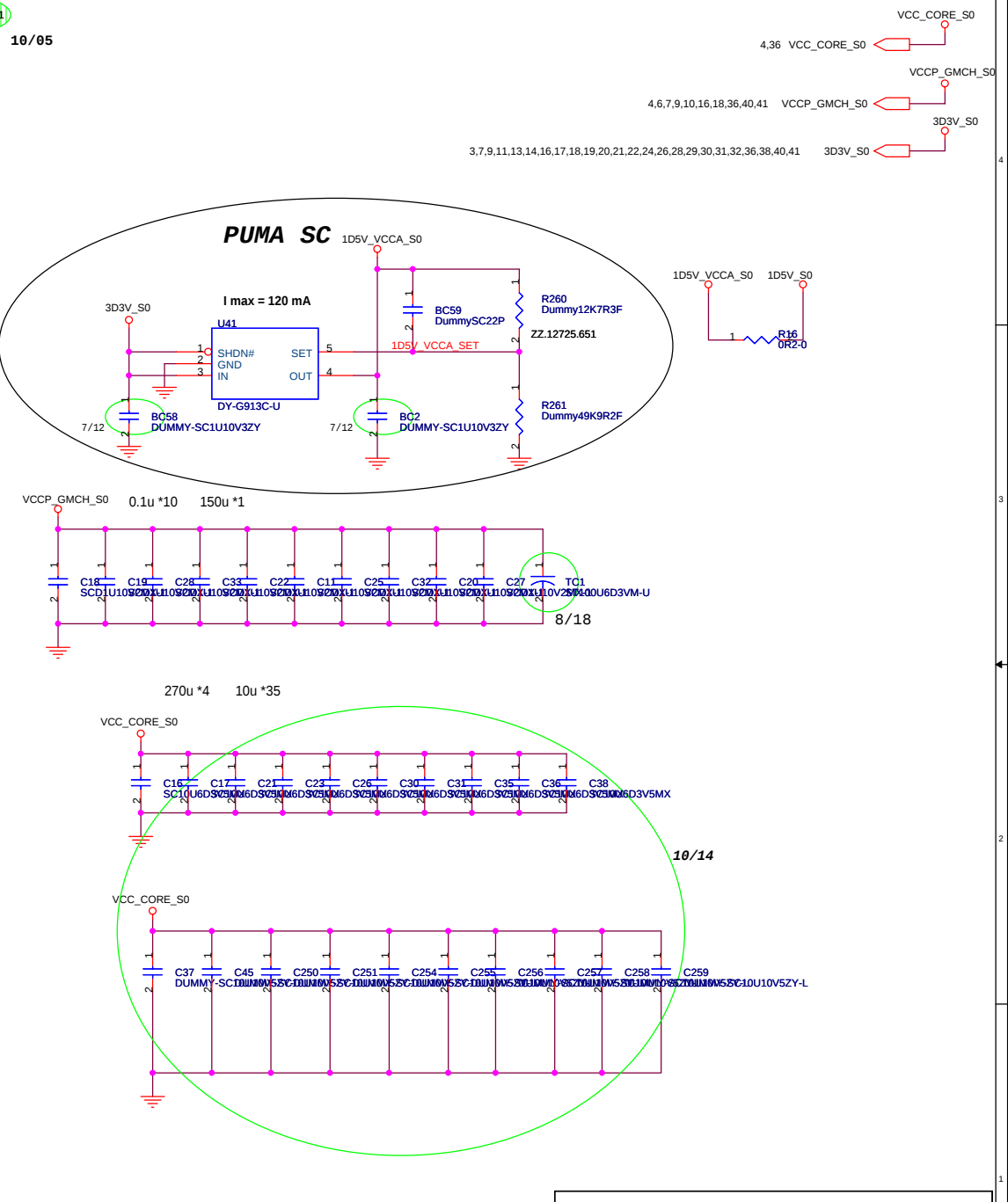
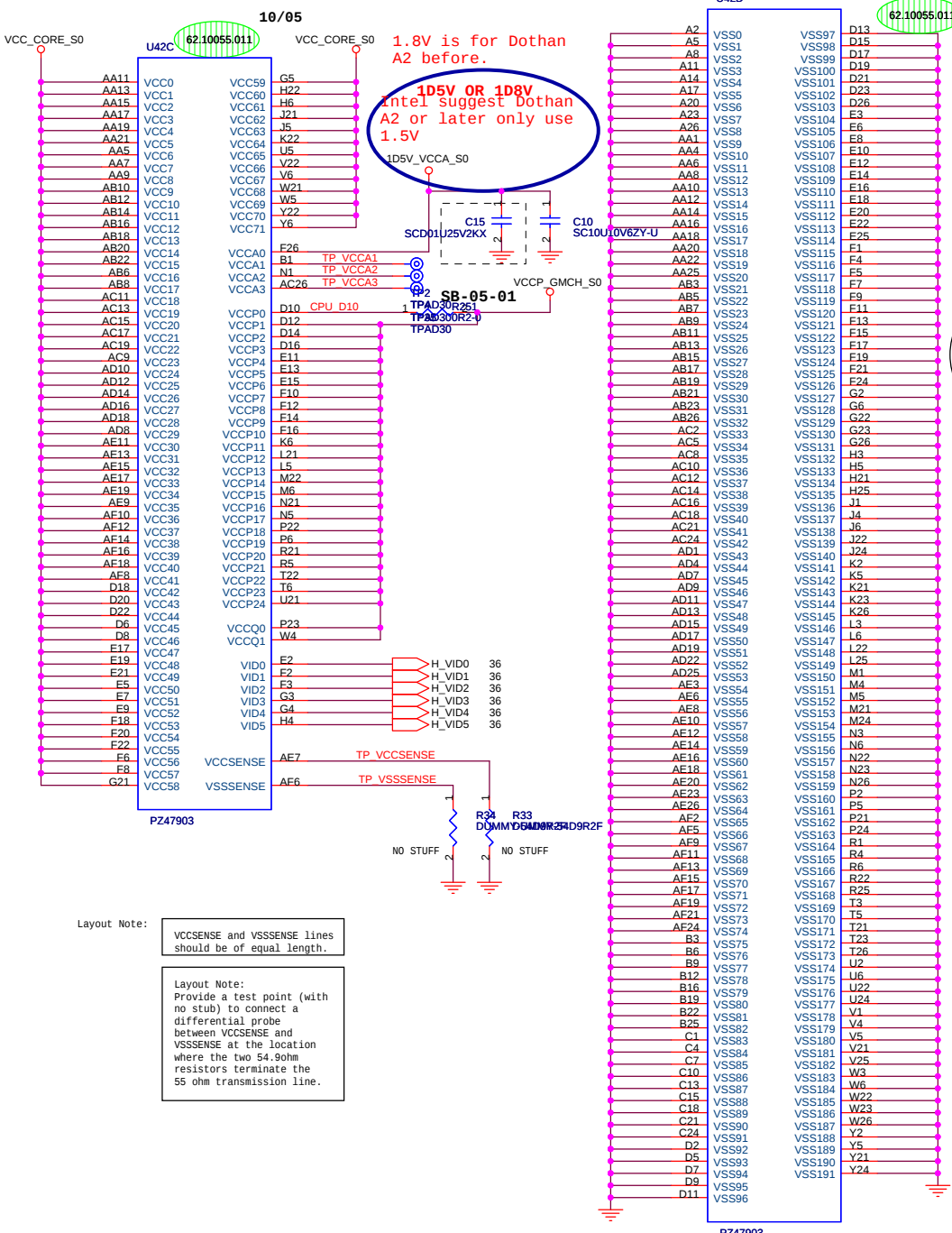
Leopard

Rev
-2

Date: Thursday, December 09, 2004

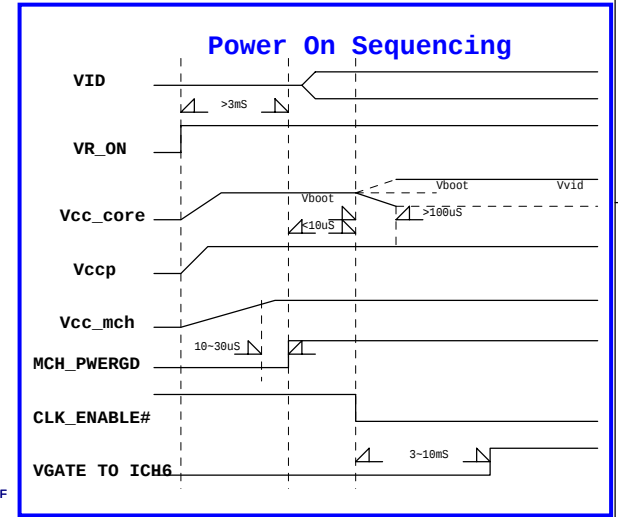
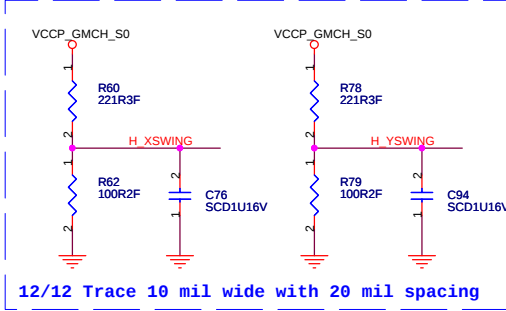
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Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

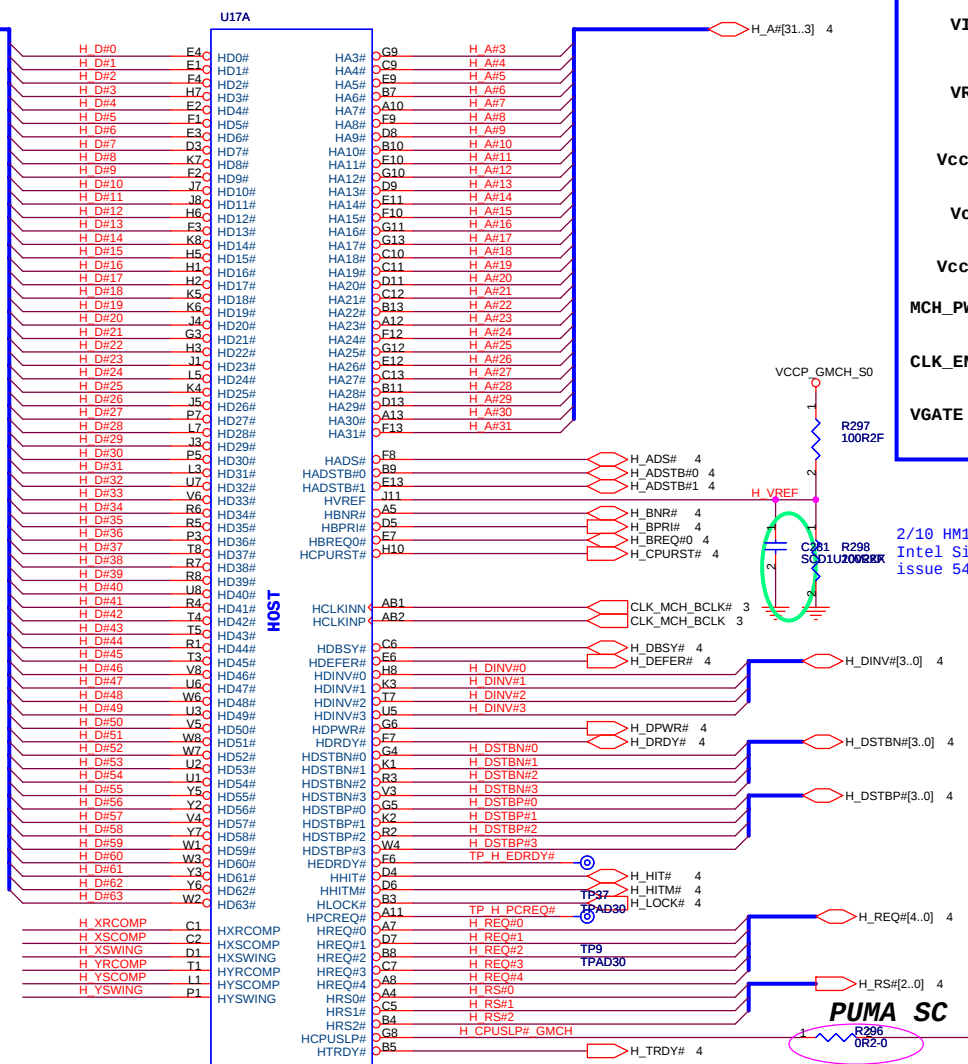


Alviso Strapping Signals and Configuration

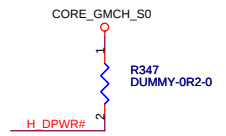
REV.NO. 1.0
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 101 = FSB400 others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	0 = DDR2 1 = DDR1 (Default)
CFG7	CPU Strap	0 = Reserved 1 = Dothan (Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes 1 = Normal (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	GMCH core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present(Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

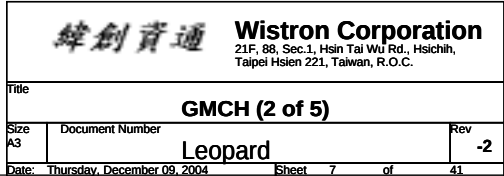


For
Banias/Celeron-M:R1079=DUMMY
For Dothan A:R1079=DUMMY
For Dothan B:R1079=0R

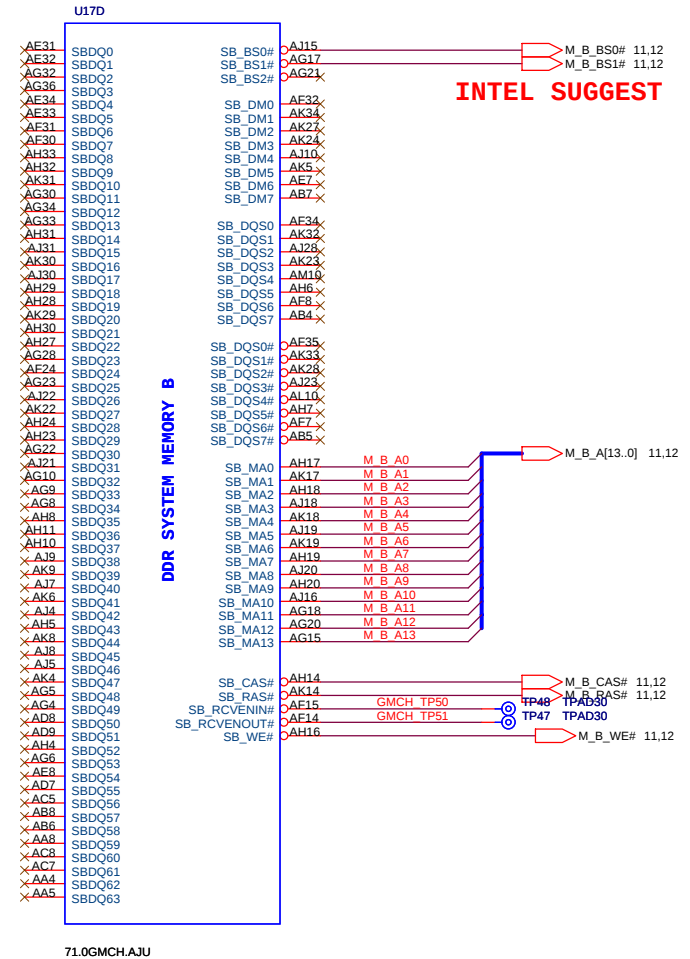
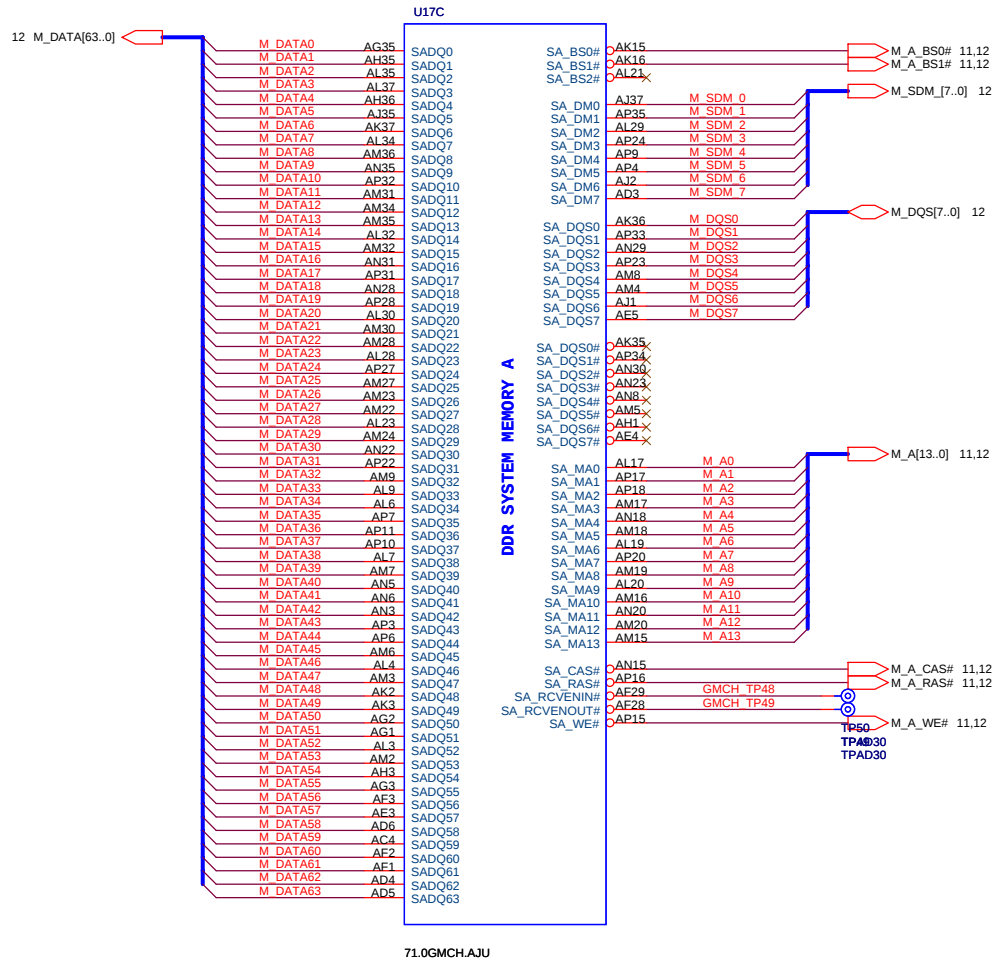


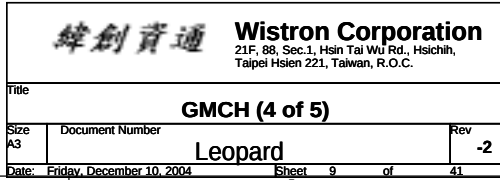
ALVISO-GM:71.0GMCH.08U
ALVISO-PM:71.0GMCH.0BU
ALVISO-GML:71.0GMCH.0JU

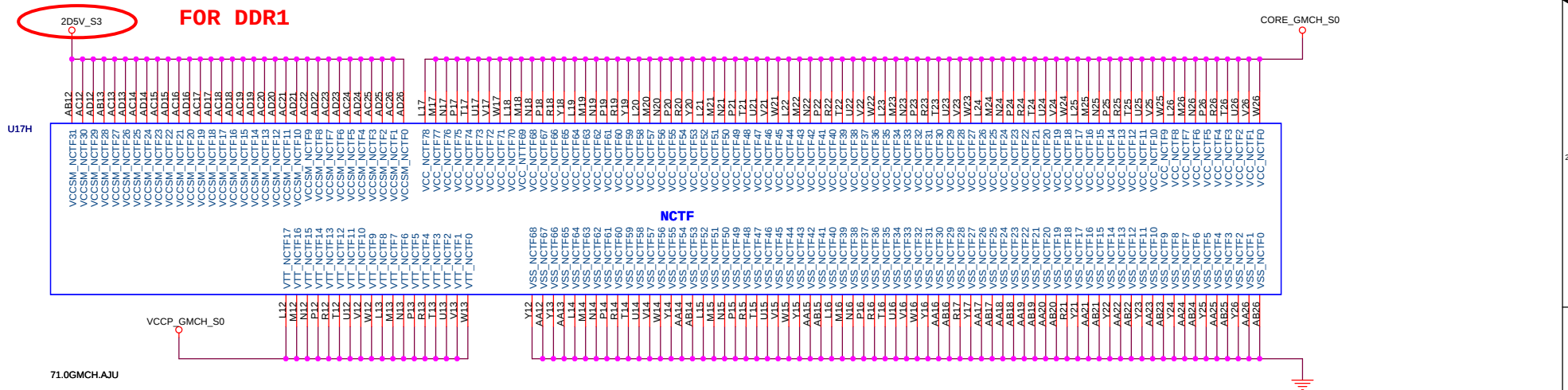
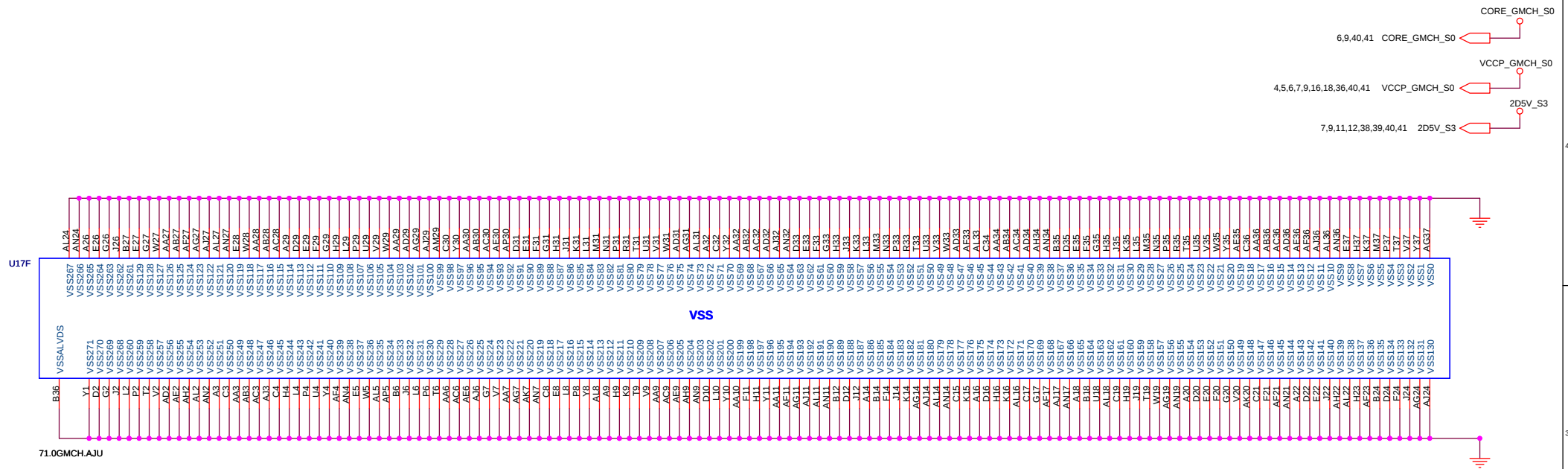
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Title			
GMCH (1 of 5)			
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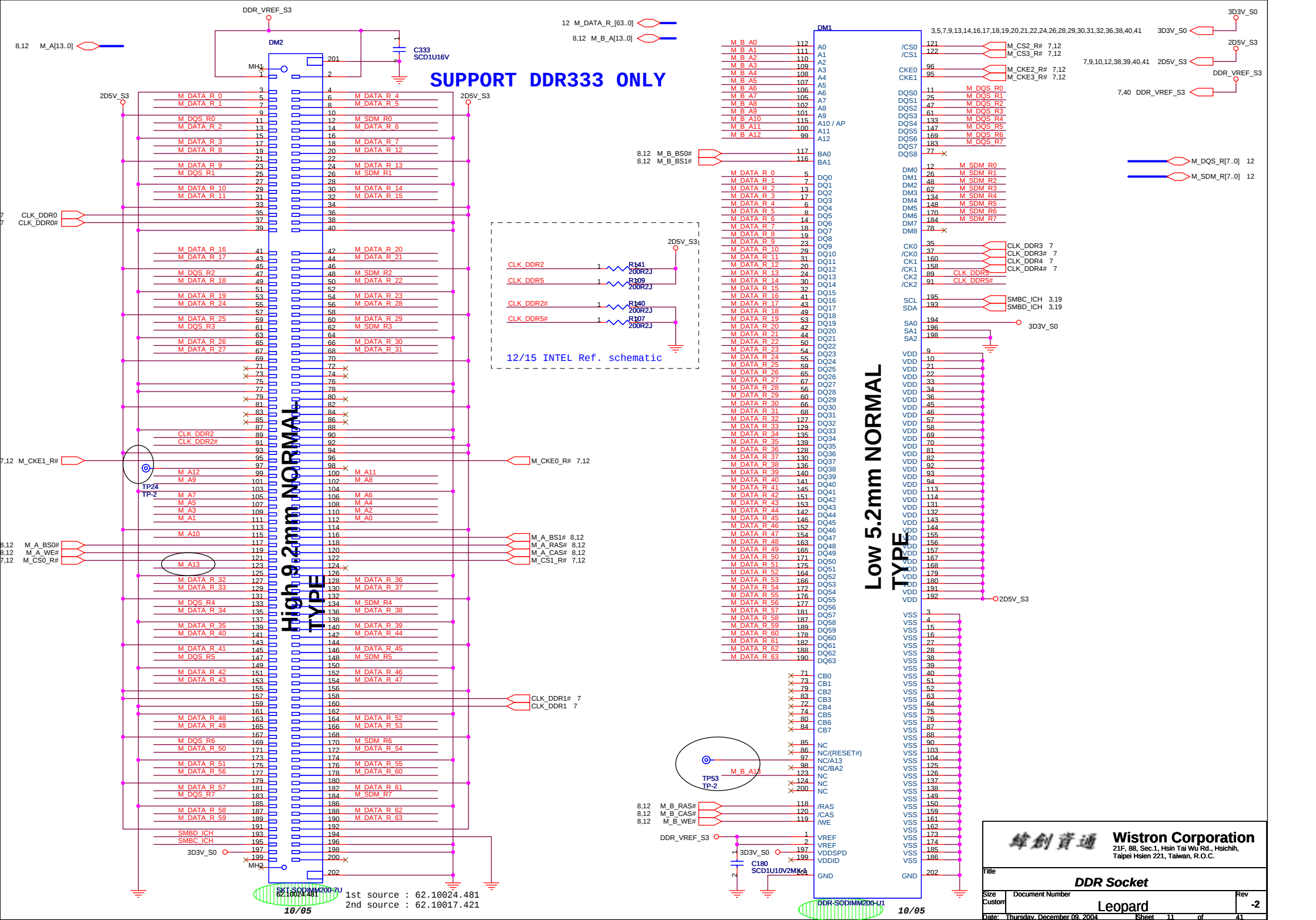


SUPPORT DDR333 ONLY









SERIES DAMPING

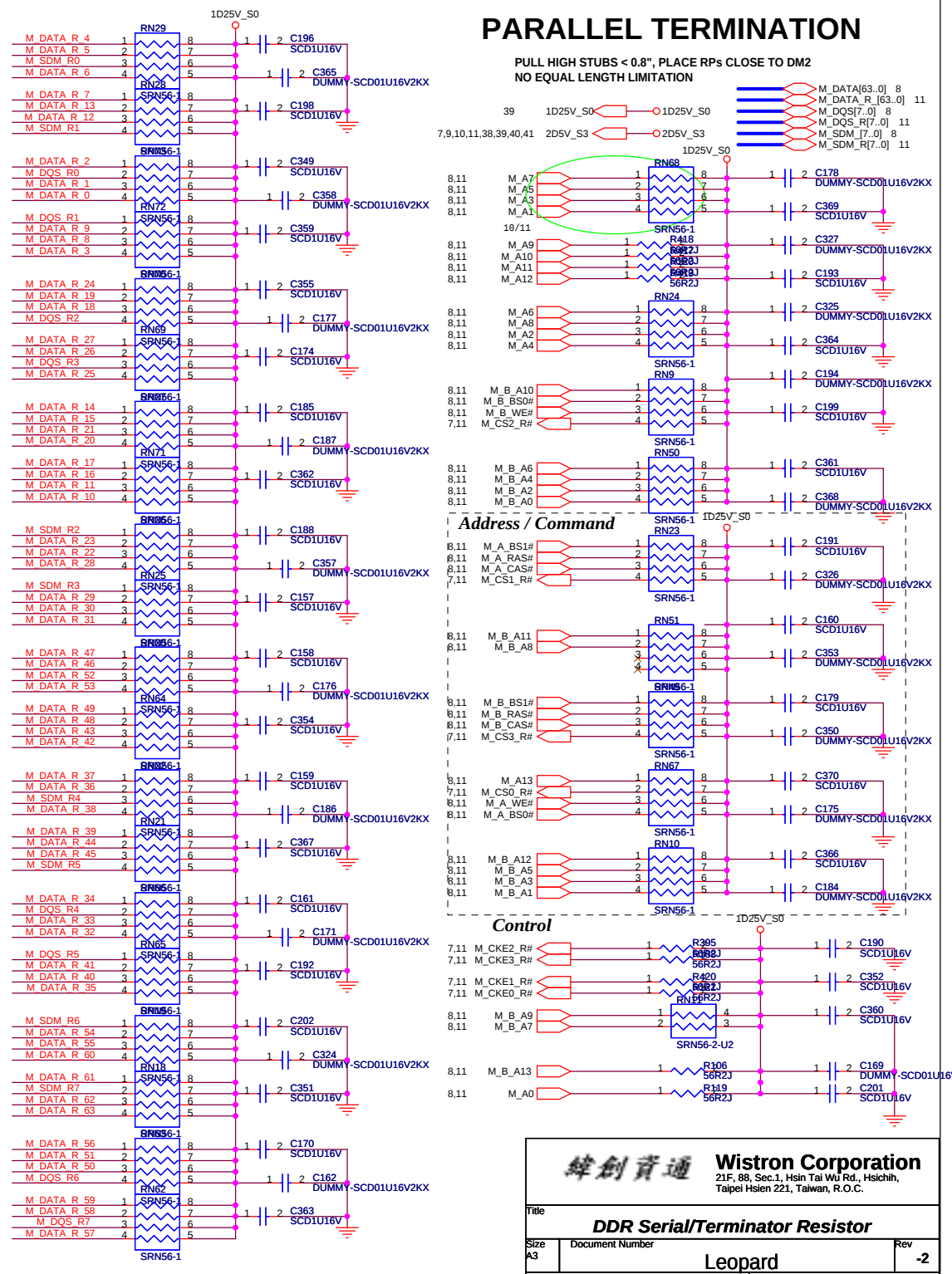
SC

Change RN to small size



PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO DM2
NO EQUAL LENGTH LIMITATION



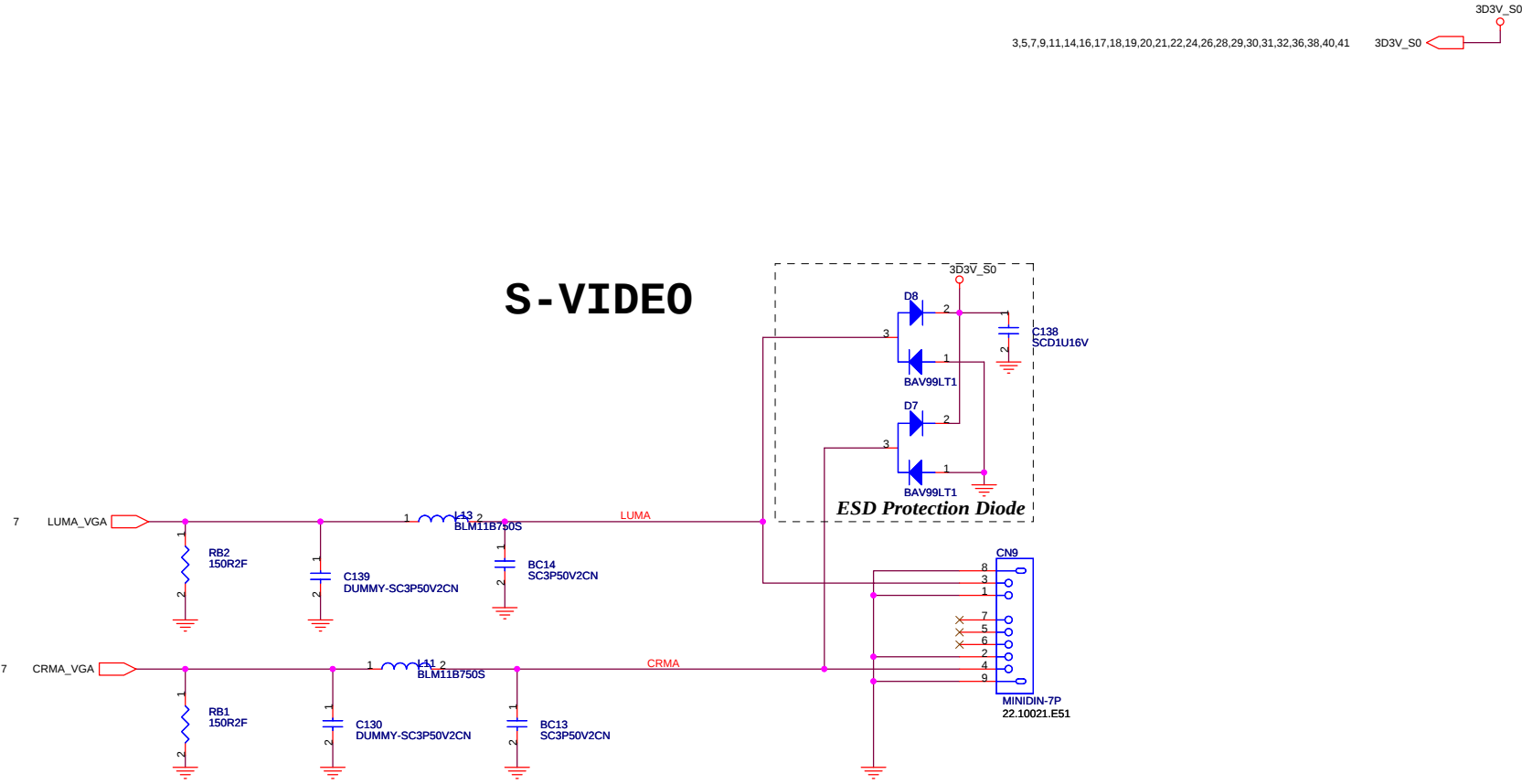
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DDR Serial/Terminator Resistor

Size A3 Document Number Leopard Rev -2

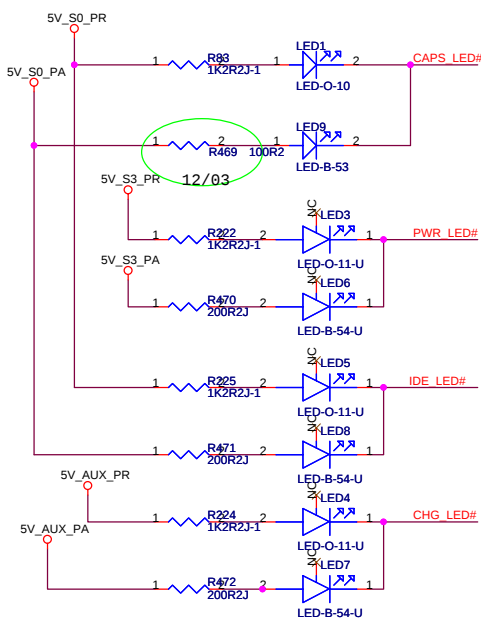
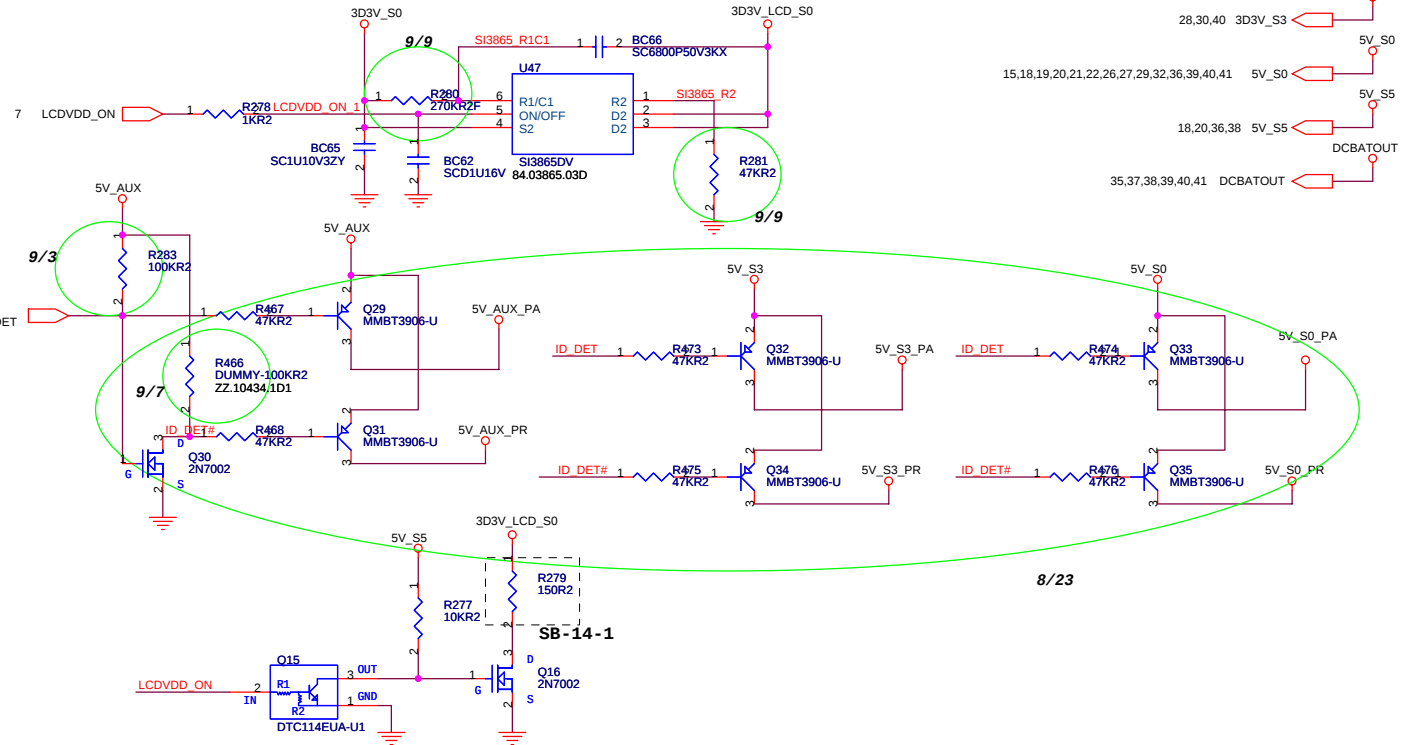
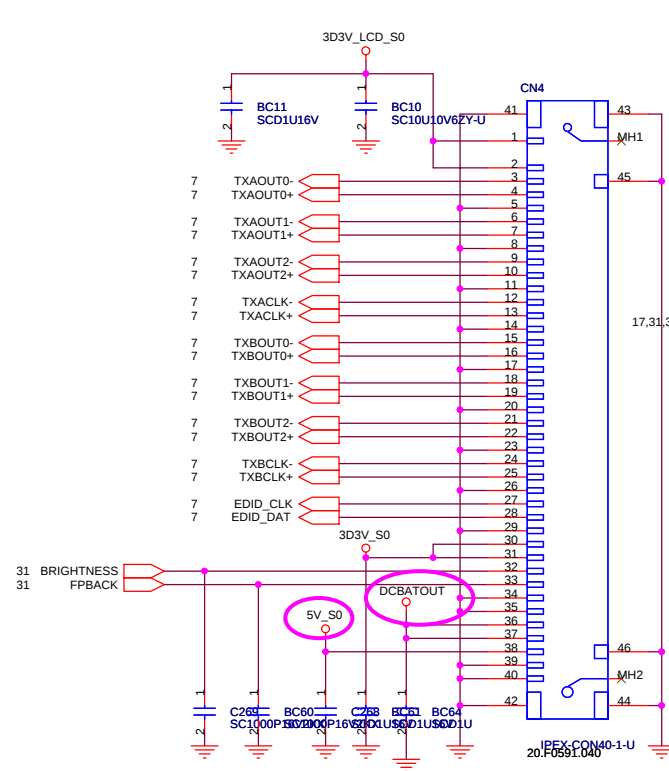
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S-VIDEO



Place on bottom side

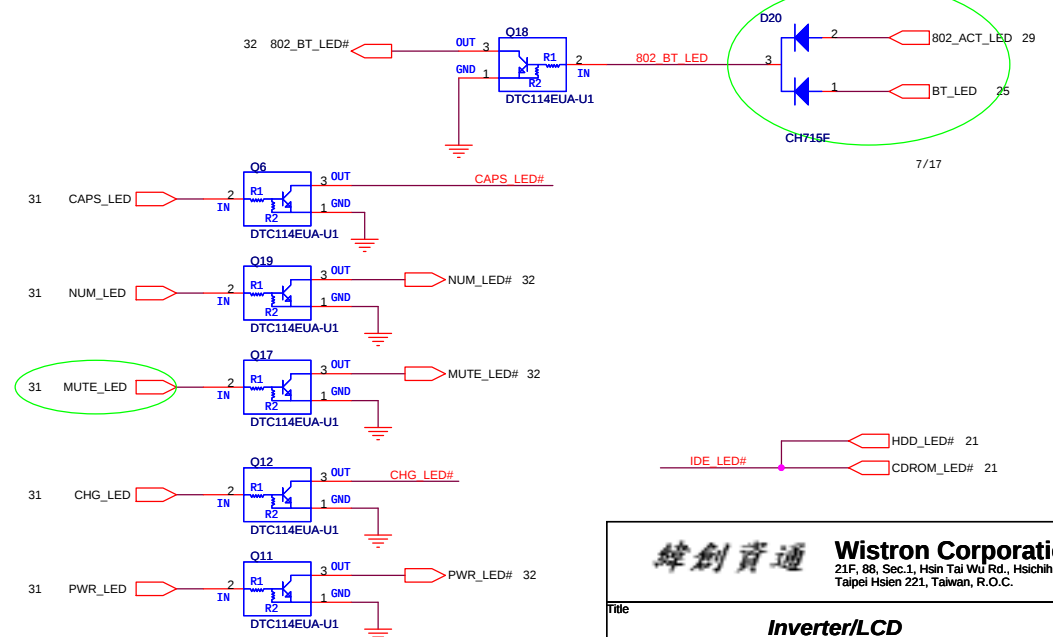
INVERTER/LCD



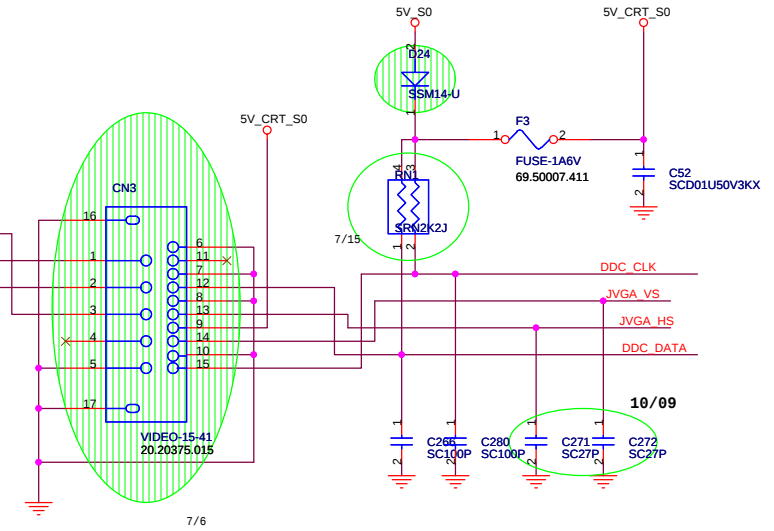
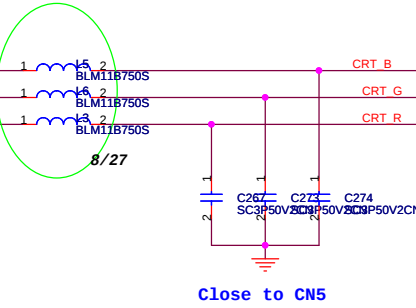
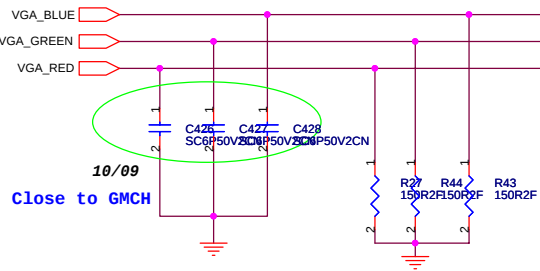
	PWR	CHR	HDD	IR	CAP3
PR Bottom	Amber LED3	Amber LED4	Amber LED5	X	Amber LED1
PA Top	Blue LED6	Blue LED7	Blue LED8	X	Blue LED1

PA & PR diffent parts

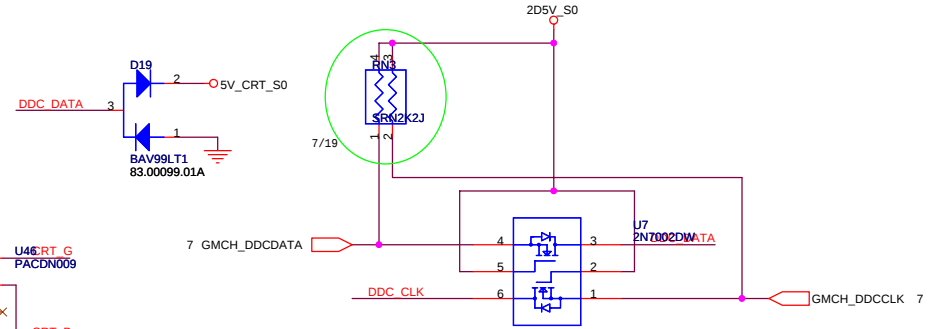
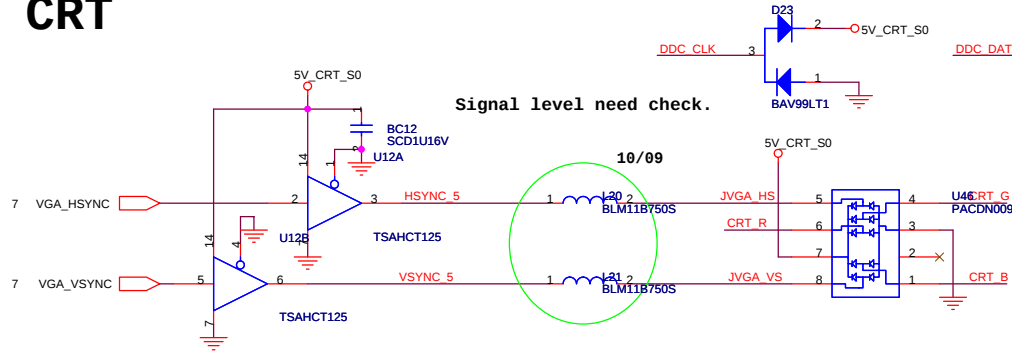
	PA	PR
LED1	83.00190.Y70	83.00190.W70
LED3	Dummy	83.00110.D70
LED4	Dummy	83.00110.D70
LED5	Dummy	83.00110.D70
LED6	83.00110.E70	Dummy
LED7	83.00110.E70	Dummy
LED8	83.00110.E70	Dummy
R83	63.20134.1D1	63.10234.1D1
R222	63.20134.1D1	63.10234.1D1
R225	63.20134.1D1	63.10234.1D1
R224	63.20134.1D1	63.10234.1D1



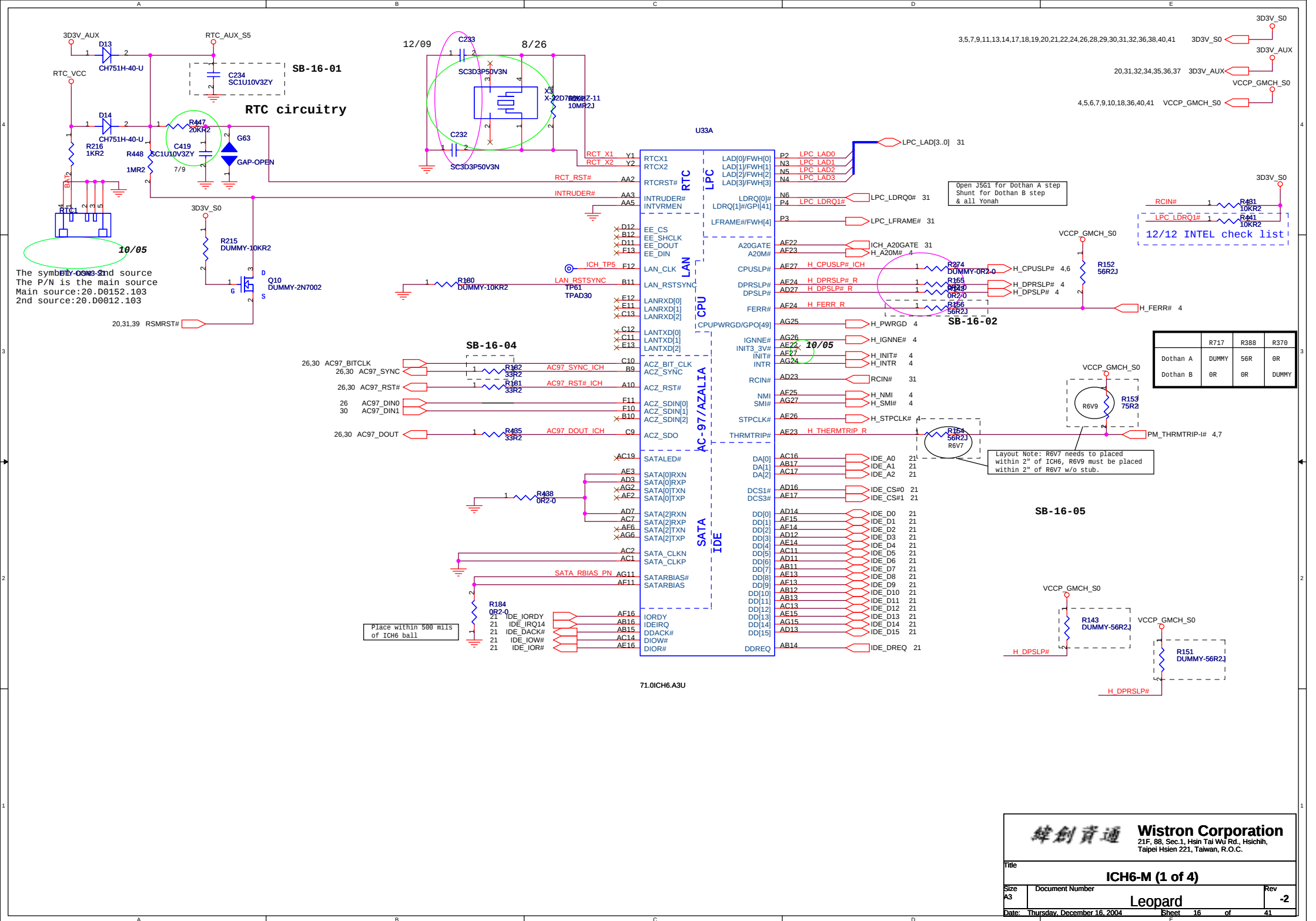
CRT

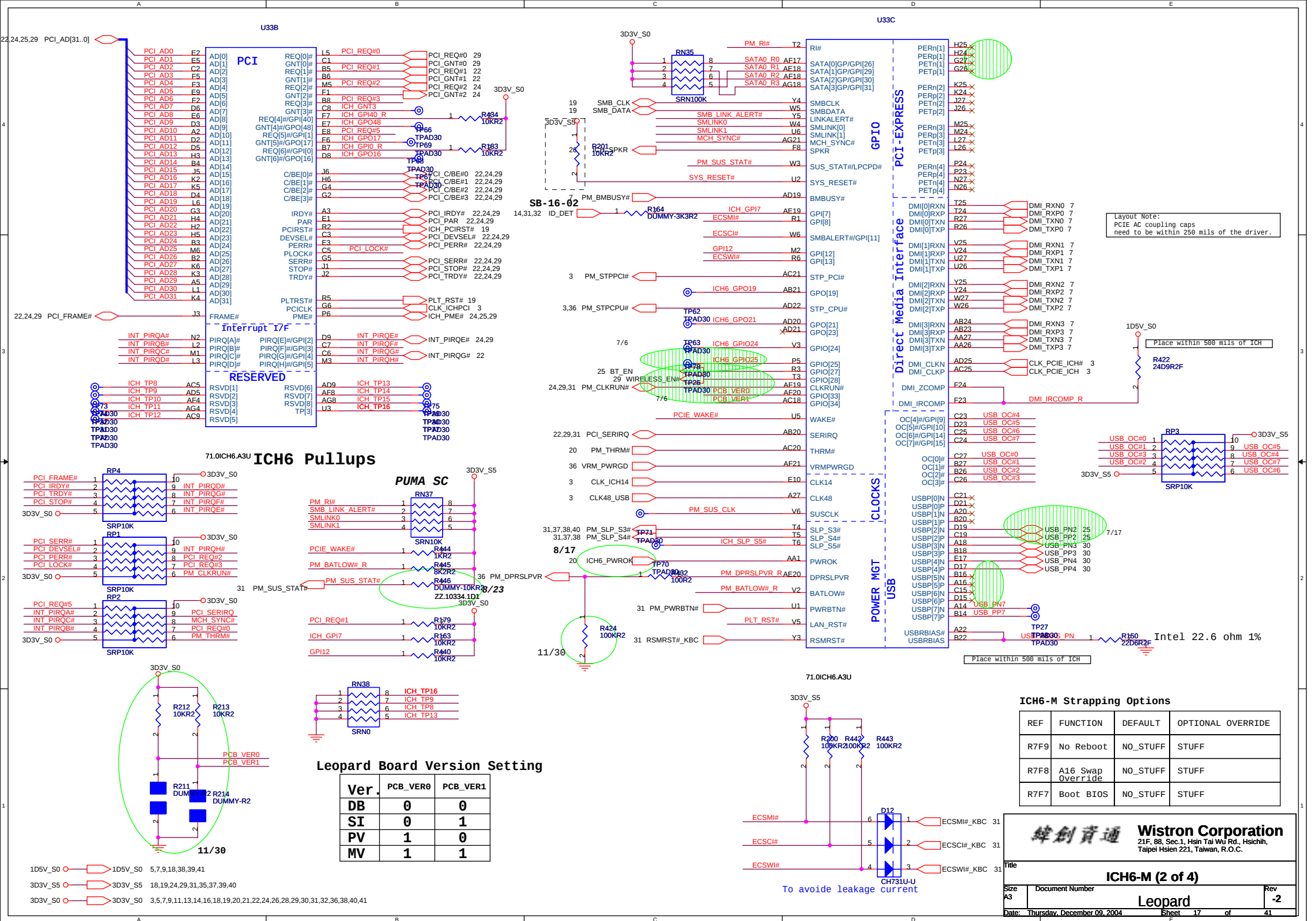


CRT



CRT CONN





Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27

Layout Note:
IDE decoupling

Layout Note:
PCI decoupling

Place within 100
mils of ICH
near pin AG5

Place within 100
mils of ICH
near pin AG9

Place within 100
mils of ICH

Place within 100
mils of ICH
near E26, E27

Place within 100
mils of ICH
pin AG10

Intel dummy
Place within 100
mils of ICH
pin A13

Place within 100
mils of ICH
pin A17

U33E

CORE

IDE

PCI

USB

CORE

PCI

IDE

USB

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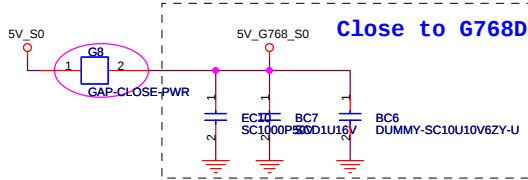
IDE

USB

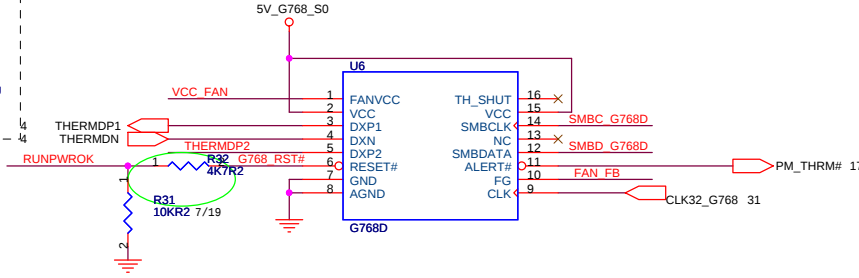
CORE

PCI

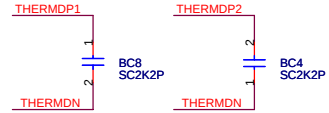
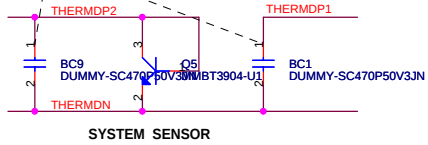
IDE



Reserve for G768B
works at High
Speed

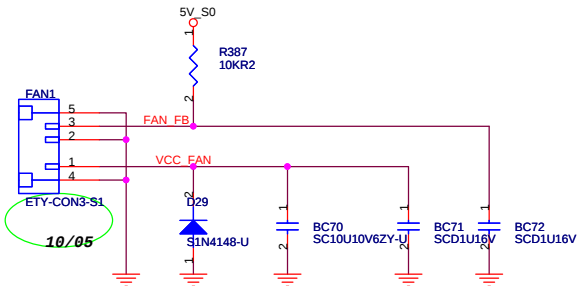


Put these two Caps near the thermal diode.

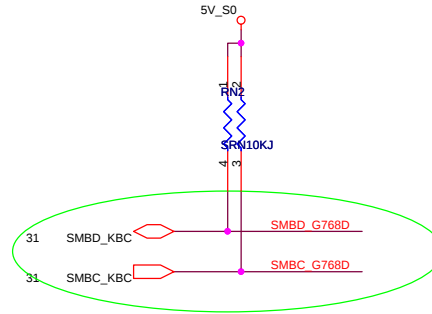


THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B

180 ms after VCC_G768 > 4.38v, p2, 7



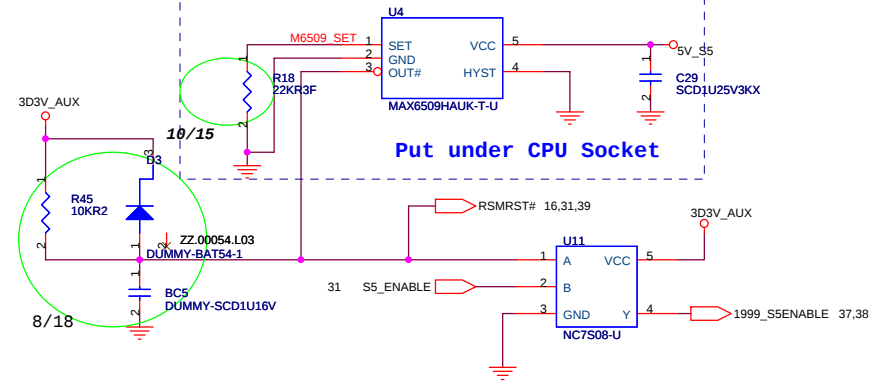
The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103



1013

$$R_{set} = 83793 / (T + 273) - 211.3569 + 129890 / (T + 273)^2$$

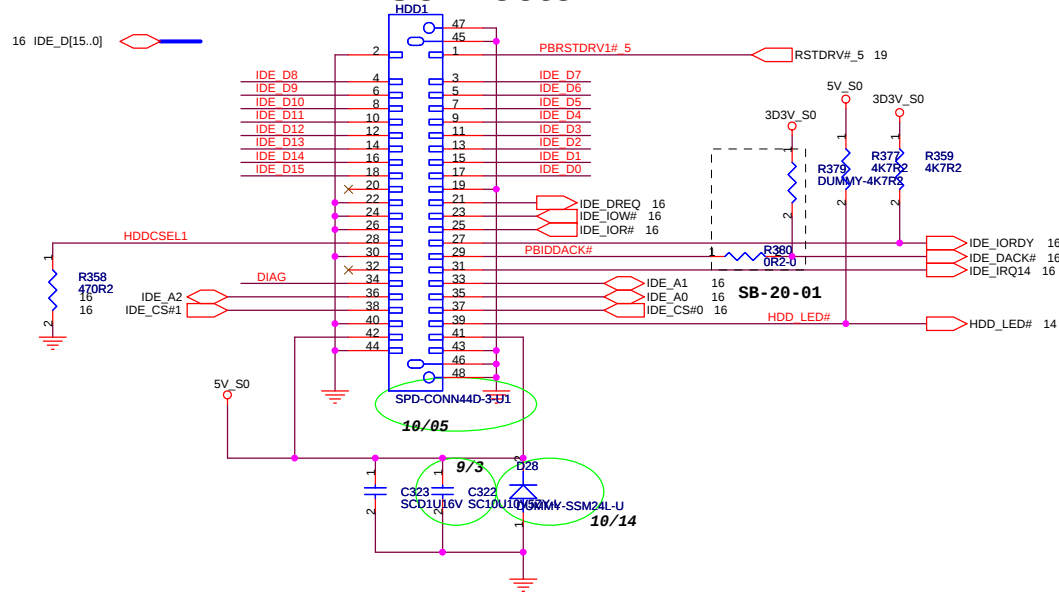
R22K SET TO 85°C
Must close to MAX6509



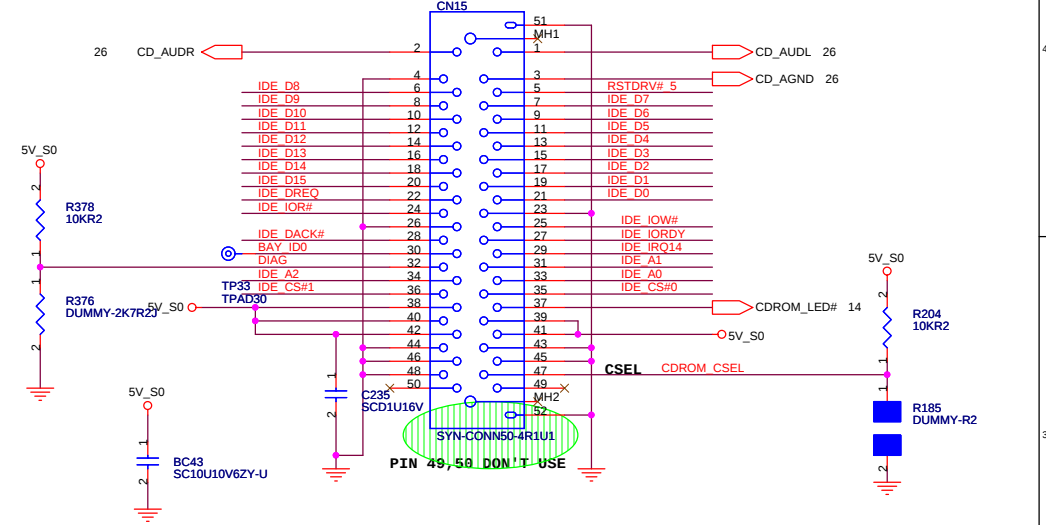
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Title		
G768D		
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HDD Connector



CDROM

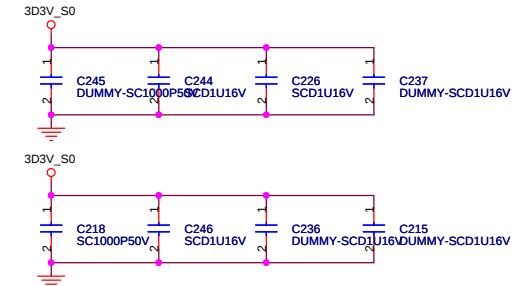


Internal : 1uF bypass cap
External : 0.1uF bypass
cap

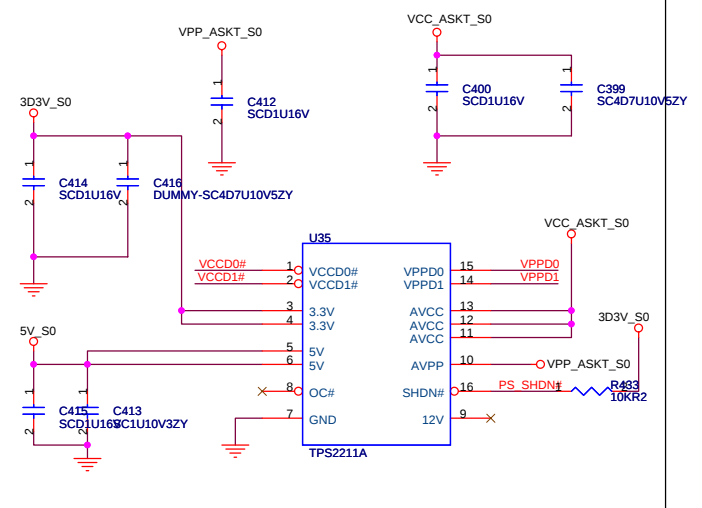
3.5,7,9,11,13,14,16,17,18,19,20,21,24,26,28,29,30,31,32,36,38,40,41

3D3V_S0

Bypass/Decupling Capacitors
Should be places as close to
PCI1510 as possible

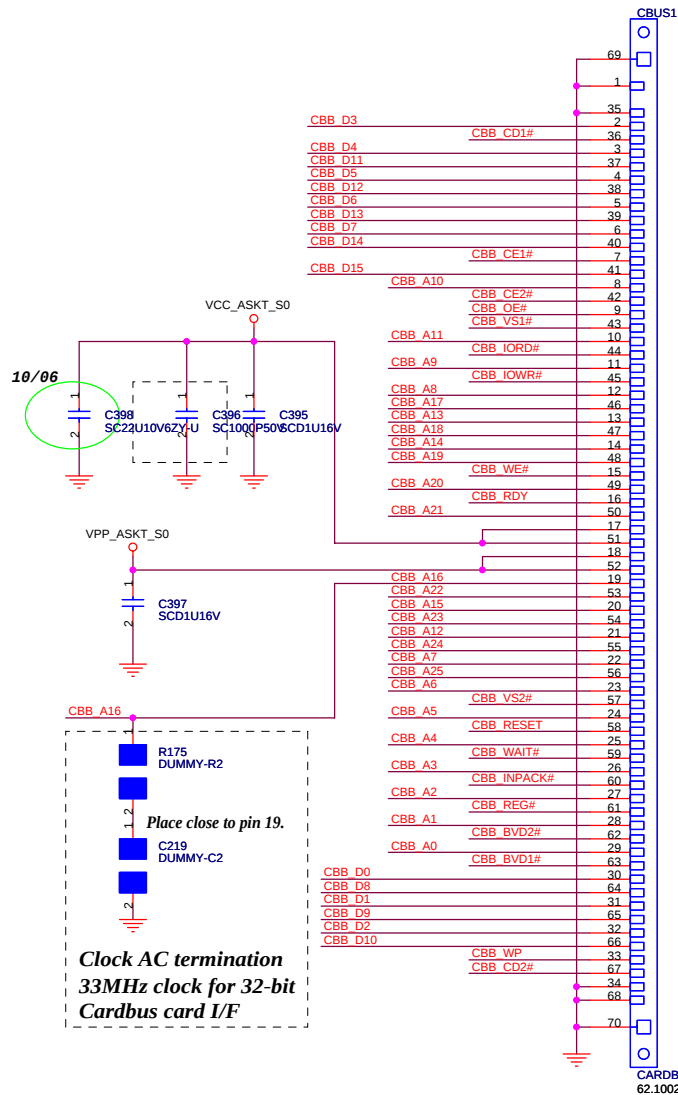


Power switch

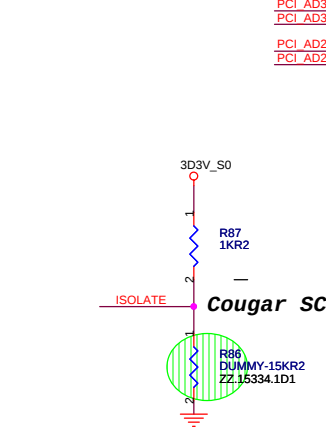
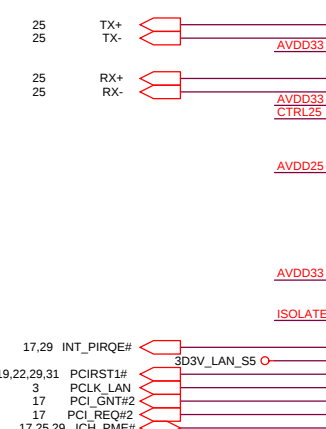
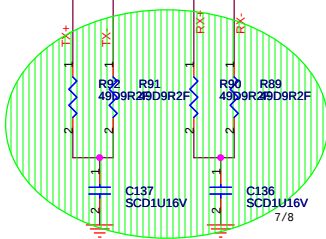
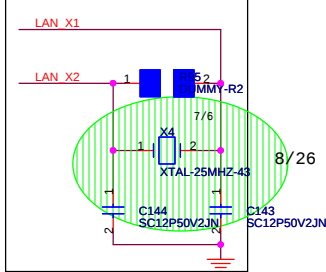


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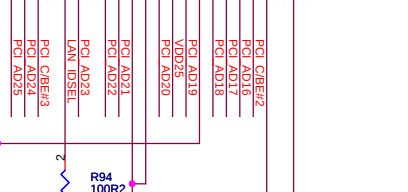
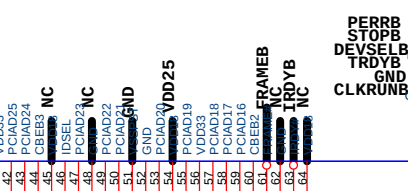
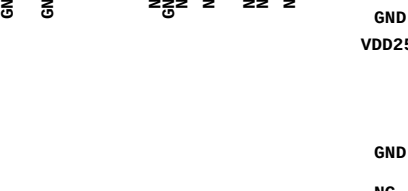
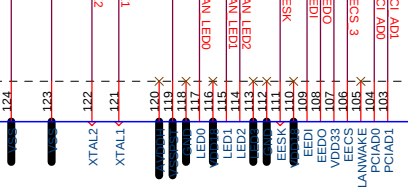
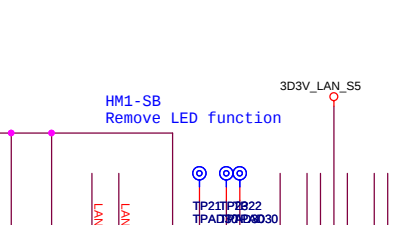
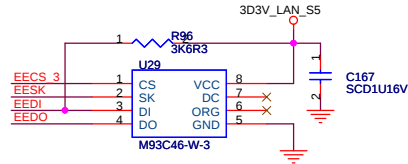
PCMCIA Socket



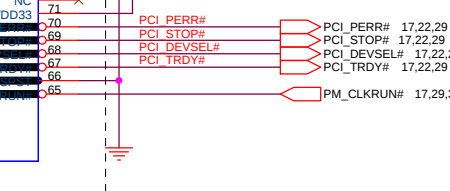
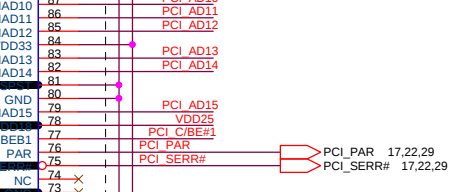
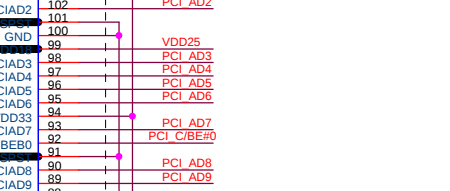
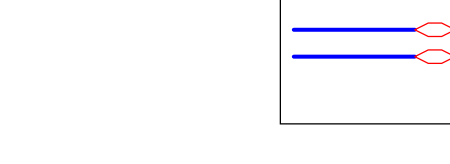
Close to RTL8100C
Pin121, Pin122



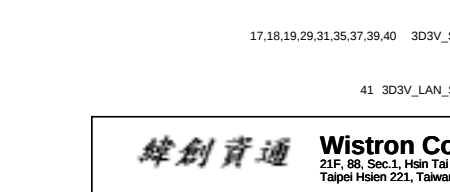
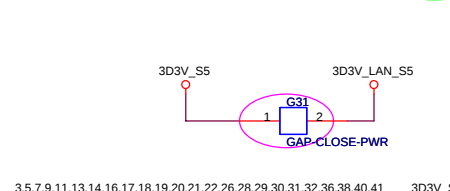
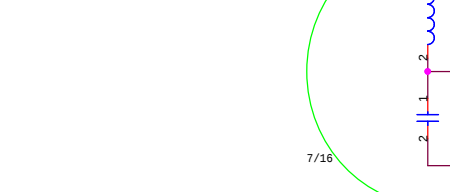
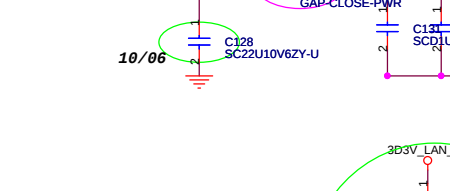
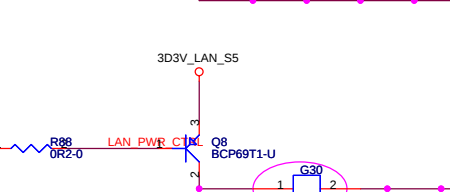
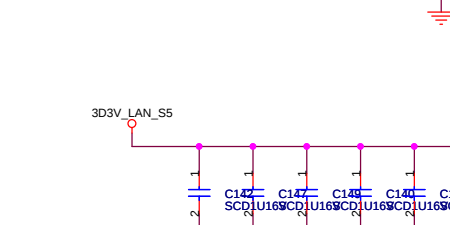
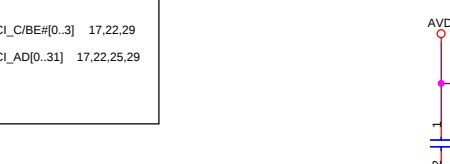
Cougar SC



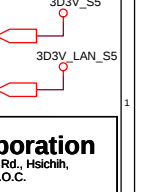
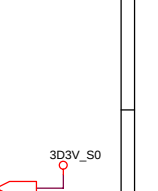
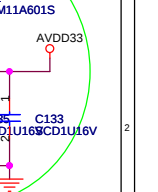
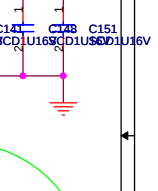
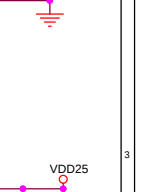
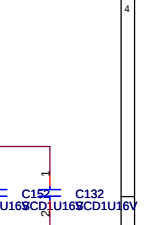
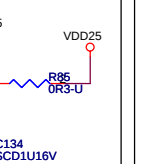
Cougar SC



Cougar SC



Cougar SC



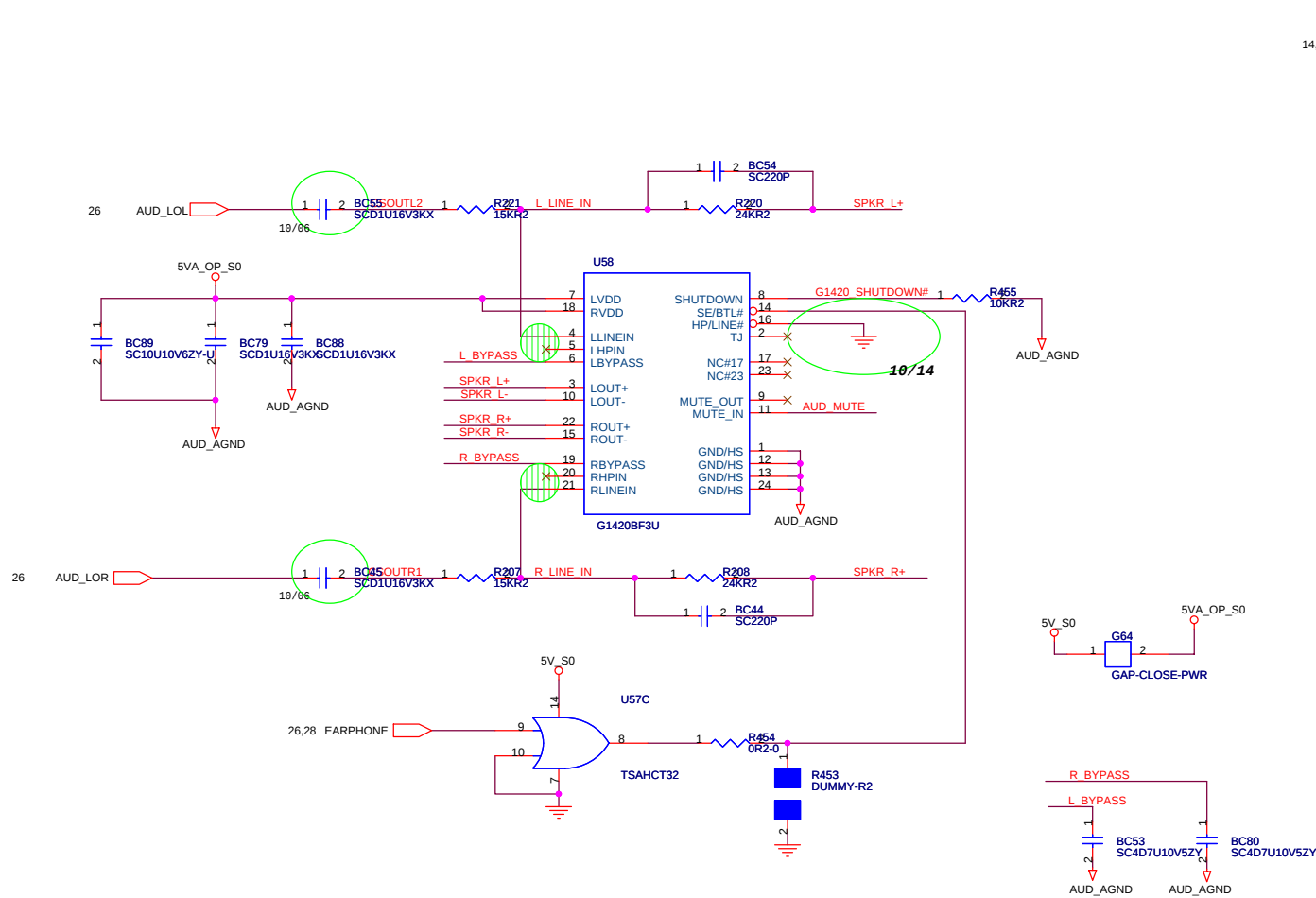
Cougar SC

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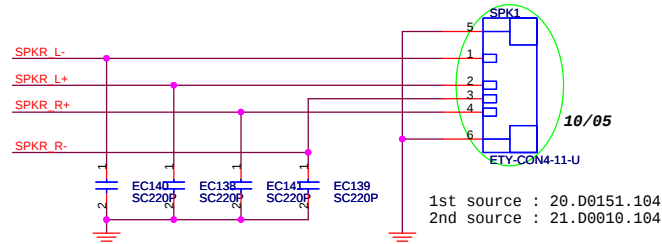
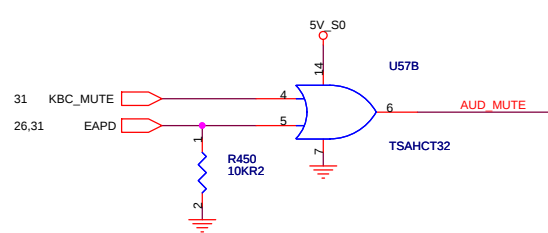
Title
LAN RTL8100C

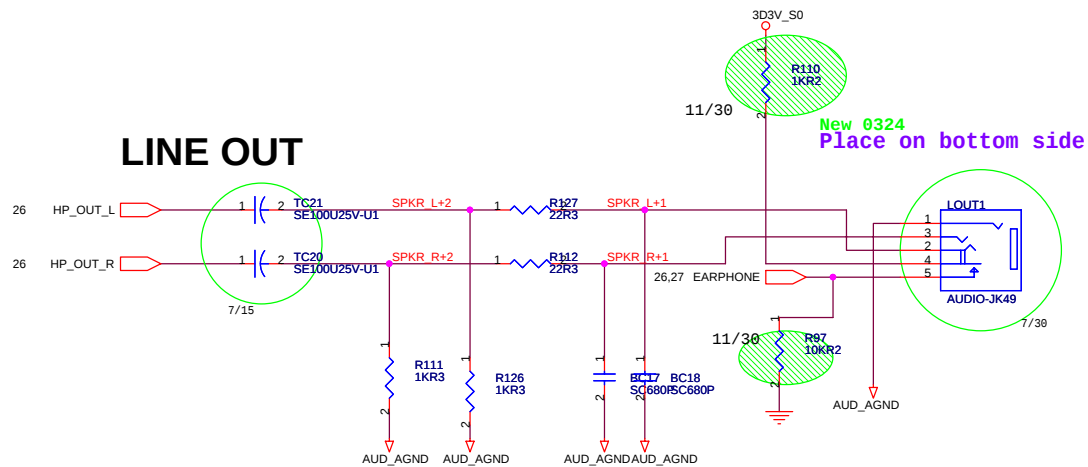
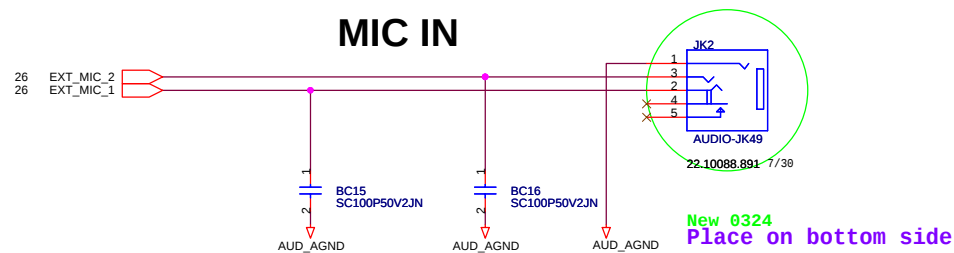
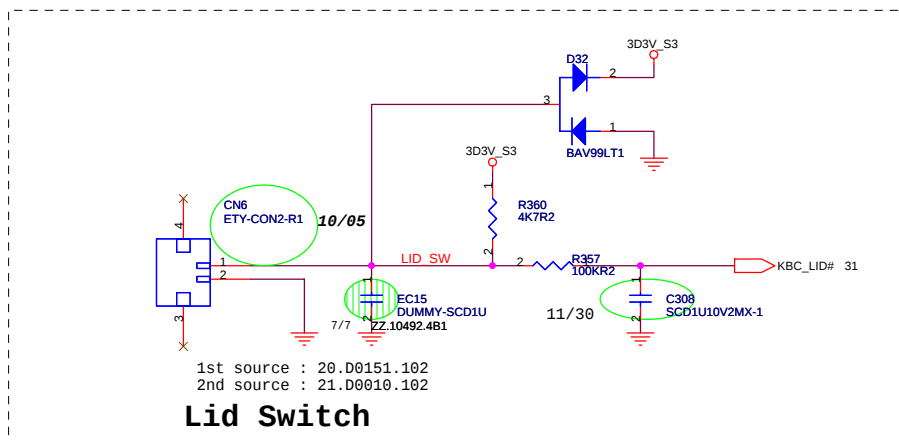
Size A3 Document Number
Leopard

Date: Thursday, December 09, 2004 Sheet 24 of 41

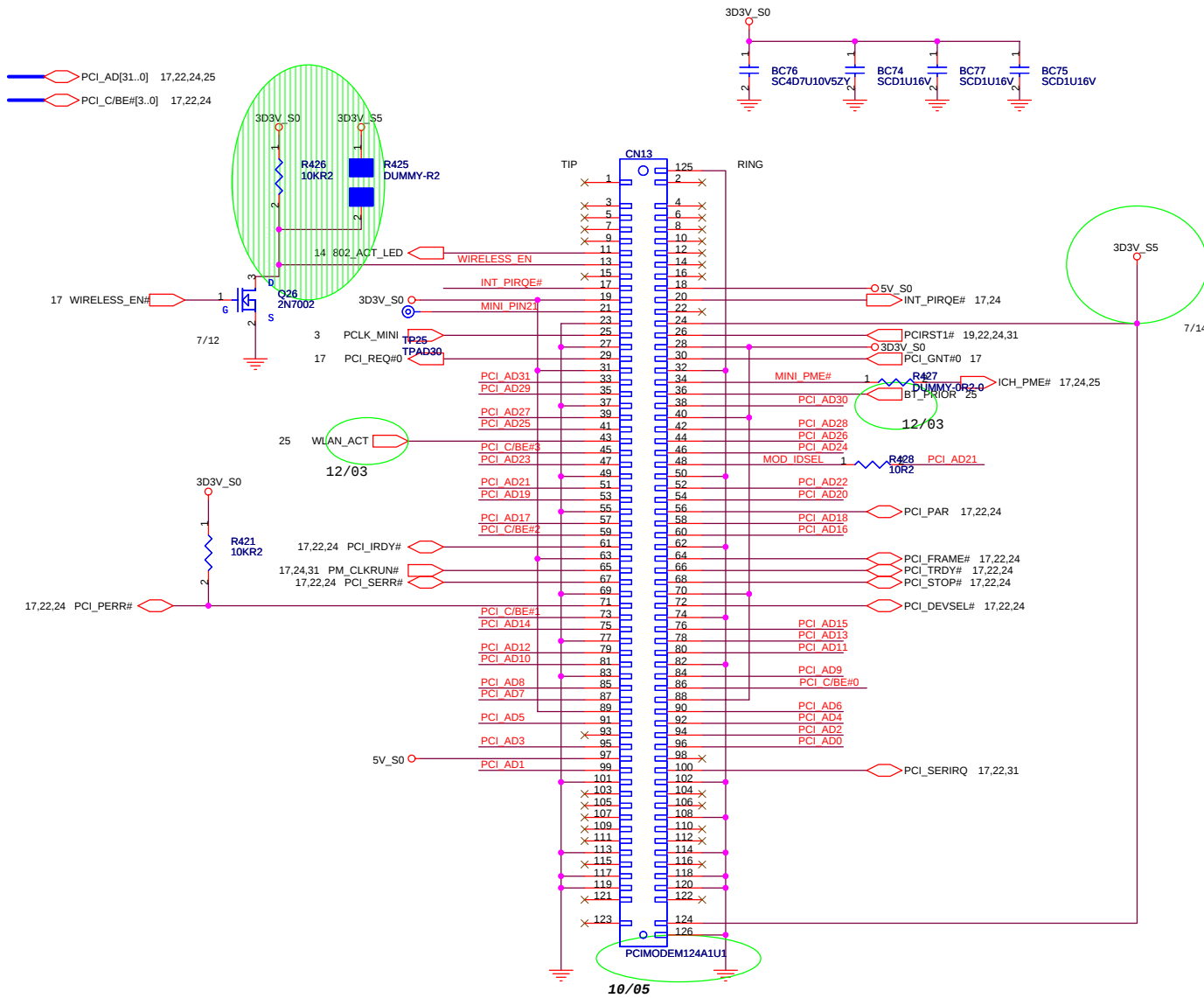


Speaker





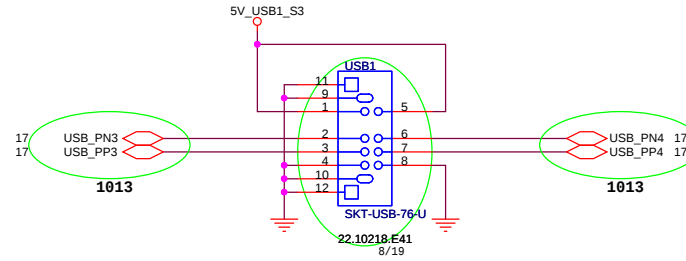
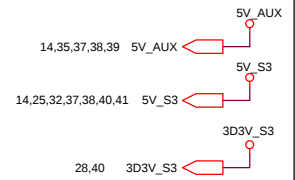
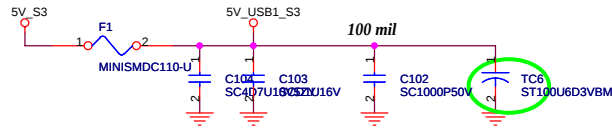
MINI-PCI



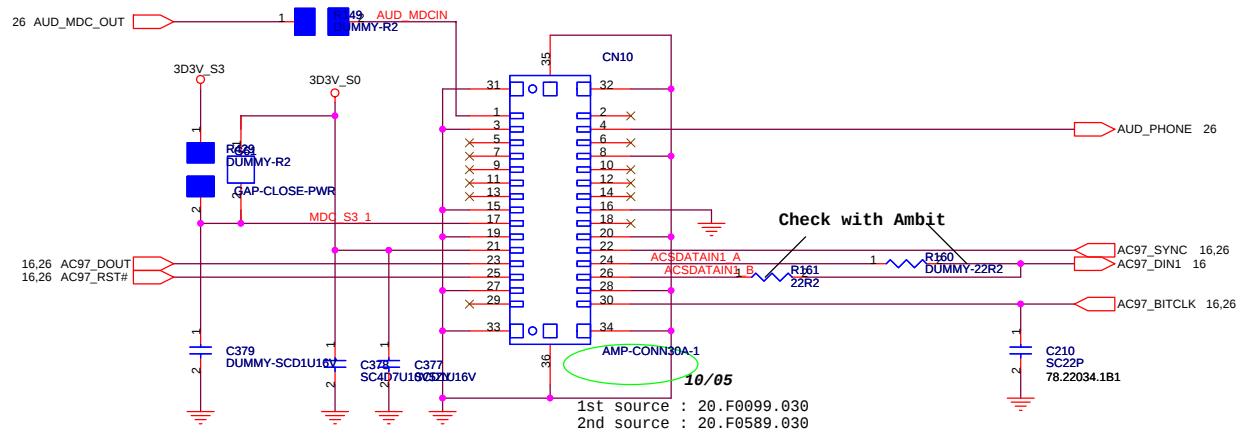
The symbol use 2nd source
The P/N is the main source
Main source:62.10032.001
2nd source:62.10032.031

3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,26,28,30,31,32,36,38,40,41 3D3V_S0
14,15,18,19,20,21,22,26,27,32,36,39,40,41 5V_S0

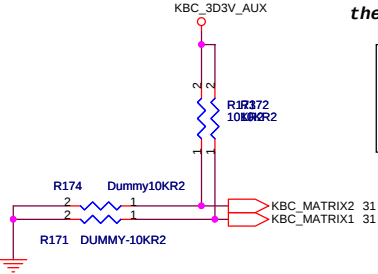
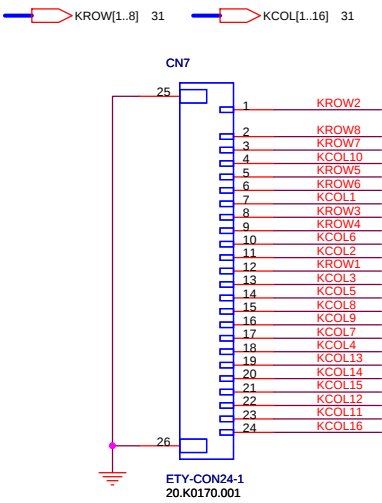
USB POWER



MDC Connector



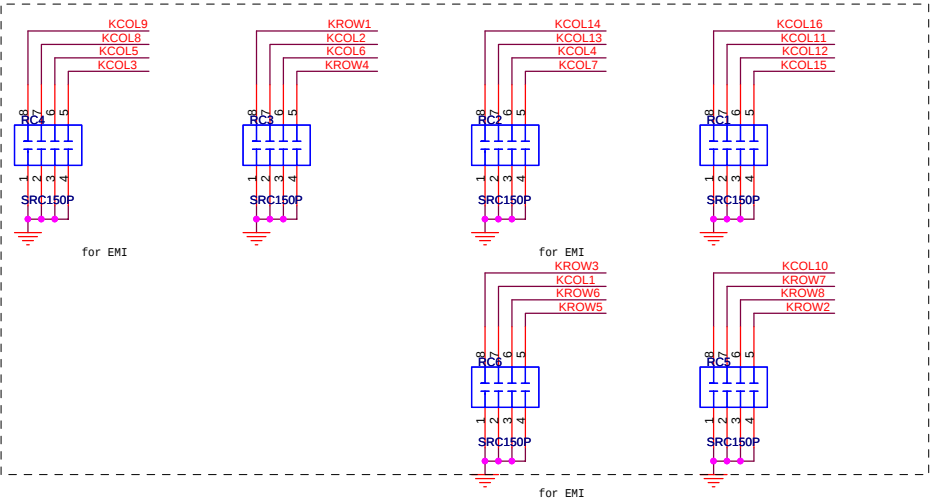
INTERNAL KEYBOARD CONNECTOR



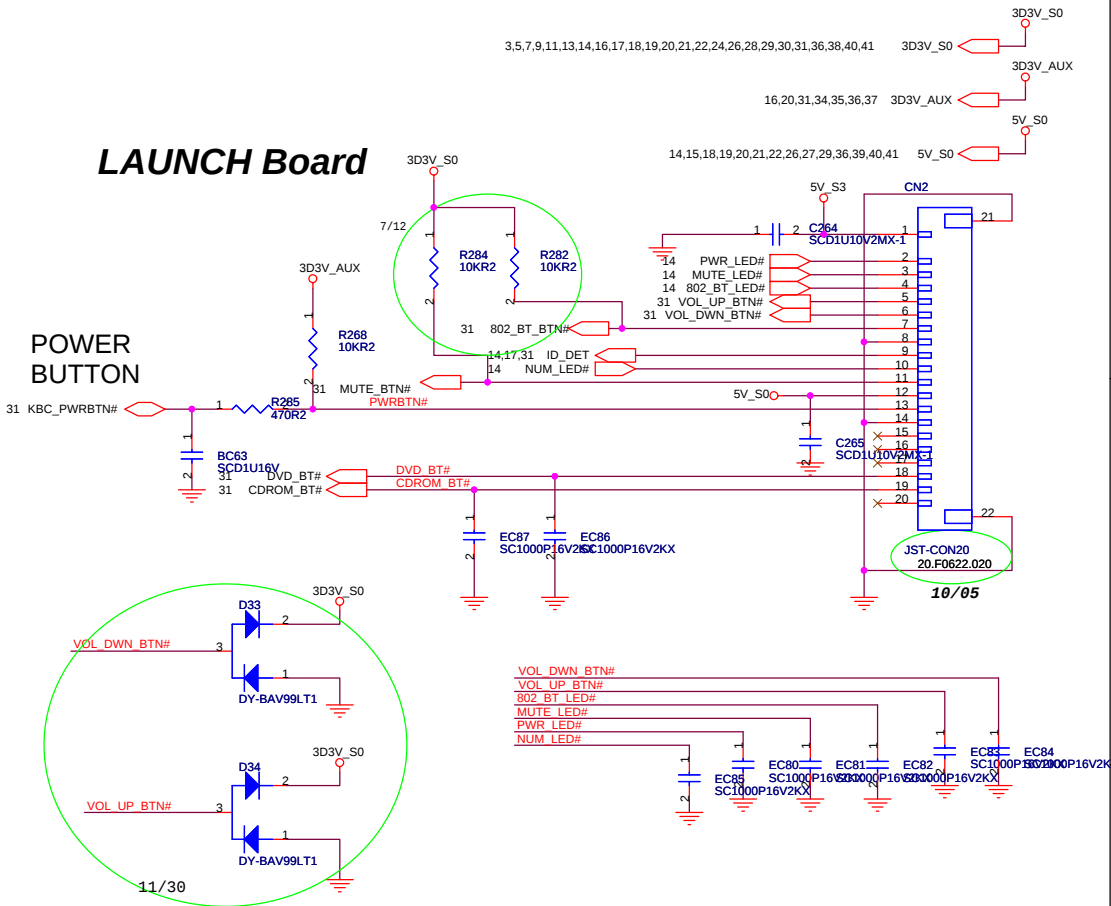
the matrix table for PCB

	PA	PR
FF	00	01
DF	10	11

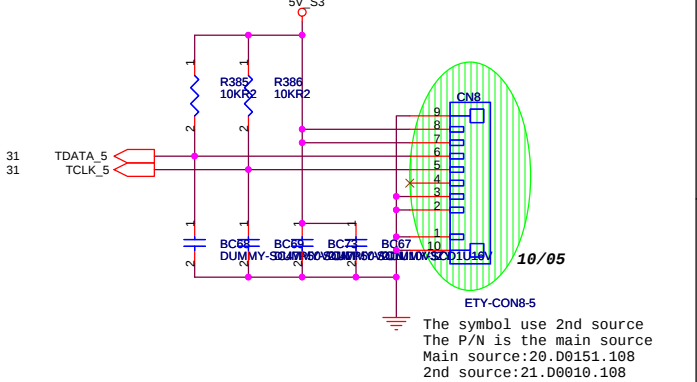
	NONE Quick Play	Quick Play
MATRIXID1#	0	1

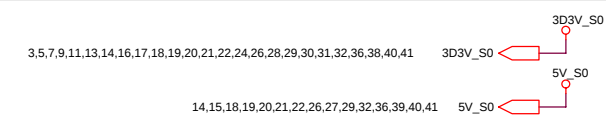
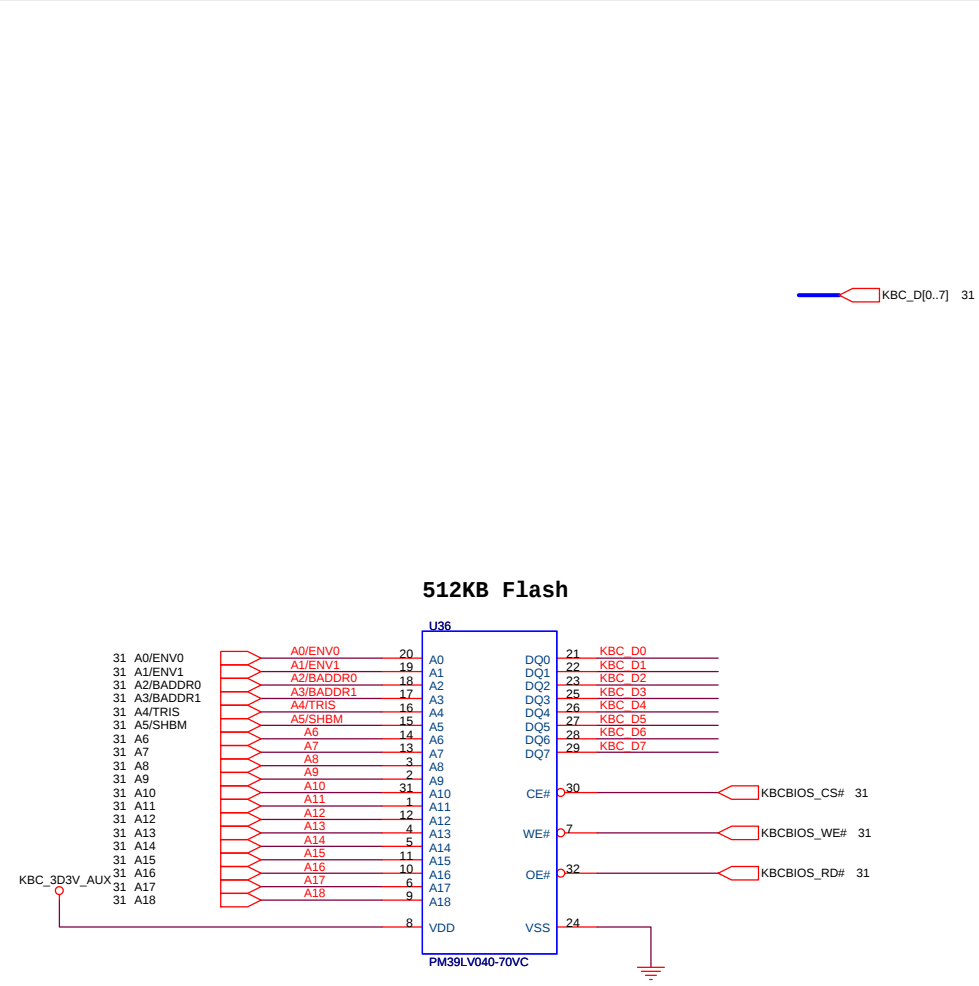


LAUNCH Board



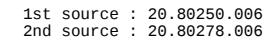
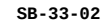
TouchPad Connector

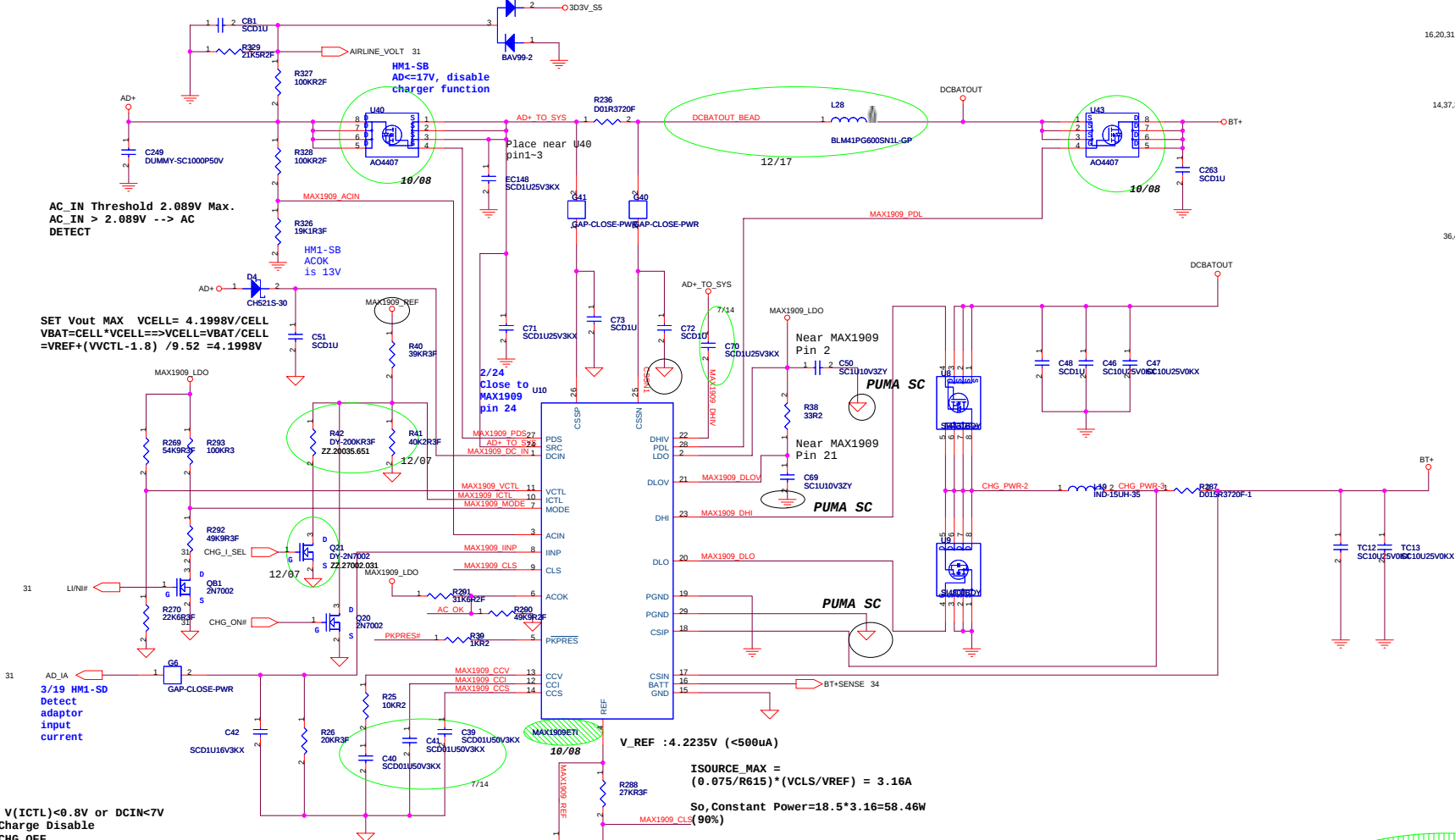




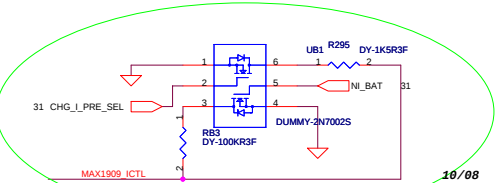
KBC_D[0..7] 31

Layout 200mil





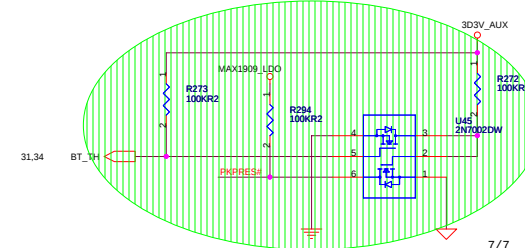
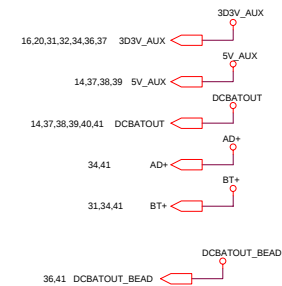
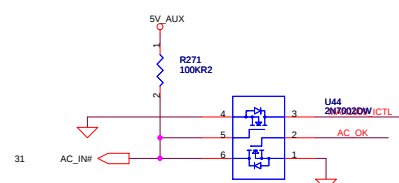
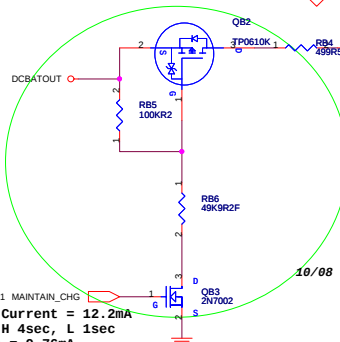
When V(ICTL)<0.8V or DCIN<7V
-->Charge Disable
SET CHG OFF
BAT_CHG_I = (0.075/R624)*(VICTL/3.6)
LI BAT :
CHG_I_SET = H(6cell),
Charge current = 3A
CHG_I_SET = L(12cell),
Charge current = 3.3A
NI-MH BAT :
NI_BAT = H,
Charge current = 2.5A
Pre-Charge (or Maintain Charge) : MAX8725
MAX1909 : Pre-Charge current = 300mA,
MAX8725 : CHG_I_PRE_SEL = H,
Pre-Charge current = 200mA
Maintain charge current = 12.5mA
==> H 4sec, L 60sec



If Charger is MAX1909, dummy them.

Maintain Charge Current = 12.2mA
MAINTAIN_CHG is H 4sec, L 1sec
So, Avg. Current = 9.76mA

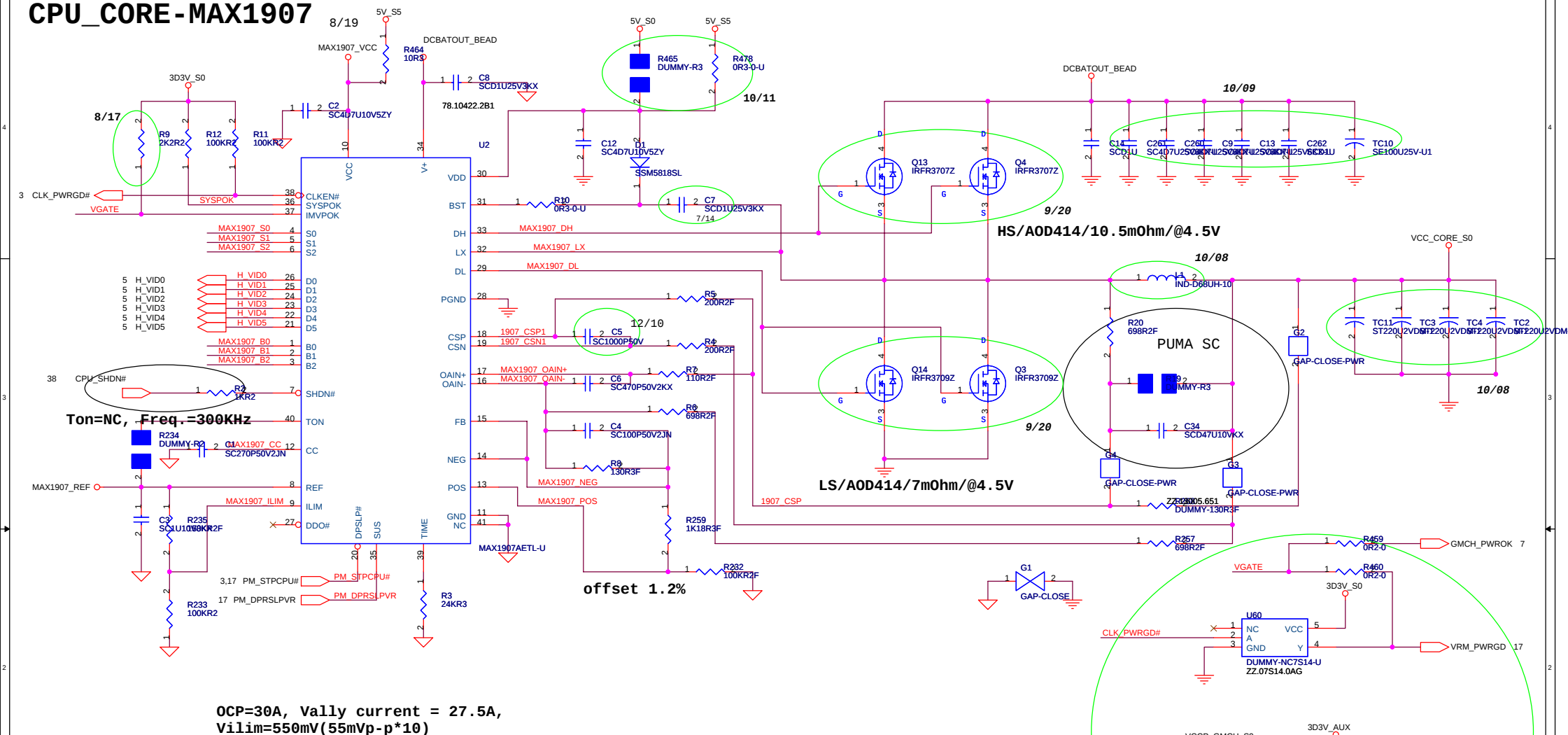
If Charger is MAX8725, dummy them.



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Taippei Hsien 221, Taiwan, R.O.C.

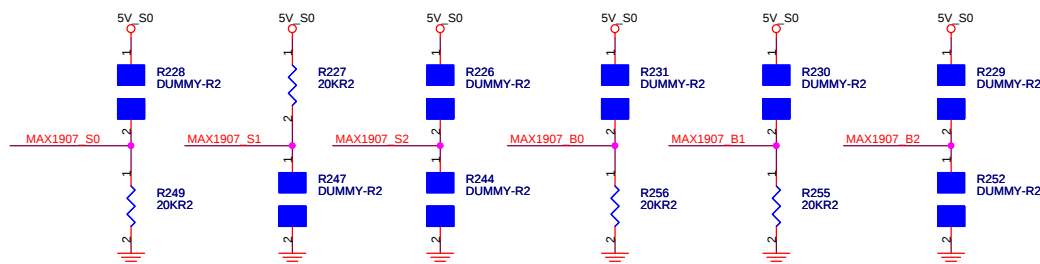
Title			CHARGER MAX8725
Size	Document Number	Leopard	
C		Rev -2	
Date:	Friday, December 17, 2004	Sheet	35 of 41

CPU_CORE-MAX1907

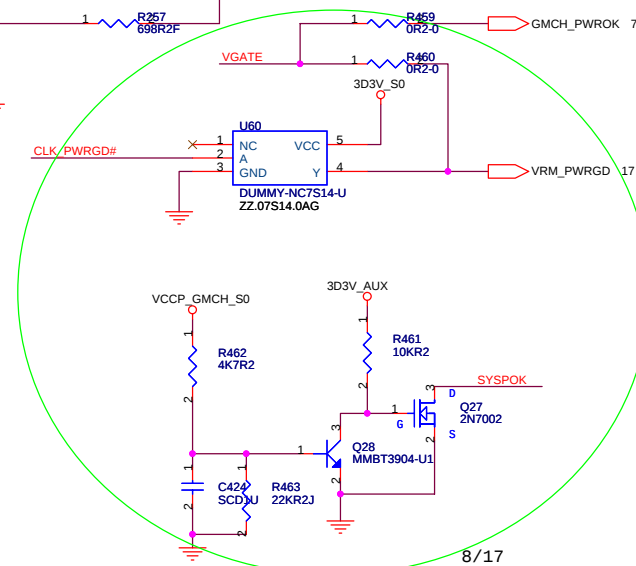


Deeper Sleep Voltage : 0.748V
, S0=L, S1=H, S2=Open,

Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.34
0	1	1	0	0	0	1.32
0	1	1	0	1	0	1.29
0	1	1	1	0	0	1.26
0	1	1	1	0	1	1.24
0	1	1	1	1	1	1.21
1	0	0	0	0	1	1.18
1	0	0	0	1	1	1.14
1	0	0	1	1	0	1.10
1	0	1	0	0	1	1.05
1	0	1	0	1	1	1.02
1	0	1	1	1	0	0.97
1	1	0	0	0	0	0.94



3,5,7,9,11,13,14,16,17,18,19,20,21,22,24,26,28,29,30,31,32,36,38,40,41 3D3V_S0 3D3V_S0

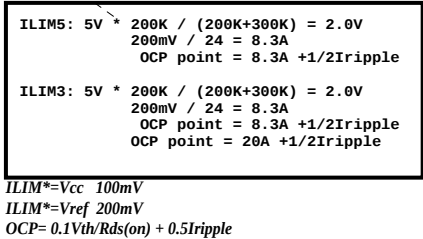
17,18,19,24,29,31,35,39,40 3D3V_S5 3D3V_S5

16,20,31,32,34,35,36 3D3V_AUX 3D3V_AUX

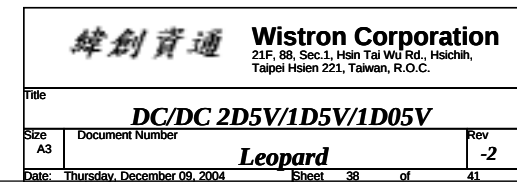
14,18,20,36,38 5V_S5 5V_S5

14,35,38,39 5V_AUX 5V_AUX

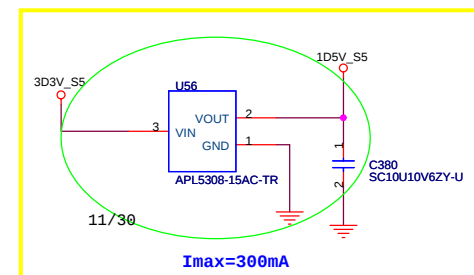
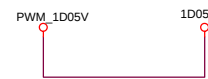
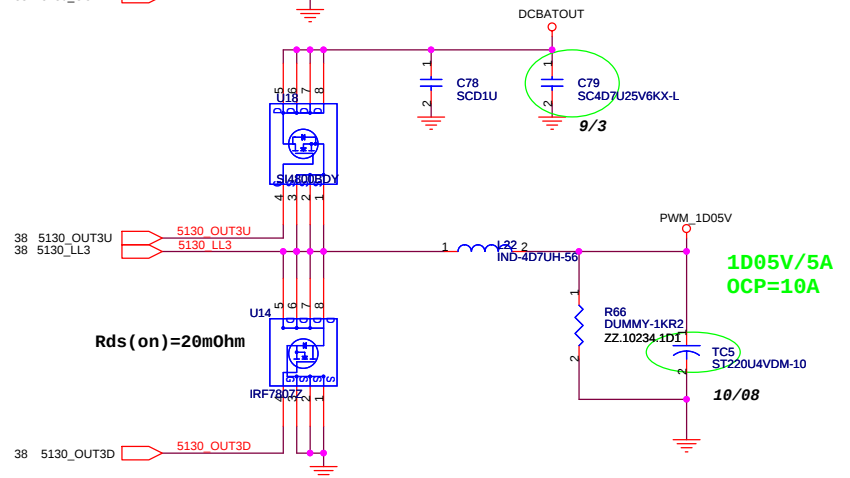
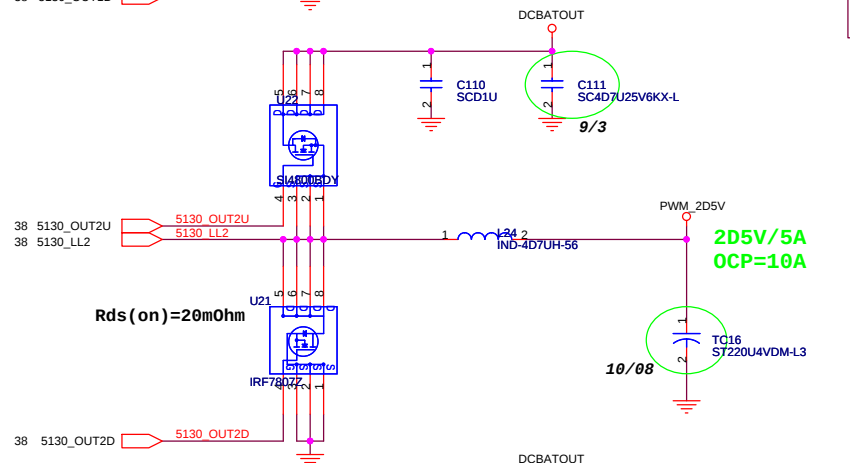
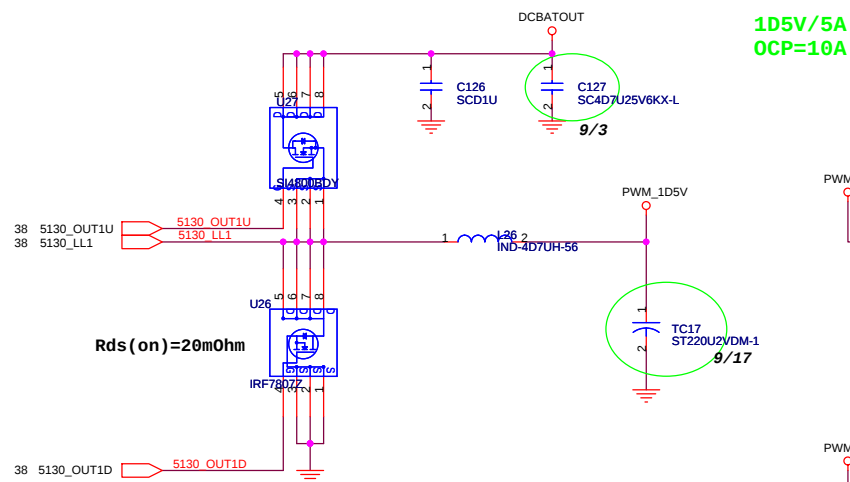
14,35,38,39,40,41 DCBATOUT DCBATOUT



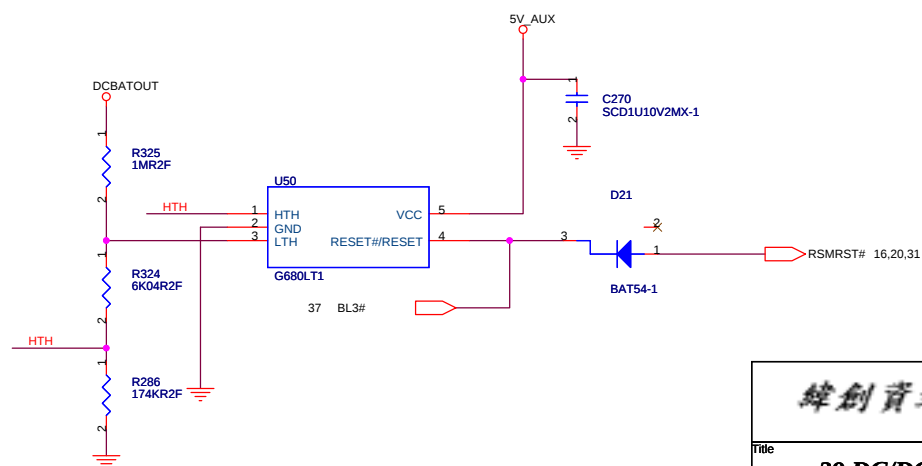
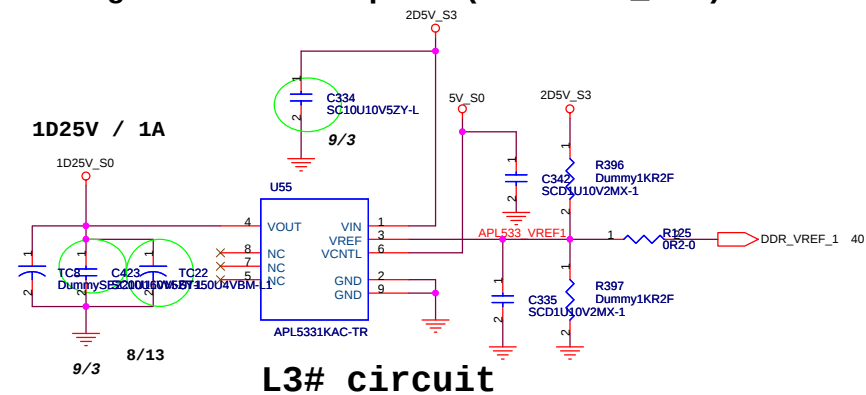
(1D5V=>CH1 , 2D5V=>CH2 , 1D05V=>CH3)



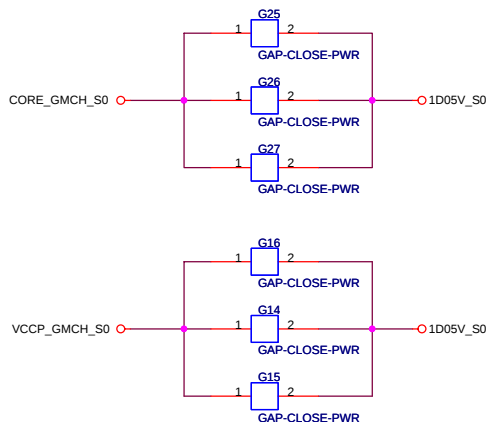
(2D5V=>CH1 , 3D3V=>CH2 , 5V =>CH3)



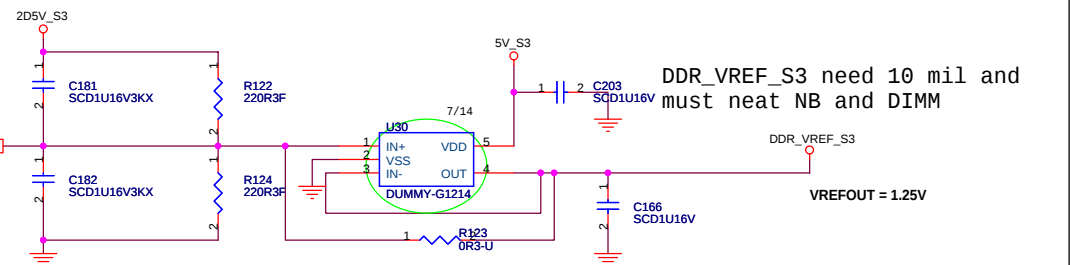
Power budget:1.25V/2.2Apeak (For DDR1_VTT)



FOR GMCH Power

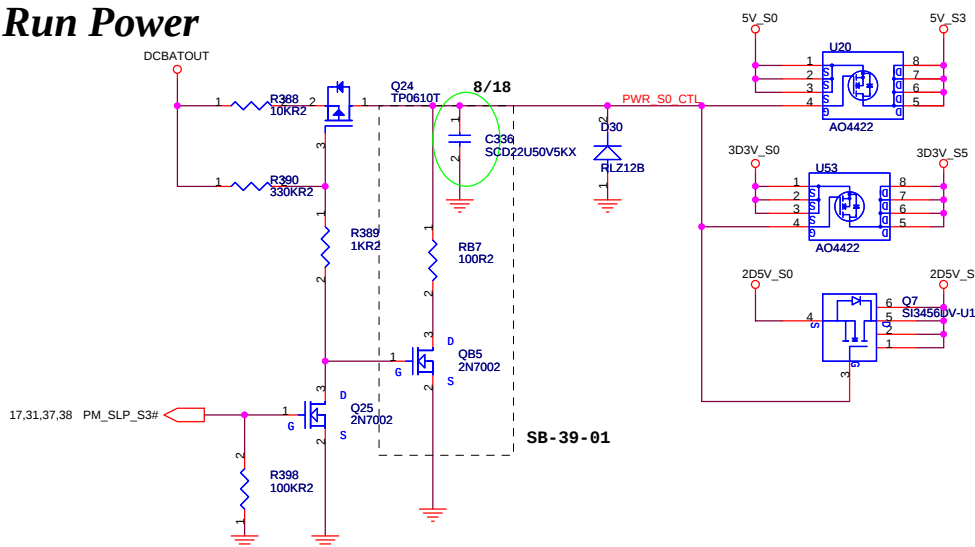


39 DDR_VREF_1

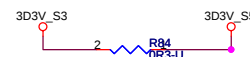


FOR DDR Power

Run Power



Suspend Power



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