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COMET DIS

SI2 BUILD

2013.02.27

21-OCT-2002		
DATE	CHANGE NO.	REV

INVENTEC					TITLE MODEL,PROJECT,FUNCTION COMET			
DRAWER	EE	DATE	POWER	DATE				
DESIGN	RAY CHEN	2013/1/8	RAY CHEN	2013/1/8				
CHECK	RAY CHEN	2013/1/8	RAY CHEN	2013/1/8				
RESPONSIBLE	RAY CHEN	2013/1/8	RAY CHEN	2013/1/8				
SIZE= A3		VER= A01			SIZE C	CODE CS	DOC NUMBER 1310XXXX-0-0	REV X01
FILE NAME: COMET DIS								
PIN 00000000000000000000								
SHEET								

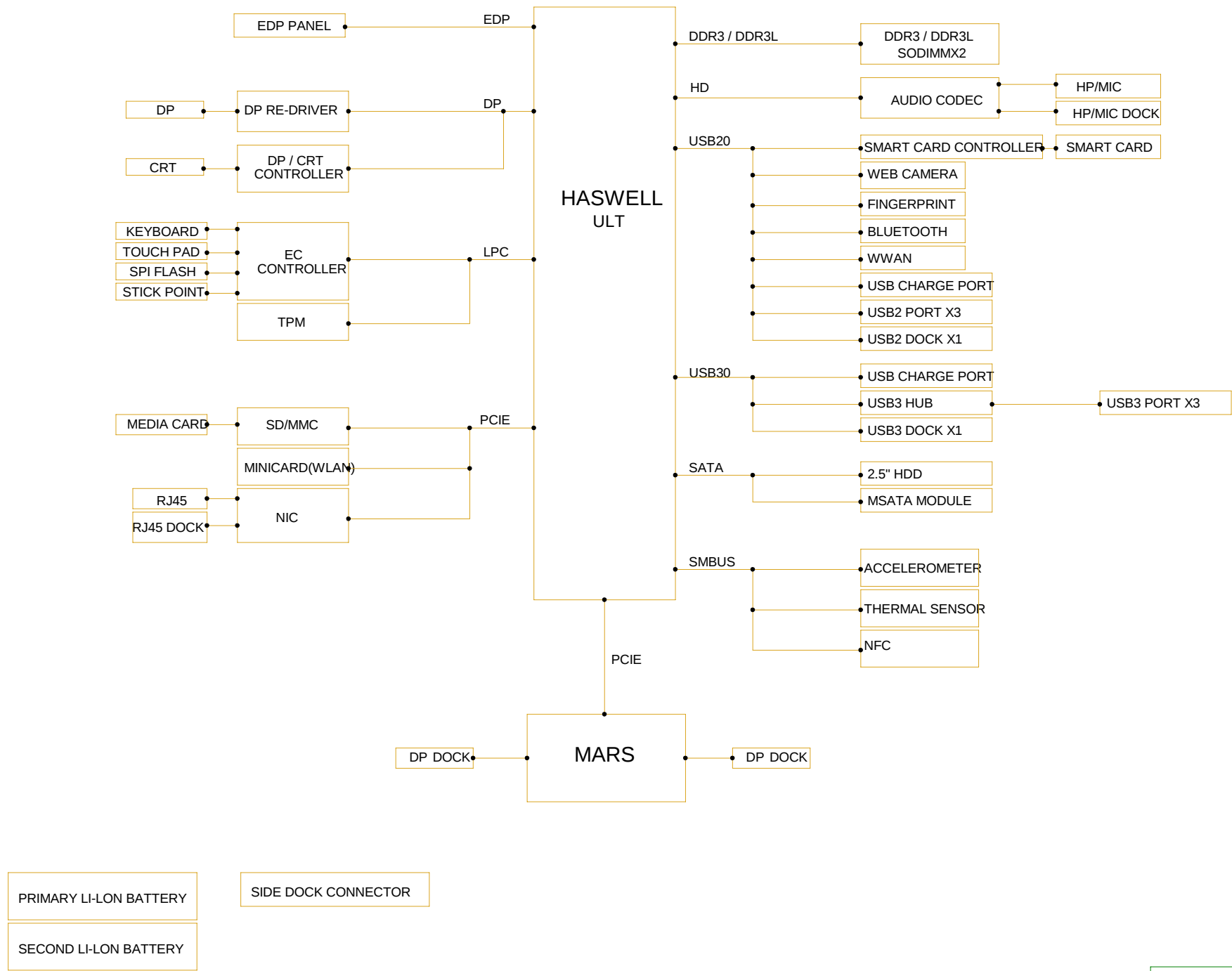
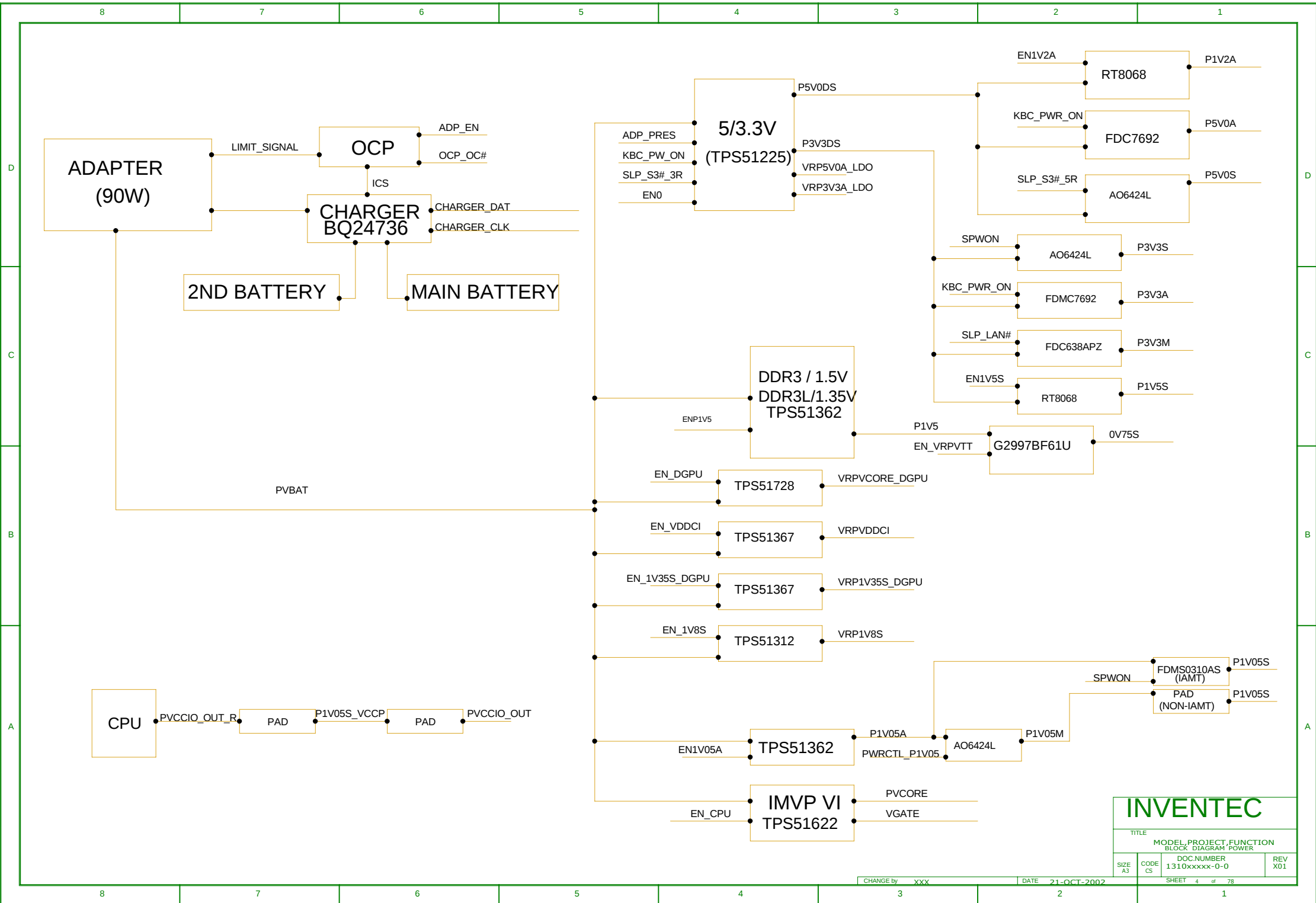
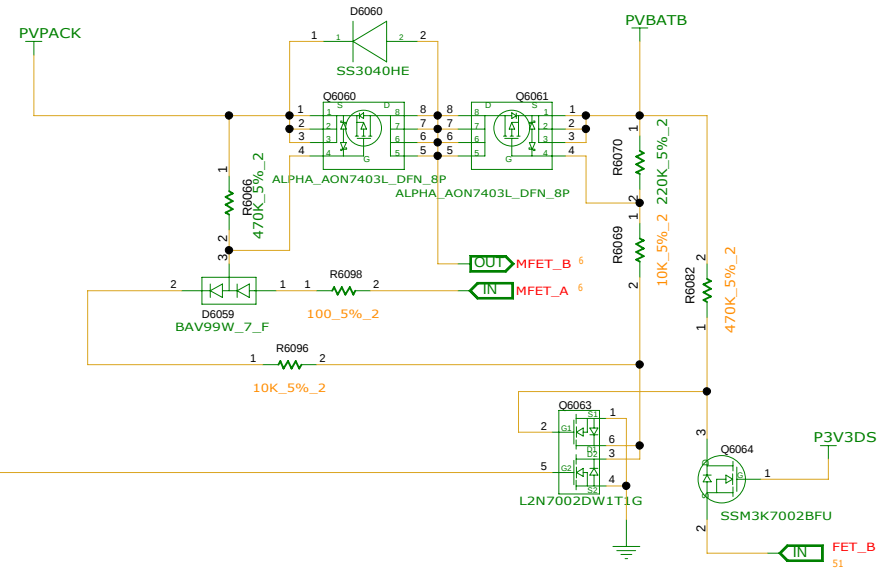
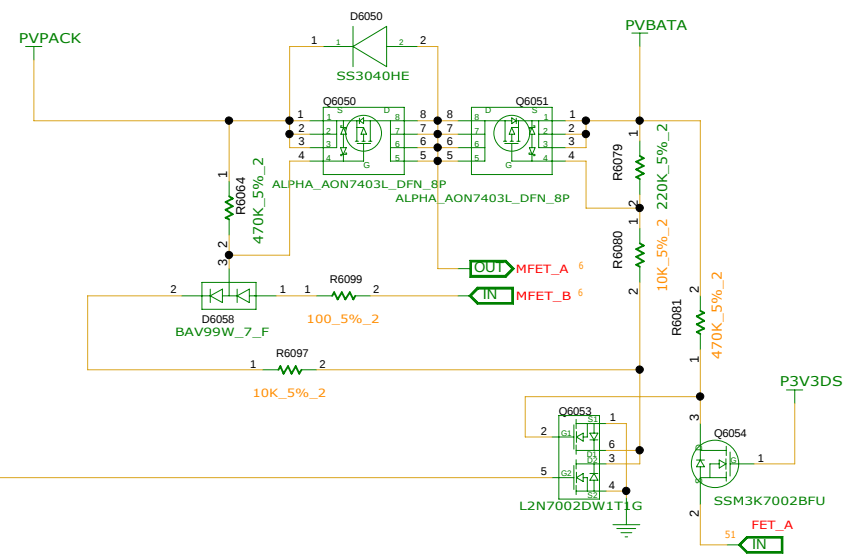
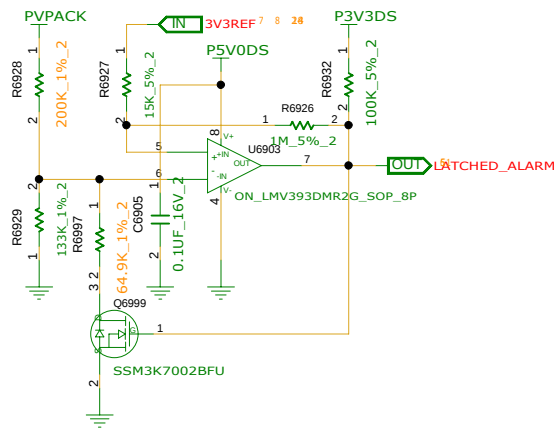


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02.BLOCK DIAGRAM	27.HASWELL_1 (MISC,JTAG)	52.KEYBOARD
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04.POWER BLOCK DIAGRAM	29.HASWELL_3 (GPIO)	54.LAN
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06.SYSTEM POWER(BATT SELECTOR)	31.HASWELL_5 (DDR)	56.WWAN SLOT, SIM SLOT
07.SYSTEM POWER(OCF)	32.HASWELL_6 (PCIE,USB)	57.DOCKING
08.SYSTEM POWER(P3V3A&P5V0A)	33.HASWELL_7 (RTC,AUDIO,SATA,JTAG)	58.B TO B CONN, POINT STICK CONN
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17.DC JACK & BATTERT CONN.	42.DP TO VGA CONVERTER	67.EMPTY
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19.PVCORE_DGPU	44.LCM & WEBCAM CONN	69.MARS-2
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25.FAN & THERMAL	50.ACCELEMETER	75.MARS-8
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		77.VRAM-2

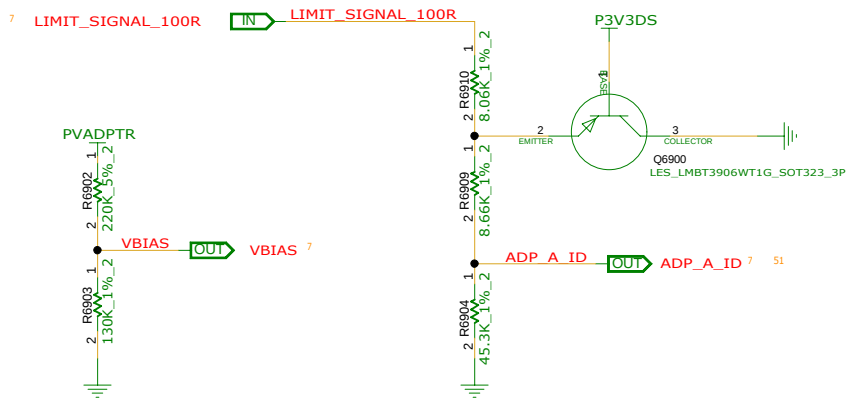
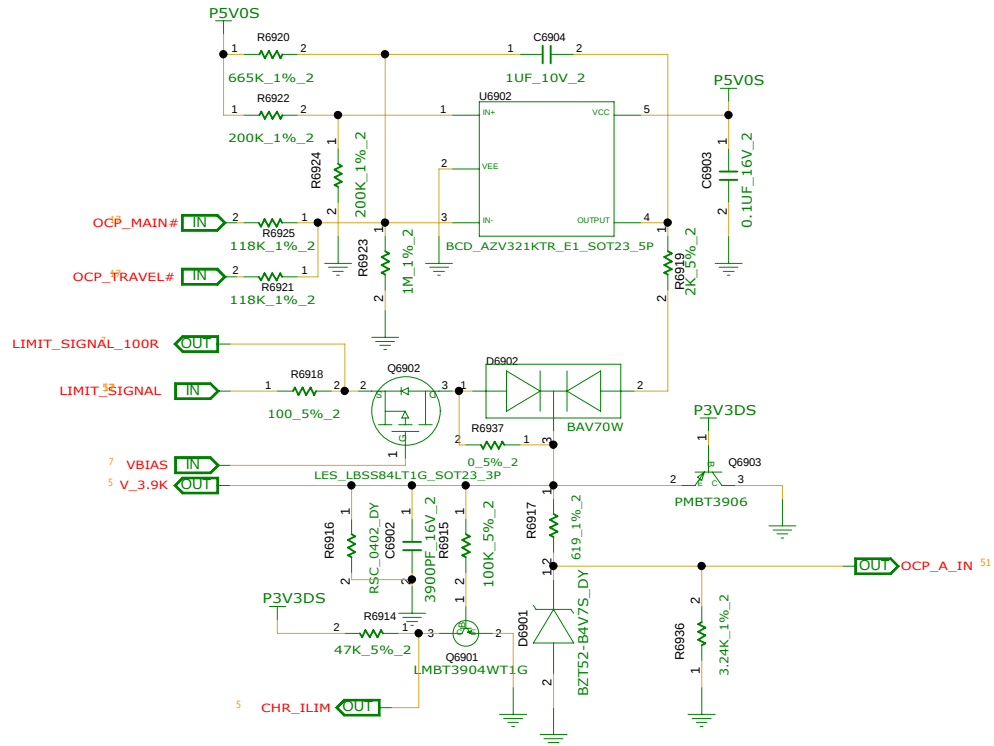
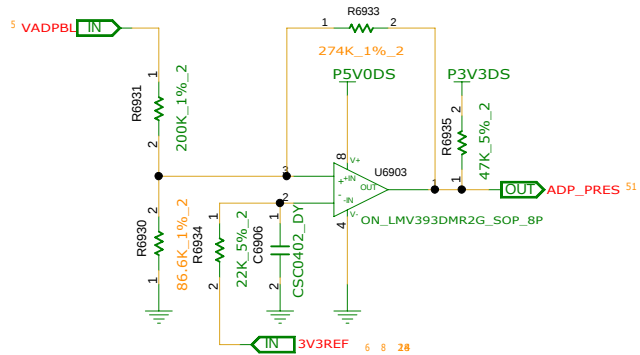
INVENTEC			
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MODEL,PROJECT,FUNCTION			
TABLE OF CONTENTS			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
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LATCHED_ALARM OUT

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
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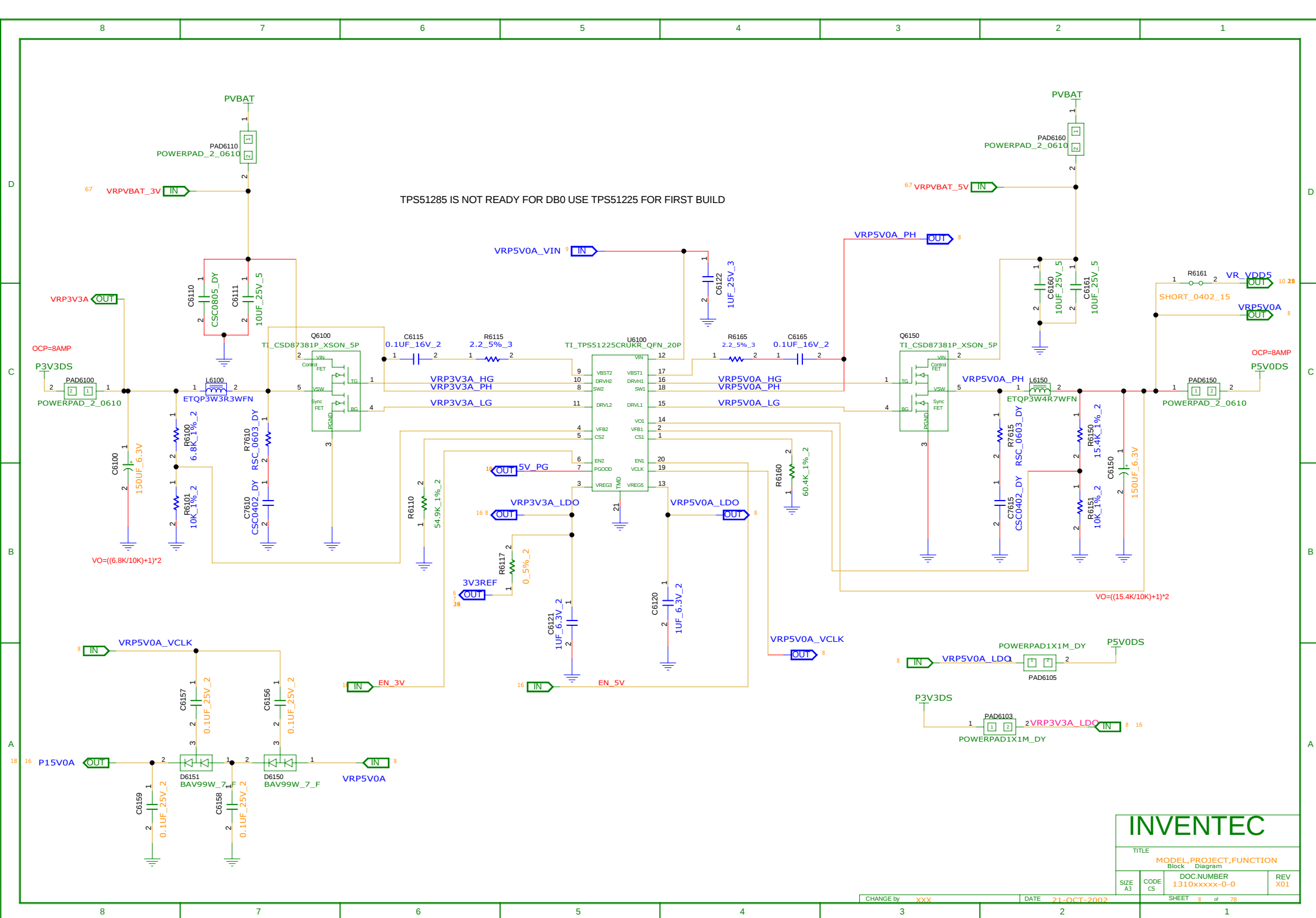
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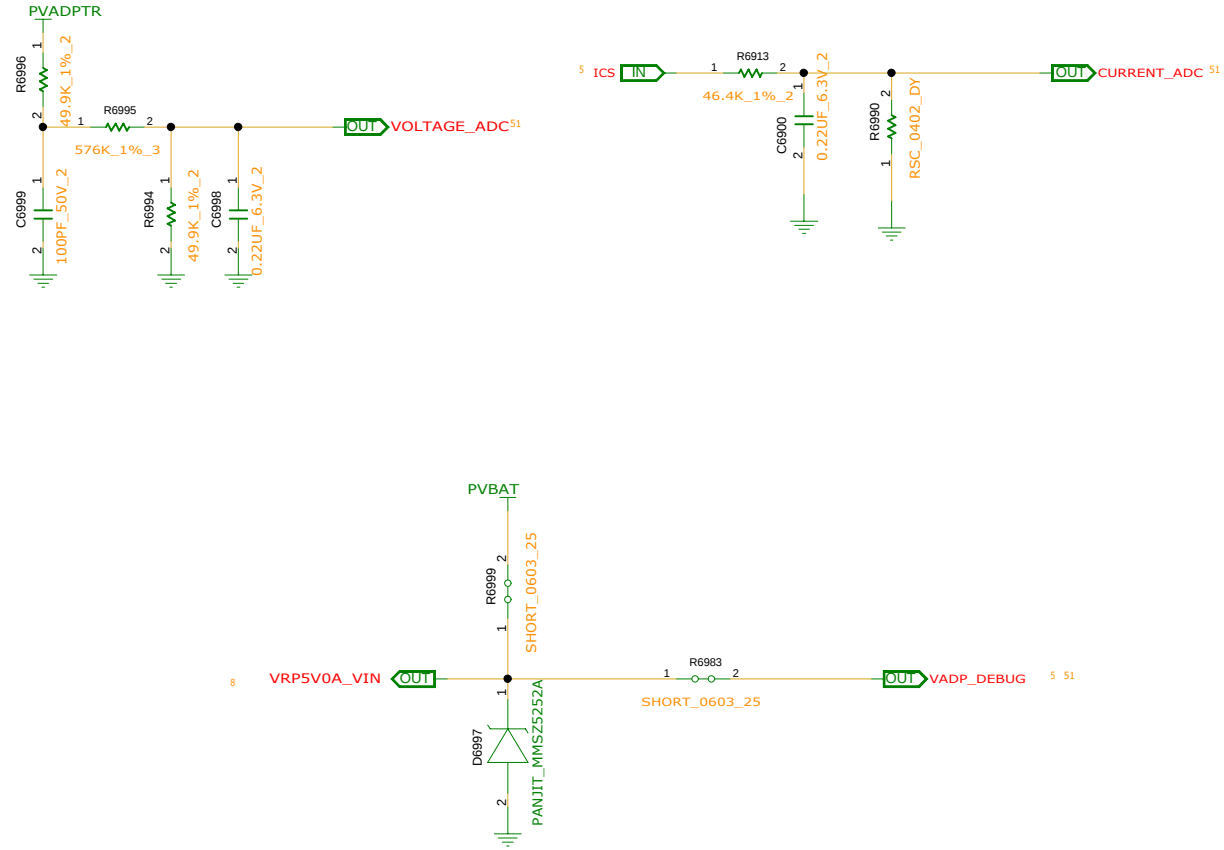
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MODEL,PROJECT,FUNCTION
Block Diagram

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CHANGE by XXX DATE 21-OCT-2002

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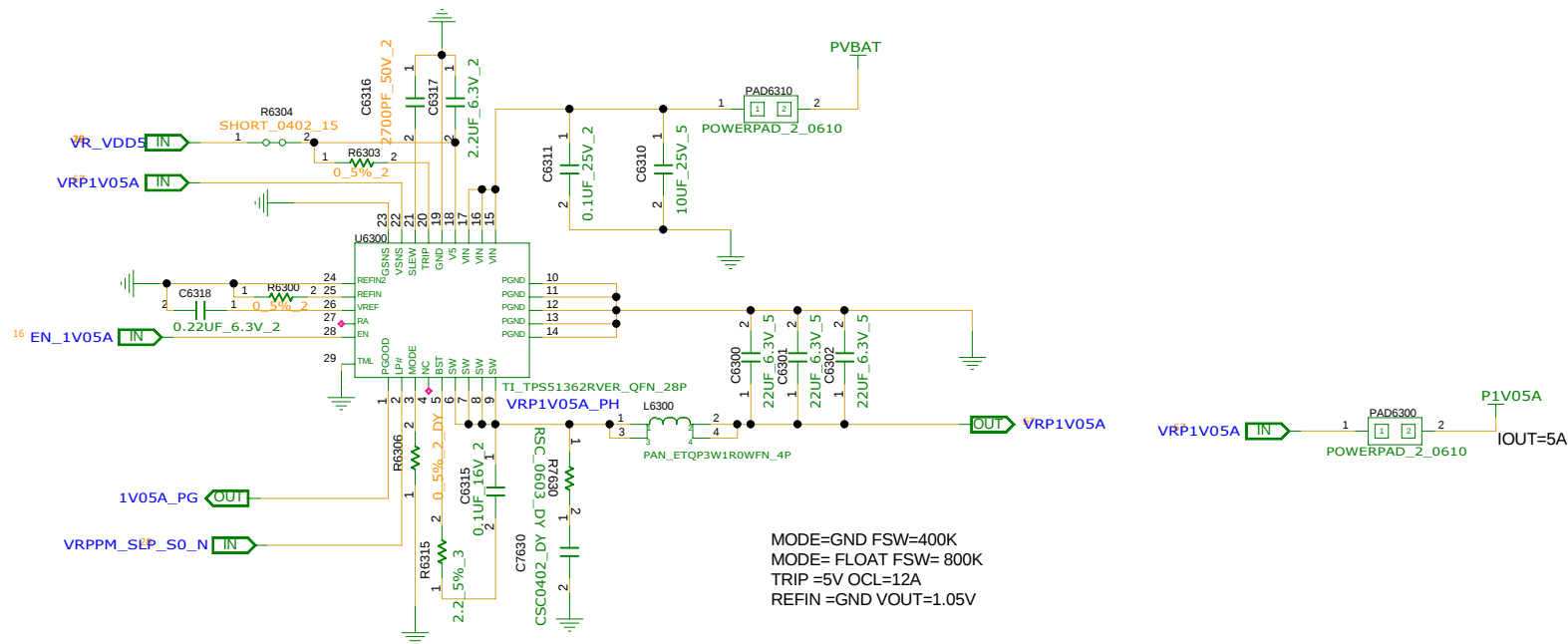


INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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INVENTEC

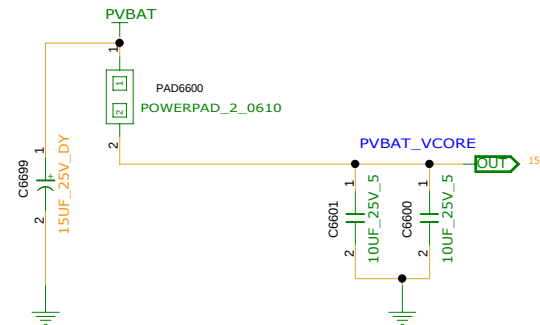
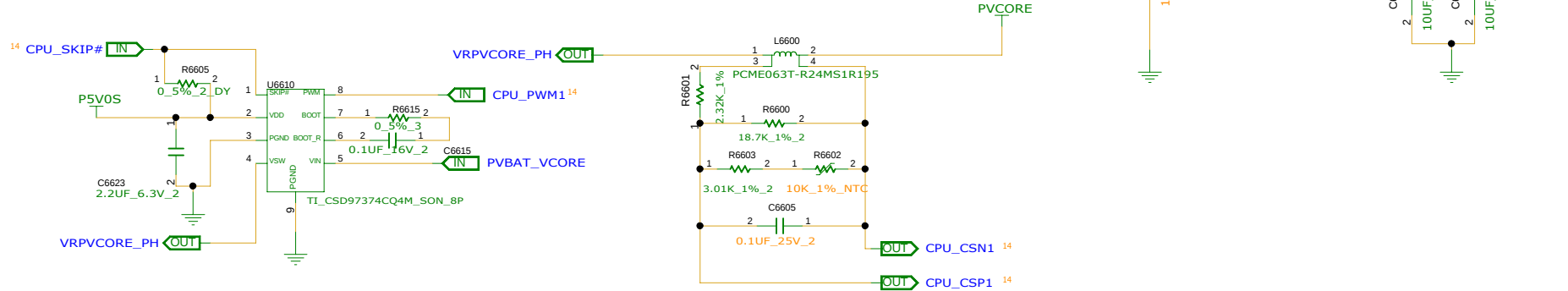
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MODEL,PROJECT,FUNCTION
Block Diagram

DOC NUMBER
1310xxxxx-0-0

REV
X01

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INVENTEC

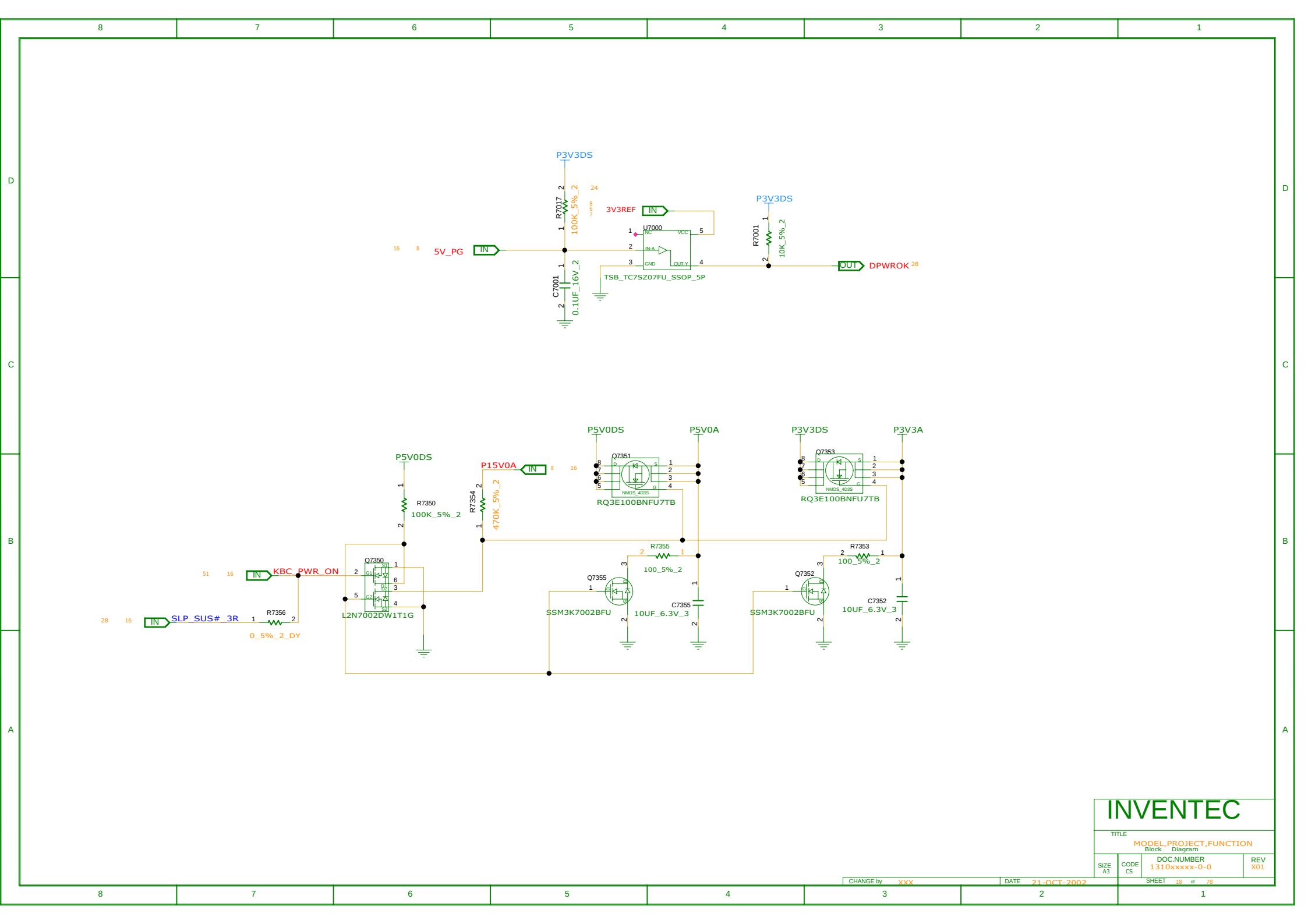
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE CODE DOC NUMBER REV
A3 CS 1310xxxxx-0-0 X01

[illegible]

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01



INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

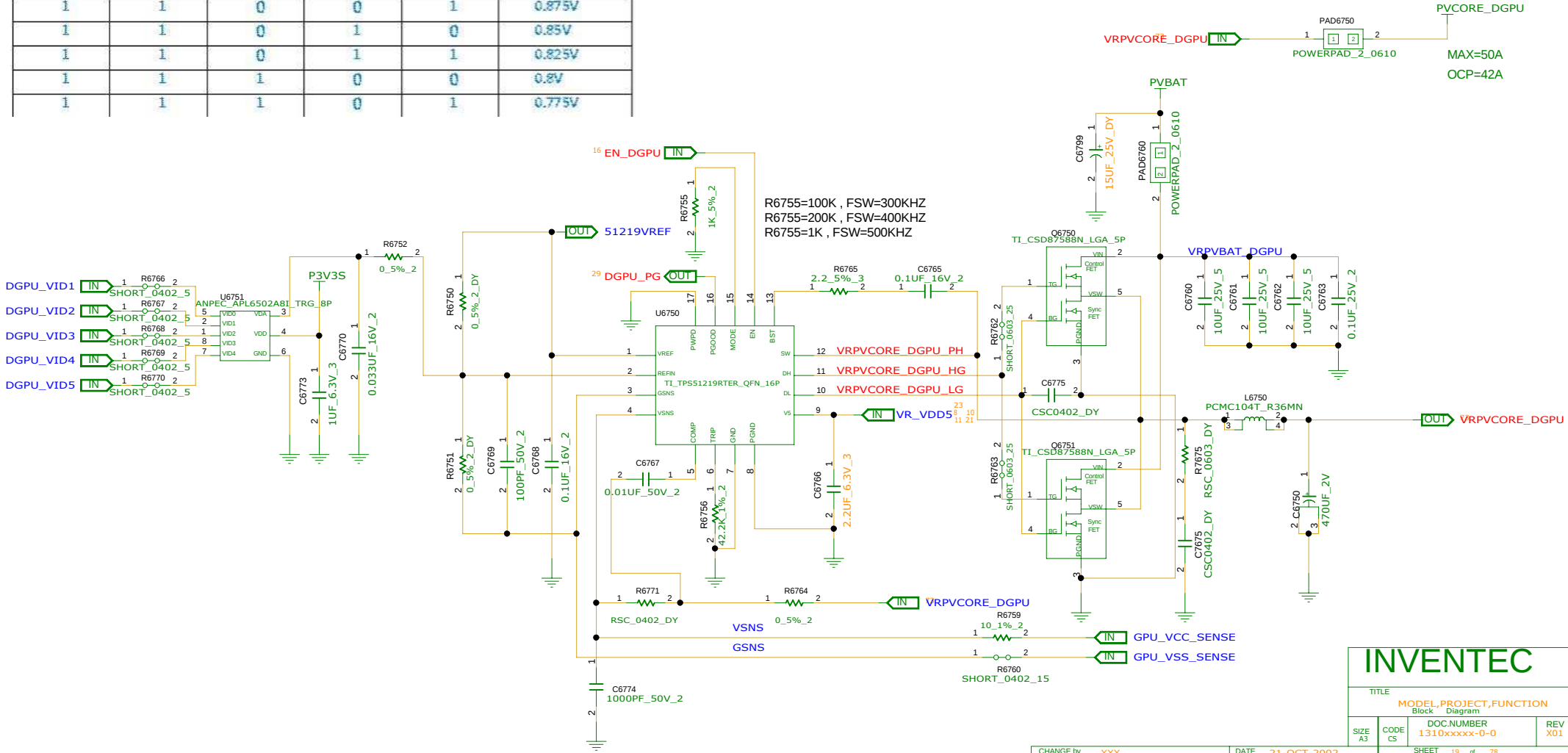
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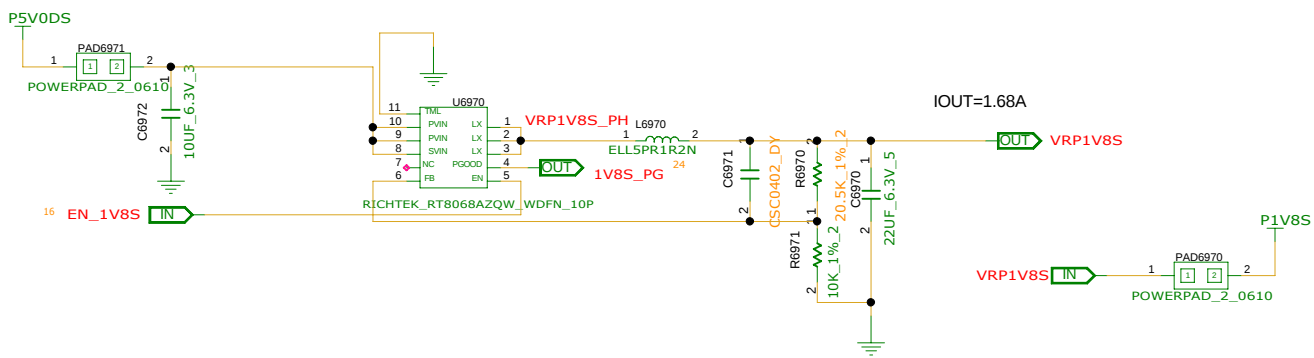
GPU_VID5 GPIO_10	GPU_VID4 GPIO_14	GPU_VID3 GPIO_15	GPU_VID2 GPIO_16	GPU_VID1 GPIO_20	Core Voltage Level
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1.0V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V

	C6762	C6752	L6750	Q6751	R6756
17W	OPEN	OPEN	ETQP4LR36AFM 6014B0164501	OPEN	80.6K_1% 6013A0072901
25W	install	install	PCMC104T-R36MN 6014B0024003	install	42.2K_1% 6013A0017701



INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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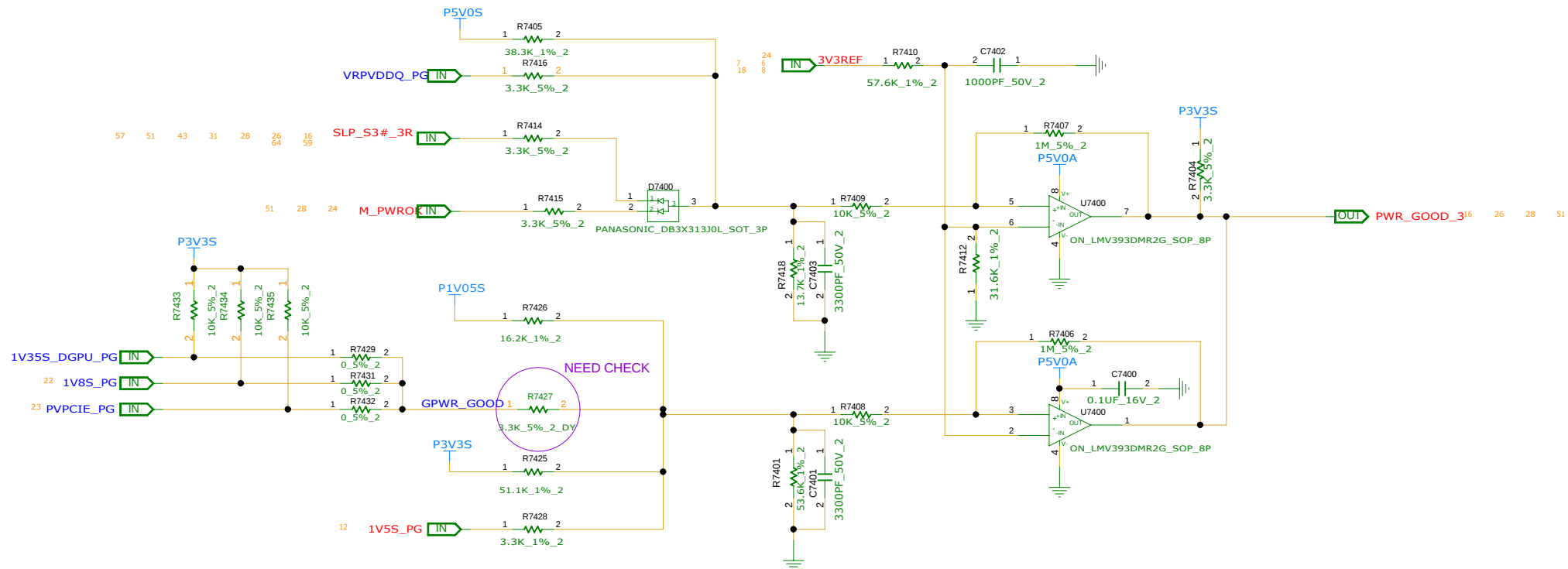
EMPTY



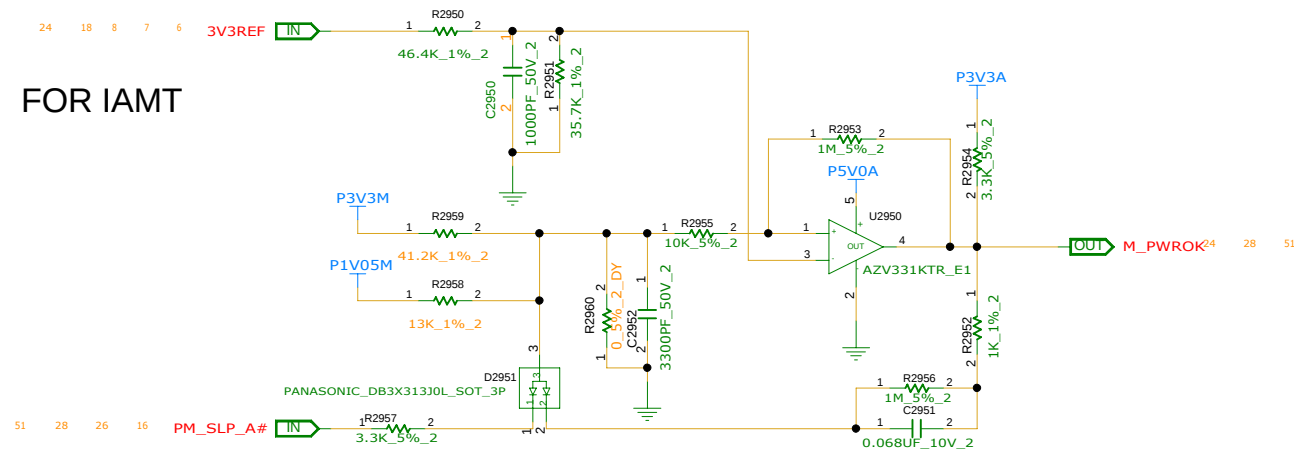
VREF=0.6V
15K=1.5V
10K=1.2V
20.5K=1.83V
MODE= FLOAT=SKIP MODE
MODE=VIN=FCCM MODE

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
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REFERENCE NUMER : 7400~7450



FOR IAMT



REFERENCE NUMER : 2950~2999

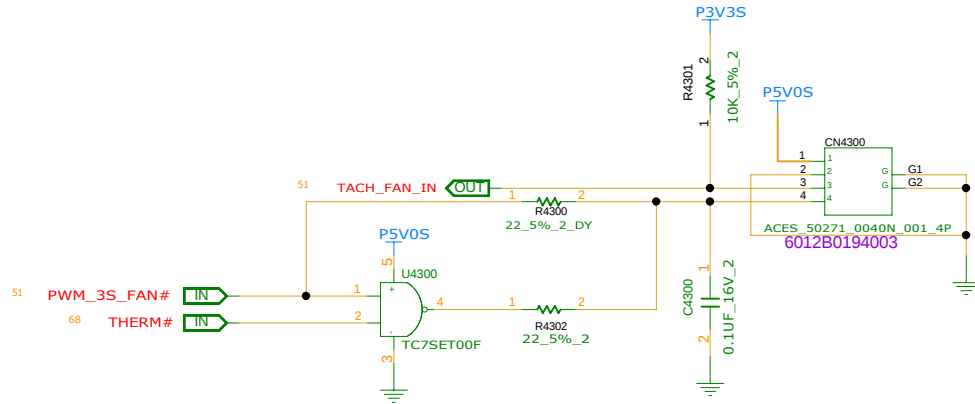
INVENTEC

TITLE			
MODEL PROJECT FUNCTION POWER (SEQUENCE)			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01

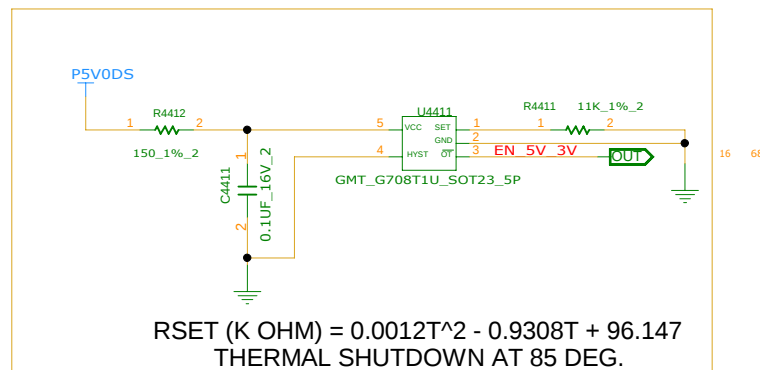
CHANGE by XXX DATE 21-OCT-2002

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REFERENCE NUMBER:4400~4349



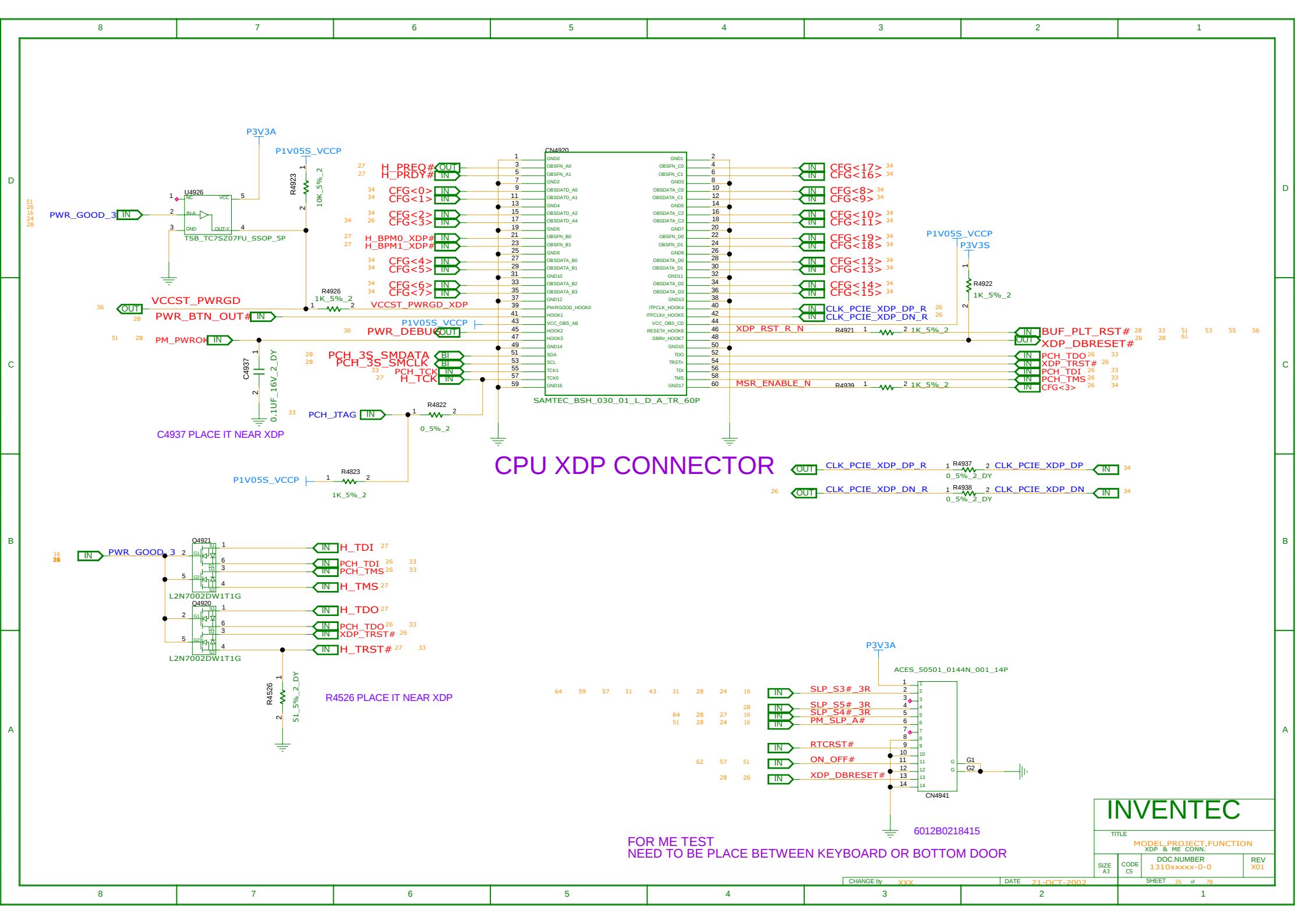
AMBIENT TEMP SENSE
WILL BE NOT USED IN 2013?

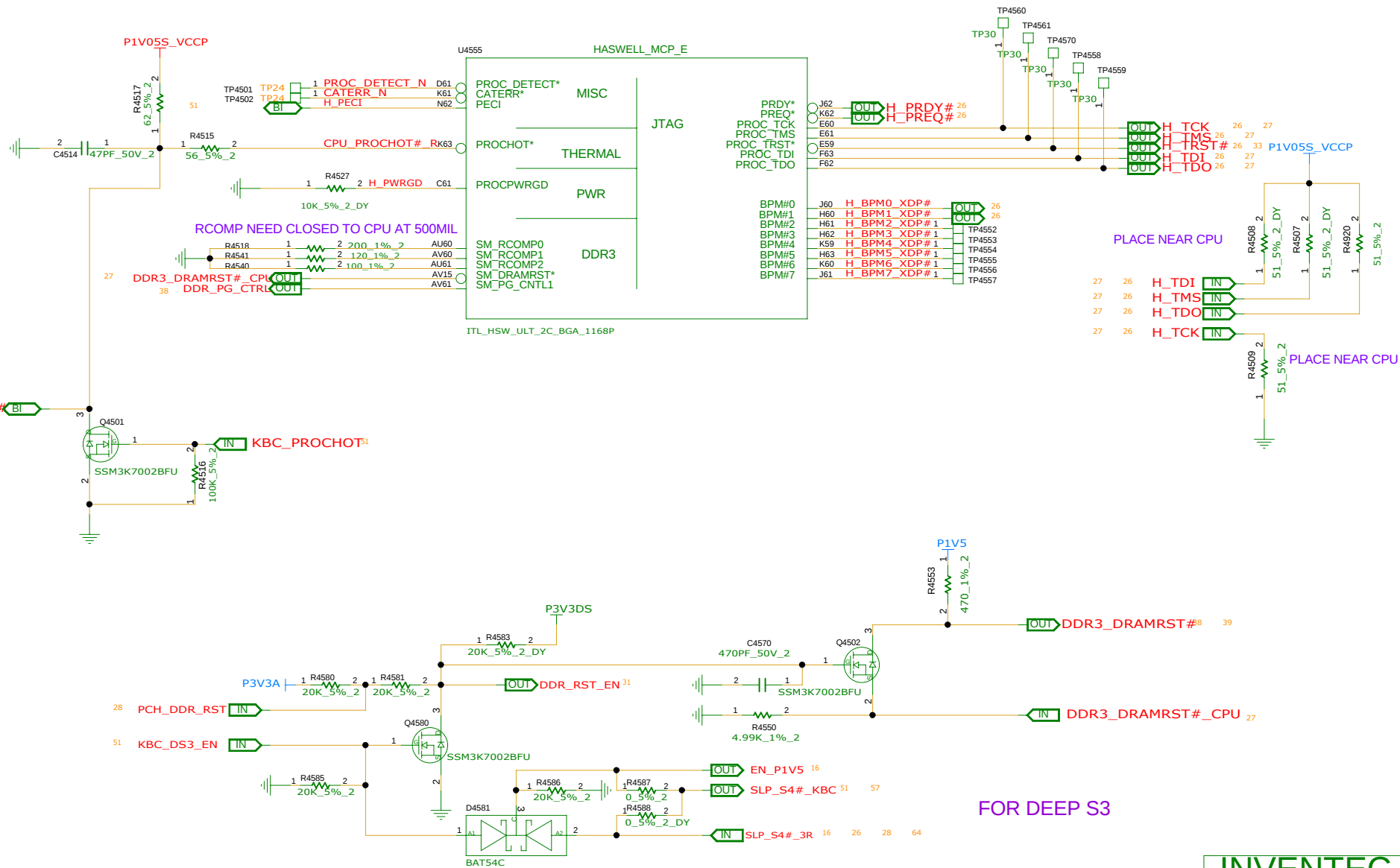


REFERENCE NUMBER:4411~4449

INVENTEC

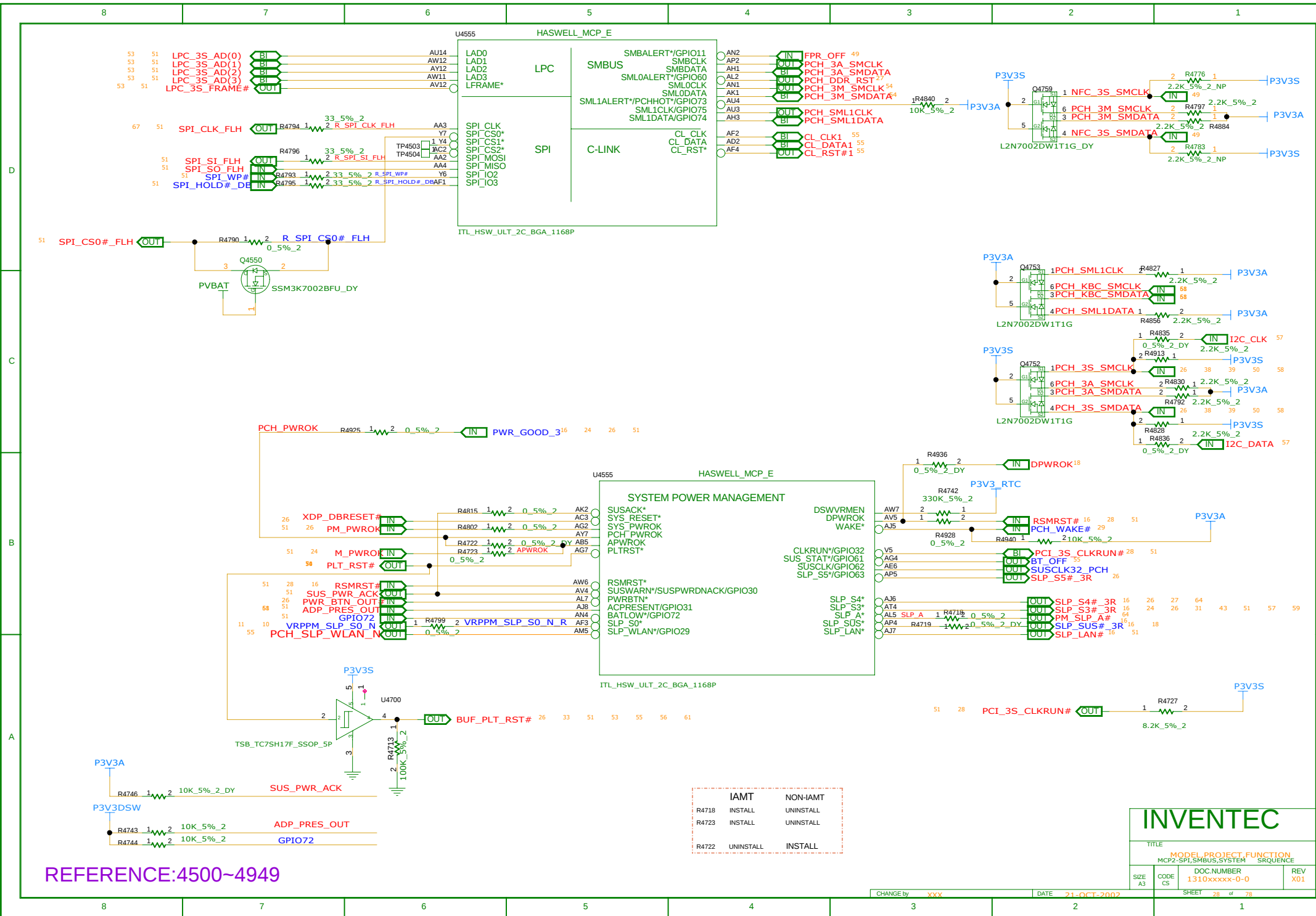
TITLE			
MODEL PROJECT,FUNCTION			
FAN & THERMAL			
SIZE	CODE	DOC NUMBER	REV
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REFERENCE:4500~4949

INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
MCP1-MISC			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by		DATE	SHEET
XXX		21-OCT-2002	27 of 78

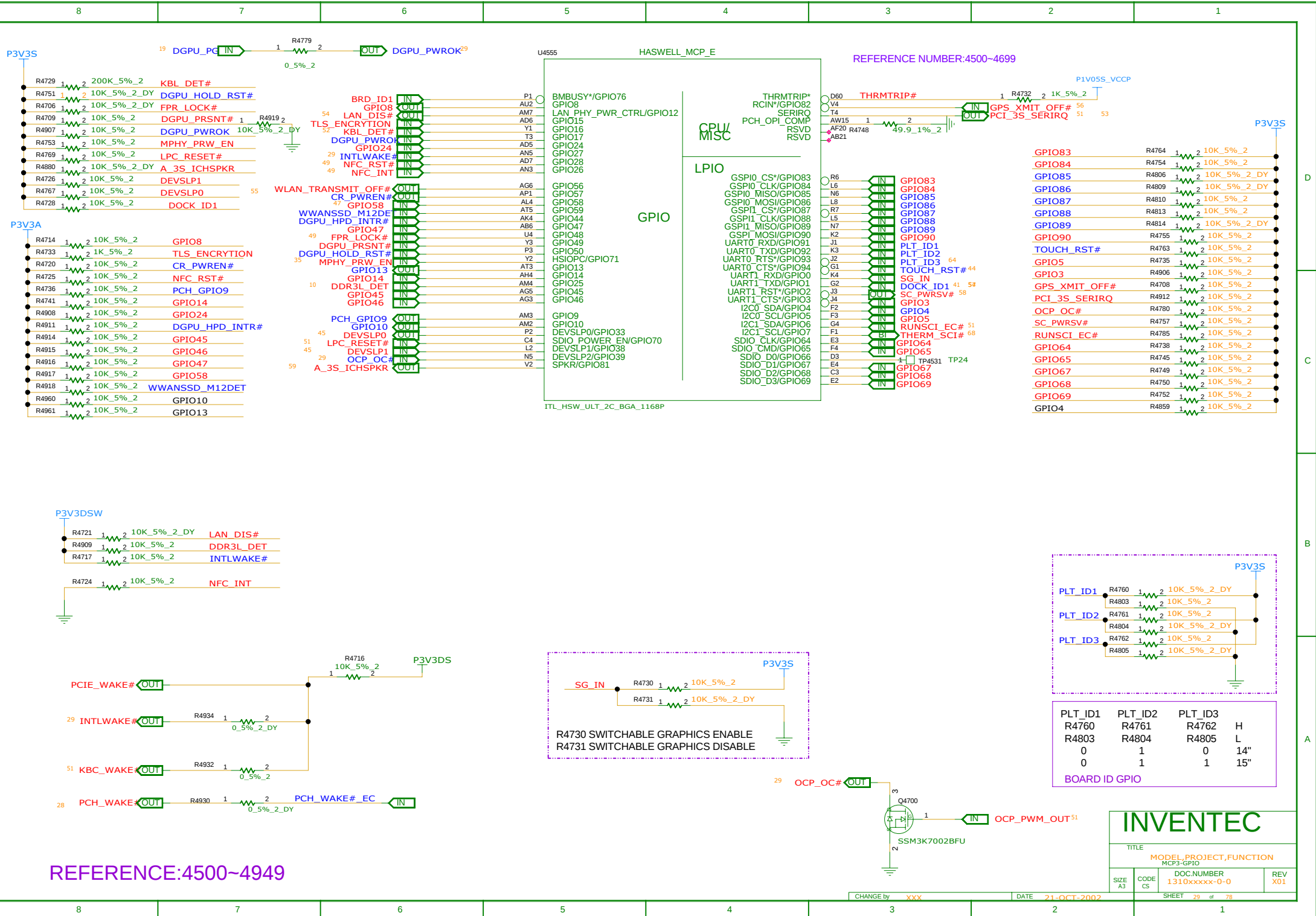


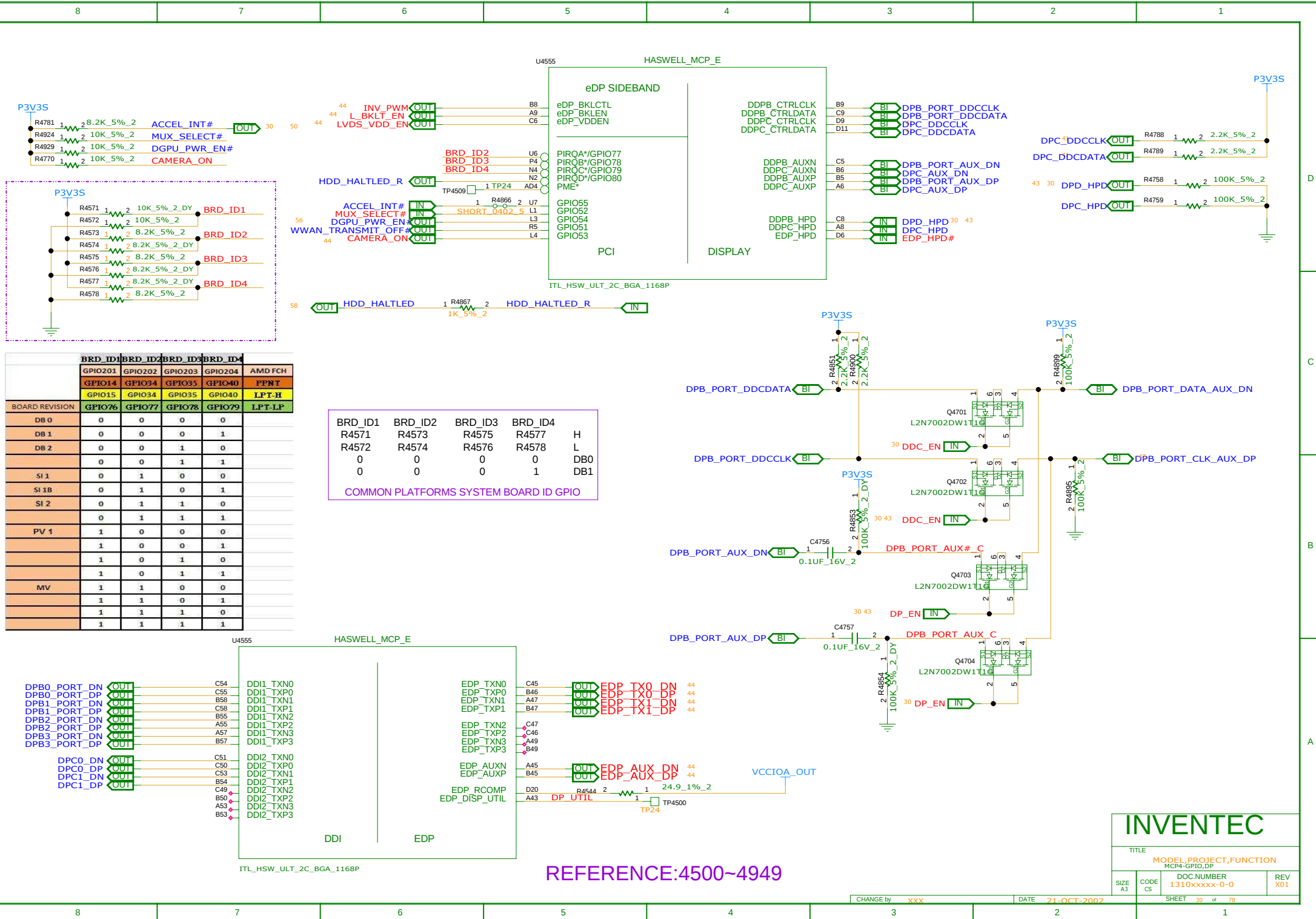
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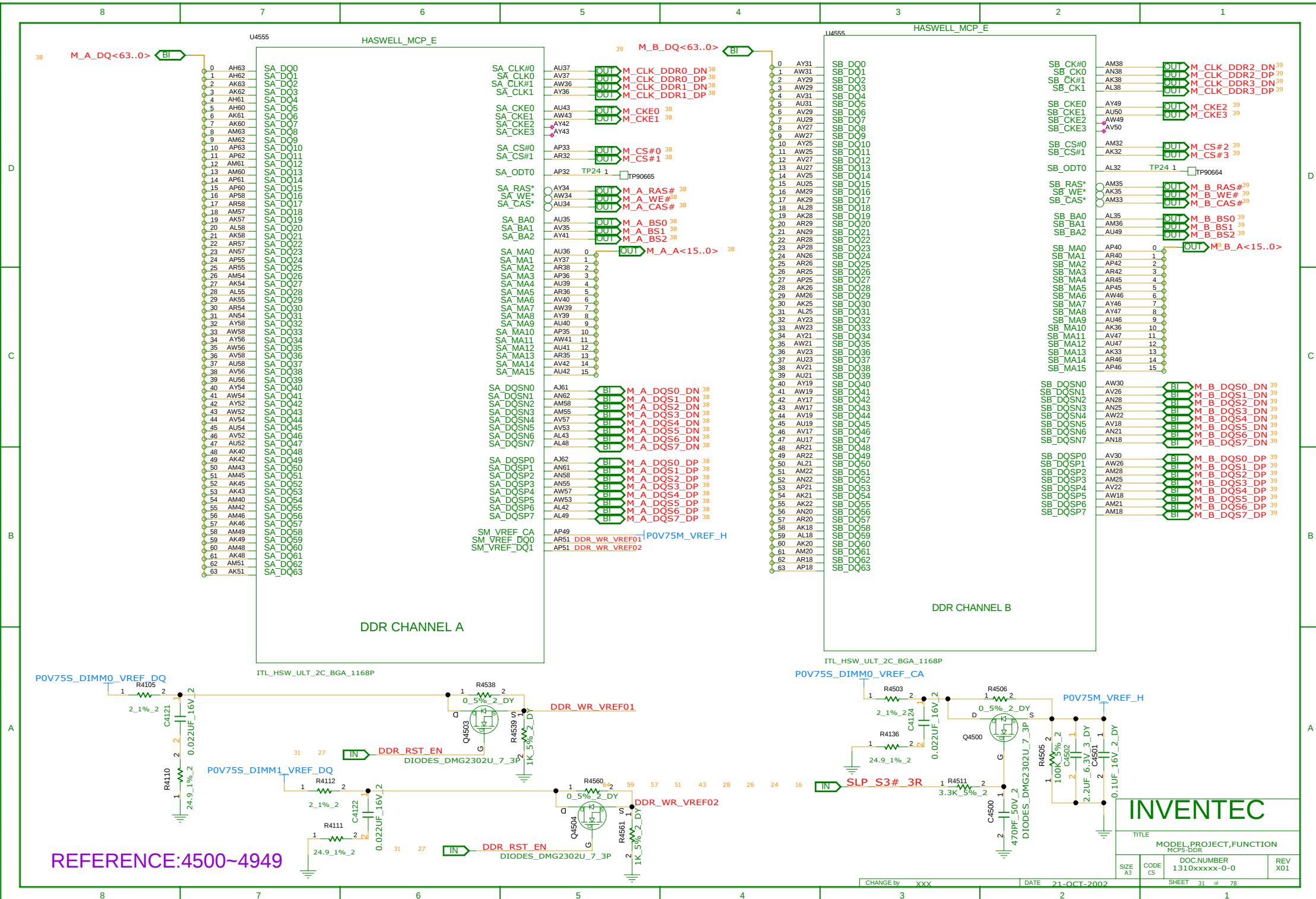
	IAMT	NON-IAMT
R4718	INSTALL	UNINSTALL
R4723	INSTALL	UNINSTALL
R4722	UNINSTALL	INSTALL

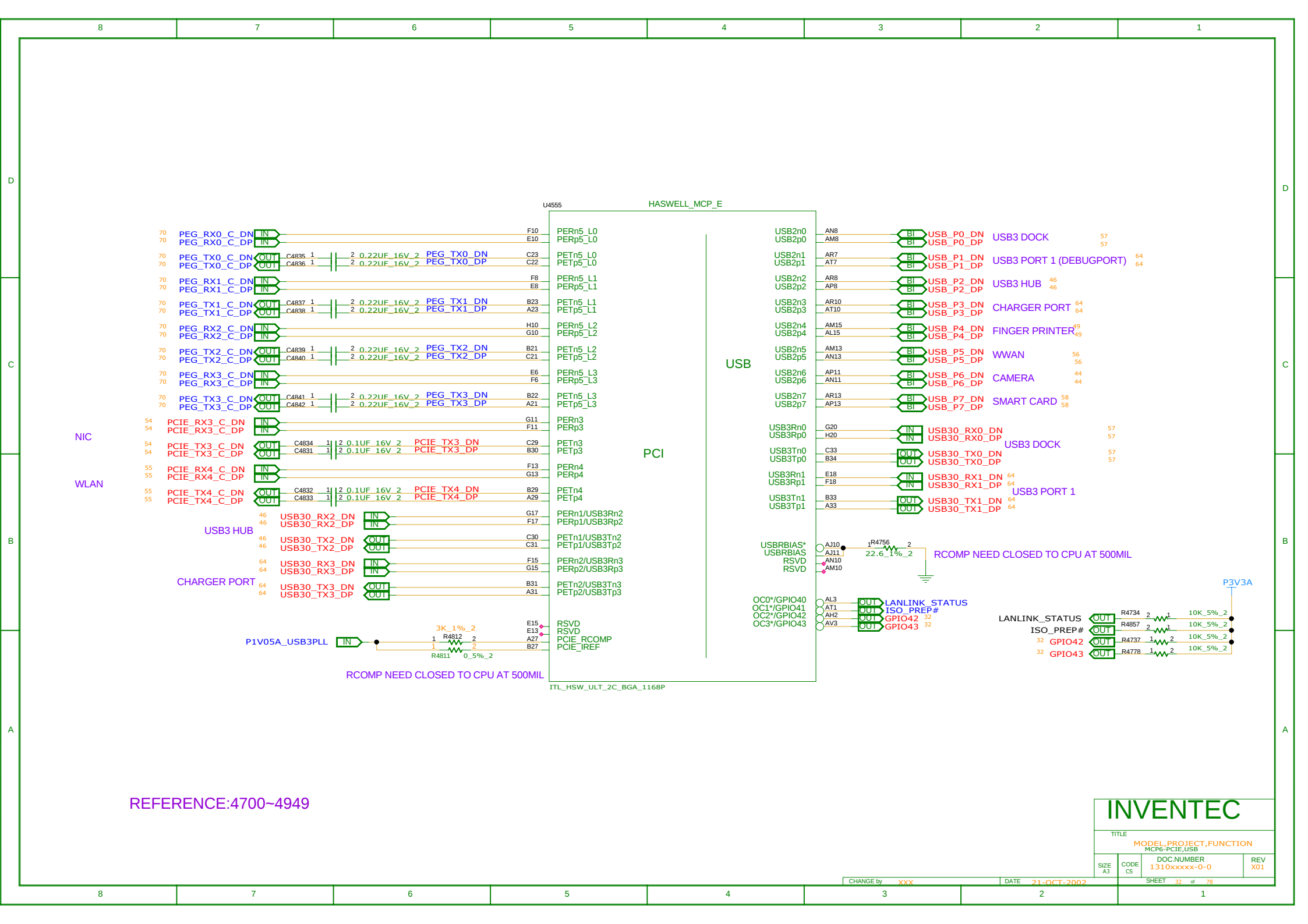
INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
MCP2-SPI,SMBUS,SYSTEM SRQUENCE			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
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REFERENCE:4700~4949

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION

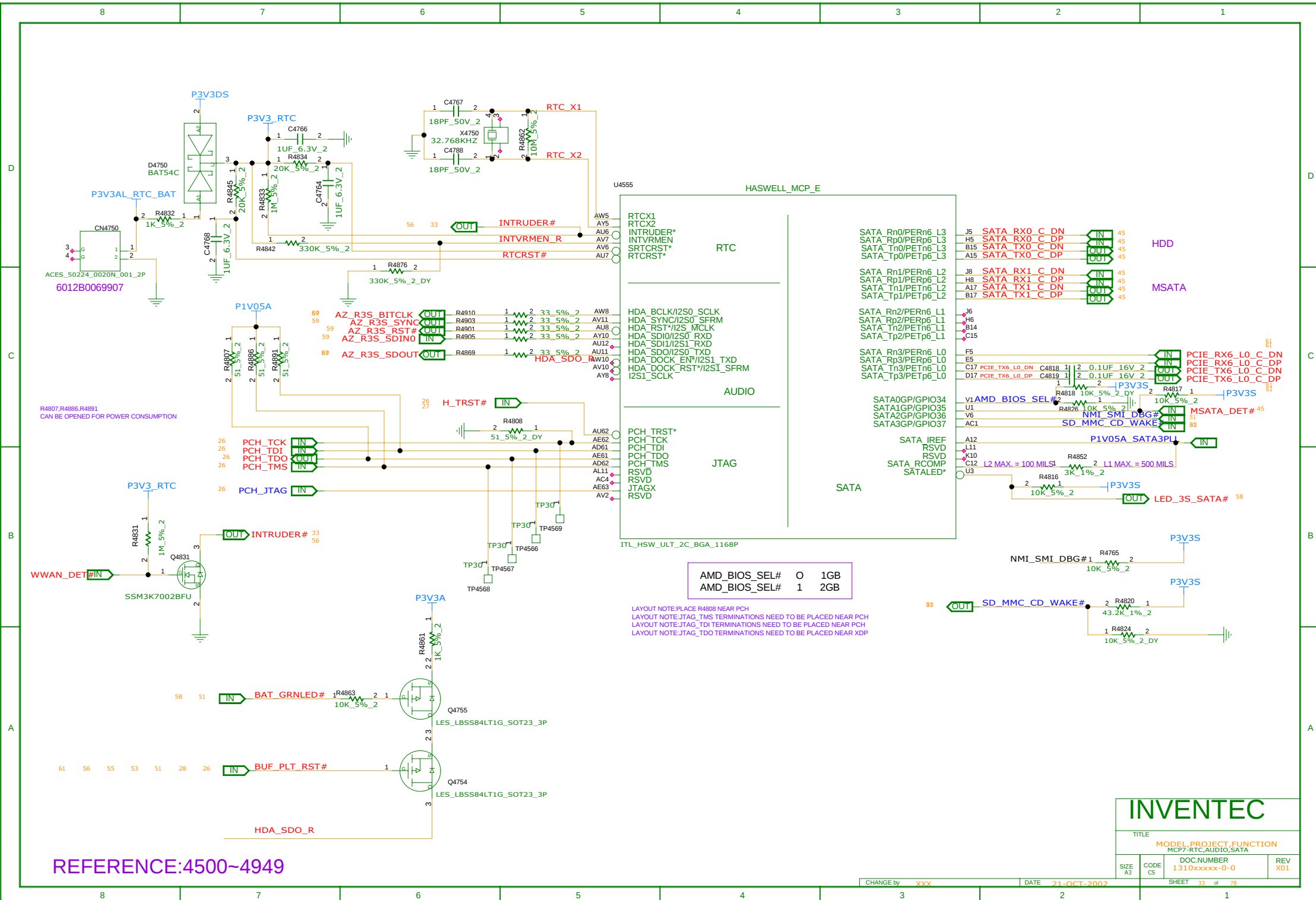
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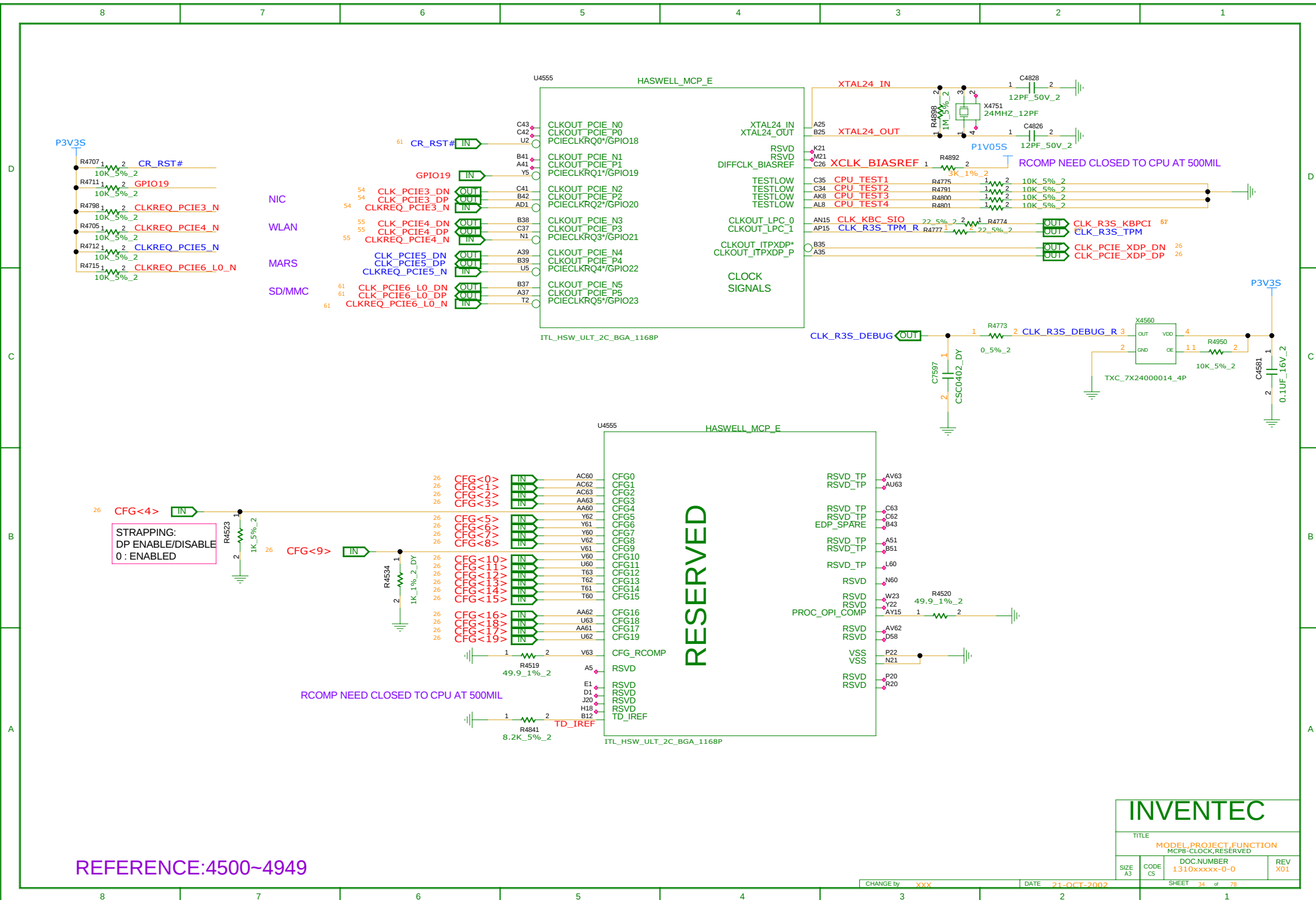
REV
X01

CHANGE by
XXX

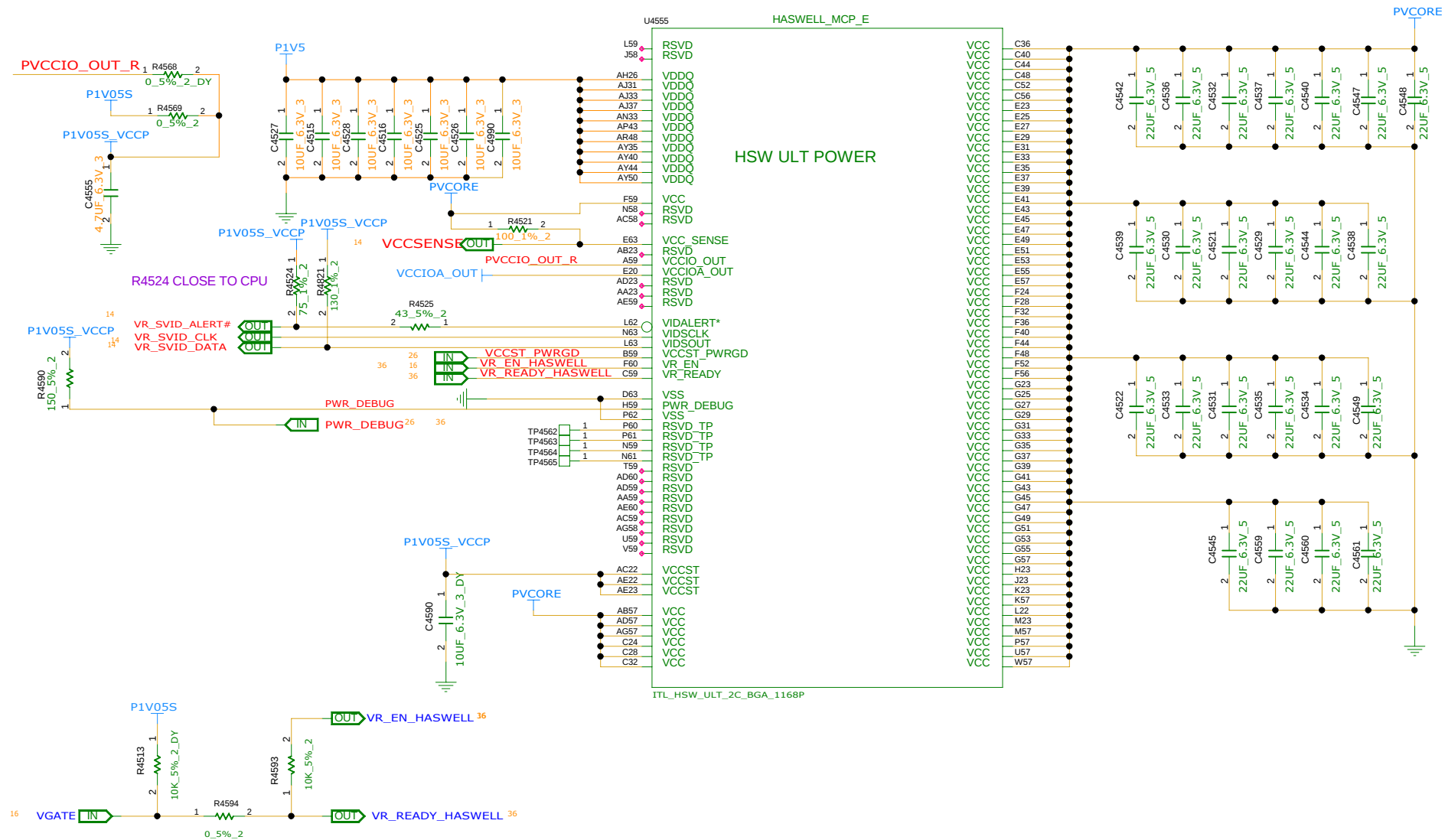
DATE
21-OCT-2002

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ROUTE VCCSENSE WITH 27.4OHM IMPEDANCE



REFERENCE:4500~4949

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION MCP10-POWER			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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C

B

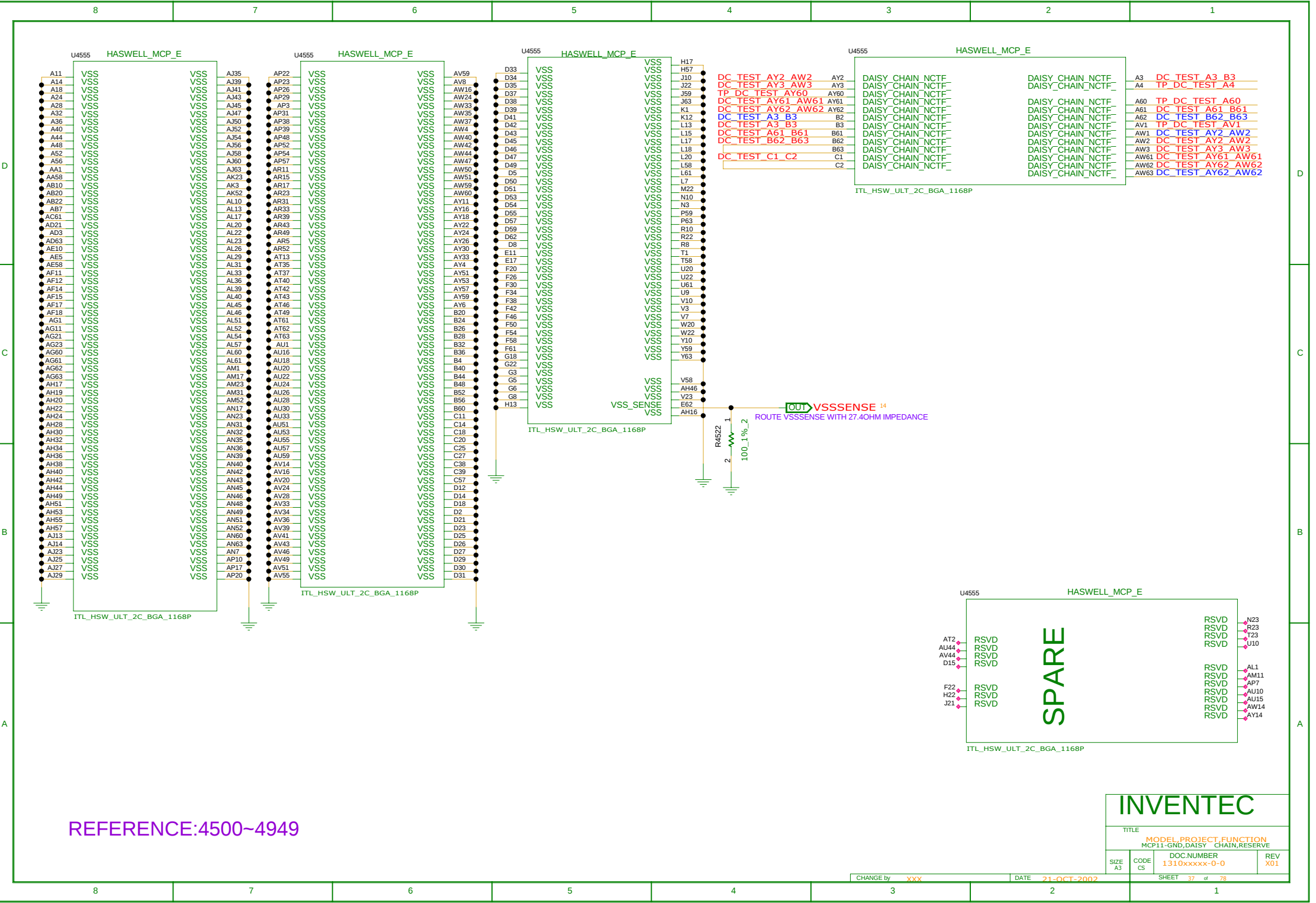
A

D

C

B

A



REFERENCE:4500~4949

INVENTEC

TITLE

MODEL PROJECT FUNCTION

MCP11-GND,DAISY_CHAIN,RESERVE

SIZE A3

CODE CS

DOC NUMBER

1310xxxxx-0-0

REV

X01

CHANGE by

XXX

DATE

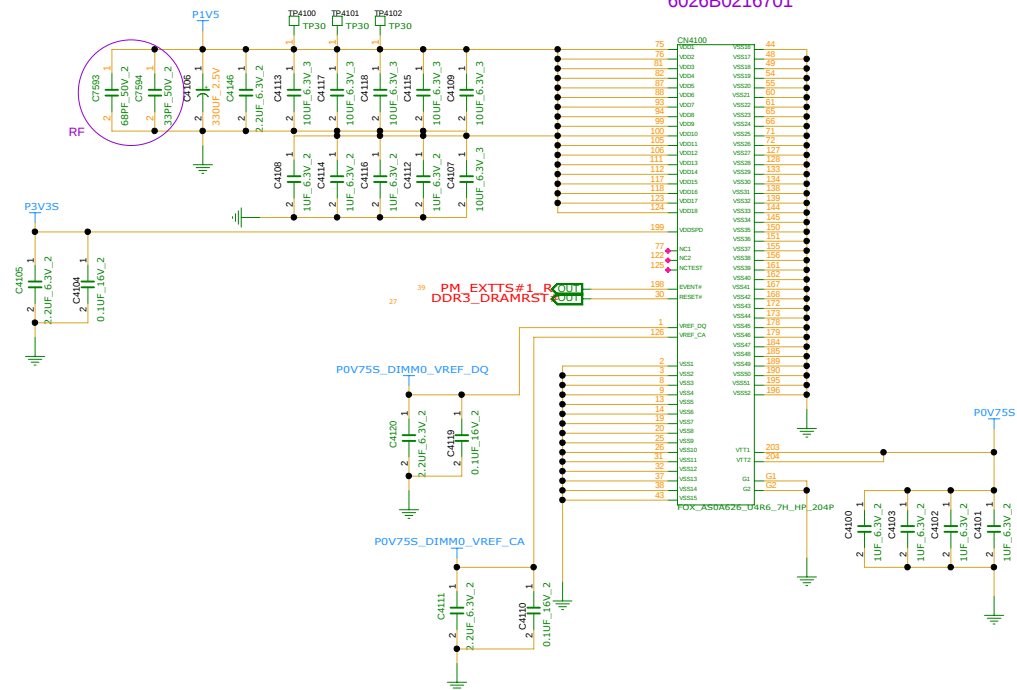
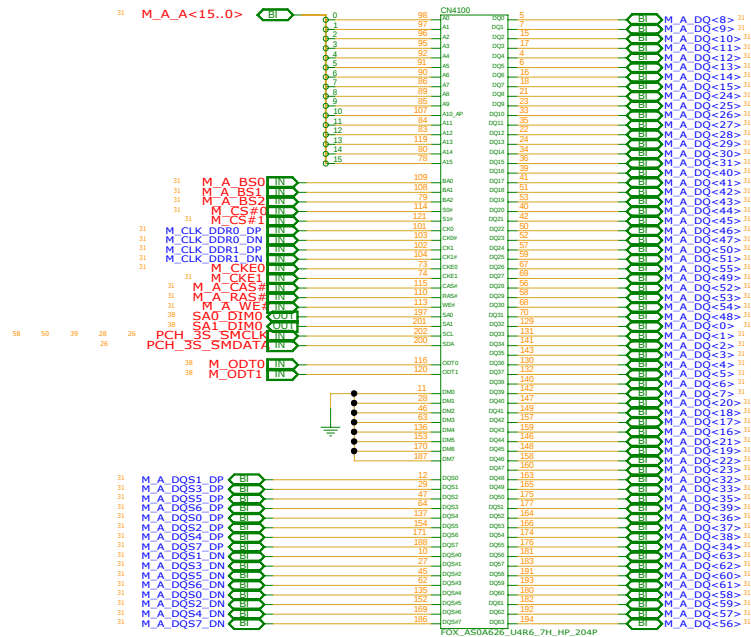
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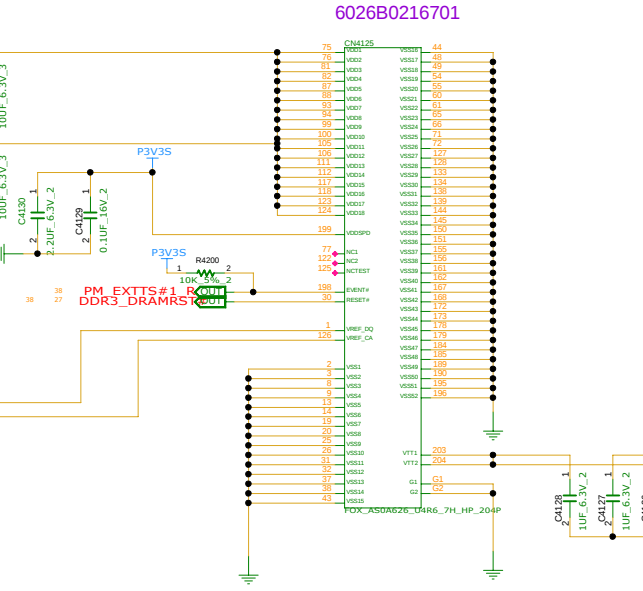
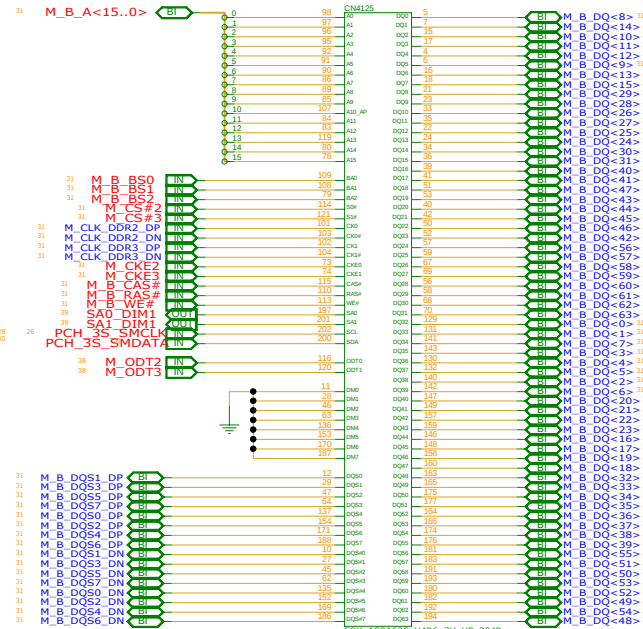
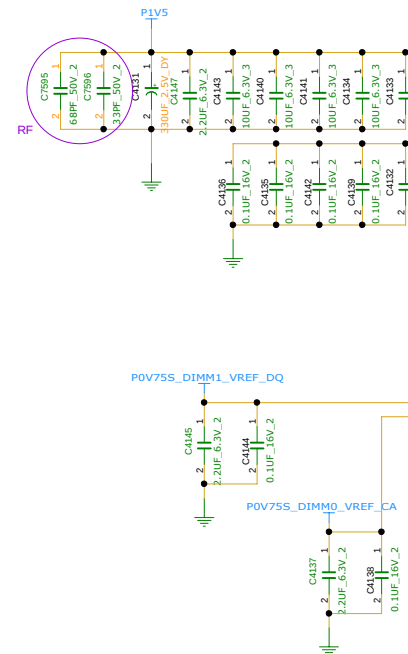
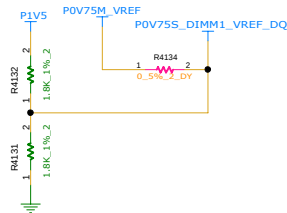
IF SA0_DIM0=1 , SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA2
SO-DIMMA TS ADDRESS IS 0X32

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION DDR3_SO-DIMM0			
SIZE C	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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NOTE:
SO-DIMM SPD ADDRESS IS 0X44
SO-DIMM TS ADDRESS IS 0X34

REFERENCE NUMBER:4100~4299



RESERVED

INVENTEC

TITLE

MODEL PROJECT FUNCTION
DPB DEMUX1 TO DP

SIZE
A3

CODE
CS

DOC NUMBER
1310xxxxx-0-0

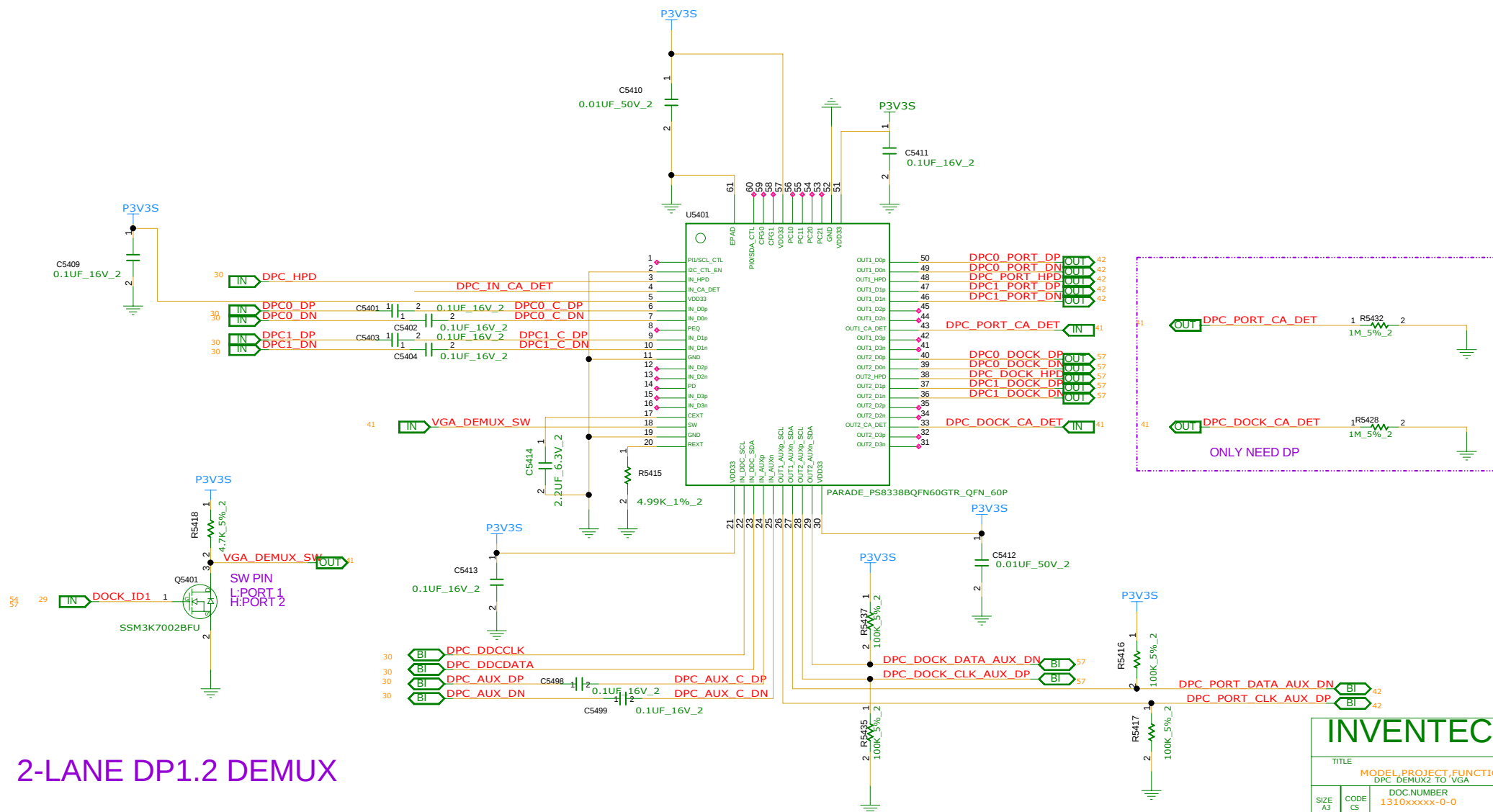
REV
X01

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DATE 21-OCT-2002

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R5409 FOR CHIP OPERATION MODE
R5411, R5412 FOR PROGRAMMABLE INPUT EQUALIZATION LEVELS
R5413, R5414 FOR AUTO TEST ENABLE

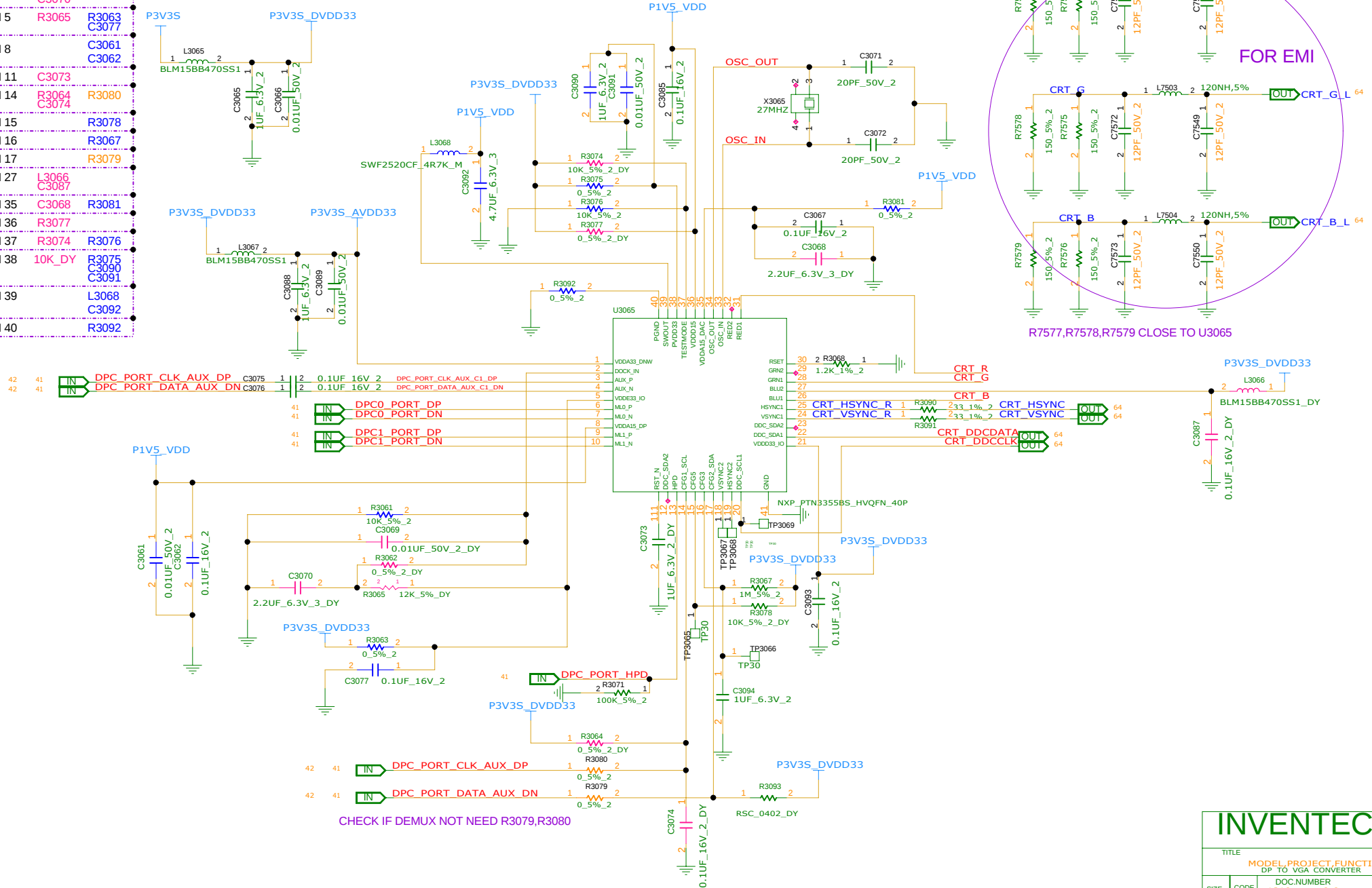


2-LANE DP1.2 DEMUX

INVENTEC

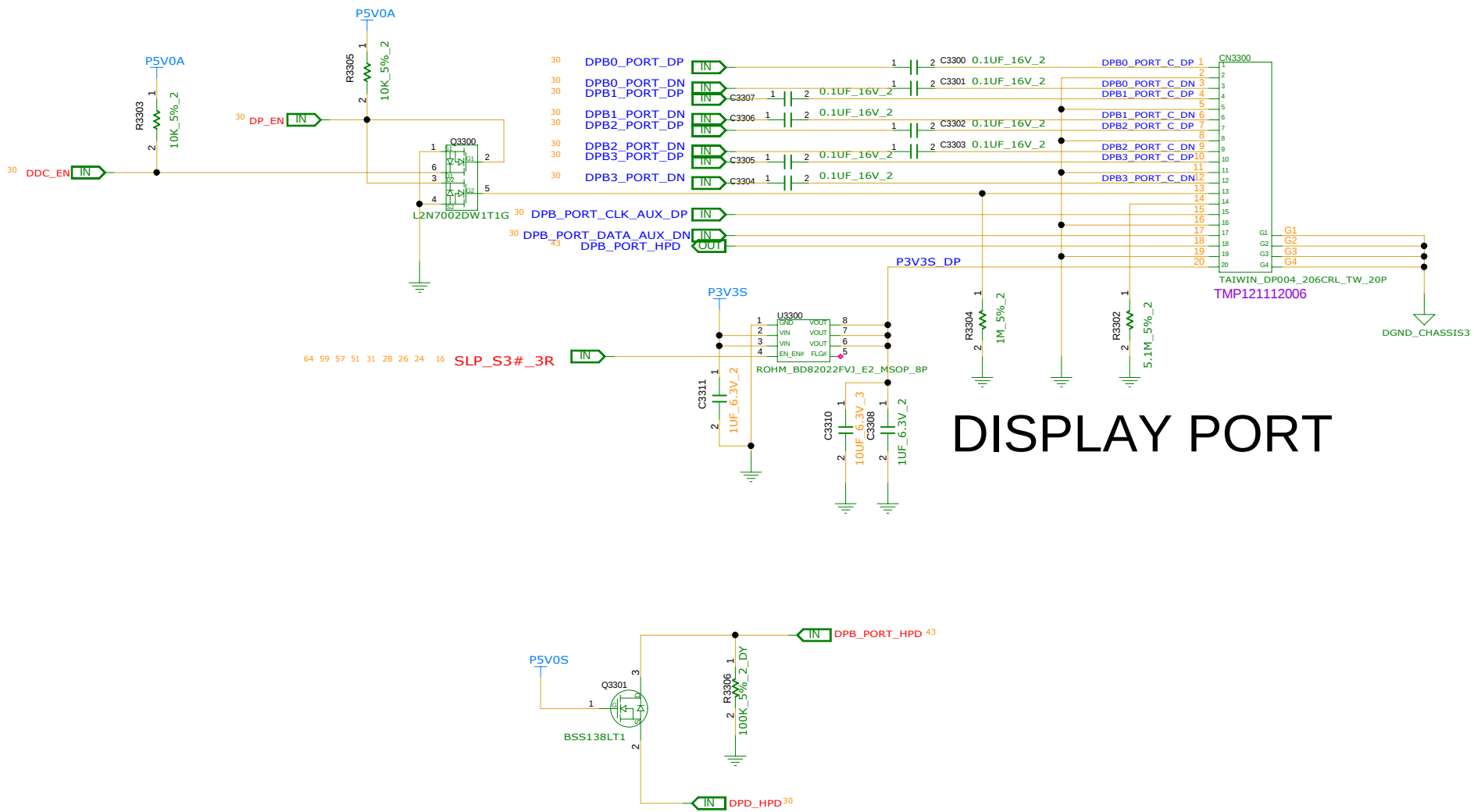
TITLE			
MODEL PROJECT FUNCTION			
DPC DEMUX2 TO VGA			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

	3393	3355
PIN 2	R3062 C3069 C3070	R3061
PIN 5	R3065	R3063 C3077
PIN 8		C3061 C3062
PIN 11	C3073	
PIN 14	R3064 C3074	R3080
PIN 15	R3078	
PIN 16	R3067	
PIN 17	R3079	
PIN 27	L3066 C3087	
PIN 35	C3068	R3081
PIN 36	R3077	
PIN 37	R3074	R3076
PIN 38	10K_DY	R3075 C3090 C3091
PIN 39	L3068	
PIN 40	C3092	R3092



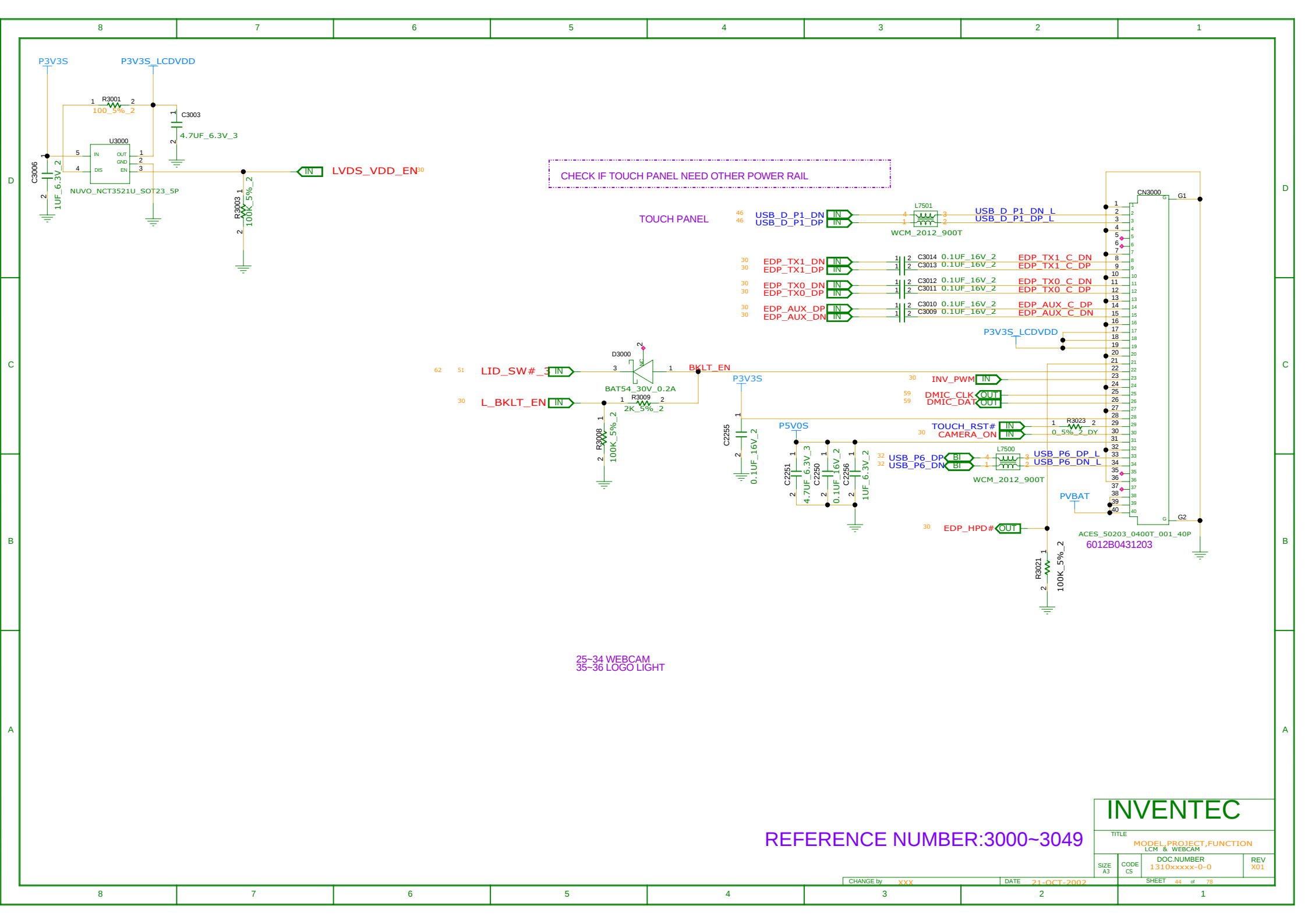
INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
DP TO VGA CONVERTER			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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REFERENCE NUMBER:3300~3399

INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
CRT & DP			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
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CHECK IF TOUCH PANEL NEED OTHER POWER RAIL

TOUCH PANEL

25-34 WEBCAM
35-36 LOGO LIGHT

REFERENCE NUMBER:3000~3049

INVENTEC			
TITLE MODEL PROJECT,FUNCTION LCM & WEBCAM			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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REFERENCE NUMBER:1700~1749

REFERENCE NUMBER:1950~1999

M TYPE
6026B0240301
NGFF SSD

SATA HDD CONNECTOR

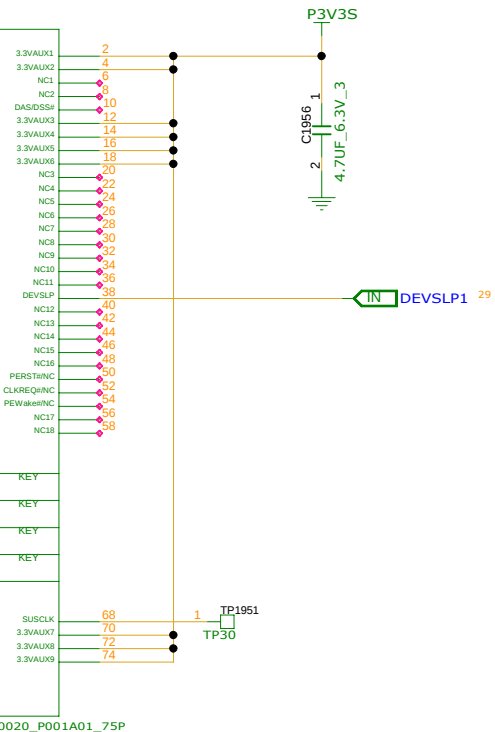
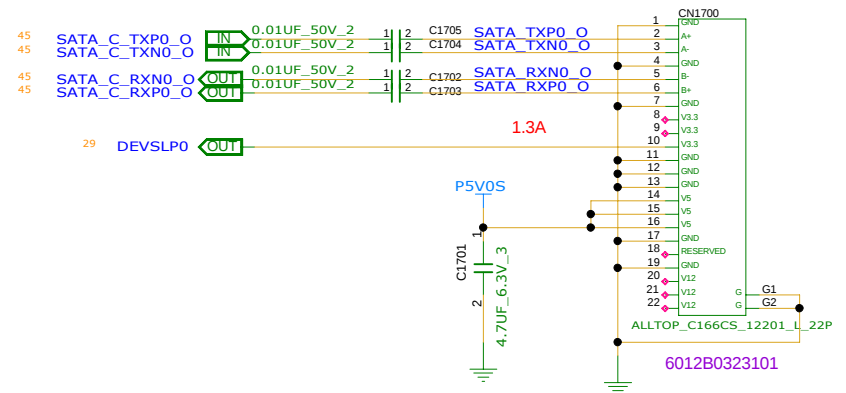
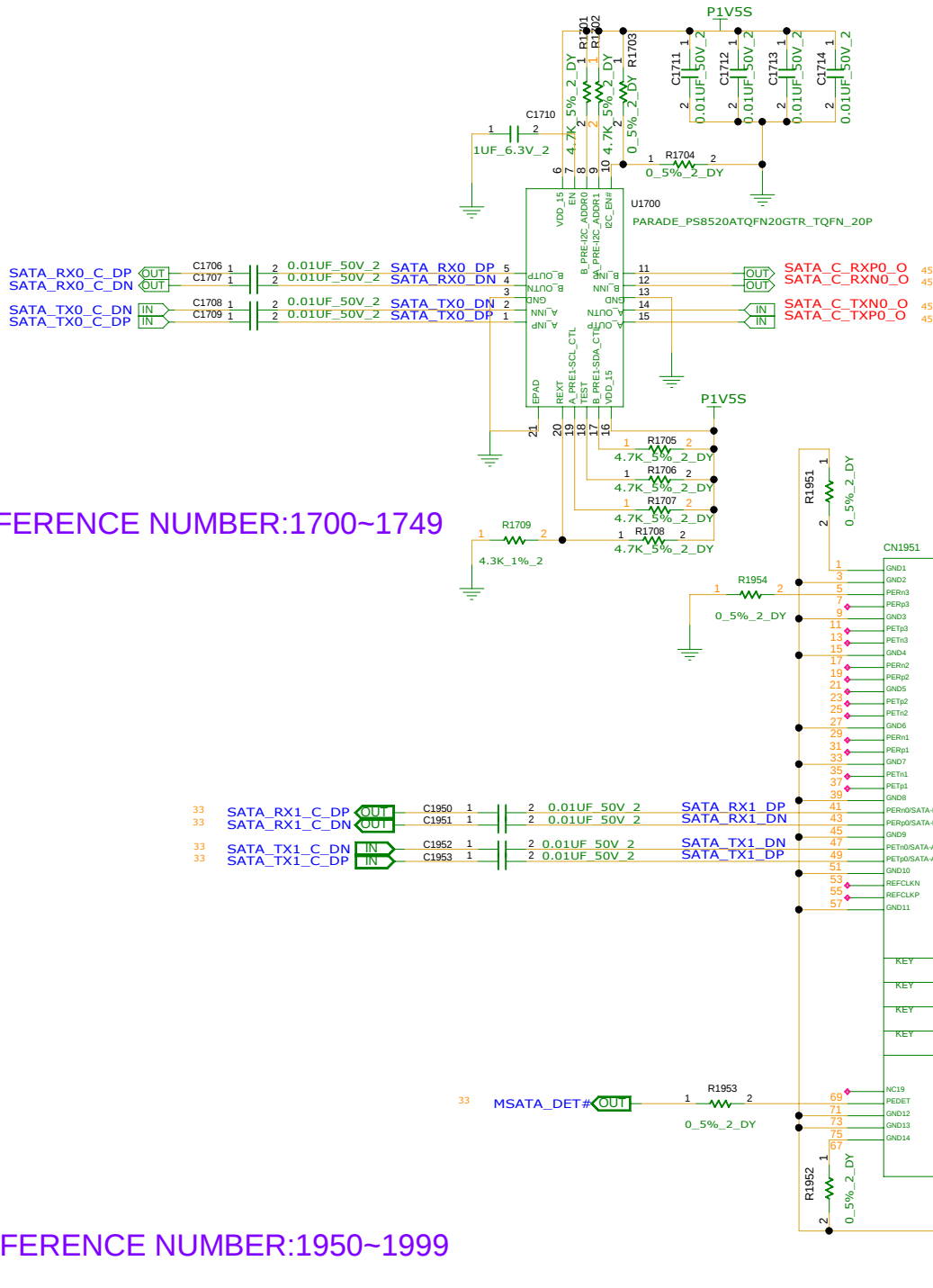
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
SATA, HDD & M-SATA CONN.

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002



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C

B

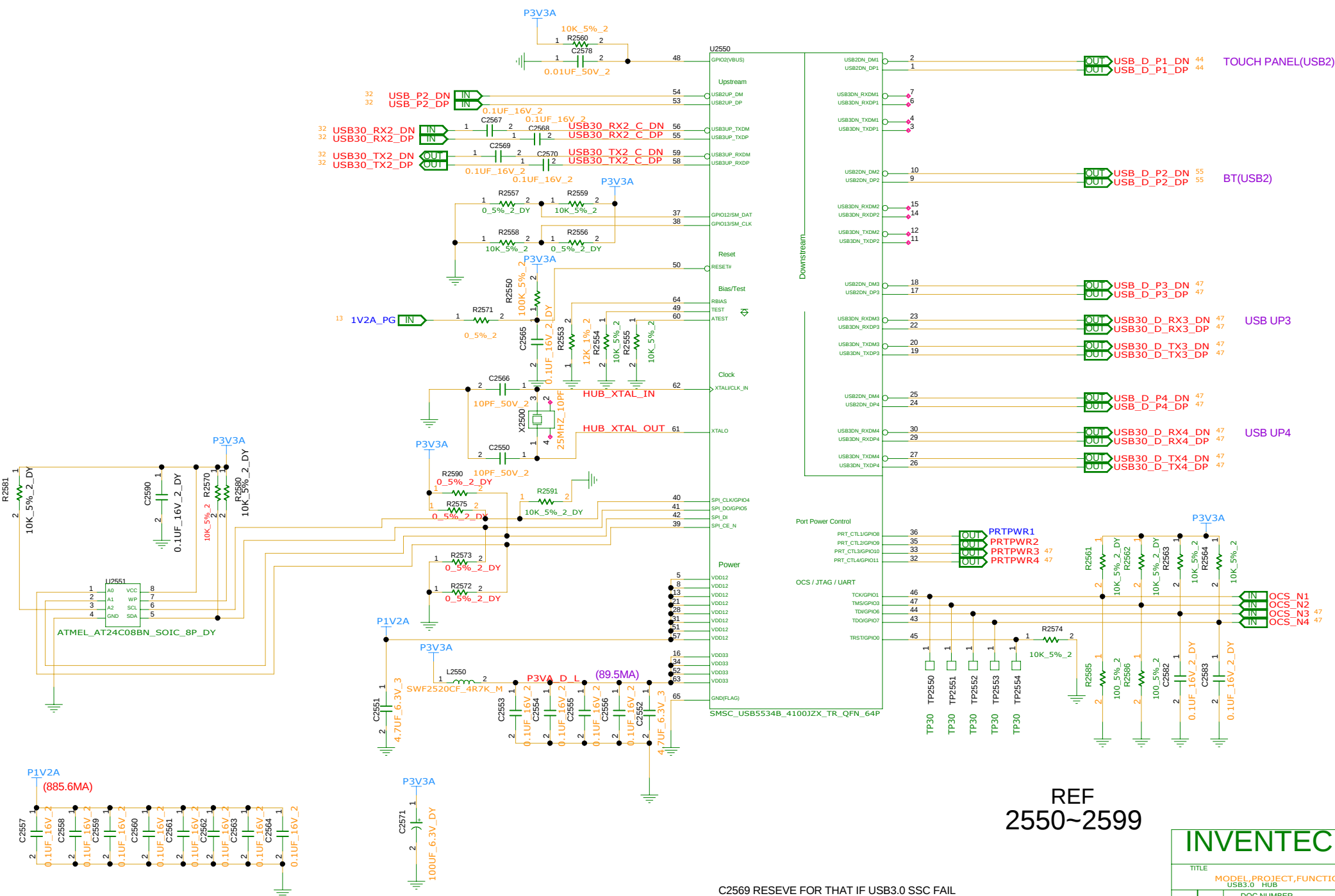
A

D

C

B

A



C2569 RESEVE FOR THAT IF USB3.0 SSC FAIL

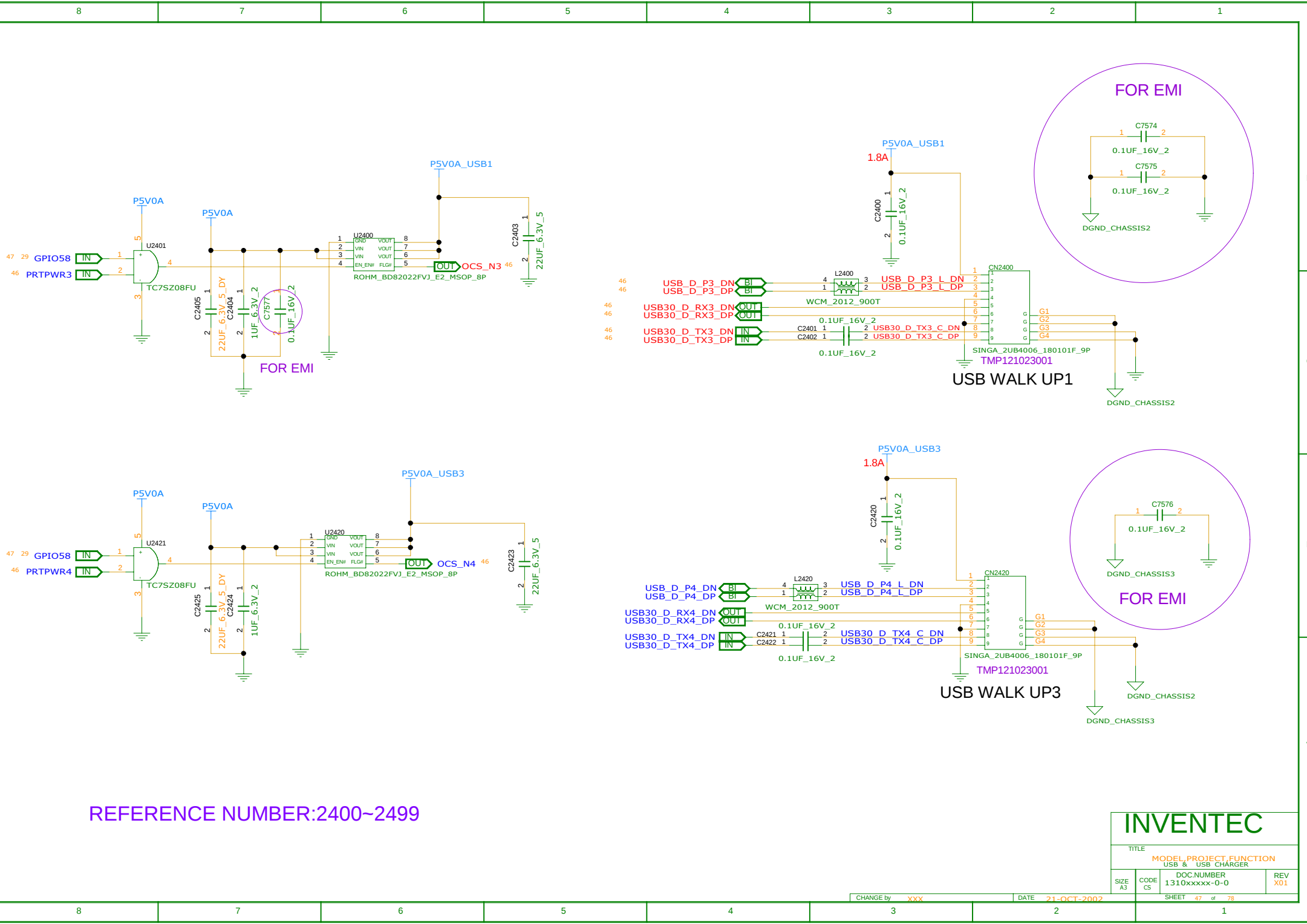
REF
2550~2599

INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
USB3.0 HUB			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

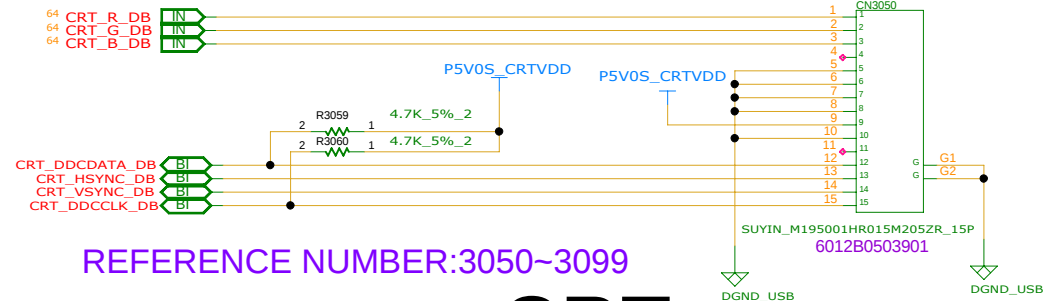
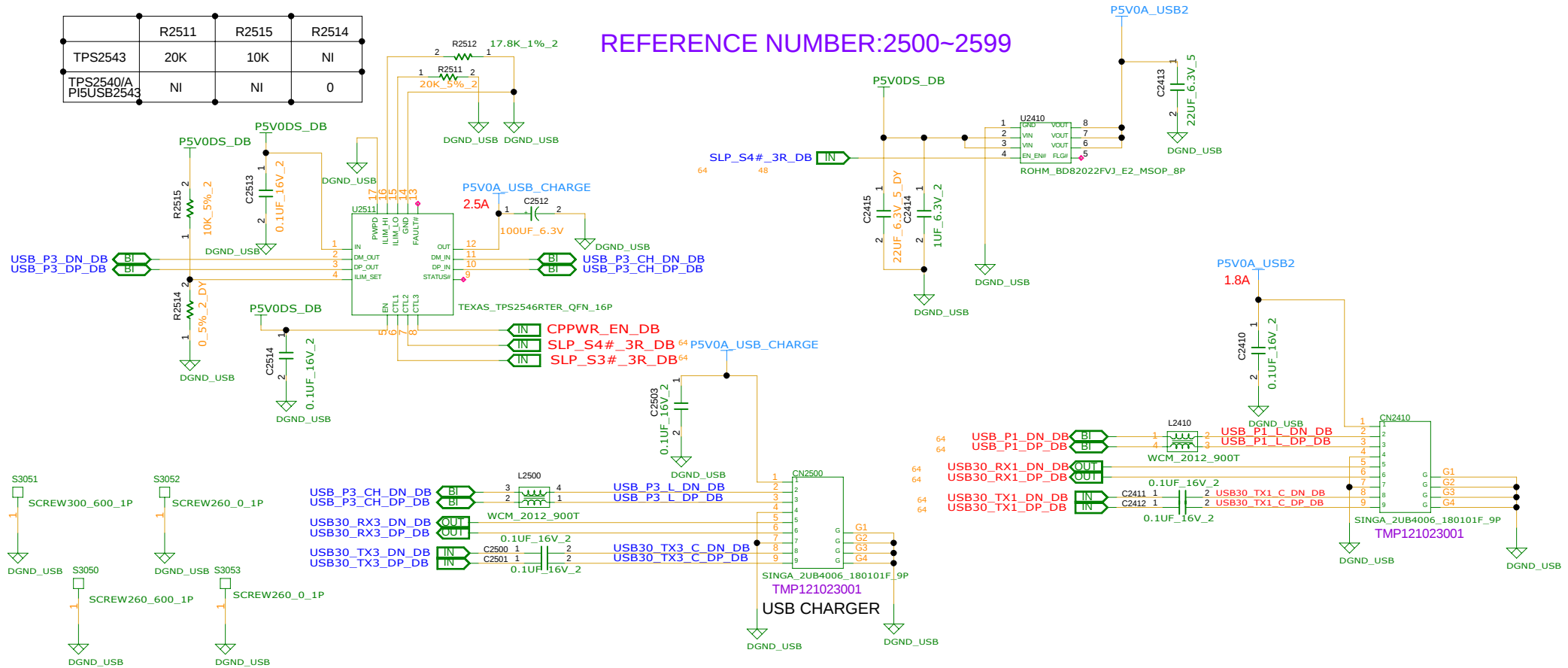
CHANGE by XXX DATE 21-OCT-2002

SHEET 46 of 78



	R2511	R2515	R2514
TPS2543	20K	10K	NI
TPS2540/A Pi5USB2543	NI	NI	0

REFERENCE NUMBER:2500~2599



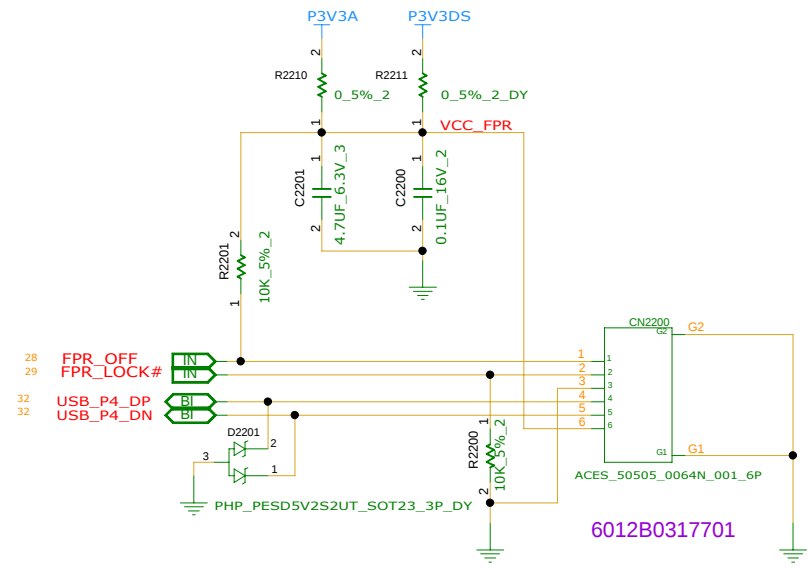
REFERENCE NUMBER:3050~3099

CRT

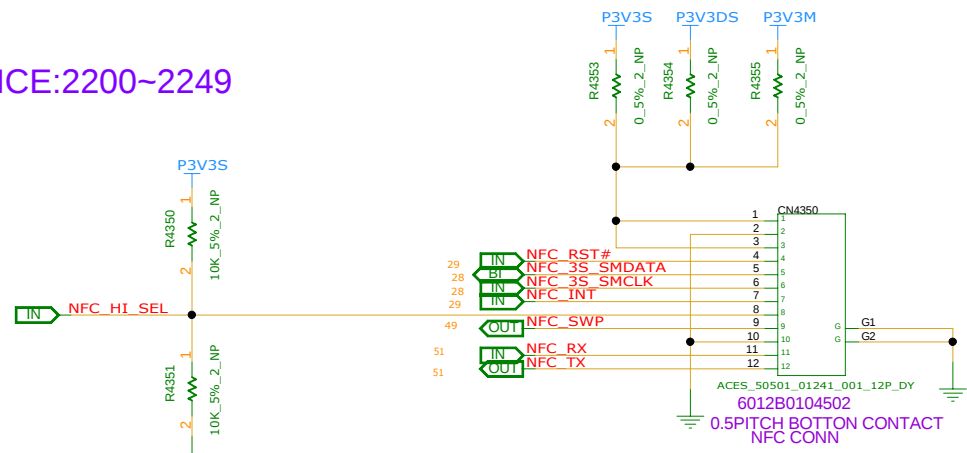
INVENTEC

TITLE			
MODEL PROJECT,FUNCTION			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		48 of 78	

CHANGE by XXX DATE 21-OCT-2002

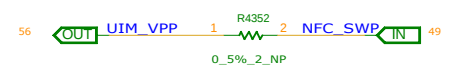


FINGER PRINT CONN



6012B0104502
0.5PITCH BOTTOM CONTACT
NFC CONN

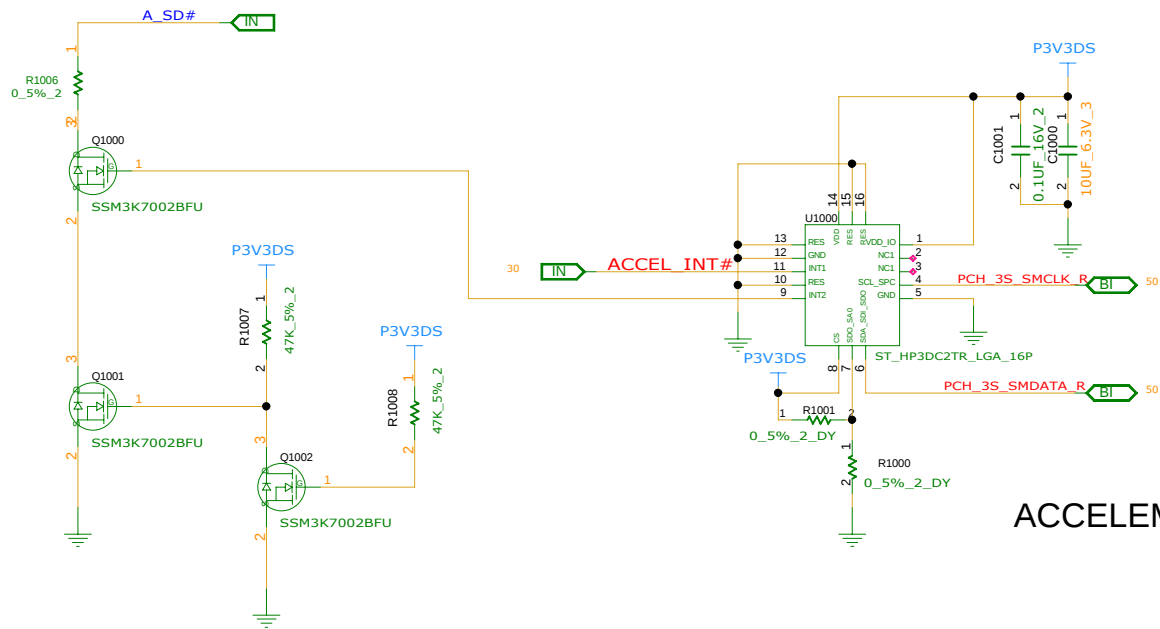
NFC_HI_SEL R4350 R4351
HIGH (UART) INSTALL
LOW (I2C) INSTALL



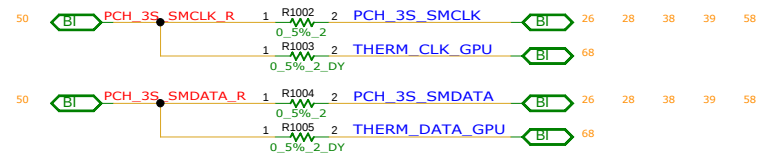
REFERENCE:2200~2249

REFERENCE:4350~4399

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION FINGER PRINTER & NFC			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 49 of 78			



ACCELEMETER



REFERENCE NUMER : 1000~1099

INVENTEC

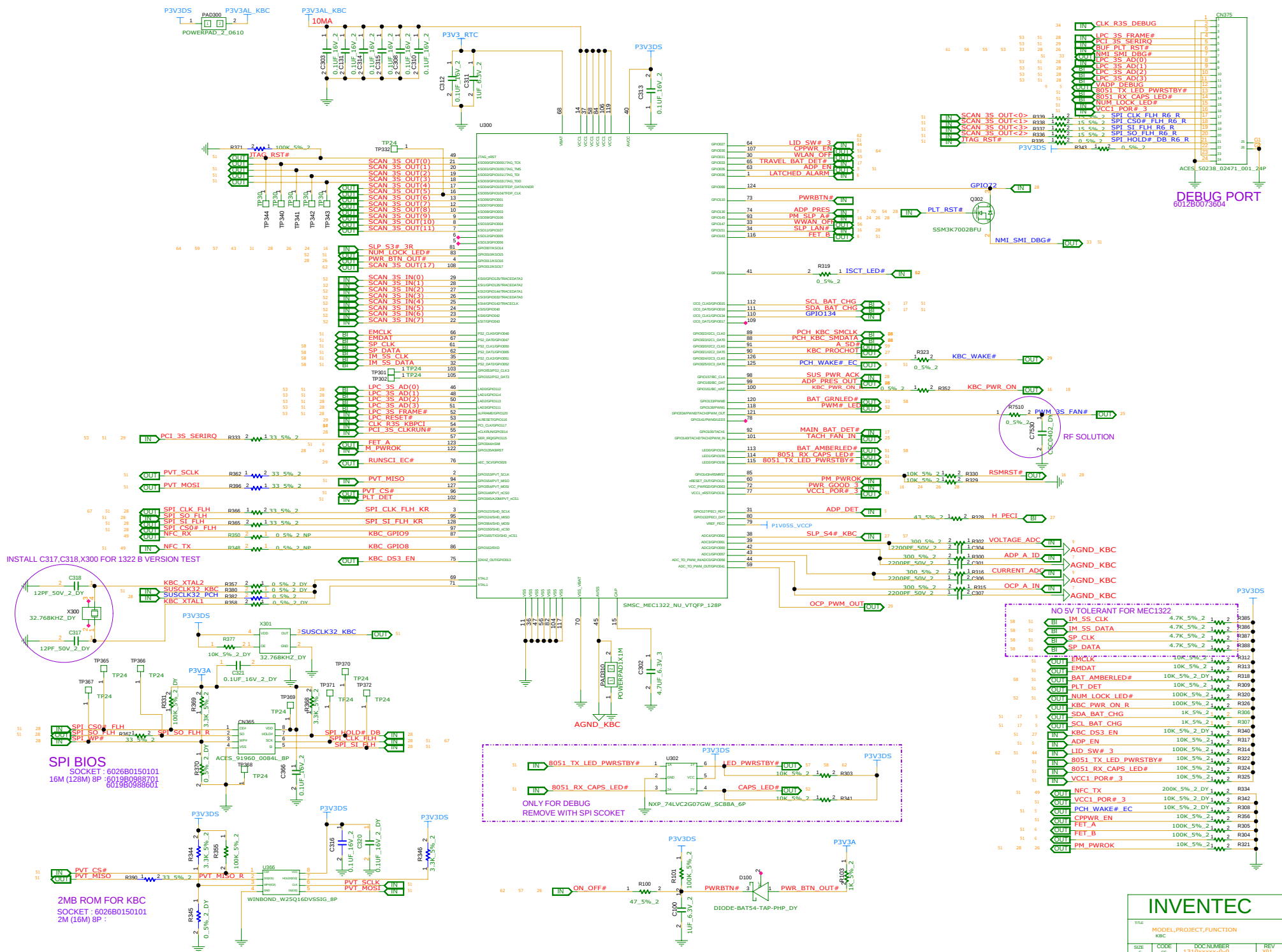
TITLE
MODEL PROJECT,FUNCTION
ACCELEMETER

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002

SHEET 50 of 78

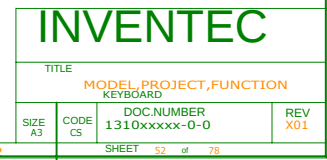
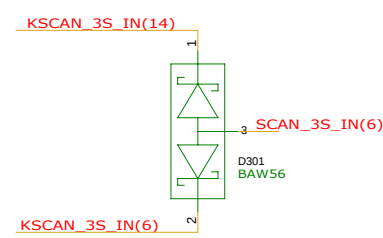
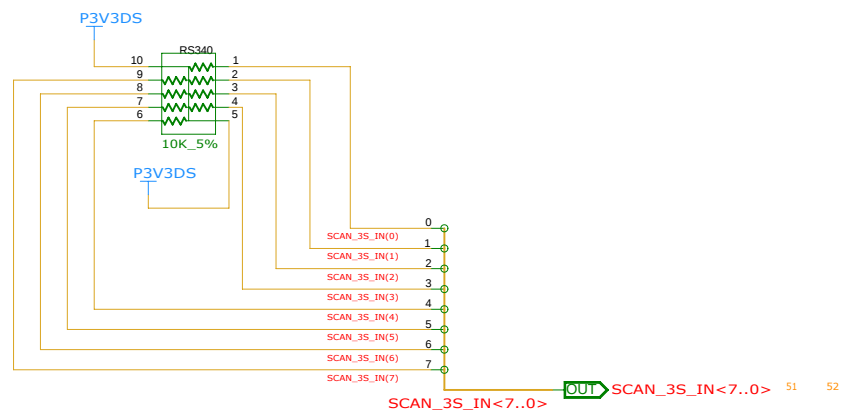
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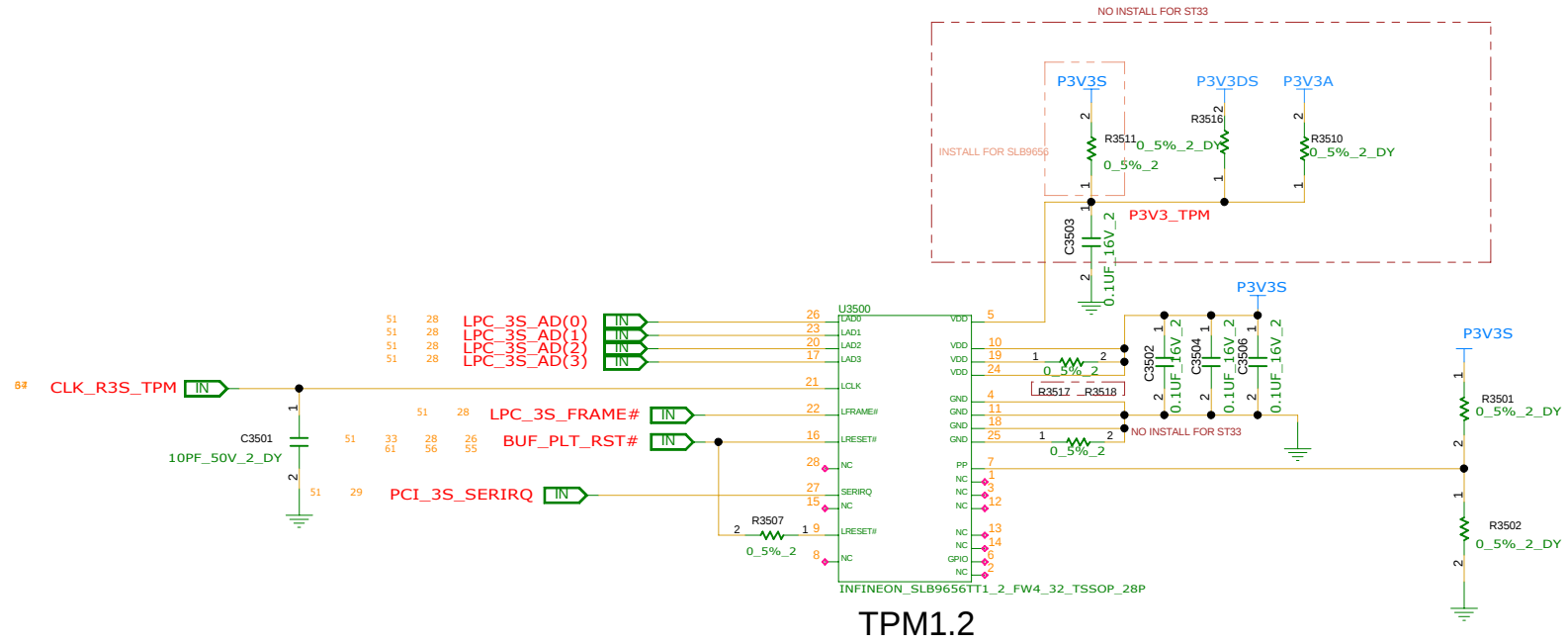


INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
KBC			
SIZE C	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 51 of 78			

A





TPM1.2

SLB9656TT1.2		ST33
C3503	INSTALL	OPEN
R3507	INSTALL	OPEN
R3511	INSTALL	OPEN
R3517	INSTALL	OPEN
R3518	INSTALL	OPEN

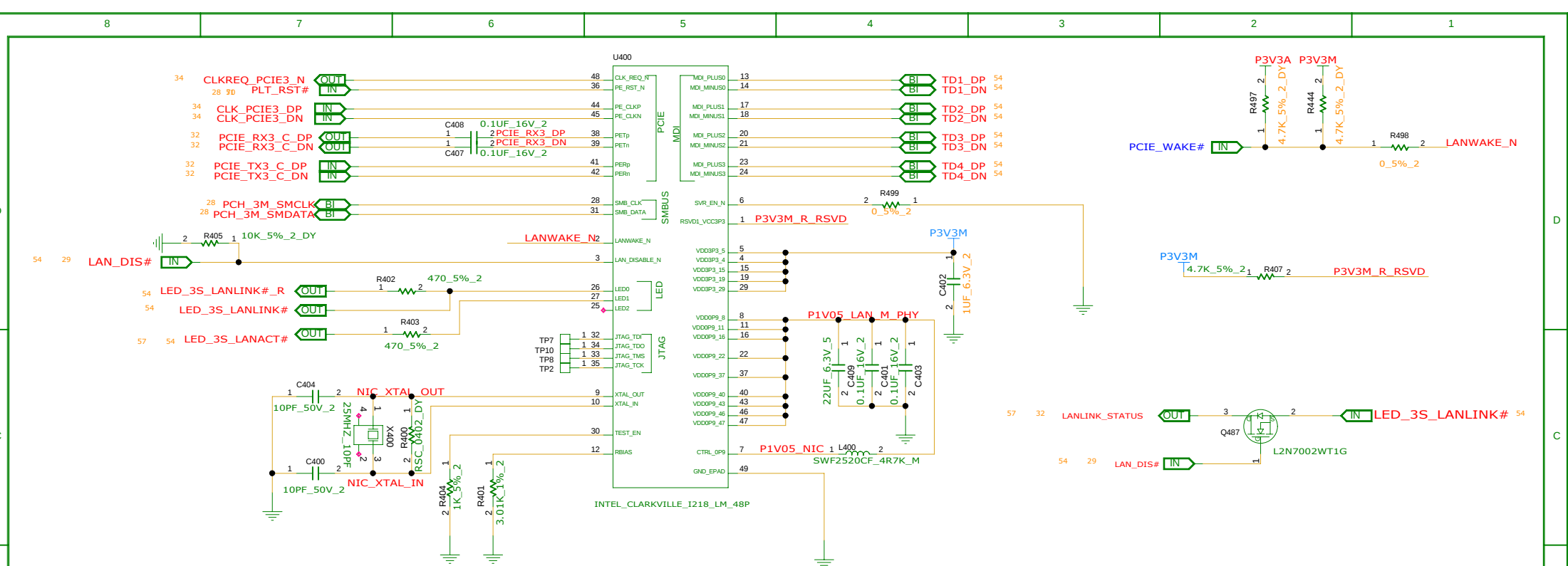
REFERENCE NUMER : 3500~3549

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
TPM

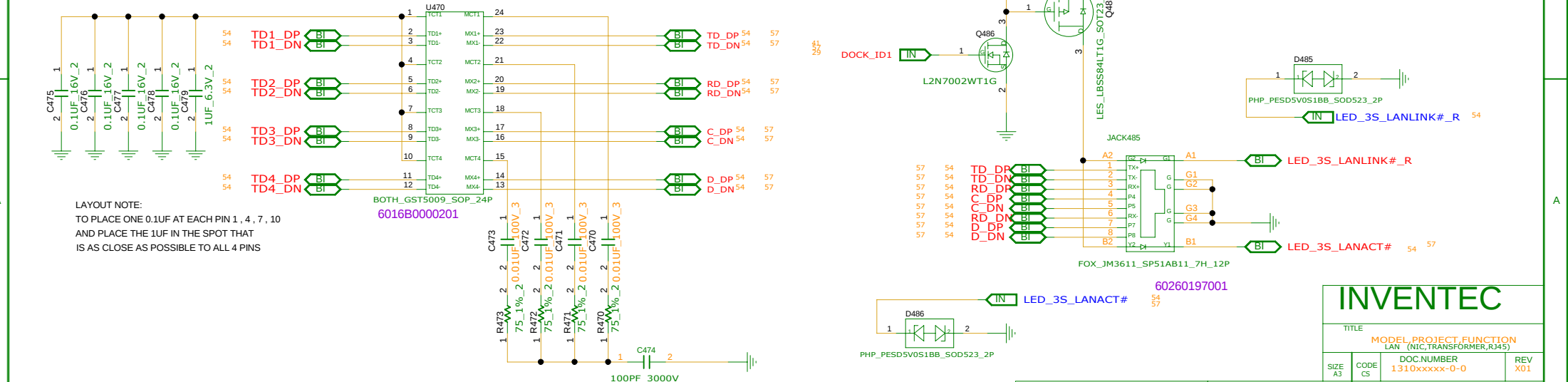
SIZE CODE DOC NUMBER REV
A3 CS 1310xxxx-0-0 X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 53 of 78



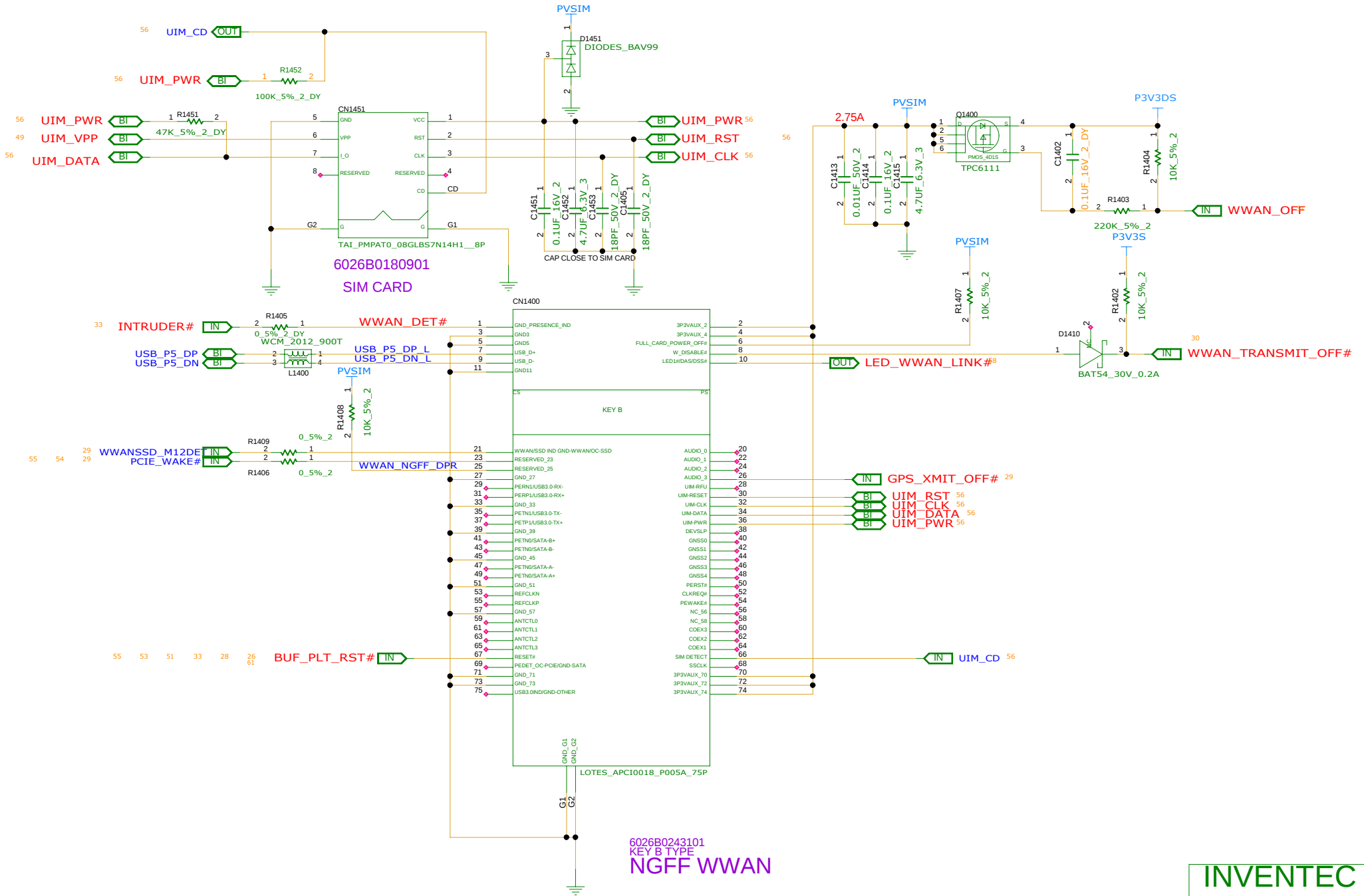
REFERENCE NUMBER : 400~469

REFERENCE NUMBER : 470~499



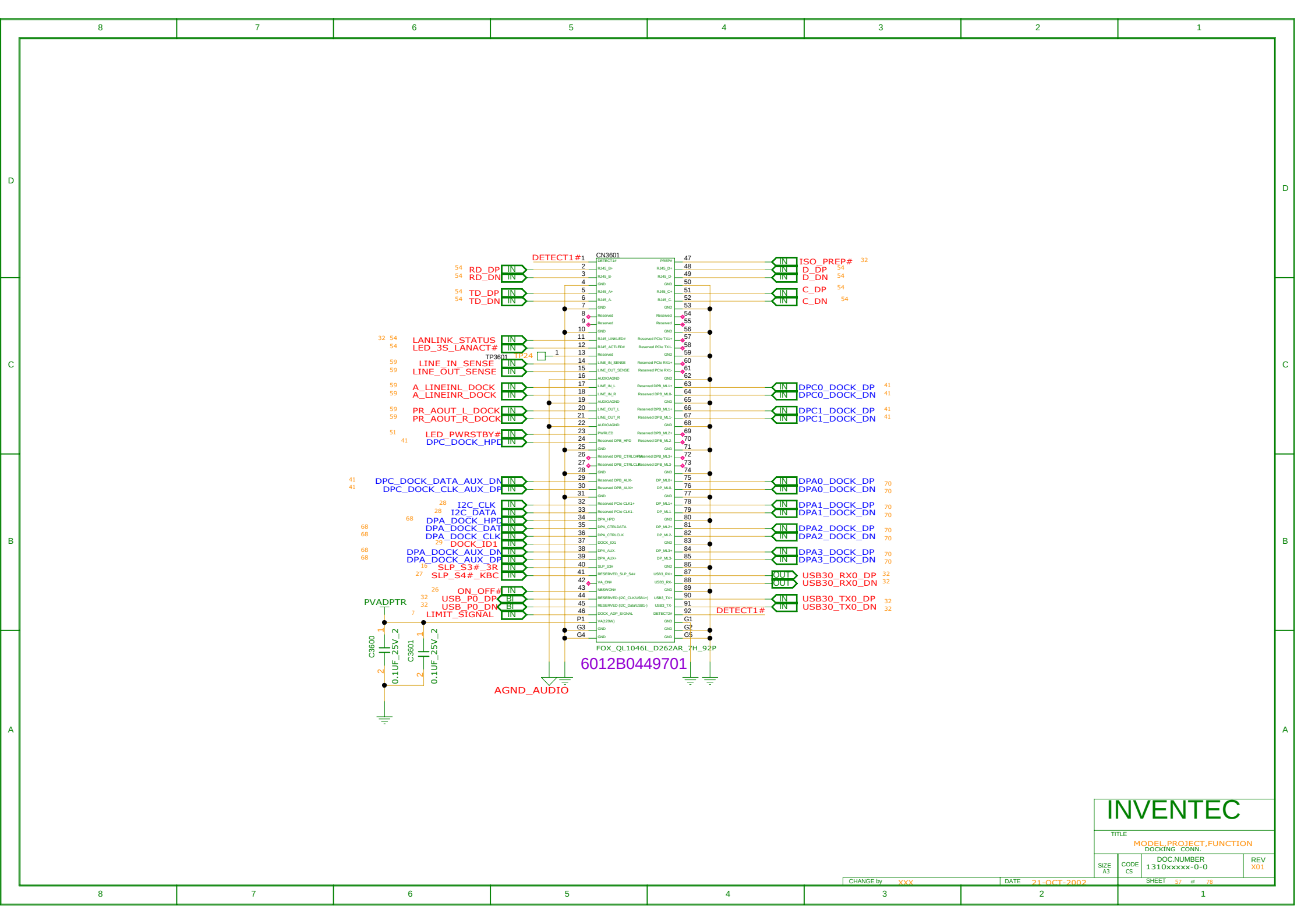
LAYOUT NOTE:
TO PLACE ONE 0.1UF AT EACH PIN 1, 4, 7, 10
AND PLACE THE 1UF IN THE SPOT THAT
IS AS CLOSE AS POSSIBLE TO ALL 4 PINS

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
LAN (NIC TRANSFORMER RJ45)			
DOC NUMBER			
1310xxxxx-0-0			
REV			
X01			
SIZE	CODE	SHEET	
A3	CS	54 of 78	



REFERENCE NUMBER:1400-1499

INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
WWAN NGFF			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 56 of 78			

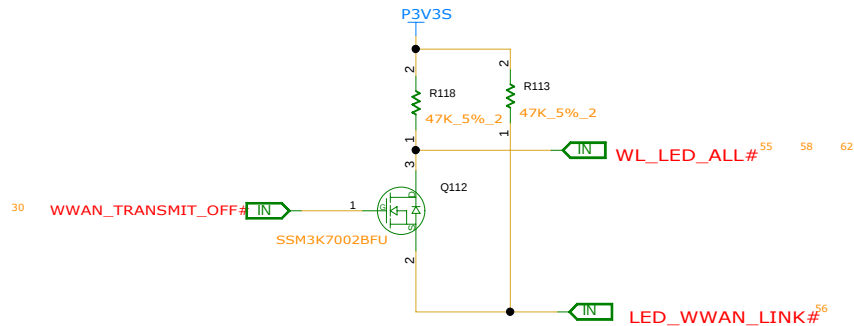


INVENTEC

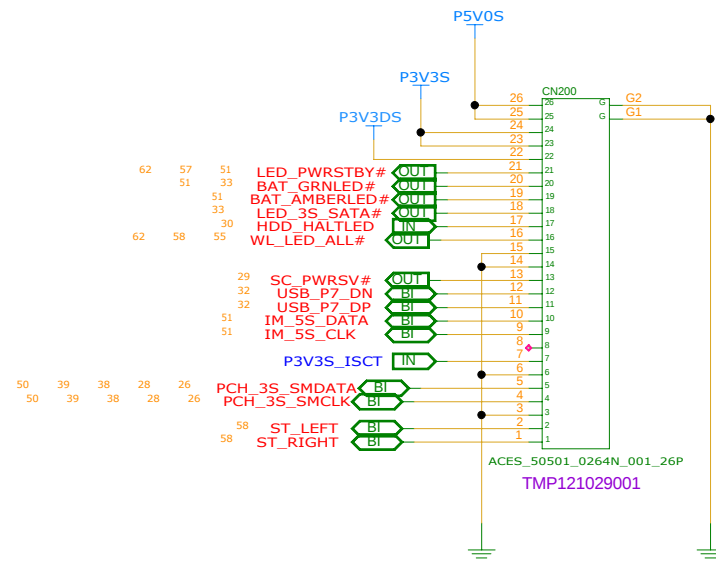
TITLE
MODEL PROJECT,FUNCTION
DOCKING CONN.

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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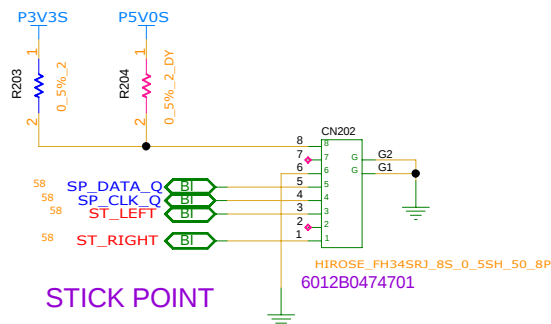
CHANGE by XXX DATE 21-OCT-2002 SHEET 57 of 78



WLAN_WWAN_BLUETOOTH_LED

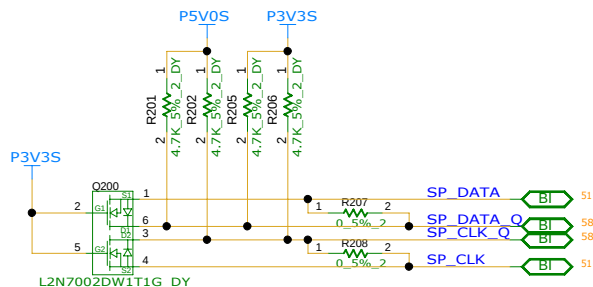


SMART CARD AND TOUCHPAD D/B W TO B CONN



STICK POINT

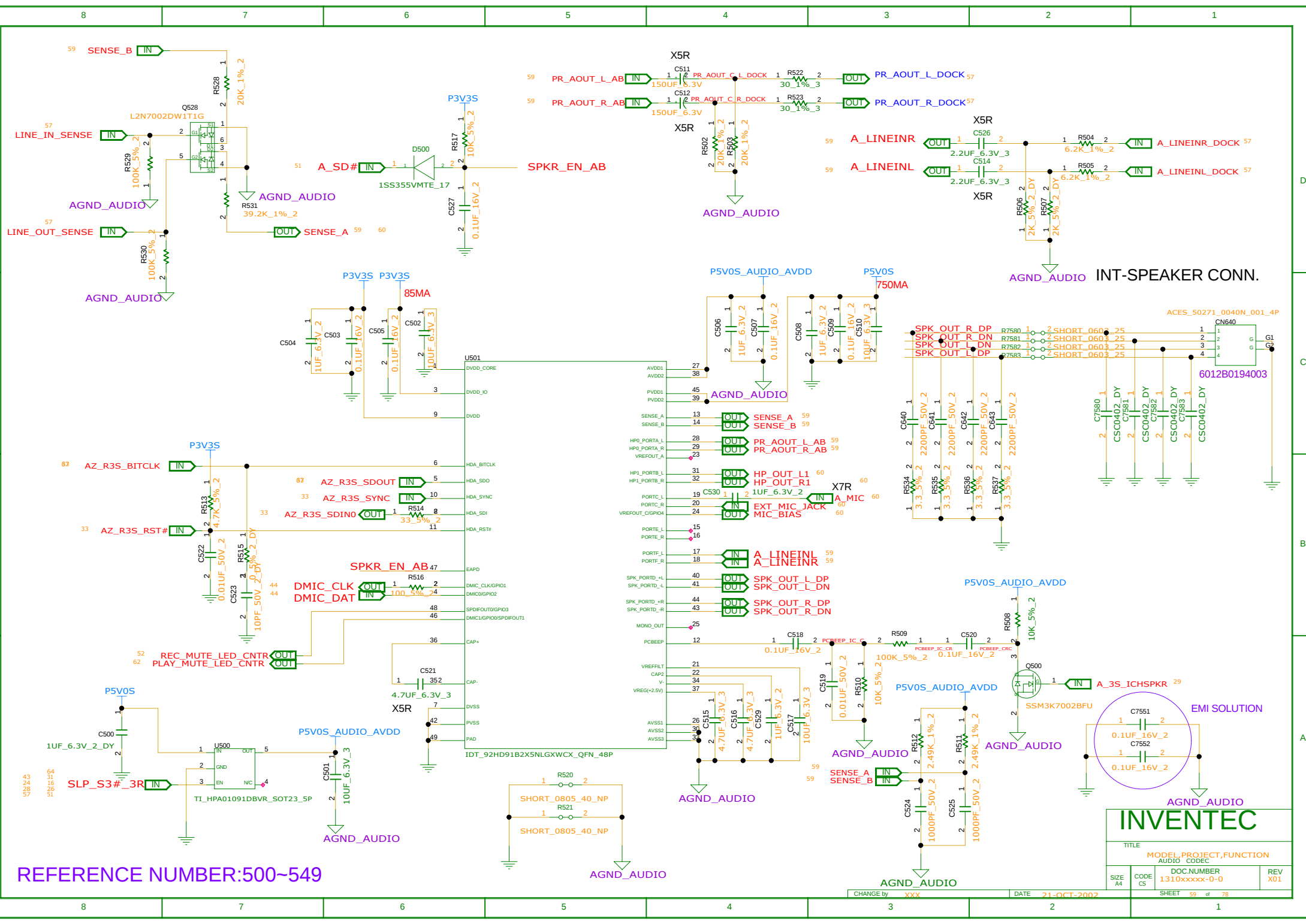
	5V	3.3V
R201	INSTALL	UNINSTALL
R202	INSTALL	UNINSTALL
R203	UNINSTALL	INSTALL
R204	INSTALL	UNINSTALL

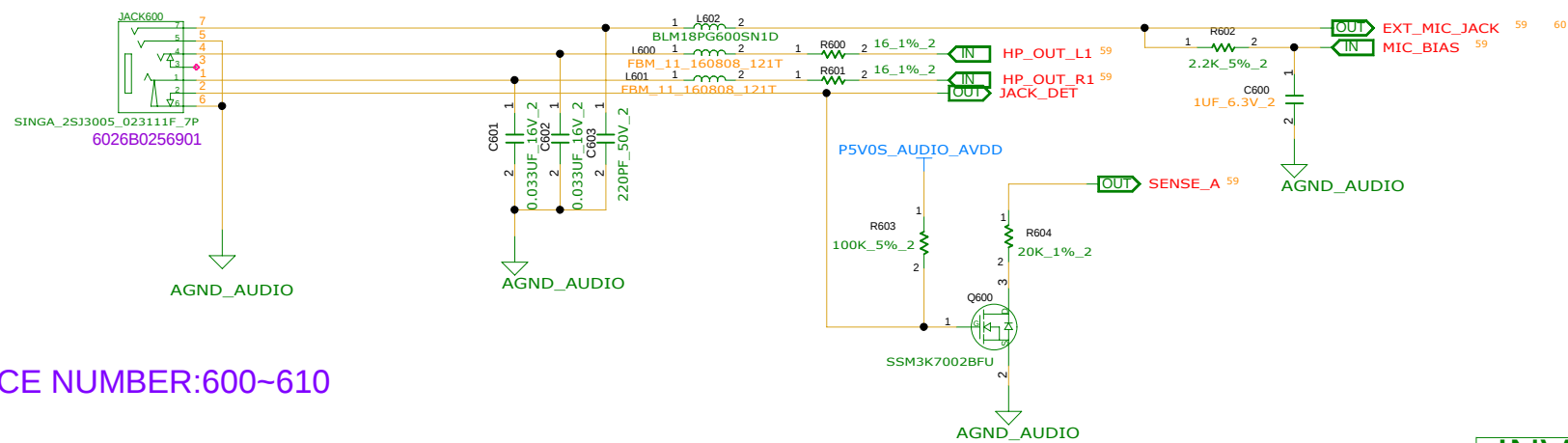
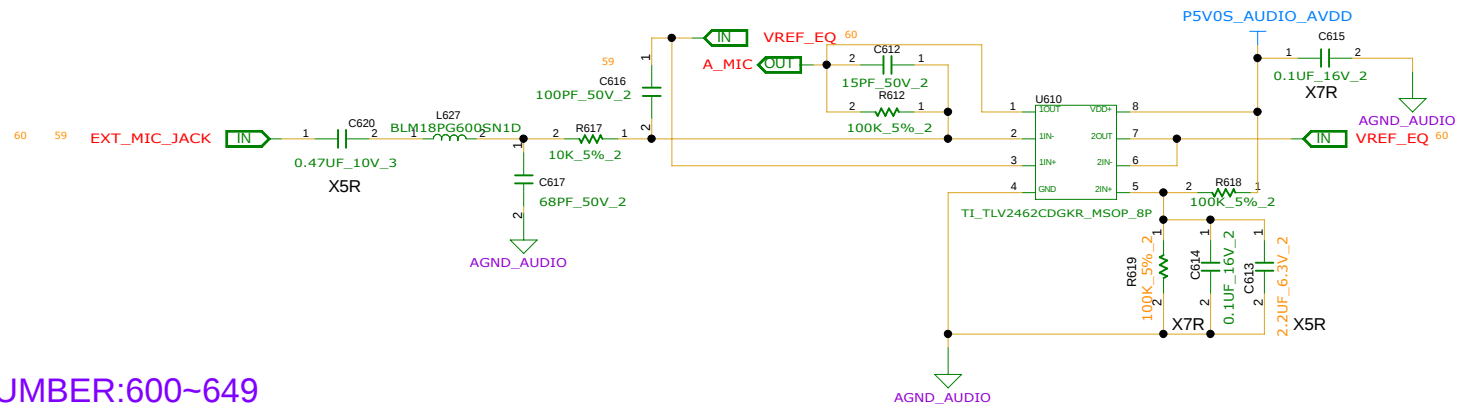


STICK POINT OPTION

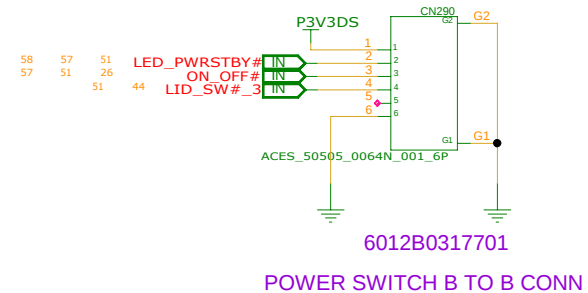
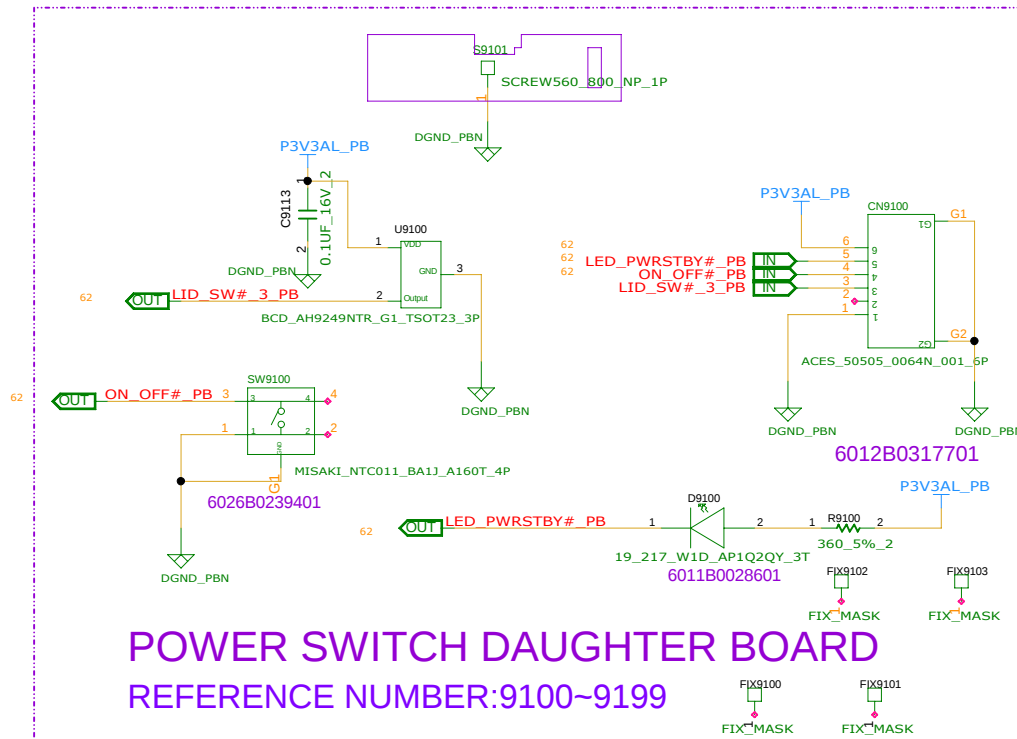
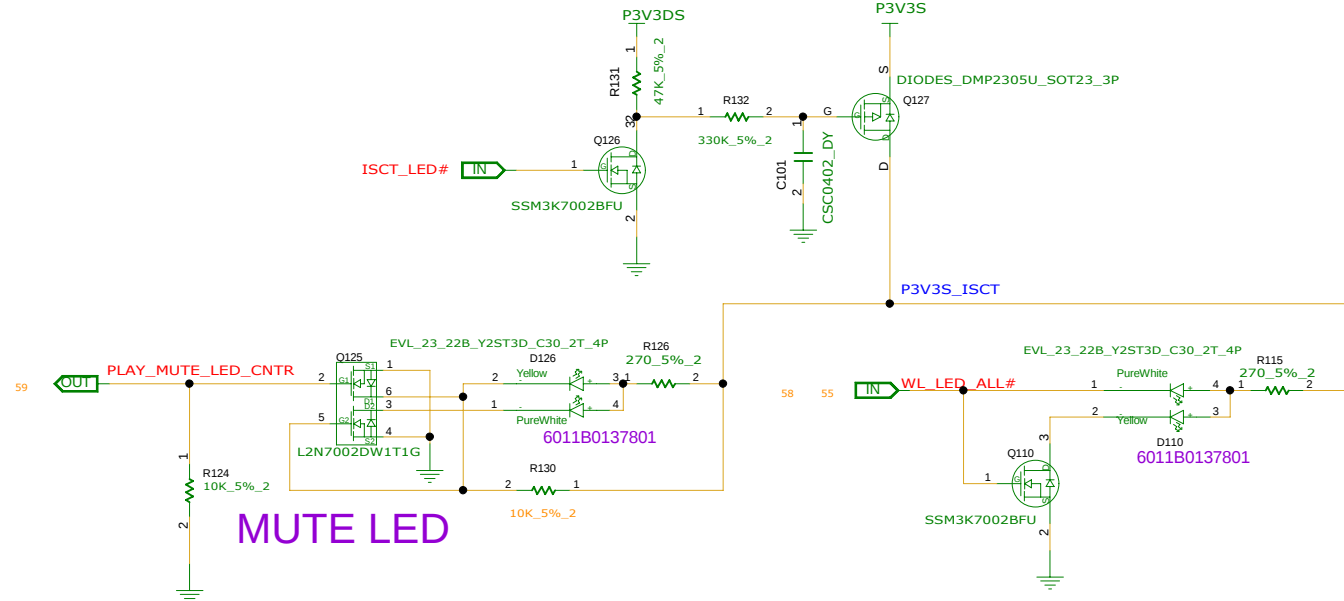
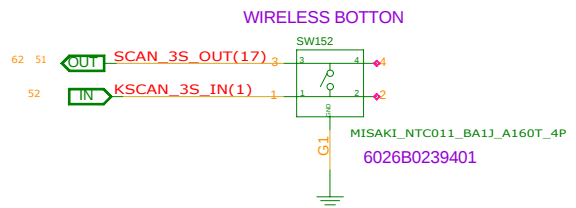
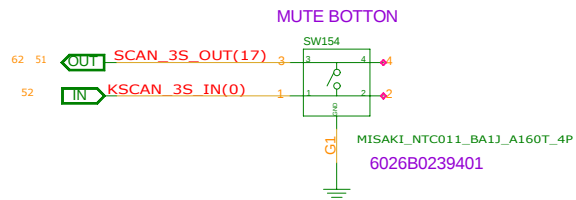
REFERENCE NUMBER:100~199

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
STICK POINT & B2B CNTR			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 58 of 78			

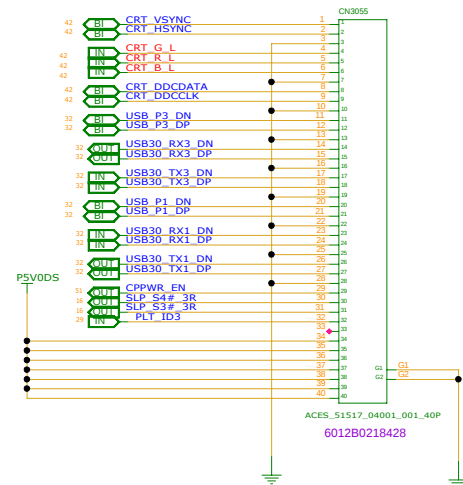
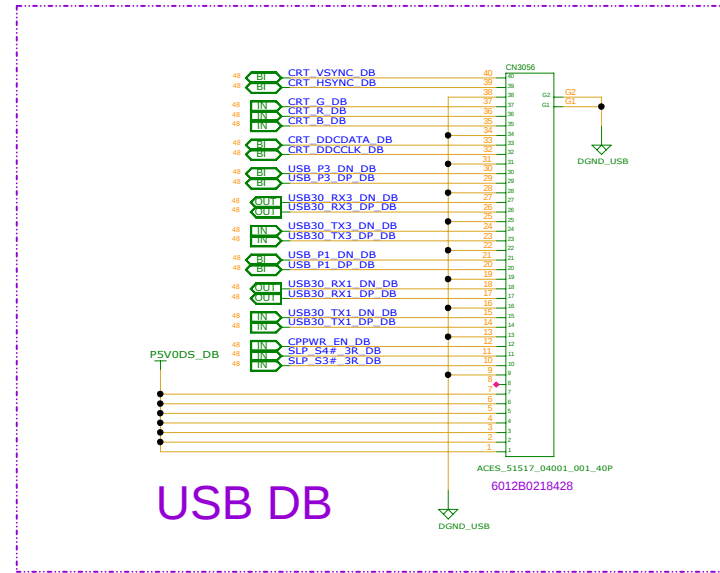




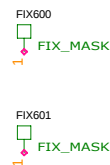
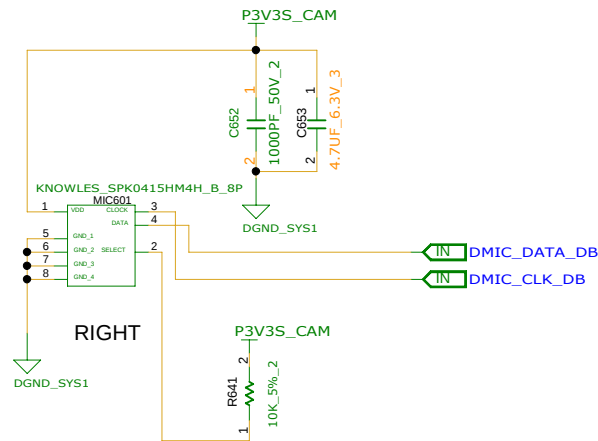
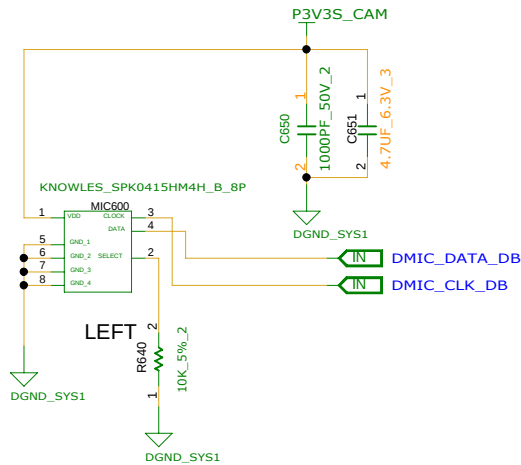
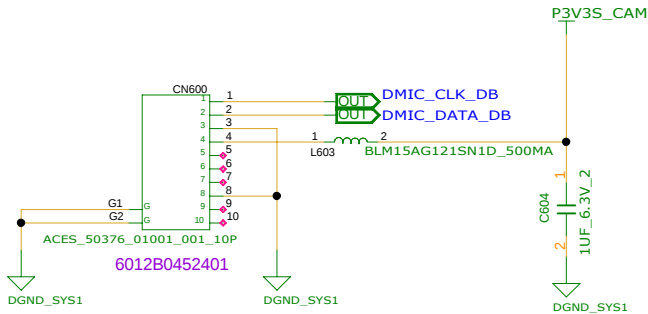
INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
EXT. MIC AMP. & AUDIO JACK			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 60 of 78			



INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
BUTTON_LED			
SIZE	CODE	DOC.NUMBER	REV
A3	C5	1310xxxx-0-0	X01
SHEET 62 of 78			

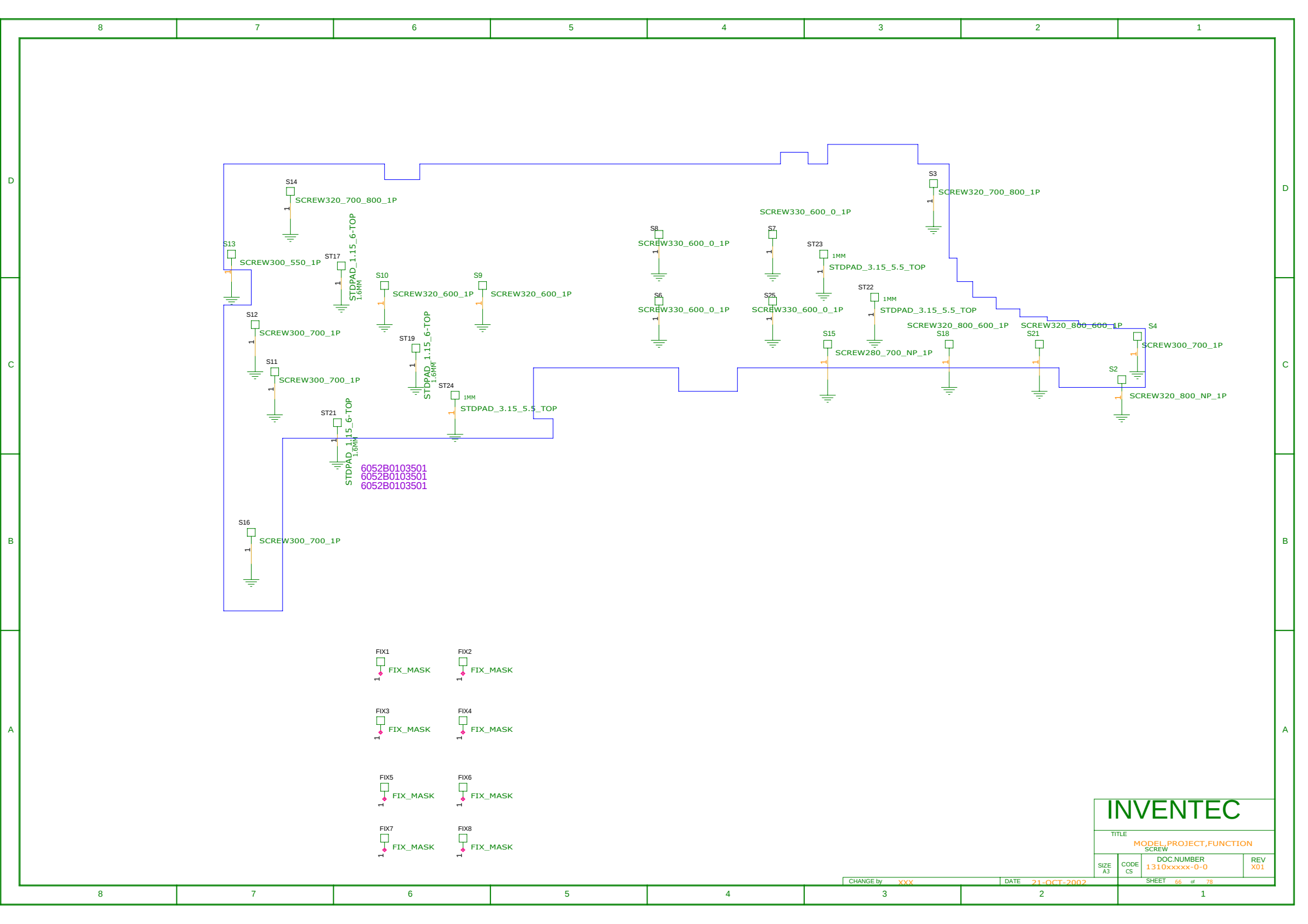


INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION				
RESERVE				
SIZE	CODE	DOC NUMBER	REV	
C	CS	1310XXXX-0-0	X01	
SHEET		64	of	68



REFERENCE NUMBER:600-649
MIC DOUGHTER BOARD

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 65 of 78			



6052B0103501
6052B0103501
6052B0103501

INVENTEC			
TITLE			
MODEL PROJECT, FUNCTION SCREW			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 66 of 78			

MLPS TABLE

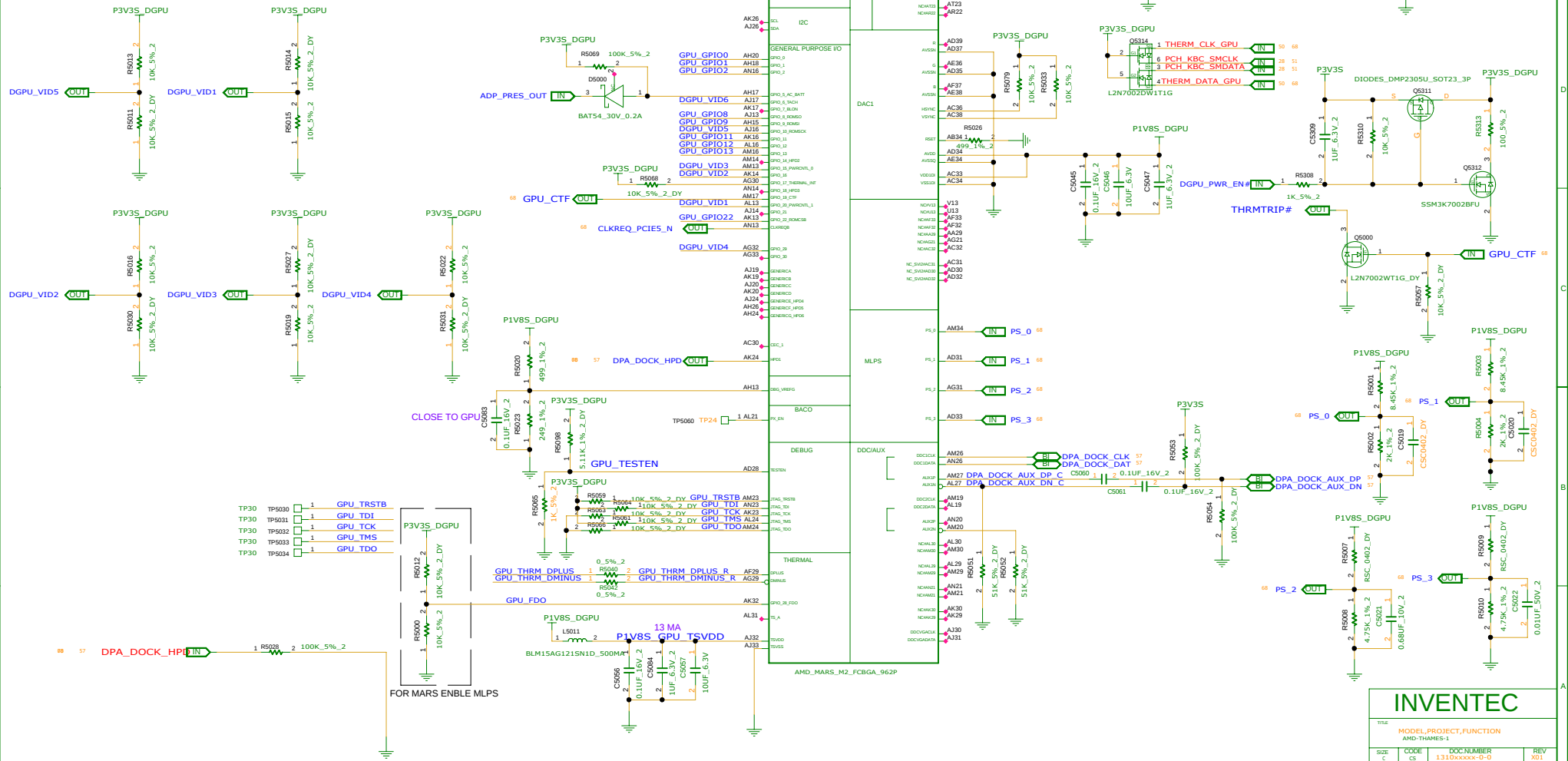
Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

Note: 0402 1% resistors are required.



LPT-LP GPIO 34	MARS MLPS Bit: PS_3 [3:1]			R _{pu} (Ω)	R _{pd} (Ω)	Vendor & PN	Die Ver.	
0	0	0	0	NC	4750	Samsung - K4G20325FD-FC04	D	GDDR5 - 64Mx32/128Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
	0	0	1	8450	2000	Hynix - H5GQ2H24AFR-T2C	A (Gemma)	GDDR5 - 64Mx32/128Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
1	1	1	0	3400	10000	*Samsung - K4G41325FC-HC04	C	*GDDR5 - 128Mx32/256Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
	1	1	1	4759	NC	*Hynix - H5GC4H24MFR-T0C	Huma	*GDDR5 - 128Mx32/256Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
VBIOS selection :	Vram configuration			Vendor ID		Vram information		
0 : VBIOS 1, 64Mx32 for 1GB sku	00: 64Mx32 (2Gb)			0: Samsung		* 2GB sku, TBD		
1 : VBIOS 2, 128Mx32 for 2GB sku	11: 128Mx32 (4Gb)			1: Hynix				
				Resistor Divider				
				Lookup Table				

MLPS Implementation

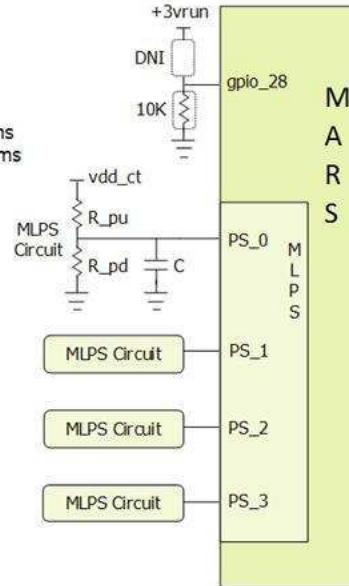
- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_{pu}, R_{pd} and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R _{pu} (Ohm)	R _{pd} (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111



MLPS Bit	Strap Name	Description
PS_0[1]	ROM_CONFIG[0]	See Primary Memory Aperture Sizes.
PS_0[2]	ROM_CONFIG[1]	
PS_0[3]	ROM_CONFIG[2]	
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap that indicates the number of audio-capable display outputs.
PS_1[1]	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 1 = The transmitter full-swing is enabled
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 1 = Tx deemphasis enabled.
PS_2[1]	N/A	Reserved.
PS_2[2]	N/A	Reserved.
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device.
PS_2[4]	STRAP_BIF_VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space). 0 = VGA controller capacity enabled.
PS_2[5]	N/A	Reserved
PS_2[1]	N/A	Reserved.
PS_2[2]	N/A	Reserved.
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device.
PS_2[4]	STRAP_BIF_VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space). 0 = VGA controller capacity enabled.
PS_2[5]	N/A	Reserved
PS_3[1]	BOARD_CONFIG[0]	See Board configuration related strapping, such as for memory ID.
PS_3[2]	BOARD_CONFIG[1]	
PS_3[3]	BOARD_CONFIG[2]	
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]	

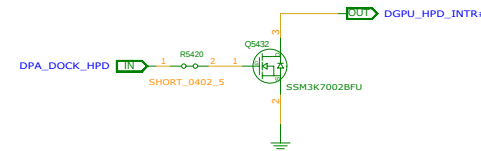
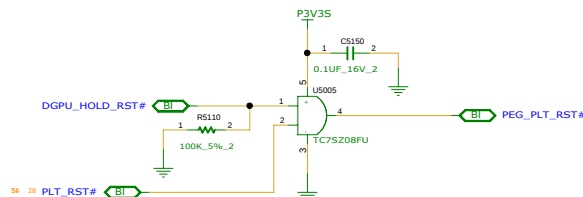
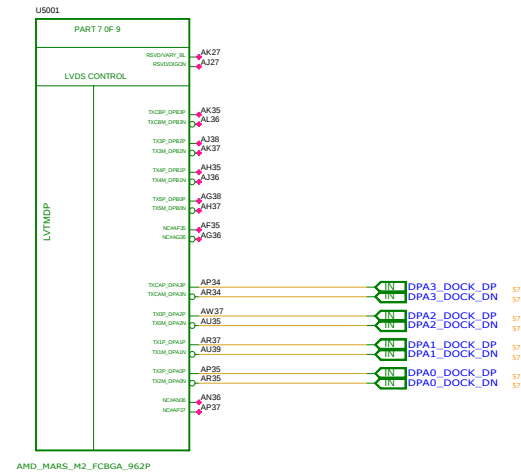
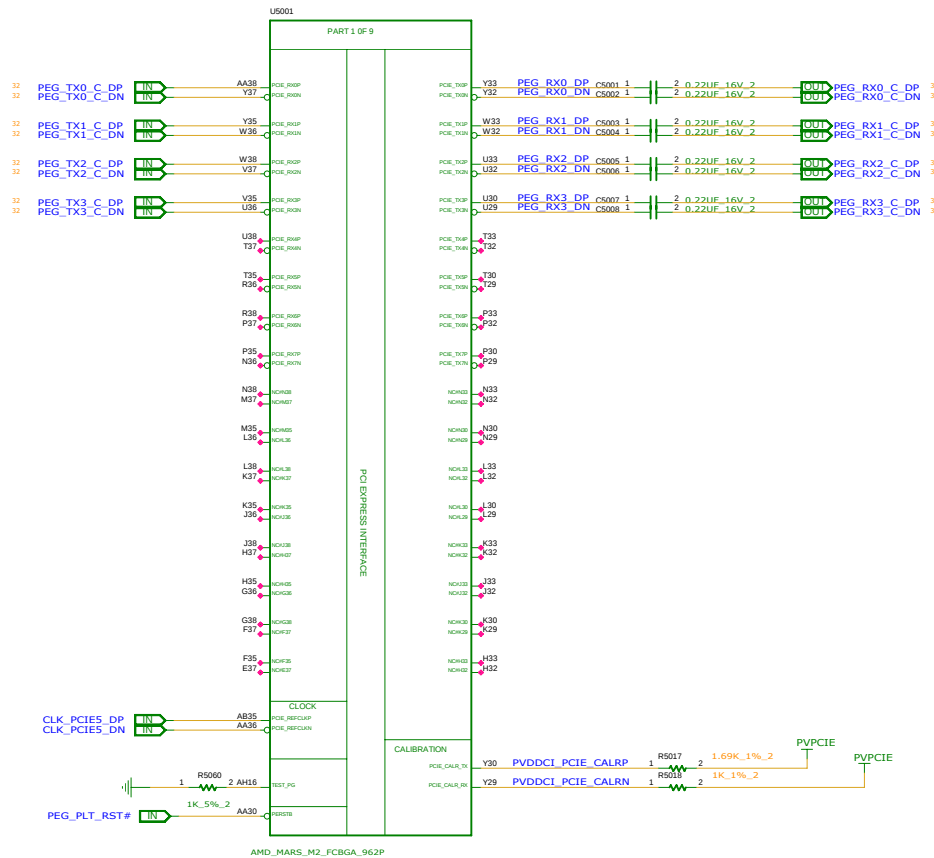
Note : AUD[1] (on HYSNC) and AUD[0] (on VSYNC) still need to be properly pin strapped even in a MLPS-based design.

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_cp[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_cp[1]			
PS_0[5]	aud_port_cp[0]			

INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310XXXX-0-0	201
SHEET		of	08

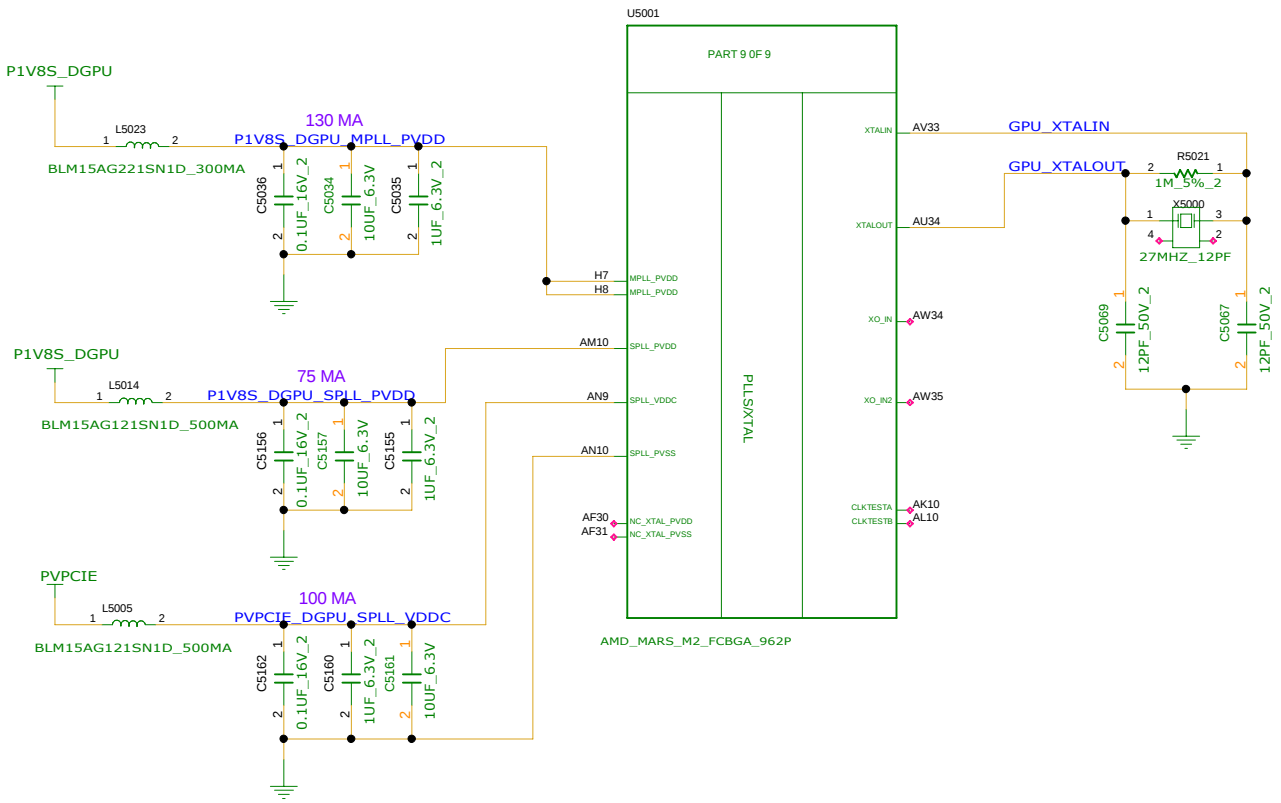
CHANGE BY: xxx DATE: 21-JULY-2007



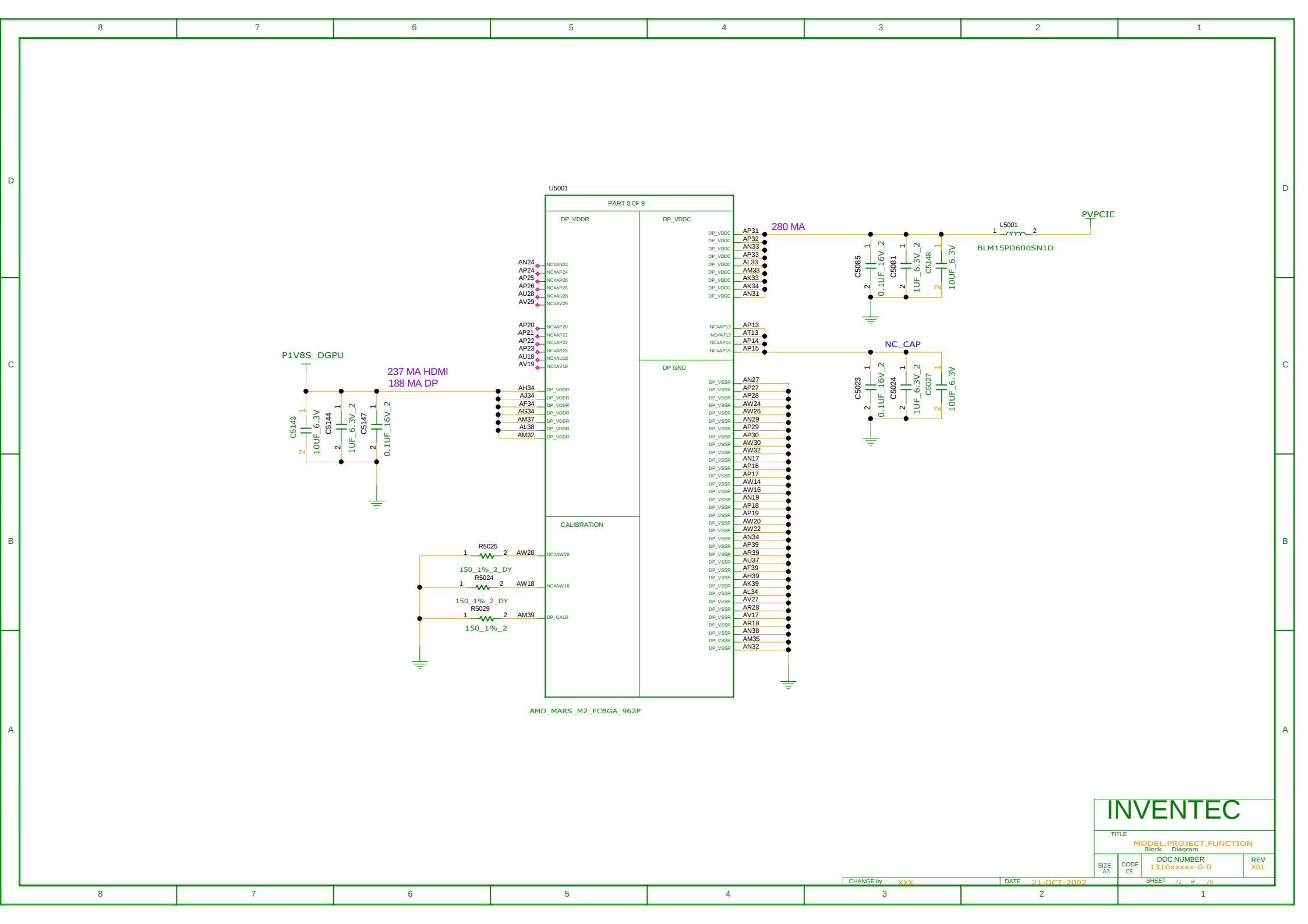
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	CS	13101000000-0-0	201
SHEET		of	10

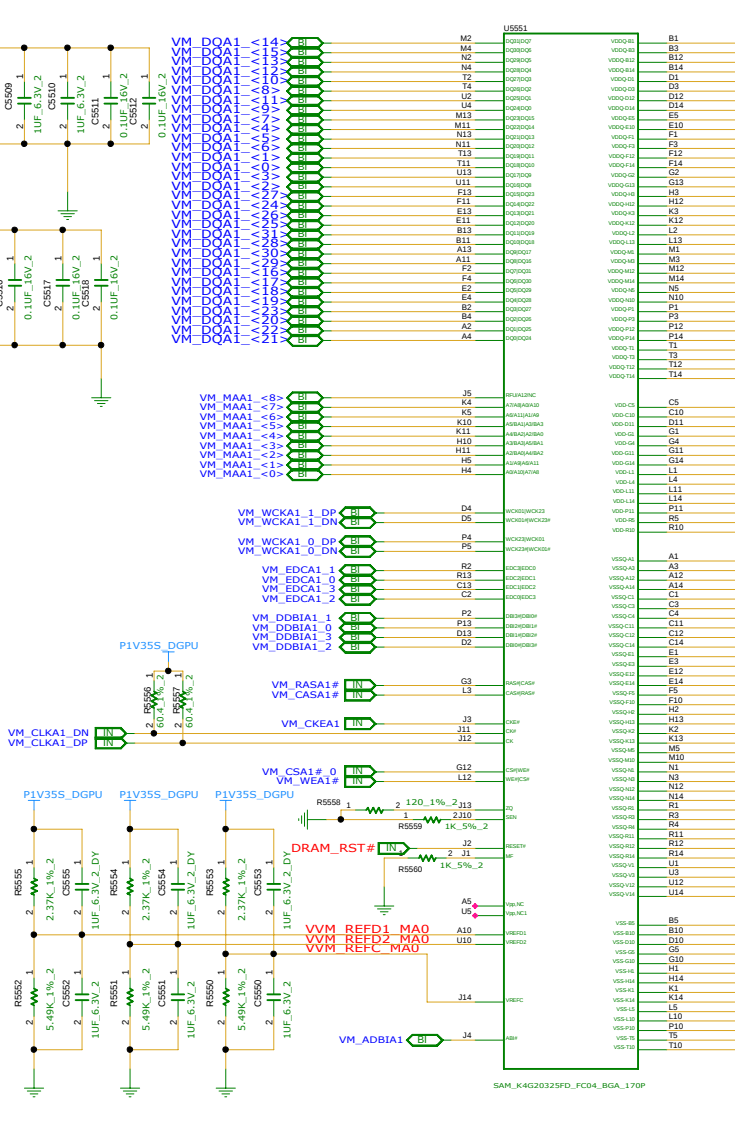
CHANGE BY: YXX DATE: 21-OCT-2002



INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 71 of 78			



	1
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SAM_K4G20325FD_FC04_BGA_170

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxxx-0-0	REV X01
SHEET 78 of 78			