

Compal confidential

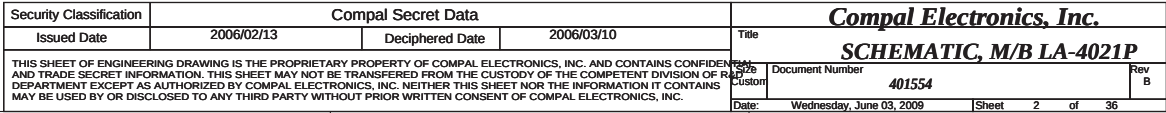
Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM+ICH9-M SFF core logic

SKYY

2008-07-29

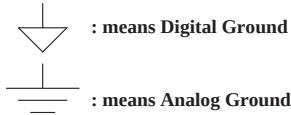
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	SCHEMATIC, M/B LA-4021P	
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Voltage Rails (0 MEANS ON X MEANS OFF)

power plane State	+B	+5VALW +3VALW +3VM +1.05VM	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +0.9V
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



@ : means just reserve , no build
CONN@ : means ME part.
45@ : means install after SMT.

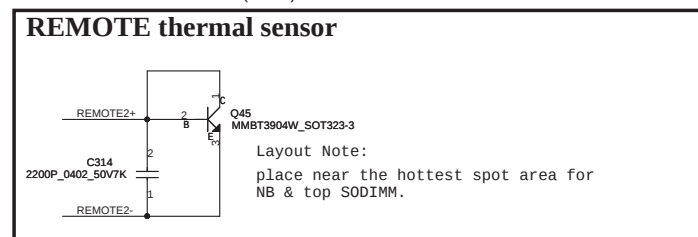
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

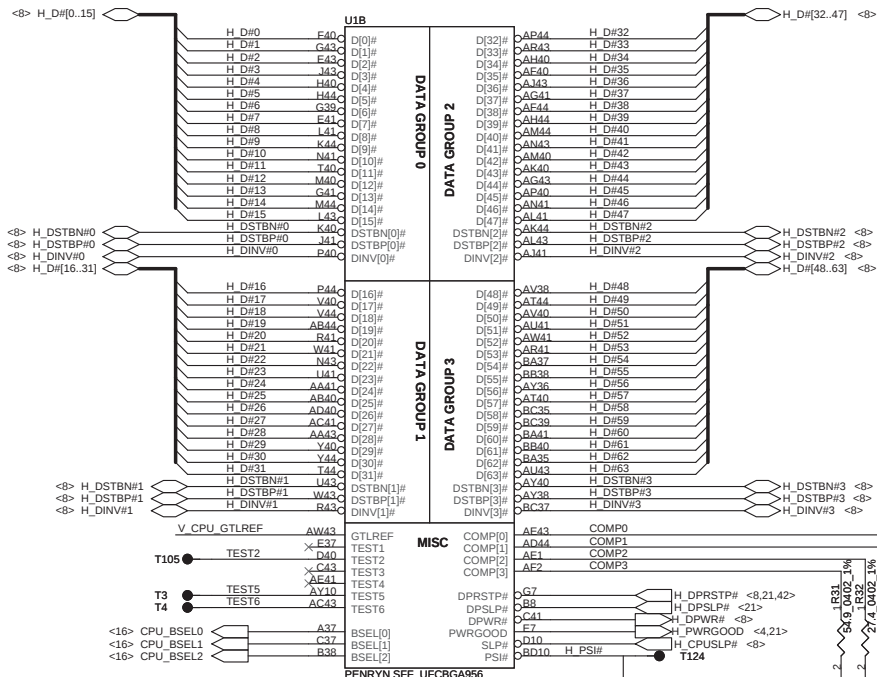
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
CLOCK GENERATOR (EXT.)	D2	11010010

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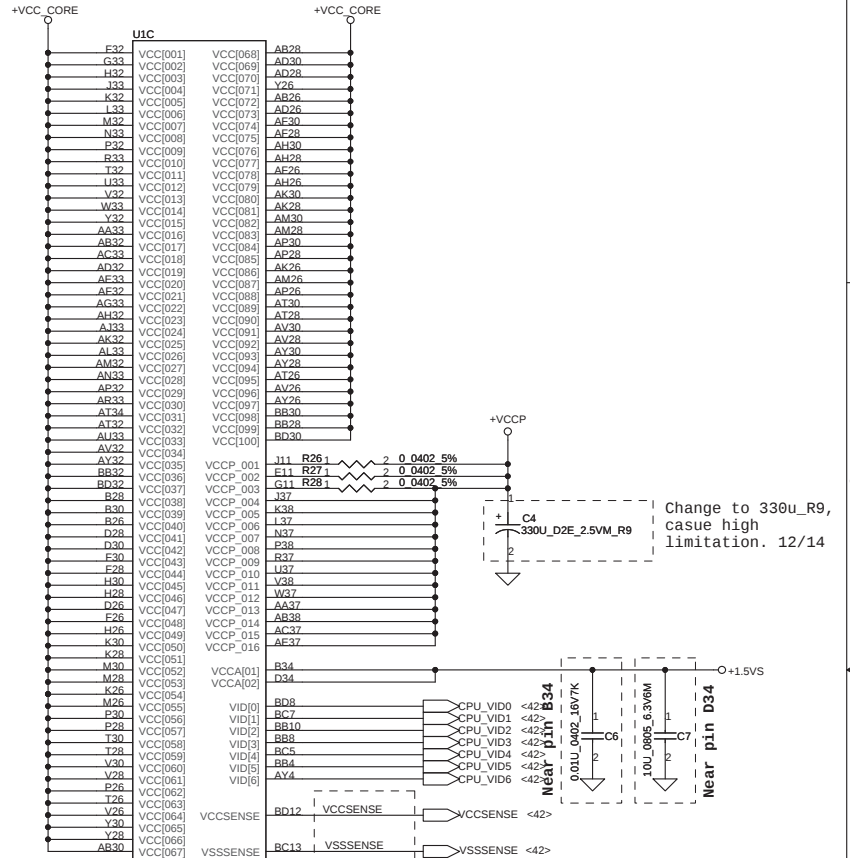
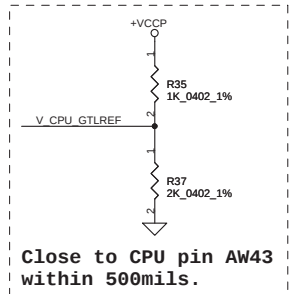


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPS

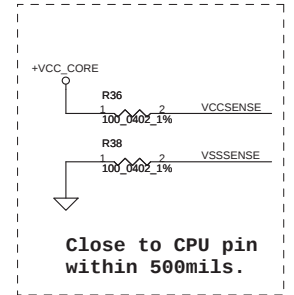
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

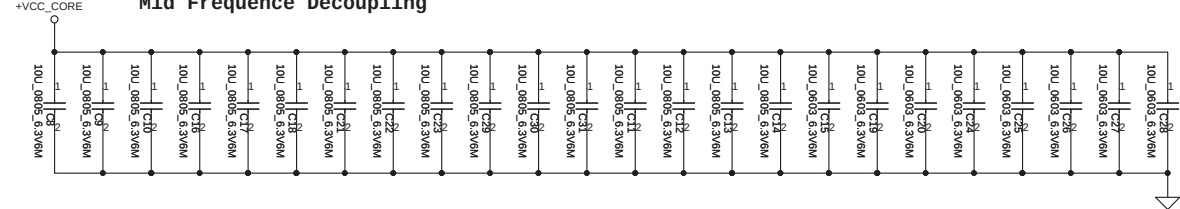


Length match within 25 mils. The trace width/space/other is 20/7/25.

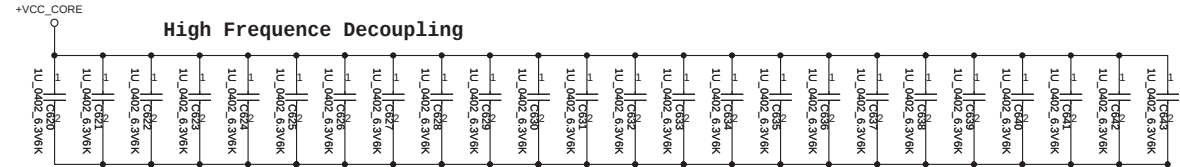


UID			UIE				
B42	VSS[001]	VSS[082]	AM36	G25	VSS_164	VSS_280	AA15
F44	VSS[002]	VSS[083]	AR35	G23	VSS_165	VSS_281	AC15
D44	VSS[003]	VSS[084]	AI35	G21	VSS_166	VSS_282	AD10
D42	VSS[004]	VSS[085]	AV34	J25	VSS_167	VSS_283	AH12
F42	VSS[005]	VSS[086]	AW35	J23	VSS_168	VSS_284	AE15
H42	VSS[006]	VSS[087]	AW33	J21	VSS_169	VSS_285	AG15
K42	VSS[007]	VSS[088]	AY34	L26	VSS_170	VSS_286	AI15
M42	VSS[008]	VSS[089]	AT36	L23	VSS_171	VSS_287	AJ15
P42	VSS[009]	VSS[090]	AV36	L21	VSS_172	VSS_288	AH10
T42	VSS[010]	VSS[091]	BA33	N25	VSS_173	VSS_289	AM12
Y42	VSS[011]	VSS[092]	BB36	N23	VSS_174	VSS_290	AN15
AB42	VSS[012]	VSS[093]	BB36	N21	VSS_175	VSS_291	AR15
AD42	VSS[014]	VSS[094]	BD36	R25	VSS_176	VSS_292	AM10
AE42	VSS[015]	VSS[095]	C27	R23	VSS_177	VSS_293	AT12
AH42	VSS[016]	VSS[096]	C29	R21	VSS_178	VSS_294	AV12
AK42	VSS[017]	VSS[097]	E29	U25	VSS_179	VSS_295	AW13
AM42	VSS[018]	VSS[098]	E27	U23	VSS_180	VSS_296	AW11
AP42	VSS[019]	VSS[099]	G29	W25	VSS_181	VSS_297	AY12
AV44	VSS[020]	VSS[100]	G29	W23	VSS_182	VSS_298	AU15
AV44	VSS[020]	VSS[101]	F31	W21	VSS_183	VSS_299	AW15
AT42	VSS[021]	VSS[102]	F31	AA25	VSS_184	VSS_300	AT10
AV42	VSS[023]	VSS[104]	J29	AA23	VSS_185	VSS_301	BA13
BA43	VSS[024]	VSS[105]	I27	AA21	VSS_186	VSS_302	BA11
BA43	VSS[025]	VSS[106]	L29	AC25	VSS_187	VSS_303	BB12
CB42	VSS[026]	VSS[107]	L27	AC23	VSS_188	VSS_304	BC11
C39	VSS[027]	VSS[108]	N29	AC21	VSS_189	VSS_305	BA15
F39	VSS[028]	VSS[109]	M27	AE25	VSS_190	VSS_306	BC15
G37	VSS[029]	VSS[110]	I31	AE23	VSS_191	VSS_307	B6
H38	VSS[030]	VSS[111]	I31	AE21	VSS_192	VSS_308	D6
I39	VSS[031]	VSS[112]	N31	AG25	VSS_194	VSS_310	E9
M38	VSS[032]	VSS[113]	R29	AG23	VSS_195	VSS_311	G8
N39	VSS[033]	VSS[114]	I29	AG21	VSS_196	VSS_312	H6
N39	VSS[034]	VSS[115]	I29	AJ25	VSS_197	VSS_313	I3
R39	VSS[035]	VSS[116]	I27	AJ23	VSS_198	VSS_314	K8
T38	VSS[036]	VSS[117]	R31	AL25	VSS_199	VSS_315	K6
U39	VSS[037]	VSS[118]	W29	AL23	VSS_200	VSS_316	M8
W39	VSS[038]	VSS[119]	W27	AL21	VSS_201	VSS_317	PR
Y38	VSS[039]	VSS[120]	W31	AN25	VSS_202	VSS_318	PR
AA39	VSS[040]	VSS[121]	AA29	AN23	VSS_203	VSS_319	PR
AD38	VSS[041]	VSS[122]	AA27	AN21	VSS_204	VSS_320	PR
AE39	VSS[042]	VSS[123]	AC29	AR25	VSS_205	VSS_321	PR
AG39	VSS[043]	VSS[124]	AC27	AR23	VSS_206	VSS_322	PR
AG39	VSS[044]	VSS[125]	AC31	AR21	VSS_207	VSS_323	PR
AH38	VSS[045]	VSS[126]	AC31	AU25	VSS_208	VSS_324	PR
AI39	VSS[046]	VSS[127]	AE29	AU23	VSS_209	VSS_325	PR
AL39	VSS[047]	VSS[128]	AE27	AU21	VSS_210	VSS_326	PR
AM38	VSS[048]	VSS[129]	AG29	AW25	VSS_211	VSS_327	PR
AN39	VSS[049]	VSS[130]	AG27	AW23	VSS_212	VSS_328	PR
AR39	VSS[050]	VSS[131]	AJ29	AW21	VSS_213	VSS_329	PR
AR37	VSS[051]	VSS[132]	AJ27	BA25	VSS_214	VSS_330	PR
AT38	VSS[052]	VSS[133]	AJ27	BA23	VSS_215	VSS_331	PR
AU39	VSS[053]	VSS[134]	AE31	BA21	VSS_216	VSS_332	PR
AU37	VSS[054]	VSS[135]	AG31	BC25	VSS_217	VSS_333	PR
AW39	VSS[055]	VSS[136]	AJ31	BC23	VSS_218	VSS_334	PR
AW37	VSS[056]	VSS[137]	AI29	BC25	VSS_219	VSS_335	PR
BA39	VSS[057]	VSS[138]	AI27	BC21	VSS_220	VSS_336	PR
BC41	VSS[058]	VSS[139]	AN29	C17	VSS_221	VSS_337	PR
BD40	VSS[059]	VSS[140]	AN27	C19	VSS_222	VSS_338	PR
BD38	VSS[060]	VSS[141]	AI31	E17	VSS_223	VSS_339	PR
R36	VSS[061]	VSS[142]	AN31	E19	VSS_224	VSS_340	PR
D36	VSS[062]	VSS[143]	AR29	G19	VSS_225	VSS_341	PR
D36	VSS[063]	VSS[144]	AR27	G17	VSS_226	VSS_342	PR
M34	VSS[064]	VSS[145]	AR31	J19	VSS_227	VSS_343	PR
M36	VSS[065]	VSS[146]	AU29	J17	VSS_228	VSS_344	PR
P34	VSS[066]	VSS[147]	AU27	I19	VSS_229	VSS_345	PR
T34	VSS[067]	VSS[148]	AW29	I17	VSS_230	VSS_346	PR
Y34	VSS[068]	VSS[149]	AW27	N19	VSS_231	VSS_347	PR
AB34	VSS[069]	VSS[150]	AU31	N17	VSS_232	VSS_348	PR
AD34	VSS[070]	VSS[151]	AW31	R19	VSS_233	VSS_349	PR
AD36	VSS[071]	VSS[152]	AI39	R17	VSS_234	VSS_350	PR
AD34	VSS[072]	VSS[153]	BA27	R19	VSS_235	VSS_351	PR
Y36	VSS[073]	VSS[154]	BC29	U17	VSS_236	VSS_352	PR
Y36	VSS[074]	VSS[155]	BC27	W19	VSS_237	VSS_353	PR
AE34	VSS[075]	VSS[156]	BA31	W17	VSS_238	VSS_354	PR
AH34	VSS[076]	VSS[157]	RC31	AA19	VSS_239	VSS_355	PR
AH34	VSS[077]	VSS[158]	RC21	AA17	VSS_240	VSS_356	PR
AH36	VSS[078]	VSS[159]	C23	AC19	VSS_241	VSS_357	PR
AK34	VSS[079]	VSS[160]	BA29	AC17	VSS_242	VSS_358	PR
AK34	VSS[079]	VSS[160]	E25	AE19	VSS_243	VSS_359	PR
AP34	VSS[080]	VSS[161]	E23	AE17	VSS_244	VSS_360	PR
AP34	VSS[081]	VSS[162]	F21	AG19	VSS_245	VSS_361	PR
		VSS[163]	F21	AG17	VSS_246	VSS_362	PR
				AI19	VSS_247	VSS_363	PR
				AI17	VSS_248	VSS_364	PR
				AI19	VSS_249	VSS_365	PR
				AI17	VSS_250	VSS_366	PR
				AN17	VSS_251	VSS_367	PR
				AN17	VSS_252	VSS_368	PR
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				AW19	VSS_257	VSS_373	PR
				AW17	VSS_258	VSS_374	PR
				BA19	VSS_259	VSS_375	PR
				BA17	VSS_260	VSS_376	PR
				BA17	VSS_261	VSS_377	PR
				BC17	VSS_262	VSS_378	PR
				C11	VSS_263	VSS_379	PR
				C15	VSS_264	VSS_380	PR
				E15	VSS_265	VSS_381	PR
				G15	VSS_266	VSS_382	PR
				H10	VSS_267	VSS_383	PR
				M12	VSS_268	VSS_384	PR
				J15	VSS_269	VSS_385	PR
				I15	VSS_270	VSS_386	PR
				N15	VSS_271	VSS_387	PR
				T12	VSS_272	VSS_388	PR
				R15	VSS_273	VSS_389	PR
				T14	VSS_274	VSS_390	PR
				W15	VSS_275	VSS_391	PR
				U10	VSS_276	VSS_392	PR
				T12	VSS_277	VSS_393	PR
				Y12	VSS_278	VSS_394	PR
				AD12	VSS_279	VSS_395	PR
							BD4
PENRRYN SFF_UFCBGA956			PENRRYN SFF_UFCBGA956				

Mid Frequency Decoupling



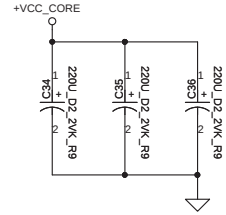
High Frequency Decoupling



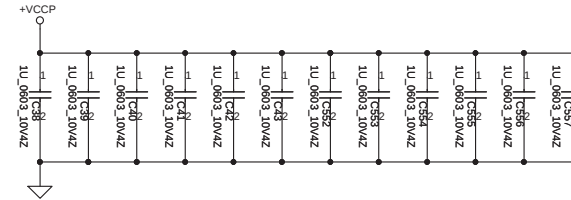
6/14 :Replace 12pcs 10uF_0805 to 24 pcs 1uF_0402 for CPU transient fail issue.

ESR <= 1.5m ohm

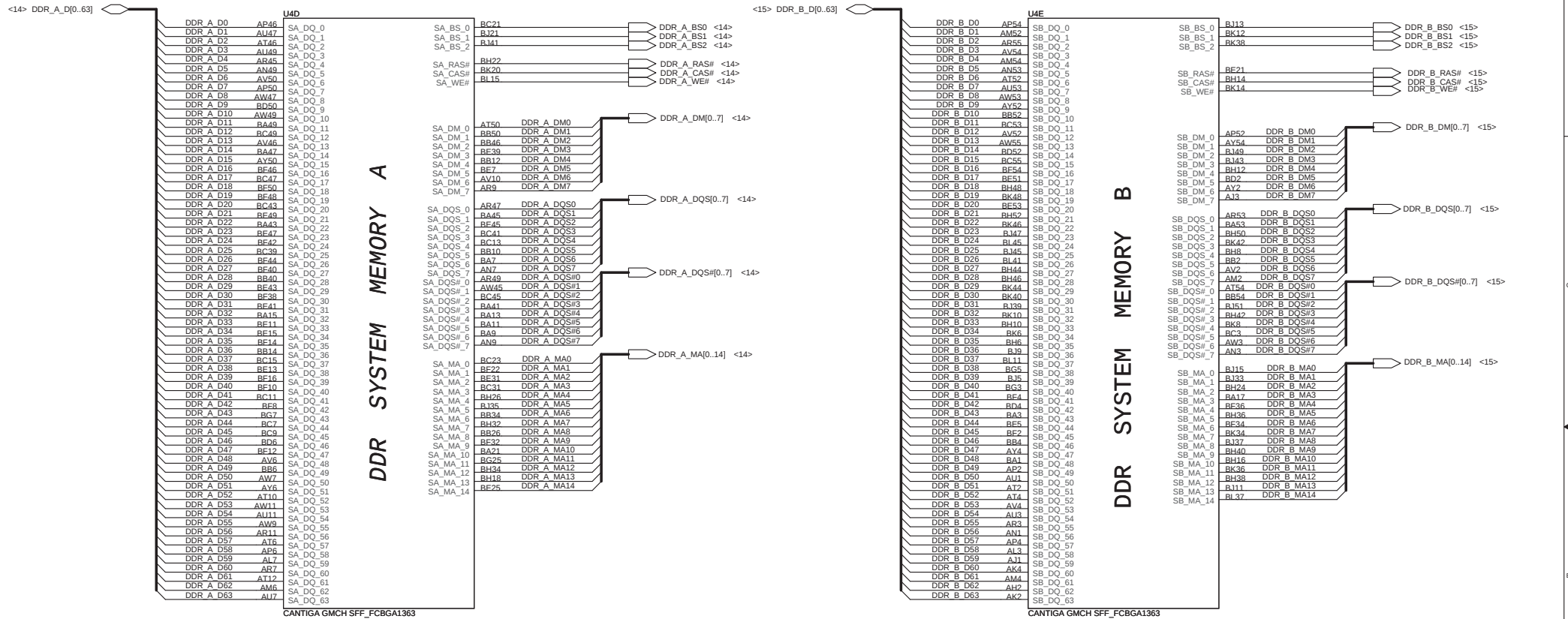
Near CPU CORE regulator

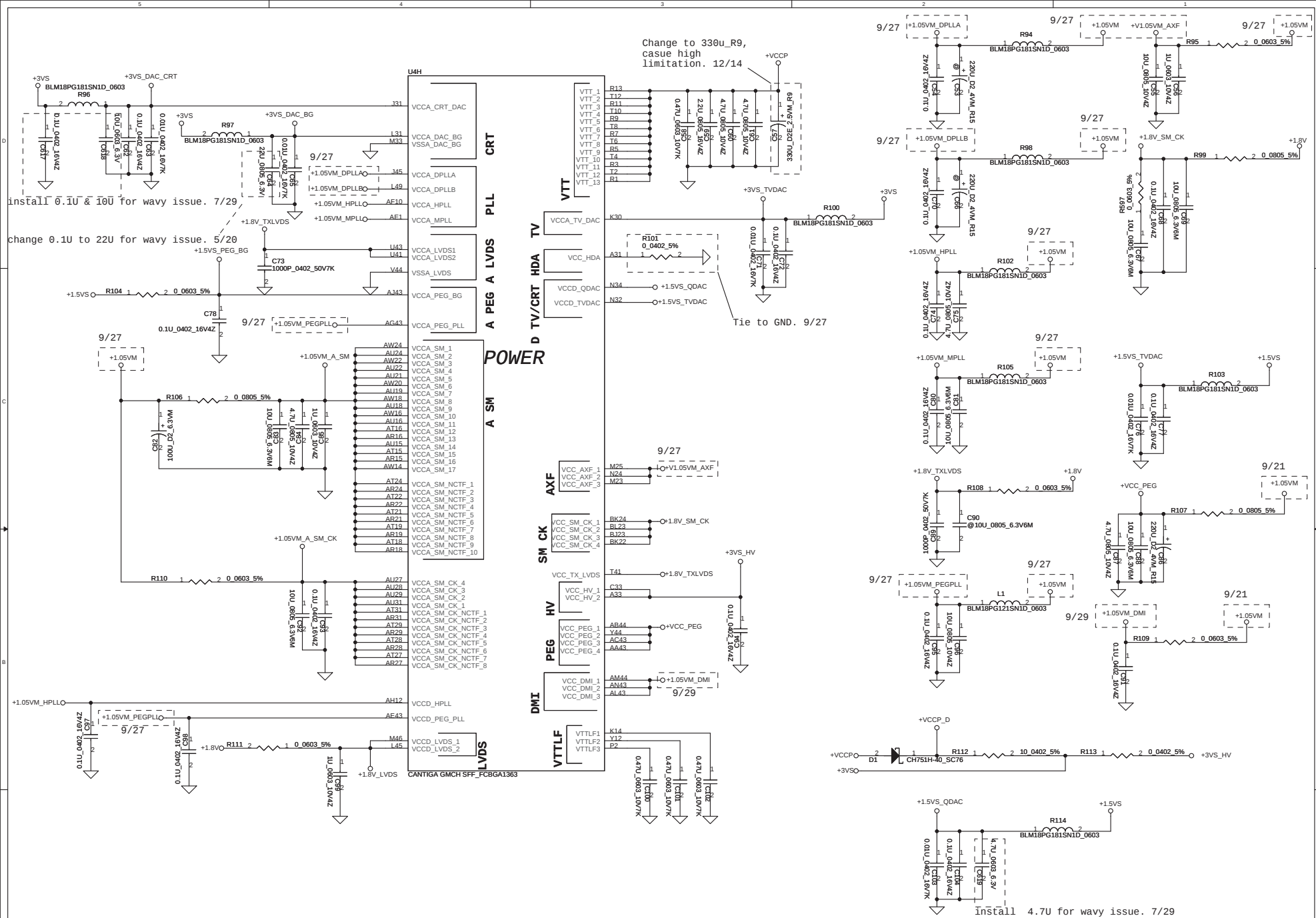


Del C37 to improve power plan. 6/14

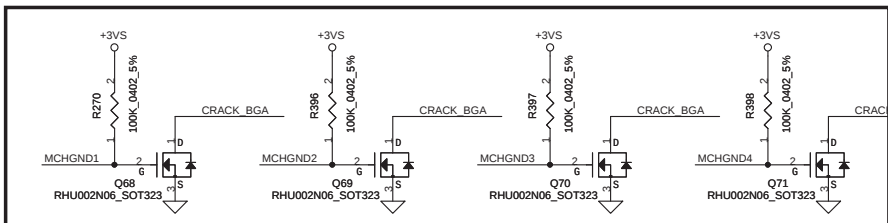
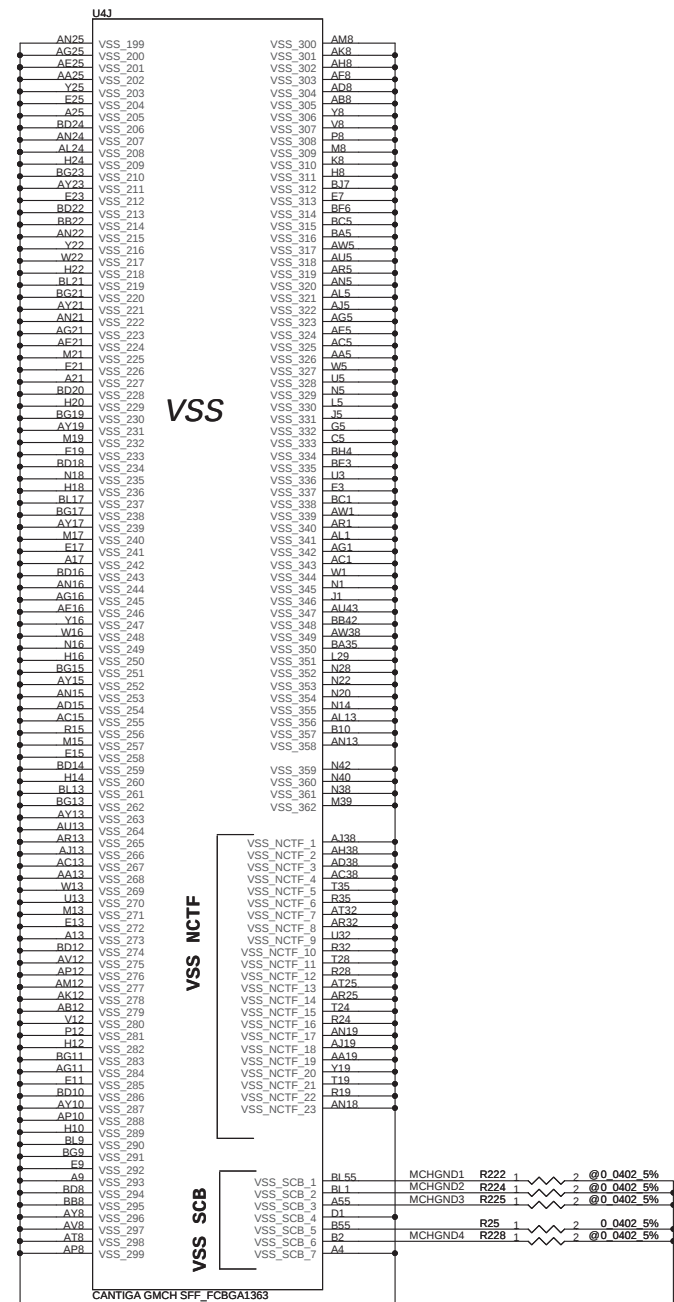
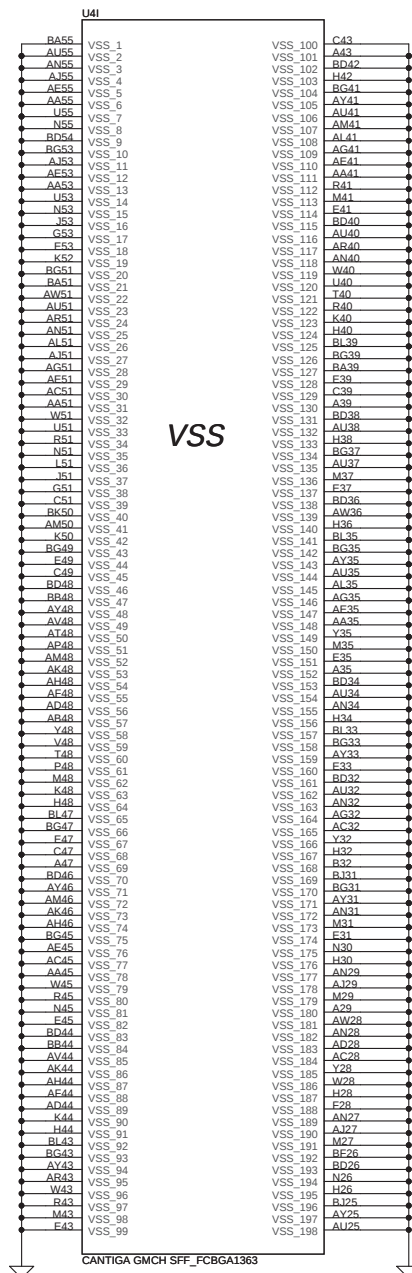


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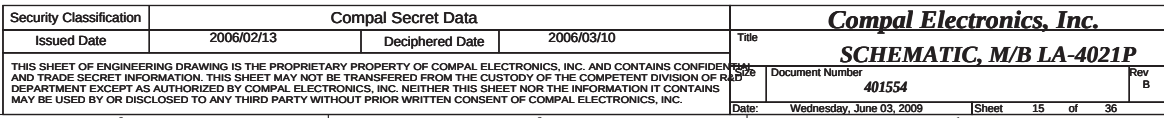


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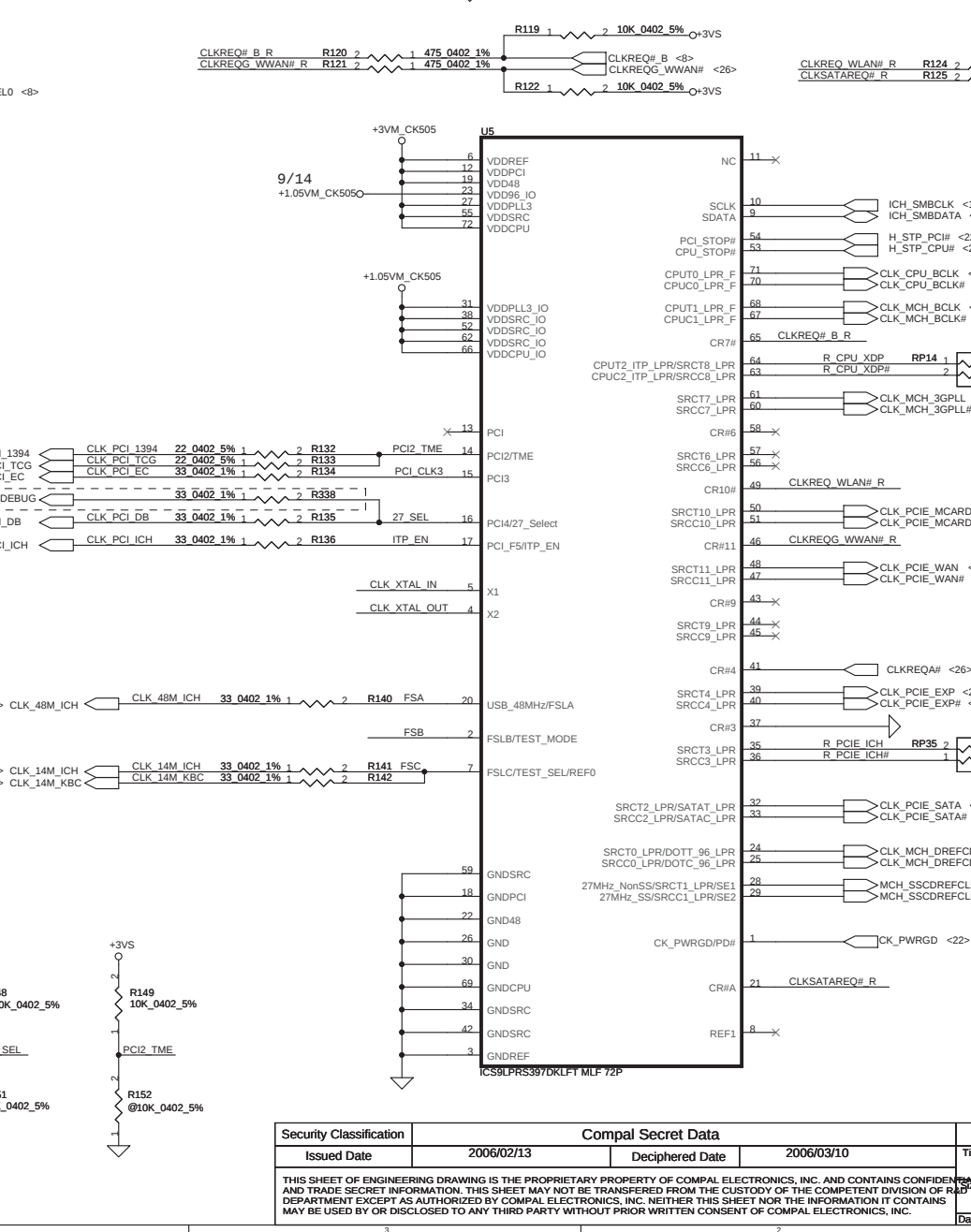


The three diagrams illustrate the connection of CPU_BSEL0, CPU_BSEL1, and CPU_BSEL2 to the +VCCP supply. Each diagram includes a pull-up resistor (R127, R137, R144) and a pull-down resistor (R131, R62, R146) to ground. The diagrams are labeled with component values and reference designators.

Diagram 1 (CPU_BSEL0): Shows the connection of CPU_BSEL0 to +VCCP. The pull-up resistor R127 is 56K_0402_5%. The pull-down resistor R131 is 1K_0402_5%. The signal line is labeled FSA.

Diagram 2 (CPU_BSEL1): Shows the connection of CPU_BSEL1 to +VCCP. The pull-up resistor R137 is 1K_0402_5%. The pull-down resistor R62 is 0_0402_5%. The signal line is labeled FSB. A note indicates "Add for port8 port.".

Diagram 3 (CPU_BSEL2): Shows the connection of CPU_BSEL2 to +VCCP. The pull-up resistor R144 is 1K_0402_5%. The pull-down resistor R146 is 0_0402_5%. The signal line is labeled FSC. A note indicates "Install. 11/06".



Place close to U5

2 1%
2 1%

R123 1

2 10K 0402 5%

3V

CLKREQ_WLAN# <26>
CLK_SATAREQ# <22>

R126 1

2 10K 0402 5%

3V

2 5%

CLK_CPU_XDP <4>
CLK_CPU_XDP# <4>

2 5%

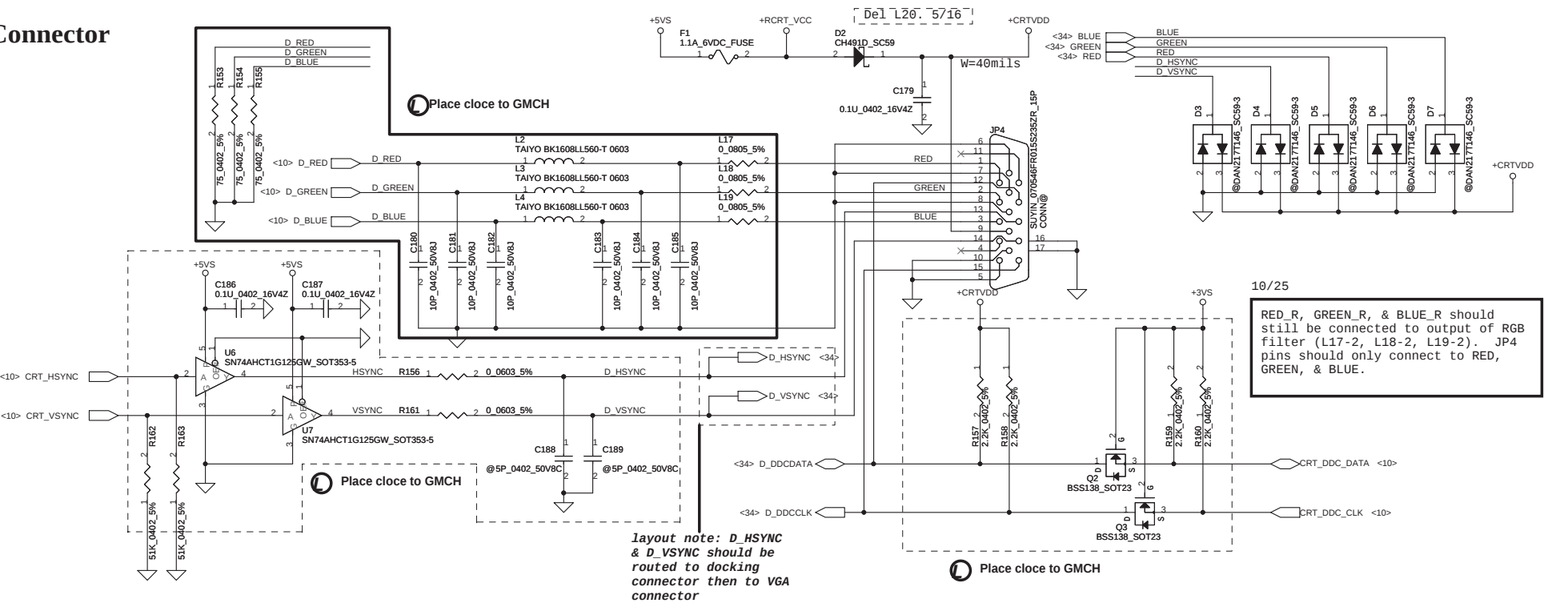
CLK_PCIE_ICH <22>
CLK_PCIE_ICH# <22>

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CHEMATIC, M/B LA-4021

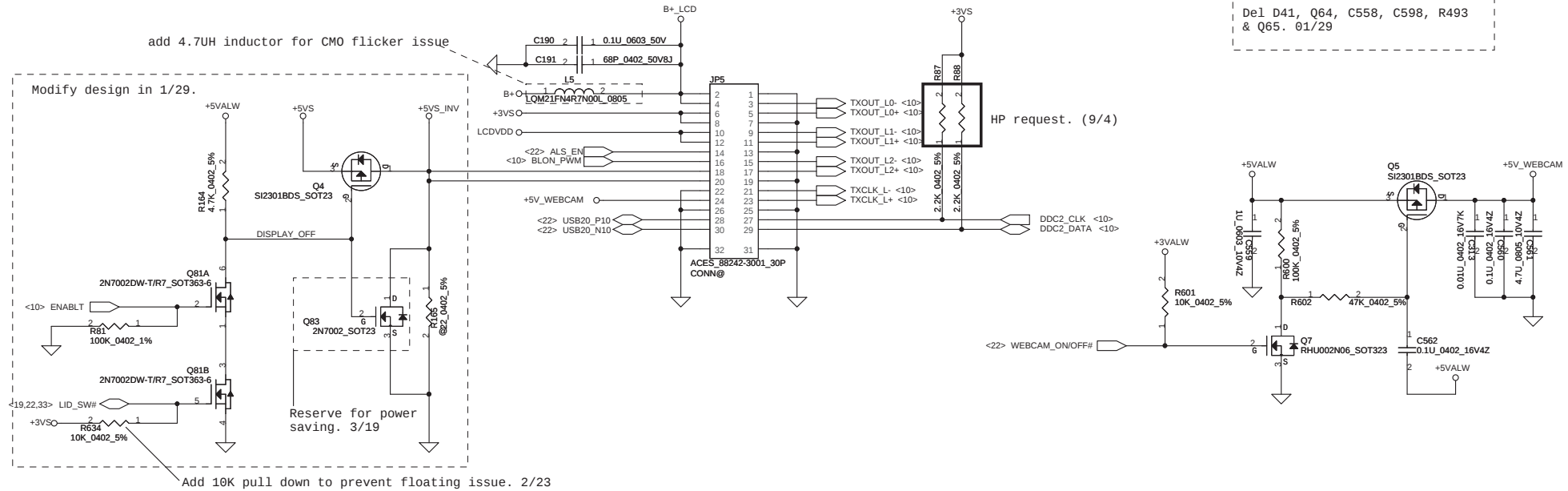
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Place close to U5

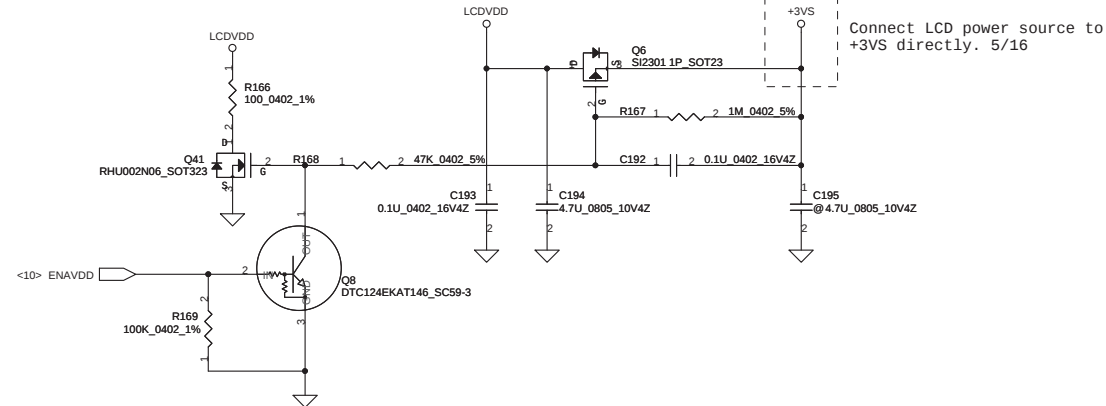
CRT Connector



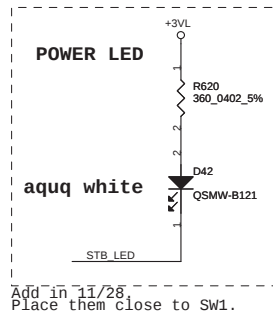
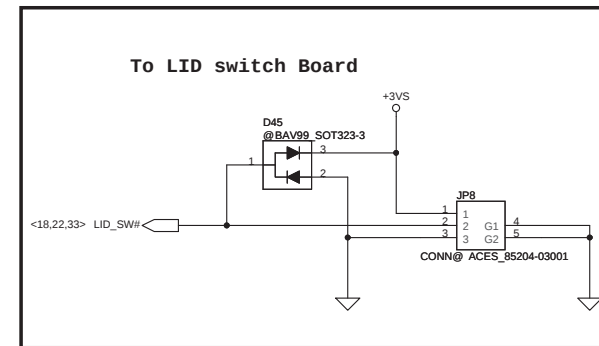
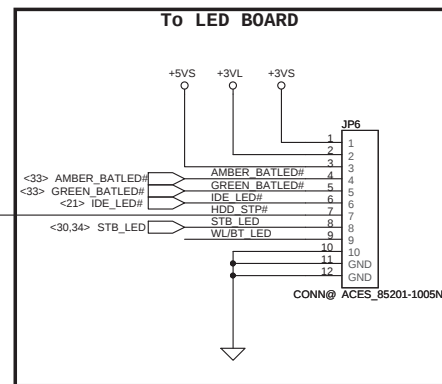
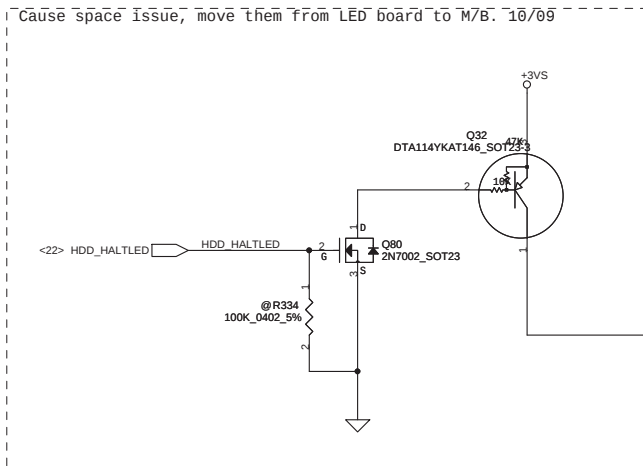
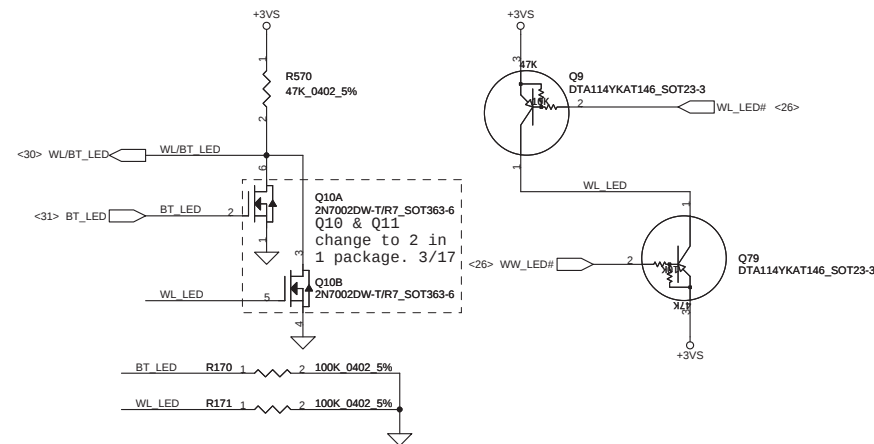
LCD/PANEL BD. CONN.



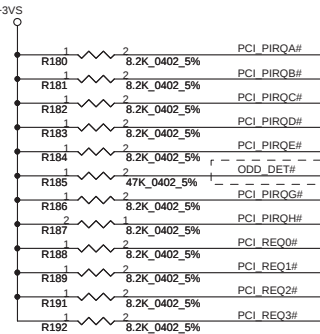
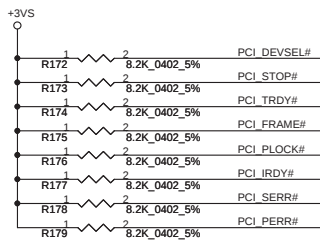
LCD POWER CIRCUIT



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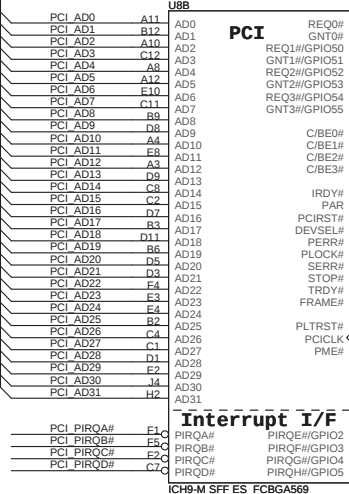


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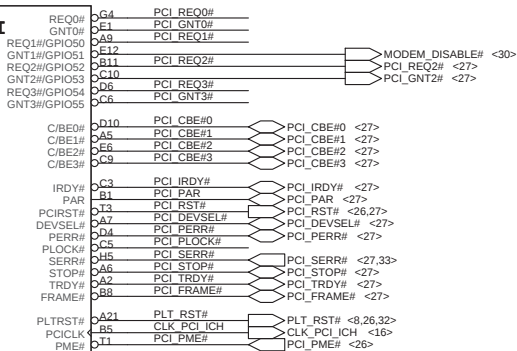


Change to ODD_DET#. 10/18

<27> PCI_AD[0..31]

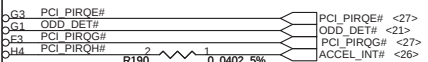


PCI

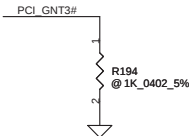


Interrupt I/F

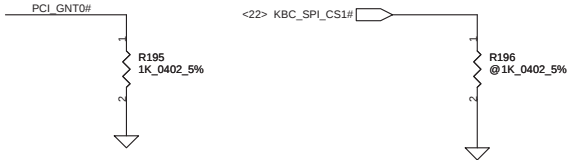
CH9-M SFF ES_FCBGA569



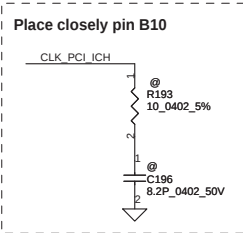
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC



DEL J3. 9/29

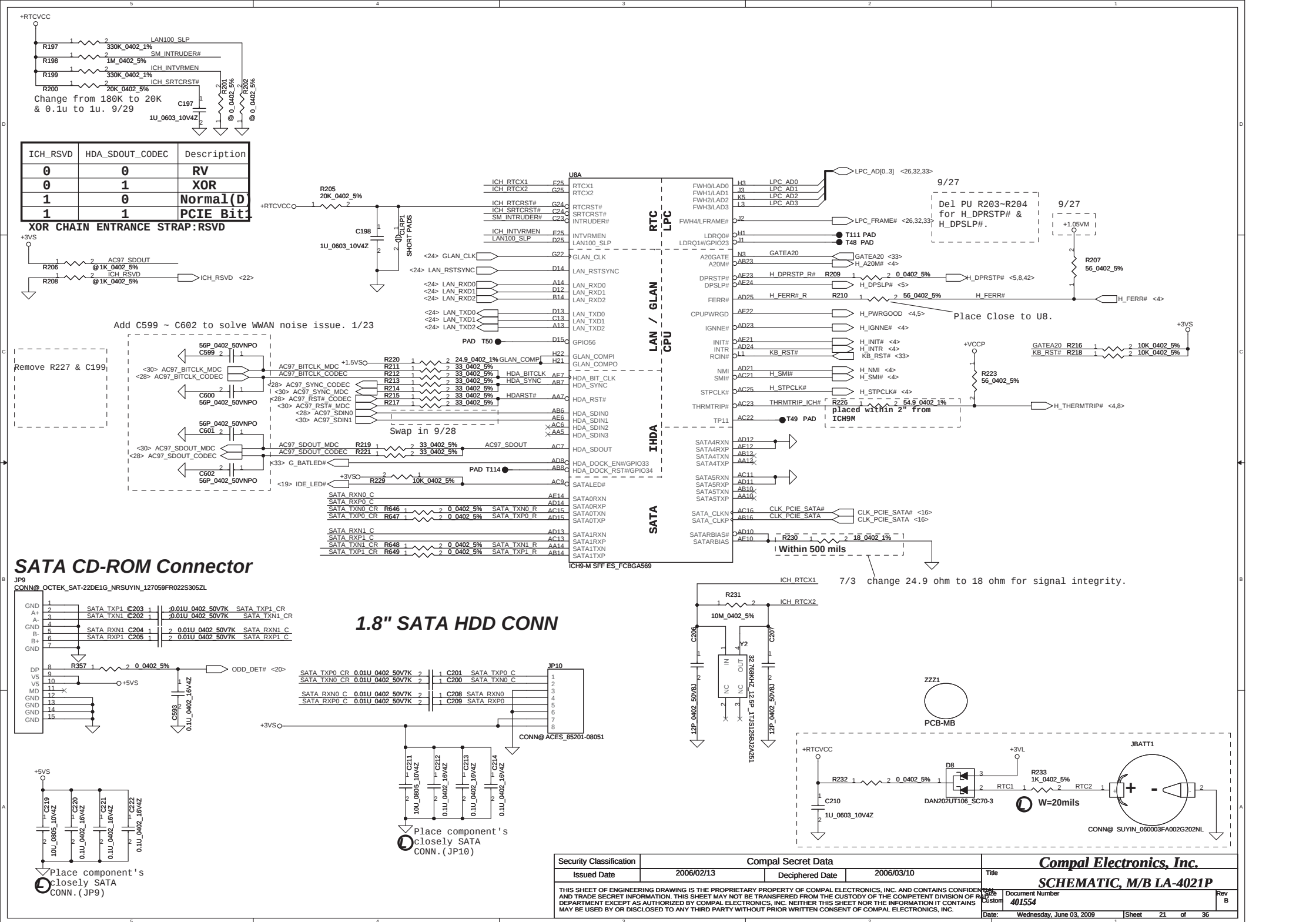


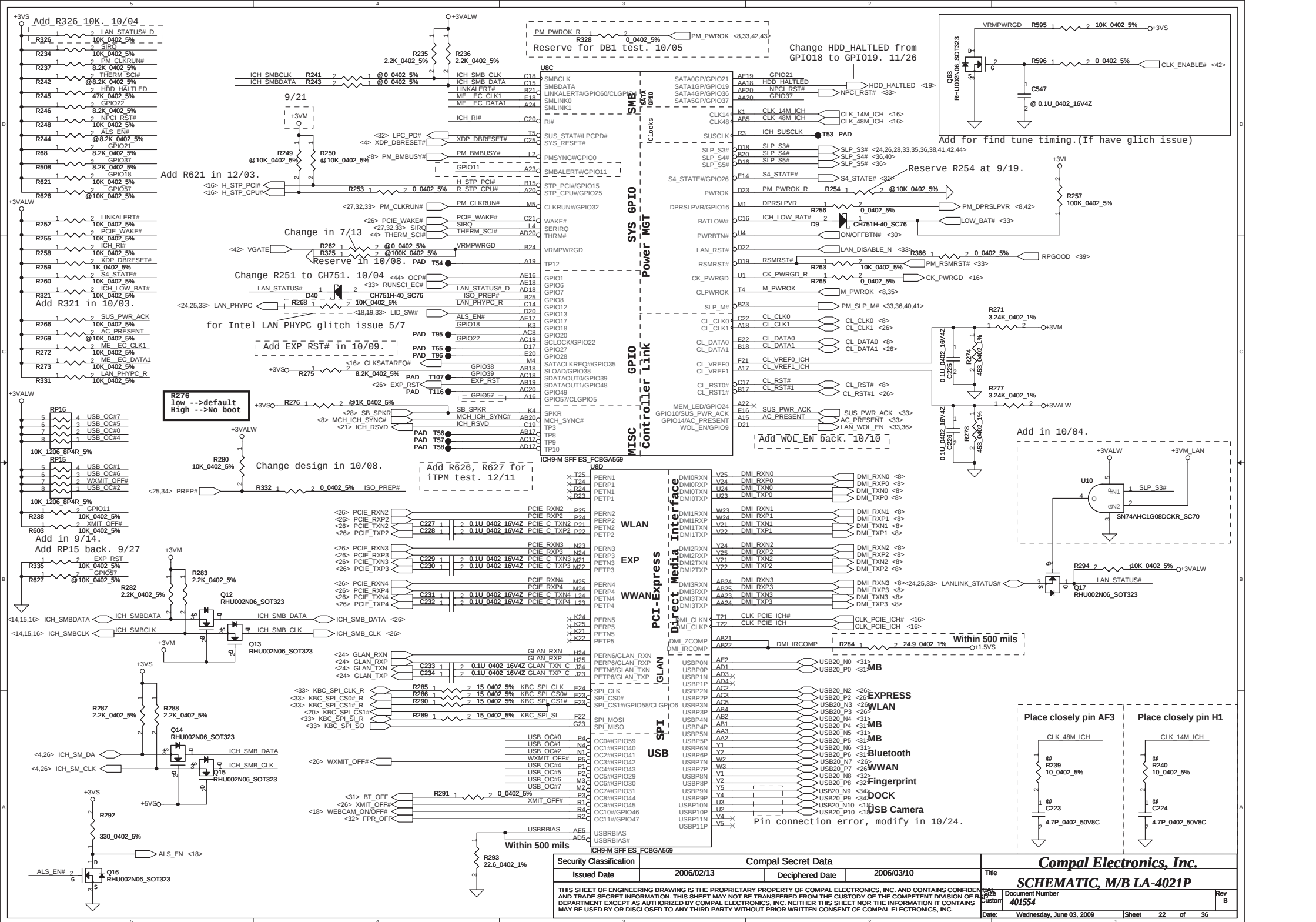
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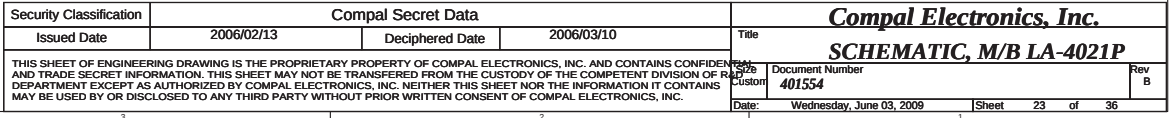
Compal Electronics, Inc.

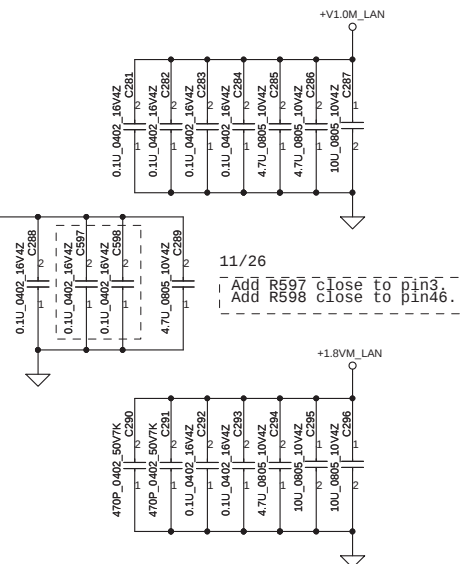
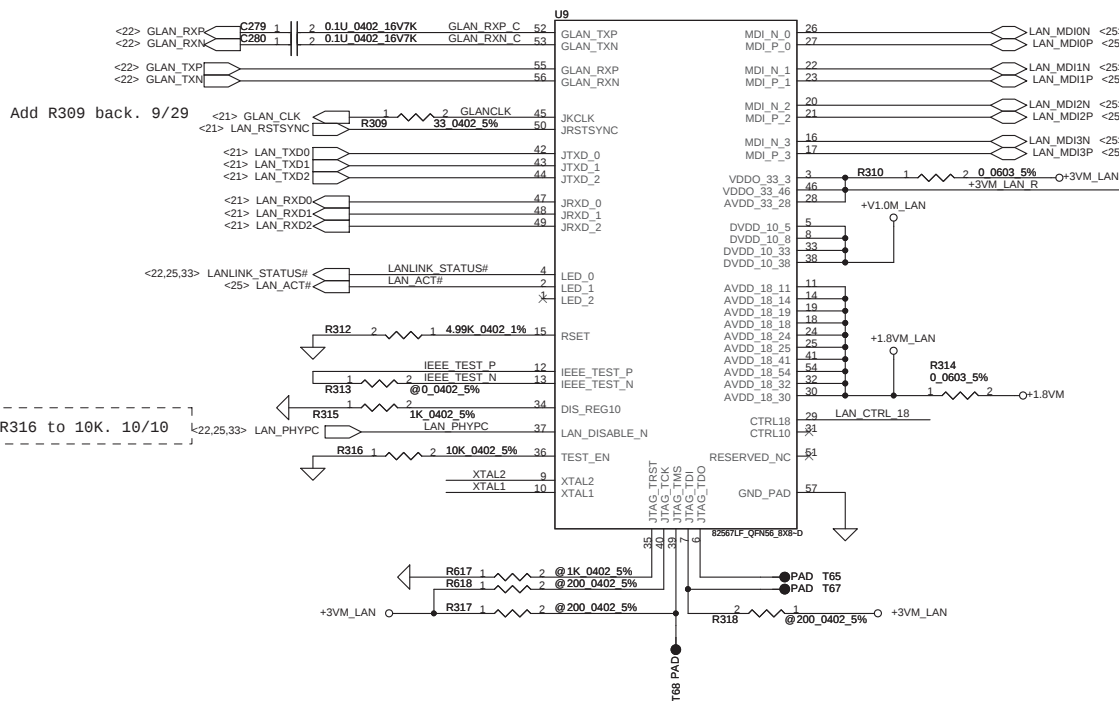
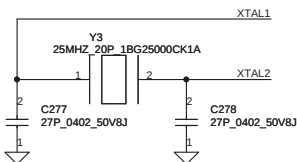
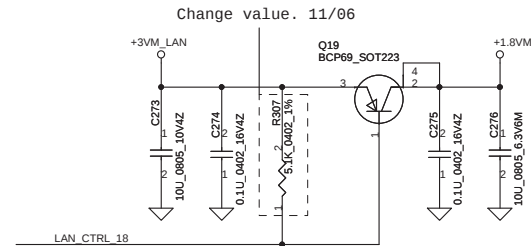
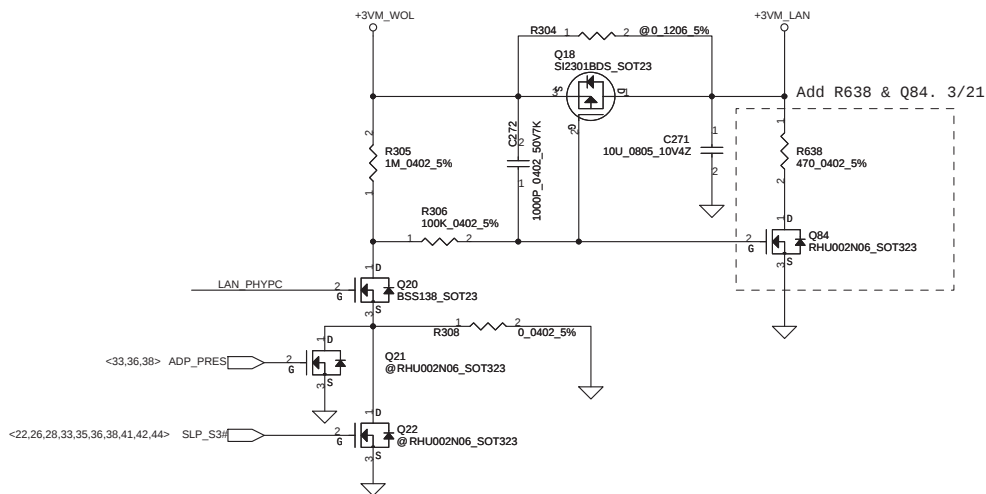
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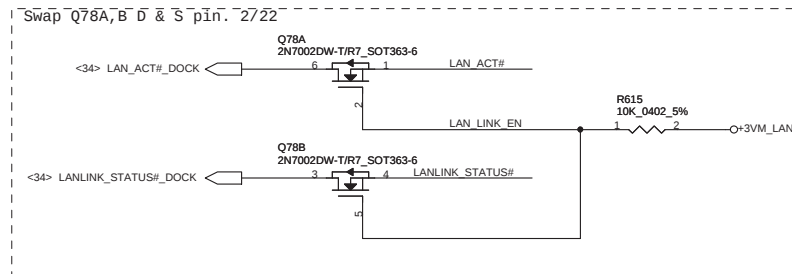




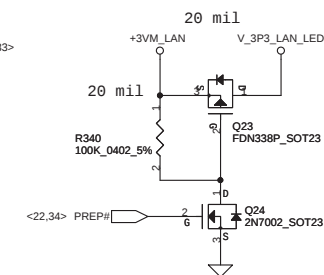
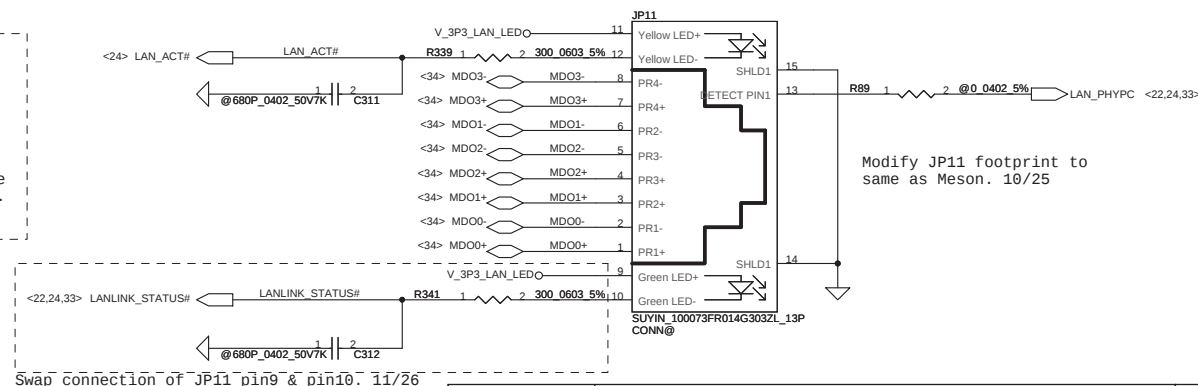
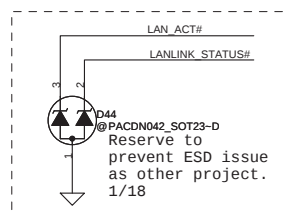
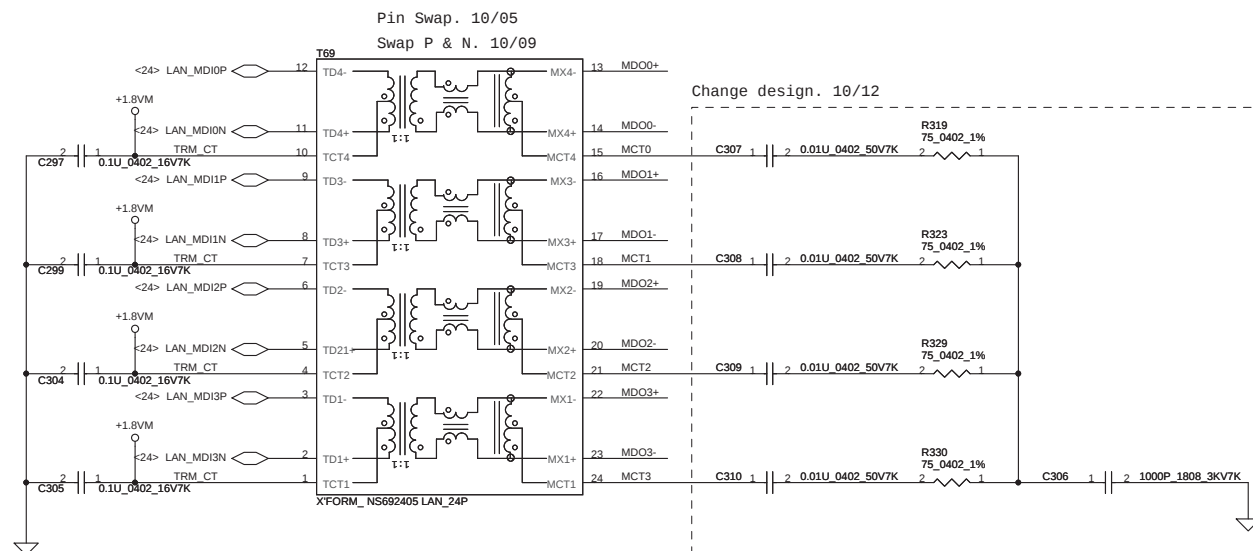




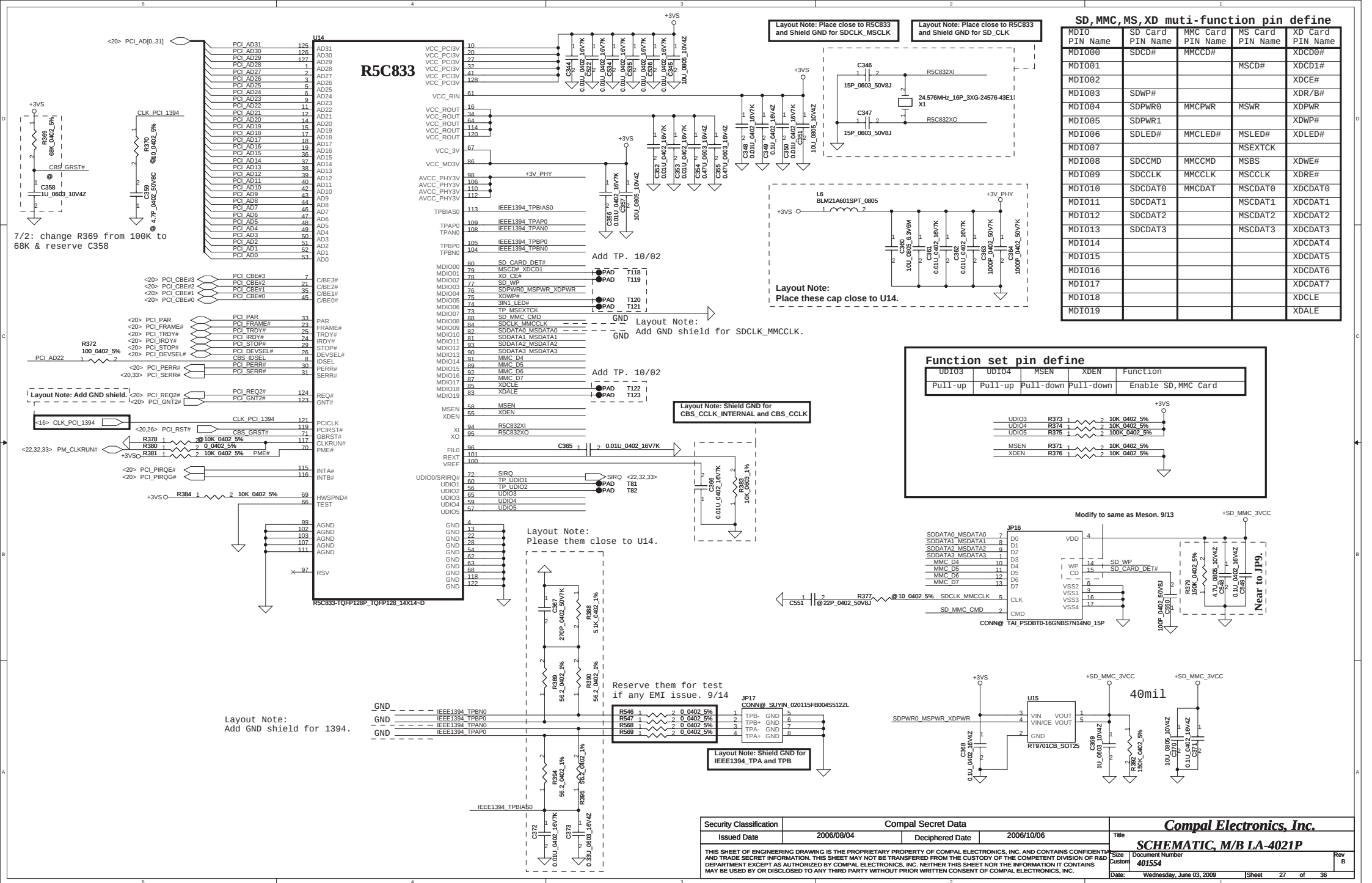
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Delete all termination cause they are already inside BOAZMAN. 9/28



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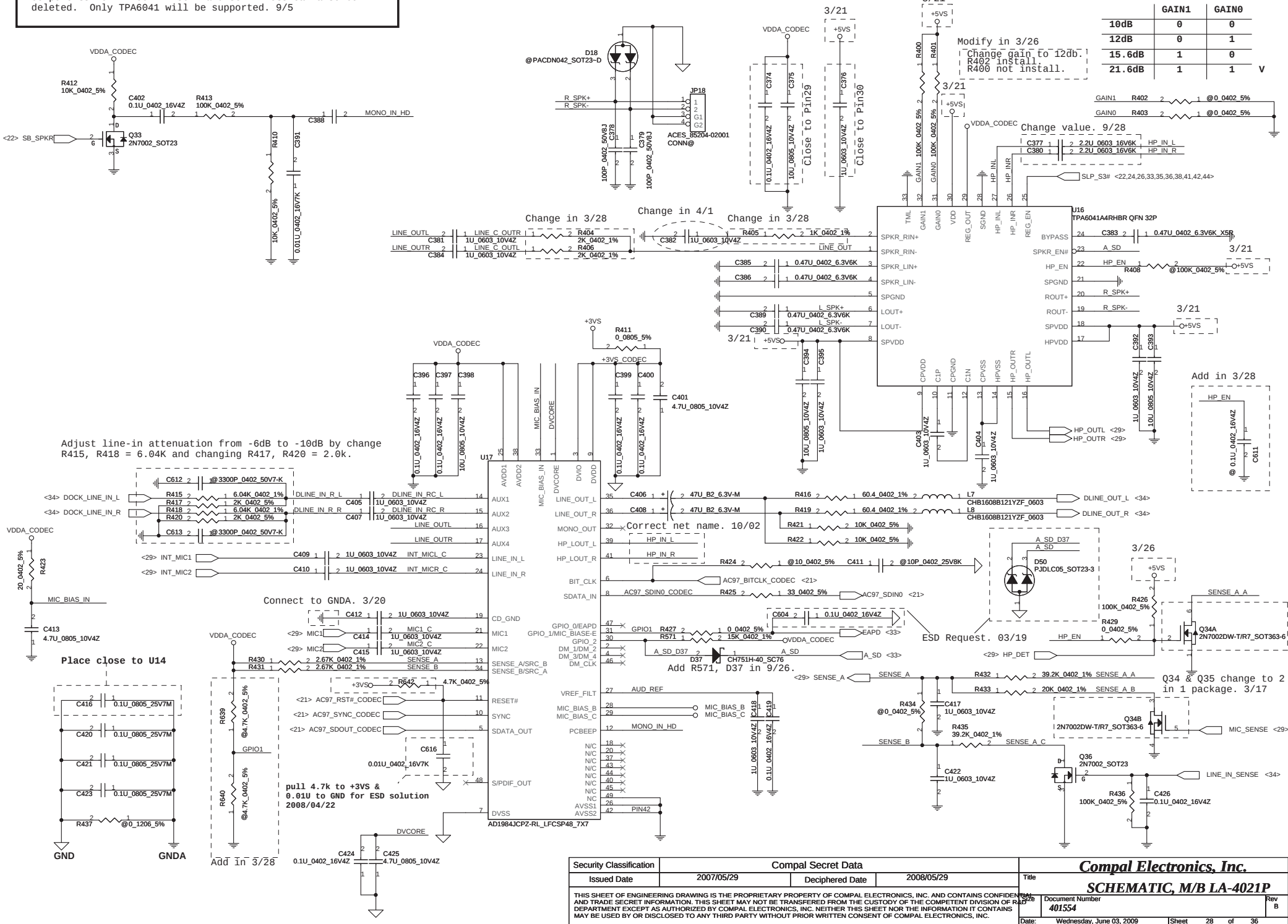


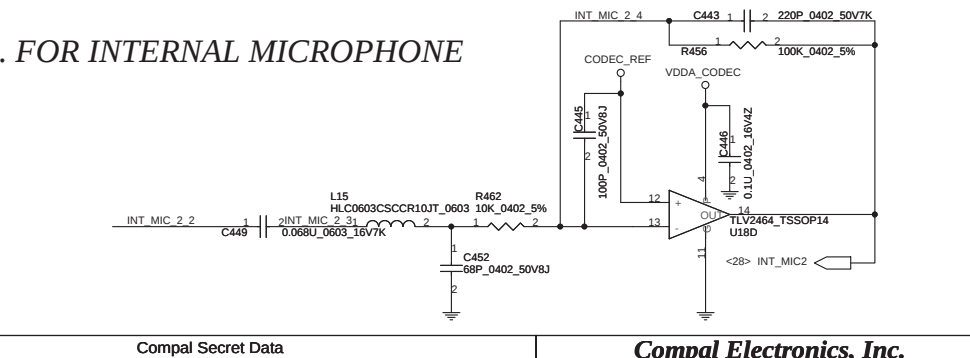
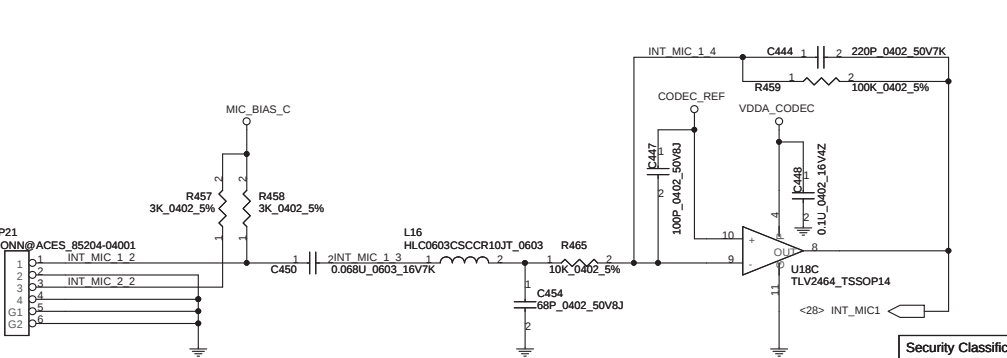
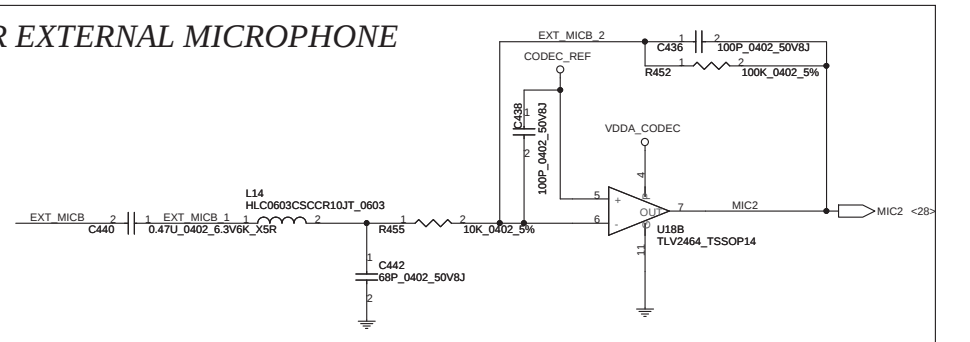
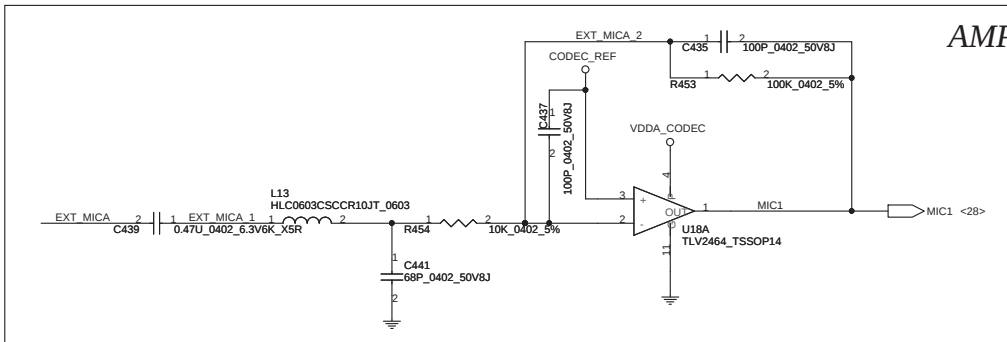
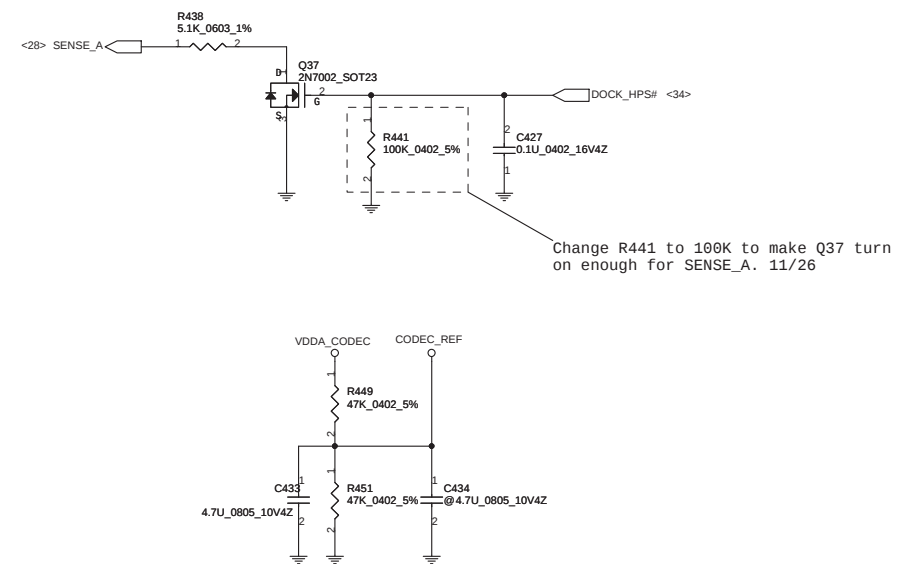
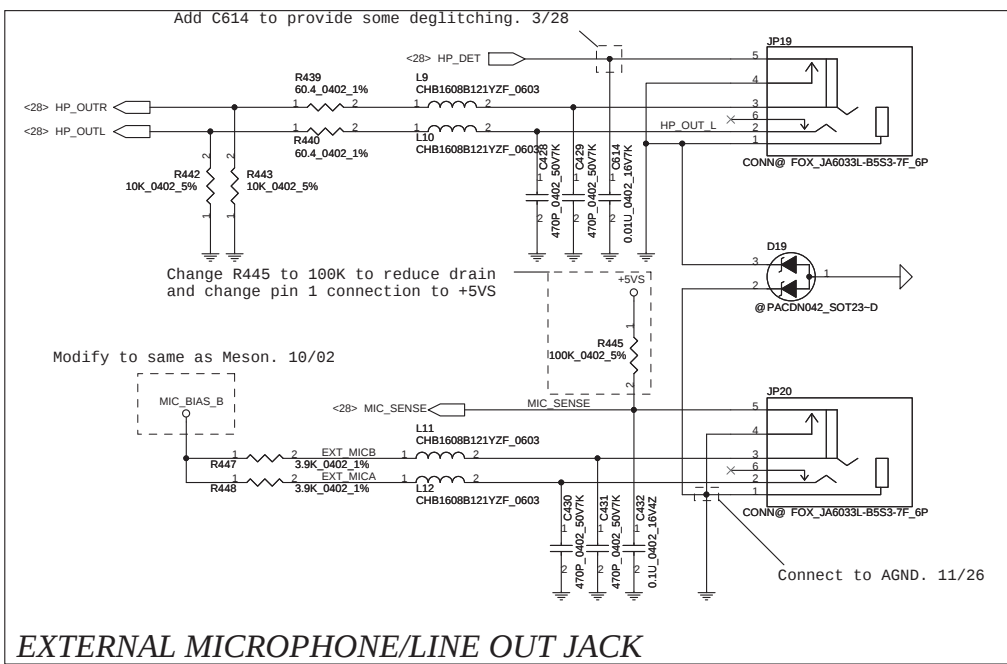
TPA6044 no longer needed. So delete BOM options & co-layout components for TPA6044. SGND and SGND1 nets can also be deleted. Only TPA6041 will be supported. 9/5

AMP. FOR INTERNAL SPEAKER

	GAIN1	GAIN0
10dB	0	0
12dB	0	1
15.6dB	1	0
21.6dB	1	1

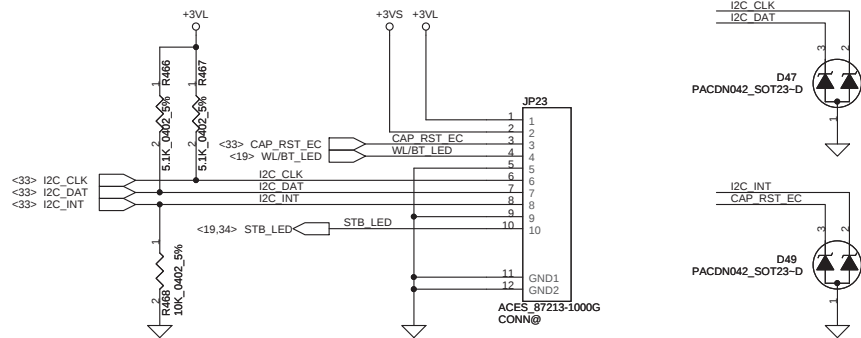
V



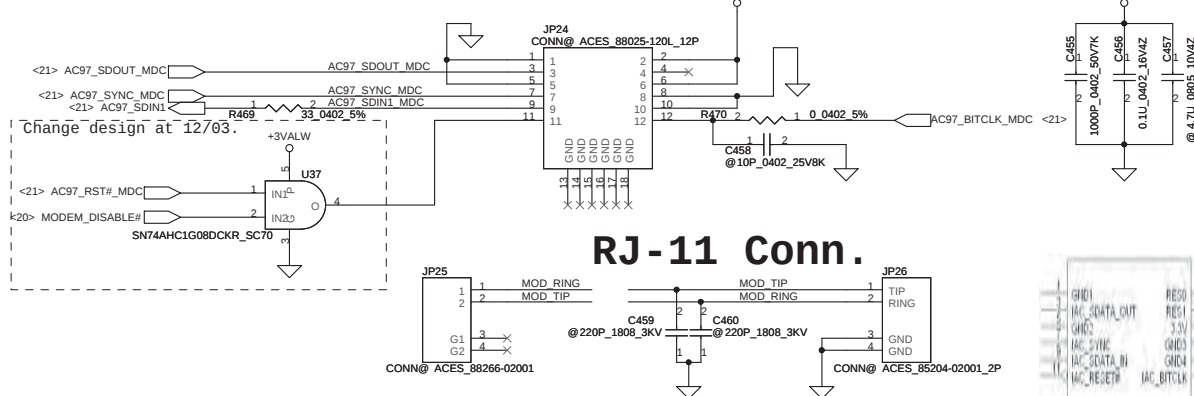


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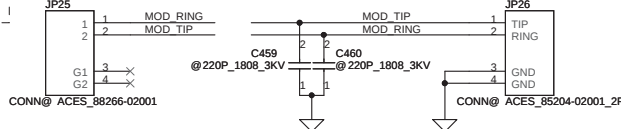
SWITCH BOARD.



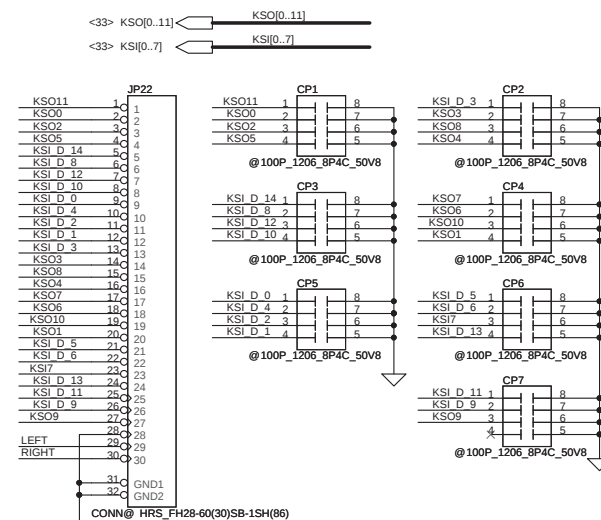
MDC 1.5 Conn.



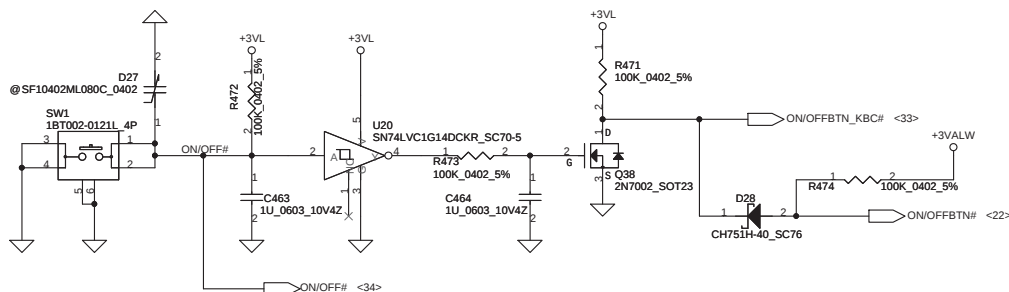
RJ-11 Conn.



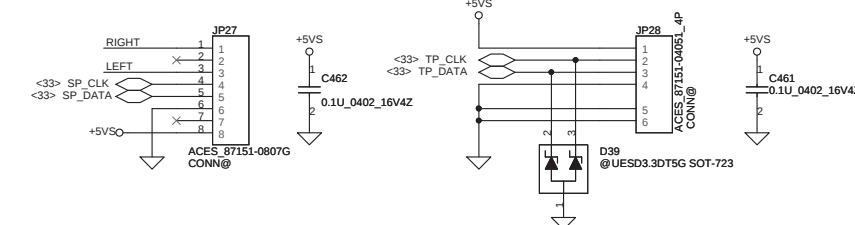
INT_KBD CONN.



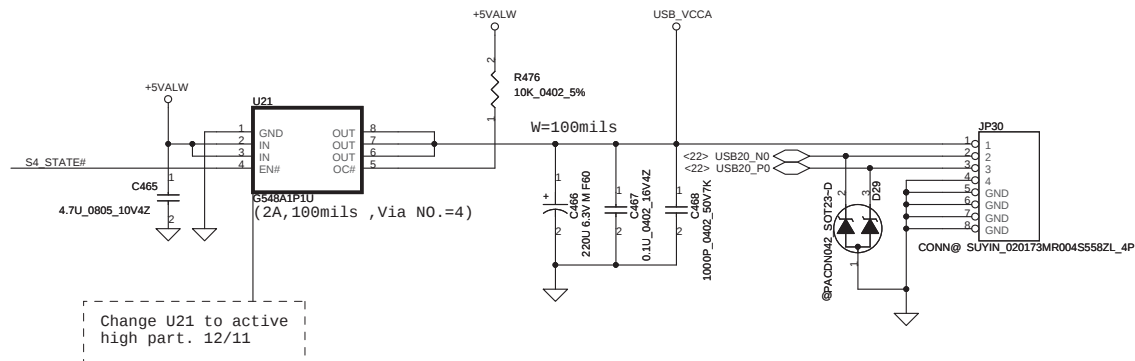
Power button



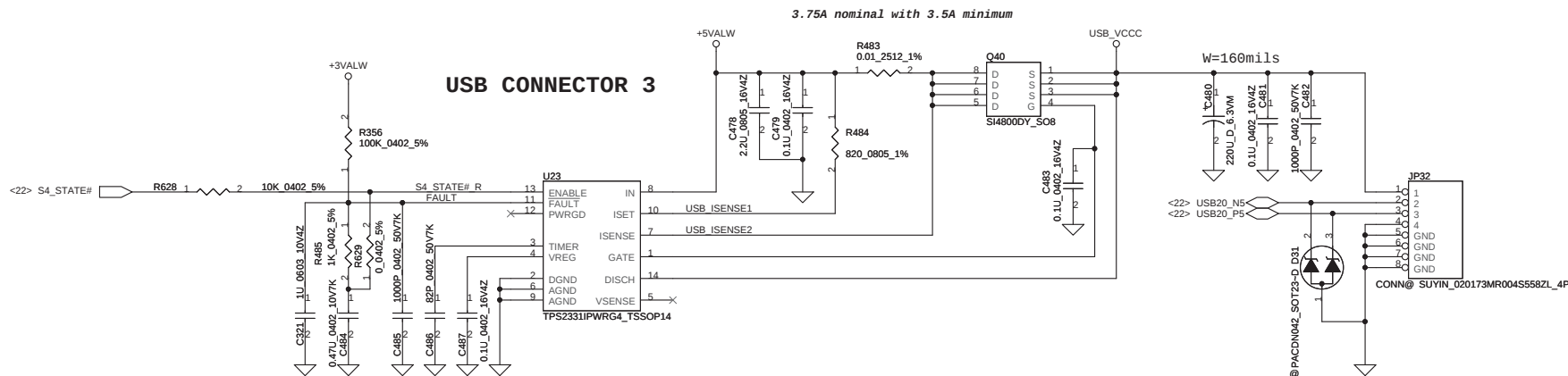
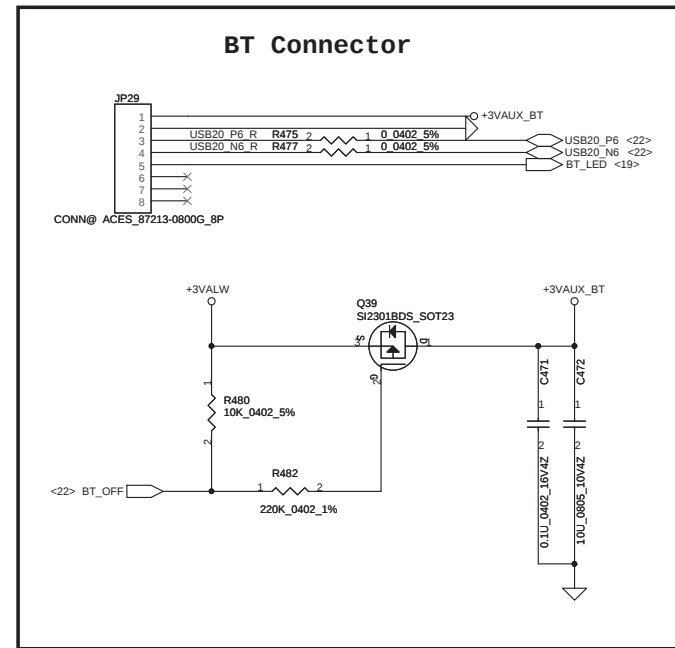
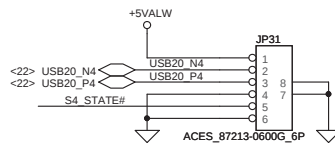
TrackPoint CONN. T/P BOARD.



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U22, D30, R481, C474 ~ C477 will move to USB board side to save M/B space.



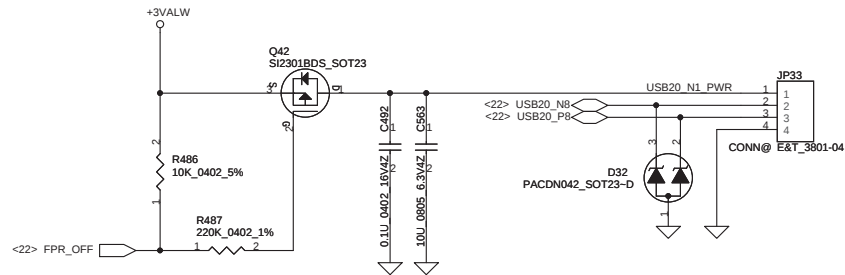
Change for SI1 to prevent USB power short to GND cause system shutdown. 0130

Change C486 from 2200pF to 680pF.
Change C321 from 1000pF to 1uF.
Change R484 from 10K to 100K.
Change C484 from 1000pF to 0.47uF.
Change R484 from 1K to 820.

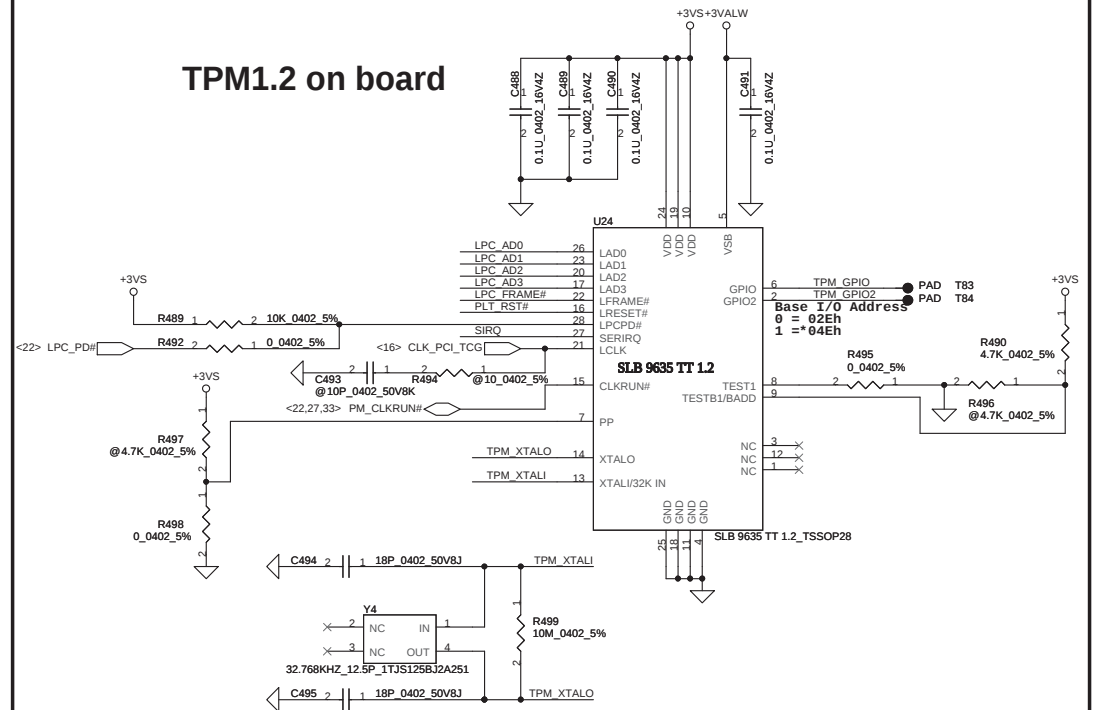
Currently power USB will not enable after OCP, so add R629 make it enable after OCP free.

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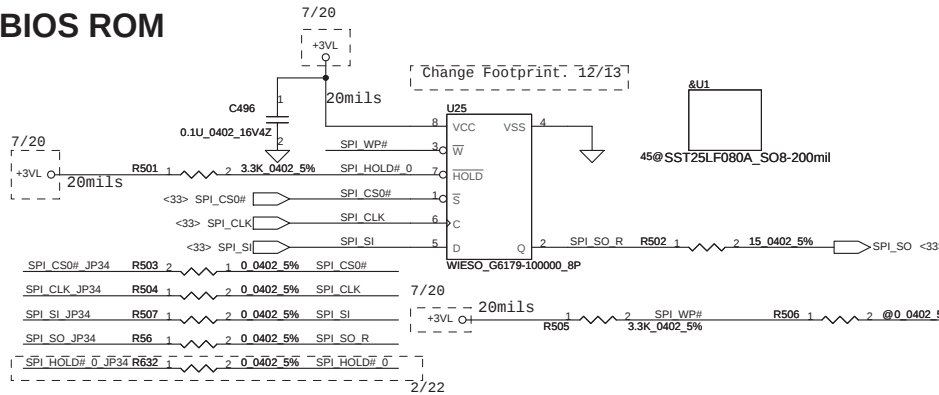
Finger printer



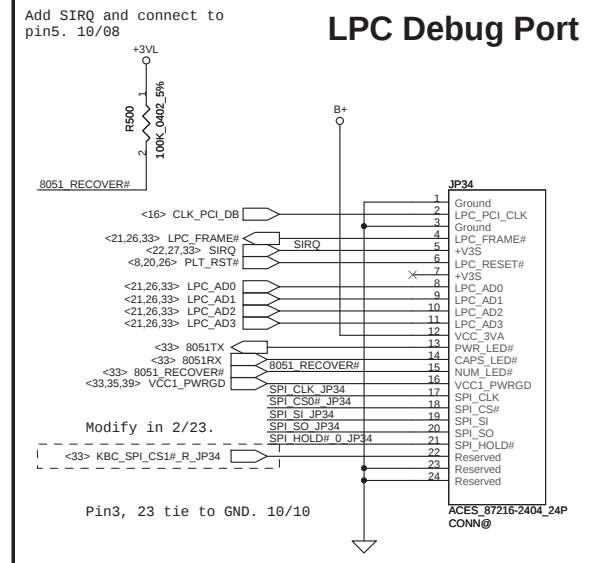
TPM1.2 on board



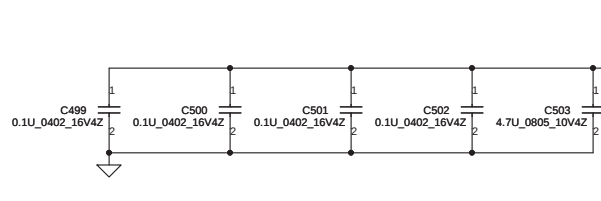
BIOS ROM



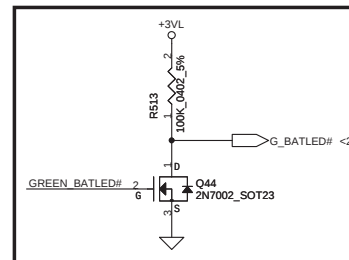
LPC Debug Port



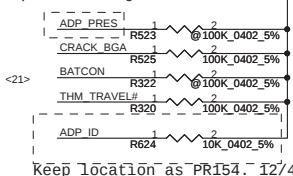
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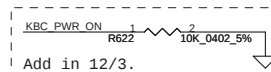
Del BATSELB_A# pin since only one battery. 10/18



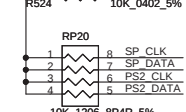
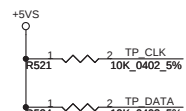
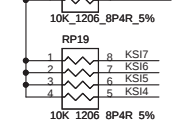
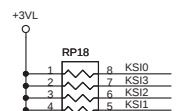
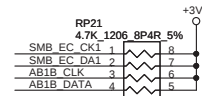
Del D35 & @523 for power saving. 0130



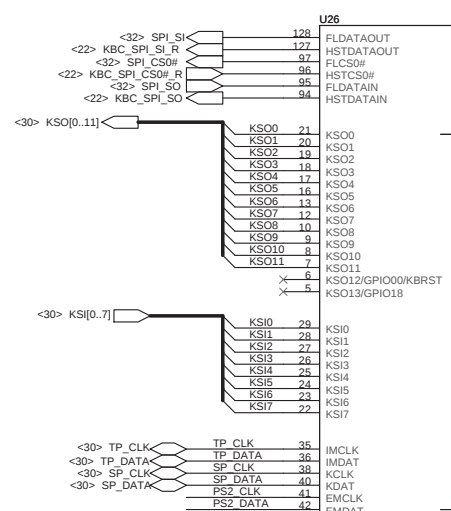
Keep location as PR154. 12/4



Add in 12/3.



delete R537 & 539 to clean up CRY1 & CRY2 traces



keyboard/mouse Interface

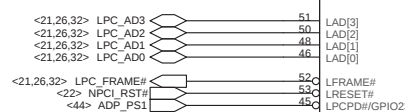
SMSC_1091-NU_TQFP-128P

General Purpose I/O Interface

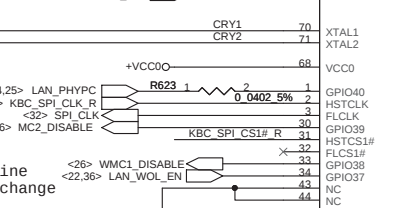
Access Bus Interface

Power Mgmt/SIRQ

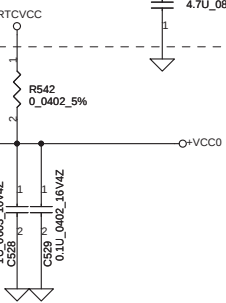
Miscellaneous



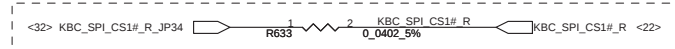
LPC Bus



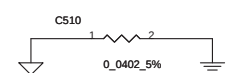
SMSC guideline suggest to change 18P to 22P



Modify in 2/23.



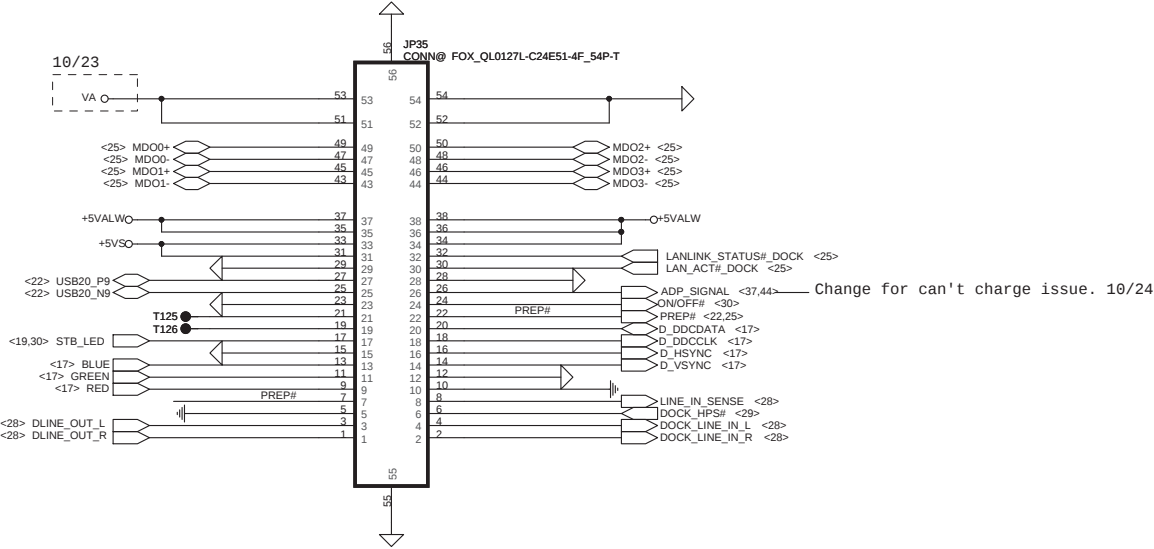
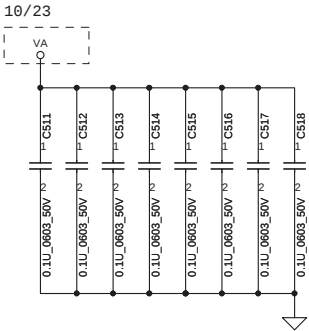
AGND FILTER



SMSC guideline suggest to change 0.1u to 0 ohm

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						Document Number		401554		Rev B	
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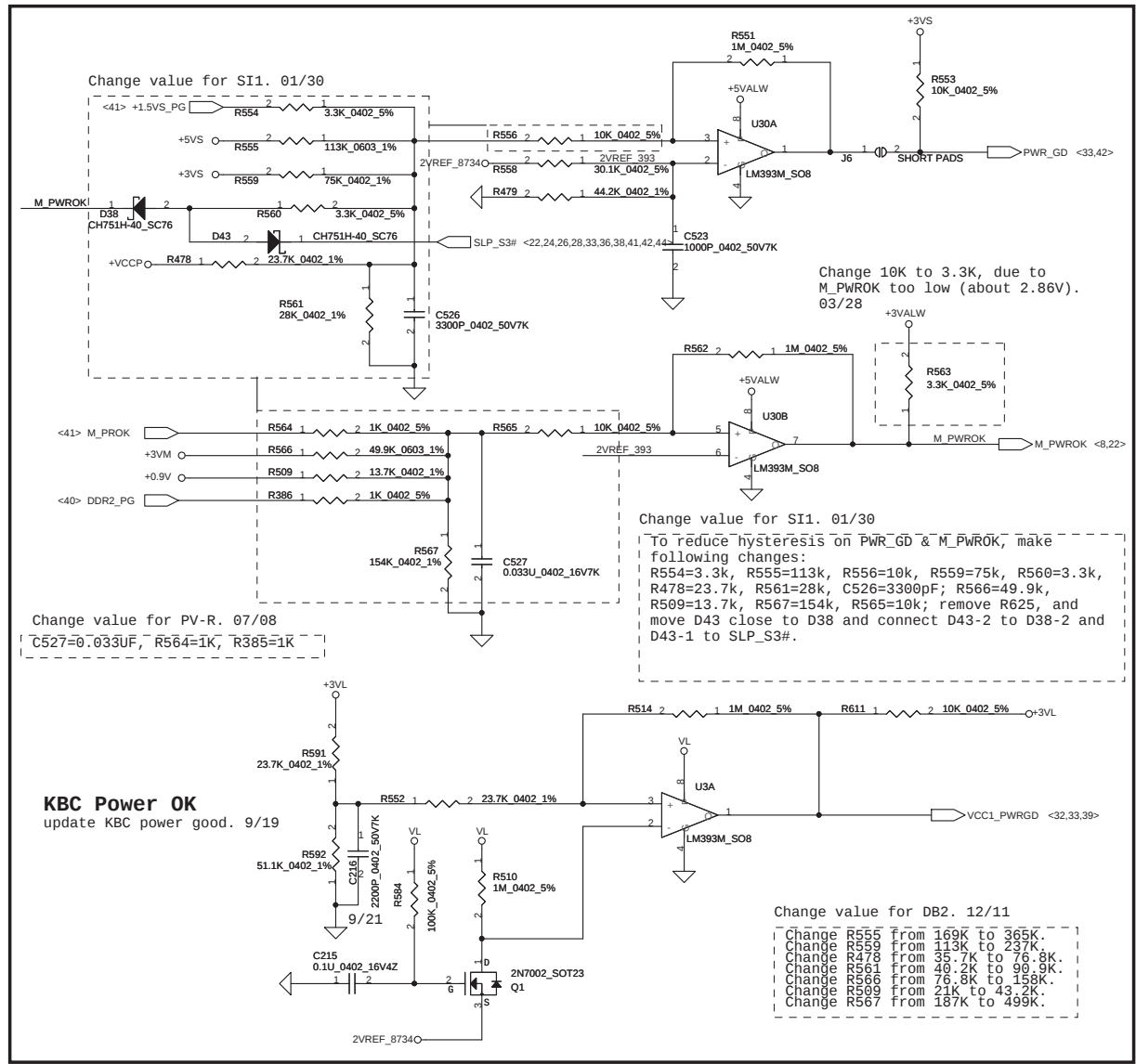
DOCKING CONNECT



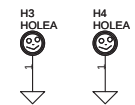
Delete:

1. L21 - L23
2. C605 - C610
3. R635 - R637
4. U27 - U29
5. C919 - C921
6. R548 - R550

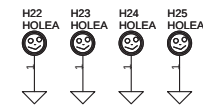
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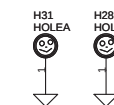
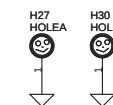
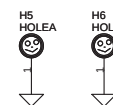
WWAN Card STANDOFF



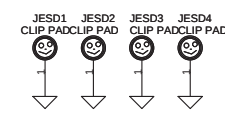
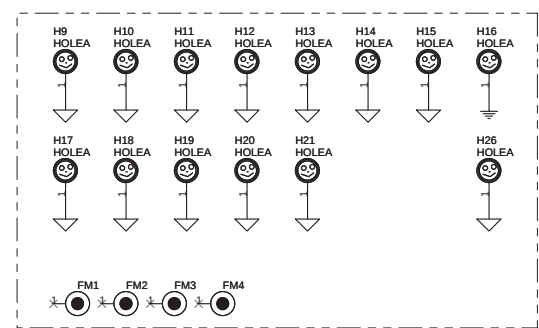
CPU support



MDC STANDOFF

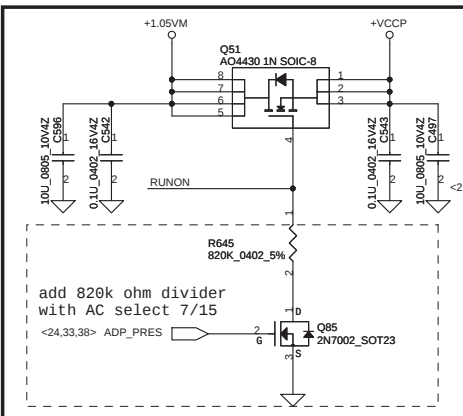


De1 H1, H7 & H8. 1/18



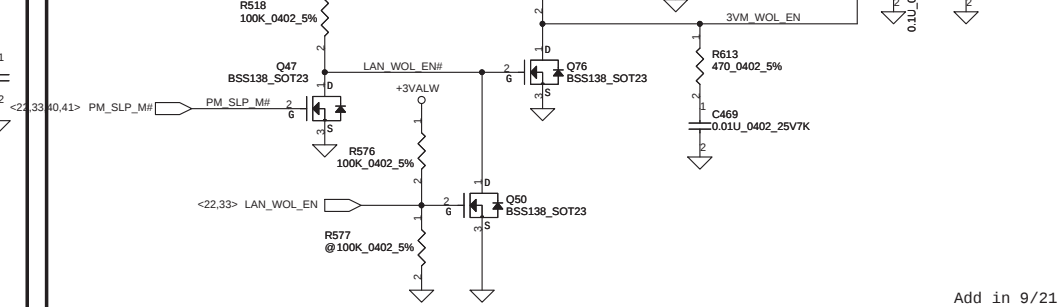
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+1.05VM to +VCCP Transfer



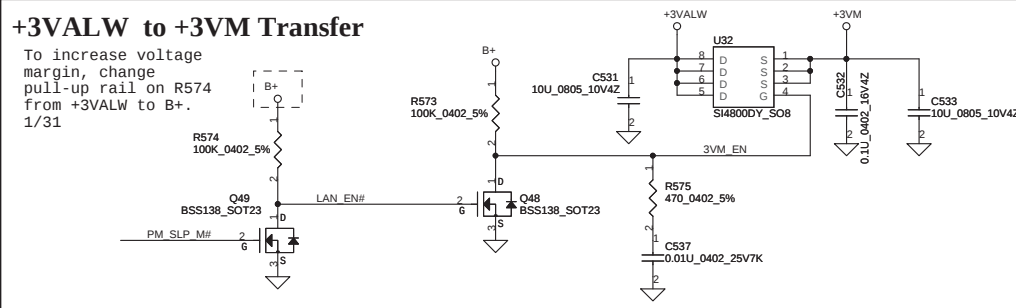
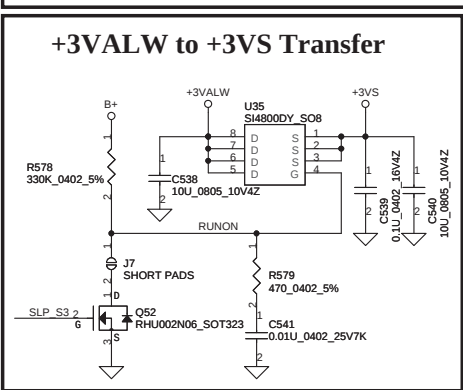
+3VALW to +3VM_WOL Transfer

To increase voltage margin, change pull-up rail on R518 from +3VALW to B+. 1/31

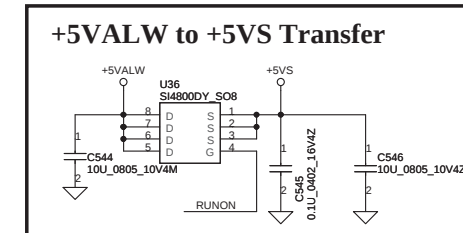


+3VALW to +3VM Transfer

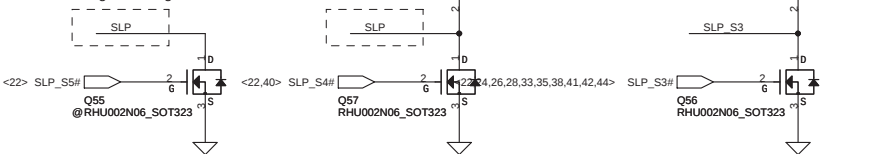
To increase voltage margin, change pull-up rail on R57 from +3VALW to B+.



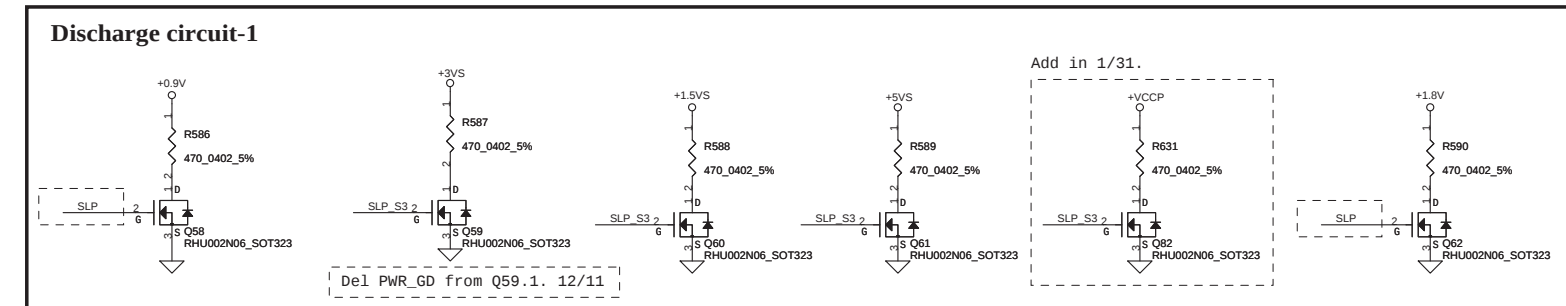
+5VALW to +5VS Transfer



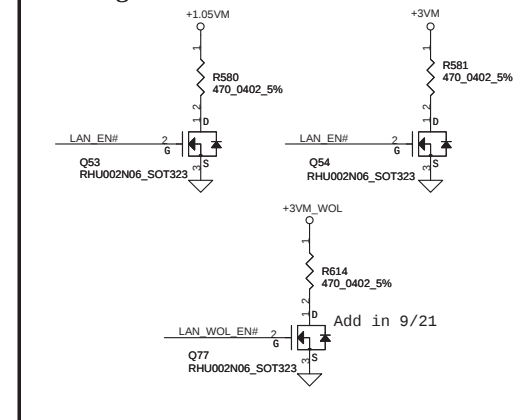
Design Change at 9/14.



Discharge circuit-1



Discharge circuit-2 for V-M



SYS. STATE	PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM
M-off / No WOL	0	0	0V	0V
M-off / WOL	0	1	3.3V	0V
M1 (ME on)	1	0	3.3V	3.3V
M1 (ME on)	1	1	3.3V	3.3V

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