Wistron Confidential

MV

2008/07/16 REV :MV-01

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *NORN 2.0*

Size	Document Number	Rev
A3	NORN 2.0	-1

Date: Wednesday, July 16, 2008 Sheet 1 of 52

NORN 2.0 Block Diagram

Project code : 91.4Y801.001
PCB P/N : 07243-SA
Revision : DB1

VGA ISL6263A	
INPUTS	OUTPUTS
B+	VCCGFX 47

SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
B+	+5VALW 5A +3VALW 4A 41

SYSTEM DC/DC TPS51124	
INPUTS	OUTPUTS
B+	+1.5VS 4A +VCCP 6A 42

CHARGER BQ24740	
INPUTS	OUTPUTS
BATT_A BATT_B	BATT 18V 3.0A 5V 100mA 39

CPU DC/DC ISL6261ACRZ	
INPUTS	OUTPUTS
B+	+VCC_CORE 0.844~1.3V 44A 44, 45

PCB LAYER	
L1:	TOP
L2:	Signal
L3:	GND
L4:	Signal
L5:	VCC
L6:	GND
L7:	Signal
L8:	Bottom

CLK GEN
ICS9LPRS397
SLG8SP553
16

Intel CPU
Penryn 6M ULV
FSB:667 MHz
5,6,7

HOST BUS
FBS
667MHz

Thermal Sensor
SMSC 2103 51
SMBus

TOTAL 8GB SUPPORT

DDRII 667
Slot 0 14
DDRII 667 Channel A

DDRII 667
Slot 1 15
DDR II 667 Channel B

Cantiga-GS
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
8,9,10,11,12,13

RGB CRT
LVDS

CRT 17
LCD 18

1394 49
SD/MMC 49

Ricoh
5C833
CardReader
48, 49

PCI

DMI x4
C-LINK0

INTEL
ICH9M SFF
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
Serial Peripheral I/F
ACPI 1.1
LPC I/F
4 SATA
PCI/PCI BRIDGE
19,20,21,22,23

Fingerprinter
AES2810 50
CAMERA 50
BLUE TOOTH 30
USB x 2 30

USB 2.0

RJ45 CONN 26
Intel WG82567LM
(BOAZ)
10/100/1000 25
PCIE/GLCI
PCI/LCI

RJ11 CONN 26
MODEM
MDC V1.5 33
HD Audio

HDD Bay
1.8" SATA 24
SATA

TPM
SLB9635TT 31
LPC Bus

INTERNAL
ARRAY MIC

AUDIO CODEC
AD1984AJCPZ
28

MIC IN
Headphone
PRE-AMP
TLV2462 29

PCIE+USB 2.0
PCIE +USB 2.0
C-LINK1
PCIE +USB 2.0
SPI
SM Bus

TI
TPS2231 24

KBC
SMSC KBC1091 32
Serial Bus
W-COM
Digitizer 18

OP AMP
TPA6211A1 29

5CC
SPEAKER

Express Card 54 24
Mini-Card
802.11abg/n 27
Mini-Card
WWAN 27
Flash ROM
32Mb x 1(AMT) 31
Aceelerometer
STMicro
LIS3LV02DL 27
Tauch Pad 33
Int. KB 33
Capacitive Button 50

DOCK
CRT LINE IN LINE OUT USB*4 Ethernet ODD 34

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A3
Document Number: NORN 2.0
Rev: -1
Date: Wednesday, July 16, 2008
Sheet 2 of 52

Voltage Rails

o MEANS ON x MEANS OFF

State \ power plane	+BB LDO3 LDO5	+3VALW +5VALW	+1.8V +0.9V	+5VS +3VS +1.5VS +1.05VM +VGA_CORE +CPU_CORE +VCCP	+3VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	X	O
S5 S4/Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EETERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader & 1394	AD22	2	G,E

DMA Channel	Device
DMA0	Modem/LAN
DMA1	ECP
DMA2	~~Floppy Disk~~
DMA3	Audio
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	Walk-up1 (Right Side)
1	Free
2	EXPRESS SLOT
3	WLAN
4	Walk-up2 (Left Side)
5	Walk-up3
6	Bluetooth
7	WWAN
8	Fingerprint
9	Dock1 (HUB)
10	Camera
11	Dock2 (IDE)

Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	~~Floppy~~
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family) PCI Express Root Port -27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family) USB Universal Host Control
18	Intel 82801H (ICH8 Family) USB Universal Host Control Richo R5C853 Integrates FlashMedia Control Richo R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family) PCI Express Root Port -27D6 Intel 82801H (ICH8 Family) USB Universal Host Control
20	Intel 82801H (ICH8 Family) USB Universal Host Control Intel 82801H (ICH8 Family) USB2 Enhanced Host Control
21	Intel 82801H (ICH8 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control
23	HP Mobile Data Protection Sensor

<Core Design>

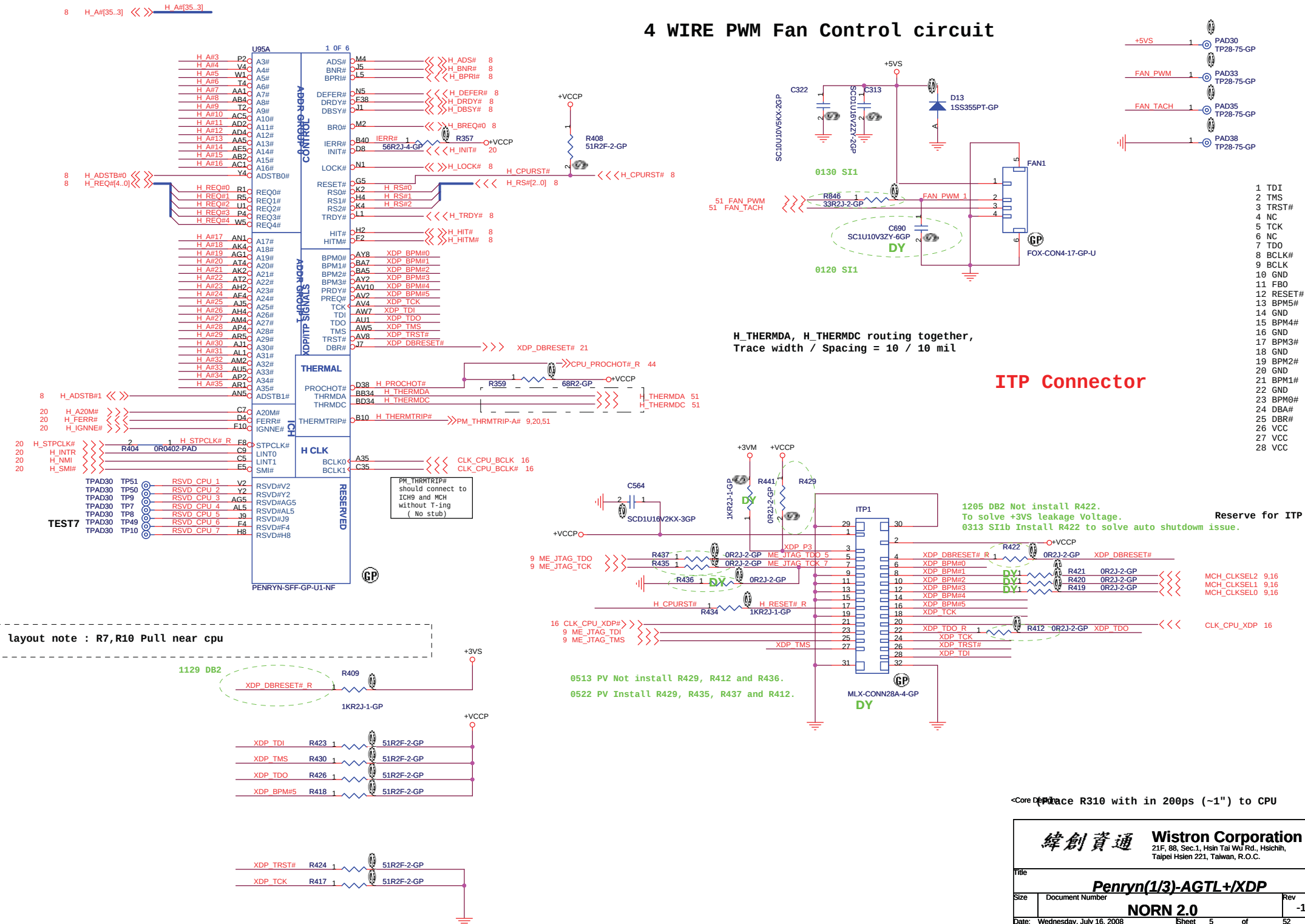
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Notes List**

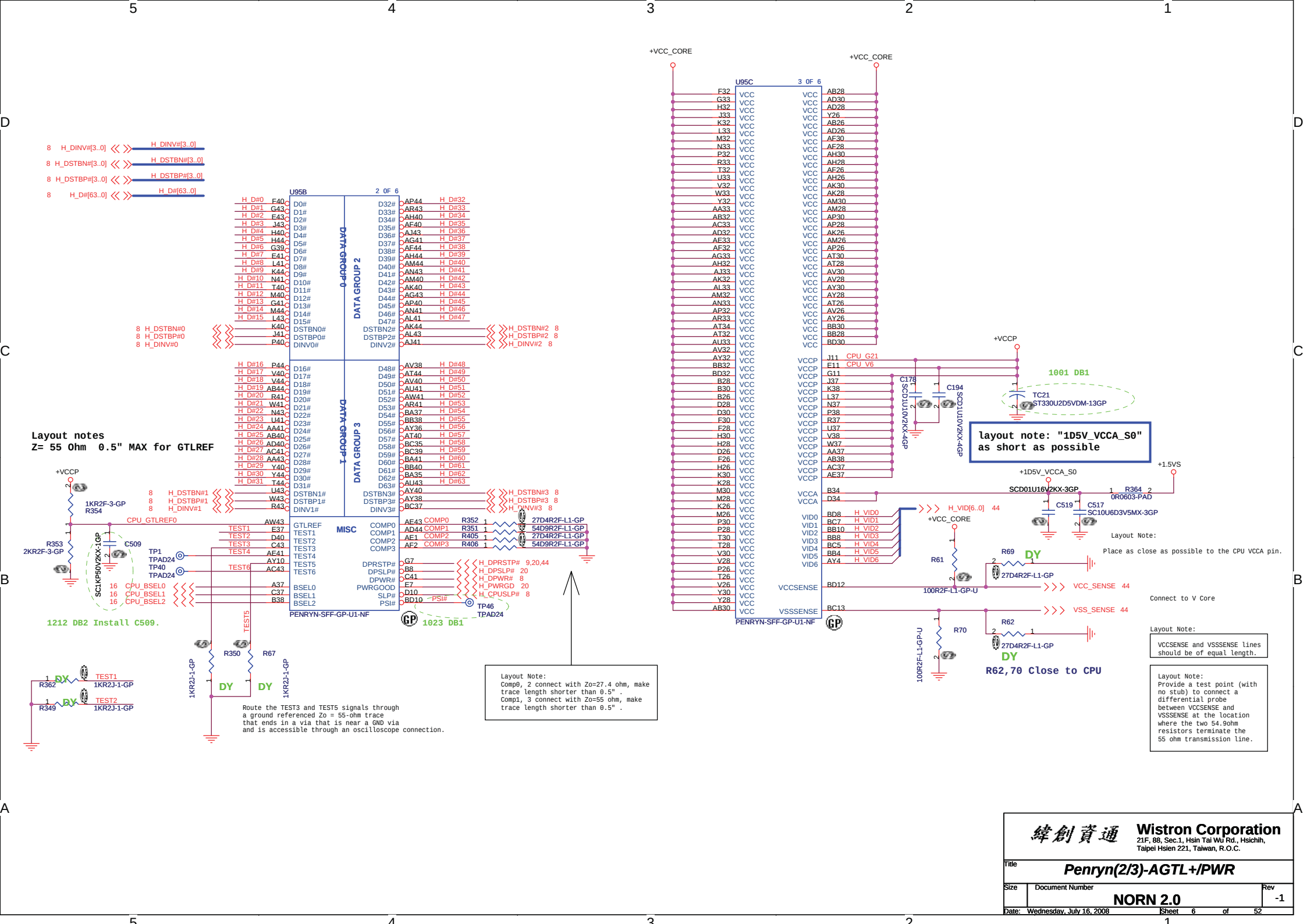
Size: A3 | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 4 of 52

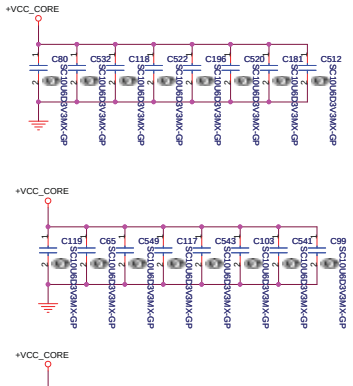
4 WIRE PWM Fan Control circuit



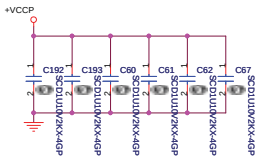
Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Penryn(1/3)-AGTL+/XDP	
Size	Document Number: NORN 2.0
Rev: -1	
Date: Wednesday, July 16, 2008	Sheet 5 of 52

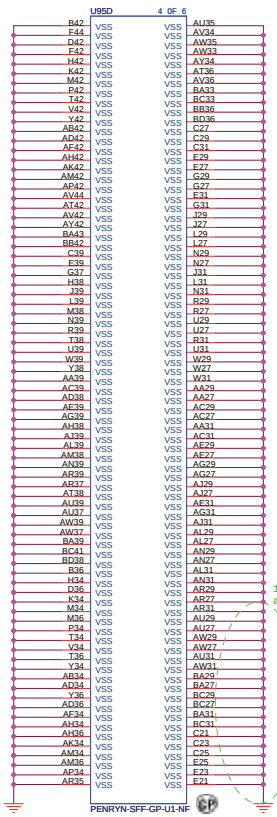

Layout notes
Z= 55 Ohm 0.5" MAX for GTLREF
U95B
2 OF 6
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
MISC
PENRYN-SFF-GP-U1-NF
U95C
3 OF 6
PENRYN-SFF-GP-U1-NF
+VCC_CORE
+VCCP
+1.5VS
+1D5V_VCCA_S0
1001 DB1
1023 DB1
1212 DB2 Install C509.
layout note: "1D5V_VCCA_S0" as short as possible
Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Layout Note: Place as close as possible to the CPU VCCA pin.
Connect to V Core
Layout Note: VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note: Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
R62,70 Close to CPU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Penryn(2/3)-AGTL+/PWR
NORN 2.0
-1
Wednesday, July 16, 2008
Sheet 6 of 52

Place these inside socket
cavity on L8(North side Secondary)

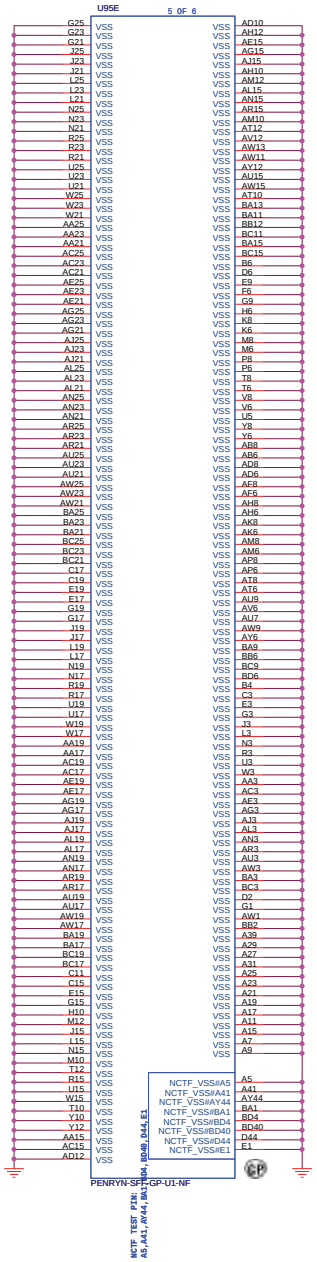


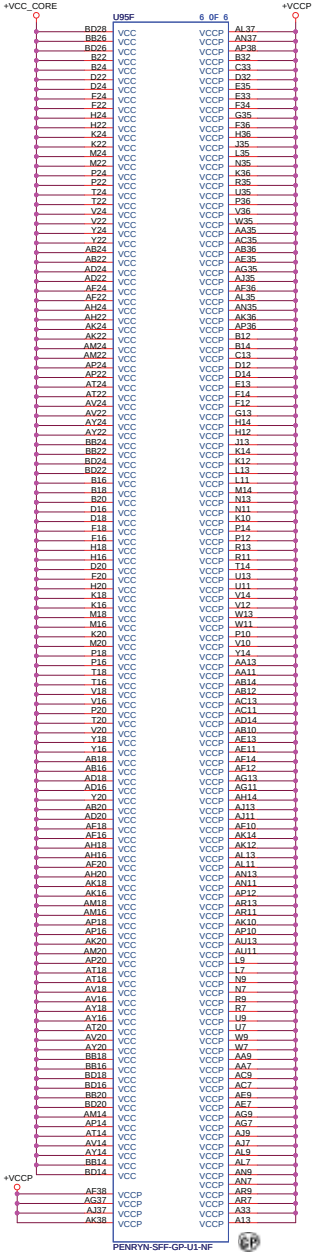
Place these inside socket
cavity on L8(North side Secondary)





1015 DB1 Connect AR31,BA27,BC29
and E23 to GND.

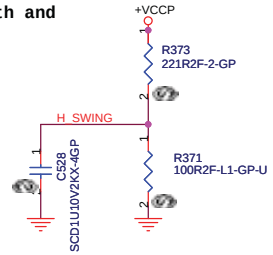




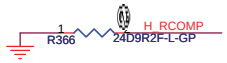
鋒創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Penryn(3/3)-GND&Bypass***	
Size	Document Number **NORN 2.0**	Rev -1
Date: Wednesday, July 16, 2008	Sheet 7 of 52	

H_SWING routing Trace width and Spacing use 10 / 20 mil

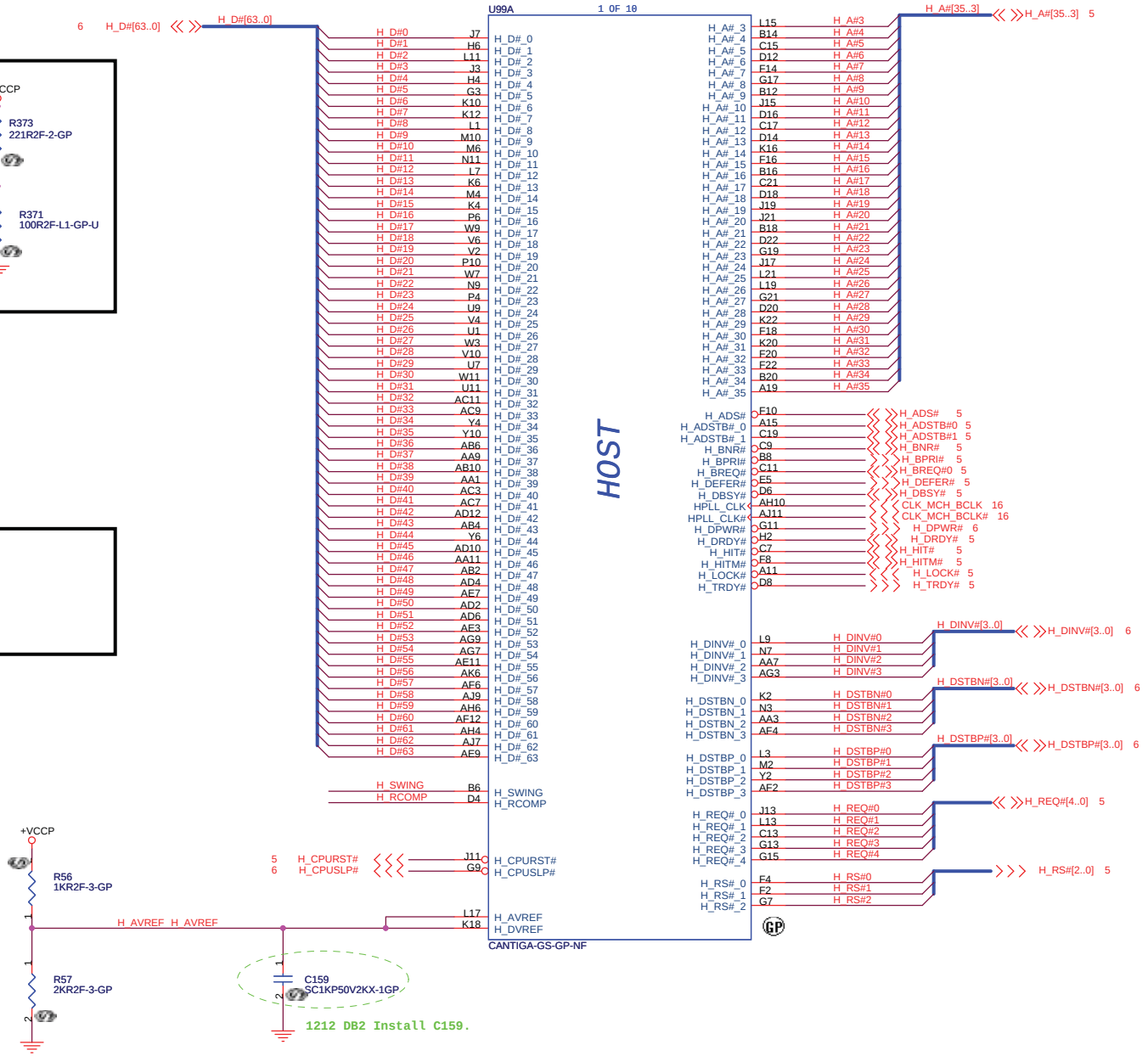
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Cantiga(1/6)-Host		
Size	Document Number	Rev
	NORN 2.0	-1
Date: Wednesday, July 16, 2008	Sheet 8 of 52	

1206 DB2 Not install R509, R510 and R511.

Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.

FSB setting

DMI Lane Reversal
MCH_CFG_19 Low = Normal (default)
High = Lanes Reversed
Teenah = 4.02K
Cantiga = 2.2K

PCI Express Graphics Lane
MCH_CFG_9 Low = Normal (default)
High = Lanes Reversed
Teenah = 4.02K
Cantiga = 2.2K

1015 DB1 Remove TV-OUT

Teenah 1.25V Rail
Cantiga 1.05V Rail

FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace width use 20 mil

Cantiga : 510hm
Teenah :392 Ohm

Place Close GMCH

1015 DB1 Remove R966,R967 and R968.

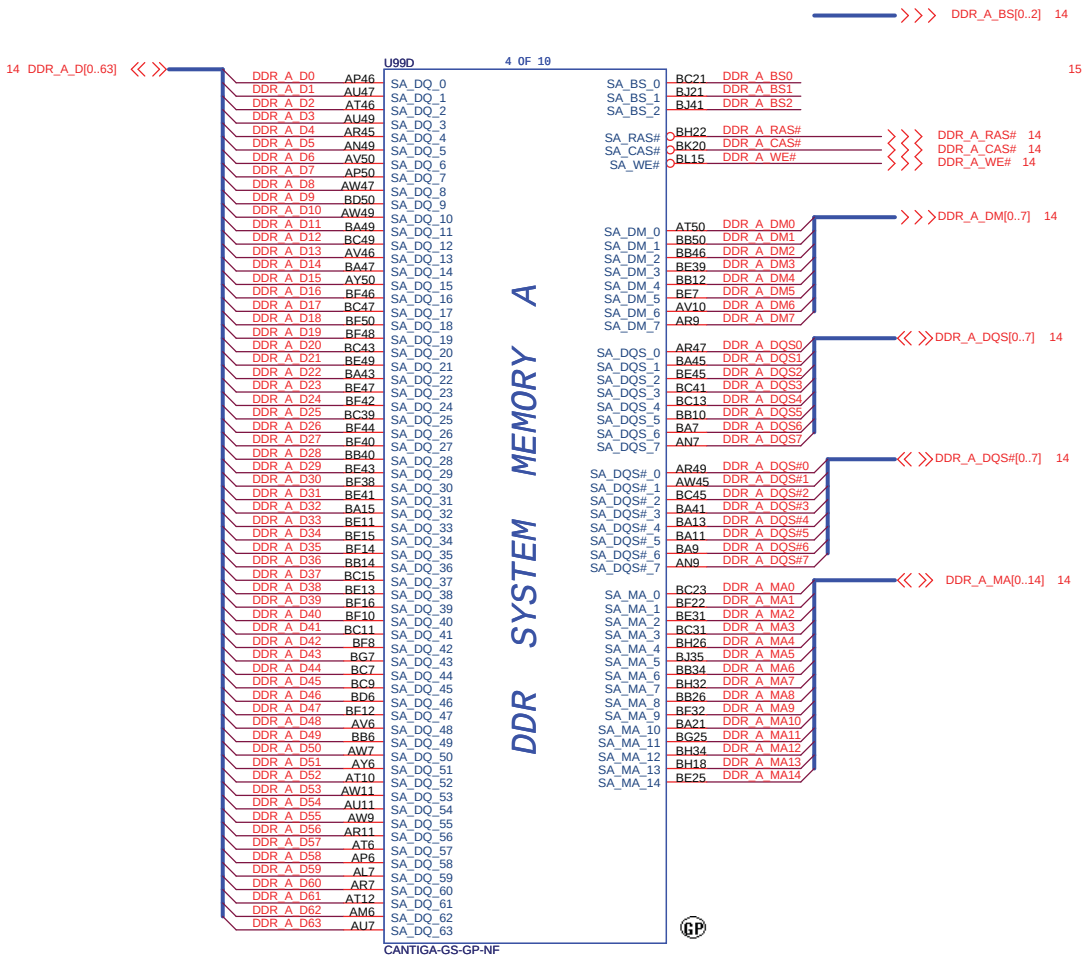
0120 SI1

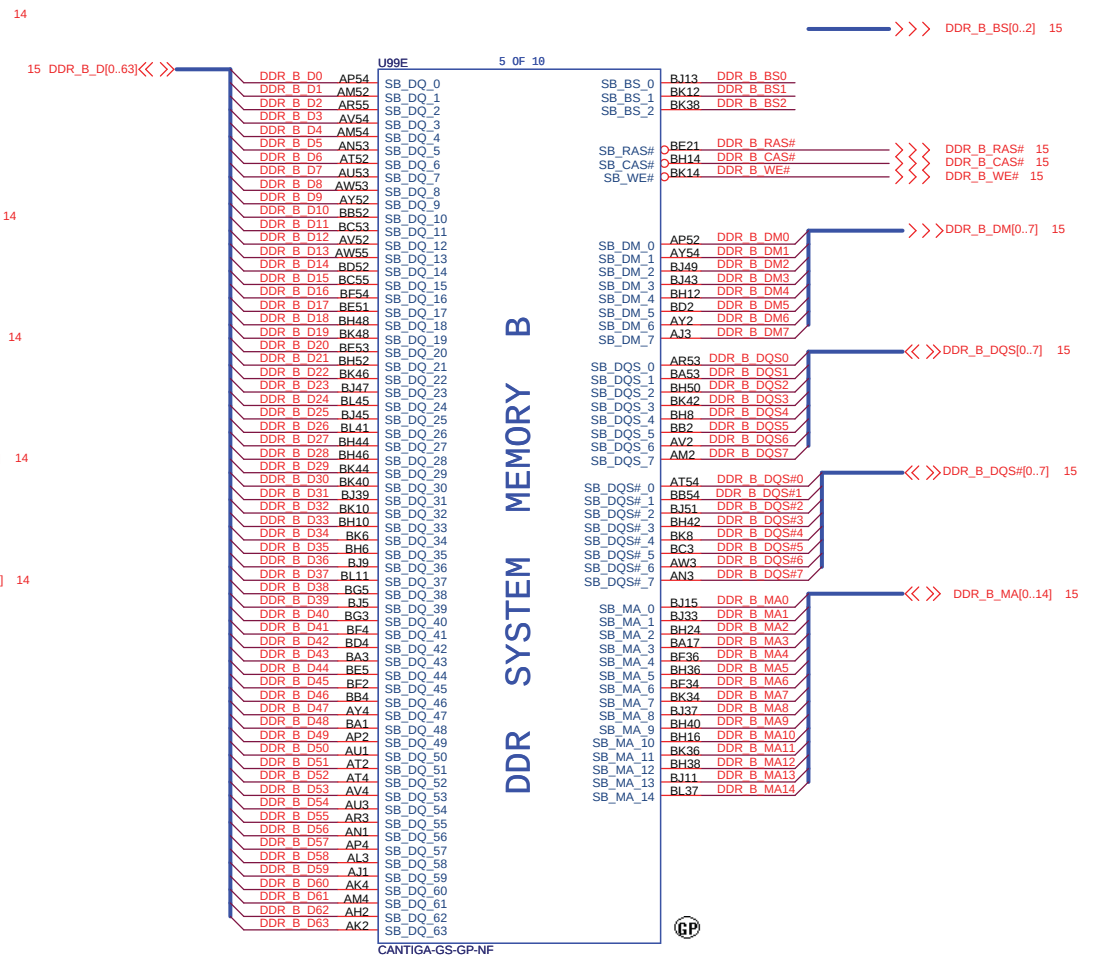
0418 SI2b Change L15, L17 and L18 from 120nH to 39nH for solving RGB rising/falling time failed issue.

CRT Termination/EMI Filter
T-Filter network should be placed near CANTIGA.

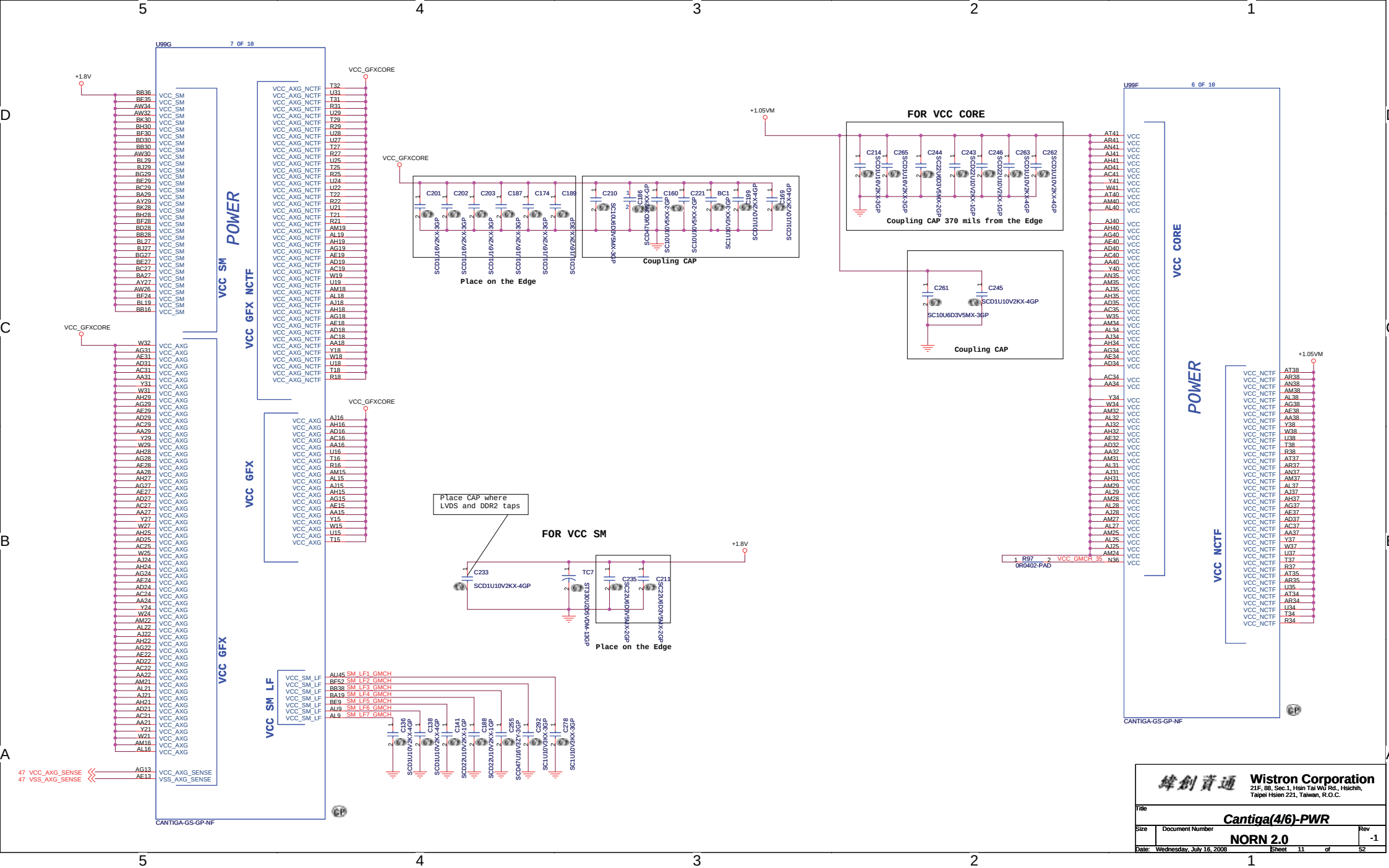
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga(2/6)-LVDS/VGA
Size: Document Number: NORN 2.0 Rev: -1
Date: Wednesday, July 16, 2008 Sheet 9 of 52





緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Cantiga(3/6)-DDR2***	
Size	Document Number **NORN 2.0**	Rev -1
Date: Wednesday, July 16, 2008	Sheet 10 of 52	

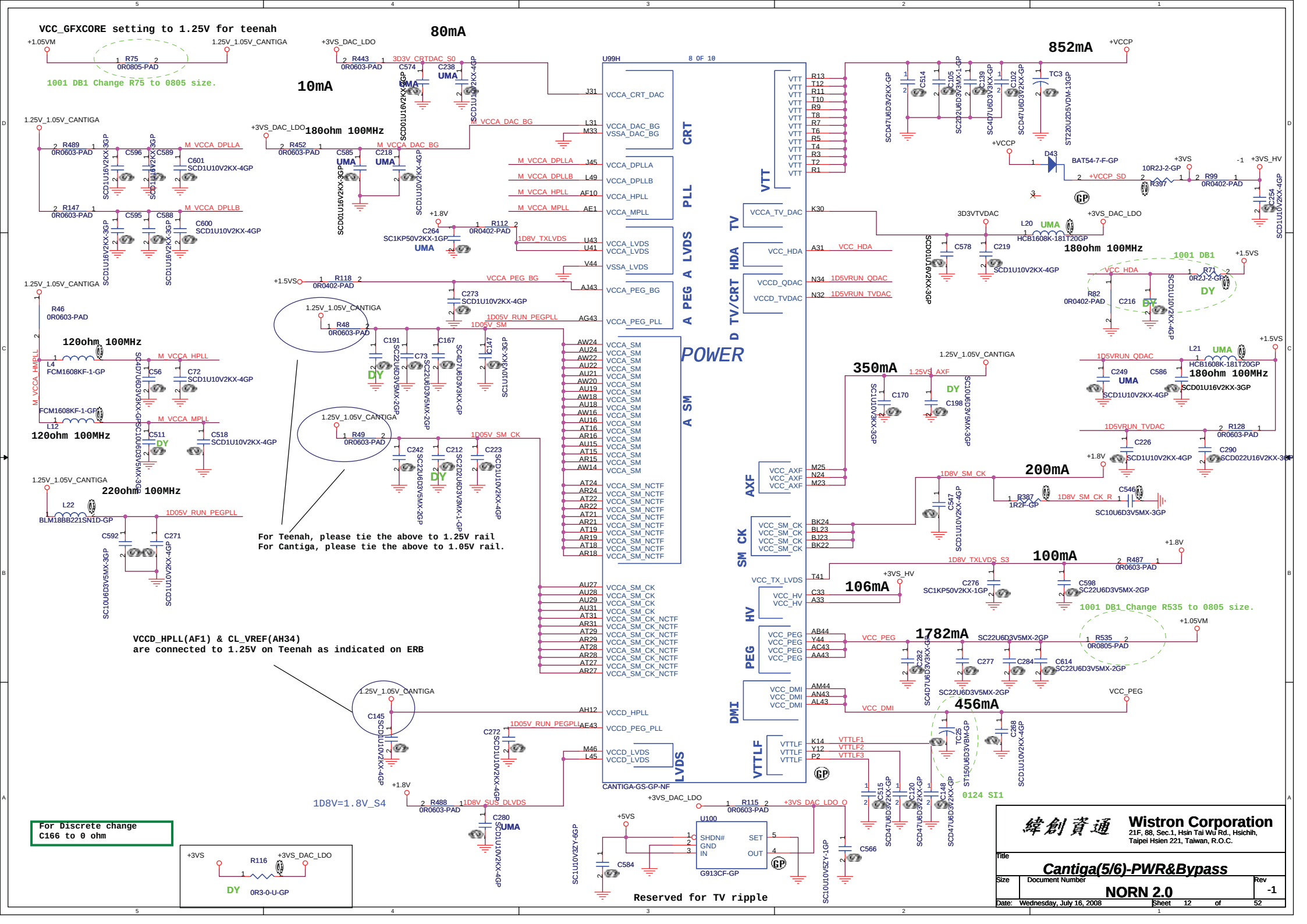


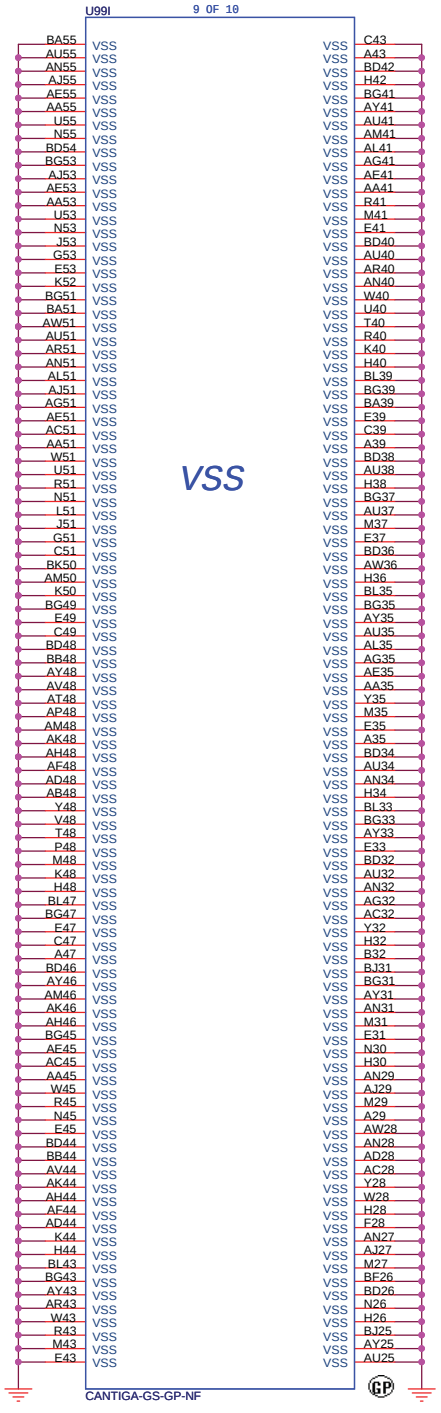
蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

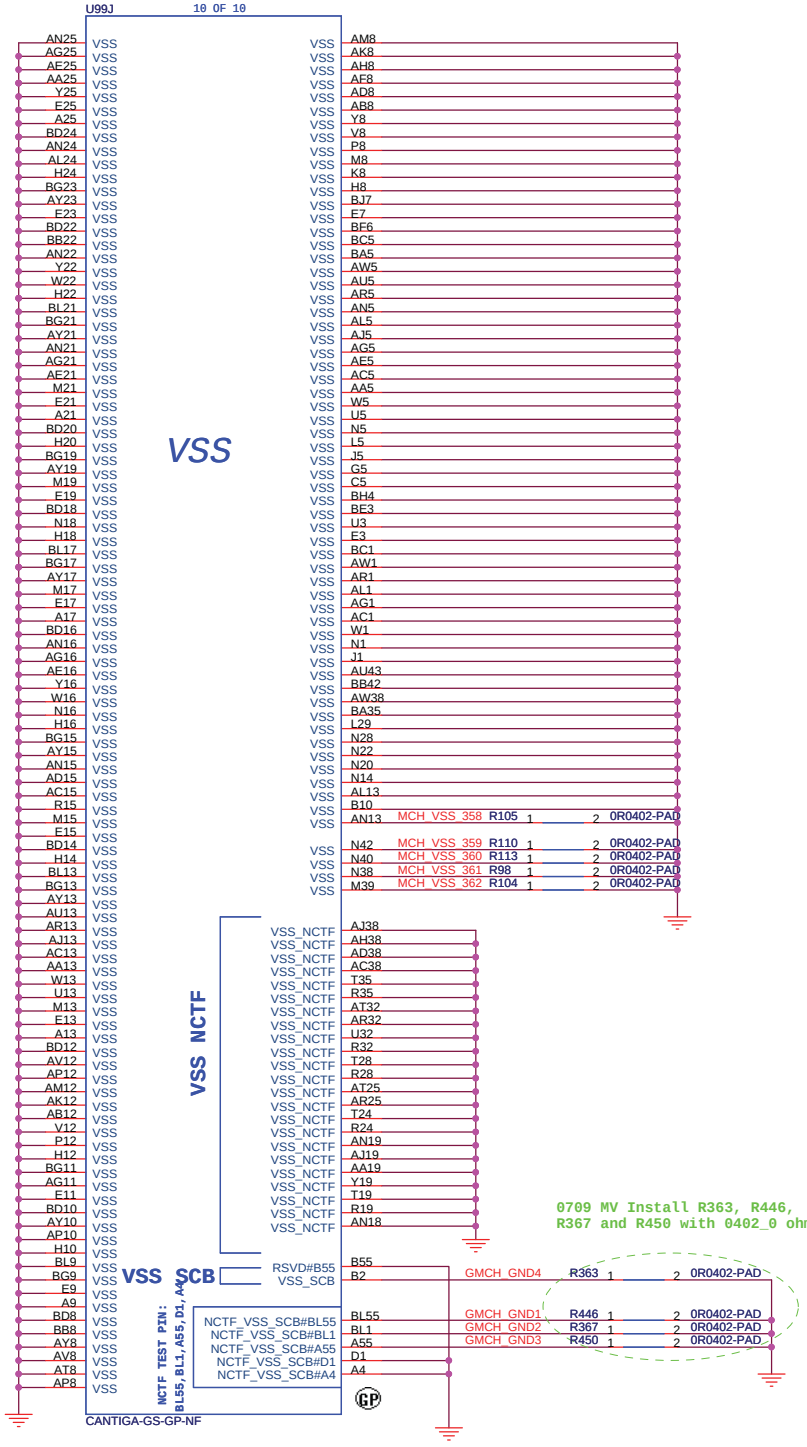
Title: Cantiga(4/6)-PWR

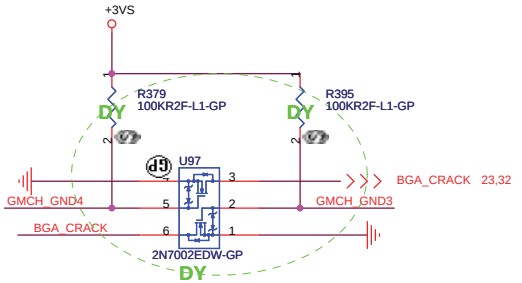
Size: | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 11 of 52

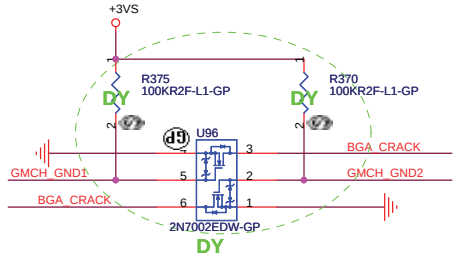

VCC_GFXCORE setting to 1.25V for teenah
1001 DB1 Change R75 to 0805 size.
80mA
10mA
852mA
350mA
200mA
100mA
106mA
1782mA
456mA
180ohm 100MHz
120ohm 100MHz
220ohm 100MHz
U99H
8 OF 10
POWER
CRT
PLL
LVDS
PEG
TV/CRT HDA
SM CK
AXF
HV
DMI
VTTLF
VTT
CANTIGA-GS-GP-NF
For Teenah, please tie the above to 1.25V rail
For Cantiga, please tie the above to 1.05V rail.
VCCD_HPLL(AF1) & CL_VREF(AH34)
are connected to 1.25V on Teenah as indicated on ERB
For Discrete change
C166 to 0 ohm
1D8V=1.8V_S4
Reserved for TV ripple
1001 DB1 Change R535 to 0805 size.
0124 SI1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Cantiga(5/6)-PWR&Bypass
NORN 2.0
Wednesday, July 16, 2008





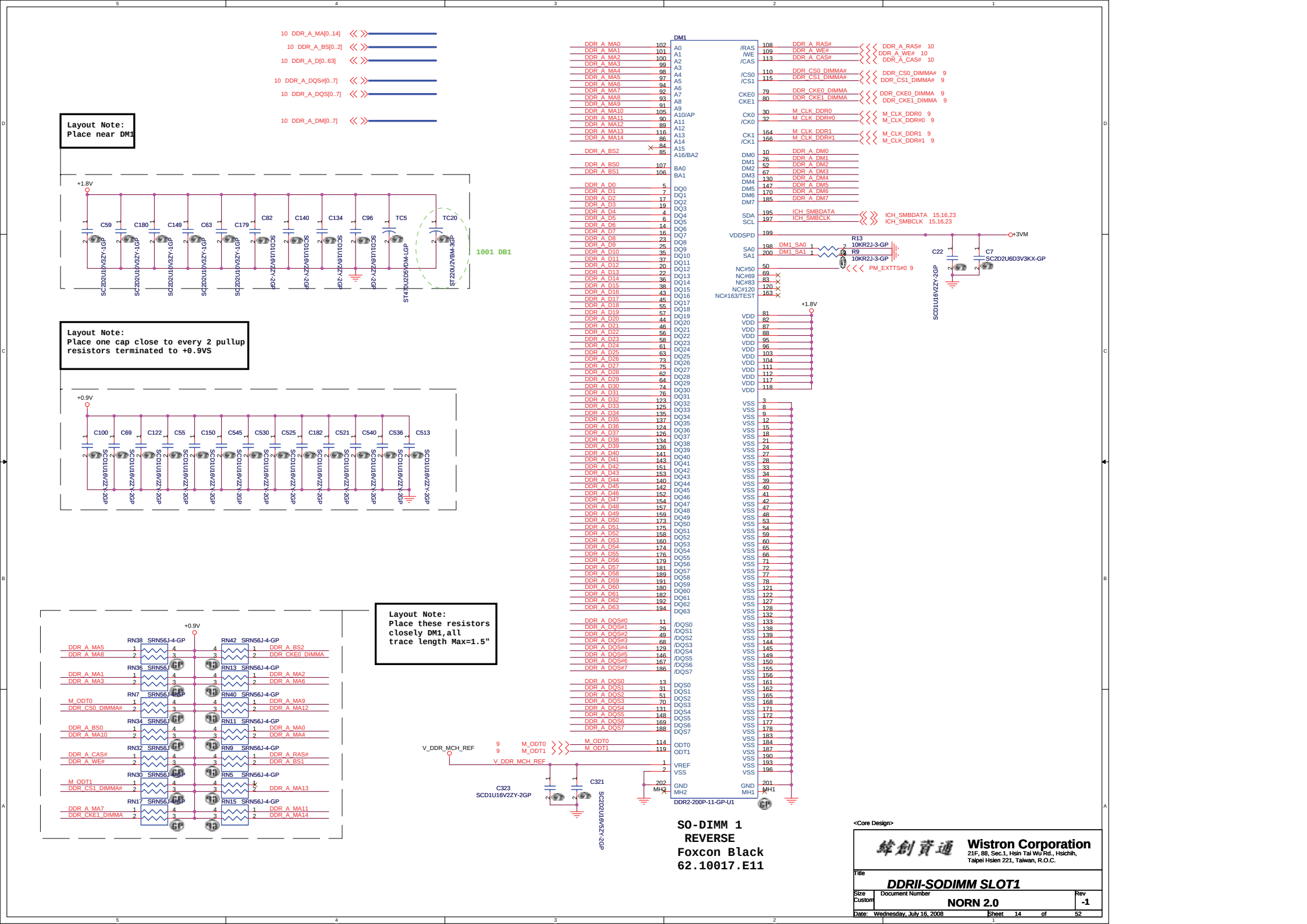


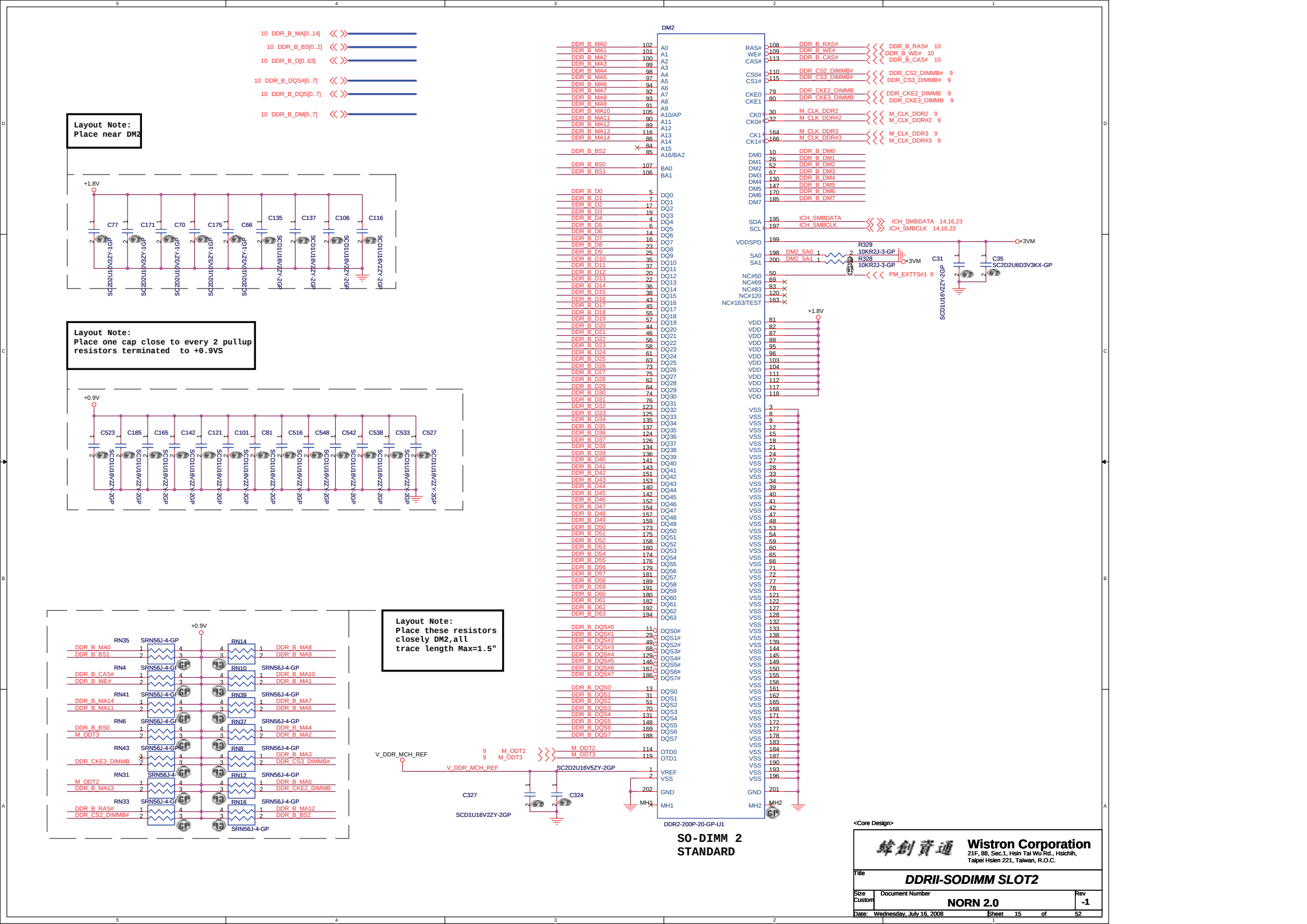
0709 MV Not install U97, U96, R379, R395, R375 and R370.

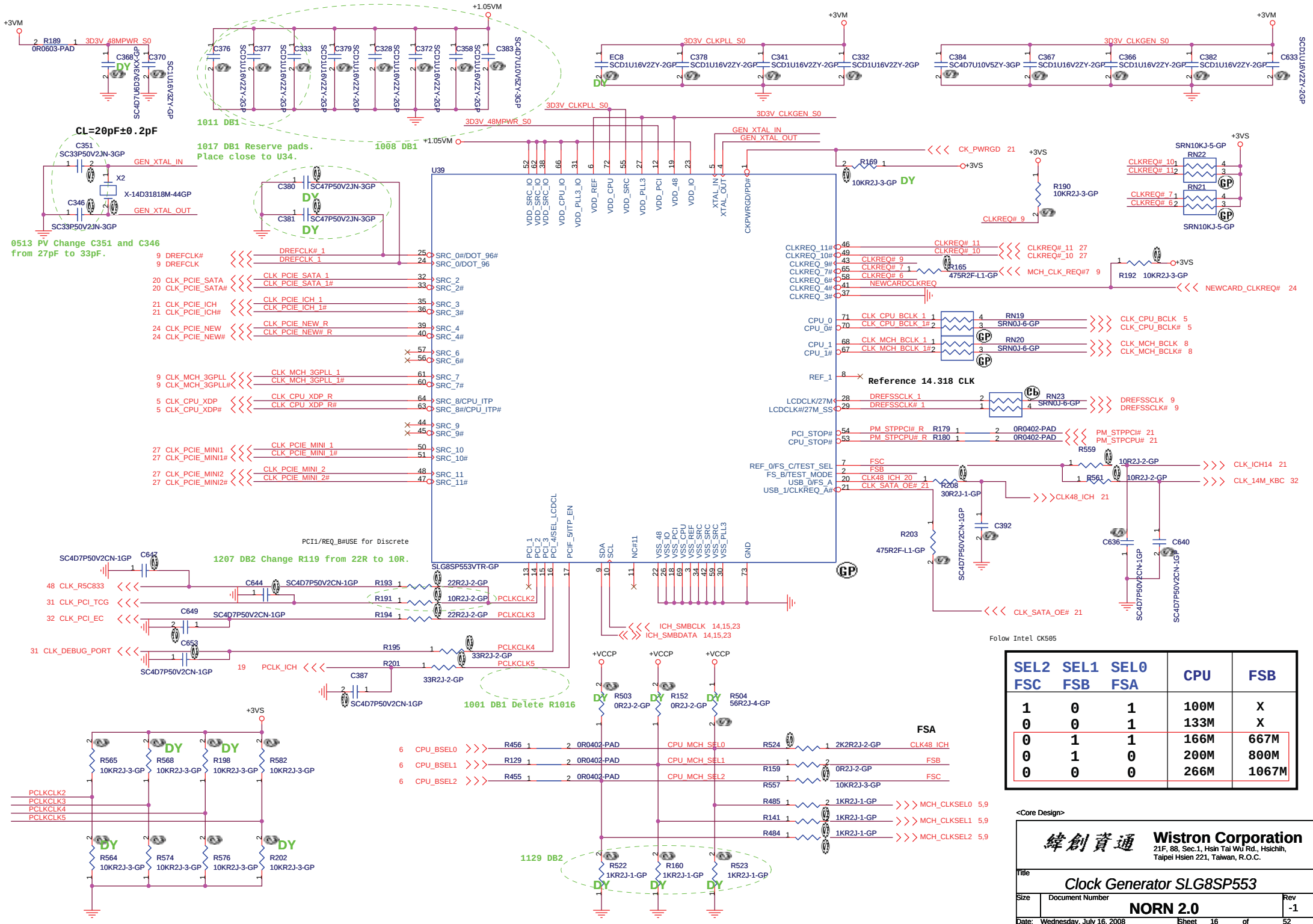


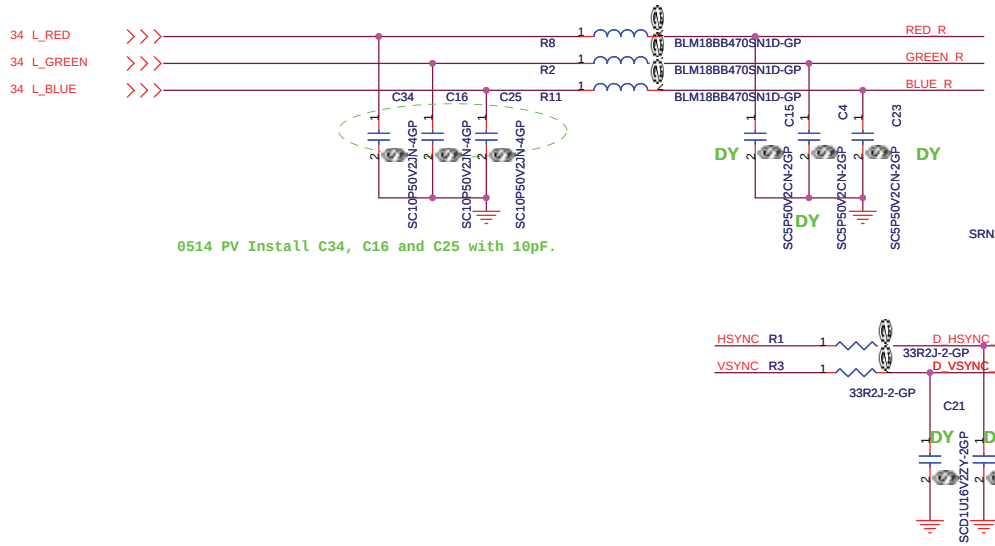
0709 MV Install R363, R446, R367 and R450 with 0402_0 ohm pads.

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Cantiga(6/6)-GND***	
Size	Document Number **NORN 2.0**	Rev -1
Date: Wednesday, July 16, 2008	Sheet 13 of 52	


10 DDR_A_MA[0..14]
10 DDR_A_BS[0..2]
10 DDR_A_D[0..63]
10 DDR_A_DQS#[0..7]
10 DDR_A_DQS[0..7]
10 DDR_A_DM[0..7]
Layout Note:
Place near DM1
+1.8V
C59
C180
C149
C63
C179
C82
C140
C134
C96
TC5
TC20
SC220U2V-1GP
SCD1U16V2ZY-2GP
ST470U2D5VDM-1GP
ST220U2VBM-3GP
1001 DB1
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
+0.9V
C100
C69
C122
C55
C150
C545
C530
C525
C182
C521
C540
C536
C513
SCD1U16V2ZY-2GP
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
+0.9V
RN38 SRN56J-4-GP
RN42 SRN56J-4-GP
RN36 SRN56J-4-GP
RN13 SRN56J-4-GP
RN7 SRN56J-4-GP
RN40 SRN56J-4-GP
RN34 SRN56J-4-GP
RN11 SRN56J-4-GP
RN32 SRN56J-4-GP
RN9 SRN56J-4-GP
RN30 SRN56J-4-GP
RN5 SRN56J-4-GP
RN17 SRN56J-4-GP
RN15 SRN56J-4-GP
DDR_A_MA5
DDR_A_MA8
DDR_A_BS2
DDR_CKE0_DIMMA
DDR_A_MA1
DDR_A_MA3
DDR_A_MA2
DDR_A_MA6
M_ODT0
DDR_CS0_DIMMA#
DDR_A_MA9
DDR_A_MA12
DDR_A_BS0
DDR_A_MA10
DDR_A_MA0
DDR_A_MA4
DDR_A_CAS#
DDR_A_WE#
DDR_A_RAS#
DDR_A_BS1
M_ODT1
DDR_CS1_DIMMA#
DDR_A_MA13
DDR_A_MA7
DDR_CKE1_DIMMA
DDR_A_MA11
DDR_A_MA14
DM1
DDR_A_MA0
DDR_A_MA1
DDR_A_MA2
DDR_A_MA3
DDR_A_MA4
DDR_A_MA5
DDR_A_MA6
DDR_A_MA7
DDR_A_MA8
DDR_A_MA9
DDR_A_MA10
DDR_A_MA11
DDR_A_MA12
DDR_A_MA13
DDR_A_MA14
DDR_A_BS2
DDR_A_BS0
DDR_A_BS1
DDR_A_D0
DDR_A_D1
DDR_A_D2
DDR_A_D3
DDR_A_D4
DDR_A_D5
DDR_A_D6
DDR_A_D7
DDR_A_D8
DDR_A_D9
DDR_A_D10
DDR_A_D11
DDR_A_D12
DDR_A_D13
DDR_A_D14
DDR_A_D15
DDR_A_D16
DDR_A_D17
DDR_A_D18
DDR_A_D19
DDR_A_D20
DDR_A_D21
DDR_A_D22
DDR_A_D23
DDR_A_D24
DDR_A_D25
DDR_A_D26
DDR_A_D27
DDR_A_D28
DDR_A_D29
DDR_A_D30
DDR_A_D31
DDR_A_D32
DDR_A_D33
DDR_A_D34
DDR_A_D35
DDR_A_D36
DDR_A_D37
DDR_A_D38
DDR_A_D39
DDR_A_D40
DDR_A_D41
DDR_A_D42
DDR_A_D43
DDR_A_D44
DDR_A_D45
DDR_A_D46
DDR_A_D47
DDR_A_D48
DDR_A_D49
DDR_A_D50
DDR_A_D51
DDR_A_D52
DDR_A_D53
DDR_A_D54
DDR_A_D55
DDR_A_D56
DDR_A_D57
DDR_A_D58
DDR_A_D59
DDR_A_D60
DDR_A_D61
DDR_A_D62
DDR_A_D63
DDR_A_DQS#0
DDR_A_DQS#1
DDR_A_DQS#2
DDR_A_DQS#3
DDR_A_DQS#4
DDR_A_DQS#5
DDR_A_DQS#6
DDR_A_DQS#7
DDR_A_DQS0
DDR_A_DQS1
DDR_A_DQS2
DDR_A_DQS3
DDR_A_DQS4
DDR_A_DQS5
DDR_A_DQS6
DDR_A_DQS7
M_ODT0
M_ODT1
V_DDR_MCH_REF
DDR2-200P-11-GP-U1
/RAS
/WE
/CAS
/CS0
/CS1
CKE0
CKE1
CK0
/CK0
CK1
/CK1
DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7
SDA
SCL
VDDSPD
SA0
SA1
NC#50
NC#69
NC#83
NC#120
NC#163/TEST
VDD
VSS
GND
MH1
MH2
DDR_A_RAS# 10
DDR_A_WE# 10
DDR_A_CAS# 10
DDR_CS0_DIMMA# 9
DDR_CS1_DIMMA# 9
DDR_CKE0_DIMMA 9
DDR_CKE1_DIMMA 9
M_CLK_DDR0 9
M_CLK_DDR#0 9
M_CLK_DDR1 9
M_CLK_DDR#1 9
DDR_A_DM0
DDR_A_DM1
DDR_A_DM2
DDR_A_DM3
DDR_A_DM4
DDR_A_DM5
DDR_A_DM6
DDR_A_DM7
ICH_SMBDATA 15,16,23
ICH_SMBCLK 15,16,23
+3VM
DM1_SA0
DM1_SA1
R13 10KR2J-3-GP
R9 10KR2J-3-GP
PM_EXTTS#0 9
C22
C7 SC2D2U6D3V3KX-GP
SCD1U16V2ZY-2GP
+1.8V
C323 SCD1U16V2ZY-2GP
C321 SC220U16V5ZY-2GP
SO-DIMM 1
REVERSE
Foxcon Black
62.10017.E11
<Core Design>
蜂創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT1
Size
Custom
Document Number
NORN 2.0
Rev
-1
Date: Wednesday, July 16, 2008
Sheet 14 of 52

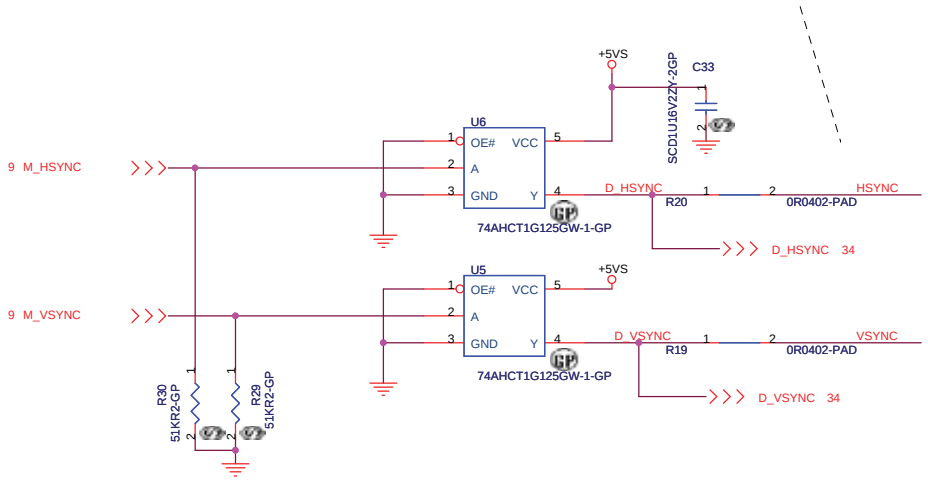

10 DDR_B_MA[0..14]
10 DDR_B_BS[0..2]
10 DDR_B_D[0..63]
10 DDR_B_DQS#[0..7]
10 DDR_B_DQS[0..7]
10 DDR_B_DM[0..7]
Layout Note:
Place near DM2
+1.8V
C77
C171
C70
C175
C66
C135
C137
C106
C116
SCD1U16V2ZY-2GP
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
+0.9V
C523
C185
C165
C142
C121
C101
C81
C516
C548
C542
C538
C533
C527
SCD1U16V2ZY-2GP
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
+0.9V
RN35
RN4
RN41
RN6
RN43
RN31
RN33
RN14
RN10
RN39
RN37
RN8
RN12
RN16
SRN56J-4-GP
DDR_B_MA0
DDR_B_BS1
DDR_B_CAS#
DDR_B_WE#
DDR_B_MA14
DDR_B_MA11
DDR_B_BS0
M_ODT3
DDR_CKE3_DIMMB
M_ODT2
DDR_B_MA13
DDR_B_RAS#
DDR_CS2_DIMMB#
DDR_B_MA8
DDR_B_MA9
DDR_B_MA10
DDR_B_MA1
DDR_B_MA7
DDR_B_MA6
DDR_B_MA4
DDR_B_MA2
DDR_B_MA3
DDR_CS3_DIMMB#
DDR_B_MA5
DDR_CKE2_DIMMB
DDR_B_MA12
DDR_B_BS2
V_DDR_MCH_REF
C327
C324
SCD1U16V2ZY-2GP
SC2D2U16V5ZY-2GP
M_ODT2
M_ODT3
DM2
DDR_B_MA0
DDR_B_MA1
DDR_B_MA2
DDR_B_MA3
DDR_B_MA4
DDR_B_MA5
DDR_B_MA6
DDR_B_MA7
DDR_B_MA8
DDR_B_MA9
DDR_B_MA10
DDR_B_MA11
DDR_B_MA12
DDR_B_MA13
DDR_B_MA14
DDR_B_BS2
DDR_B_BS0
DDR_B_BS1
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12
A13
A14
A15
A16/BA2
BA0
BA1
DDR_B_D0
DDR_B_D1
DDR_B_D2
DDR_B_D3
DDR_B_D4
DDR_B_D5
DDR_B_D6
DDR_B_D7
DDR_B_D8
DDR_B_D9
DDR_B_D10
DDR_B_D11
DDR_B_D12
DDR_B_D13
DDR_B_D14
DDR_B_D15
DDR_B_D16
DDR_B_D17
DDR_B_D18
DDR_B_D19
DDR_B_D20
DDR_B_D21
DDR_B_D22
DDR_B_D23
DDR_B_D24
DDR_B_D25
DDR_B_D26
DDR_B_D27
DDR_B_D28
DDR_B_D29
DDR_B_D30
DDR_B_D31
DDR_B_D32
DDR_B_D33
DDR_B_D34
DDR_B_D35
DDR_B_D36
DDR_B_D37
DDR_B_D38
DDR_B_D39
DDR_B_D40
DDR_B_D41
DDR_B_D42
DDR_B_D43
DDR_B_D44
DDR_B_D45
DDR_B_D46
DDR_B_D47
DDR_B_D48
DDR_B_D49
DDR_B_D50
DDR_B_D51
DDR_B_D52
DDR_B_D53
DDR_B_D54
DDR_B_D55
DDR_B_D56
DDR_B_D57
DDR_B_D58
DDR_B_D59
DDR_B_D60
DDR_B_D61
DDR_B_D62
DDR_B_D63
DDR_B_DQS#0
DDR_B_DQS#1
DDR_B_DQS#2
DDR_B_DQS#3
DDR_B_DQS#4
DDR_B_DQS#5
DDR_B_DQS#6
DDR_B_DQS#7
DDR_B_DQS0
DDR_B_DQS1
DDR_B_DQS2
DDR_B_DQS3
DDR_B_DQS4
DDR_B_DQS5
DDR_B_DQS6
DDR_B_DQS7
M_ODT2
M_ODT3
VREF
VSS
GND
MH1
DDR2-200P-20-GP-U1
RAS#
WE#
CAS#
CS0#
CS1#
CKE0
CKE1
CK0
CK0#
CK1
CK1#
DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7
SDA
SCL
VDDSPD
SA0
SA1
NC#50
NC#69
NC#83
NC#120
NC#163/TEST
VDD
VSS
GND
MH2
DDR_B_RAS#
DDR_B_WE#
DDR_B_CAS#
DDR_CS2_DIMMB#
DDR_CS3_DIMMB#
DDR_CKE2_DIMMB
DDR_CKE3_DIMMB
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3
DDR_B_DM0
DDR_B_DM1
DDR_B_DM2
DDR_B_DM3
DDR_B_DM4
DDR_B_DM5
DDR_B_DM6
DDR_B_DM7
ICH_SMBDATA
ICH_SMBCLK
ICH_SMBDATA 14,16,23
ICH_SMBCLK 14,16,23
+3VM
R329
10KR2J-3-GP
R328
10KR2J-3-GP
DM2_SA0
DM2_SA1
PM_EXTTS#1 9
C31
C35
SC2D2U6D3V3KX-GP
SCD1U16V2ZY-2GP
+1.8V
SO-DIMM 2
STANDARD
<Core Design>
蜂創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT2
Size
Custom
Document Number
NORN 2.0
Rev
-1
Date: Wednesday, July 16, 2008
Sheet 15 of 52

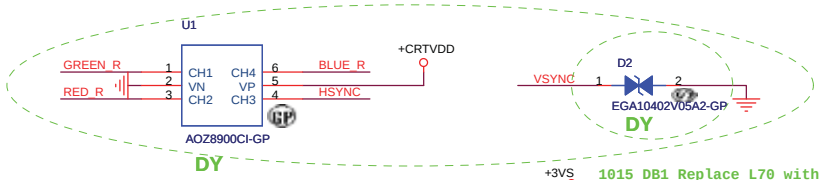

CL=20pF±0.2pF
1011 DB1
1017 DB1 Reserve pads.
Place close to U34.
1008 DB1
0513 PV Change C351 and C346
from 27pF to 33pF.
U39
SLG8SP553VTR-GP
Reference 14.318 CLK
PCI1/REQ_B#USE for Discrete
1207 DB2 Change R119 from 22R to 10R.
1001 DB1 Delete R1016
1129 DB2
Folow Intel CK505
FSA
SEL2 FSC | SEL1 FSB | SEL0 FSA | CPU | FSB
1 | 0 | 1 | 100M | X
0 | 0 | 1 | 133M | X
0 | 1 | 1 | 166M | 667M
0 | 1 | 0 | 200M | 800M
0 | 0 | 0 | 266M | 1067M
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator SLG8SP553
Size
Document Number
NORN 2.0
Rev
-1
Date: Wednesday, July 16, 2008
Sheet 16 of 52



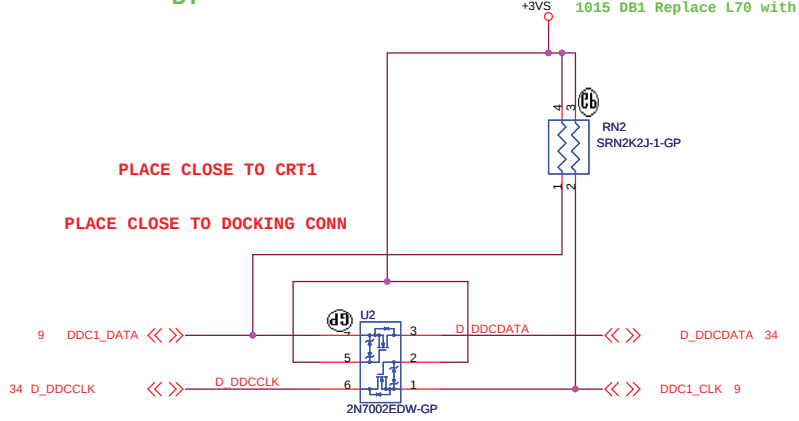
CRT

Layout Note : HSYNC & VSYNC SHOULD BE ROUTED TO DOCK CRT CONN. ,THEN TO SYSTEM CRT CONN.





1015 DB1 Replace L70 with D84.



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

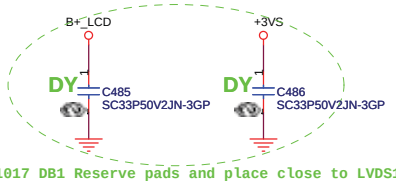
Title: ***CRT/TV CONNECTOR***

Size	Document Number	Rev
A3	NORN 2.0	-1

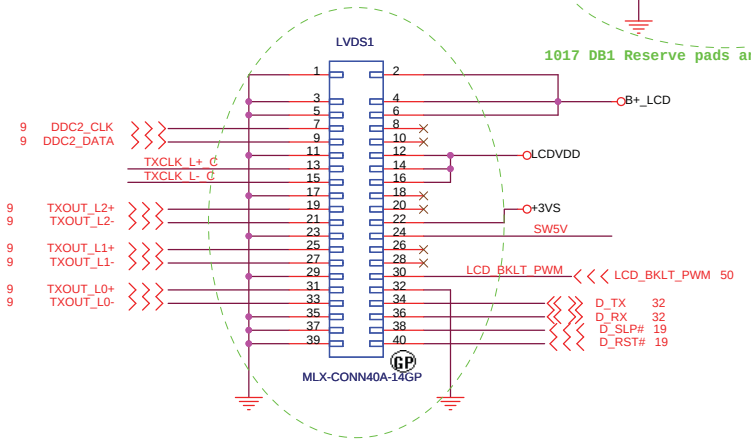
Date: Wednesday, July 16, 2008 Sheet 17 of 52

LVDS CONN

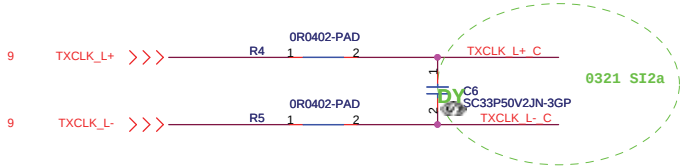
1016 DB1 Change the P/N of LVDS.



1017 DB1 Reserve pads and place close to LVDS1.

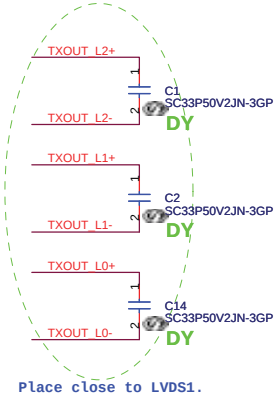


Near the LVDS1 connector

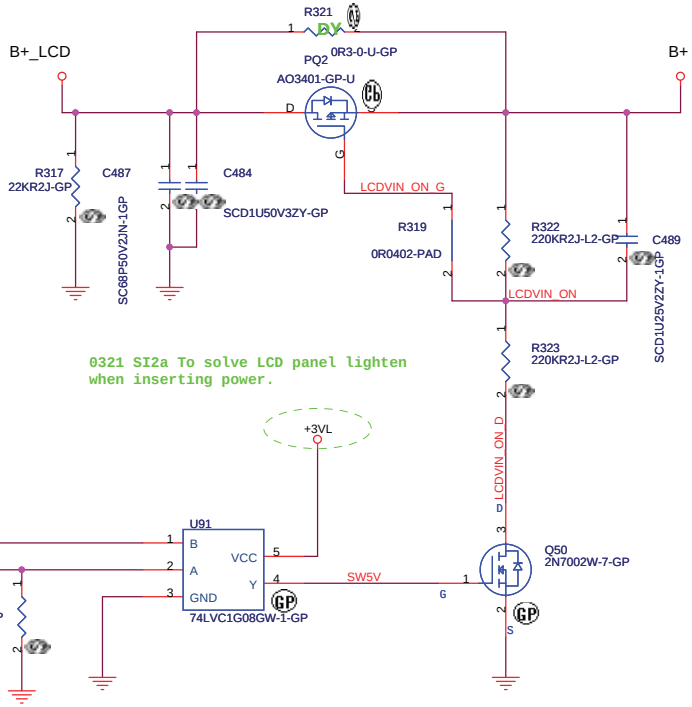


SUPPORT LED INVETER

1019 DB1 Reserve C700, C710 and C711 and place near to LVDS1.

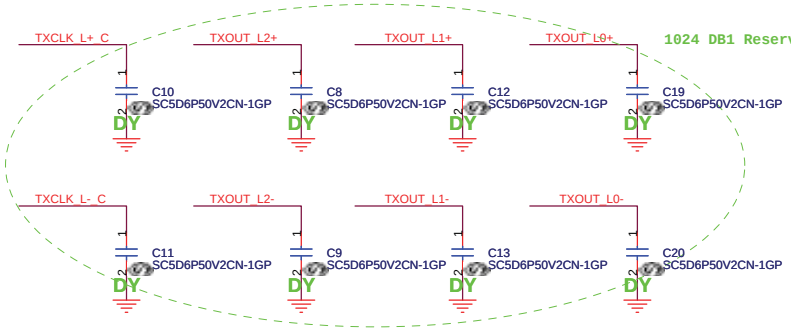


Place close to LVDS1.



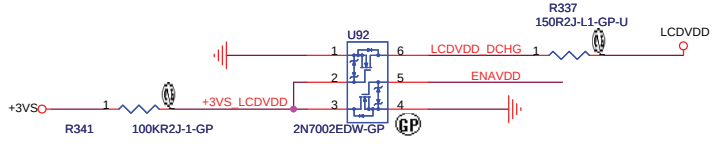
0321 SI2a To solve LCD panel lighten when inserting power.

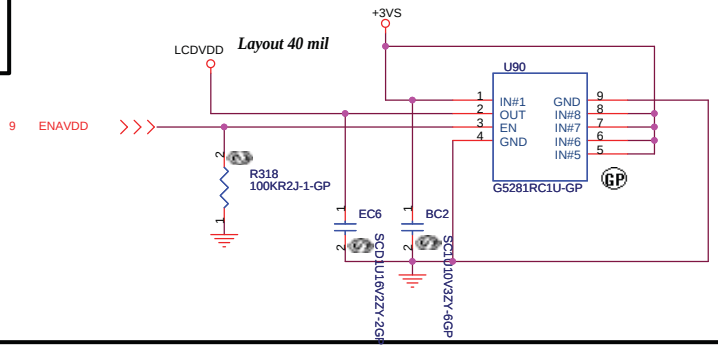
1024 DB1 Reserve Pads for RF solution.



Place close to LVDS1.

LCD POWER CIRCUIT

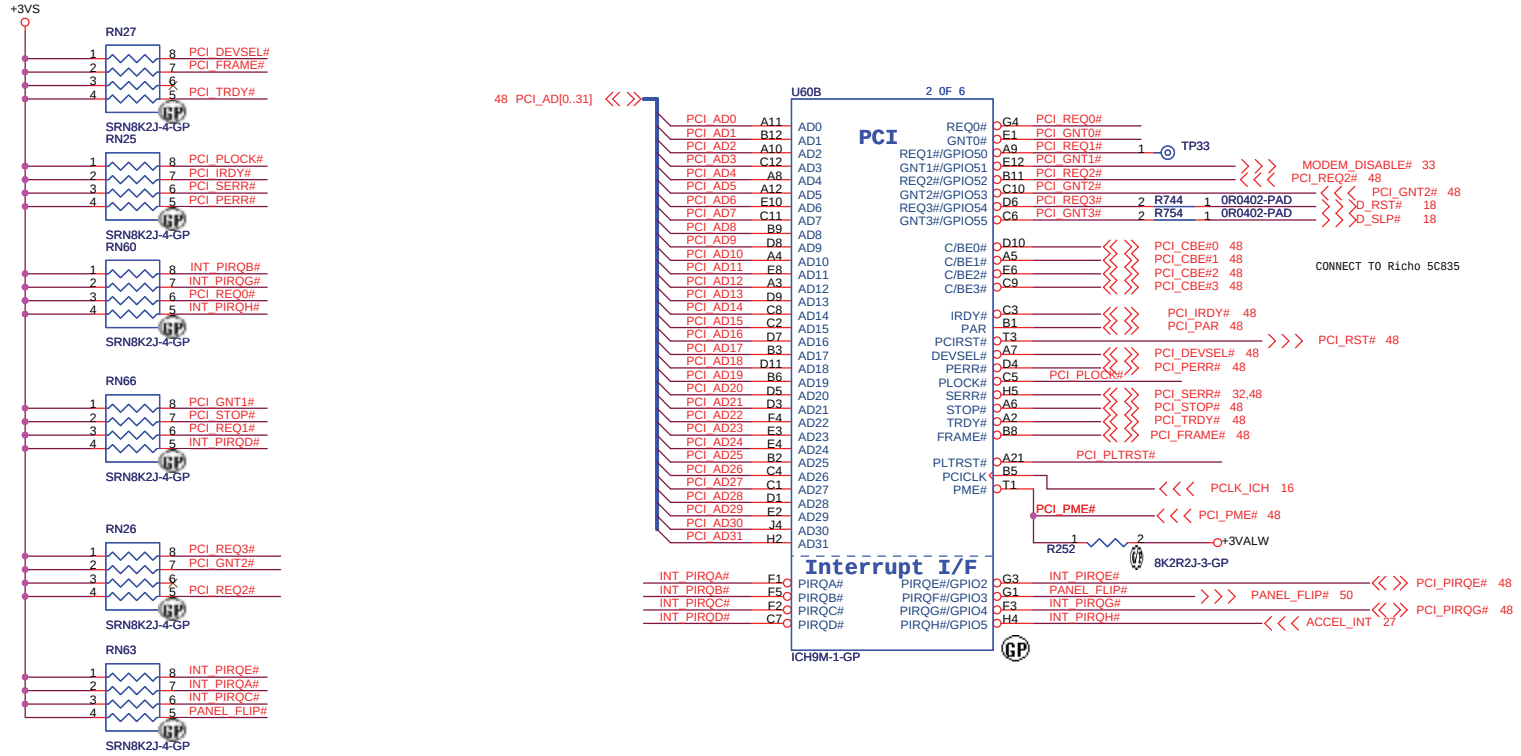




<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD CONN.	
Size A3	Document Number NORN 2.0	Rev -1
Date: Wednesday, July 16, 2008	Sheet 18 of 52	



BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	

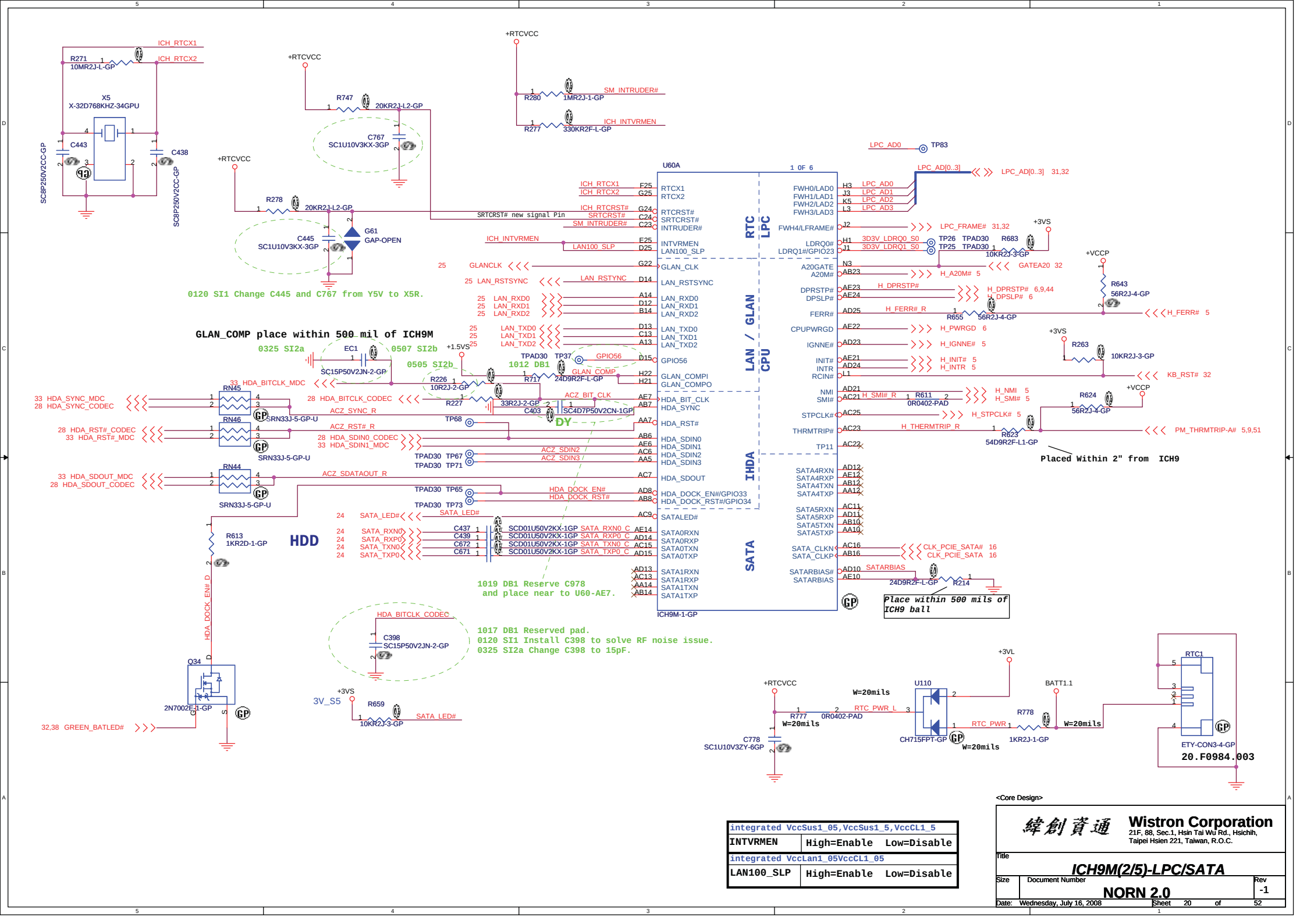
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9M(1/5)-PCI

Size | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 19 of 52



integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

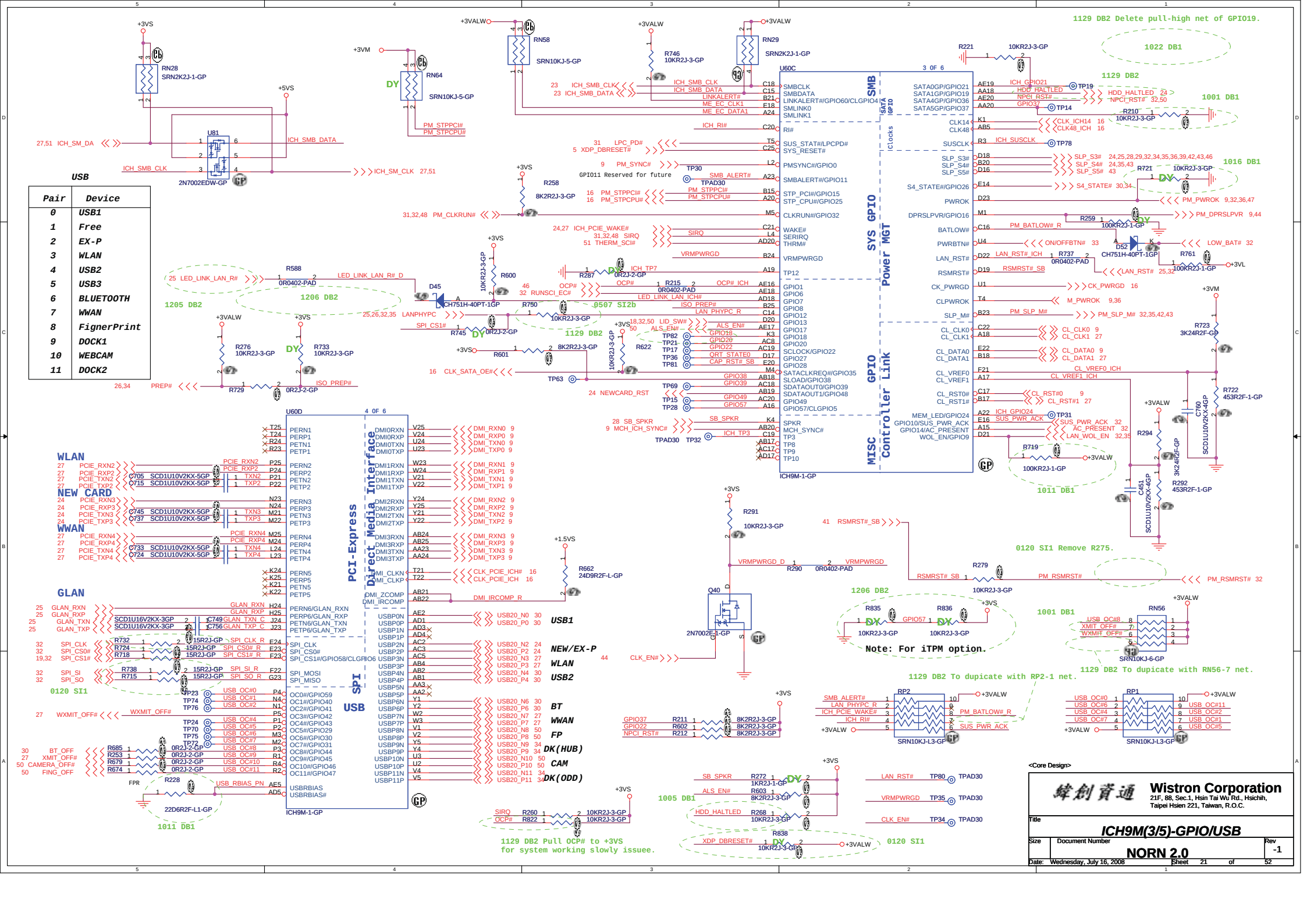
<Core Design>

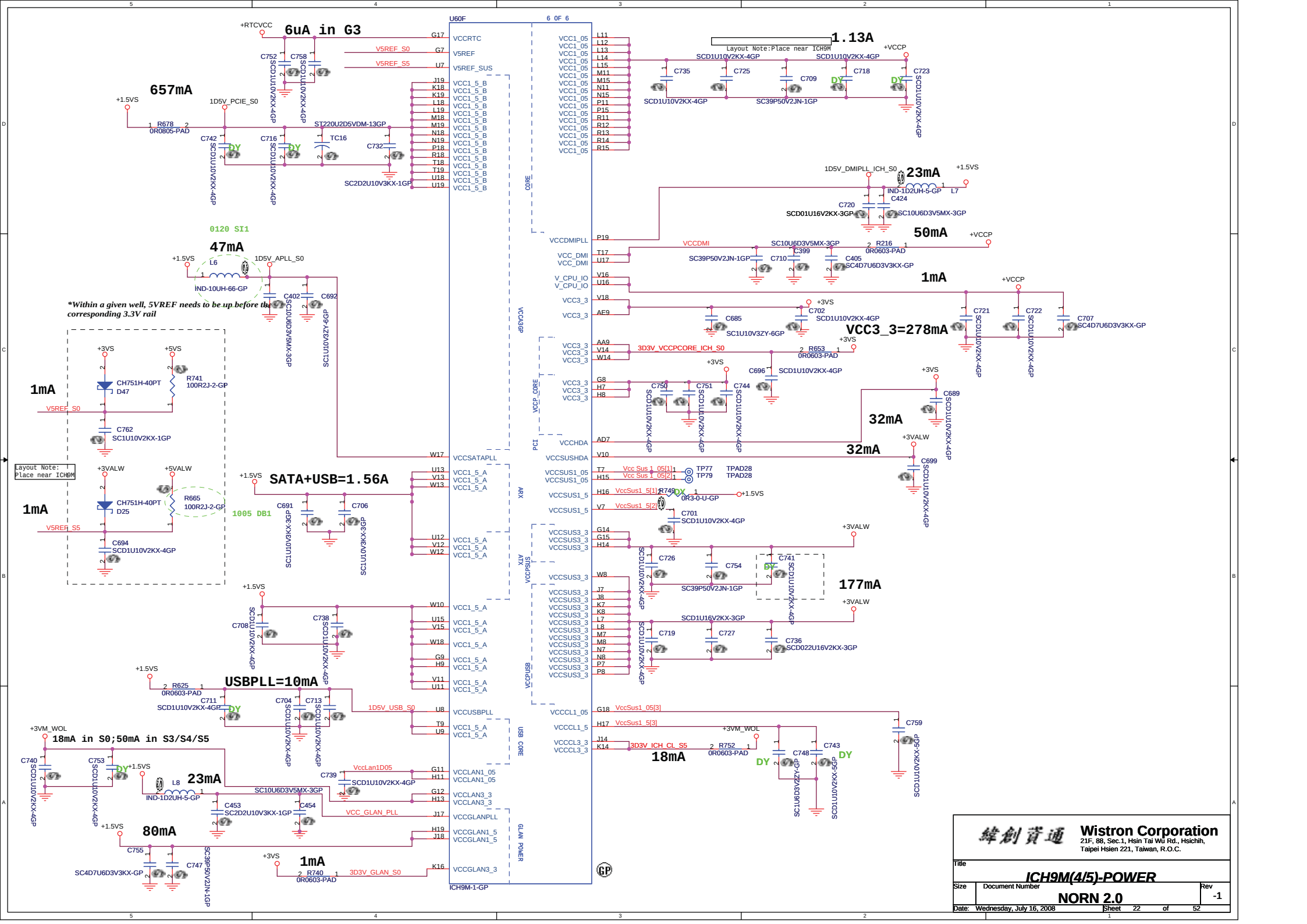
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

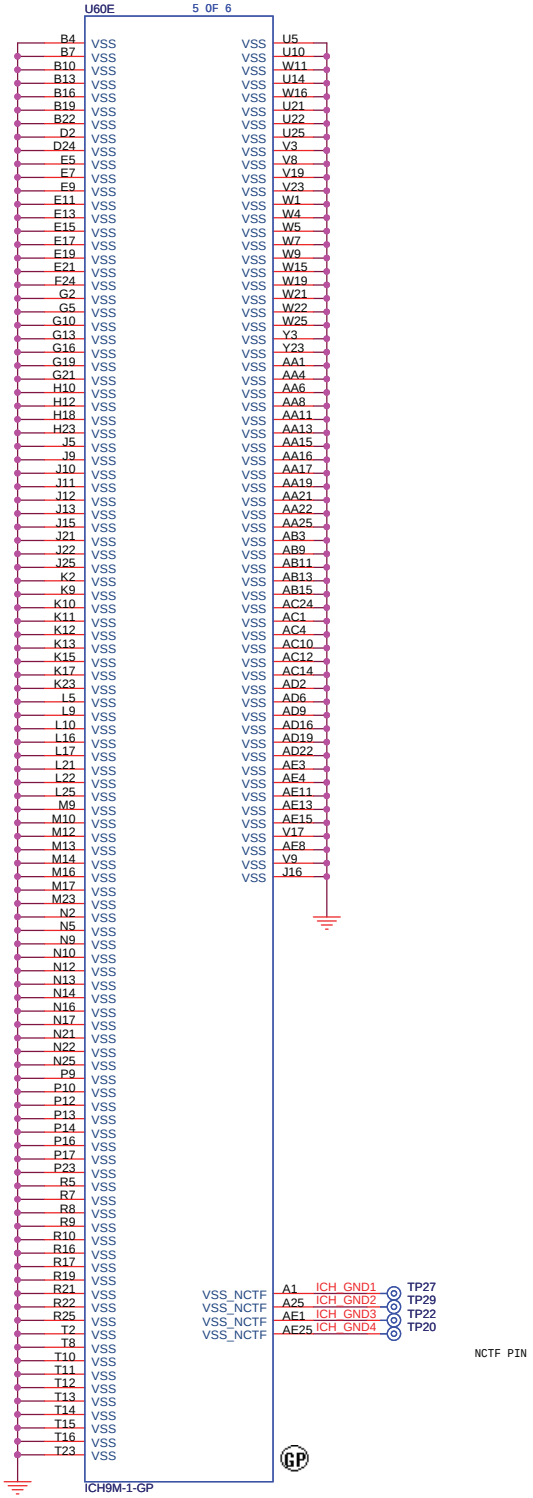
Title: ICH9M(2/5)-LPC/SATA

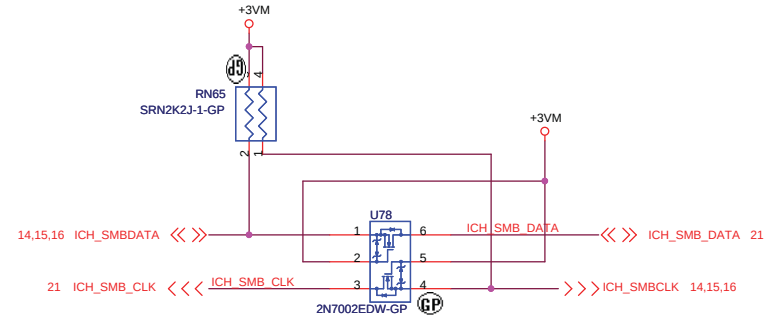
Size	Document Number	Rev
	NORN 2.0	-1

Date: Wednesday, July 16, 2008 Sheet 20 of 52


1129 DB2 Delete pull-high net of GPIO19.
1022 DB1
1129 DB2
1001 DB1
1016 DB1
USB
Pair Device
0 USB1
1 Free
2 EX-P
3 WLAN
4 USB2
5 USB3
6 BLUETOOTH
7 WWAN
8 FignerPrint
9 DOCK1
10 WEBCAM
11 DOCK2
U60C
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-1-GP
U60D
PCI-Express
Direct Media Interface
SPI
USB
WLAN
NEW CARD
WWAN
GLAN
USB1
NEW/EX-P
WLAN
USB2
BT
WWAN
FP
DK(HUB)
CAM
DK(ODD)
1205 DB2
1206 DB2
0507 SI2b
1129 DB2
1011 DB1
0120 SI1
0120 SI1 Remove R275.
1206 DB2
Note: For iTPM option.
1001 DB1
1129 DB2 To dupicate with RP2-1 net.
1129 DB2 To dupicate with RN56-7 net.
1005 DB1
1129 DB2 Pull OCP# to +3VS
for system working slowly issuee.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9M(3/5)-GPIO/USB
Size
Document Number
NORN 2.0
Rev
-1
Date: Wednesday, July 16, 2008
Sheet 21 of 52

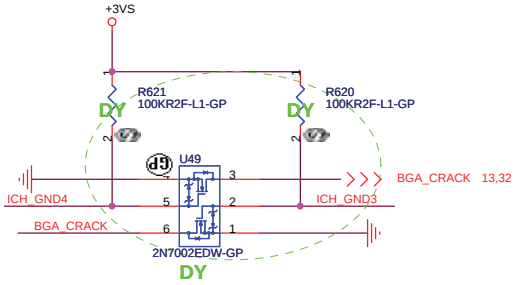

U60F
6 OF 6
6uA in G3
+RTCVCC
VCCRTC
V5REF_S0
V5REF
V5REF_S5
V5REF_SUS
657mA
1D5V_PCIE_S0
R678
0R0805-PAD
ST220U2D5VDM-13GP
TC16
SC2D2U10V3KX-1GP
0120 SI1
47mA
1D5V_APLL_S0
L6
IND-10UH-66-GP
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
1mA
CH751H-40PT
D47
R741
100R2J-2-GP
V5REF_S0
C762
SC1U10V2KX-1GP
Layout Note: Place near ICH9M
1mA
CH751H-40PT
D25
R665
100R2J-2-GP
V5REF_S5
C694
SCD1U10V2KX-4GP
SATA+USB=1.56A
1005 DB1
USBPLL=10mA
1D5V_USB_S0
18mA in S0;50mA in S3/S4/S5
23mA
IND-1D2UH-5-GP
80mA
1mA
3D3V_GLAN_S0
R740
0R0603-PAD
1.13A
Layout Note:Place near ICH9M
23mA
IND-1D2UH-5-GP
50mA
1mA
VCC3_3=278mA
32mA
32mA
177mA
18mA
3D3V_VCCPCORE_ICH_S0
R653
0R0603-PAD
3D3V_ICH_CL_S5
R752
0R0603-PAD
VccSus1_05[1]
VccSus1_05[2]
VccSus1_5[1]
VccSus1_5[2]
R749
0R3-0-U-GP
VccSus1_05[3]
VccSus1_5[3]
TP77
TP79
TPAD28
ICH9M-1-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9M(4/5)-POWER
Size
Document Number
NORN 2.0
Rev
-1
Date: Wednesday, July 16, 2008
Sheet 22 of 52



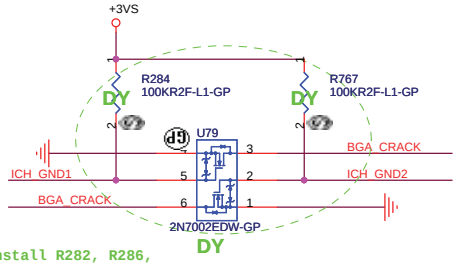


Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS



0709 MV Not install U49, U79, R621, R620, R284 and R767.



0709 MV Install R282, R286, R234 and R225 with 0402_0 ohm pads.

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

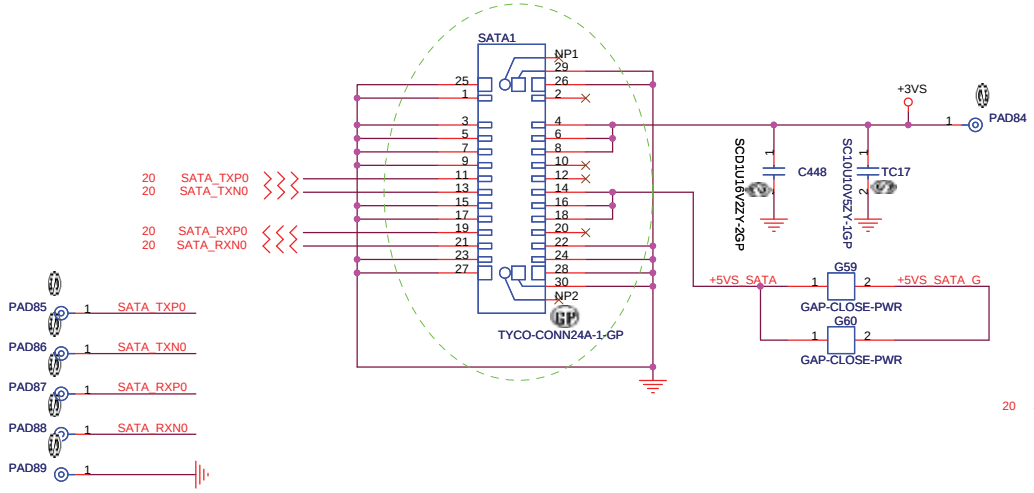
Title: **ICH9M(5/5)-GND**

Size | Document Number: **NORN 2.0** | Rev: -1

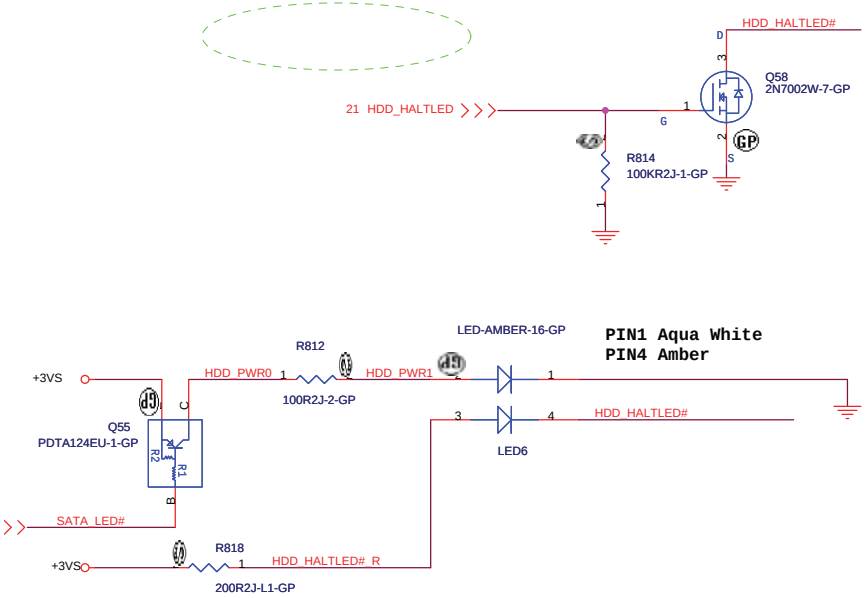
Date: Wednesday, July 16, 2008 | Sheet 23 of 52

SATA HDD

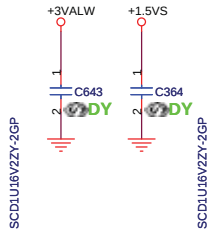
1016 DB1 Change SATA1 connector to 14 pins.
1018 DB1 Change SATA1 connector to 30 pins.
1018 DB1 Change SATA1 connector to 24 pins.



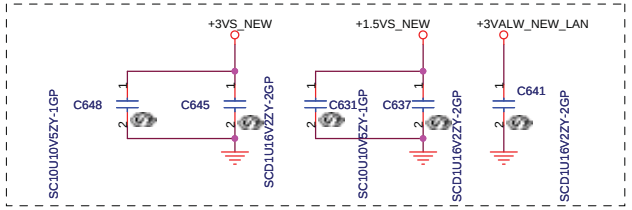
1023 DB1 Remove R384.

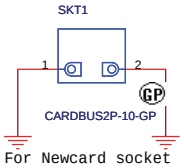


Place them Near to Chip

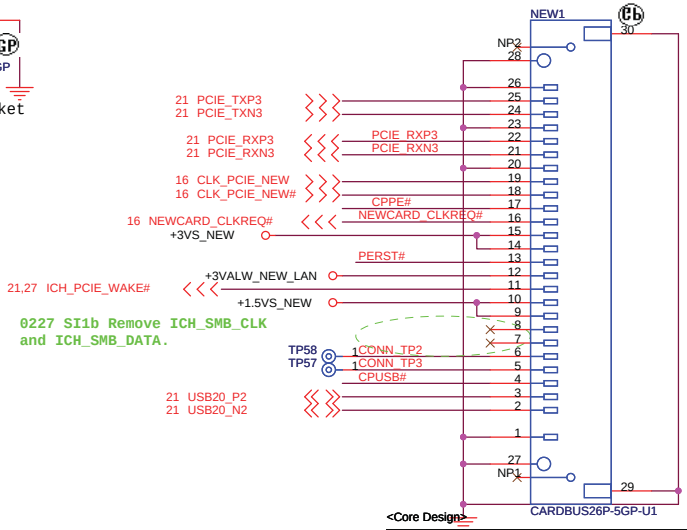


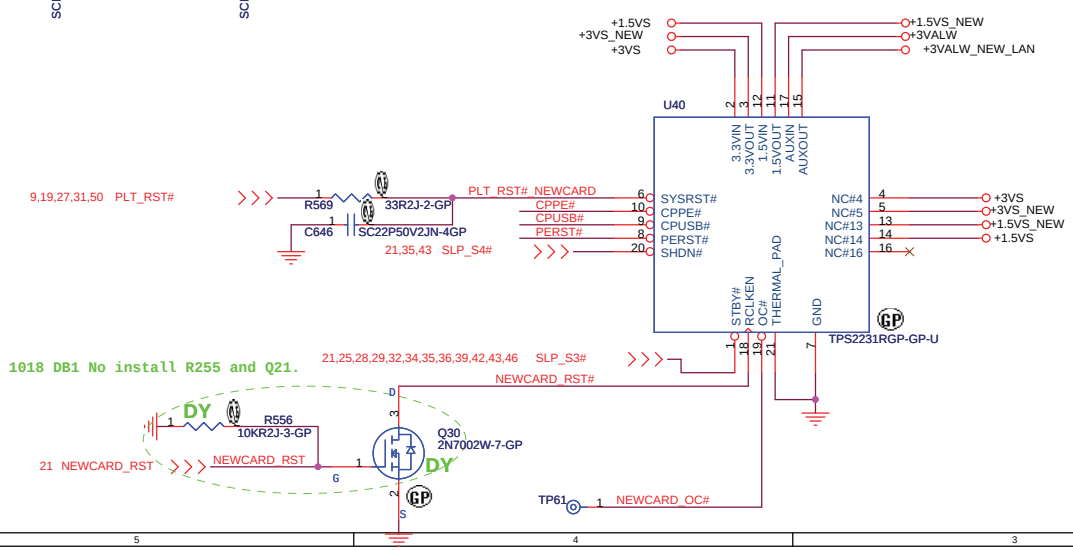
Place them Near to Connector





NEWCARD Connector



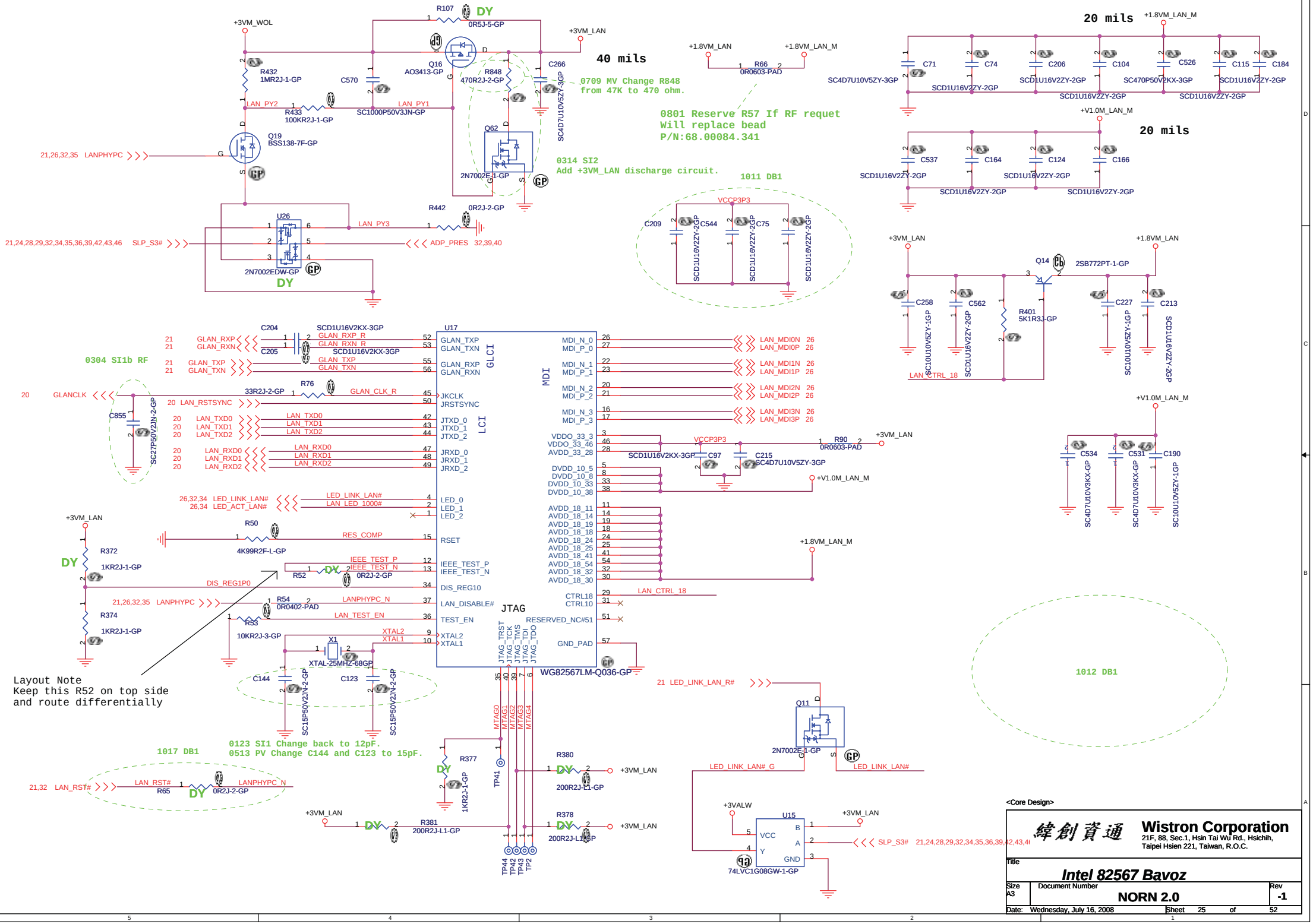


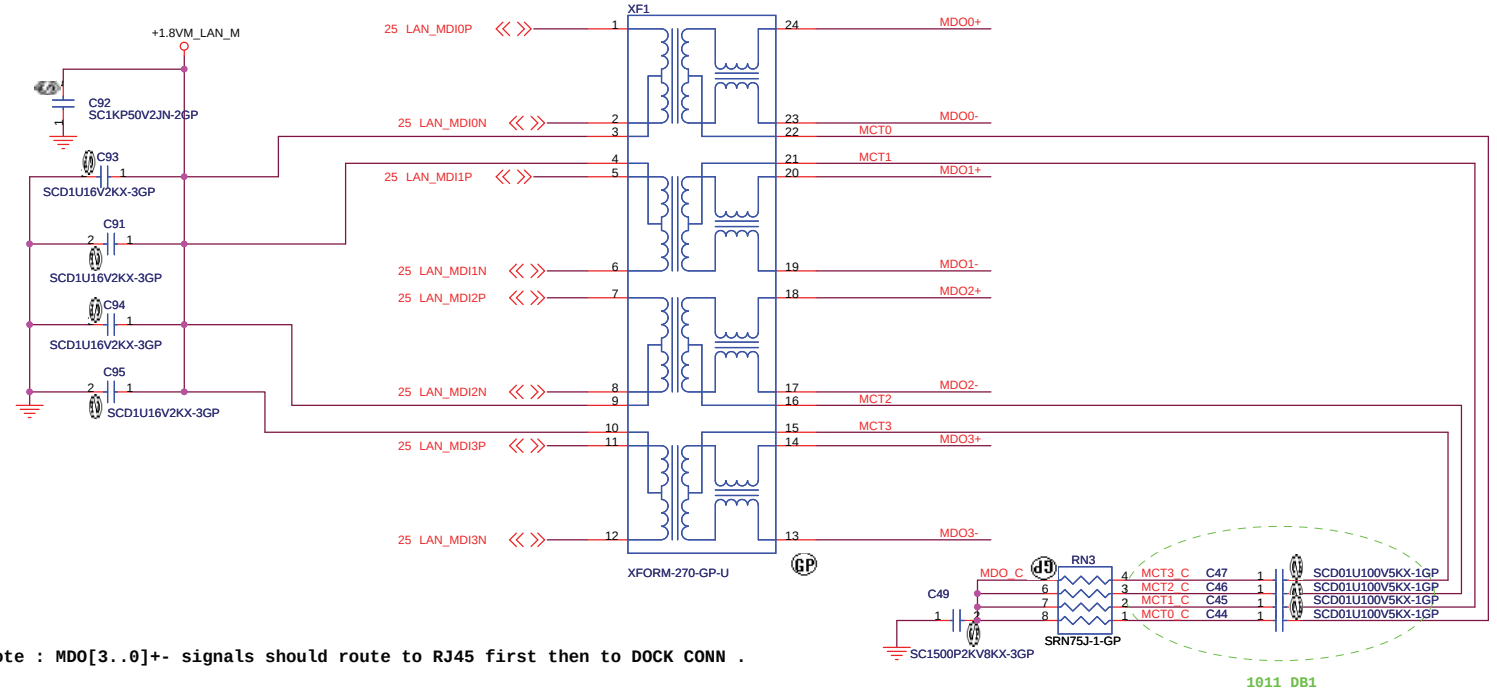
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD /NEW CARD CONN.

Size	Document Number	Rev
A3	NORN 2.0	-1

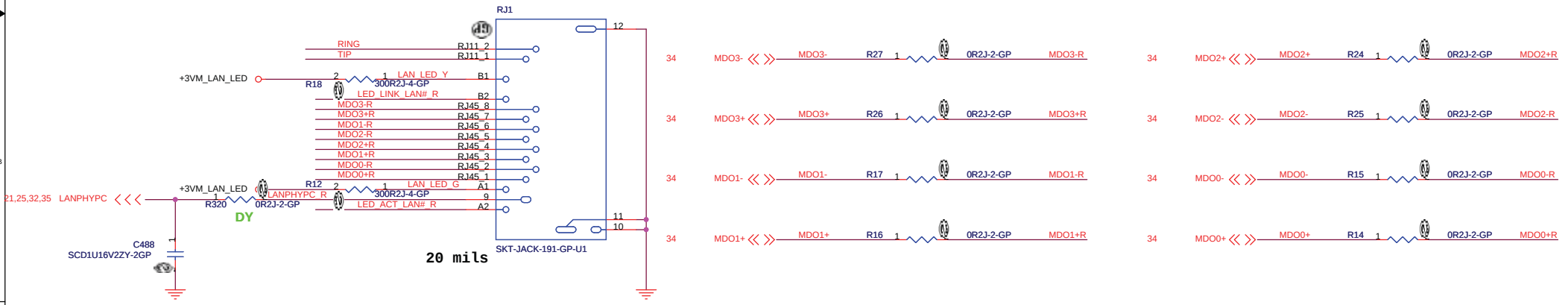
Date: Wednesday, July 16, 2008 Sheet 24 of 52

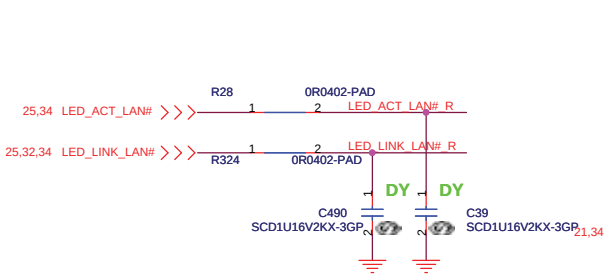

20 mils
20 mils
40 mils
0709 MV Change R848
from 47K to 470 ohm.
0801 Reserve R57 If RF requet
Will replace bead
P/N:68.00084.341
0314 SI2
Add +3VM_LAN discharge circuit.
1011 DB1
0304 SI1b RF
Layout Note
Keep this R52 on top side
and route differentially
0123 SI1 Change back to 12pF.
0513 PV Change C144 and C123 to 15pF.
1017 DB1
1012 DB1
JTAG
WG82567LM-Q036-GP
GLCI
LCI
MDI
2N7002E-1-GP
2SB772PT-1-GP
74LVC1G08GW-1-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Intel 82567 Bavoz
NORN 2.0
Size A3
Rev -1
Date: Wednesday, July 16, 2008
Sheet 25 of 52

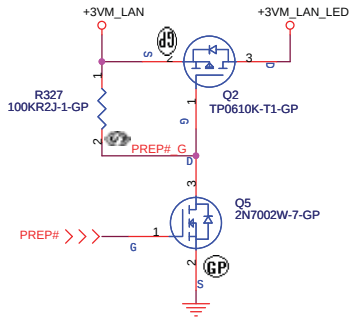


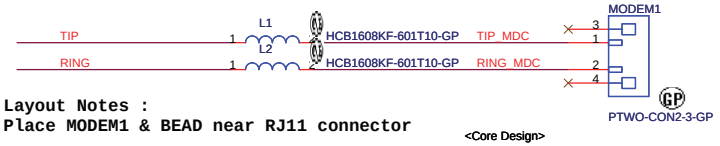
Note : MDO[3..0]+- signals should route to RJ45 first then to DOCK CONN .

1011 DB1









Layout Notes :
Place MODEM1 & BEAD near RJ11 connector

3.2 mm keep out on all layers from TIP/RING to all other traces, vias and pads

<Core Design>

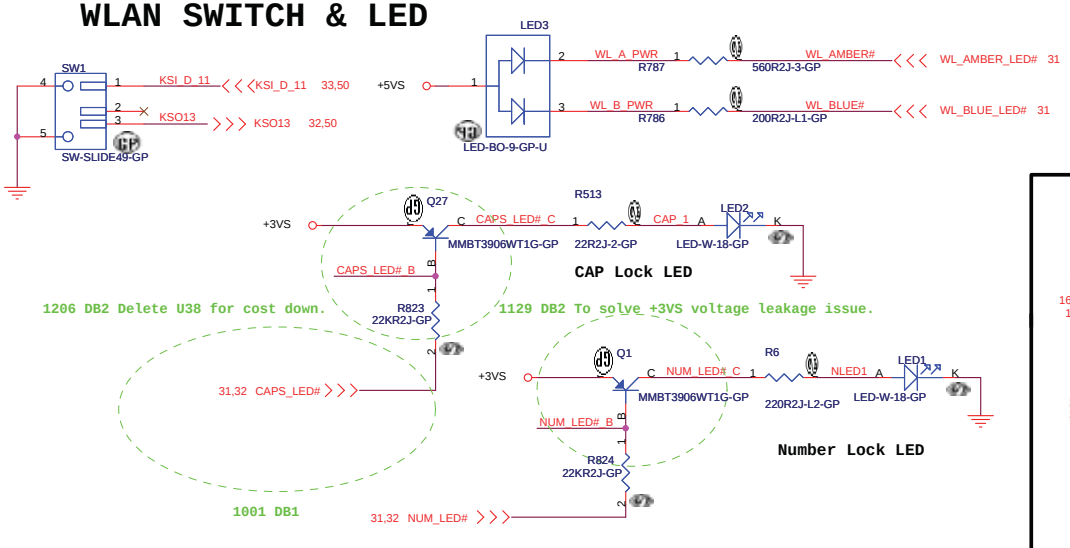
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Magnetic & RJ45/RJ11***

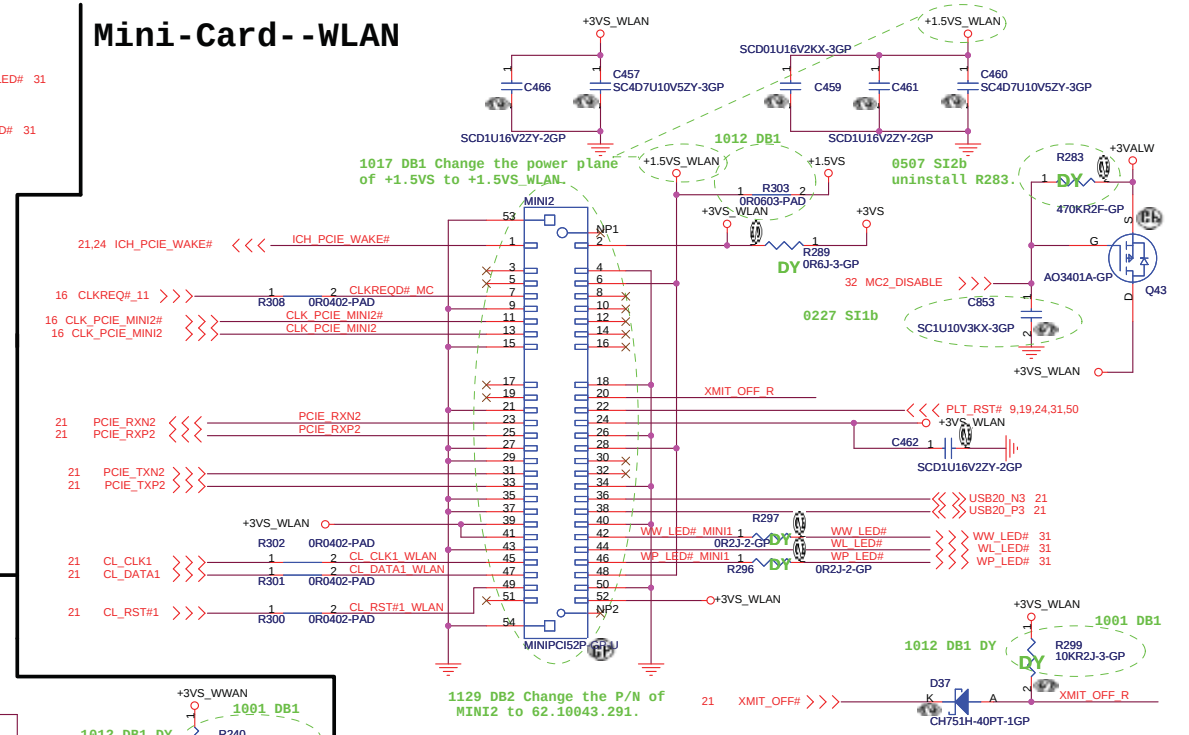
Size	Document Number	Rev
A3	NORN 2.0	-1

Date: Wednesday, July 16, 2008 Sheet 26 of 52

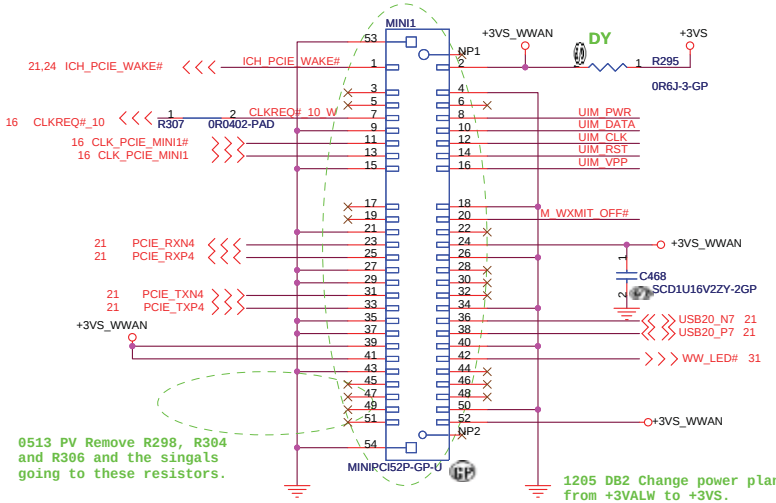
WLAN SWITCH & LED

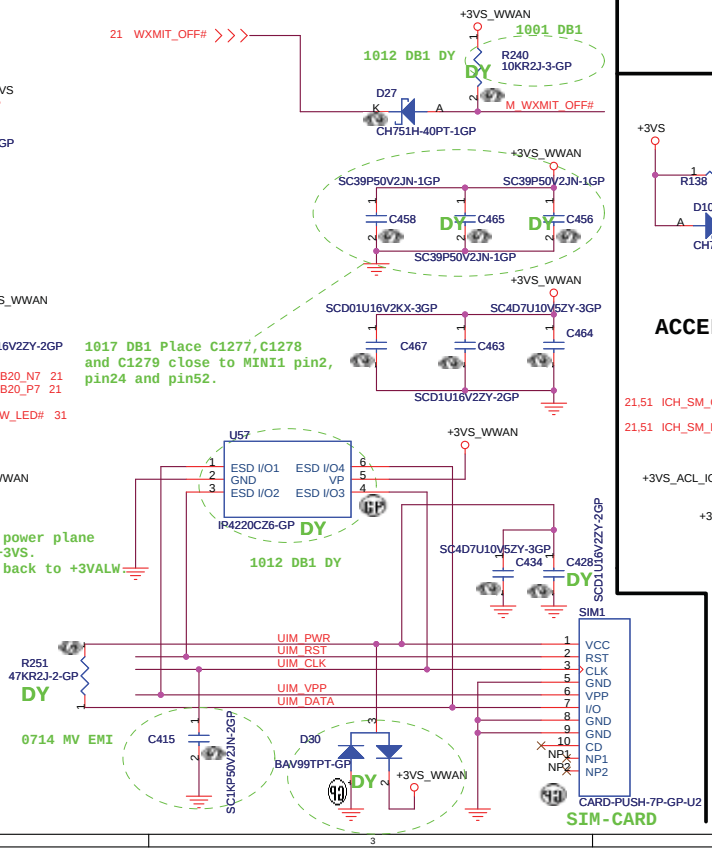


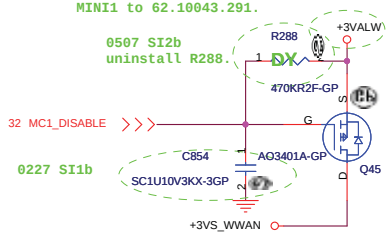
Mini-Card--WLAN

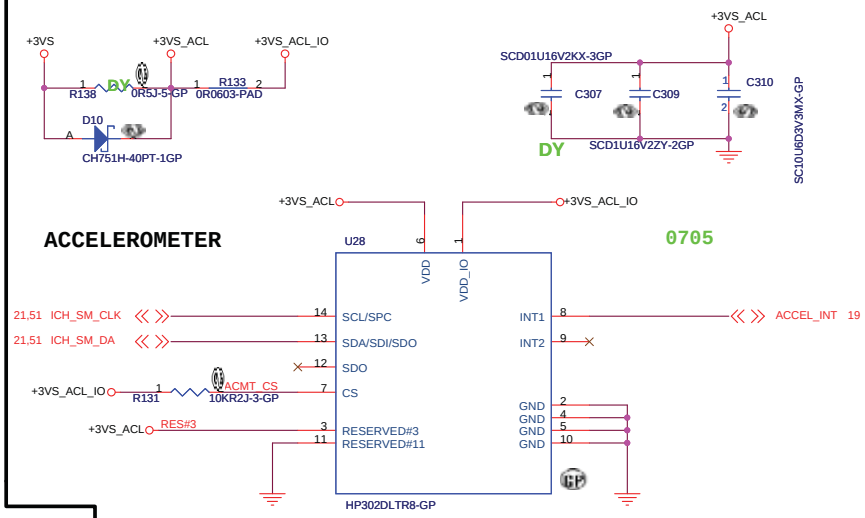


Mini-Card--WWAN









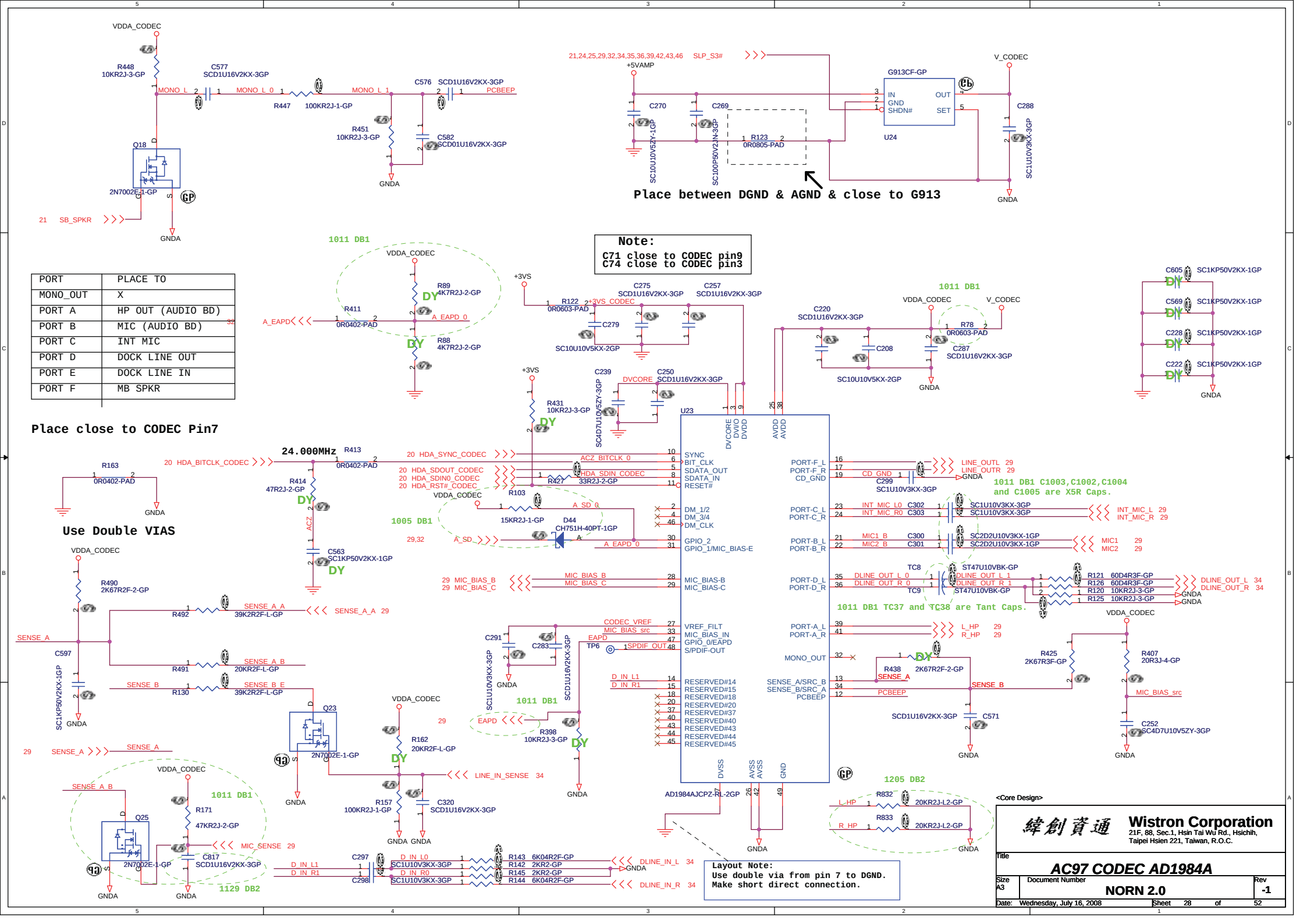
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

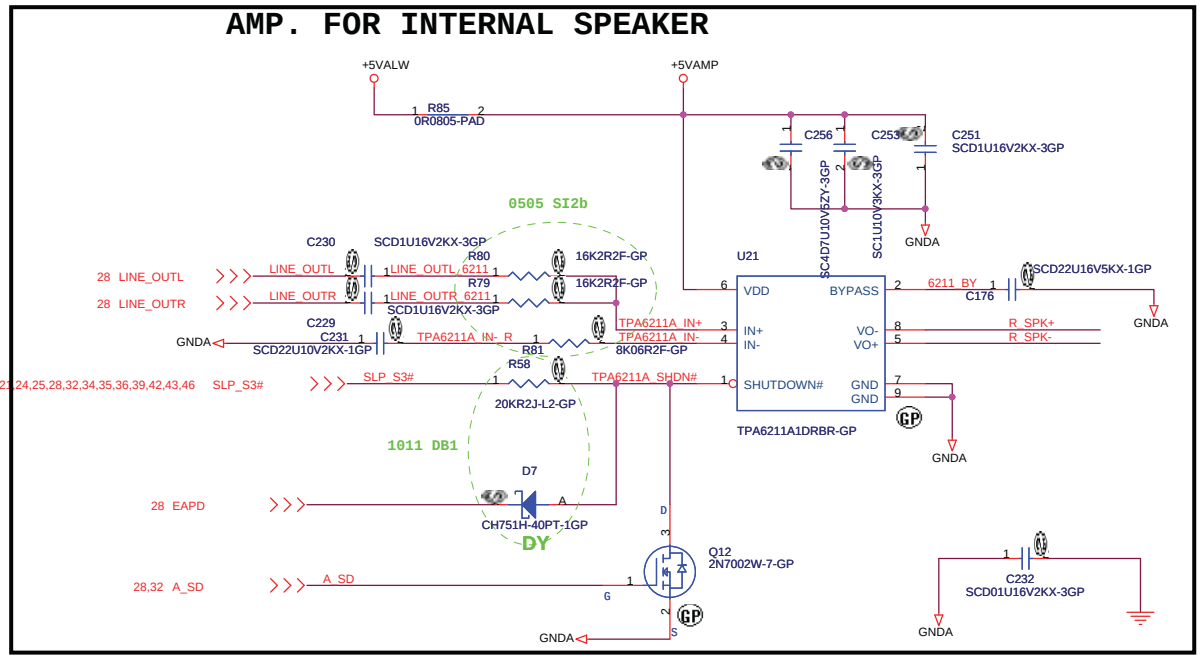
Title: Mini-Card/Accelerometer

Size: Custom | Document Number: NORN 2.0 | Rev: -1

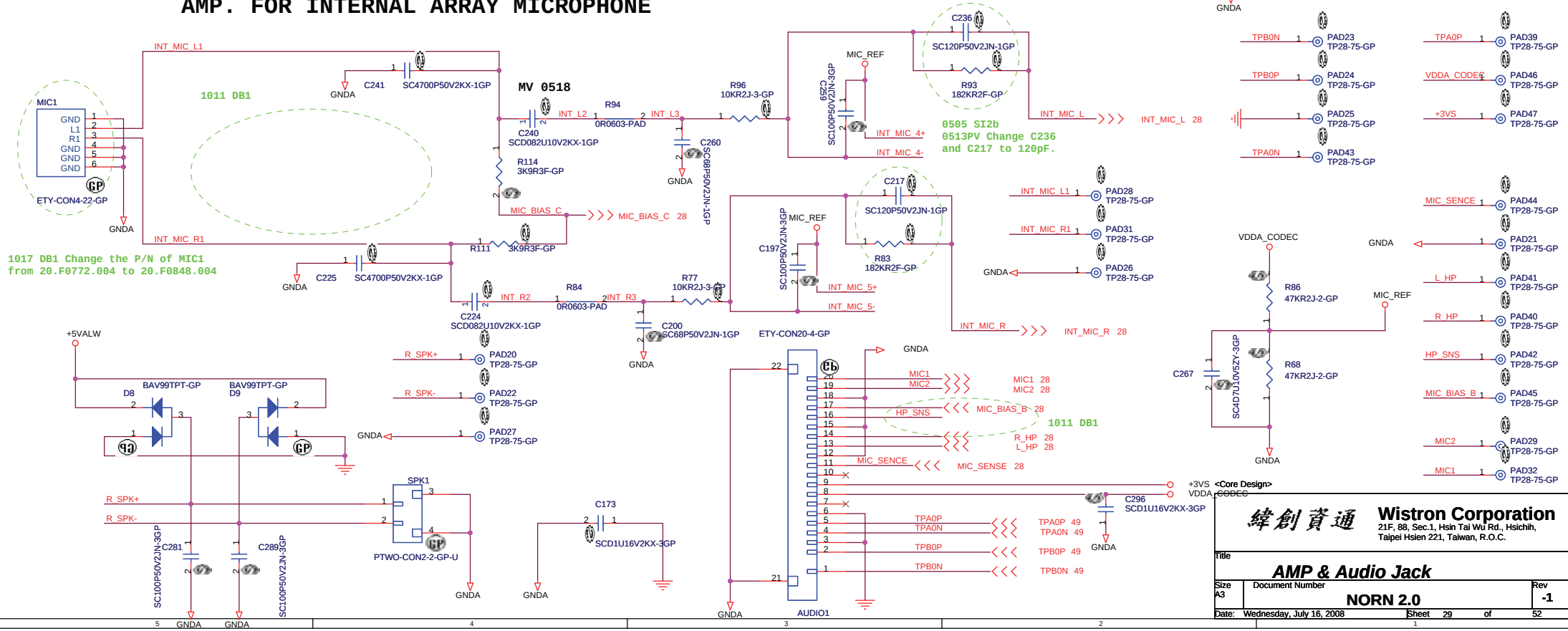
Date: Wednesday, July 16, 2008 | Sheet 27 of 52


VDDA_CODEC
R448 10KR2J-3-GP
C577 SCD1U16V2KX-3GP
MONO_L
MONO_L_0
R447 100KR2J-1-GP
MONO_L_1
C576 SCD1U16V2KX-3GP
PCBEEP
R451 10KR2J-3-GP
C582 SCD01U16V2KX-3GP
GNDA
Q18
2N7002E-1-GP
21 SB_SPKR
21,24,25,29,32,34,35,36,39,42,43,46 SLP_S3#
+5VAMP
C270
C269
SC10U10V5ZY-1GP
SC100P50V2JN-3GP
R123 0R0805-PAD
G913CF-GP
IN
GND
SHDN#
OUT
SET
U24
V_CODEC
C288
SC1U10V3KX-3GP
Place between DGND & AGND & close to G913
1011 DB1
R89 4K7R2J-2-GP
R411 0R0402-PAD
A_EAPD
A_EAPD_0
R88 4K7R2J-2-GP
DY
32
Note:
C71 close to CODEC pin9
C74 close to CODEC pin3
+3VS
R122 0R0603-PAD
+3VS_CODEC
C275 SCD1U16V2KX-3GP
C257 SCD1U16V2KX-3GP
C279
SC10U10V5KX-2GP
C220 SCD1U16V2KX-3GP
C208
R78 0R0603-PAD
C287 SCD1U16V2KX-3GP
C605 SC1KP50V2KX-1GP
C569 SC1KP50V2KX-1GP
C228 SC1KP50V2KX-1GP
C222 SC1KP50V2KX-1GP
PORT | PLACE TO
MONO_OUT | X
PORT A | HP OUT (AUDIO BD)
PORT B | MIC (AUDIO BD)
PORT C | INT MIC
PORT D | DOCK LINE OUT
PORT E | DOCK LINE IN
PORT F | MB SPKR
Place close to CODEC Pin7
24.000MHz
R413 0R0402-PAD
R163 0R0402-PAD
R414 47R2J-2-GP
ACZ
C563 SC1KP50V2KX-1GP
20 HDA_BITCLK_CODEC
20 HDA_SYNC_CODEC
20 HDA_SDOUT_CODEC
20 HDA_SDIN0_CODEC
20 HDA_RST#_CODEC
ACZ_BITCLK_0
HDA_SDIN_CODEC
R427 33R2J-2-GP
R103
A_SD_0
15KR2J-1-GP
1005 DB1
D44 CH751H-40PT-1GP
29,32 A_SD
A_EAPD_0
R431 10KR2J-3-GP
C239 SC4D7U10V5ZY-3GP
DVCORE
C250 SCD1U16V2KX-3GP
U23
DVCORE DVI/O DVDD
AVDD AVDD
SYNC
BIT_CLK
SDATA_OUT
SDATA_IN
RESET#
DM_1/2
DM_3/4
DM_CLK
GPIO_2
GPIO_1/MIC_BIAS-E
MIC_BIAS_B
MIC_BIAS_C
29 MIC_BIAS_B
29 MIC_BIAS_C
PORT-F_L
PORT-F_R
CD_GND
LINE_OUTL 29
LINE_OUTR 29
C299 SC1U10V3KX-3GP
1011 DB1 C1003,C1002,C1004
and C1005 are X5R Caps.
PORT-C_L
PORT-C_R
INT_MIC_L0 C302
INT_MIC_R0 C303
SC1U10V3KX-3GP
INT_MIC_L 29
INT_MIC_R 29
PORT-B_L
PORT-B_R
MIC1_B C300
MIC2_B C301
SC2D2U10V3KX-1GP
MIC1 29
MIC2 29
TC8 ST47U10VBK-GP
TC9 ST47U10VBK-GP
PORT-D_L
PORT-D_R
DLINE_OUT_L_0
DLINE_OUT_R_0
DLINE_OUT_L_1
DLINE_OUT_R_1
R121 60D4R3F-GP
R126 60D4R3F-GP
R120 10KR2J-3-GP
R125 10KR2J-3-GP
DLINE_OUT_L 34
DLINE_OUT_R 34
1011 DB1 TC37 and TC38 are Tant Caps.
PORT-A_L
PORT-A_R
L_HP 29
R_HP 29
MONO_OUT
R438 2K67R2F-P-GP
SENSE_A
SENSE_B
PCBEEP
SENSE_A/SRC_B
SENSE_B/SRC_A
R425 2K67R3F-GP
R407 20R3J-4-GP
MIC_BIAS_src
C252 SC4D7U10V5ZY-3GP
SCD1U16V2KX-3GP
C571
CODEC_VREF
MIC_BIAS_src
EAPD
TP6
SPDIF_OUT
VREF_FILT
MIC_BIAS_IN
GPIO_0/EAPD
S/PDIF-OUT
C291
C283
SC1U10V3KX-3GP
SCD1U16V2KX-3GP
D_IN_L1
D_IN_R1
RESERVED#14
RESERVED#15
RESERVED#18
RESERVED#20
RESERVED#37
RESERVED#40
RESERVED#43
RESERVED#44
RESERVED#45
1011 DB1
EAPD
R398 10KR2J-3-GP
DVSS
AVSS
AVSS
GND
AD1984AJCPZ-RL-2GP
1205 DB2
R832 20KR2J-L2-GP
R833 20KR2J-L2-GP
L_HP
R_HP
<Core Design>
Use Double VIAS
SC1KP50V2KX-1GP
R490 2K67R2F-2-GP
SENSE_A
C597
R492 39K2R2F-L-GP
SENSE_A_A
SENSE_A_A 29
R491 20KR2F-L-GP
SENSE_A_B
R130 39K2R2F-L-GP
SENSE_B_E
Q23
2N7002E-1-GP
29 SENSE_A
SENSE_A
R162 20KR2F-L-GP
29
LINE_IN_SENSE 34
R157 100KR2J-1-GP
C320 SCD1U16V2KX-3GP
SENSE_A_B
Q25
2N7002E-1-GP
1011 DB1
R171 47KR2J-2-GP
MIC_SENSE 29
C817 SCD1U16V2KX-3GP
1129 DB2
C297
C298
D_IN_L0
D_IN_R0
SC1U10V3KX-3GP
R143 6K04R2F-GP
R142 2KR2-GP
R145 2KR2-GP
R144 6K04R2F-GP
DLINE_IN_L 34
DLINE_IN_R 34
Layout Note:
Use double via from pin 7 to DGND.
Make short direct connection.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AC97 CODEC AD1984A
Size A3
Document Number
NORN 2.0
Rev -1
Date: Wednesday, July 16, 2008
Sheet 28 of 52

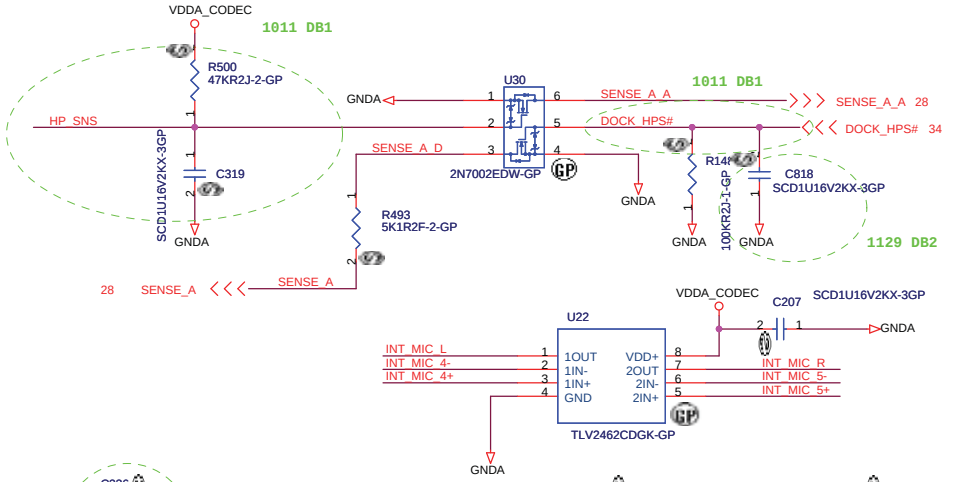
AMP. FOR INTERNAL SPEAKER



AMP. FOR INTERNAL ARRAY MICROPHONE



1011 DB1

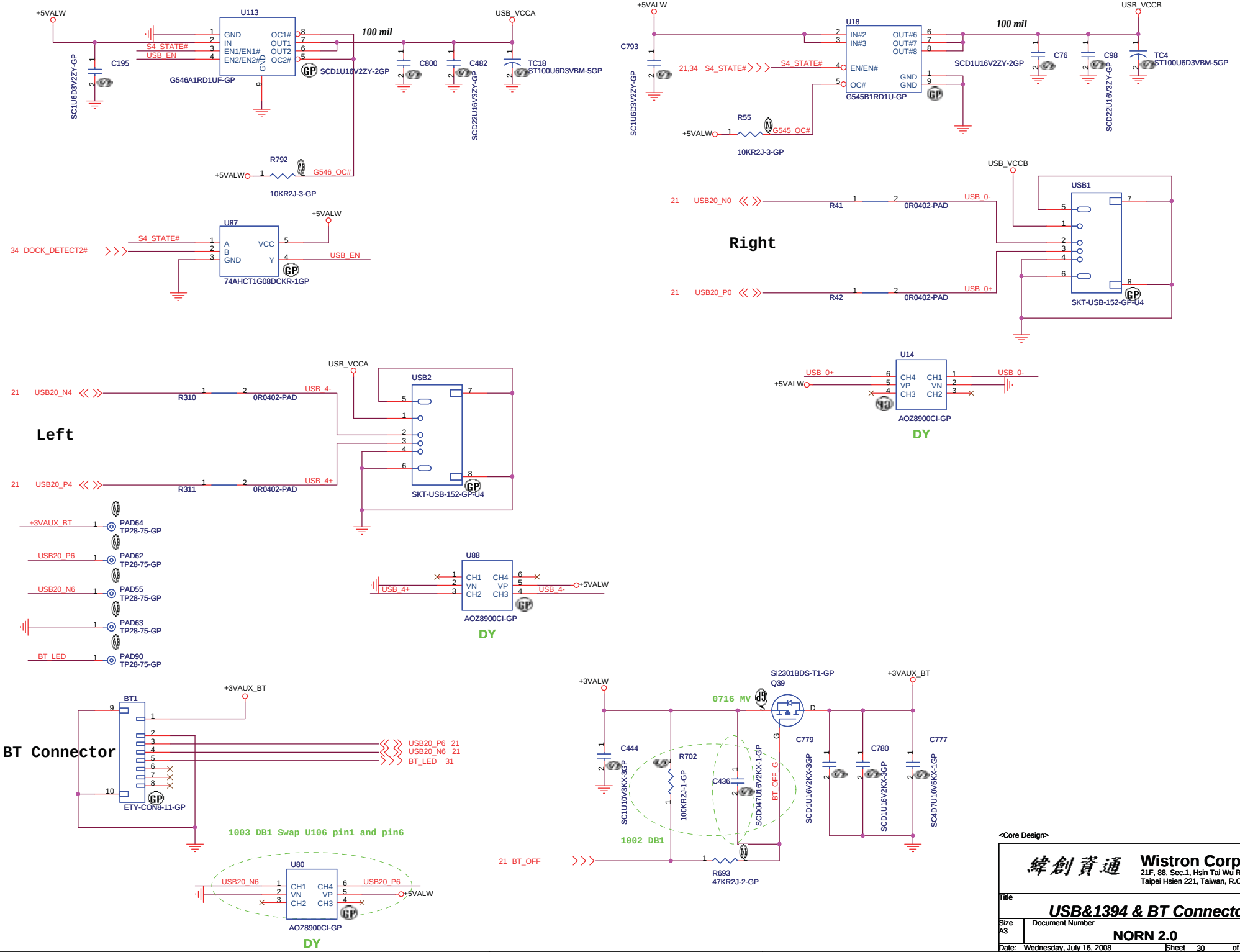


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AMP & Audio Jack**

Size	Document Number	Rev
A3	NORN 2.0	-1

Date: Wednesday, July 16, 2008 Sheet 29 of 52


+5VALW
U113
GND
IN
EN1/EN1#
EN2/EN2#
OC1#
OUT1
OUT2
OC2#
S4_STATE#
USB_EN
G546A1RD1UF-GP
100 mil
SCD1U16V2ZY-2GP
USB_VCCA
C195
C800
C482
TC18
ST100U6D3VBM-5GP
SC1U6D3V2ZY-GP
SCD22U16V3ZY-GP
R792
10KR2J-3-GP
G546_OC#
U87
74AHCT1G08DCKR-1GP
34 DOCK_DETECT2#
U18
IN#2
IN#3
EN/EN#
OC#
OUT#6
OUT#7
OUT#8
GND
G545B1RD1U-GP
21,34 S4_STATE#
C793
C76
C98
R55
G545_OC#
Right
USB_VCCB
USB1
SKT-USB-152-GP-U4
21 USB20_N0
21 USB20_P0
R41
R42
0R0402-PAD
USB_0-
USB_0+
U14
CH4
CH1
VP
VN
CH3
CH2
AOZ8900CI-GP
DY
Left
21 USB20_N4
21 USB20_P4
R310
R311
USB_4-
USB_4+
USB2
PAD64
PAD62
PAD55
PAD63
PAD90
TP28-75-GP
+3VAUX_BT
USB20_P6
USB20_N6
BT_LED
U88
BT Connector
BT1
ETY-CON8-11-GP
USB20_P6 21
USB20_N6 21
BT_LED 31
1003 DB1 Swap U106 pin1 and pin6
U80
1002 DB1
SI2301BDS-T1-GP
Q39
0716 MV
C444
R702
C436
C779
C780
C777
SC1U10V3KX-3GP
100KR2J-1-GP
SCD047U16V2KX-1-GP
SCD1U16V2KX-3GP
SC4D7U10V5KX-1GP
BT_OFF_G
21 BT_OFF
R693
47KR2J-2-GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
USB&1394 & BT Connector
Size
A3
Document Number
NORN 2.0
Rev
-1
Date: Wednesday, July 16, 2008
Sheet 30 of 52

32Mb x 1

0120 SI1 Change R249 from 56R to 15R.

0120 SI1 Remove R250, R248, R273 and R274.

0128 SI1 Change R266 and R267 from 15Rto 47R.

62.10089.001 is SPI Socket part number

32M SPI
> 72.25325.A01 MX25L3205DM2I-12G, by MXIC
32M SPI
> 72.26321.A01 IC FEROM AT26DF321-SU, by Atmel

Debug port

1001 DB1

0128 SI1

0128 SI1

1. Keep traces of SPI as short as possible and keep trace spacing close to 7mils to any other signal (basically follow specs).

2. AMT designs need 2x2MB SPI parts in addition to connecting to a debug connector. Keep stuffing options from 2nd SPI part to debug connector very close to 2nd part so stub effect can be eliminated during testing as needed.

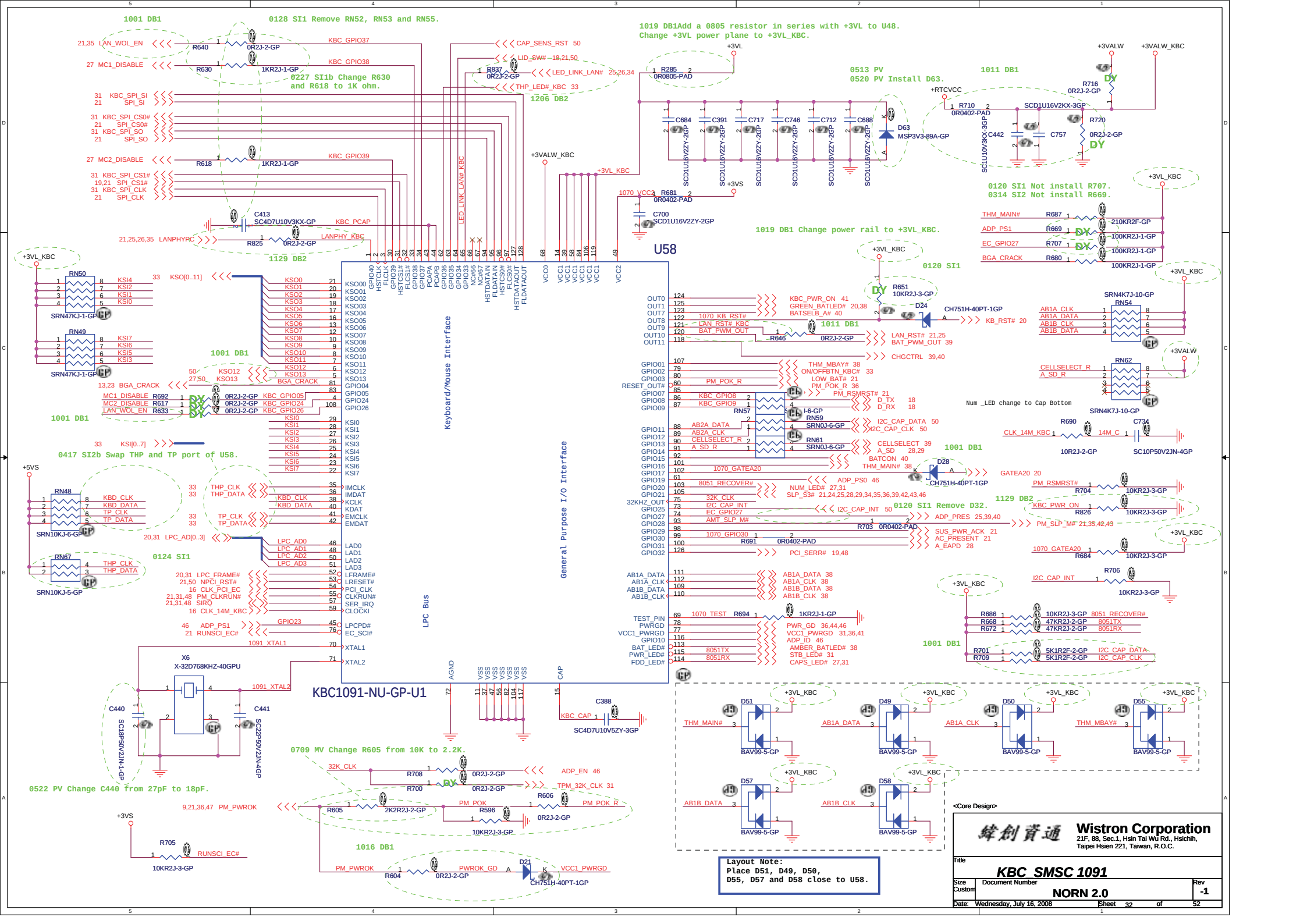
TPM 1.2

0522 PV Change C412 from 22pF to 18pF and C420 from 18pF to 15pF.

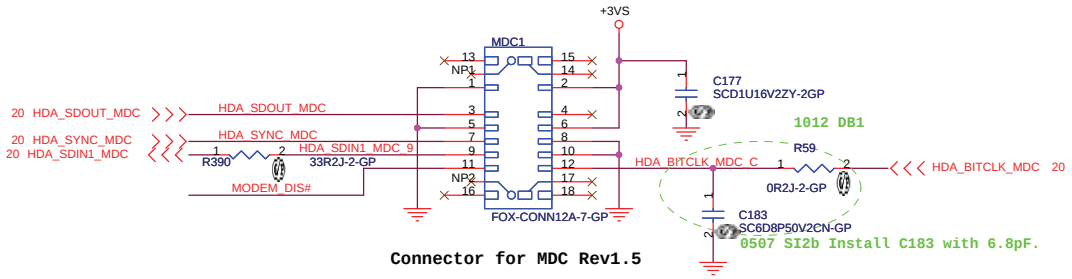
Mini-PCIE Card LED control circuit

<Core Design>

Wistron Corporation 緯創資通	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: TPM/BIOS/24 DEBUG PORT		
Size: A3	Document Number: NORN 2.0	Rev: -1
Date: Wednesday, July 16, 2008	Sheet 31 of 52	

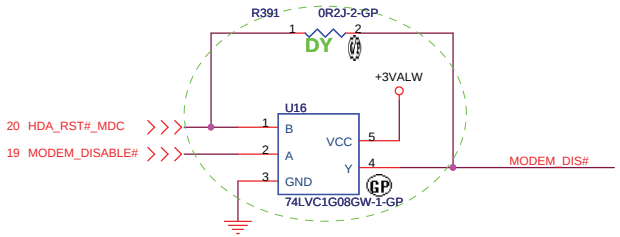

1001 DB1
0128 SI1 Remove RN52, RN53 and RN55.
1019 DB1Add a 0805 resistor in series with +3VL to U48.
Change +3VL power plane to +3VL_KBC.
0227 SI1b Change R630 and R618 to 1K ohm.
1206 DB2
0513 PV
0520 PV Install D63.
1011 DB1
0120 SI1 Not install R707.
0314 SI2 Not install R669.
1019 DB1 Change power rail to +3VL_KBC.
1129 DB2
0120 SI1
0417 SI2b Swap THP and TP port of U58.
0124 SI1
0120 SI1 Remove D32.
0709 MV Change R605 from 10K to 2.2K.
0522 PV Change C440 from 27pF to 18pF.
1016 DB1
U58
KBC1091-NU-GP-U1
Keyboard/Mouse Interface
General Purpose I/O Interface
LPC Bus
Num _LED change to Cap Bottom
Layout Note:
Place D51, D49, D50,
D55, D57 and D58 close to U58.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_SMSC 1091
NORN 2.0
Wednesday, July 16, 2008
Sheet 32 of 52

MDC 1.5 Conn.

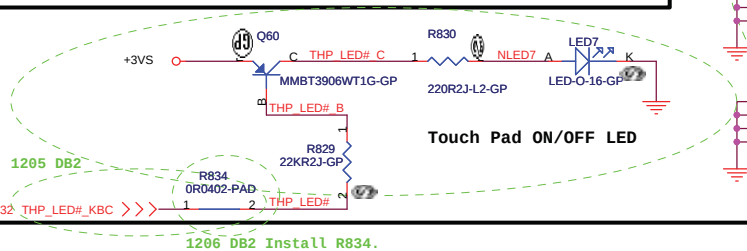


Connector for MDC Rev1.5

1129 DB2



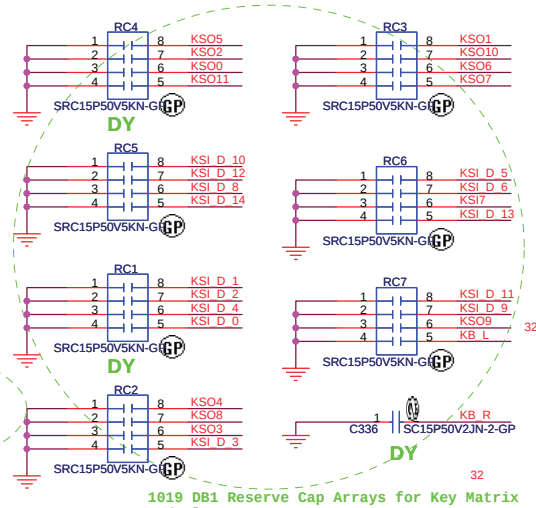
1203 DB2 Add Touch Pad ON/OFF LED circuit.



Touch Pad ON/OFF LED

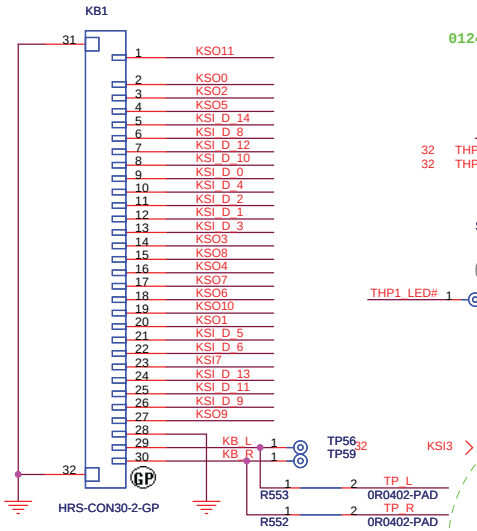
1205 DB2

1206 DB2 Install R834.



1019 DB1 Reserve Cap Arrays for Key Matrix and place near to KB1.

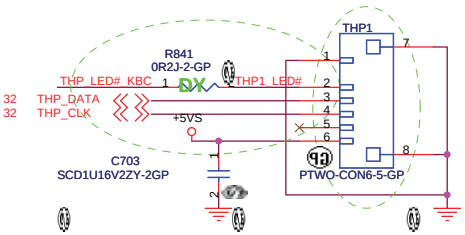
INT_KBD CONN.

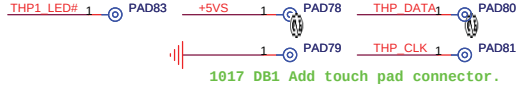


Touch_Pad CONN.

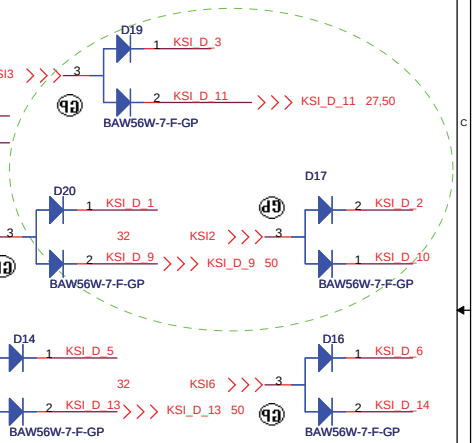
1203 DB2 Change THP1 from 8pin to 6pin.
0227 SI1b Reverse the pin define of THP1.

0124 SI1

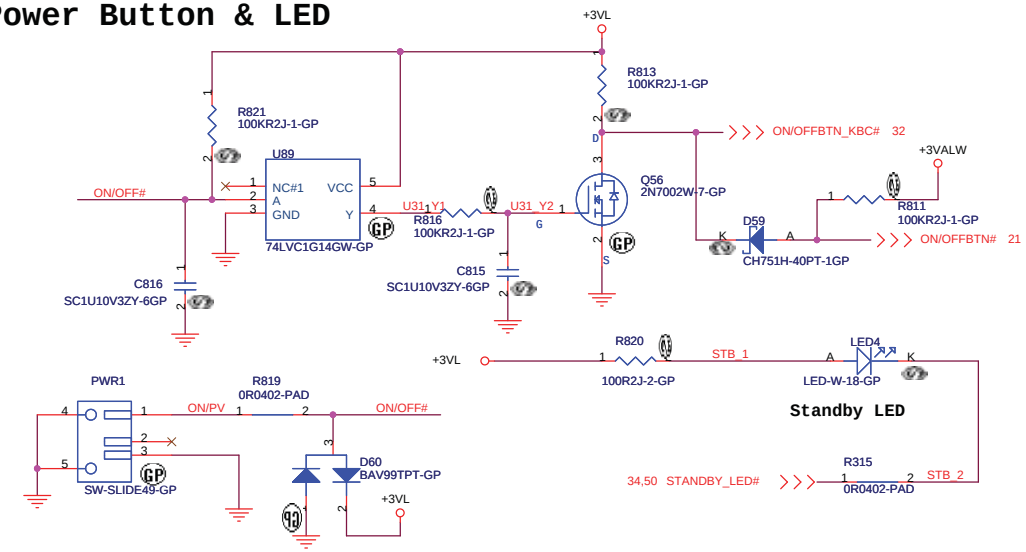




1017 DB1 Add touch pad connector.

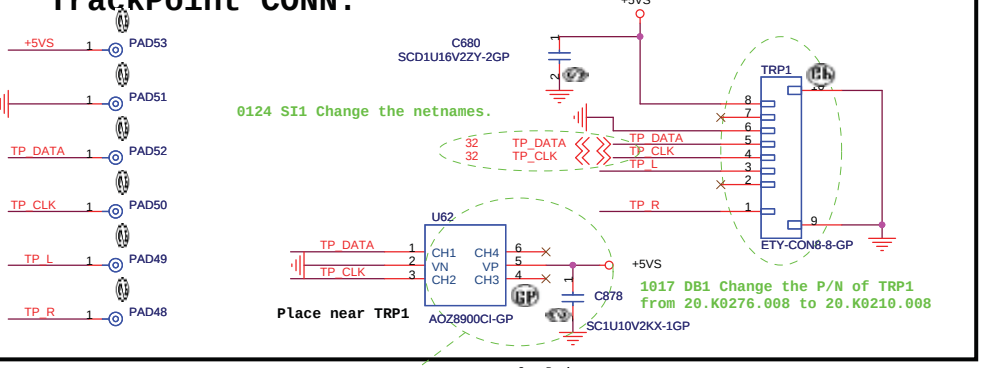


Power Button & LED



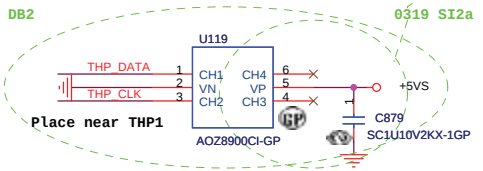
Standby LED

TrackPoint CONN.



1130 DB2

0319 SI2a



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MDC/KBD/ON OFF/T.P.

Size: A3 | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 33 of 52

current rating 6A

L11 BLM21PG220SN1DGP

VIN — DOCKVIN

C503 SC1KP50V2KX-1GP

C504 SC1KP50V2KX-1GP

1002 DB1

C37 DY SC1KP50V2KX-1GP

C38 DY SC1KP50V2KX-1GP

GNDA

1001 DB1 Add RC for EMI resuest.

28 DLINE_OUT_R — DLINE_OUT_R — R39 0R3-0-U-GP — DLINE_OUT_R_D

28 DLINE_OUT_L — DLINE_OUT_L — R38 0R3-0-U-GP — DLINE_OUT_L_D

28 DLINE_IN_R — DLINE_IN_R — R37 0R3-0-U-GP — DLINE_IN_R_D

28 DLINE_IN_L — DLINE_IN_L — R36 0R3-0-U-GP — DLINE_IN_L_D

C43 DY SC5P50V2CN-2GP

C42 DY SC5P50V2CN-2GP

C41 DY SC5P50V2CN-2GP

C40 DY SC5P50V2CN-2GP

GNDA

MAX4596

IN	NO TO COM COM TO NO
L	OFF
H	ON

CLOSE DOCKING CONN.

+5VS

R34 10KR2J-3-GP

U8 MAX4596DCKR-GP

30 DOCK_DETECT2# — DOCK_DETECT2# — 9 RED — L_RED 17

U9 MAX4596DCKR-GP

DOCK_DETECT2# — 9 GREEN — L_GREEN 17

U7 MAX4596DCKR-GP

DOCK_DETECT2# — 9 BLUE — L_BLUE 17

DOCK CONN. 100 PIN

DOCK1

DOCKVIN — DOCKVIN

DOCK_DETECT2#

GNDA

DLINE_OUT_R_D

DLINE_OUT_L_D

DLINE_IN_R_D

DLINE_IN_L_D

28 LINE_IN_SENSE — LINE_IN_SENSE

29 DOCK_HPS# — DOCK_HPS#

LIMIT_SIGNAL

0513 PV Change the power source of +3VM_LAN_LED to +3VM_LAN.

+3VM_LAN

26 MDO3- — MDO3-

26 MDO3+ — MDO3+

26 MDO1- — MDO1-

26 MDO1+ — MDO1+

26 MDO2- — MDO2-

26 MDO2+ — MDO2+

26 MDO0+ — MDO0+

26 MDO0- — MDO0-

1015 DB1 Remove TV-OUT connection.

D_VSYNC 17

D_HSYNC 17

GREEN_C

RED_C

BLUE_C

B+

C508 SC1KP50V2KX-1GP

NP1

NP2

JAE-CONN100-1-GP-U4

USB20_N11 — USB20_N11 21

USB20_P11 — USB20_P11 21

USB20_N9 — USB20_N9 21

USB20_P9 — USB20_P9 21

STANDBY_LED# — STANDBY_LED# 33,50

DK(ODD)

DK(HUB)

SLP_S3# — SLP_S3# 21,24,25,28,29,32,35,36,39,42,43,46

LED_ACT_LAN#_DOCK

LED_LINK_LAN#_DOCK

D_DDCDATA — D_DDCDATA 17

D_DDCCLK — D_DDCCLK 17

S4_STATE# — S4_STATE# 21,30

DOCK_DETECT1# — R7 0R0402-PAD

Power Pins

2 sets

Set 1 = 18.5V @ 4A per contact

Set 2 = VBATR @ 3A per contact

0514 PV Change R344, R345 and R346 from 0 ohm to 22 ohm@100MHz beads.

GREEN — R346 BLM18BB220SN-GP — GREEN_C

RED — R345 BLM18BB220SN-GP — RED_C

BLUE — R344 BLM18BB220SN-GP — BLUE_C

C507 DY SC5P50V2CN-2GP

C505 DY SC5P50V2CN-2GP

C506 DY SC5P50V2CN-2GP

U4 AOZ8900CI-GP

USB20_N9 — CH1 — CH4 — USB20_N11

USB20_P9 — VN — VP — USB20_P11

CH2 — CH3 — +5VALW

DY

1018 DB1

+5VS

R40 10KR2J-3-GP

U12 2N7002EDW-GP

DOCK_DETECT2# — PREP# DOCK

21,26 PREP# — PREP#

+3VM_LAN

R21 10KR2J-3-GP

LAN_LINK_EN

U3 2N7002EDW-GP

25,26 LED_ACT_LAN# — LED_ACT_LAN#_DOCK

LED_LINK_LAN#_DOCK — LED_LINK_LAN# — LED_LINK_LAN# 25,26,32

0227 SI1b Swap the connections of U3-1 and U3-6.

<Core Design>

緯創資通 Wistron Corporation

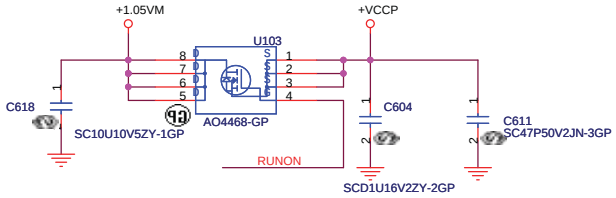
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Docking CONN

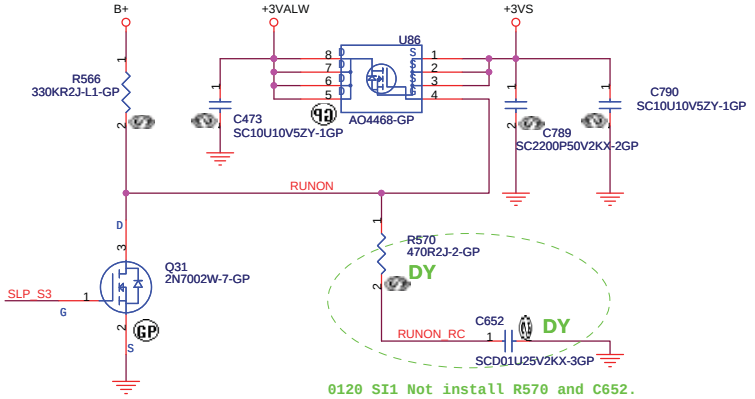
Size: A3 | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 34 of 52

+1.05VM to +VCCP Transfer

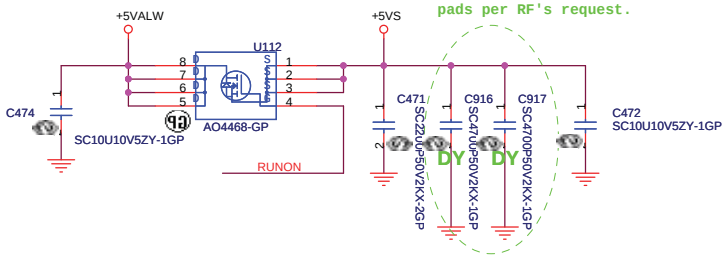


+3VALW to +3VS Transfer



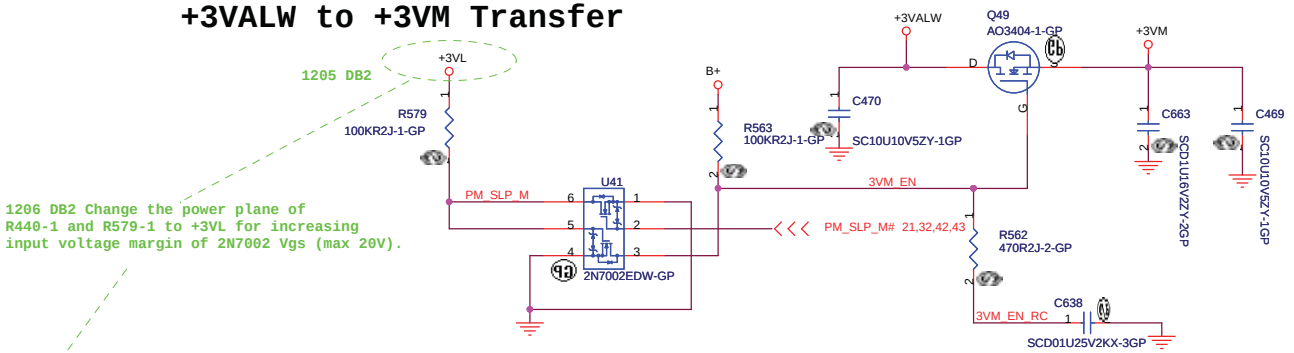
0120 SI1 Not install R570 and C652.

+5VALW to +5VS Transfer



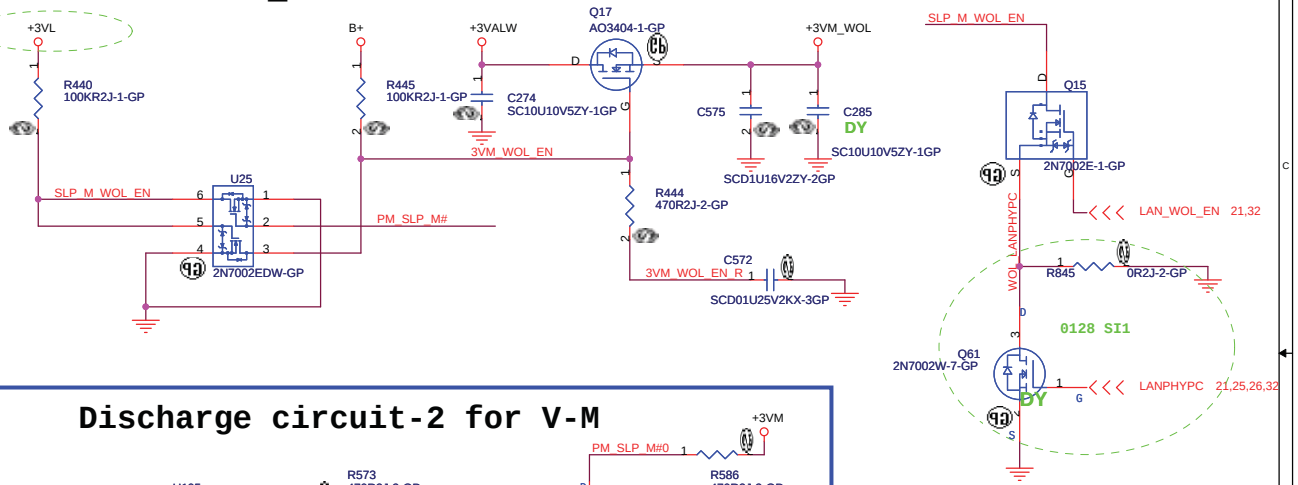
0421 SI2b Reserve two cap pads per RF's request.

+3VALW to +3VM Transfer

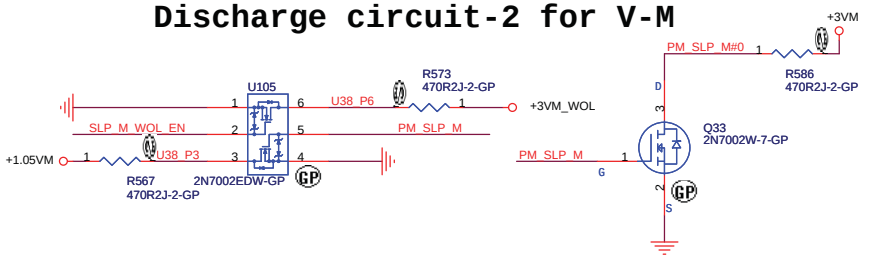


1206 DB2 Change the power plane of R440-1 and R579-1 to +3VL for increasing input voltage margin of 2N7002 Vgs (max 20V).

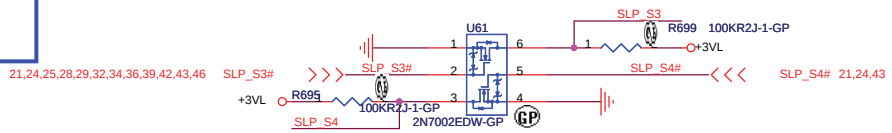
+3VALW to +3VM_WOL

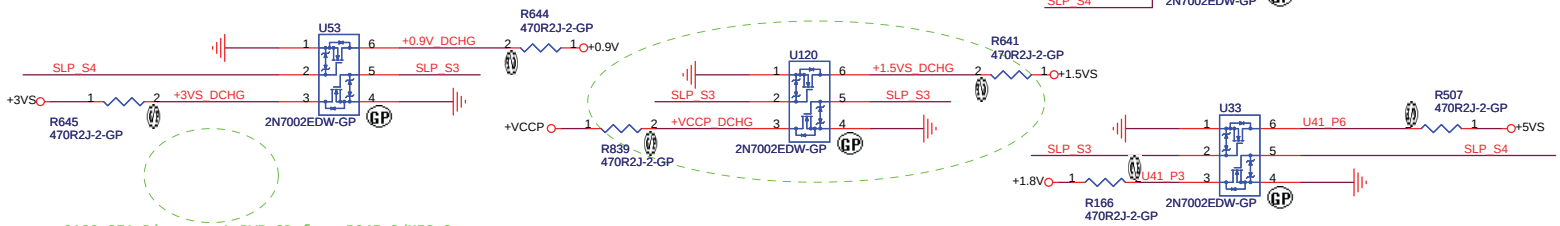


Discharge circuit-2 for V-M



Discharge circuit-1





0120 SI1 Disconnect PWR_GD from R645-2/U53-3.

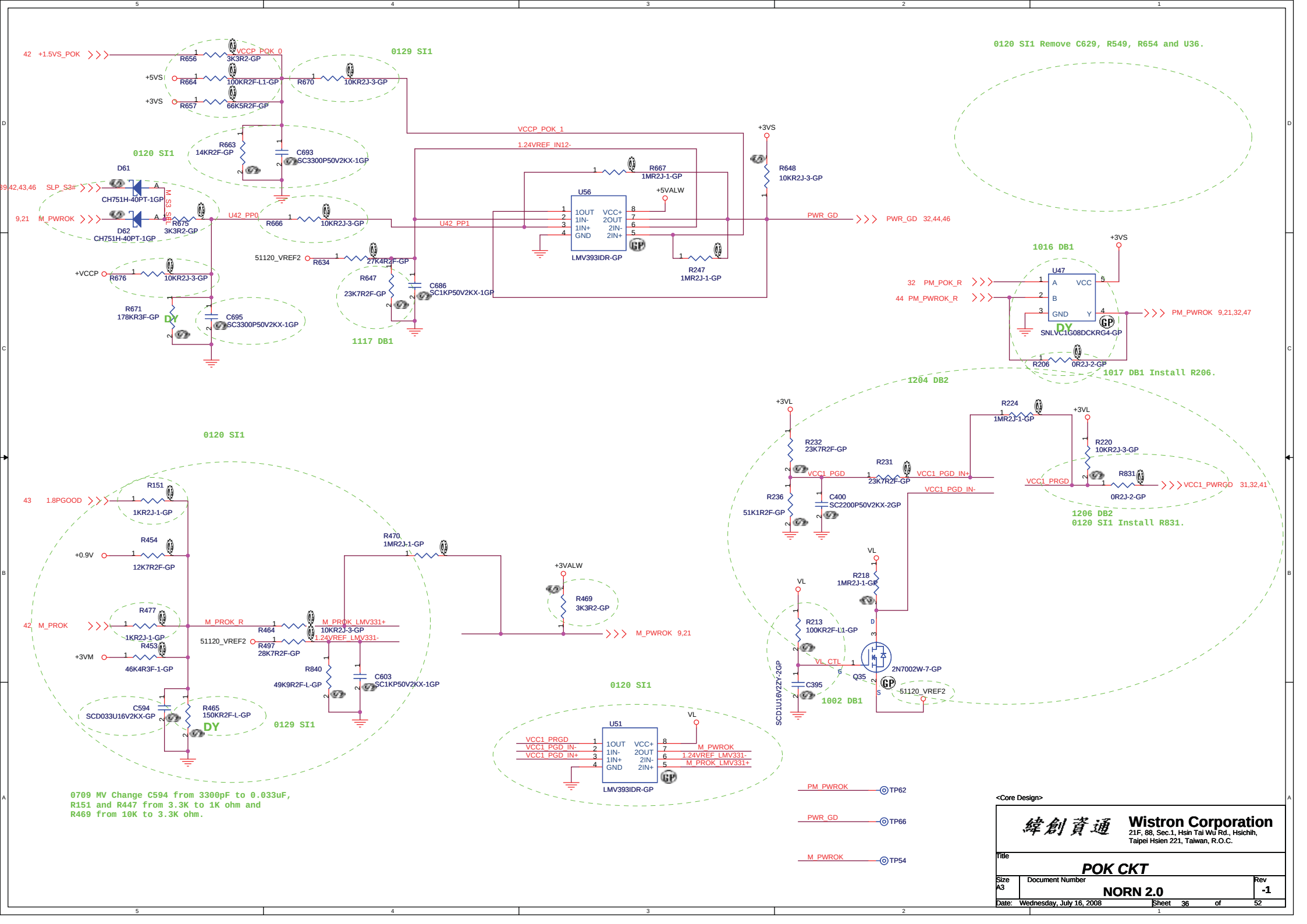
<Core Design>

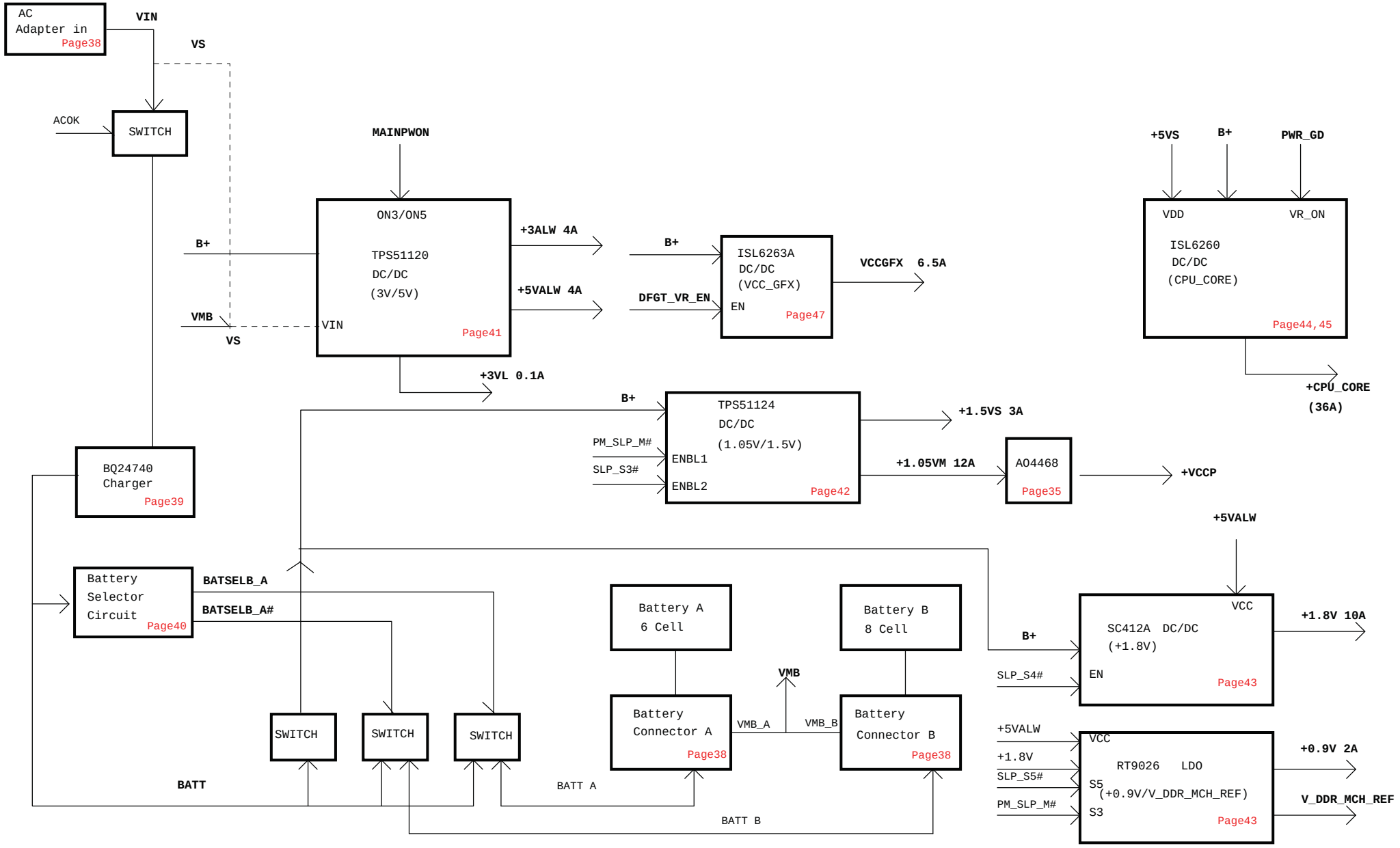
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC Circuit

Size: A3 | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 35 of 52


0120 SI1 Remove C629, R549, R654 and U36.
0129 SI1
0120 SI1
1016 DB1
1017 DB1 Install R206.
1204 DB2
1206 DB2
0120 SI1 Install R831.
0120 SI1
1117 DB1
1002 DB1
0129 SI1
0120 SI1
0709 MV Change C594 from 3300pF to 0.033uF,
R151 and R447 from 3.3K to 1K ohm and
R469 from 10K to 3.3K ohm.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
POK CKT
Size A3
Document Number
NORN 2.0
Rev -1
Date: Wednesday, July 16, 2008
Sheet 36 of 52



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

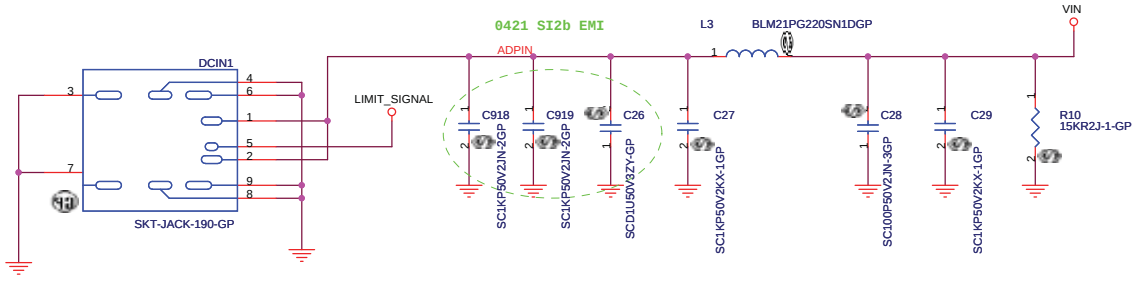
Title: ***Power Block Diagram***

Size	Document Number	Rev
A3	NORN 2.0	-1

Date: Wednesday, July 16, 2008 Sheet 37 of 52

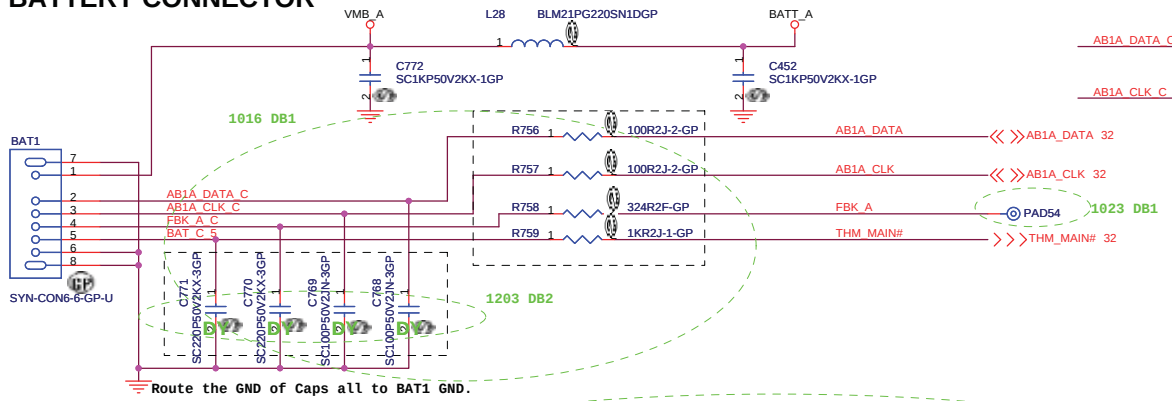
Adaptor in to generate DCBATOUT

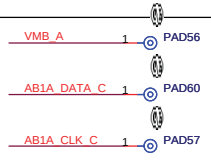
Current Rating 6 A

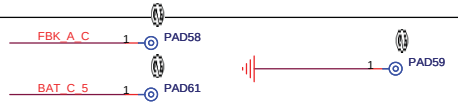


MAIN BATTERY CONNECTOR

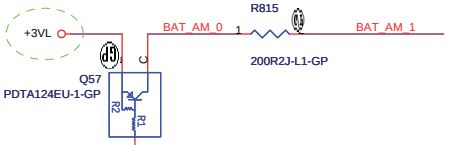
Current Rating 6 A



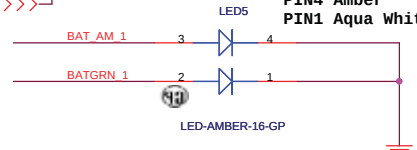




1017 DB1 Change +3VALW to +3VL.



PIN4 Amber
PIN1 Aqua White

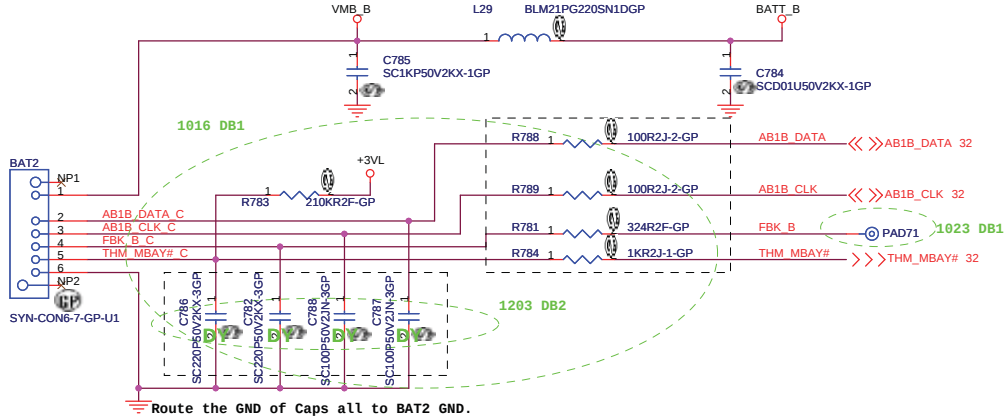


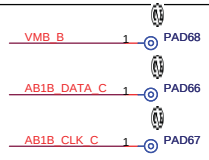
Layout Note:
Place R677, R678, R423, R818, C618, C617, C613 and C609 close to BAT1.

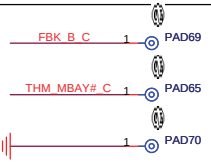
1008 DB1 Remove D74 and
move D68, D73 and D75 to Page32.

BAY BATTERY CONNECTOR

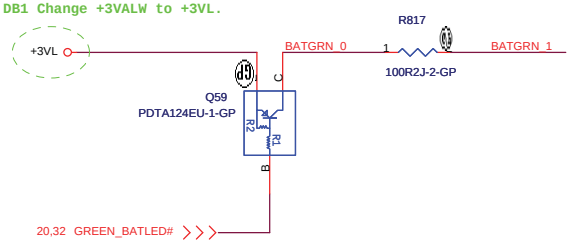
Current Rating 6 A







1017 DB1 Change +3VALW to +3VL.



Layout Note:
Place R704, R705, R709, R707, C639, C640, C635 and C636 close to BAT2.

1008 DB1 Remove D77 and
move D76, D78 and D79 to Page32.

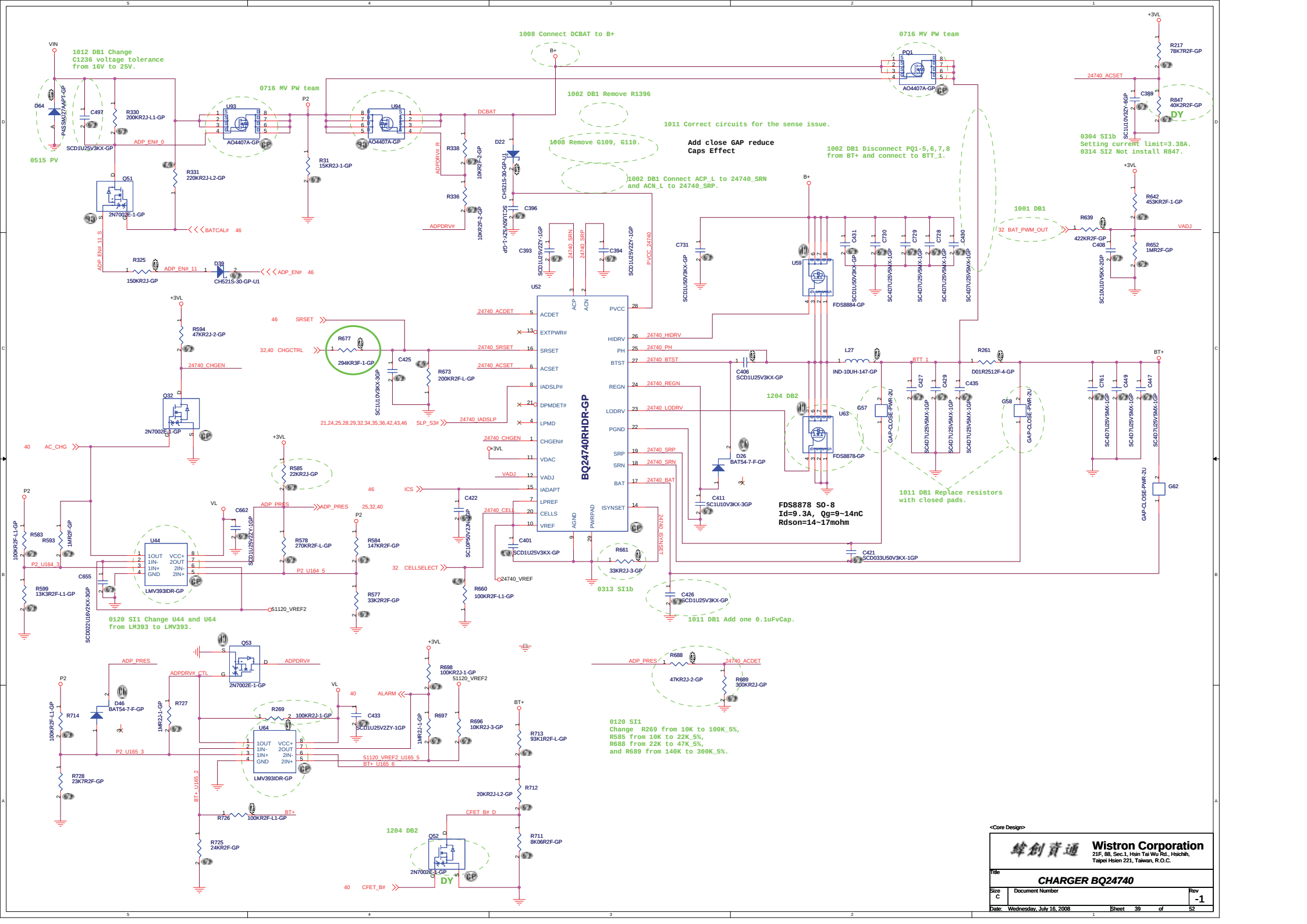
<Core Design>

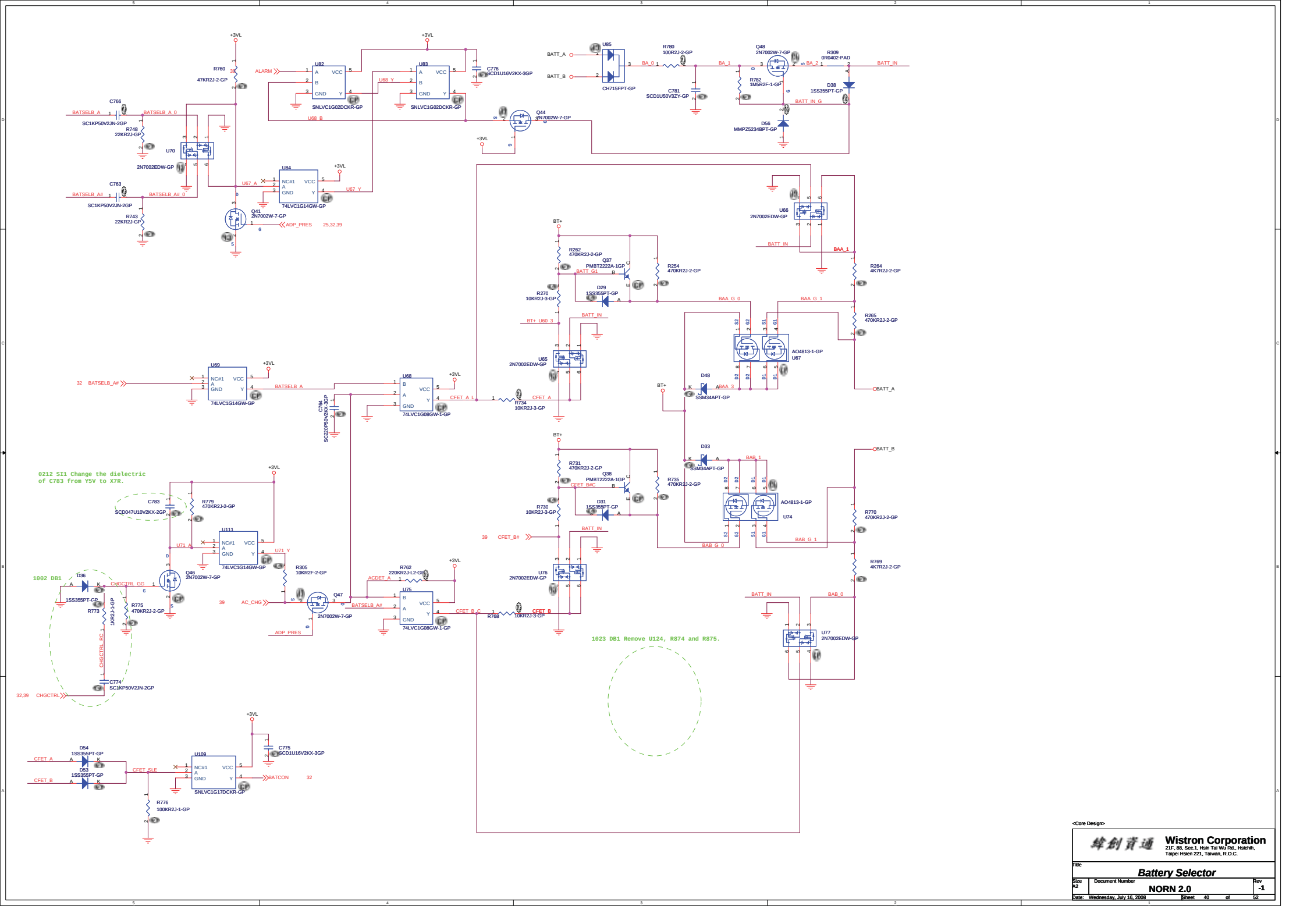
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

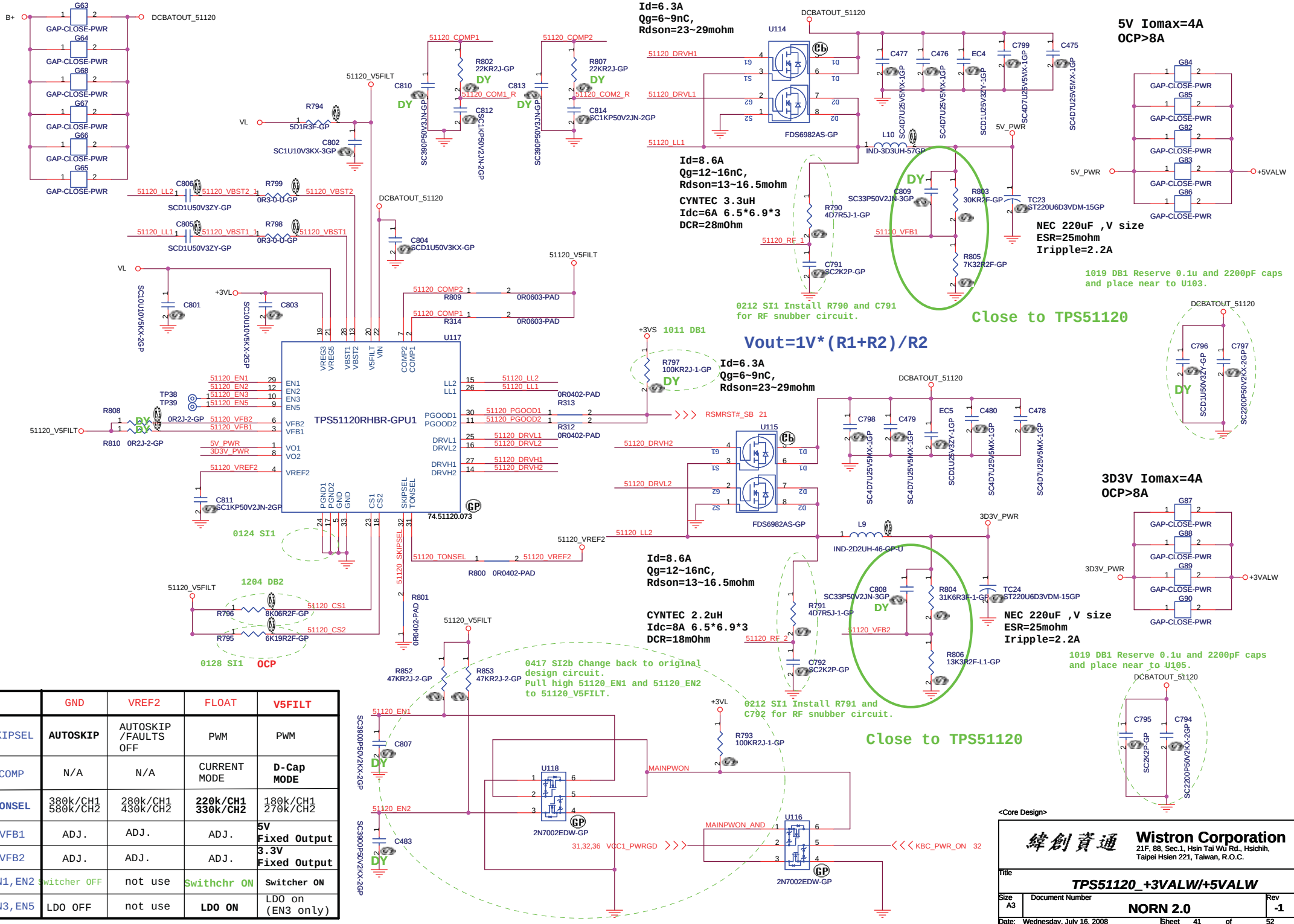
Title: DC & BATTERT CONN.

Size	Document Number	Rev
Custom	NORN 2.0	-1

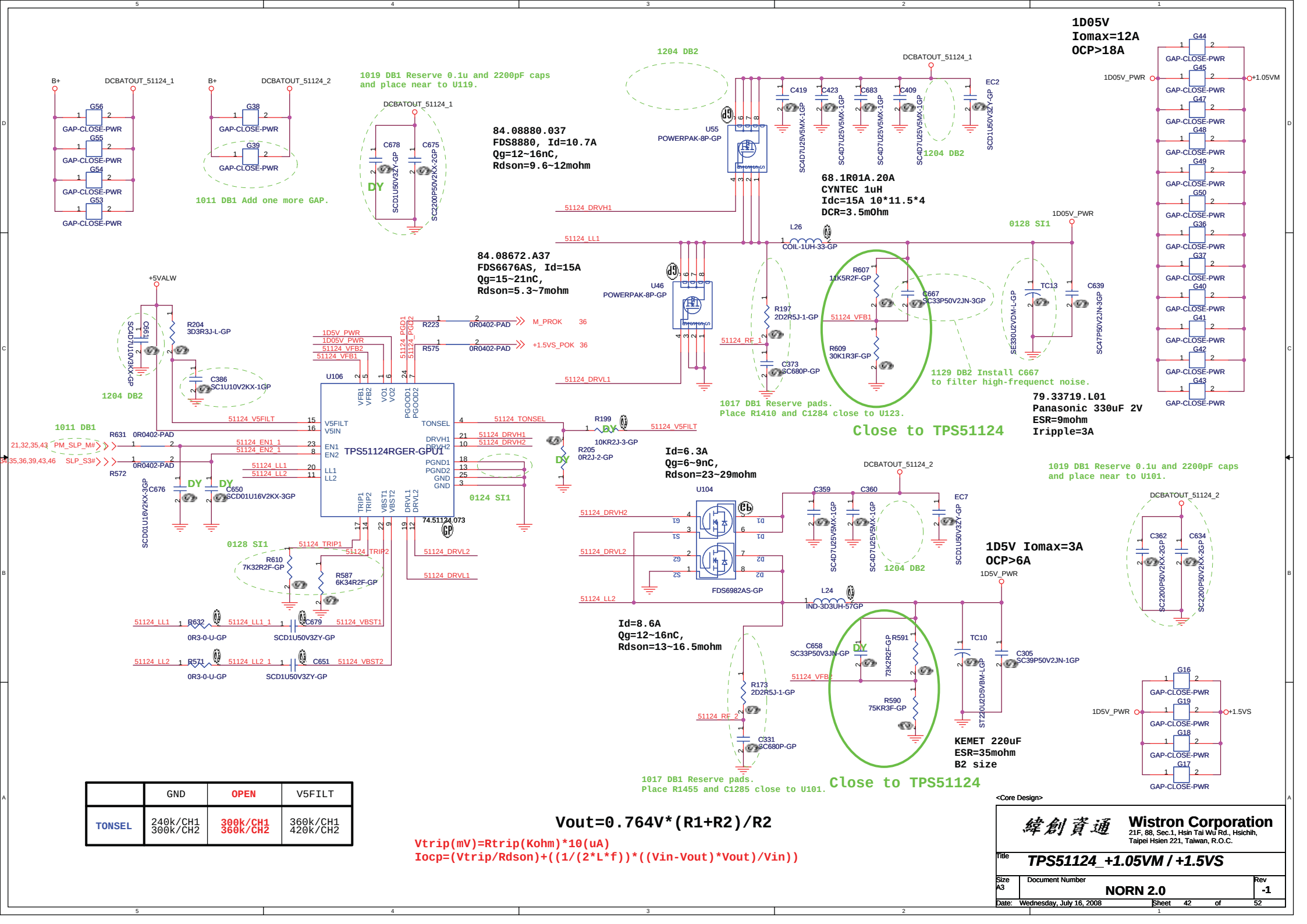
Date: Wednesday, July 16, 2008 Sheet 38 of 52


1008 Connect DCBAT to B+
0716 MV PW team
1012 DB1 Change
C1236 voltage tolerance
from 16V to 25V.
1002 DB1 Remove R1396
1011 Correct circuits for the sense issue.
1008 Remove G109, G110.
Add close GAP reduce
Caps Effect
1002 DB1 Disconnect PQ1-5,6,7,8
from BT+ and connect to BTT_1.
1002 DB1 Connect ACP_L to 24740_SRN
and ACN_L to 24740_SRP.
0304 SI1b
Setting current limit=3.38A.
0314 SI2 Not install R847.
0515 PV
1001 DB1
1204 DB2
BQ24740RHDR-GP
FDS8878 SO-8
Id=9.3A, Qg=9~14nC
Rdson=14~17mohm
1011 DB1 Replace resistors
with closed pads.
0313 SI1b
1011 DB1 Add one 0.1uFvCap.
0120 SI1 Change U44 and U64
from LM393 to LMV393.
0120 SI1
Change R269 from 10K to 100K_5%,
R585 from 10K to 22K_5%,
R688 from 22K to 47K_5%,
and R689 from 140K to 300K_5%.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER BQ24740
Size C
Document Number
Rev -1
Date: Wednesday, July 16, 2008
Sheet 39 of 52


0212 SI1 Change the dielectric of C783 from Y5V to X7R.
1002 DB1
1023 DB1 Remove U124, R874 and R875.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
Battery Selector
Size A2
Document Number
NORN 2.0
Rev -1
Date: Wednesday, July 16, 2008
Sheet 40 of 52



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	**220k/CH1 330k/CH2**	180k/CH1 270k/CH2
VFB1	ADJ.	ADJ.	ADJ.	**5V Fixed Output**
VFB2	ADJ.	ADJ.	ADJ.	**3.3V Fixed Output**
EN1, EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3, EN5	LDO OFF	not use	**LDO ON**	LDO on (EN3 only)



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_+1.05VM / +1.5VS

Size: A3 | Document Number: NORN 2.0 | Rev: -1

Date: Wednesday, July 16, 2008 | Sheet 42 of 52

SC412A for 1D8V / RT9026_0D9V

1019 DB1 Reserve 0.1u and 2200pF caps and place near to U147.

0120 SI1 Not install R246 and C714.

84.08880.037
FDS8880, Id=10.7A
Qg=12~16nC,
Rdson=9.6~12mohm

0522 PV
Change R238 to 15K ohm.

1204 DB2

1212 DB2

0128 SI1

84.08672.A37
FDS6676AS, Id=15A
Qg=15~21nC,
Rdson=5.3~7mohm

0212 SI1 Install R581 and C659 for RF snubber circuit.

68.1R01A.20B
CYNTEC 1uH
Idc=11A 6.5*6.9*3
DCR=10mOhm

77.C3371.051
NEC 330uF 2.5V
ESR=9mOhm
Iripple=3.725A

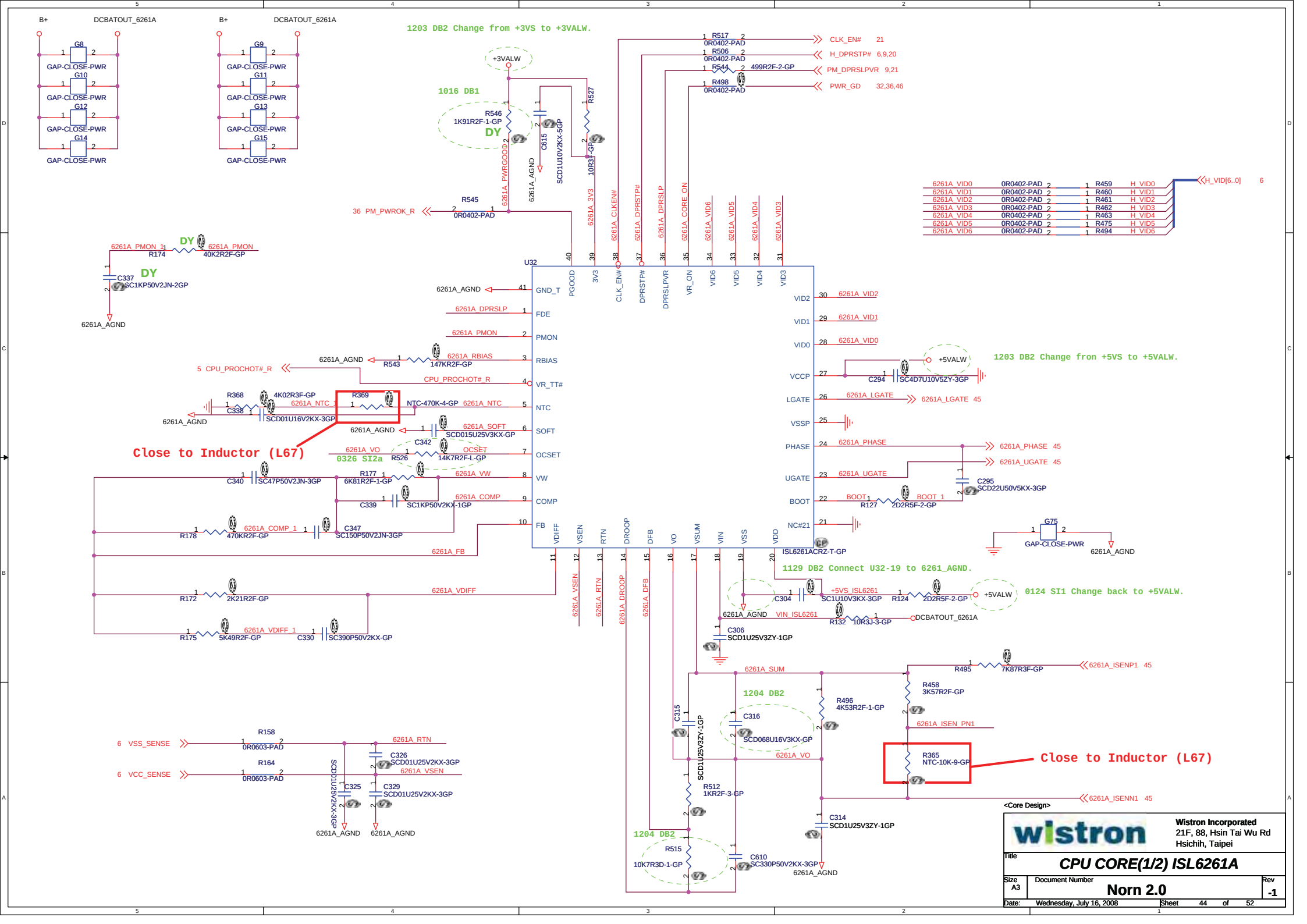
Close to SC412A

1D8V_PWR
10A , OCP >16A

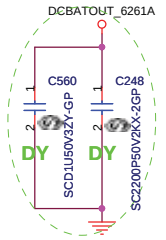
0D9V
Iomax=2A

<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: SC 412A_1D8V/0.9VP_RT9026		
Size: A3	Document Number: NORN 2.0	Rev: -1
Date: Wednesday, July 16, 2008	Sheet 43 of 52	


1203 DB2 Change from +3VS to +3VALW.
1016 DB1
DY
U32
ISL6261ACRZ-T-GP
Close to Inductor (L67)
1129 DB2 Connect U32-19 to 6261_AGND.
1203 DB2 Change fron +5VS to +5VALW.
0124 SI1 Change back to +5VALW.
0326 SI2a
1204 DB2
Close to Inductor (L67)
<Core Design>
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
CPU CORE(1/2) ISL6261A
Norn 2.0
Wednesday, July 16, 2008
Sheet 44 of 52

1019 DB1 Reserve 0.1u and 2200pF caps
and place near to U152.



1019 DB1 Reserve pads.
Place R1457 and C1287 close to U154.

When test without cpu,
R581 & R582 change to 0 ohms

<Core Design>

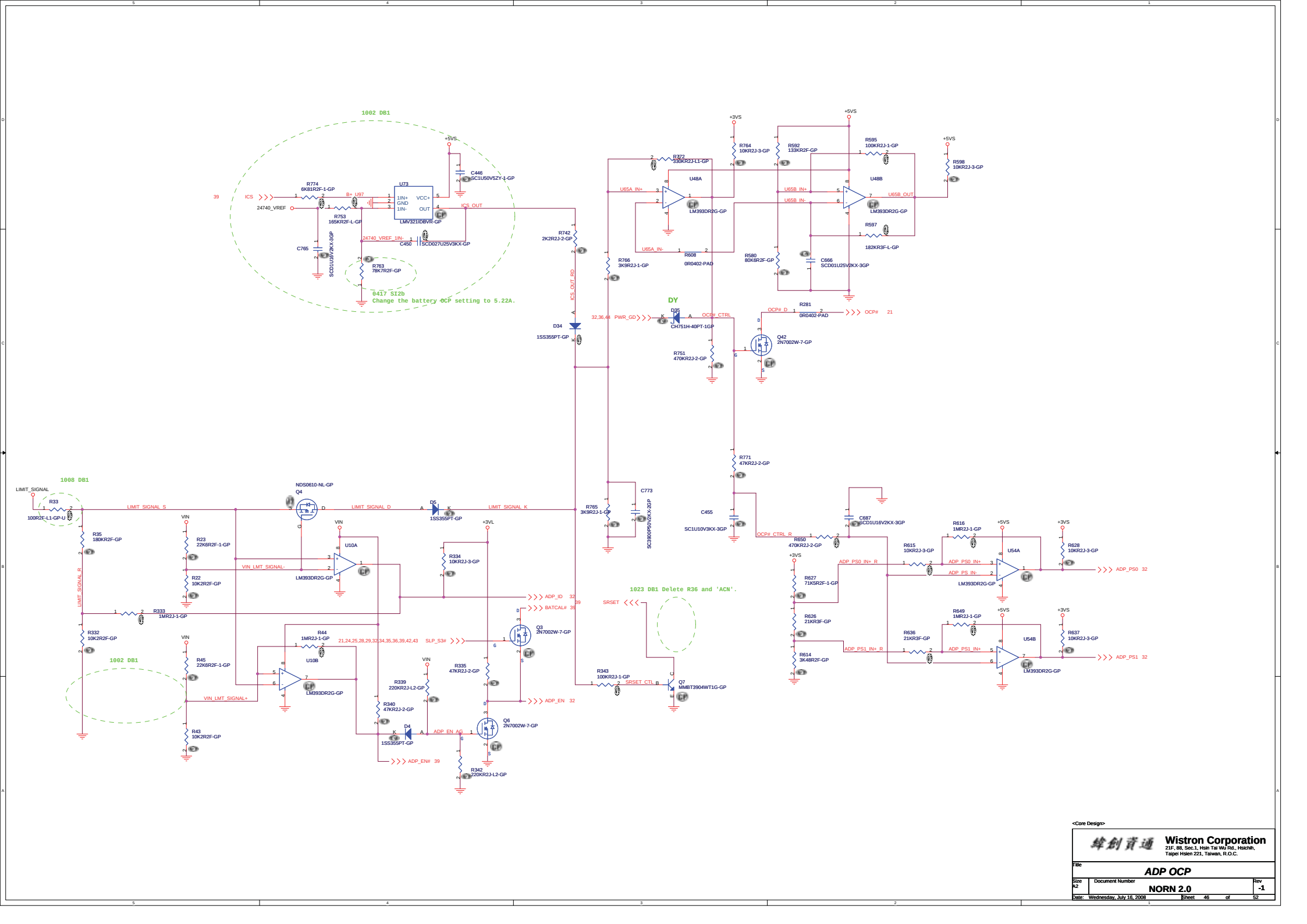
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU CORE(2/2) ISL6261A

Size	Document Number	Rev
A3	Norn 2.0	-1

Date: Wednesday, July 16, 2008 Sheet 45 of 52



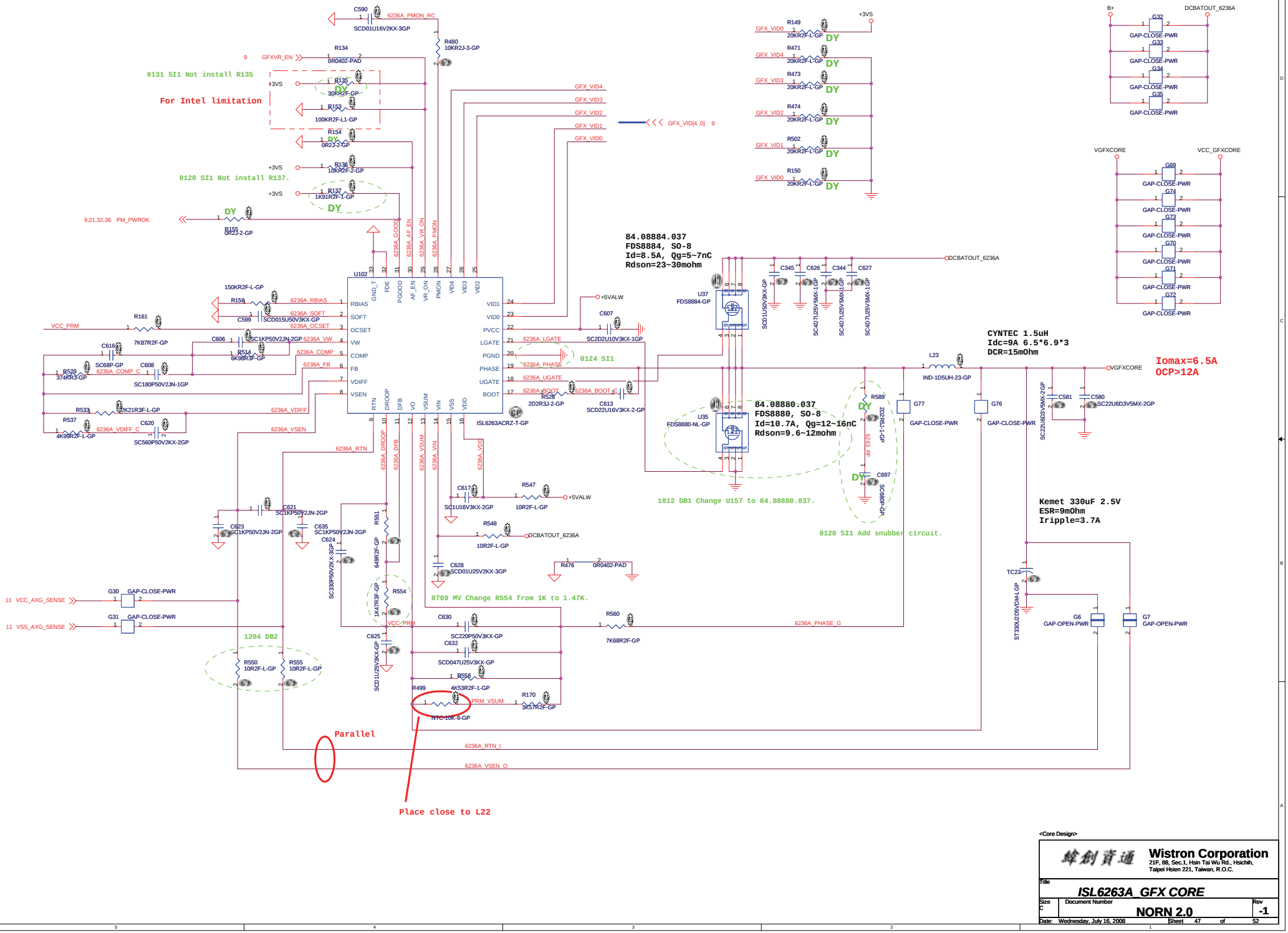
<Core Design>

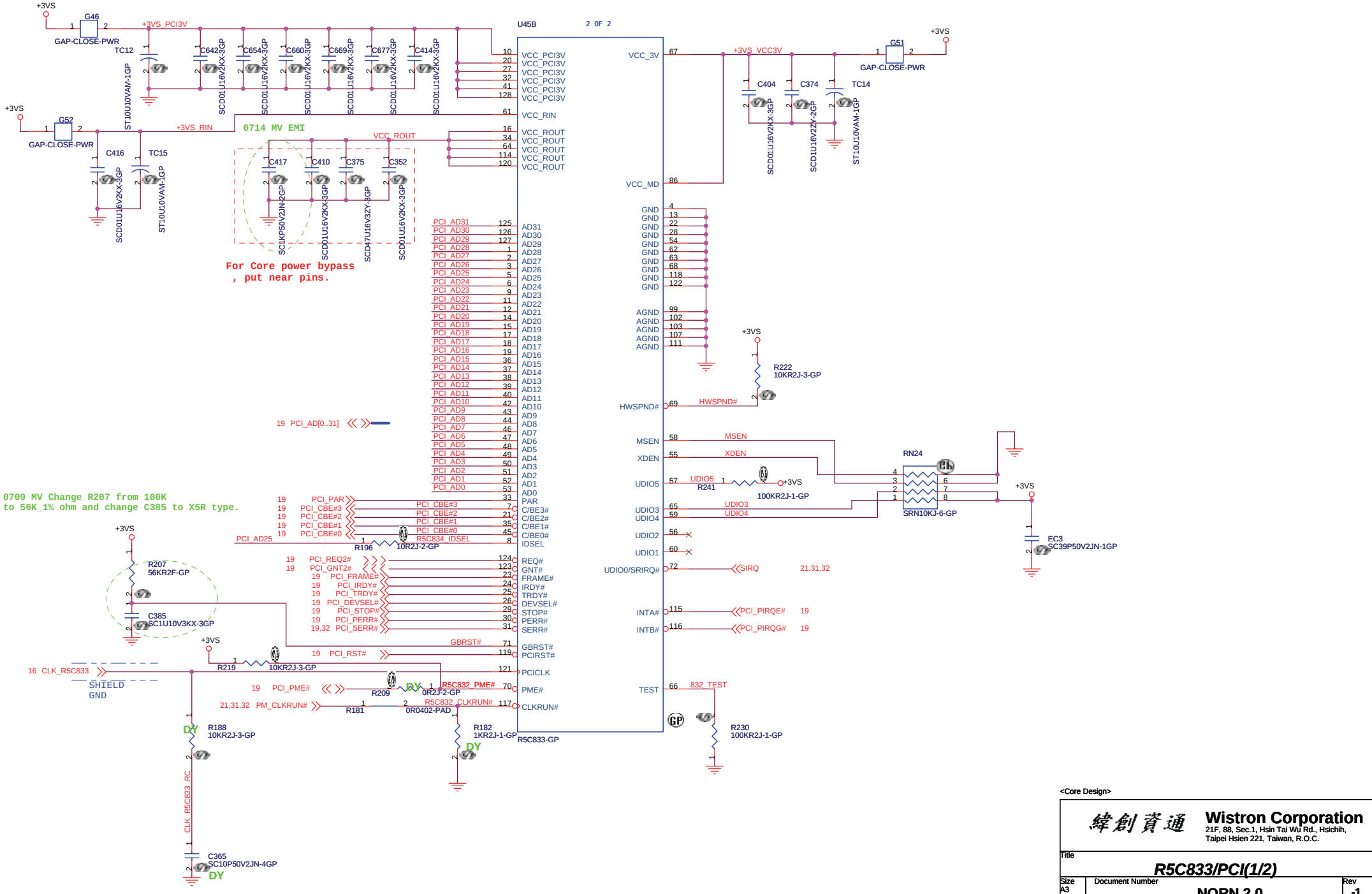
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

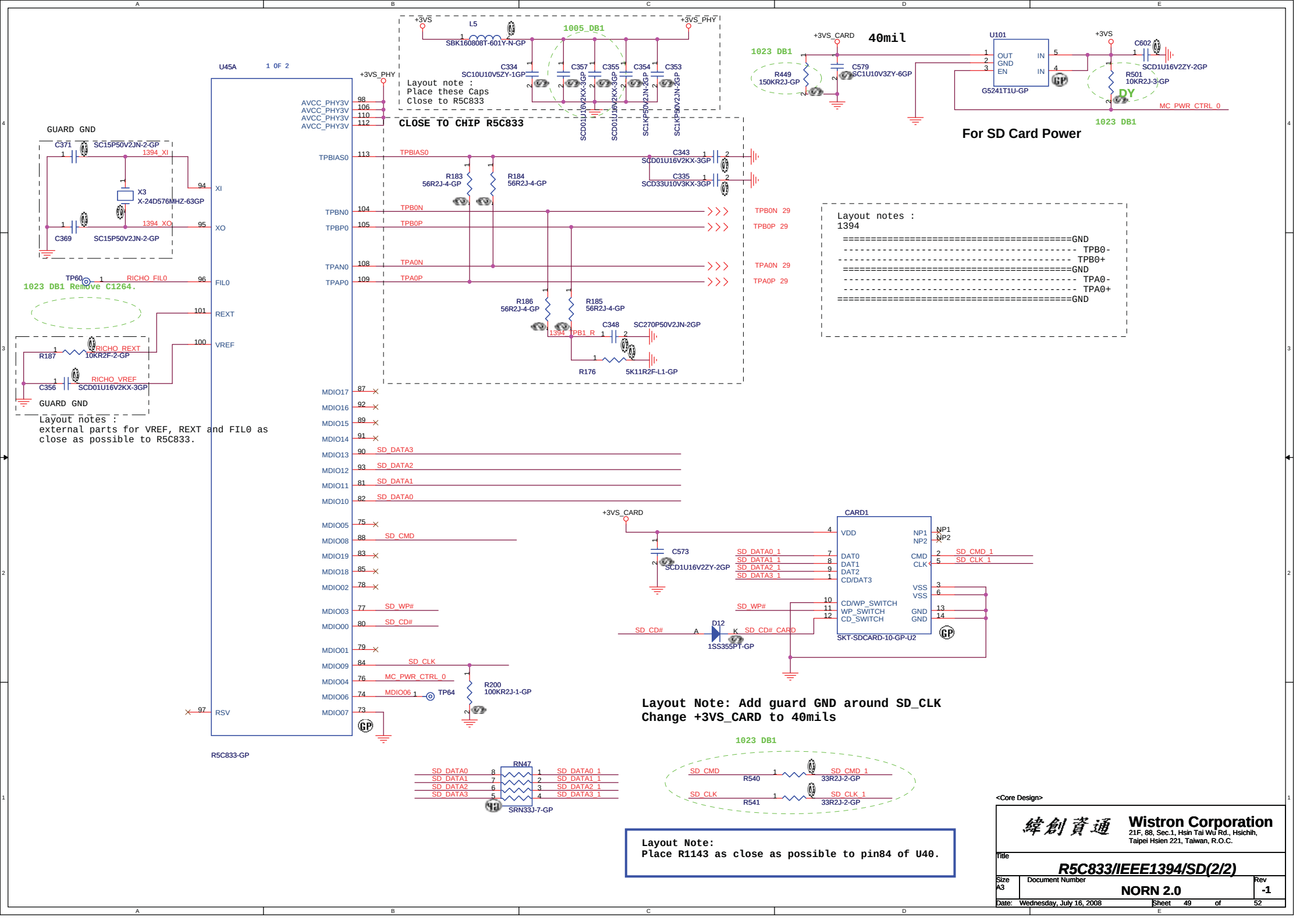
Title: **ADP OCP**

Size	Document Number	Rev
A2	NORN 2.0	-1

Date: Wednesday, July 16, 2008 Sheet 46 of 52


0131 SI1 Not install R135
For Intel limitation
0120 SI1 Not install R137.
84.08884.037
FDS8884, SO-8
Id=8.5A, Qg=5~7nC
Rdson=23~30mohm
84.08880.037
FDS8880, SO-8
Id=10.7A, Qg=12~16nC
Rdson=9.6~12mohm
CYNTEC 1.5uH
Idc=9A 6.5*6.9*3
DCR=15mOhm
Iomax=6.5A
OCP>12A
Kemet 330uF 2.5V
ESR=9mOhm
Iripple=3.7A
0124 SI1
1012 DB1 Change U157 to 84.08880.037.
0120 SI1 Add snubber circuit.
0709 MV Change R554 from 1K to 1.47K.
1204 DB2
Parallel
Place close to L22
ISL6263ACRZ-T-GP
GFX_VID[4..0]
6236A_RTN_I
6236A_VSEN_O
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6263A_GFX CORE
NORN 2.0
Wednesday, July 16, 2008


U45B
2 OF 2
0714 MV EMI
For Core power bypass
, put near pins.
0709 MV Change R207 from 100K
to 56K_1% ohm and change C385 to X5R type.
SHIELD
GND
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
R5C833/PCI(1/2)
Size
A3
Document Number
NORN 2.0
Rev
-1
Date: Wednesday, July 16, 2008
Sheet 48 of 52



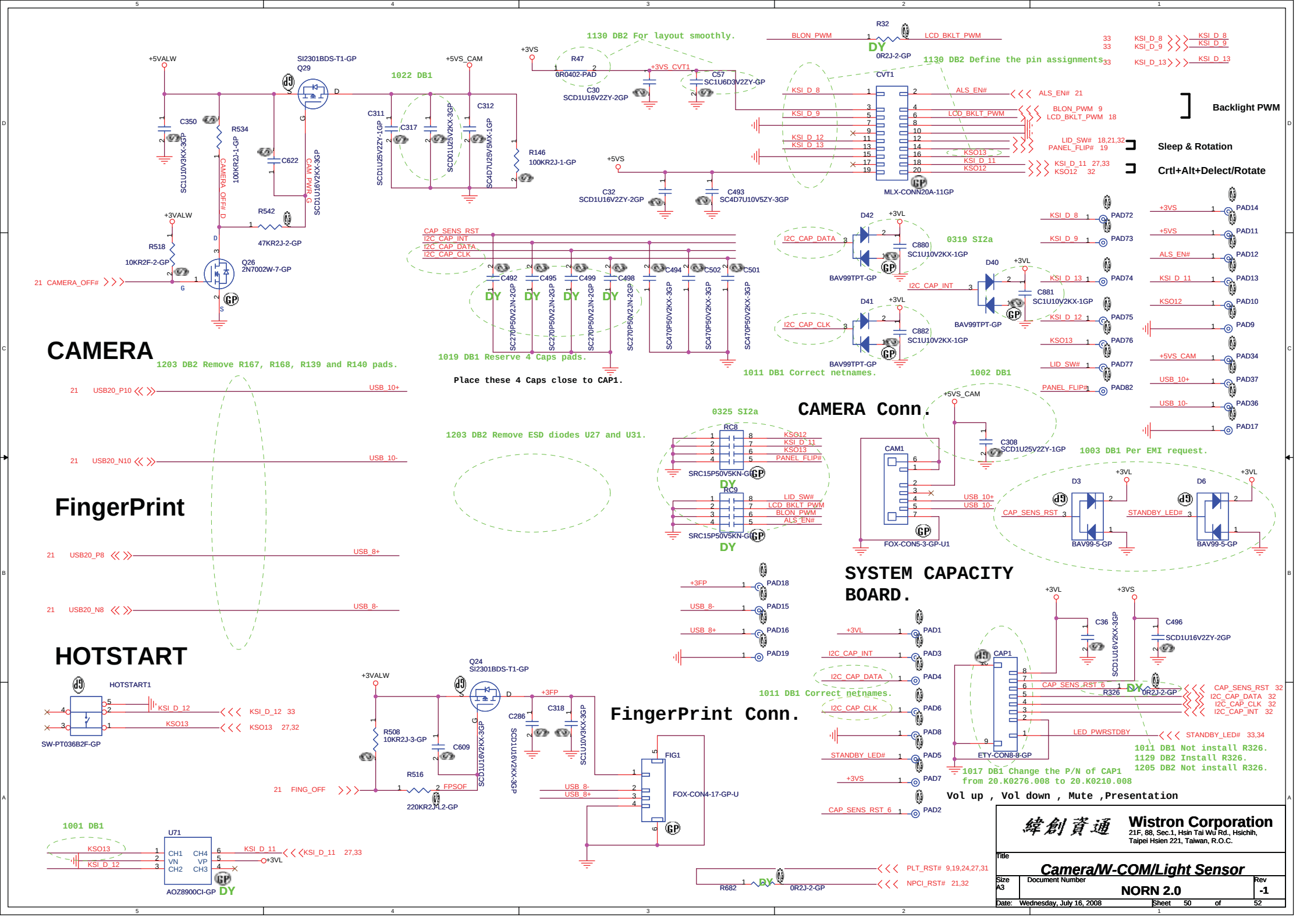
<Core Design>

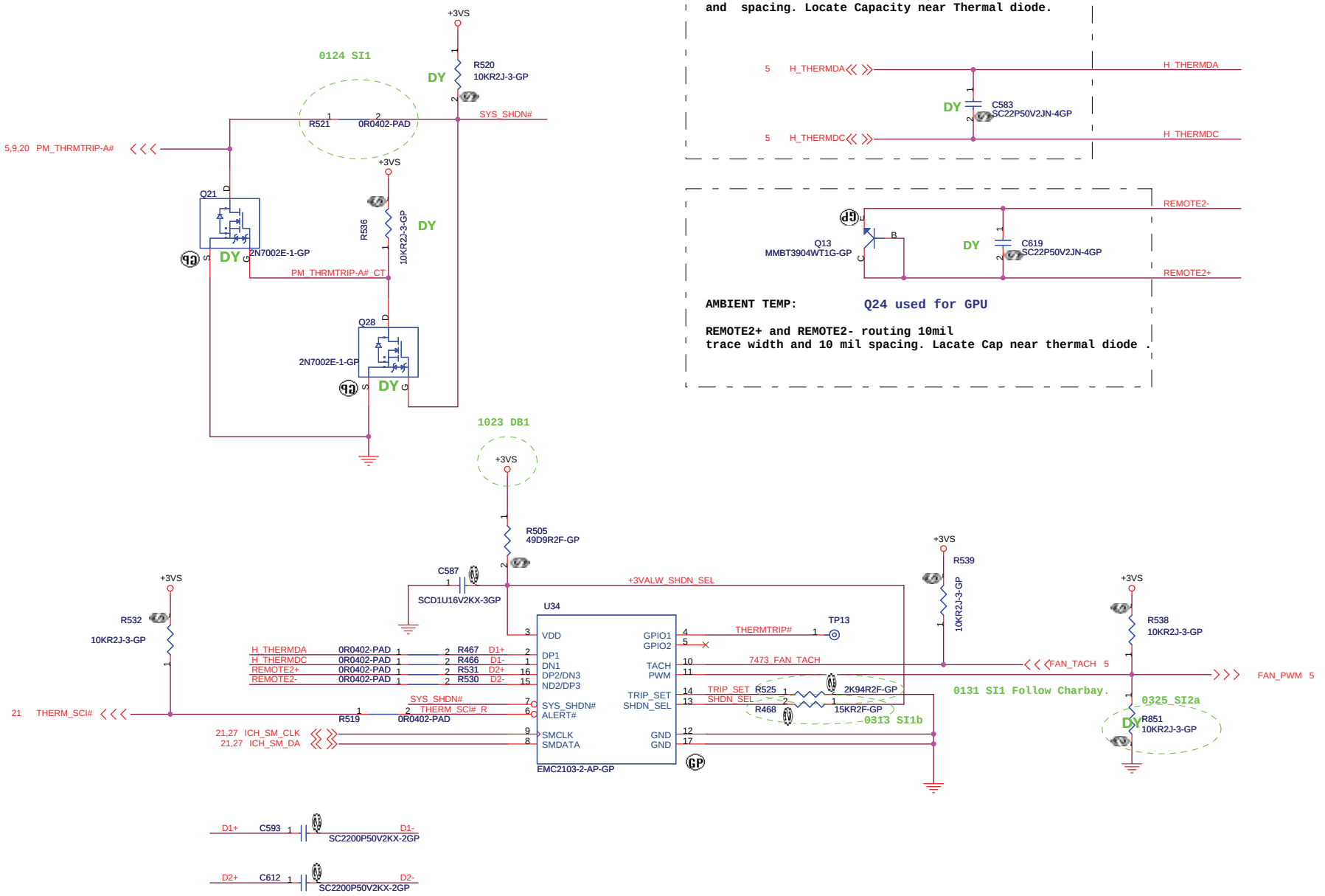
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C833/IEEE1394/SD(2/2)

Size	Document Number	Rev
A3	NORN 2.0	-1

Date: Wednesday, July 16, 2008 Sheet 49 of 52


CAMERA
1203 DB2 Remove R167, R168, R139 and R140 pads.
FingerPrint
HOTSTART
1203 DB2 Remove ESD diodes U27 and U31.
1130 DB2 For layout smoothly.
1130 DB2 Define the pin assignments
1022 DB1
1019 DB1 Reserve 4 Caps pads.
Place these 4 Caps close to CAP1.
1011 DB1 Correct netnames.
0319 SI2a
1002 DB1
0325 SI2a
CAMERA Conn.
1003 DB1 Per EMI request.
SYSTEM CAPACITY BOARD.
FingerPrint Conn.
1011 DB1 Correct netnames.
1017 DB1 Change the P/N of CAP1 from 20.K0276.008 to 20.K0210.008
1011 DB1 Not install R326.
1129 DB2 Install R326.
1205 DB2 Not install R326.
Vol up , Vol down , Mute ,Presentation
1001 DB1
Backlight PWM
Sleep & Rotation
Crtl+Alt+Delect/Rotate
MLX-CONN20A-11GP
FOX-CON5-3-GP-U1
FOX-CON4-17-GP-U
ETY-CON8-8-GP
SRC15P50V5KN-GP
BAV99TPT-GP
BAV99-5-GP
SW-PT036B2F-GP
AOZ8900CI-GP
SI2301BDS-T1-GP
2N7002W-7-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Camera/W-COM/Light Sensor
Size A3
Document Number
NORN 2.0
Rev -1
Date: Wednesday, July 16, 2008
Sheet 50 of 52



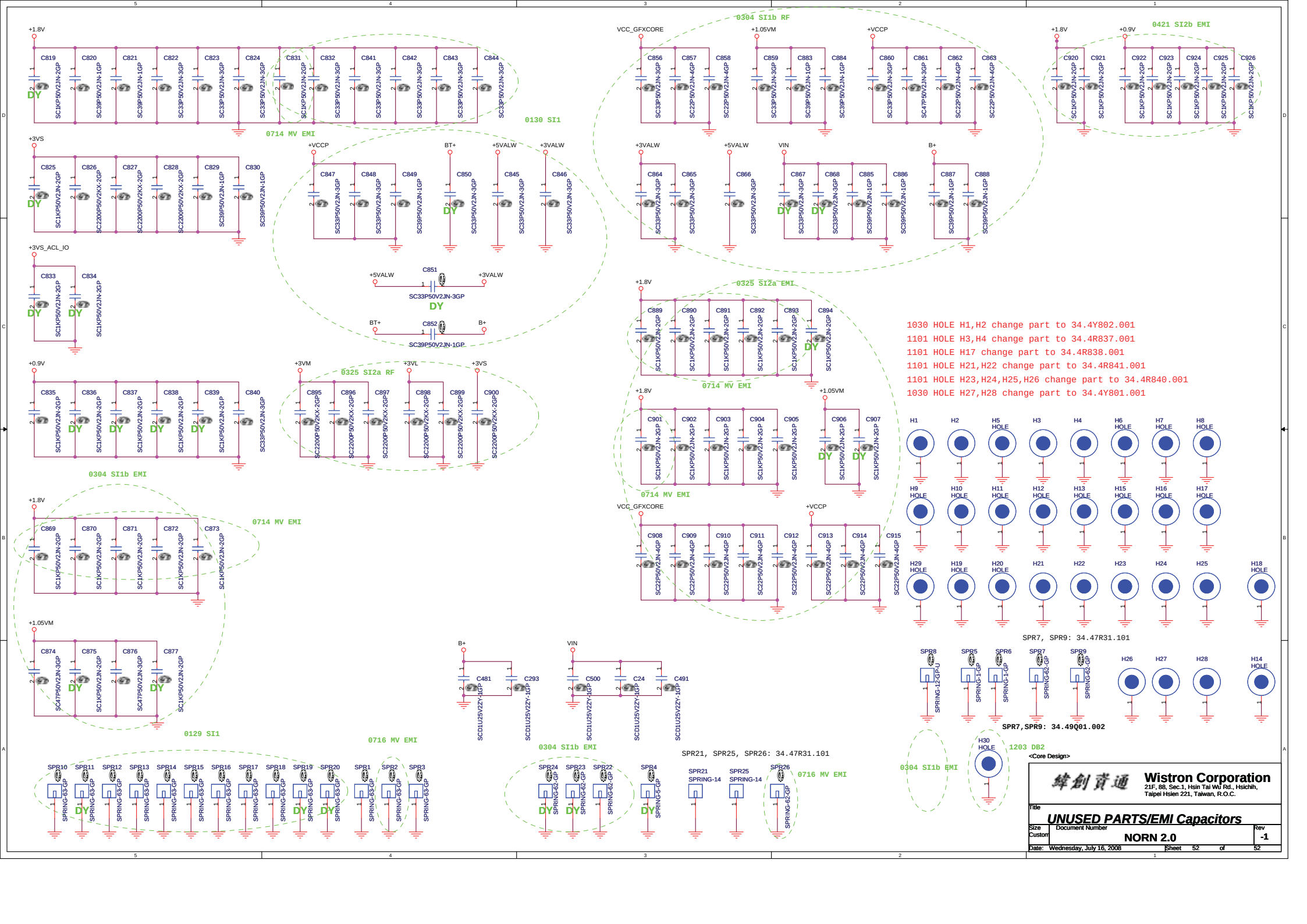
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SMSC2103 Thermal Sensor***

Size	Document Number	Rev
A3	NORN 2.0	-1

Date: Wednesday, July 16, 2008 Sheet 51 of 52


0304 SI1b RF
0421 SI2b EMI
0130 SI1
0714 MV EMI
0325 SI2a EMI
0325 SI2a RF
0304 SI1b EMI
0129 SI1
0716 MV EMI
1030 HOLE H1,H2 change part to 34.4Y802.001
1101 HOLE H3,H4 change part to 34.4R837.001
1101 HOLE H17 change part to 34.4R838.001
1101 HOLE H21,H22 change part to 34.4R841.001
1101 HOLE H23,H24,H25,H26 change part to 34.4R840.001
1030 HOLE H27,H28 change part to 34.4Y801.001
SPR7, SPR9: 34.47R31.101
SPR7,SPR9: 34.49Q01.002
SPR21, SPR25, SPR26: 34.47R31.101
1203 DB2
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
UNUSED PARTS/EMI Capacitors
Size Custom
Document Number
NORN 2.0
Rev
-1
Date: Wednesday, July 16, 2008
Sheet 52 of 52