Wistron Confidential

SI2

2009/09/10 REV :SI2-01

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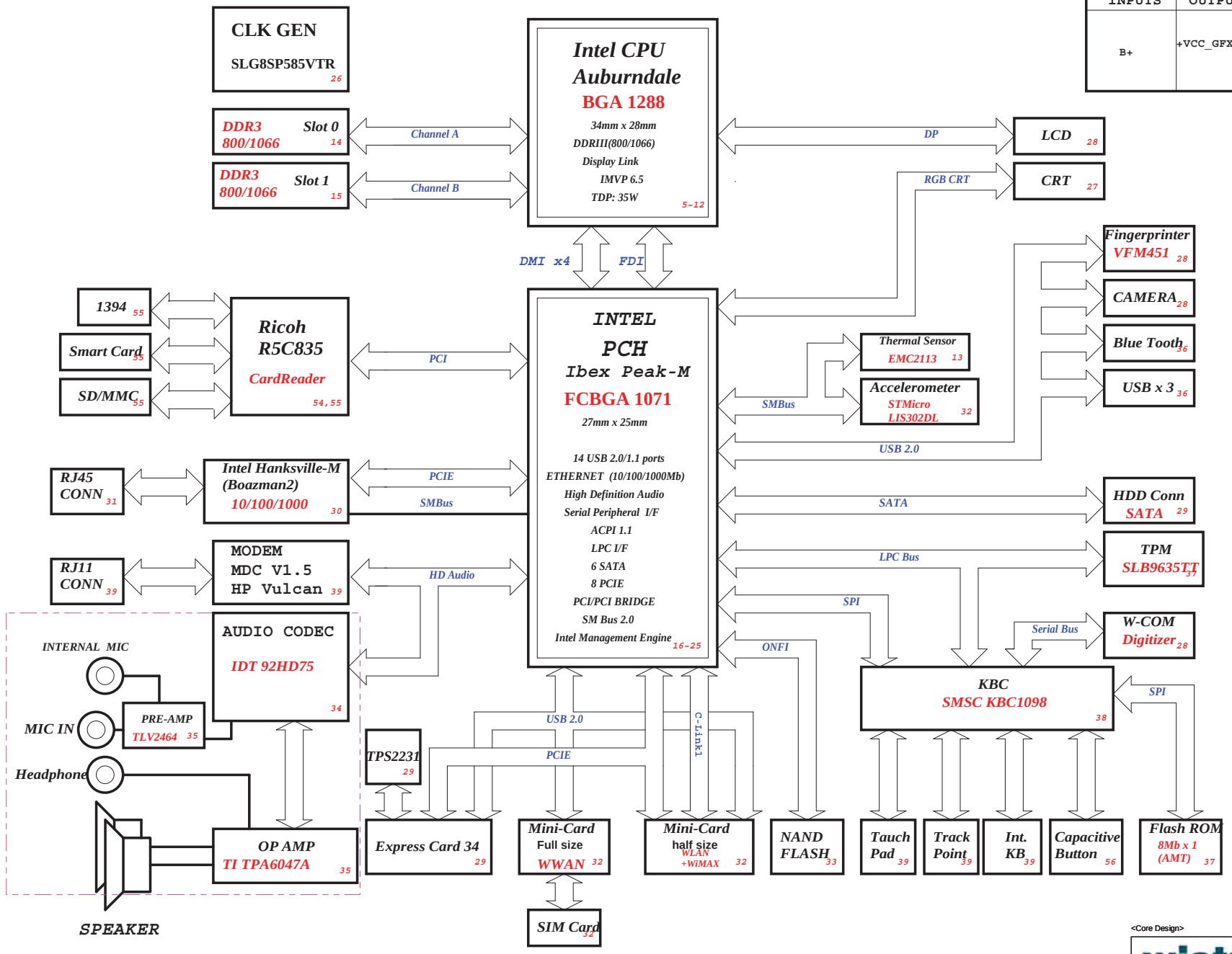
Title: NORN 3.0

Size: A3 | Document Number: NORN 3.0 | Rev: SE

Date: Thursday, September 10, 2009 Sheet 1 of 57

Norn3.0 BLOCK DIAGRAM



VGA TPS51611	
INPUTS	OUTPUTS
B+	+VCC_GFXCORE 15A 53

SYSTEM DC/DC TPS51125	
INPUTS	OUTPUTS
B+	+5VALW 5.5A +3VALW 6.5A 47

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
B+	+1.5V 9.5A +1.05VM_LAN 9A +VCCP 18A 48, 49

CHARGER BQ24740	
INPUTS	OUTPUTS
	BATT
BATT_A	18V 3.0A
BATT_B	5V 100mA 45

CPU DC/DC TPS51621	
INPUTS	OUTPUTS
B+	+VCC_CORE 0.844~1.3V 35A 50, 51

PCB LAYER

L1:	Signal 1
L2:	GND/VCC
L3:	Signal 2
L4:	GND/VCC
L5:	Signal 3
L6:	Signal 4
L7:	VCC/GND
L8:	Signal 5
L9:	GND/VCC
L10:	Signal 6

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Title: Block Diagram

Size: Custom | Document Number: NORN 3.0 | Rev: SE

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Title

Change Notes List

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Voltage Rails

o MEANS ON x MEANS OFF

State \ power plane	+3VL VL	+3VALW +5VALW	+1.5V +0.75VS	+5VS +3VS +1.8VS +1.5VS +VCCP +1.05VS +VCC_CORE +VCC_GFXCORE	+3VM +1.05VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	X	O
S5 S4/Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EETERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader & 1394	AD22	2	G,E

DMA Channel	Device
DMA0	Modem/LAN
DMA1	ECP
DMA2	~~Floppy Disk~~
DMA3	Audio
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	Walk-up1 (Right Side)
1	Walk-up2 (Right Side)
2	Walk-up3 (Left Side)
3	Free
4	EXPRESS SLOT
5	Free
6	WLAN
7	Free
8	Bluetooth
9	WWAN
10	Fingerprint
11	Dock1 (HUB)
12	Webcam
13	Dock2 (IDE)

Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	~~Floppy~~
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family) PCI Express Root Port -27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family) USB Universal Host Control
18	Intel 82801H (ICH8 Family) USB Universal Host Control Richo R5C853 Integrates FlashMedia Control Richo R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family) PCI Express Root Port -27D6 Intel 82801H (ICH8 Family) USB Universal Host Control
20	Intel 82801H (ICH8 Family) USB Universal Host Control Intel 82801H (ICH8 Family) USB2 Enhanced Host Control
21	Intel 82801H (ICH8 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control
23	HP Mobile Data Protection Sensor

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Title: *Notes List*

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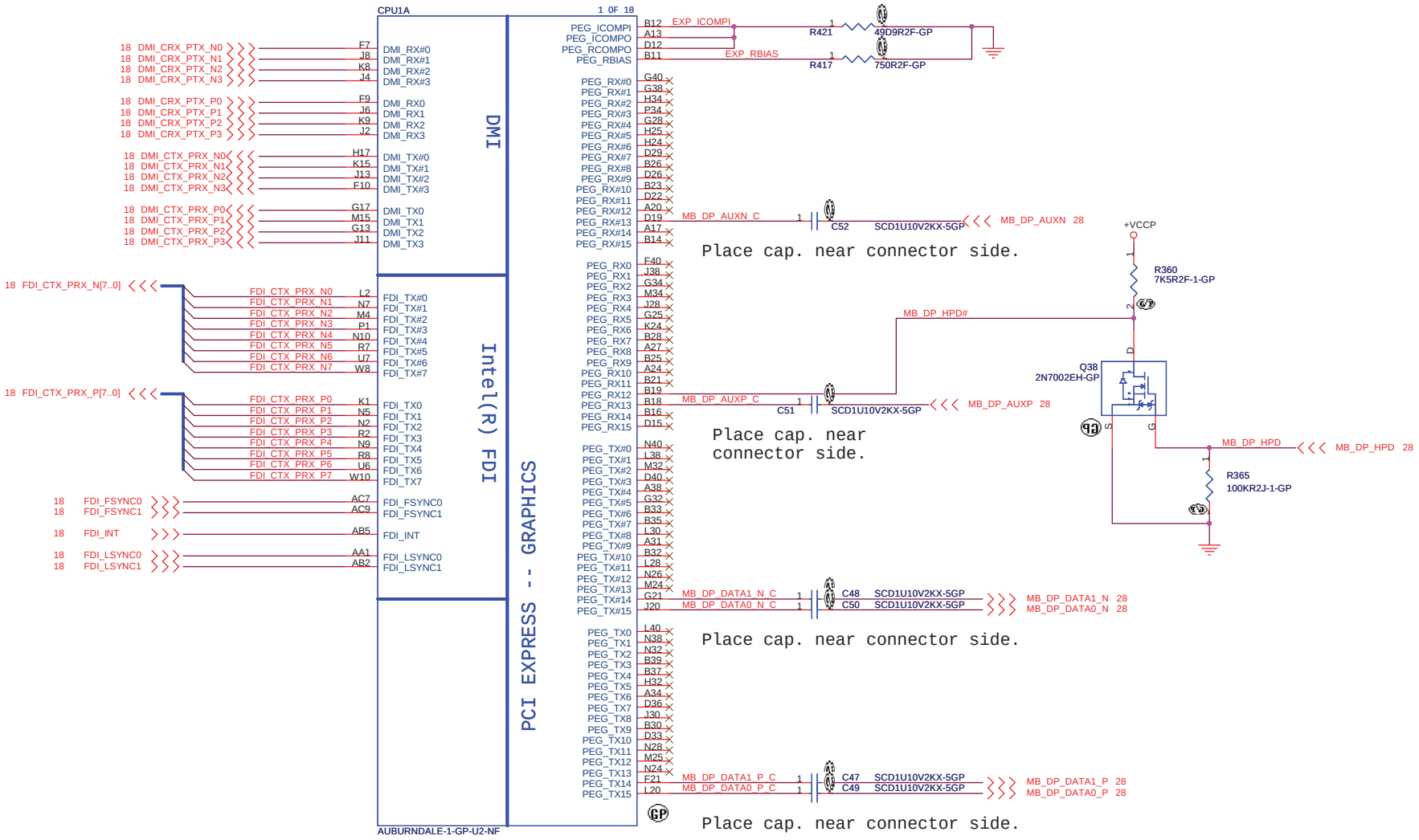
trace lenth <0.5"



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Title: Auburndale(1/8)-DMI+PEG+FDI

Size: A3 | Document Number: NORN 3.0 | Rev: SE

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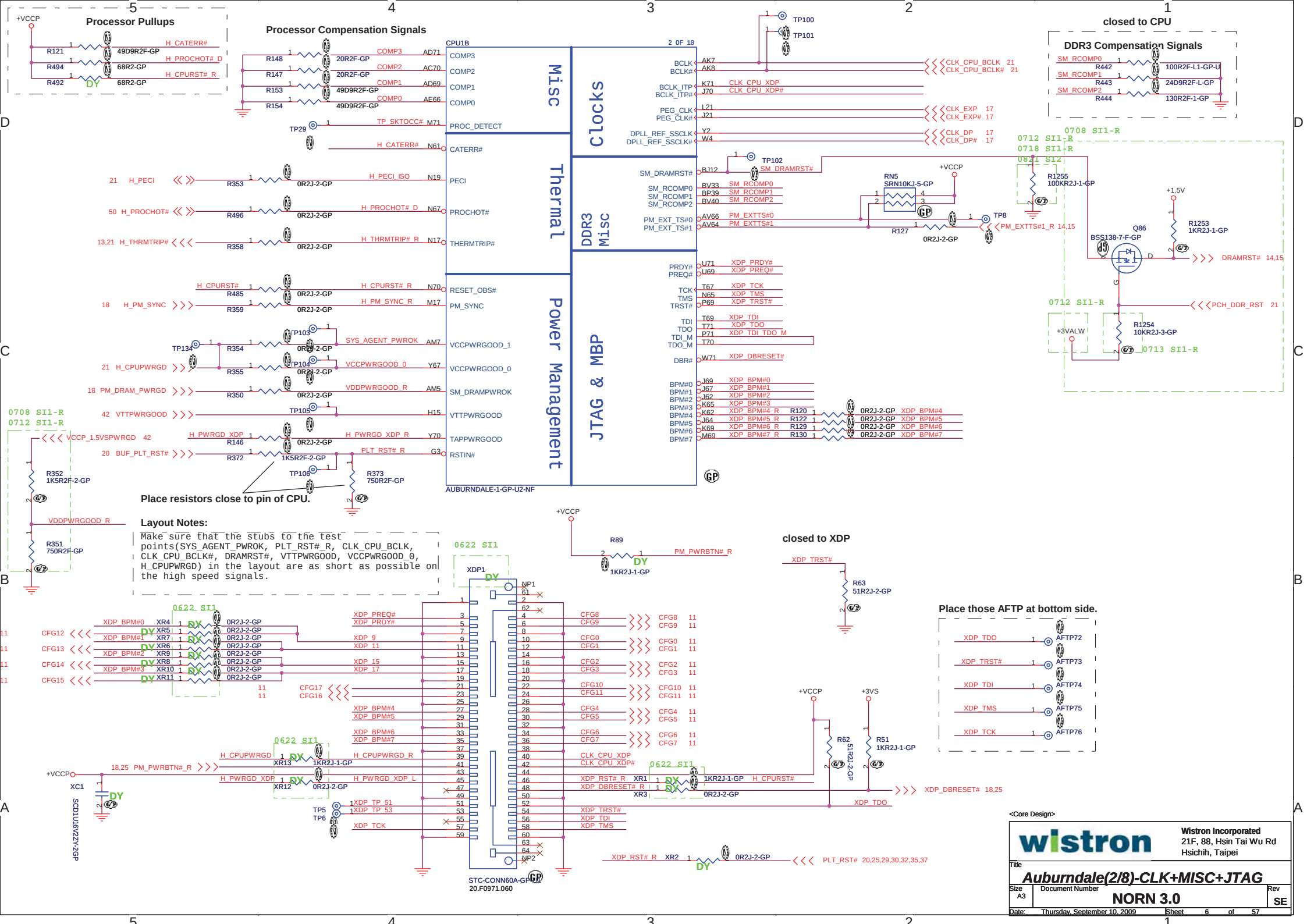
Processor Pullups
Processor Compensation Signals
CPU1B
Misc
Clocks
Thermal
DDR3 Misc
Power Management
JTAG & MBP
AUBURNDALE-1-GP-U2-NF
closed to CPU
DDR3 Compensation Signals
Place resistors close to pin of CPU.
Layout Notes:
Make sure that the stubs to the test points(SYS_AGENT_PWROK, PLT_RST#_R, CLK_CPU_BCLK, CLK_CPU_BCLK#, DRAMRST#, VTTPWRGOOD, VCCPWRGOOD_0, H_CPUPWRGD) in the layout are as short as possible on the high speed signals.
closed to XDP
Place those AFTP at bottom side.
STC-CONN60A-GP-2
20.F0971.060
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Auburndale(2/8)-CLK+MISC+JTAG
NORN 3.0
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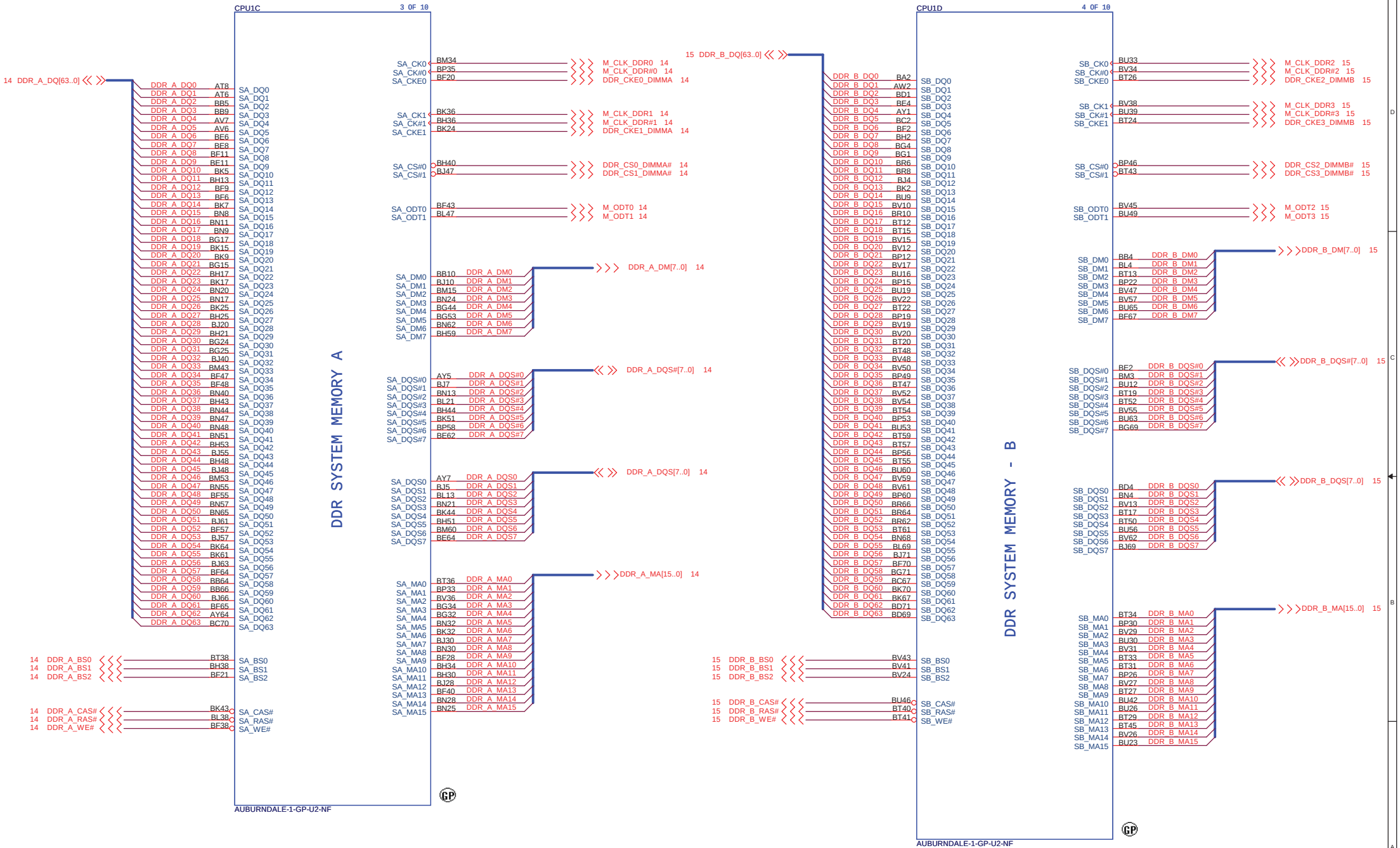

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Title: Auburndale(3/8)-DDR3

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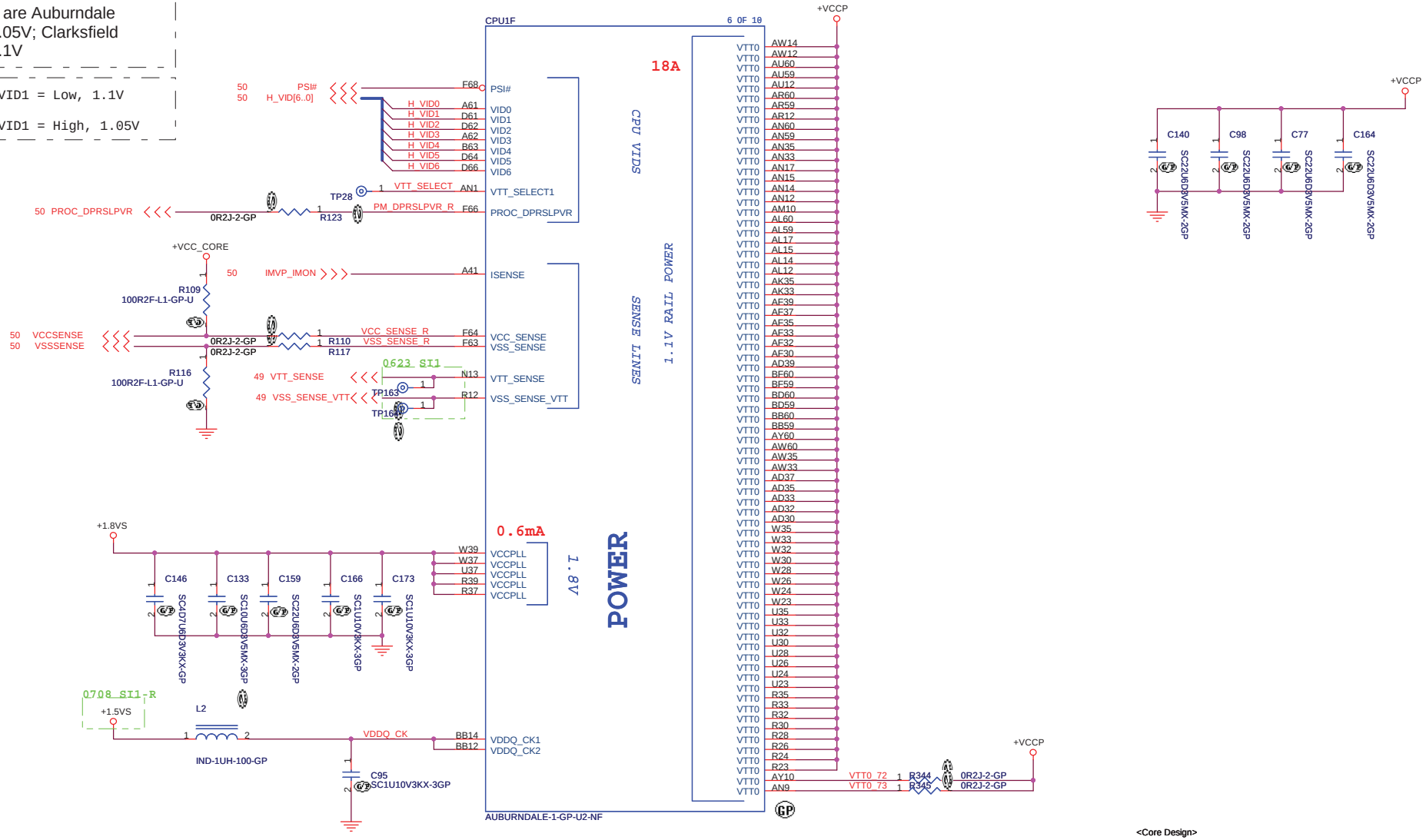
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

H_VTTVID1 = Low, 1.1V

H_VTTVID1 = High, 1.05V



<core design>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: *Auburndale(4/8)-POWER*		
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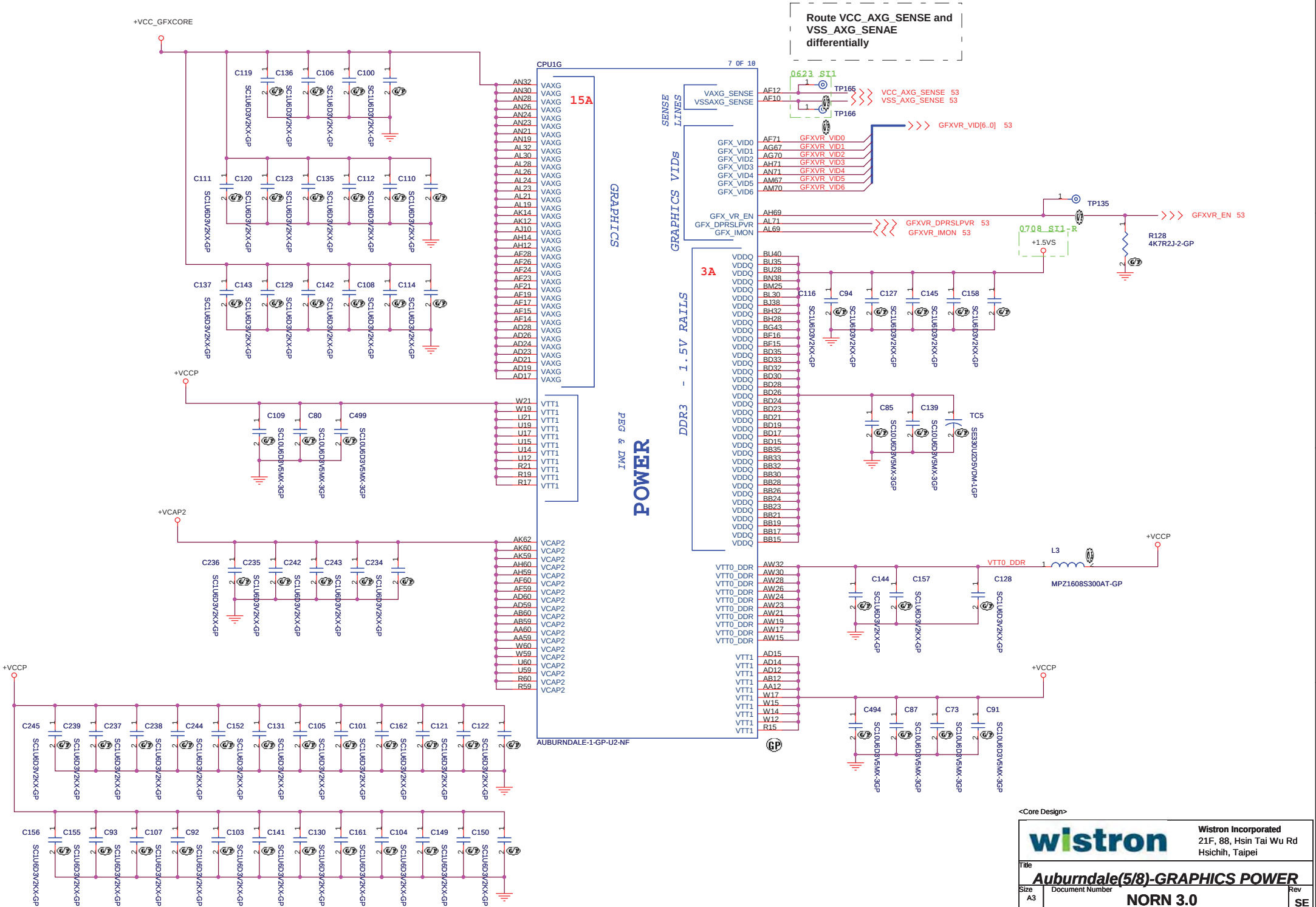
Route VCC_AXG_SENSE and VSS_AXG_SENAE differentially
+VCC_GFXCORE
CPU1G
7 OF 10
15A
3A
GRAPHICS
POWER
PEG & DMI
DDR3 - 1.5V RAILS
GRAPHICS VIDs
SENSE LINES
VAXG_SENSE
VSSAXG_SENSE
VCC_AXG_SENSE 53
VSS_AXG_SENSE 53
GFXVR_VID[6..0] 53
GFX_VID0
GFX_VID1
GFX_VID2
GFX_VID3
GFX_VID4
GFX_VID5
GFX_VID6
GFX_VR_EN
GFX_DPRSLPVR
GFX_IMON
GFXVR_DPRSLPVR 53
GFXVR_IMON 53
GFXVR_EN 53
TP135
TP165
TP166
0623_SI1
0708_SI1-R
+1.5VS
R128
4K7R2J-2-GP
+VCCP
+VCAP2
VTT0_DDR
L3
MPZ1608S300AT-GP
AUBURNDALE-1-GP-U2-NF
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Title
Auburndale(5/8)-GRAPHICS POWER
Size A3
Document Number
NORN 3.0
Rev SE
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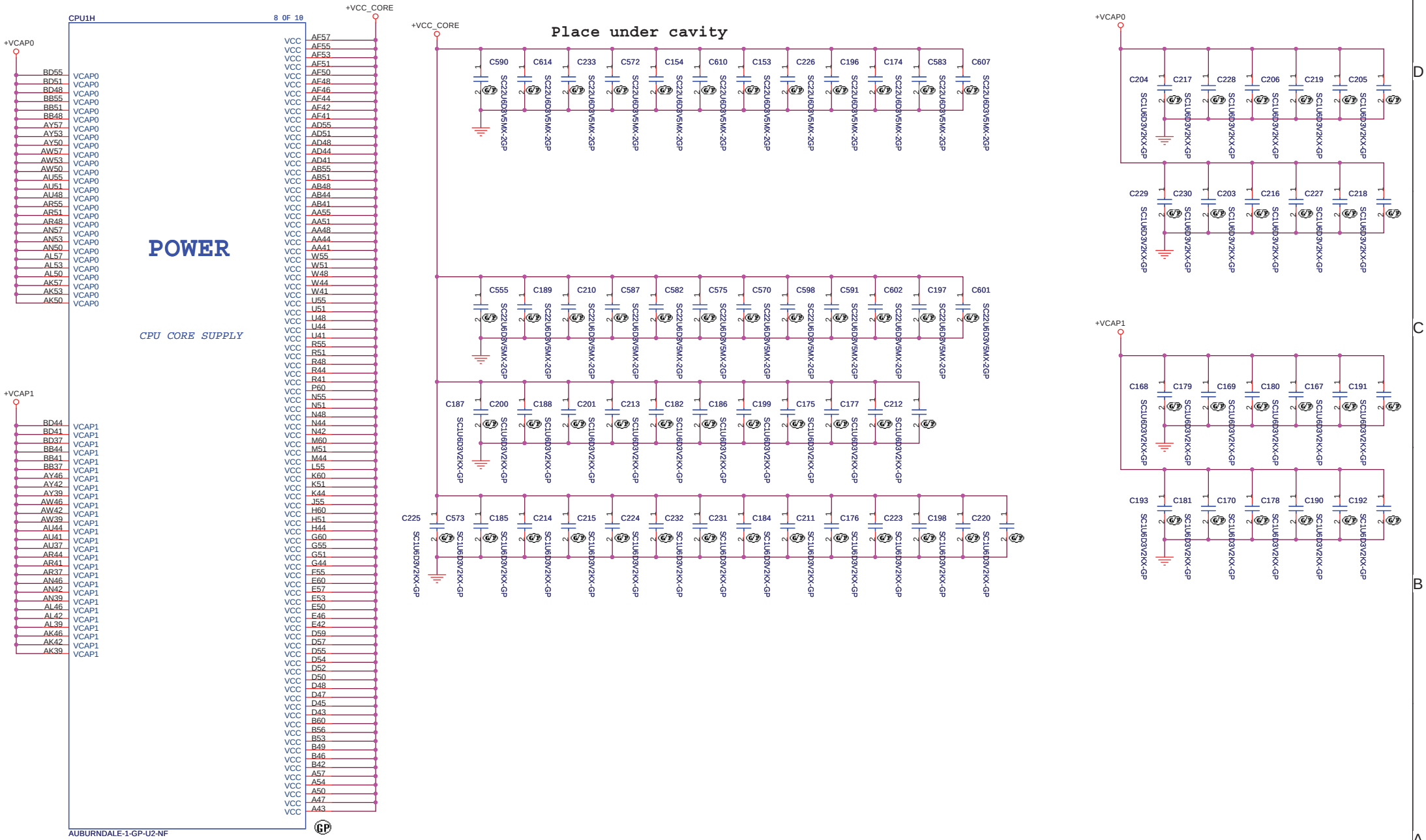

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Title: *Auburndale(6/8)-GND*

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CFG Straps for Processor

CFG0 — R346 3K01R2F-3-GP (DY)

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 — R347 3K01R2F-3-GP (DY)

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 — R348 3K3R2J-3-GP (0623 SI1)

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

Only temporary for early CFD samples (rPGA/BGA)

CFG7 — R349 3K01R2F-3-GP (DY)

BGA Ball Cracking Prevention and Detection

+3VS — R118 100KR2J-1-GP — VSS_NCTF2_R — U20 — CRACK_BGA (21,38 CRACK_BGA) — R108 100KR2J-1-GP — VSS_NCTF6_R

2N7002EDWH-GP
84.2N702.C3F
2nd = 84.DMN66.03F

+3VS — R490 100KR2J-1-GP — VSS_NCTF1_R — U88 — CRACK_BGA — R504 100KR2J-1-GP — VSS_NCTF7_R

2N7002EDWH-GP
84.2N702.C3F
2nd = 84.DMN66.03F

CPU1E — 5 OF 10 — AUBURNDALE-1-GP-U2-NF

RESERVED

CFG0 AL4 CFG1 AM2 CFG2 AK1 CFG3 AK2 CFG4 AK4 CFG5 AJ2 CFG6 AT2 CFG7 AG7 CFG8 AF4 CFG9 AG2 CFG10 AH1 CFG11 AC2 CFG12 AC4 CFG13 AE2 CFG14 AD1 CFG15 AF8 CFG16 AF6 CFG17 AB7

RSVD_TP0 AU1 — TP3

RSVD#T4 T4, RSVD#T2 T2

R357 0R2J-2-GP RSVD17 U1 RSVD#U1
R356 0R2J-2-GP RSVD18 V2 RSVD#V2

RSVD#AV71 AV71, RSVD#AW70 AW70

RSVD#AY69 AY69, RSVD#BB69 BB69

RSVD#D8 D8, RSVD#B7 B7

RSVD#A10 A10, RSVD#B9 B9

RSVD_NCTF#C5 C5, RSVD_NCTF#A6 A6

RSVD_NCTF#E3 E3, RSVD_NCTF#F1 F1

RSVD#W66 W66, RSVD#W64 W64 — RSVD#W66 — RSVD#W64 — TP167 TP168

RSVD#AC69 AC69, RSVD#AC71 AC71 — RSVD#AC69 — TP169

RSVD#AA71 AA71, RSVD#AA69 AA69 — RSVD#AA71 — TP170

RSVD#R66 R66, RSVD#R64 R64

RSVD_NCTF#BT5 BT5, RSDV_NCTF#BR5 BR5 — RSVD_NCTF#BR5 — TP171

RSDV_NCTF#BV6 BV6, RSDV_NCTF#BV8 BV8

RSVD#AV69 AV69, RSVD#AK71 AK71, RSVD#AN69 AN69, RSVD#AP66 AP66, RSVD#AH66 AH66, RSVD#AK66 AK66, RSVD#AR71 AR71, RSVD#AM66 AM66, RSVD#AK69 AK69, RSVD#AU71 AU71, RSVD#AT70 AT70, RSVD#AR69 AR69, RSVD#AU69 AU69, RSVD#AT67 AT67

RSVD_TP2 AP2, RSVD_TP1 AN7 — RSVD_TP2 — RSVD_TP1 — TP4 TP7

RSVD#AV4 AV4, RSVD#AU2 AU2

RSVD#BE69 BE69, RSVD#BE71 BE71 — RSVD64 — RSVD65 — R131 0R2J-2-GP, R133 0R2J-2-GP

NCTF_DC_TEST#BV71 BV71 — DC_TEST#_BV71_69
NCTF_DC_TEST#BV69 BV69
NCTF_DC_TEST#BV68 BV68 — DC_TEST#_BV68 — R491 0R2J-2-GP
NCTF_DC_TEST#BV5 BV5 — DC_TEST#_BV5 — R381 0R2J-2-GP
NCTF_DC_TEST#BV3 BV3 — DC_TEST_BT3_BV3
NCTF_DC_TEST#BV1 BV1 — DC_TEST#_BV1_BT1
NCTF_DC_TEST#BT71 BT71 — DC_TEST_BT69_71
DC_TEST_BT69 BT69
DC_TEST_BT3 BT3
NCTF_DC_TEST#BT1 BT1
NCTF_DC_TEST#BR71 BR71 — VSS_NCTF2_R
NCTF_DC_TEST#BR1 BR1 — VSS_NCTF6_R
NCTF_DC_TEST#E71 E71 — DC_TEST#_E71 — R493 0R2J-2-GP
NCTF_DC_TEST#E1 E1
NCTF_DC_TEST#C71 C71 — DC_TEST#_C71_A71
DC_TEST_C69 C69 — DC_TEST_C69_A69
NCTF_DC_TEST#C3 C3 — DC_TEST#_C3 — R374 0R2J-2-GP
NCTF_DC_TEST#A71 A71
NCTF_DC_TEST#A69 A69
NCTF_DC_TEST#A68 A68 — VSS_NCTF1_R
NCTF_DC_TEST#A5 A5 — VSS_NCTF7_R

NCTF TEST PIN: A5, A68, A69, A71, C3, C71, E1, E71, BR1, BR71, BT1, BT71, BV1, BV3, BV5, BV68, BV69, BV71

DC_TEST#_C71_A71 — TP31
DC_TEST_BT69_71 — TP30
DC_TEST#_BV5 — TP26
DC_TEST#_C3 — TP27

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Title: Auburndale(7/8)-RESERVED

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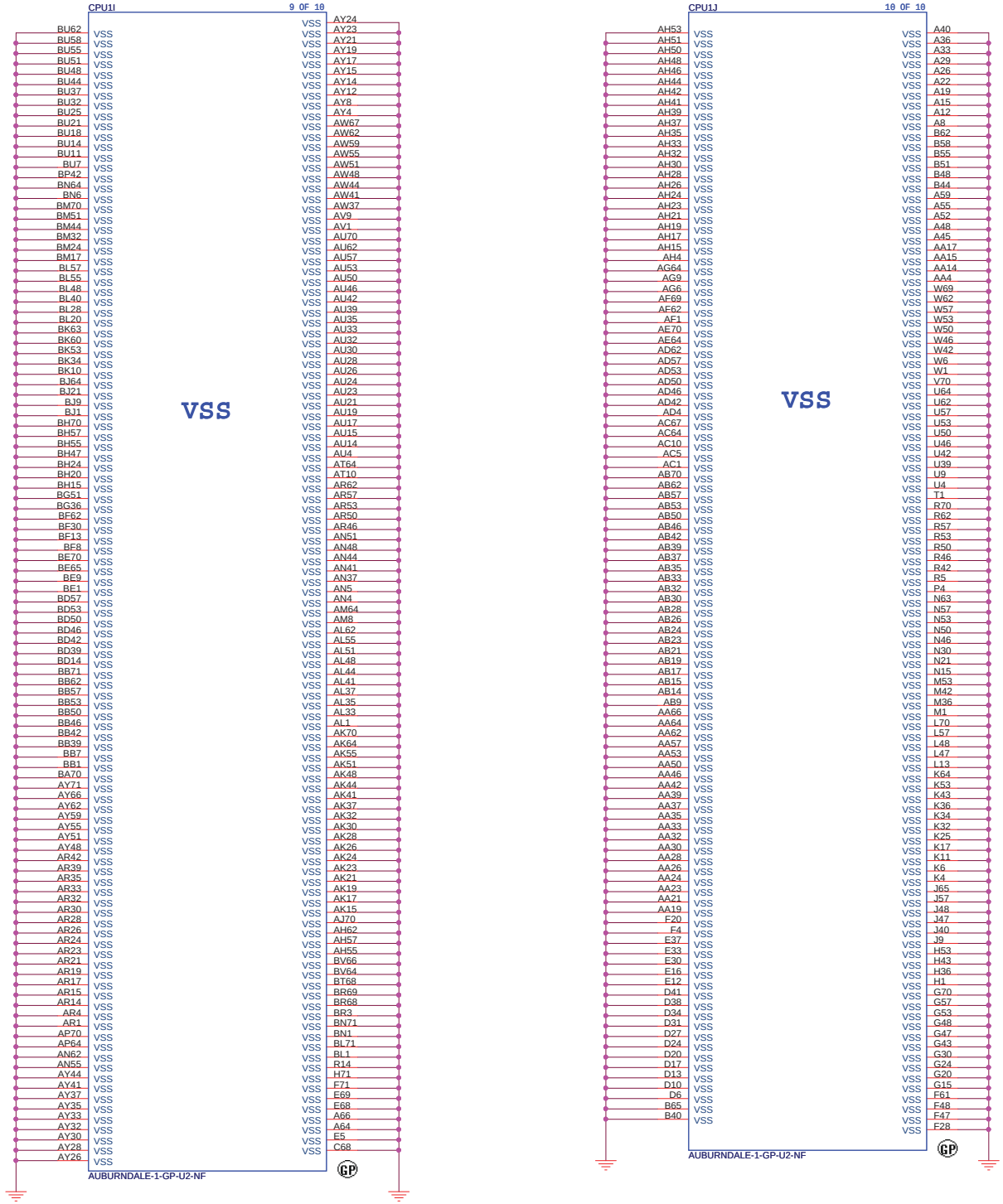

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Title

Auburndale(8/8)-VSS

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CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

H_THERMDA
C290
SC2200P50V2KX-2GP
H_THERMDC

REMOTE2-
Q10
MMBT3904WT1G-1-GP
84.M3904.D11
2nd = 84.03904.Y11
C202
SC2200P50V2KX-2GP
REMOTE2+

AMBIENT TEMP: Q24 used for GPU

REMOTE2+ and REMOTE2- routing 10mil trace width and 10 mil spacing. Lacate Cap near thermal diode .

4 WIRE PWM Fan Control circuit

+5VS
D10
1SS355GP-GP
83.00355.F1F
2nd = 83.00355.F1F
C291
SCD1U16V2ZY2GP
R516
10KR2J-3-GP
FAN1
MLX-CON4-28-GP
20.F1035.004
FAN_PWM
FAN_TACH
R515
0R2J-2-GP
FAN_PWM_C

+3VS
R166
10KR2J-3-GP
6,21 H_THRMTRIP#
R173
0R2J-2-GP
SYS_SHDN#

+3VS
R159
68R2-GP
C289
SCD1U10V2KX-4GP
+3VS_THER
R1219
10KR2J-3-GP

0630 SI1
FAN_PWM-R
FAN_PWM-R 38
C292
SCD1U16V2KX-3GP

RN12
+3VS
SRN10KJ-5-GP

U32
EMC2113-1-AP-TR-GP
VDD
DP1
DN1
DP2/DN3
ND2/DP3
SYS_SHDN#
ALERT#
SMCLK
SMDATA
PWM_IN
ADDR_SEL
TACH
PWM
TRIP_SET
SHDN_SEL
GND
GND
FAN_PWM-R
ADDR_SEL
FAN_TACH
FAN_PWM
TRIP_SET
R164
2K05R2F-GP
SHDN_SEL
H_THERMDA
H_THERMDC
REMOTE2+
REMOTE2-
21 THERM_SCI#
R165
0R2J-2-GP
SYS_SHDN#
THERM_SCI#_R
14,15,17,26,32 SMB_CLK_S3
14,15,17,26,32 SMB_DATA_S3

+5VS
AFTP43
FAN_PWM_C
AFTP39
FAN_TACH
AFTP40
AFTP41

+3VS
R170
15KR2J-1-GP
SHDN_SEL

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Title: SMSC2113 Thermal Sensor

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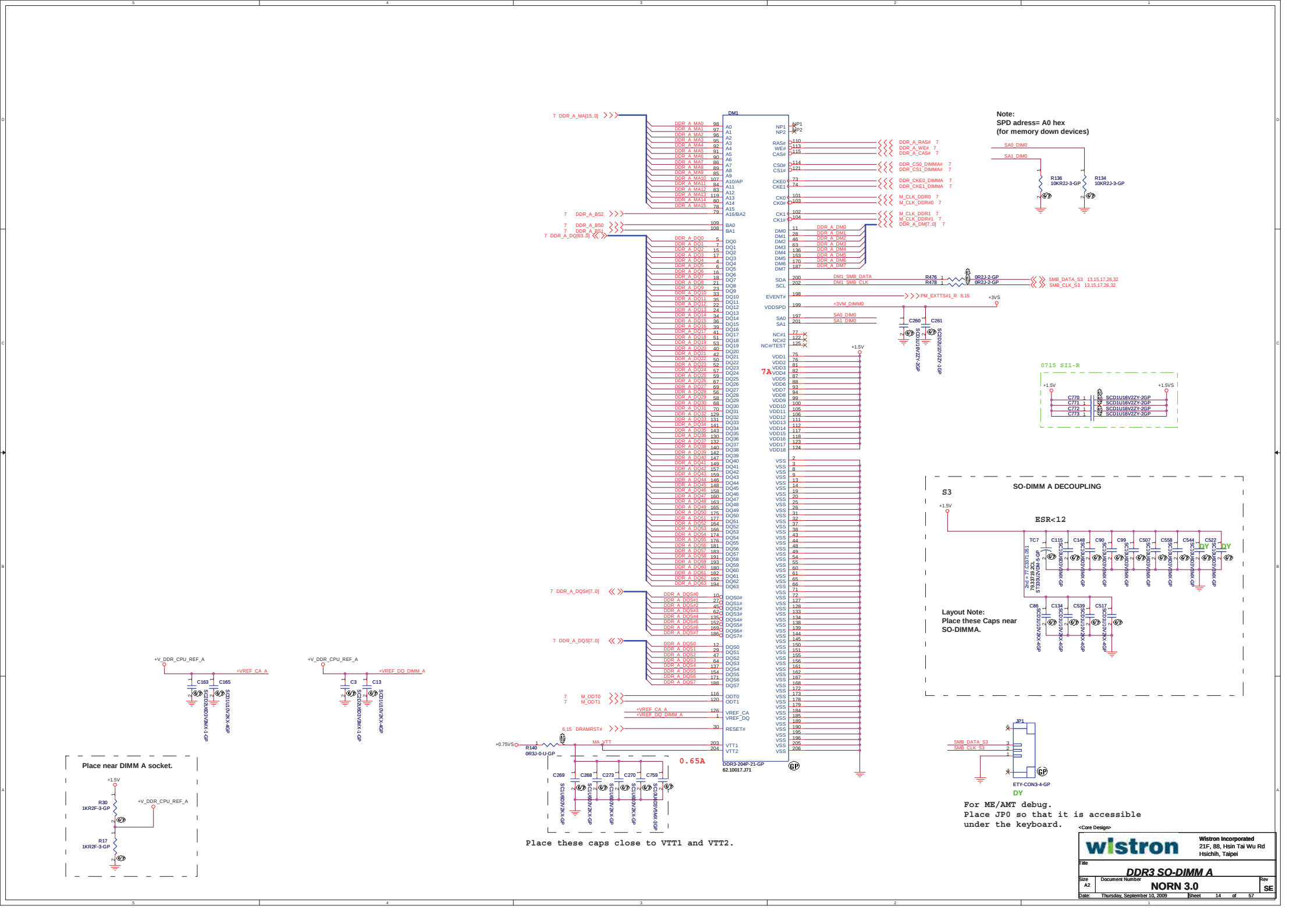
DDR3-204P-21-GP
62.10017.J71
Note:
SPD adress= A0 hex
(for memory down devices)
SA0_DIM0
SA1_DIM0
R136
10KR2J-3-GP
R134
10KR2J-3-GP
SO-DIMM A DECOUPLING
S3
+1.5V
ESR<12
Layout Note:
Place these Caps near
SO-DIMMA.
Place near DIMM A socket.
+V_DDR_CPU_REF_A
+VREF_CA_A
+VREF_DQ_DIMM_A
R30
1KR2F-3-GP
R17
1KR2F-3-GP
Place these caps close to VTT1 and VTT2.
0.65A
R140
0R3J-0-U-GP
+0.75VS
MA_VTT
DRAMRST#
JP1
ETY-CON3-4-GP
SMB_DATA_S3
SMB_CLK_S3
For ME/AMT debug.
Place JP0 so that it is accessible
under the keyboard.
0715 SI1-R
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DDR3 SO-DIMM A
NORN 3.0
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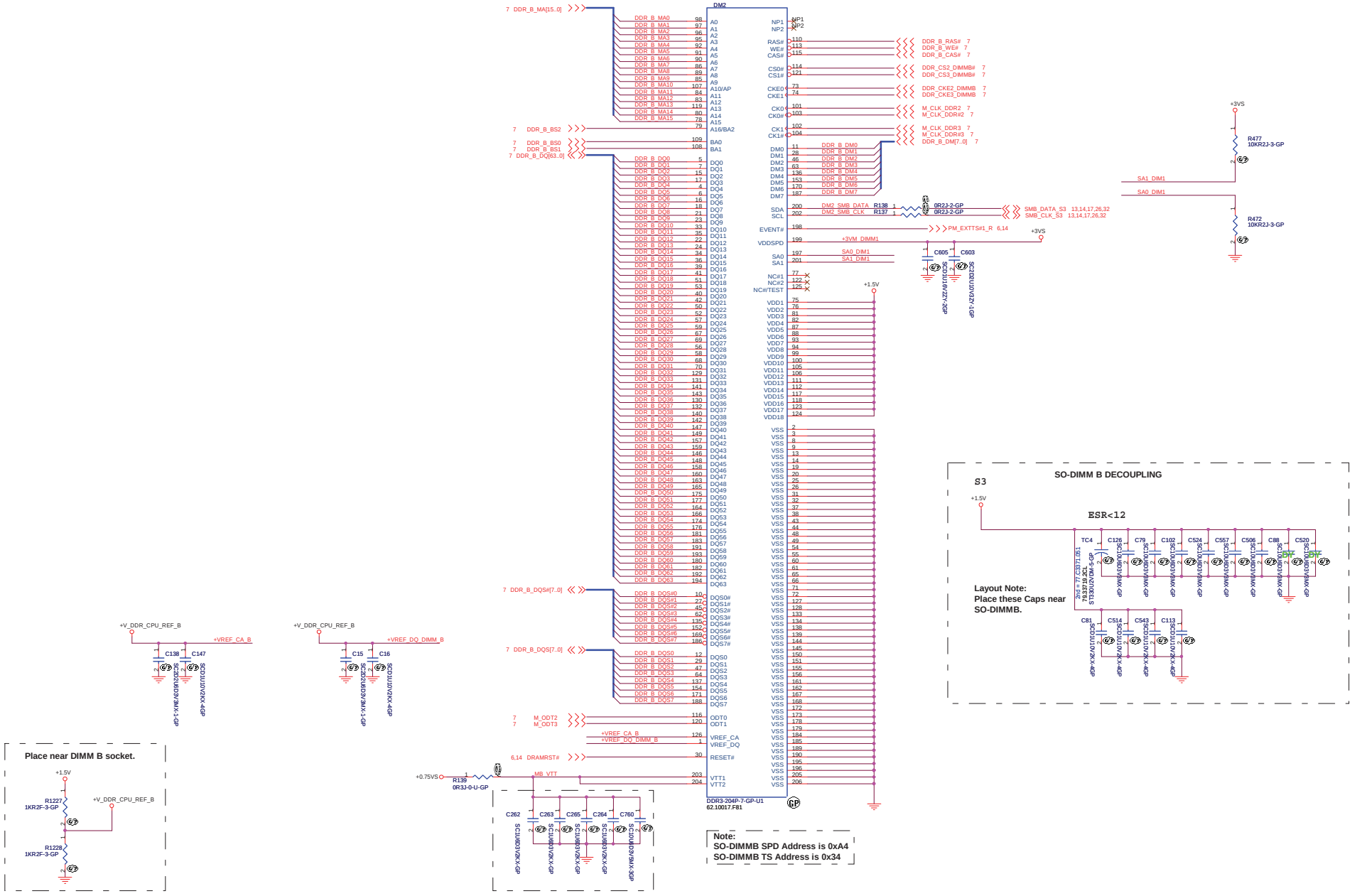

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Title: DDR3 SO-DIMM B

Size: A2 | Document Number: NORN 3.0 | Rev: SE

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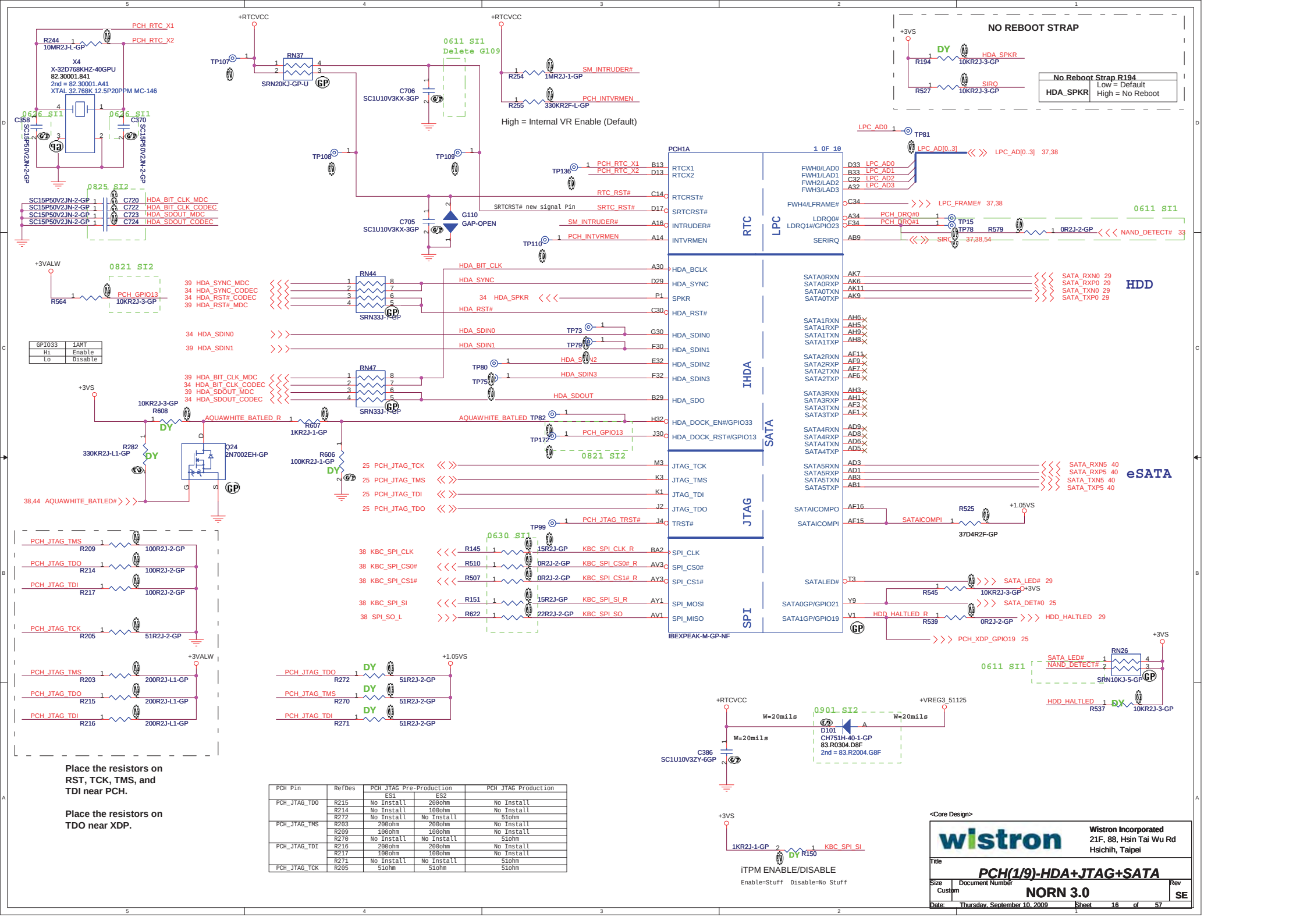
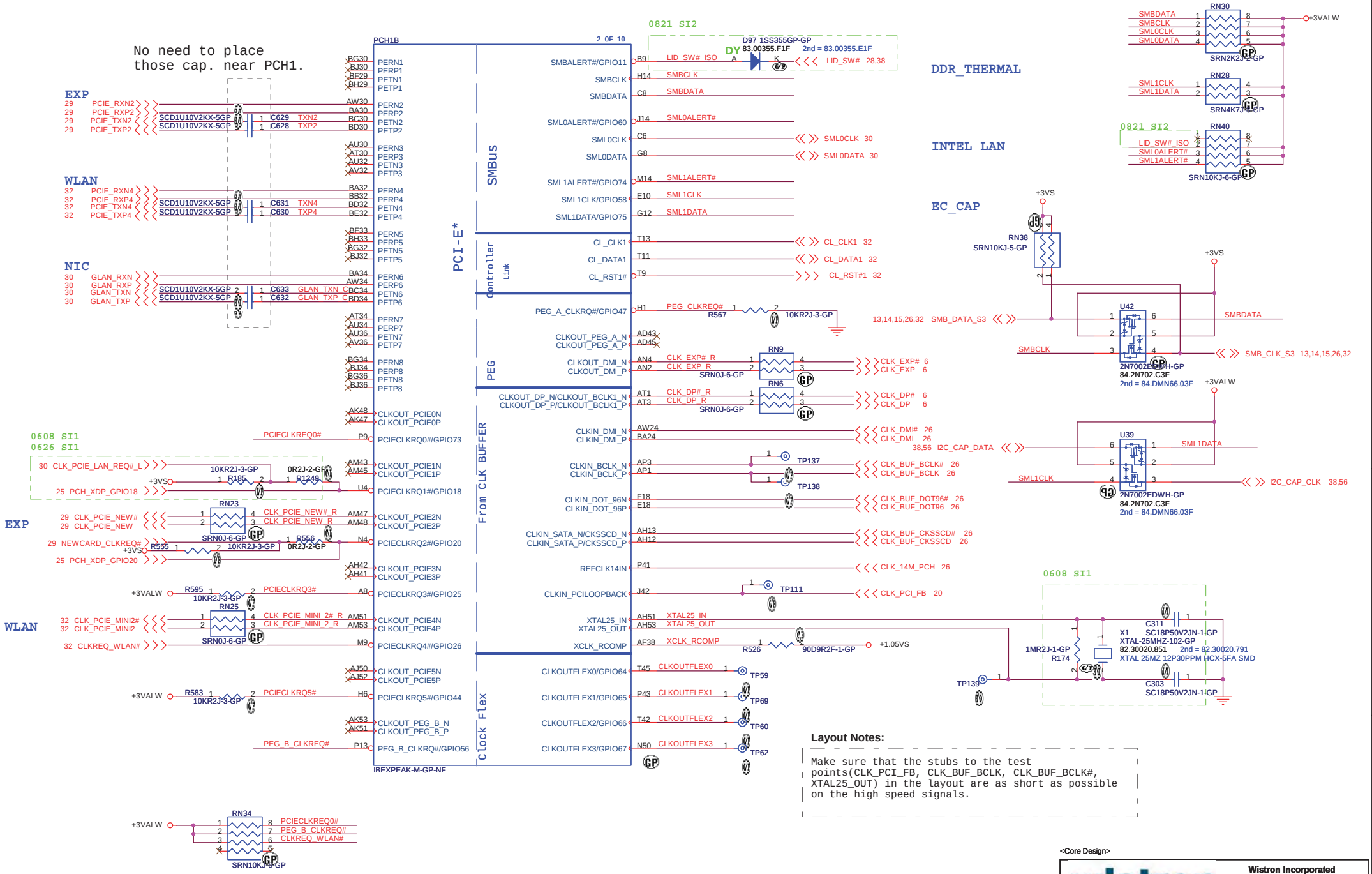


GPIO33	iAMT
Hi	Enable
Lo	Disable

PCH Pin	RefDes	PCH JTAG Pre-Production		PCH JTAG Production
		ES1	ES2	
PCH_JTAG_TDO	R215	No Install	200ohm	No Install
	R214	No Install	100ohm	No Install
	R272	No Install	No Install	51ohm
PCH_JTAG_TMS	R203	200ohm	200ohm	No Install
	R209	100ohm	100ohm	No Install
	R270	No Install	No Install	51ohm
PCH_JTAG_TDI	R216	200ohm	200ohm	No Install
	R217	100ohm	100ohm	No Install
	R271	No Install	No Install	51ohm
PCH_JTAG_TCK	R205	51ohm	51ohm	51ohm


No need to place those cap. near PCH1.
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
EXP
WLAN
NIC
0821 SI2
DDR_THERMAL
INTEL LAN
EC_CAP
0608 SI1
0626 SI1
Layout Notes:
Make sure that the stubs to the test points(CLK_PCI_FB, CLK_BUF_BCLK, CLK_BUF_BCLK#, XTAL25_OUT) in the layout are as short as possible on the high speed signals.
<Core Design>
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Title
PCH(2/9)-PCIE+SMBUS+CLK
Size A3
Document Number
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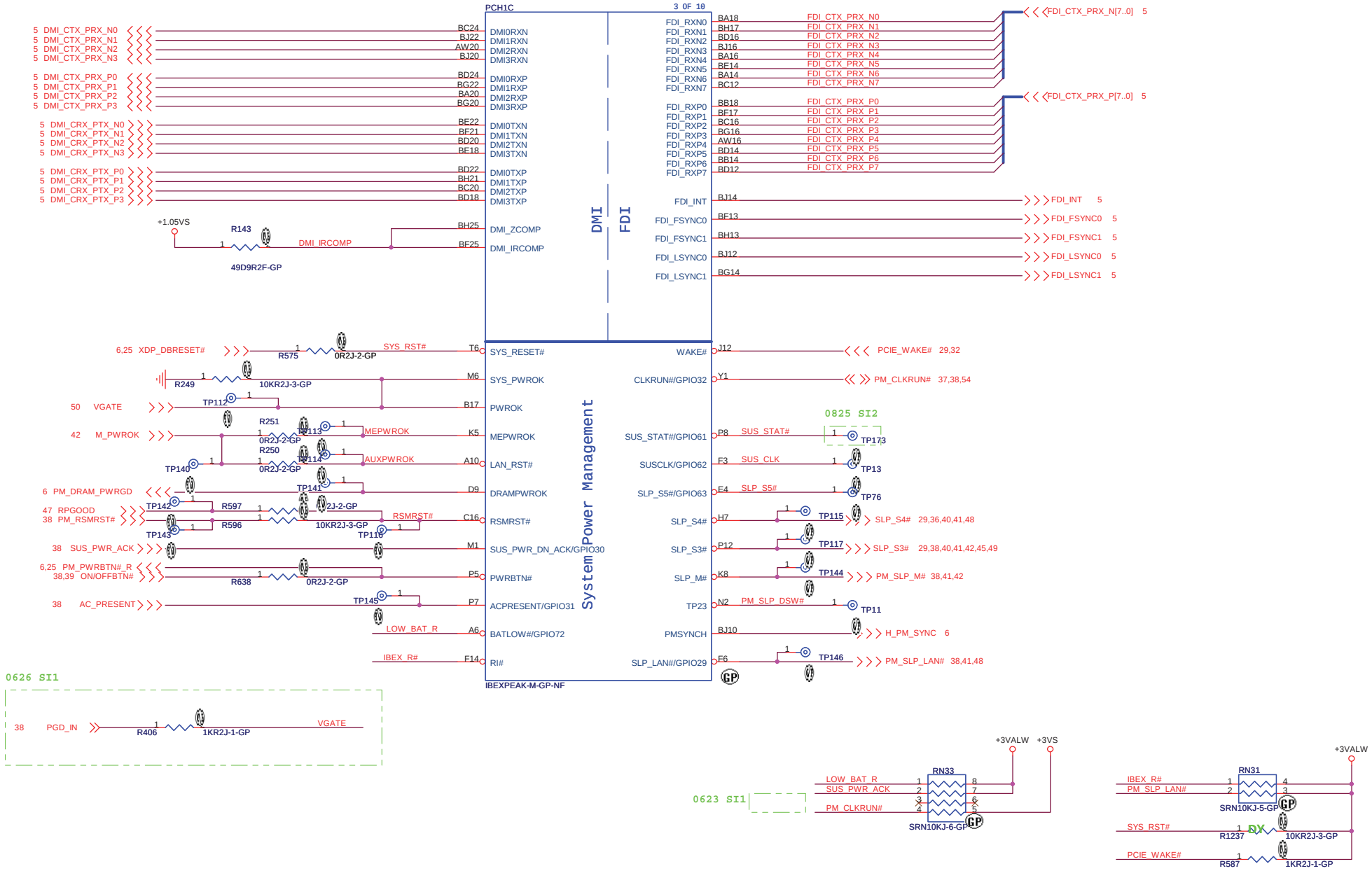

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Hsichih, Taipei

Title: PCH(3/9)-DMI+FDI+GPIO

Size: A3 | Document Number: NORN 3.0 | Rev: SE

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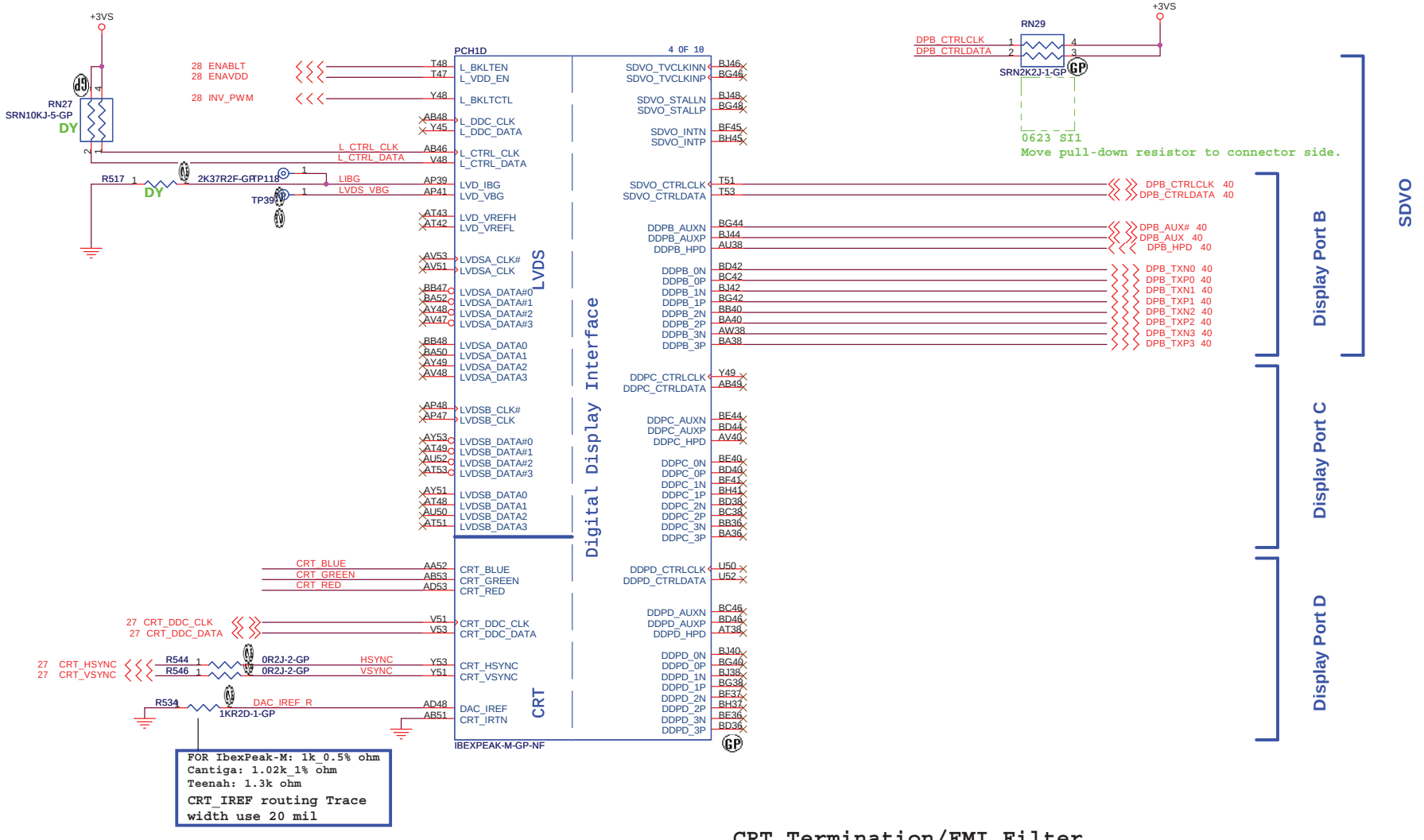

<Core Design>

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Title: PCH(4/9)-LVDS+DDI

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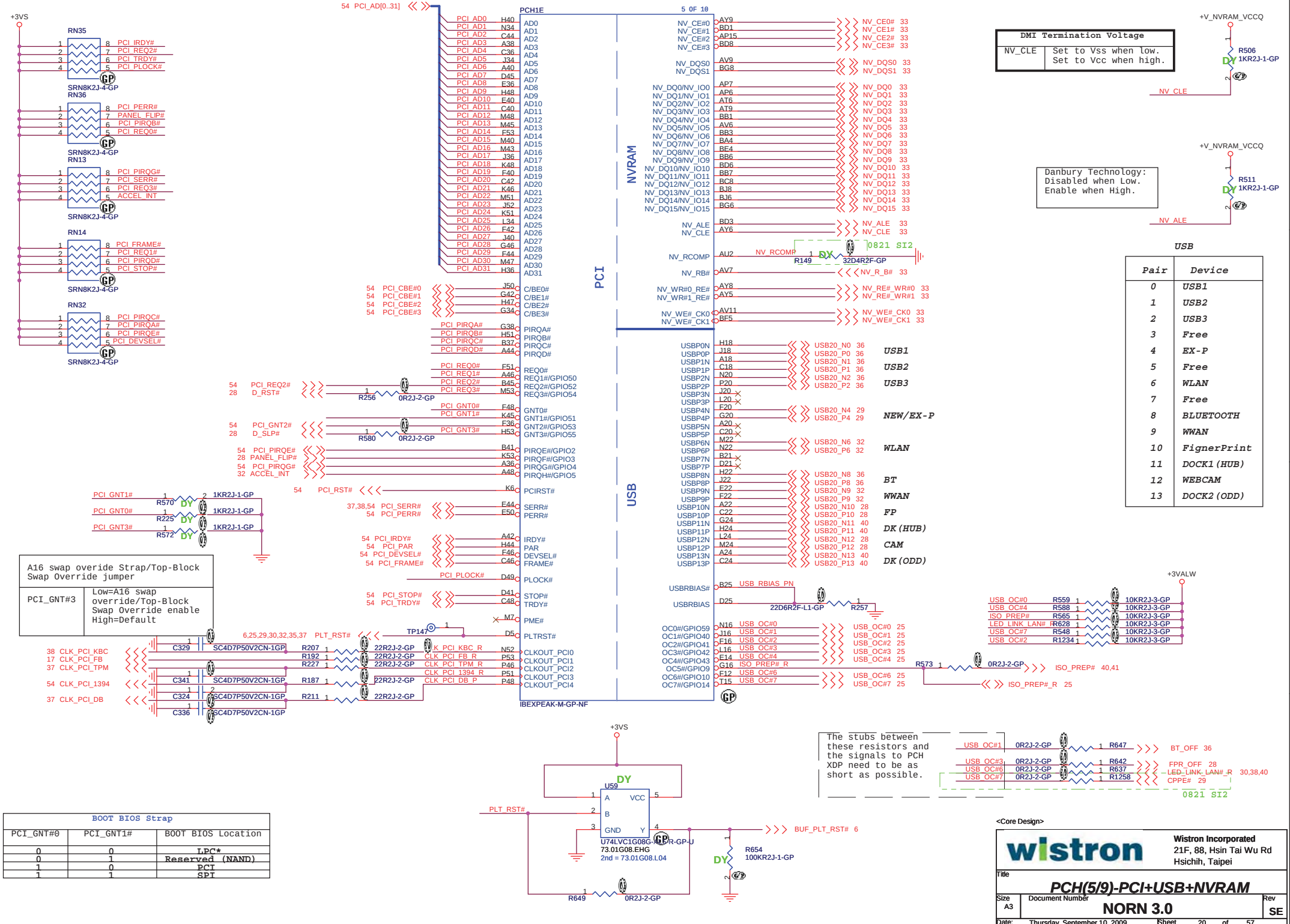
PCH1E
5 OF 10
PCI
NVRAM
USB
IBEXPEAK-M-GP-NF
SRN8K2J-4-GP
RN35
RN36
RN13
RN14
RN32
PCI_IRDY#
PCI_REQ2#
PCI_TRDY#
PCI_PLOCK#
PCI_PERR#
PANEL_FLIP#
PCI_PIRQB#
PCI_REQ0#
PCI_PIRQG#
PCI_SERR#
PCI_REQ3#
ACCEL_INT
PCI_FRAME#
PCI_REQ1#
PCI_PIRQD#
PCI_STOP#
PCI_PIRQC#
PCI_PIRQA#
PCI_PIRQE#
PCI_DEVSEL#
54 PCI_AD[0..31]
54 PCI_CBE#0
54 PCI_CBE#1
54 PCI_CBE#2
54 PCI_CBE#3
54 PCI_REQ2#
28 D_RST#
54 PCI_GNT2#
28 D_SLP#
54 PCI_PIRQE#
28 PANEL_FLIP#
54 PCI_PIRQG#
32 ACCEL_INT
54 PCI_RST#
37,38,54 PCI_SERR#
54 PCI_PERR#
54 PCI_IRDY#
54 PCI_PAR
54 PCI_DEVSEL#
54 PCI_FRAME#
PCI_PLOCK#
54 PCI_STOP#
54 PCI_TRDY#
6,25,29,30,32,35,37 PLT_RST#
TP147
38 CLK_PCI_KBC
17 CLK_PCI_FB
37 CLK_PCI_TPM
54 CLK_PCI_1394
37 CLK_PCI_DB
SC4D7P50V2CN-1GP
22R2J-2-GP
CLK_PCI_KBC_R
CLK_PCI_FB_R
CLK_PCI_TPM_R
CLK_PCI_1394_R
CLK_PCI_DB_P
CLKOUT_PCI0
CLKOUT_PCI1
CLKOUT_PCI2
CLKOUT_PCI3
CLKOUT_PCI4
PCI_GNT1#
PCI_GNT0#
PCI_GNT3#
1KR2J-1-GP
DY
NV_CE#0
NV_CE#1
NV_CE#2
NV_CE#3
NV_DQS0
NV_DQS1
NV_DQ0/NV_IO0
NV_DQ1/NV_IO1
NV_DQ2/NV_IO2
NV_DQ3/NV_IO3
NV_DQ4/NV_IO4
NV_DQ5/NV_IO5
NV_DQ6/NV_IO6
NV_DQ7/NV_IO7
NV_DQ8/NV_IO8
NV_DQ9/NV_IO9
NV_DQ10/NV_IO10
NV_DQ11/NV_IO11
NV_DQ12/NV_IO12
NV_DQ13/NV_IO13
NV_DQ14/NV_IO14
NV_DQ15/NV_IO15
NV_ALE
NV_CLE
NV_RCOMP
NV_RB#
NV_WR#0_RE#
NV_WR#1_RE#
NV_WE#_CK0
NV_WE#_CK1
NV_CE0# 33
NV_CE1# 33
NV_CE2# 33
NV_CE3# 33
NV_DQS0 33
NV_DQS1 33
NV_DQ0 33
NV_DQ1 33
NV_DQ2 33
NV_DQ3 33
NV_DQ4 33
NV_DQ5 33
NV_DQ6 33
NV_DQ7 33
NV_DQ8 33
NV_DQ9 33
NV_DQ10 33
NV_DQ11 33
NV_DQ12 33
NV_DQ13 33
NV_DQ14 33
NV_DQ15 33
NV_ALE 33
NV_CLE 33
NV_R_B# 33
NV_RE#_WR#0 33
NV_RE#_WR#1 33
NV_WE#_CK0 33
NV_WE#_CK1 33
R149
32D4R2F-GP
0821 SI2
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
USBP12N
USBP12P
USBP13N
USBP13P
USB20_N0 36
USB20_P0 36
USB20_N1 36
USB20_P1 36
USB20_N2 36
USB20_P2 36
USB20_N4 29
USB20_P4 29
USB20_N6 32
USB20_P6 32
USB20_N8 36
USB20_P8 36
USB20_N9 32
USB20_P9 32
USB20_N10 28
USB20_P10 28
USB20_N11 40
USB20_P11 40
USB20_N12 28
USB20_P12 28
USB20_N13 40
USB20_P13 40
USB1
USB2
USB3
NEW/EX-P
WLAN
BT
WWAN
FP
DK(HUB)
CAM
DK(ODD)
USBRBIAS#
USBRBIAS
USB_RBIAS_PN
22D6R2F-L1-GP
R257
OC0#/GPIO59
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO9
OC6#/GPIO10
OC7#/GPIO14
USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
ISO_PREP#_R
USB_OC#6
USB_OC#7
R573
0R2J-2-GP
ISO_PREP# 40,41
ISO_PREP#_R 25
+3VALW
USB_OC#0 R559
USB_OC#4 R588
ISO_PREP# R565
LED_LINK_LAN#_R R628
USB_OC#7 R548
USB_OC#2 R1234
10KR2J-3-GP
DMI Termination Voltage
NV_CLE
Set to Vss when low.
Set to Vcc when high.
+V_NVRAM_VCCQ
R506
1KR2J-1-GP
NV_CLE
Danbury Technology:
Disabled when Low.
Enable when High.
R511
NV_ALE
USB
Pair
Device
0 USB1
1 USB2
2 USB3
3 Free
4 EX-P
5 Free
6 WLAN
7 Free
8 BLUETOOTH
9 WWAN
10 FignerPrint
11 DOCK1(HUB)
12 WEBCAM
13 DOCK2(ODD)
A16 swap overide Strap/Top-Block
Swap Override jumper
PCI_GNT#3
Low=A16 swap override/Top-Block Swap Override enable
High=Default
BOOT BIOS Strap
PCI_GNT#0
PCI_GNT1#
BOOT BIOS Location
0 0 LPC*
0 1 Reserved (NAND)
1 0 PCI
1 1 SPI
+3VS
U59
U74LVC1G08G-AL5-R-GP-U
73.01G08.EHG
2nd = 73.01G08.L04
PLT_RST#
BUF_PLT_RST# 6
R654
100KR2J-1-GP
R649
The stubs between these resistors and the signals to PCH XDP need to be as short as possible.
USB_OC#1
USB_OC#3
USB_OC#6
USB_OC#7
R647
R642
R637
R1258
BT_OFF 36
FPR_OFF 28
LED_LINK_LAN#_R 30,38,40
CPPE# 29
0821 SI2
<Core Design>
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Hsichih, Taipei
Title
PCH(5/9)-PCI+USB+NVRAM
Size A3
Document Number
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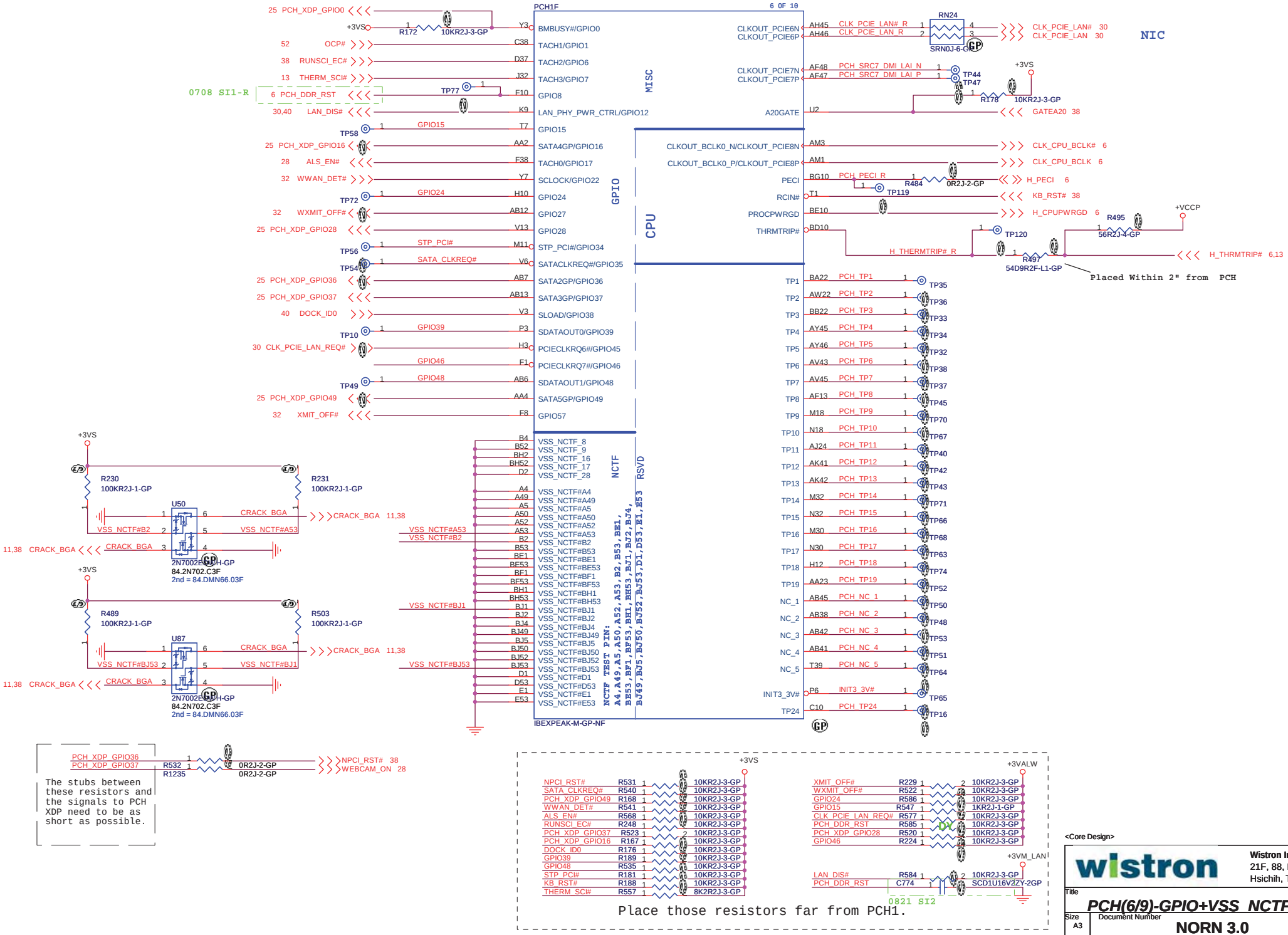

<Core Design>

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Title

PCH(6/9)-GPIO+VSS_NCTF+RSVD

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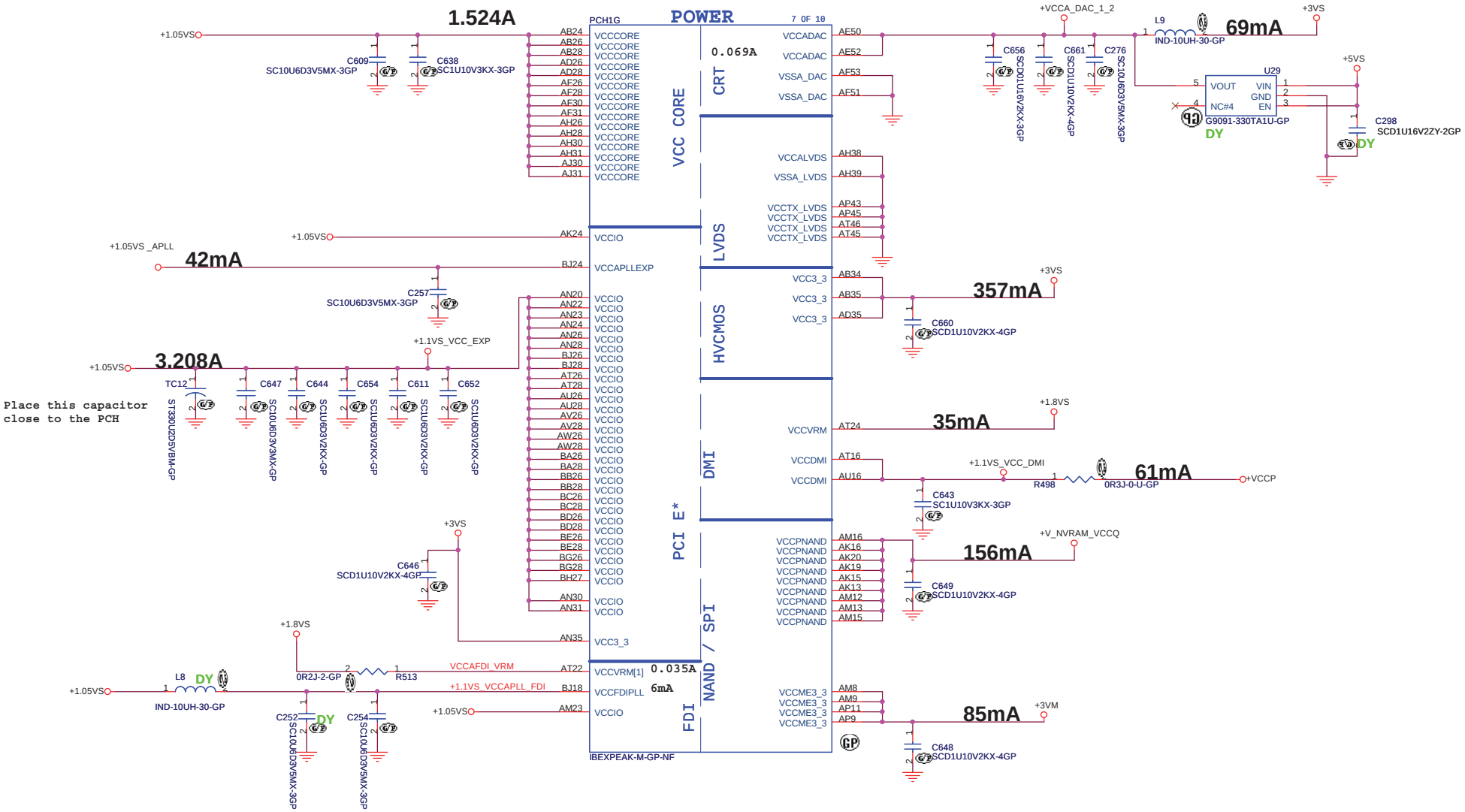

<Core Design>

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Title: PCH(7/9)-POWER

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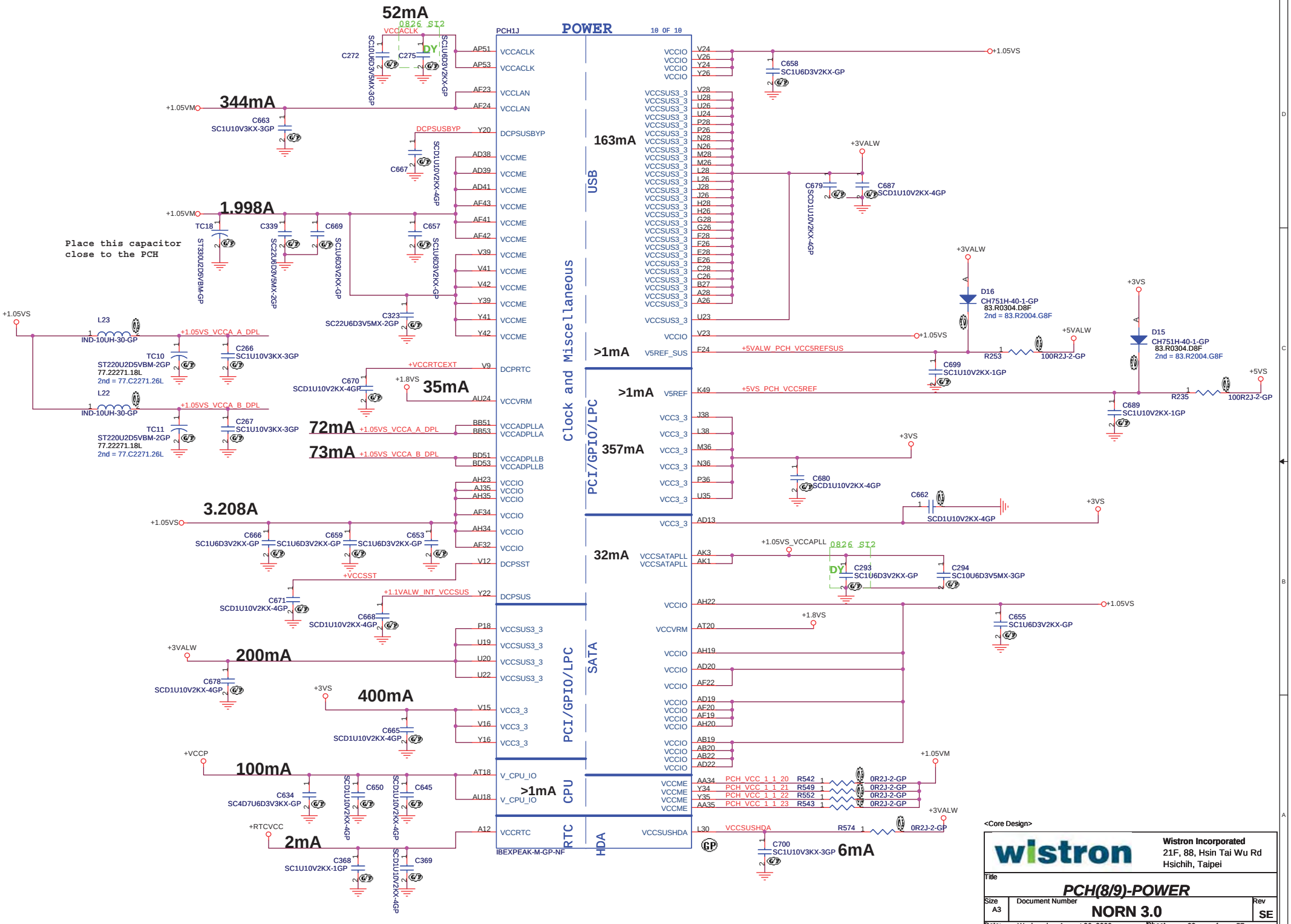
POWER
PCH1J
10 OF 10
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
52mA
344mA
1.998A
163mA
>1mA
>1mA
35mA
72mA
73mA
357mA
3.208A
32mA
200mA
400mA
100mA
>1mA
2mA
6mA
Place this capacitor close to the PCH
IBEXPEAK-M-GP-NF
<Core Design>
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Hsichih, Taipei
Title
PCH(8/9)-POWER
Size A3
Document Number
NORN 3.0
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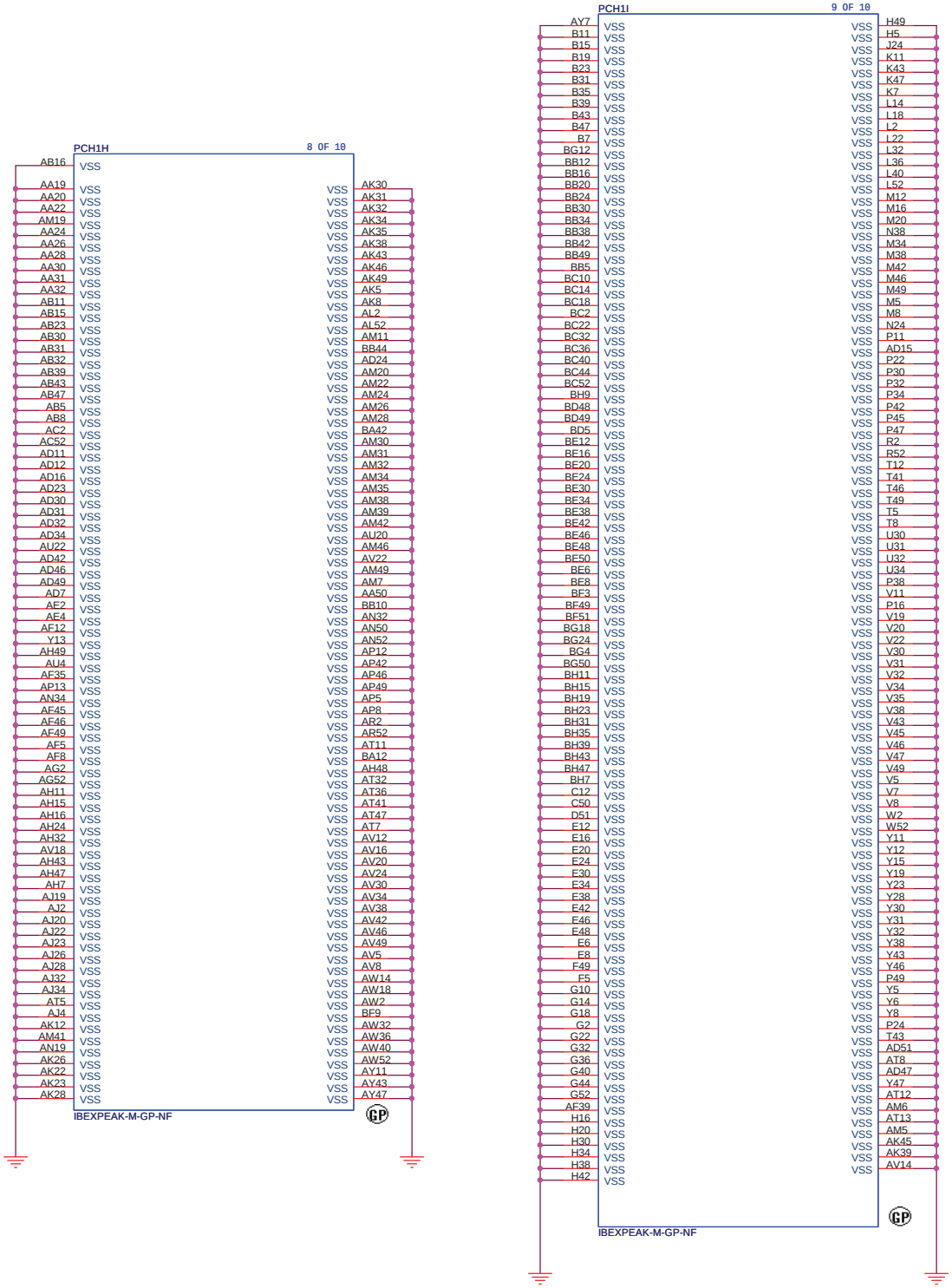

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Title: PCH(9/9)-GND

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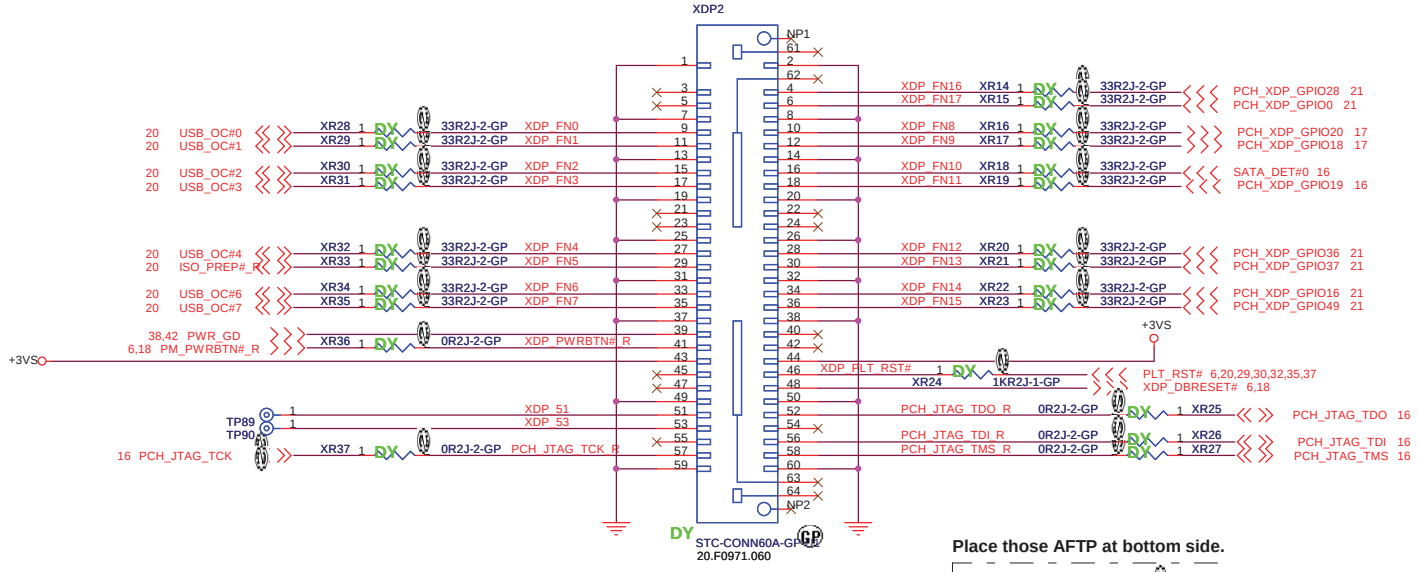
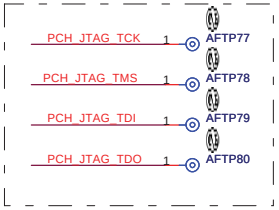
0626 SI1
Remove XDP2 and relative circuits.
0711 SI1-R
Add back.



Place those AFTP at bottom side.



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Title: PCH XDP

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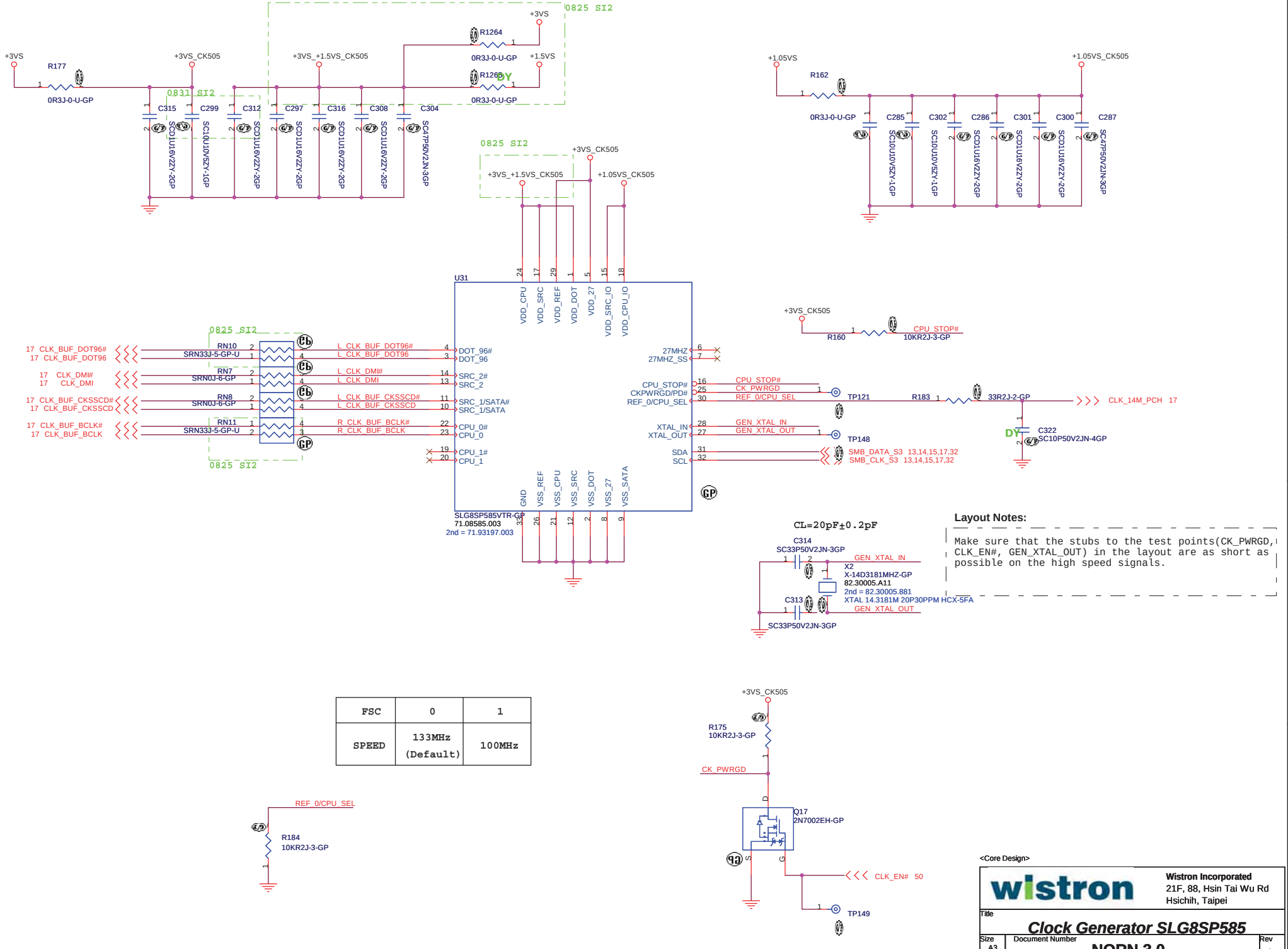
0825 SI2
+3VS
R1264
0R3J-0-U-GP
+1.5VS
R1265
DY
0831 SI2
+3VS_CK505
+3VS_+1.5VS_CK505
R177
C315
C299
C312
C297
C316
C308
C304
SCD1U16V2ZY-2GP
SC10U10V5ZY-1GP
SC47P50V2JN-3GP
+1.05VS
+1.05VS_CK505
R162
C285
C302
C286
C301
C300
C287
U31
VDD_CPU
VDD_SRC
VDD_REF
VDD_DOT
VDD_27
VDD_SRC_IO
VDD_CPU_IO
GND
VSS_REF
VSS_CPU
VSS_SRC
VSS_DOT
VSS_27
VSS_SATA
SLG8SP585VTR-GP
71.08585.003
2nd = 71.93197.003
RN10
SRN33J-5-GP-U
RN7
SRN0J-6-GP
RN8
RN11
17 CLK_BUF_DOT96#
17 CLK_BUF_DOT96
17 CLK_DMI#
17 CLK_DMI
17 CLK_BUF_CKSSCD#
17 CLK_BUF_CKSSCD
17 CLK_BUF_BCLK#
17 CLK_BUF_BCLK
L_CLK_BUF_DOT96#
L_CLK_BUF_DOT96
L_CLK_DMI#
L_CLK_DMI
L_CLK_BUF_CKSSCD#
L_CLK_BUF_CKSSCD
R_CLK_BUF_BCLK#
R_CLK_BUF_BCLK
DOT_96#
DOT_96
SRC_2#
SRC_2
SRC_1/SATA#
SRC_1/SATA
CPU_0#
CPU_0
CPU_1#
CPU_1
27MHZ
27MHZ_SS
CPU_STOP#
CKPWRGD/PD#
REF_0/CPU_SEL
XTAL_IN
XTAL_OUT
SDA
SCL
R160
10KR2J-3-GP
CK_PWRGD
TP121
R183
33R2J-2-GP
CLK_14M_PCH 17
GEN_XTAL_IN
GEN_XTAL_OUT
TP148
C322
SC10P50V2JN-4GP
SMB_DATA_S3 13,14,15,17,32
SMB_CLK_S3 13,14,15,17,32
CL=20pF±0.2pF
C314
SC33P50V2JN-3GP
X2
X-14D3181MHZ-GP
82.30005.A11
2nd = 82.30005.881
XTAL 14.3181M 20P30PPM HCX-5FA
C313
Layout Notes:
Make sure that the stubs to the test points(CK_PWRGD, CLK_EN#, GEN_XTAL_OUT) in the layout are as short as possible on the high speed signals.
FSC
0
1
SPEED
133MHz (Default)
100MHz
REF_0/CPU_SEL
R184
10KR2J-3-GP
R175
10KR2J-3-GP
Q17
2N7002EH-GP
CLK_EN# 50
TP149
<Core Design>
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Hsichih, Taipei
Title
Clock Generator SLG8SP585
Size A3
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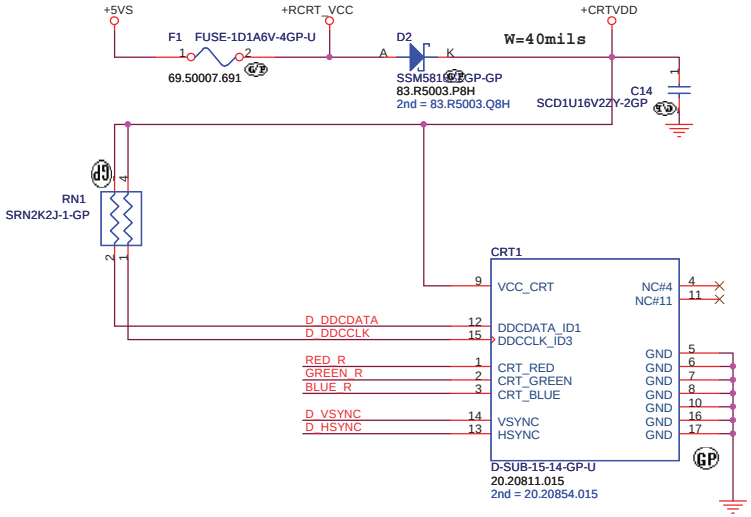
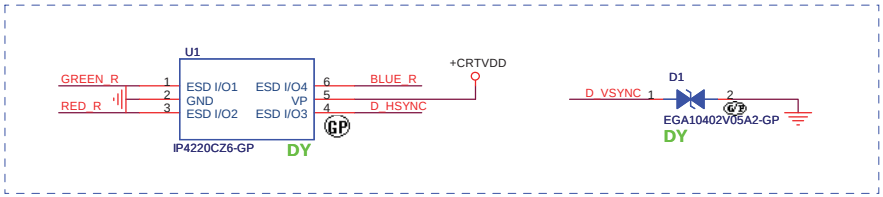
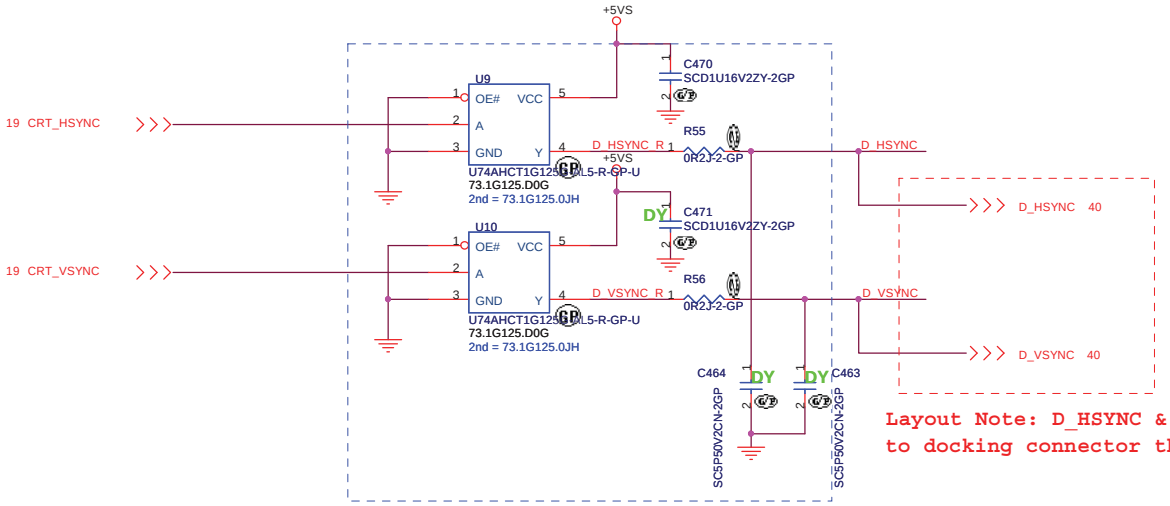
CRT connector



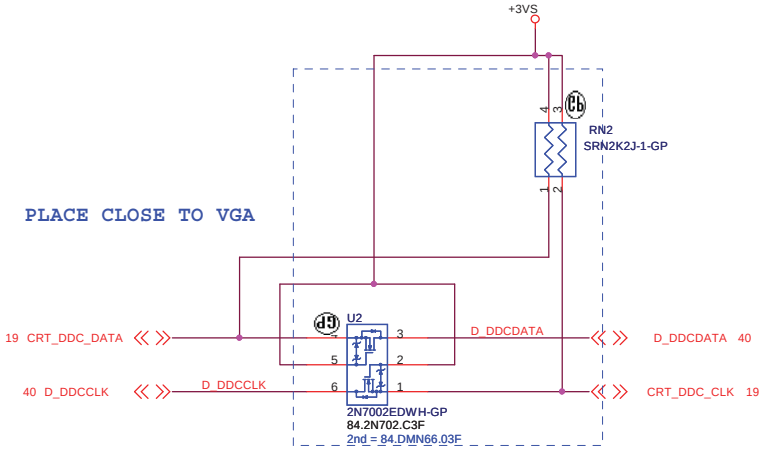


Place near the CRT connector



PLACE CLOSE TO VGA

Layout Note: D_HSYNC & D_VSYNC should be routed to docking connector then to VGA connector



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Title: CRT/TV CONNECTOR

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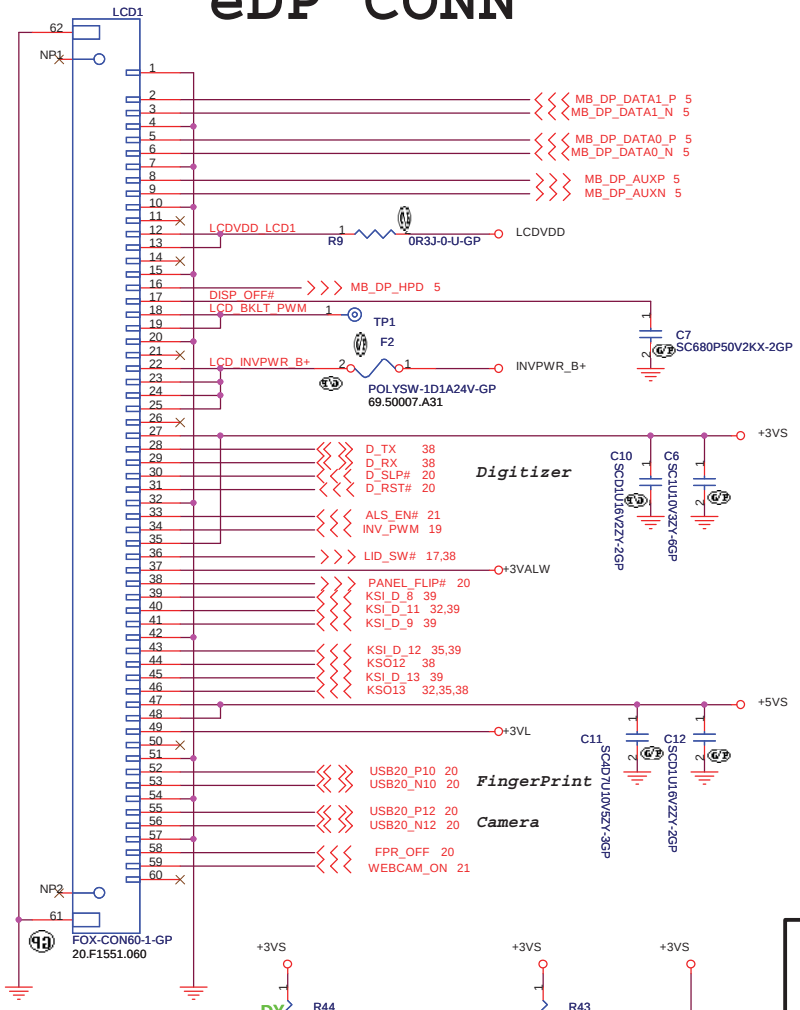
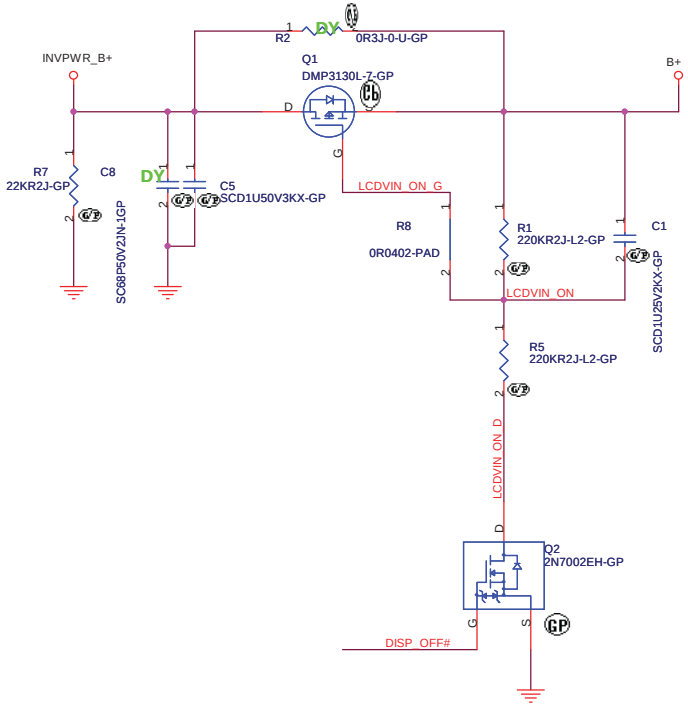
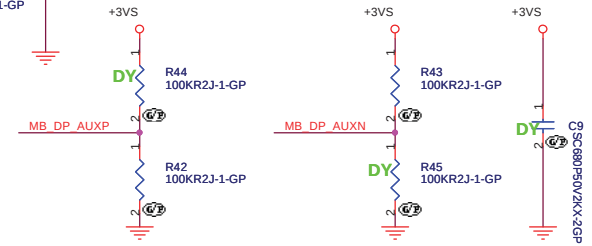
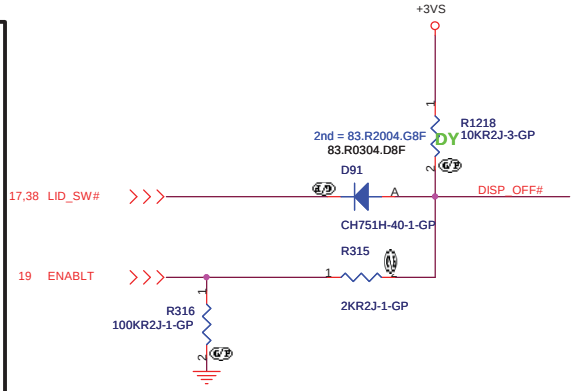
eDP CONN







LCD POWER CIRCUIT



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Hsichih, Taipei

Title: LCD CONN.

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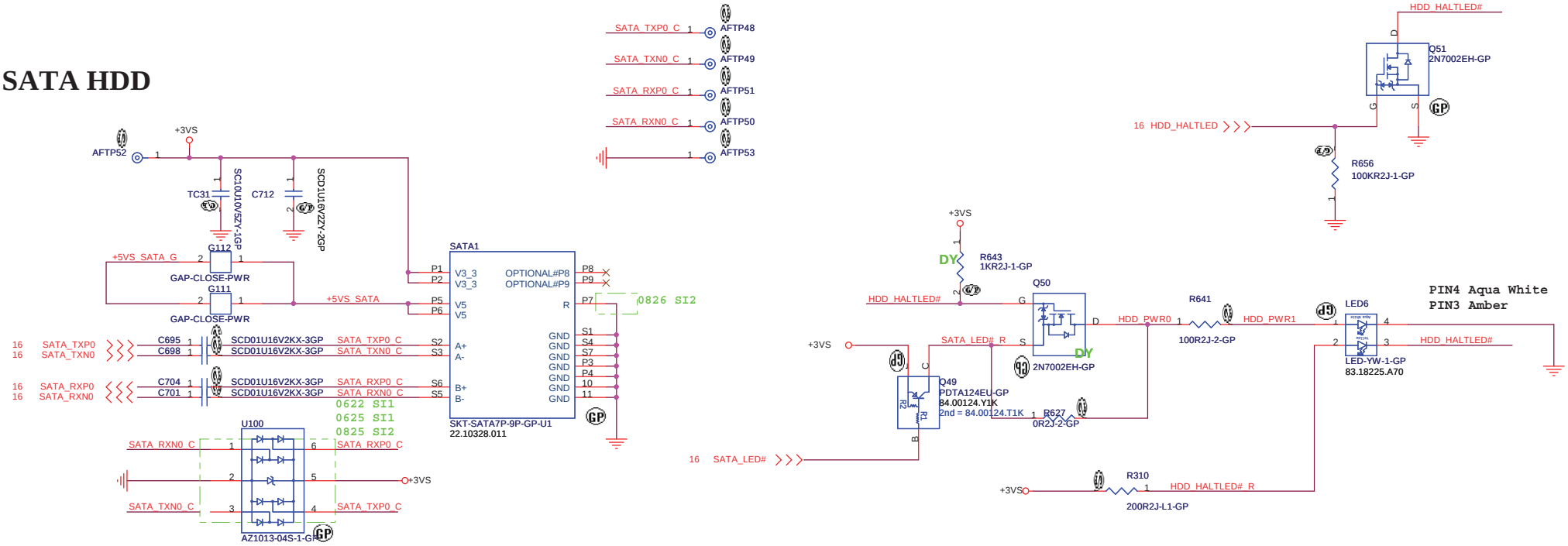
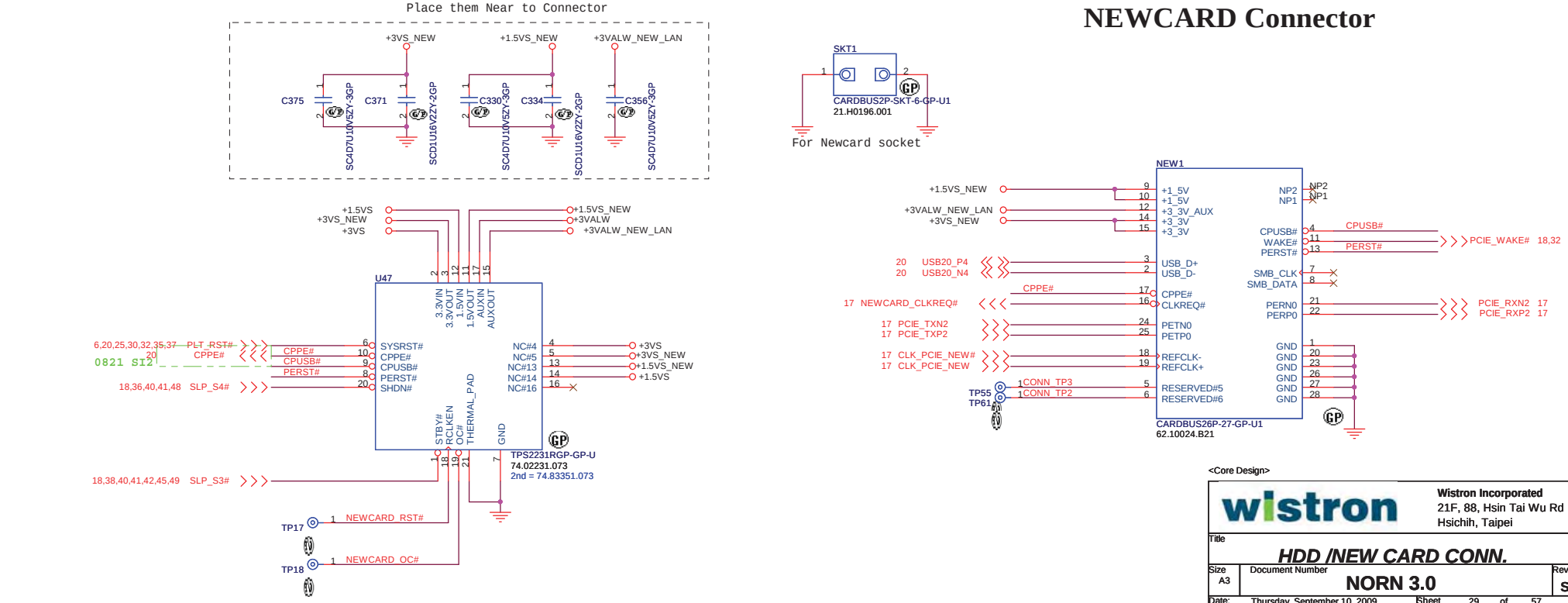
SATA HDD



NEWCARD Connector



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Title: HDD /NEW CARD CONN.

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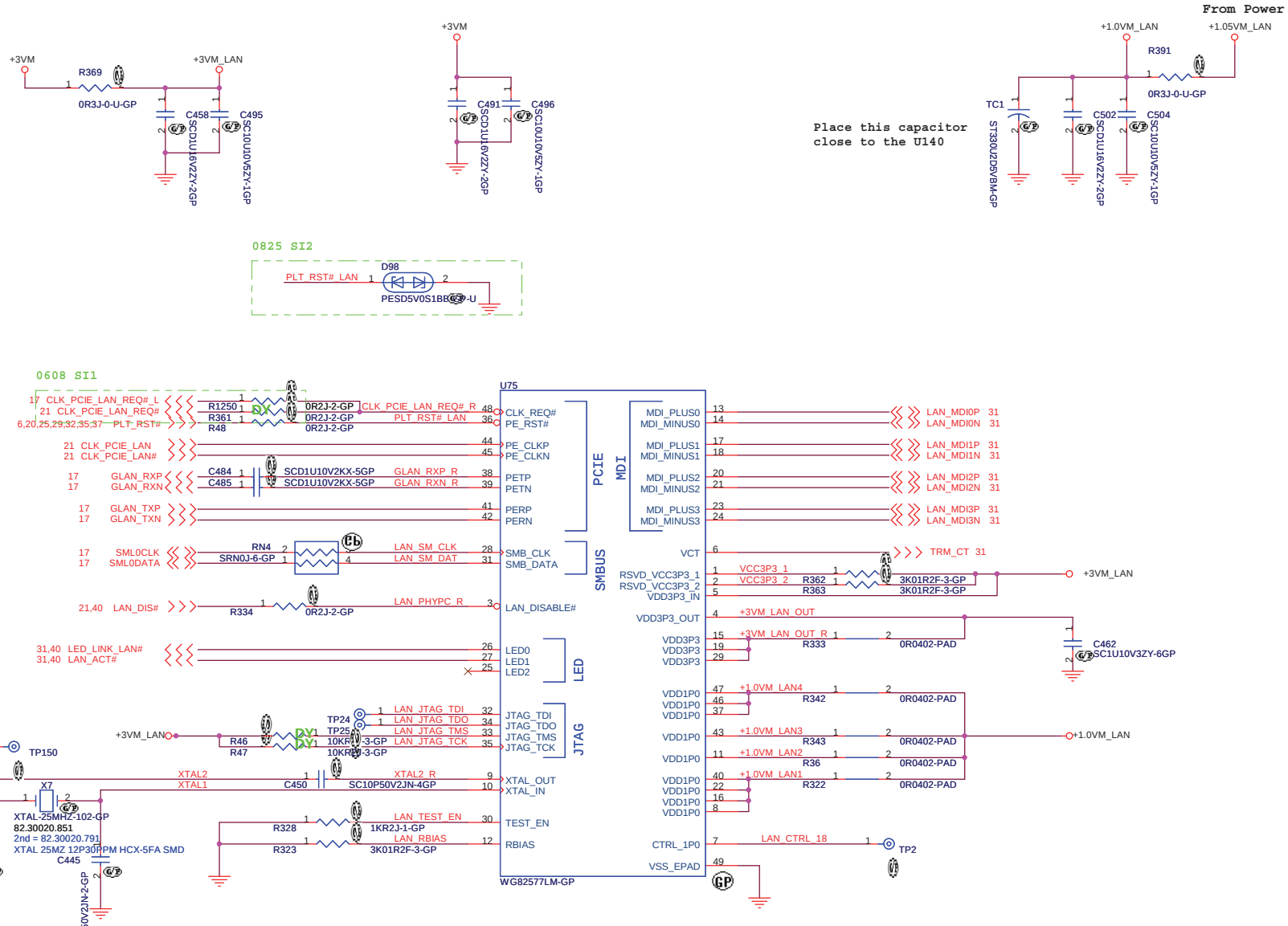

Layout Notes:

Make sure that the stubs to the test points(XTAL2) in the layout are as short as possible on the high speed signals.

<Core Design>

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Hsichih, Taipei

Title: *Intel 82577 Bavoz*

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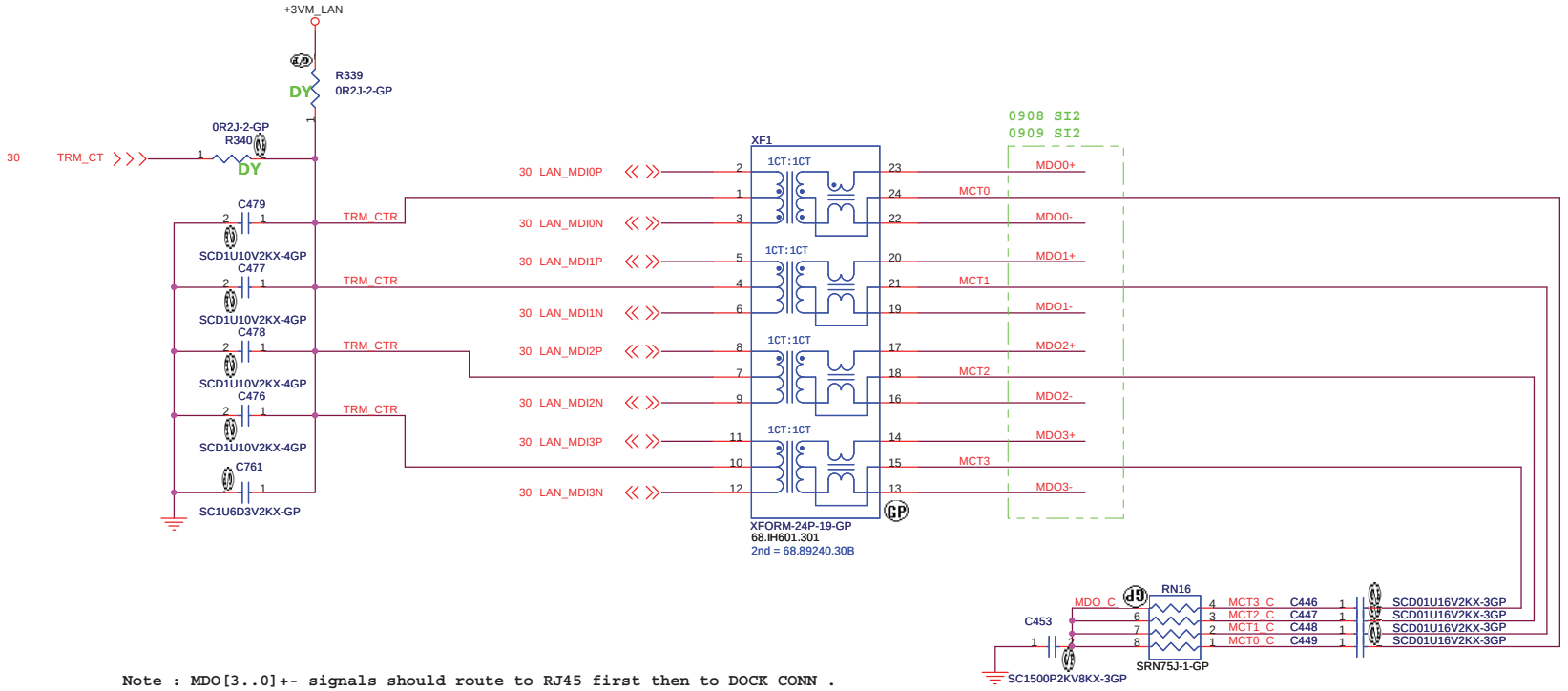
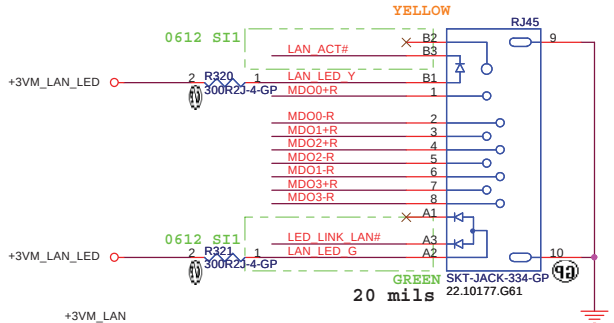
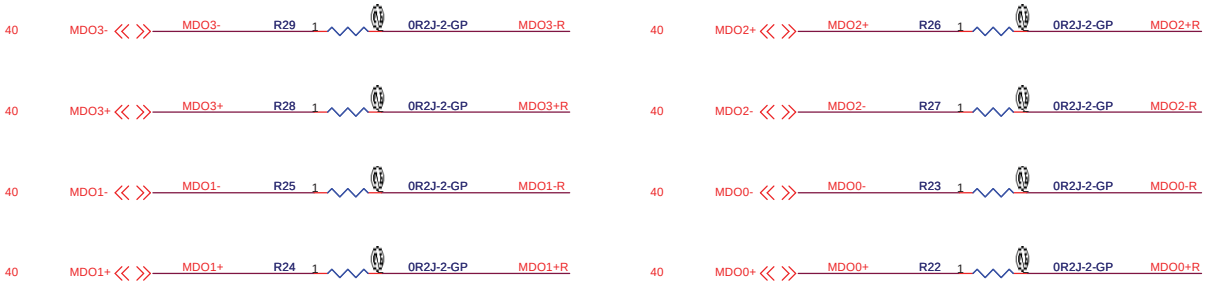
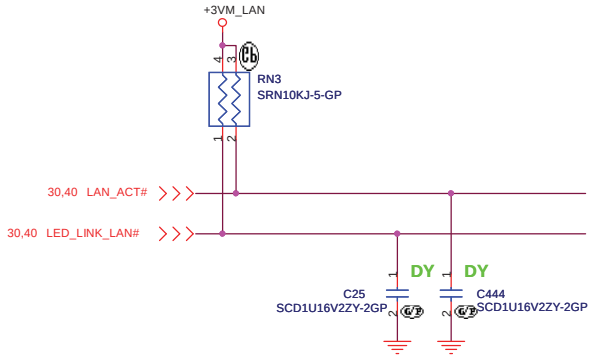
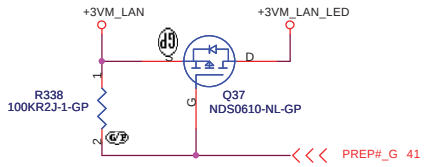


Note : MDO[3..0]+- signals should route to RJ45 first then to DOCK CONN .









<Core Design>

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Hsichih, Taipei

Title: Magnetic & RJ45

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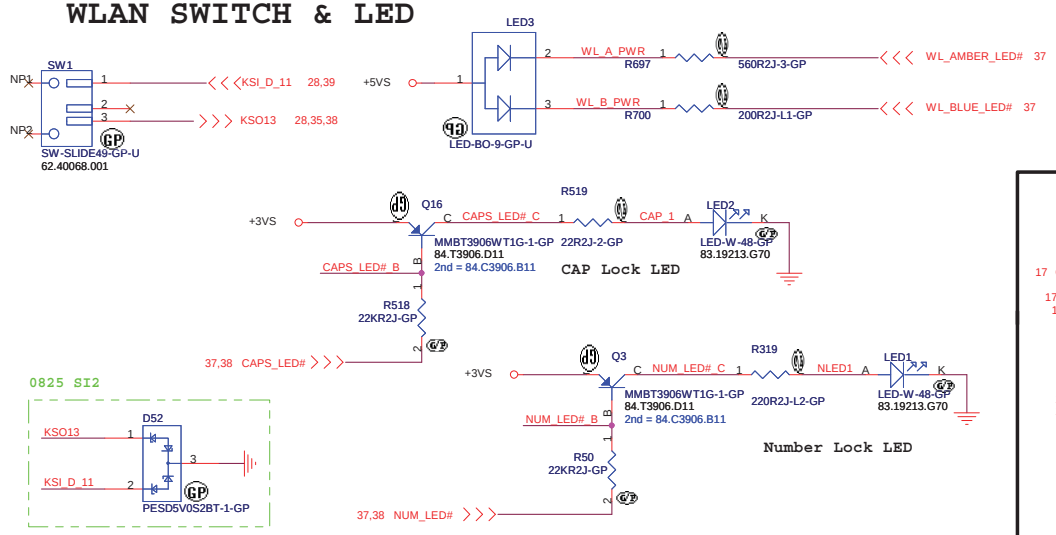
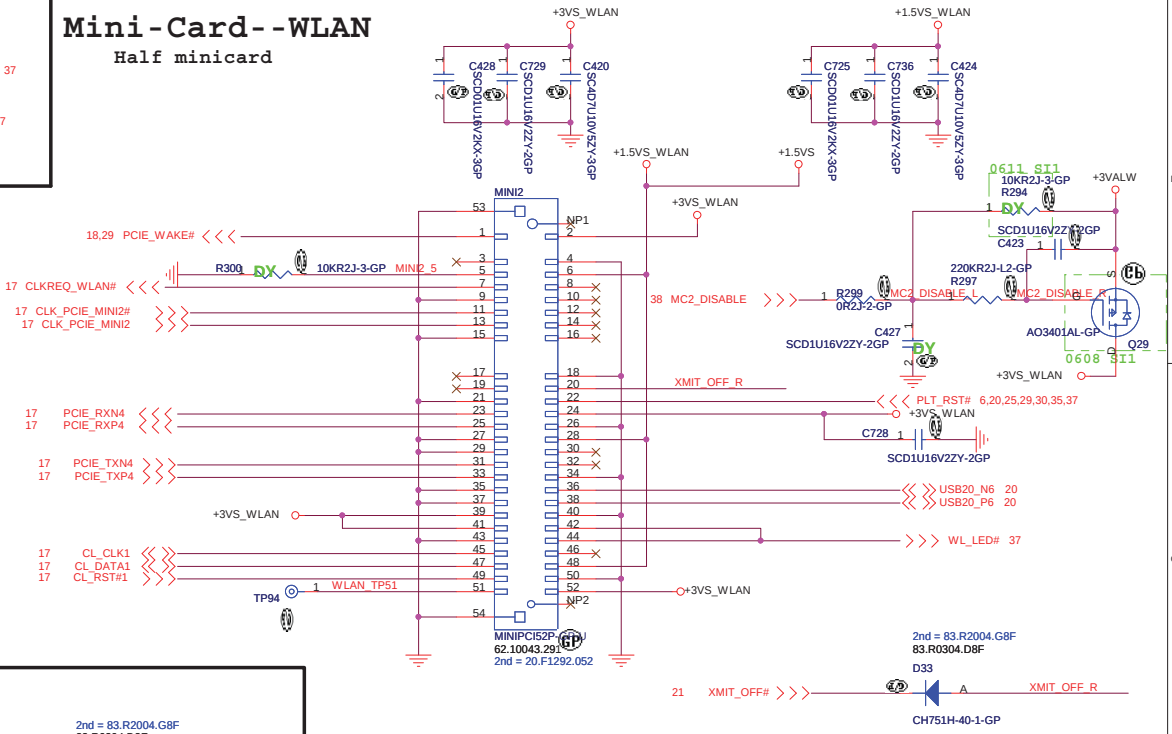
WLAN SWITCH & LED



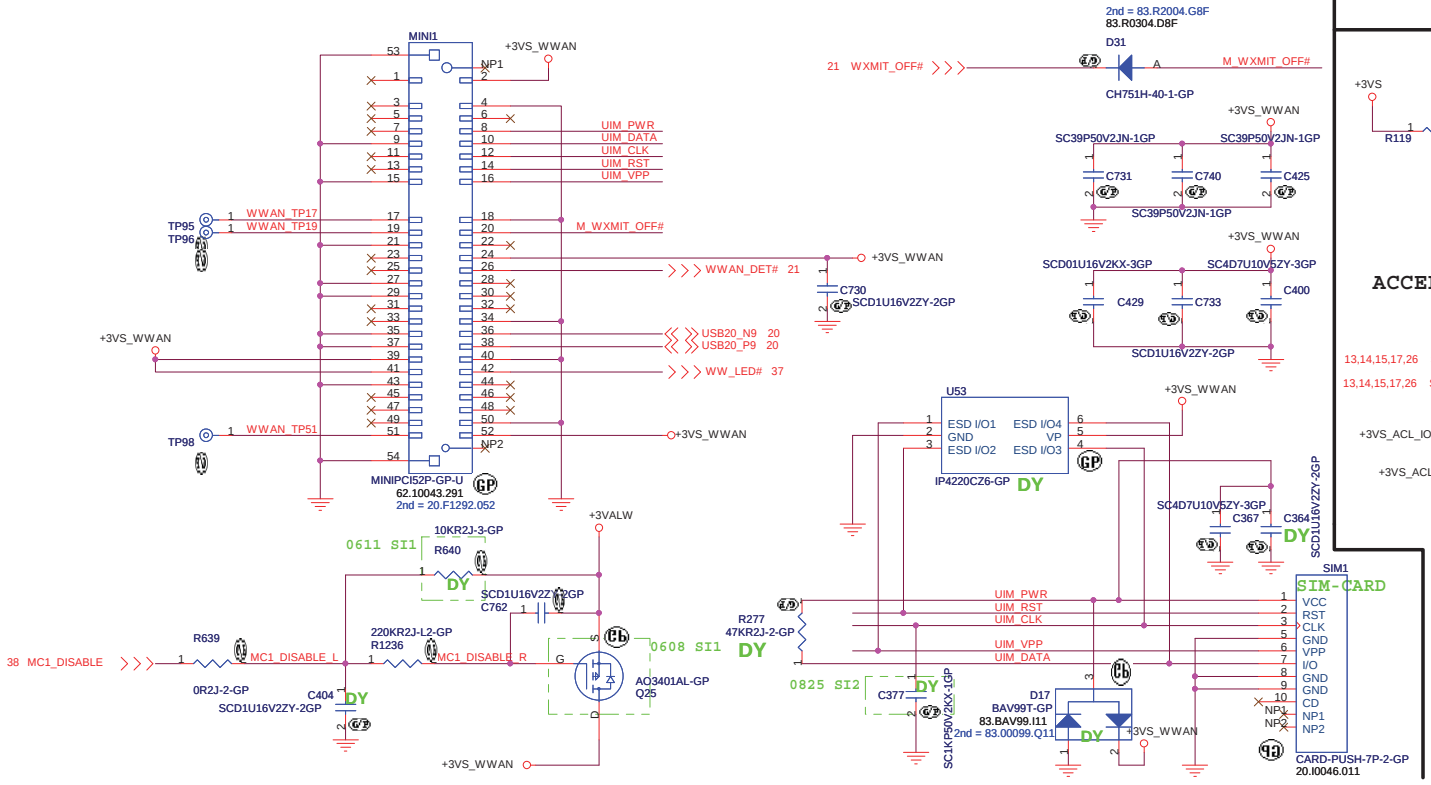
Mini-Card--WLAN

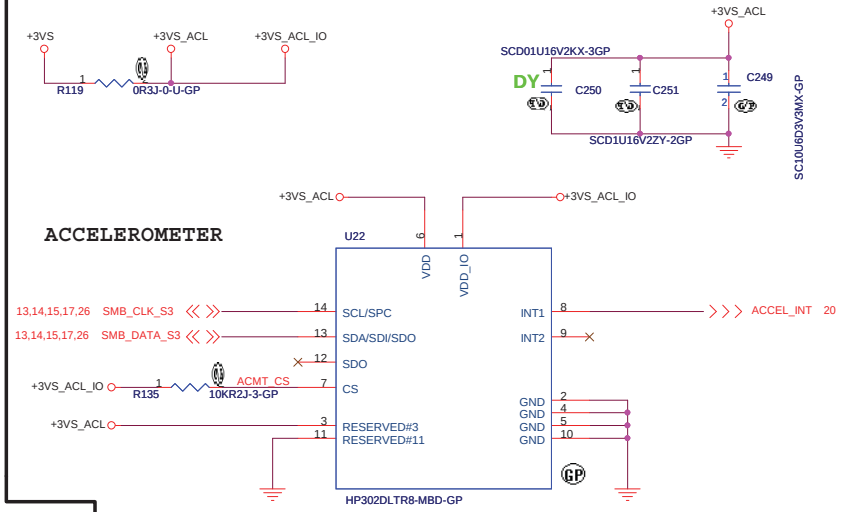
Half minicard



Mini-Card--WWAN

Full minicard





<Core Design>

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Title: Mini-Card/Accelerometer

Size: Custom | Document Number: NORN 3.0 | Rev: SE

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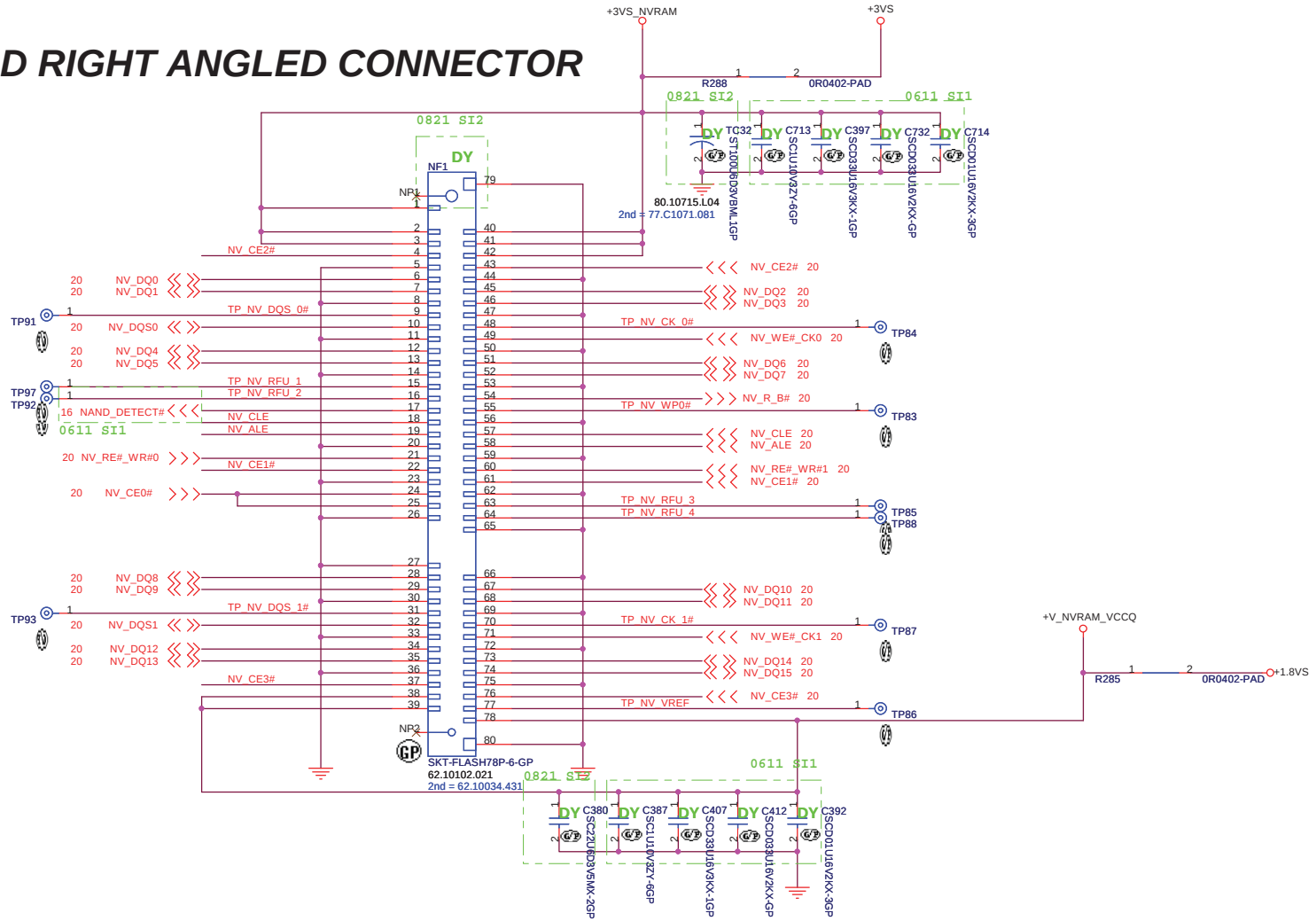
BRAIDWOOD RIGHT ANGLED CONNECTOR



<Core Design>

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: NAND FLASH CONN

Size: A3 | Document Number: NORN 3.0 | Rev: SE

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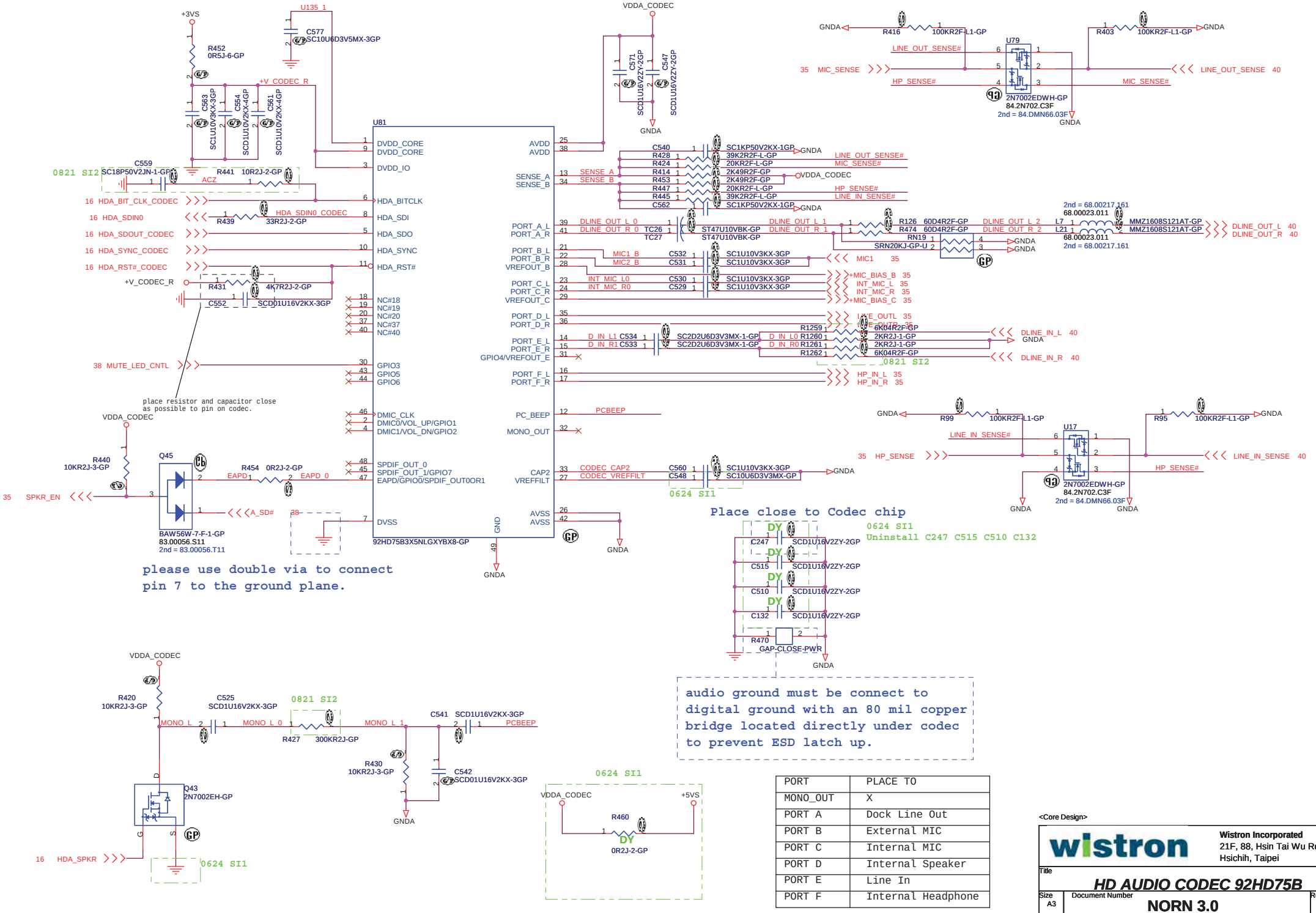

PORT	PLACE TO
MONO_OUT	X
PORT A	Dock Line Out
PORT B	External MIC
PORT C	Internal MIC
PORT D	Internal Speaker
PORT E	Line In
PORT F	Internal Headphone

<Core Design>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HD AUDIO CODEC 92HD75B

Size: A3 | Document Number: NORN 3.0 | Rev: SE

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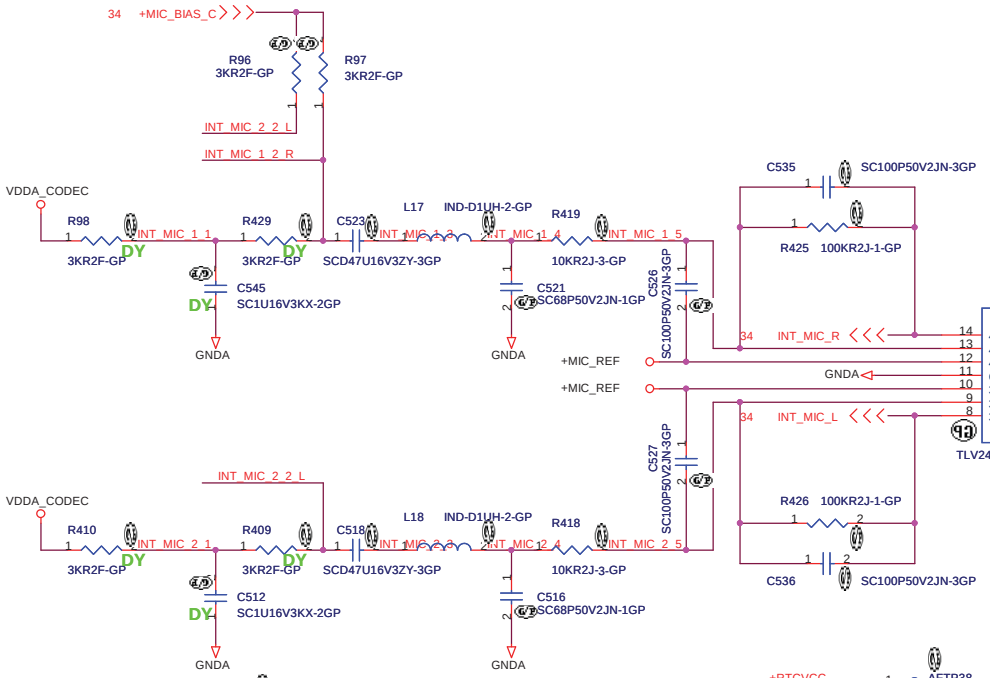
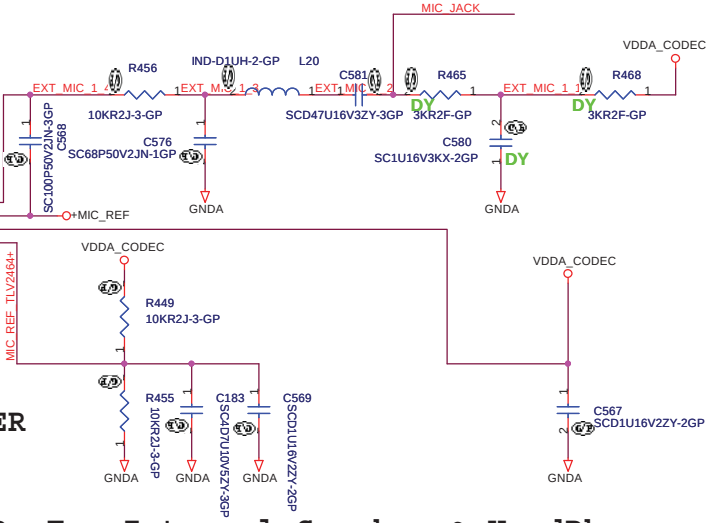
AMP. for Internal Microphone

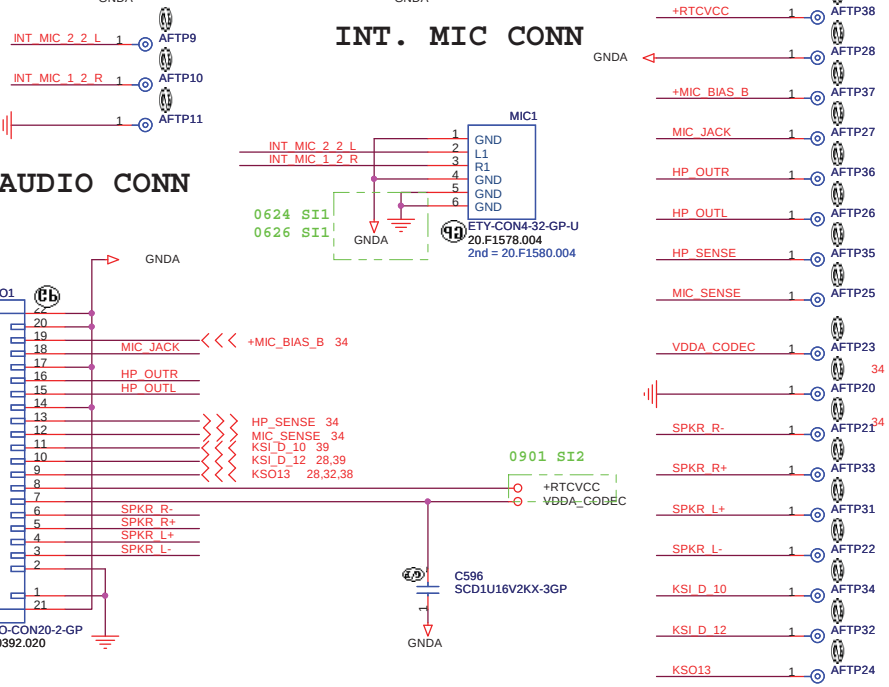


AMP. for External Microphone



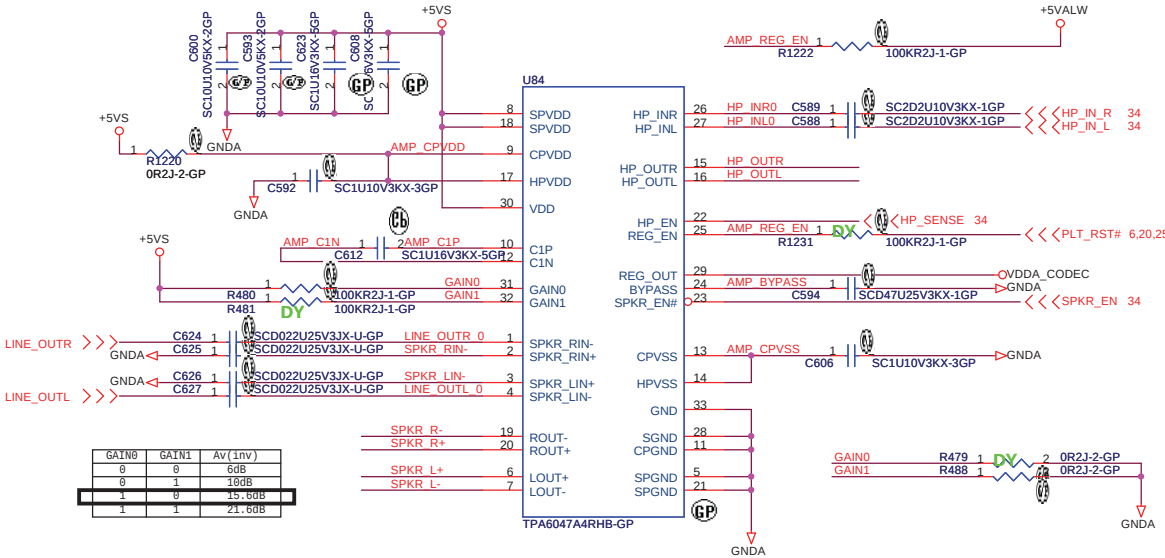
VREF BUFFER

INT. MIC CONN



AUDIO CONN

AMP. For Internal Speaker & HeadPhone.



<Core Design>

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Hsichih, Taipei

Title: AMP & Audio Conn.

Size: A3 | Document Number: NORN 3.0 | Rev: SE

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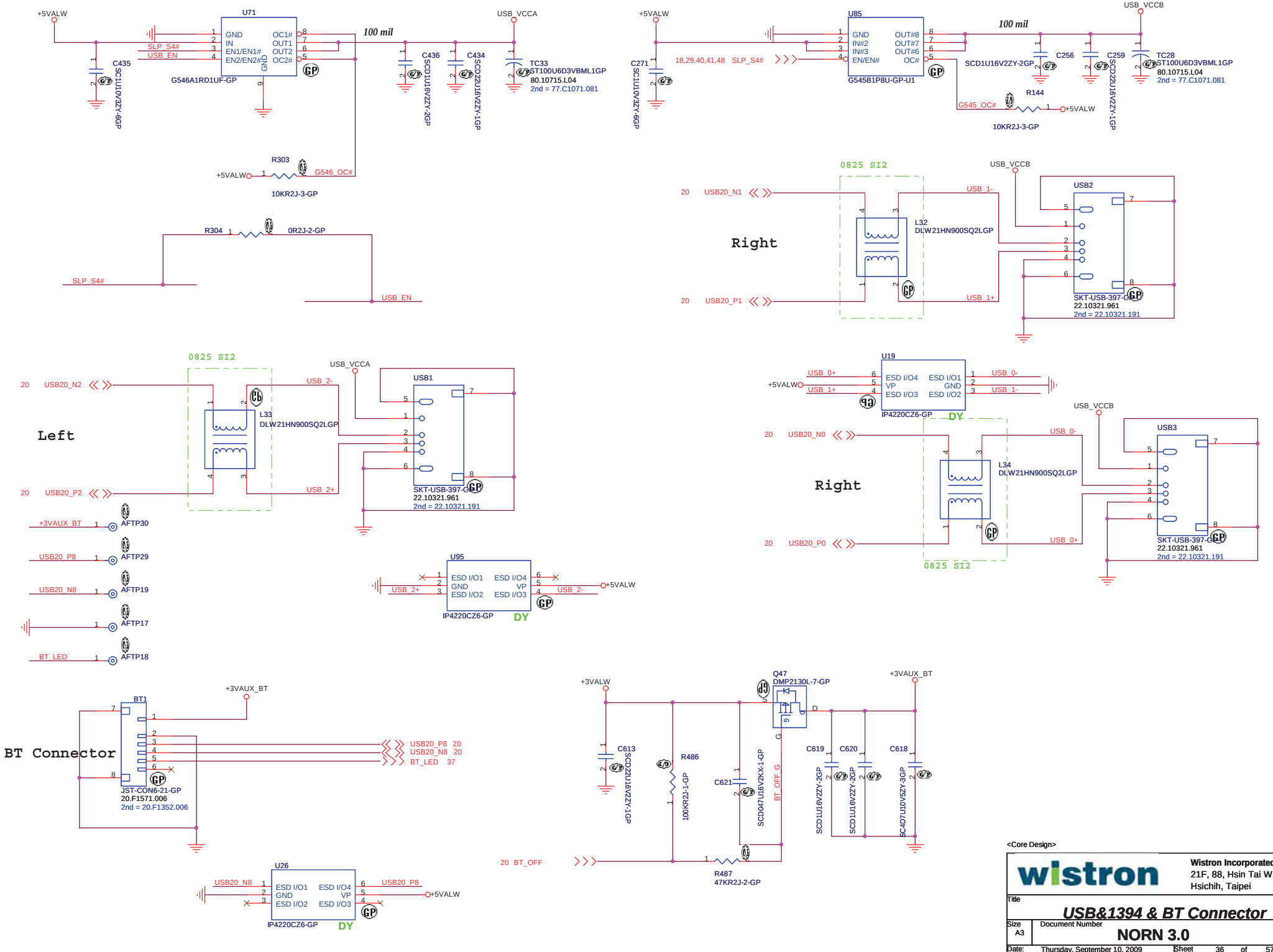

<Core Design>

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Hsichih, Taipei

Title: USB&1394 & BT Connector

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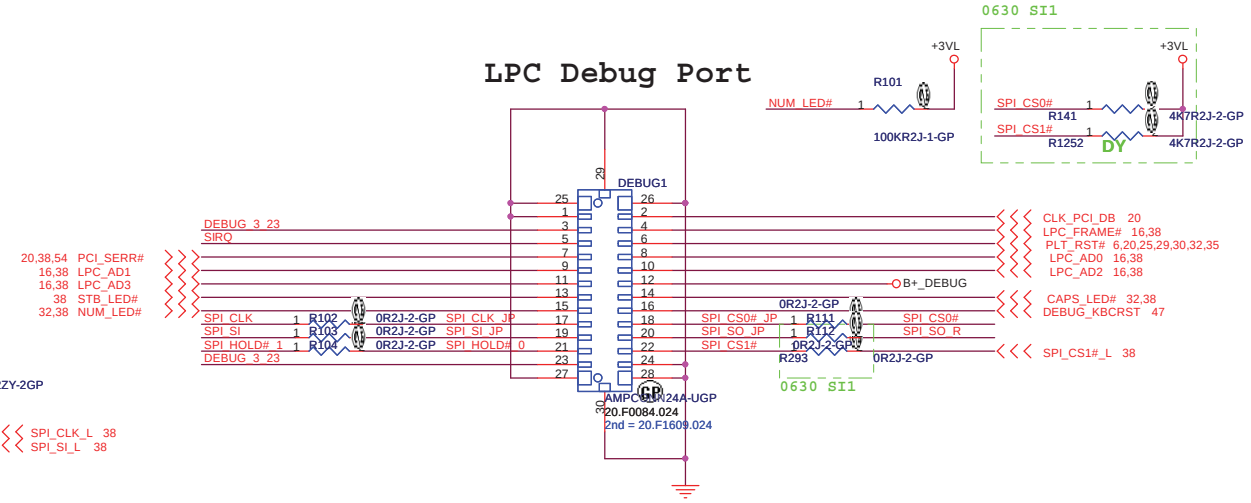
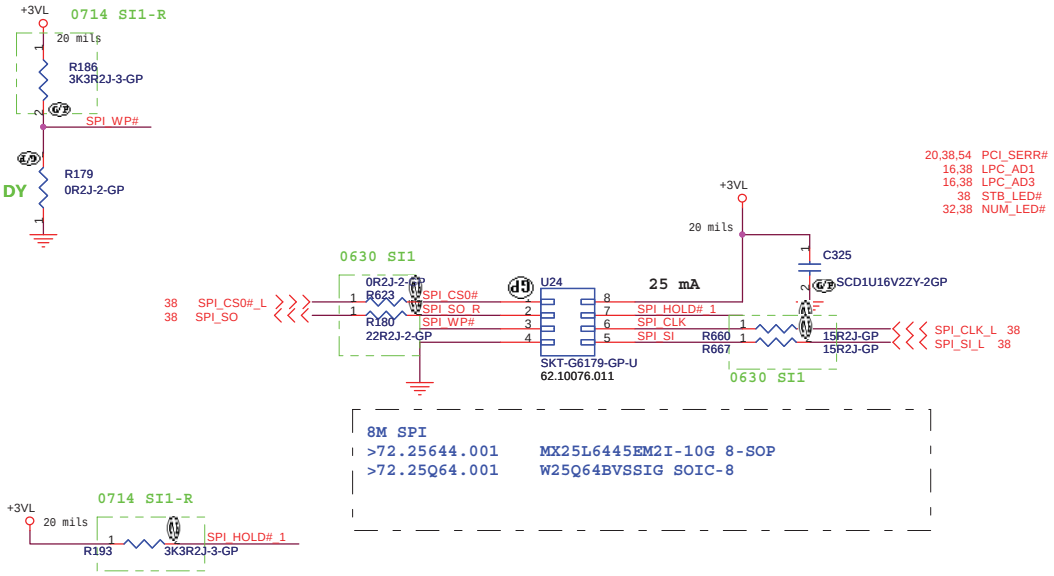
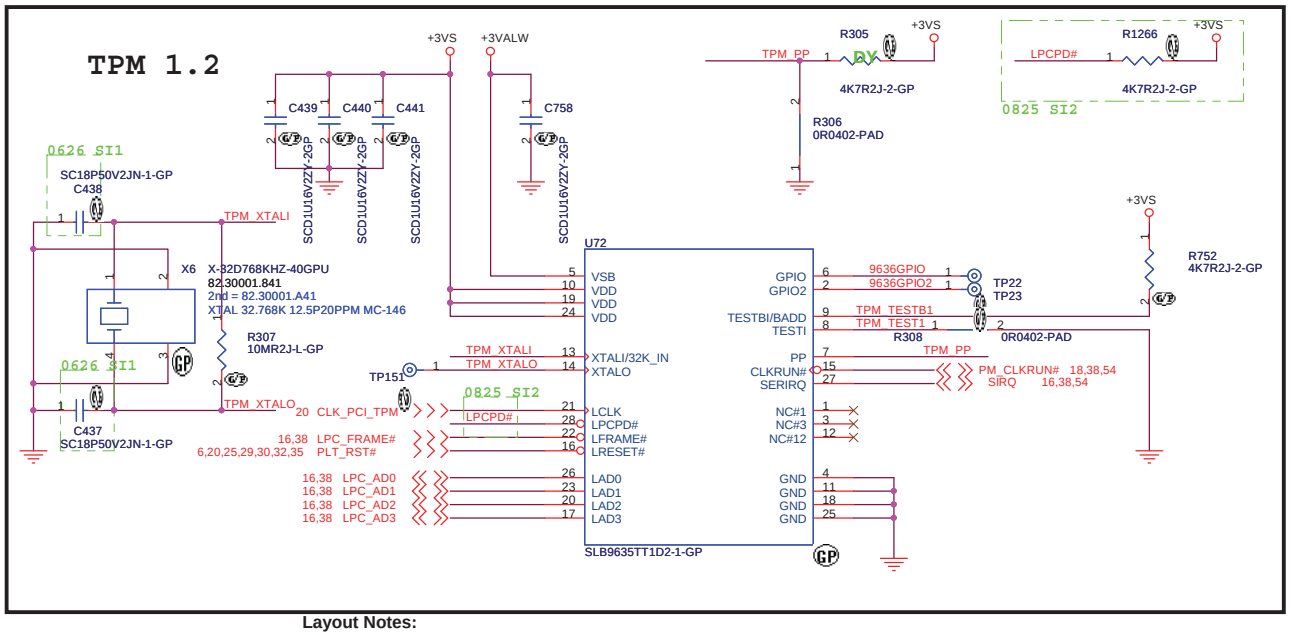
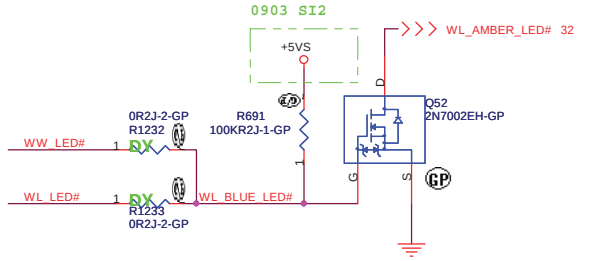
8Mb x 1

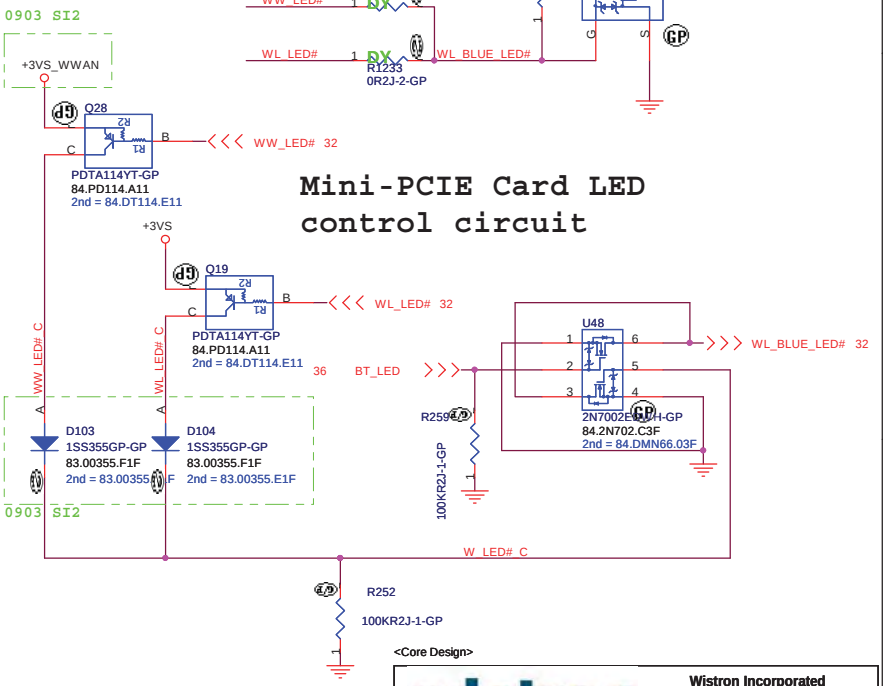
LPC Debug Port











Layout Notes:

Make sure that the stubs to the test points(TPM_XTALO) in the layout are as short as possible on the high speed signals.

<Core Design>

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Title: TPM/BIOS/24 DEBUG PORT

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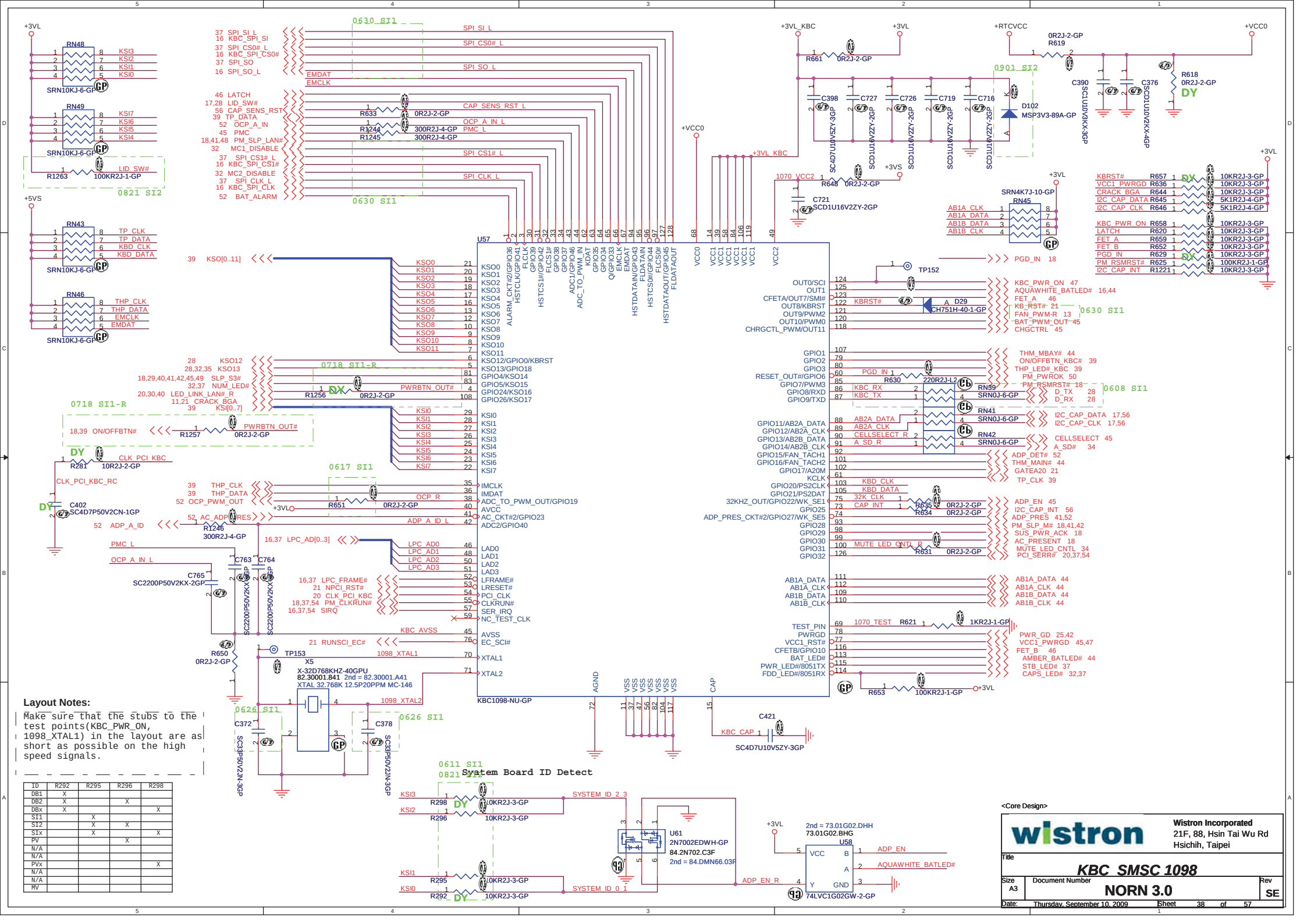
U57
KBC1098-NU-GP
0630 SI1
0821 SI2
0718 SI1-R
0617 SI1
0626 SI1
0611 SI1
0901 SI2
0630 SI1
0608 SI1
System Board ID Detect
Layout Notes:
Make sure that the stubs to the test points(KBC_PWR_ON, 1098_XTAL1) in the layout are as short as possible on the high speed signals.
ID R292 R295 R296 R298
DB1 X
DB2 X X
DBx X X
SI1 X
SI2 X X
SIx X X
PV X
N/A
N/A
PVx X
N/A
N/A
MV
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Hsichih, Taipei
KBC SMSC 1098
NORN 3.0
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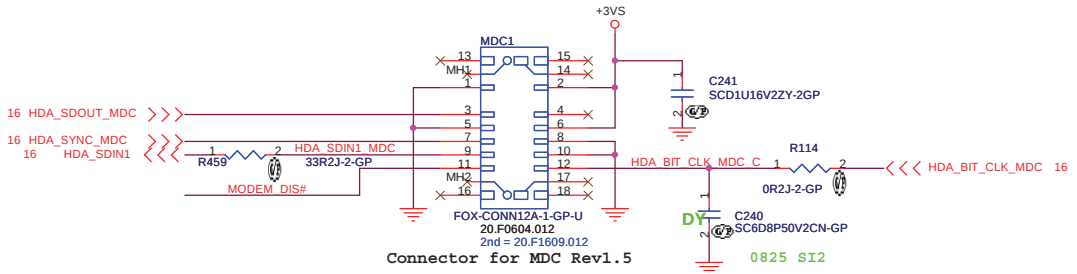
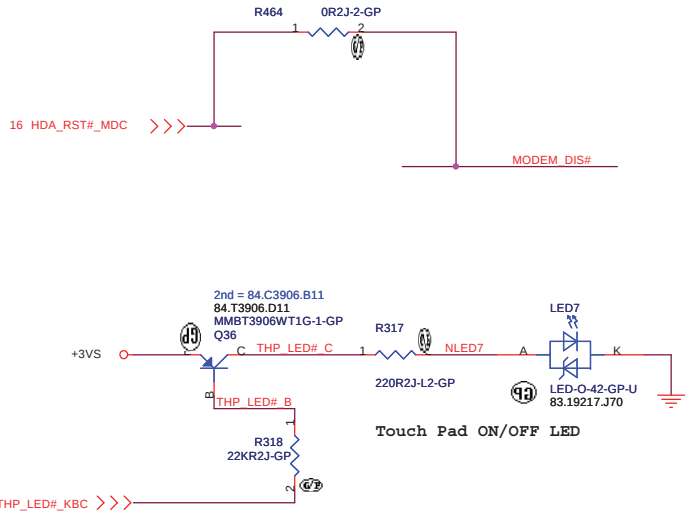
MDC 1.5 Conn.

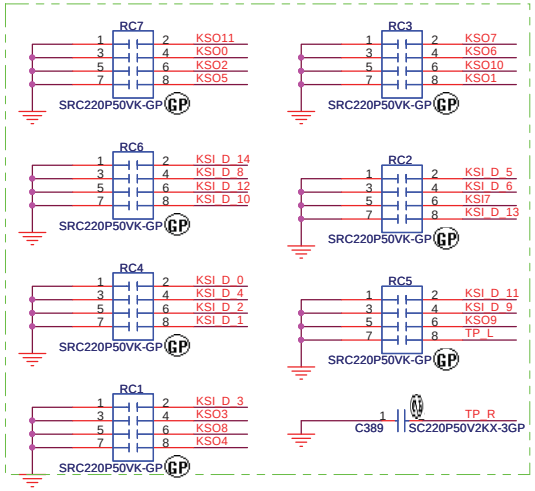


Connector for MDC Rev1.5



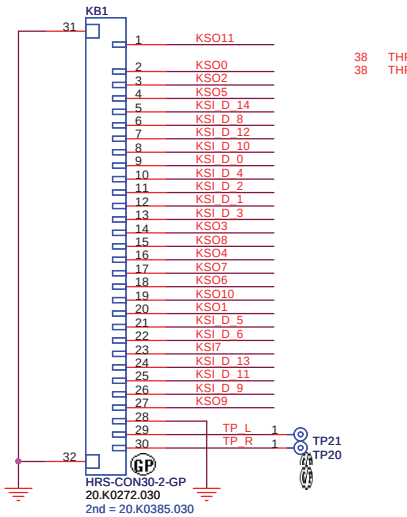
Touch Pad ON/OFF LED

0825 SI2

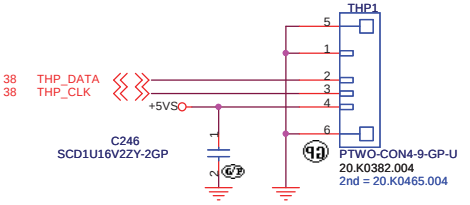


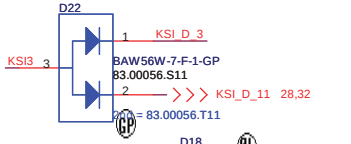
INT_KBD CONN.

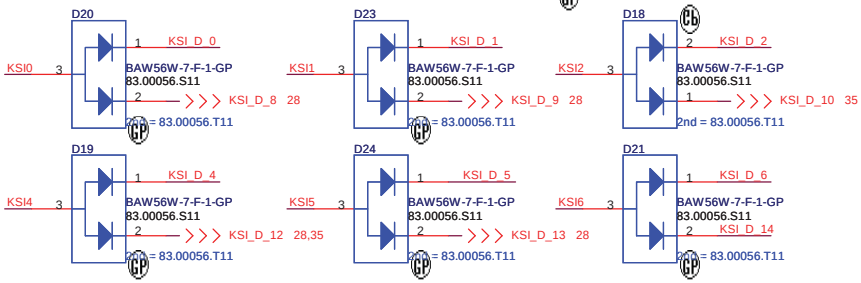
38 KSO[0..11] → KSO[0..11]
38 KSI[0..7] → KSI[0..7]



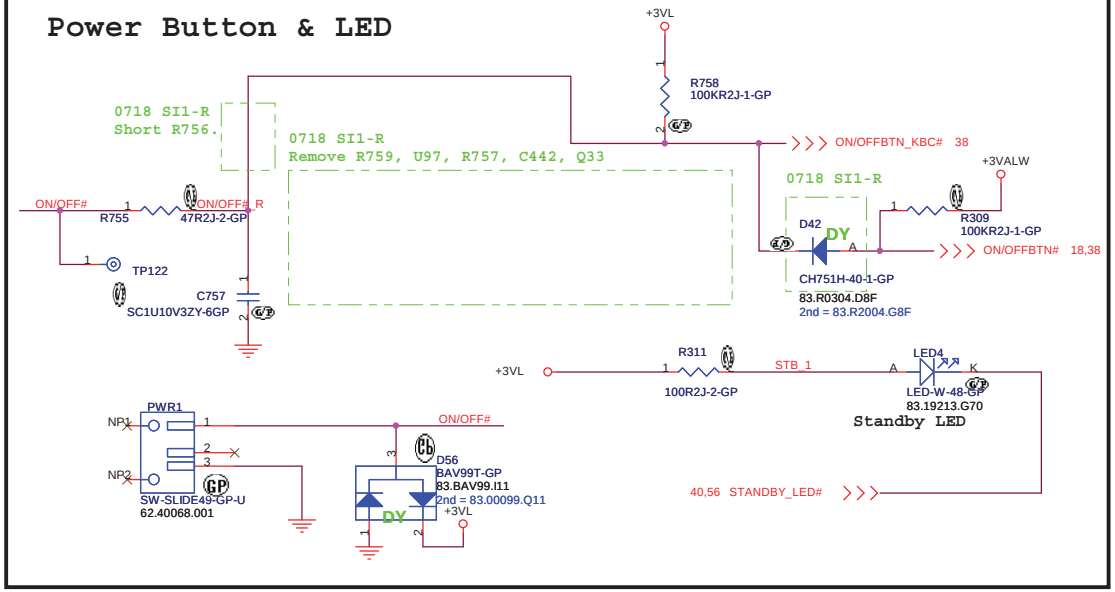
Touch_Pad CONN.



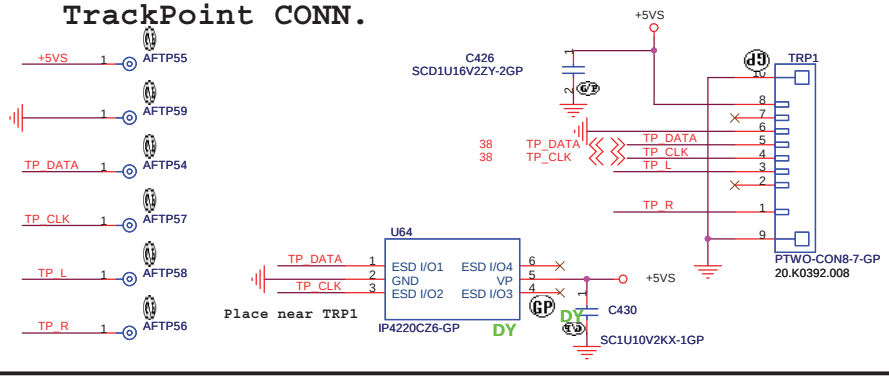


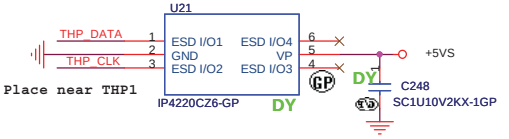


Power Button & LED



TrackPoint CONN.





<Core Design>
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Hsichih, Taipei

Title: **MDC/KBD/ON OFF/T.P.**

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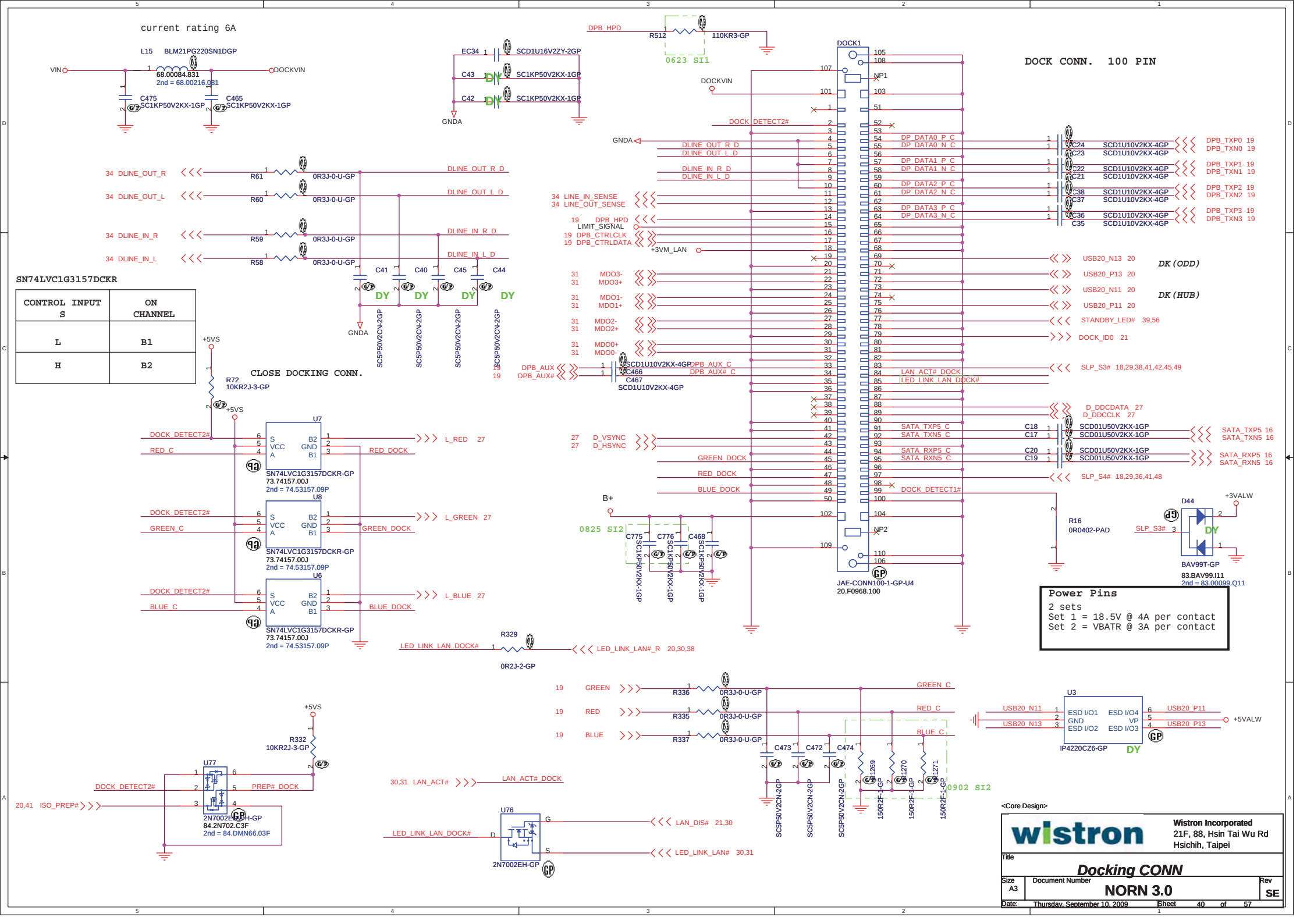
current rating 6A
L15 BLM21PG220SN1DGP
68.00084.831
2nd = 68.00216.031
VIN
DOCKVIN
C475 SC1KP50V2KX-1GP
C465 SC1KP50V2KX-1GP
EC34 SCD1U16V2ZY-2GP
C43 DY SC1KP50V2KX-1GP
C42 DY SC1KP50V2KX-1GP
GNDA
DPB_HPD
R512 110KR3-GP
0623 SI1
DOCK1
DOCKVIN
NP1
NP2
DOCK_DETECT2#
GNDA
DLINE_OUT_R_D
DLINE_OUT_L_D
DLINE_IN_R_D
DLINE_IN_L_D
34 DLINE_OUT_R
34 DLINE_OUT_L
34 DLINE_IN_R
34 DLINE_IN_L
R61 0R3J-0-U-GP
R60 0R3J-0-U-GP
R59 0R3J-0-U-GP
R58 0R3J-0-U-GP
C41 C40 C45 C44
DY DY DY DY
SC5P50V2CN-2GP
34 LINE_IN_SENSE
34 LINE_OUT_SENSE
19 DPB_HPD
LIMIT_SIGNAL
19 DPB_CTRLCLK
19 DPB_CTRLDATA
+3VM_LAN
DP_DATA0_P_C
DP_DATA0_N_C
DP_DATA1_P_C
DP_DATA1_N_C
DP_DATA2_P_C
DP_DATA2_N_C
DP_DATA3_P_C
DP_DATA3_N_C
C24 SCD1U10V2KX-4GP
C23 SCD1U10V2KX-4GP
C22 SCD1U10V2KX-4GP
C21 SCD1U10V2KX-4GP
C38 SCD1U10V2KX-4GP
C37 SCD1U10V2KX-4GP
C36 SCD1U10V2KX-4GP
C35 SCD1U10V2KX-4GP
DPB_TXP0 19
DPB_TXN0 19
DPB_TXP1 19
DPB_TXN1 19
DPB_TXP2 19
DPB_TXN2 19
DPB_TXP3 19
DPB_TXN3 19
DOCK CONN. 100 PIN
USB20_N13 20
USB20_P13 20
USB20_N11 20
USB20_P11 20
DK (ODD)
DK (HUB)
STANDBY_LED# 39,56
DOCK_ID0 21
SLP_S3# 18,29,38,41,42,45,49
LAN_ACT# DOCK
LED_LINK_LAN_DOCK#
D_DDCDATA 27
D_DDCCLK 27
SATA_TXP5_C
SATA_TXN5_C
SATA_RXP5_C
SATA_RXN5_C
C18 C17 C20 C19
SCD01U50V2KX-1GP
SATA_TXP5 16
SATA_TXN5 16
SATA_RXP5 16
SATA_RXN5 16
SLP_S4# 18,29,36,41,48
DOCK_DETECT1#
31 MDO3-
31 MDO3+
31 MDO1-
31 MDO1+
31 MDO2-
31 MDO2+
31 MDO0+
31 MDO0-
DPB_AUX
DPB_AUX#
DPB_AUX_C
DPB_AUX#_C
C466 C467 SCD1U10V2KX-4GP
27 D_VSYNC
27 D_HSYNC
GREEN_DOCK
RED_DOCK
BLUE_DOCK
B+
0825 SI2
C775 C776 C468 SC1KP50V2KX-1GP
JAE-CONN100-1-GP-U4
20.F0968.100
R16 0R0402-PAD
D44 BAV99T-GP
83.BAV99.I11
2nd = 83.00099.Q11
+3VALW
SLP_S3#
Power Pins
2 sets
Set 1 = 18.5V @ 4A per contact
Set 2 = VBATR @ 3A per contact
SN74LVC1G3157DCKR
CONTROL INPUT S
ON CHANNEL
L
B1
H
B2
CLOSE DOCKING CONN.
R72 10KR2J-3-GP
+5VS
U7
U8
U6
DOCK_DETECT2#
RED_C
GREEN_C
BLUE_C
RED_DOCK
GREEN_DOCK
BLUE_DOCK
L_RED 27
L_GREEN 27
L_BLUE 27
SN74LVC1G3157DCKR-GP
73.74157.00J
2nd = 74.53157.09P
LED_LINK_LAN_DOCK#
R329 0R2J-2-GP
LED_LINK_LAN#_R 20,30,38
19 GREEN
19 RED
19 BLUE
R336 R335 R337 0R3J-0-U-GP
C473 C472 C474
150R2F-1-GP
0902 SI2
U3
IP4220CZ6-GP
USB20_N11
USB20_N13
USB20_P11
USB20_P13
+5VALW
R332 10KR2J-3-GP
U77
2N7002EH-GP
84.2N702.C3F
2nd = 84.DMN66.03F
PREP#_DOCK
20,41 ISO_PREP#
30,31 LAN_ACT#
LAN_ACT#_DOCK
U76
LED_LINK_LAN_DOCK#
LAN_DIS# 21,30
LED_LINK_LAN# 30,31
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Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
Docking CONN
Size A3
Document Number
NORN 3.0
Rev SE
Date: Thursday, September 10, 2009
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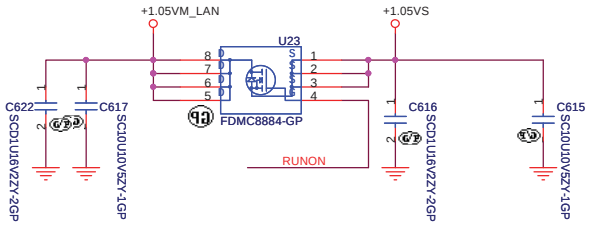
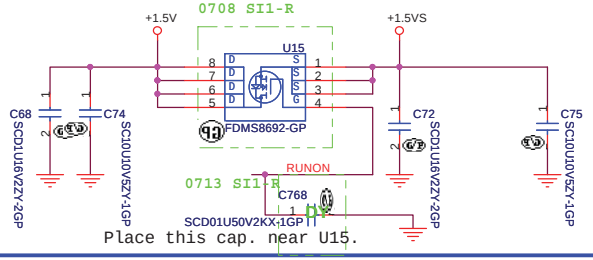
+1.05VM_LAN to +1.05VS Transfer

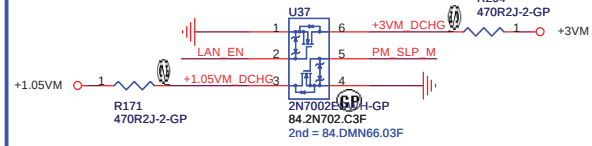


+1.5V to +1.5VS Transfer

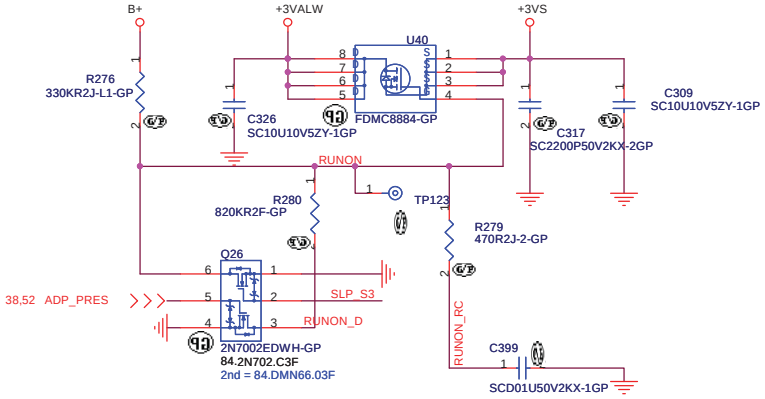


Place this cap. near U15.

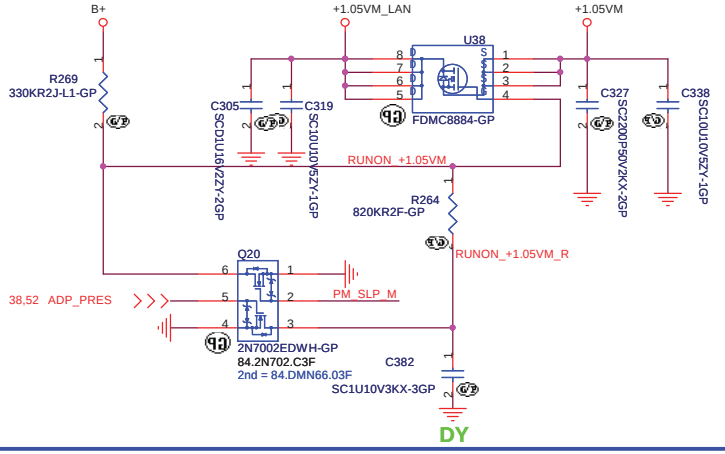
Discharge circuit-2 fot V-M



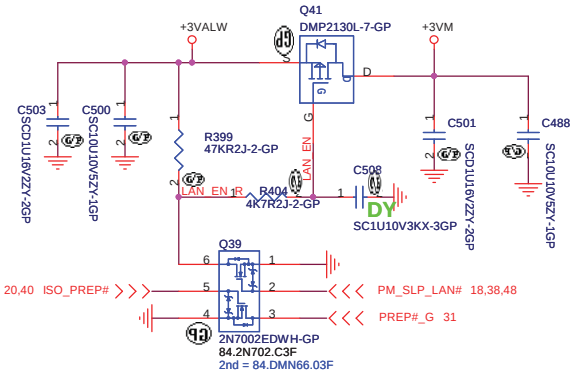
+3VALW to +3VS Transfer



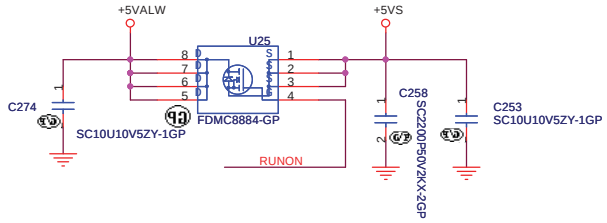
+1.05VM_LAN to +1.05VM Transfer

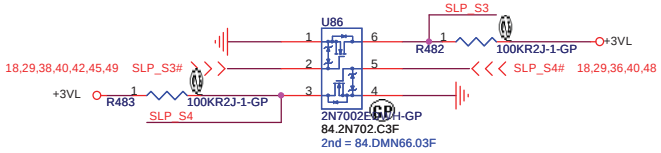


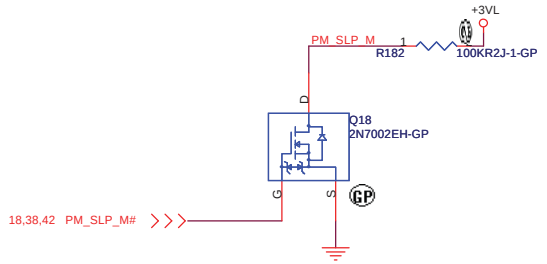
+3VALW to +3VM Transfer



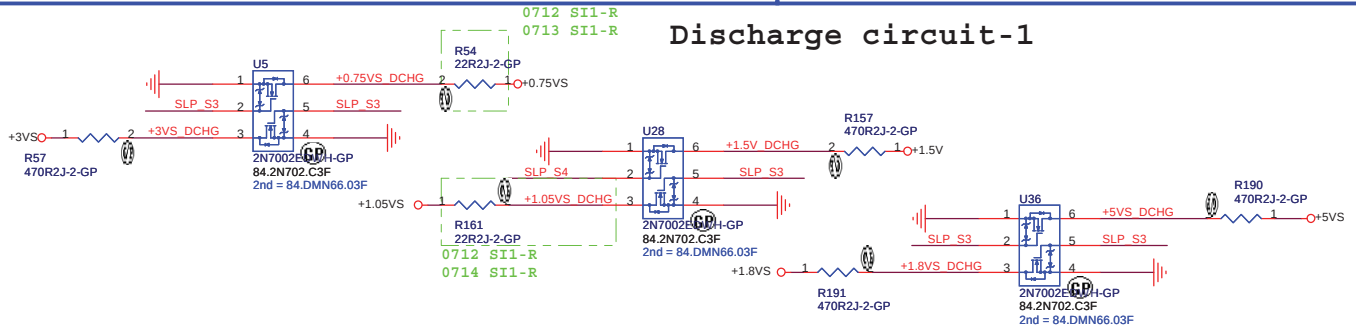
+5VALW to +5VS Transfer

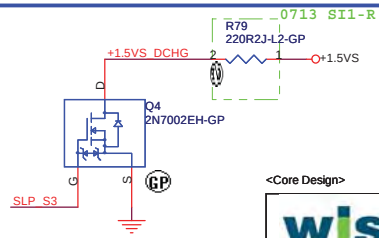






Discharge circuit-1





<Core Design>

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Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DC/DC Circuit

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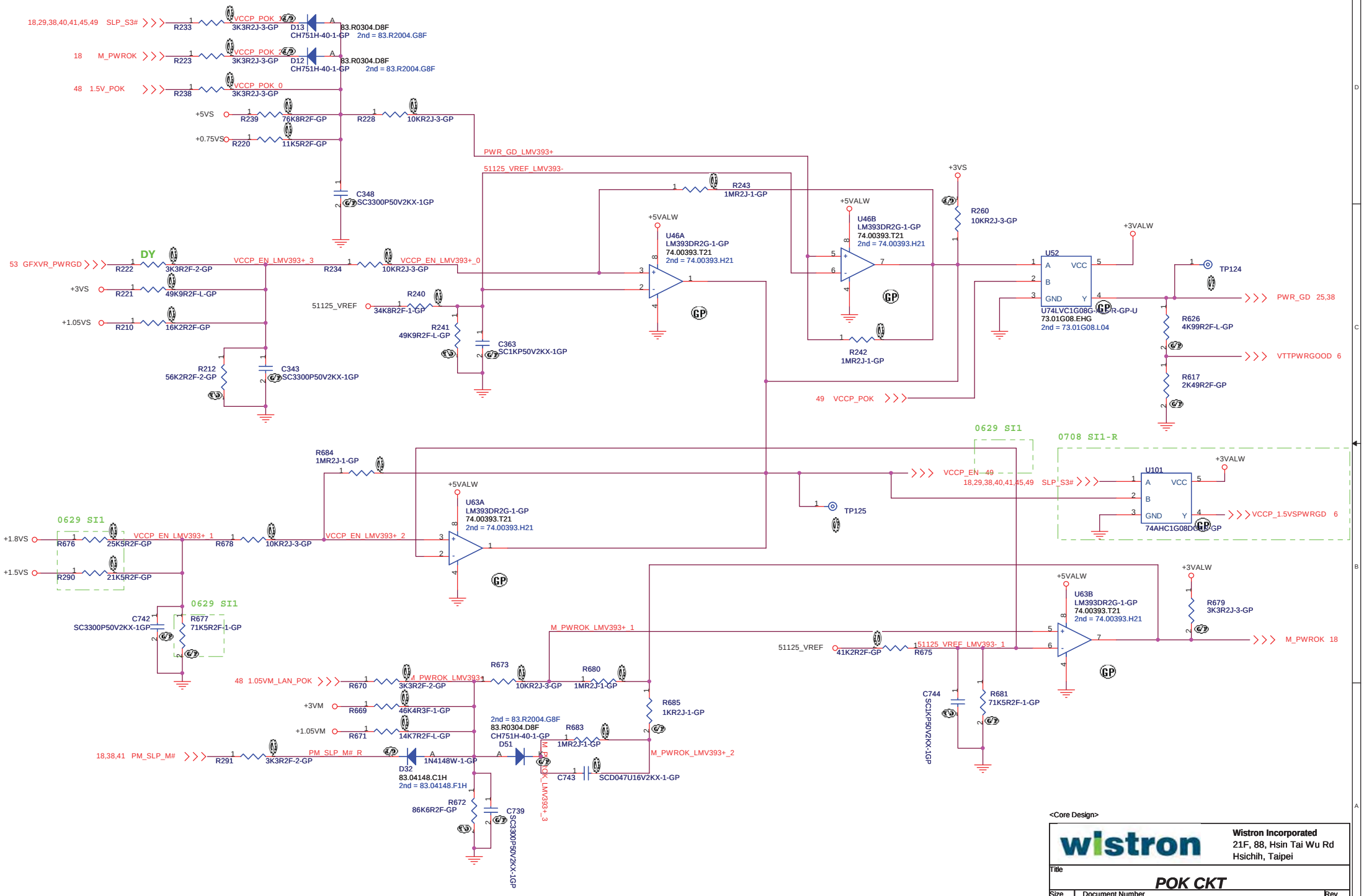

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Hsichih, Taipei

Title: POK CKT

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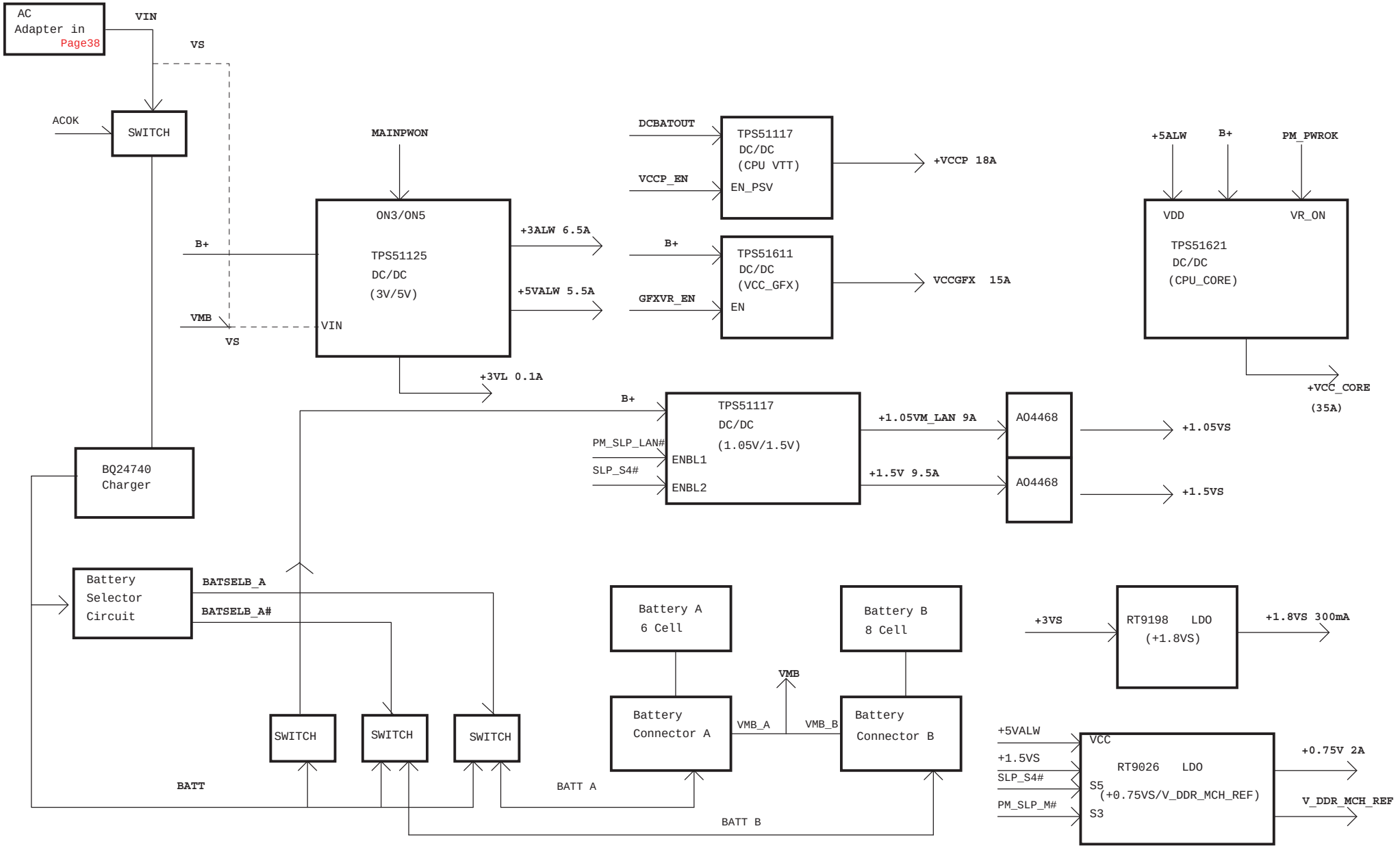

<Core Design>

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: **Power Block Diagram**

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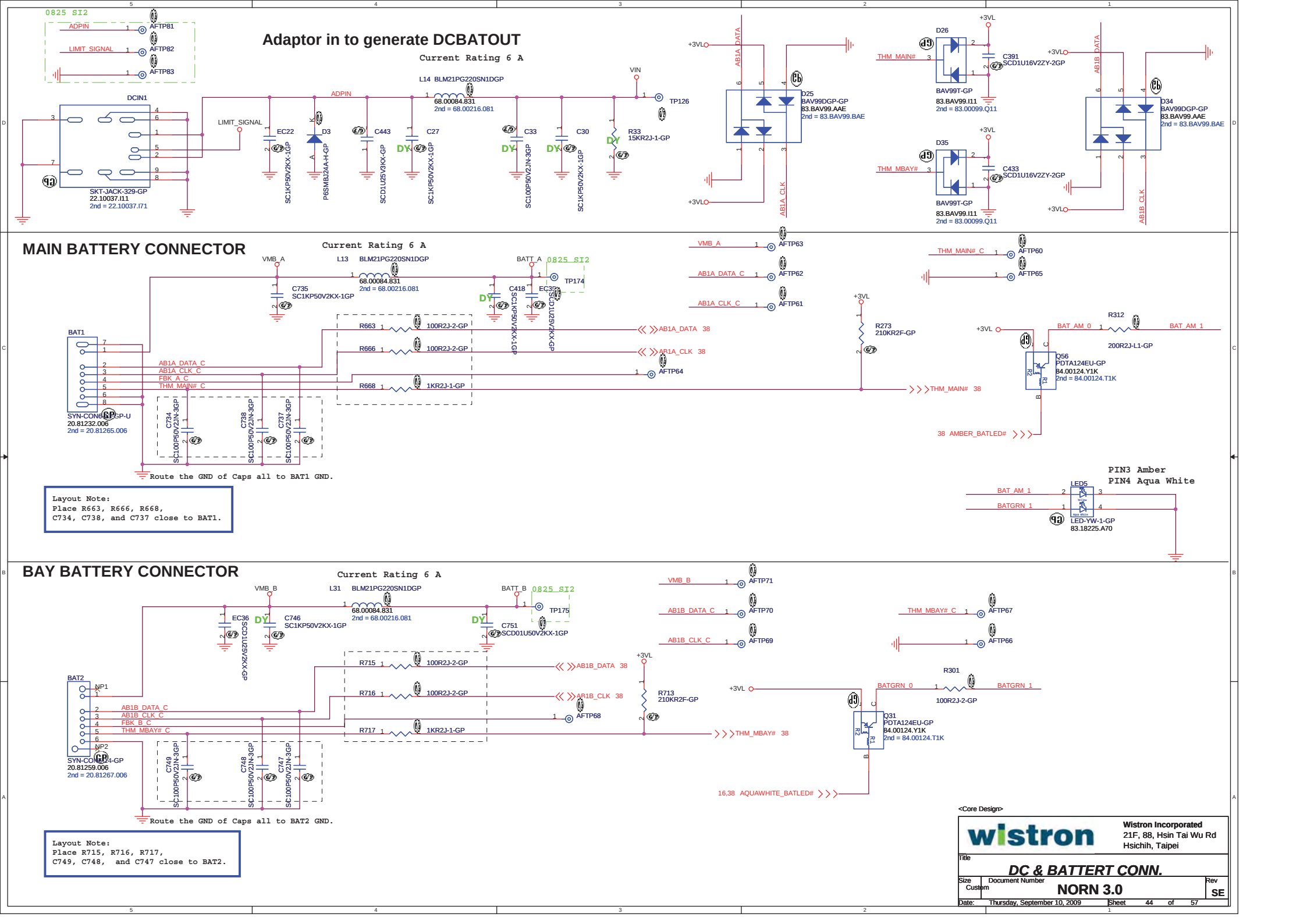
0825_SI2
ADPIN
LIMIT_SIGNAL
AFTP81
AFTP82
AFTP83
Adaptor in to generate DCBATOUT
Current Rating 6 A
DCIN1
SKT-JACK-329-GP
22.10037.I11
2nd = 22.10037.I71
LIMIT_SIGNAL
EC22
SC1KP50V2KX-1GP
D3
P6SMBJ24A-H-GP
ADPIN
C443
SCD1U25V3KX-GP
C27
SC1KP50V2KX-1GP
L14 BLM21PG220SN1DGP
68.00084.831
2nd = 68.00216.081
C33
SC100P50V2JN-3GP
C30
SC1KP50V2KX-1GP
VIN
R33
15KR2J-1-GP
TP126
+3VLO
AB1A_DATA
AB1A_CLK
D25
BAV99DGP-GP
83.BAV99.AAE
2nd = 83.BAV99.BAE
D26
BAV99T-GP
83.BAV99.I11
2nd = 83.00099.Q11
THM_MAIN#
C391
SCD1U16V2ZY-2GP
+3VL
D35
THM_MBAY#
C433
SCD1U16V2ZY-2GP
AB1B_DATA
AB1B_CLK
D34
BAV99DGP-GP
83.BAV99.AAE
2nd = 83.BAV99.BAE
MAIN BATTERY CONNECTOR
Current Rating 6 A
VMB_A
L13 BLM21PG220SN1DGP
68.00084.831
2nd = 68.00216.081
BATT_A
0825_SI2
TP174
C735
SC1KP50V2KX-1GP
C418
SC1KP50V2KX-1GP
EC35
SCD1U25V2KX-GP
BAT1
SYN-CON-6P-GP-U
20.81232.006
2nd = 20.81265.006
AB1A_DATA_C
AB1A_CLK_C
FBK_A_C
THM_MAIN#_C
R663
100R2J-2-GP
R666
100R2J-2-GP
R668
1KR2J-1-GP
AB1A_DATA 38
AB1A_CLK 38
AFTP64
C734
SC100P50V2JN-3GP
C738
SC100P50V2JN-3GP
C737
SC100P50V2JN-3GP
Route the GND of Caps all to BAT1 GND.
VMB_A
AB1A_DATA_C
AB1A_CLK_C
AFTP63
AFTP62
AFTP61
R273
210KR2F-GP
THM_MAIN# 38
THM_MAIN#_C
AFTP60
AFTP65
R312
BAT_AM_0
BAT_AM_1
200R2J-L1-GP
Q56
PDTA124EU-GP
84.00124.Y1K
2nd = 84.00124.T1K
38 AMBER_BATLED#
PIN3 Amber
PIN4 Aqua White
LED5
BAT_AM_1
BATGRN_1
LED-YW-1-GP
83.18225.A70
Layout Note:
Place R663, R666, R668,
C734, C738, and C737 close to BAT1.
BAY BATTERY CONNECTOR
Current Rating 6 A
VMB_B
L31 BLM21PG220SN1DGP
68.00084.831
2nd = 68.00216.081
BATT_B
0825_SI2
TP175
EC36
SCD1U25V2KX-GP
C746
SC1KP50V2KX-1GP
C751
SCD01U50V2KX-1GP
BAT2
SYN-CON-4-GP
20.81259.006
2nd = 20.81267.006
AB1B_DATA_C
AB1B_CLK_C
FBK_B_C
THM_MBAY#_C
R715
100R2J-2-GP
R716
100R2J-2-GP
R717
1KR2J-1-GP
AB1B_DATA 38
AB1B_CLK 38
AFTP68
C749
SC100P50V2JN-3GP
C748
SC100P50V2JN-3GP
C747
SC100P50V2JN-3GP
Route the GND of Caps all to BAT2 GND.
VMB_B
AB1B_DATA_C
AB1B_CLK_C
AFTP71
AFTP70
AFTP69
R713
210KR2F-GP
THM_MBAY# 38
THM_MBAY#_C
AFTP67
AFTP66
R301
BATGRN_0
BATGRN_1
100R2J-2-GP
Q31
PDTA124EU-GP
84.00124.Y1K
2nd = 84.00124.T1K
16,38 AQUAWHITE_BATLED#
Layout Note:
Place R715, R716, R717,
C749, C748, and C747 close to BAT2.
<Core Design>
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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
DC & BATTERT CONN.
Size
Custom
Document Number
NORN 3.0
Rev
SE
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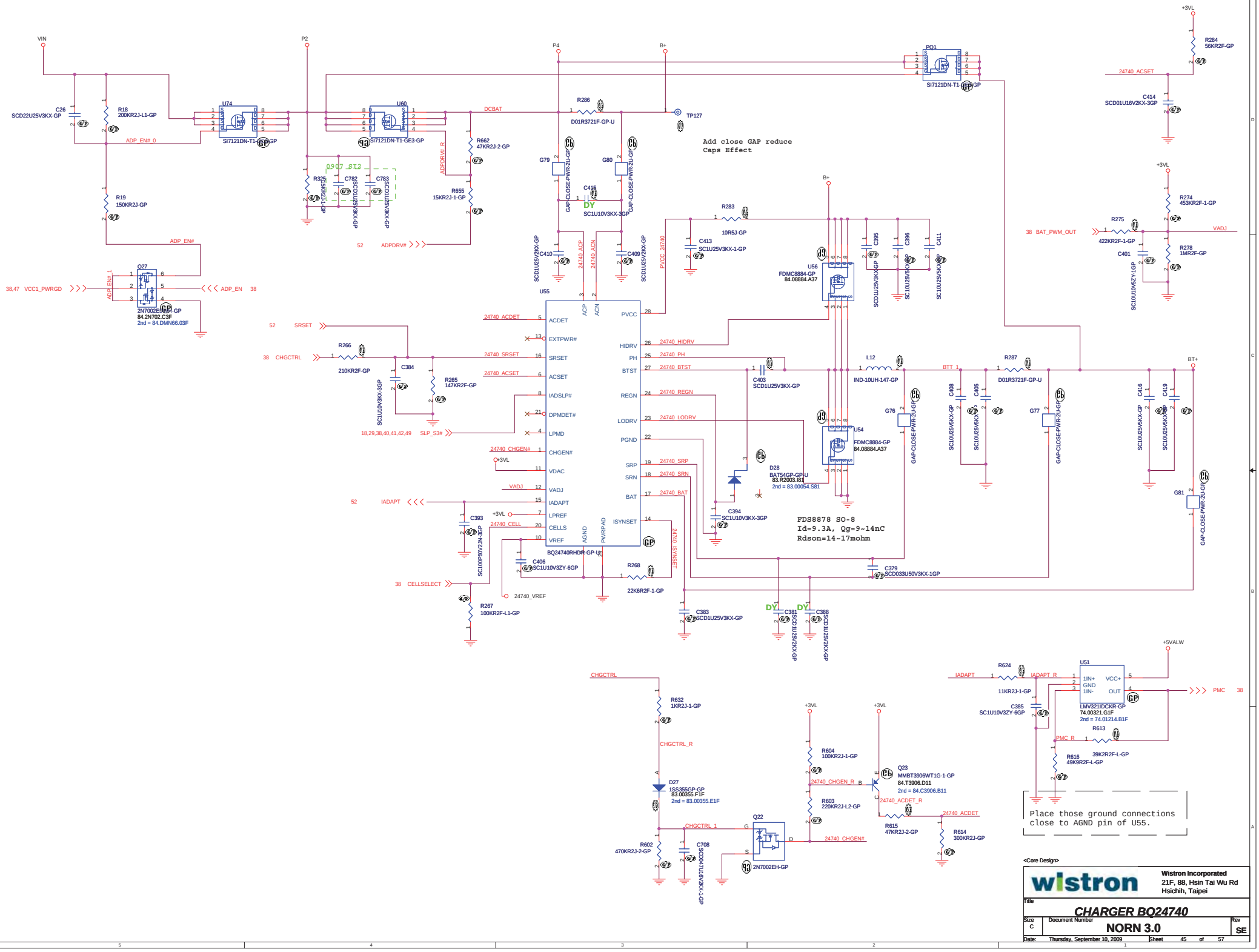
VIN
P2
P4
B+
DCBAT
ADP_EN# 0
ADP_EN#
ADP_EN
VCC1_PWRGD
SRSET
CHGCTRL
SLP_S3#
IADAPT
CELLSELECT
ADPDRV#
Add close GAP reduce
Caps Effect
FDS8878 SO-8
Id=9.3A, Qg=9~14nC
Rdson=14~17mohm
Place those ground connections
close to AGND pin of U55.
BQ24740RHDR-GP-U
2N7002EH-GP
SI7121DN-T1-GE3-GP
FDMC8884-GP
84.08884.A37
IND-10UH-147-GP
D01R3721F-GP-U
LMV321IDCKR-GP
74.00321.G1F
2nd = 74.01214.B1F
MMBT3906WT1G-1-GP
84.T3906.D11
2nd = 84.C3906.B11
BAT54GP-GP-U
83.R2003.I81
2nd = 83.00054.S81
1SS355GP-GP
83.00355.F1F
2nd = 83.00355.E1F
2N7002EH-GP
84.2N702.C3F
2nd = 84.DMN66.03F
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
CHARGER BQ24740
NORN 3.0
Size C
Rev SE
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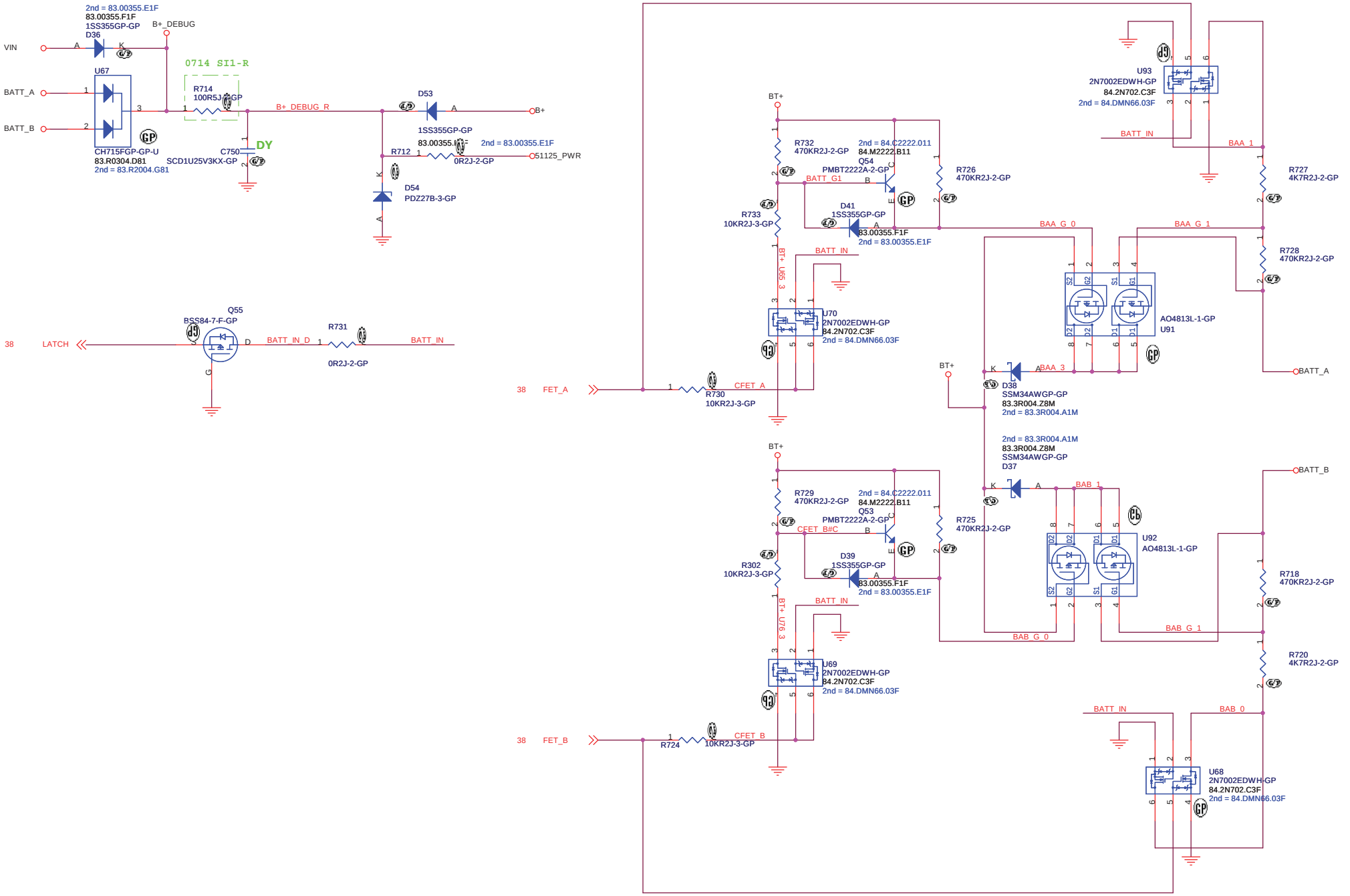

<Core Design>

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Hsichih, Taipei

Title: **Battery Selector**

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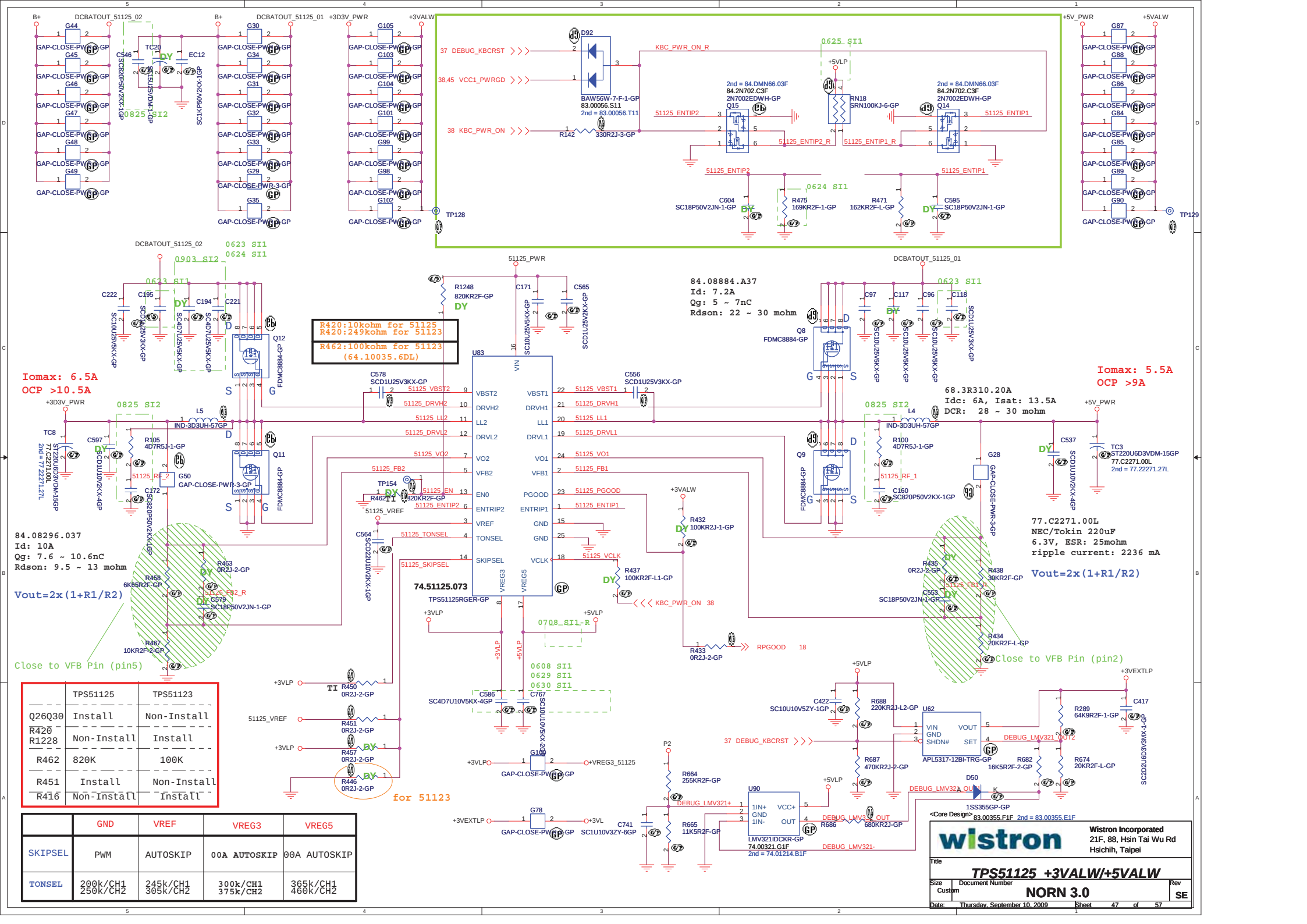
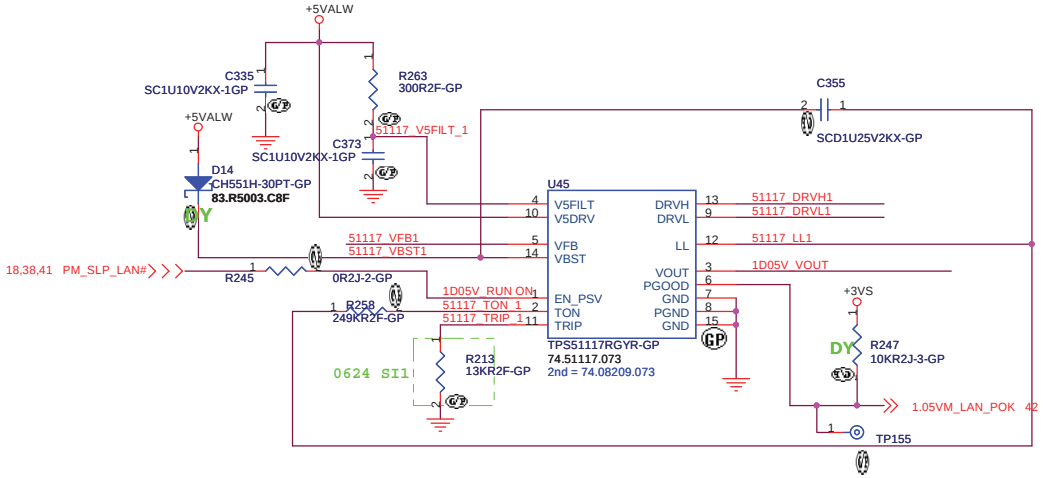
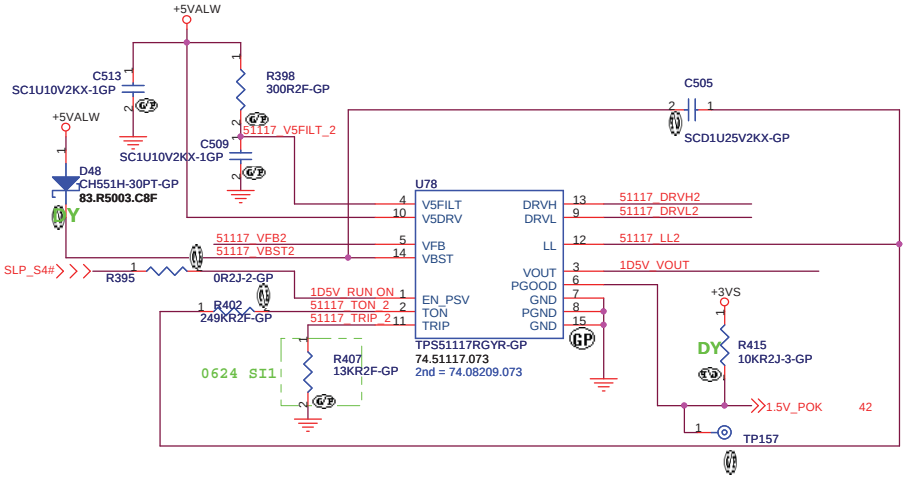


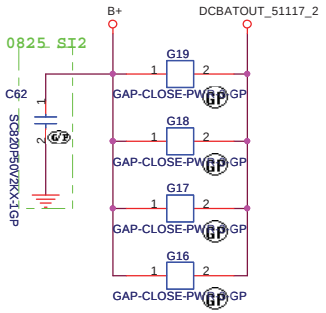
	TPS51125	TPS51123
Q26Q30	Install	Non-Install
R420 R1228	Non-Install	Install
R462	820K	100K
R451 R416	Install Non-Install	Non-Install Install

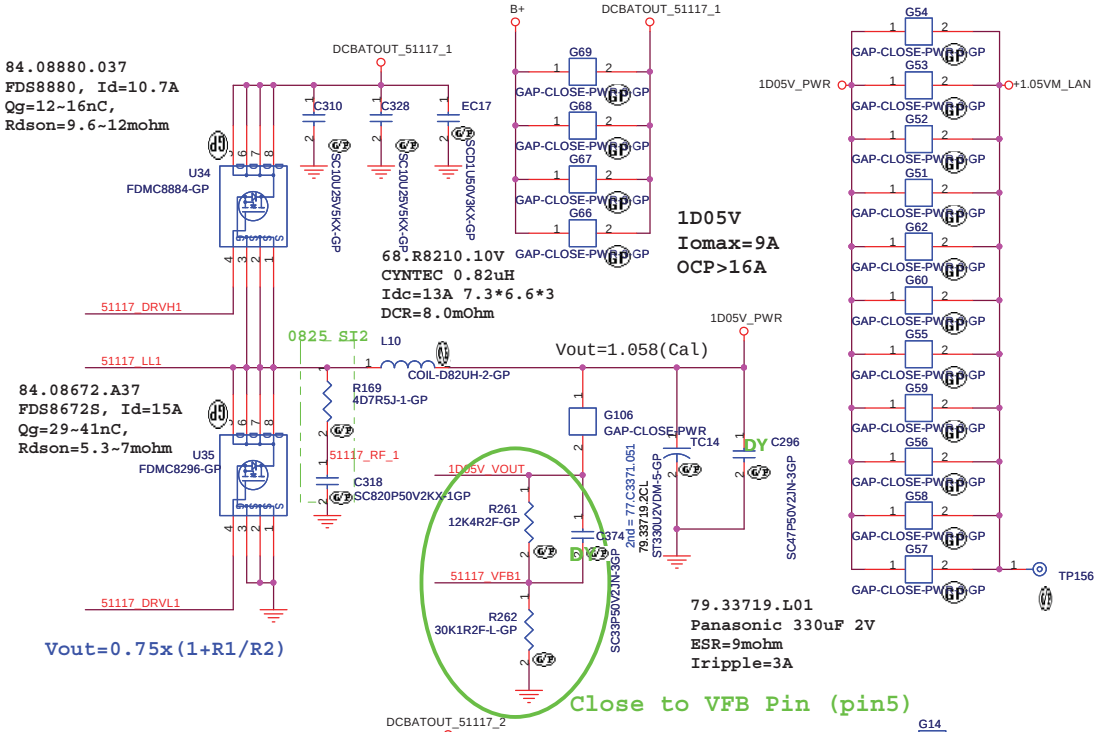
	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

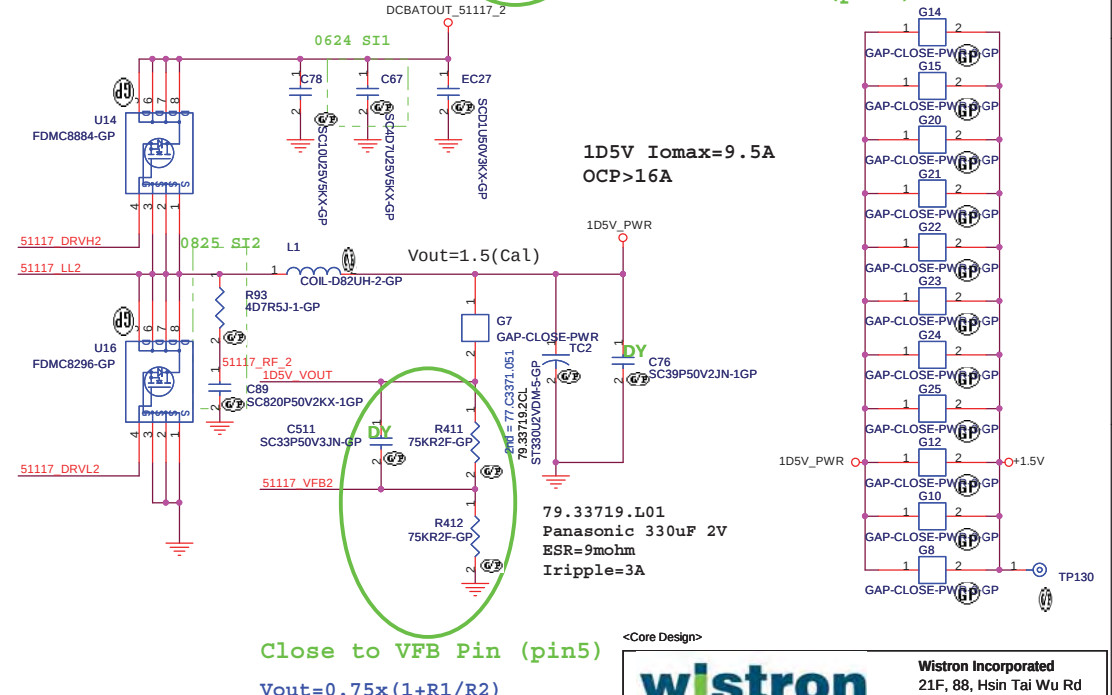




	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2







<Core Design>
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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: TPS51117_+1.05VM_LAN / +1.5V

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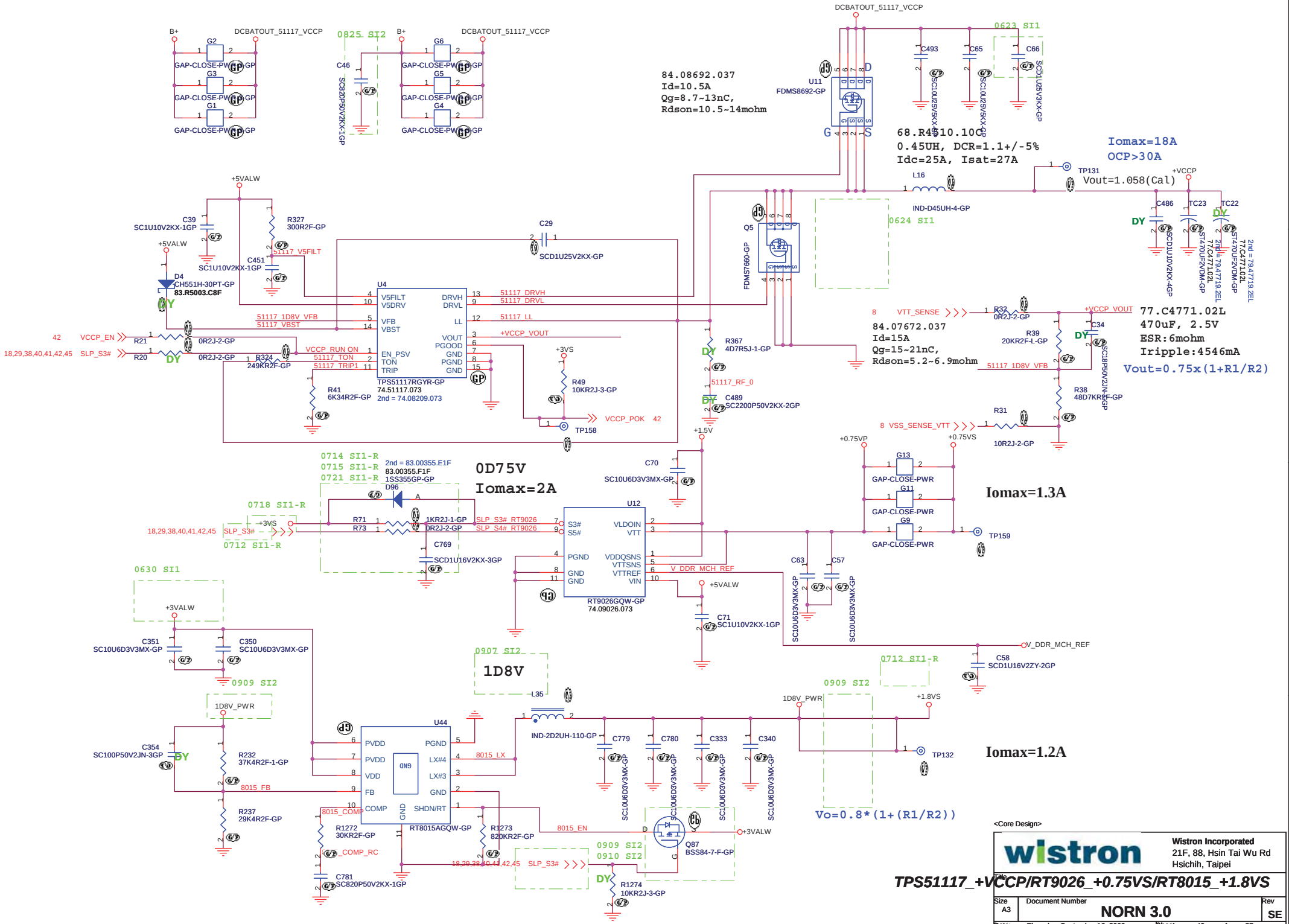
DCBATOUT_51117_VCCP
84.08692.037
Id=10.5A
Qg=8.7~13nC,
Rdson=10.5~14mohm
U11
FDMS8692-GP
68.R4510.10G
0.45UH, DCR=1.1+/-5%
Idc=25A, Isat=27A
Iomax=18A
OCP>30A
L16
IND-D45UH-4-GP
TP131
Vout=1.058(Cal)
+VCCP
77.C4771.02L
470uF, 2.5V
ESR:6mohm
Iripple:4546mA
Vout=0.75x(1+R1/R2)
+5VALW
U4
TPS51117RGYR-GP
74.51117.073
2nd = 74.08209.073
VCCP_EN
SLP_S3#
VCCP_RUN ON
VCCP_POK
TP158
84.07672.037
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
VTT_SENSE
VSS_SENSE_VTT
+VCCP_VOUT
0D75V
Iomax=2A
U12
RT9026GQW-GP
74.09026.073
Iomax=1.3A
TP159
V_DDR_MCH_REF
1D8V
U44
RT8015AGQW-GP
IND-2D2UH-110-GP
Iomax=1.2A
Vo=0.8*(1+(R1/R2))
TP132
Q87
BSS84-7-F-GP
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
TPS51117_+VCCP/RT9026_+0.75VS/RT8015_+1.8VS
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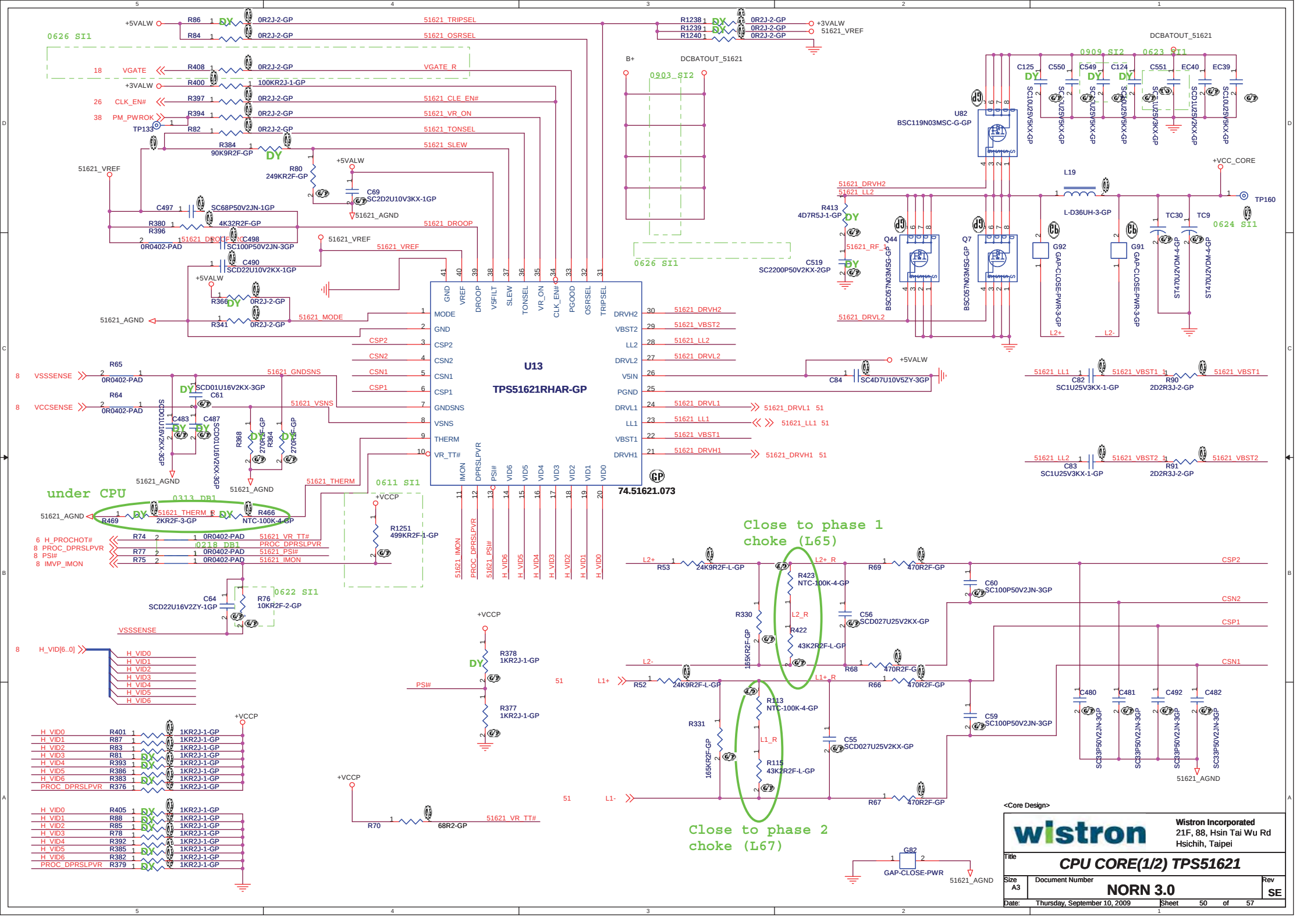
U13
TPS51621RHAR-GP
74.51621.073
under CPU
Close to phase 1 choke (L65)
Close to phase 2 choke (L67)
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Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
CPU CORE(1/2) TPS51621
NORN 3.0
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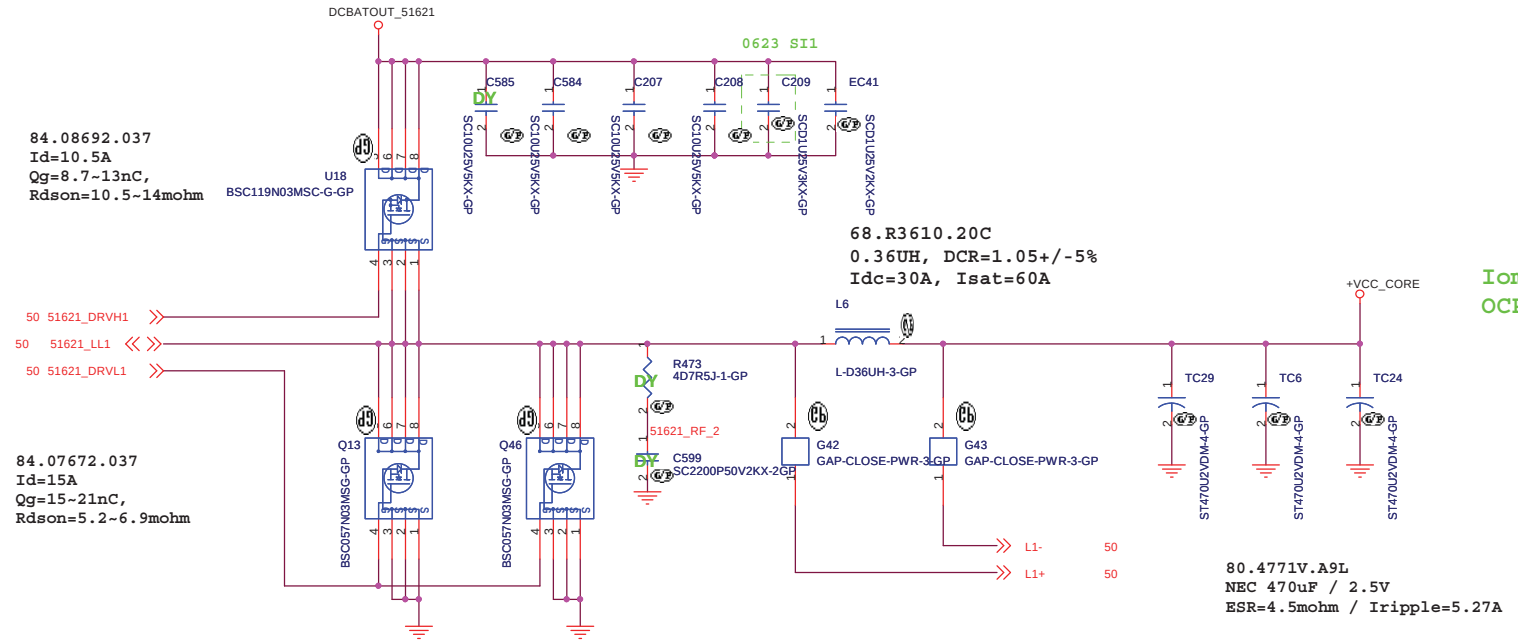
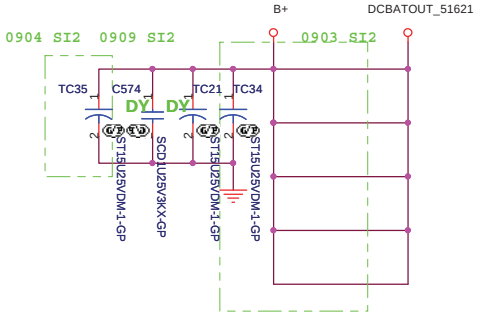
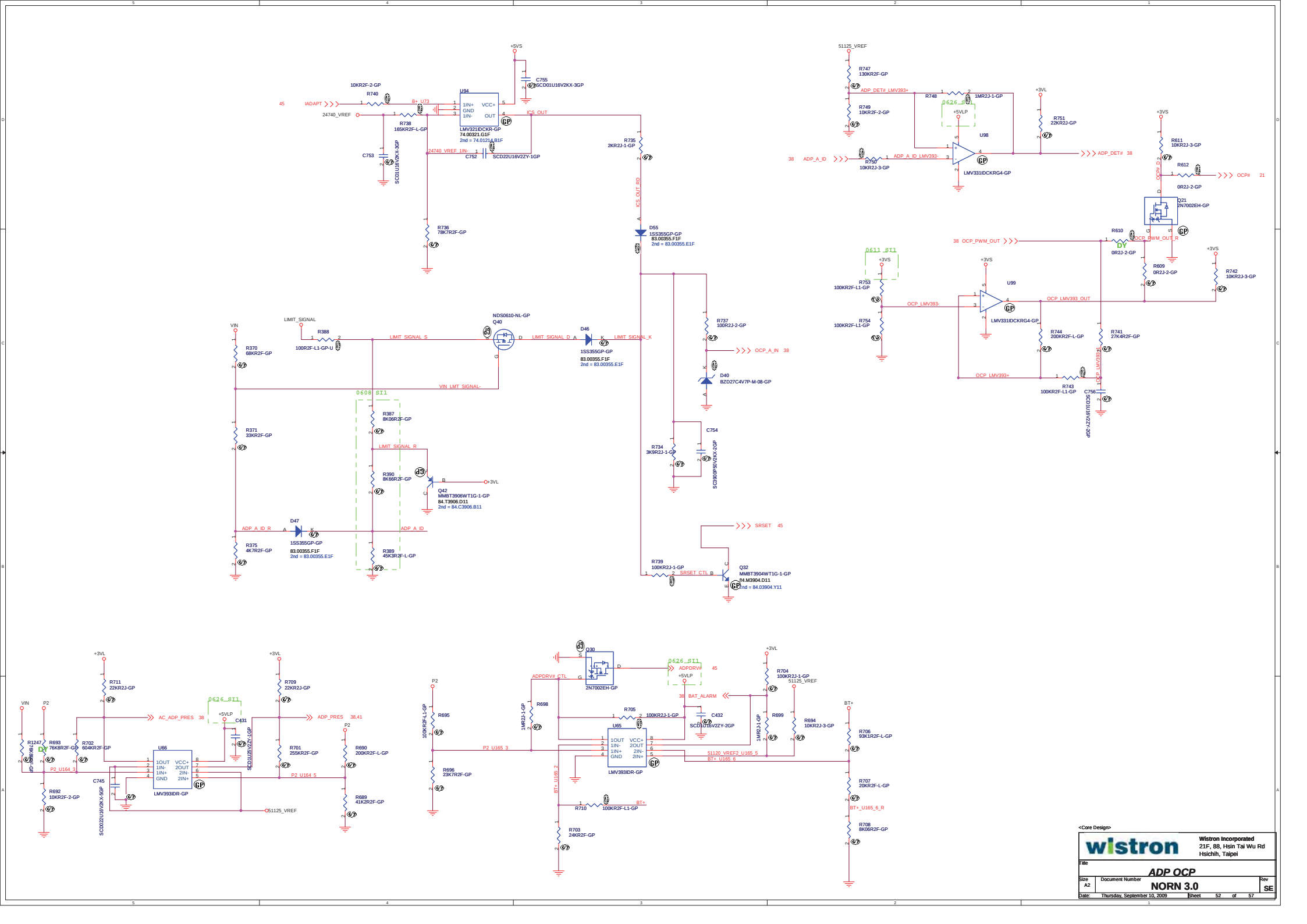

DCBATOUT_51621
0623 SI1
C585
C584
C207
C208
C209
EC41
DY
SC10U25V5KX-GP
SCD1U25V3KX-GP
SCD1U25V2KX-GP
84.08692.037
Id=10.5A
Qg=8.7~13nC,
Rdson=10.5~14mohm
U18
BSC119N03MSC-G-GP
68.R3610.20C
0.36UH, DCR=1.05+/-5%
Idc=30A, Isat=60A
Iomax=35A
OCP>=52A
+VCC_CORE
L6
L-D36UH-3-GP
50 51621_DRVH1
50 51621_LL1
50 51621_DRVL1
R473
4D7R5J-1-GP
51621_RF_2
C599
SC2200P50V2KX-2GP
G42
GAP-CLOSE-PWR-3-GP
G43
GAP-CLOSE-PWR-3-GP
TC29
TC6
TC24
ST470U2VDM-4-GP
Q13
Q46
BSC057N03MSG-GP
84.07672.037
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
L1-
L1+
50
80.4771V.A9L
NEC 470uF / 2.5V
ESR=4.5mohm / Iripple=5.27A


B+
DCBATOUT_51621
0904 SI2
0909 SI2
0903 SI2
TC35
C574
TC21
TC34
DY
ST15U25VDM-1-GP
SCD1U25V3KX-GP


+5VS
C755
SCD01U16V2KX-3GP
10KR2F-2-GP
R740
45
IADAPT
B+_UI73
24740_VREF
R738
165KR2F-L-GP
U94
1IN+
GND
1IN-
VCC+
OUT
LMV321IDCKR-GP
74.00321.G1F
2nd = 74.01214.B1F
ICS_OUT
C753
SCD01U16V2KX-3GP
24740_VREF_1IN-
C752
SCD22U16V2ZY-1GP
R735
2KR2J-1-GP
ICS_OUT_RD
R736
78K7R2F-GP
D55
1SS355GP-GP
83.00355.F1F
2nd = 83.00355.E1F
51125_VREF
R747
130KR2F-GP
ADP_DET#_LMV393+
R749
10KR2F-2-GP
R748
1MR2J-1-GP
0626_SI1
+5VLP
U98
+3VL
R751
22KR2J-GP
38
ADP_A_ID
R750
10KR2J-3-GP
ADP_A_ID_LMV393-
LMV331IDCKRG4-GP
ADP_DET#
38
+3VS
R611
10KR2J-3-GP
OCP#_R
R612
0R2J-2-GP
OCP#
21
Q21
2N7002EH-GP
R610
OCP_PWM_OUT_R
DY
0R2J-2-GP
38
OCP_PWM_OUT
0611_SI1
R753
100KR2F-L1-GP
R754
100KR2F-L1-GP
OCP_LMV393-
U99
LMV331IDCKRG4-GP
OCP_LMV393_OUT
R609
0R2J-2-GP
R742
10KR2J-3-GP
R744
200KR2F-L-GP
R741
27K4R2F-GP
OCP_LMV393+
R743
100KR2F-L1-GP
C756
SCD01U16V2ZY-2GP
OCP_LMV393+1
VIN
LIMIT_SIGNAL
R388
100R2F-L1-GP-U
LIMIT_SIGNAL_S
Q40
NDS0610-NL-GP
LIMIT_SIGNAL_D
D46
1SS355GP-GP
83.00355.F1F
2nd = 83.00355.E1F
LIMIT_SIGNAL_K
R737
100R2J-2-GP
OCP_A_IN
38
D40
BZD27C4V7P-M-08-GP
R370
68KR2F-GP
VIN_LMT_SIGNAL-
0608_SI1
R387
8K06R2F-GP
R371
33KR2F-GP
LIMIT_SIGNAL_R
R390
8K06R2F-GP
Q42
MMBT3906WT1G-1-GP
84.T3906.D11
2nd = 84.C3906.B11
+3VL
ADP_A_ID_R
D47
1SS355GP-GP
83.00355.F1F
2nd = 83.00355.E1F
ADP_A_ID
R375
4K7R2F-GP
R389
45K3R2F-L-GP
C754
SC390P50V2KX-3GP
R734
3K9R2J-1-GP
SRSET
45
R739
100KR2J-1-GP
SRSET_CTL
Q32
MMBT3904WT1G-1-GP
84.M3904.D11
2nd = 84.03904.Y11
VIN
P2
+3VL
R711
22KR2J-GP
0626_SI1
+5VLP
AC_ADP_PRES
38
C431
SCD1U25V2ZY-1GP
R709
22KR2J-GP
ADP_PRES
38,41
R1247
DY
R693
76K8R2F-GP
R702
604KR2F-GP
U66
1OUT
1IN-
1IN+
GND
VCC+
2OUT
2IN-
2IN+
LMV393IDR-GP
P2_U164_3
R701
255KR2F-GP
P2_U164_5
R690
200KR2F-L-GP
R692
10KR2F-2-GP
C745
SCD22U16V2KX-5GP
R689
41K2R2F-GP
51125_VREF
Q30
2N7002EH-GP
ADPDRV#_CTL
0626_SI1
ADPDRV#
45
+5VLP
38
BAT_ALARM
R704
100KR2J-1-GP
51125_VREF
P2
R695
10KR2F-L1-GP
R698
1MR2J-1-GP
R705
100KR2J-1-GP
C432
SCD1U16V2ZY-2GP
R699
1MR2J-1-GP
R694
10KR2J-3-GP
U65
1OUT
1IN-
1IN+
GND
VCC+
2OUT
2IN-
2IN+
LMV393IDR-GP
P2_U165_3
51120_VREF2_U165_5
BT+_U165_6
BT+_U165_2
R696
23K7R2F-GP
R710
100KR2F-L1-GP
BT+
R703
24KR2F-GP
BT+
R706
93K1R2F-L-GP
R707
20KR2F-L-GP
BT+_U165_6_R
R708
8K06R2F-GP
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Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
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Date:
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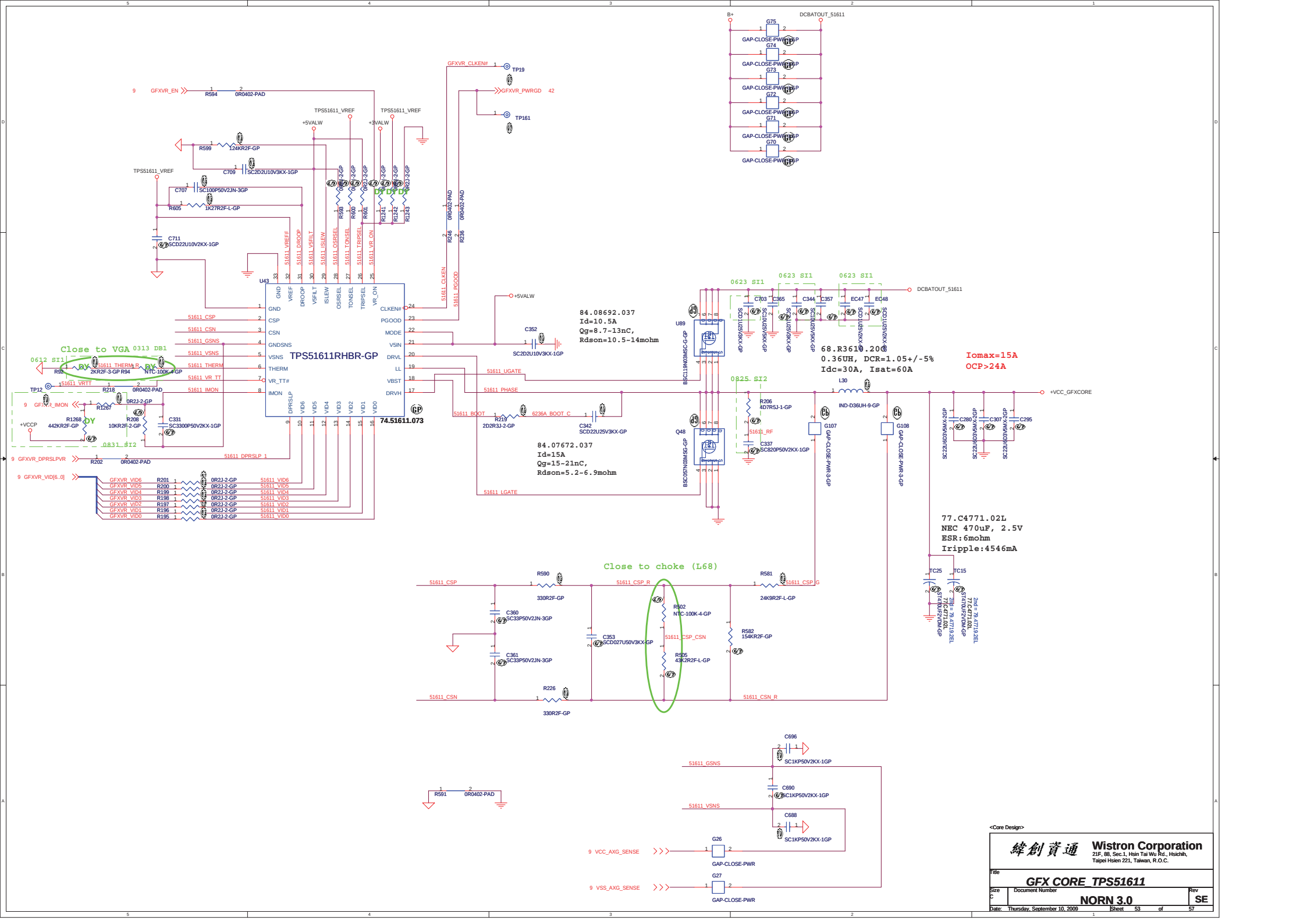
TPS51611RHBR-GP
74.51611.073
Close to VGA
Close to choke (L68)
84.08692.037
Id=10.5A
Qg=8.7~13nC,
Rdson=10.5~14mohm
84.07672.037
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
68.R3610.2DS
0.36UH, DCR=1.05+/-5%
Idc=30A, Isat=60A
Iomax=15A
OCP>24A
77.C4771.02L
NEC 470uF, 2.5V
ESR:6mohm
Iripple:4546mA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
GFX CORE_TPS51611
NORN 3.0
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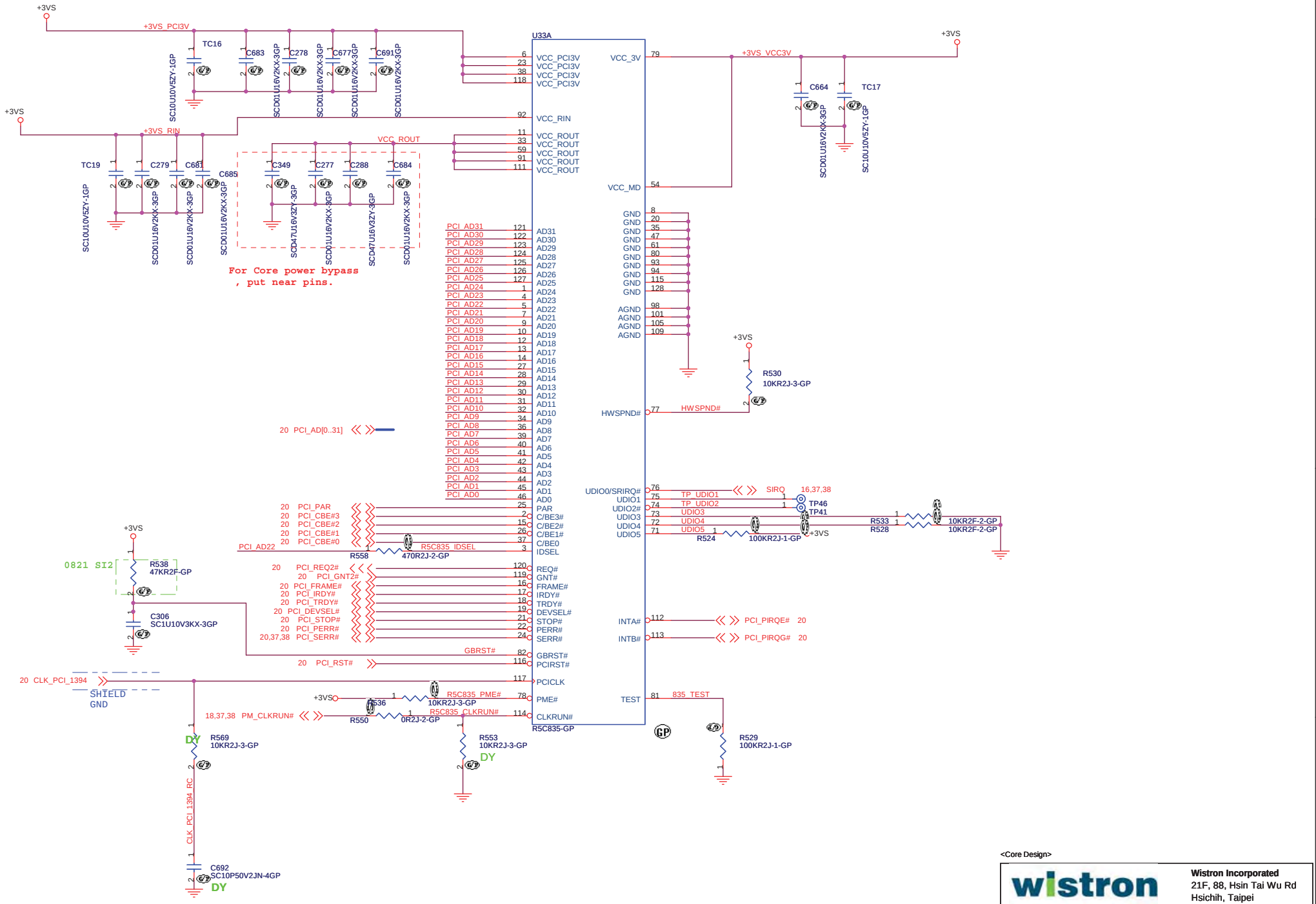
U33A
R5C835-GP
For Core power bypass , put near pins.
20 PCI_AD[0..31]
0821 SI2
SHIELD
GND
DY
<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
R5C835/PCI(1/2)
Size A3
Document Number
NORN 3.0
Rev SE
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Place C345 and C346, and X3 as close to R5C835 as possible.

GUARD GND

X3 should be 50 ppm or better.

X3
X-24D576MHZ-62GP
82.30023.511
2nd = 82.30023.611
XTAL 24.576M 12P30PPM HCX-5FA

Place R576 and C693 as close to R5C835 as possible.

GUARD GND

U33B

R5C835-GP

CLOSE TO CHIP R5C835

Layout notes :
external parts for VREF, REXT and FIL0 as close as possible to R5C835.

Layout Notes:

Make sure that the stubs to the test points(1394_XO) in the layout are as short as possible on the high speed signals.

Layout note :
Place these Caps
Close to R5C835

Layout notes :
1394

The shield GND is needed for SD_CLK(MDIO09).
Also, the wide-width (more than 0.02inch) trace for MDIO09 should be used.

SD_CLK need to 25mil

Place U41 within 2 inches of the card connector

40mil

For SD Card Power

Place resistor close to CARD1

Layout Note: Add guard GND around SD_CLK
Change +3VS_CARD to 40mils

Please ensure that TPA+/- and TPB+/- are routed the same wire length.

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Title: R5C835/IEEE1394/SD/Smart(2/2)

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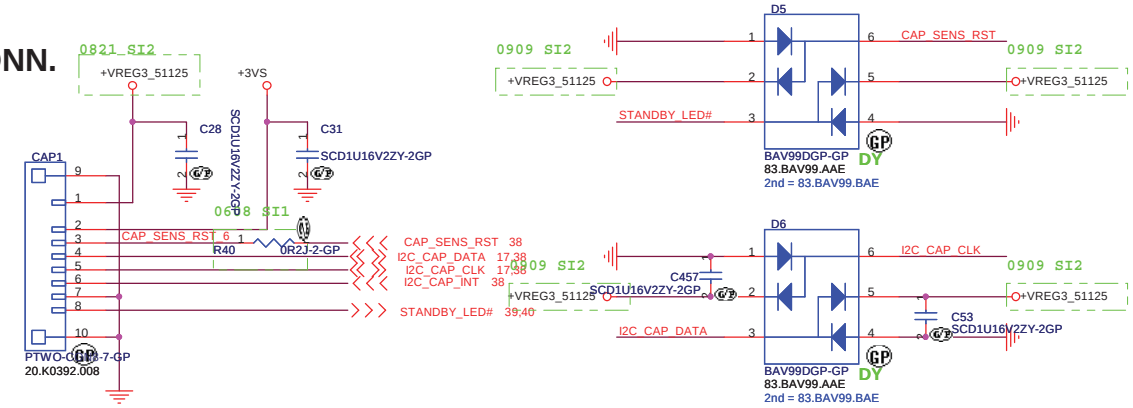
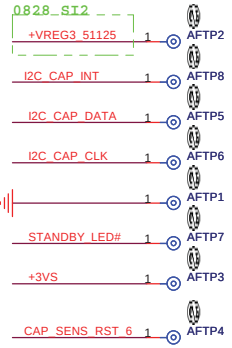
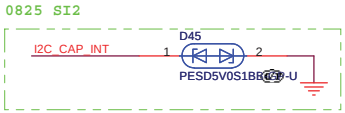
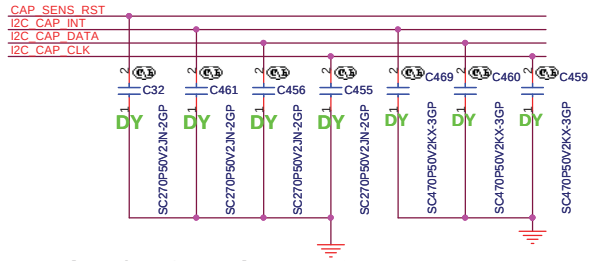
CAP BD CONN.



Vol up , Vol down , Mute ,Presentation







Place these 4 Caps close to CAP1.

<Core Design>

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Title: CAP CONN.

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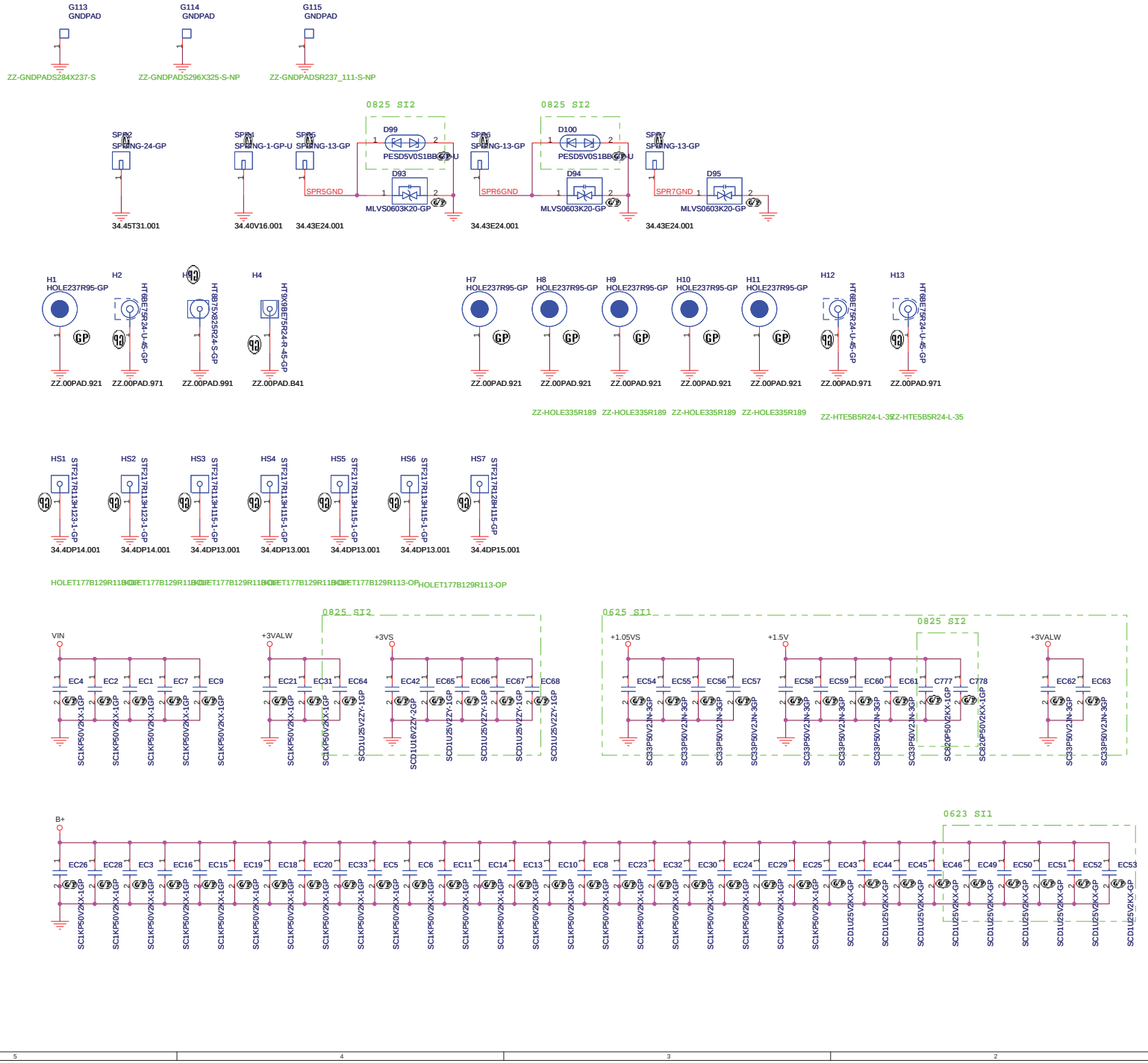
G113 GNDPAD
G114 GNDPAD
G115 GNDPAD
ZZ-GNDPADS284X237-S
ZZ-GNDPADS296X325-S-NP
ZZ-GNDPADSR237_111-S-NP
0825 SI2
0825 SI2
SPR2 SPRING-24-GP
SPR4 SPRING-1-GP-U
SPR5 SPRING-13-GP
SPR6 SPRING-13-GP
SPR7 SPRING-13-GP
D99 PESD5V0S1BB-GP-U
D100 PESD5V0S1BB-GP-U
D93 MLVS0603K20-GP
D94 MLVS0603K20-GP
D95 MLVS0603K20-GP
SPR5GND
SPR6GND
SPR7GND
34.45T31.001
34.40V16.001
34.43E24.001
34.43E24.001
34.43E24.001
H1 HOLE237R95-GP
H2 HT6BE75R24-U-45-GP
H3 HT8B75X825R24-S-GP
H4 HT9X9BE75R24-R-45-GP
H7 HOLE237R95-GP
H8 HOLE237R95-GP
H9 HOLE237R95-GP
H10 HOLE237R95-GP
H11 HOLE237R95-GP
H12 HT6BE75R24-U-45-GP
H13 HT6BE75R24-U-45-GP
ZZ.00PAD.921
ZZ.00PAD.971
ZZ.00PAD.991
ZZ.00PAD.B41
ZZ-HOLE335R189
ZZ-HTE5B5R24-L-35
HS1 STF217R113H123-1-GP
HS2 STF217R113H123-1-GP
HS3 STF217R113H115-1-GP
HS4 STF217R113H115-1-GP
HS5 STF217R113H115-1-GP
HS6 STF217R113H115-1-GP
HS7 STF217R128H115-GP
34.4DP14.001
34.4DP14.001
34.4DP13.001
34.4DP13.001
34.4DP13.001
34.4DP13.001
34.4DP15.001
HOLET177B129R113-OP
0825 SI2
0625 SI1
0825 SI2
VIN
+3VALW
+3VS
+1.05VS
+1.5V
+3VALW
+3VALW
EC4 EC2 EC1 EC7 EC9
EC21 EC31 EC64
EC42 EC65 EC66 EC67 EC68
EC54 EC55 EC56 EC57
EC58 EC59 EC60 EC61 C777 C778
EC62 EC63
SC1KP50V2KX-1GP
SCD1U25V2ZY-1GP
SC33P50V2JN-3GP
SC820P50V2KX-1GP
0623 SI1
B+
EC26 EC28 EC3 EC16 EC15 EC19 EC18 EC20 EC33 EC5 EC6 EC11 EC14 EC13 EC10 EC8 EC23 EC32 EC30 EC24 EC29 EC25 EC43 EC44 EC45 EC46 EC49 EC50 EC51 EC52 EC53
SC1KP50V2KX-1GP
SCD1U25V2KX-GP
<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
UNUSED PARTS/EMI Capacitors
Size Custom
Document Number
NORN 3.0
Rev
SE
Date: Thursday, September 10, 2009
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