

Compal Confidential

Schematics Document

AUBURNDALE/CLARKSFIELD with
Intel IBEX PEAK-M core logic

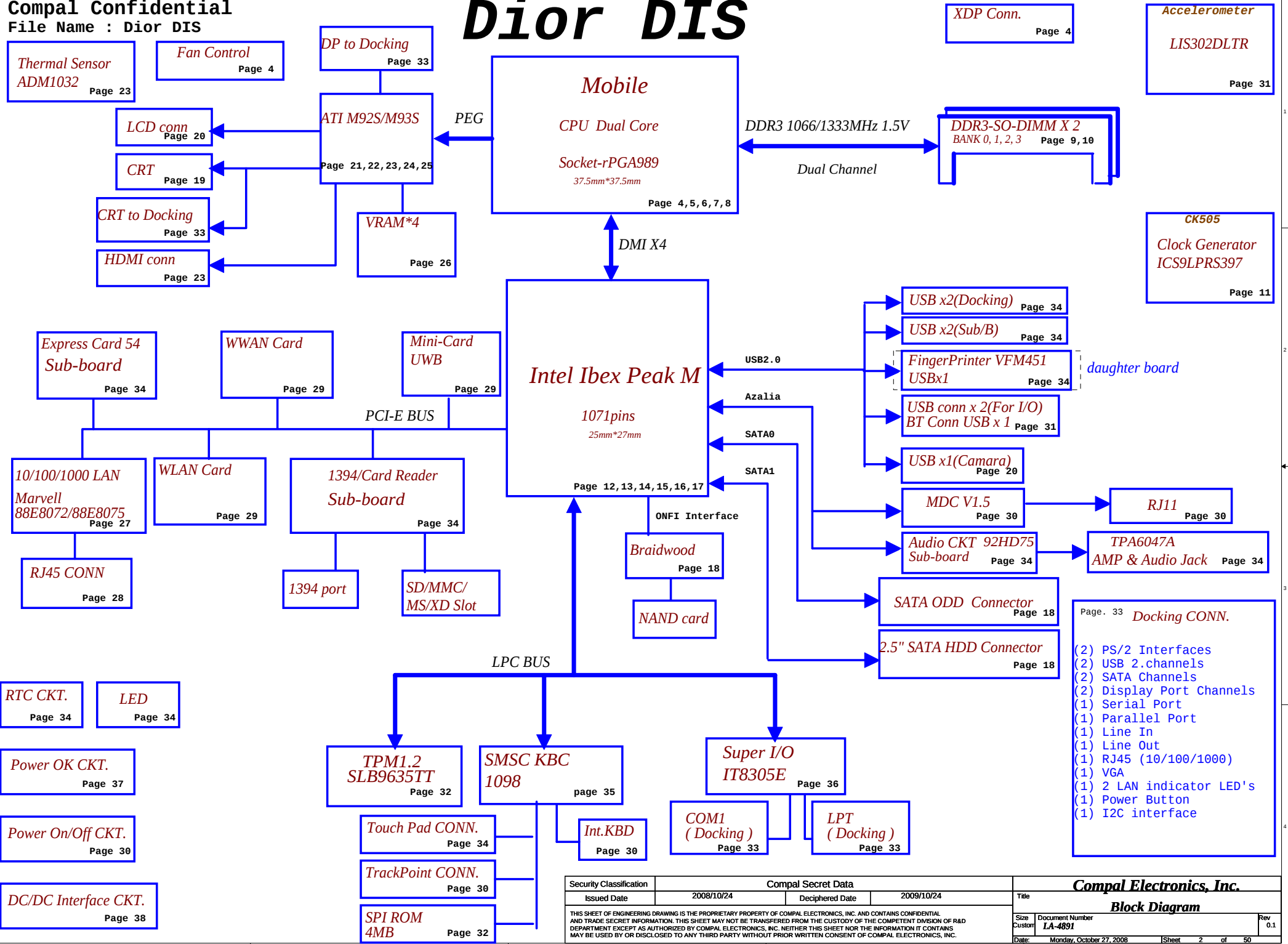
Dior DIS

2008-10-30

REV:0.1

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Issued Date	2008/10/24	Deciphered Date	2009/10/24	Cover Sheet		
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				Date: Thursday, October 30, 2008 Sheet 1 of 50		

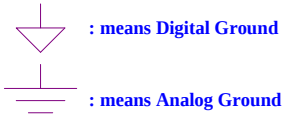
Dior DIS



Voltage Rails (0 MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B +3VL	+5VALW +3VALW	+1.5V +0.75V	+5VS +3VS +1.5VS +NVVDD +VCCP +CPU_CORE +1.05VS +1.8VS
S0	0	0	0	0	0
S1	0	0	0	0	0
S3	0	0	0	0	X
S5 S4/AC	0	0	0	X	X
S5 S4/ Battery only	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X

Symbol Note :



Install below 43 level BOM structure for ver. 0.1

- DEBUG@ : means just build when PCIE port 80 CARD function enable. Remove before MP
- M92@ : Install for M92 Graphic controller
- 8072@ : Install for 8072 NIC controller
- 1098@ : Install for 1098 KBC controller
- CK32@ : Install for 32 pin CLOCK GEN

Install below 45 level BOM structure for ver. 0.1

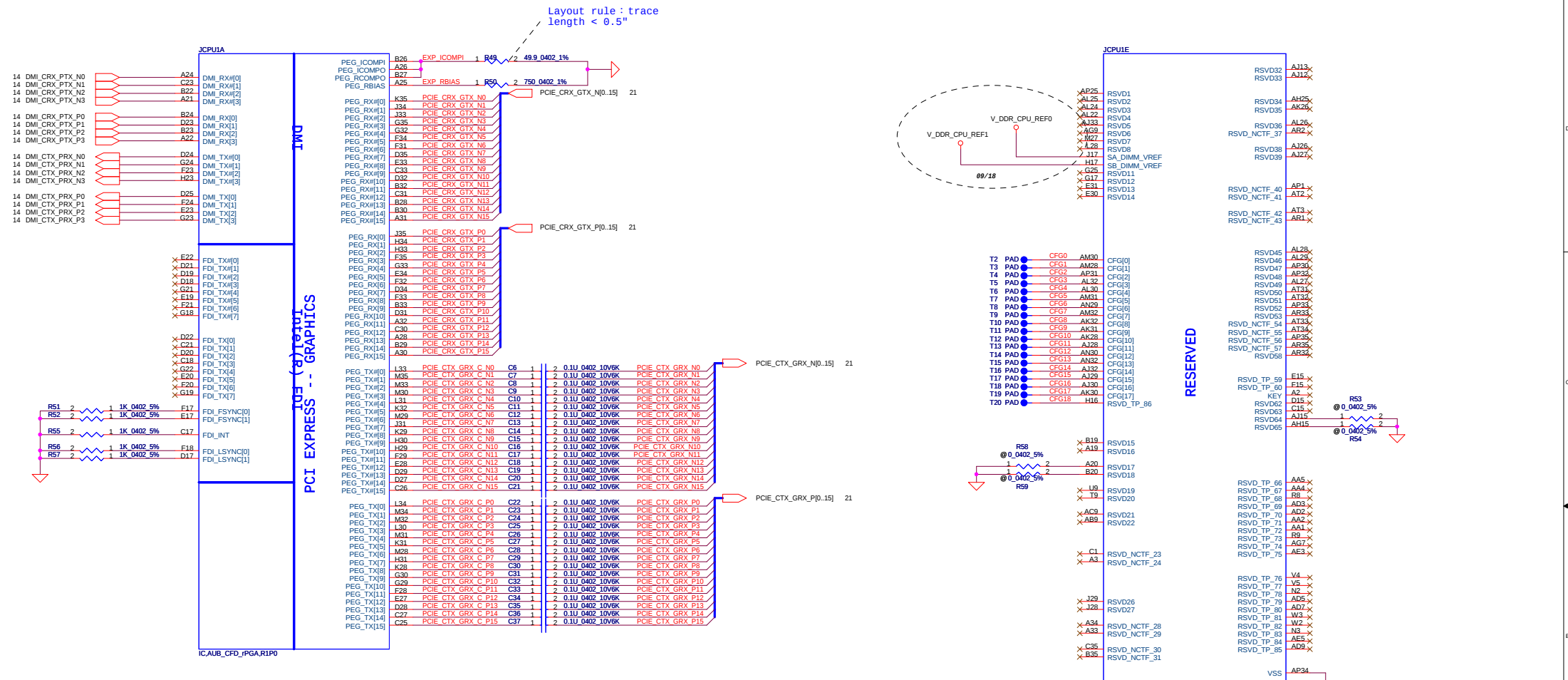
- 45@ : means just put it in the BOM of 45 level.

Reserve below BOM structure for ver. 0.1

- @ : means just reserve , no build
- CONN@ : means ME part.
- M93@ : Install for M93 Graphic controller
- 8075@ : Install for 8075 NIC controller
- 1091@ : Install for 1091 KBC controller
- CK72@ : Install for 72 pin CLOCK GEN

SMBUS Control Table

	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	V	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	X



CFG Straps for PROCESSOR

CFG0 $\text{R60} @ 3.01K_0.0402_1\%$

PCI-Express Configuration Select
1: Single PEG
0: Bifurcation enabled
Not applicable for Clarkfield Processor

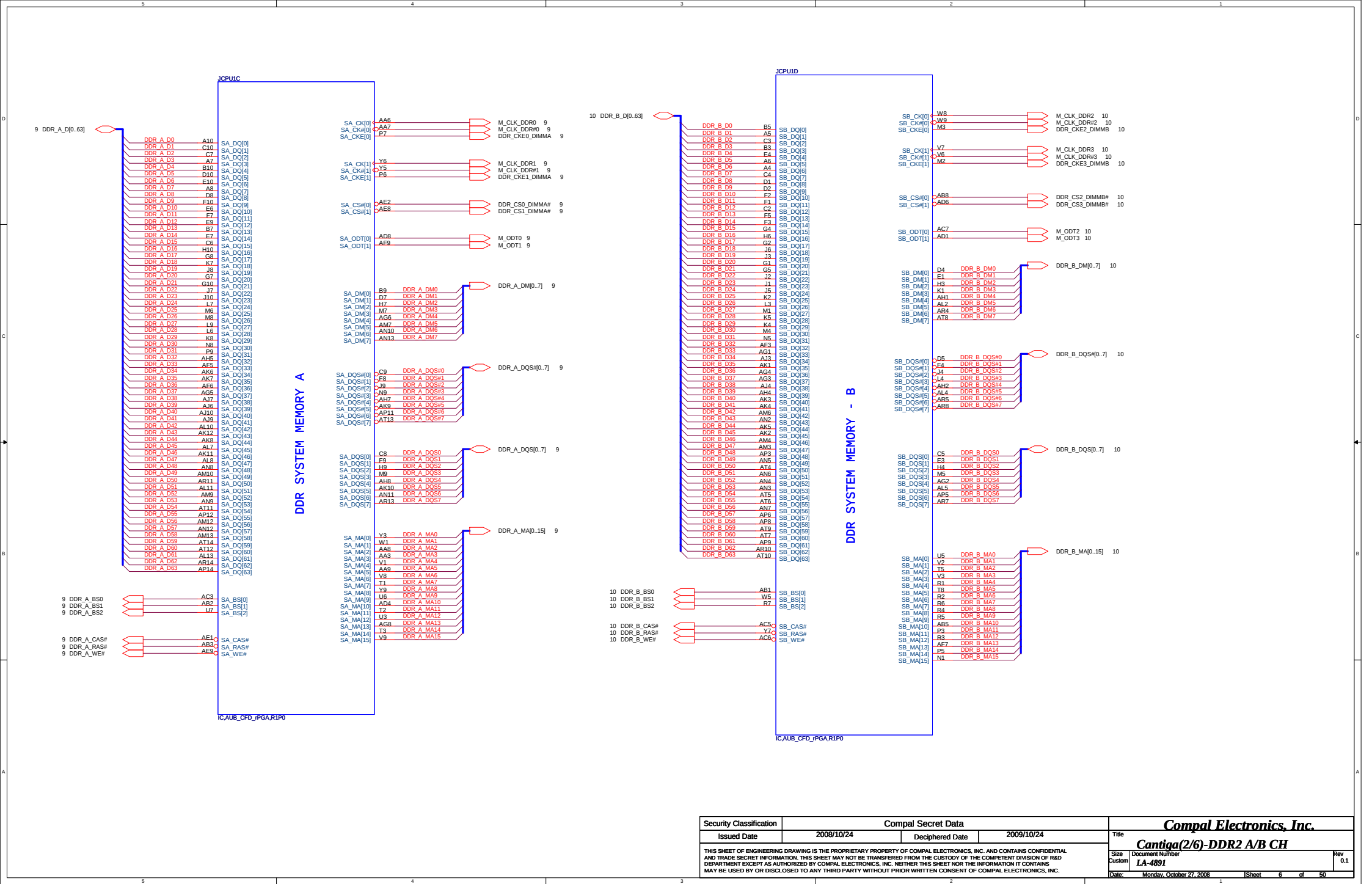
CFG3 $\text{R62} @ 3.01K_0.0402_1\%$

CFG3-PCI Express Static Lane Reversal
1: Normal Operation
0: Lane Numbers Reversed
15 -> 0, 14 -> 1,

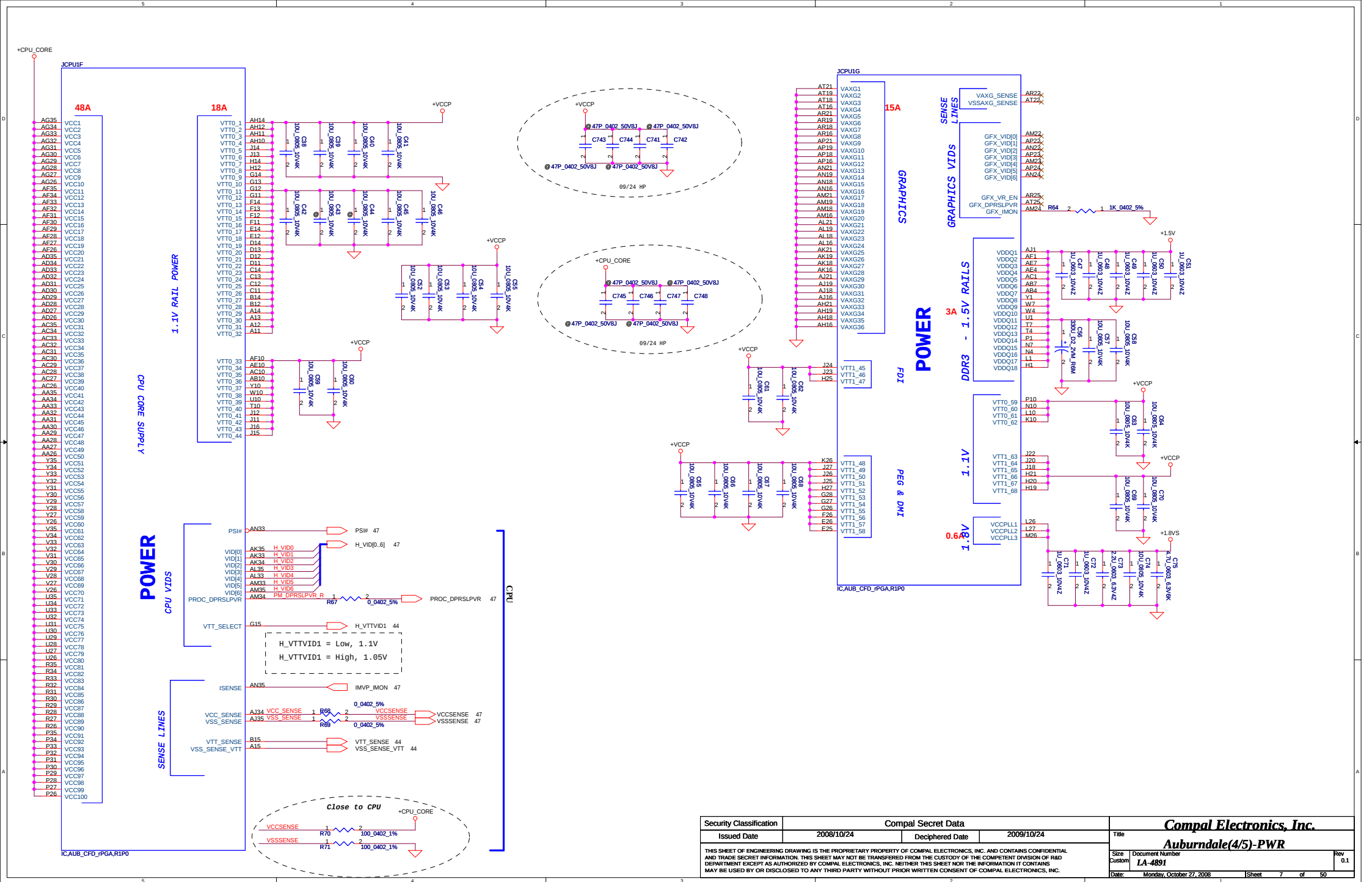
CFG4 $\text{R63} @ 3.01K_0.0402_1\%$

CFG4-Display Port Presence
1: Disabled; No Physical Display Port attached to Embedded Display Port
0: Enabled; An external Display Port device is connected to the Embedded Display Port

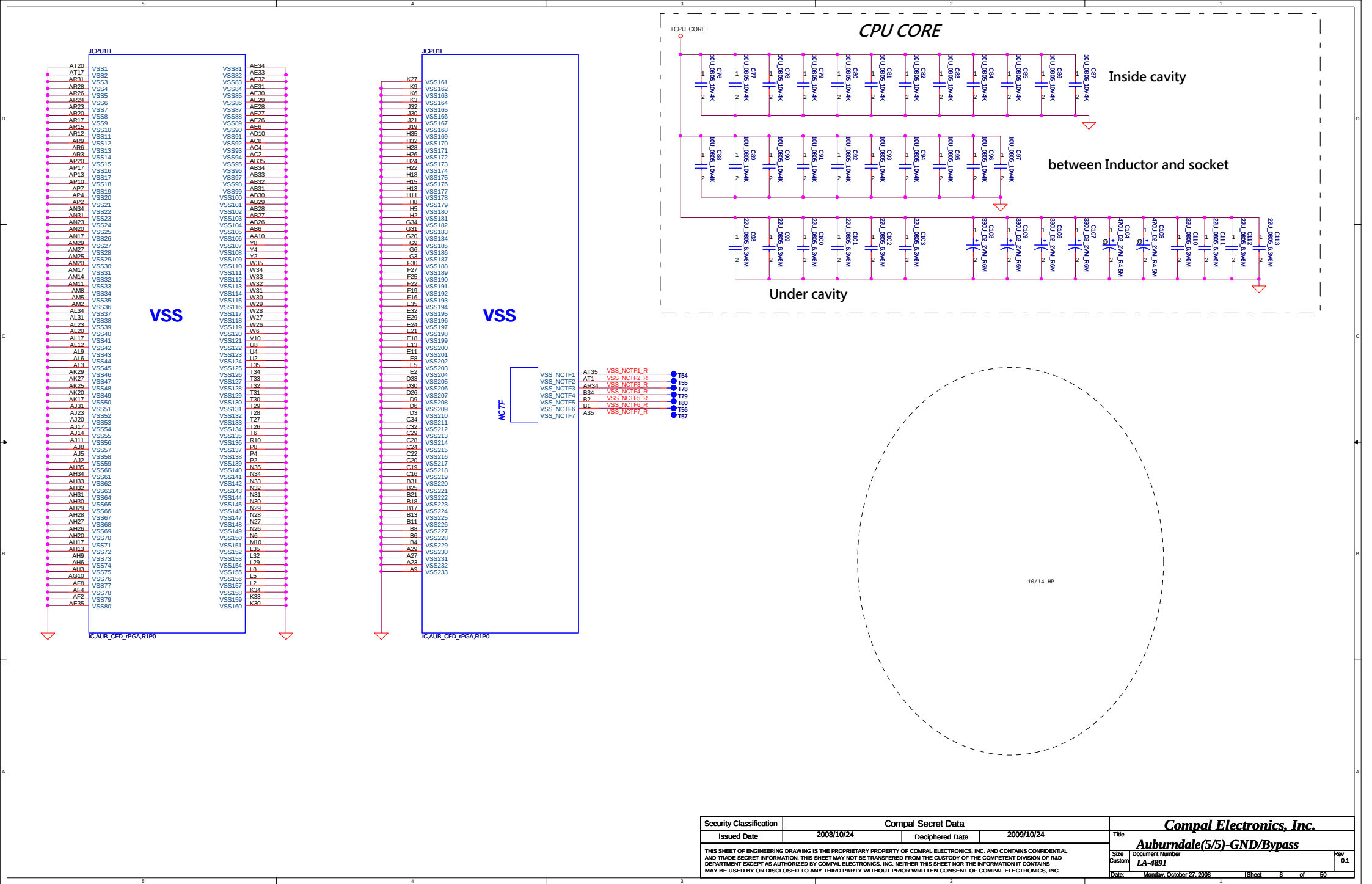
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				Document Number	
				Rev	
		LA-4981		0.1	
		Date: Monday, October 27, 2008		Sheet 5 of 50	



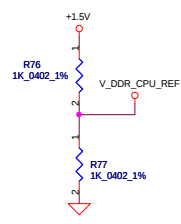
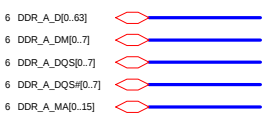
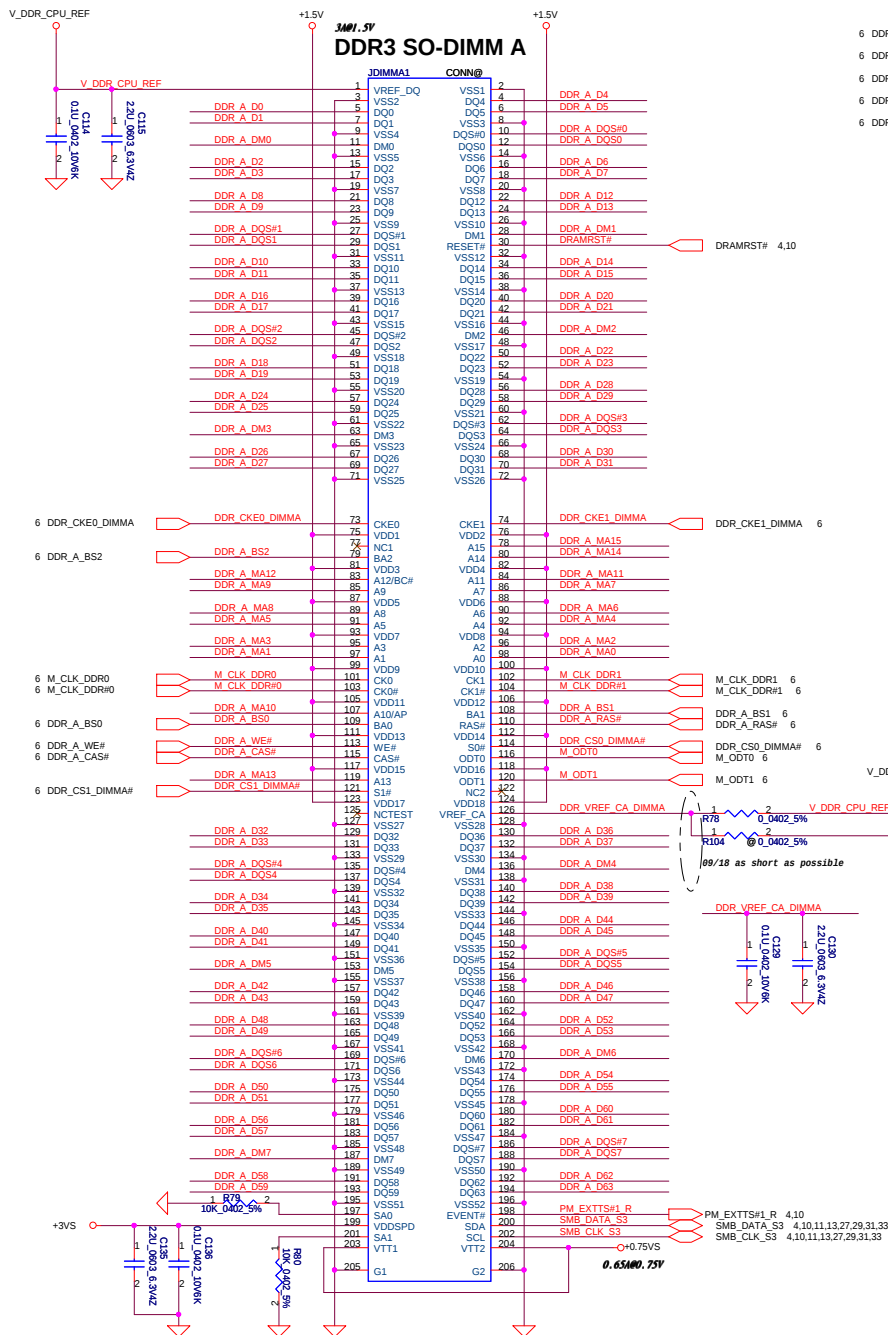
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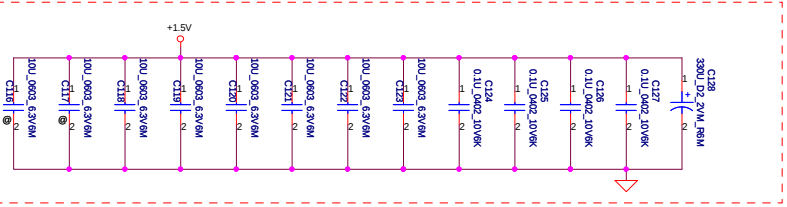


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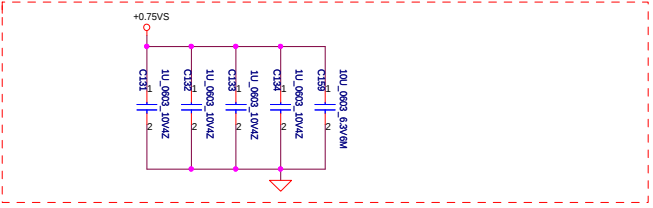


VREFDQ			
M1	V_DDR_CPU_REF	R76, R77, R78, R81,	
M3	V_DDR_CPU_REF0	R104, R110	

Layout Note:
Place near DIMM

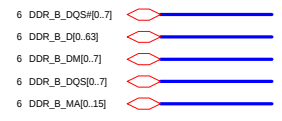
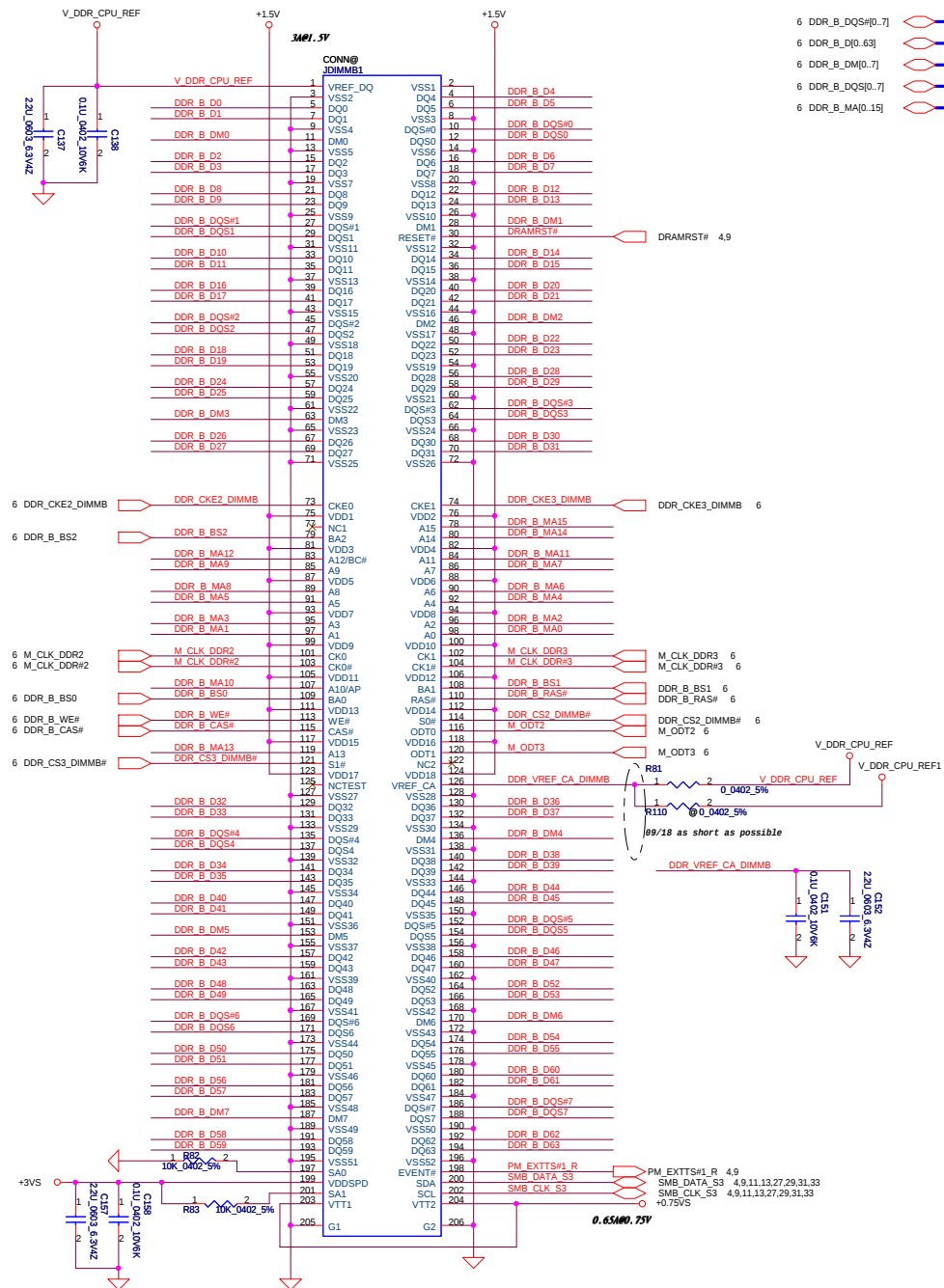


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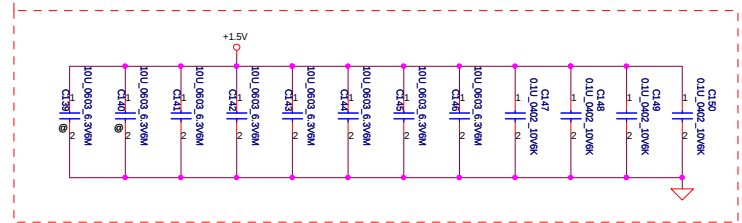


TOP SLOT

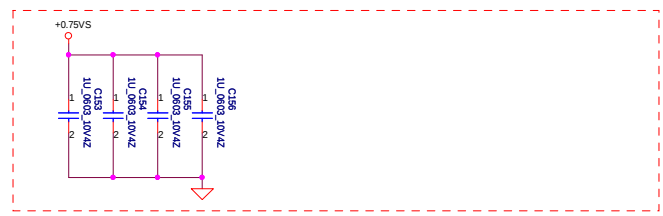
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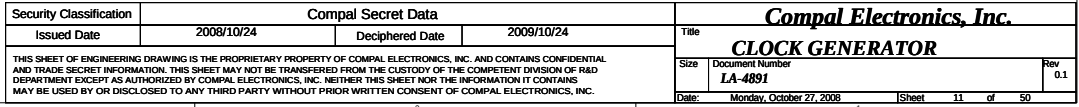


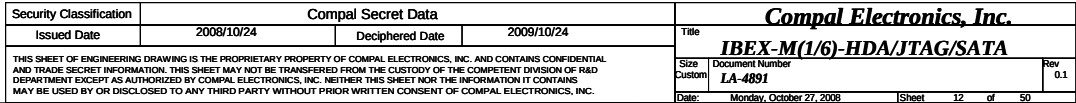
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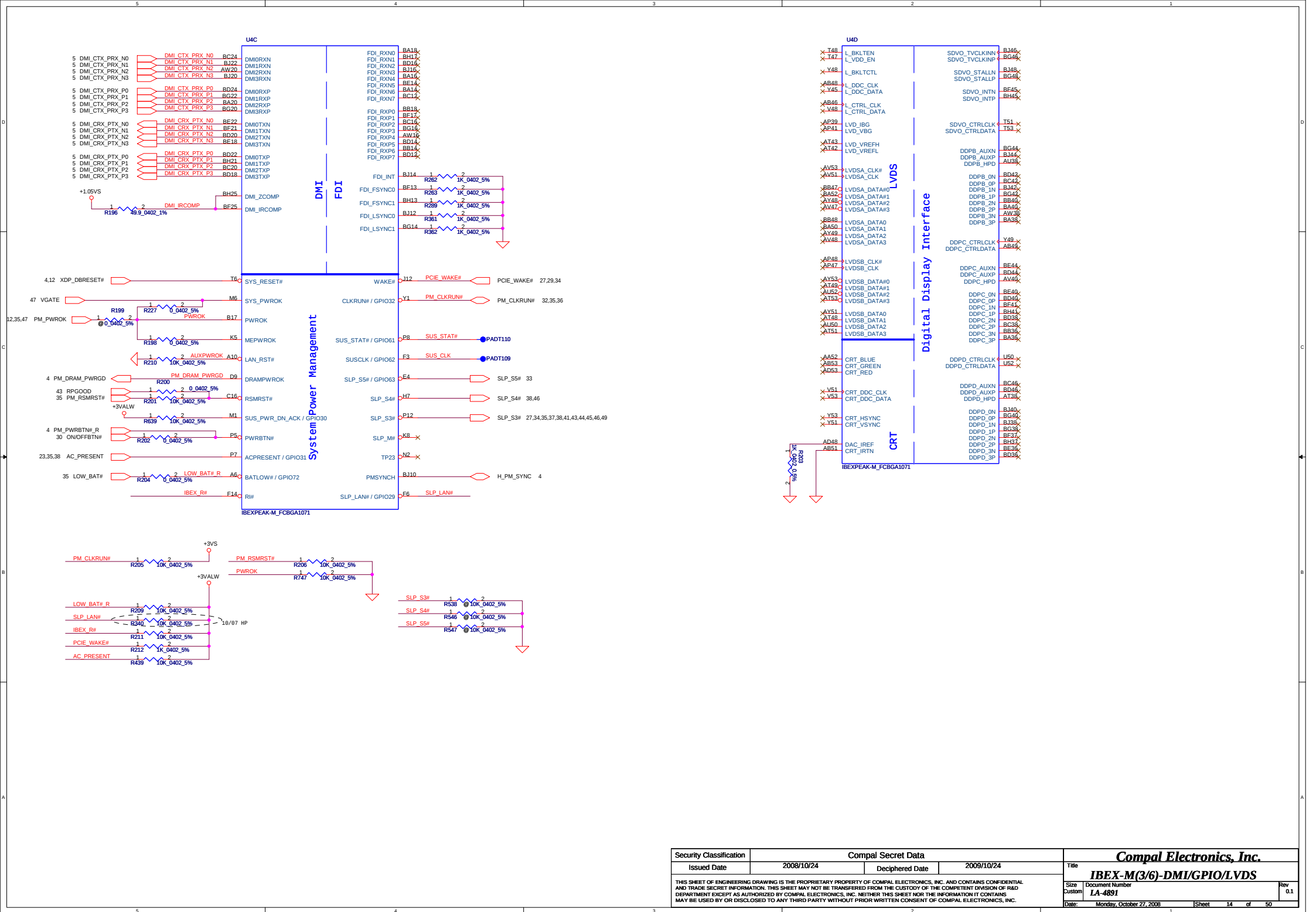


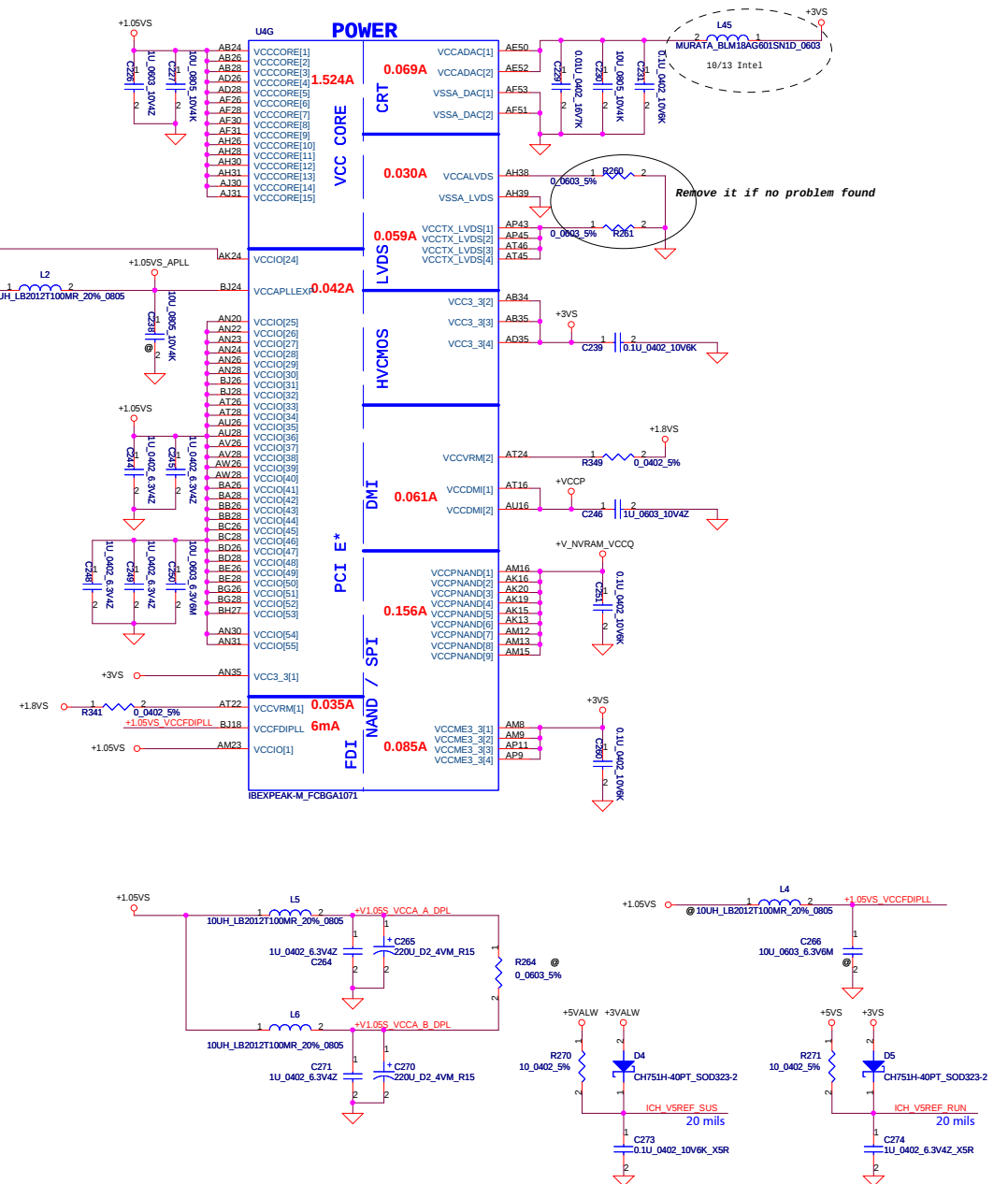
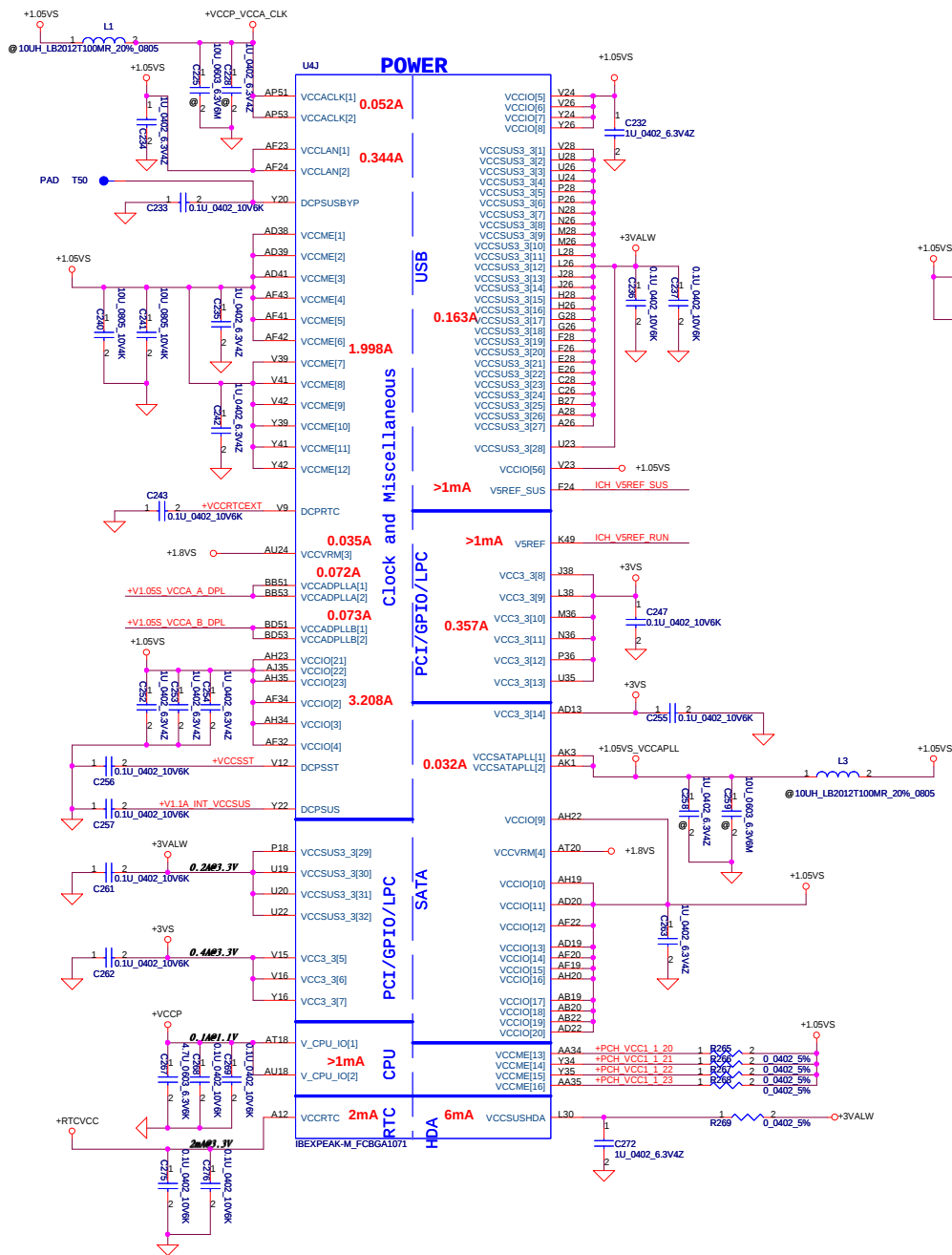
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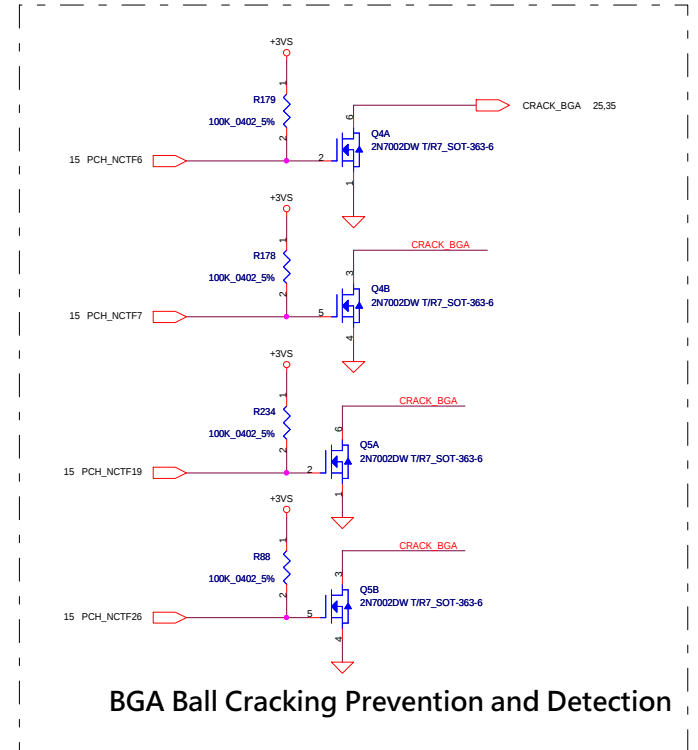
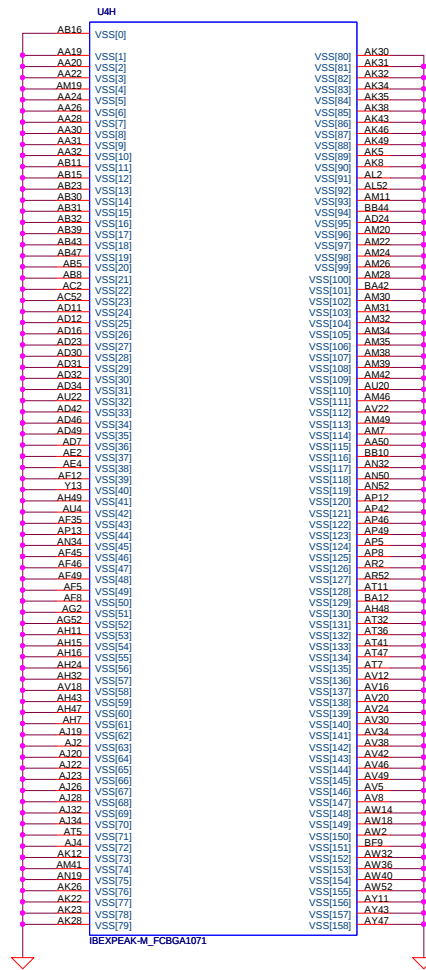
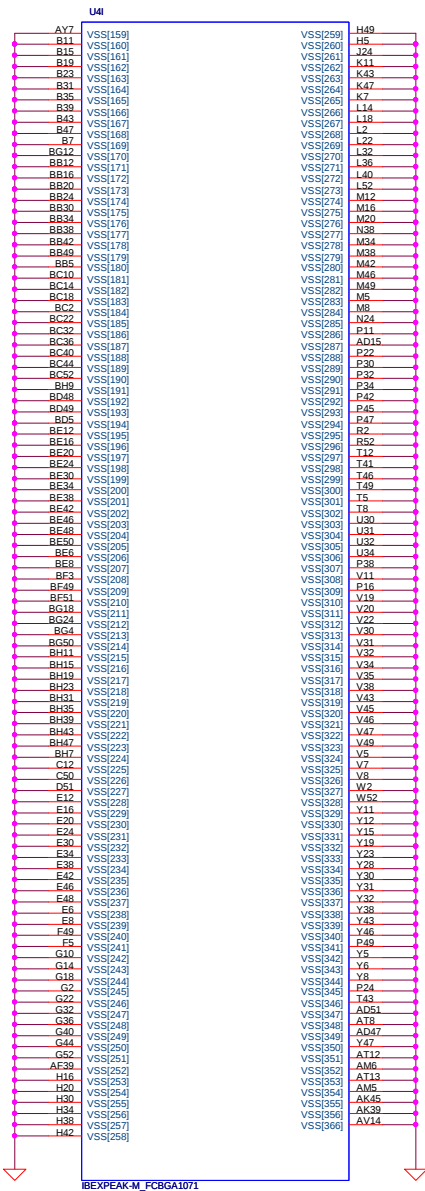






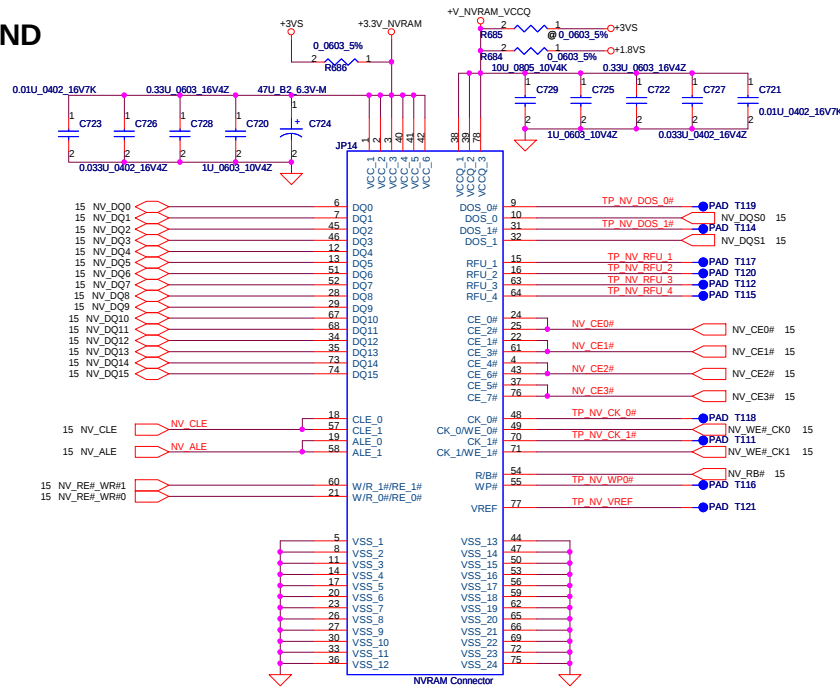


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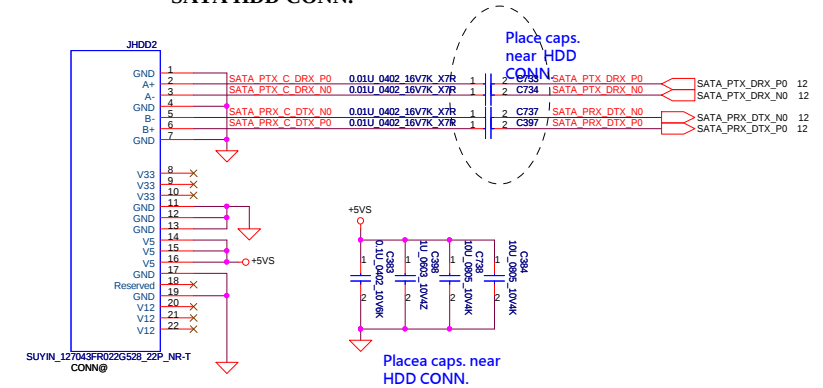


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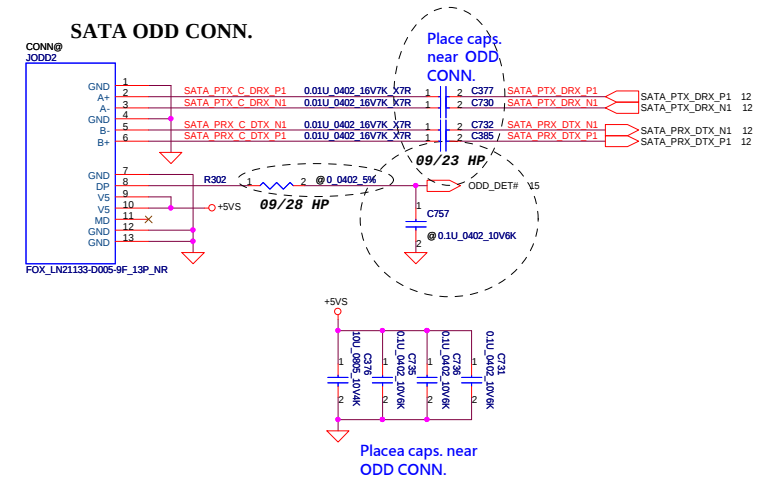
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SATA HDD CONN.

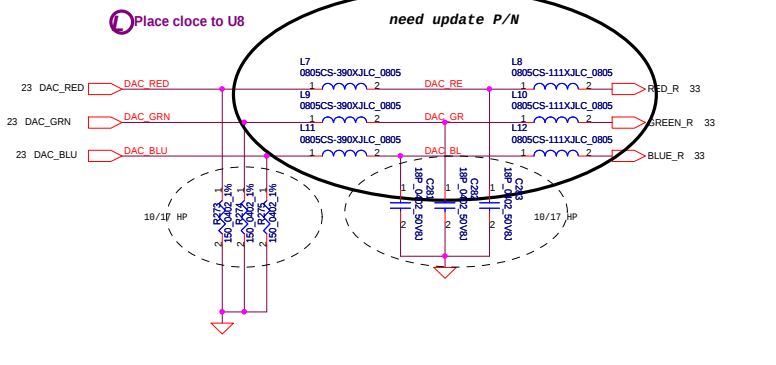
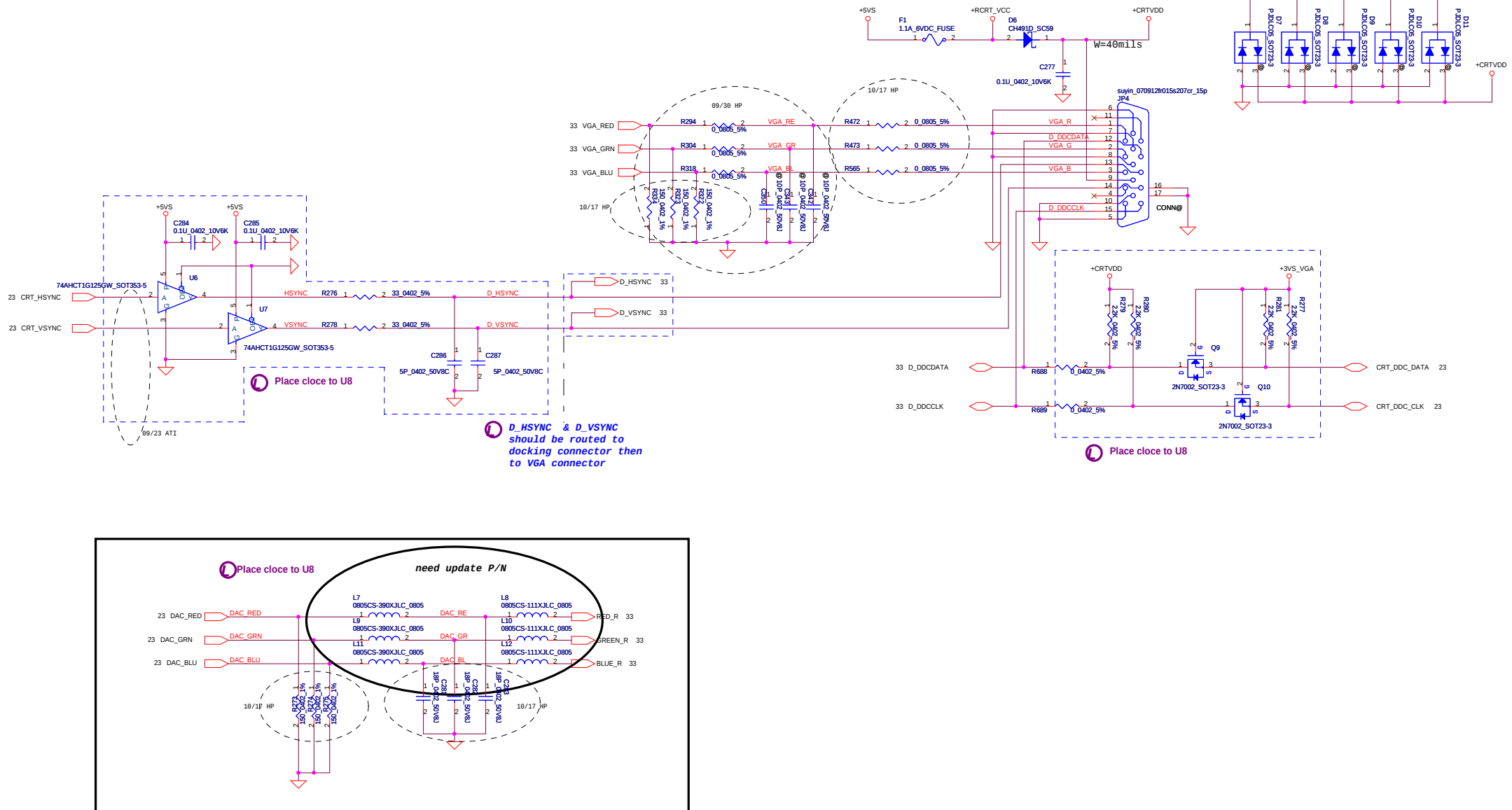


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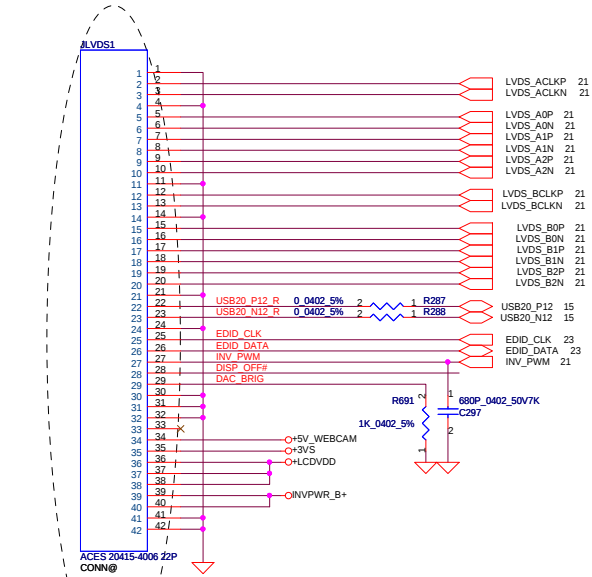
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CRT Connector

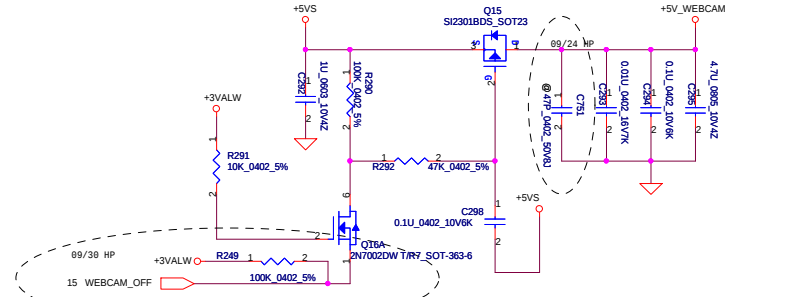
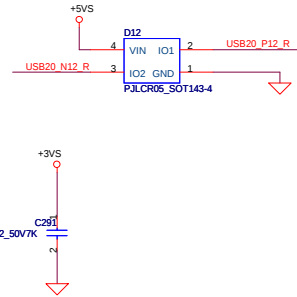
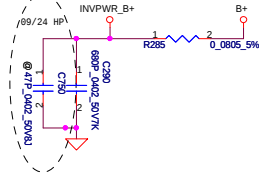
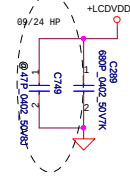


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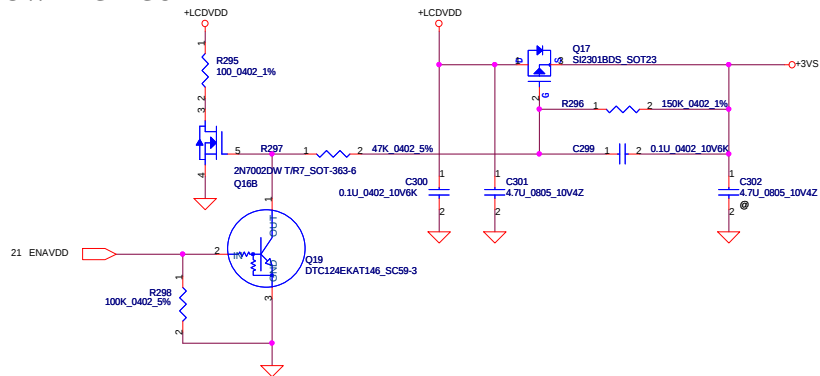
LCD/PANEL BD. CONN.



10/01 Change the footprint

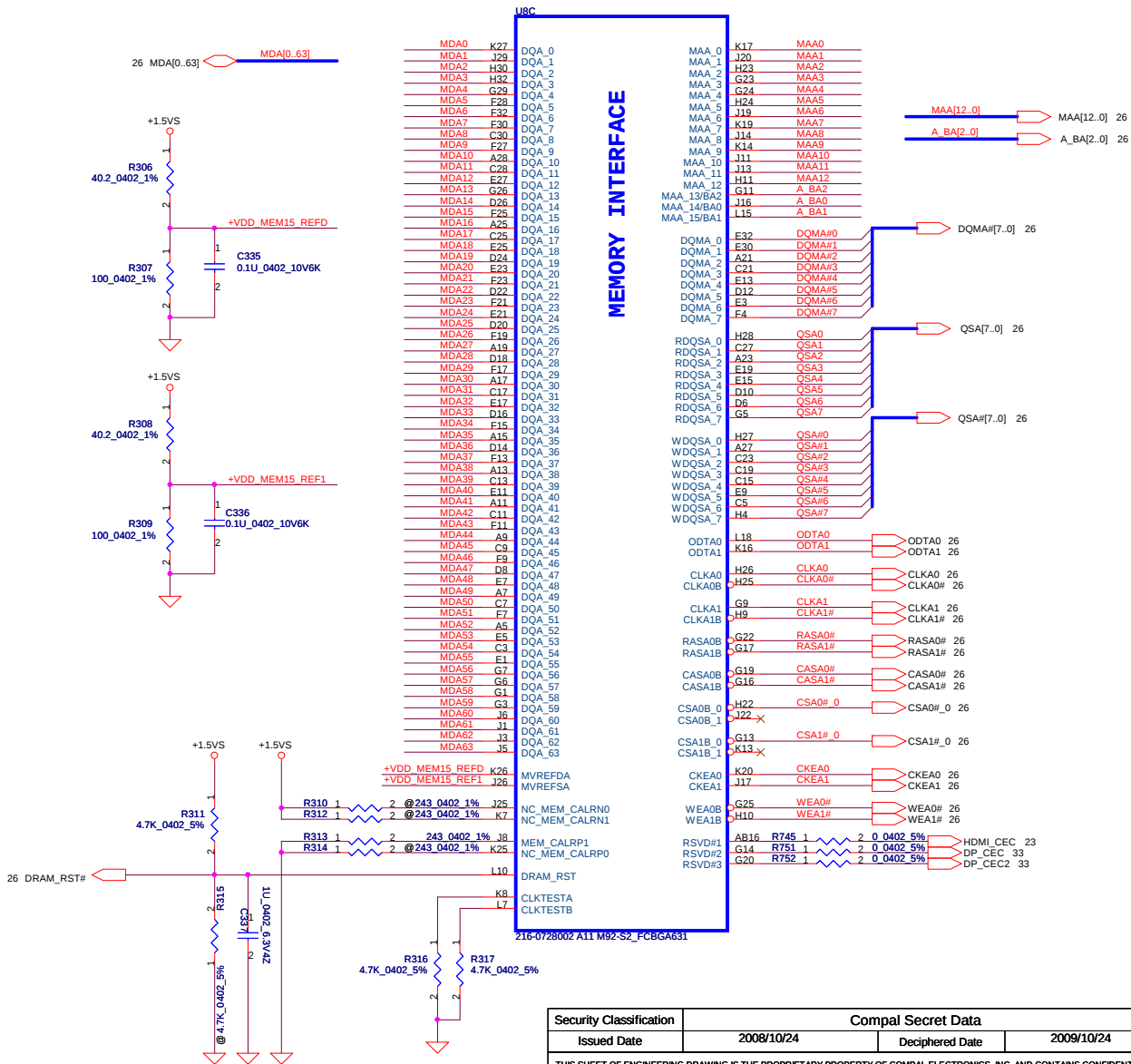


LCD POWER CIRCUIT

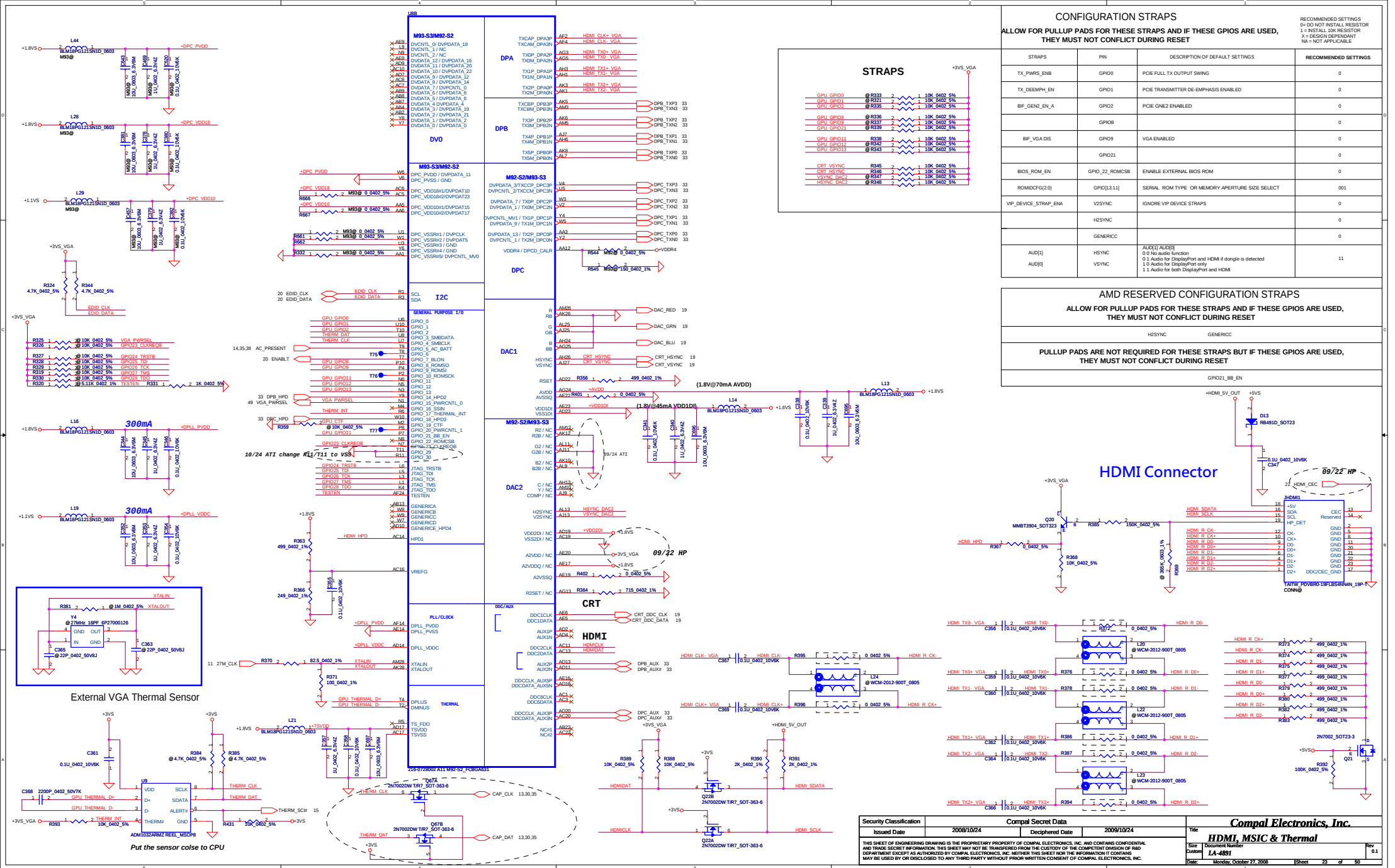


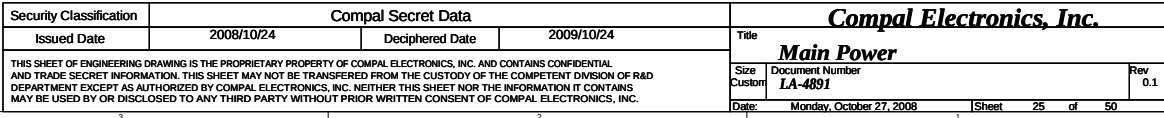
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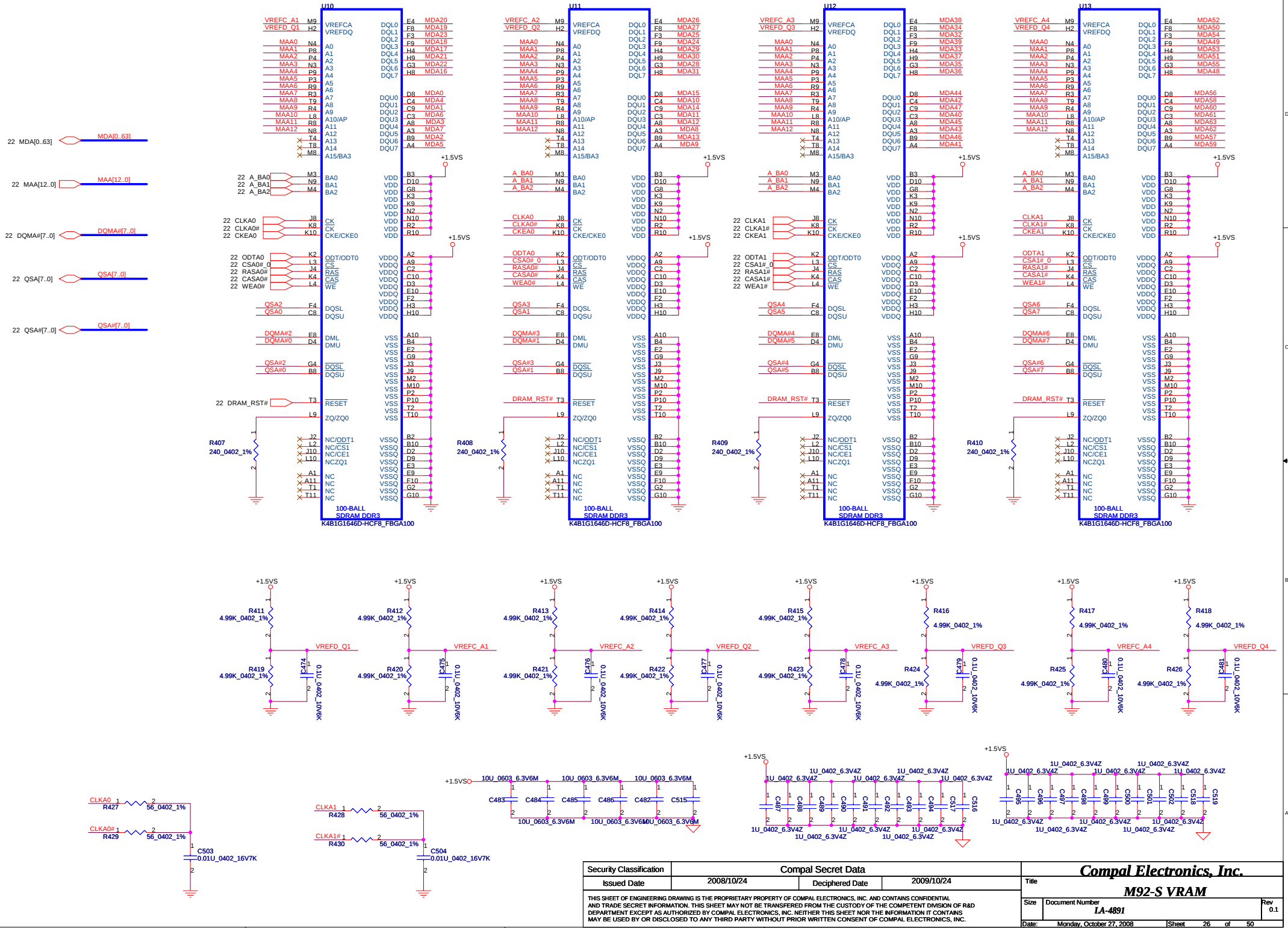
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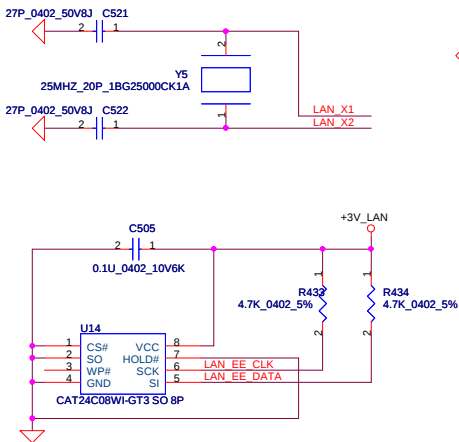
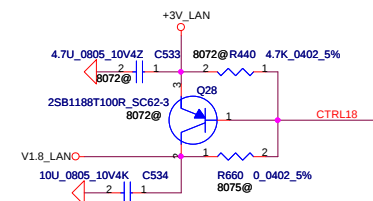
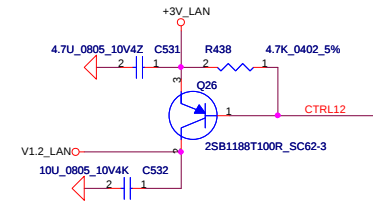
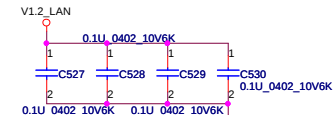
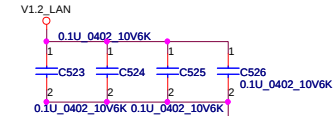
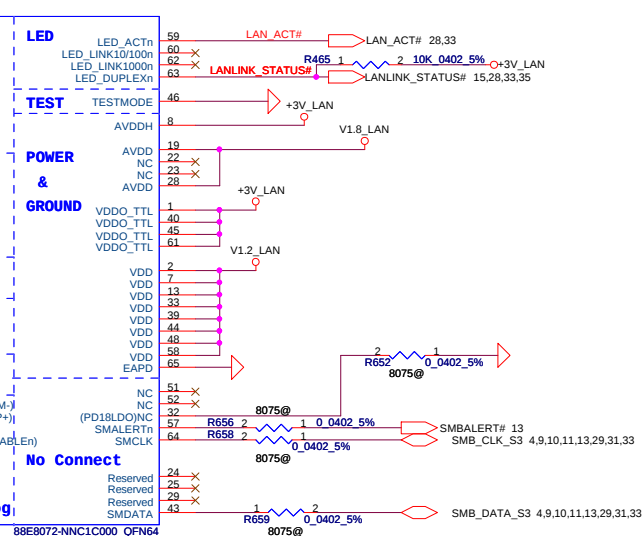
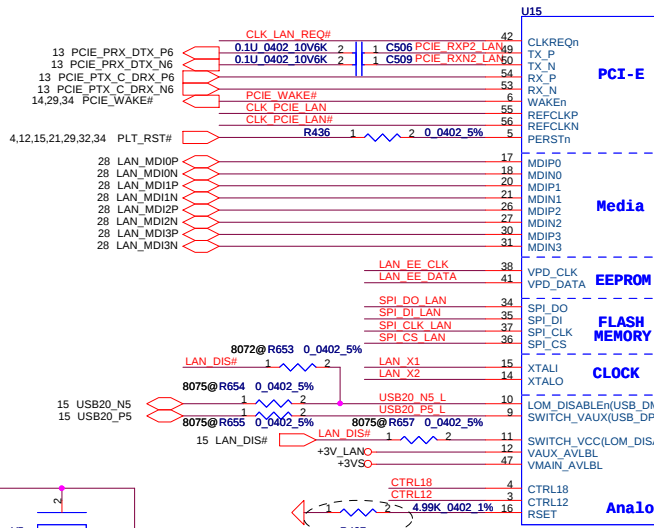
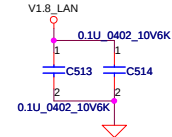
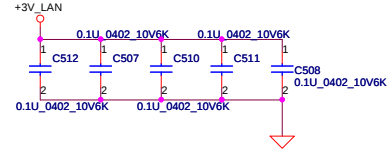
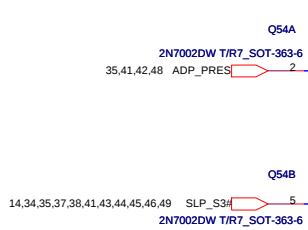
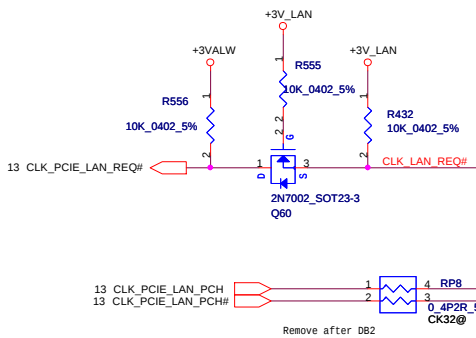
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/10/24	Deciphered Date	2009/10/24	Title	Memory Interface
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				Document Number	0.1
				LA-4891	
				Date:	Monday, October 27, 2008
				Sheet	22 of 50



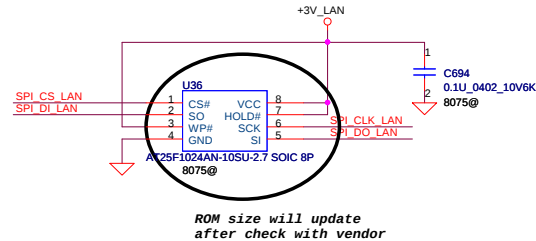




Security Classification				Compal Secret Data				Title			
Issued Date				2008/10/24				Deciphered Date			
				2009/10/24				2009/10/24			
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								LA-4891			
								Rev 0.1			
								Date: Monday, October 27, 2008			
								Sheet 26 of 50			

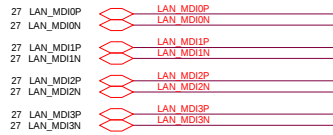


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Insert	R653	R654
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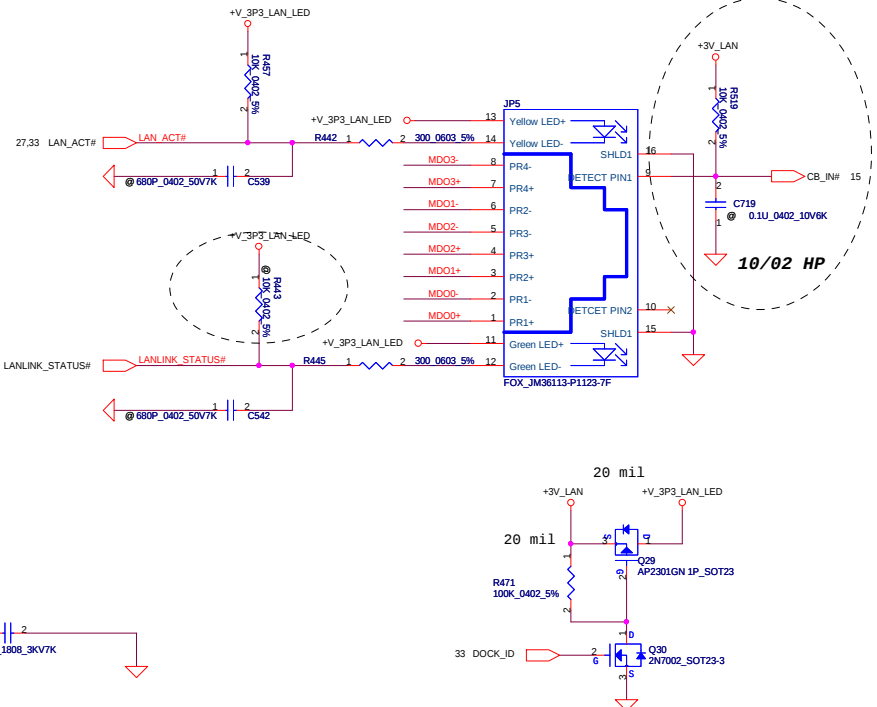
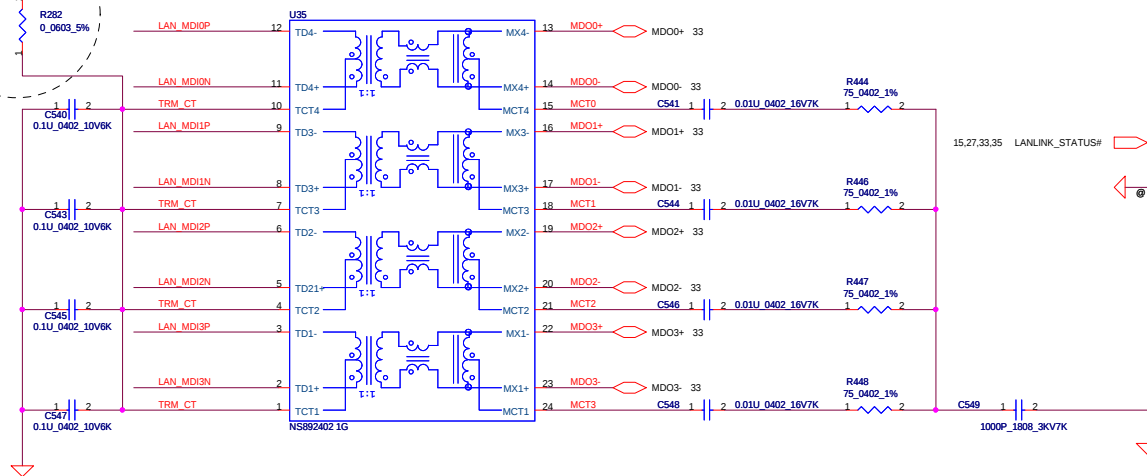


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						Date		Monday, October 27, 2008			Sheet 27 of 50	

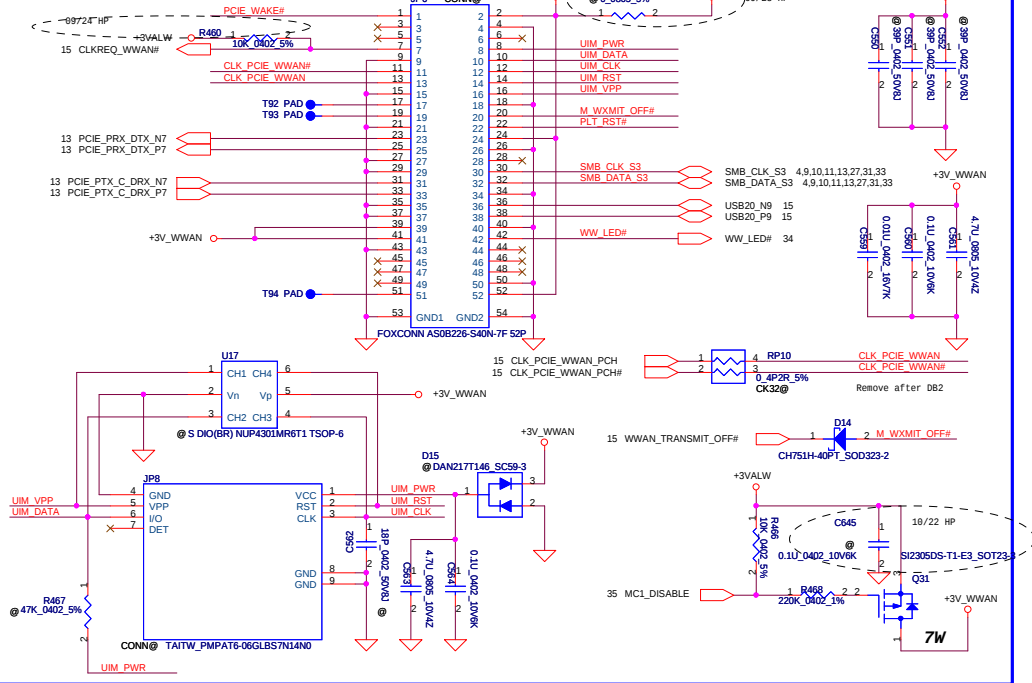
10/15 HP



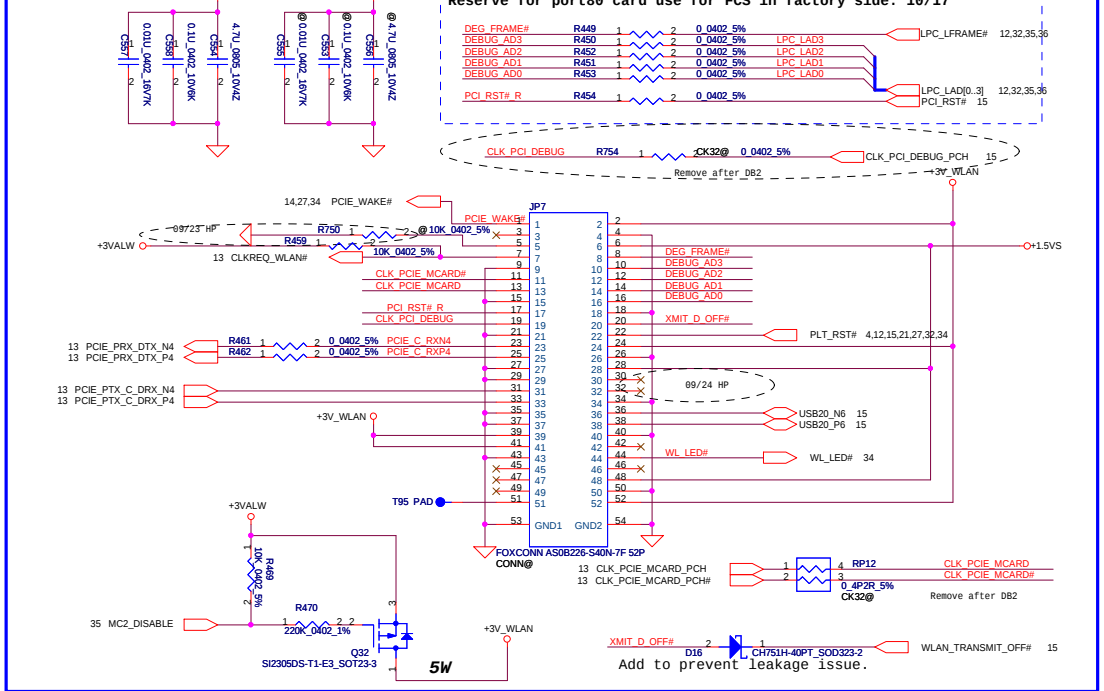
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WWAN

WLAN



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				WWAN/NAND mini		
				Size	Document Number LA-4891	
Date:				Wednesday, October 29, 2008		
Sheet				29 of 50		

[illegible]

MDC 1.5 Conn.

JP13
CONN# ACES_88020-12101_12P

12 HDA_SDOUT_MDC
12 HDA_SYNC_MDC
12 HDA_SDIIN1_MDC
12 HDA_RST#_MDC
15 MODEM_DISABLE#
12 HDA_BIT_CLK_MDC

R482 33_0402 5%
R493 0 0402 5%
C586 @ 10P_0402_50V/BJ

+3VALW
U18
MC74AHC1G08DFT2G SC70 5P

+3VS
C585 0.1u 0402 10V/K
C584 1000P 0402 50V/7K
C583 4.7u 0905 10V/4Z

1 2 3 4 5 6 7 8 9 10 11 12
GND GND GND GND GND GND GND GND GND GND GND GND

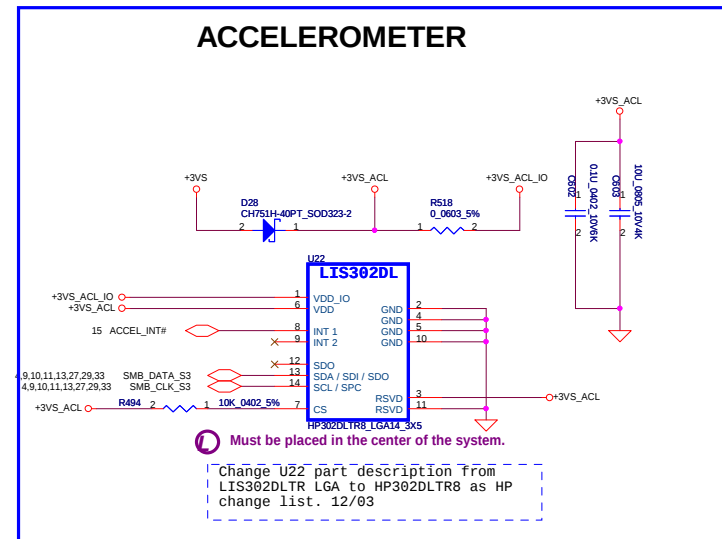
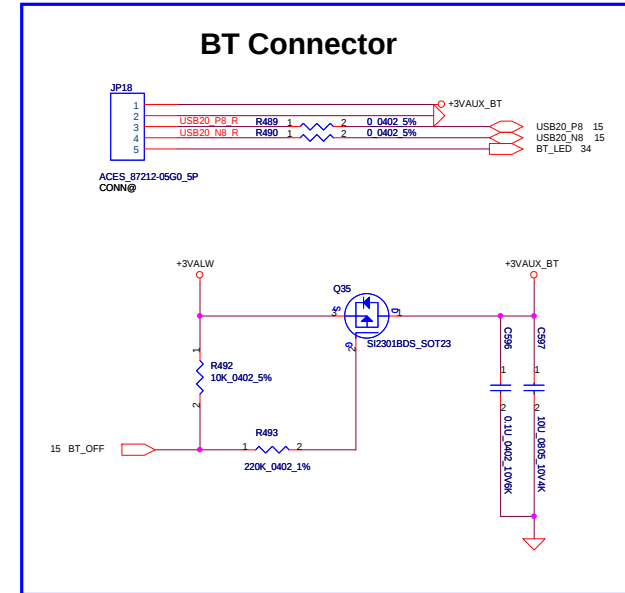
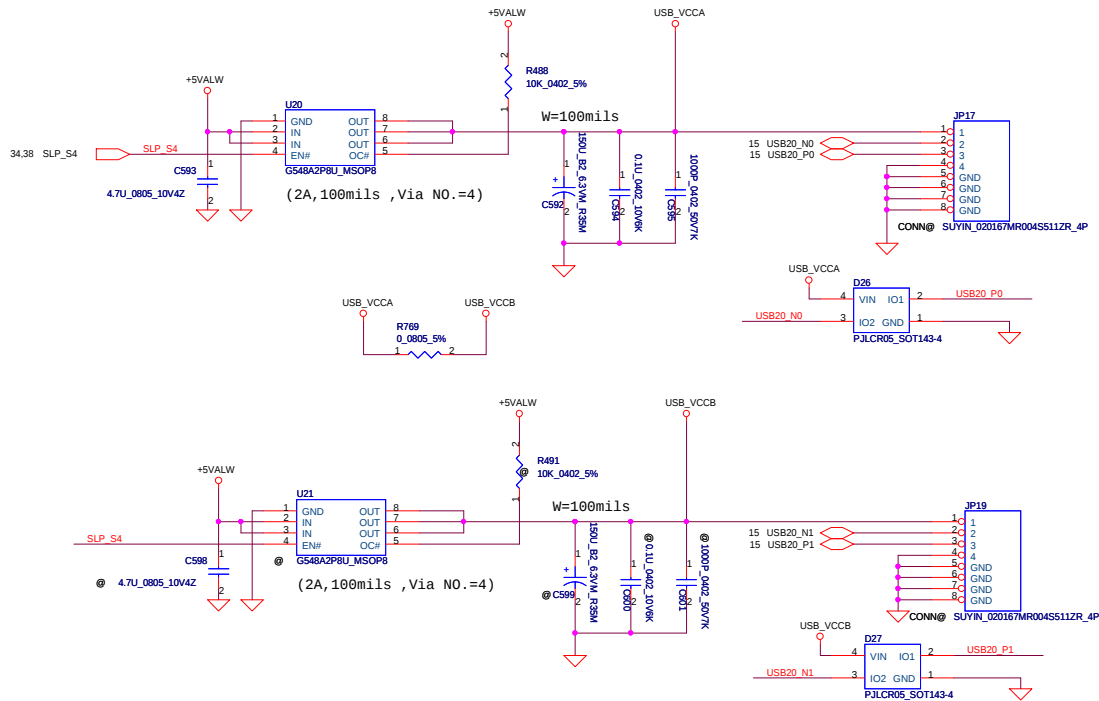
1 2 3 4 5 6 7 8 9 10 11 12
HDA_SDOUT_MDC HDA_SYNC_MDC HDA_SDIIN1_MDC HDA_RST#_MDC MODEM_DISABLE# HDA_BIT_CLK_MDC HDA_RESET# HDA_BITCLK

Power button

[illegible]

TrackPoint CONN.

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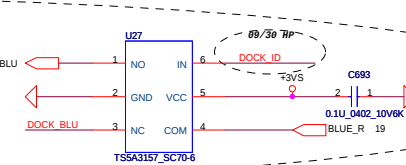
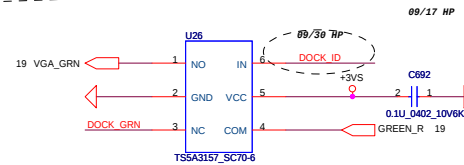
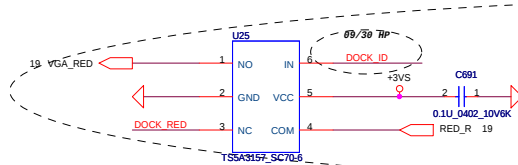
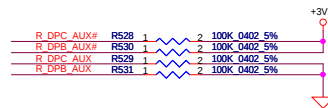
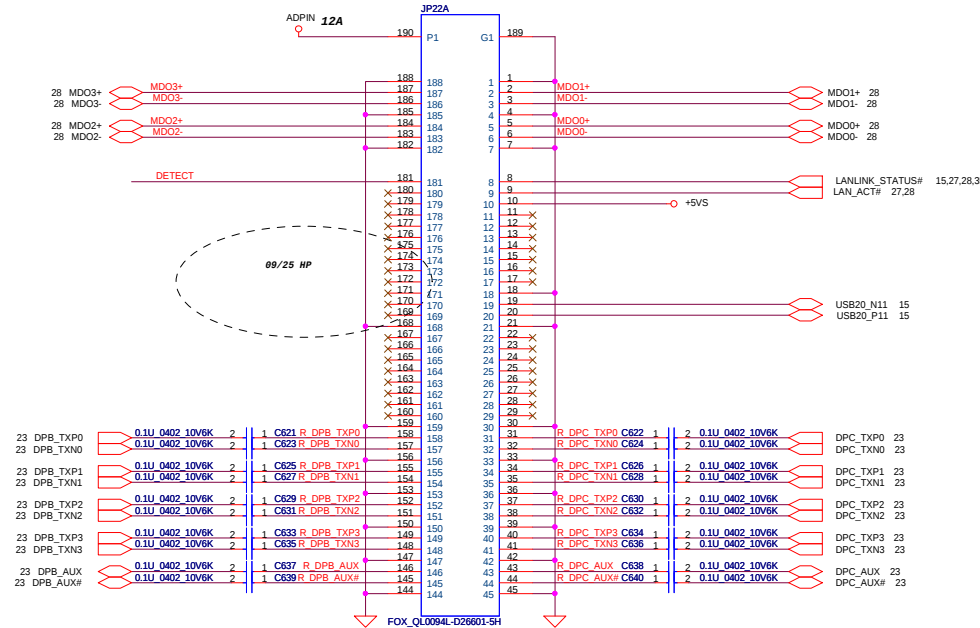
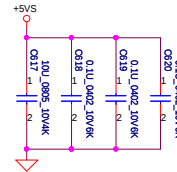
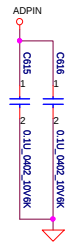


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Date: Monday, October 27, 2008				Sheet	31 of 50

DOCK CONN. 190PIN

DOCKING CONNECTOR

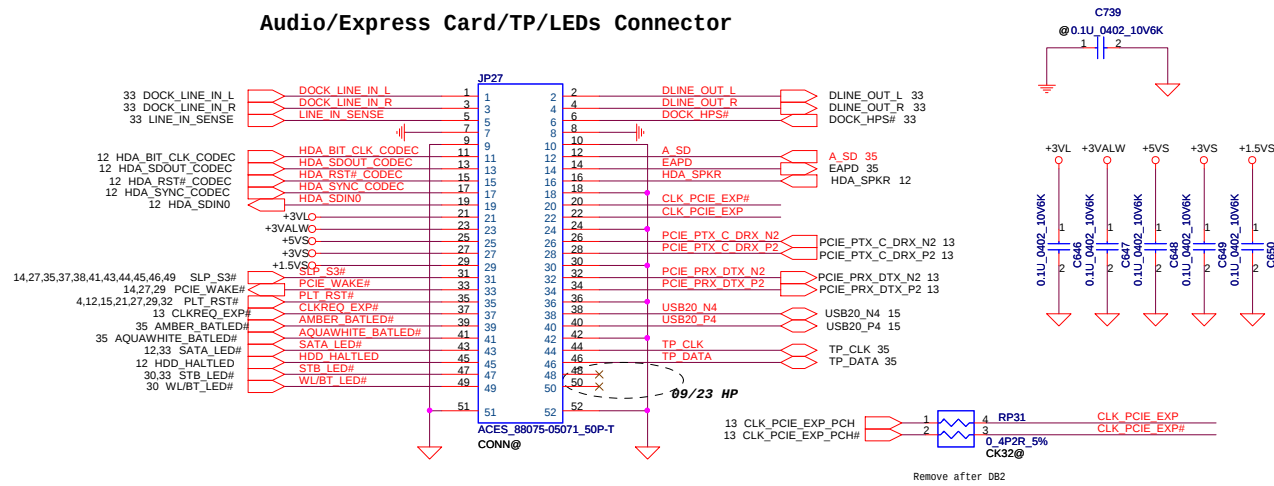
- (2) PS/2 Interfaces
- (2) USB 2 channels
- (2) SATA Channels
- (1) Serial Port
- (1) Parallel Port
- (1) Line In
- (1) Line Out
- (1) RJ45 (10/100/1000)
- (1) VGA
- (1) 2 LAN indicator LED's
- (1) Power Button
- (1) I2C interface



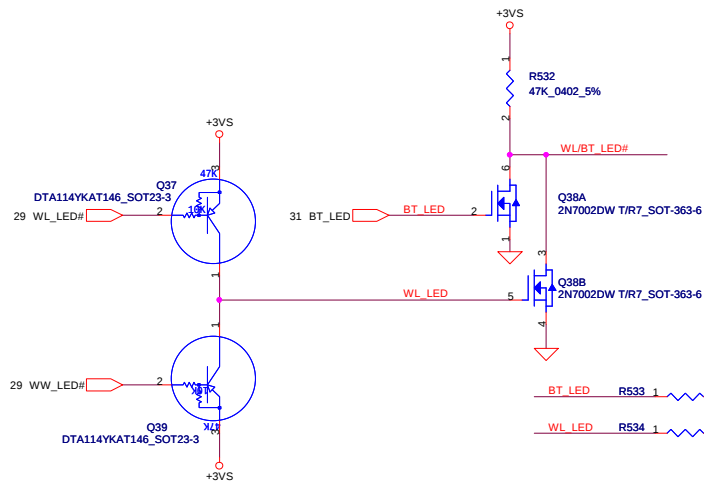
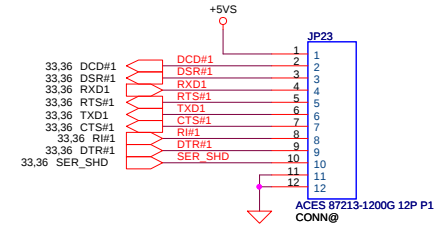
IN	NC<->COM	NO<->COM
L	ON	OFF
H	OFF	ON

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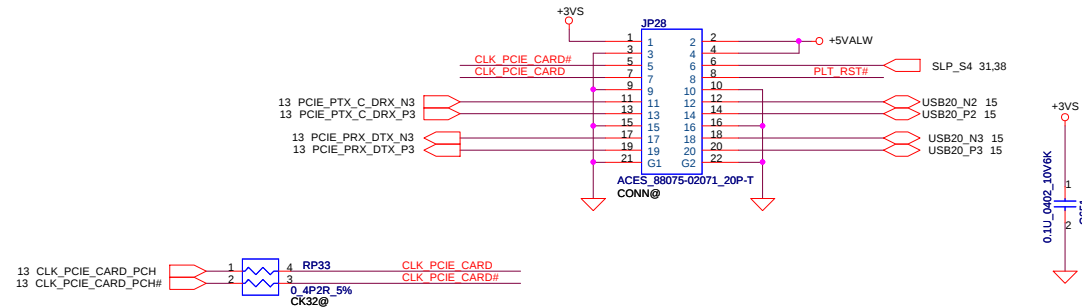
Audio/Express Card/TP/LEDs Connector



Serial Port CONN

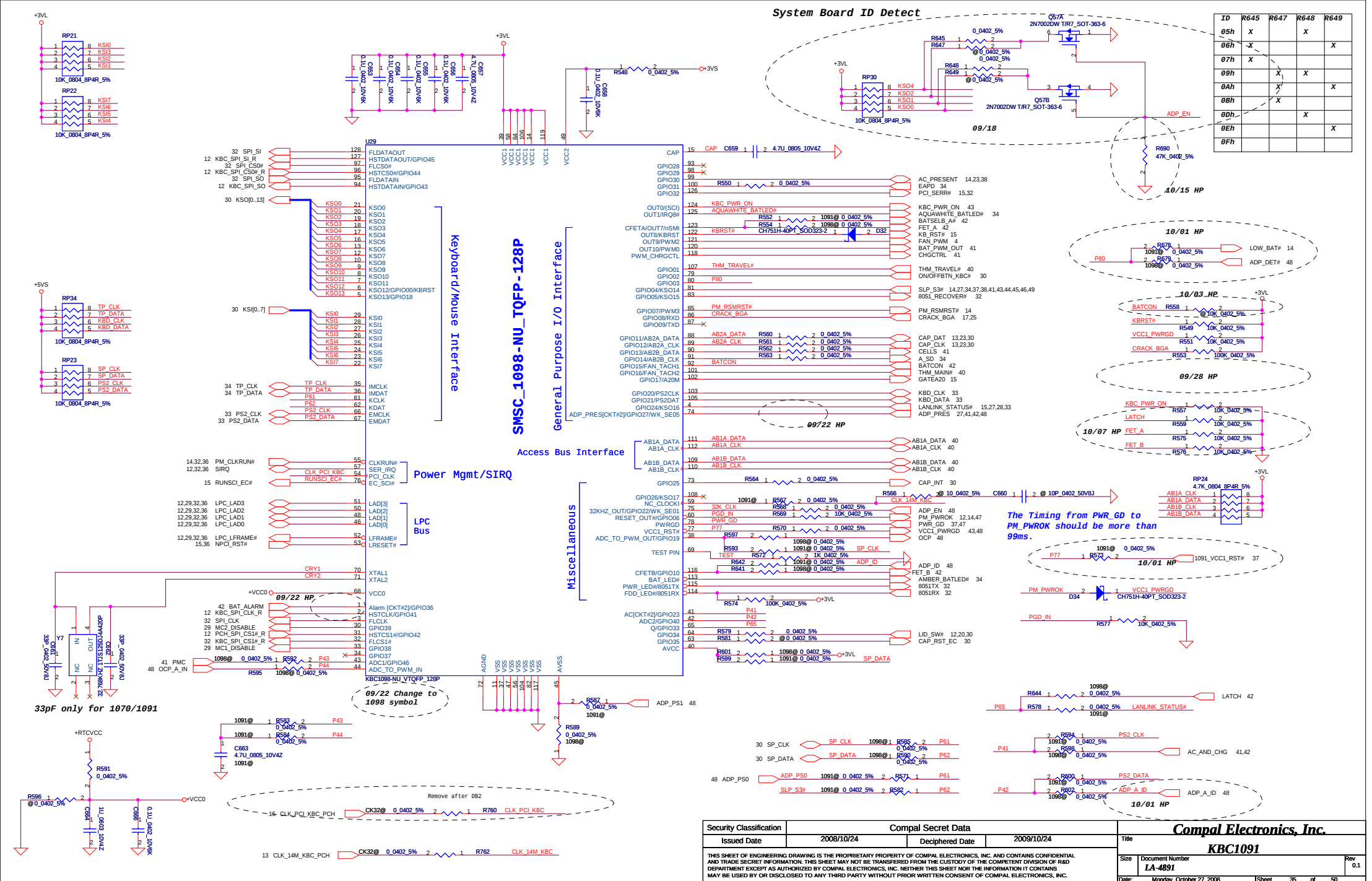


Card Reader 7 in 1 + 2 Port USB Connector



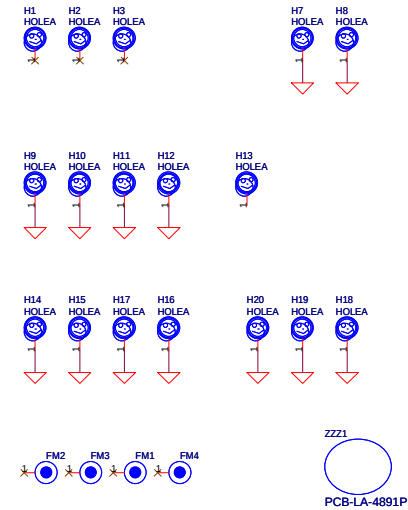
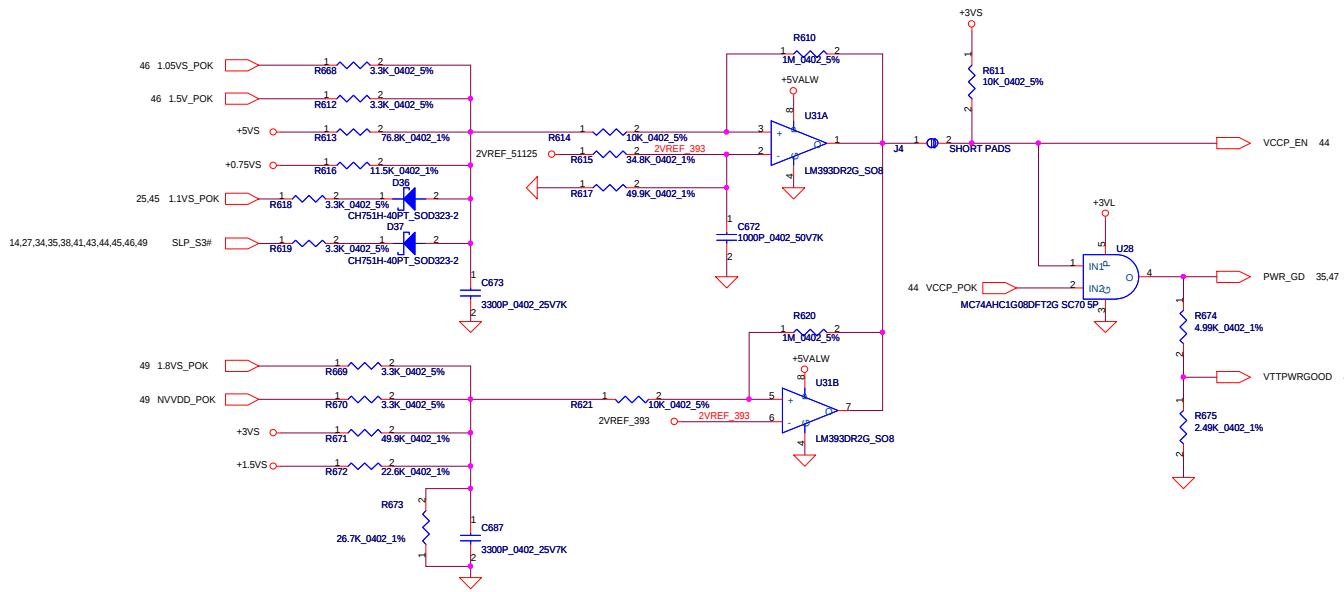
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				Size	Document Number
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System Board ID Detect

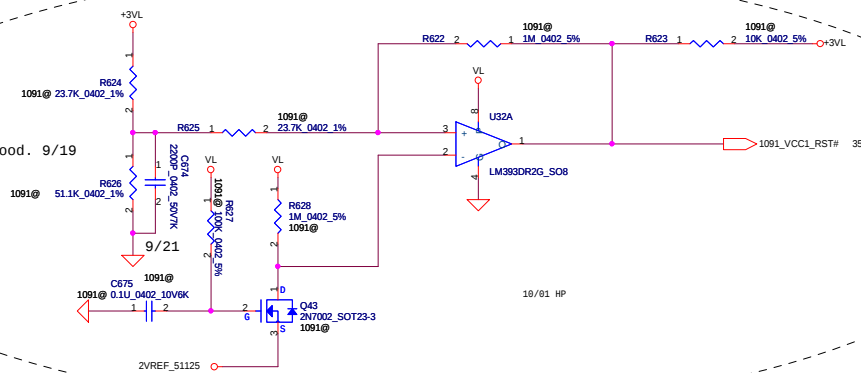


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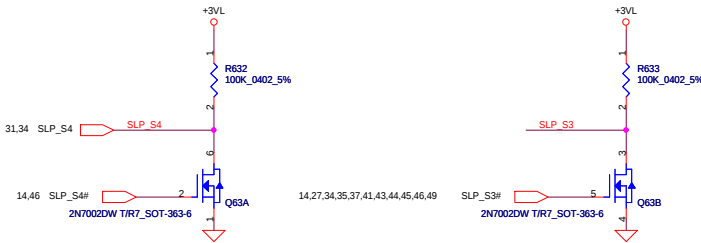
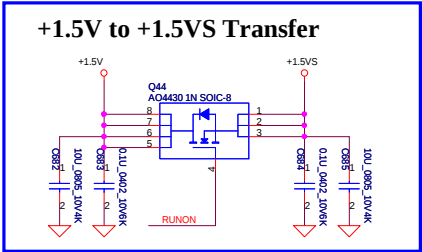
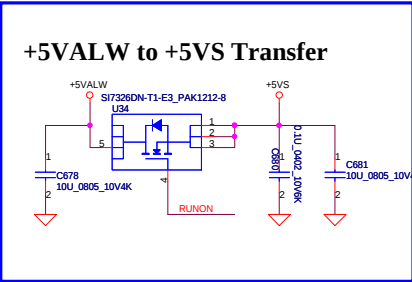
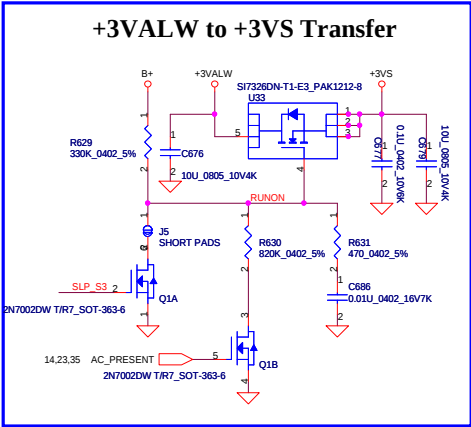
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				Size Custom	Document Number LA-4891	Rev 0.1
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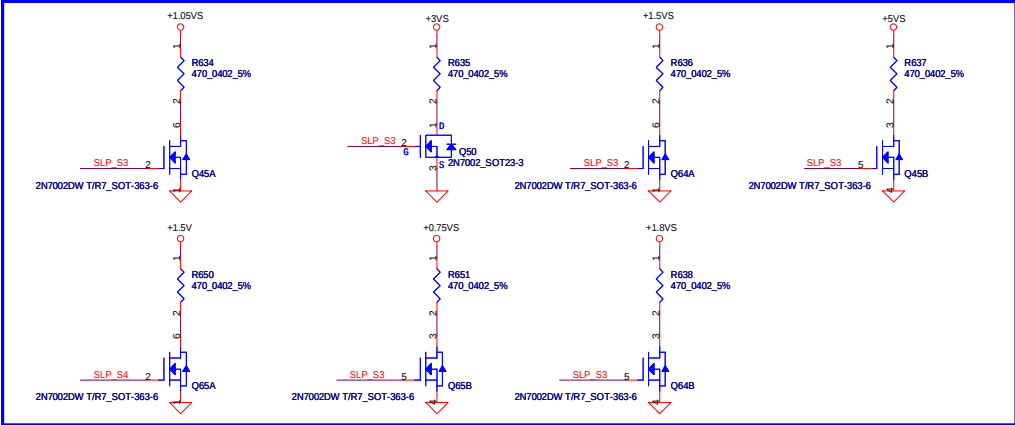
KBC Power OK
update KBC power good. 9/19



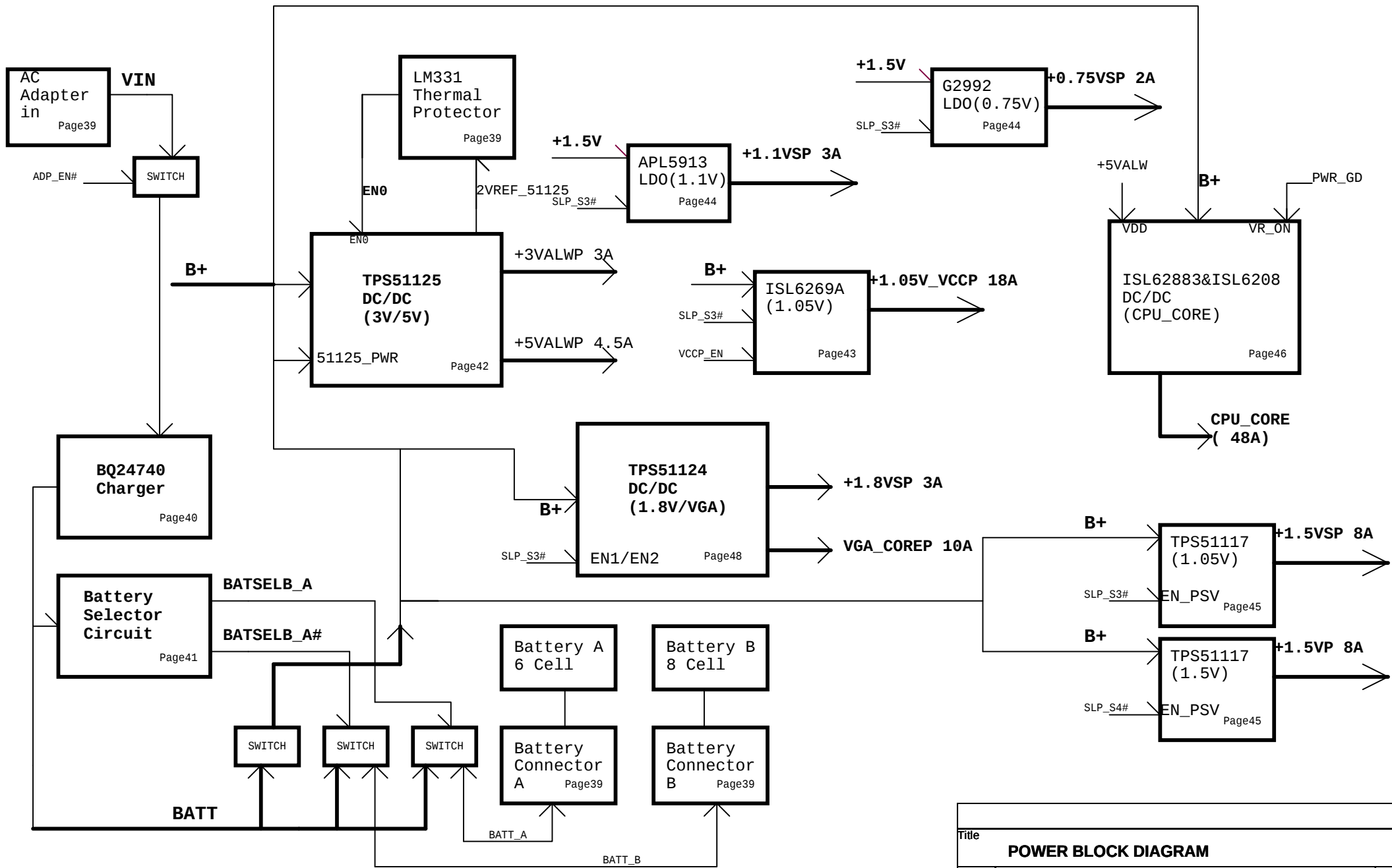
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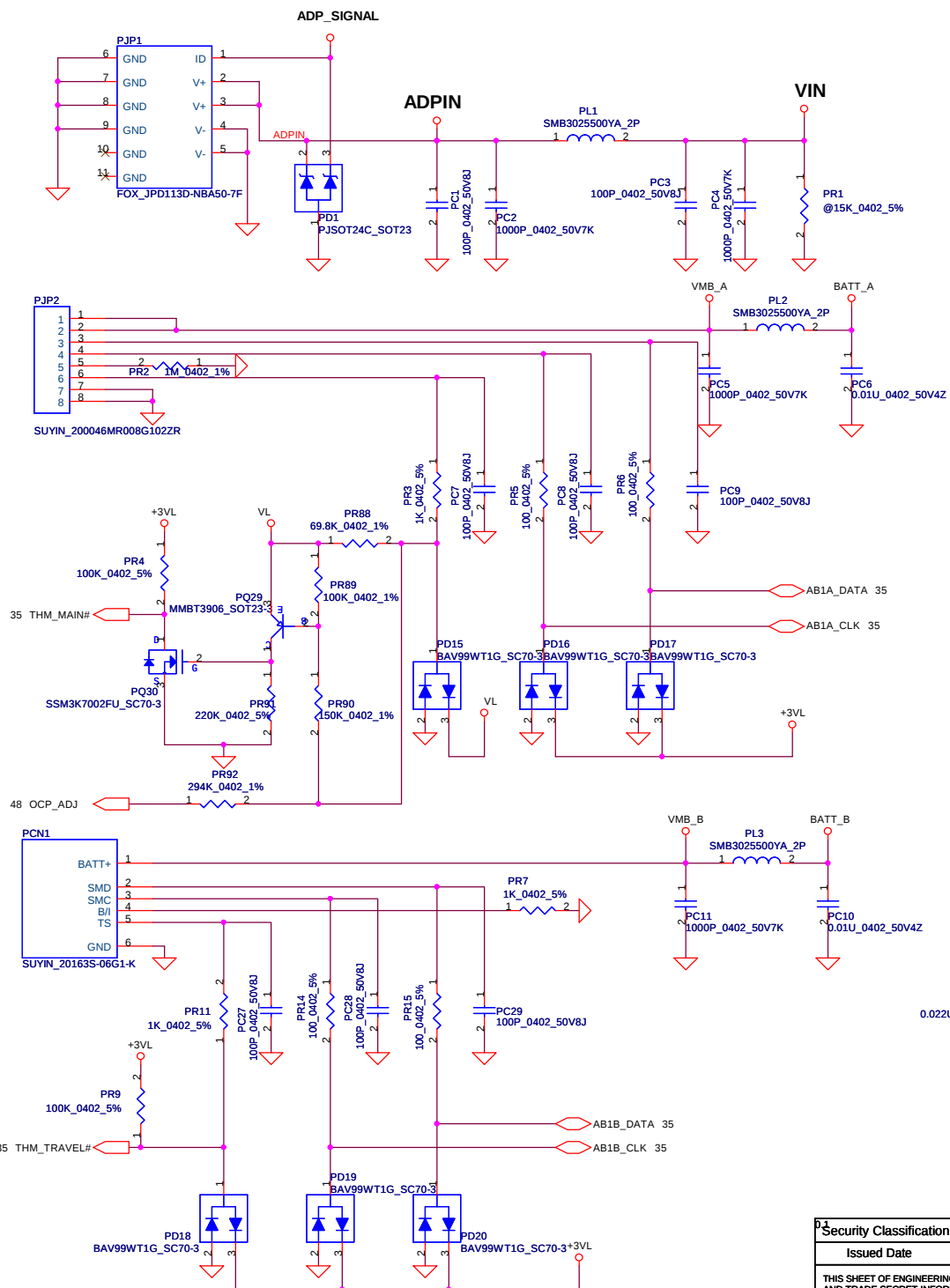
Discharge circuit-1



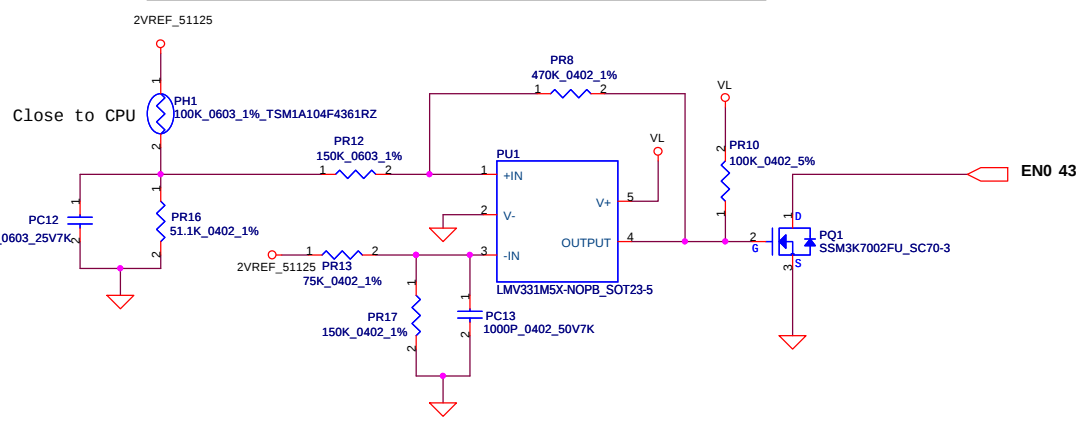
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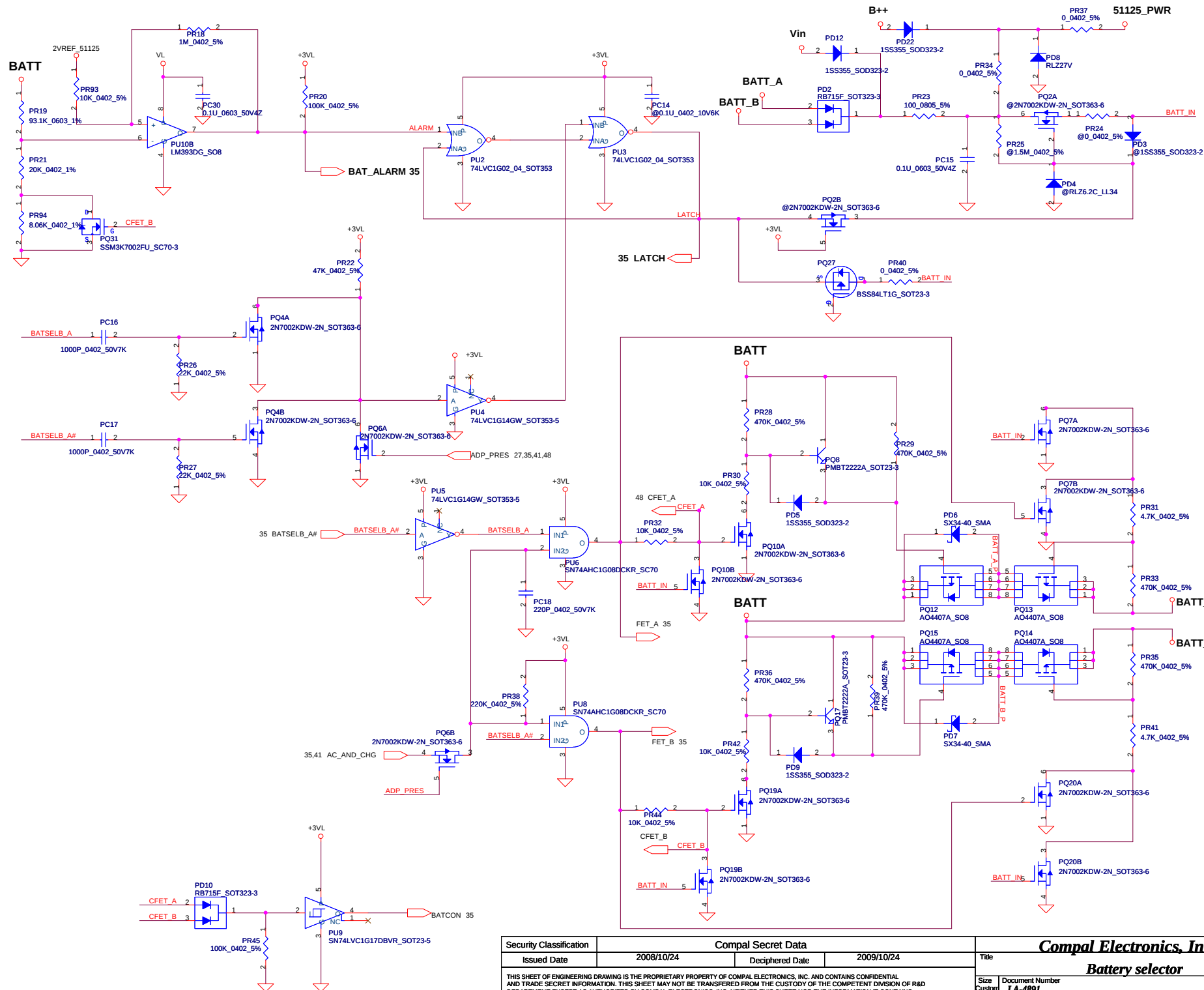
Title		
POWER BLOCK DIAGRAM		
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PH1 under CPU bottom side :
CPU thermal protection at 90 +-3 degree C
(Need to be checked)

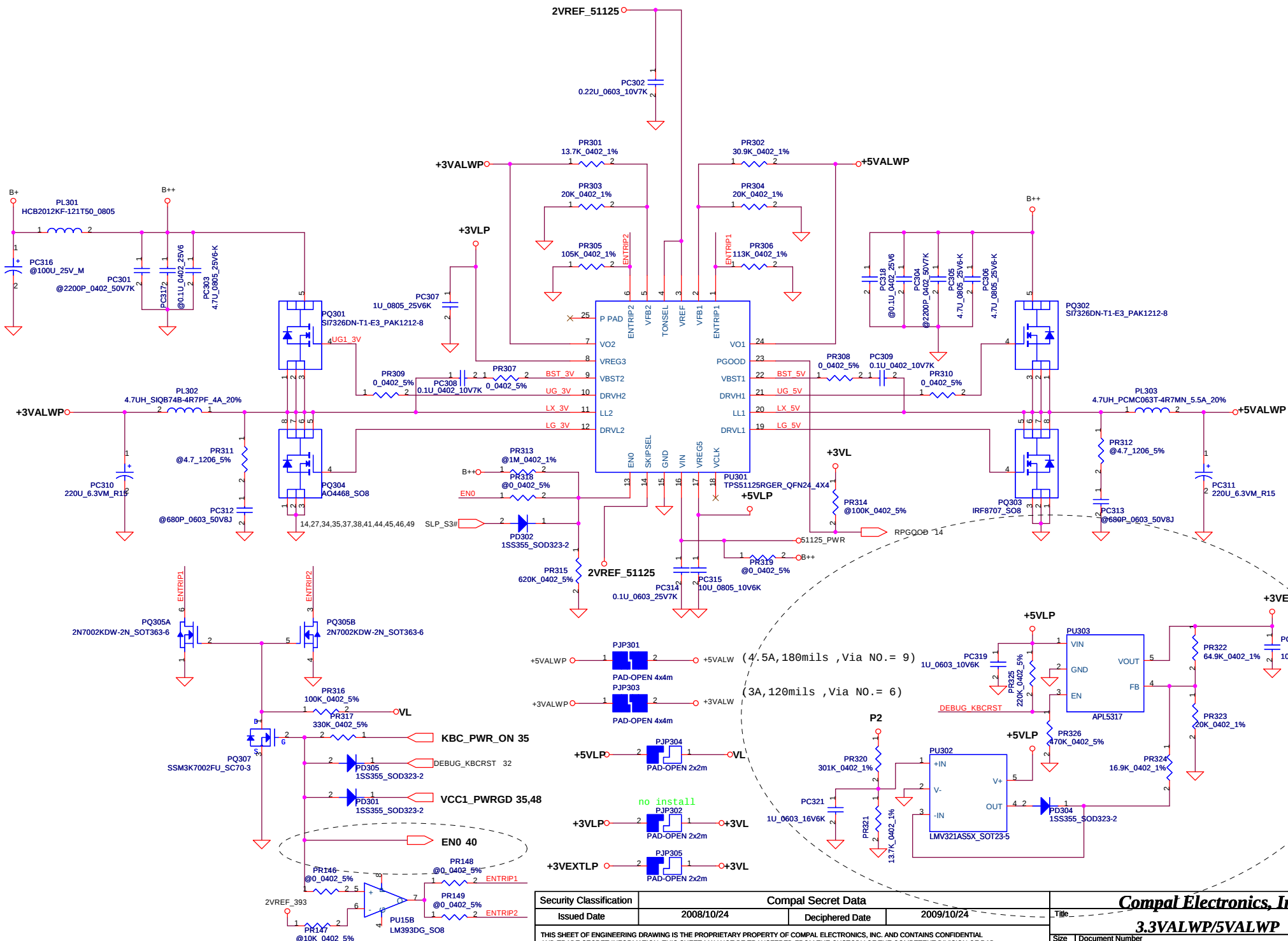


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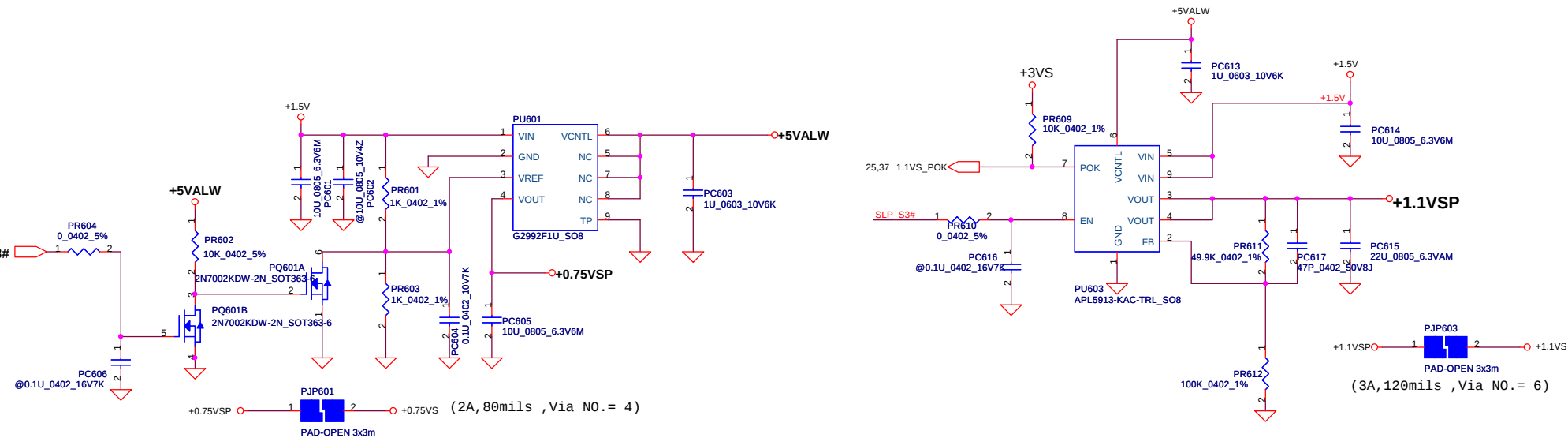
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				Size	Document Number	Rev
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Compal Electronics, Inc.
Battery selector

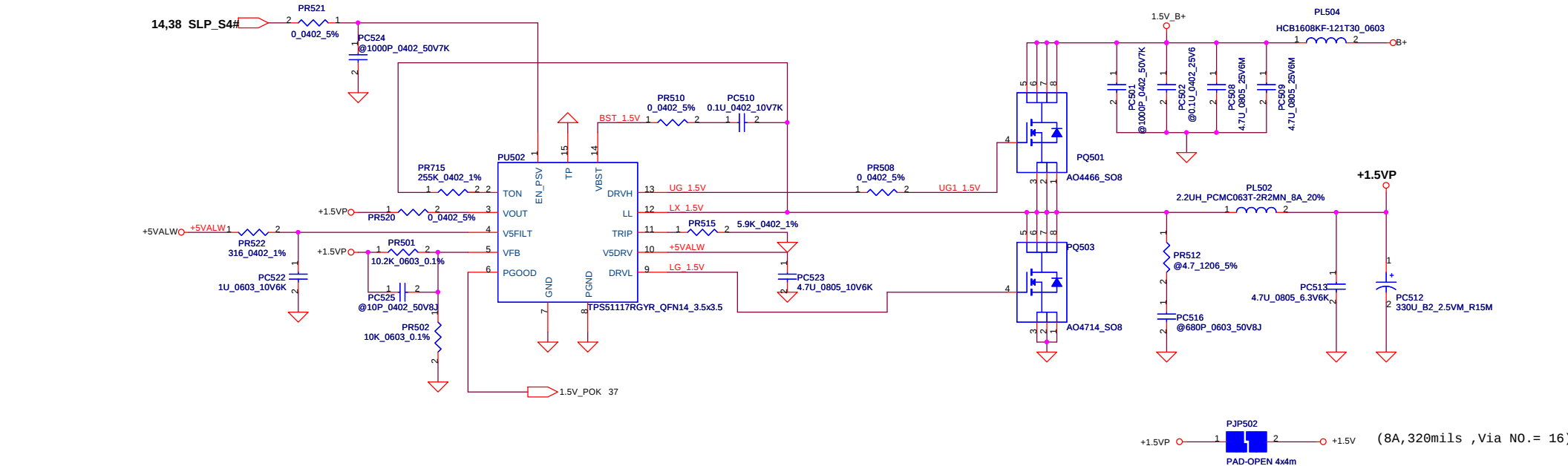
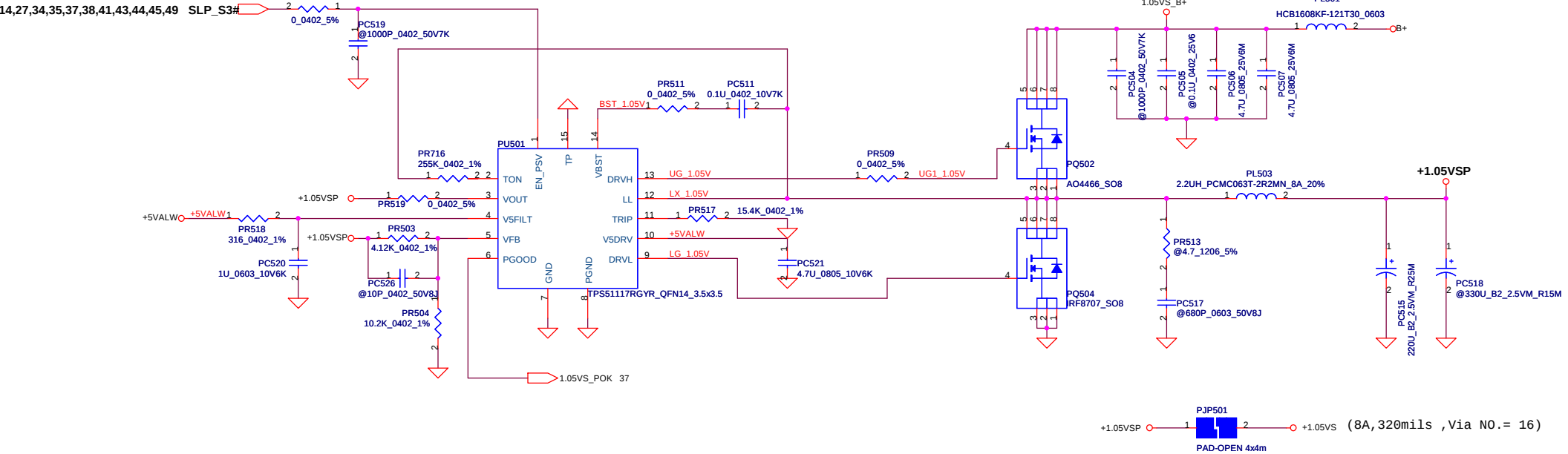


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						Size	Document Number			Rev
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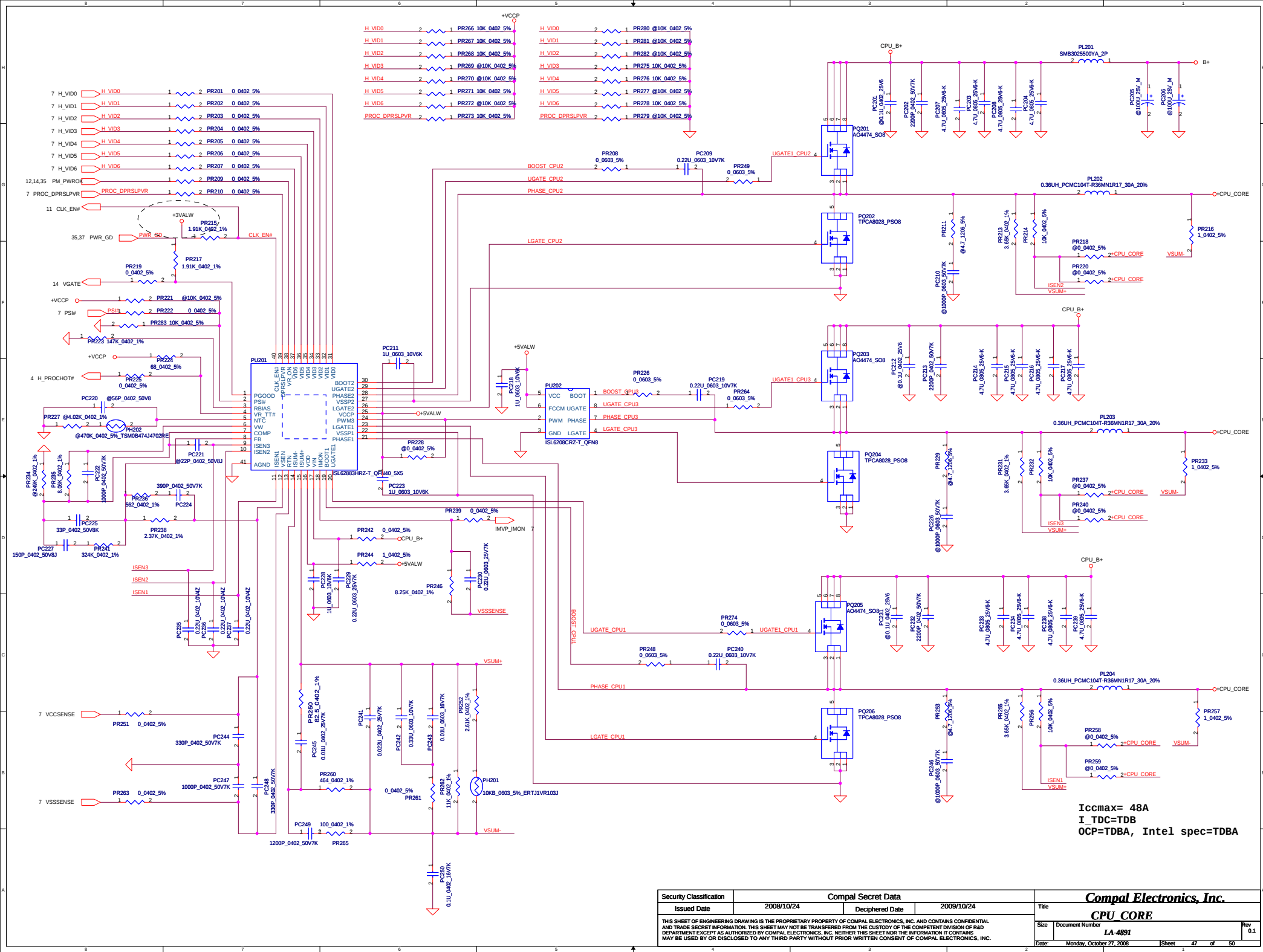
44,46,49 SLP_S3#



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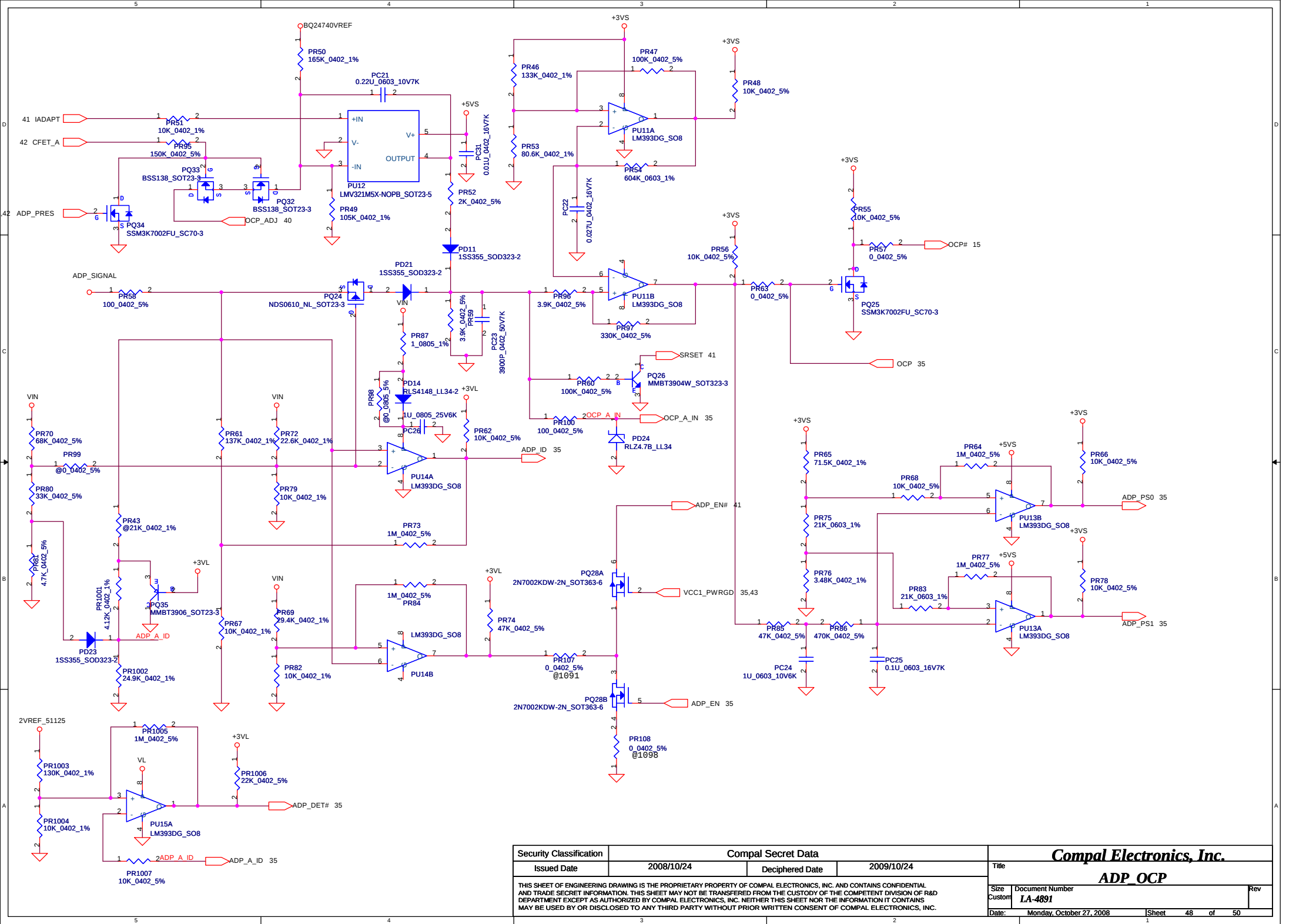


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