

Compal Confidential

Schematics Document

Intel CLARKSFIELD/ARRANDALE
with IBEX PEAK-M core logic

Cartier DIS

LA-4901P

2009-12-01

REV:1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2008/09/15	Deciphered Date	2009/12/31	Title		
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Voltage Rails (0 MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B +3VL	+5VALW +3VALW	+3VM +1.05VM	+1.5V +0.75V	+5VS +3VS +1.5VS +VGA_CORE +VCCP +CPU_CORE +1.05VS +1.8VS
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	X	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

Symbol Note :



: means Digital Ground



: means Analog Ground

Install below 45 level BOM structure

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure

@ : means just reserve , no build

CONN@ : means ME part.

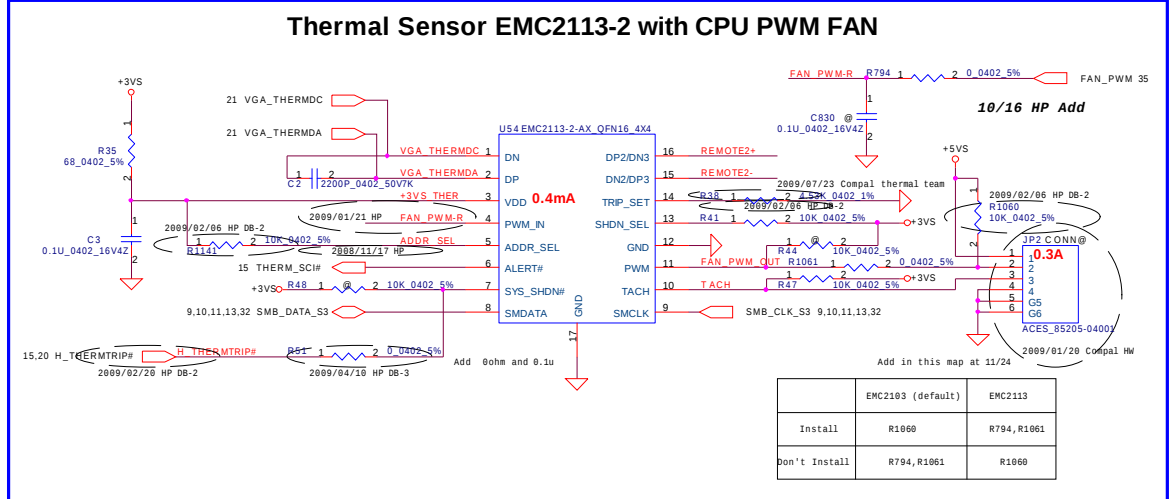
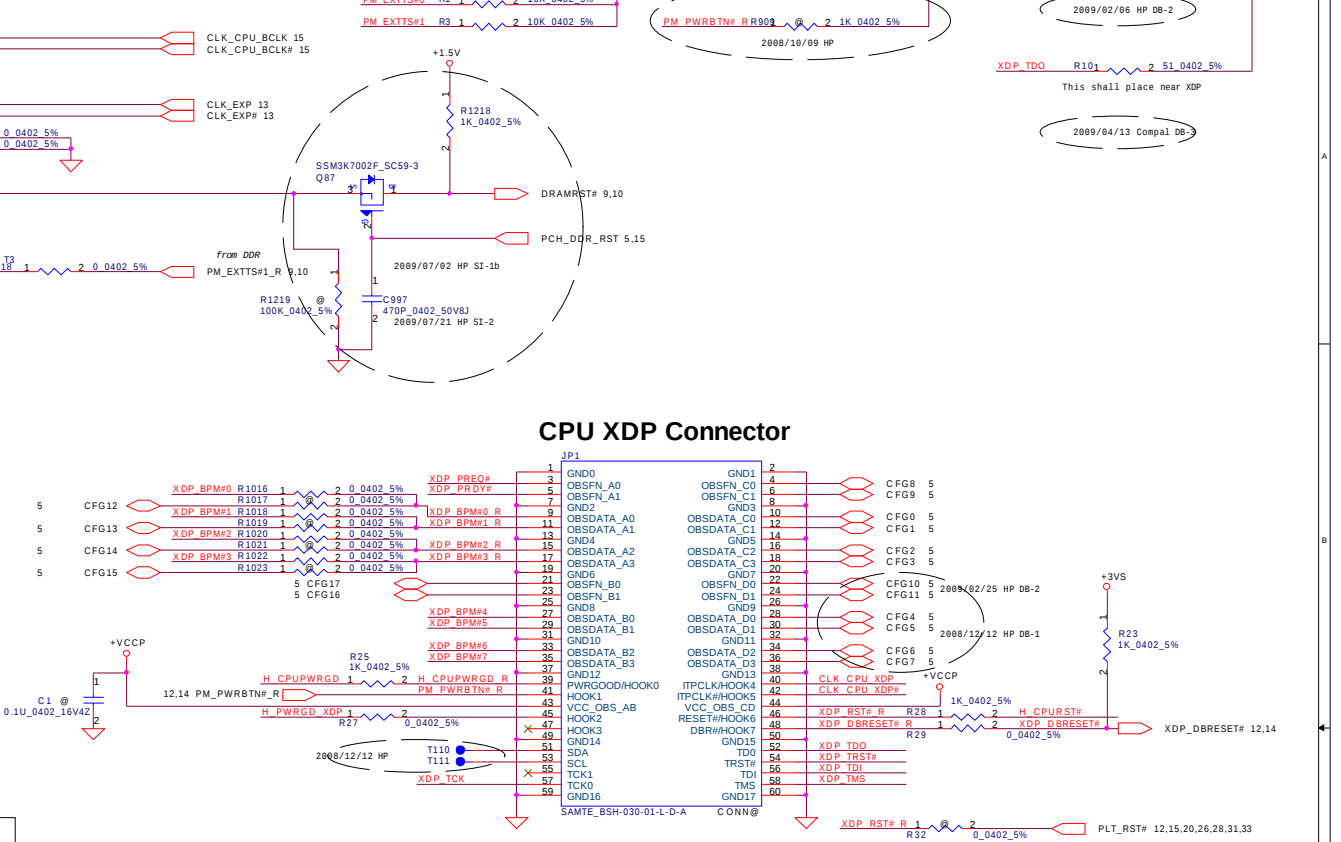
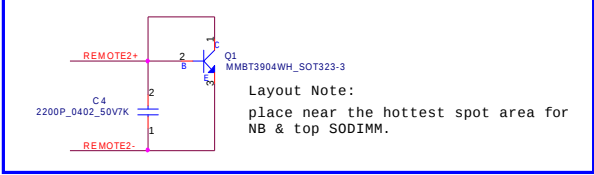
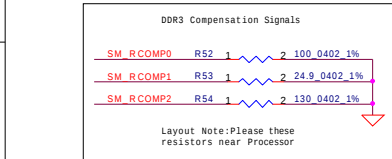
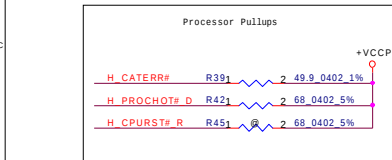
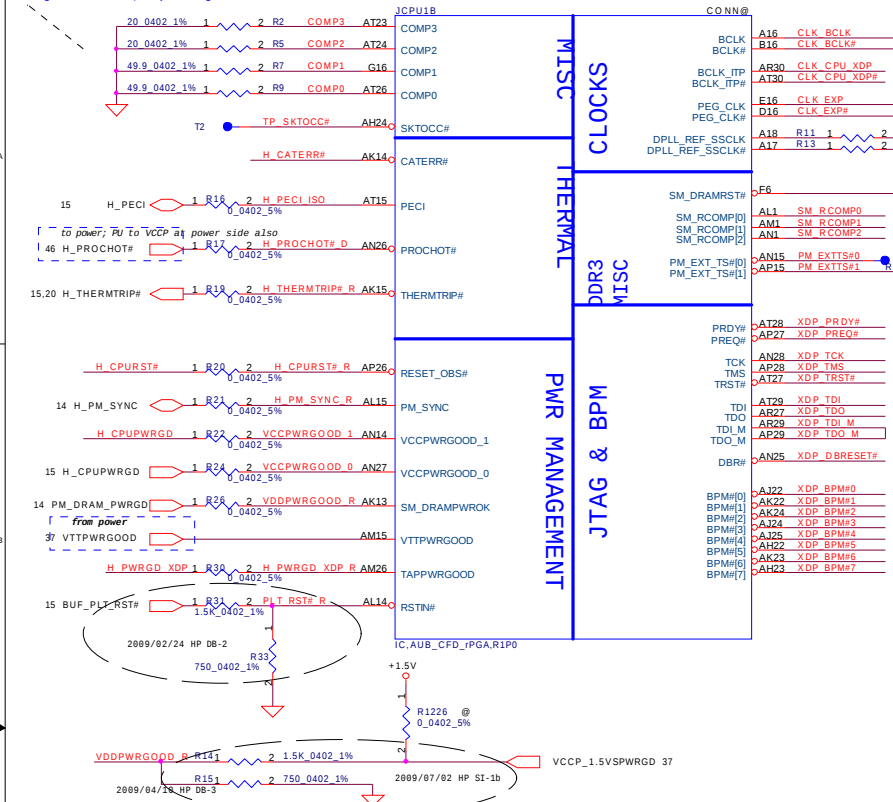
VRAM@ : means VRAM strip pin part.

SMBUS Control Table

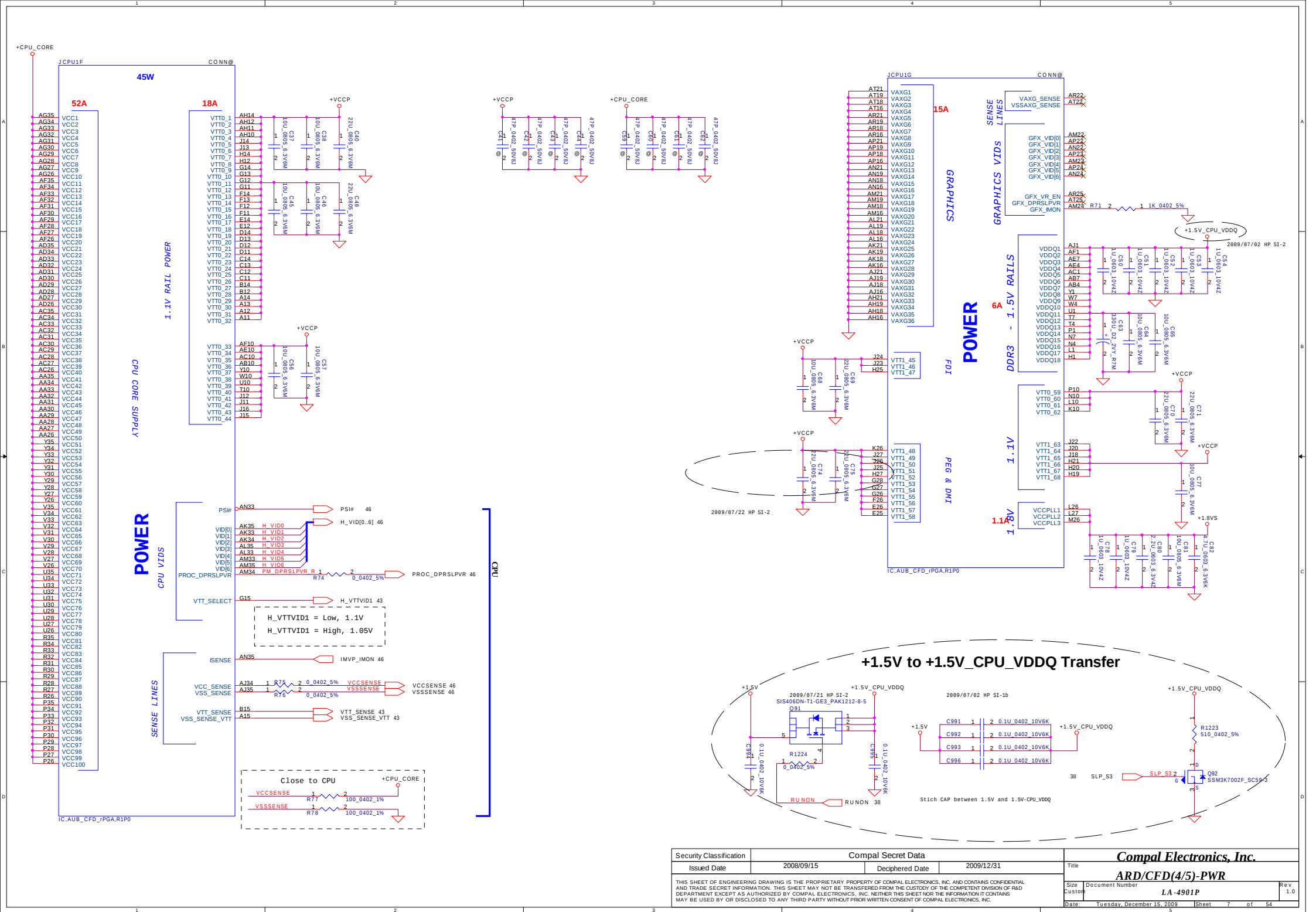
	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	X	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	V	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	X

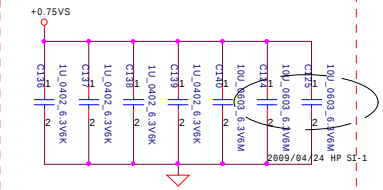
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Layout rule: 10mil width trace
length < 0.5", spacing 20mil



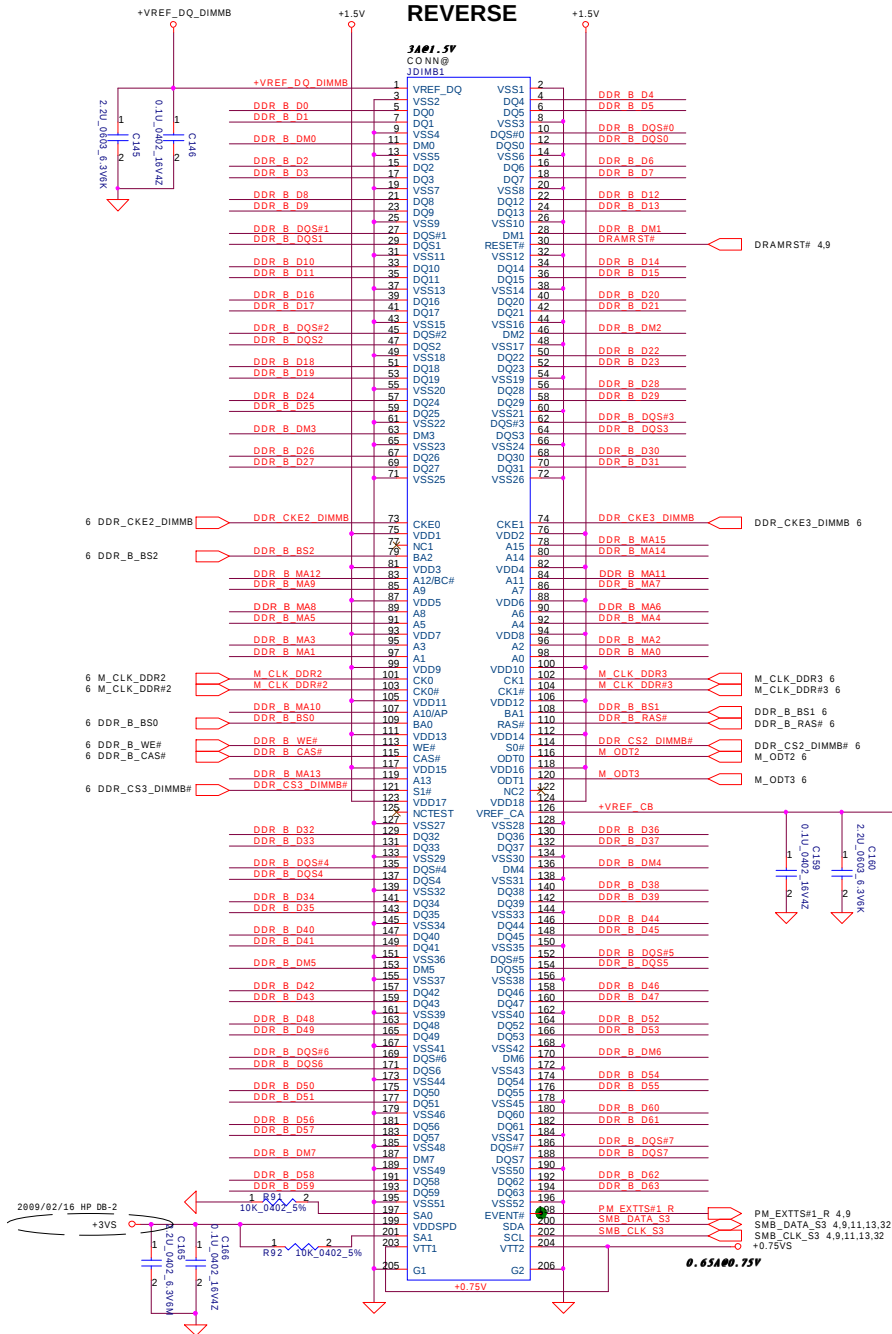
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2008/09/15	Deciphered Date	2009/12/31	Title	ARD/CFD(1/5)-Thermal/XDP	
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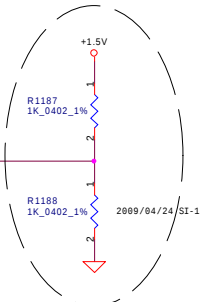
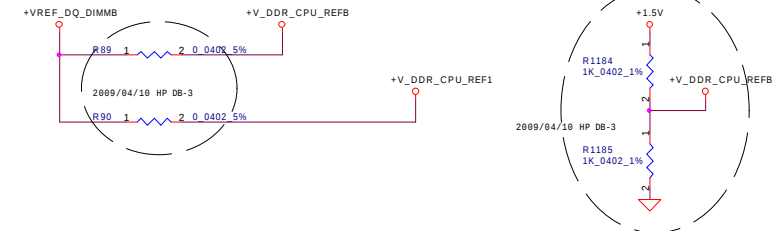
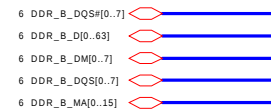


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Issued Date	2008/09/15	Deciphered Date	2009/12/31	Title	DDRIII-SODIMM SLOT1	
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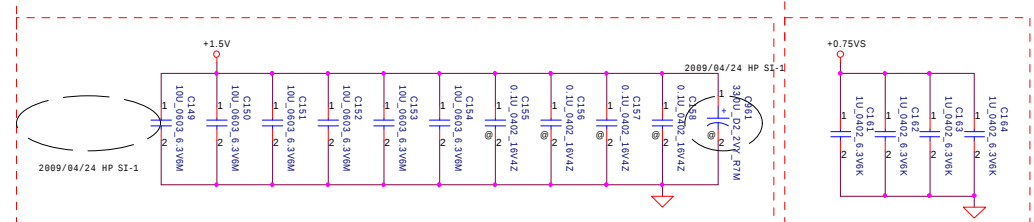
DDR3 SO-DIMM B
REVERSE



BOT SLOT

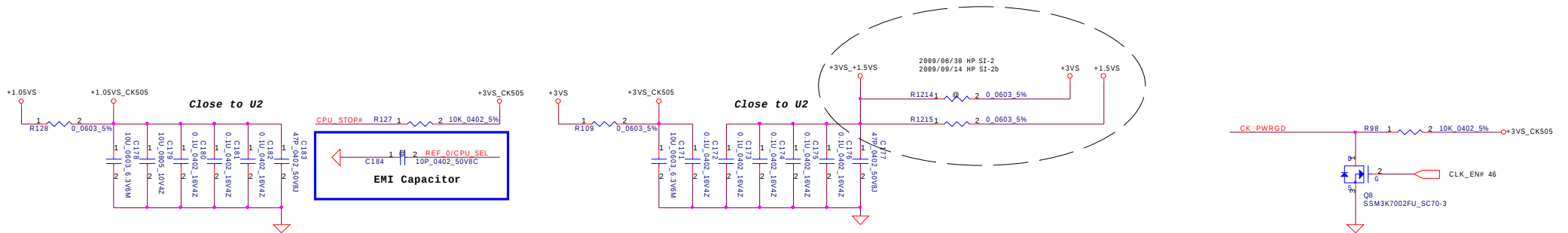
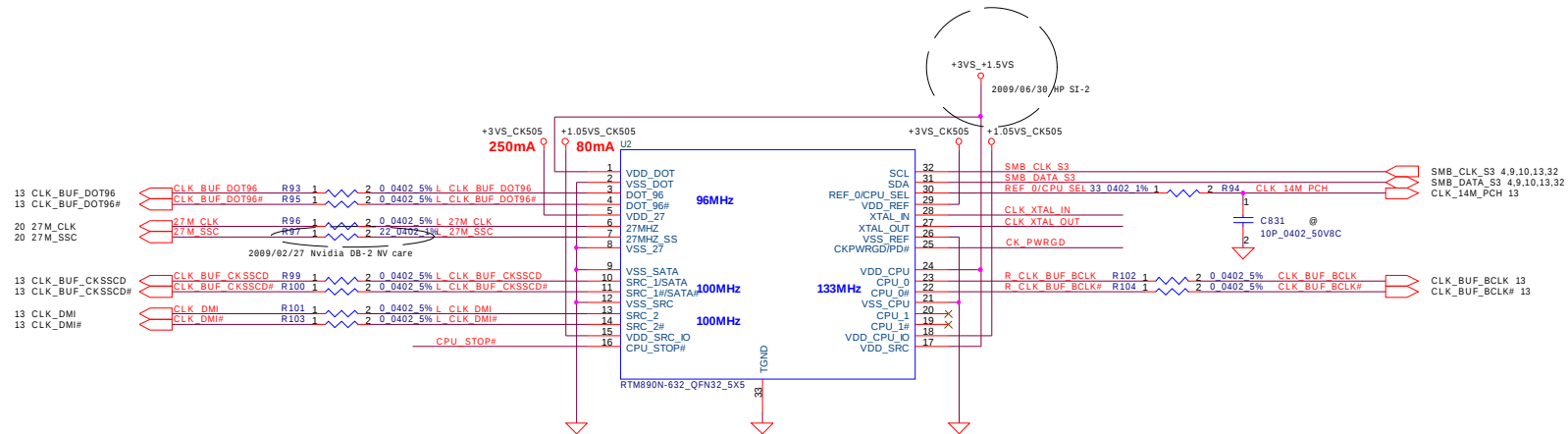


Layout Note:
Place near JDIMMB

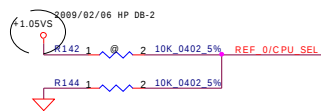


Layout Note:
Place near JDIMMB.203 & JDIMMB.204

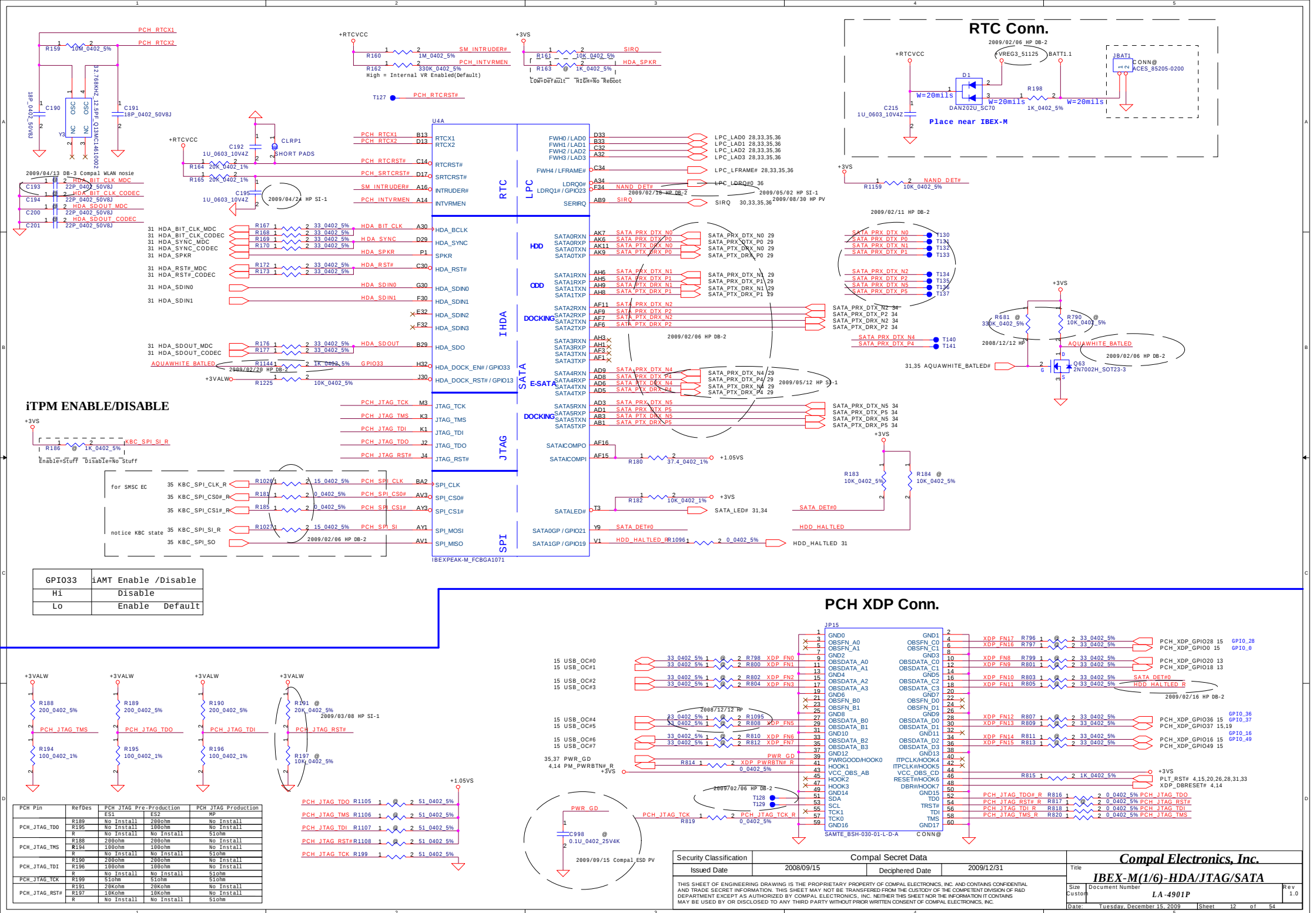
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Issued Date	2008/09/15	Deciphered Date	2009/12/31	Title	DDRIII-SODIMM SLOT2
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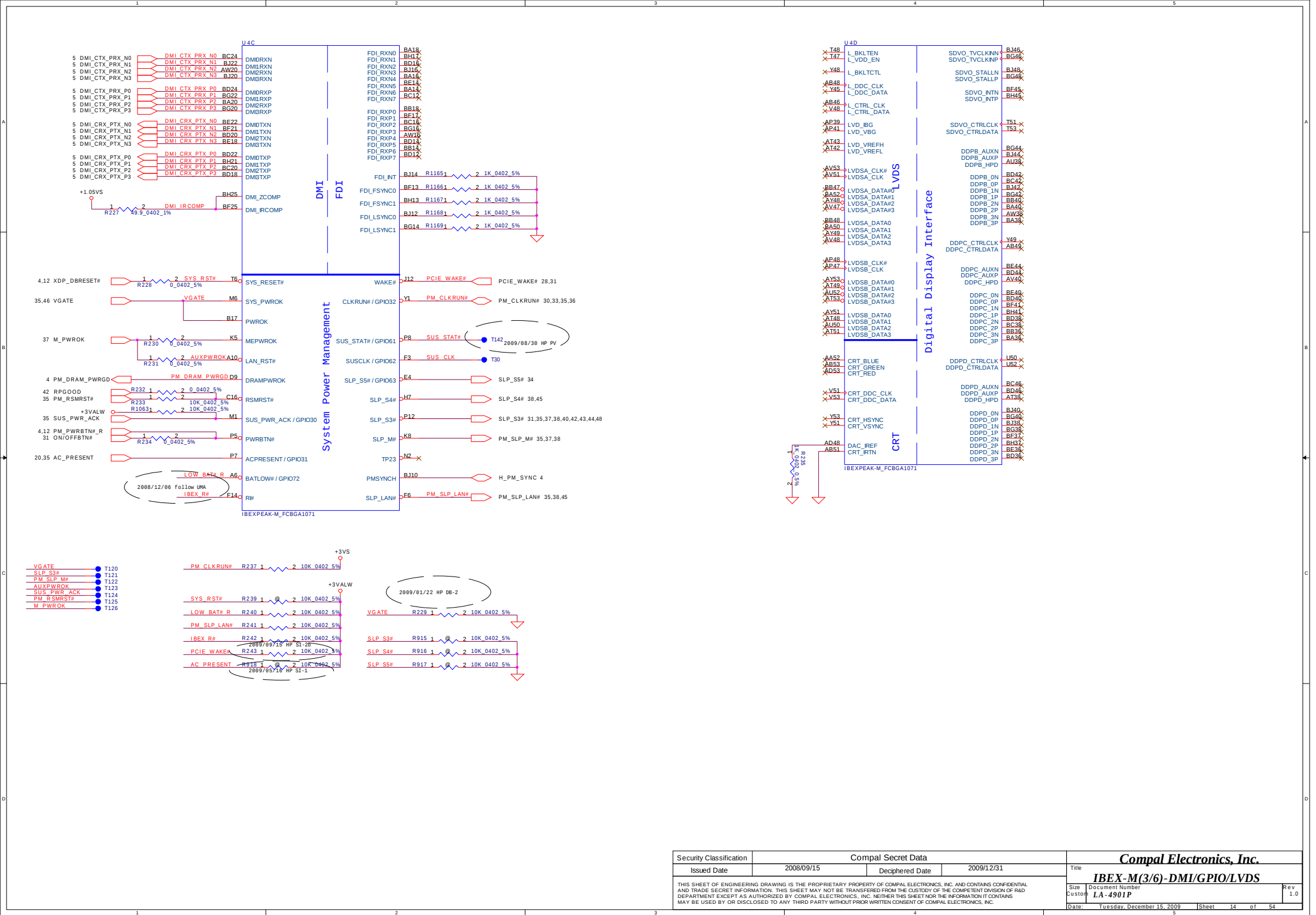


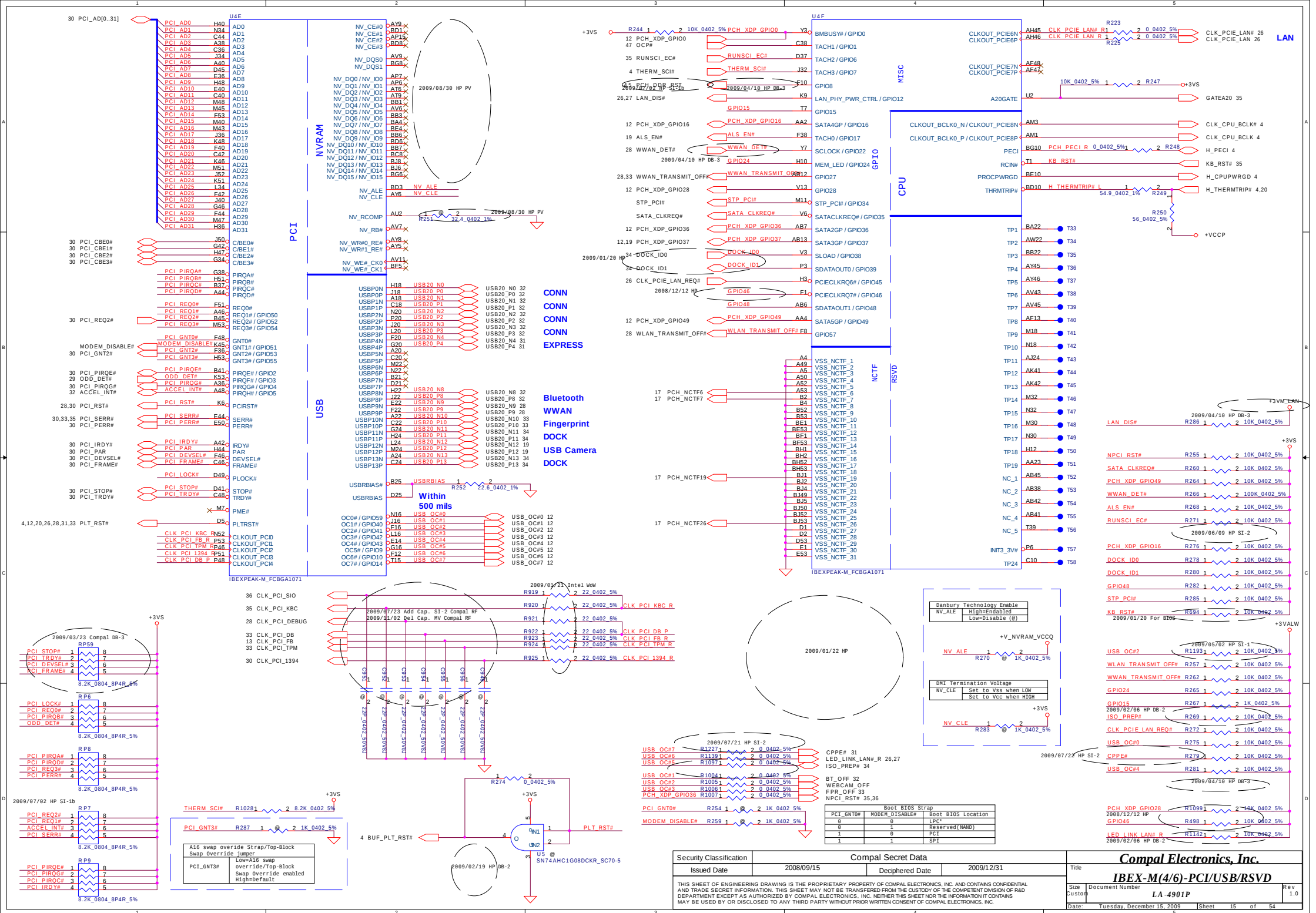
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

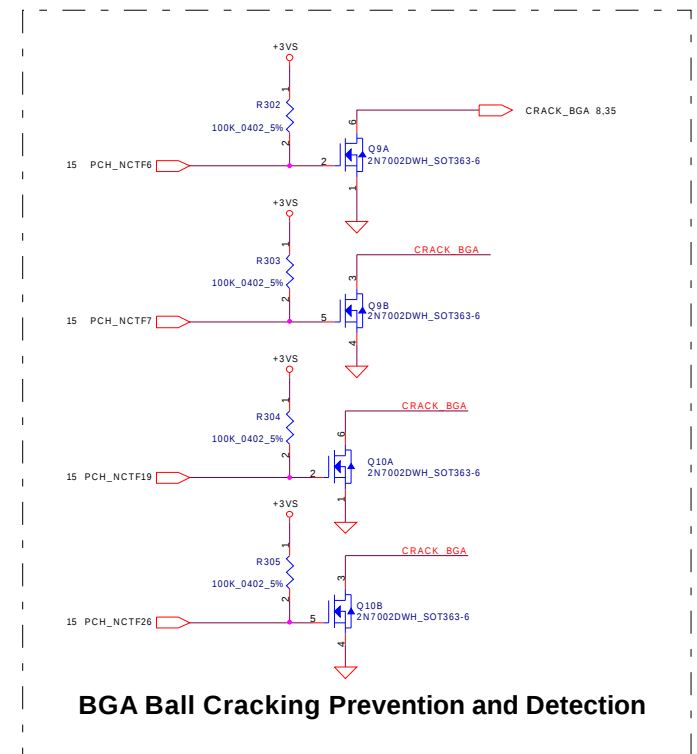
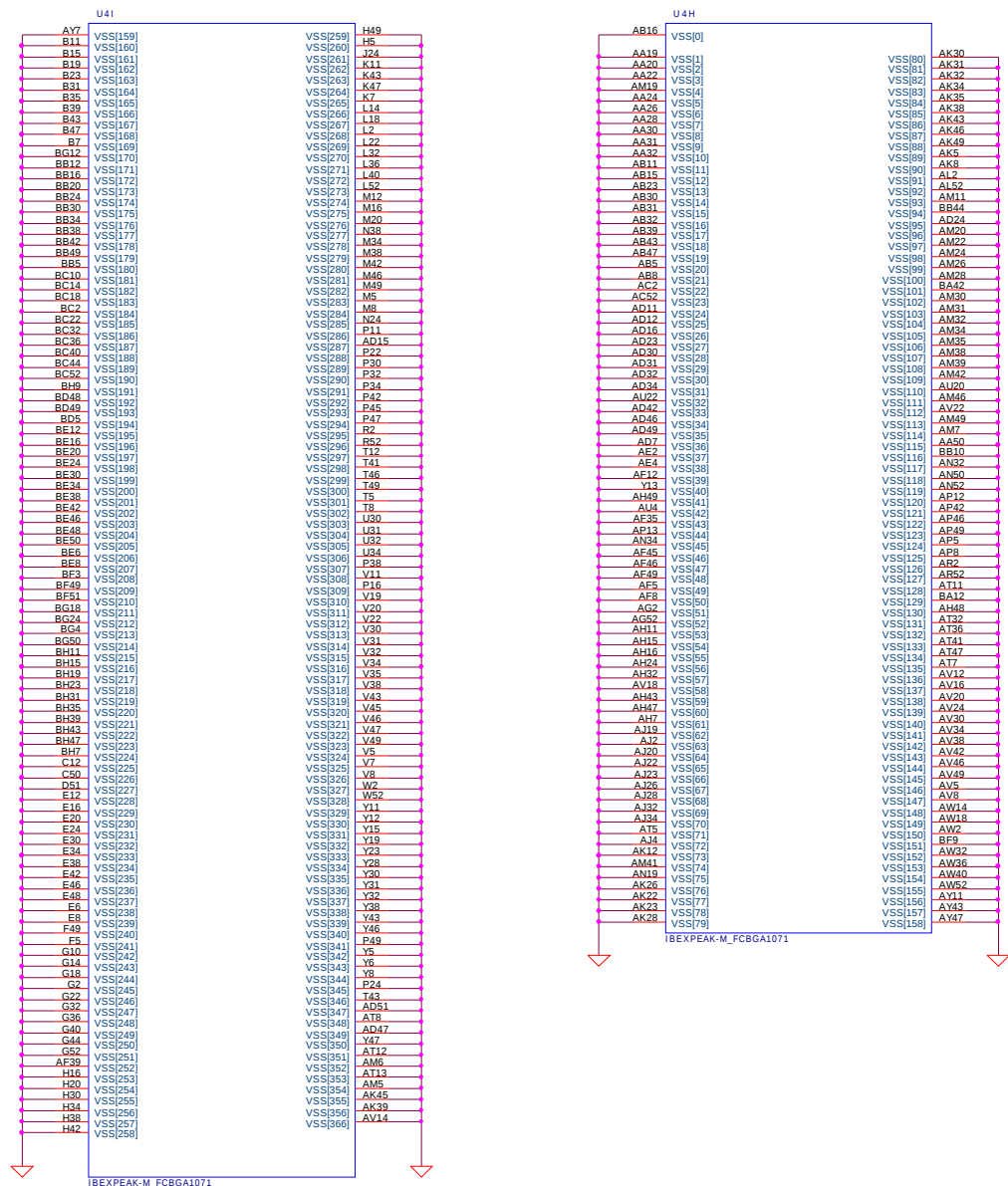


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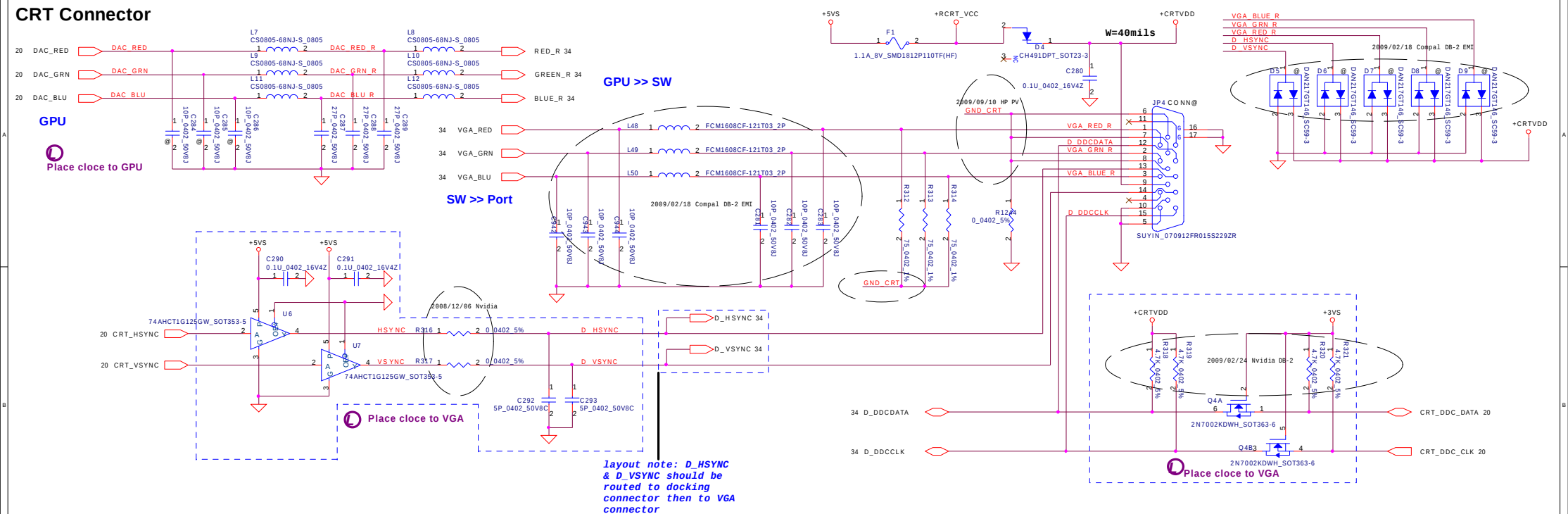




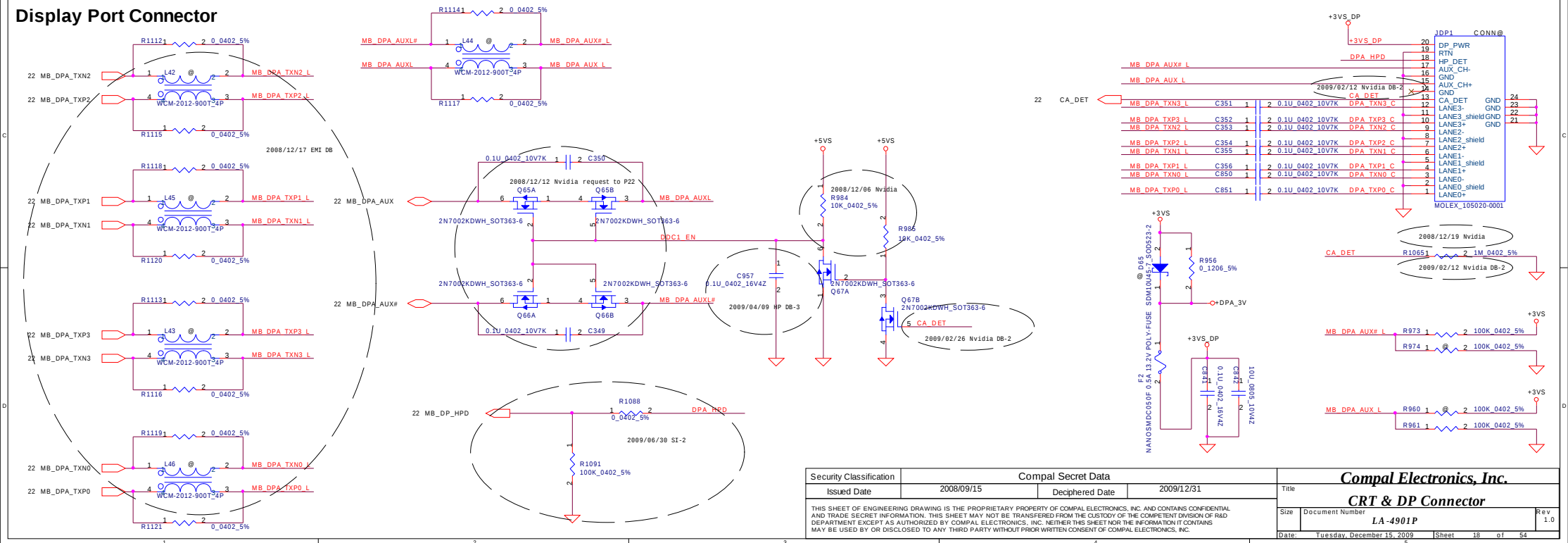




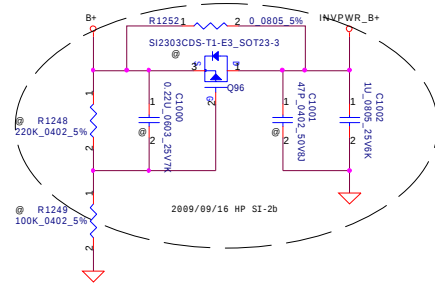
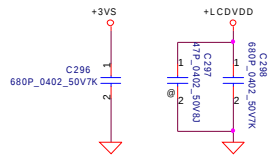
CRT Connector



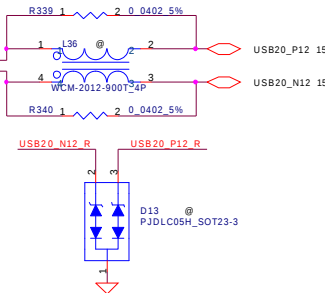
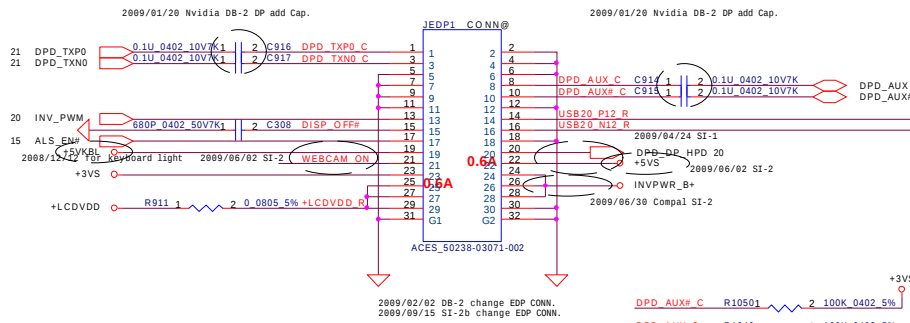
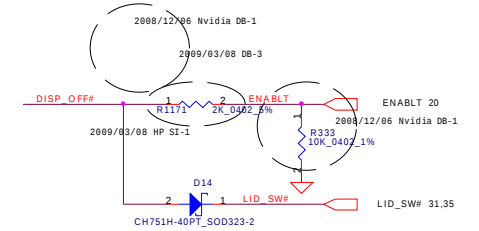
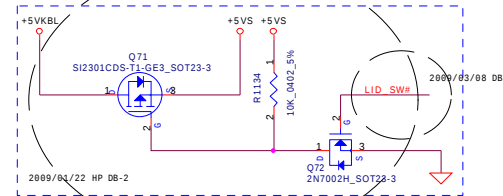
Display Port Connector



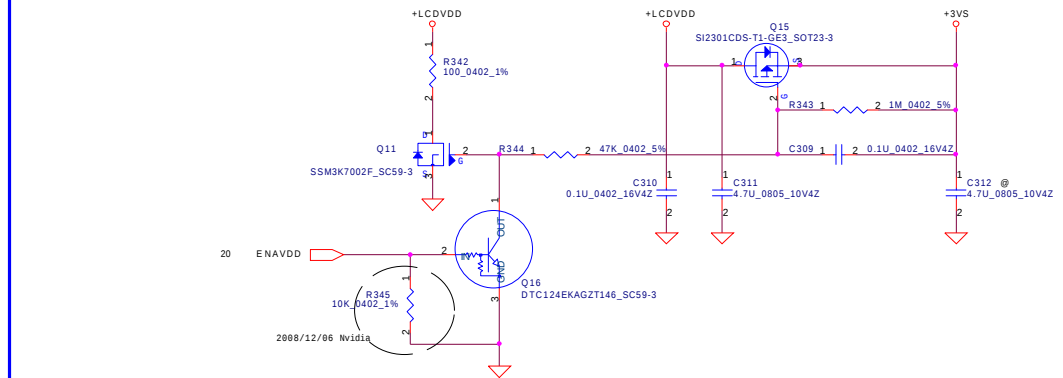
LCD/PANEL BD. CONN.



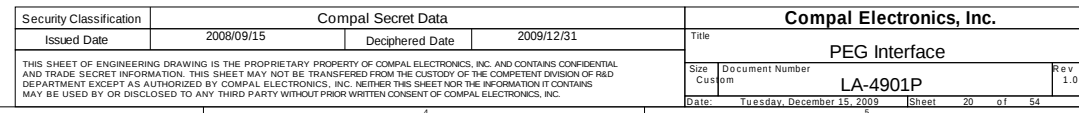
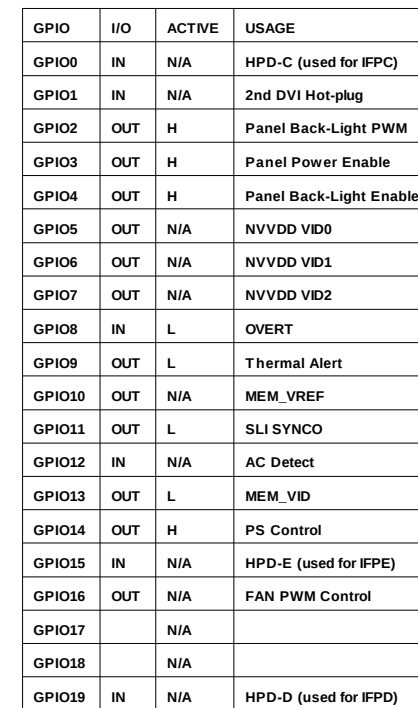
Key_Board_Light power Control



LCD POWER CIRCUIT



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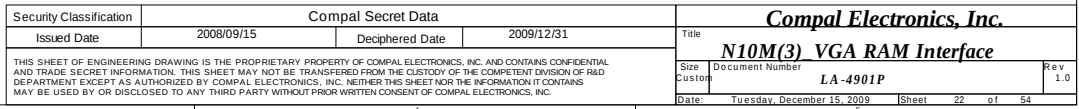


DPA AUX	R976	1	2	100K	0402	5%
DPA AUX#	R977	1	2	100K	0402	5%
DPD AUX	R1056	1	2	100K	0402	5%
DPD AUX#	R1057	1	2	100K	0402	5%
DPE AUX	R1103	1	2	100K	0402	5%
DPE AUX#	R1104	1	2	100K	0402	5%

MULTI LEVEL STRAPS

R402/R403:
- 15K: VBIOS combined in SBIOS
- 35K: use VBIOS rom chip

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						1.0				



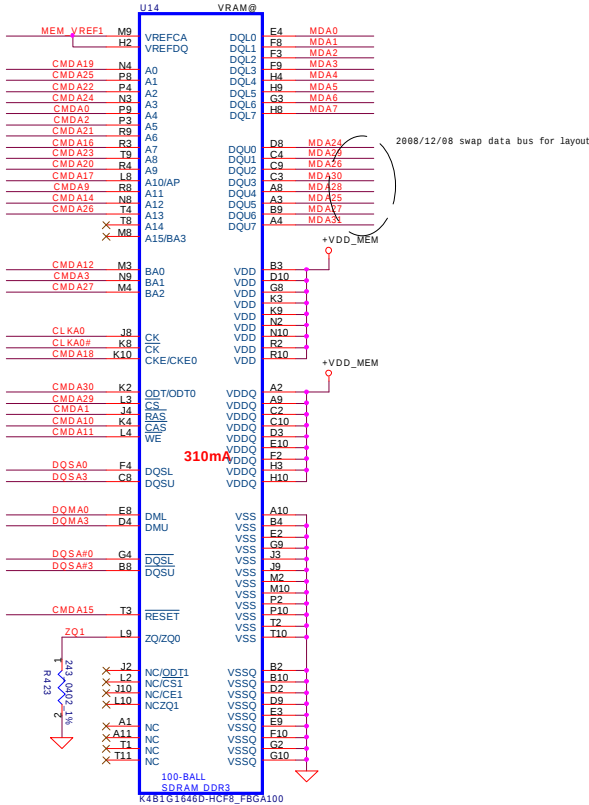
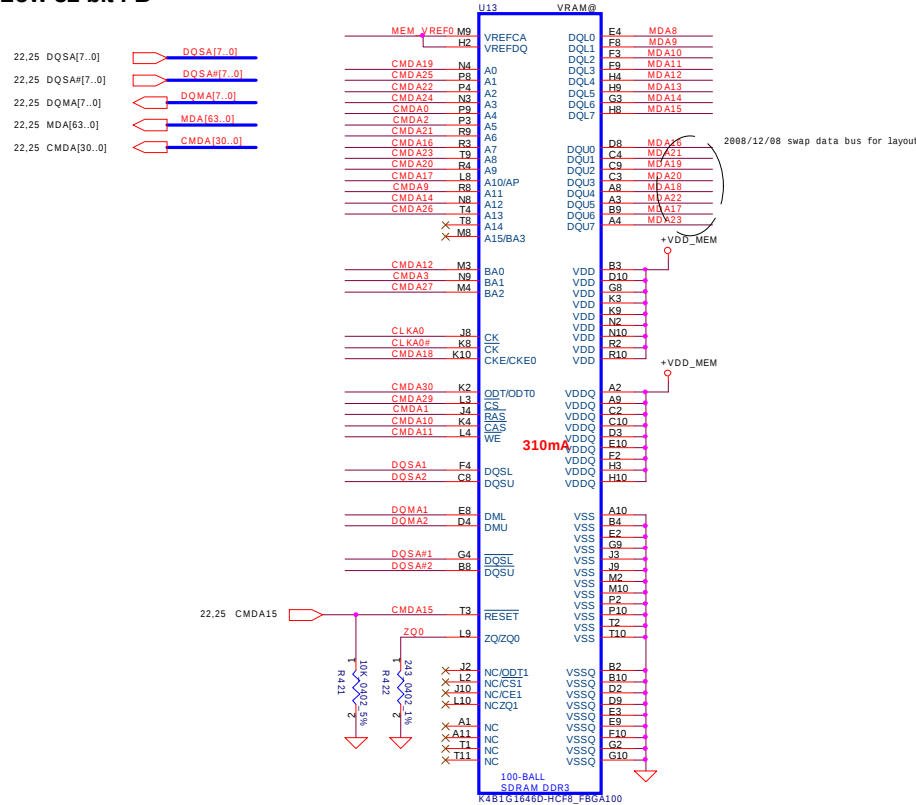


VRAM DDR3 chips (512MB)

64Mx16 DDR3 800MHz*4==>512MB

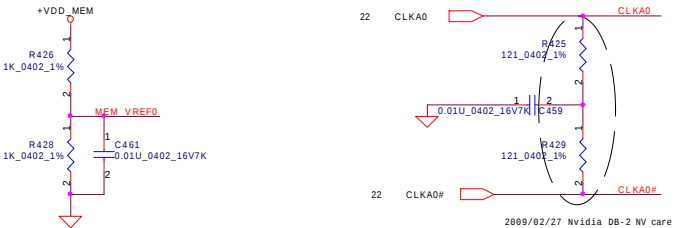
Low 32 bit FB

Hynix : H5TQ1G63BFR-12C-->SA000032400
Samsung : K4W1G1646E-HC12-->SA000035700

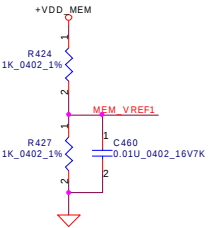
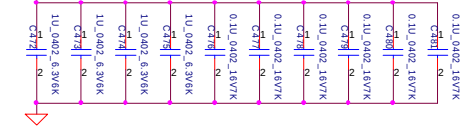


DATA Bus		
Address	0..31	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS#	
CMD30	ODT	

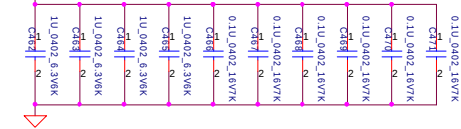
LOW HIGH



DDR3 BGA MEMORY

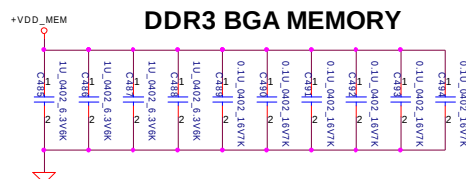
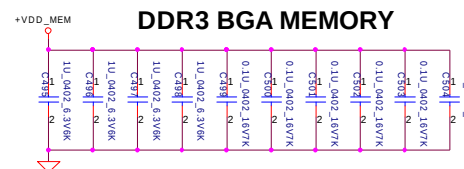
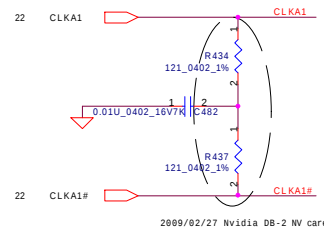
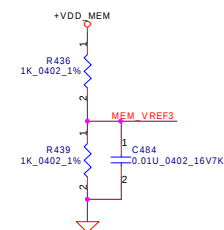


DDR3 BGA MEMORY

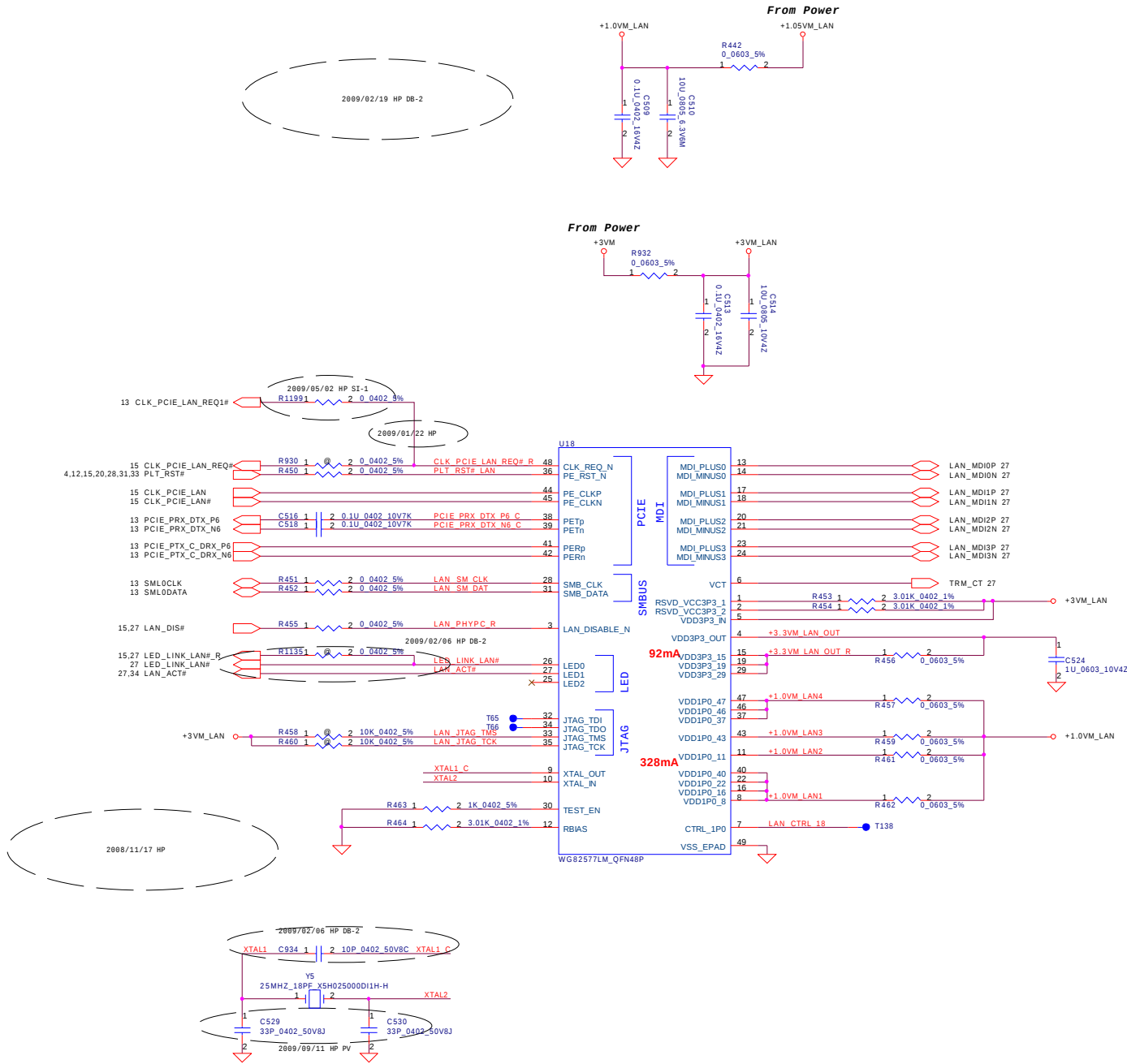


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Size		Document Number		LA-4901P		Rev		0.1	
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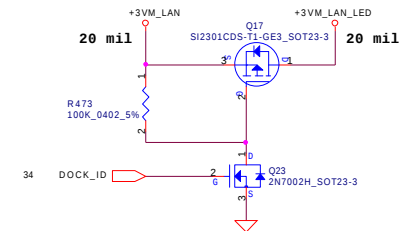
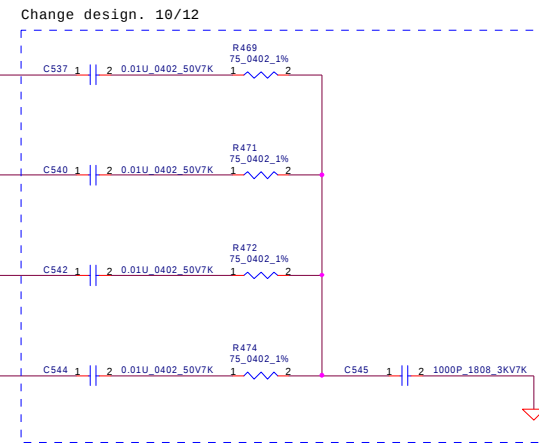
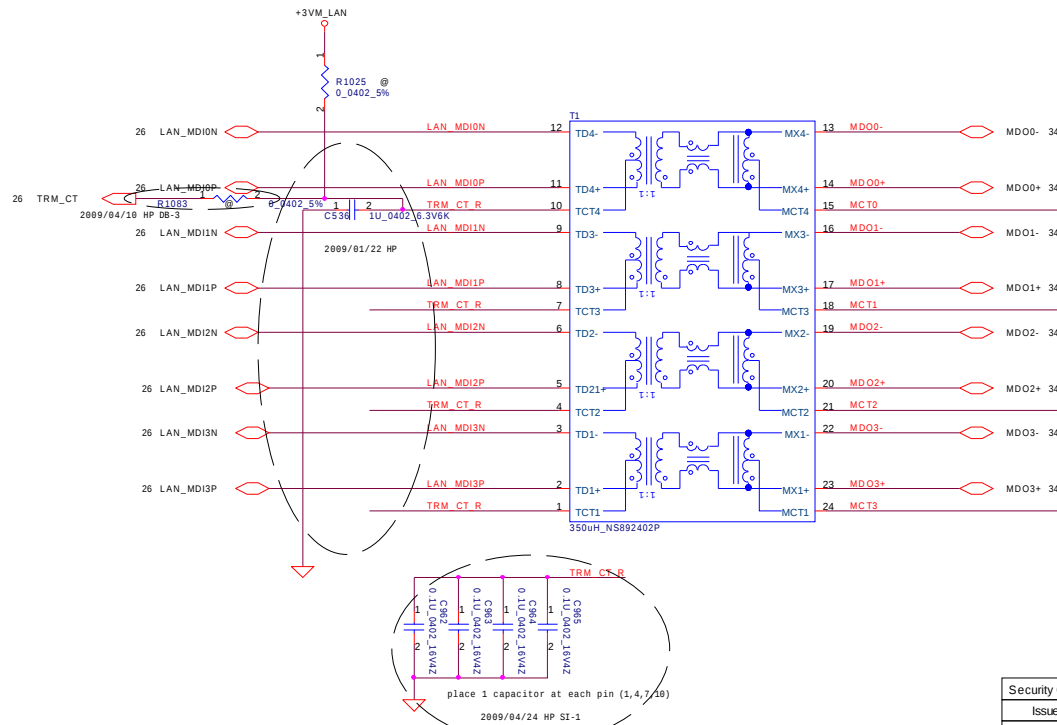
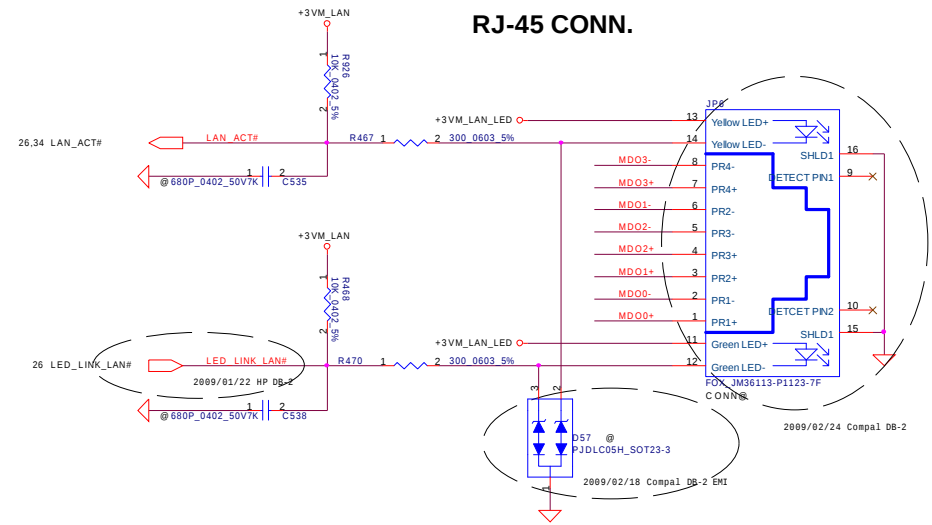
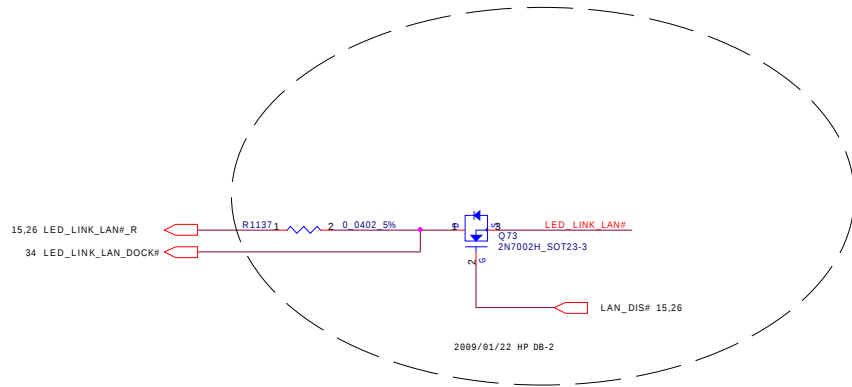
High 32 bit FB



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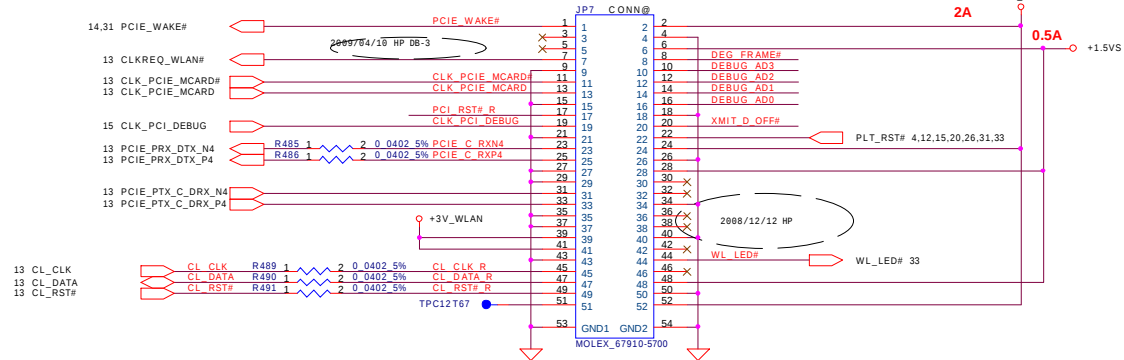
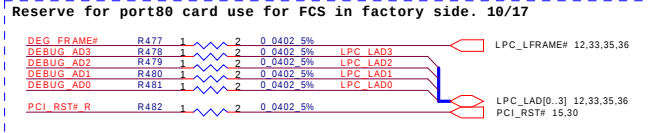
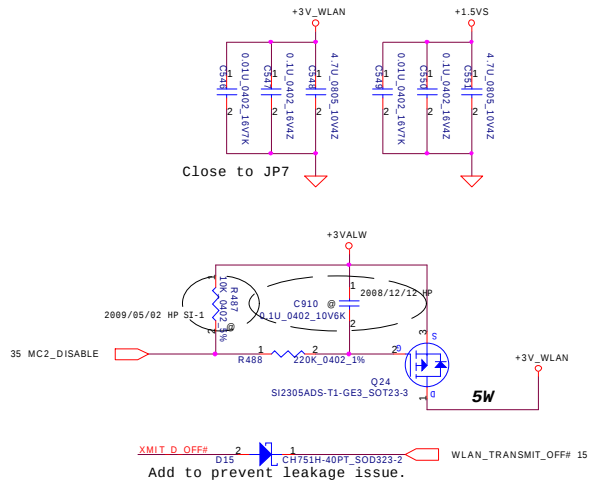


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Size	Document Number	LA-4901P		Rev	
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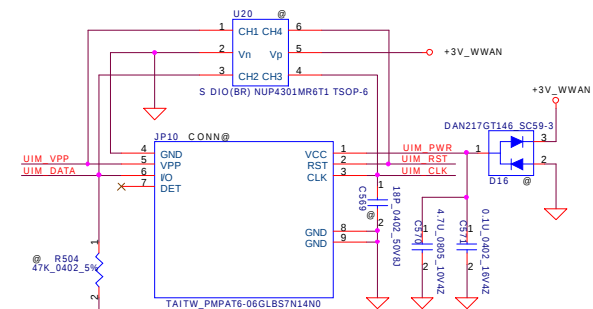
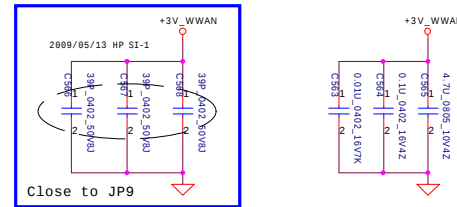
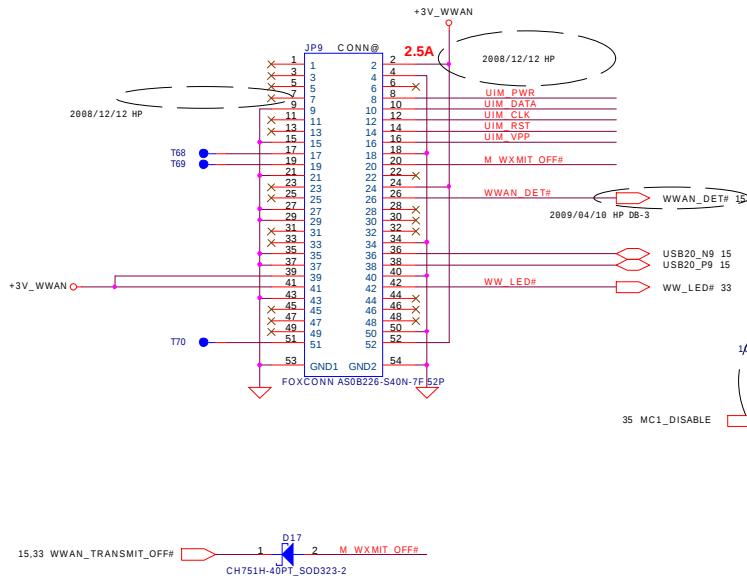


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Size	Document Number	Rev		Date	
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WLAN (Halt mini Card)

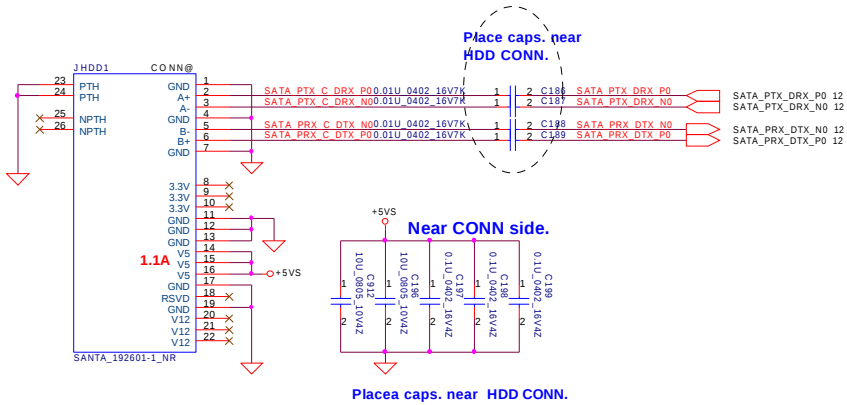


WWAN (Full mini Card)

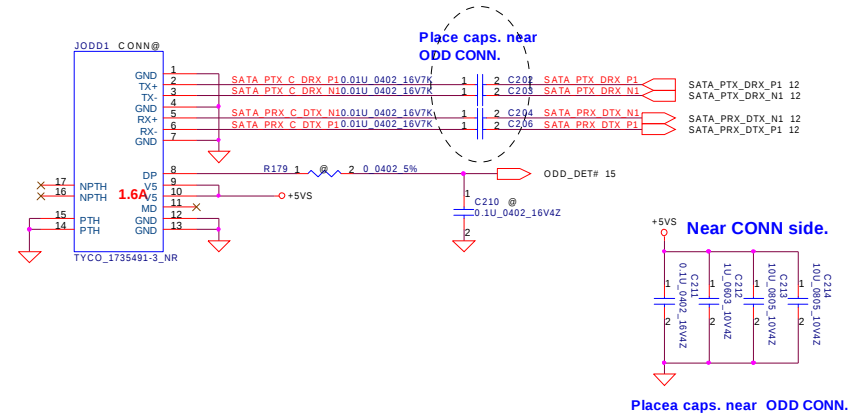


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				WLAN&WWAN	
				Size	Document Number
					LA-4901P
					Rev 1.0
Date:		Tuesday, December 15, 2009		Sheet 28 of 54	

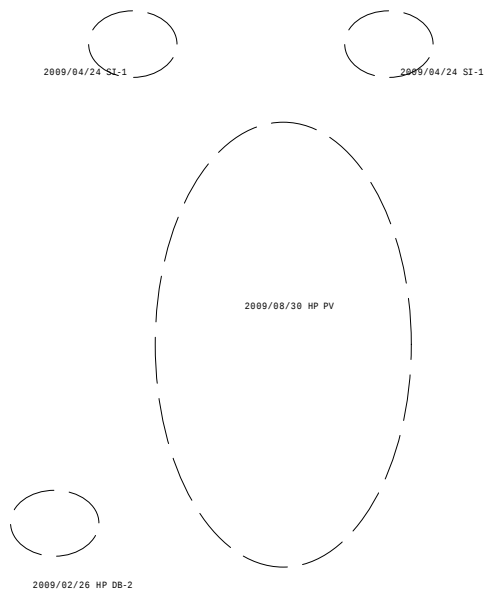
SATA HDD CONN.



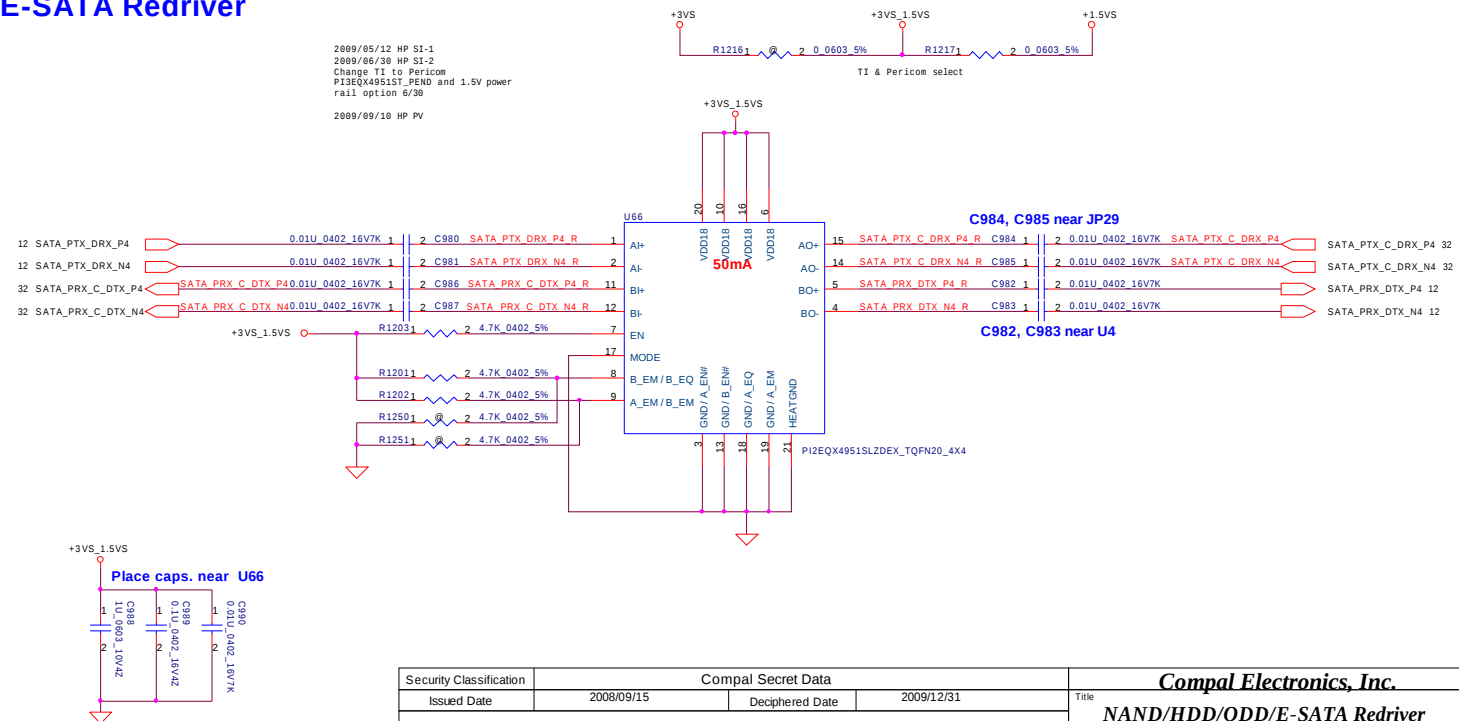
SATA ODD CONN.



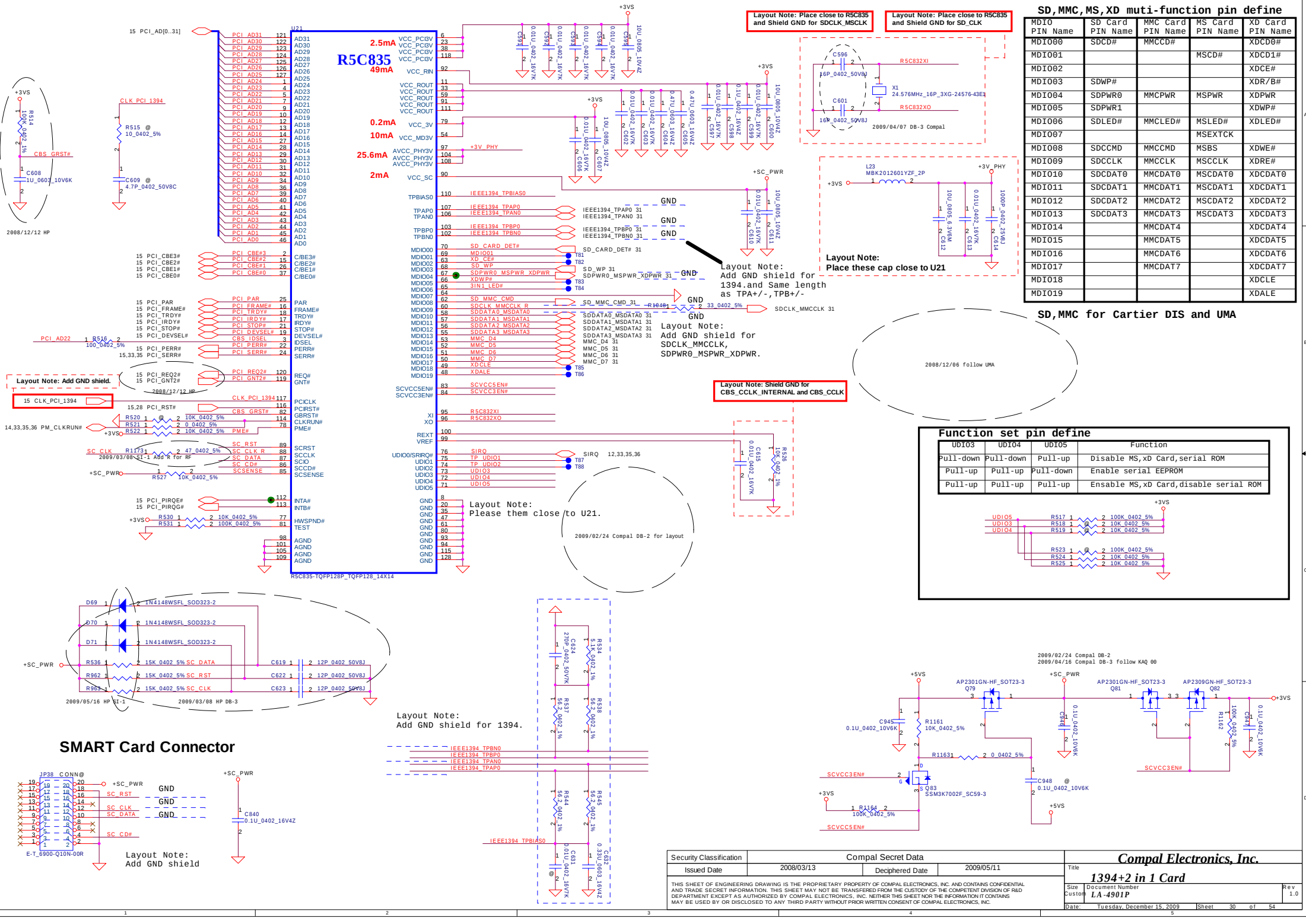
NAND FLASH



E-SATA Redriver



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				Date	Tuesday, December 15, 2009
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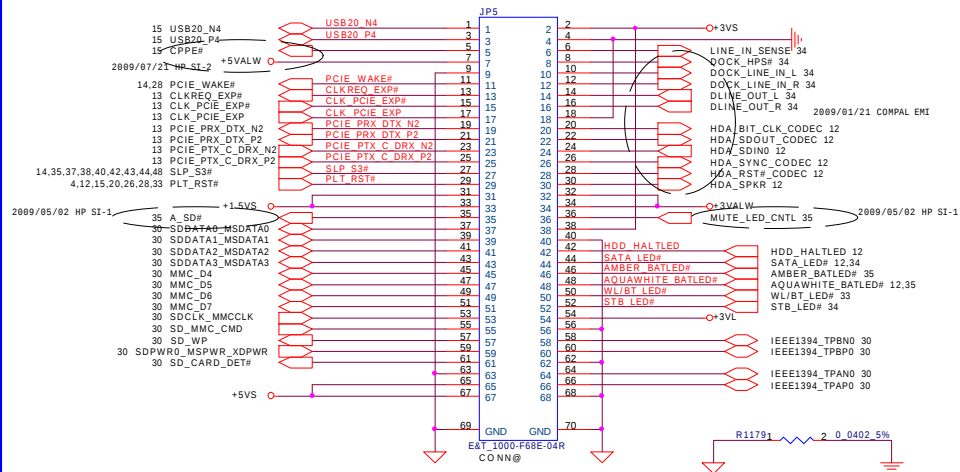
SD, MMC, MS, XD multi-function pin define				
MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SDCD#	MMCCD#		XDCD0#
MDIO01			MSCD#	XDCD1#
MDIO02				XDCE#
MDIO03	SDWP#			XDR/B#
MDIO04	SDPWR0	MMCPWR	MSPWR	XDPR
MDIO05	SDPWR1			XDWP#
MDIO06	SDLED#	MMCLCD#	MSLED#	XDLED#
MDIO07			MSEXTC	
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCLK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT0	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1	MMCDAT1	MSCDAT1	XDCDAT1
MDIO12	SDCDAT2	MMCDAT2	MSCDAT2	XDCDAT2
MDIO13	SDCDAT3	MMCDAT3	MSCDAT3	XDCDAT3
MDIO14		MMCDAT4		XDCDAT4
MDIO15		MMCDAT5		XDCDAT5
MDIO16		MMCDAT6		XDCDAT6
MDIO17		MMCDAT7		XDCDAT7
MDIO18				XDCL
MDIO19				XDALE

SD, MMC for Cartier DIS and UMA

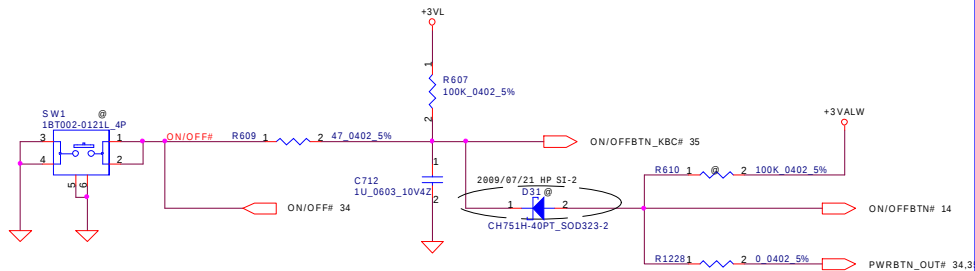
Function set pin define			
UDIO3	UDIO4	UDIO5	Function
Pull-down	Pull-down	Pull-up	Disable MS, XD Card, serial ROM
Pull-up	Pull-up	Pull-down	Enable serial EEPROM
Pull-up	Pull-up	Pull-up	Enable MS, XD Card, disable serial ROM

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Compal Electronics, Inc.			
Title 1394+2 in 1 Card			
Size	Document Number	Rev 1.0	
Customer	LA-4901P		
Date	Tuesday, December 15, 2009	Sheet	30 of 54

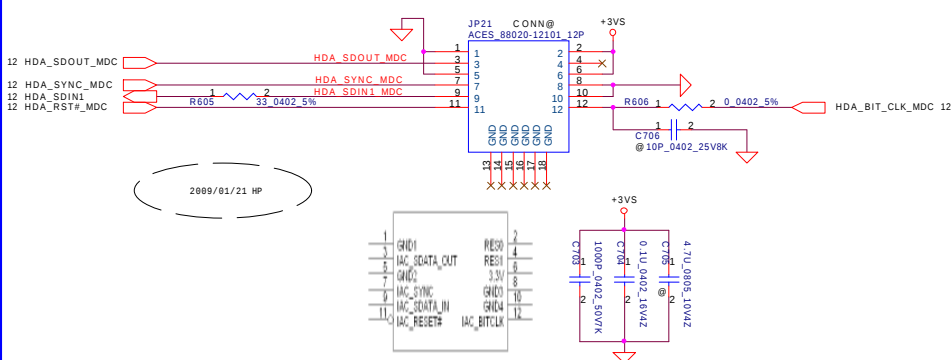
AUDIO BOARD CONNECTOR (MALE)



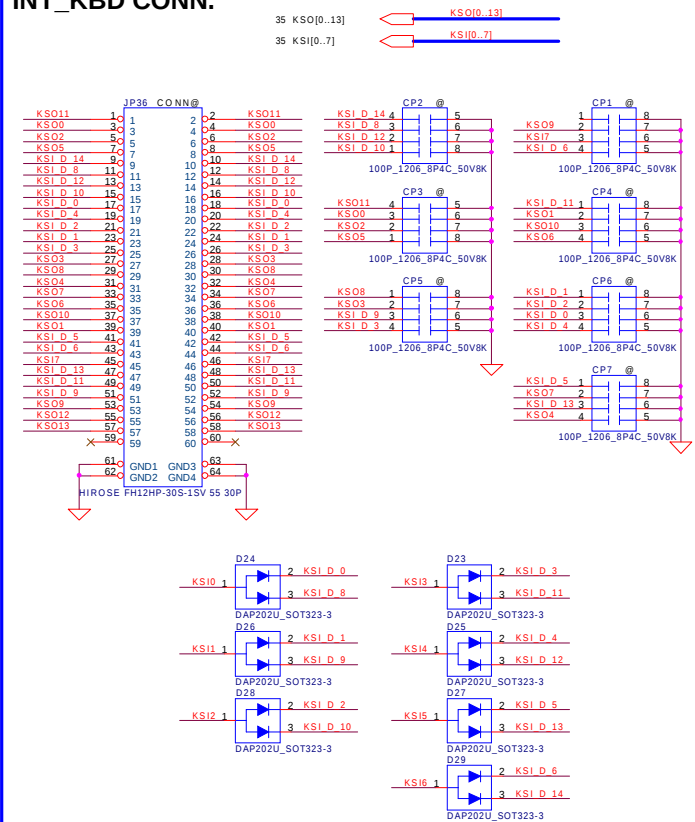
Power Button



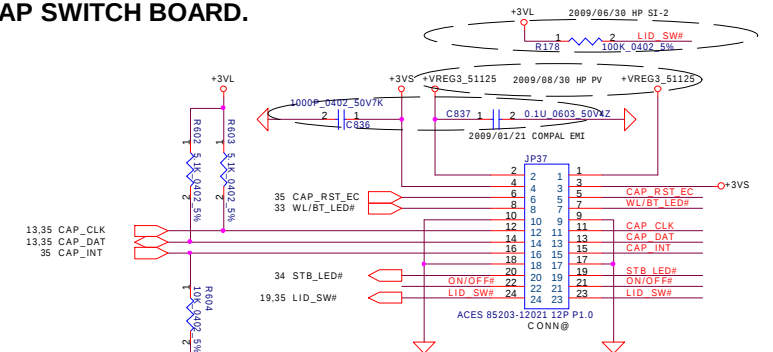
MDC 1.5 Conn.



INT_KBD CONN.

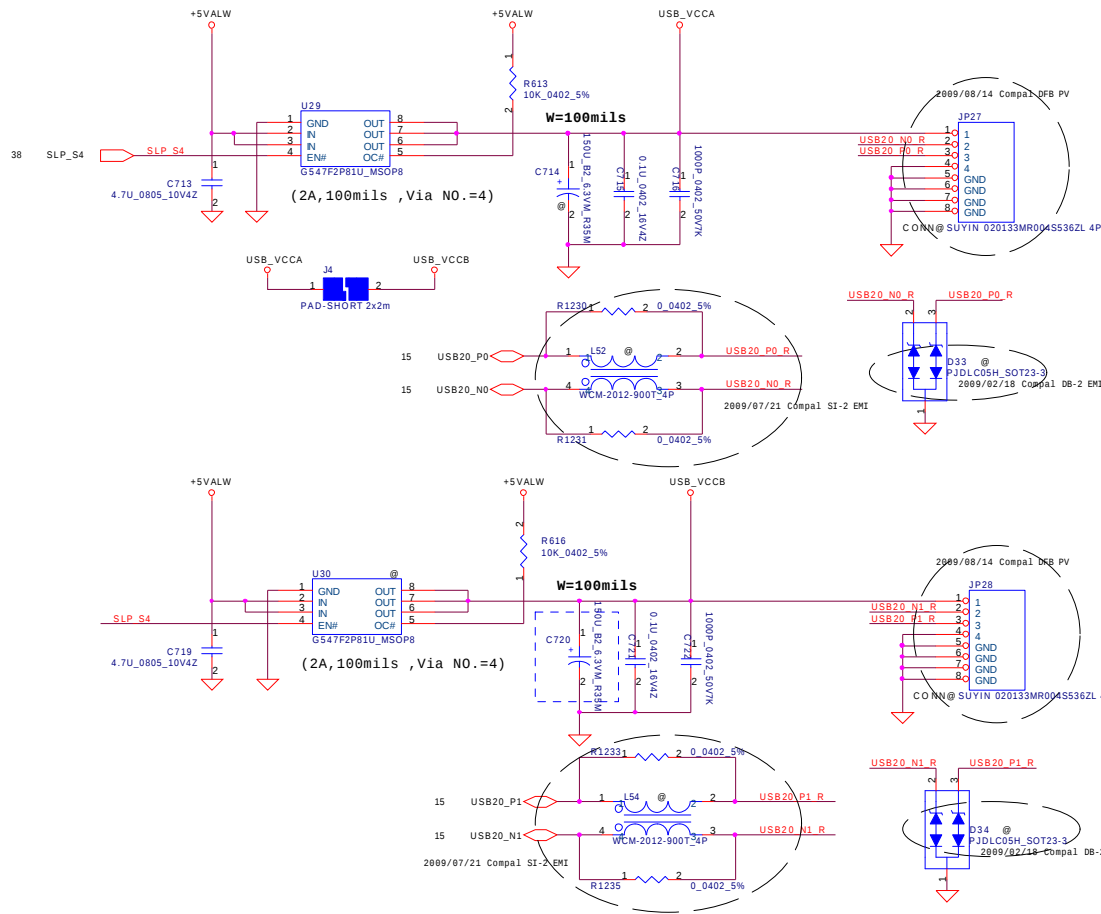


CAP SWITCH BOARD.



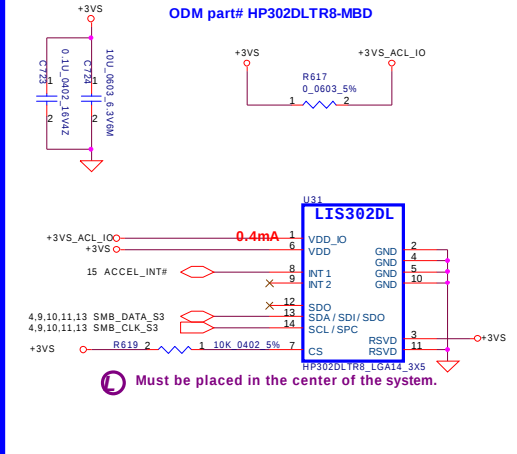
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2009/12/31	Title	MDC/KBD/ON OFF/CAP
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USB CONN.

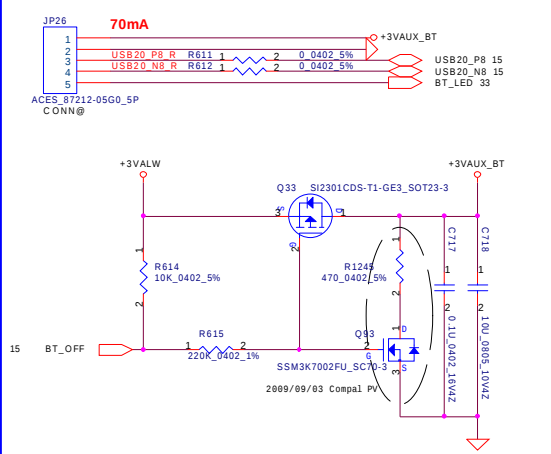


ACCELEROMETER

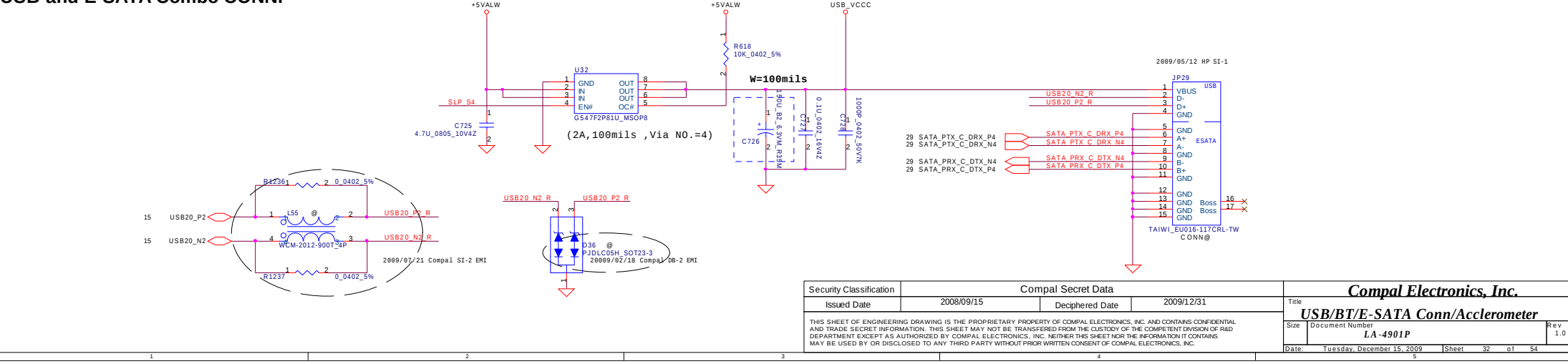
ODM part# HP302DLTR8-MBD



BT Connector



USB and E-SATA Combo CONN.



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LPC Debug Port

The diagram illustrates the pinout of the LPC1114 debug port. The pins are organized into two columns, with the left column representing the microcontroller pins and the right column representing the debug port connector pins. The pins are numbered 1 through 24. The pins are connected as follows:

- 80S1_RECOVER# (Pin 1) is connected to R632 (Pin 2).
- 100K (Pin 3) is connected to 0402_5% (Pin 4).
- +3V_L (Pin 5) is connected to BP*_DEBUG (Pin 6).
- BP*_DEBUG (Pin 6) is connected to JP13 (Pin 7).
- C_CONN# (Pin 8) is connected to C_CONN# (Pin 9).
- JP13 (Pin 9) is connected to C_CONN# (Pin 10).
- Ground (Pin 11) is connected to LPC_PCI_CLK (Pin 12).
- Ground (Pin 13) is connected to LPC_FRAME# (Pin 14).
- +VSS (Pin 15) is connected to LPC_RESET# (Pin 16).
- +VSS (Pin 17) is connected to LPC_ADO (Pin 18).
- LPC_ADO (Pin 18) is connected to LPC_AD1 (Pin 19).
- LPC_AD1 (Pin 19) is connected to LPC_AD2 (Pin 20).
- LPC_AD2 (Pin 20) is connected to LPC_AD3 (Pin 21).
- VCC_3VA (Pin 22) is connected to PWR_LED# (Pin 23).
- PWR_LED# (Pin 23) is connected to CAPS_LED# (Pin 24).
- CAPS_LED# (Pin 24) is connected to NUM_LED# (Pin 25).
- NUM_LED# (Pin 25) is connected to SPI_CLK (Pin 26).
- SPI_CLK (Pin 26) is connected to SPI_CS# (Pin 27).
- SPI_CS# (Pin 27) is connected to SPI_SI (Pin 28).
- SPI_SI (Pin 28) is connected to SPI_SO (Pin 29).
- SPI_SO (Pin 29) is connected to SPI_HOLD# (Pin 30).
- SPI_HOLD# (Pin 30) is connected to Reserved (Pin 31).
- Reserved (Pin 31) is connected to Reserved (Pin 32).
- Reserved (Pin 32) is connected to Reserved (Pin 33).
- Reserved (Pin 33) is connected to Reserved (Pin 34).
- Reserved (Pin 34) is connected to Reserved (Pin 35).
- Reserved (Pin 35) is connected to Reserved (Pin 36).
- Reserved (Pin 36) is connected to Reserved (Pin 37).
- Reserved (Pin 37) is connected to Reserved (Pin 38).
- Reserved (Pin 38) is connected to Reserved (Pin 39).
- Reserved (Pin 39) is connected to Reserved (Pin 40).
- Reserved (Pin 40) is connected to Reserved (Pin 41).
- Reserved (Pin 41) is connected to Reserved (Pin 42).
- Reserved (Pin 42) is connected to Reserved (Pin 43).
- Reserved (Pin 43) is connected to Reserved (Pin 44).
- Reserved (Pin 44) is connected to Reserved (Pin 45).
- Reserved (Pin 45) is connected to Reserved (Pin 46).
- Reserved (Pin 46) is connected to Reserved (Pin 47).
- Reserved (Pin 47) is connected to Reserved (Pin 48).
- Reserved (Pin 48) is connected to Reserved (Pin 49).
- Reserved (Pin 49) is connected to Reserved (Pin 50).
- Reserved (Pin 50) is connected to Reserved (Pin 51).
- Reserved (Pin 51) is connected to Reserved (Pin 52).
- Reserved (Pin 52) is connected to Reserved (Pin 53).
- Reserved (Pin 53) is connected to Reserved (Pin 54).
- Reserved (Pin 54) is connected to Reserved (Pin 55).
- Reserved (Pin 55) is connected to Reserved (Pin 56).
- Reserved (Pin 56) is connected to Reserved (Pin 57).
- Reserved (Pin 57) is connected to Reserved (Pin 58).
- Reserved (Pin 58) is connected to Reserved (Pin 59).
- Reserved (Pin 59) is connected to Reserved (Pin 60).
- Reserved (Pin 60) is connected to Reserved (Pin 61).
- Reserved (Pin 61) is connected to Reserved (Pin 62).
- Reserved (Pin 62) is connected to Reserved (Pin 63).
- Reserved (Pin 63) is connected to Reserved (Pin 64).
- Reserved (Pin 64) is connected to Reserved (Pin 65).
- Reserved (Pin 65) is connected to Reserved (Pin 66).
- Reserved (Pin 66) is connected to Reserved (Pin 67).
- Reserved (Pin 67) is connected to Reserved (Pin 68).
- Reserved (Pin 68) is connected to Reserved (Pin 69).
- Reserved (Pin 69) is connected to Reserved (Pin 70).
- Reserved (Pin 70) is connected to Reserved (Pin 71).
- Reserved (Pin 71) is connected to Reserved (Pin 72).
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- Reserved (Pin 96) is connected to Reserved (Pin 97).
- Reserved (Pin 97) is connected to Reserved (Pin 98).
- Reserved (Pin 98) is connected to Reserved (Pin 99).
- Reserved (Pin 99) is connected to Reserved (Pin 100).

[illegible]

TrackPoint CONN.

The diagram shows the TrackPoint connector (JP24) with 12 pins. Pin 1 is connected to +5VS. Pin 2 is connected to SP_DATA. Pin 3 is connected to SP_CLK. Pin 4 is connected to TP_DATA. Pin 5 is connected to TP_CLK. Pin 6 is connected to TP_DATA. Pin 7 is connected to TP_CLK. Pin 8 is connected to TP_DATA. Pin 9 is connected to TP_CLK. Pin 10 is connected to TP_DATA. Pin 11 is connected to TP_CLK. Pin 12 is connected to TP_DATA. The connector is labeled ACES 87153-08011 CONN@.

The diagram also shows a 0.1uF 0402 16V4Z capacitor (C709) connected between +5VS and ground.

The diagram also shows a 2009/06/02 Compal SI-2 for DFB connector (JP25) with 12 pins. Pin 1 is connected to +5VS. Pin 2 is connected to TP_DATA. Pin 3 is connected to TP_CLK. Pin 4 is connected to TP_DATA. Pin 5 is connected to TP_CLK. Pin 6 is connected to TP_DATA. Pin 7 is connected to TP_CLK. Pin 8 is connected to TP_DATA. Pin 9 is connected to TP_CLK. Pin 10 is connected to TP_DATA. Pin 11 is connected to TP_CLK. Pin 12 is connected to TP_DATA. The connector is labeled ACES 85203-04021 CONN@.

The diagram also shows a D32 @ PJDLC05H SOT23-3 2009/02/18 Compal DB-2 EMI component connected between TP_DATA and TP_CLK.

WLAN/WWAN/BT LED

2009/04/24 HP SI-1
2009/08/30 HP SI-2b

28 WL_LED# WL_LED# R1191 2 0 0402 5%

15,28 WWAN_TRANSMIT_OFF#

28 WW_LED# WW_LED# R1192 2 0 0402 5%

32 BT_LED

Q60B
2N7002DWH_SOT363-6

Q60A
2N7002DWH_SOT363-6

R953
47K 0402 5%

R954 1 2 100K 0402 5%

R955 1 2 100K 0402 5%

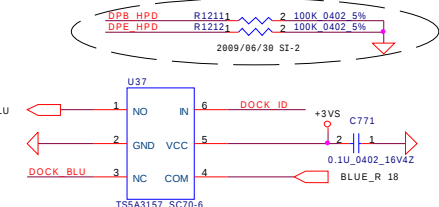
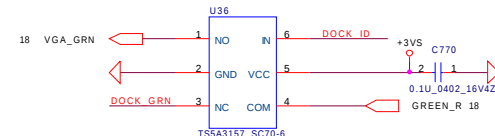
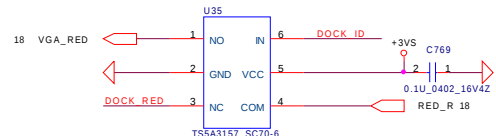
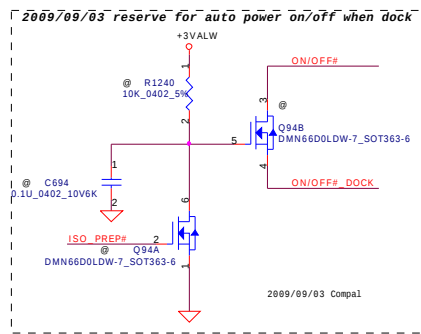
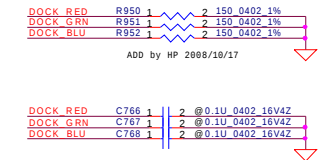
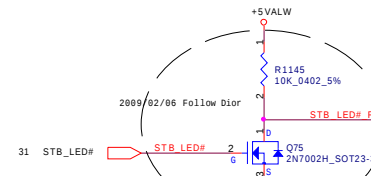
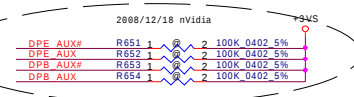
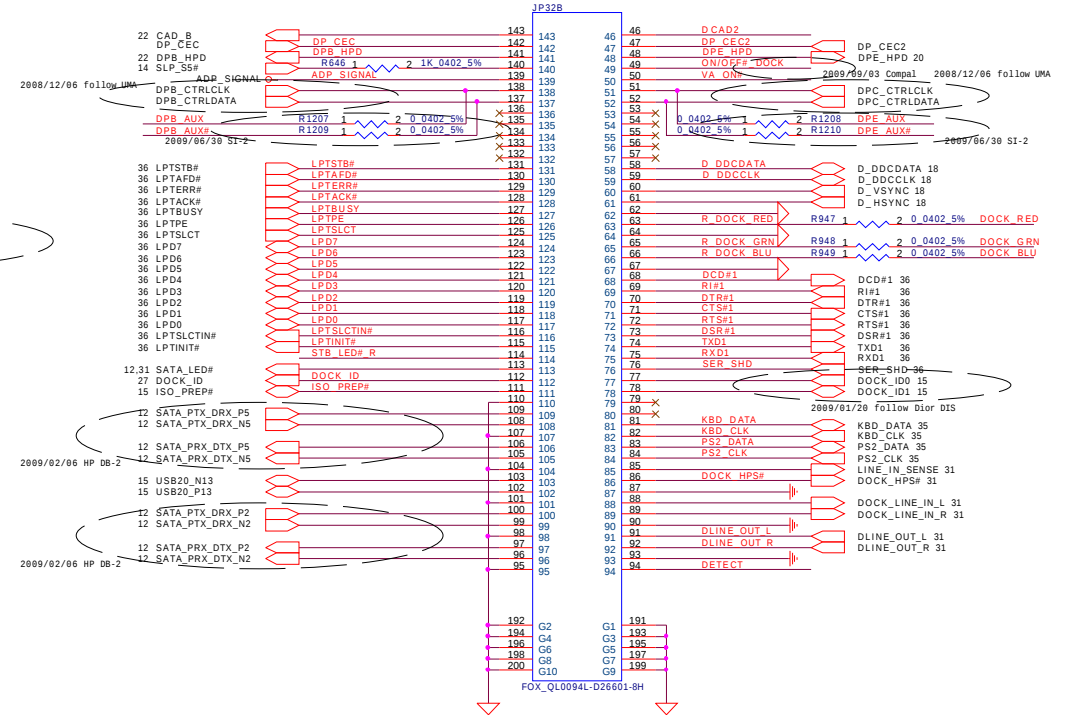
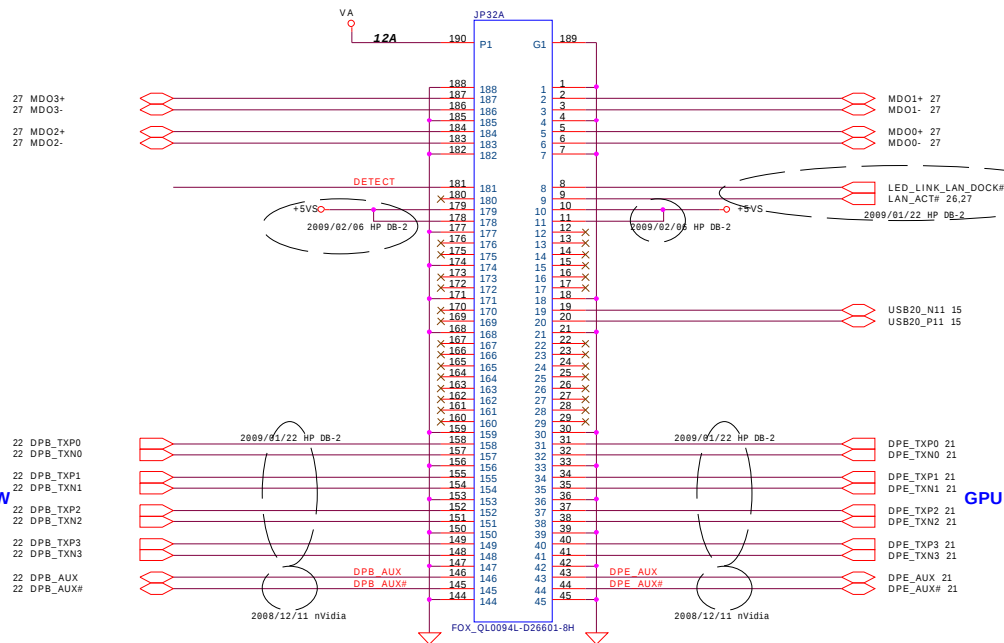
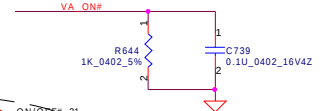
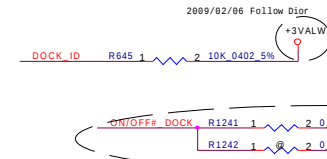
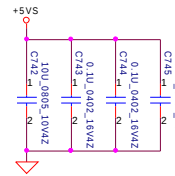
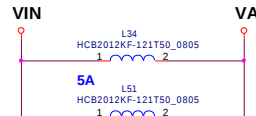
+3VS

[illegible]

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Issued Date	2008/09/15	Deciphered Date	2009/12/31	Size	Document Number LA-491P	Rev 1.0
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DOCKING CONNECT

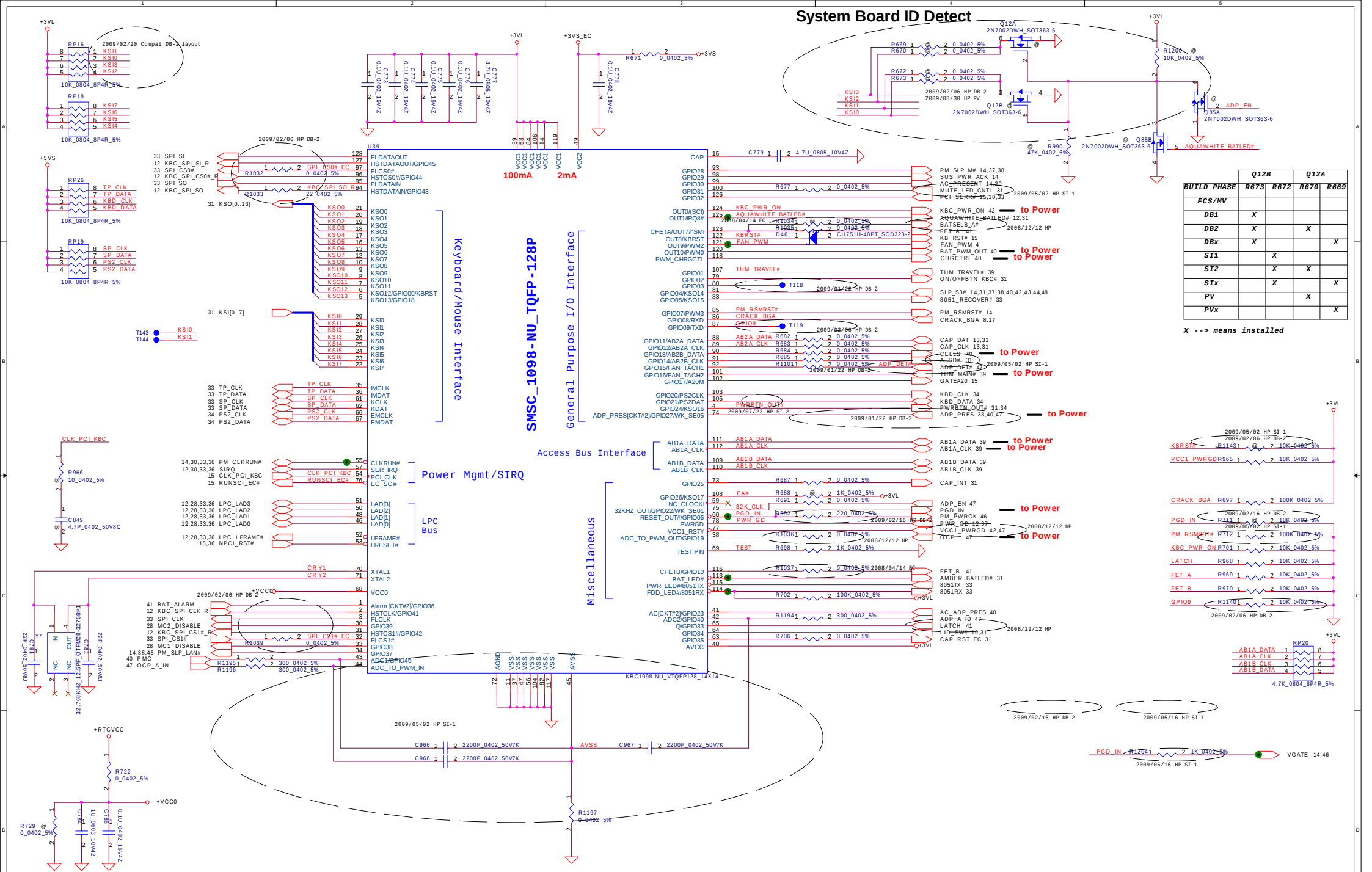
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IN	NC<-->COM	NO<-->COM
L	ON	OFF
H	OFF	ON

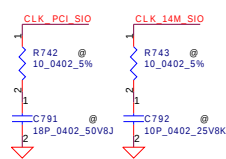
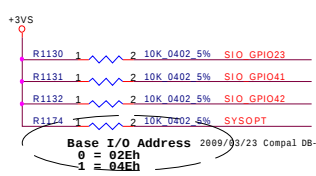
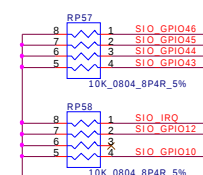
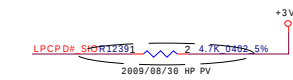
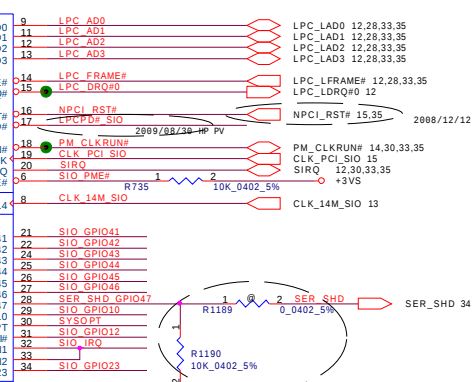
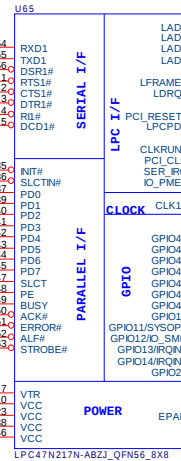
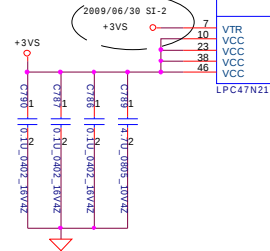
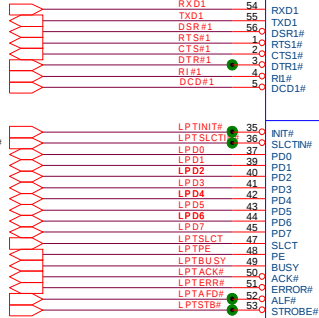
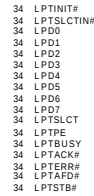
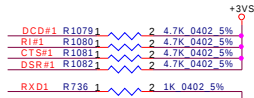
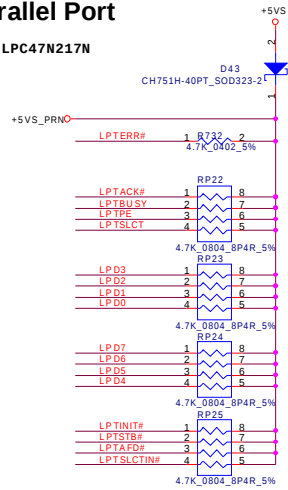
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Issued Date	2008/09/15	Deciphered Date	2009/12/31	Title	DOCK CONN	
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				Custor	LA-4901P	1.0
				Date:	Tuesday, December 15, 2009	Sheet 34 of 54

System Board ID Detect

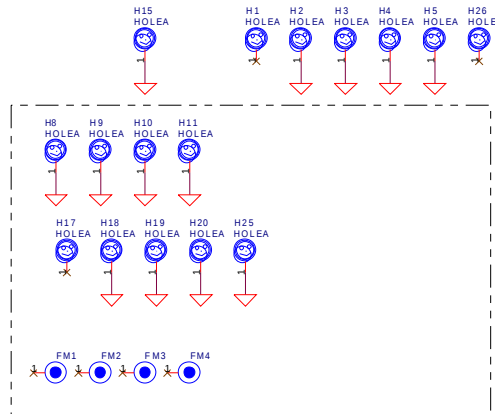
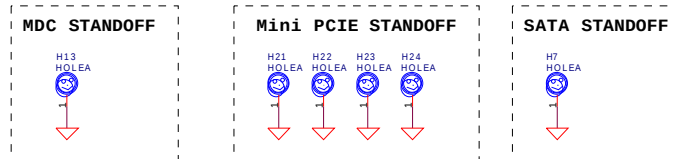
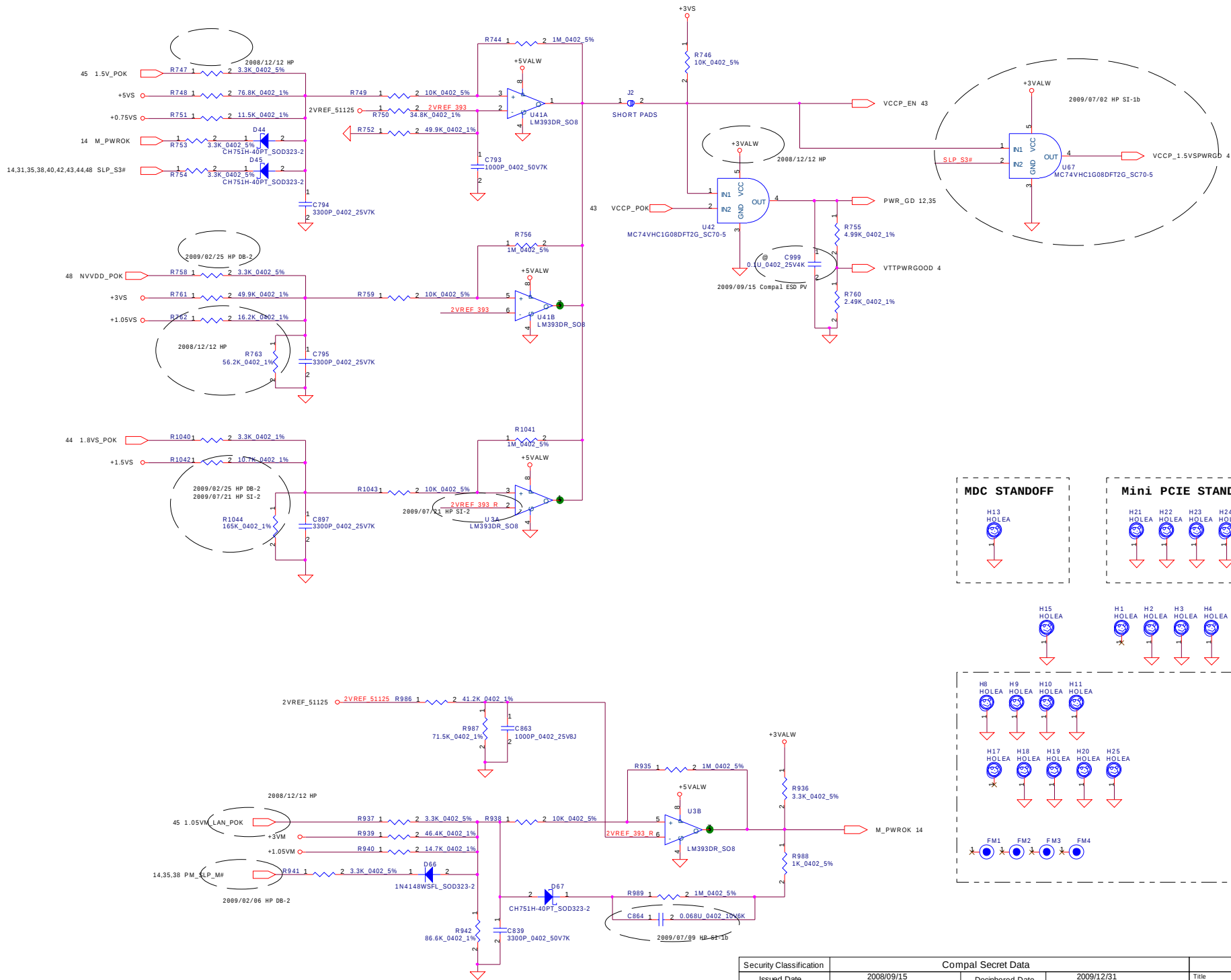


Parallel Port

TO LPC47N217N

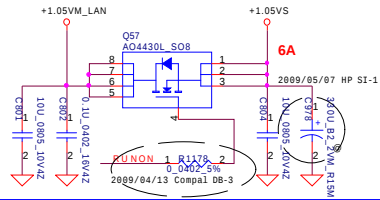


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2008/09/09	Deciphered Date	2009/09/09	Title	SUPER I/O LPC47N217N-ABZJ	
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					LA-4901P	1.0
				Date:	Tuesday, December 15, 2009	Sheet 36 of 54

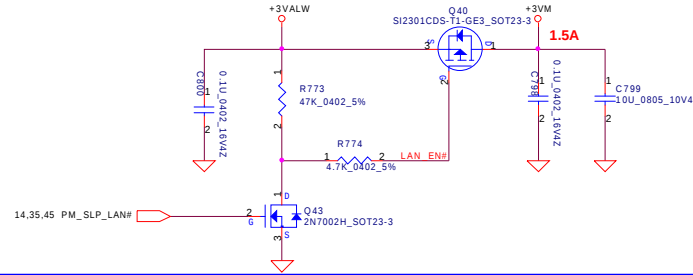


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Issued Date	2008/09/15	Deciphered Date	2009/12/31	Title	
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Size	Document Number	LA-4901P		Rev	
				1.0	
Date:	Tuesday, December 15, 2009	Sheet	37	of	54

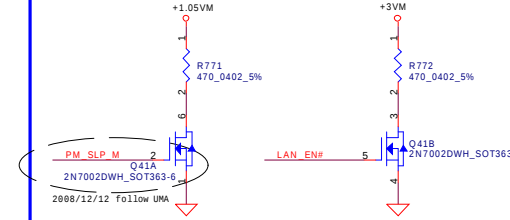
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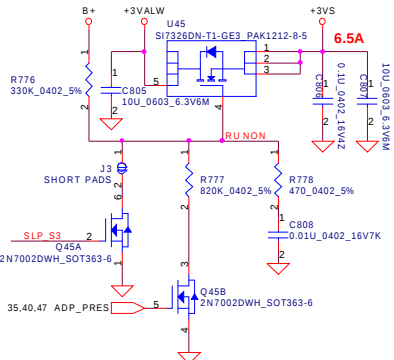
+3VALW to +3VM Transfer



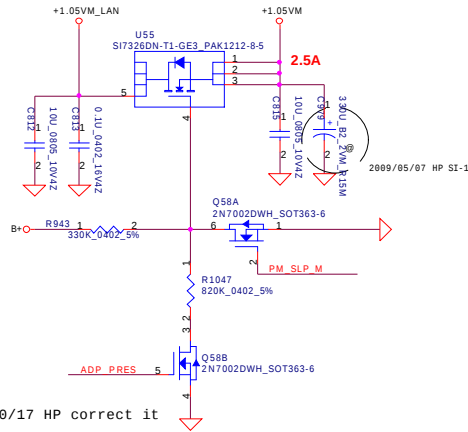
Discharge circuit-2 for V-M



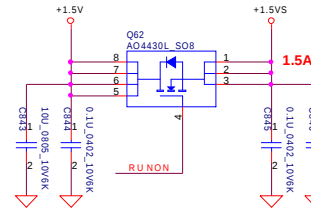
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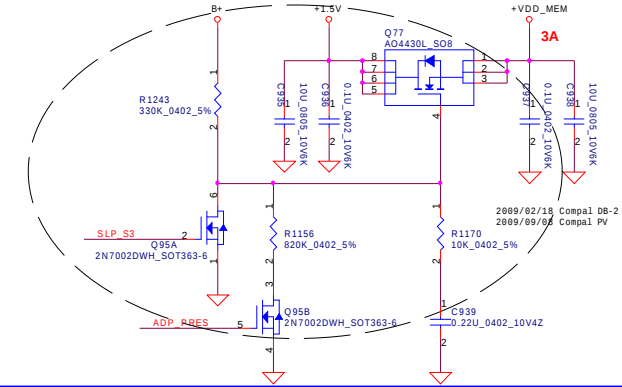
+1.05VM_LAN to +1.05VM Transfer



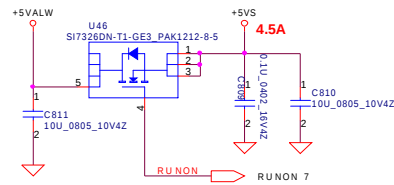
+1.5V to +1.5VS Transfer



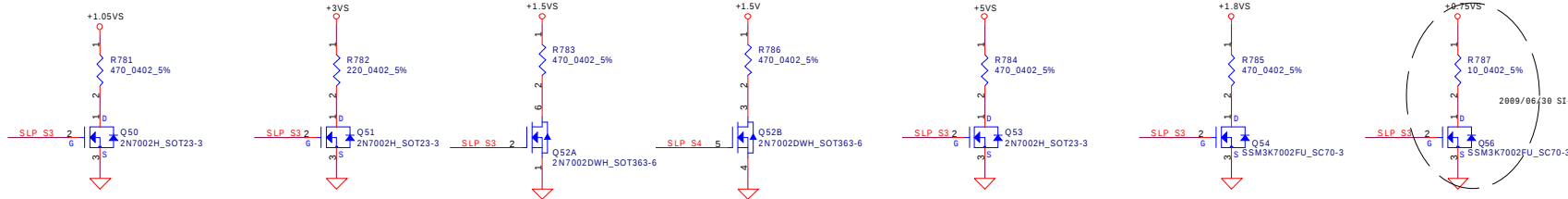
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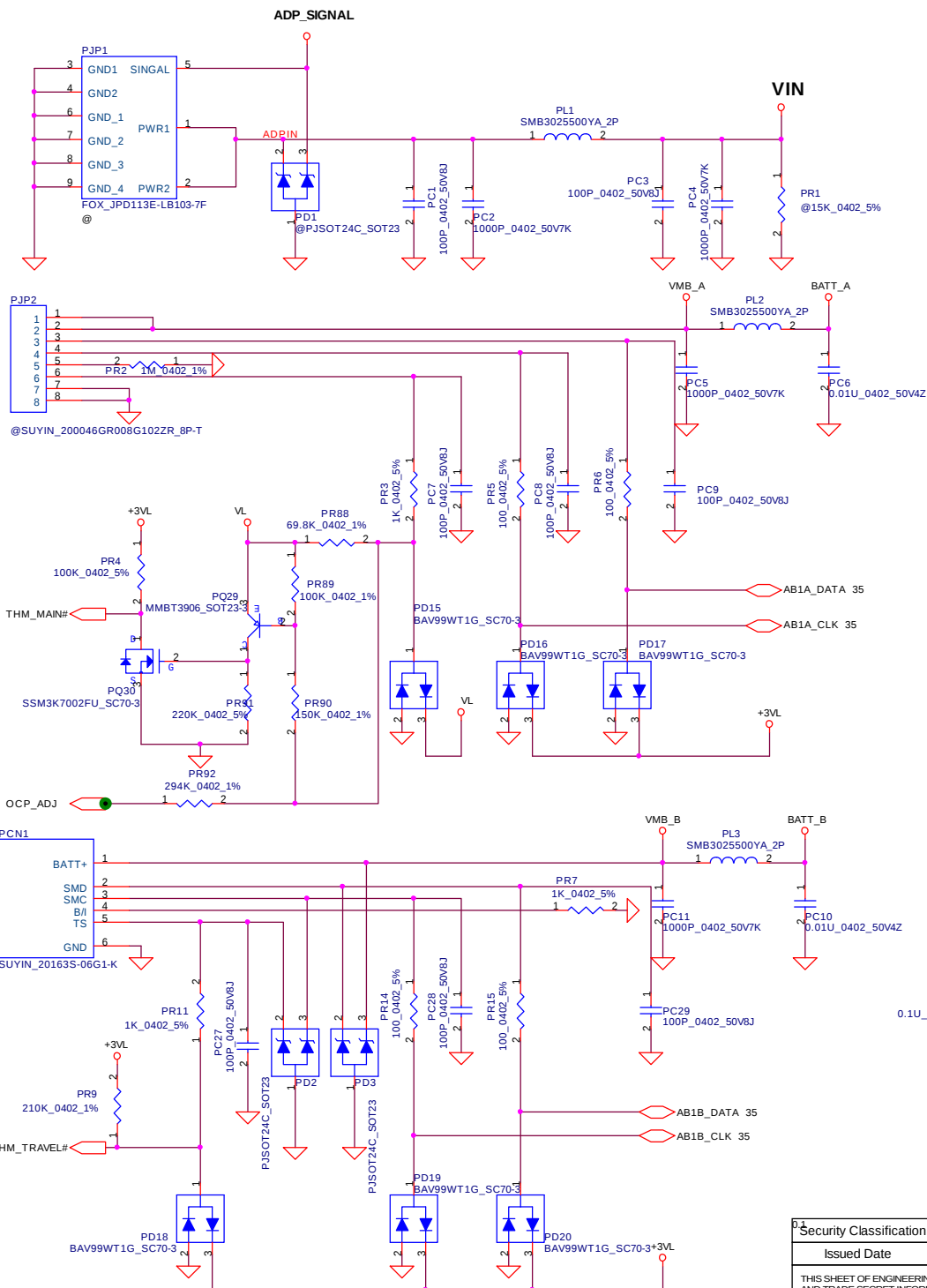
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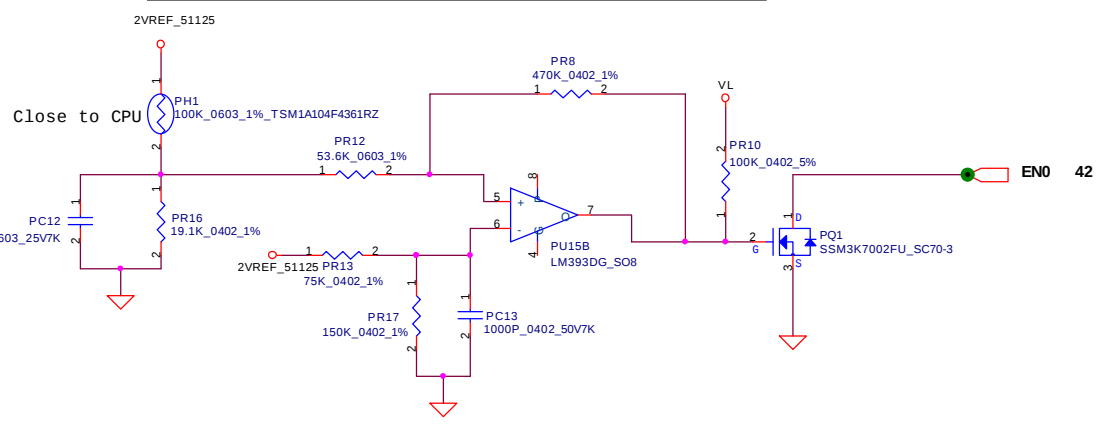
Discharge circuit-1



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Issued Date	2008/09/15	Deciphered Date	2009/12/31	DC/DC Circuits	
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Date:	Tuesday, December 15, 2009	Sheet	38	of	54

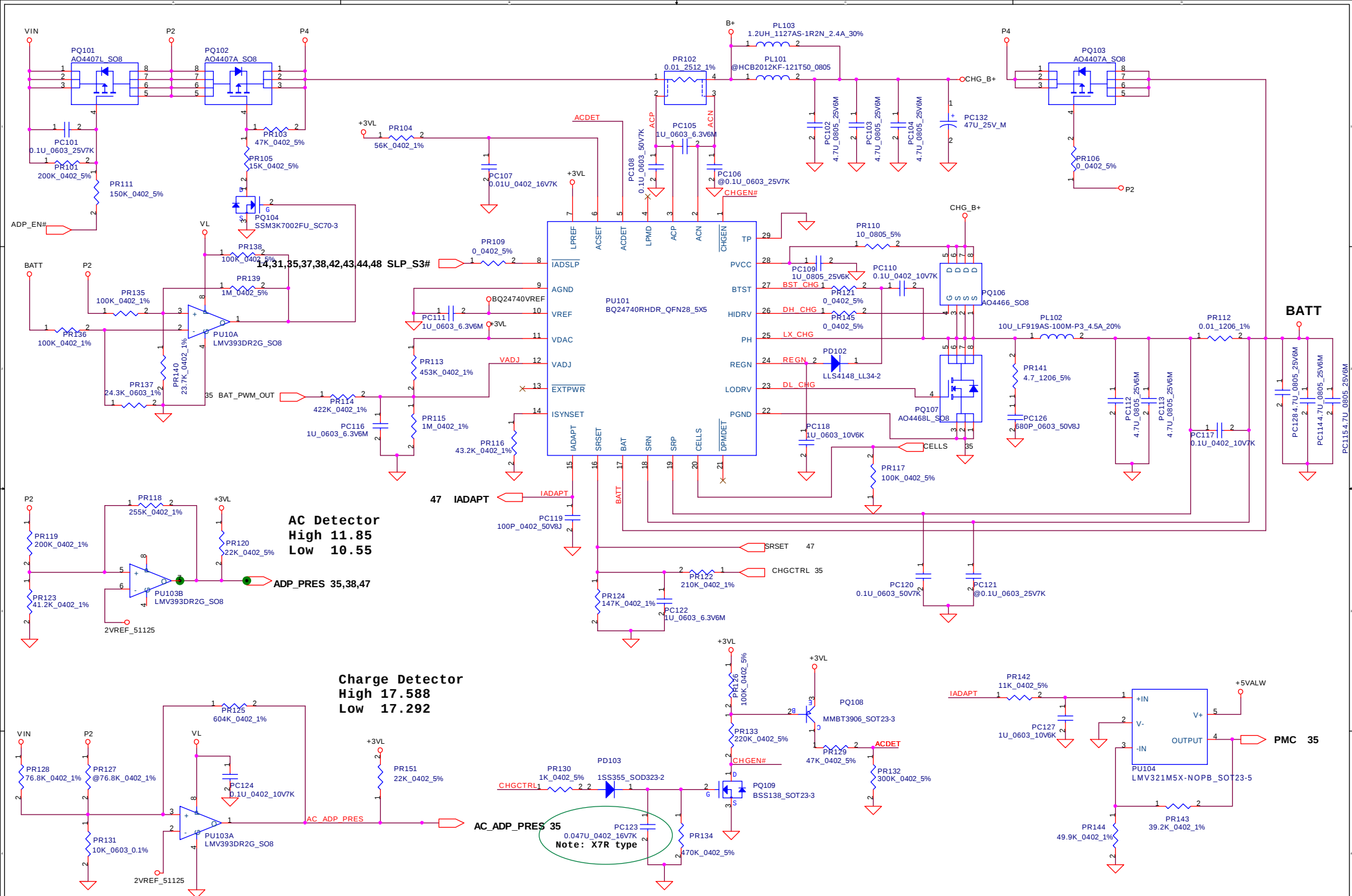


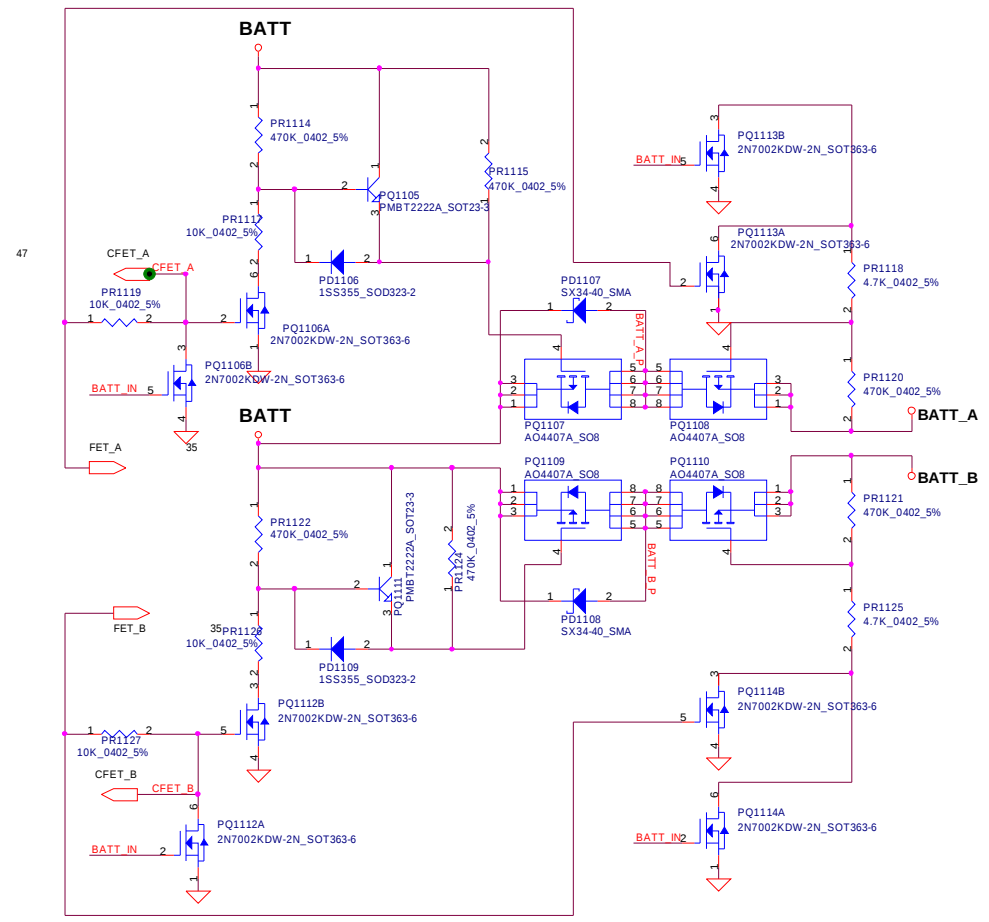
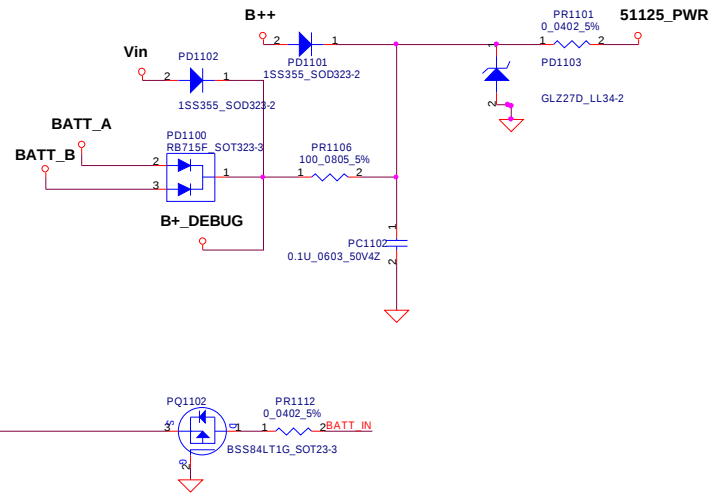
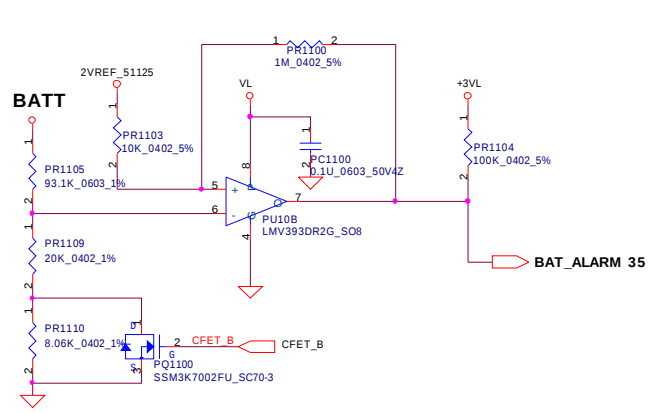
PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
(Need to be checked)



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Issued Date		2008/09/15		Deciphered Date		2009/09/15		Title			
								DC-IN/ BATTERY CONN			
Size		Document Number						Rev			
Custom		LA-4902P									
Date:		Tuesday, December 15, 2009		Sheet		39		of		54	

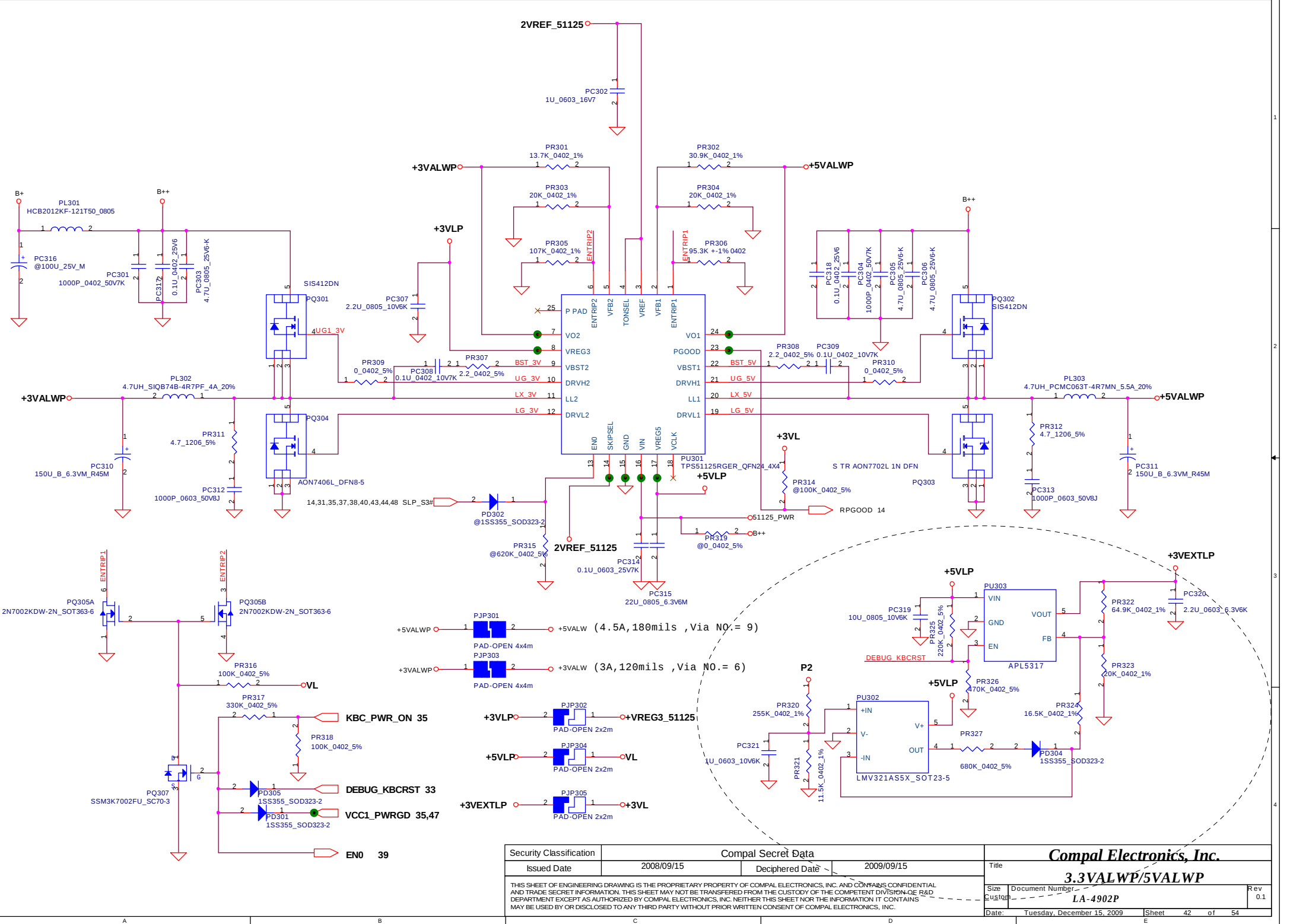
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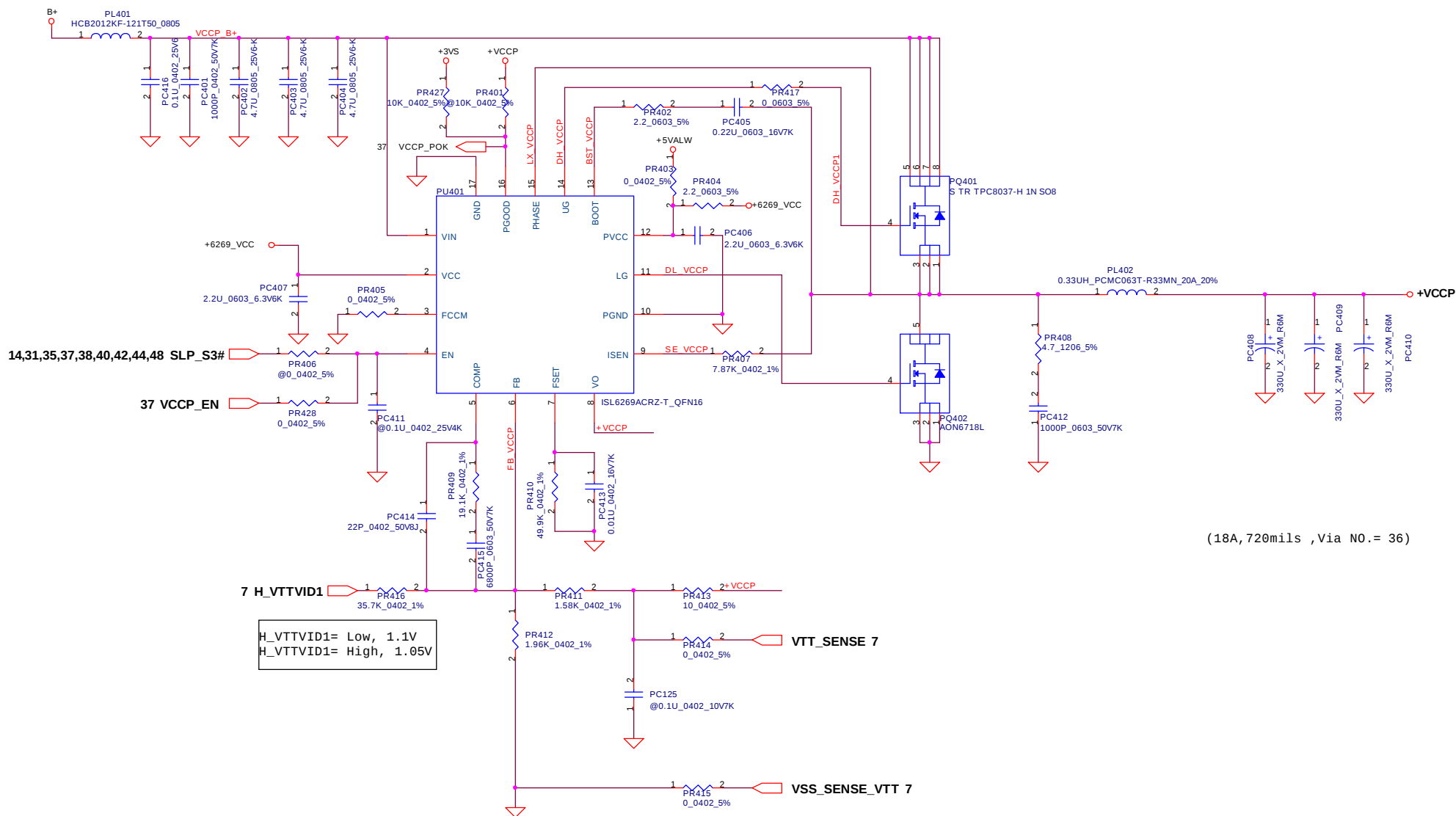


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Issued Date		2008/09/15	Deciphered Date		2009/09/15			
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				Battery selector				
				Size	Document Number		Rev	
				Customer	LA-4902P			
				Date:	Tuesday, December 15, 2009		Sheet 41 of 54	

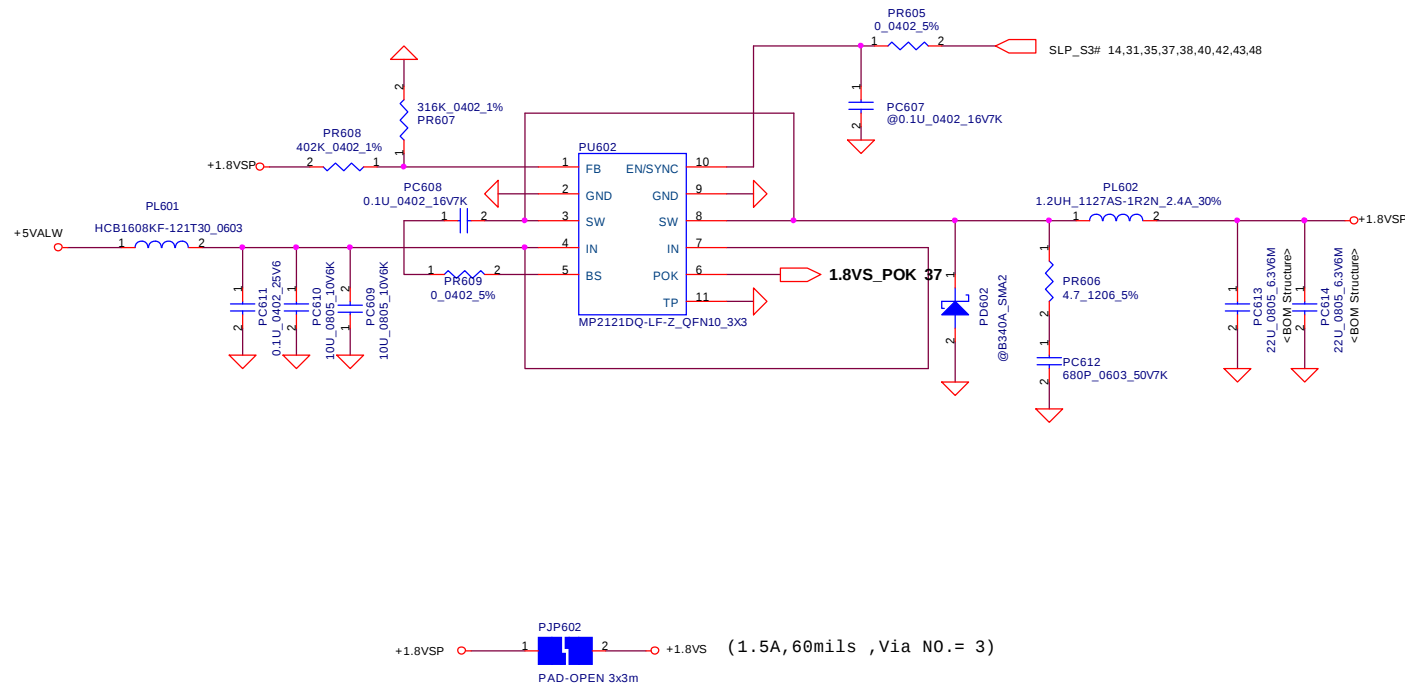
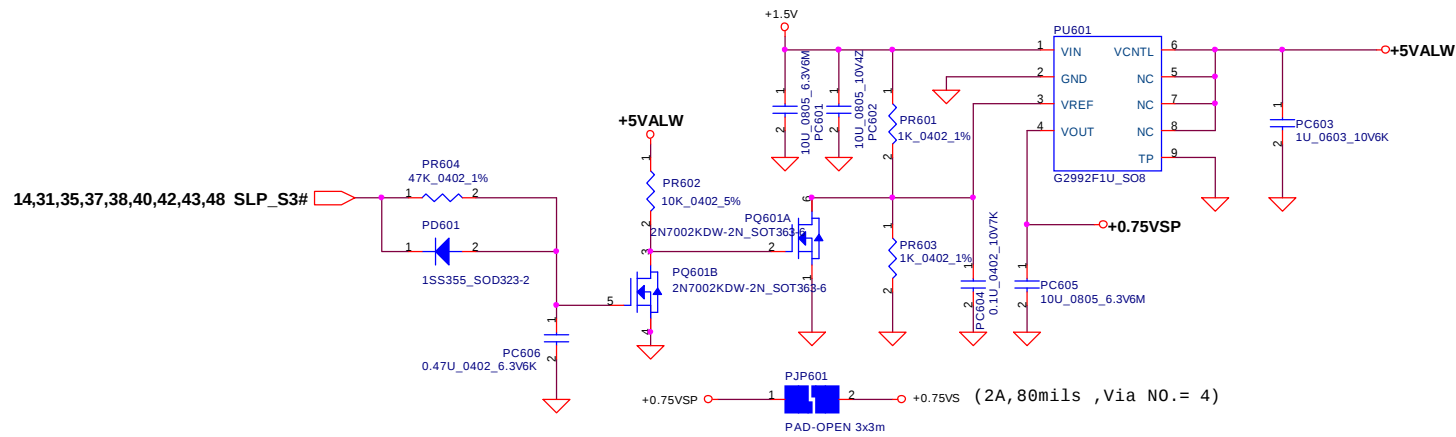
Compal Electronics, Inc.
Battery selector



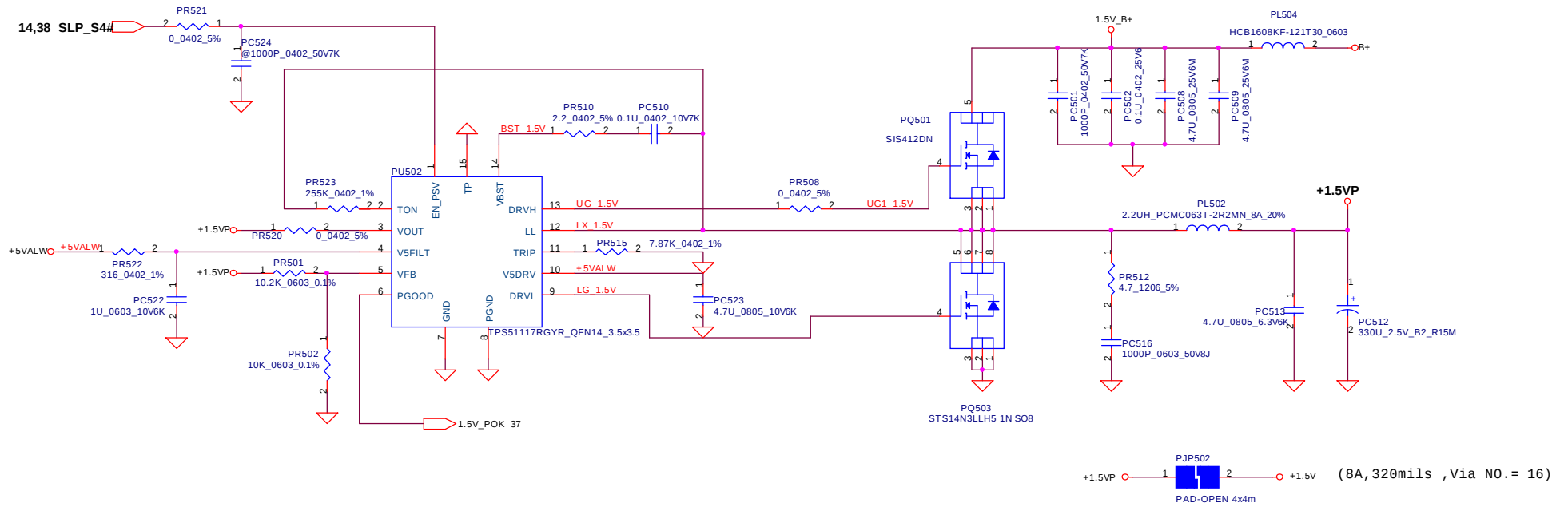
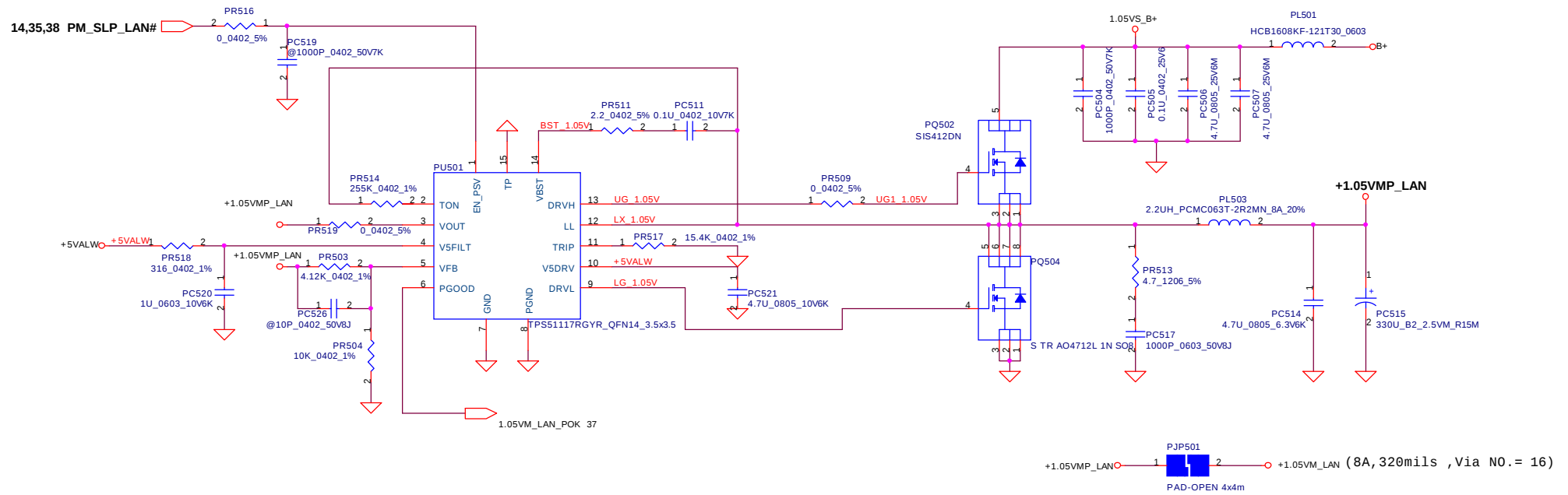
Security Classification		Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2009/09/15	3.3VALWP/5VALWP	
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				Document Number	0.1
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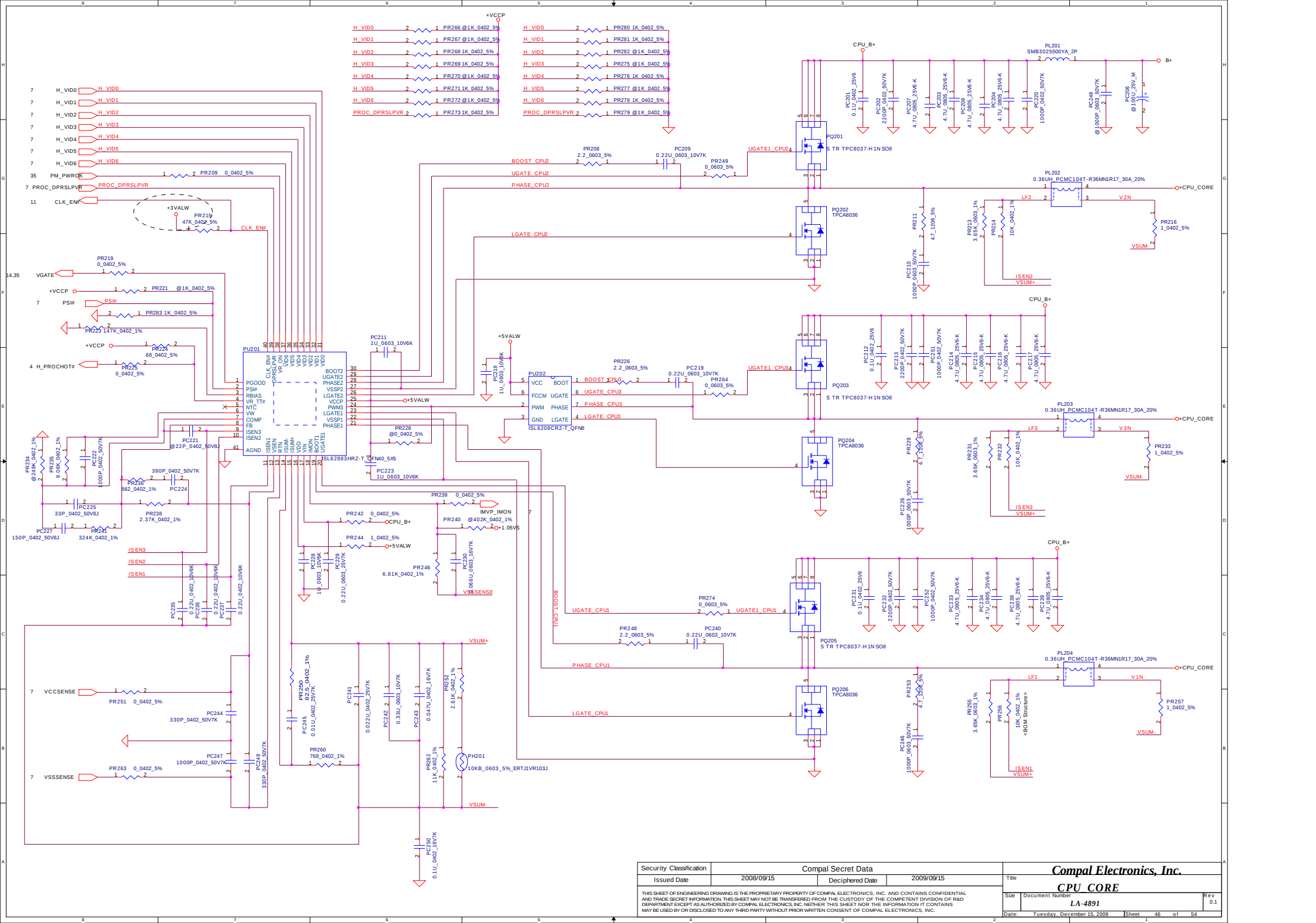
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Issued Date	2008/09/15	Deciphered Date	2009/09/15	Title	
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Size	Document Number	Rev		0.1	
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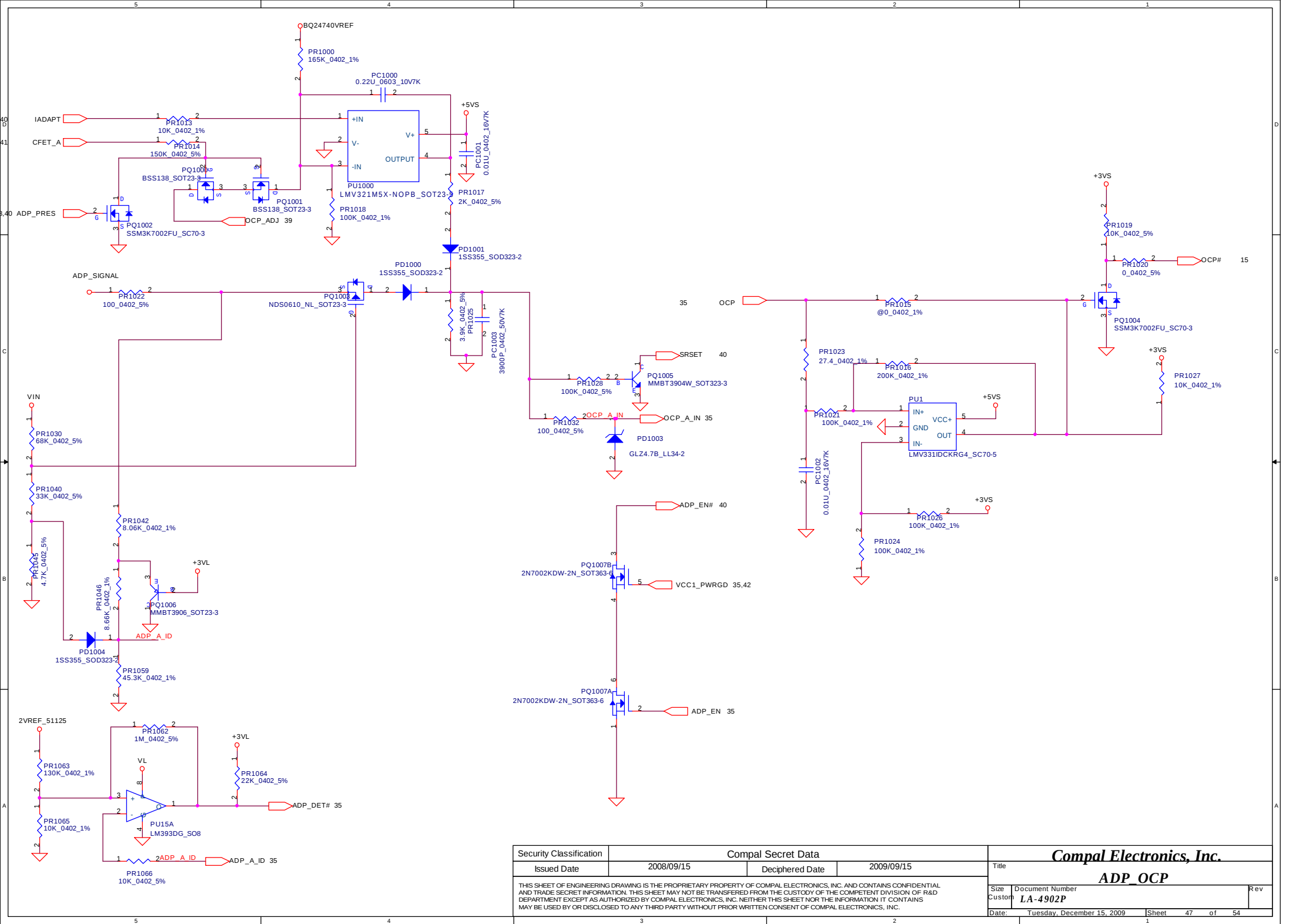


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Issued Date	2008/09/15	Deciphered Date	2009/09/15	Title	
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Size		Document Number		Rev	
		LA-4902P		0.1	
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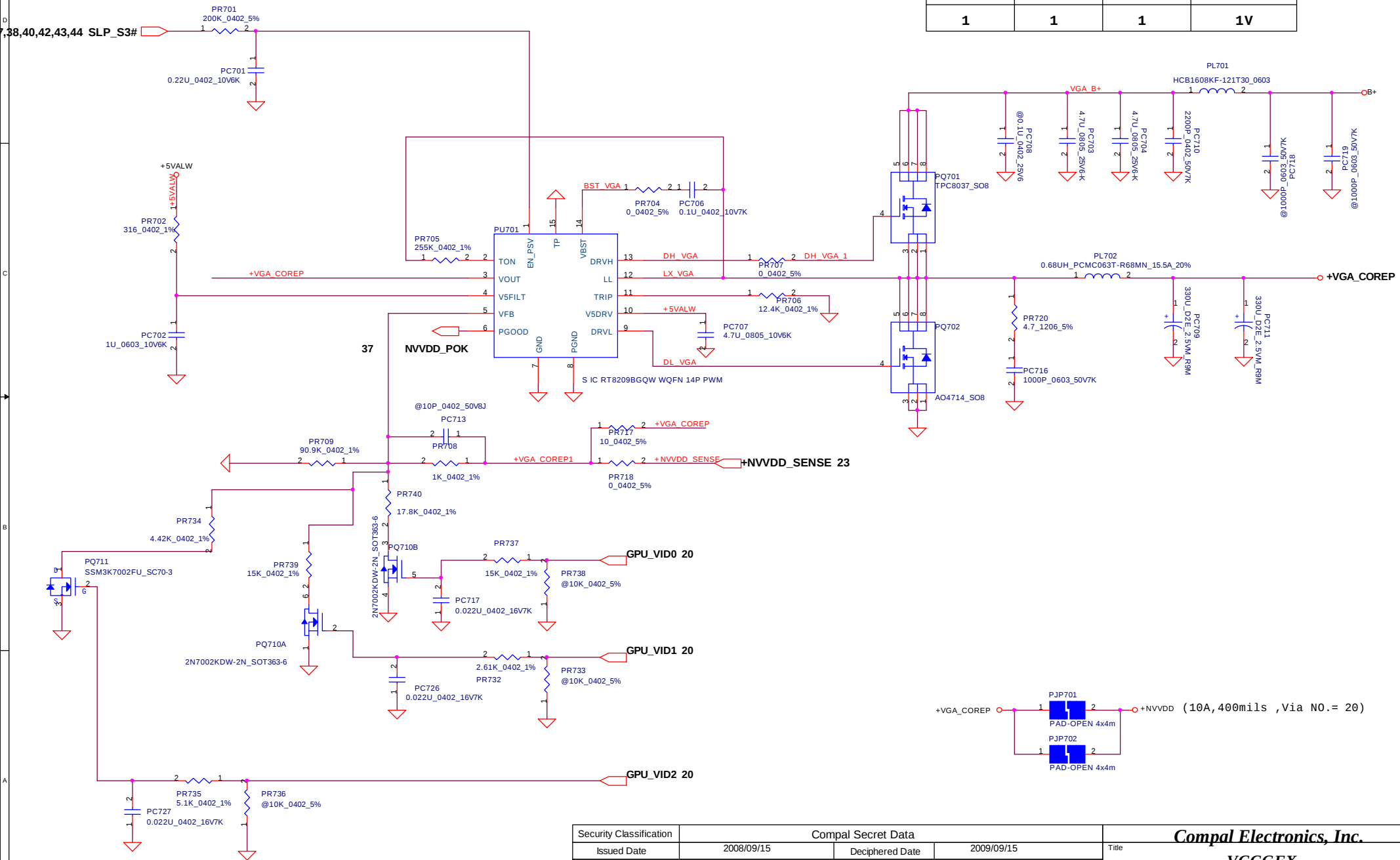
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Issued Date	2008/09/15	Deciphered Date	2009/09/15	Title	
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GPU_VID0	GPU_VID1	GPU_VID2	+NVVDD
0	0	0	0.75V
1	0	0	0.8V
1	1	0	0.85V
1	1	1	1V



Version Change List (P. I. R, List)for HW Circuit DB-1>> DB-2

Item	Page #	Date	Request Owner	Solution Description	Rev.
1	01	2009/02/06	HP	Del R4, R6, R8 for XDP.	0.2
2	01	2009/02/06	HP	Del R40 for Thermal sensor.	0.2
3	01	2009/02/06	HP	Del R34, R36, R46, R49, R37 for XDP.	0.2
4	01	2009/02/24	HP	Change R31 24.9K ohm to 1.5K ohm and R33 12.4K ohm to 750 ohm for intel WOW.	0.2
5	01	2009/02/25	HP	Debug port design guide changed XDP debug ports to CFG4 - pin 28, CFG5 - pin 30, CFG10 - pin 22, and CFG11 pin 24.	0.2
6	02	2009/02/19	HP	No install R60, R61.	0.2
7	12	2009/02/25	Compal	Install C193, C194 for WLAN nosie	0.2
8	12	2009/02/06	HP	Change R1026, R181, R185, R1027 from 15 ohm to 0 ohm.	0.2
9	12	2009/02/06	HP	Del C205, C207, C208, C209 for docking.	0.2
10	12	2009/02/06	HP	Change D1 pin 2 form +3VL to +VREG3_51125	0.2
11	12	2009/02/06	HP	Del JP15 pin 51, 53 trace (SMB_DATA_S3, SMB_CLK_S3) and add test point.	0.2
12	12	2009/02/11	HP	Add R1144 1K ohm	0.2
13	12	2009/02/11	HP	Add Test point for SATA bus.	0.2
14	12	2009/02/18	HP	Add NAND Flash dect pin (BRAID_DET)	0.2
15	13	2009/02/06	HP	Install R354	0.2
16	13	2009/02/06	HP	Add R1138 10K ohm	0.2
17	13	2009/02/20	HP	Change R1092, R1093 power sourece form +3VS to +3VS.	0.2
18	13	2009/02/20	HP	Del R208, R210	0.2
19	13	2009/02/22	HP	Add Q76A and Q76B for CBB	0.2
20	13	2009/02/22	HP	Reserve R1146 and R1147 for external VGA thermal	0.2
21	14	2009/01/22	HP	Del R238, because double pull down.	0.2
22	14	2009/02/19	HP	Del R288	0.2
23	14	2009/02/06	HP	Stuff R296	0.2
24	14	2009/02/06	HP	Add R1142 10K ohm	0.2
25	14	2009/02/25	Compal	Add C949 for RF	0.2
26	16	2009/01/22	HP	Del L1, C228, C229 and add test point.	0.2
27	16	2009/01/22	HP	Del L2, C241 and add test point.	0.2
28	16	2009/01/22	HP	Del C847 and add test point.	0.2
29	16	2009/01/22	HP	Del L4, C269 and add test point.	0.2
30	16	2009/01/22	HP	Del L3, C263, C262 and add test point.	0.2
31	16	2009/02/03	HP	Change R299, R300 form 10 ohm to 100ohm.	0.2
32	16	2009/02/03	HP	Change C278 form 0.1uF to 1uF.	0.2
33	16	2009/02/05	HP	Change C243, C244 form 10uF to 22uF.	0.2
34	18	2009/02/18	Compal	Add L48, L49, L50, C944, C943, C942 for EMI	0.2
35	18	2009/02/24	Nvidia	Change R321, R320, R319, R318 form 2.2K ohm to 4.7K ohm.	0.2
36	18	2009/02/18	Compal	Reserve D5, D6, D7, D8, D9 for ESD	0.2
37	18	2009/02/12	Nvidia	Del R1066	0.2
38	19	2009/01/22	HP	Add Q71, Q72, R1134 for Keyboard light	0.2

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Version Change List (P. I. R, List) for HW Circuit DB-1>> DB-2

Item	Page #	Date	Request Owner	Solution Description	Rev.
39	19	2009/02/06	Nvidia	Add C914, C915, C916, C917 for eDP.	0.2
40	19	2009/02/06	HP	Change R341 pin 1 power plan form +5VS to +3VALW.	0.2
41	20	2009/02/12	Nvidia	Reserve R1150	0.2
42	20	2009/02/24	HP	Change R355, R356 from 2K ohm to 10K ohm.	0.2
43	20	2009/02/25	HP	Add Q78, R1158, R1157 for thermal trip.	0.2
44	21	2009/01/20	HP	Del LVDS function	0.2
45	21	2009/02/26	Nvidia	Del C346, because no SPDIF.	0.2
46	22	2009/01/20	Nvidia	Add C924 ~ C931 for DP function	0.2
47	22	2009/02/06	Nvidia	Del RP28, 31, 34, 40, 49, 52, 55, 29, 43, 35, 39, 44, 48, 53, 56, 30, 33, 36, 38, 45, 46, 42 for VRAM	0.2
48	22	2009/02/06	Nvidia	Del C904, 899, 900, 901, 902, 903 for VRAM	0.2
49	23	2009/02/23	Nvidia	Add L47, C941 for SP_PLLVDD	0.2
50	26	2009/02/19	HP	Del C505, C509, C507, C508, C905, Q18, R440, R1062, R441	0.2
51	26	2009/02/06	HP	Add C934	0.2
52	27	2009/02/18	HP	ReserveD57 for ESD	0.2
53	28	2009/02/06	HP	Recover Q25, R503, R483	0.2
54	29	2009/02/26	HP	Add R1159 for NAND Flash detect	0.2
55	30	2009/02/24	Compal	Del R529, R528, R535, C618, U22	0.2
56	30	2009/02/24	Compal	Add Q79 ~ Q83, R1163, R1162, R1164, C945, C946, C947, C948	0.2
57	31	2009/02/22	Compal	Del D30, U28, C711, R608	0.2
58	32	2009/02/18	HP	Reserve D33, D34, D36, D68 for ESD	0.2
59	33	2009/02/18	Compal	Reserve D32 for ESD	0.2
60	34	2009/02/06	HP	Add JP32 of pin 179, 178, 11, 10 to +5VS	0.2
61	34	2009/01/22	HP	Del C746 ~ C761	0.2
62	34	2009/02/06	HP	Add Q75, R1145.	0.2
63	34	2009/02/06	HP	Del R647~ R650	0.2
64	35	2009/02/06	HP	Reserve R711	0.2
65	35	2009/02/06	HP	Add R1140	0.2
66	35	2009/02/16	HP	Change R692 from 10K ohm to 220 ohm	0.2
67	35	2009/01/22	HP	Del L4, C269 and add test point.	0.2
68	36	2009/02/18	Compal	change Super IQ from ITE to SMSC	0.2
69	37	2009/02/25	HP	Del R758	0.2
70	37	2009/02/06	HP	Change R941 pin from PM_SLP_LAN# to PM_SLP_M#	0.2
71	37	2009/02/25	HP	change R1044 from 49.9K ohm to 78.7K ohm.	0.2
72	38	2009/02/18	Compal	Add Q77, R1170, C939, R1156, C935 ~ C938	0.2
73					0.2
74					0.2
75					0.2
76					0.2

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Version Change List (P. I. R, List)for HW Circuit DB-3>> SI-1

Item	Page #	Date	Request Owner	Solution Description	Rev.
01	16	2009/04/24	HP	Del R294	0.4
02	13	2009/04/24	HP	Del CLRP2	0.4
03	14	2009/04/24	HP	Del C147, C148 location	0.4
04	14	2009/04/24	HP	Add C961	0.4
05	14	2009/04/24	HP	Add R1188, R1187 for intel spec	0.4
06	27	2009/04/24	HP	Add C962 ~ C965	0.4
07	36	2009/04/24	HP	Add R1190, R1189	0.4
08	29	2009/04/24	HP	Del C574~C577 and C579~C582.	0.4
09	33	2009/04/24	HP	Add R1191, R1192	0.4
10	26	2009/05/02	HP	Add R1198, R1199	0.4
11	04	2009/05/02	HP	Install R1060	0.4
12	35	2009/05/02	HP	Add R1197, C967, C966, C968, R1195, R1196	0.4
13	38	2009/05/02	HP	Add C978, C979	0.4

Version Change List (P. I. R, List)for HW Circuit SI-1>> SI-16

Item	Page #	Date	Request Owner	Solution Description	Rev.
01	04	2009/07/21	HP	Add C997, R1219, Q87, R1218 for CPU S3 power savings issue	0.5
02	04	2009/07/02	HP	Add R1226 for CPU S3 power savings issue	0.5
03	05	2009/07/21	HP	Add Q88, Q89 and reserve R1220, R1222 for CPU S3 power savings issue	0.5
04	07	2009/07/02	HP	Add Q91, R1224, C994, C995, C991, C992, C993, C996, Q92, R1223 for CPU S3 power savings issue	0.5
05	19	2009/06/30	HP	Add R1213, D72 for Lid SW issue	0.5
06	37	2009/07/09	HP	Change C864 from 0.047uF to 0.068uF.	0.5

Version Change List (P. I. R. List) for HW Circuit SI-16>>SI-2

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