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SLC M/B Schematics Document

14": Tabo; 15.6" Pochacco

Intel Ivy Bridge ULV Processor with DDRIII + Panther Point

Date : 2013/11/13
Version 0.1

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title: Block Diagrams
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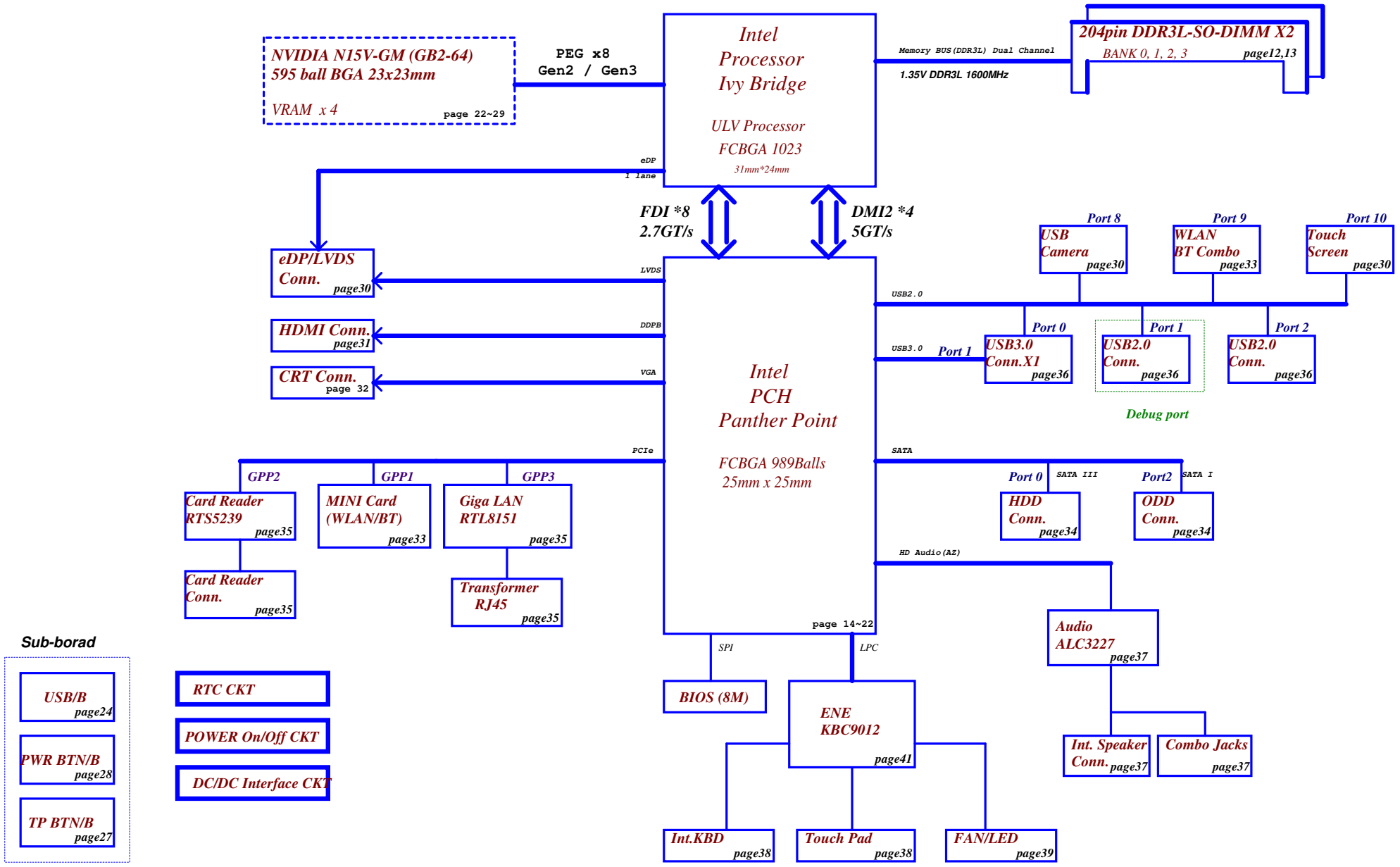

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Compal Electronics, Inc.

Title: Block Diagrams

Size: Custom | Document Number: LA-A999P | Rev: 0.1

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ZSO40/50 (LA-A998P/LA-A999 Ver:0.1)

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
		ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.675VS	+0.675VP to +0.675VS switched power rail for DDR3L terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.35V	+1.35V_VDDQP to +1.35V power rail for DDR3L	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+3VALW) to 1.8V LDO power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VL to KBC	ON	ON	ON*
+LAN_VDD_3V3	+3VALW to +LAN_VDD_3V3 power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S1	S3	S5
+3VGS	GPU power	PX	OFF	OFF
+VGA_CORE	GPU power	PX	OFF	OFF
+1.05VGS	GPU power	PX	OFF	OFF
+1.5VGS	GPU power	PX	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	
G-sensor	0x50/0x52
Charger IC BQ24738	0xFFH

EC SM Bus2 address

Device	Address
PCH SML1	
N15V-GE dGPU	

PCH SM Bus address

Device	Address
DDR DIMM0	
DDR DIMM1	

SMBUS Control Table

	SOURCE	BATT	WLAN MIINI1	BATT Charger	TP	SODIMM	EC_SMB_CK2 EC_SMB_DA2	PCH_SML1CLK PCH_SML1DATA	G-Sensor	dGPU	
EC_SMB_CK1 EC_SMB_DA1	KB9012	V		V					V		
EC_SMB_CK2 EC_SMB_DA2	KB9012							V		V	
PCH_SMBCLK PCH_SMBDATA	PCH					V					
PCH_SML0CLK PCH_SML0DATA	PCH										
PCH_SML1CLK PCH_SML1DATA	PCH						V				

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC/TPM
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	JHDD1
SATA1	None
SATA2	JODD1
SATA3	None
SATA4	None
SATA5	None

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB2.0 (For USB3.0 Conn.)
		1	USB2.0 (D/B)
	UHCI1	2	USB2.0 (D/B)
		3	None
	UHCI2	4	None
		5	None
	UHCI3	6	None
		7	None
EHCI2	UHCI4	8	Camera
		9	Mini Card(WLAN& BT)
	UHCI5	10	Touch Screen
		11	None
	UHCI6	12	None
		13	None

USB 3.0	Port	2 External USB Port
	1	USB3.0 (left Side)
	2	None
	3	None
	4	None

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	mini WLAN	CLKOUTFLEX0	None
			CLKOUTFLEX1	None
	CLKOUT_PCIE1	CARD READER	CLKOUTFLEX2	None
	CLKOUT_PCIE2	PCIE LAN	CLKOUTFLEX3	DGPU_PRSNT#
	CLKOUT_PCIE3	None		
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

BY SKU		
TPM	9635@	9656@
CPU	CPUUMA1@ CPUUMA2@ CPUDIS@	
VRAM	X76@	SAM@
	MIC@	HY@

Symbol Note :

: means Digital Ground

: means Analog Ground

Option	@	CONN@	SP@	PX@	UMA@	DIS@	
UMA	X	X	V	X	V	X	
DIS	X	X	V	V	X	V	

Project ID	UMA@	DIS@		

PCB	LA-A998P	LA-A999P
	14@	15@

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Size	Document Number	Rev
C	LA-A999P	0.1

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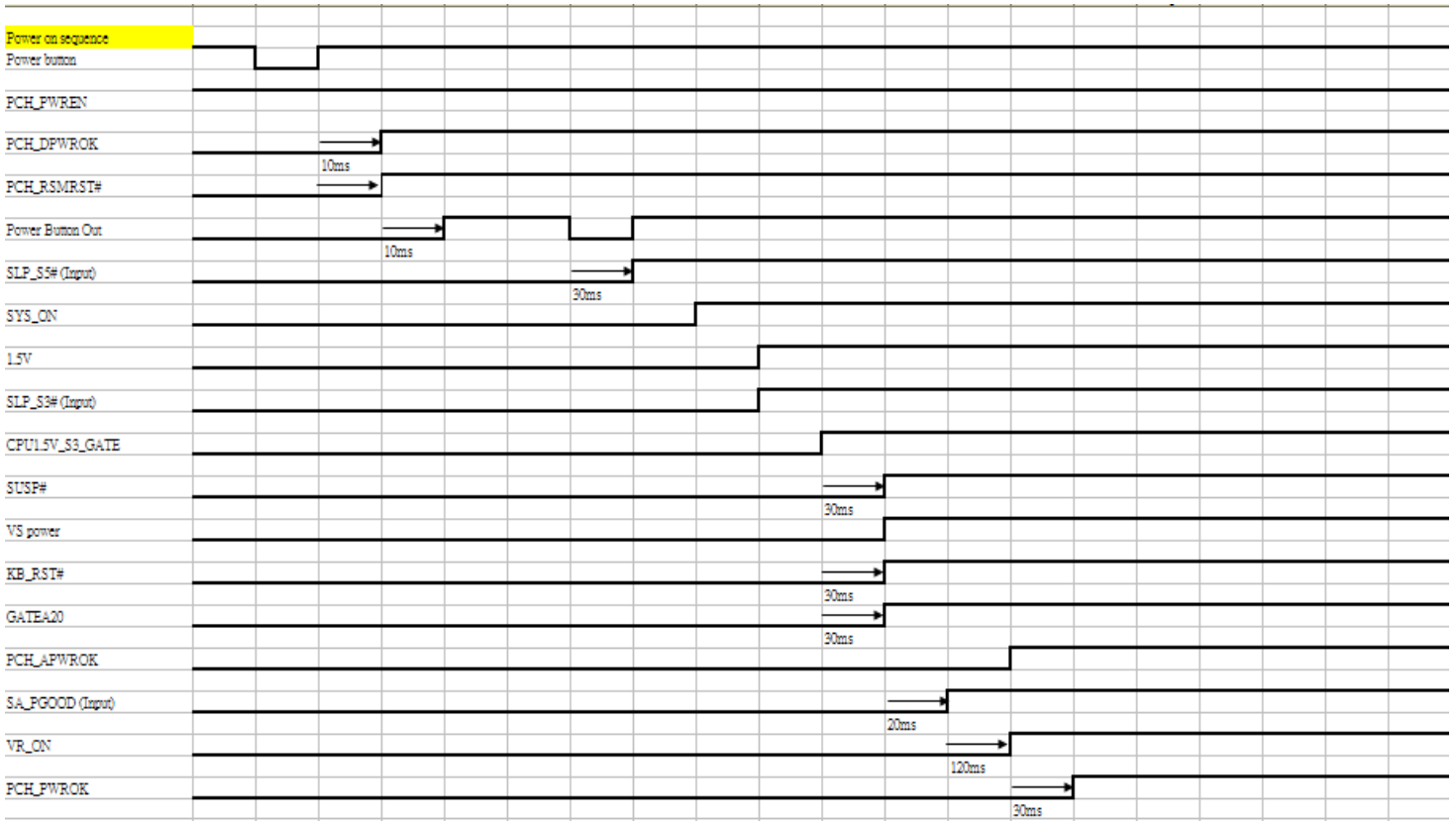

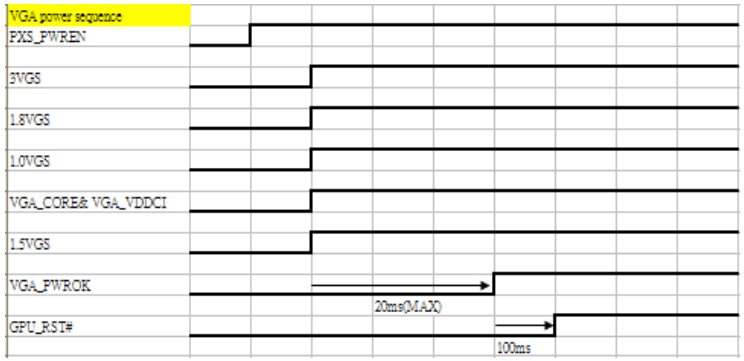

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Title: ***PROCESSOR(1/7) DMI,FDI,PEG***

Size	Document Number	Rev
B		0.1

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UCPU1 CPUDIS01@
i5-2467M CPU
SA00004X000

UCPU1 CPUDIS02@
i5-2367M CPU
SA000051H20

UCPU1 CPUDIS03@
i5-2367M CPU
SA000051H20

UCPU1 CPUDIS04@
i5-3317U CPU
SA00005K600

UCPU1 CPUUMA3@
i5-2367M CPU
SA000051H20

UCPU1 CPUUMA1@
17W 1.5GHz GT2 ES2 QBP8
SA00005AZ10

UCPU1 CPUUMA4@
17W 1.7GHz GT2 ES2 QBP7
SA00005B010

UCPU1 CPUUMA2@
17W 1.5GHz no cnfg ES2 QBTP
SA00005AZ20

UCPU1 CPUUMA5@
17W 1.7GHz no cnfg ES2 QBTQ
SA00005B020

Sandy Bridge:
Intel Core i5-2467M: SA00004X000 (4619HY32L01)

Ivy Bridge:
1.5GHz GT2 ES2 QBP8: SA00005AZ10 (4619HZ32L01)
1.5GHz ES2 QBTP: SA00005AZ20(4619HZ32L02)

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

+VCCP
RC1 24.9_0402_1%
131204 Del CU65 by EMI requested

UCPU1A @

PEG_ICOMPI G3 — PEG_COMP
PEG_ICOMPO G1
PEG_RCOMPO G4

DMI
<16> DMI_CRX_PTX_N0 M2 DMI_RX#[0]
<16> DMI_CRX_PTX_N1 P6 DMI_RX#[1]
<16> DMI_CRX_PTX_N2 P1 DMI_RX#[2]
<16> DMI_CRX_PTX_N3 P10 DMI_RX#[3]
<16> DMI_CRX_PTX_P0 N3 DMI_RX[0]
<16> DMI_CRX_PTX_P1 P7 DMI_RX[1]
<16> DMI_CRX_PTX_P2 P3 DMI_RX[2]
<16> DMI_CRX_PTX_P3 P11 DMI_RX[3]
<16> DMI_CTX_PRX_N0 K1 DMI_TX#[0]
<16> DMI_CTX_PRX_N1 M8 DMI_TX#[1]
<16> DMI_CTX_PRX_N2 N4 DMI_TX#[2]
<16> DMI_CTX_PRX_N3 R2 DMI_TX#[3]
<16> DMI_CTX_PRX_P0 K3 DMI_TX[0]
<16> DMI_CTX_PRX_P1 M7 DMI_TX[1]
<16> DMI_CTX_PRX_P2 P4 DMI_TX[2]
<16> DMI_CTX_PRX_P3 T3 DMI_TX[3]

Intel(R) FDI
<16> FDI_CTX_PRX_N0 U7 FDI0_TX#[0]
<16> FDI_CTX_PRX_N1 W11 FDI0_TX#[1]
<16> FDI_CTX_PRX_N2 W1 FDI0_TX#[2]
<16> FDI_CTX_PRX_N3 AA6 FDI0_TX#[3]
<16> FDI_CTX_PRX_N4 W6 FDI1_TX#[0]
<16> FDI_CTX_PRX_N5 V4 FDI1_TX#[1]
<16> FDI_CTX_PRX_N6 Y2 FDI1_TX#[2]
<16> FDI_CTX_PRX_N7 AC9 FDI1_TX#[3]
<16> FDI_CTX_PRX_P0 U6 FDI0_TX[0]
<16> FDI_CTX_PRX_P1 W10 FDI0_TX[1]
<16> FDI_CTX_PRX_P2 W3 FDI0_TX[2]
<16> FDI_CTX_PRX_P3 AA7 FDI0_TX[3]
<16> FDI_CTX_PRX_P4 W7 FDI1_TX[0]
<16> FDI_CTX_PRX_P5 T4 FDI1_TX[1]
<16> FDI_CTX_PRX_P6 AA3 FDI1_TX[2]
<16> FDI_CTX_PRX_P7 AC8 FDI1_TX[3]
<16> FDI_FSYNC0 AA11 FDI0_FSYNC
<16> FDI_FSYNC1 AC12 FDI1_FSYNC
<16> FDI_INT U11 FDI_INT
<16> FDI_LSYNC0 AA10 FDI0_LSYNC
<16> FDI_LSYNC1 AG8 FDI1_LSYNC

eDP
EDP_COMP AF3 eDP_COMPIO
AD2 eDP_ICOMPO
EDP_HPD# AG11 eDP_HPD#
<30> EDP_HPD#
<30> EDP_CPU_AUX#_C AG4 eDP_AUX#
<30> EDP_CPU_AUX_C AF4 eDP_AUX
<30> EDP_CPU_LANE_N0_C AC3 eDP_TX#[0]
AC4 eDP_TX#[1]
AE11 eDP_TX#[2]
AE7 eDP_TX#[3]
<30> EDP_CPU_LANE_P0_C AC1 eDP_TX[0]
AA4 eDP_TX[1]
AE10 eDP_TX[2]
AE6 eDP_TX[3]

PCI EXPRESS - GRAPHICS

PEG_RX#[0] H22
PEG_RX#[1] J21
PEG_RX#[2] B22
PEG_RX#[3] D21
PEG_RX#[4] A19
PEG_RX#[5] D17
PEG_RX#[6] B14
PEG_RX#[7] D13
PEG_RX#[8] A11 PEG_GTX_C_HRX_N7
PEG_RX#[9] B10 PEG_GTX_C_HRX_N6
PEG_RX#[10] G8 PEG_GTX_C_HRX_N5
PEG_RX#[11] A8 PEG_GTX_C_HRX_N4
PEG_RX#[12] B6 PEG_GTX_C_HRX_N3
PEG_RX#[13] H8 PEG_GTX_C_HRX_N2
PEG_RX#[14] E5 PEG_GTX_C_HRX_N1
PEG_RX#[15] K7 PEG_GTX_C_HRX_N0

<PEG>

PEG_GTX_C_HRX_N[0..7] — PEG_GTX_C_HRX_N[0..7] <22>
PEG_GTX_C_HRX_P[0..7] — PEG_GTX_C_HRX_P[0..7] <22>
PEG_HTX_C_GRX_N[0..7] — PEG_HTX_C_GRX_N[0..7] <22>
PEG_HTX_C_GRX_P[0..7] — PEG_HTX_C_GRX_P[0..7] <22>

PEG_RX[0] K22
PEG_RX[1] K19
PEG_RX[2] C21
PEG_RX[3] D19
PEG_RX[4] C19
PEG_RX[5] D16
PEG_RX[6] C13
PEG_RX[7] D12
PEG_RX[8] C11 PEG_GTX_C_HRX_P7
PEG_RX[9] C9 PEG_GTX_C_HRX_P6
PEG_RX[10] F8 PEG_GTX_C_HRX_P5
PEG_RX[11] C8 PEG_GTX_C_HRX_P4
PEG_RX[12] C5 PEG_GTX_C_HRX_P3
PEG_RX[13] H6 PEG_GTX_C_HRX_P2
PEG_RX[14] F6 PEG_GTX_C_HRX_P1
PEG_RX[15] K6 PEG_GTX_C_HRX_P0

PEG_TX#[0] G22
PEG_TX#[1] C23
PEG_TX#[2] D23
PEG_TX#[3] F21
PEG_TX#[4] H19
PEG_TX#[5] C17
PEG_TX#[6] K15
PEG_TX#[7] F17
PEG_TX#[8] F14 PEG_HTX_GRX_N7 CU41 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N7
PEG_TX#[9] A15 PEG_HTX_GRX_N6 CU42 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N6
PEG_TX#[10] J14 PEG_HTX_GRX_N5 CU43 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N5
PEG_TX#[11] H13 PEG_HTX_GRX_N4 CU44 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N4
PEG_TX#[12] M10 PEG_HTX_GRX_N3 CU45 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N3
PEG_TX#[13] F10 PEG_HTX_GRX_N2 CU46 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N2
PEG_TX#[14] D9 PEG_HTX_GRX_N1 CU47 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N1
PEG_TX#[15] J4 PEG_HTX_GRX_N0 CU48 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N0

<PEG>

PEG_TX[0] F22
PEG_TX[1] A23
PEG_TX[2] D24
PEG_TX[3] E21
PEG_TX[4] G19
PEG_TX[5] B18
PEG_TX[6] K17
PEG_TX[7] G17
PEG_TX[8] E14 PEG_HTX_GRX_P7 CU57 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P7
PEG_TX[9] C15 PEG_HTX_GRX_P6 CU58 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P6
PEG_TX[10] K13 PEG_HTX_GRX_P5 CU59 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P5
PEG_TX[11] G13 PEG_HTX_GRX_P4 CU60 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P4
PEG_TX[12] K10 PEG_HTX_GRX_P3 CU61 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P3
PEG_TX[13] G10 PEG_HTX_GRX_P2 CU62 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P2
PEG_TX[14] D8 PEG_HTX_GRX_P1 CU63 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P1
PEG_TX[15] K4 PEG_HTX_GRX_P0 CU64 DIS@ 1 2 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P0

IVY-BRIDGE_BGA1023

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

NOTE:eDP_COMPIO and eDP_ICOMPO should not be left floating even if Internal Graphic is disabled since they are shared with other interfaces

+VCCP
eDP@ RC88 1K_0402_5%
RC2 24.9_0402_1%

<1111> Co-lay eDP function.

10/05 Change to 0.22uF.

Typ- suggest 220nF. The change in AC capacitor value from 180nF to 265nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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Buffered reset to CPU

Reset# signal is driven by the PCH to multiple agents on the platform. PCH Reset# output DC levels are 0-V and 3.3 V, processor Reset input DC levels are 0V and 1.0 V. Processor high-voltage level is lower than PCH high voltage level, therefore a voltage level shifter is required on the Reset# signal. In order for Reset# to meet the signal quality requirement at the input to the processor OD buffer must be placed on the motherboard between the PCH and the processor.

+3VS, CC1 0.1U_0402_16V4Z, +VCCP, RC3 75_0402_5%, UC1 SN74LVC1G07DCKR_SC70-5, RC4 43_0402_1%, RC6 @ 750_0402_1%, R375 @ 0_0402_5%

<17,22,33,35,40,41> PLT_RST# → PLT_RST# → BUFO_CPU_RST# → BUF_CPU_RST#

Requires a series resistor of 43±5% between processor and PCH. It also a needs an Rtt of 75±5% to VCCP after the OD buffer and before the series resistor.

+3VS, XDP_DBRESET#, RC5 1K_0201_5%

SI2 change to 0201
12.19

Processor Pullups

+VCCP, RC8 62_0402_5% PROCHOT#

RC11 10K_0201_5% H_CPUPWRGD_R

SI2 change to 0201
12.19

UCPU1B @ — IVY-BRIDGE_BGA1023

This pin is for compability with future platforms. A pull up resistor to VCCIO is required if connected to the DF_TVS strap on the PCH.

PROC_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present

<18> H_SNB_IVB# → F49 PROC_SELECT#

@RC7 10K_0201_5% → C57 PROC_DETECT#

SI2 change to 0201
12.19

PAD T5 @ → C49 CATERR#

<18,41> H_PECI → A48 PECI

<41,46> PROCHOT# → RC10 56_0402_5% → C45 PROCHOT#

C295 10P_0402_50V8J @ESD@ Near CPU

<18> H_THRMTRIP# → RC12 0_0402_5% short@ → D45 THERMTRIP#

<16> H_PM_SYNC → RC13 short@ 0_0201_5% → C48 PM_SYNC

<18> H_CPUPWRGD → RC16 short@ 0_0201_5% → B46 UNCOREPWRGOOD

UNCOREPWRGOOD:非CORE外的電OK

PM_SYS_PWRGD_BUF → RC18 130_0402_5% → BE45 SM_DRAMPWROK

SM_DRAMPWROK:DRAM power ok

BUF_CPU_RST# → D44 RESET#

CLOCKS: BCLK/BCLK# → J3/H2 CLK_CPU_DMI/CLK_CPU_DMI# <15> <15> 100MHz

DPLL_REF_CLK/DPLL_REF_CLK# → AG3/AG1 CLK_EDP/CLK_EDP# RC85/RC84 eDP@/eDP@ 0_0402_5% → CLK_R_EDP/CLK_R_EDP# <15> <15>

131224
If motherboard only supports external graphics or if it supports integrated graphic but without eDP:
Connect DPLL_REF_SSCLK on Processor to GND through 1K ± 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K ± 5% resistor

DDR3 MISC: SM_DRAMRST# → AT30 H_DRAMRST# → H_DRAMRST# <7>

SM_RCOMP[0] → BF44 SM_RCOMP0
SM_RCOMP[1] → BE43 SM_RCOMP1
SM_RCOMP[2] → BG43 SM_RCOMP2

CC104 0.1U_0402_16V7K @ESD@ Near CPU

JTAG & BPM: PRDY# → N53 PAD T35; PREQ# → N55 PAD T39

TCK → L56 XDP_TCK
TMS → L55 XDP_TMS
TRST# → J58 XDP_TRST#
TDI → M60 XDP_TDI
TDO → L59 XDP_TDO

DBR# → K58 XDP_DBRESET#_R → RC17 short@ 0_0201_5% → XDP_DBRESET# <16>

12/16:Change to 0201 for SI2

BPM#[0] → G58 XDP_BPM#0_R → T60 @PAD
BPM#[1] → E56 XDP_BPM#1_R → T61 @PAD
BPM#[2] → E59 XDP_BPM#2_R → T62 @PAD
BPM#[3] → G55 XDP_BPM#3_R → T63 @PAD
BPM#[4] → G59 XDP_BPM#4_R
BPM#[5] → H60 XDP_BPM#5_R
BPM#[6] → J59 XDP_BPM#6_R
BPM#[7] → J61 XDP_BPM#7_R

2011.10.18 delete all reserved XDP conponent.
Just reserve test point for XDP.

+3VS, RC81 10K_0402_5%, +3V_PCH, CC2 0.1U_0402_16V4Z, UC2 74AHC1G09GW_TSSOP5, +1.5V_CPU_VDDQ, RC25 200_0402_5%

<16> SYS_PWROK → @RC27 0_0402_5%
<16> PM_DRAM_PWRGD → RC28 200_0402_5%
PM_SYS_PWRGD_BUF → RC29 39_0402_5%

Part Number = SA00003Y000

<43> SUSP → QC1 2N7002_SOT23

11.06 Change to +3V_PCH

DDR3 Compensation Signals

SM_RCOMP0 RC23 140_0402_1%
SM_RCOMP1 RC24 25.5_0402_1%
SM_RCOMP2 RC26 200_0402_1%

PU/PD for JTAG signals

XDP_TMS → T40 @PAD
XDP_TDI → T41 @PAD
XDP_TDO → T42 @PAD
XDP_TCK → T43 @PAD
XDP_TRST# → T46 @PAD

SI2 change to 0201
12.19

C263 0.1U_0201_16V4Z
XDP_TRST#
C264 220P_0402_50V7K
PLT_RST#
C265 @ 100P_0402_50V8J
PM_SYS_PWRGD_BUF
C266 220P_0402_50V7K
BUF_CPU_RST#

XDP_DBRESET#_R → CC4 0.1U_0201_16V4Z
H_CPUPWRGD_R → C118 220P_0402_50V7K

SI2 change to 0201
12.19

6/27 Add ESD solution

2011.10.18 delete all reserved XDP conponent.
Just reserve test point for XDP.

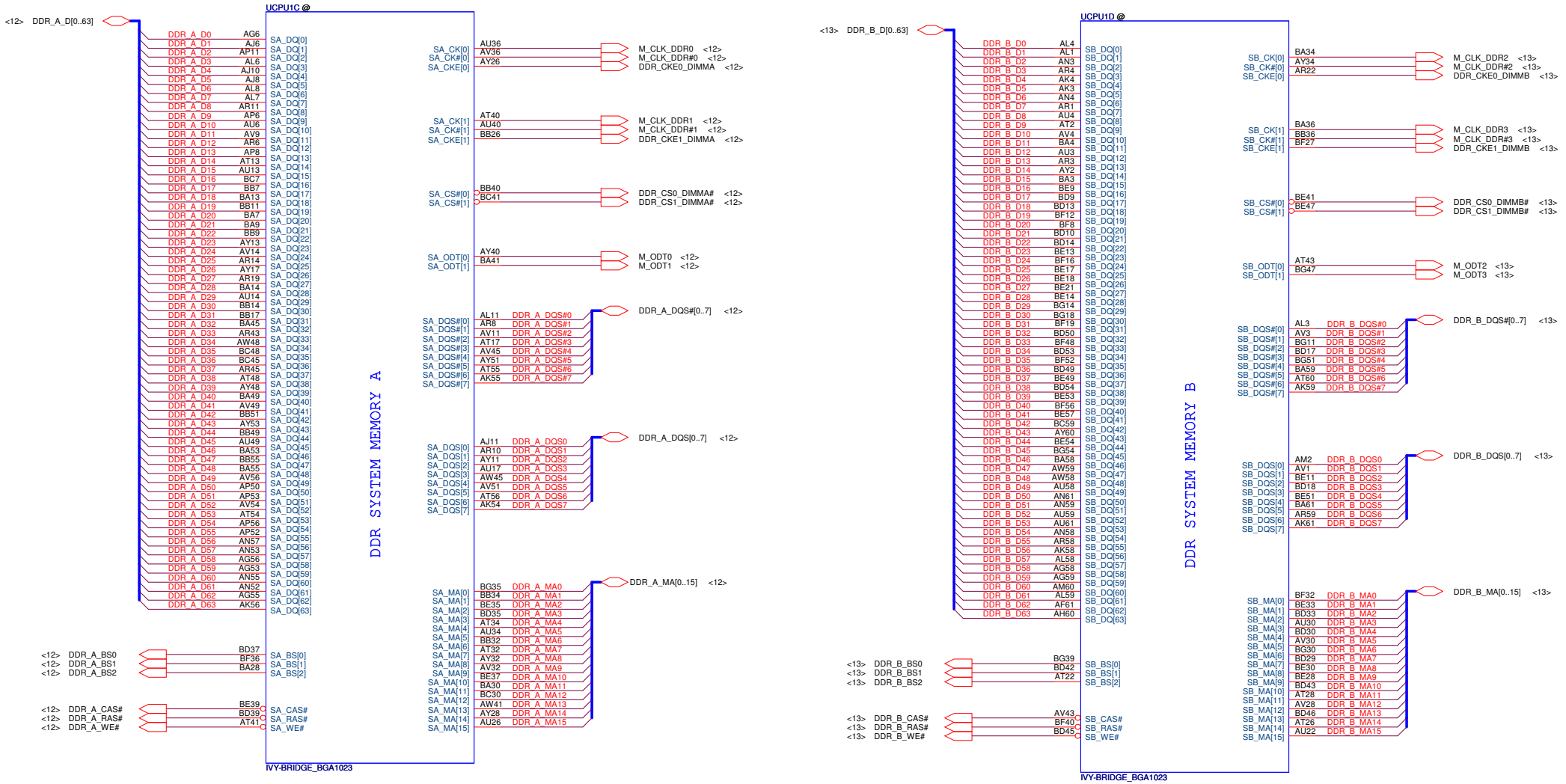
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

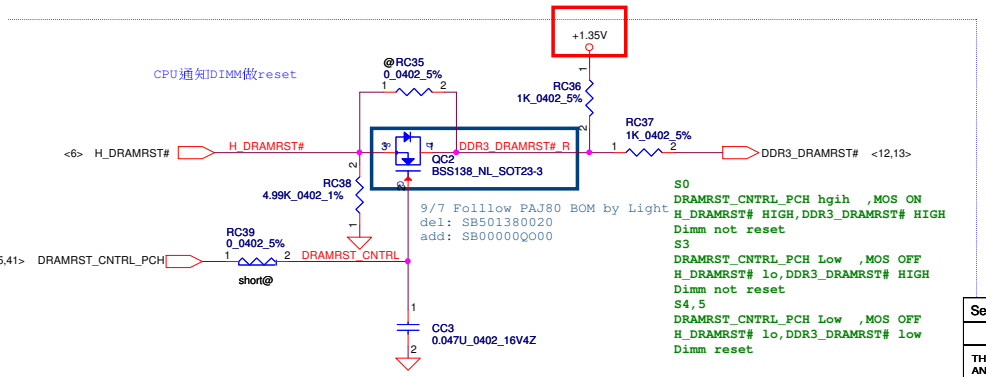
Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size	Document Number	Rev
C	LA-8041P	0.1

Date: Friday, March 14, 2014 Sheet 6 of 58





Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	LA-8041P	0.1

Date: Friday, March 14, 2014 Sheet 7 of 58

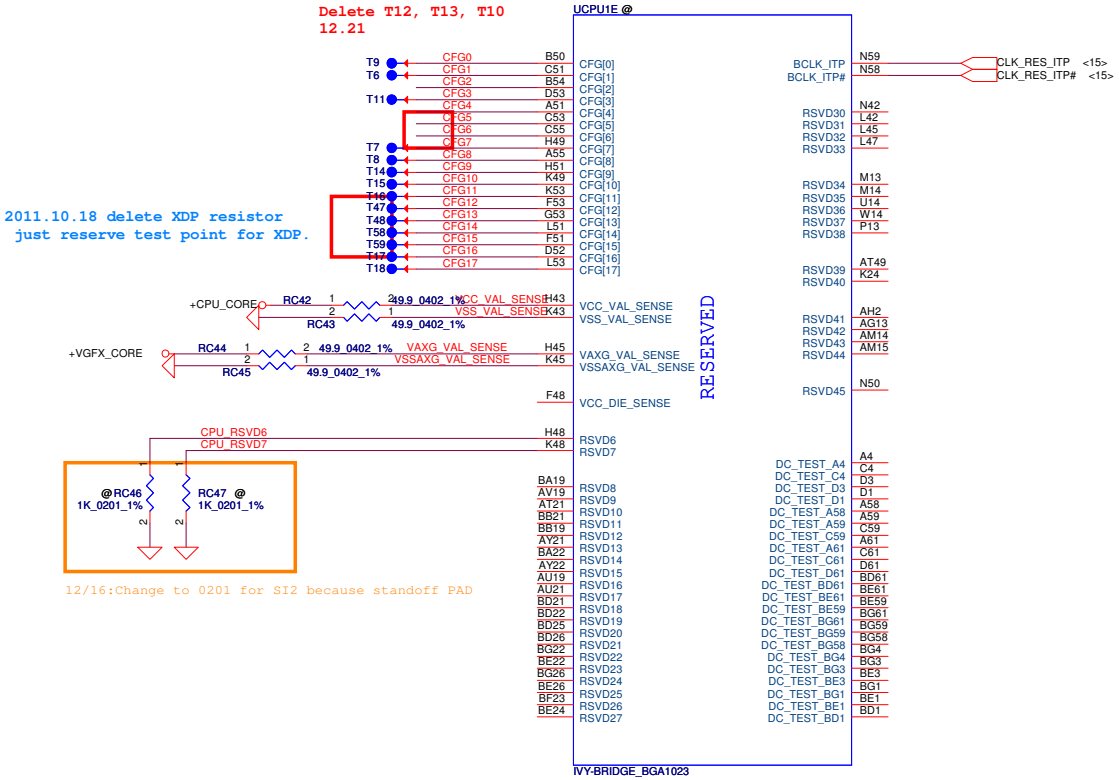
CFG Straps for Processor

PEG bus is reversed, need to PD.
11.01

Change to part G.

Delete T12, T13, T10
12.21

2011.10.18 delete XDP resistor
just reserve test point for XDP.



12/16:Change to 0201 for SI2 because standoff PAD

CFG2

RC40 1K_0201_1%

RC40 SI2 change to 0201
12.19

PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

CFG4

RC41 eDP@ 1K_0201_1%

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG6
CFG5

RC48 1K_0201_1%
RC49 1K_0201_1%

RC48, RC49 SI2 change to 0201
12.19

Change CFG[6:5] to 00= 1x8, 2x4 PCIe
because AMD driver can't install issue
11.21

PCIE Port Bifurcation Straps	
CFG[6:5]	* 00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express

12/16:Change to 0201 for SI2 because standoff PAD

CFG7

RC50 @ 1K_0201_1%

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

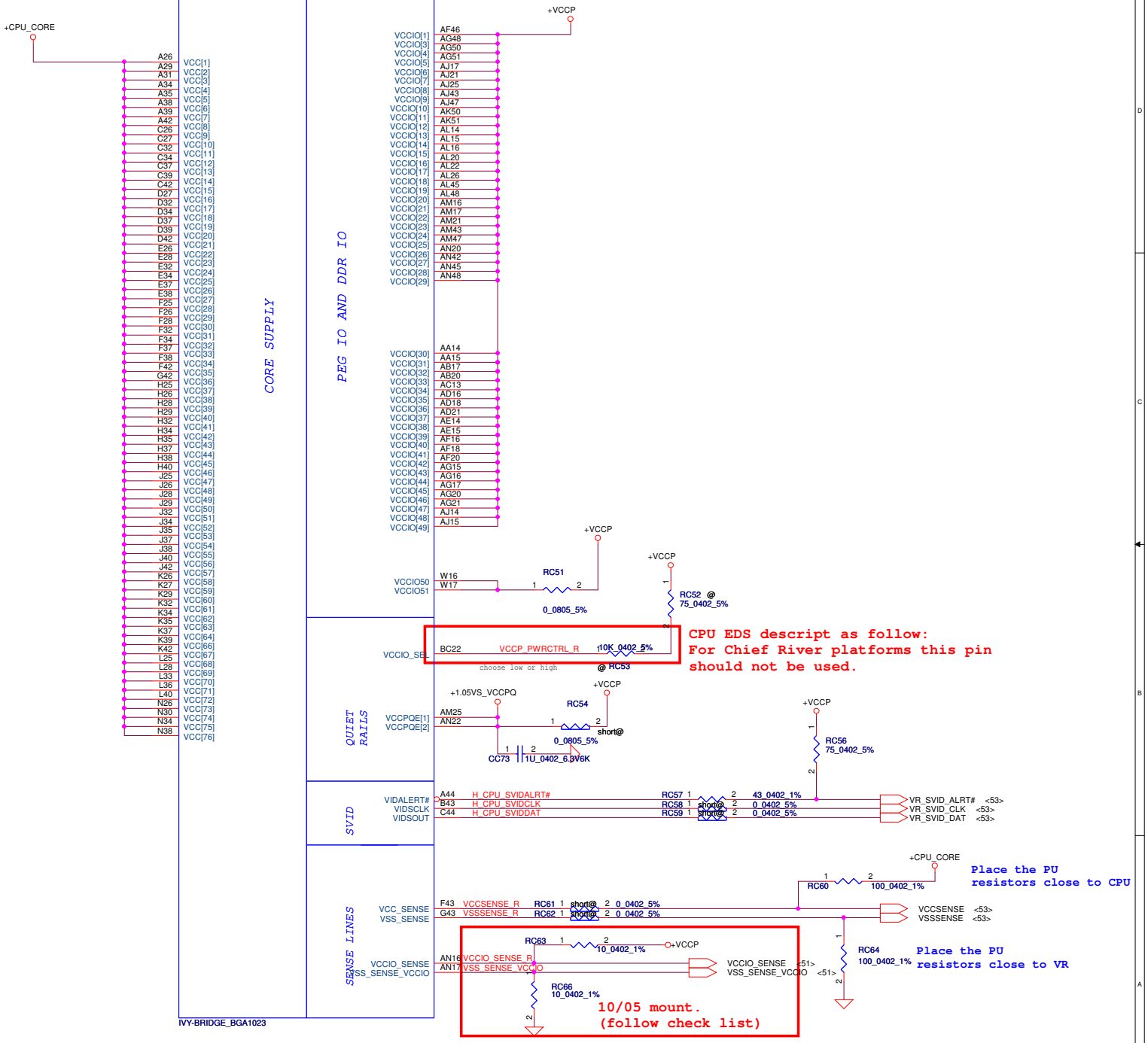
Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: LA-8661P | Rev: 0.1

Date: Friday, March 14, 2014 | Sheet 8 of 58

POWER



CPU EDS descript as follow:
For Chief River platforms this pin should not be used.

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.			
Title: PROCESSOR(5/7) PWR,BYPASS			
Size: Custom	Document Number: LA-8661P		Rev: 0.1
Date: Friday, March 14, 2014	Sheet 9 of 58		

POWER

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

+1.5V_CPU_VDDQ
+1.35V
CC74 2 1 0.1U_0402_10V7K
CC75 2 1 0.1U_0402_10V7K

+VGFX_CORE

UCPU1G

GRAPHICS: AA46 AB47 AB50 AB51 AB52 AB53 AB55 AB56 AB58 AB59 AC61 AD47 AD48 AD50 AD51 AD52 AD53 AD55 AD56 AD58 AD59 AE46 N45 P47 P48 P50 P51 P52 P53 P55 P56 P61 T48 T58 T59 T61 U46 V47 V48 V50 V51 V52 V53 V55 V56 V58 V59 W50 W51 W52 W53 W55 W56 W61 Y48 Y61
VAXG[1] VAXG[2] VAXG[3] VAXG[4] VAXG[5] VAXG[6] VAXG[7] VAXG[8] VAXG[9] VAXG[10] VAXG[11] VAXG[12] VAXG[13] VAXG[14] VAXG[15] VAXG[16] VAXG[17] VAXG[18] VAXG[19] VAXG[20] VAXG[21] VAXG[22] VAXG[23] VAXG[24] VAXG[25] VAXG[26] VAXG[27] VAXG[28] VAXG[29] VAXG[30] VAXG[31] VAXG[32] VAXG[33] VAXG[34] VAXG[35] VAXG[36] VAXG[37] VAXG[38] VAXG[39] VAXG[40] VAXG[41] VAXG[42] VAXG[43] VAXG[44] VAXG[45] VAXG[46] VAXG[47] VAXG[48] VAXG[49] VAXG[50] VAXG[51] VAXG[52] VAXG[53] VAXG[54] VAXG[55] VAXG[56]

VREF: SM_VREF, SA_DIMM_VREFDQ, SB_DIMM_VREFDQ
AY43 +V_SM_VREF_CNT
BE7 +V_DDR_REFA_R
BG7 +V_DDR_REFB_R

+V_SM_VREF should have 20 mil trace width

RC67 0_0402_5% short@
RC68 1K_0402_1%
RC69 1K_0402_1%
@QC3 AP2302GN-HF_SOT23-3
CC79 0.1U_0402_16V4Z
RUN_ON_CPU1.5VS3
+V_SM_VREF

DDR3 - 1.5V RAILS

VDDQ[1] AJ28
VDDQ[2] AJ33
VDDQ[3] AJ36
VDDQ[4] AJ40
VDDQ[5] AL30
VDDQ[6] AL34
VDDQ[7] AL38
VDDQ[8] AL42
VDDQ[9] AM33
VDDQ[10] AM36
VDDQ[11] AM40
VDDQ[12] AN30
VDDQ[13] AN34
VDDQ[14] AN38
VDDQ[15] AR26
VDDQ[16] AR28
VDDQ[17] AR30
VDDQ[18] AR32
VDDQ[19] AR34
VDDQ[20] AR36
VDDQ[21] AR40
VDDQ[22] AV41
VDDQ[23] AW26
VDDQ[24] BA40
VDDQ[25] BB28
VDDQ[26] BG33

5A

Check with Power Team
CC100 (330UF) can be taken off.
10.31

+1.5V_CPU_VDDQ
CC85 CC86 CC87 CC88 CC89 CC90 CC91 CC92 1U_0402_6.3V6K
CC93 CC94 CC95 CC96 CC97 CC98 CC99 10U_0603_6.3V6M

QC7 SB00000S700 BSS138W-7-F_SOT323-3
DRAMRST_CNTRL_PCH
DRAMRST_CNTRL_PCH <15,41,47>
+V_DDR_REFA
RC15 @ 0_0402_5%
+V_DDR_REFA_R
RC14 @ 1K_0402_1%
QC8 SB00000S700 BSS138W-7-F_SOT323-3
DRAMRST_CNTRL_PCH
+V_DDR_REFB
RC82 @ 0_0402_5%
+V_DDR_REFB_R
RC83 @ 1K_0402_1%

For Chief River only

M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

10/03 add +V_DDR_REFB

QC4 Change to SA0000JA00 for small package 1016

+1.5V_CPU_VDDQ Source

B+
+1.35V
QC4 AON6718L_DFN8-5
+1.5V_CPU_VDDQ
RC70 100K_0402_5%
RC71 470_0603_5%
R78 @ 20K_0402_5%
RUN_ON_CPU1.5VS3
+3VALW
RC72 100K_0402_5%
RC74 0_0402_5%
CPU1.5V_S3_GATE_R
RUN_ON_CPU1.5VS3# 5
2N7002DWH_SOT363-6 QC5B
RC73 330K_0402_5%
CC118 0.1U_0402_25V6
Q10A 2N7002DWH_SOT363-6
RUN_ON_CPU1.5VS3#
<41> CPU1.5V_S3_GATE
@RC75 0_0402_5%
<41,43,50,51,52,55,58> SUSP#
2N7002DWH_SOT363-6 QC5A

SI# BOM Change CC118 0.1u 25V form 0.1u 16V

131203 del RC76

Follow DG 0.71 page 6

QUIET RAILS: VCCDQ[1] AM28, VCCDQ[2] AN26
1U_0402_6.3V6K CC119

SENSE LINES: VAXG_SENSE F45, VSSAXG_SENSE G45
<53> VCC_AXG_SENSE
<53> VSS_AXG_SENSE
+VGFX_CORE
RC86 100_0402_1%
RC87 100_0402_1%
<1119>check list.

1.8V RAIL: VCCPLL[1] BB3, VCCPLL[2] BC1, VCCPLL[3] BC4
+1.8VS
RC77 0_0805_5% short@
+1.8VS_VCCPLL
CC26 CC121 CC122 10U_0603_6.3V6M 1U_0402_6.3V6K

SENSE LINES: VDDQ_SENSE BC43, VSS_SENSE_VDDQ BA43

SA RAIL: VCCSA[1] L17, VCCSA[2] L21, VCCSA[3] N16, VCCSA[4] N20, VCCSA[5] N22, VCCSA[6] P17, VCCSA[7] P20, VCCSA[8] R16, VCCSA[9] R18, VCCSA[10] R21, VCCSA[11] U15, VCCSA[12] V16, VCCSA[13] V17, VCCSA[14] V18, VCCSA[15] V21, VCCSA[16] W20
+VCCSA
CC20 CC21 CC22 CC23 CC24 10U_0603_6.3V6M
CC129 CC130 CC131 CC132 CC133 1U_0402_6.3V6K

SENSE LINES: VCCSA_SENSE U10
U10 VCCSA_SENSE
@RC78 0_0402_5%
VCCSA_SENSE <52>

VCCSA VID lines: VCCSA_VID[0] D48, VCCSA_VID[1] D49
VCCSA_VID0 VCCSA_VID0 <52>
VCCSA_VID1 VCCSA_VID1 <52>

VID[0]	VID[1]		2011	2012
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

+1.35V
+1.5V_CPU_VDDQ
QC9 @
CPU1.5V_S3_GATE_R3
VIN1 VIN1 VOUT1 VOUT1 ON1 CT1 VBIAS GND ON2 CT2 VIN2 VIN2 VOUT2 VOUT2 GPAD
CC136 @ 100P_0402_50V8J
TPS22966DPUR_SON14_2X3-0

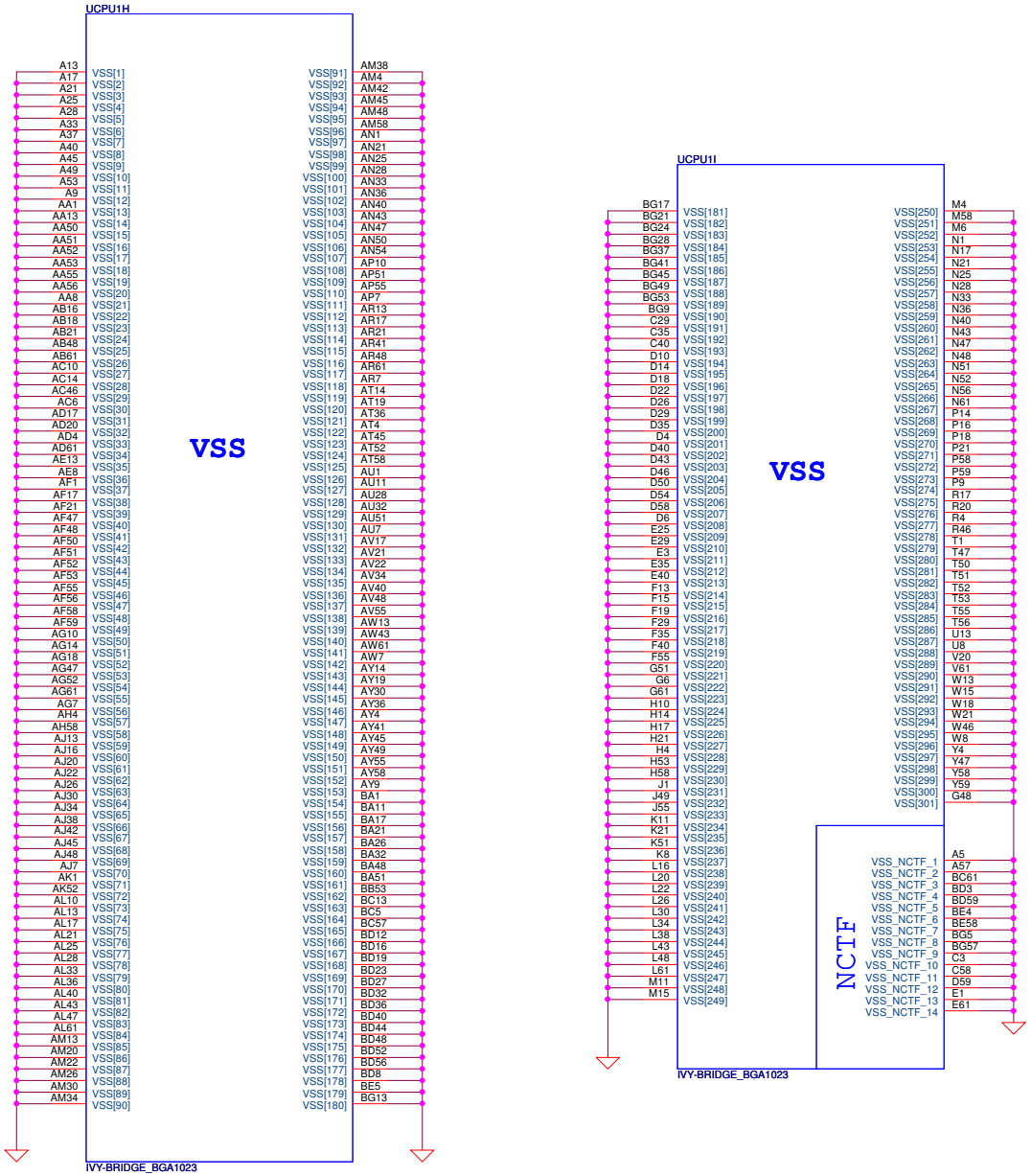
<1111>Reserve low power switch for +1.5V_CPU_VDDQ.

Delete CC25 330U cap 10.19
(after check with power)

IVY-BRIDGE_BGA1023

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.
Title: PROCESSOR(6/7) PWR
Size: Custom | Document Number: LA-8661P | Rev: 0.1
Date: Friday, March 14, 2014 | Sheet 10 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

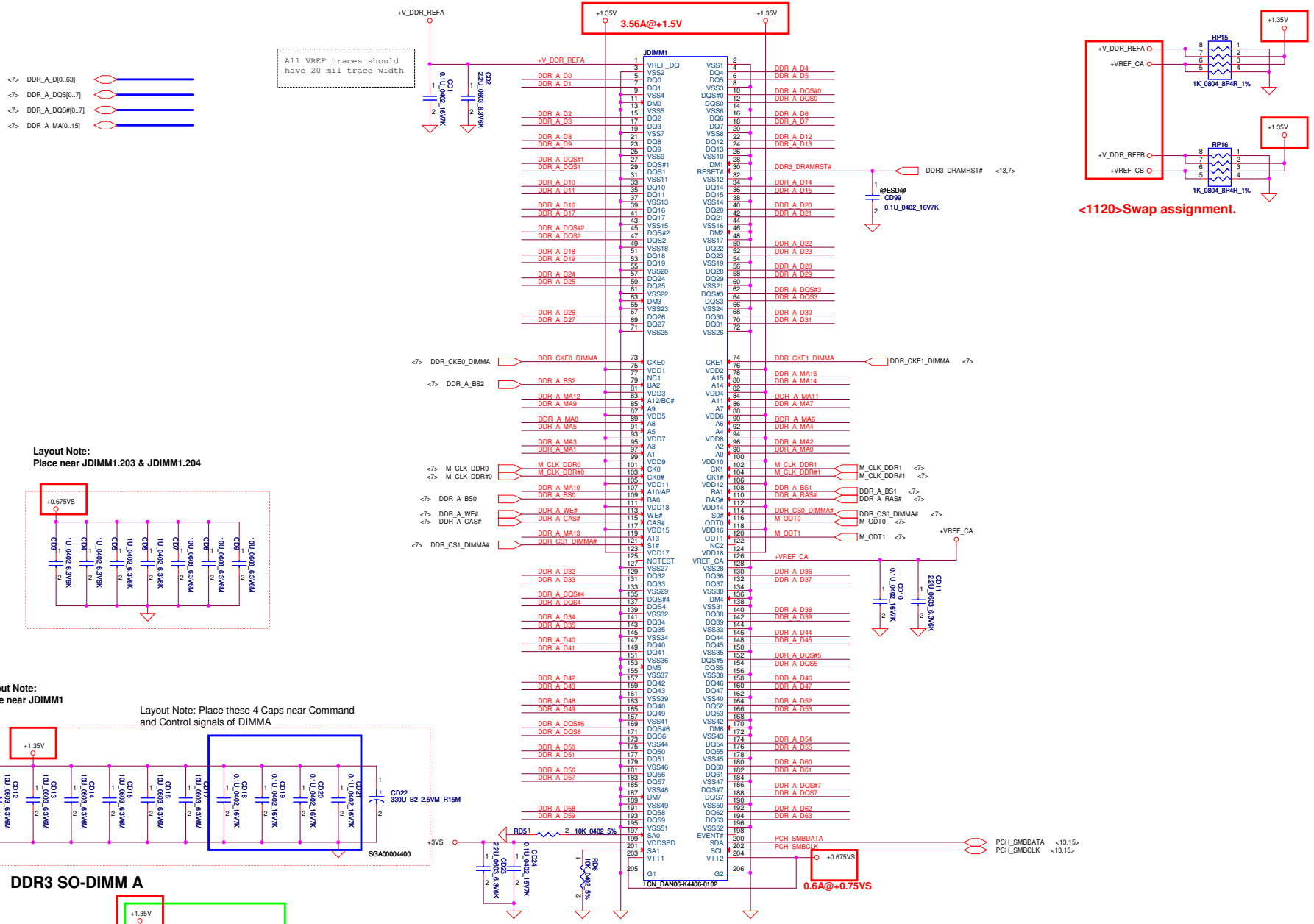
Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	LA-8041P	0.1

Date: Friday, March 14, 2014 Sheet 11 of 58

DDR3 SO-DIMM A



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Title	DDRIII DIMM		
Size	Document Number		Rev
C	LA-8661P		0.1
Date:	Friday, March 14, 2014	Sheet	12 of 58

DDR3 SO-DIMM B

10/03 change to +V_DDR_REFB

+V_DDR_REFB

All VREF traces should have 20 mil trace width

CD50 0.1U_0402_16V7K

CD39 220U_0603_6.3V6K

+1.35V 3.56A@+1.5V +1.35V

JDIMM2

<7> DDR_B_D[0..63]
<7> DDR_B_DQS[0..7]
<7> DDR_B_DQS#[0..7]
<7> DDR_B_MA[0..15]

Delete DDR_B_DM[0..7]

10/03 change to +V_DDR_REFB

	+V_DDR_REFB	1	VREF_DQ	VSS1	2		
	DDR_B_D0	3	VSS2	DQ4	4	DDR_B_D4	
	DDR_B_D1	5	DQ0	DQ5	6	DDR_B_D5	
		7	DQ1	VSS3	8		
		9	VSS4	DQS#0	10	DDR_B_DQS#0	
		11	DM0	DQS0	12	DDR_B_DQS0	
		13	VSS5	DQ6	14		
	DDR_B_D2	15	DQ2	DQ7	16	DDR_B_D6	
	DDR_B_D3	17	DQ3	VSS8	18	DDR_B_D7	
		19	VSS7	DQ12	20		
	DDR_B_D8	21	DQ8	DQ13	22	DDR_B_D12	
	DDR_B_D9	23	DQ9	VSS10	24	DDR_B_D13	
		25	VSS9	DM1	26		
	DDR_B_DQS#1	27	DQS#1	RESET#	28		
	DDR_B_DQS1	29	DQS1	VSS12	30	DDR3_DRAMRST#	DDR3_DRAMRST# <12,7>
		31	VSS11	DQ14	32		
	DDR_B_D10	33	DQ10	DQ15	34	DDR_B_D14	
	DDR_B_D11	35	DQ11	VSS14	36	DDR_B_D15	
		37	VSS13	DQ20	38		
	DDR_B_D16	39	DQ16	DQ21	40	DDR_B_D20	
	DDR_B_D17	41	DQ17	VSS16	42	DDR_B_D21	
		43	VSS15	DM2	44		
	DDR_B_DQS#2	45	DQS#2	VSS17	46		
	DDR_B_DQS2	47	DQS2	DQ22	48	DDR_B_D22	
		49	VSS18	DQ23	50	DDR_B_D23	
	DDR_B_D18	51	DQ18	VSS19	52		
	DDR_B_D19	53	DQ19	DQ28	54	DDR_B_D28	
		55	VSS20	DQ29	56	DDR_B_D29	
	DDR_B_D24	57	DQ24	VSS21	58		
	DDR_B_D25	59	DQ25	DQS#3	60	DDR_B_DQS#3	
		61	VSS22	DQS3	62	DDR_B_DQS3	
		63	DM3	VSS24	64		
		65	VSS23	DQ30	66		
	DDR_B_D26	67	DQ26	DQ31	68	DDR_B_D30	
	DDR_B_D27	69	DQ27	VSS26	70	DDR_B_D31	
		71	VSS25		72		
<7> DDR_CKE0_DIMMB	DDR_CKE0_DIMMB	73	CKE0	CKE1	74	DDR_CKE1_DIMMB	DDR_CKE1_DIMMB <7>
		75	VDD1	VDD2	76		
		77	NC1	A15	78	DDR_B_MA15	
<7> DDR_B_BS2	DDR_B_BS2	79	BA2	A14	80	DDR_B_MA14	
		81	VDD3	VDD4	82		
	DDR_B_MA12	83	A12/BC#	A11	84	DDR_B_MA11	
	DDR_B_MA9	85	A9	A7	86	DDR_B_MA7	
		87	VDD5	VDD6	88		
	DDR_B_MA8	89	A8	A6	90	DDR_B_MA6	
	DDR_B_MA5	91	A5	A4	92	DDR_B_MA4	
		93	VDD7	VDD8	94		
	DDR_B_MA3	95	A3	A2	96	DDR_B_MA2	
	DDR_B_MA1	97	A1	A0	98	DDR_B_MA0	
		99	VDD9	VDD10	100		
<7> M_CLK_DDR2	M_CLK_DDR2	101	CK0	CK1	102	M_CLK_DDR3	M_CLK_DDR3 <7>
<7> M_CLK_DDR#2	M_CLK_DDR#2	103	CK0#	CK1#	104	M_CLK_DDR#3	M_CLK_DDR#3 <7>
		105	VDD11	VDD12	106		
	DDR_B_MA10	107	A10/AP	BA1	108	DDR_B_BS1	DDR_B_BS1 <7>
<7> DDR_B_BS0	DDR_B_BS0	109	BA0	RAS#	110	DDR_B_RAS#	DDR_B_RAS# <7>
		111	VDD13	VDD14	112		
<7> DDR_B_WE#	DDR_B_WE#	113	WE#	S0#	114	DDR_CS0_DIMMB#	DDR_CS0_DIMMB# <7>
<7> DDR_B_CAS#	DDR_B_CAS#	115	CAS#	ODT0	116	M_ODT2	M_ODT2 <7>
		117	VDD15	VDD16	118		
	DDR_B_MA13	119	A13	ODT1	120	M_ODT3	M_ODT3 <7>
<7> DDR_CS1_DIMMB#	DDR_CS1_DIMMB#	121	S1#	NC2	122		
		123	VDD17	VDD18	124		
		125	NCTEST	VREF_CA	126	+VREF_CB	
		127	VSS27	VSS28	128		
	DDR_B_D32	129	DQ32	DQ36	130	DDR_B_D36	
	DDR_B_D33	131	DQ33	DQ37	132	DDR_B_D37	
		133	VSS29	VSS30	134		
	DDR_B_DQS#4	135	DQS#4	DM4	136		
	DDR_B_DQS4	137	DQS4	VSS31	138		
		139	VSS32	DQ38	140	DDR_B_D38	
	DDR_B_D34	141	DQ34	DQ39	142	DDR_B_D39	
	DDR_B_D35	143	DQ35	VSS33	144		
		145	VSS34	DQ44	146	DDR_B_D44	
	DDR_B_D40	147	DQ40	DQ45	148	DDR_B_D45	
	DDR_B_D41	149	DQ41	VSS35	150		
		151	VSS36	DQS#5	152	DDR_B_DQS#5	
		153	DM5	DQS5	154	DDR_B_DQS5	
		155	VSS37	VSS38	156		
	DDR_B_D42	157	DQ42	DQ46	158	DDR_B_D46	
	DDR_B_D43	159	DQ43	DQ47	160	DDR_B_D47	
		161	VSS39	VSS40	162		
	DDR_B_D48	163	DQ48	DQ52	164	DDR_B_D52	
	DDR_B_D49	165	DQ49	DQ53	166	DDR_B_D53	
		167	VSS41	VSS42	168		
	DDR_B_DQS#6	169	DQS#6	DM6	170		
	DDR_B_DQS6	171	DQS6	VSS43	172		
		173	VSS44	DQ54	174	DDR_B_D54	
	DDR_B_D50	175	DQ50	DQ55	176	DDR_B_D55	
	DDR_B_D51	177	DQ51	VSS45	178		
		179	VSS46	DQ60	180	DDR_B_D60	
	DDR_B_D56	181	DQ56	DQ61	182	DDR_B_D61	
	DDR_B_D57	183	DQ57	VSS47	184		
		185	VSS48	DQS#7	186	DDR_B_DQS#7	
		187	DM7	DQS7	188	DDR_B_DQS7	
		189	VSS49	VSS50	190		
	DDR_B_D58	191	DQ58	DQ62	192	DDR_B_D62	
	DDR_B_D59	193	DQ59	DQ63	194	DDR_B_D63	
		195	VSS51	VSS52	196		
		197	SA0	EVENT#	198		
		199	VDDSPD	SDA	200	PCH_SMBDATA	PCH_SMBDATA <12,15>
		201	SA1	SCL	202	PCH_SMBCLK	PCH_SMBCLK <12,15>
		203	VTT1	VTT2	204	+0.675VS	
		205			206		
			G1	G2			

LCN_DAN06-K4406-0102

0.6A@+0.75VS

VREF_CB

CD55 0.1U_0402_16V7K

CD20 220U_0603_6.3V6K

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

+0.675VS

CD41 10U_0603_6.3V6M
CD51 1U_0402_6.3V6K
CD54 1U_0402_6.3V6K
CD48 1U_0402_6.3V6K
CD53 10U_0603_6.3V6M
CD52 10U_0603_6.3V6M
CD49 10U_0603_6.3V6M

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.35V

CD57 10U_0603_6.3V6M
CD46 10U_0603_6.3V6M
CD45 10U_0603_6.3V6M
CD40 10U_0603_6.3V6M
CD42 10U_0603_6.3V6M
CD58 10U_0603_6.3V6M
CD44 0.1U_0402_16V7K
CD3 0.1U_0402_16V7K
CD47 0.1U_0402_16V7K
CD59 0.1U_0402_16V7K
CD38 470U_6.3V_M_B1_ESR70M
CD57 47U 6.3V M B1 ESR70M @

+3VS

RD71 2 10K_0402_5%

CD31 220U_0603_6.3V6K

CD36 0.1U_0402_16V7K

RD9 10K_0402_5%

+3VS

DDR3 SO-DIMM B

+1.35V

CD33 0.1U_0402_16V7K @
CD34 0.1U_0402_16V7K @
CD35 0.1U_0402_16V7K @
CD32 0.1U_0402_16V7K

SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

10/05 change to PH.

Standard
<Address(SA1,SA0):10>

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: DDRIII-DDRH

Size | Document Number: LA-8661P | Rev: 0.1

Date: Friday, March 14, 2014 | Sheet 13 of 58

PCH_RTCX1
PCH_RTCX2
RH115 10M_0402_5%
XH1
32.768KHZ QT3FC1350000500
SJT0000EC00
<1111> Follow common 10ppm.
CH2 18P_0201_50V8J
CH3 18P_0201_50V8J

+RTCVCC
This is needed to reduce leakage from Coin Cell Battery in G3 state
RH1161 1M_0402_5%
SM_INTRUDER#

9/7 SMT memo:Follow PM requirement change R1 p/n into PV BOM
R1: SA00004EES0
R3: SA00004QOB0

UH1A

+RTCVCC
CH4 1U_0402_6.3V6K
CLRP1 SHORT PADS
RH117 20K_0402_5%
RH118 20K_0402_5%
CH5 1U_0402_6.3V6K
CLRP2 SHORT PADS
CMOS
ME CMOS
CLP1 & CLP2 place near DIMM

For EMI
131204 SWAP
RP12 33_0804_8P4R_5%
<37> HDA_BITCLK_AUDIO
<37> HDA_RST_AUDIO#
<37> HDA_SYNC_AUDIO
<37> HDA_SDOUT_AUDIO
HDA_BIT_CLK
HDA_RST#
HDA_SYNC_R
HDA_SDOUT

+5VS
Prevent back drive issue.
QH1 SB00000S700 BSS138W-7-F_SOT323-3
RH158 1M_0402_5%
RH122 0_0402_5%
7/12 SI add 1M pull down

9/7 SMT memo:Follow intel ME update requirement add: RH123
<41> HDA_SDO
RH123 0_0402_5%

PCH_RTCX1 A20 RTCX1
PCH_RTCX2 C20 RTCX2
PCH_RTCRST# D20 RTCRST#
PCH_SRTCRST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC

HDA_BIT_CLK_OUT N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
HDA_SPKR T10 SPKR
HDA_RST# K34 HDA_RST#
HDA_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
HDA_SDOUT A36 HDA_SDO
C36 HDA_DOCK_EN# / GPIO33
N32 HDA_DOCK_RST# / GPIO13
IHDA

PCH_JTAG_TCK J3 JTAG_TCK
PCH_JTAG_TMS H7 JTAG_TMS
PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO
JTAG

SPI_CLK_PCH_OUT T3 SPI_CLK
SPI_SB_CS0# Y14 SPI_CS0#
T1 SPI_CS1#
SPI_SI_PCH V4 SPI_MOSI
SPI_SO_PCH U3 SPI_MISO
SPI

PANTHER-POINT_FCBGA989

LPC:
FWH0 / LAD0 C38 LPC_AD0 <40,41>
FWH1 / LAD1 A38 LPC_AD1 <40,41>
FWH2 / LAD2 B37 LPC_AD2 <40,41>
FWH3 / LAD3 C37 LPC_AD3 <40,41>
FWH4 / LFRAME# D36 LPC_FRAME# <40,41>
LDRQ0# E36
LDRQ1# / GPIO23 K36
SERIRQ V5 SERIRQ <40,41>
EC and TPM.

SATA 6G:
SATA0RXN AM3
SATA0RXP AM1
SATA0TXN AP7
SATA0TXP AP5
SATA_PRX_DTX_N0 <34>
SATA_PRX_DTX_P0 <34>
SATA_PTX_DRX_N0 <34>
SATA_PTX_DRX_P0 <34>
SATA HDD

SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11
SATA1TXP AP10

SATA:
SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
SATA_PRX_DTX_N2 <34>
SATA_PRX_DTX_P2 <34>
SATA_PTX_DRX_N2 <34>
SATA_PTX_DRX_P2 <34>
ODD

SATA3RXN AB8
SATA3RXP AF3
SATA3TXN AF1
SATA3TXP
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1

SATAICOMPO Y11
SATAICOMPI Y10
SATA_COMP RH130 37.4_0402_1%
+1.05VS_VCC_SATA
SATA3RCOMPO AB12
SATA3COMPI AB13
SATA3_COMP RH132 49.9_0402_1%
+1.05VS_SATA3
SATA3RBIAS AH1
RBIAS_SATA3 RH137 750_0402_1%

SATALED# P3 SATA_LED# <39>
SATA0GP / GPIO21 V1 HDDHALT_LED#
SATA1GP / GPIO19 P1 BBS_BIT0_R

change to RP 11.06

RP17 10K_0804_8P4R_5%
BBS_BIT0_R
SATA_LED#
HDDHALT_LED#
SERIRQ
+3VS

HDA_SPKR RH139 1K_0402_5%
LOW=Default
HIGH=No Reboot

PCH_INTVRMEN RH124 330K_0402_5%
PCH_INTVRMEN RH126 330K_0402_5%
INTVRMEN
H : Integrated VRM enable
L : Integrated VRM disable

HDA_SDO
ME debug mode , this signal has a weak internal PD
L=>security measures defined in the Flash Descriptor will be in effect (default)
H=>Flash Descriptor Security will be overridden
HDA_SDOUT RH140 1K_0402_5%
Low = Disabled
High = Enabled

RTC Battery
+RTCVCC
CH7 1U_0402_6.3V6K
Place CH95 close to PCH.
DH1 BAV70W 3P C/C_SOT-323
1K_0402_5%
RH148 10mils
20mils
+RTCBATT
+3VL
<1118> change to +3VL.

HDA_SYNC
This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom
HDA_SYNC RH149 1K_0402_5%

SI2 delete RH128& RH127 200 ohm for CPU screw PAD
12.19
+3V_PCH
RH129 200_0402_5%
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_JTAG_TDI
RH133 100_0201_1%
RH134 100_0402_1%
RH135 100_0402_1%

SI2 change to RH133 0201
12.19

PCH_JTAG_TCK
51_0402_5%
RH150

SPI_CLK_PCH_1
RH507 0_0402_5%
SPI_CLK_PCH_OUT

SPI BIOS Pinout
(1)CS# (2)DO (3)WP# (4)GND (5)DIO (6)CLK (7)HOLD# (8)VCC
W25X32

SPI BIOS Pinout
(1)CS# (2)DO (3)WP# (4)GND (5)DIO (6)CLK (7)HOLD# (8)VCC
W25X32

RTC BAT conn
+RTCBATT
15mils
JRTC1
LOTES_AAA-BAT-054-K01
CONN@

SPI ROM 8M
(Share ROM)
EON SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P
MXIC SA000069100 S IC FL 64M MX25L6473EMI-10G SOP 8P
WINBOND SA000039A30 S IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM
Micron SA00005L100 S IC FL 64M N25Q064A13ESEC0F SO8W 8P

EC
ROM
place close to UH2
RPH17 15_0804_8P4R_5%
<41> EC_SPI_SO
<41> EC_SPI_SI
<41> EC_SPI_CLK
<41> EC_SPI_CS#
EC_SPI_SO
EC_SPI_SI
EC_SPI_CLK
EC_SPI_CS#
SPI_SO_PCH_R
SPI_SI_PCH_R
SPI_CLK_PCH_R
SPI_SB_CS0#_R

ROM
CPU
RPH18 15_0804_8P4R_5%
SPI_SO_PCH
SPI_SI_PCH
SPI_CLK_PCH
SPI_SB_CS0#

+3V_PCH
R127 3.3K_0402_5% SPI_WP#
R129 3.3K_0402_5% SPI_HOLD#
UH2 EN25Q64-104HIP
SPI_SB_CS0#_R
SPI_SO_PCH_R
SPI_WP#
CS# SO/SIO1 WP# GND VCC HOLD# SCLK SI/SIO0
SPI_HOLD#
SPI_CLK_PCH_R
SPI_SI_PCH_R

<1111>Modified SPI ROM fix code.
<1119>Add ROM socket.
<1205>Del ROM socket.

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.
Title: PCH (1/8) SATA,HDA,SPI, LPC
Size: Document Number: LA-A999P
Rev: 0.1
Date: Friday, March 14, 2014 Sheet 14 of 58

PV# 9/13 change power rail form +3VALW->+3V_PCH

10/03 change to PCIE port1.

Mini card WLAN

Card Reader

PCIE LAN

UH1B

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

PANTHER-POINT_FCBGA989

MiniWLAN

<1119>Change back to +3V_PCH.

Card Reader

PCIE LAN

SI2 change to 0201
12.19

SI2 change to 0201
12.19

Change WL_OFF# to GPIO45 (pull-high) +3V_PCH
2012.01.04

<1118>change to standard part.

<1126>Del RH193/CH14/RH195/CH15

131202 Follow 15" CRV

131224
For Integrated Graphics designs using eDP on Ivy Bridge.
For designs not using eDP, can leave as No Connect

131127 SWAP Pin of RP9.1 & RP9.2 by layout requested

<1113>change to RP18.

If use external CLK gen, please place close to CLK gen else, please place close to PCH

<1113>Swap.
<1118> add SML0 ; SMB2 removed.

SI# 8/8 Add SML1CLK/SML1DATA for EC detect Thermal

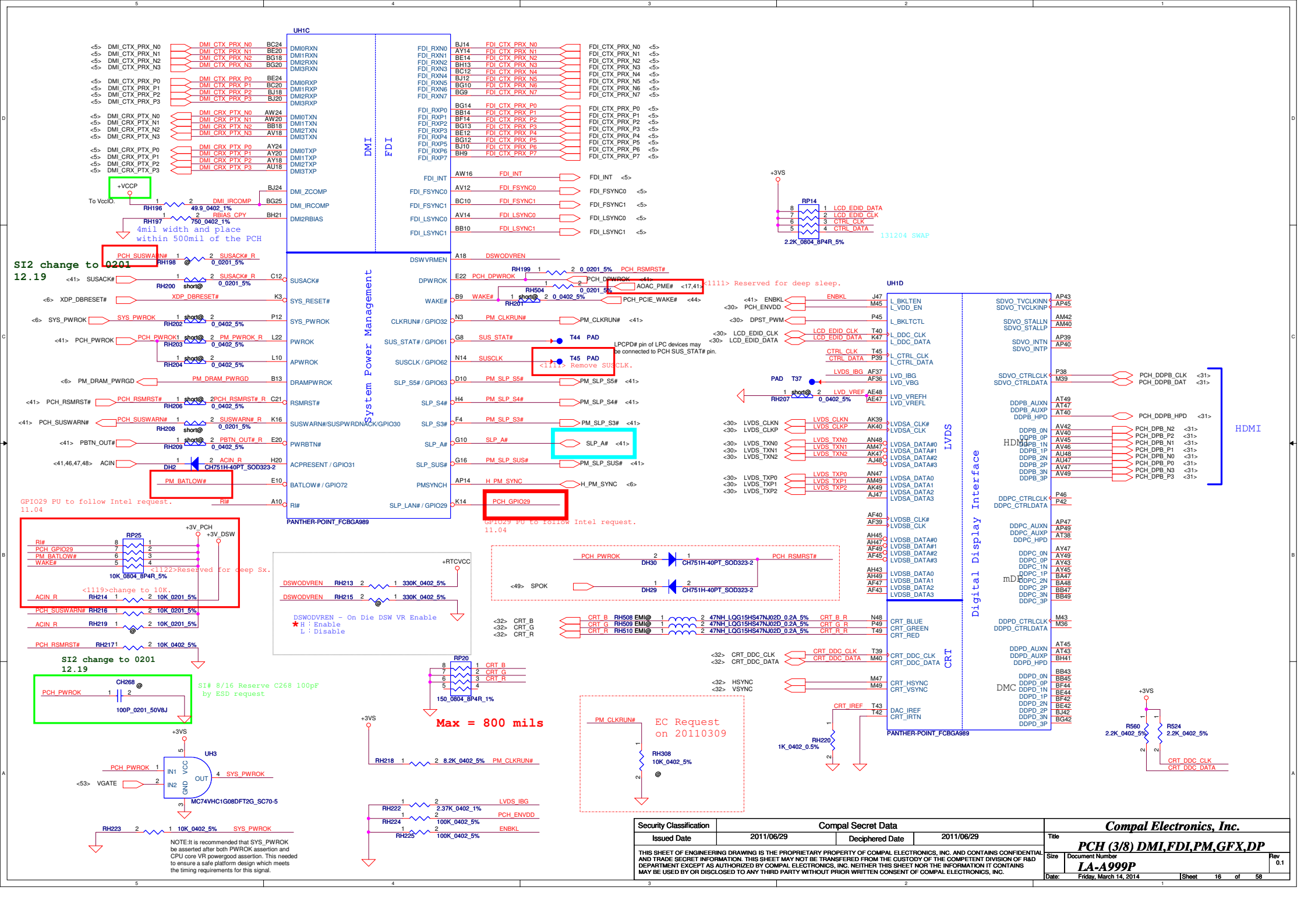
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size: | Document Number: LA-A999P | Rev: 0.1

Date: Friday, March 14, 2014 | Sheet 15 of 58



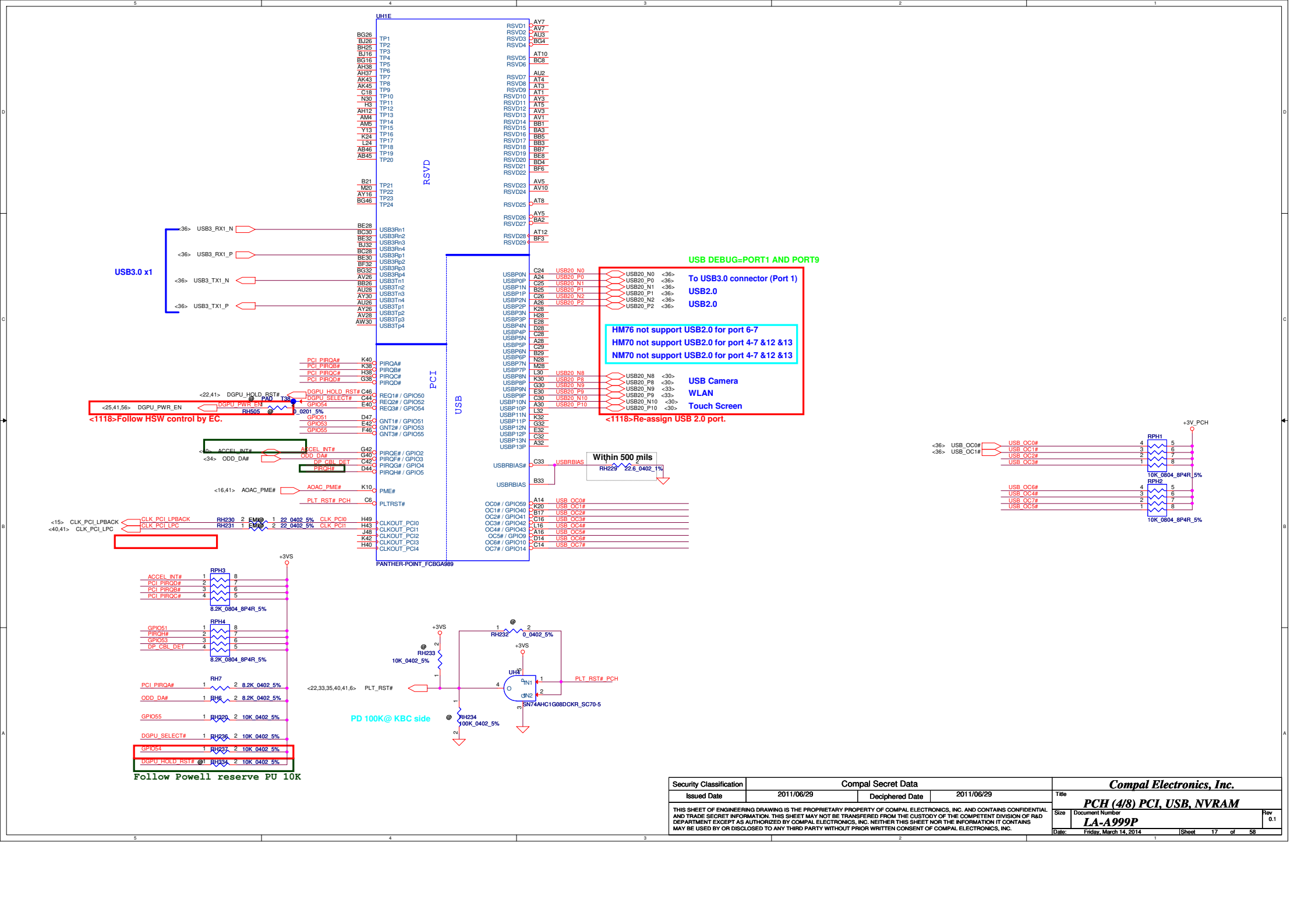
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: **PCH (3/8) DMI,FDI,PM,GFX,DP**

Size	Document Number	Rev
	LA-A999P	0.1

Date: Friday, March 14, 2014 | Sheet 16 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PCH (4/8) PCI, USB, NVRAM

Size	Document Number	Rev
	LA-A999P	0.1

Date: Friday, March 14, 2014 Sheet 17 of 58

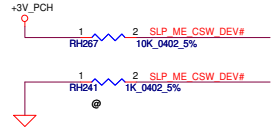
GPIO28

On-Die PLL Voltage Regulator

This signal has a weak internal pull up

★ H : On-Die voltage regulator enable

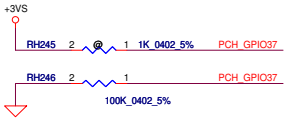
L : On-Die PLL Voltage Regulator disable



PCH_GPIO37

FDI TERMINATION VOLTAGE OVERRIDE

★ LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)

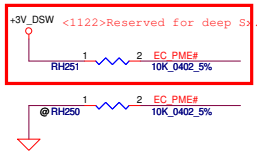


GPIO27

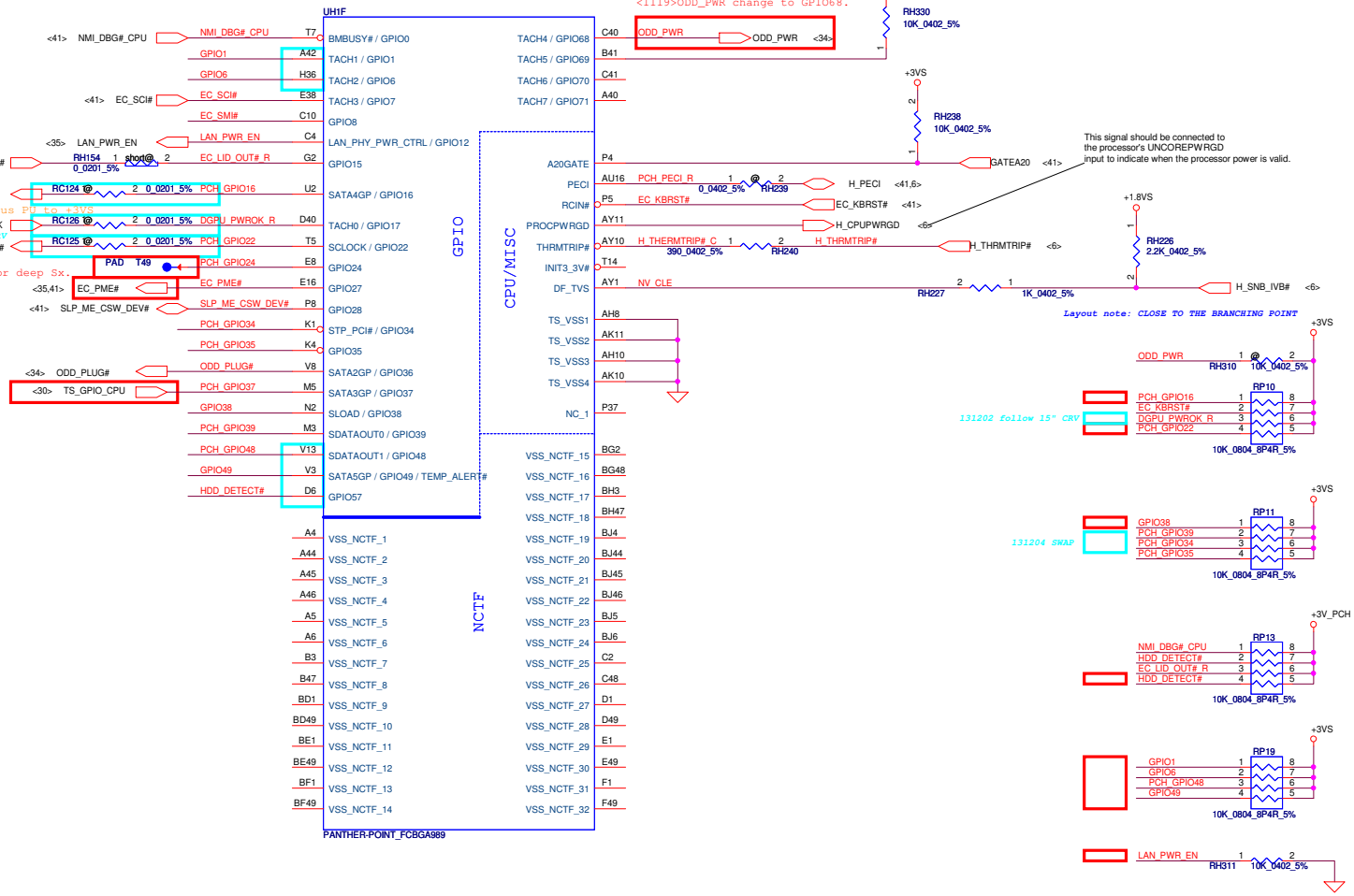
PCH_GPIO27 (Have internal Pull-High)

★High: VCCVRM VR Enable

Low: VCCVRM VR Disable



DB# 10/20 Reserve GPIO 36 pull up resistor and add pull down resistor



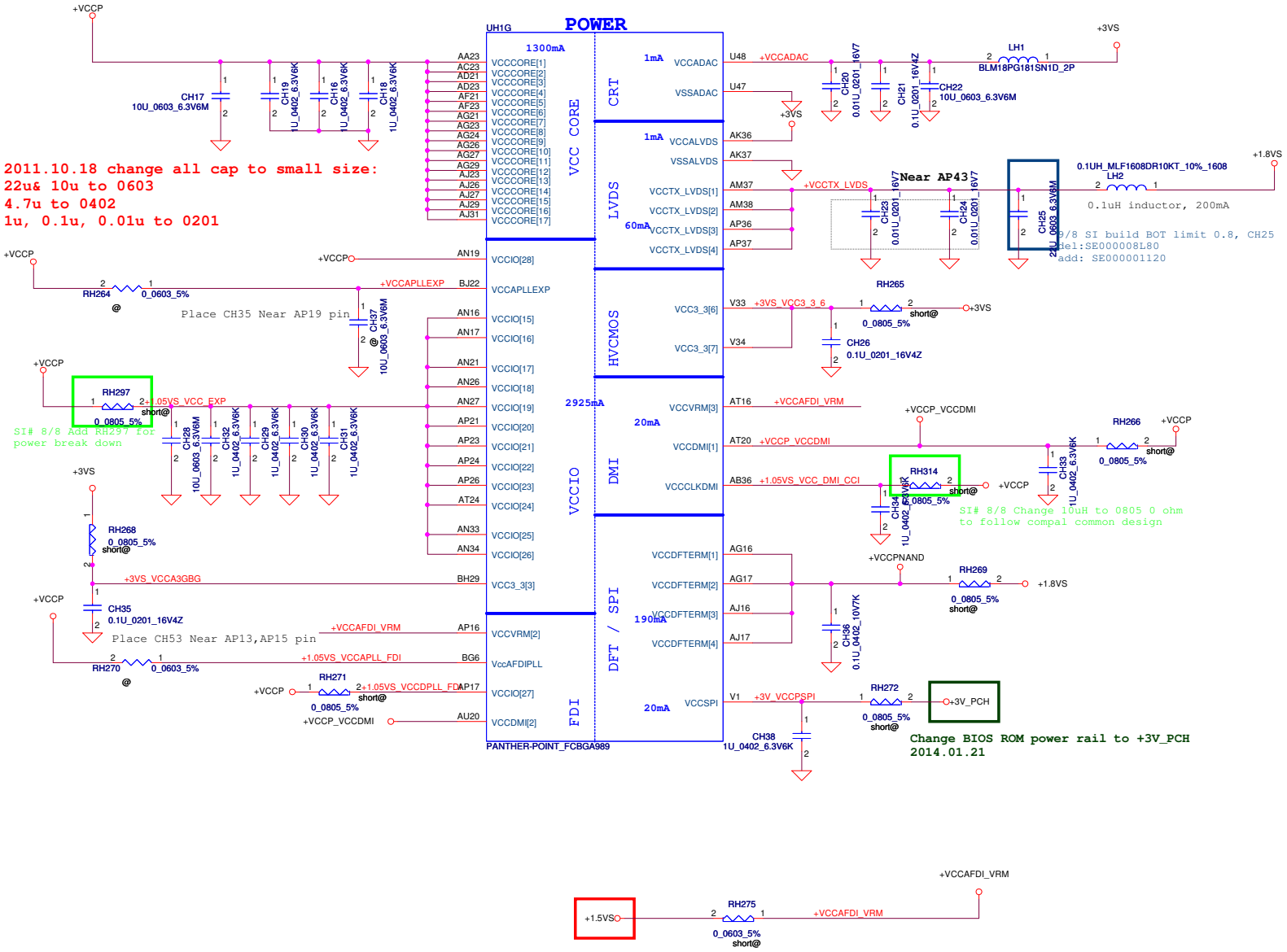
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PCH (5/8) GPIO, CPU, MISC

Size	Document Number	Rev
	LA-A999P	0.1

Date: Friday, March 14, 2014 Sheet 18 of 58



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

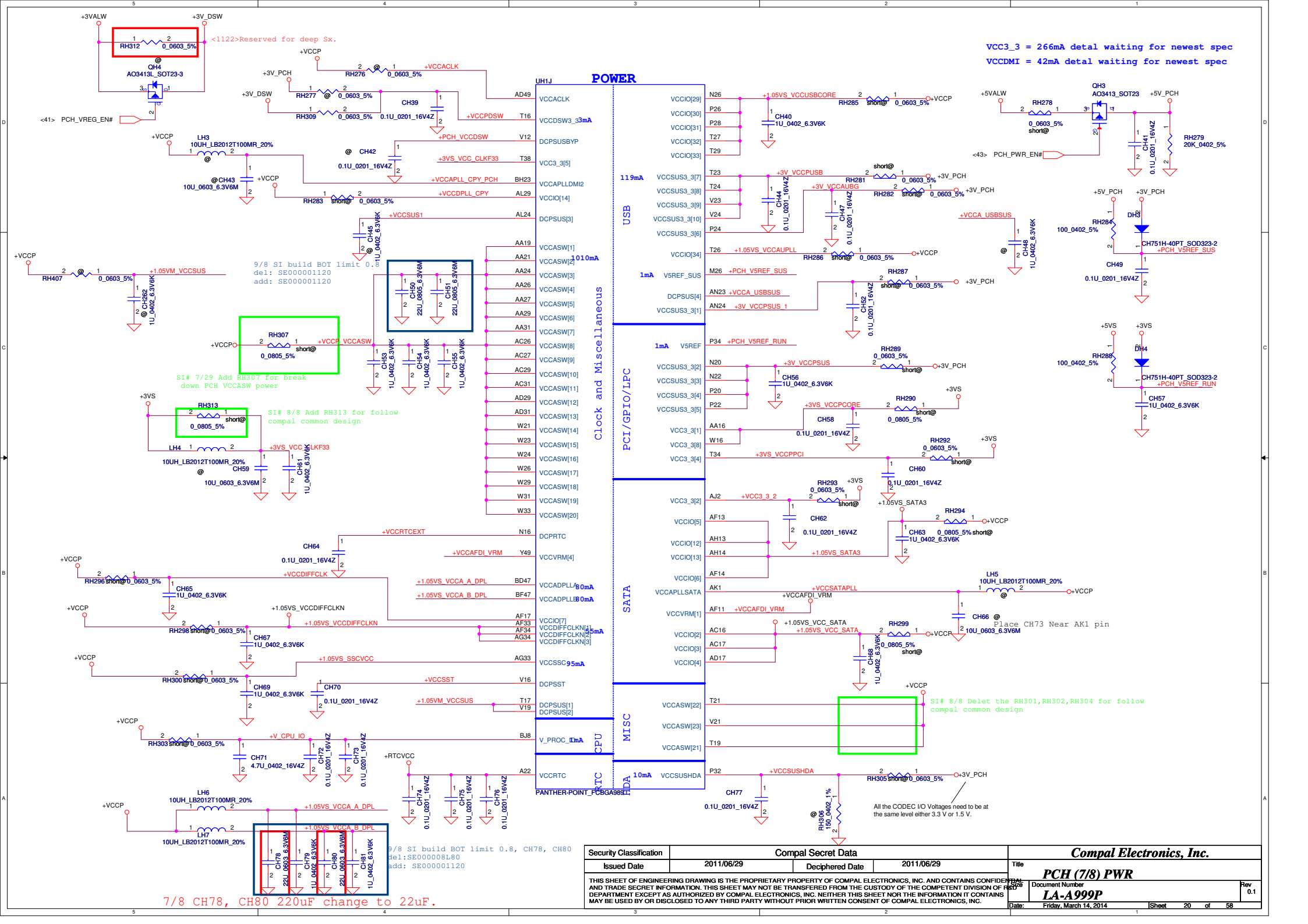
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size: | Document Number: LA-A999P | Rev: 0.1

Date: Friday, March 14, 2014 | Sheet 19 of 58



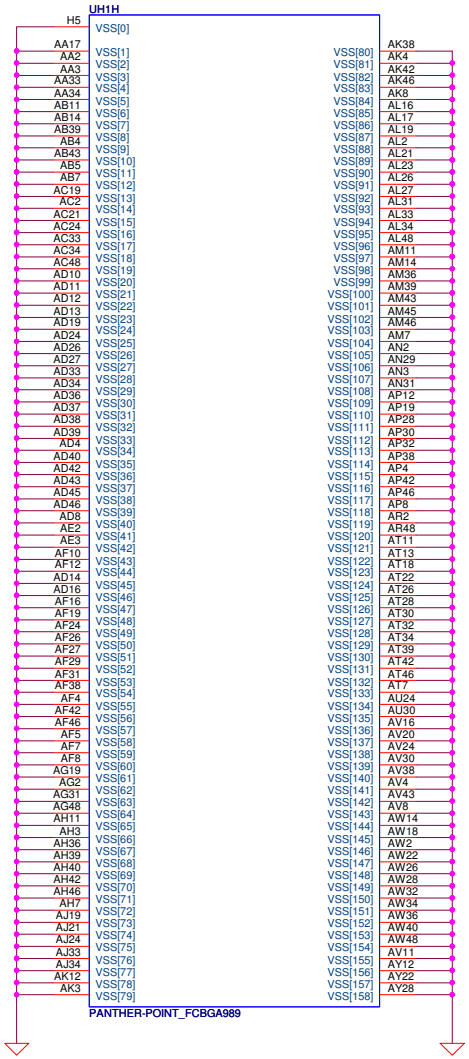
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

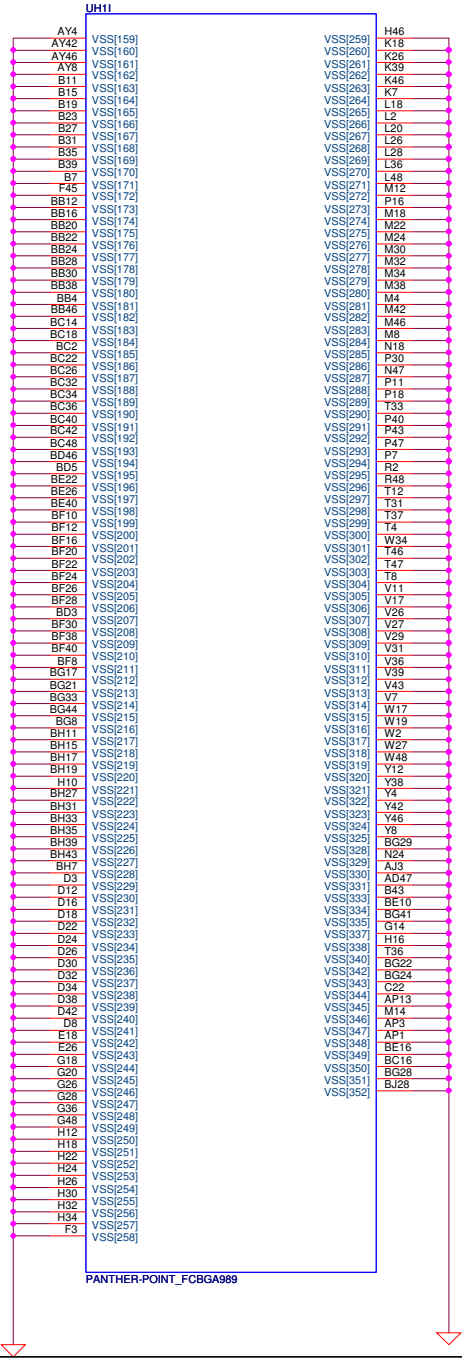
Compal Electronics, Inc.

Title: **PCH (7/8) PWR**

Size	Document Number	Rev
	LA-A999P	0.1

Date: Friday, March 14, 2014 Sheet 20 of 58





Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size	Document Number	Rev
	LA-A999P	0.1

Date: Friday, March 14, 2014 Sheet 21 of 58

#9/2 , Add RV191 between.
GPU_PWR_LEVEL# and GPU_THERMAL_DET#

#8/19 ,N15V-GM didn't support GC6,
unpop QV13 ,QV14.

131127 SWAP Pin of RV36.1, RV36.2 & RV36.4 by layout requested

#08/22,unused I2C change to pull-down.

#08/22,unused I2C change to pull-down.

Internal Thermal Sensor

<CPU>

<CPU>

<CPU>

Differential signal

Controlled by EC "AND" PCH

SI 11/05 change RV182,1
change to +3VGS from GPU_PWR_EN

PU AT EC SIDE, +3VS AND 4.7K

SJ10000CV00 cost is better.
<1118>change to standard part.

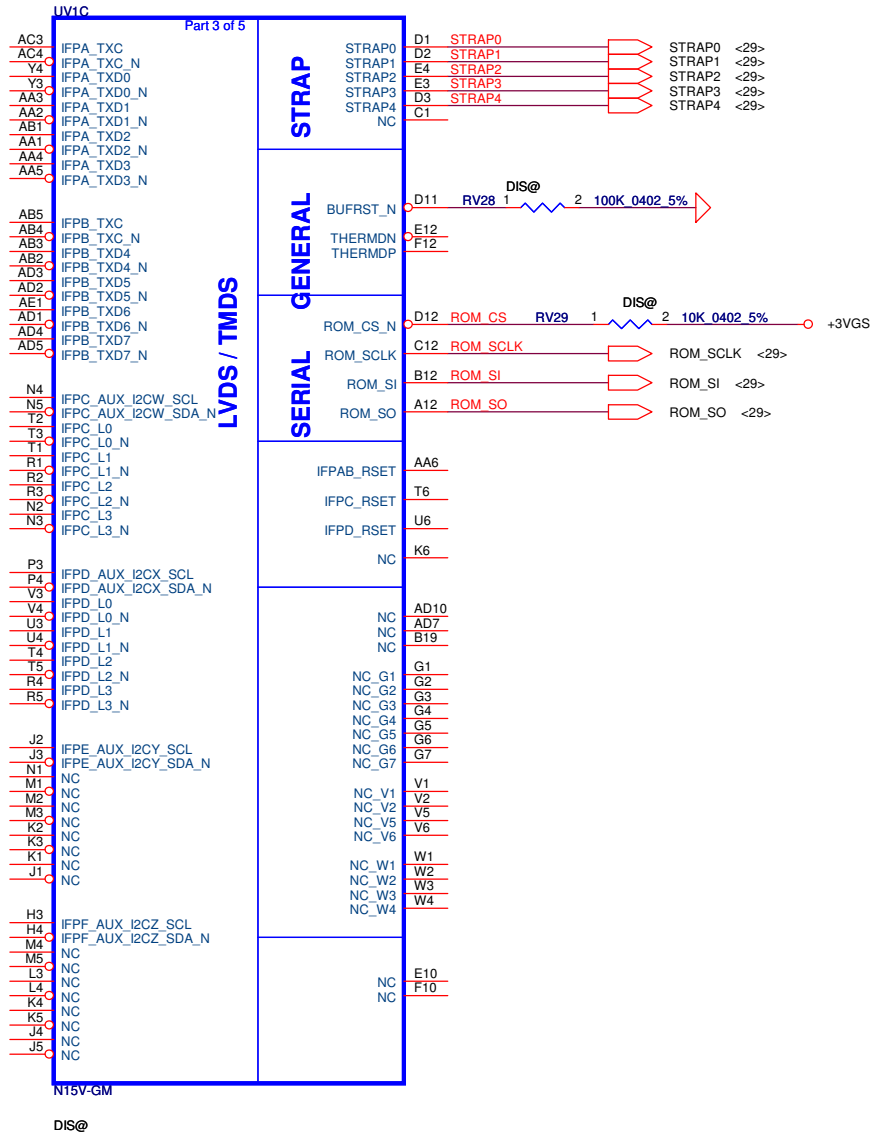
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: N15V-GM PCIE/DAC/GPIO

Size: Custom | Document Number: LA-A999P | Rev: 0.1

Date: Friday, March 14, 2014 | Sheet 22 of 58



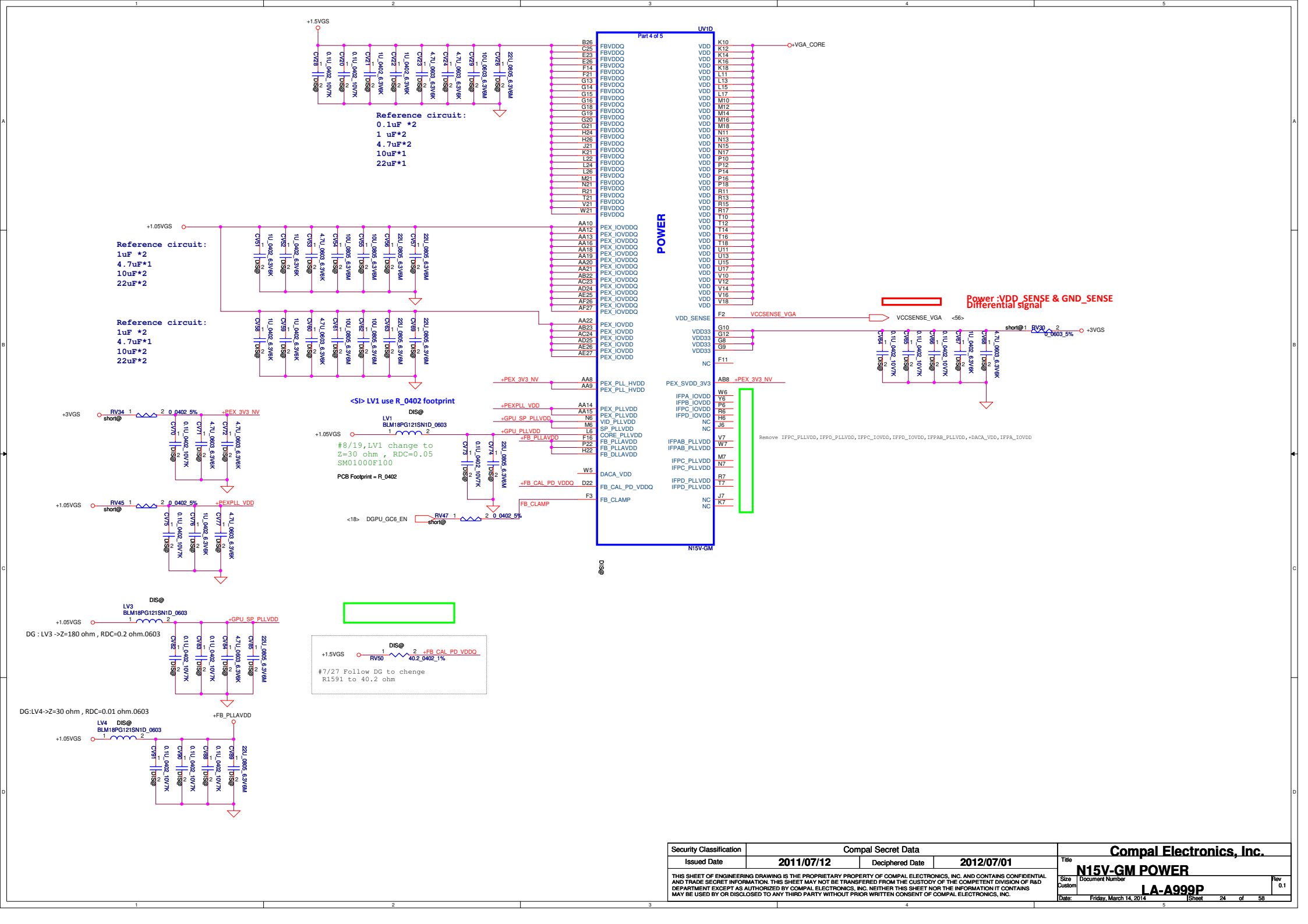
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: N15V-GM LVDS/HDMI/DP/THM

Size: B | Document Number: LA-A999P | Rev: 0.1

Date: Friday, March 14, 2014 | Sheet 23 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: N15V-GM POWER

Size: Custom | Document Number: LA-A999P | Rev: 0.1

Date: Friday, March 14, 2014 | Sheet 24 of 58

#8/20 : N15V-GM don't support GC6 function. UV20 unpop.

+1.05VGS=1.6A,4vias.

+3VALW to +3VGS

+1.05V to +1.05VGS

+1.5VGS=3.6A,8vias.

#8/19.QV15 change to TPS22967

+1.5V to +1.5VGS

+3VGS=0.5A,2vias.

#8/19.RV70 unpop , N15V-GM use binary mode.

Contrl by power

Power :VDD_SENSE & GND_SENSE

Differential signal

Power on

DGPU_PWR_EN

+3VGS

+VGA_CORE

DGPU_PWROK

+1.05VGS

+1.5VGS

40us < Rt < 2ms

#08/20 Don't support GC6,Add RV66.
Unpop QV16,RV41,RV42,CV78.

PV# 2013.01.08 Add +1.05VGS discharge circuit

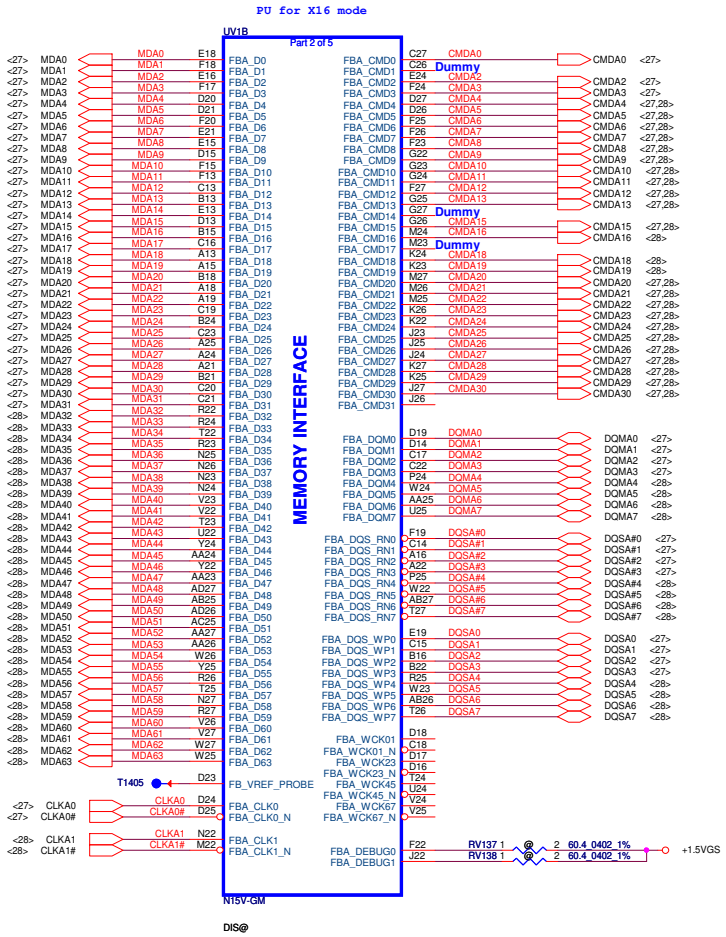
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

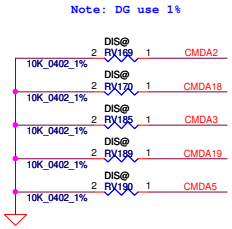
Compal Electronics, Inc.

Title: N15V-GM VGA CORE, GND

Size: Custom | Document Number: LA-A999P | Rev: 0.1

Date: Friday, March 14, 2014 | Sheet 25 of 58





Mode D Command Mapping

	RANK 0	
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Compal Electronics, Inc.

Title: N15V-GM MEM Interface

Size: Custom | Document Number: LA-A999P | Rev: 0.1

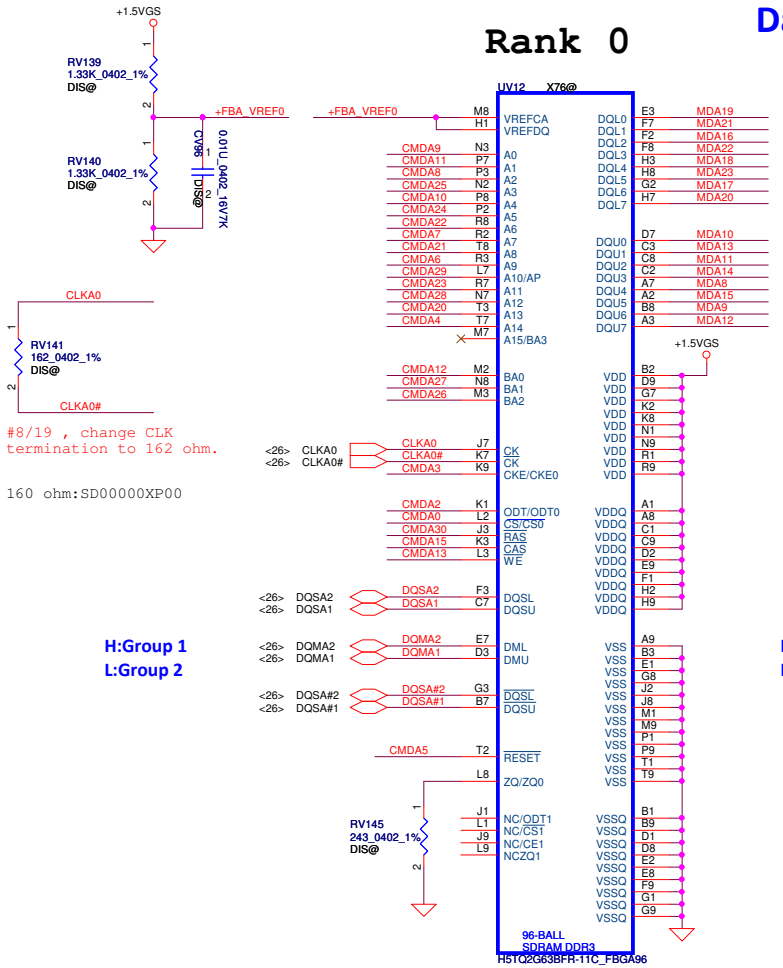
Date: Friday, March 14, 2014 | Sheet 26 of 58

Memory Partition A RANK 0

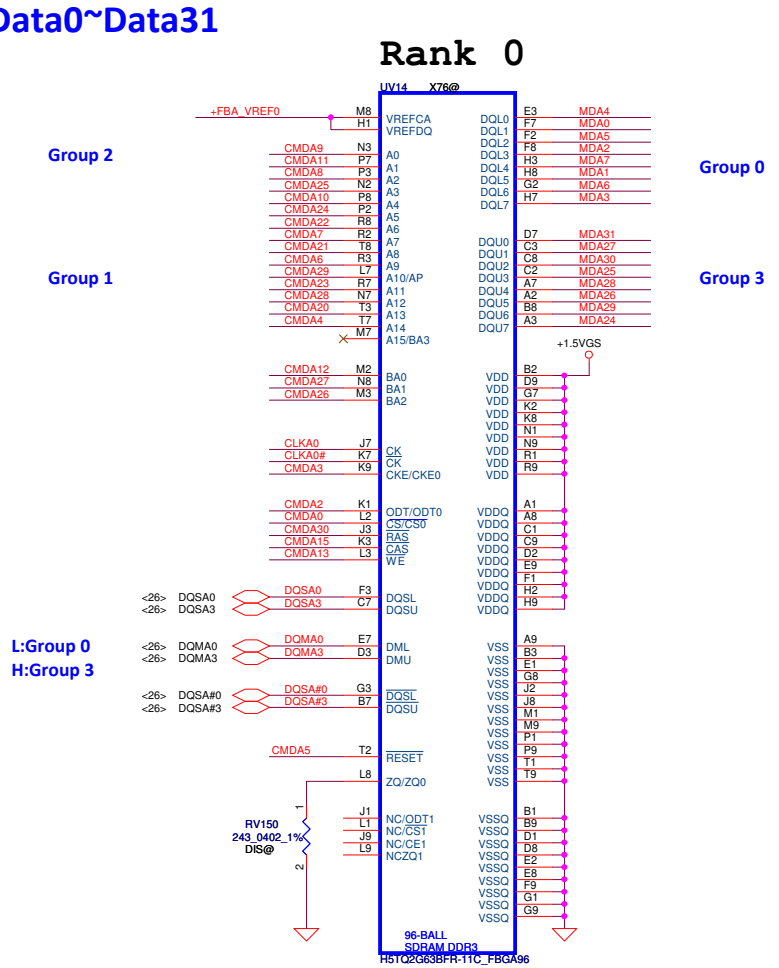
Data0~Data31

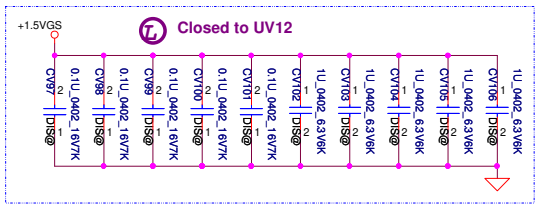
MDA[0..63] <26,28>
CMDA[30..0] <26,28>

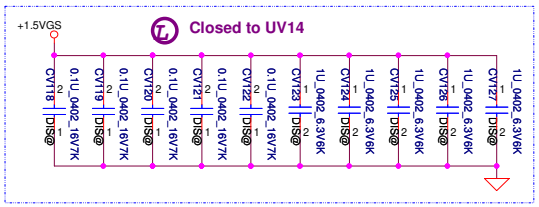
Rank 0



Rank 0







Mode D Command Mapping

	RANK 0	
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: N15V-GM VRAM A Lower

Size: Custom | Document Number: LA-A999P | Rev: 0.1

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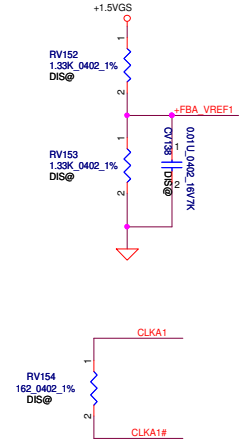
Memory Partition A RANK 0 32 bits

Rank 0

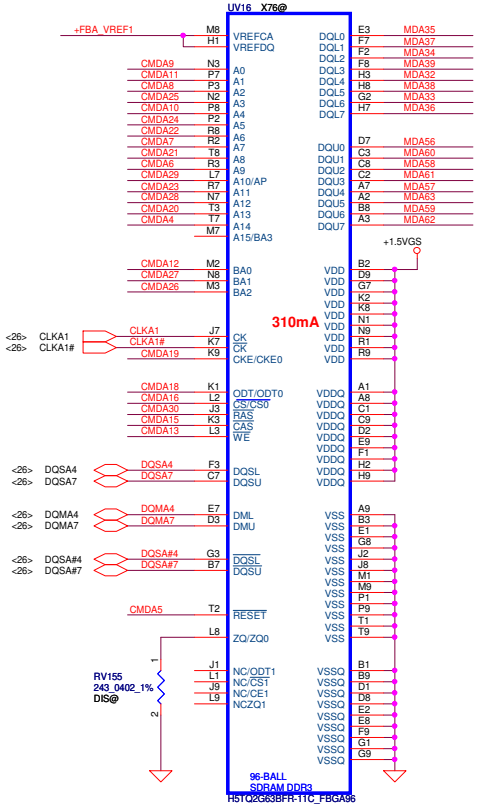
Data32~Data63

Rank 0

MDA[0..63] <26,27>
CMDA[30..0] <26,27>



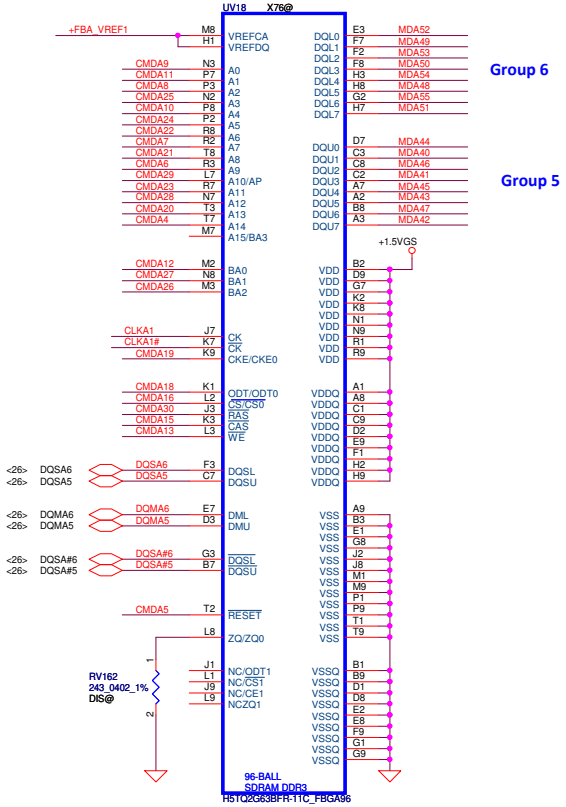
#8/19 , change CLK termination to 162 ohm.



Group 4

Group 7

L:Group 4
H:Group 7



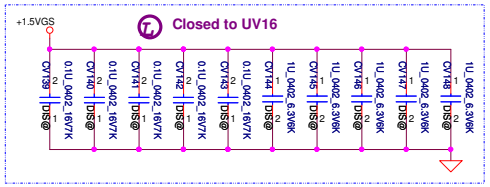
Group 6

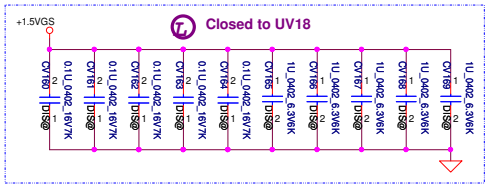
Group 5

L:Group 6
H:Group 5

Mode D Command Mapping

	RANK 0	
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#





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Issued Date	2011/07/12	Deciphered Date	2012/07/01

Compal Electronics, Inc.

Title: **N15V-GM VRAM C Lower**

Size: Custom | Document Number: **LA-A999P** | Rev: 0.1

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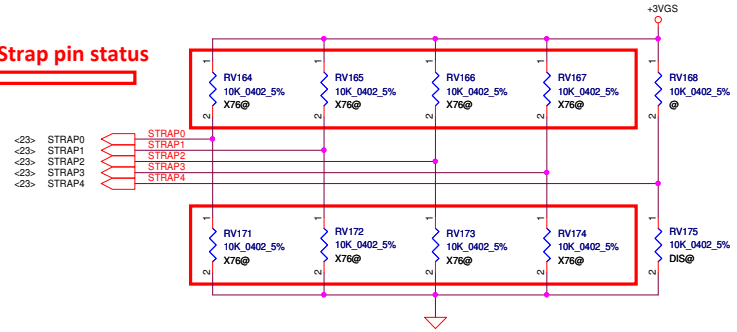
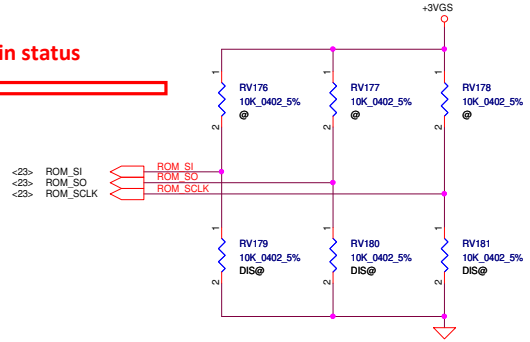
Check Strap pin status



Check SPI pin status



GPU	Project	VRAM size	CH	Description	Compal VRAM P/N	VRAM description	ROM CFG setup [3...0]	RAM_CFG	R P/N
N15V-GM (23x23) 64bit (One CH single rank)	ZSO40 ZSO50	128M(X16)	CHA	DDR3 Hynix 128Mx16 1.5V	SA00006H400	H5TC2G63FFR-11C 1000MHz	1100	RV171+RV172+RV167+RV166	
		128M(X16)	CHA	DDR3 Micron 128Mx16 1.5V	SA000067500	MT41J128M16JT-093G:K 1000MHz	**0001**	RV164+RV172+RV173+RV174	
		128M(X16)	CHA	DDR3 Samsung 128Mx16 1.5V	SA000068U00	K4W2G1646E-BC1A 1000MHz	**0101**	RV164+RV172+RV166+RV174	

#9/5 RAM_CFG follow RVL-06891-001 table 1.
Dule Rank layout with single Rank population.

Table 123

Strap pin Name	Strap Mapping	Resistance	Polarity	Logical Strapping Bit0
ROM_SCLK	SMB_ALT_ADDR	10K	Pull-down to GND.	
ROM_SI	SUB_VENDOR	10K	Pull-down to GND if no VBIOS ROM.	
ROM_SO	VGA_DEVICE	10K	Pull-down to GND(no diaplay).	
STRAP0	RAM_CFG[0]	10K		
STRAP1	RAM_CFG[1]	10K		
STRAP2	RAM_CFG[2]	10K		
STRAP3	RAM_CFG[3]	10K		
STRAP4	PCIE_MAX_SPEED	10K	Pull-down to GND(PCIE Gen1).	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

SUB_VENDOR	
0	Disable (Default)
1	

VGA_DEVICE	
0	Non-Primary 3D Acceleration Device(Class Code 302h)(Default)
1	Primary Display or VGA Device .

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

USER Straps	
User[3:0]	
1000-1100	Customer defined

Compal Electronics, Inc.

Title: N15V-GM MISC

Size: Custom | Document Number: LA-A999P | Rev: 1.0

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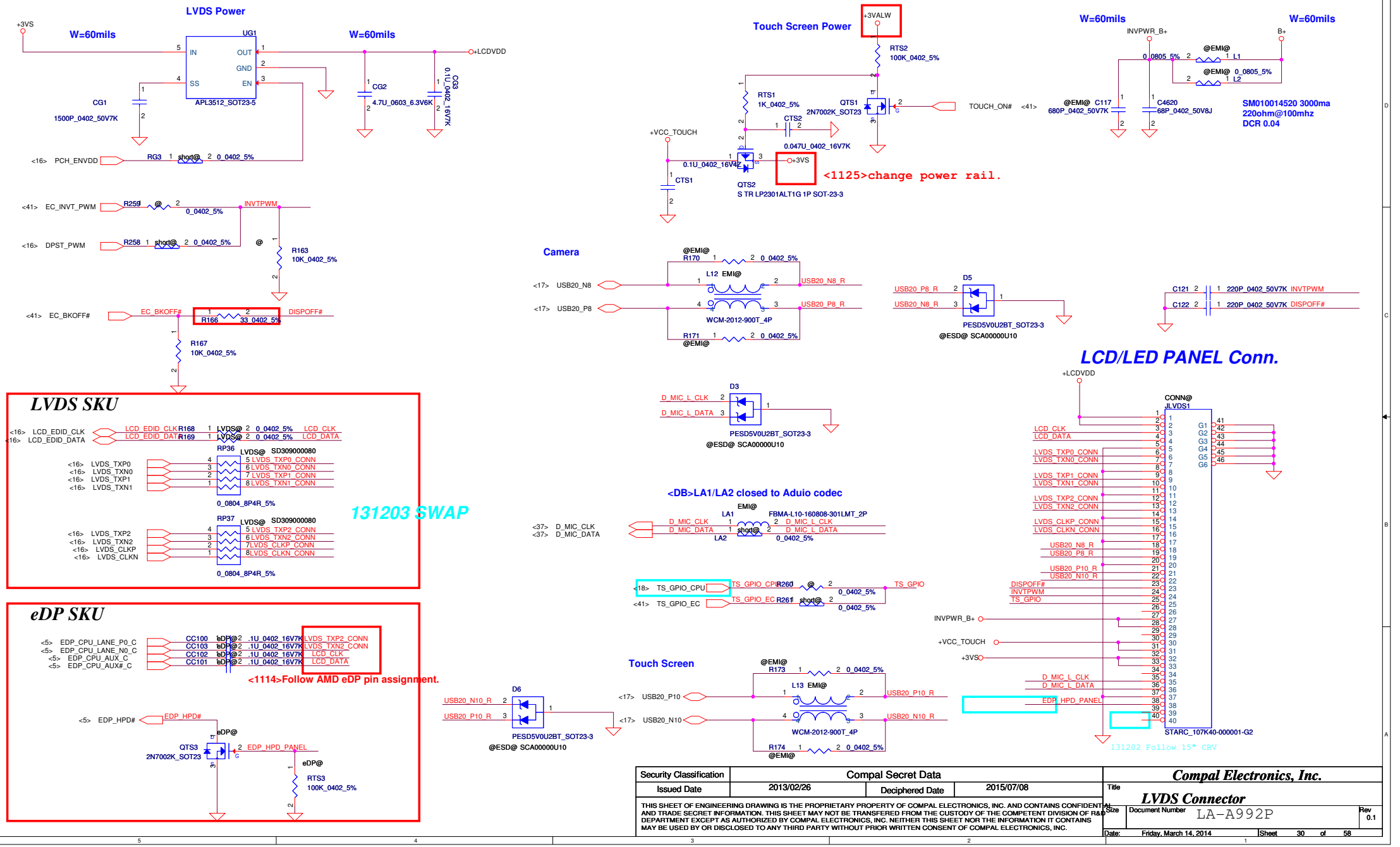


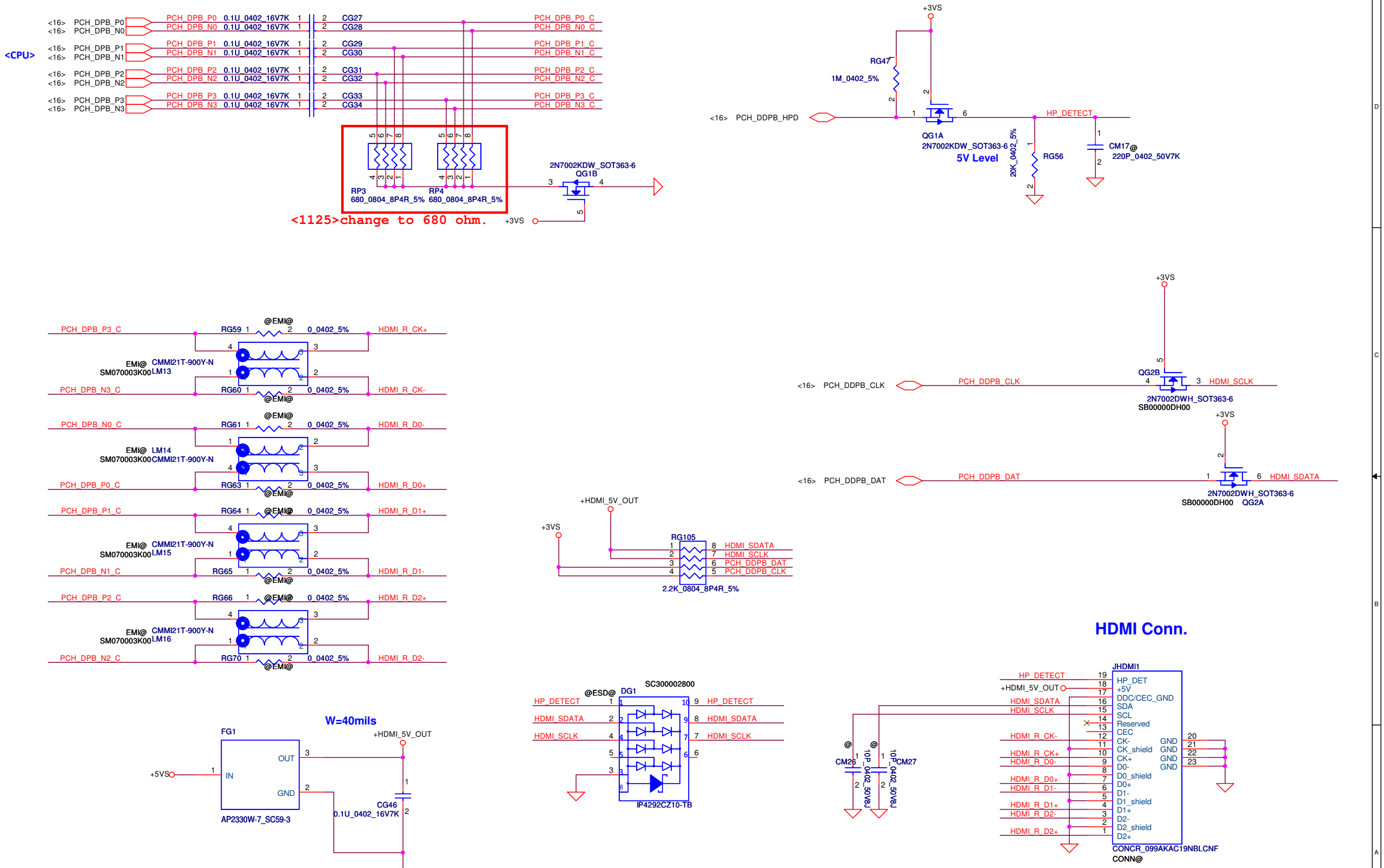
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: **LVDS Connector**

Size	Document Number	Rev
	LA-A992P	0.1

Date: Friday, March 14, 2014 Sheet 30 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: **HDMI_Conn/Level shift**

Size	Document Number	Rev
	LA-A999P	0.1

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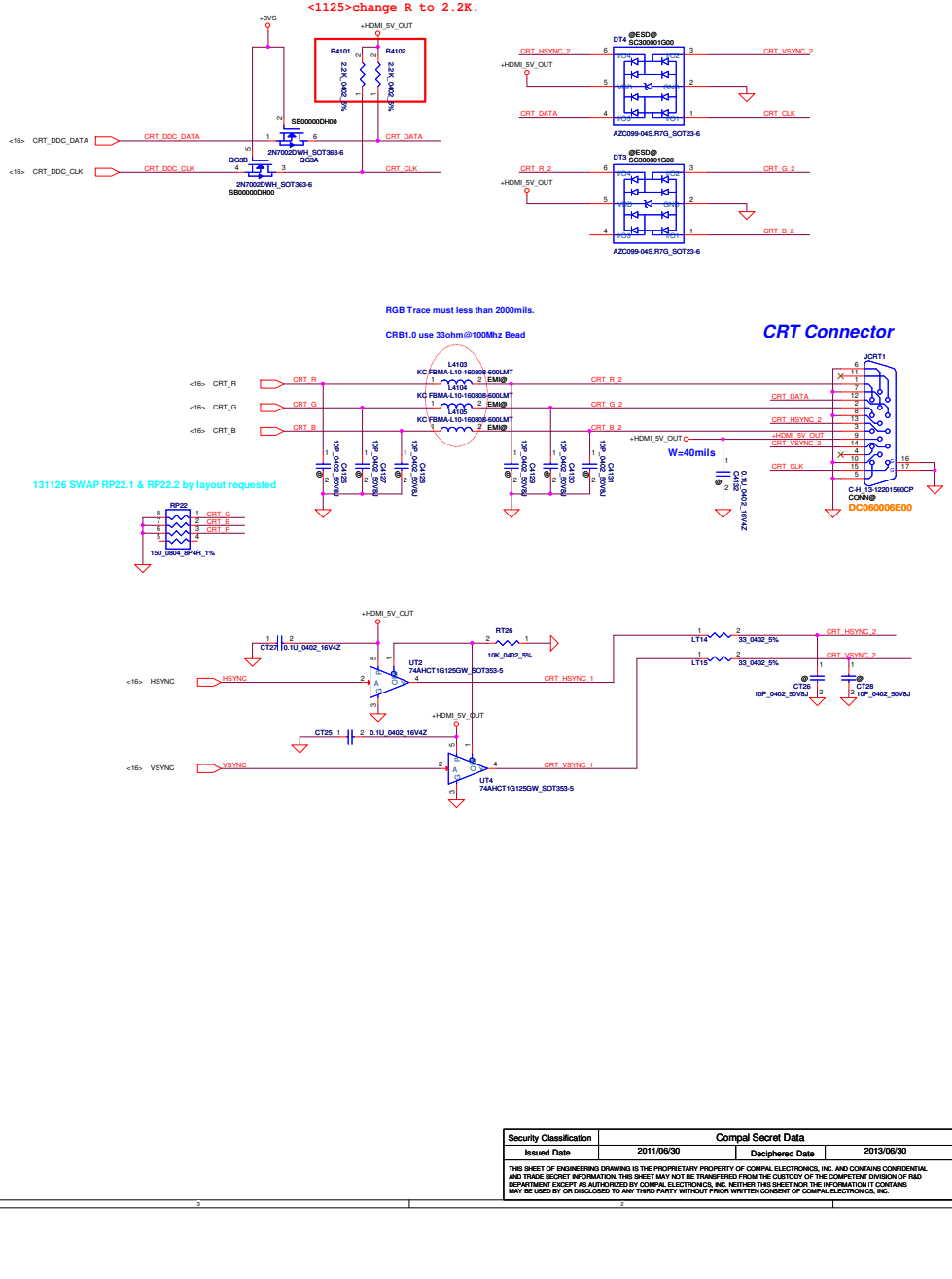

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: CRT

Size	Document Number	Rev
Custom	LA-A999P	0.1

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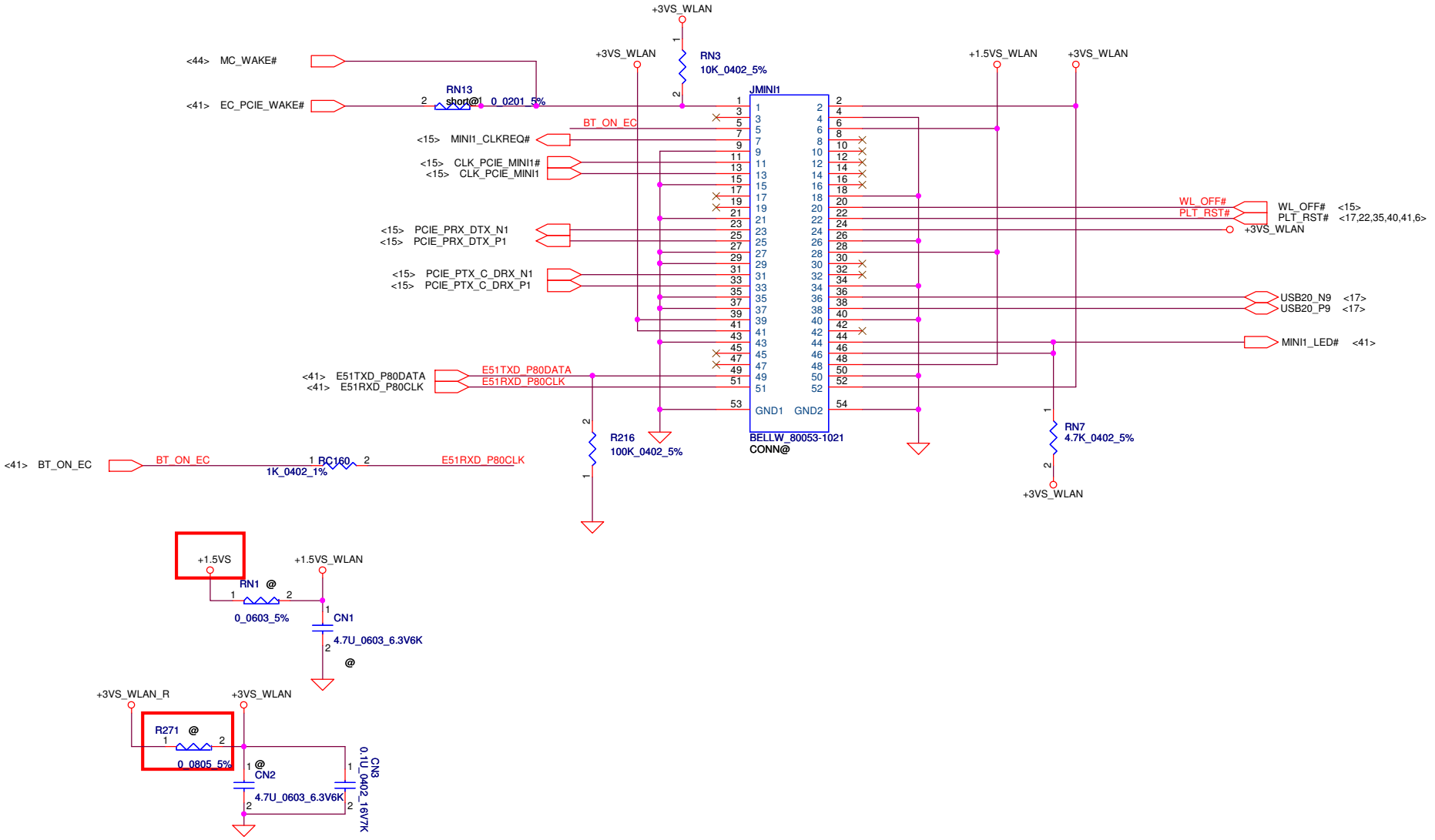

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: **WLAN**

Size	Document Number	Rev
	LA-A999P	0.1

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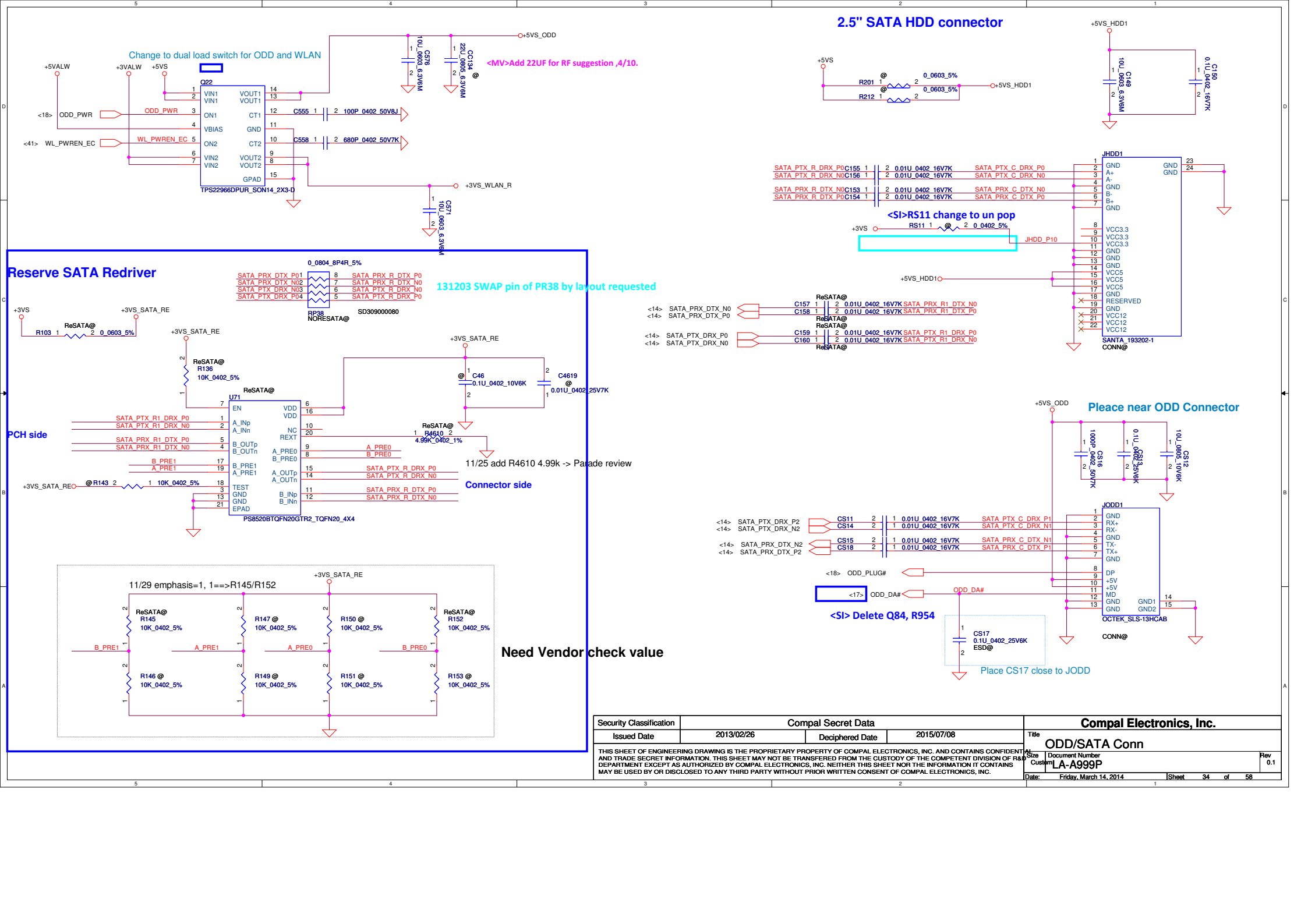

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: ODD/SATA Conn

Size	Document Number	Rev
Custom	LA-A999P	0.1

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JHW1 need to short

+LAN_VDD_3V3 Rising time need>0.5mS and <100mS

	LDO mode	Switcing mode
LL1	SMT	@
CL21	SMT	@
LL2	@	SMT
CL8	@	SMT

RTL8151G (LDO mode)

CL14 & CL15 close UL1 Pin22
CL26 & CL27 close UL1 Pin30

Place CL11~CL13 close UL1 Pin 3, 8 , 22

LL2, CL8, CL23 for 8161
CL8 & CL18 close LL2

8151/8166 Co-Lay

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

CL9 & CL5 close to UL1: Pin 11,32
CL19 close to UL1: Pin 32
CL20 close to UL1: Pin 11

CL10& CL16 close to UL1: Pin 23

SP050005L00 Footprint

(SA000063500) 10/100 8166@
(SA00005YT00) Giga 8151@

<1118>change to standard part.

(SP050003P00) 10/100 8166@
(SP050007M00) Giga 8161@

131127 SWAP Pin of DL1.2 & DL1.3 by layout requested

RTS5239

Card Reader Connector

Close to Chip

Close to Conn

RR4~RR9 close to chip
CR12~CR13 close to chip or socket

RR9 close to chip

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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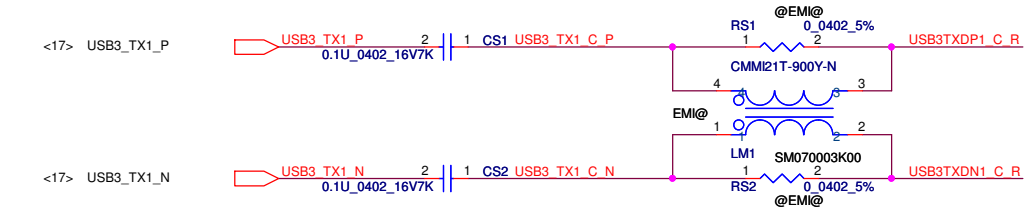
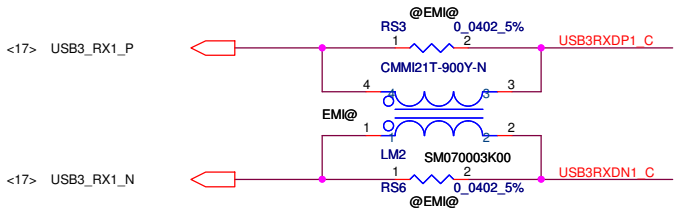
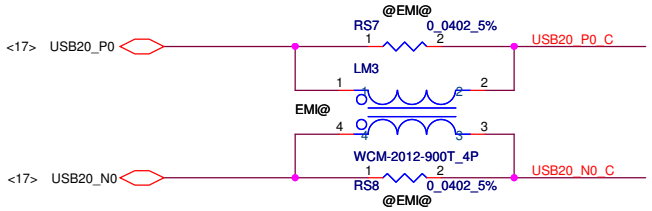
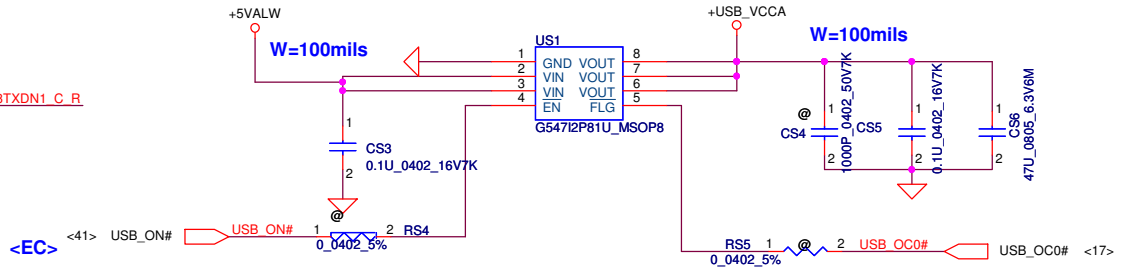
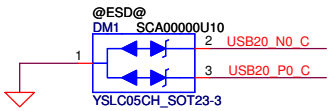


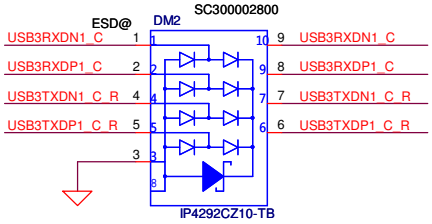




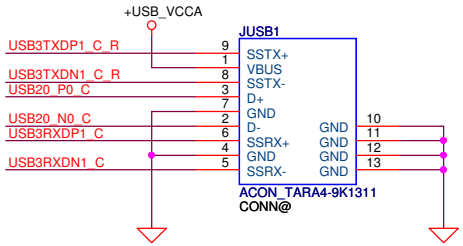
USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active



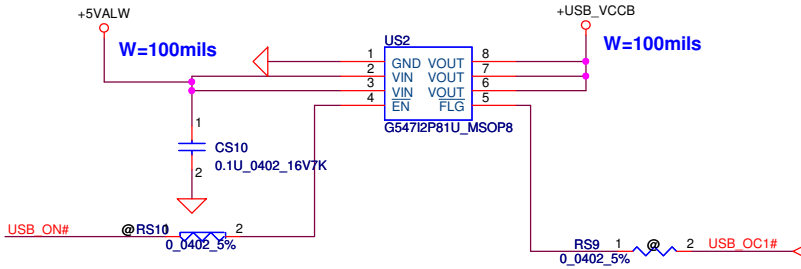




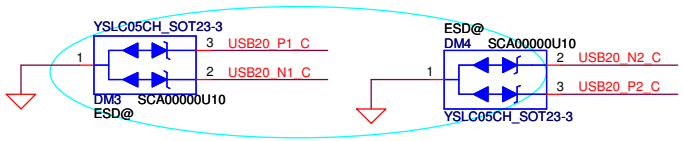
USB2.0/USB3.0 port 1



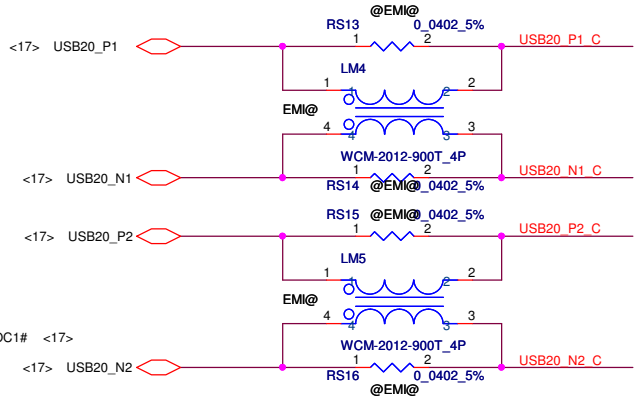
USB2.0 port x 2



131126 SWAP DM4.2 & DM4.3 by layout requested

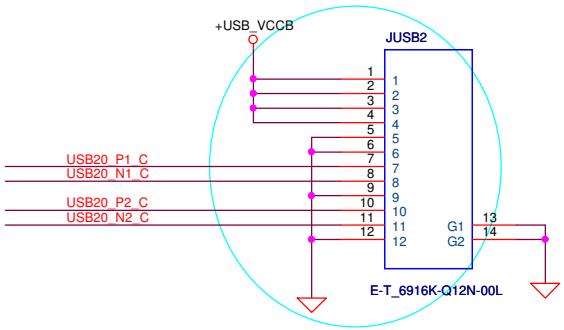


131129 change DM3 & DM4 to pop by ESD requested



131203 SWAP pin of LM5 by layout requested

131126 reverse the JUSB2, follow haswell 14"



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: USB 3.0/2.0 conn

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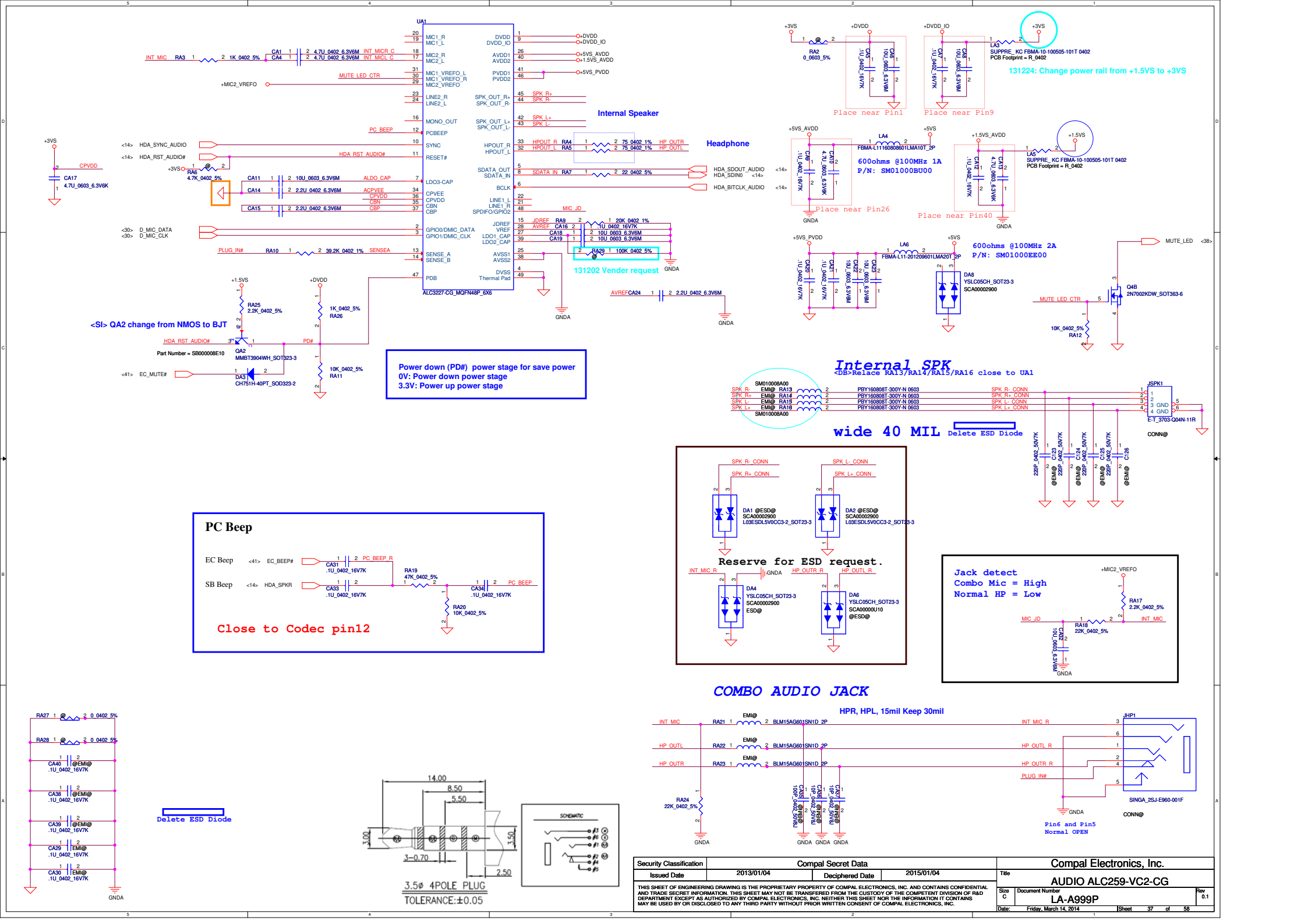

Security Classification	Compal Secret Data		
Issued Date	2013/01/04	Deciphered Date	2015/01/04

Compal Electronics, Inc.

Title: AUDIO ALC259-VC2-CG

Size	Document Number	Rev
C	LA-A999P	0.1

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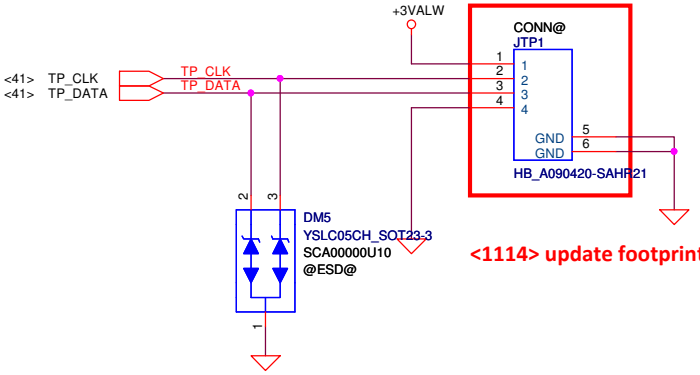
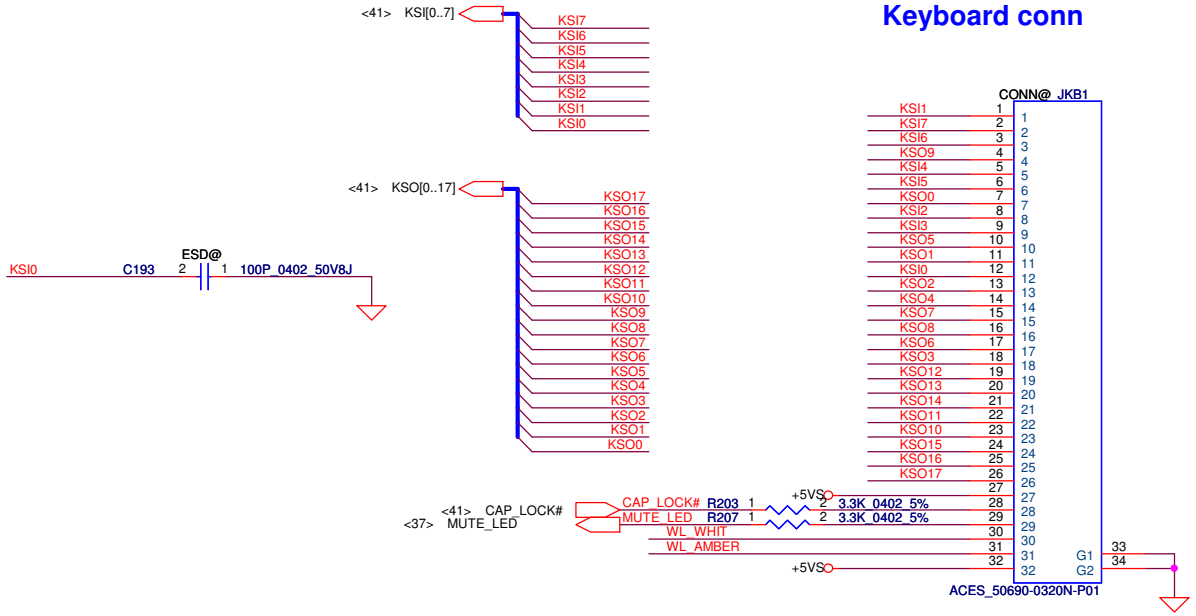
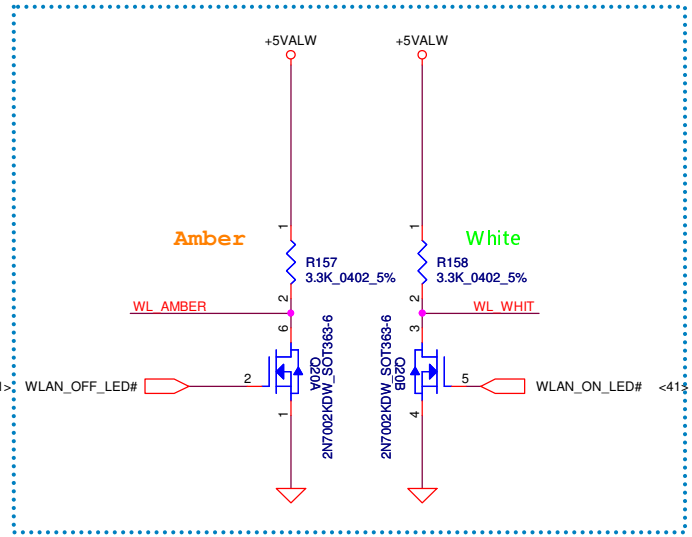
Touch pad conn

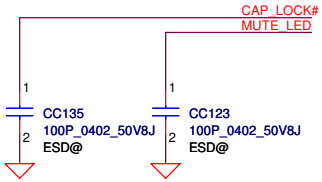


<1114> update footprint.

Keyboard conn







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Compal Electronics, Inc.

Title	KB/TP	
Size: B	Document Number: LA-A999P	Rev: 0.1
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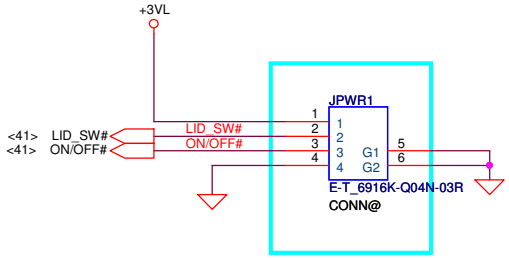
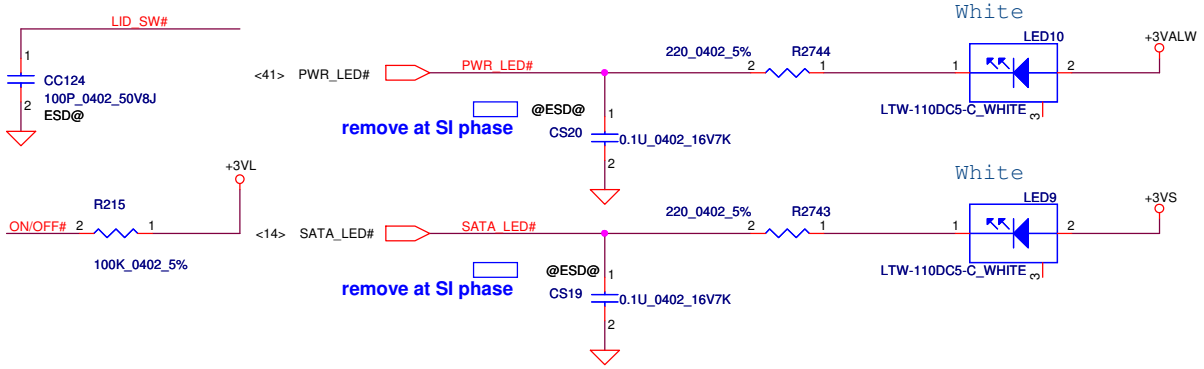
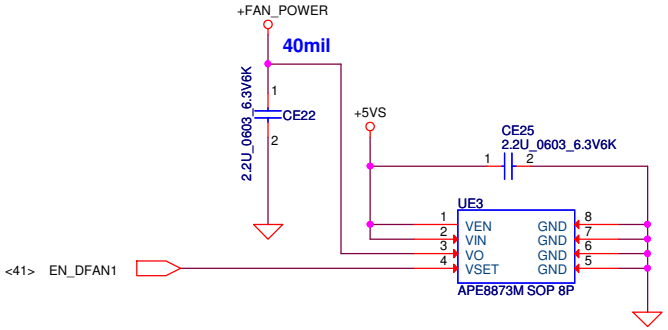
Powert Button Connector



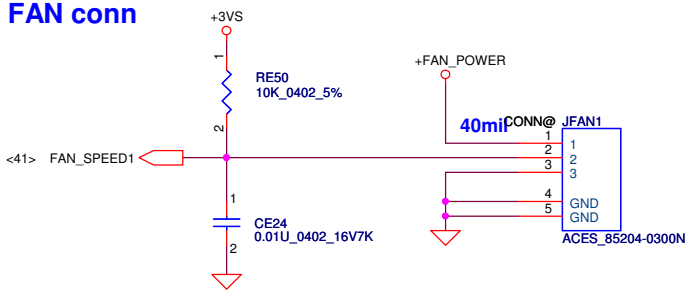


<1205> update footprint.

<SI> Del New Lid SW conn



FAN conn



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: PWRBTN/FAN

Size	Document Number	Rev
B	LA-A999P	0.1

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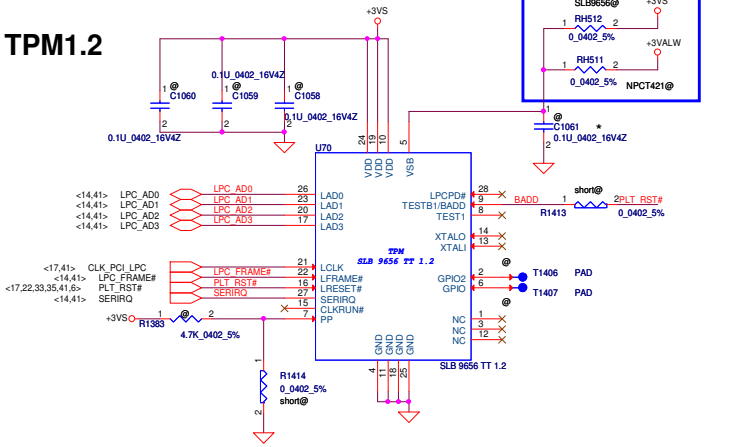
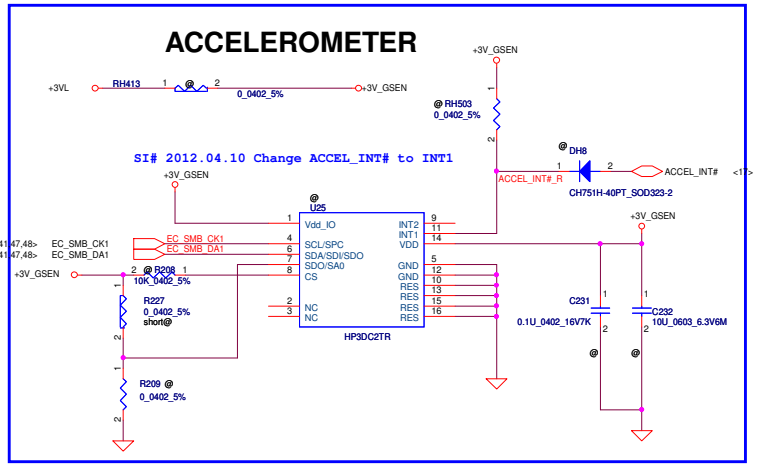
TPM1.2

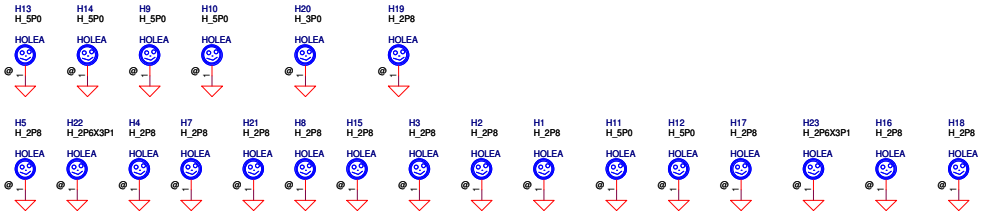


ACCELEROMETER



Screw Hole

131127 follow haswell 14"



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.			
Title: TPM/Screw hole			
Size	Document Number: LA-A999P		Rev: 0.1
Date: Friday, March 14, 2014		Sheet 40 of 58	

15"	DB	SI	PV	MV
UMA RK13	12k ohm	20K ohm	33K ohm	56K ohm
DIS RK13	160k ohm	240k ohm	330k ohm	560k ohm

14"	DB	SI	PV	MV
UMA RK13	0 ohm	15K ohm	27K ohm	43K ohm
DIS RK13	130k ohm	200k ohm	270k ohm	430k ohm

PV# 2013.01.29 Add CK4 for ESD protection

ESD@ CK4 2 1 PLT_RST# 0.1U_0402_16V7K

Board ID control

<DB>RK13 change to 160K ==>for 15" DIS

<DB>RK13 change to 12K ==>for 15" UMA

+3VL RK57 2 1 0_0603_5% CK2 0.1U_0402_16V7K CK3 0.1U_0402_16V7K

+3VALW_EC LK1 FBMA-L11-160808-800LMT_0603 +EC_VCCA CK7 0.1U_0402_16V7K ECAGND

+3V_EC_VDD RK12 short@ 0_0402_5% +3VL

+3VALW_EC RK6 100K_0402_5% BOARD_ID

DIS@ RK13 240K_0402_1% SD000001B80

UMA@ RK13 20K_0402_1% SD034200280

+3VALW_EC RK15 330K_0402_5% EC_RST# CK9 0.1U_0402_16V7K

+3VALW_EC +3VS RP7 2.2K_0804_8P4R_5%

+3VS RK36 @ 10K_0402_5% EC_SCI#

UK1

KB9012QF-A3_LQFP128_14X14

Part Number = SA00004OB30

20mil

LPC & MISC

GATEA20	1	GATEA20/GPIO00
EC_KBRST#	2	KBRST#/GPIO01
SERIRQ	3	SERIRQ
LPC_FRAME#	4	LPC_FRAME#
LPC_AD3	5	LPC_AD3
LPC_AD2	7	LPC_AD2
LPC_AD1	8	LPC_AD1
LPC_AD0	10	LPC_AD0
CLK_PCI_LPC	12	CLK_PCI_EC
PLT_RST#	13	PCIRST#/GPIO05
EC_RST#	37	EC_RST#
EC_SCI#	20	EC_SCI#/GPIO0E
PM_CLKRUN# R	38	GPIO1D

PWM Output

GPIO0F	21	GPU_HOT# <56>
BEEP#/GPIO10	23	EC_BEEP# <37>
GPIO12	26	TS_GPIO_EC <30>
ACOFF/GPIO13	27	AC_AND_CHAG <47>

AD Input

BATT_TEMP/AD0/GPIO38	63	B/I# <46,47>
AD1/GPIO39	64	BOARD_ID
ADP_I/AD2/GPIO3A	65	ADP_I
AD3/GPIO3B	66	USB_ON#
AD4/GPIO42	75	ADP_ID
IMON/AD5/GPIO43	76	ENBKL

DA Output

DAC_BRIG/GPIO3C	68	PCH_VREG_EN# R
EN_DFAN1/GPIO3D	70	EN_DFAN1 <39>
IREF/GPIO3E	71	DGPU_HOLD_RST# <17,22>
CHGVADJ/GPIO3F	72	DRAMRST_CNTRL_PCH <10,15,7>

PS2 Interface

EC_MUTE#/GPIO4A	83	EC_MUTE# <37>
USB_EN#/GPIO4B	84	PM_SLP_S4# <16>
CAP_INT#/GPIO4C	85	WLAN_OFF_LED# <38>
EAPD/GPIO4D	86	SLP_A# <16>
TP_CLK/GPIO4E	87	TP_CLK <38>
TP_DATA/GPIO4F	88	TP_DATA <38>

Int. K/B Matrix

KSI[0..7] KSO[0..17]

KSI0/GPIO30	55	KSO0
KSI1/GPIO31	56	KSO1
KSI2/GPIO32	57	KSO2
KSI3/GPIO33	58	KSO3
KSI4/GPIO34	59	KSO4
KSI5/GPIO35	60	KSO5
KSI6/GPIO36	61	KSO6
KSI7/GPIO37	62	KSO7
KSO0/GPIO20	39	KSO8
KSO1/GPIO21	40	KSO9
KSO2/GPIO22	41	KSO10
KSO3/GPIO23	42	KSO11
KSO4/GPIO24	43	KSO12
KSO5/GPIO25	44	KSO13
KSO6/GPIO26	45	KSO14
KSO7/GPIO27	46	KSO15
KSO8/GPIO28	47	KSO16
KSO9/GPIO29	48	KSO17/GPIO49
KSO10/GPIO2A	49	
KSO11/GPIO2B	50	
KSO12/GPIO2C	51	
KSO13/GPIO2D	52	
KSO14/GPIO2E	53	
KSO15/GPIO2F	54	
KSO16/GPIO48	81	
KSO17/GPIO49	82	

SPI Device Interface

CPU1.5V_S3_GATE/GPIOA00	97	EC_PME#
WOL_EN/GPIOA01	98	WL_PWREN_EC <34>
ME_EN/GPIOA02	99	HDA_SDO
VCIN0_PH/GPIOD00	109	VCIN0_PH

SPI Flash ROM

SPIDI/GPIO5B	119	EC_SPI_SO
SPIDO/GPIO5C	120	EC_SPI_SI
SPICLK/GPIO58	126	EC_SPI_CLK
SPICS#/GPIO5A	128	EC_SPI_CS#

SM Bus

EC_SMB_CK1/GPIO44	77	EC_SMB_CK1 <40,47,48>
EC_SMB_DA1/GPIO45	78	EC_SMB_DA1 <40,47,48>
EC_SMB_CK2/GPIO46	79	EC_SMB_CK2 <15,22>
EC_SMB_DA2/GPIO47	80	EC_SMB_DA2 <15,22>

GPIO

ENBKL/AD6/GPIO40	73	TOUCH_ON# <30>
PECI_KB930/AD7/GPIO41	74	EC_FB_CLAMP_TGL_REQ#
FSTCHG/GPIO50	89	AOAC_PME#
BATT_CHG_LED#/GPIO52	90	BAT_CHG_LED <46>
CAPS_LED#/GPIO53	91	CAP_LOCK#
PWR_LED#/GPIO54	92	PWR_LED#
BATT_LOW_LED#/GPIO55	93	WLAN_ON_LED# <38>
SYSON/GPIO56	95	SYSON
VR_ON/GPIO57	121	VR_ON
PM_SLP_S4#/GPIO59	127	PCH_DPWROK

GPIO

PM_SLP_S3#/GPIO04	6	PM_SLP_S3# <16>
PM_SLP_S5#/GPIO07	14	PM_SLP_S5# <16>
EC_SMI#/GPIO08	15	SUSACK# <16>
GPIO0A	16	MINI1_LED# <33>
GPIO0B	17	PCH_SUSWARN# <16>
GPIO0C	18	SLP_ME_CSW_DEV# <18>
GPIO0D	19	CPU1.5V_S3_GATE <10>
EC_INVT_PWM/GPIO11	25	EC_INVT_PWM <30>
FAN_SPEED1/GPIO14	28	FAN_SPEED1 <39>
EC_PME#/GPIO15	29	PM_SLP_SUS# <16>
EC_TX/GPIO16	30	E51TXD_P80DATA <33>
EC_RX/GPIO17	31	E51RXD_P80CLK <33>
PCH_PWROK/GPIO18	32	PCH_PWROK <16>
SUSP_LED#/GPIO19	34	AC_LED# <46>
NUM_LED#/GPIO1A	36	DGPU_PWR_EN <17,25,56>

GPO

EC_RSMRST#/GPXIOA03	100	PCH_RSMRST#
EC_LID_OUT#/GPXIOA04	101	
PROCHOT_IN/GPXIOA05	102	VCIN1_PH
H_PROCHOT#_EC/GPXIOA06	103	H_PROCHOT#_EC
VCOUT0_PH/GPXIOA07	104	MAINPWON
BKOFF#/GPXIOA08	105	EC_BKOFF#
PBTN_OUT#/GPXIOA09	106	PBTN_OUT#
PCH_APWROK/GPXIOA10	107	PCH_PWR_EN
SA_PGOOD/GPXIOA11	108	SA_PGOOD

GPI

AC_IN/GPXIOD01	110	EC_ACIN
EC_ON/GPXIOD02	112	EC_ON <49>
ON/OFF#/GPXIOD03	114	ON/OFF# <39>
LID_SW#/GPXIOD04	115	LID_SW# <39>
SUSP#/GPXIOD05	116	SUSP#
GPXIOD06	117	NMI_DBG#
PECI_KB9012/GPXIOD07	118	EC_PECI RK34 1 2 43_0402_1% H_PECI <18,6>

GPU_THERMAL_DET#	122	<22> GPU_THERMAL_DET#
BT_ON_EC	123	<33> BT_ON_EC
XCLKI/GPIO5D		
XCLKO/GPIO5E		
V18R	124	+V18R

CK17 1 2 4.7U_0603_6.3V6K

LK2 ECAGND 2 1 FBMA-L11-160808-800LMT_0603 ECAGND <46>

@RK49 100K_0402_5% PCH_DPWROK

@RK50 100K_0402_5% PCH_PWROK

+3VALW_EC RK18 10K_0402_5% NMI_DBG# DK2 CH751H-40PT_SOD323-2 NMI_DBG#_CPU <18>

EC_ACIN DK1 CH751H-40PT_SOD323-2 ACIN <16,46,47,48>

CK8 2 1 100P_0402_50V8J

short@ RK17 0_0402_5% <53> VR_HOT# PROCHOT# <46,6>

<46> H_PROCHOT#_EC Q10B 2N7002DWH_SOT363-6

<PWR>

<1120>Combine with Q10.

short@ RK53 2 0_0201_5% PCH_VREG_EN# <20>

<1118> Remove SYS_PWROK.

+3VALW_EC EC_FB_CLAMP_TGL_REQ# RK60 1 DIS@ 2 10K_0402_5%

<SI> Update Pin119 and Pin120 net name

+3VALW TP_CLK RK2 4.7K_0402_5% TP_DATA RK4 4.7K_0402_5%

100P_0402_50V8J CK10 2 1 ECAGND EC_LID_OUT# <18>

+3VL RP8 100K_0804_8P4R_5% RK51 VR_ON 100K_0402_5%

<1112> Add it.

+3VALW_EC LID_SW# RK44 2 1 47K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: EC ENE-KB9012

Size: Custom | Document Number: LA-A999P | Rev: 0.1

Date: Friday, March 14, 2014 | Sheet 41 of 58

Green CLK no reserved.

BOM control

Platform	Silego P/N	Compal PN	25MHz(A)	32.768KHz	25MHz(B)	27MHz	8MHz	Remark
Intel CRV UMA	SLG3NB244VTR	SA000063300	1	1	1	X	X	GCLKUMA@
Intel CRV Dis	SLG3NB304VTR	SA000057I00	1	1	1	1	X	GCLKDIS@

Base on A32 32.768KHz use 10ppm, G-CLK 25MHz X'TAL use 10ppm.

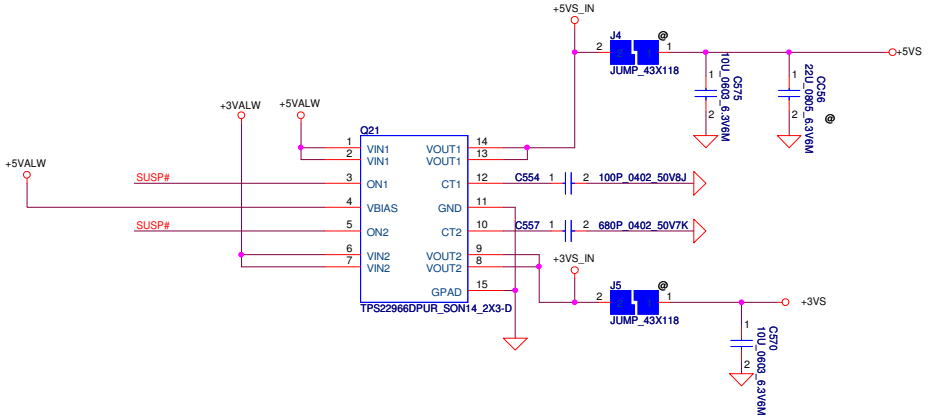
Security Classification	Compal Secret Data		
Issued Date	2013/06/10	Deciphered Date	2014/07/01

Compal Electronics, Inc.

Title: GCLK

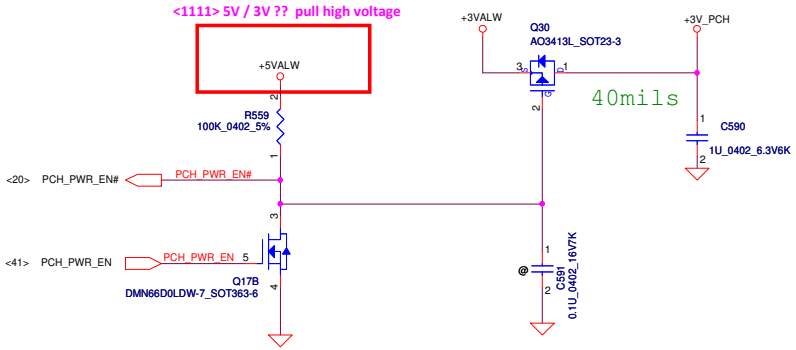
Size | Document Number: LA-A999P | Rev: 0.1

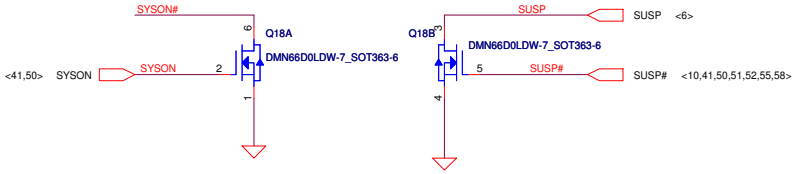
Date: Friday, March 14, 2014 | Sheet 31 of 58

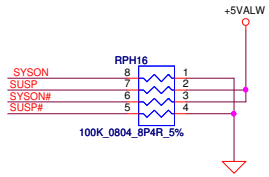


+1.5V to +1.5VS

<1111> Remove +1.5VS DCDC.

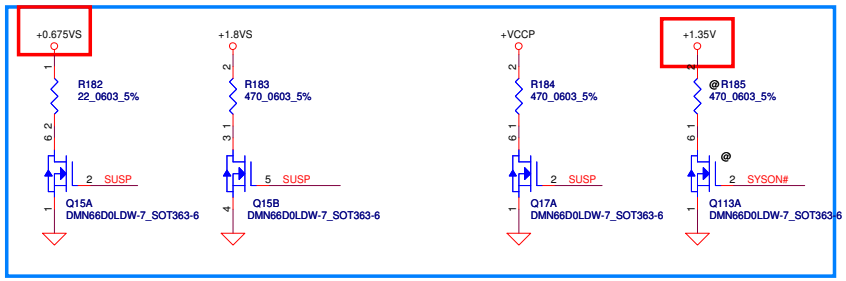






AO4430L
VGS Max=+/- 20V
VGS(Th) max=2.5V

Rds Max=5.5m @VGS=10V
Rds Max=7.5m @VGS=4.5V



AO4430L
VGS Max=+/- 20V
VGS(Th) max=2.5V

Rds Max=5.5m @VGS=10V
Rds Max=7.5m @VGS=4.5V

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-A999P	0.1

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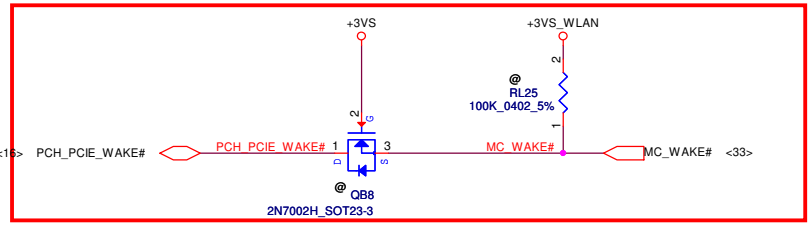
NGFF and WLAN



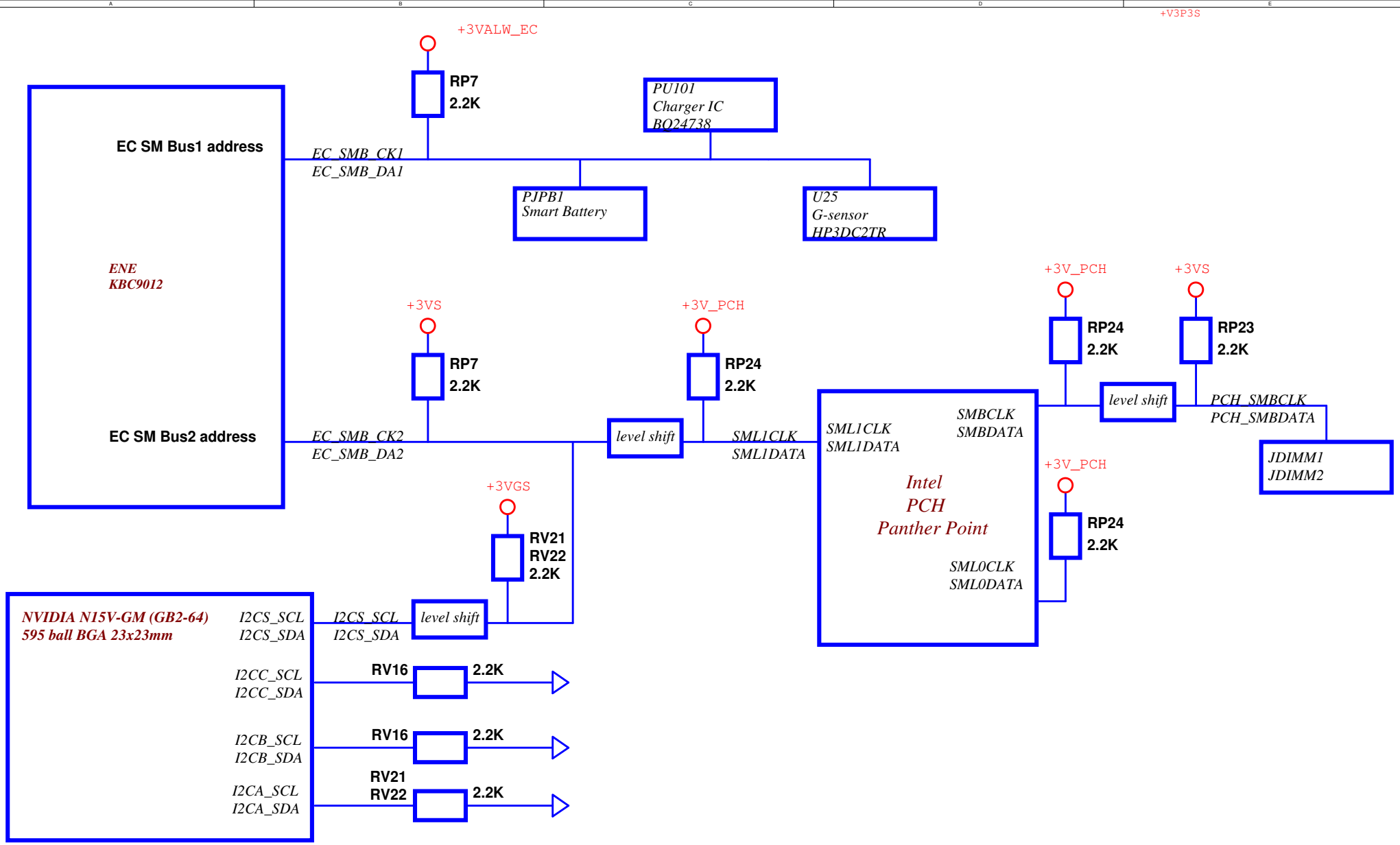
PV# 2013.01.23 Add QB8 abd RL25 to support OBFF

PV# 2013.02.22 Unpop QB4 and RL23 for not support OBFF

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: WAKE and RST-1

Size	Document Number	Rev
Custom	LA-A999P	0.1

Date: Friday, March 14, 2014 Sheet 44 of 58

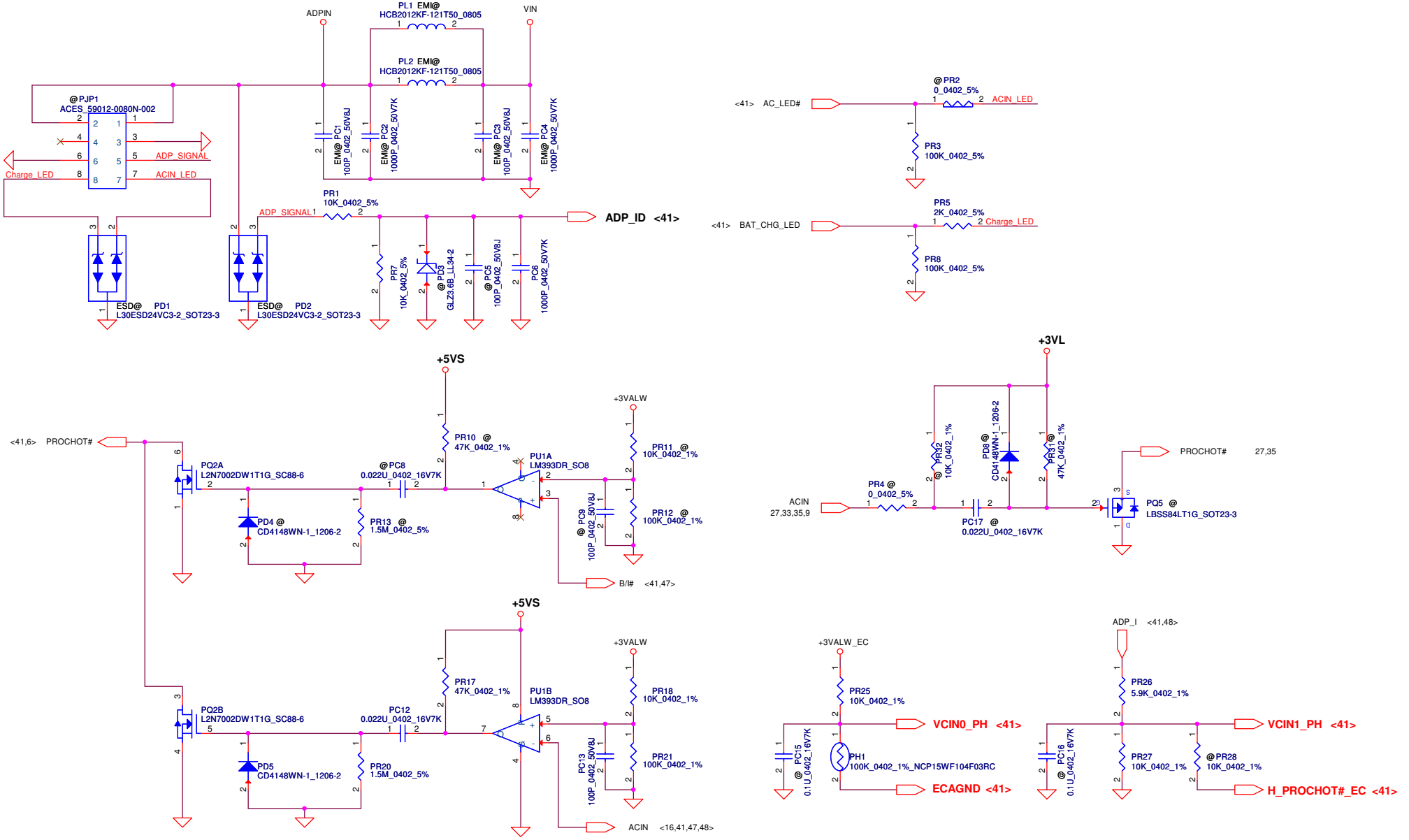


Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: I2C Mapping

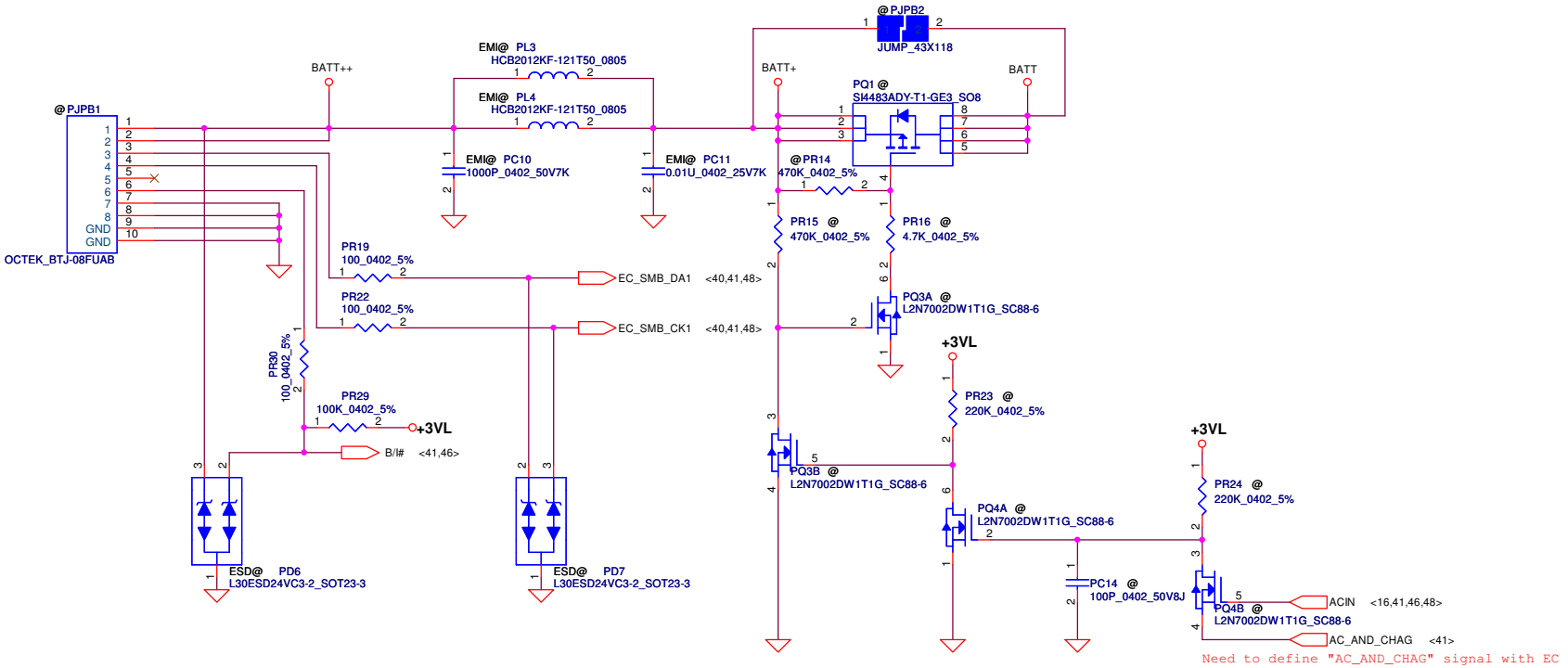
Size: Custom	Document Number: LA-A999P	Rev: 0.1
Date: Friday, March 14, 2014	Sheet 45 of 58	



Security Classification	Compal Secret Data		
Issued Date	2013/08/07	Deciphered Date	2016/08/06

Compal Electronics, Inc.

Title	***PWR-DC Conn***	
Size	Document Number **LA-A998P**	Rev 0.2
Date: Friday, March 14, 2014	Sheet 46 of 58	



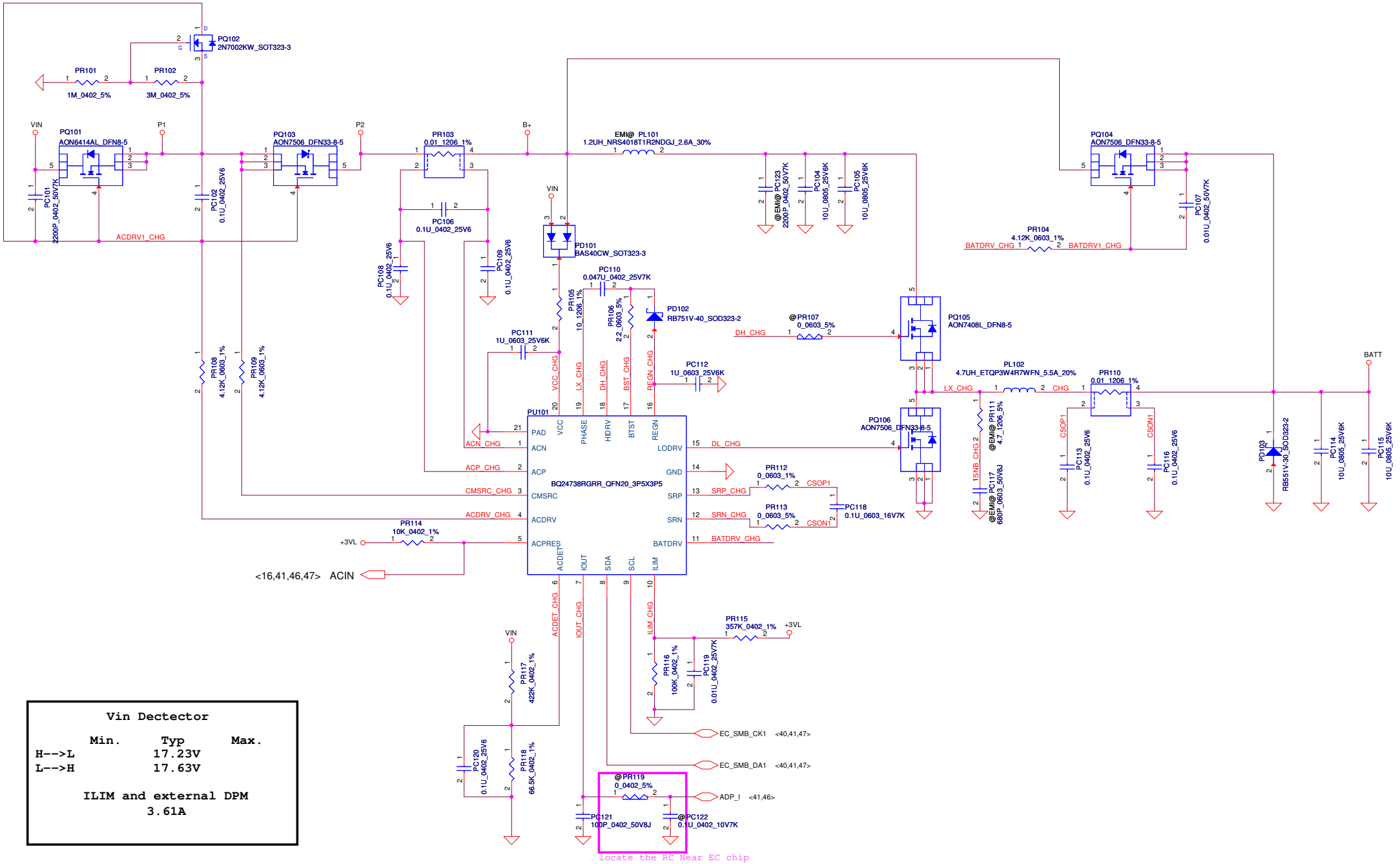
Security Classification	Compal Secret Data		
Issued Date	2013/08/07	Deciphered Date	2016/08/06

Compal Electronics, Inc.

Title: ***PWR-BATT Conn***

Size | Document Number: **LA-A998P** | Rev: 0.2

Date: Friday, March 14, 2014 | Sheet 47 of 58



Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	

ILIM and external DPM
3.61A

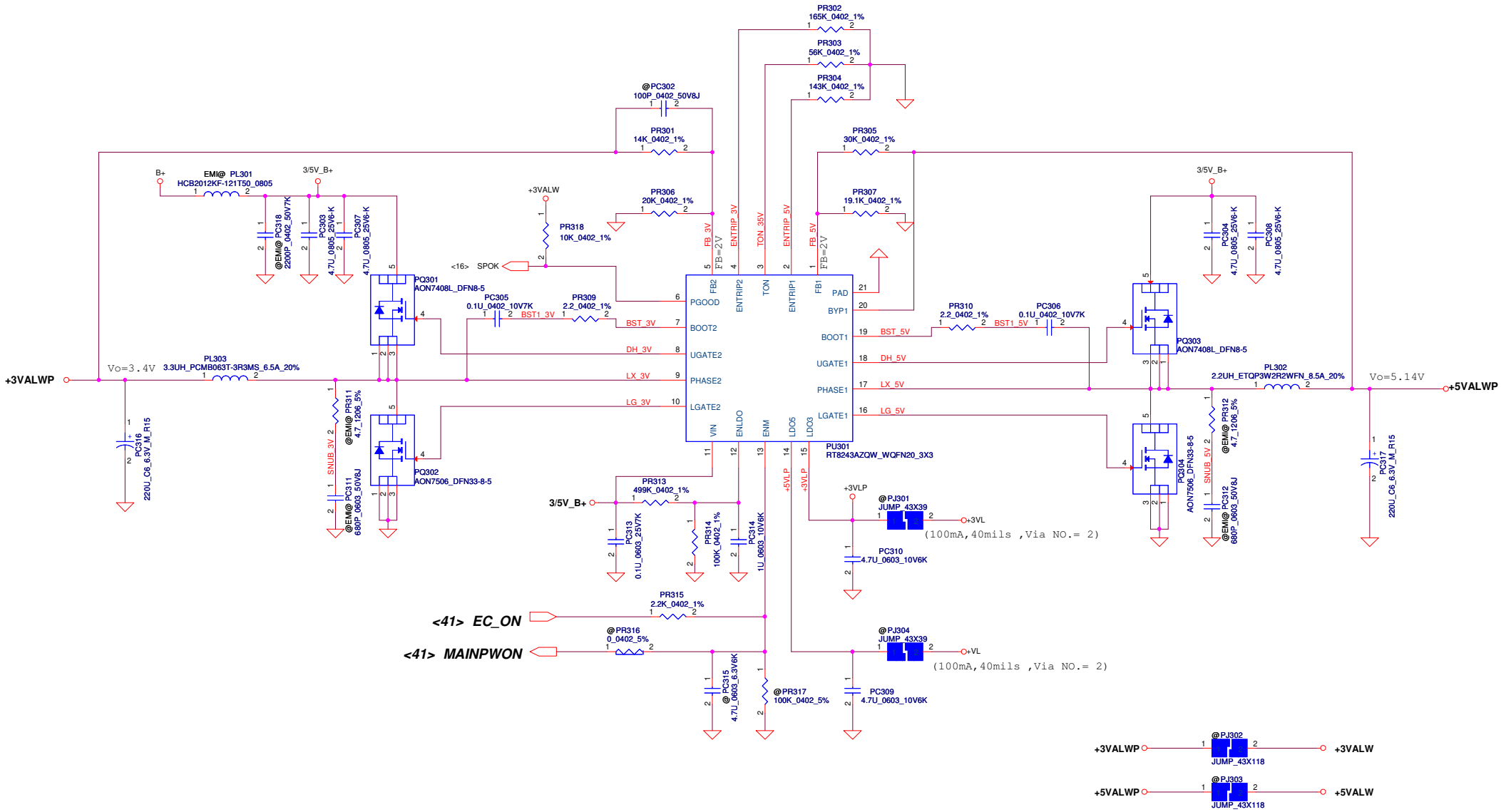
Security Classification	Compal Secret Data		
Issued Date	2013/08/07	Deciphered Date	2016/08/06

Compal Electronics, Inc.

Title: *PWR-CHARGER*

Size: Custom | Document Number: LA-A998P | Rev: 0.2

Date: | Sheet 48 of 58



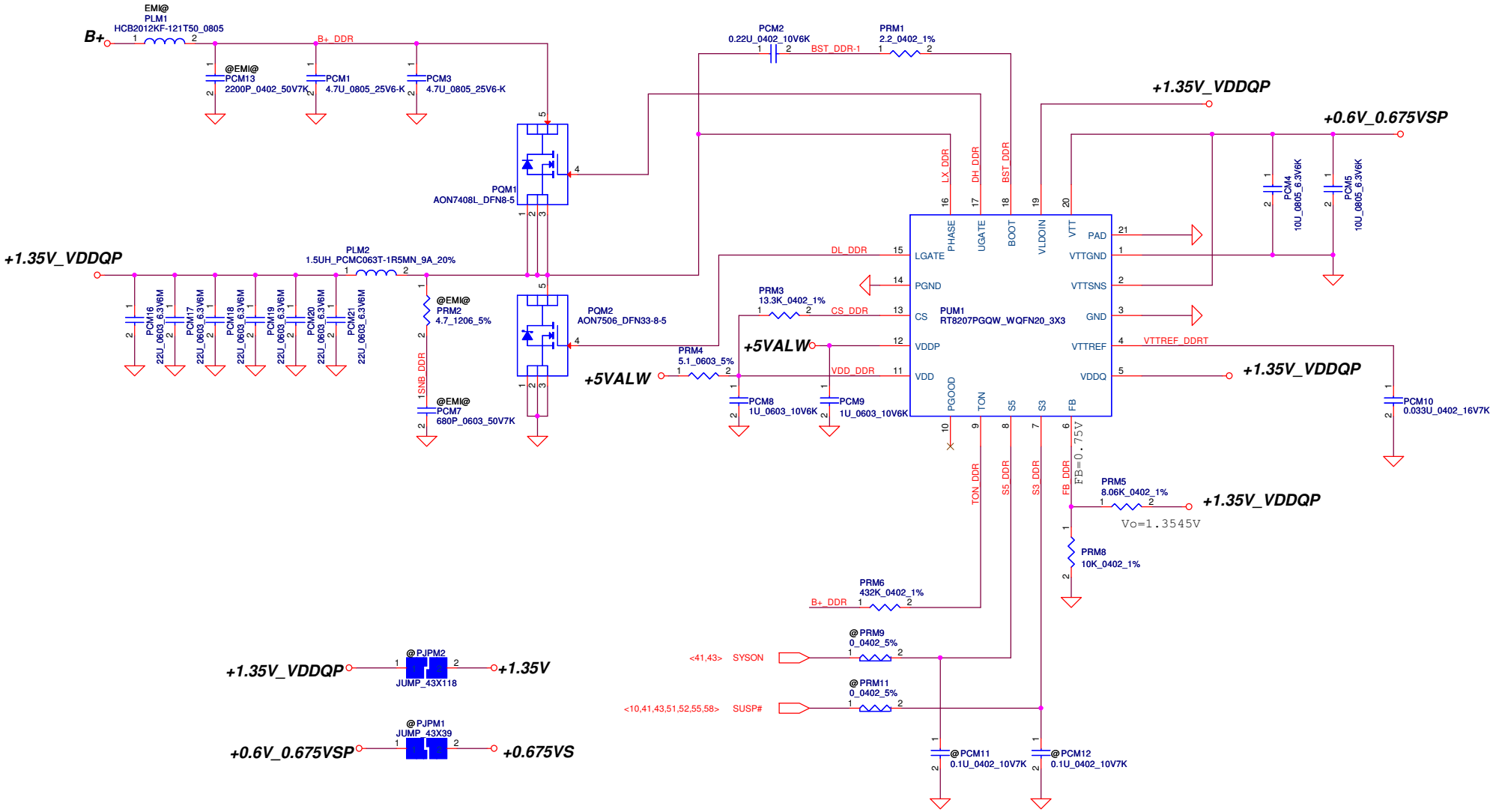
Security Classification	Compal Secret Data		
Issued Date	2013/08/07	Deciphered Date	2016/08/06

Compal Electronics, Inc.

Title: *PWR-3VALW/5VALW*

Size: Custom | Document Number: LA-A998P | Rev: 0.2

Date: | Sheet 49 of 58



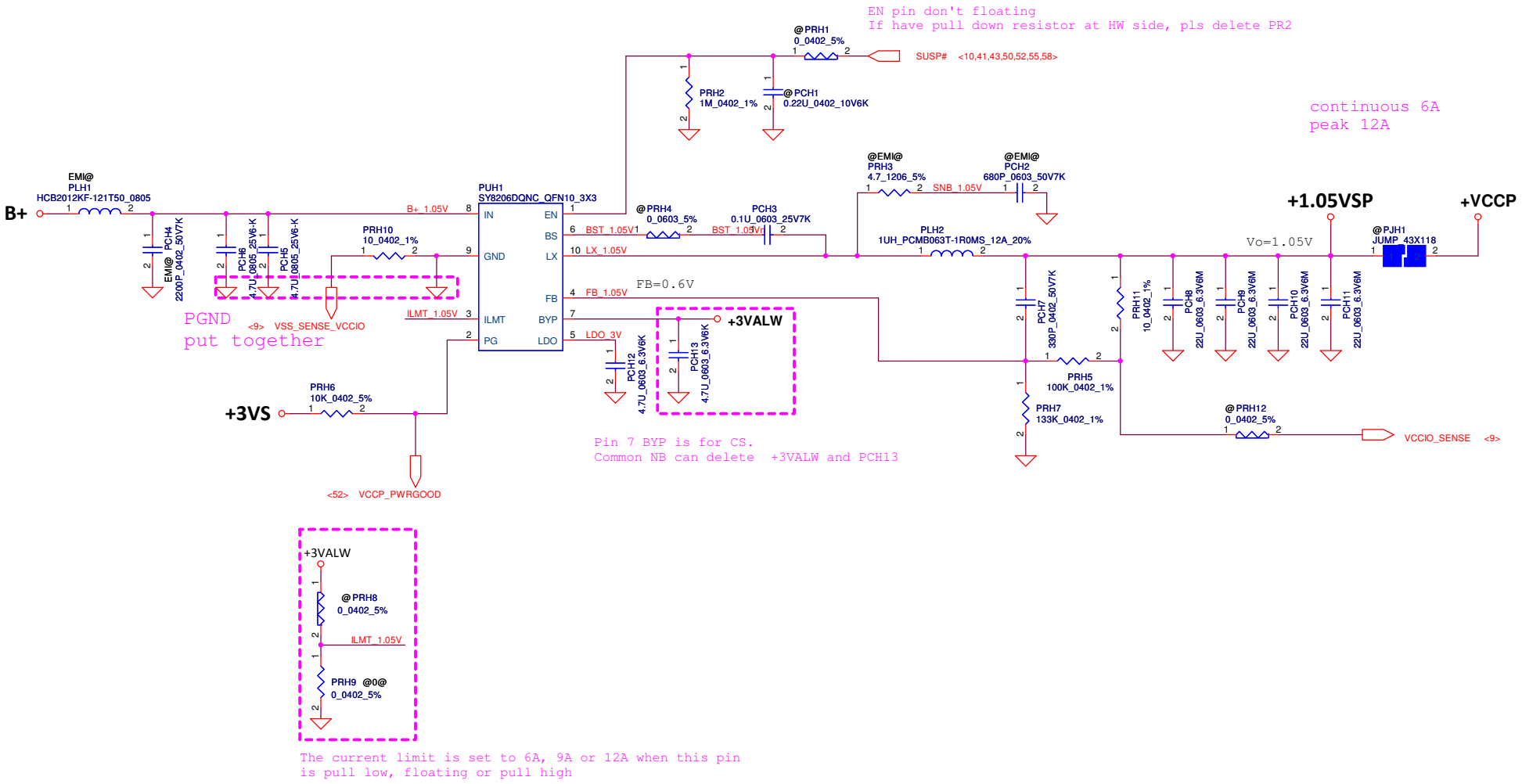
Security Classification	Compal Secret Data		
Issued Date	2013/08/07	Deciphered Date	2016/08/06

Compal Electronics, Inc.

Title: PWR-1.35V/0.675VS

Size: Custom | Document Number: LA-A998P | Rev: 0.2

Date: Friday, March 14, 2014 | Sheet 50 of 58



Security Classification	Compal Secret Data		
Issued Date	2013/08/07	Deciphered Date	2016/08/06

Compal Electronics, Inc.

Title: PWR-1.05VS_VCCP

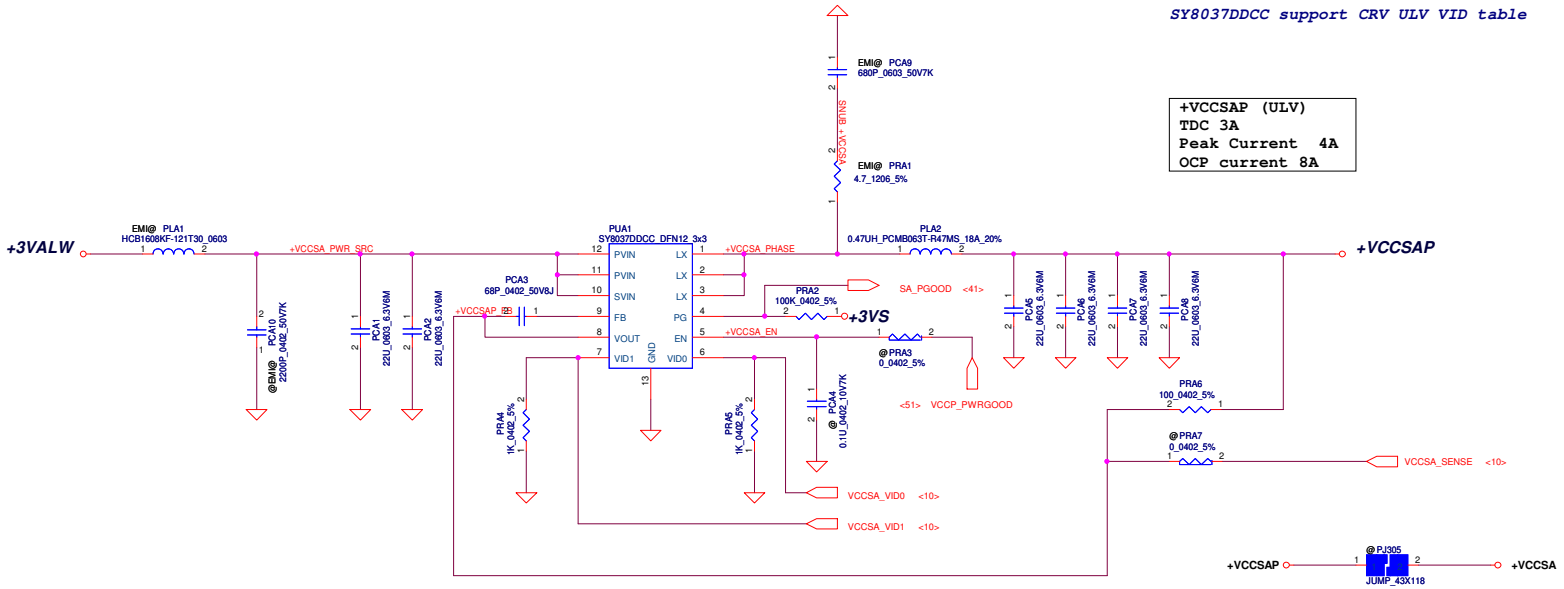
Size: Custom | Document Number: LA-A998P | Rev: 0.2

Date: Friday, March 14, 2014 | Sheet 51 of 58

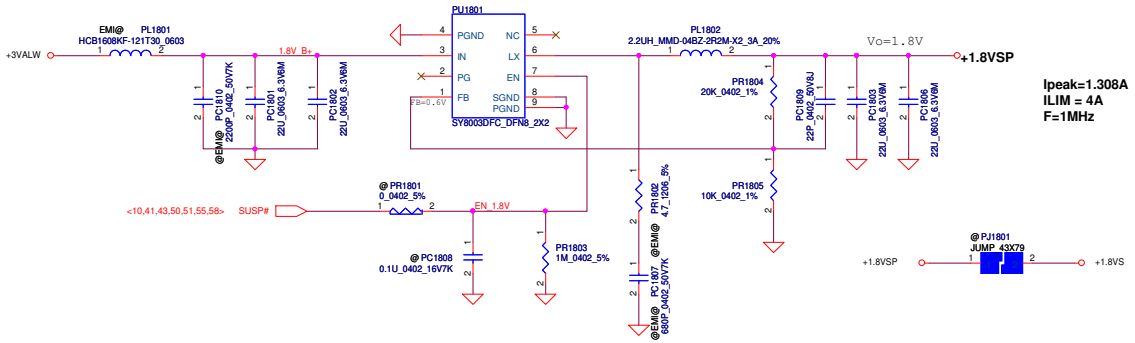
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

SY8037DDCC support CRV ULV VID table

+VCCSAP (ULV)
TDC 3A
Peak Current 4A
OCP current 8A



The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



Ipeak=1.308A
ILIM = 4A
F=1MHz

Security Classification	Compal Secret Data		
Issued Date	2013/08/07	Deciphered Date	2016/08/06

Compal Electronics, Inc.

Title: PWR-VCCSAP/1.8VSP

Size	Document Number	Rev
C	LA-A998P	0.2

Date: Friday, March 14, 2014 Sheet 52 of 58

Design Note
This circuit is for ULV 1+1 17W.
CPU: IccMax=33A, TDC=16A(TDP NOM)
Loadline: -2.9 m V/A
Output Cap. follow Intel PDDG
330uF/9m*1, 560uF/4.5m*1 22uF_0603*12, 2.2uF_0402*16
GFX(GT2): IccMax=33A, TDC=21.5A
Loadline: -3.9 m V/A
Output Cap. follow Intel PDDG
560uF/4.5m*1, 22uF_0603*6, 10uF_0603*6 , 1uF_0402*11

Close GFX choke

Close GFX L/S MOS

Close CPU L/S MOS

Close CPU choke

PRZ15 and PRG5
27.4K ohm for 100 degree
61.9K ohm for 110 degree

For VR_HOT#, already pull high at power side.

VDD source use +5VS and PGOOD source use +3VS
Please confirm power on and down sequence, make sure VGATE after CPU_CORE on.

Layout Note
Reduce Acoustic Noise
1. The AL bulk capacitor of B+ should be very close to CPU_CORE MOSFET.
2. Input ceramic caps must place on symmetry same location on top side and bottom side.

OCP setting=39.9~44.99A
0.22uH DCR= 0.97+-5% m ohm, Idc~Isat= 25~34A

OCP setting=39.9~44.99A
0.22uH DCR= 0.97+-5% m ohm, Idc~Isat= 25~34A

Cn = L/((Rntcnet*Rsum)/(Rntcnet+Rsum))*DCR)
If Cn is correctly selected, when the load current has a square change, the output voltage also has a square response.

Layout Note
SVID routing
1. Alert# signal must be routed between the Clock and Date lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Date.
2. SVID spacing requirement is 18mils(0.475mm).
3. Maximum total microstrip routing length of each SVID signal must not exceed 6000mils(152.4mm).
4. The SVID bus must be ground reference, It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.
5. Avoid routing under noisy circuit, e.g. switch node , Gate driver, B+, Vin, high speed signal.
6. When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.

Security Classification	Compal Secret Data		
Issued Date	2013/08/07	Deciphered Date	2016/08/06

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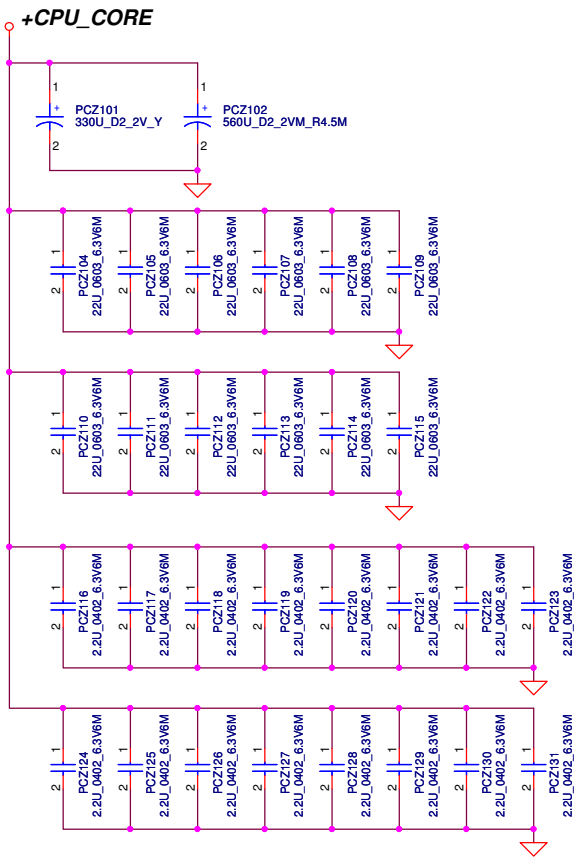
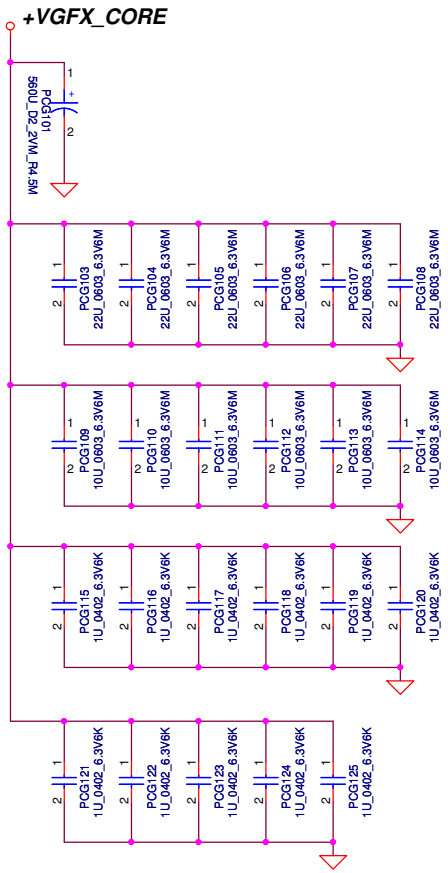
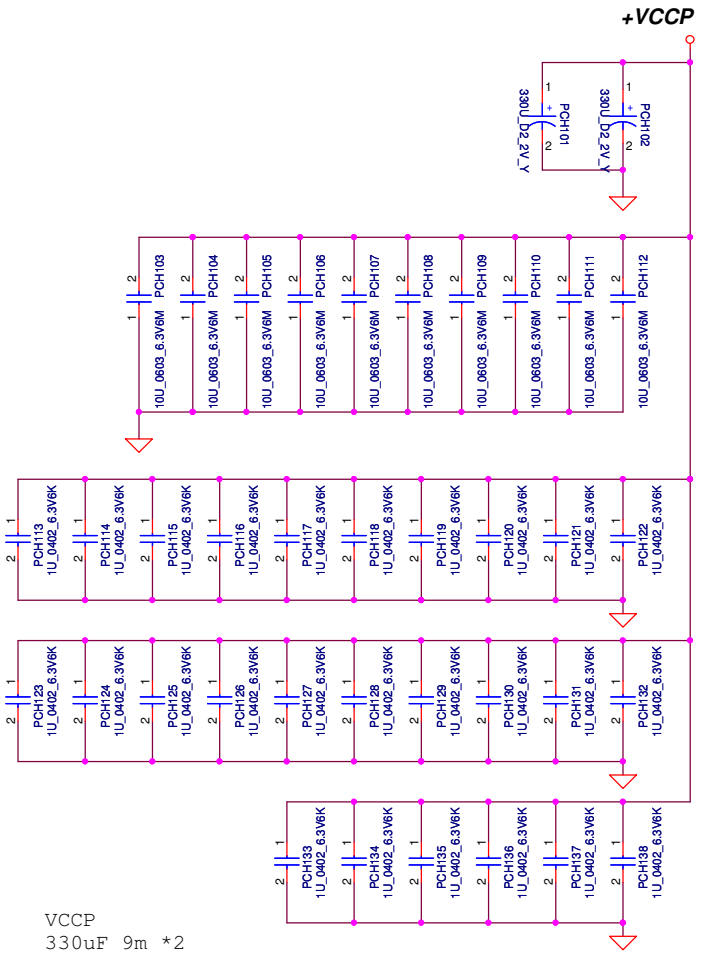
Compal Electronics, Inc.
Title: PWR-CPU_CORE/GFX_CORE
Document Number: LA-A998P
Rev: 0.2
Date: Friday, March 14, 2014 Sheet 53 of 58



CPU_CORE
330uF 9m *1
560uF 4.5m *1
22uF 0603 *12
2.2uF 0402 *16



GFX_CORE
560uF 4.5m *1
22uF 0603 *6
10uF 0603 *6
1uF 0402 *11



VCCP
330uF 9m *2
10uF 0603 *10
1uF 0402 *26

Security Classification	Compal Secret Data		
Issued Date	2013/08/07	Deciphered Date	2016/08/06

Compal Electronics, Inc.

Title: PWR-CPU_CORE DECOUPLING

Size	Document Number	Rev
	LA-A998P QFKAA	0.2

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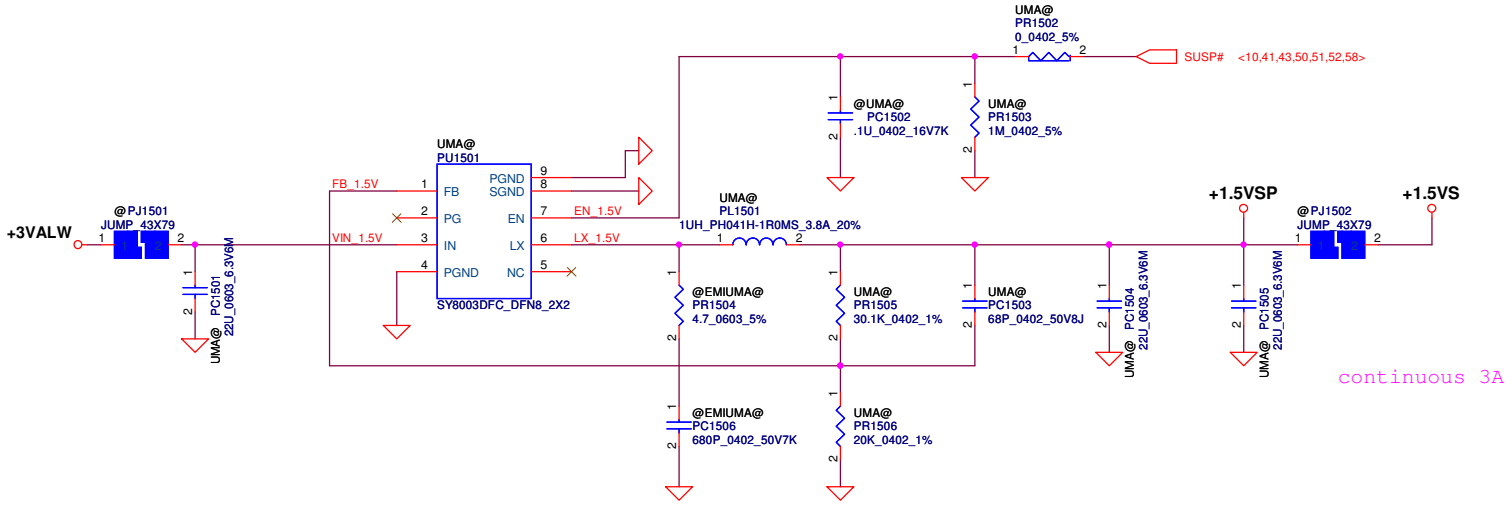

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Title	***PWR-1.5VS***	
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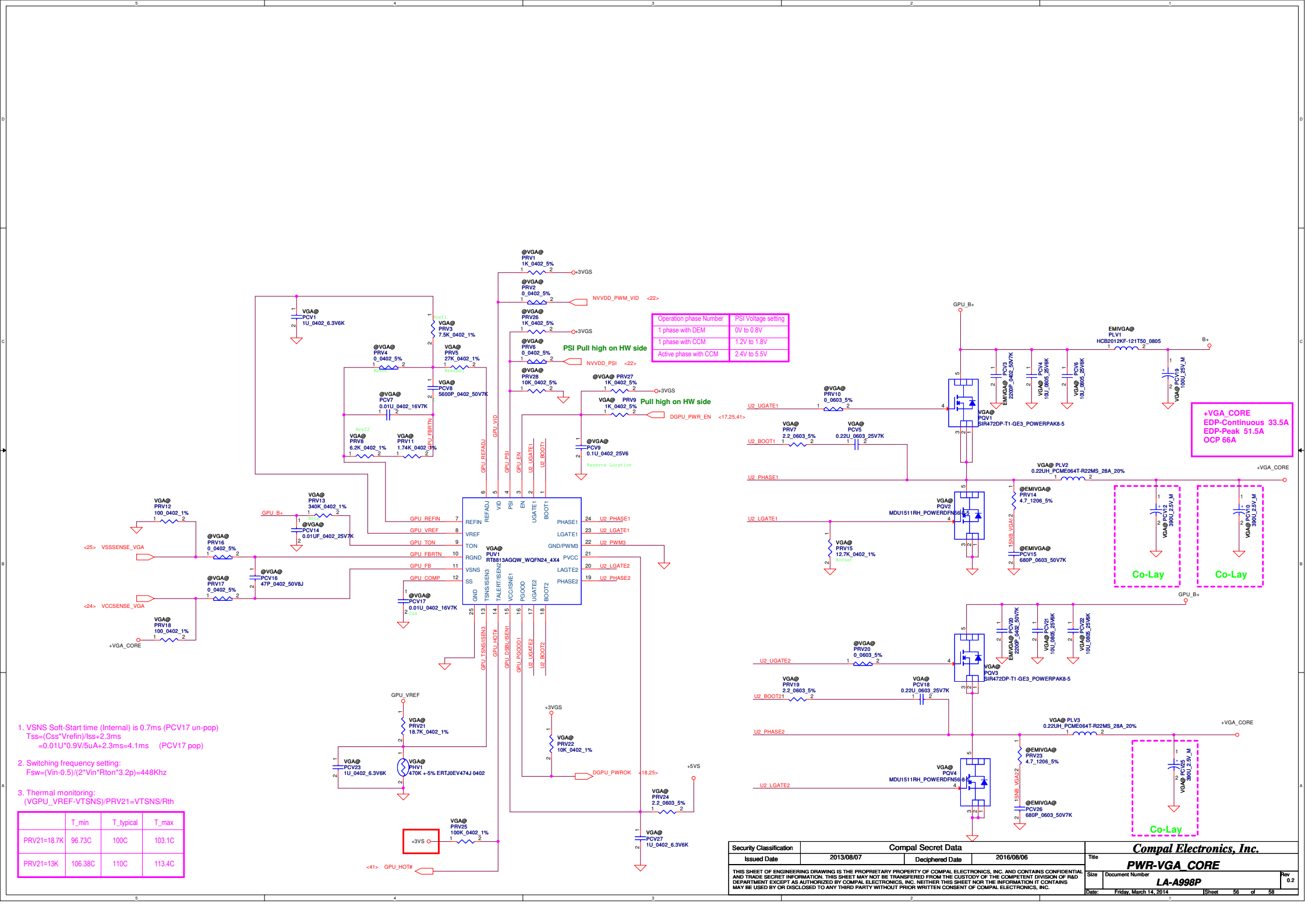
PSI Pull high on HW side
Pull high on HW side
Operation phase Number | PSI Voltage setting
1 phase with DEM | 0V to 0.8V
1 phase with CCM | 1.2V to 1.8V
Active phase with CCM | 2.4V to 5.5V
+VGA_CORE
EDP-Continuous 33.5A
EDP-Peak 51.5A
OCP 66A
Co-Lay
Co-Lay
Co-Lay
1. VSNS Soft-Start time (Internal) is 0.7ms (PCV17 un-pop)
Tss=(Css*Vrefin)/Iss+2.3ms
=0.01U*0.9V/5uA+2.3ms=4.1ms (PCV17 pop)
2. Switching frequency setting:
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=448Khz
3. Thermal monitoring:
(VGPU_VREF-VTSNS)/PRV21=VTSNS/Rth
T_min | T_typical | T_max
PRV21=18.7K | 96.73C | 100C | 103.1C
PRV21=13K | 106.38C | 110C | 113.4C
Security Classification | Compal Secret Data
Issued Date | 2013/08/07 | Deciphered Date | 2016/08/06
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Compal Electronics, Inc.
Title
PWR-VGA_CORE
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+VGA_CORE

PLACE UNDER GPU

VGA@ PCV51 4.7U_0603_6.3V6M
VGA@ PCV52 4.7U_0603_6.3V6M
VGA@ PCV53 4.7U_0603_6.3V6M
VGA@ PCV54 4.7U_0603_6.3V6M
VGA@ PCV55 4.7U_0603_6.3V6M
VGA@ PCV56 4.7U_0603_6.3V6M
VGA@ PCV57 4.7U_0603_6.3V6M
VGA@ PCV58 4.7U_0603_6.3V6M
VGA@ PCV59 4.7U_0603_6.3V6M
VGA@ PCV60 4.7U_0603_6.3V6M
VGA@ PCV61 1U_0402_6.3V6K
VGA@ PCV62 1U_0402_6.3V6K
VGA@ PCV63 1U_0402_6.3V6K
VGA@ PCV64 1U_0402_6.3V6K

PLACE NEAR GPU

VGA@ PCV65 4.7U_0603_6.3V6K
VGA@ PCV66 4.7U_0603_6.3V6K
VGA@ PCV67 4.7U_0603_6.3V6K
VGA@ PCV68 4.7U_0603_6.3V6K
VGA@ PCV69 4.7U_0603_6.3V6K
VGA@ PCV70 22U_0603_6.3V6M
VGA@ PCV71 47U_0805_6.3V6M

Security Classification	Compal Secret Data		
Issued Date	2013/08/07	Deciphered Date	2016/08/06

Compal Electronics, Inc.

Title: PWR-VGA CHIP DECOUPLING

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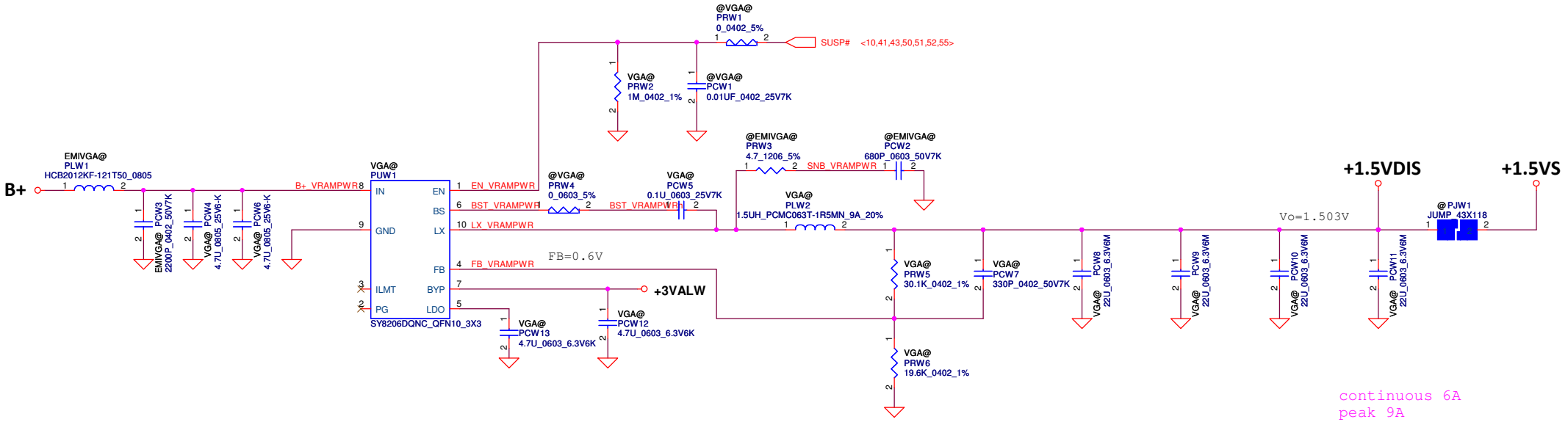

Security Classification	Compal Secret Data		
Issued Date	2013/08/07	Deciphered Date	2016/08/06

Compal Electronics, Inc.

Title: **PWR-VRAM Power**

Size	Document Number	Rev
Custom	LA-A998P	0.2

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