

Compal Confidential

ULC AMD M/B LA-A996P DIS Schematics Document

AMD APU Beema/Kabini FT3 + ATI SUN LE + DDR3

Project Code : ZSO51

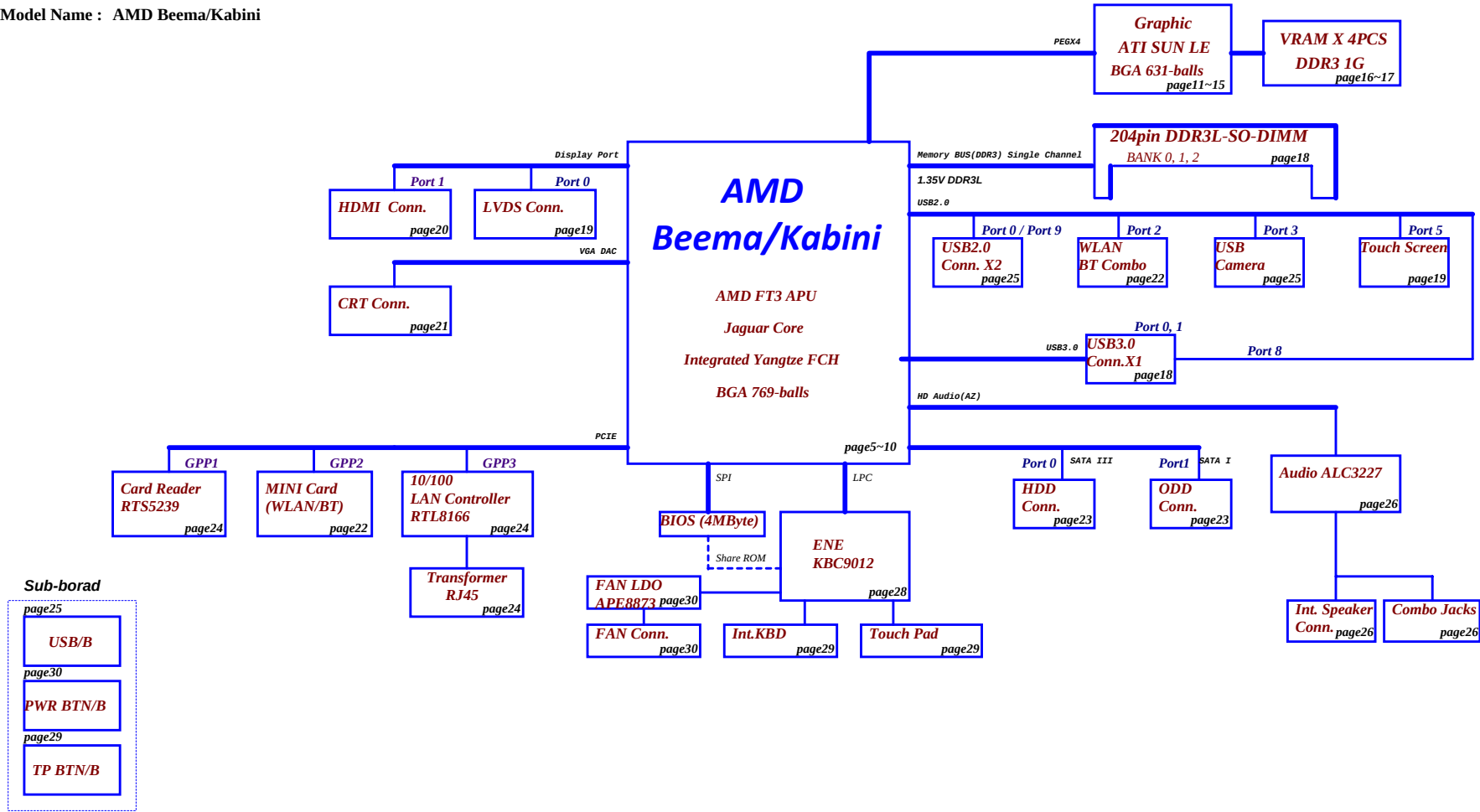
2014/02/08

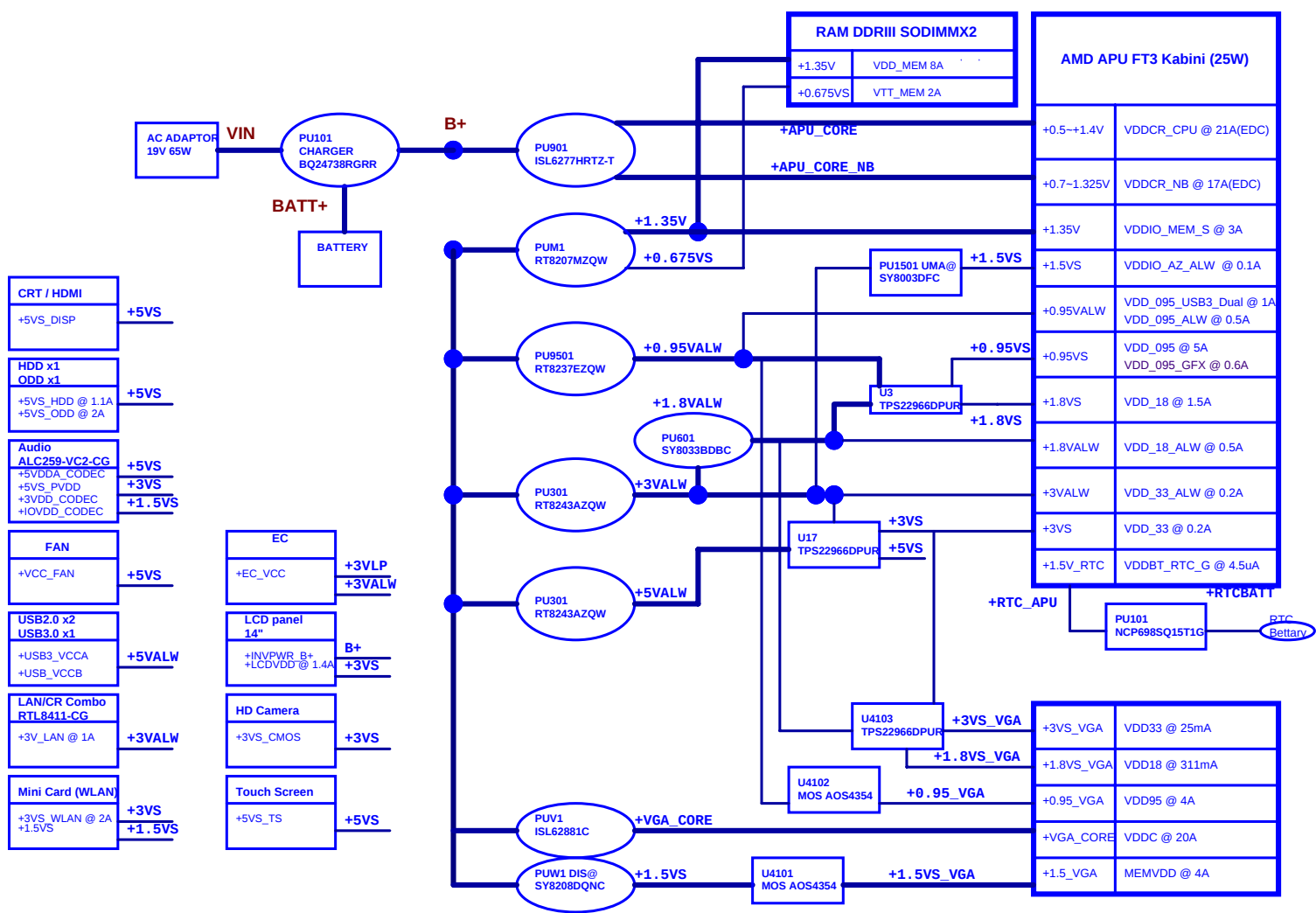
PV Rev. 4.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title COVER PAGE	
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Model Name : AMD Beema/Kabini





Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power			

STATE	SIGNAL		SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	HIGH	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF



A4-6300
Part Number = SA00007QP20
S IC A32 A4-6300 AM6300ITJ44JB



E2-6200
Part Number = SA00007OQ20
S IC A32 E2-6200 EM6200ITJ44JB 1.5G BGA



E1-6050
Part Number = SA00007IQ50
S IC A32 E1-6050 ZM1332M2J2370 1.35G BGA



A8-6410 15W
Part Number = SA00007TQ20
AM6410ITJ34JB



A4-6210 R3 15W
Part Number = SA00007RA60
AM6210ITJ34JB



E2-6110 R2 15W
Part Number = SA00007RB60
EM6110ITJ34JB



E1-6010 R2 10
Part Number = SA00007RC60
EM6010IUJ23JB



A8-6410 15W
Part Number = SA00007TQ10
AM6410ITJ34JB



A4-6210 R1 15W
Part Number = SA00007RA40
AM6210ITJ34JB



E2-6110 R2 15W
Part Number = SA00007RB40
EM6110ITJ34JB



E1-6010 R2 10
Part Number = SA00007RC40
EM6010IUJ23JB



PCB
Part Number = DAZ14D00203
PCB LA-A996P REV4.0 MIB



E1-2100
Part Number = SA00006QX10
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P



A4-5000
Part Number = SA00006R410
S IC A4 SERIES AT1250IDJ23HM 1G BGA 769P



E2-3800
Part Number = SA00007BX20
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P



A6-5200
Part Number = SA00006R350
S IC KABINI AM5200IAJ44HM 2G BGA769P APU



HDMI
Part Number = RO0000003HM
PCB 102 LA-A996P REV0 MIB 2



E1-2100
Part Number = SA00006QX60
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P



A4-5000
Part Number = SA00006R460
S IC A4 SERIES AT1250IDJ23HM 1G BGA 769P



E2-3800
Part Number = SA00007BX60
S IC A32 KABINI EM2100ICJ23HM 1G BGA769P

SMBus List

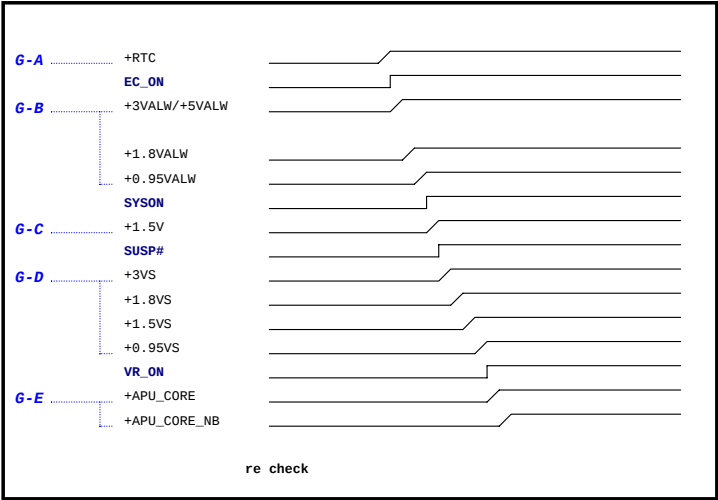
EC SMBus Port1 (+3VALW)			EC SMBus Port2 (+3VS)		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	SB-TSI (APU)	1001 100X b	98H

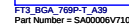
APU SMBus Port0 (+3VS)			APU SMBus Port1(+3VALW)		
Device	Address	HEX	Device	Address	HEX
DDR DIMM2	1010 000Xb	A0H			
DDR DIMM1	1010 001Xb	A2H			
Mini Card (DNI)					

BOM Structure Table

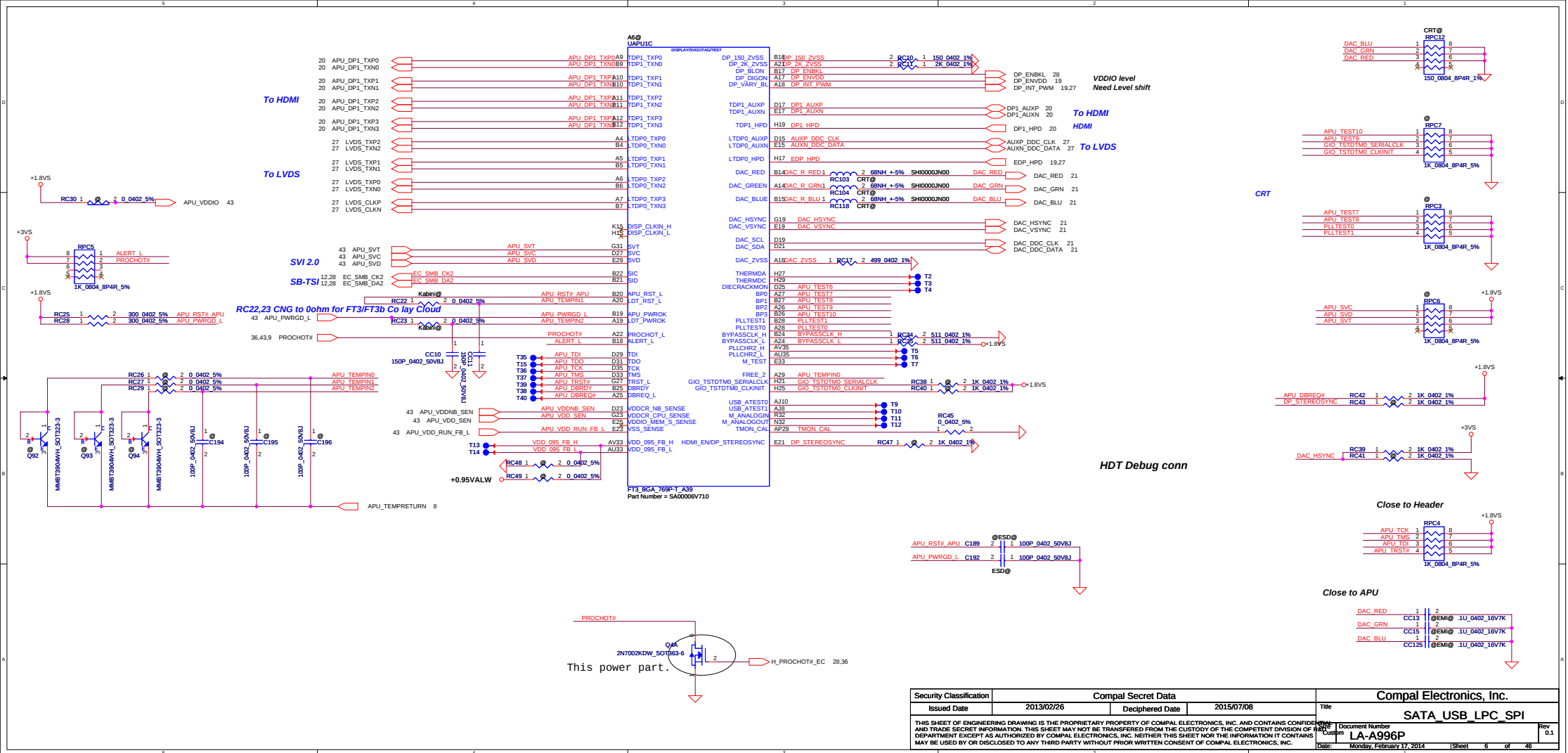
BOM Structure	BT0 Item
@	Unpop
CONN@	Connector Part Control by ME
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD Unpop component
PX@	GPU SUN LE Componet
R166@	10/100 LAN
R151@	Giga LAN
UMA@	UMA Componet
display@	display Componet
EDP@	EDP Componet
KLVDs@	Kabini LVDS Componet
BLVDs@	Beema LVDS Componet
Kabini@	Kabini Componet
Beema@	Beema Componet
LVDS@	LVDS Componet

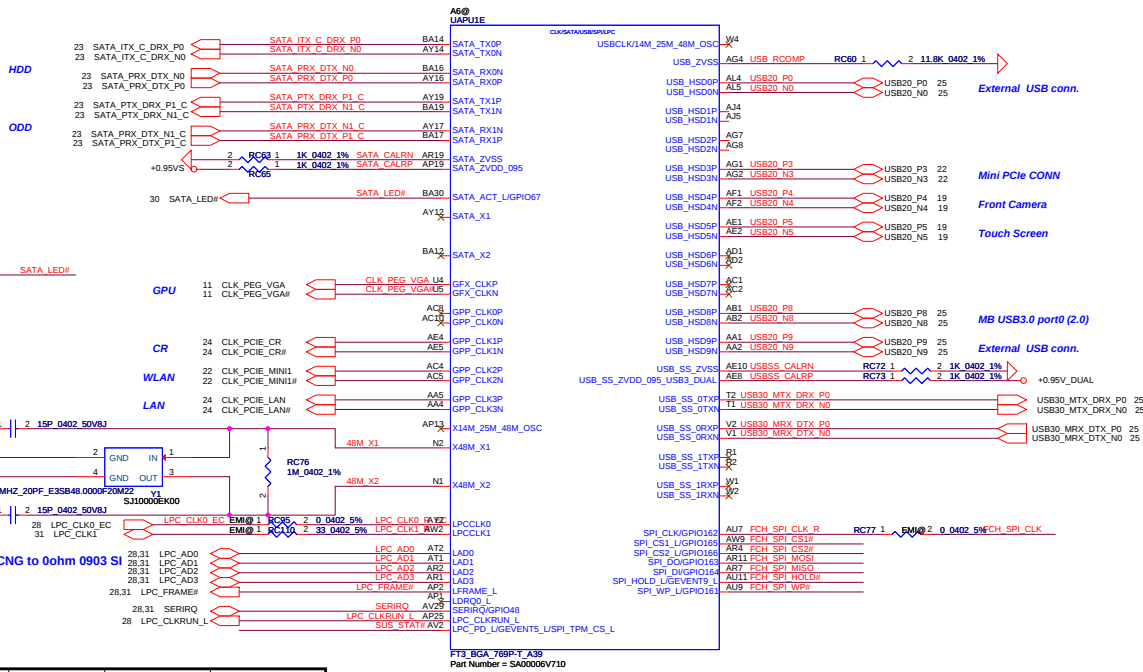
APU POWER SEQUENCE





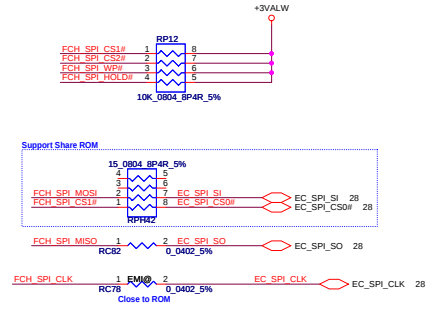
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	MEM & PCIE	
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4MB SPI ROM & Non-share ROM.

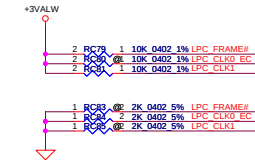
Check CS# PU R 10k10k and popinop
SCL v1.20 : If an SPI ROM is shared between
the FCH and the Embedded Controller
a 10K pull-up resistor to +3.3V_55 is installed.

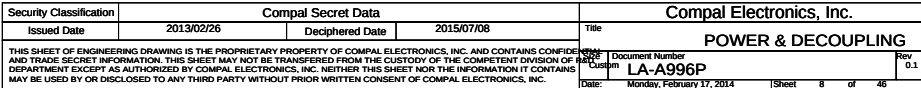


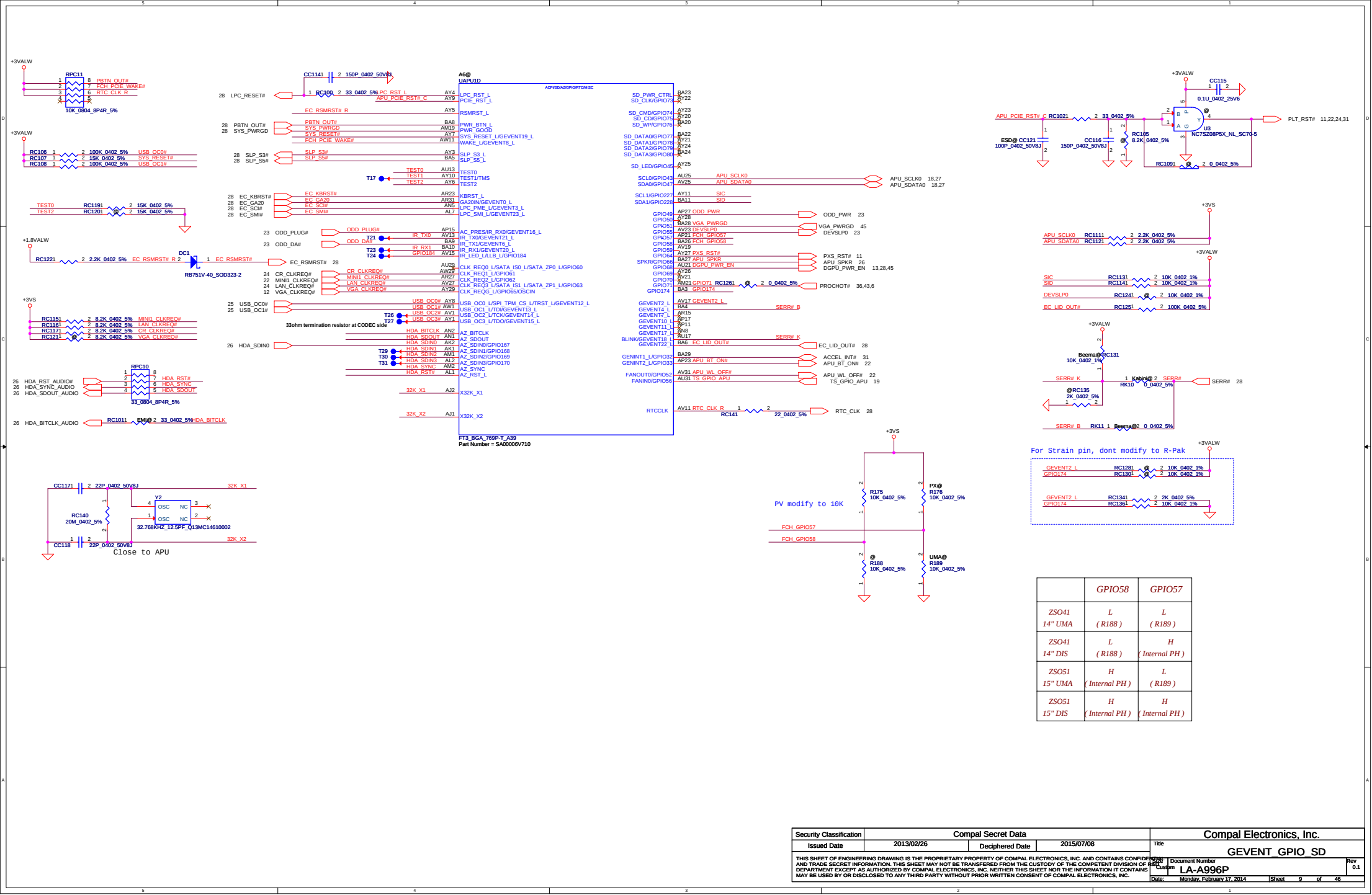
RC78, RC82 CNG to 0ohm 0903 SI

STRAPS OF APU

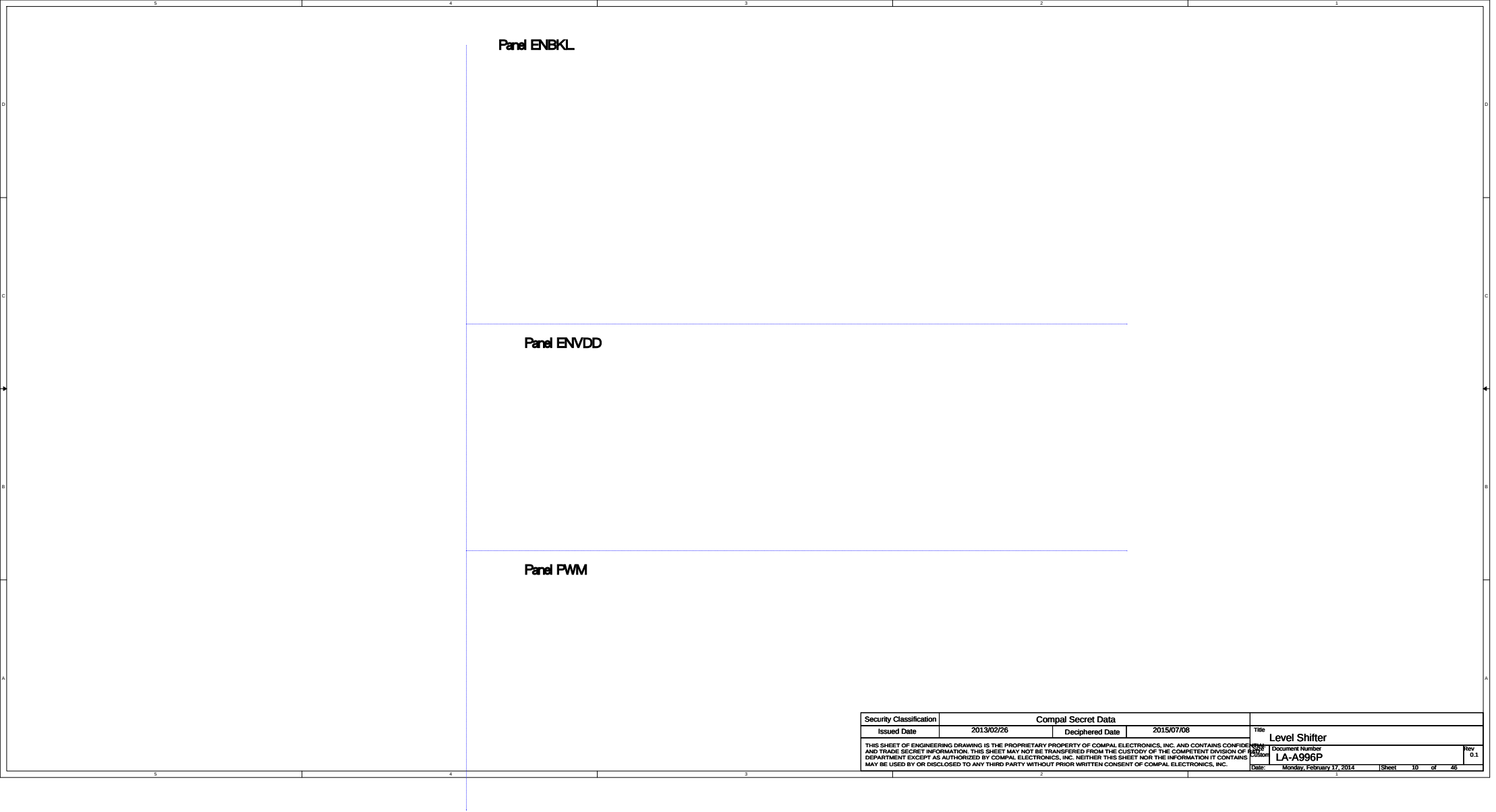
	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWR UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMING FOR SIMULATION







	GPIO58	GPIO57
ZSO41 14" UMA	L (R188)	L (R189)
ZSO41 14" DIS	L (R188)	H (Internal PH)
ZSO51 15" UMA	H (Internal PH)	L (R189)
ZSO51 15" DIS	H (Internal PH)	H (Internal PH)



Panel ENBKL

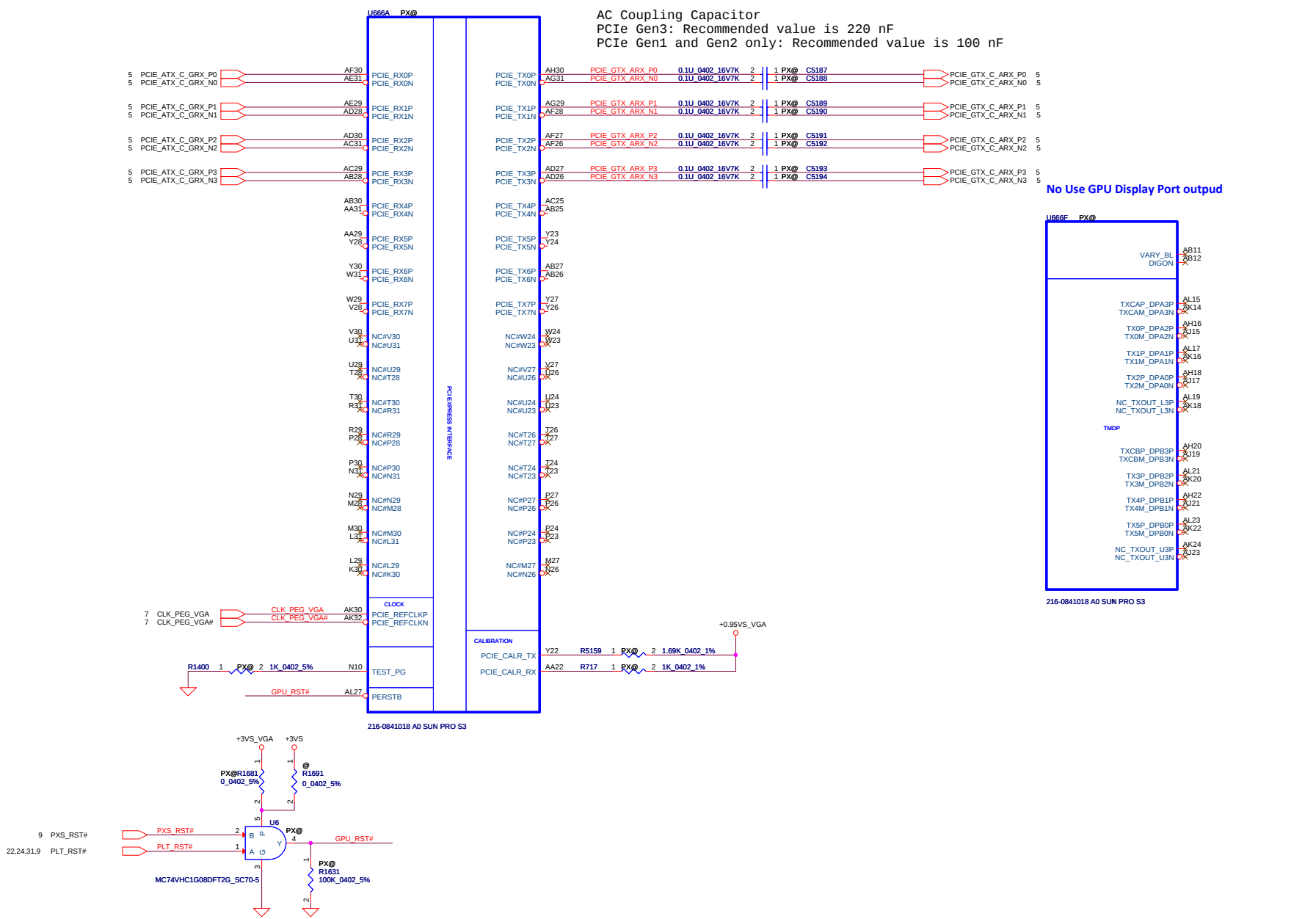
Panel ENVDD

Panel PWM

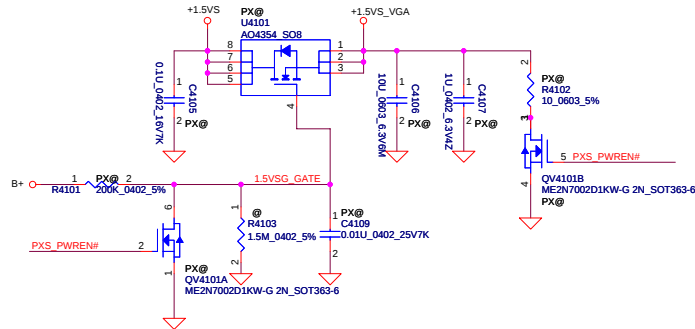
Security Classification	Compal Secret Data			Title	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Level Shifter	
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A
B
C
D

1
2
3
4
5



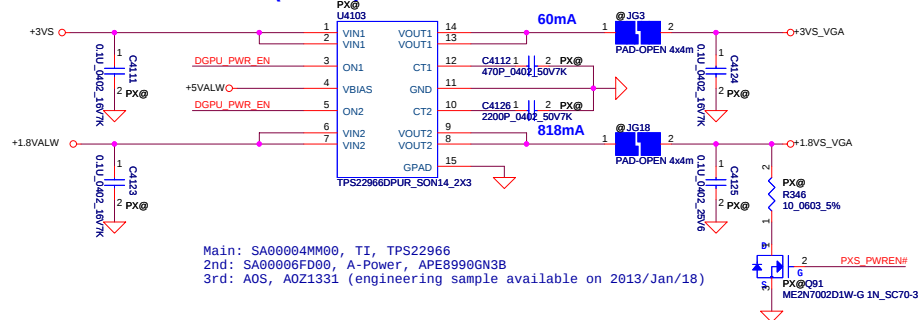
+1.5VS to +1.5VS_VGA (2.096A)



+3VS to +3VS_VGA (25mA)

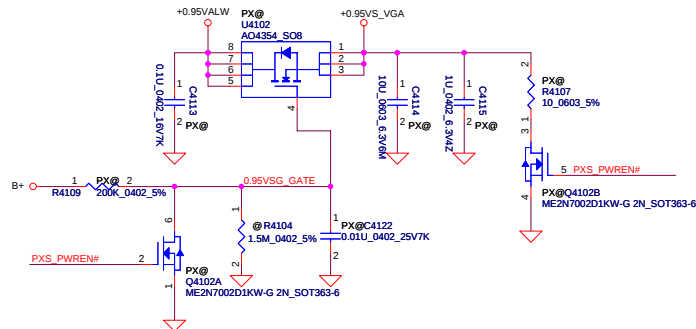
+1.8VALW to +1.8VS_VGA (311mA)

+1.8VS_VGA 必須比 +VGA_CORE晚起來



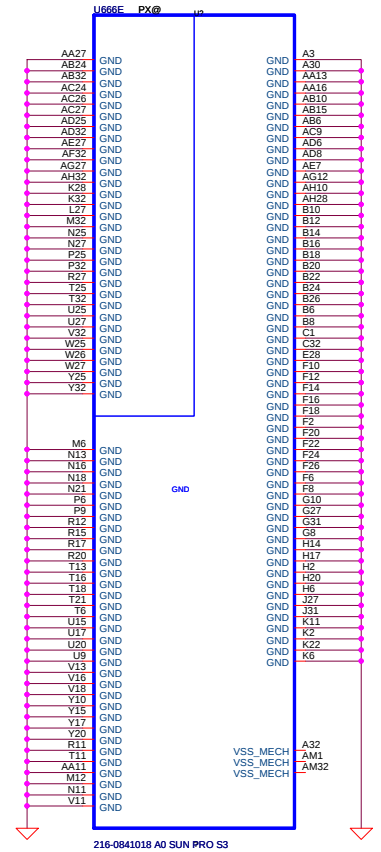
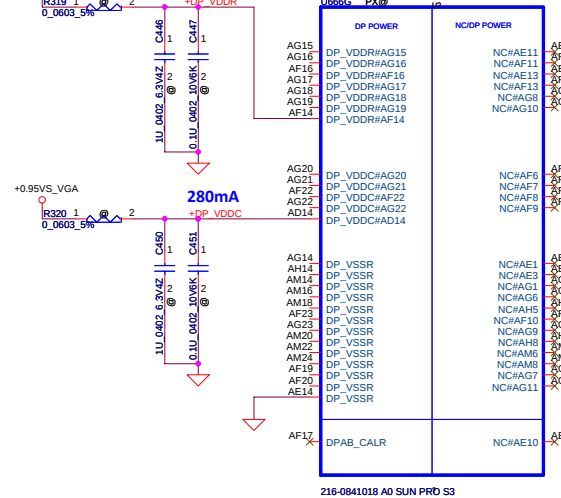
Main: SA00004MM00, TI, TPS22966
2nd: SA00006FD00, A-Power, APE8990GN3B
3rd: A0S, A0Z1331 (engineering sample available on 2013/Jan/18)

+0.95VALW to +0.95VSG (4.016A)

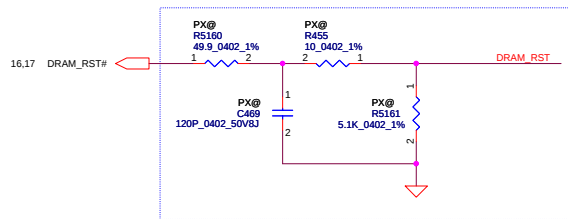
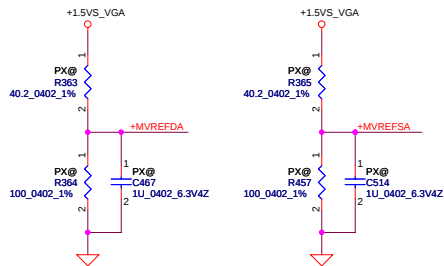


370mA (HDMI) 188mA (Display Port)

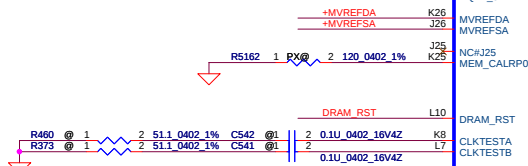
No Use GPU Display Port output



16.17 M_DA[63..0] M_DA[63..0]
16.17 M_MA[15..0] M_MA[15..0]
16.17 M_DQM[7..0] M_DQM[7..0]
16.17 M_DQS[7..0] M_DQS[7..0]
16.17 M_DQS# [7..0] M_DQS# [7..0]



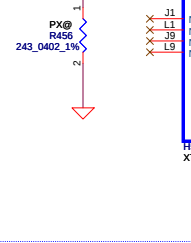
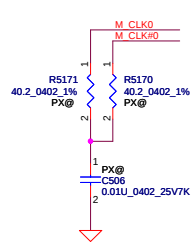
Place close to GPU (within 25mm)
and place component close to each other



Route 50ohms single-ended/100ohm diff and keep short
debug only, for clock observation, if not need, DNI.

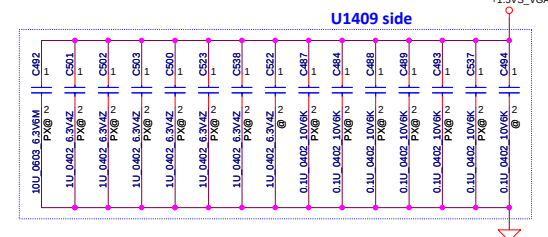
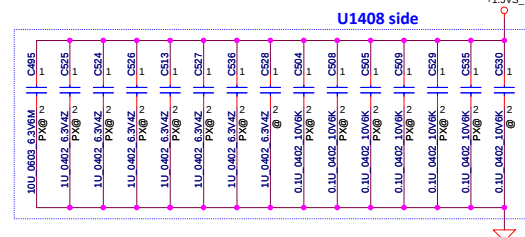
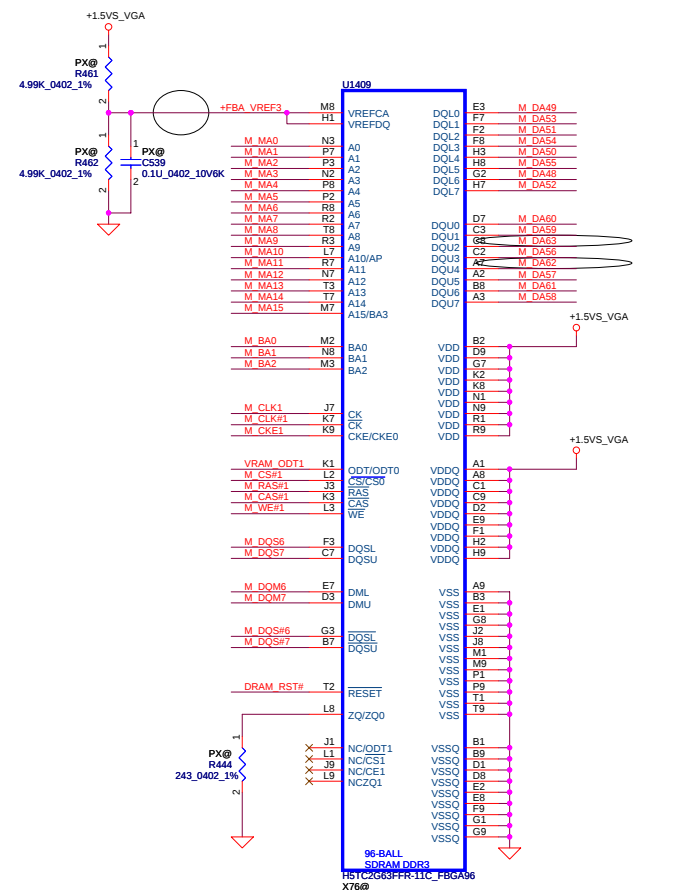
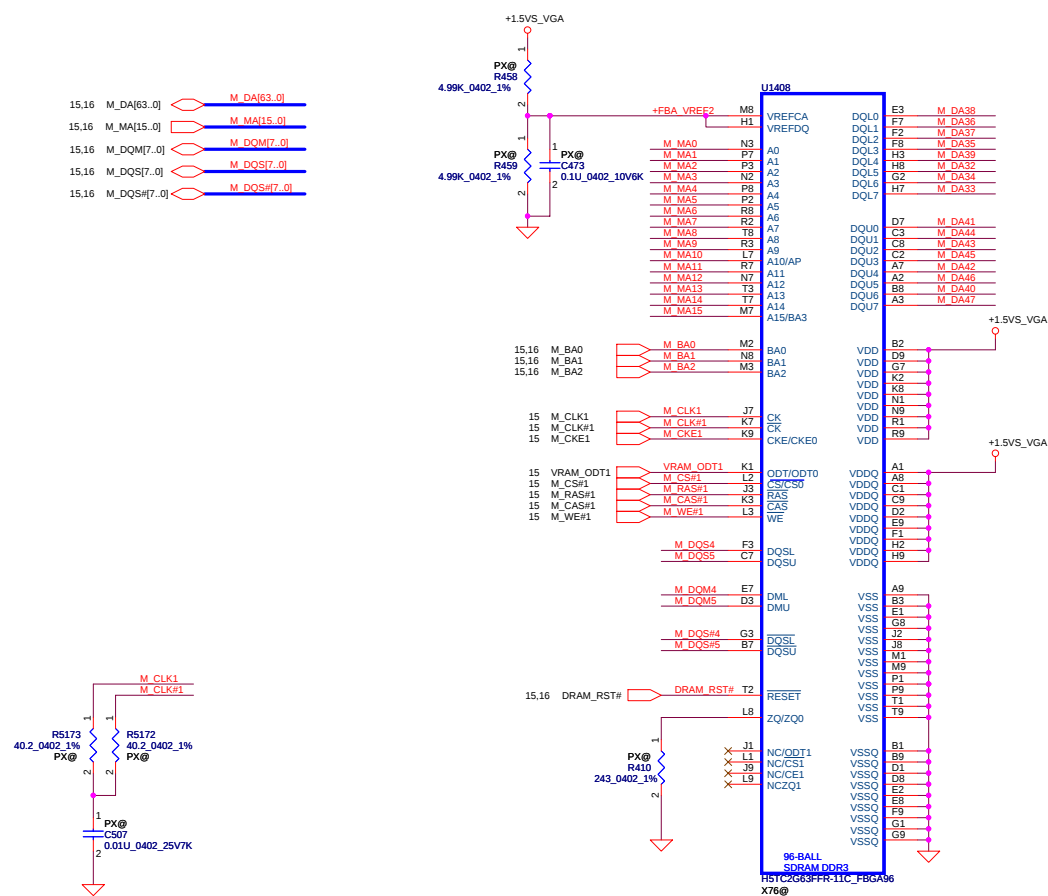
PX@		U665C		IP	
GDORS/DOR3		GDORS/DOR3		GDORS/DOR3	
M_DA0	K27	DQA0_0	MAA0_0MAA_0	K17	M_MAA0
M_DA1	J29	DQA0_1	MAA0_1MAA_1	J20	M_MAA1
M_DA2	H30	DQA0_2	MAA0_2MAA_2	H23	M_MAA2
M_DA3	H32	DQA0_3	MAA0_3MAA_3	G23	M_MAA3
M_DA4	G29	DQA0_4	MAA0_4MAA_4	G24	M_MAA4
M_DA5	F28	DQA0_5	MAA0_5MAA_5	H24	M_MAA5
M_DA6	F32	DQA0_6	MAA0_6MAA_6	J19	M_MAA6
M_DA7	F30	DQA0_7	MAA0_7MAA_7	K19	M_MAA7
M_DA8	C30	DQA0_8	MAA0_8MAA_8	G20	M_MAA8
M_DA9	F27	DQA0_9	MAA0_9MAA_9	L17	M_MAA9
M_DA10	A28	DQA0_10	MAA1_0MAA_0	J14	M_MAA10
M_DA11	C28	DQA0_11	MAA1_1MAA_1	K14	M_MAA11
M_DA12	E27	DQA0_12	MAA1_2MAA_2	J11	M_MAA12
M_DA13	G26	DQA0_13	MAA1_3MAA_3	J13	M_MAA13
M_DA14	D26	DQA0_14	MAA1_4MAA_4	H11	M_MAA14
M_DA15	F25	DQA0_15	MAA1_5MAA_5	G11	M_MAA15
M_DA16	A25	DQA0_16	MAA1_6MAA_6	M_BA2	16.17
M_DA17	C25	DQA0_17	MAA1_7MAA_7	M_BA0	16.17
M_DA18	E25	DQA0_18	MAA1_8MAA_8	M_BA1	16.17
M_DA19	D24	DQA0_19	MAA1_9MAA_9		
M_DA20	E23	DQA0_20	MAA1_10MAA_10		
M_DA21	F22	DQA0_21	MAA1_11MAA_11		
M_DA22	D22	DQA0_22	MAA1_12MAA_12		
M_DA23	F21	DQA0_23	MAA1_13MAA_13		
M_DA24	E21	DQA0_24	MAA1_14MAA_14		
M_DA25	D20	DQA0_25	MAA1_15MAA_15		
M_DA26	F19	DQA0_26	MAA1_16MAA_16		
M_DA27	A19	DQA0_27	MAA1_17MAA_17		
M_DA28	D18	DQA0_28	MAA1_18MAA_18		
M_DA29	F17	DQA0_29	MAA1_19MAA_19		
M_DA30	A17	DQA0_30	MAA1_20MAA_20		
M_DA31	C17	DQA0_31	MAA1_21MAA_21		
M_DA32	E17	DQA0_32	MAA1_22MAA_22		
M_DA33	D16	DQA0_33	MAA1_23MAA_23		
M_DA34	F15	DQA0_34	MAA1_24MAA_24		
M_DA35	A15	DQA0_35	MAA1_25MAA_25		
M_DA36	D14	DQA0_36	MAA1_26MAA_26		
M_DA37	F13	DQA0_37	MAA1_27MAA_27		
M_DA38	A13	DQA0_38	MAA1_28MAA_28		
M_DA39	C13	DQA0_39	MAA1_29MAA_29		
M_DA40	E11	DQA0_40	MAA1_30MAA_30		
M_DA41	A11	DQA0_41	MAA1_31MAA_31		
M_DA42	C11	DQA0_42	MAA1_32MAA_32		
M_DA43	F11	DQA0_43	MAA1_33MAA_33		
M_DA44	A9	DQA0_44	MAA1_34MAA_34		
M_DA45	C9	DQA0_45	MAA1_35MAA_35		
M_DA46	F9	DQA0_46	MAA1_36MAA_36		
M_DA47	D8	DQA0_47	MAA1_37MAA_37		
M_DA48	A7	DQA0_48	MAA1_38MAA_38		
M_DA49	C7	DQA0_49	MAA1_39MAA_39		
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M_DA54	A3	DQA0_54	MAA1_44MAA_44		
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M_DA56	F3	DQA0_56	MAA1_46MAA_46		
M_DA57	A1	DQA0_57	MAA1_47MAA_47		
M_DA58	C1	DQA0_58	MAA1_48MAA_48		
M_DA59	F1	DQA0_59	MAA1_49MAA_49		
M_DA60	A0	DQA0_60	MAA1_50MAA_50		
M_DA61	C0	DQA0_61	MAA1_51MAA_51		
M_DA62	F0	DQA0_62	MAA1_52MAA_52		
M_DA63	A0	DQA0_63	MAA1_53MAA_53		
M_DA64	C0	DQA0_64	MAA1_54MAA_54		
M_DA65	F0	DQA0_65	MAA1_55MAA_55		
M_DA66	A0	DQA0_66	MAA1_56MAA_56		
M_DA67	C0	DQA0_67	MAA1_57MAA_57		
M_DA68	F0	DQA0_68	MAA1_58MAA_58		
M_DA69	A0	DQA0_69	MAA1_59MAA_59		
M_DA70	C0	DQA0_70	MAA1_60MAA_60		
M_DA71	F0	DQA0_71	MAA1_61MAA_61		
M_DA72	A0	DQA0_72	MAA1_62MAA_62		
M_DA73	C0	DQA0_73	MAA1_63MAA_63		
M_DA74	F0	DQA0_74	MAA1_64MAA_64		
M_DA75	A0	DQA0_75	MAA1_65MAA_65		
M_DA76	C0	DQA0_76	MAA1_66MAA_66		
M_DA77	F0	DQA0_77	MAA1_67MAA_67		
M_DA78	A0	DQA0_78	MAA1_68MAA_68		
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M_DA83	F0	DQA0_83	MAA1_73MAA_73		
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M_DA93	A0	DQA0_93	MAA1_83MAA_83		
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M_DA95	F0	DQA0_95	MAA1_85MAA_85		
M_DA96	A0	DQA0_96	MAA1_86MAA_86		
M_DA97	C0	DQA0_97	MAA1_87MAA_87		
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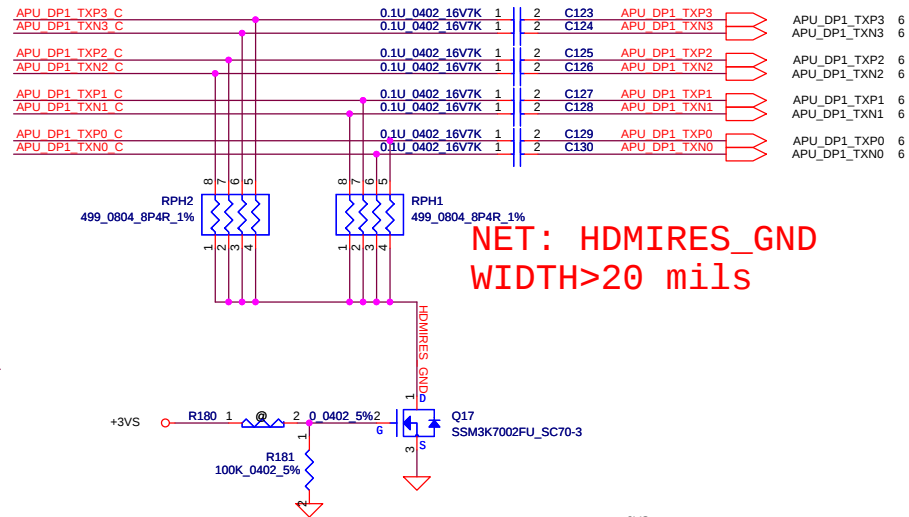
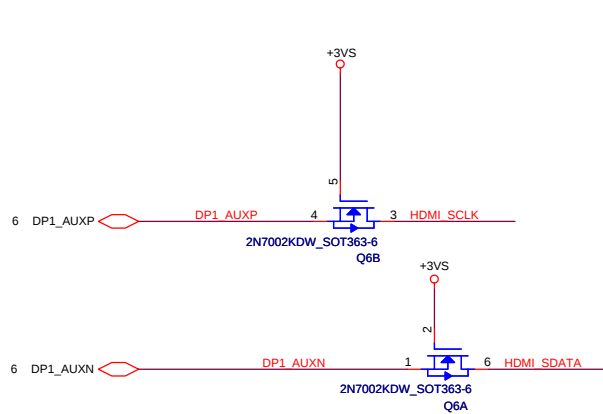
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Issued Date	2013/01/11	Deciphered Date	2013/12/31	Title	SUN_VRAM A Lower	
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1	2
Memory Partition A - Upper 32 bits	



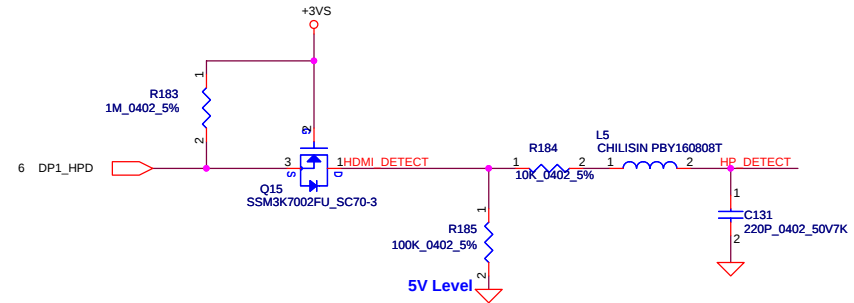
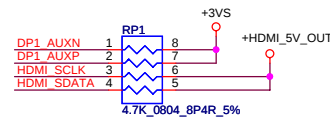
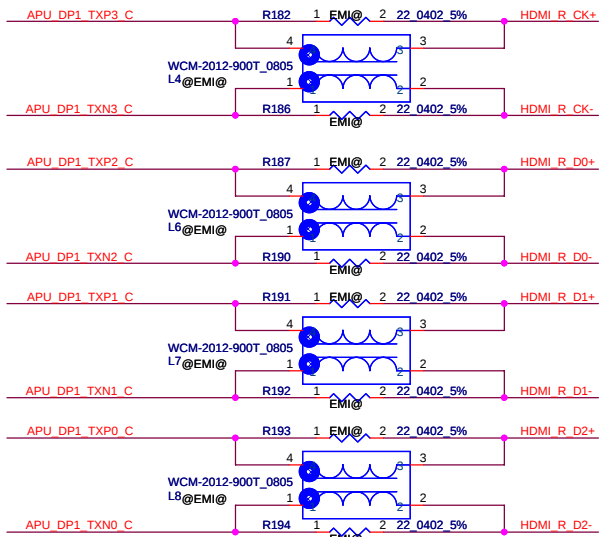
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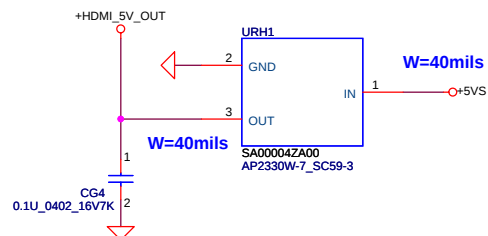
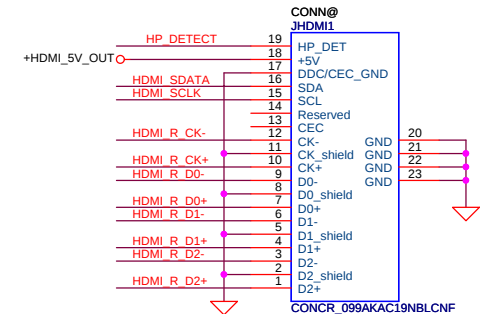
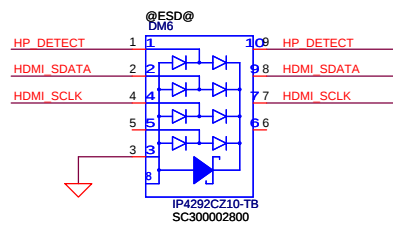


CLK
Data0
Data1
Data2

SM070001310 400ma 90ohm@100mhz DCR 0.3

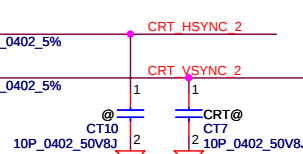
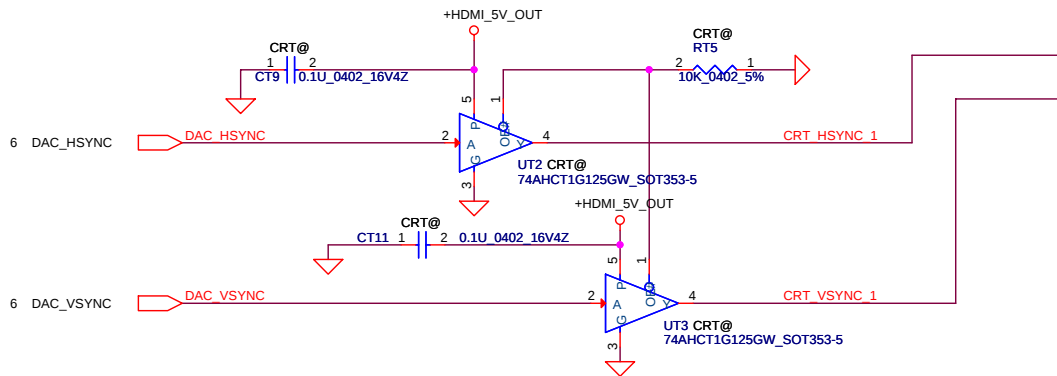
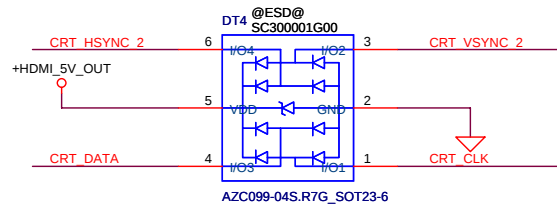
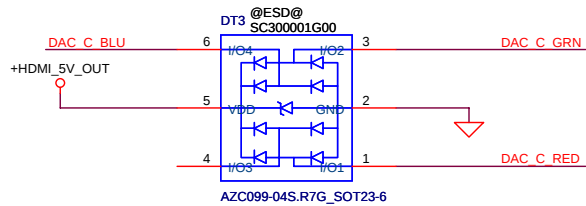


8/20 change HDMI Conn HDMI Conn.

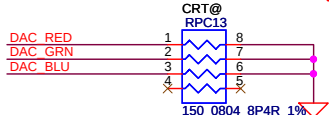
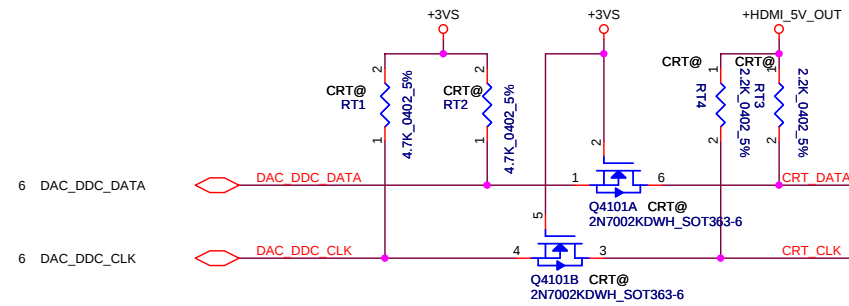
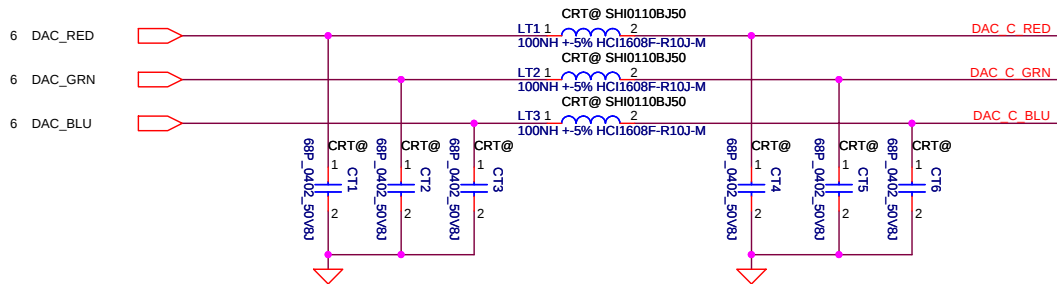
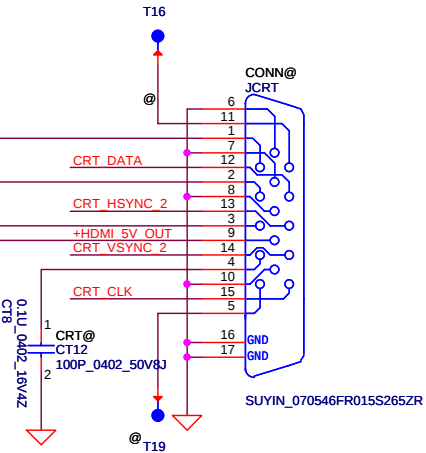


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2013/02/26			2015/07/08			HDMI Connector		
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Date			Monday, February 17, 2014			Sheet 20 of 46		

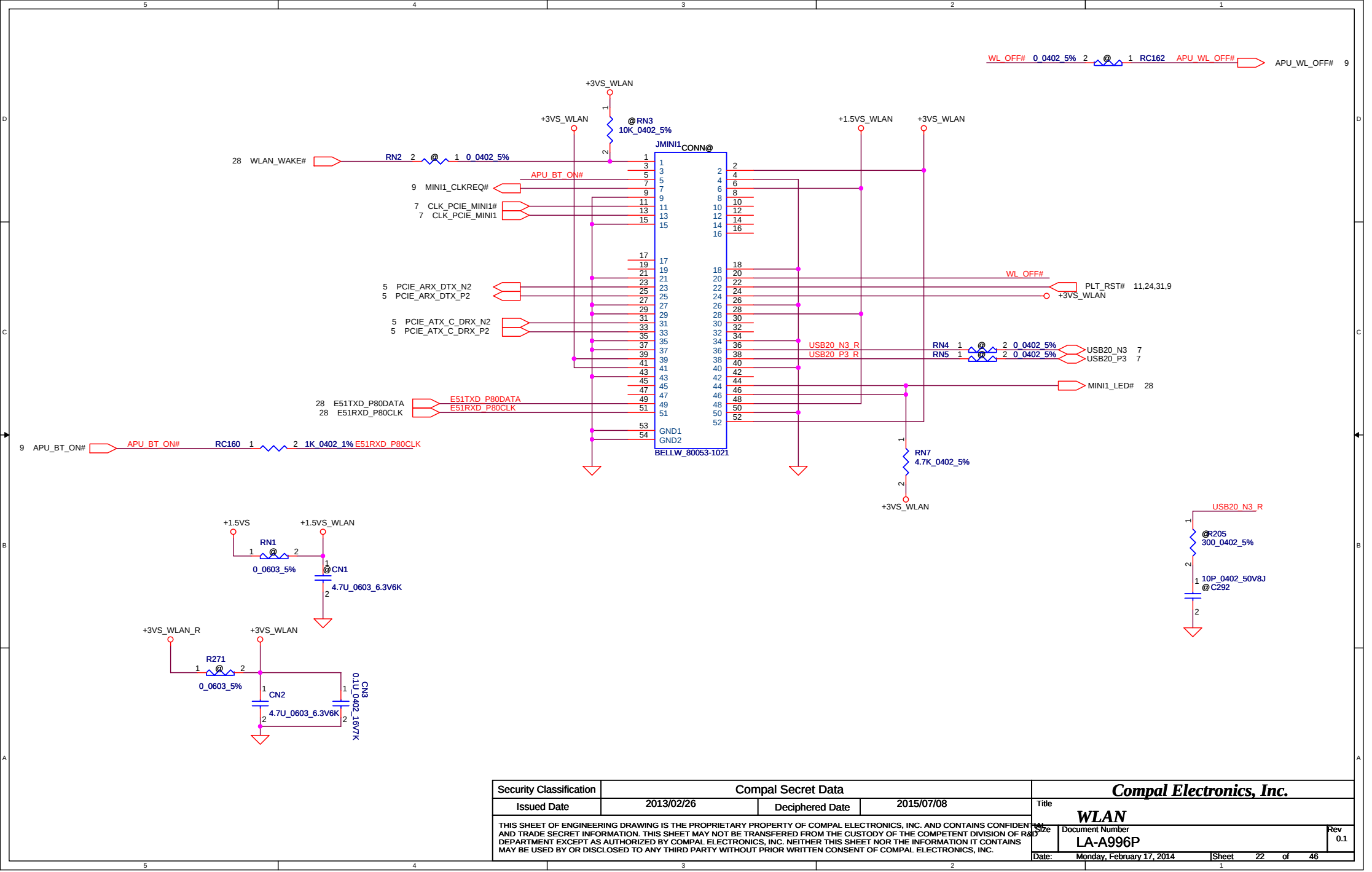
CRT share HDMI Power



W=40mils

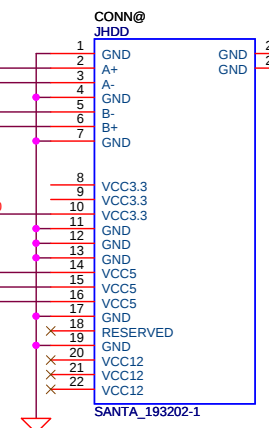
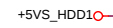
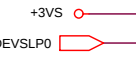
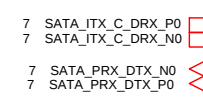
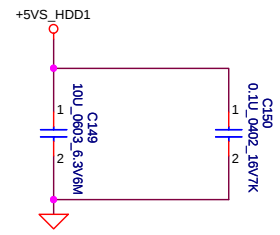
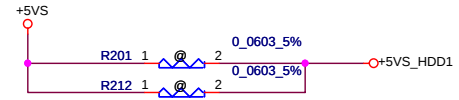


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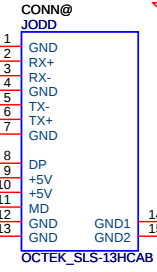
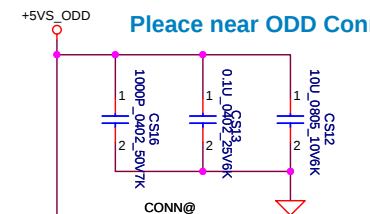
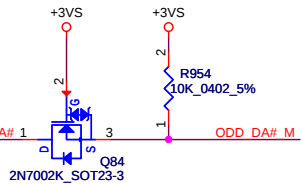
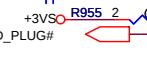
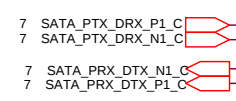
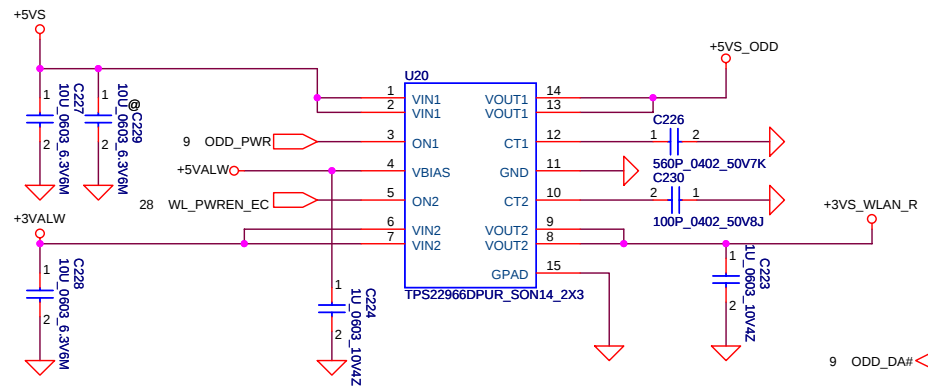
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Monday, February 17, 2014		Sheet		0.1	
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1		46			

2.5" SATA HDD connector

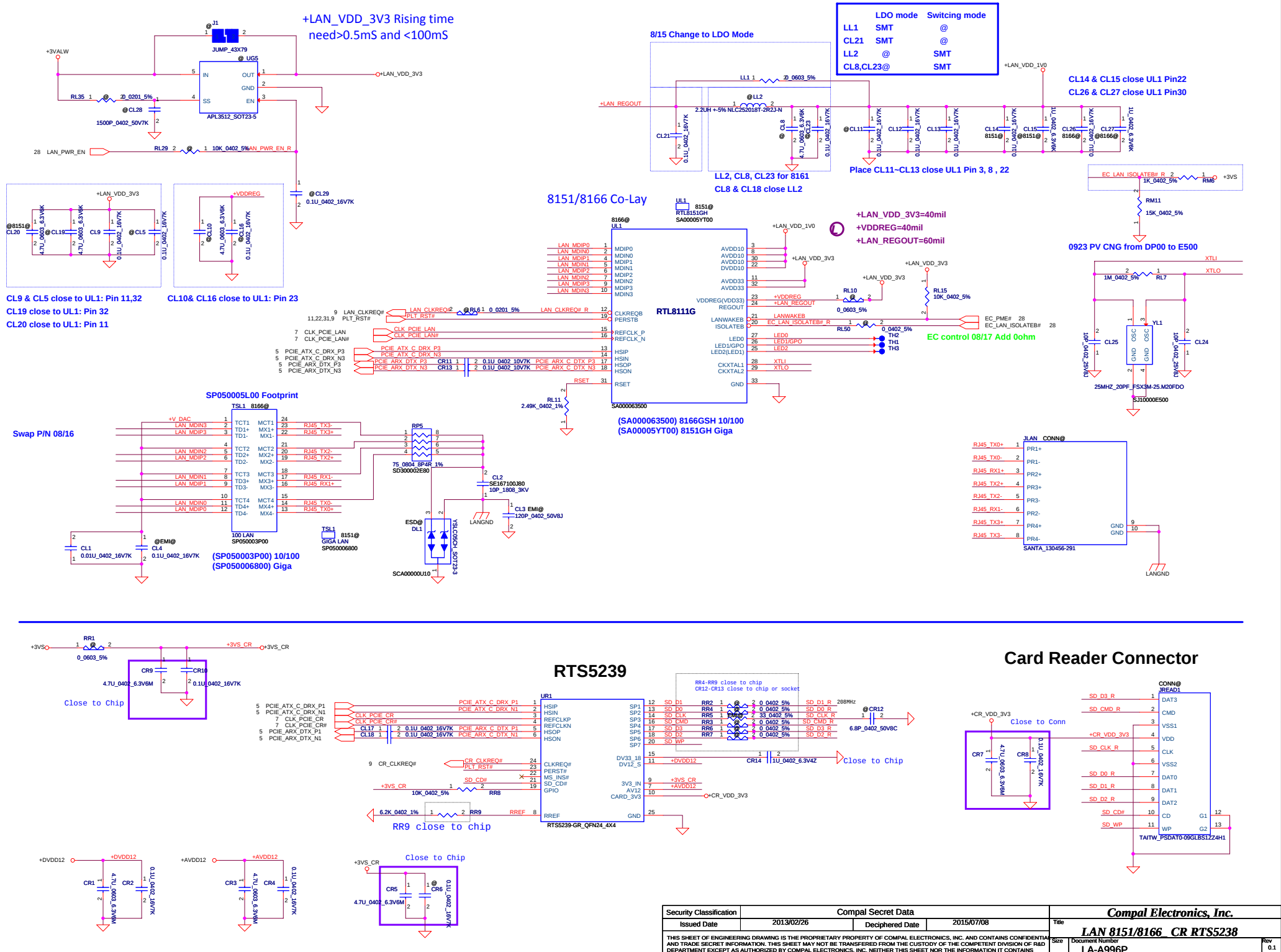


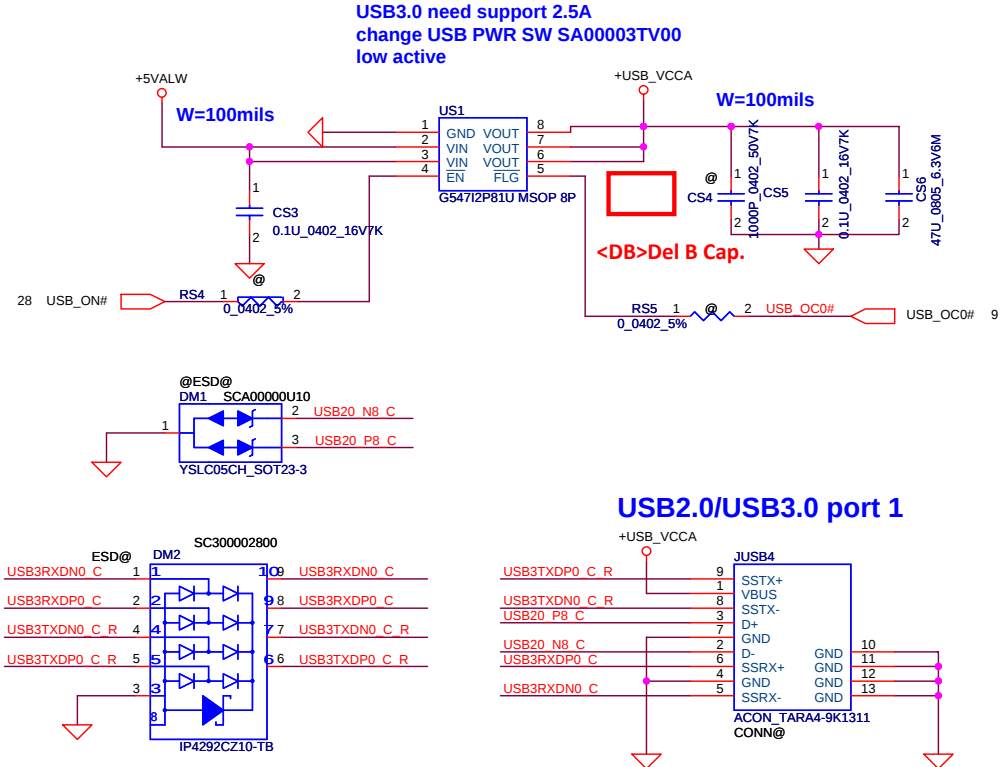
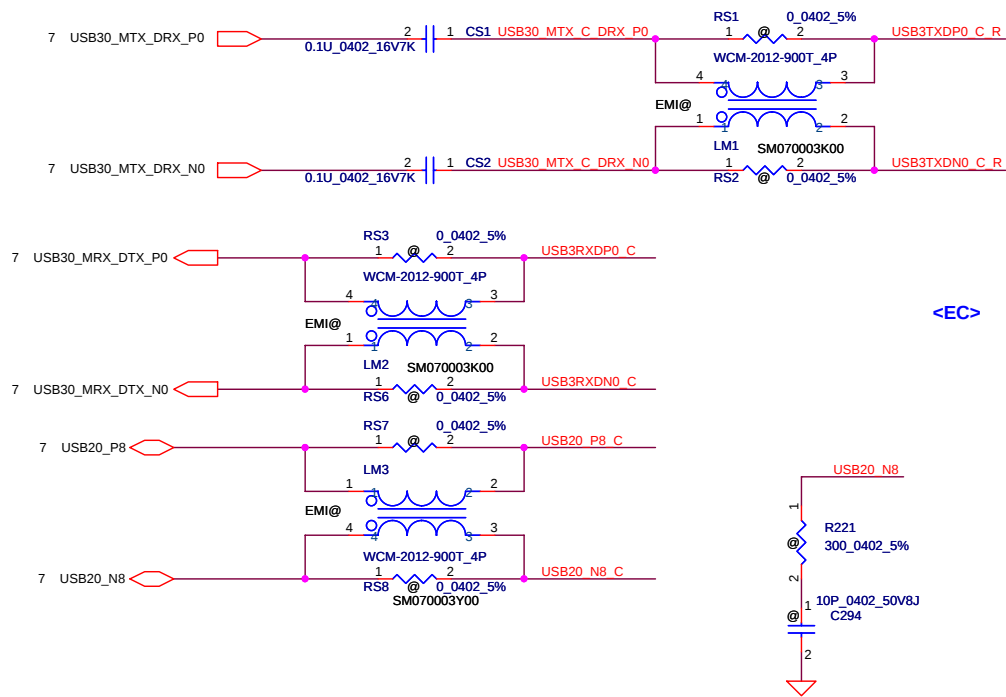
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Place near ODD Connector

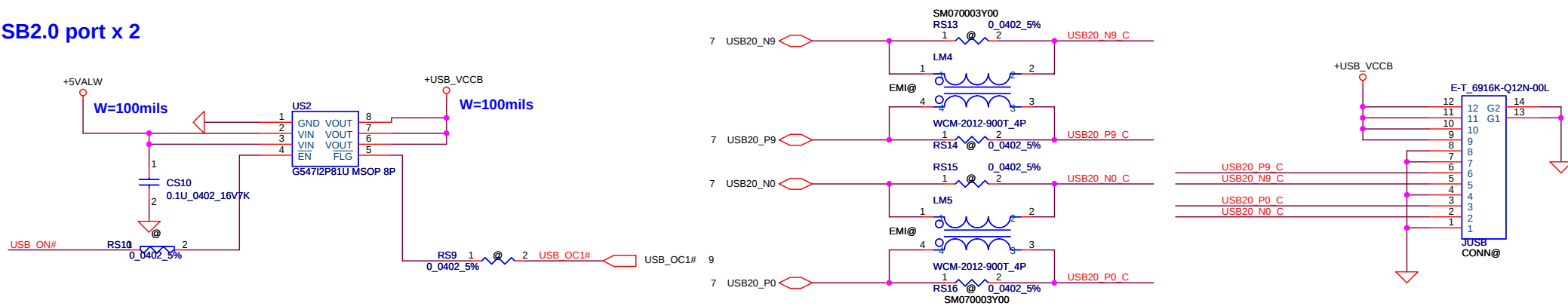


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				Date:	Monday, February 17, 2014
				Sheet	23 of 46

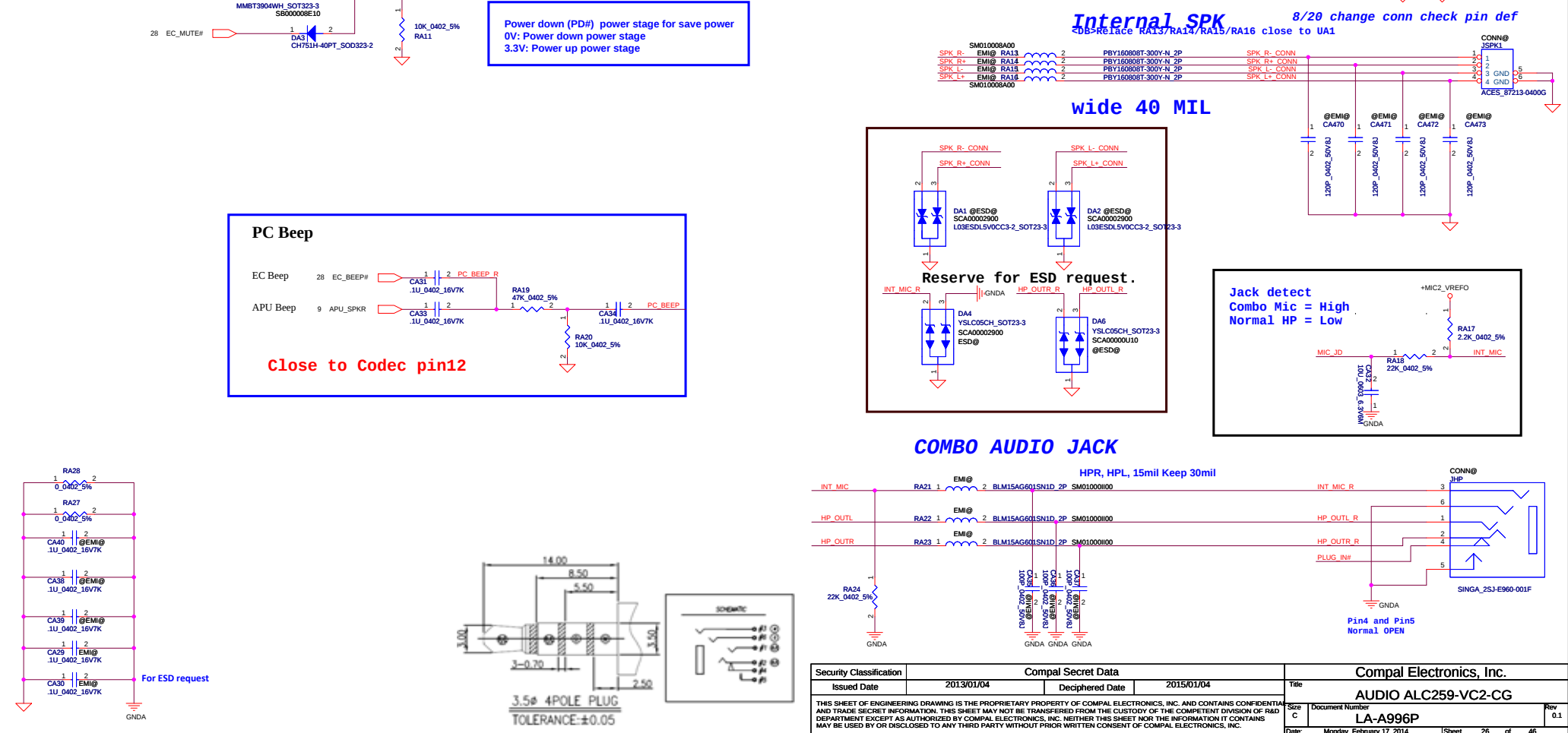
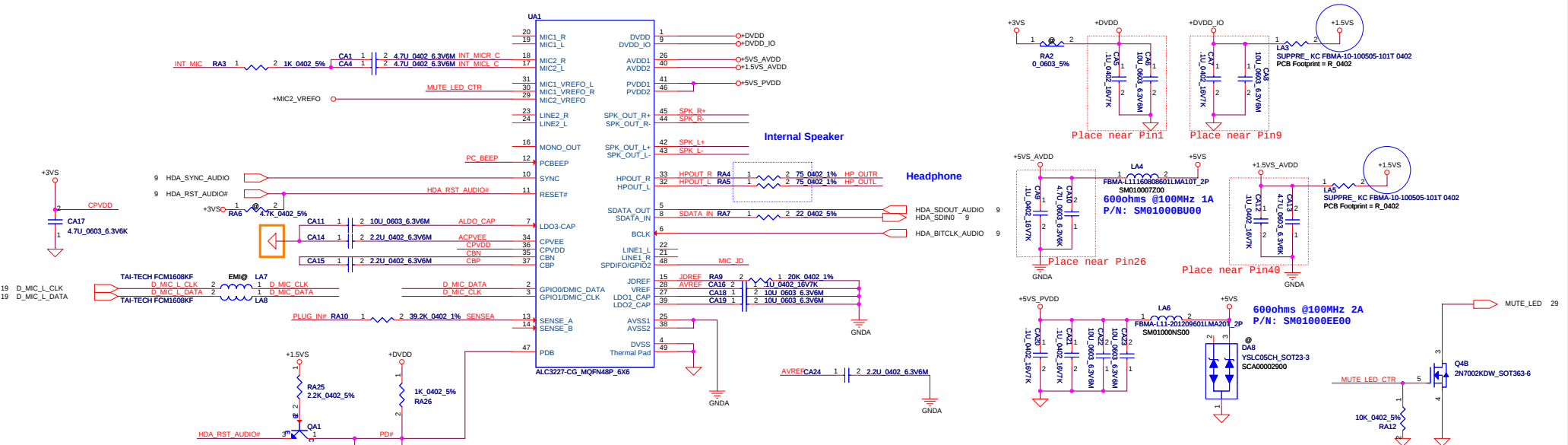




USB2.0 port x 2



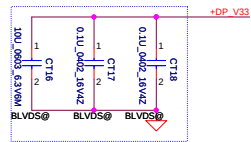
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Issued Date		2013/02/26		Deciphered Date		2015/07/08		Title									
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								Doc Number		LA-A996P				Rev		0.1	
								Date: Friday, February 21, 2014								Sheet 25 of 46	



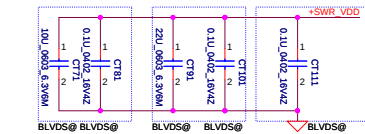
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Issued Date	2013/01/04	Deciphered Date	2015/01/04	Title	AUDIO ALC259-VC2-CG
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Size	C	Document Number	LA-A996P	Rev	0.1
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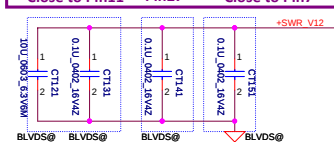
Layout note
Close to Pin3



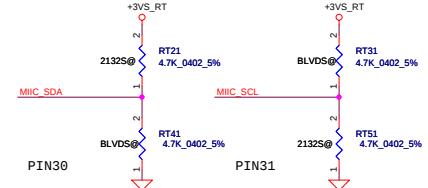
Layout note
Close to LT5 Close to Pin18 Close to Pin13



Layout note
Close to Pin11 Close to Pin27 Close to Pin7

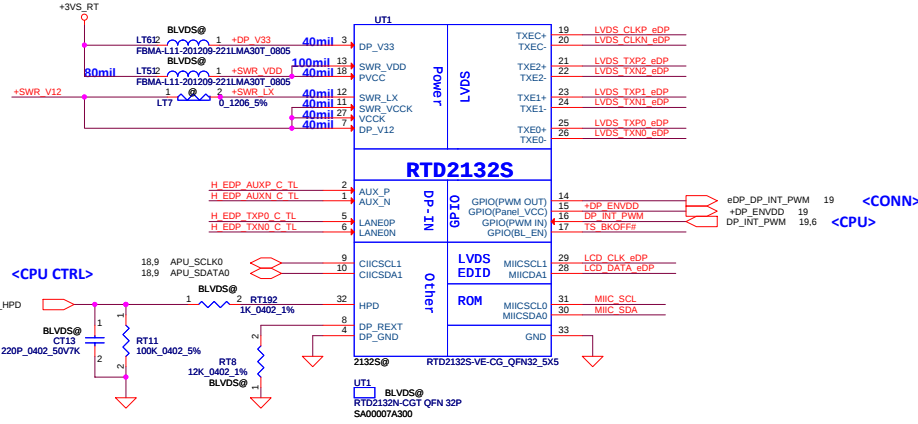


※ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.
EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.
(※Default mode)

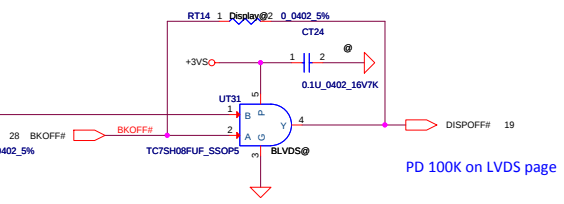


	LDO	SWR
2132S	Do not support	mount LT7
2132N	Use 0 ohm	mount LT7

※ If use 2132N, please select LDO mode as default.



Layout note
Close to Pin8



<LVDS Panel>

<CPU>

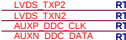
LTDP0_TXP3
LTDP0_TXN3
LTDP0_TXP2
LTDP0_TXN2

LTDP0_TXP1
LTDP0_TXN1

LTDP0_TXP0
LTDP0_TXN0

LTDP0_AUXP
LTDP0_AUXN

RP40 Close CPU



RT24~27 Close JLVDS conn

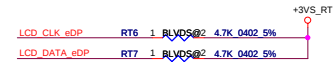


	PIN15
2132S	TL_ENVDD
BLVDS	+LCD_VDD *

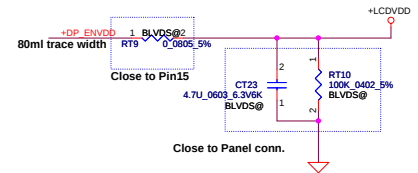
* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

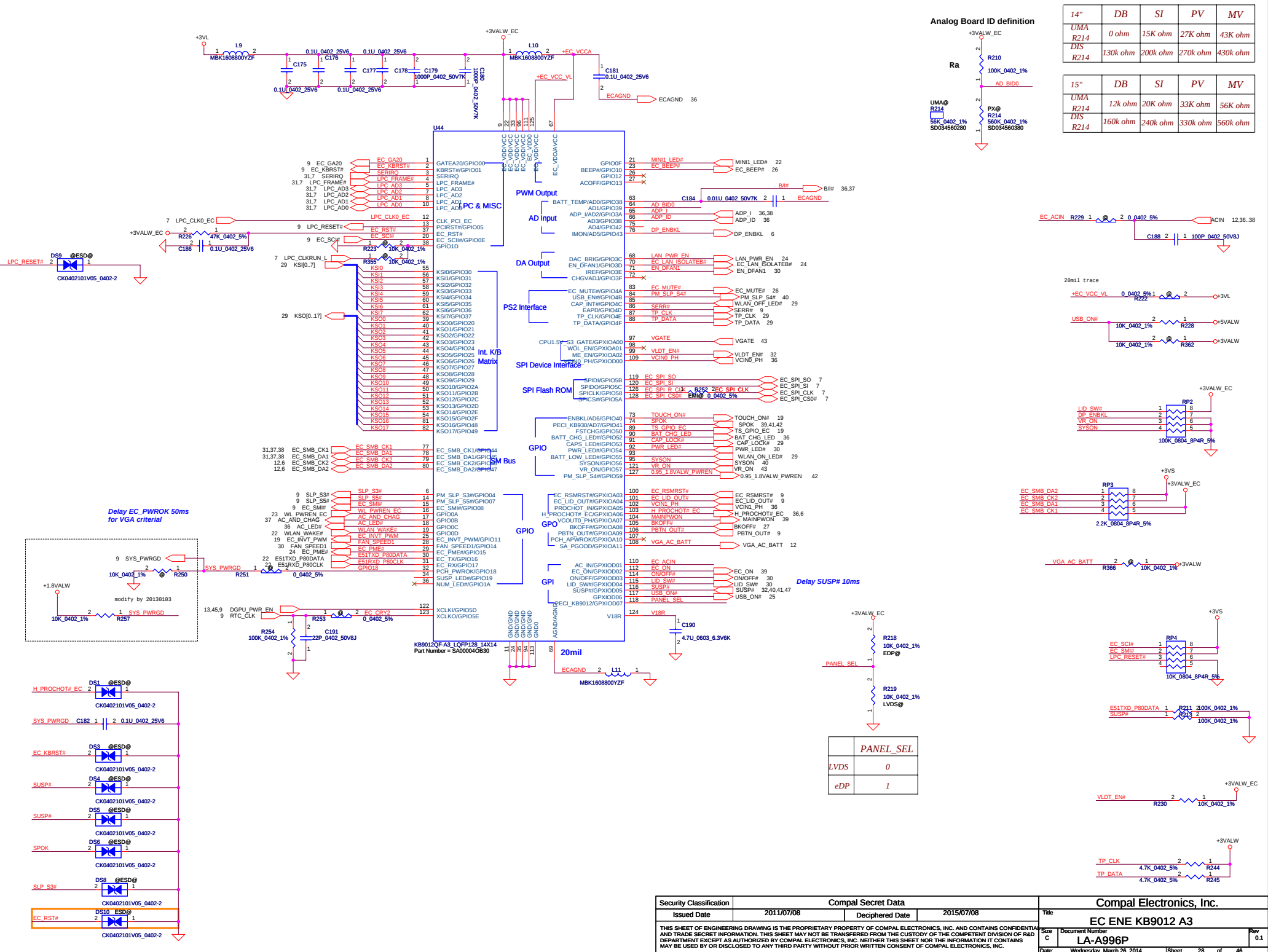
PIN16	Accept voltage input (high level)
2132S	3.3V
BLVDS	1.5~3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform



Different between 2132S and 2132N(BLVDS)	
2132S	2132N
1. Support SWR mode	1. Support LDO mode and SWR mode
	2. Internal ROM
	3. Support LCD_VDD(internal Power switch)
	4. Integrates Level shifter

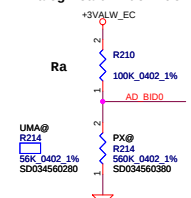




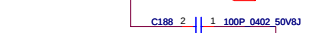
14"	DB	SI	PV	MV
UMA	0 ohm	15K ohm	27K ohm	43K ohm
R214	130k ohm	200k ohm	270k ohm	430k ohm

15"	DB	SI	PV	MV
UMA	12k ohm	20K ohm	33K ohm	56K ohm
R214	160k ohm	240k ohm	330k ohm	560k ohm

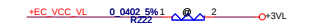
Analog Board ID definition



EC ACIN R229 1 2 0 0.402 5%



28mil trace



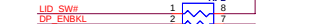
EC VCC_VL 0 0.402 5% 1 2 R222



USB_ON# 10K_0402_1% 2 1 R228



EC VCC_VL 10K_0402_1% 2 1 R362



LID_SW# DP_ENBK# VR_ON SYSON



EC SMB_DA2 EC SMB_CK2 EC SMB_DA1 EC SMB_CK1



2.2K_0804_8P4R_5%



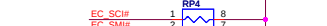
VGA_AC_BATT 2 1 10K_0402_1%



EC SCH# EC SMIF# LPC_RESET#



ES1TXD_P80DATA SUSP#



VLDI_EN#



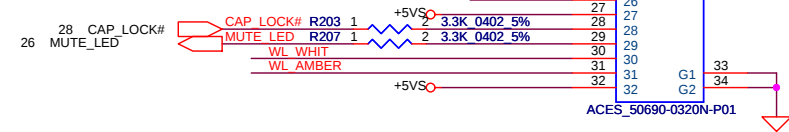
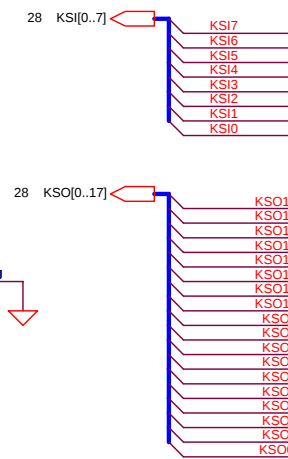
TP_CLK 4.7K_0402_5% 2 1 R244



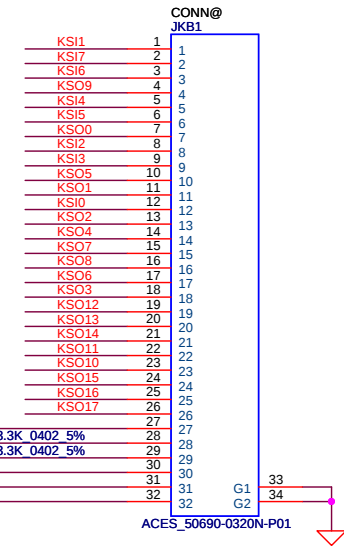
TP_DATA 4.7K_0402_5% 2 1 R245



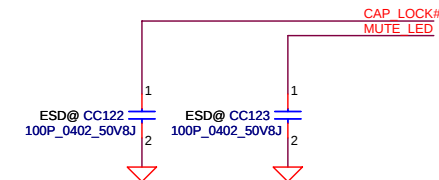
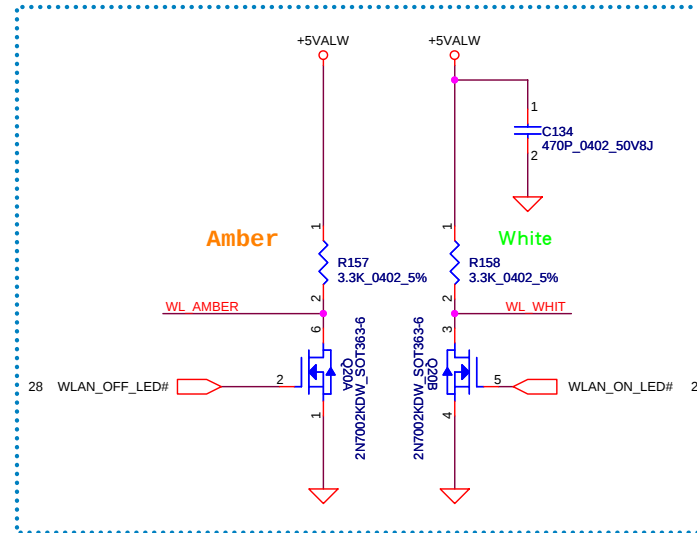
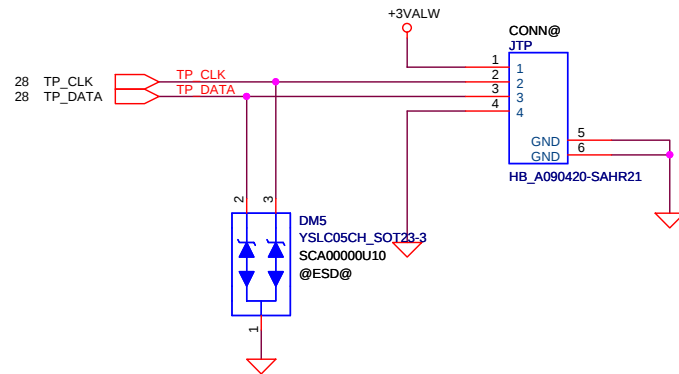
PANEL_SEL	
LVDI	0
eDP	1



Keyboard conn

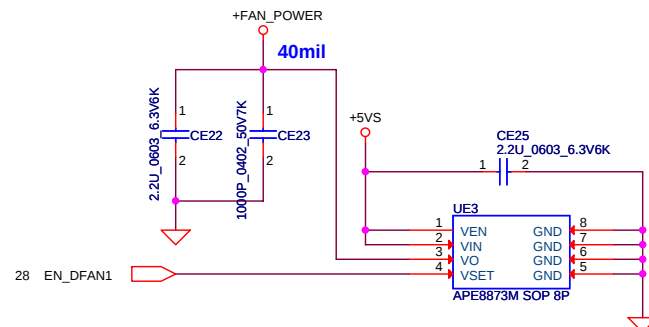
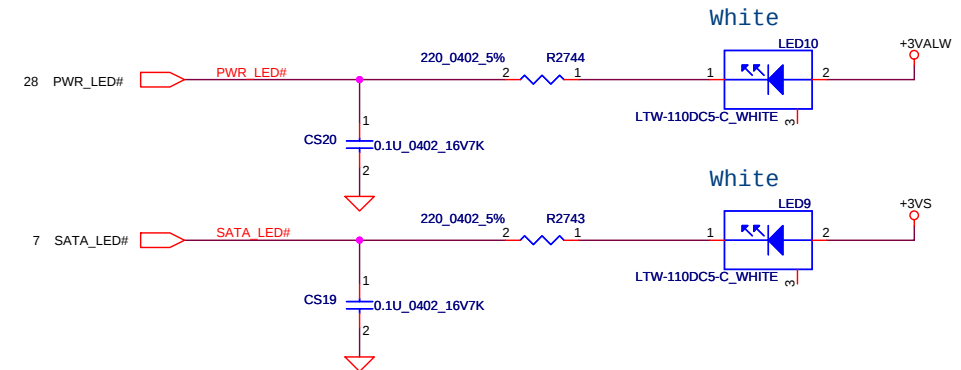
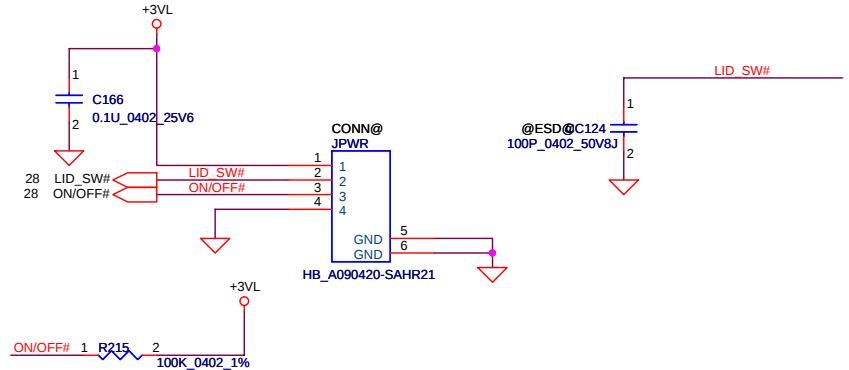


Touch pad conn

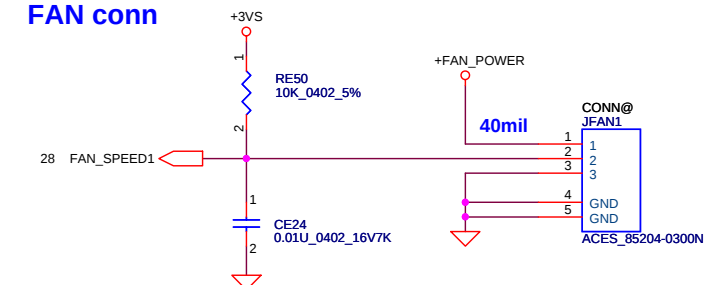


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Power Button Connector



FAN conn



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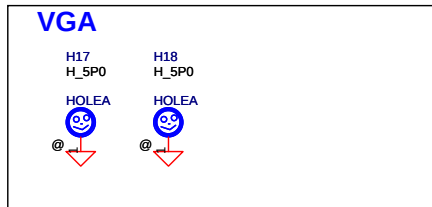
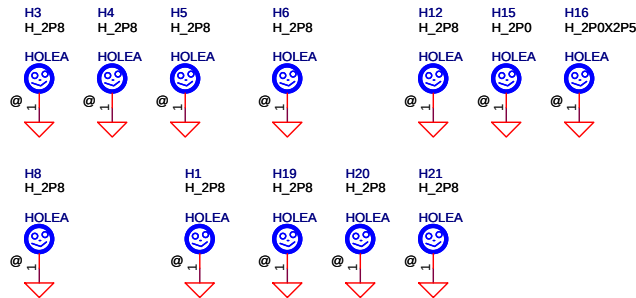
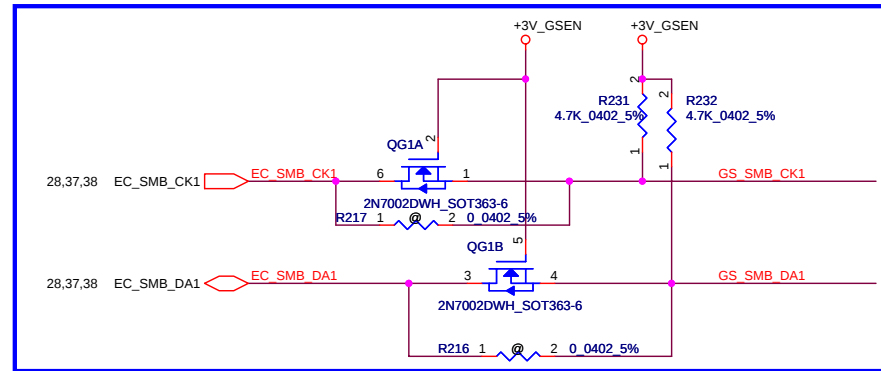
ACCELEROMETER

ACCELEROMETER

SI# 2012.04.10 Change ACCEL_INT# to INT1

Components and Connections:

- U25 (HP3DC2TR):** Accelerometer chip with pins 1-16.
- Resistors:** R208, R227, R209 (all 10K_0402_5%).
- Capacitors:** C231 (0.1uF_0402_16V7K), C232 (10uF_0603_6.3V6M).
- Supply:** +3V_GSEN.
- Signal:** ACCEL_INT# (INT1).



CPU

H9 H_5P0	H10 H_5P0	H11 H_5P0	H13 H_5P0
HOlea	HOlea	HOlea	HOlea

PM1.2

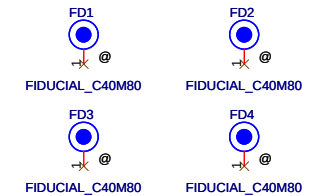
The schematic diagram illustrates the connection of the SLB 9656 TT 1.2 chip to the LPC1114 microcontroller. The chip is connected to the LPC1114 via I2C (LPC_AD0-LPC_AD3 to LAD0-LAD3) and SPI (LPC_CLK1 to LCLK, LPC_FRAME# to LFRAME#, PLT_RST# to LRESET#, SERIRQ to SERIRQ, and PLT_RST# to CLKRUN#). The chip is also connected to a +3VS supply and ground. The chip has two pins labeled T45 PAD and T46 PAD. The chip is labeled SLB 9656 TT 1.2.

SLB 9656 TT 1.2 Pin Connections:

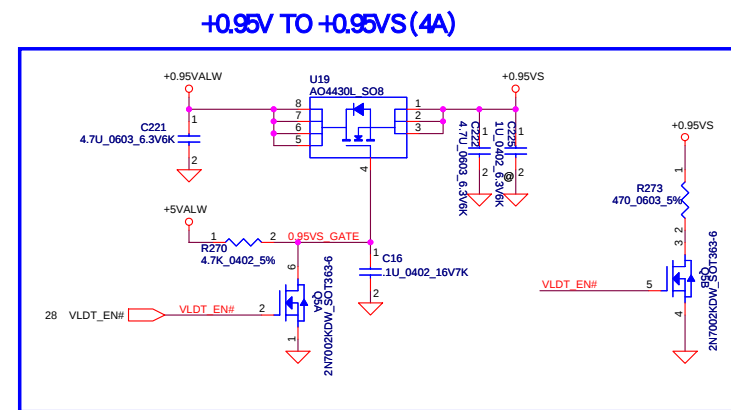
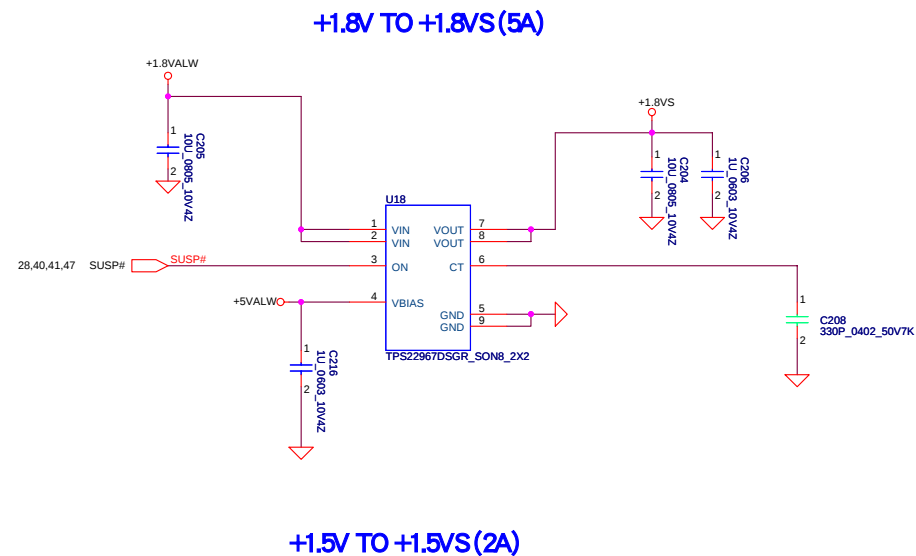
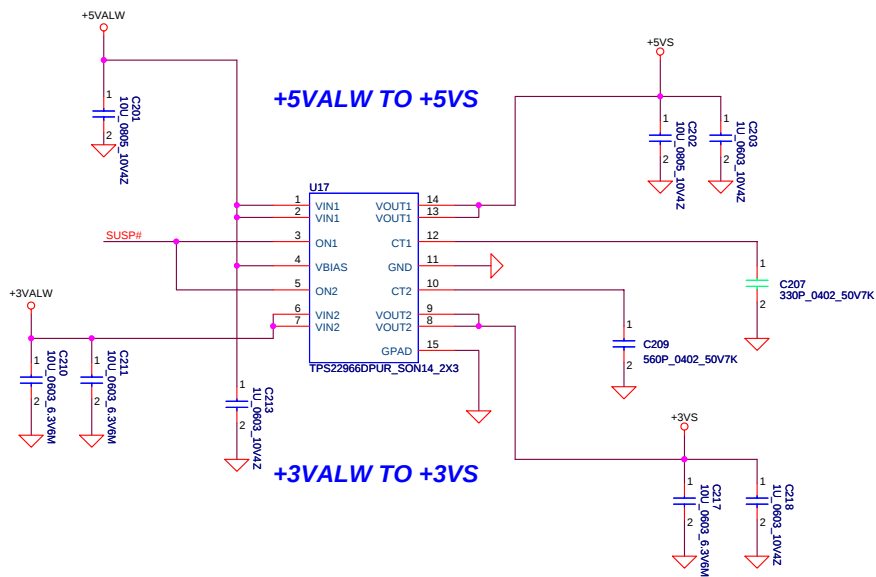
- Power:** VDD (24, 19, 10) to +3VS; VSB (5) to +3VS; GND (4, 11, 18, 25) to ground.
- I2C:** LAD0 (26) to LPC_AD0 (28.7); LAD1 (23) to LPC_AD1 (28.7); LAD2 (20) to LPC_AD2 (28.7); LAD3 (17) to LPC_AD3 (28.7).
- SPI:** LCLK (21) to LPC_CLK1 (7); LFRAME# (22) to LPC_FRAME# (28.7); LRESET# (16) to PLT_RST# (21.22.24.9); SERIRQ (27) to SERIRQ (28.7); CLKRUN# (15) to PLT_RST# (21.22.24.9).
- Other:** TESTB1/BADD (28) to BADD (1) via R1412 0_0402_5%; XTALO (14) to XTALI (13) via R1412 0_0402_5%; GPIO2 (2) to T45 PAD; GPIO (6) to T46 PAD.

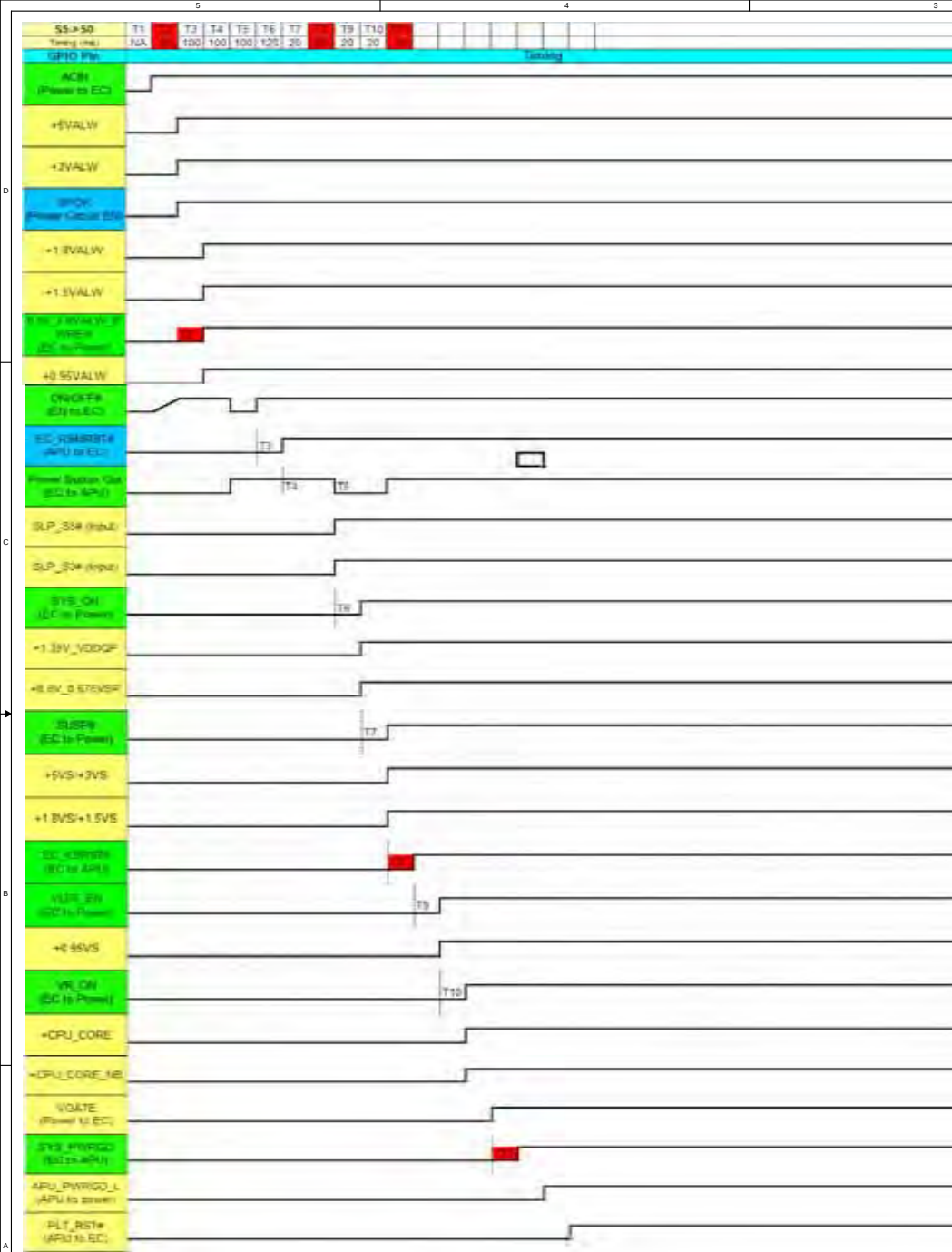
LPC1114 Pin Connections:

- Power:** ZVAVST_20P00_0T10 (1) to +3VS; ZVAVST_20P00_0T10 (2) to ground; ZVAVST_20P00_0T10 (1) to +3VS; ZVAVST_20P00_0T10 (2) to ground; ZVAVST_20P00_0T10 (1) to +3VS; ZVAVST_20P00_0T10 (2) to ground.
- Capacitors:** C1053, C1054, C1055, C1052 (0.1uF 0402 16V4Z).
- Resistors:** R1380 (4.7K 0402 5%), R1409 (0_0402_5%).

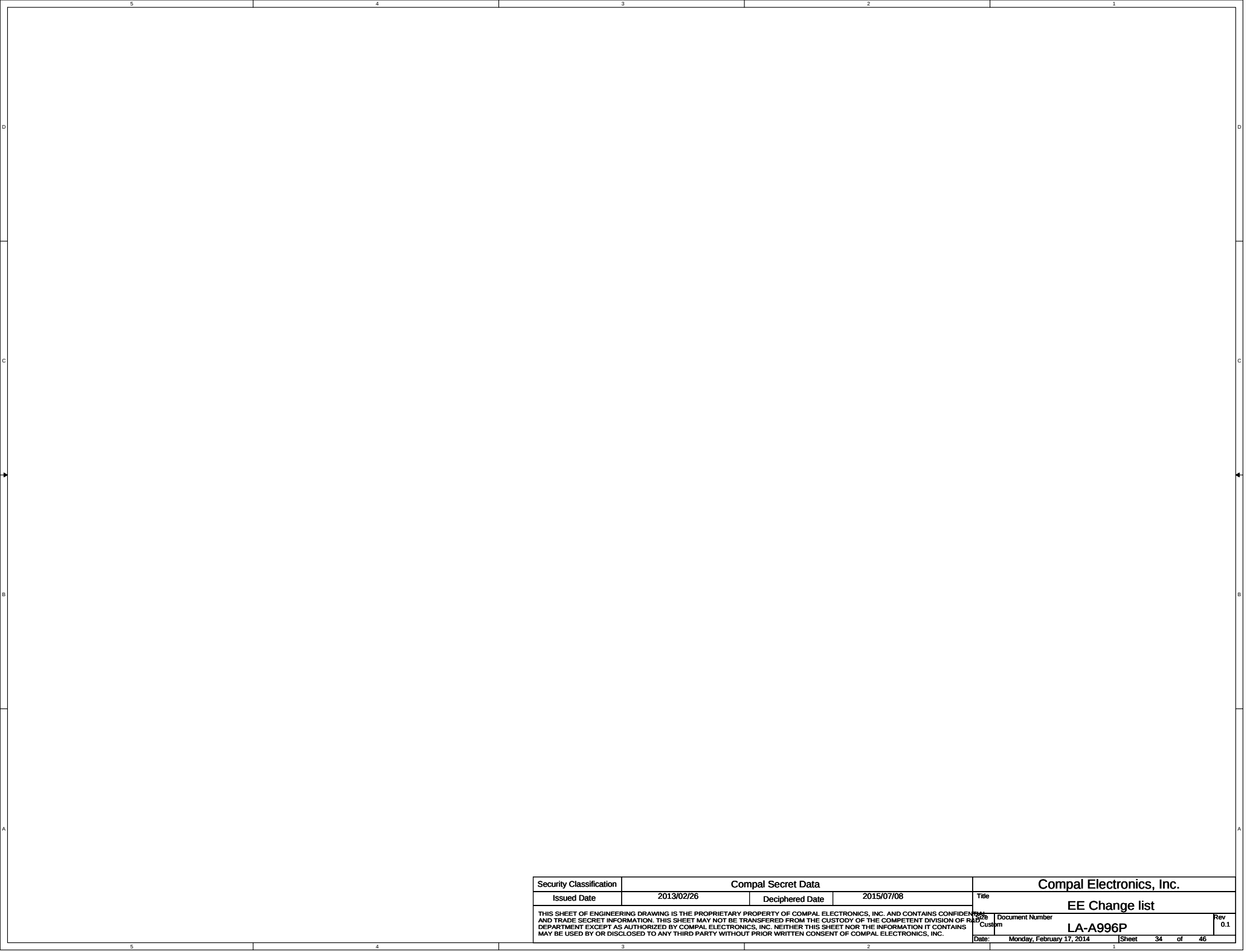


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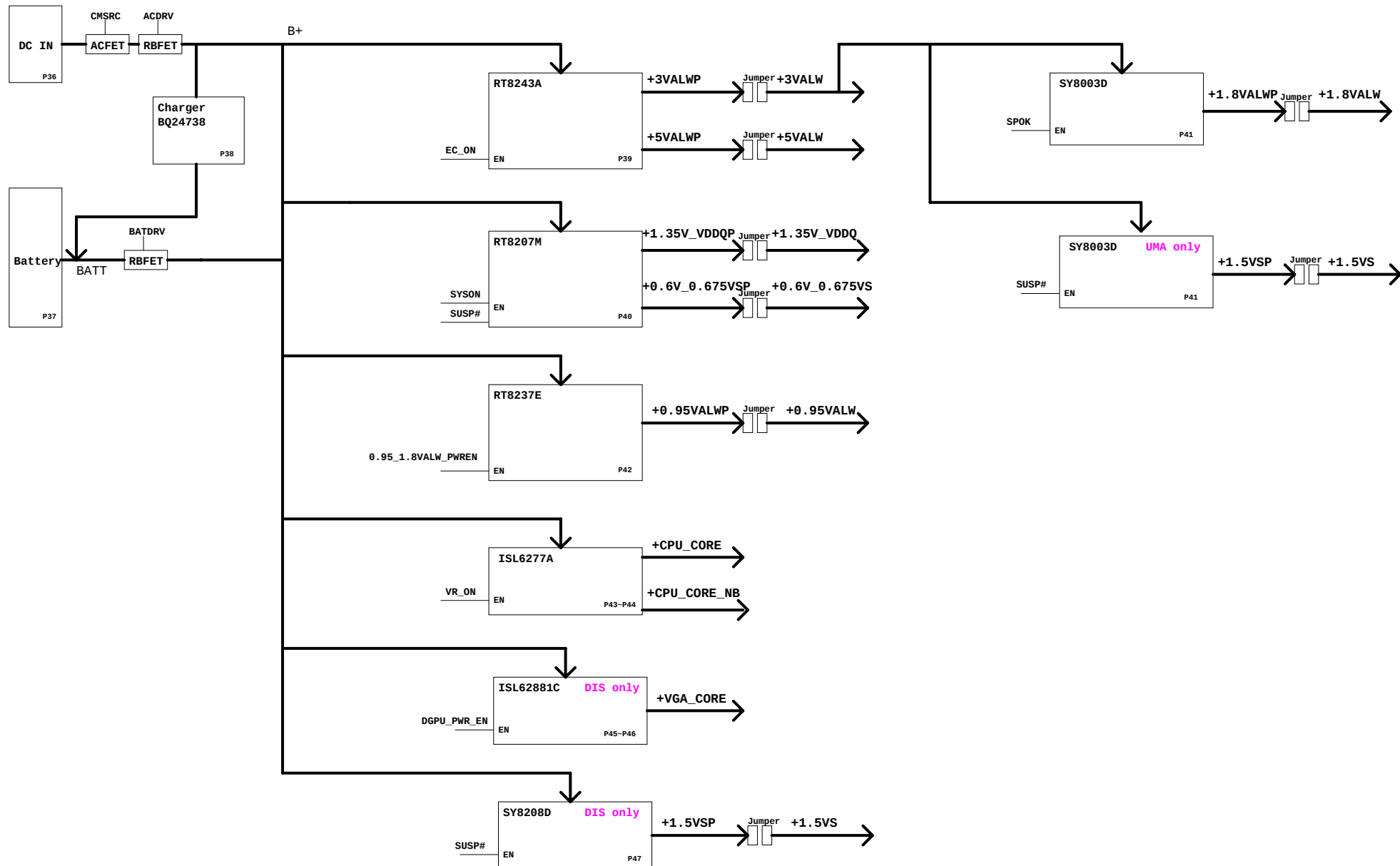




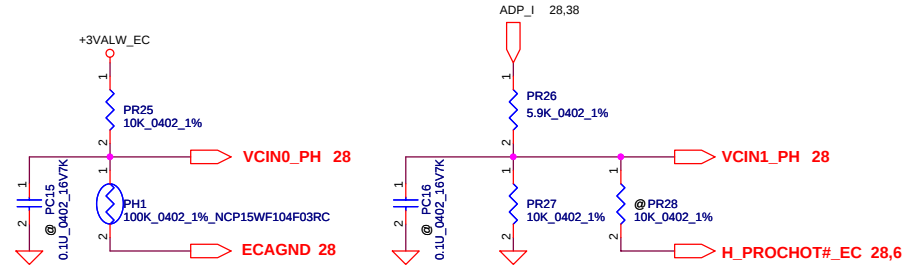
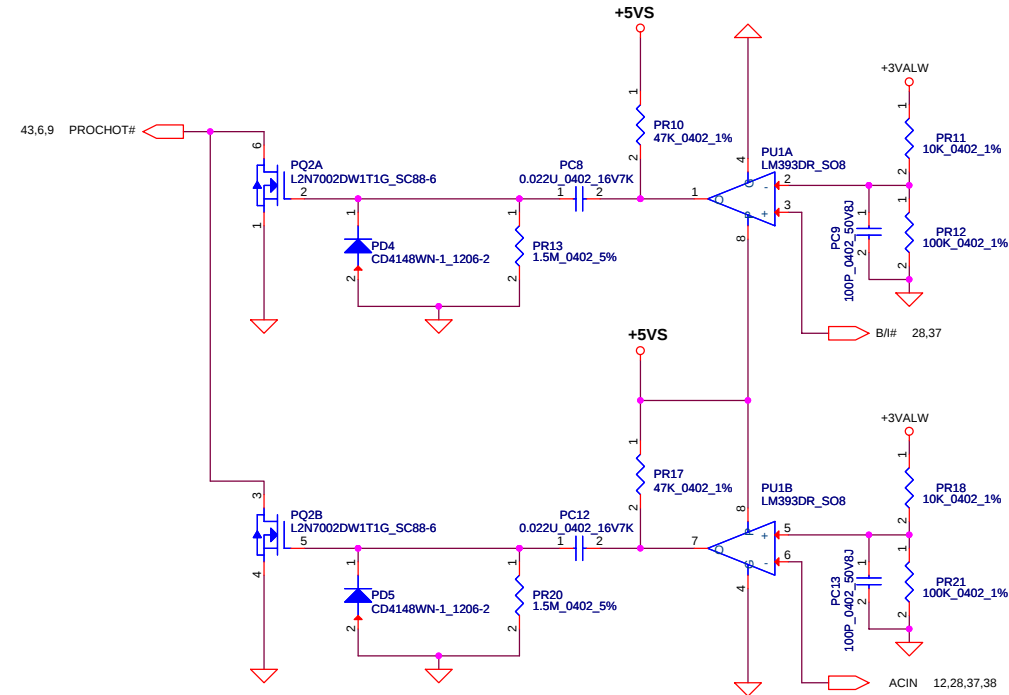
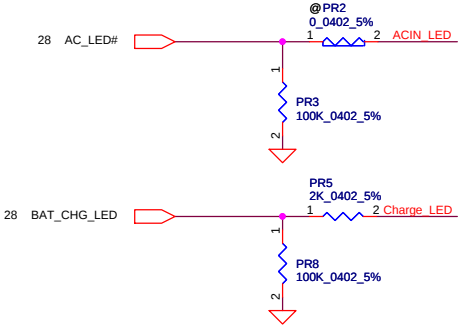
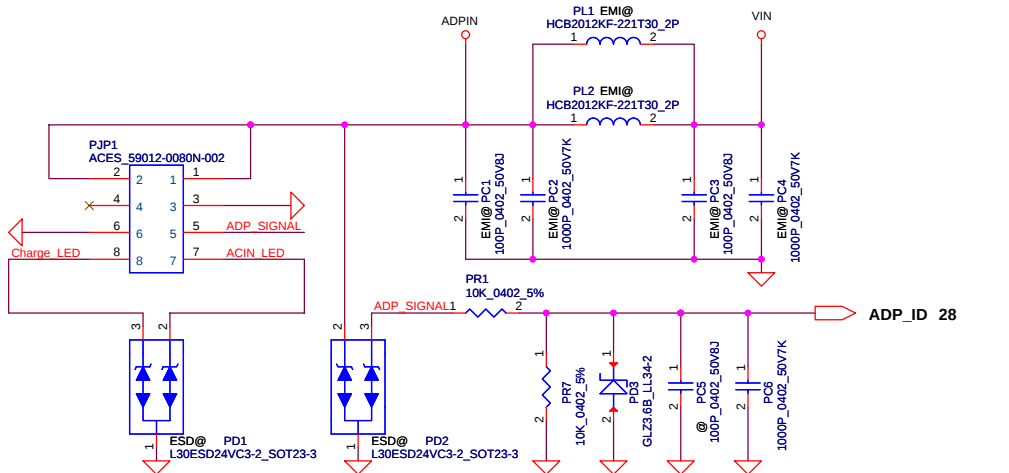
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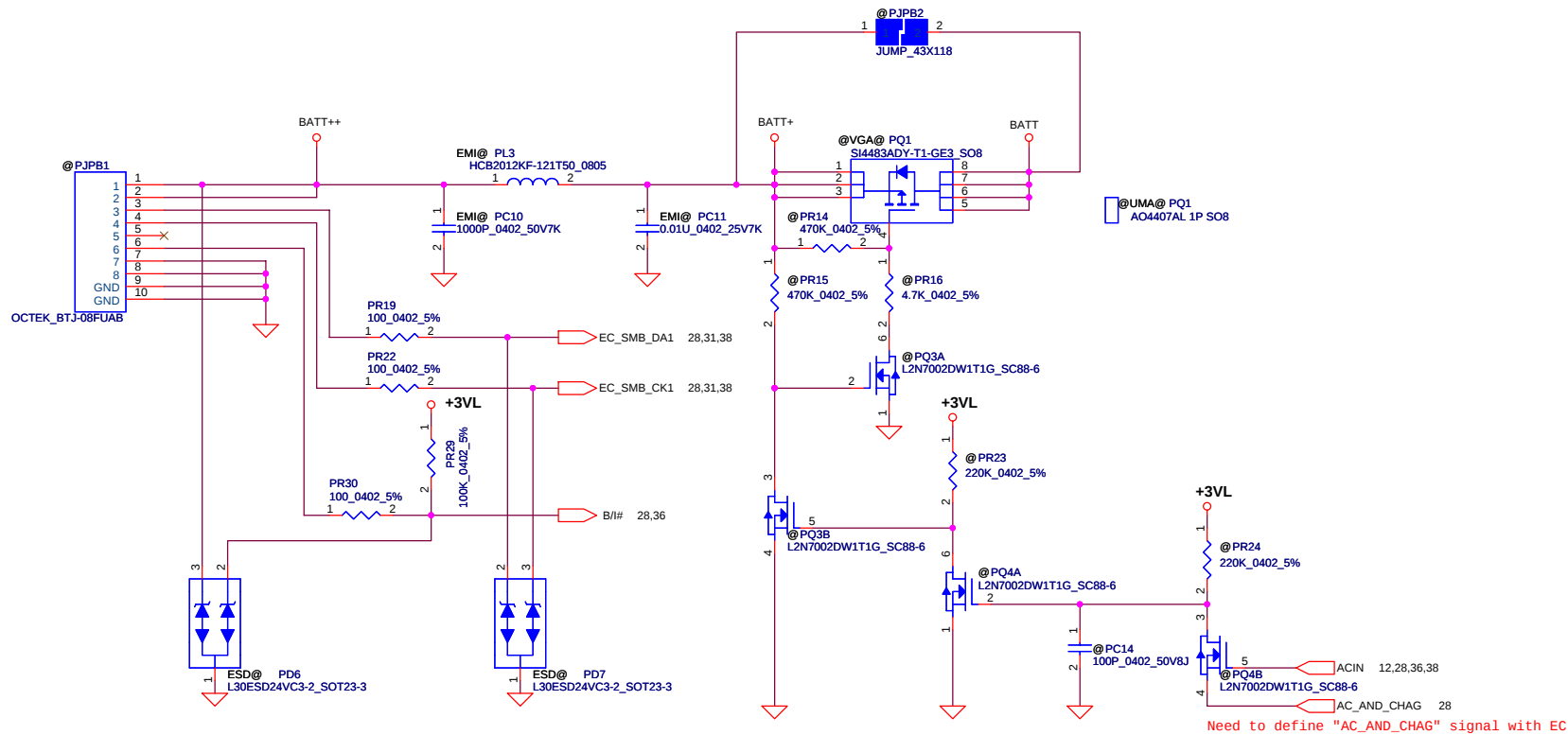
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	EE Change list
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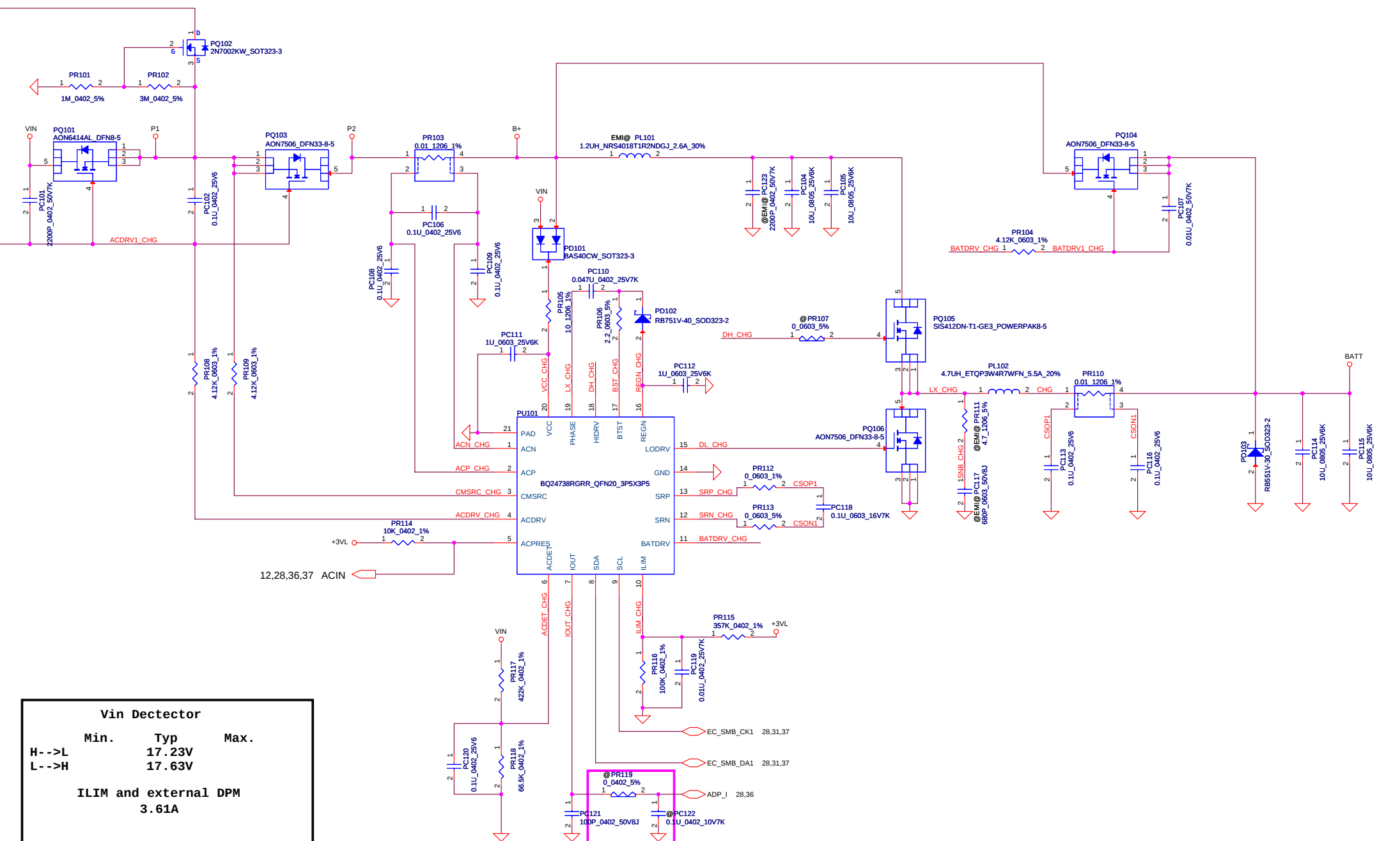
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				Document Number	Rev
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				Date:	Tuesday, February 25, 2014
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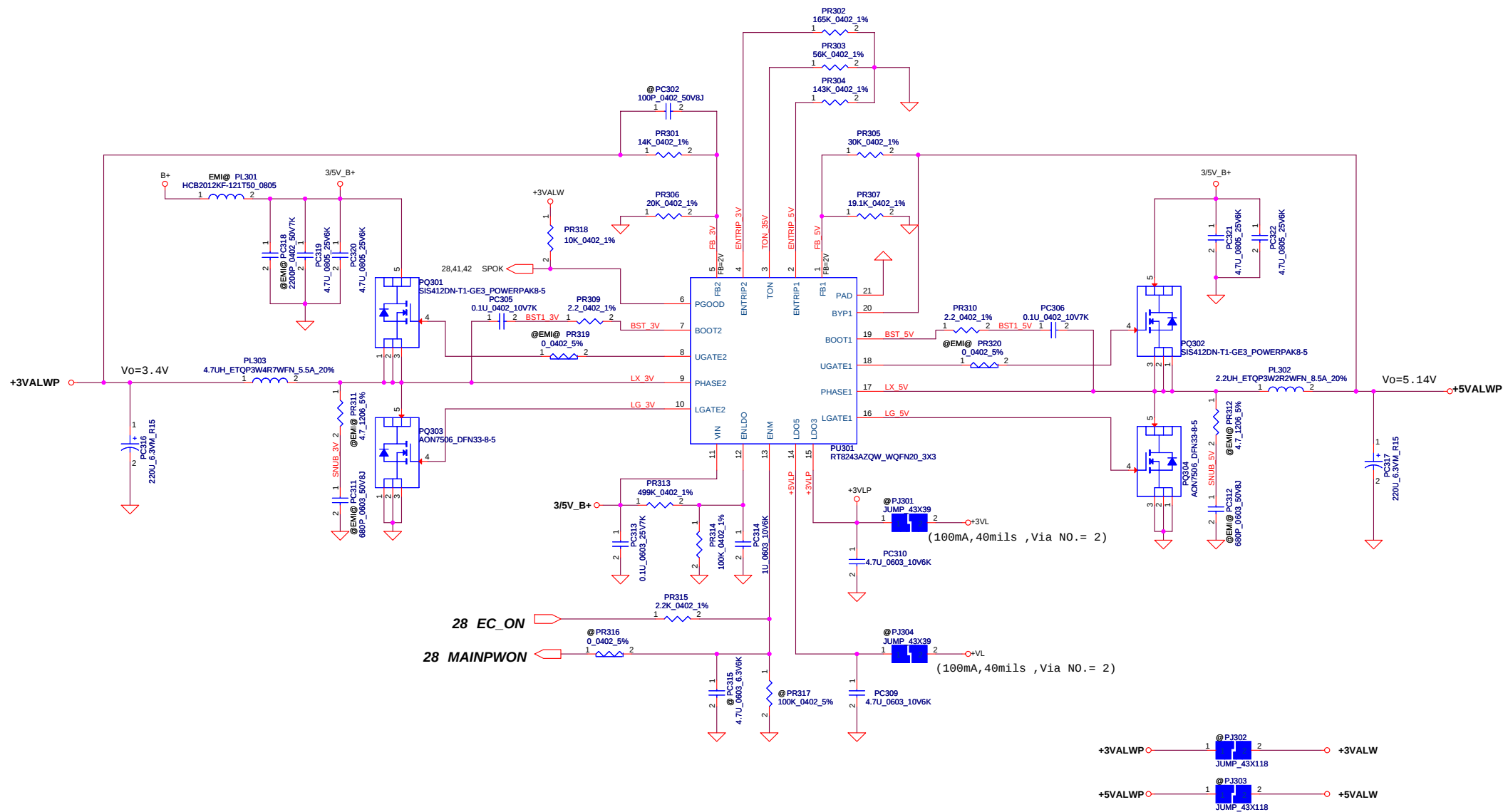
Vin Detector

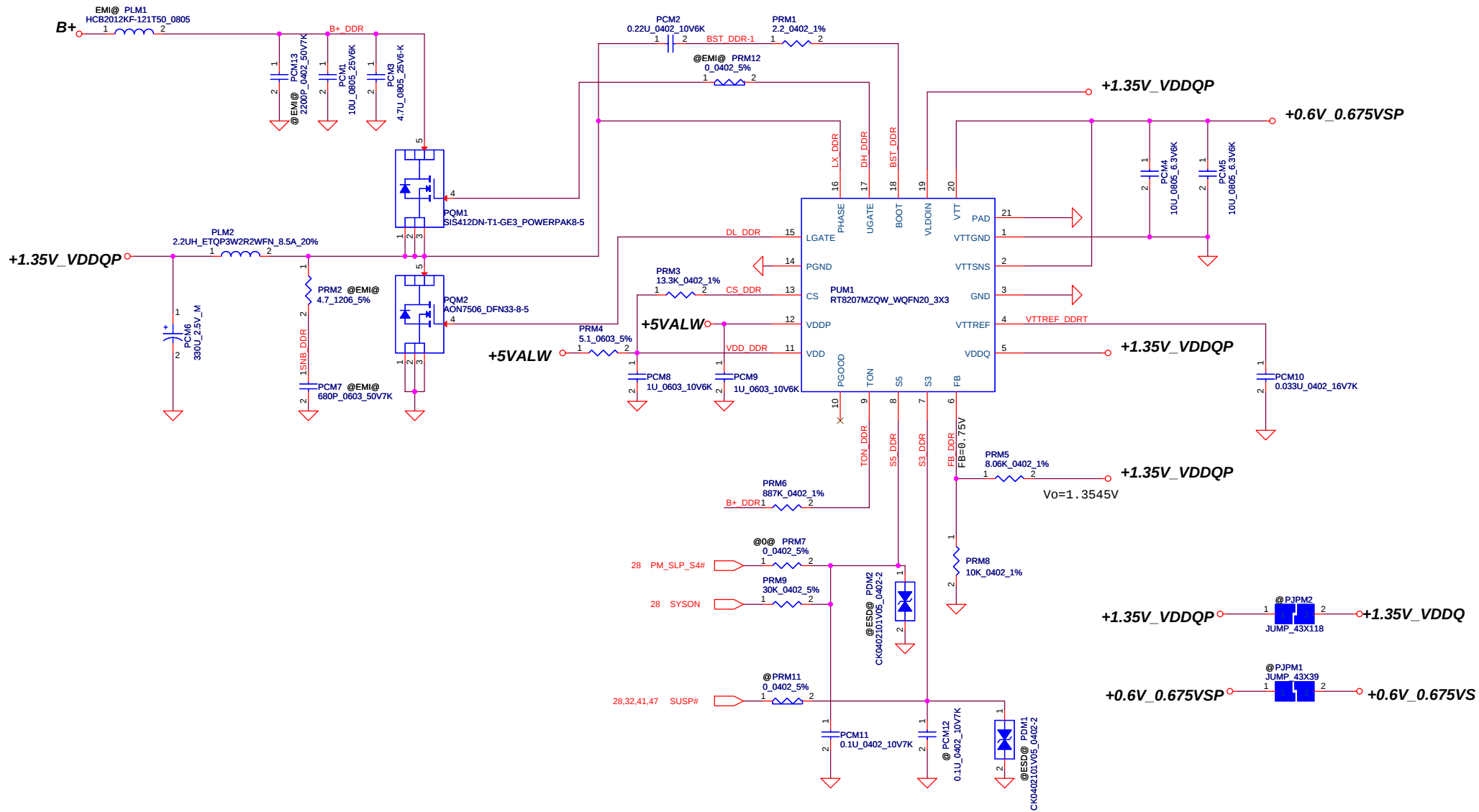
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H-->L		17.23V	
L-->H		17.63V	

ILIM and external DPM

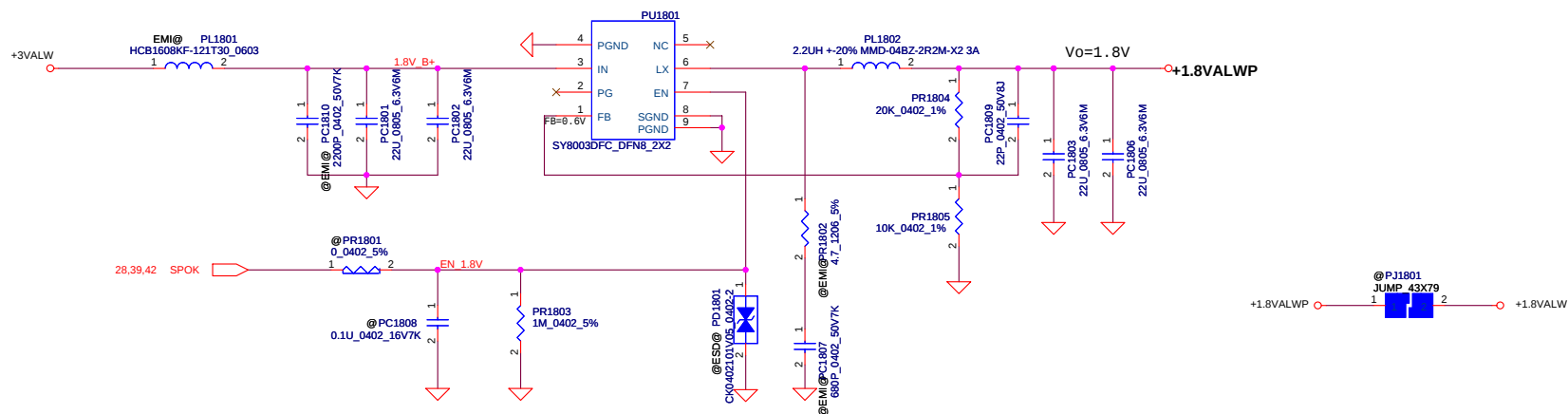
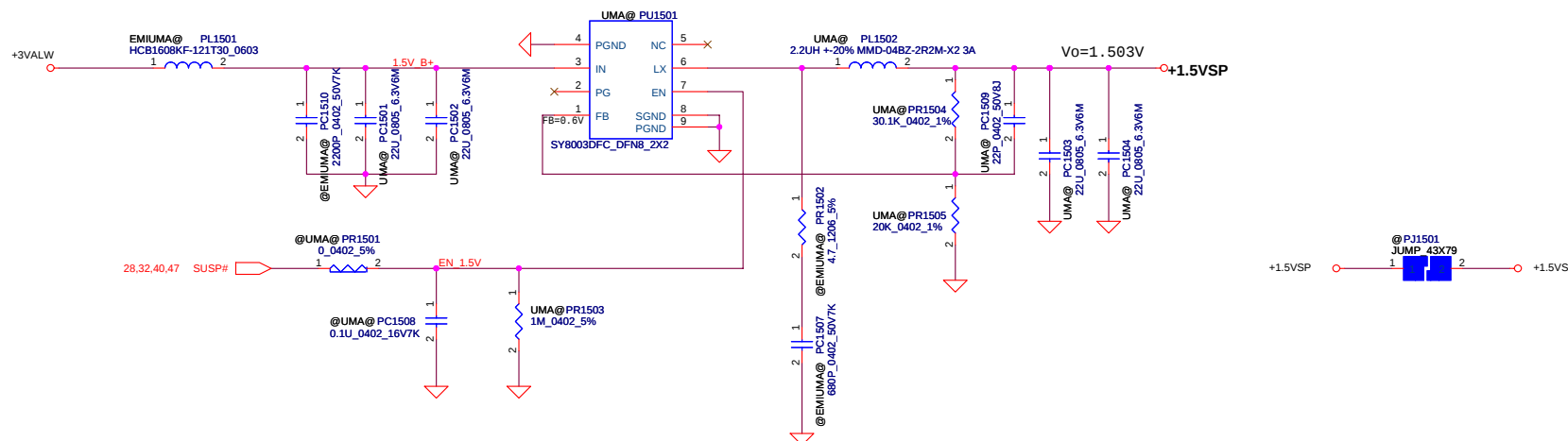
3.61A

Please locate the RC
Near EC chip
2011-02-22

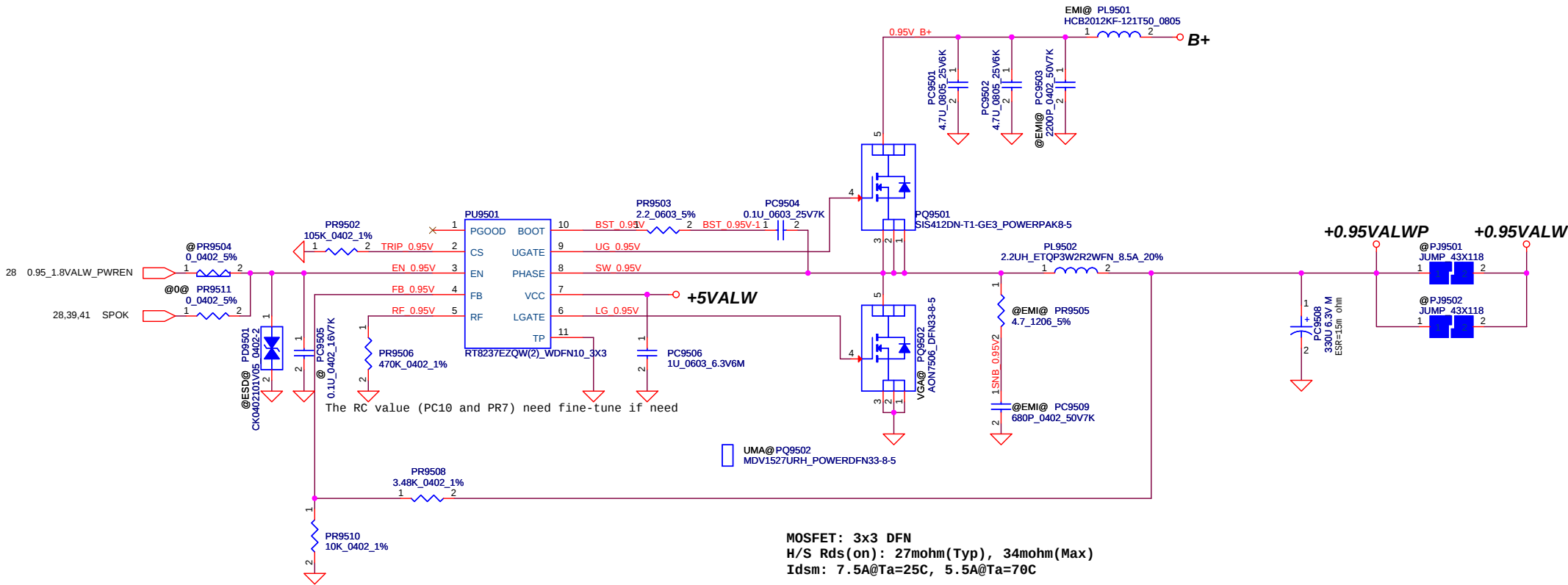




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MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

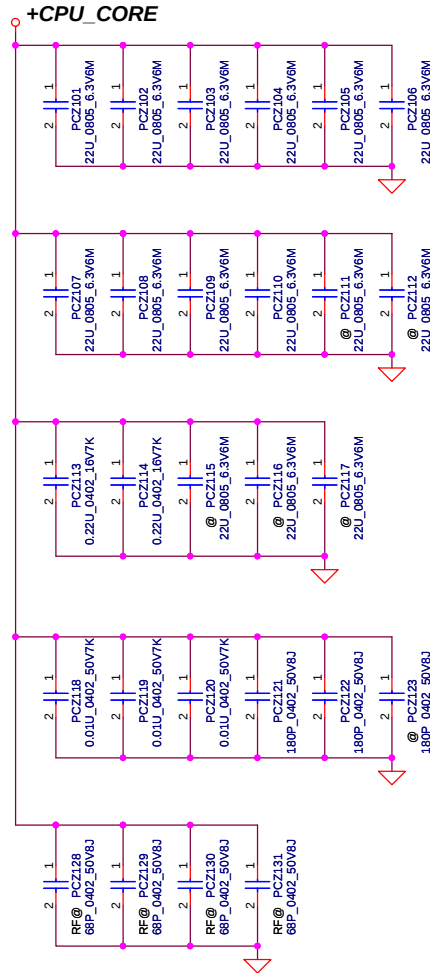
L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=15.5mohm +/-15%

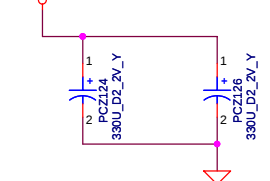
Switching Frequency: 290kHz
Imax=8A
OCP~10.977A
OVP: 120%~130%
VFB=0.704V, Vout=0.949V
MOSFET footprint: SIS412DN

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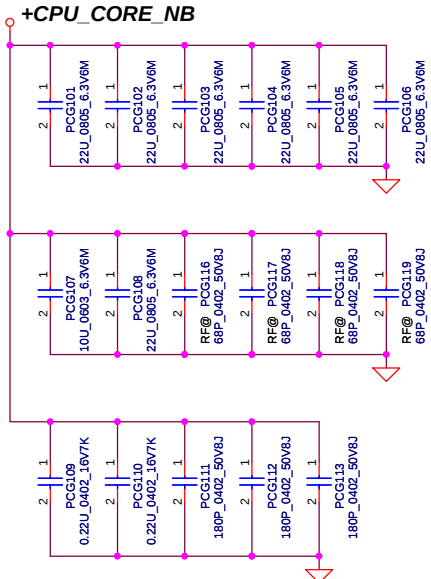
+CPU_CORE



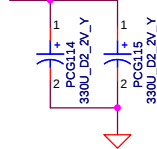
+CPU_CORE Local



+CPU_CORE_NB



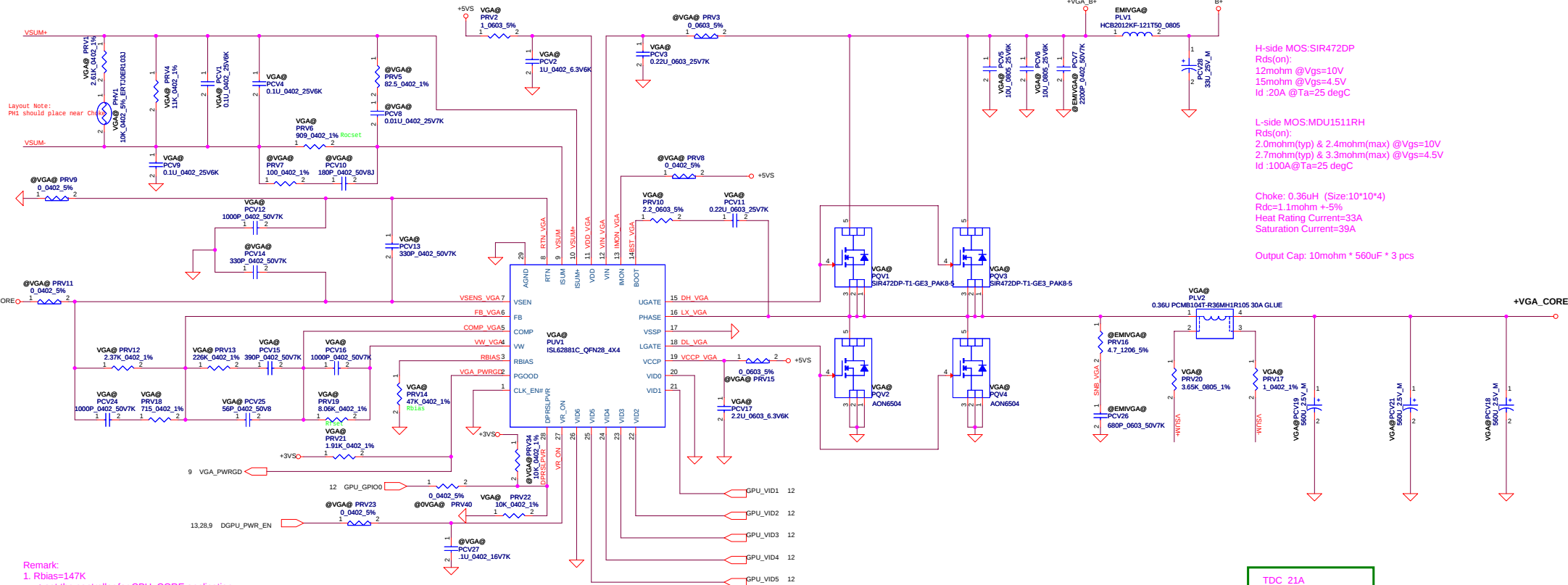
+CPU_CORE_NB Local



	330uF/9m	22uF/0805	0.22uF/0402	10uF/0603	0.01uF/0402	180pF/0402
+CPU_CORE	2	10	2		3	2
+CPU_CORE_NB	2	7	2	1		3

GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Vboot(merge)



H-side MOS: SIR472DP
Rds(on):
12mohm @Vgs=10V
15mohm @Vgs=4.5V
Id: 20A @Ta=25 degC

L-side MOS: MDU1511RH
Rds(on):
2.0mohm(typ) & 2.4mohm(max) @Vgs=10V
2.7mohm(typ) & 3.3mohm(max) @Vgs=4.5V
Id: 100A @Ta=25 degC

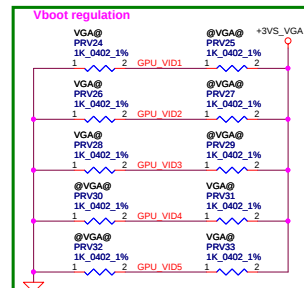
Choke: 0.36uH (Size: 10*10*4)
Rdc=1.1mohm +5%
Heat Rating Current=33A
Saturation Current=39A

Output Cap: 10mohm * 560uF * 3 pcs

Remark:
1. Rbias=147K
=>set the controller for CPU_CORE application
Rbias=47K
=>set the controller for GPU_CORE application

2. Switching frequency setting:
Rset(kohm)=[period(us)-0.29]*2.65
=8.06Kohm
Fsw=1/period(us)=300KHZ

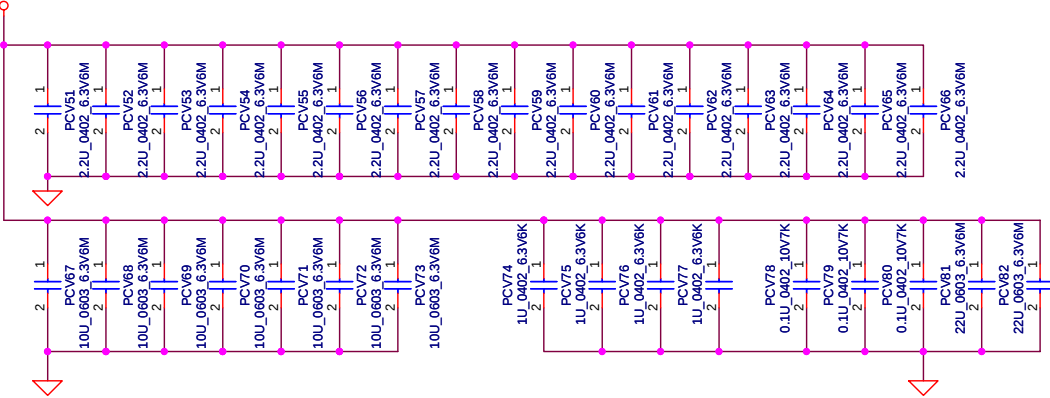
3. Operation mode:
when GPU_CORE VR application
DPRSLPVR (pin28)=0 => 1 phase CCM mode
DPRSLPVR (pin28)=1 => 1 phase DE mode



Module model information:
ISL62881C_V1A for IC
ISL62881C_V1B for SW

TDC 21A
Peak Current = 31.5A
OCP Current = 37.8A
Load line disable

+VGA_CORE



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