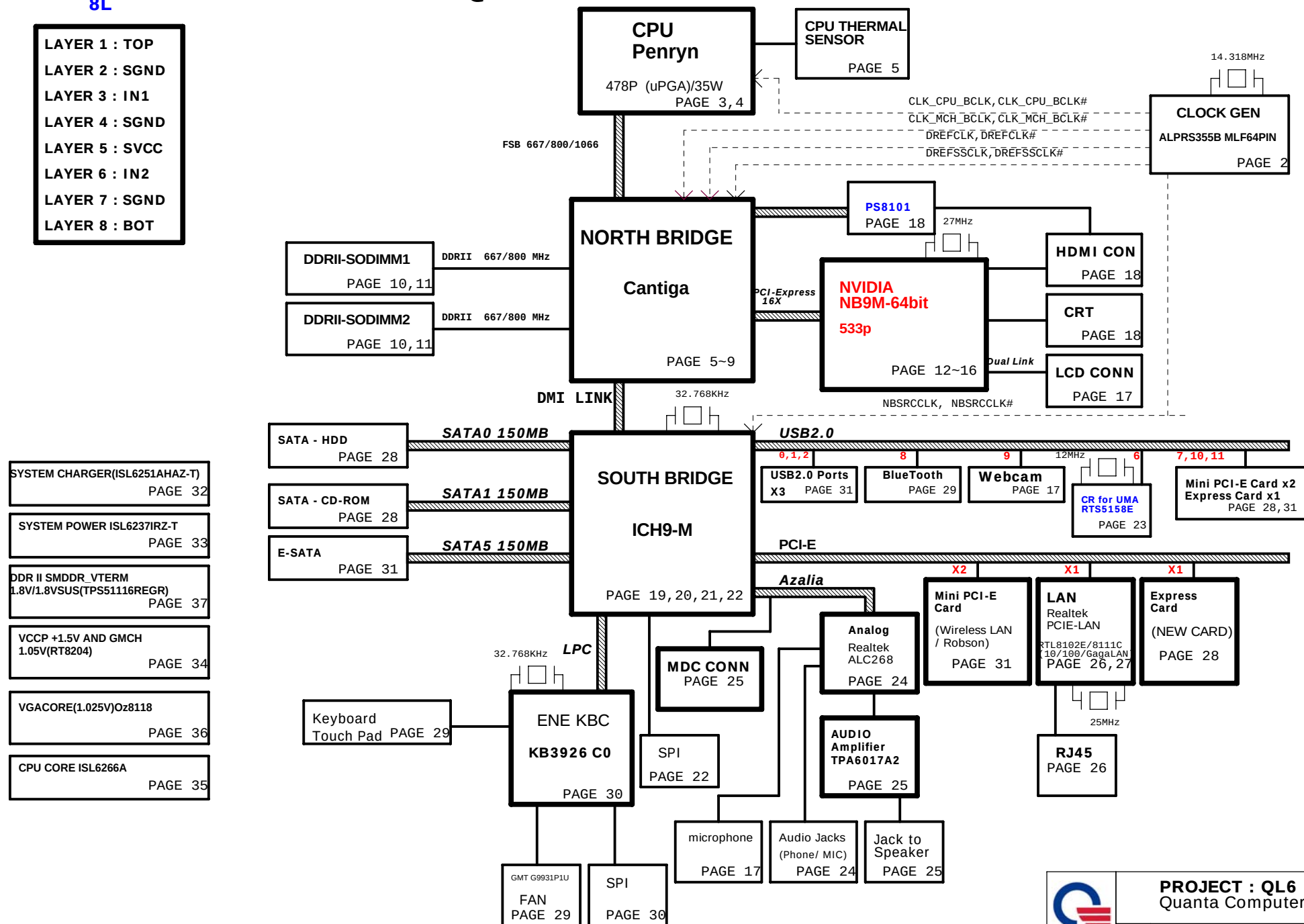
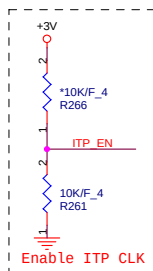
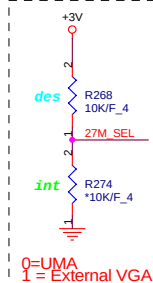
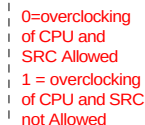


01

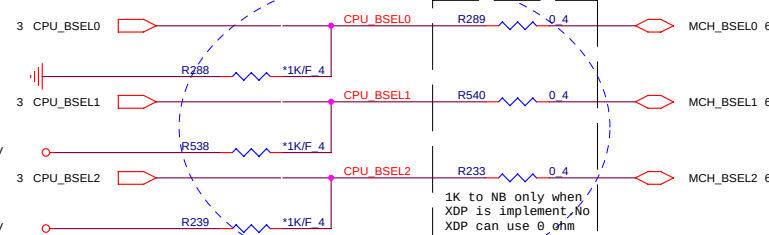
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SGND
LAYER 5 : SVCC
LAYER 6 : IN2
LAYER 7 : SGND
LAYER 8 : BOT





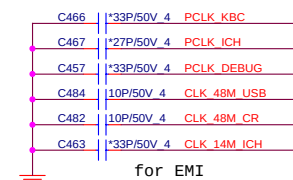
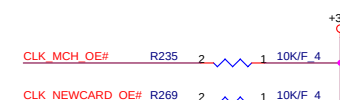
27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDDT_100	SRCT1/LCDDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

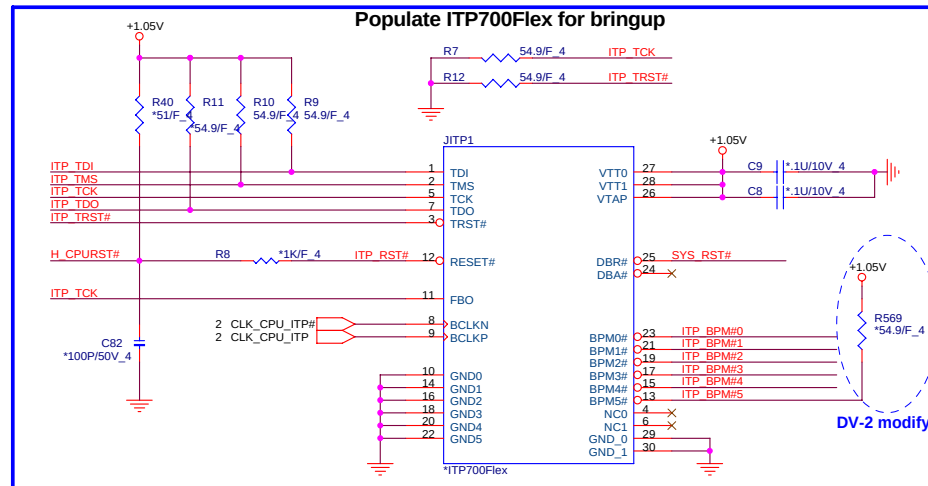
DV-2 modify

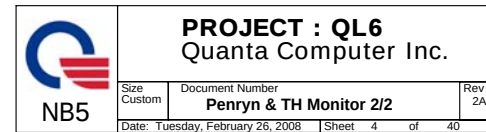


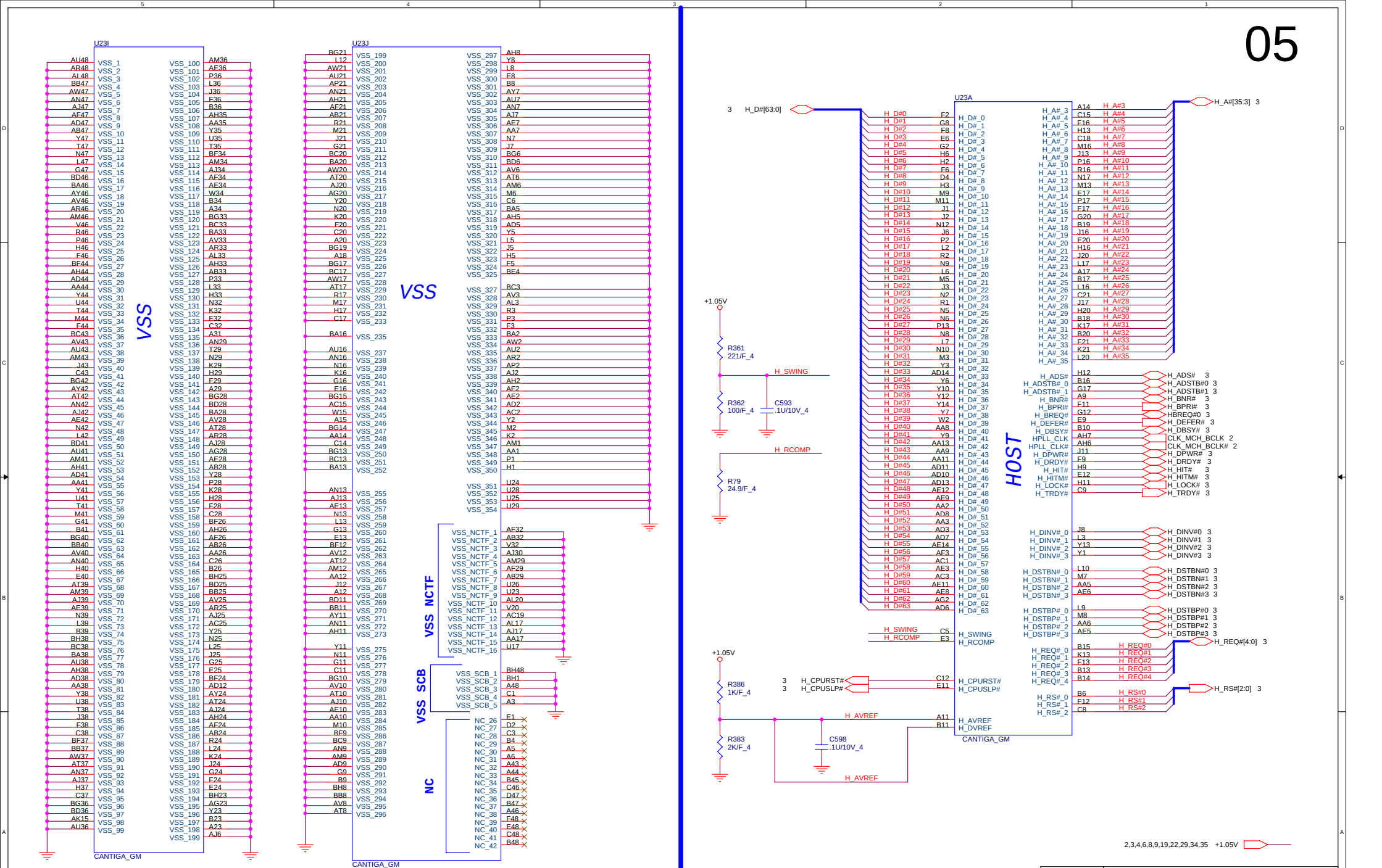
ICS	ICS9LPRS355BKLF	ALPRS355000
Silego	SLG8SP513VTR	AL8SP513000
Realtek	RTM875N-606-VD-GR	AL000875000

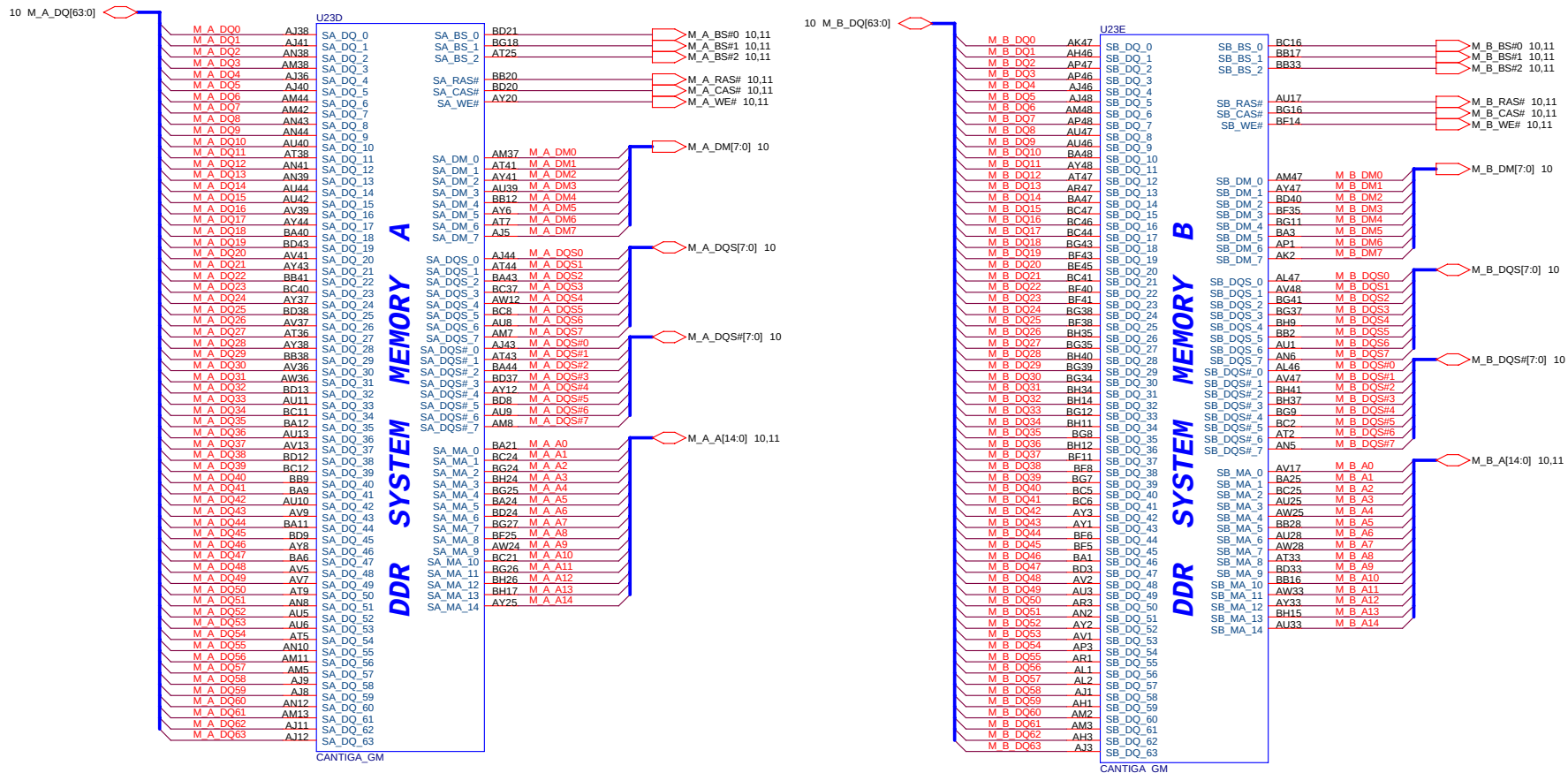
FSC	FSB	FSA	CPU	SRC	PO
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

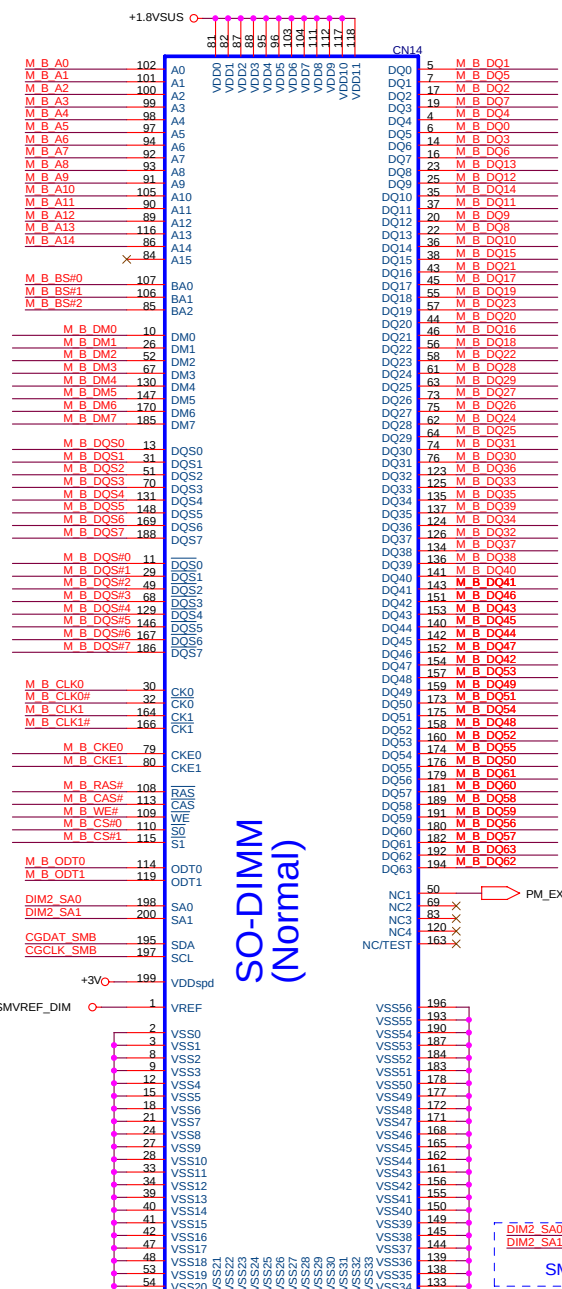




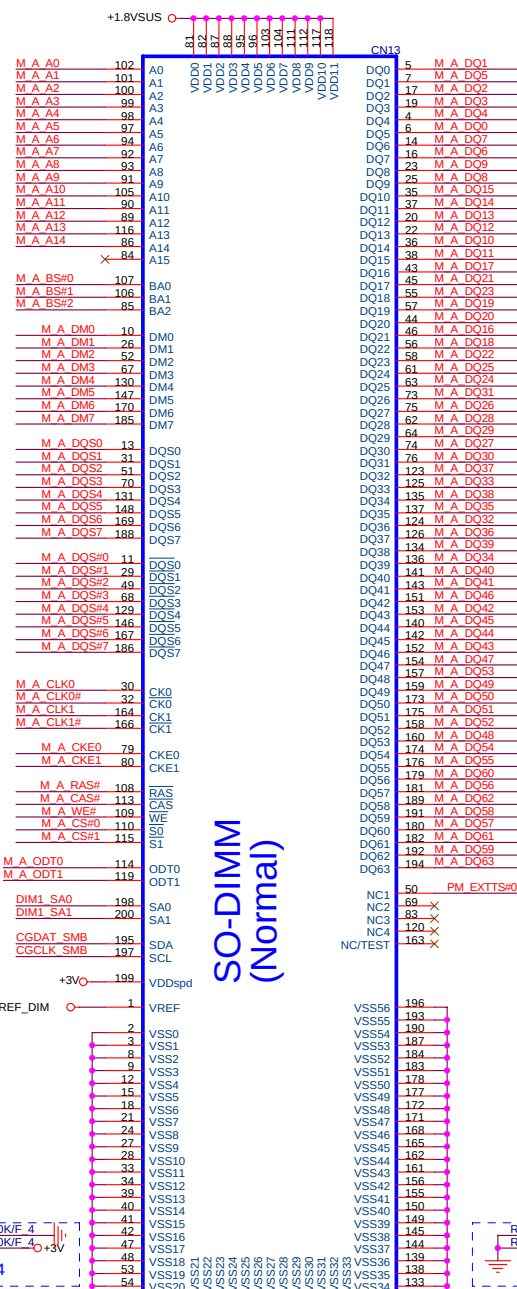




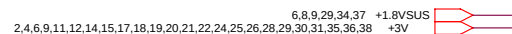
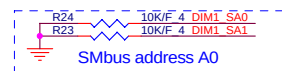
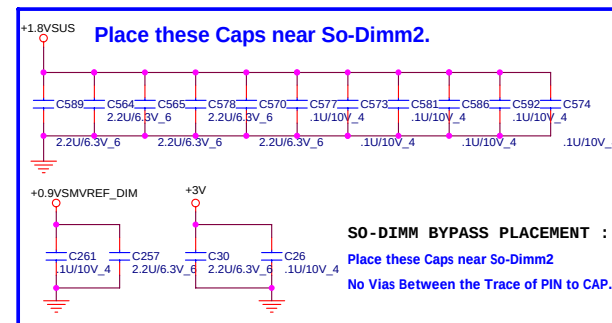
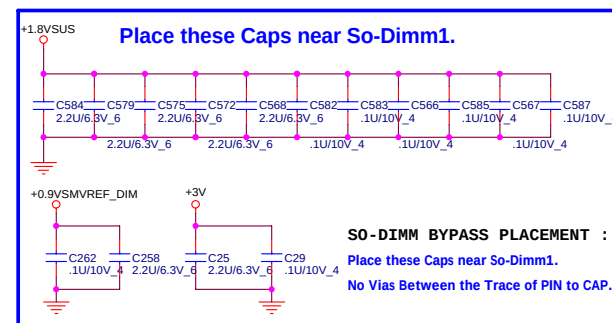
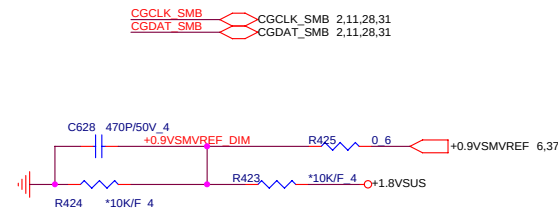
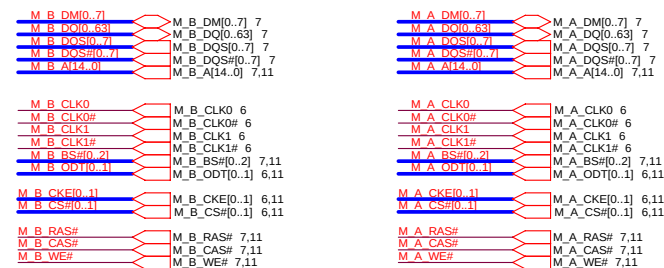




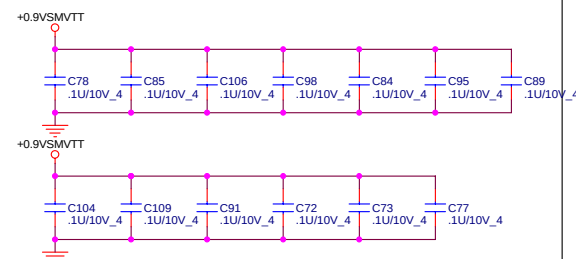
H 9.2



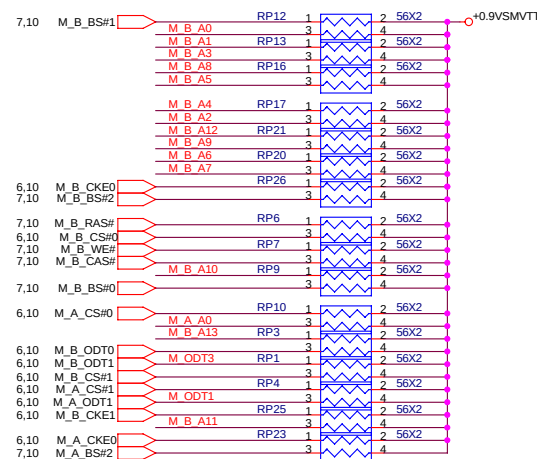
H 5.2



DDRII B CHANNEL

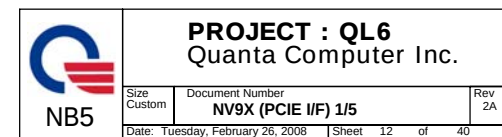


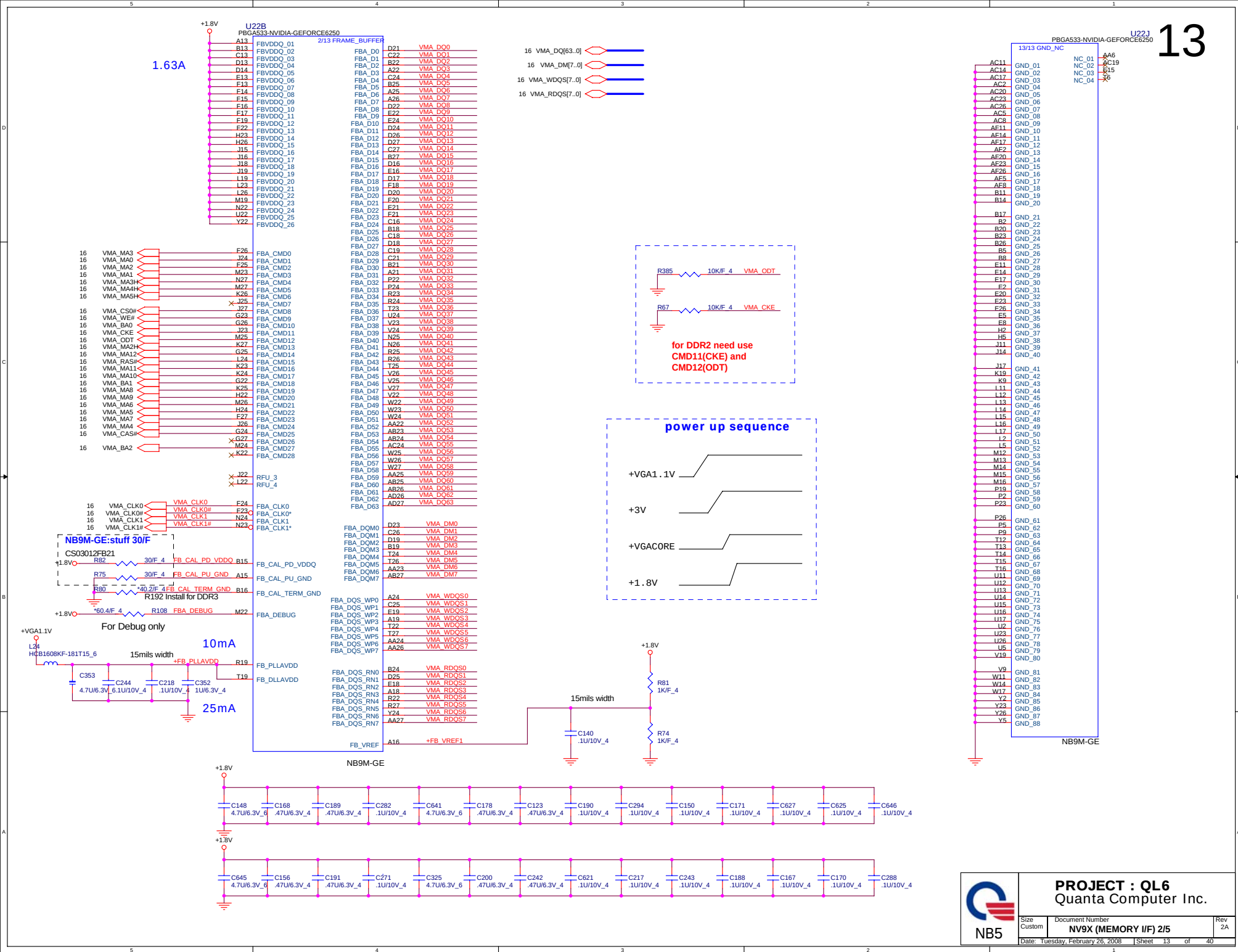
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

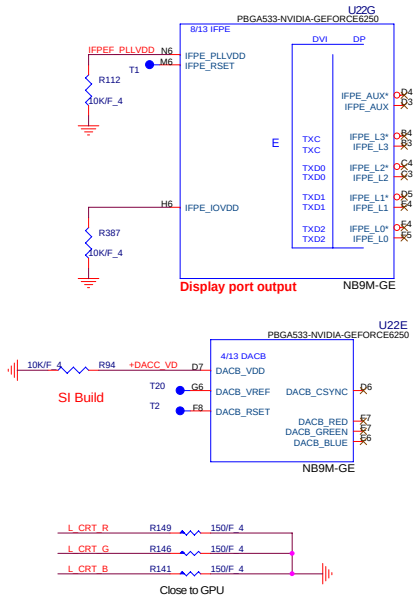
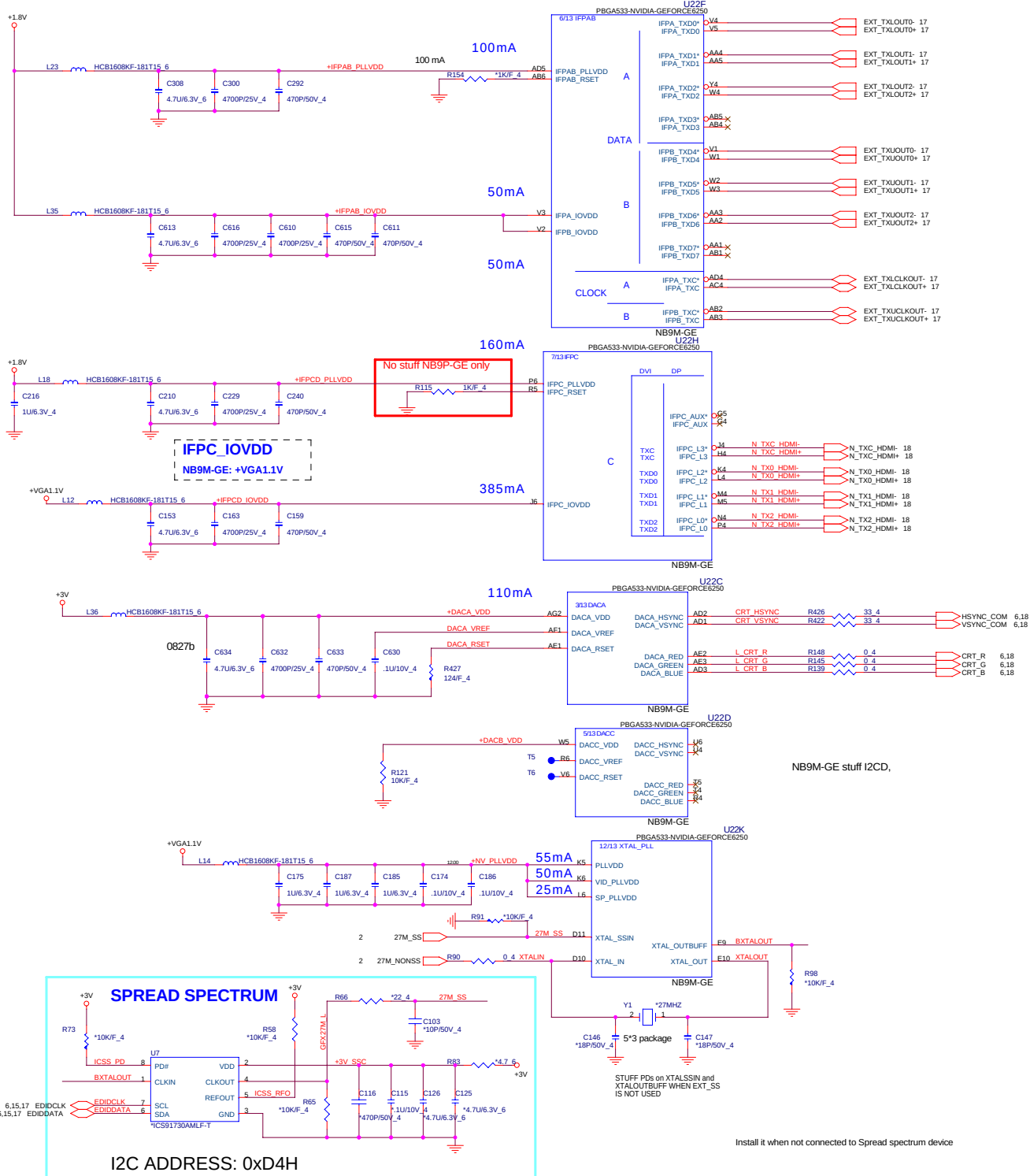


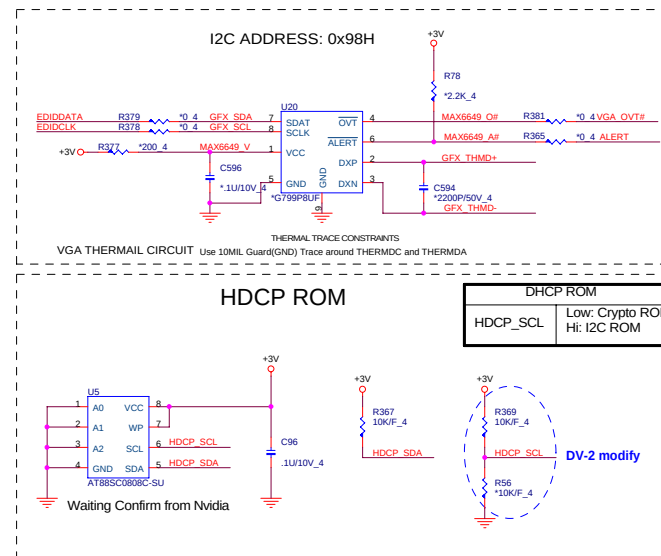
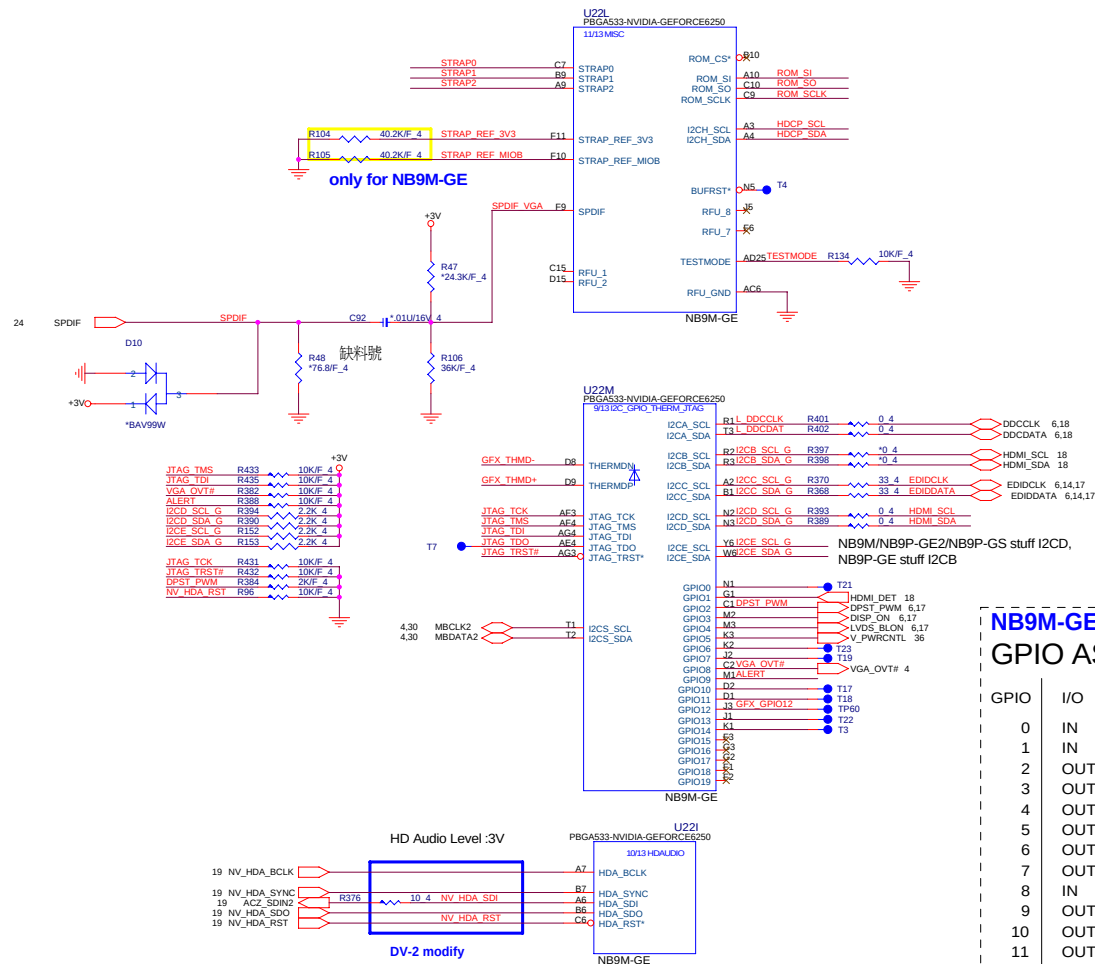
M A A[14..0] M A A[14..0] 7.10





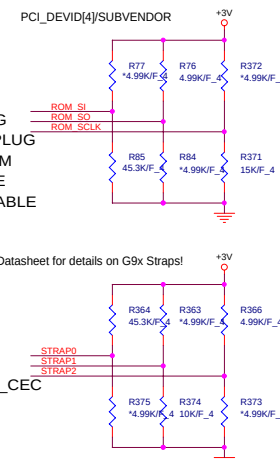






NB9M-GE (G98) Straps

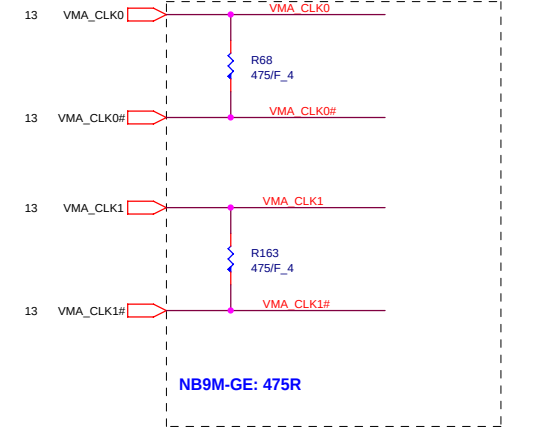
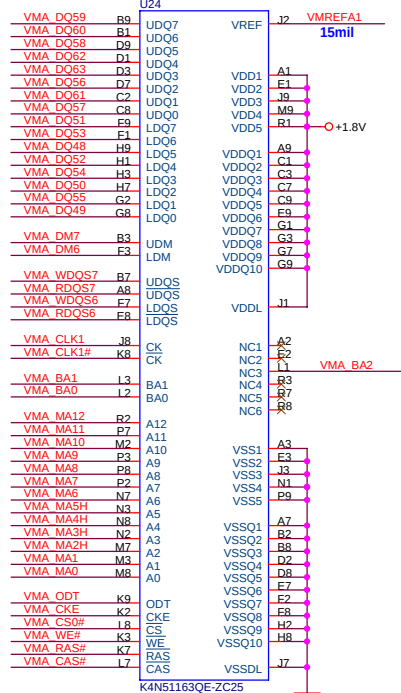
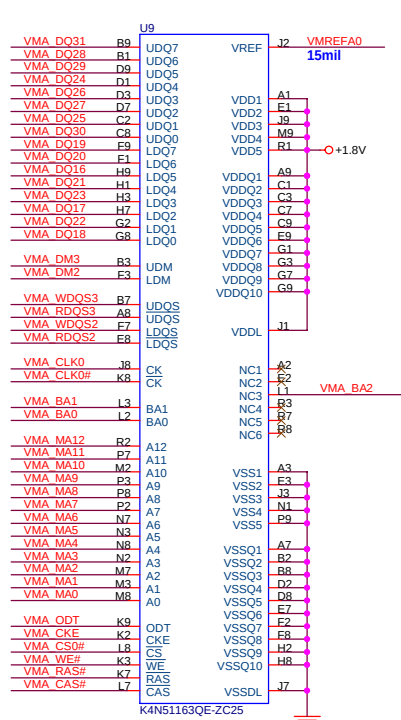
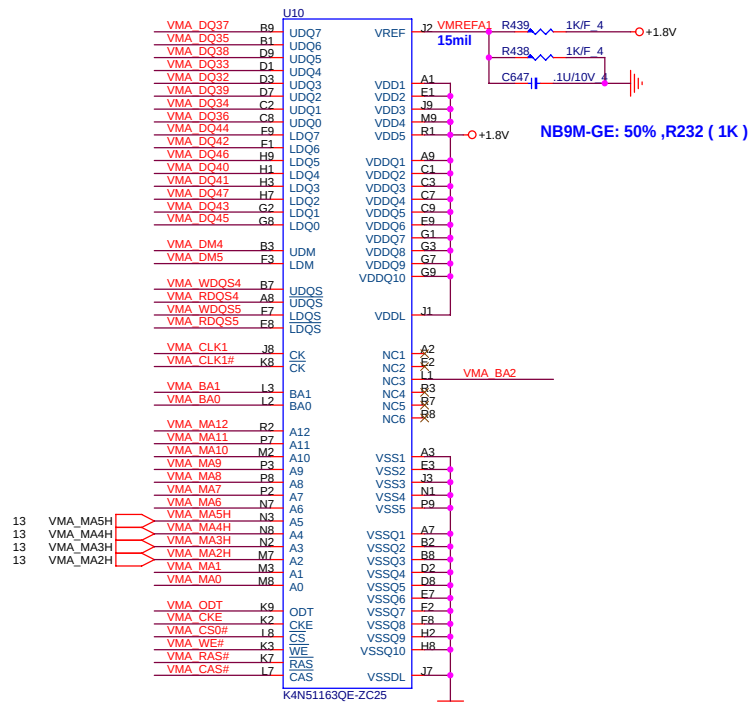
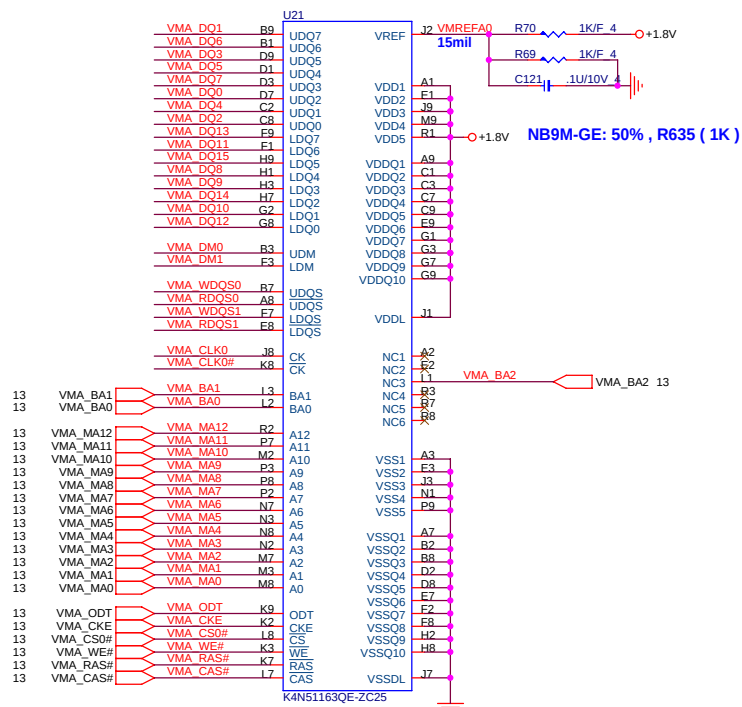
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



VRAM ID	
ROM_SI	PD 30K: Samsung PD 35K: Qimonda PD 45K: Hynix

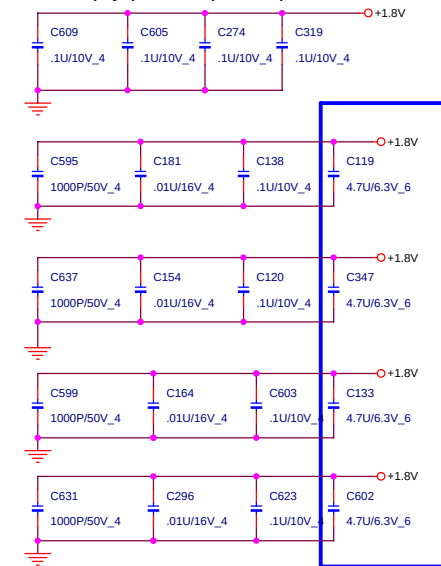
Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



CS14752FB11 RES CHIP 475 1/16W +-1%(0402)

(By pass capacitor)



13 VMA_DQ[63..0]  

13 VMA_DM[7..0]  

13 VMA_WDQS[7..0]  

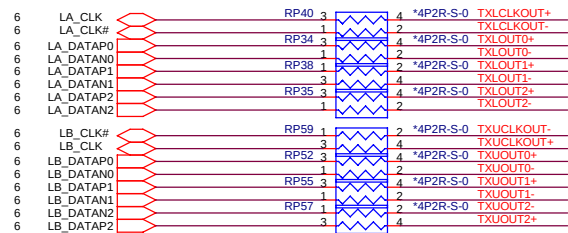
13 VMA_RDQS[7..0]  

256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01

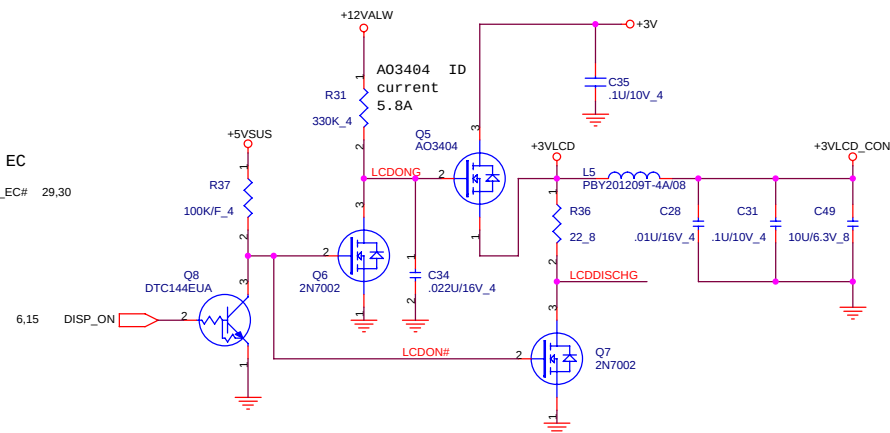
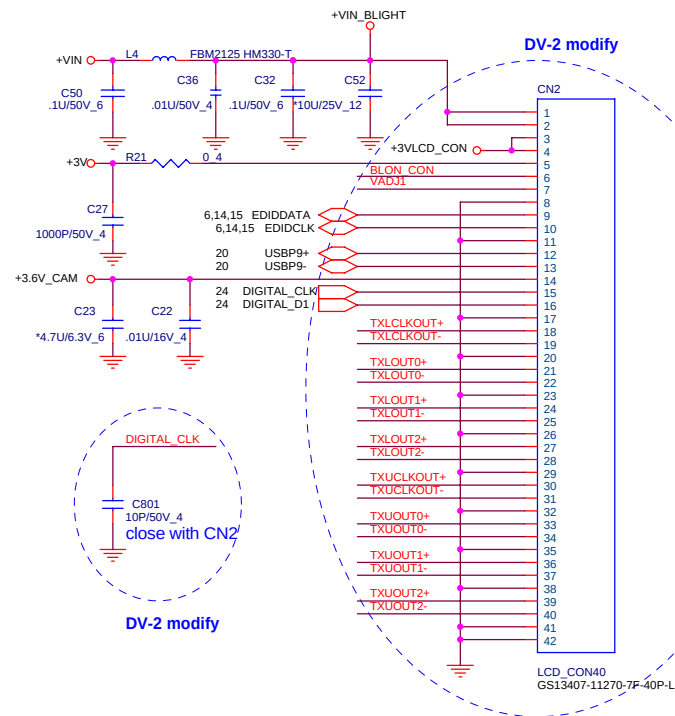
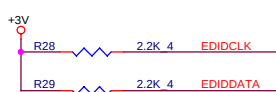
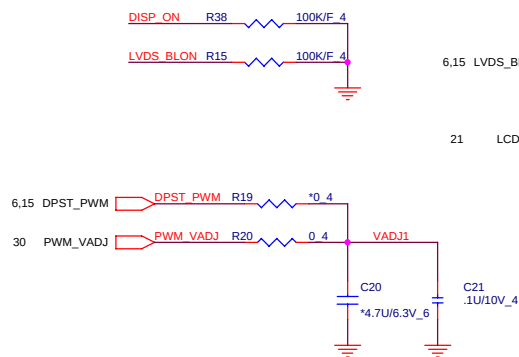
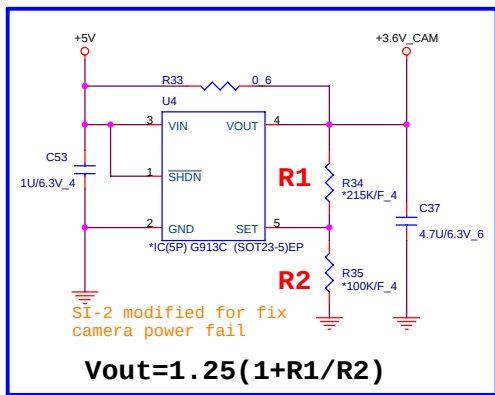
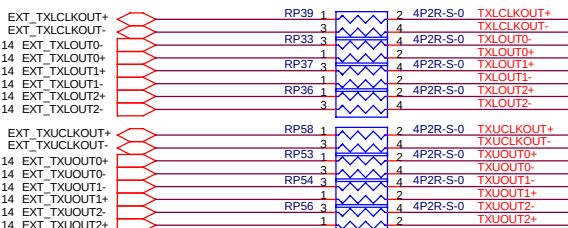
NB9M : AKD5FG-TW31(Hynix,32M*16)
AKD5FG-T^03(Qimonda 32M*16)

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

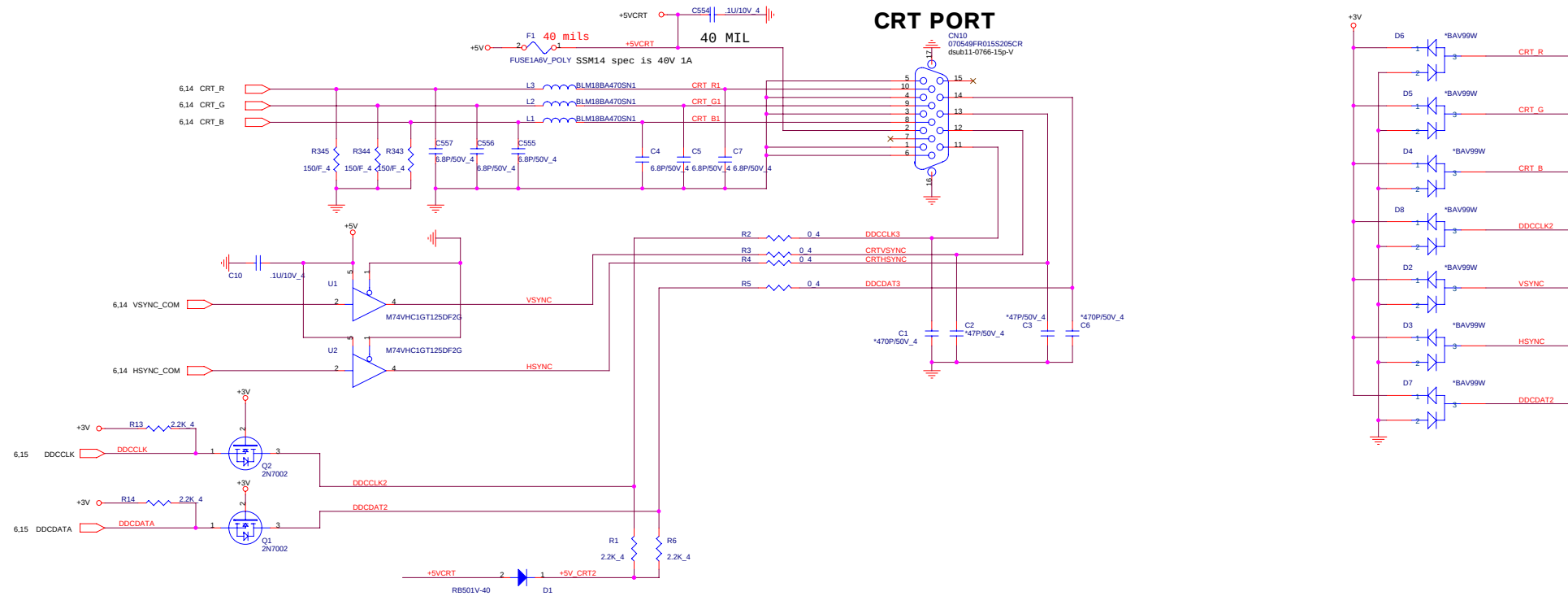
OPTION SIGNAL FROM NB FOR UMA VGA



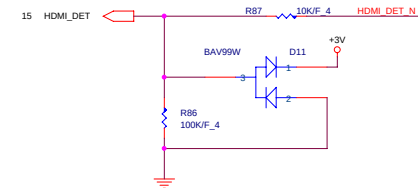
OPTION SIGNAL FROM Nvidia to VGA



CRT PORT



HDMI PORT

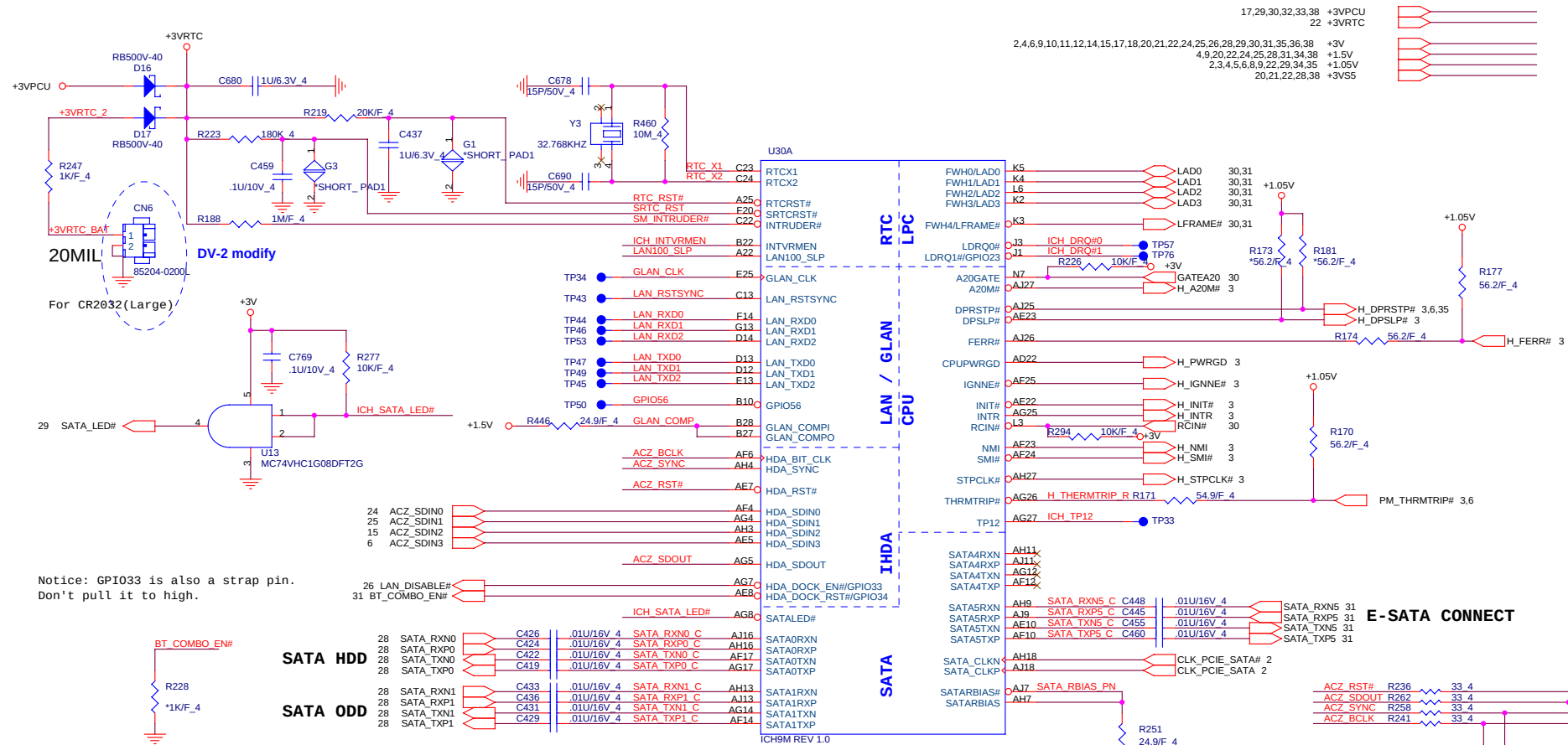


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for EMI request

```

PROJECT : QL6
Quanta Computer Inc.



SB Strap

ICH9-M Internal VR Enable strap
(Internal VR for Vccsus1_05, VccSus1_5 and VccCL1_5)

ICH9-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

INTVRMEN Low = Internal VR disable
High = Internal VR enable(Default)

LAN100_SLP Low = Internal VR disable
High = Internal VR enable(Default)

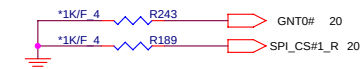
XOR Chain Entrance Strap

ICH_TP3	HDA_SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS select

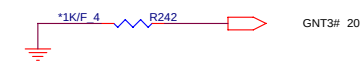
STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

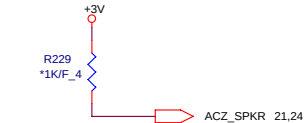


A16 swap override strap

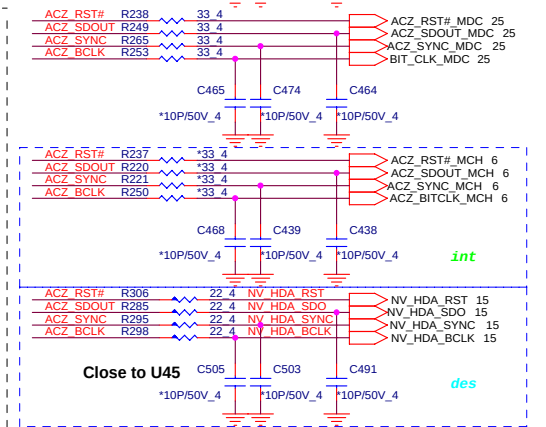
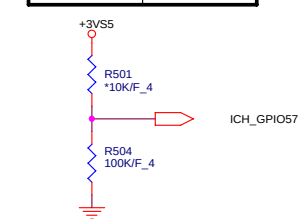
PCI_GNT#3	Low = A16 swap override enabled Hi = Default
-----------	---

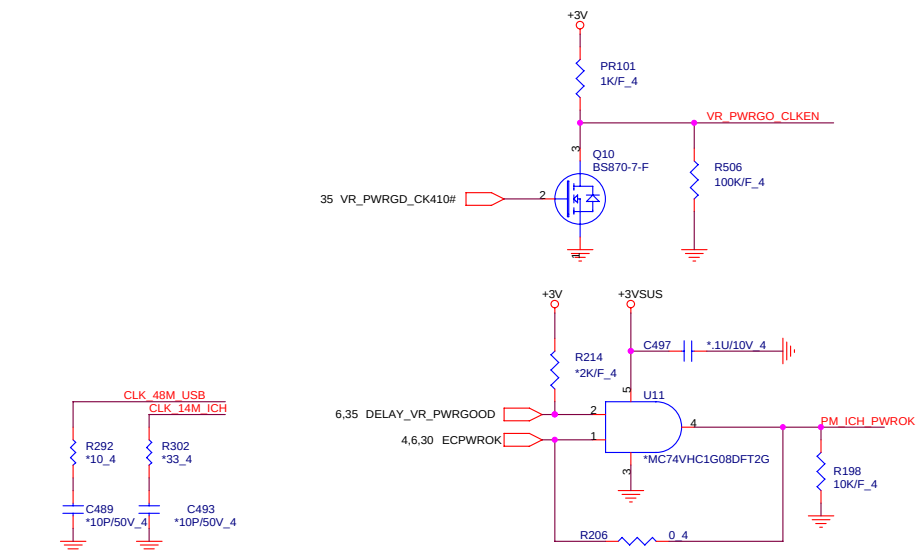
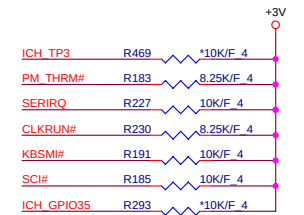
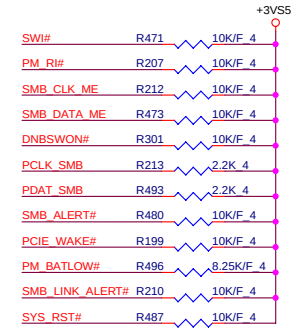
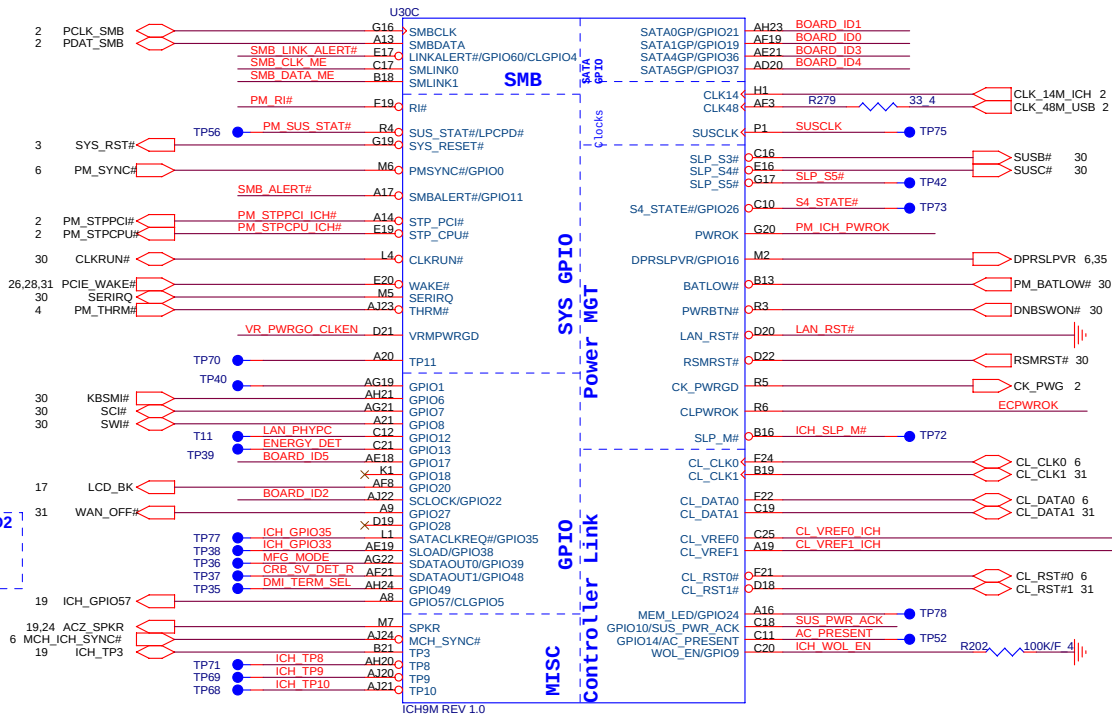


No Reboot Strap
ACZ_SPKR Low: Default Hi: No reboot

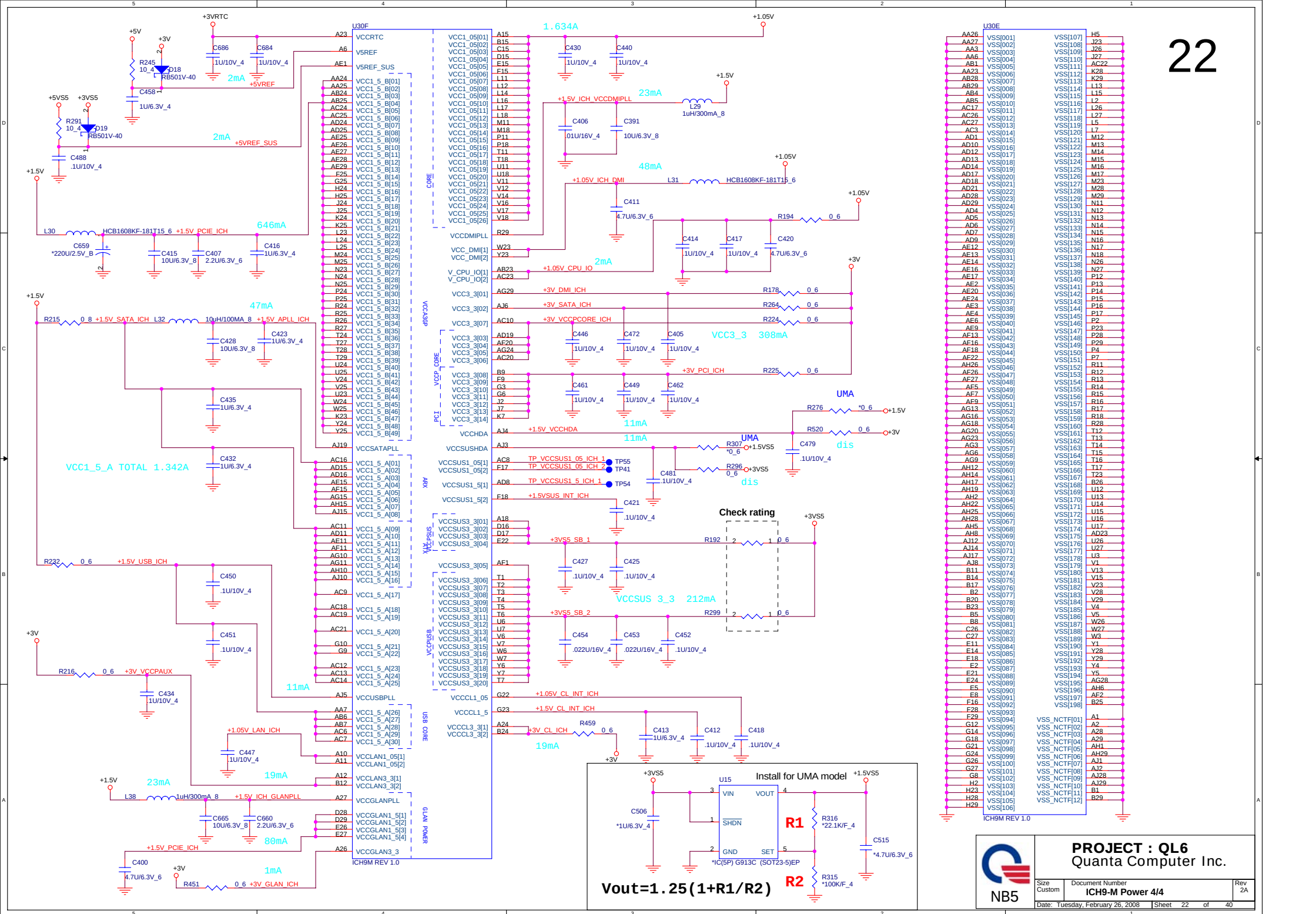


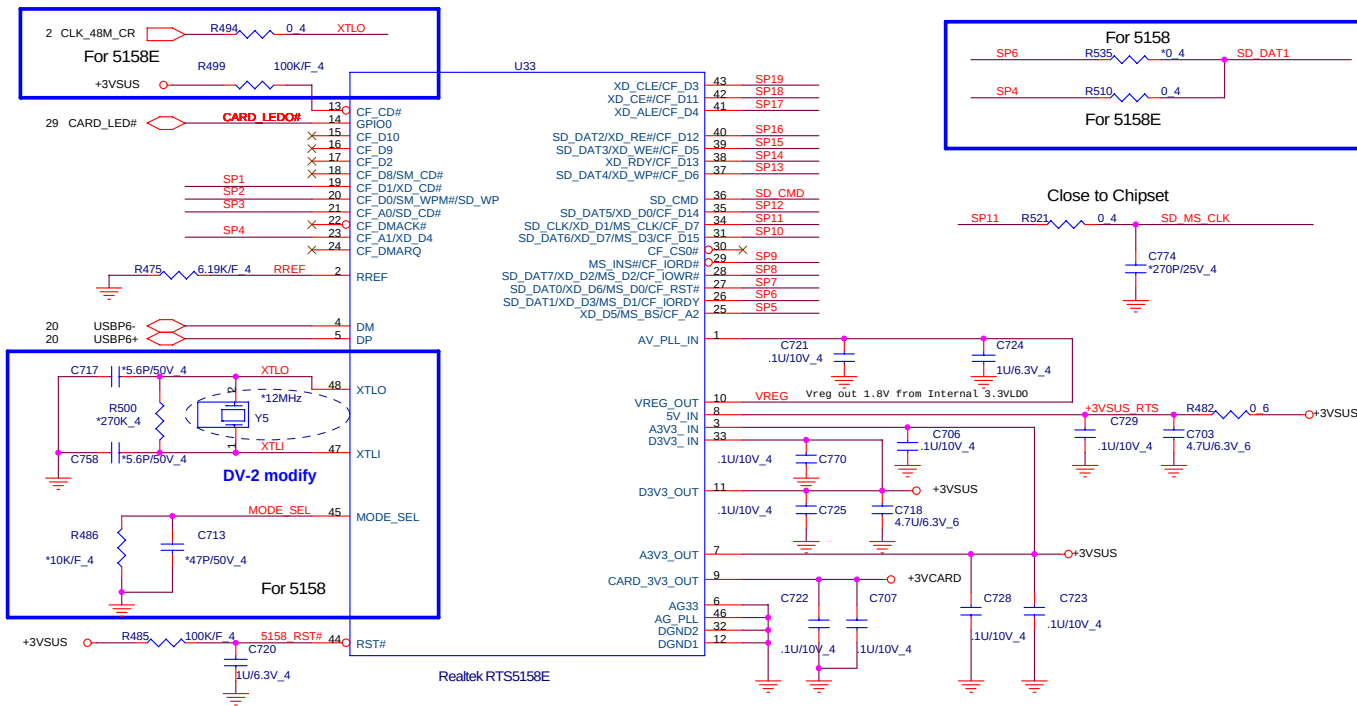
TPM physical presence
ICH_GPIO57 Low: Default





Model	Board ID 3	Board ID 2	Board ID 1	Board ID
QL8/GM	0	0	0	0
QL8/9M	0	0	0	1
QL8/9P	0	0	1	0
QL6/GM	0	0	1	1
QL6/9M	0	1	0	0
TW8/GM	0	1	0	1
TW8/9M	0	1	1	0
TW8/9P	0	1	1	1
SW8/GM	1	0	0	0
SW8/9M	1	0	0	1
DW8/GM	1	0	1	0



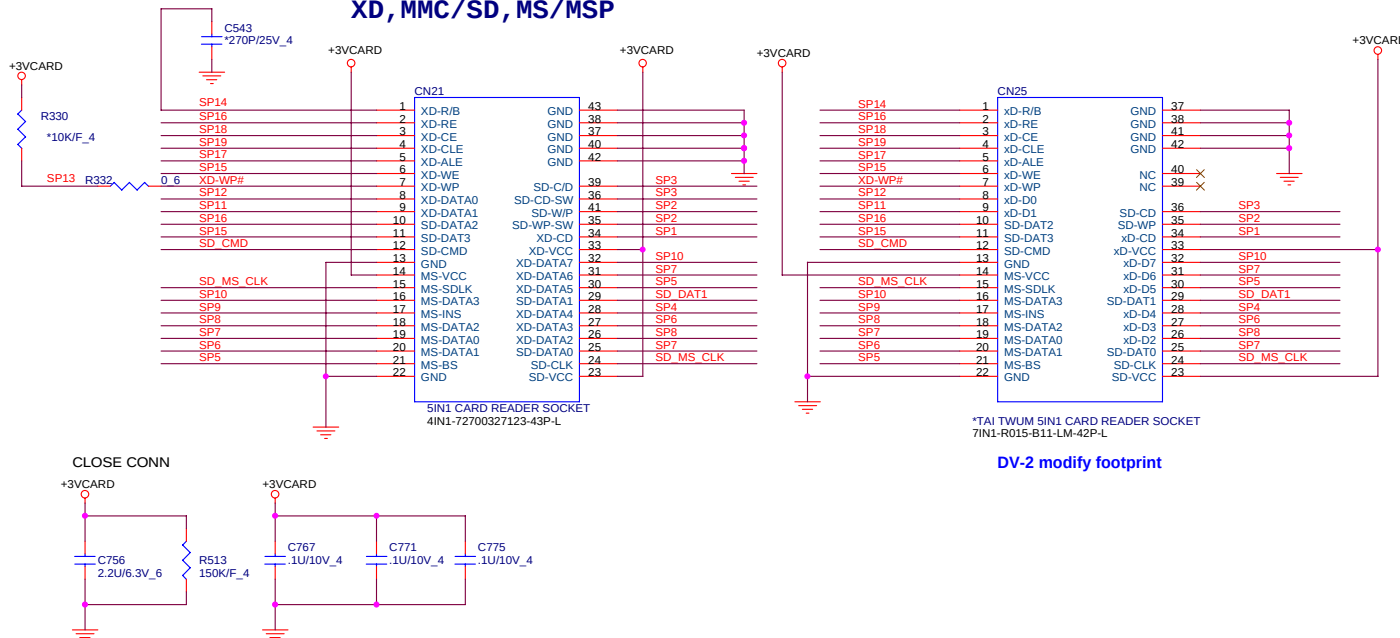


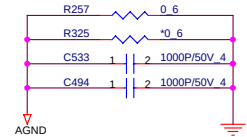
Note:

SD/MMC	MS	XD
SP0		XD_CD#
SP1	SD_WP	XD_CD#
SP2		
SP3	SD_CD#	
SP4	SD_DAT1	XD D4
SP5	SD DAT1	MS BS
SP6	SD DAT1	MS D1
SP7	SD DAT0	MS D0
SP8	SD DAT7	MS D2
SP9	MS INS#	
SP10	SD DAT6	MS D3
SP11	SD CLK	MS SCLK
SP12	SD DAT5	XD D0
SP13	SD DAT4	XD WP#
SP14		XD R/B#
SP15	SD DAT3	XD WE#
SP16	SD DAT2	XD RE#
SP17		XD ALE
SP18		XD CE#
SP19		XD CLE

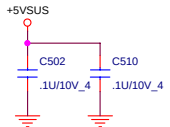
23

5 IN1 CARD READER XD, MMC/SD, MS/MSP





DV-2 modify



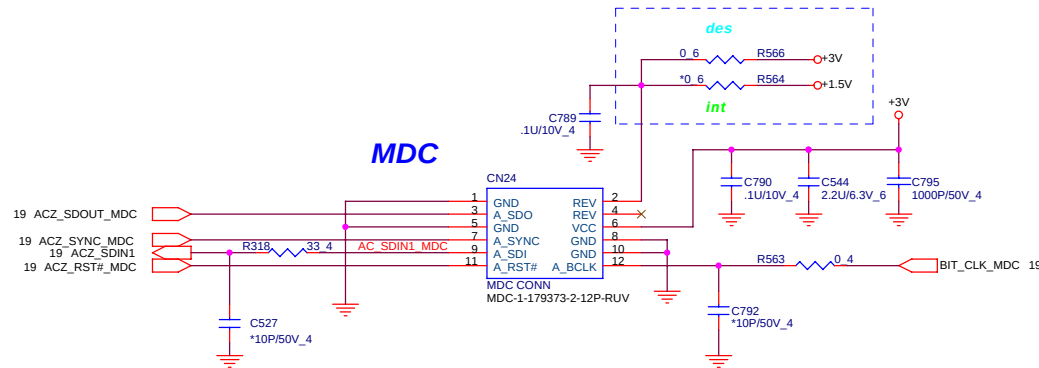
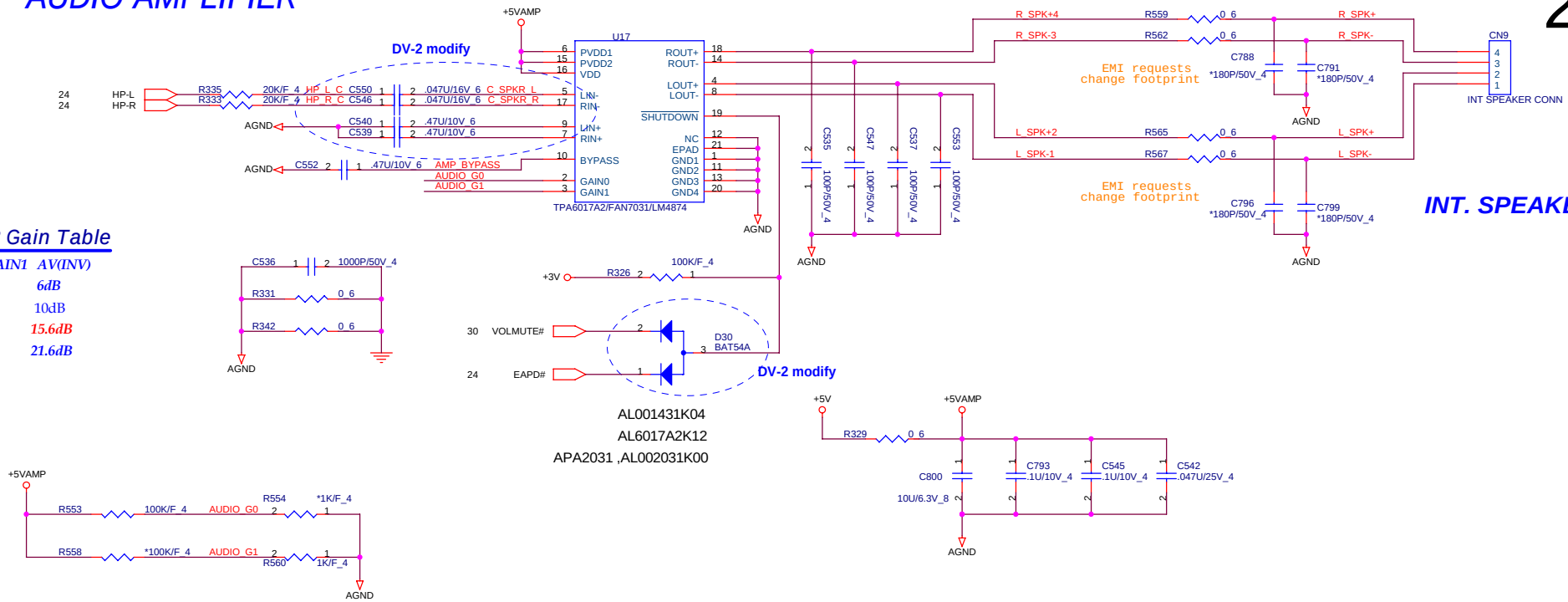
Date: Tuesday, February 26, 2008 Sheet 24 of 40

AUDIO AMPLIFIER

25

6017A2 Gain Table

GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



H20
FB5A1017

H21
FB5A1017

Needs to change Library as ME request

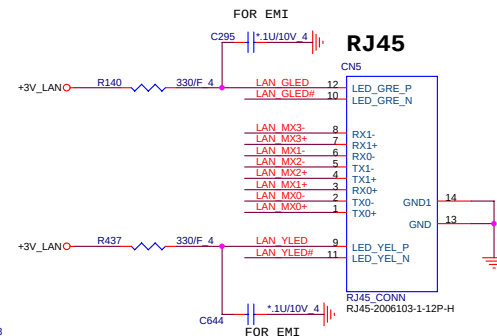
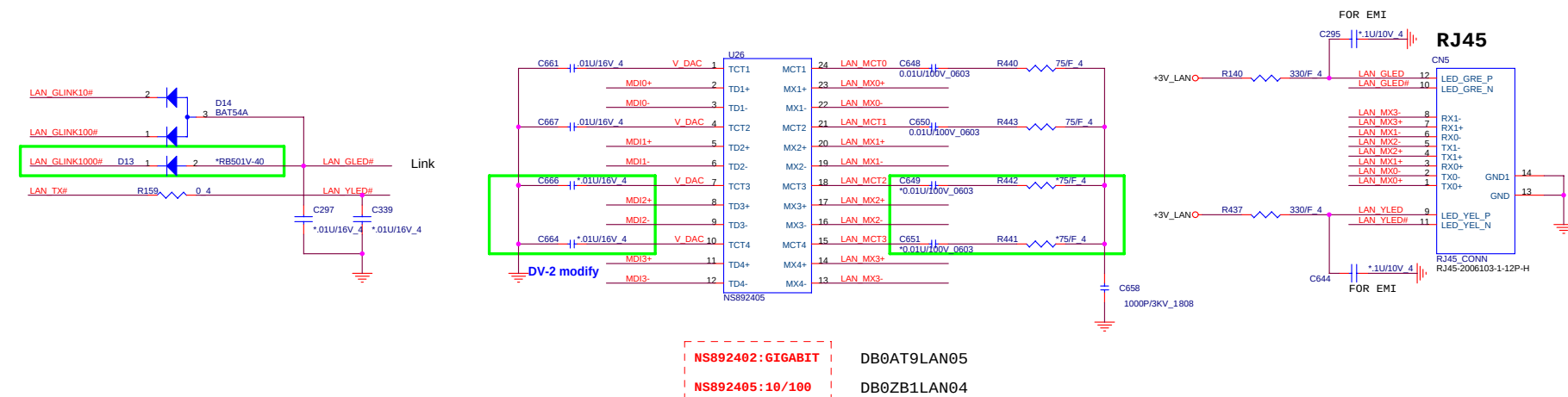
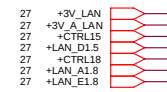


PROJECT : QL6
Quanta Computer Inc.

Size Custom	Document Number AMP_TPA6017/MDC	Rev 2A
Date: Tuesday, February 26, 2008	Sheet 25 of 40	

E : Stuffed for 8102E(10/100)

26



NS892402: GIGABIT	DB0AT9LAN05
NS892405: 10/100	DB0ZB1LAN04

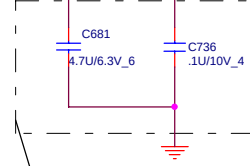
T : Stuffed for RTL8111C(10/100/1000)

E : Stuffed for 8102E(10/100)

other

LANVCC
1.2W
364mA

+3VLANVCC



C735 .1U/10V_4 C682 .1U/10V_4 C699 .1U/10V_4 C683 .1U/10V_4

these CAP are for LAN CHIP LANVCC pins--16, 37, 46 and 53.placement close lan chip

+3V LAN

+3V_A_LAN

C732 .1U/10V_4 C743 .1U/10V_4

these CAP are for LAN CHIP LAN_A3.3 pins-- 2 and 59.placement close lan chip

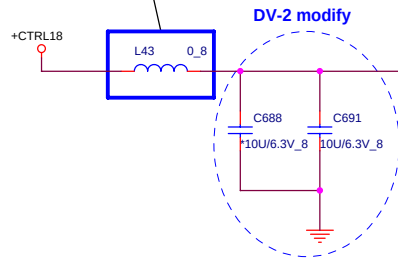
8111C CV-4706MN00
8102E CS00004JA40

For Giga must change L65 to Inductor (Chipset include switch power)
+CTRL18 will become to switch power phase

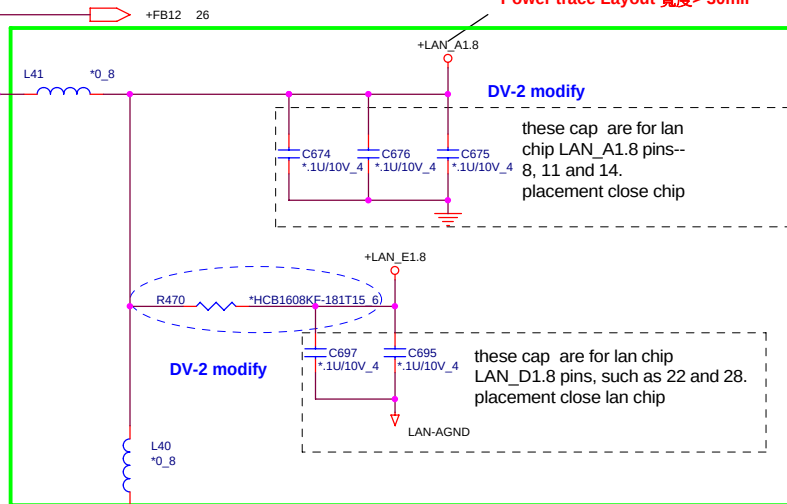
L43 for Giga lan use 4.7uH power choke
A>500mA tolerance $\pm 15\%$

placement close to lan chipset

Power trace Layout 寬度> 30mil



DV-2 modify



DV-2 modify

these cap are for lan chip LAN_A1.8 pins-- 8, 11 and 14.
placement close chip

DV-2 modify

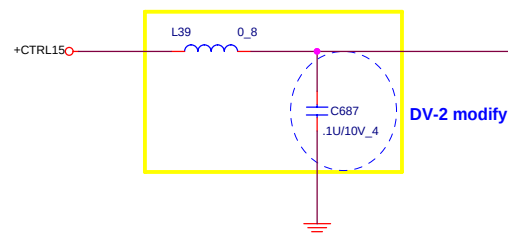
these cap are for lan chip LAN_D1.8 pins, such as 22 and 28.
placement close lan chip

Power domain chart

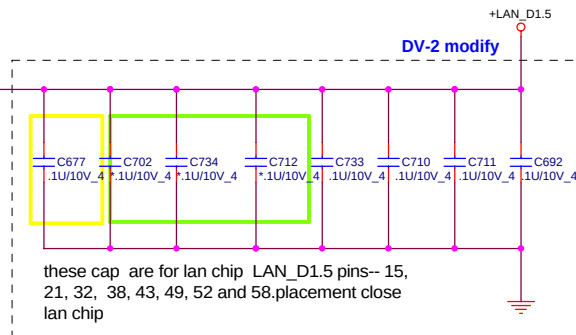
RTL8111C / RTL8102E

LANVCC	3.3V
LAN_D1.8	1.2V
LAN_A1.8	1.2V
LAN_D1.5	1.2V

Power trace Layout 寬度> 30mil



DV-2 modify



DV-2 modify

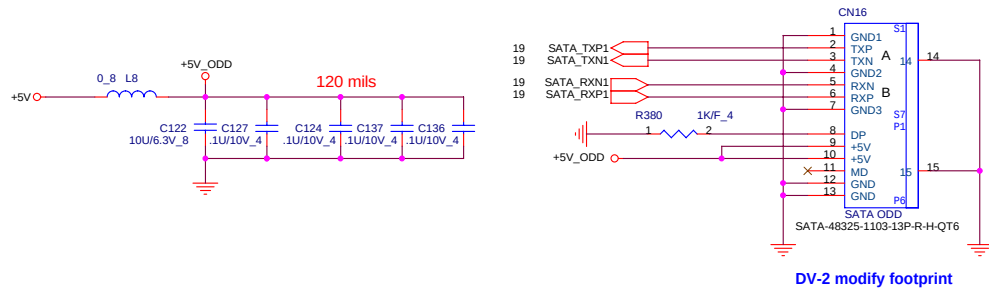
these cap are for lan chip LAN_D1.5 pins-- 15, 21, 32, 38, 43, 49, 52 and 58.placement close lan chip



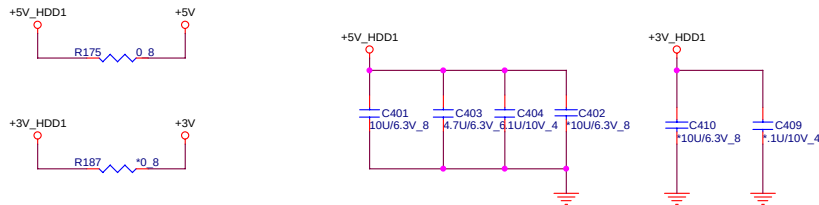
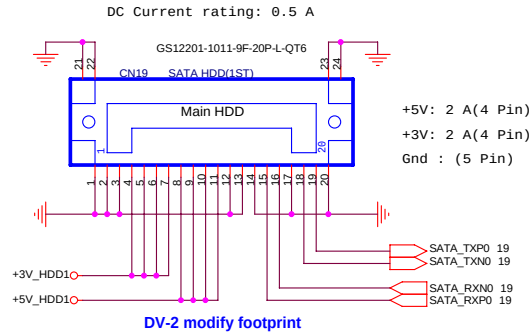
PROJECT : QL6
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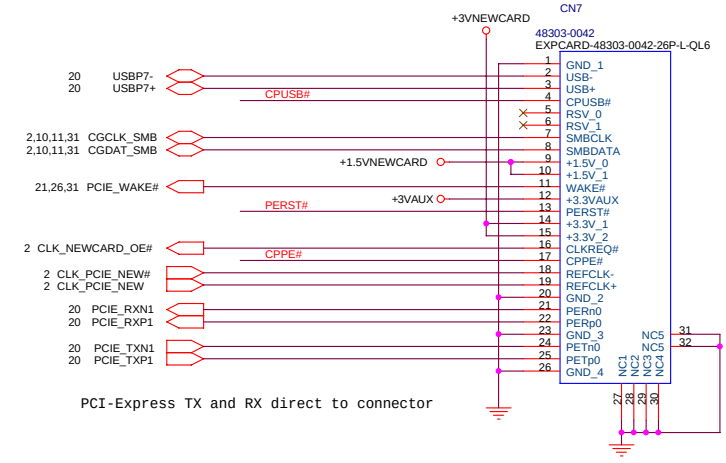
SATA ODD CONECTOR



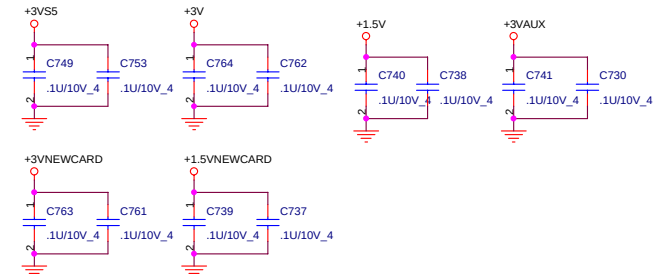
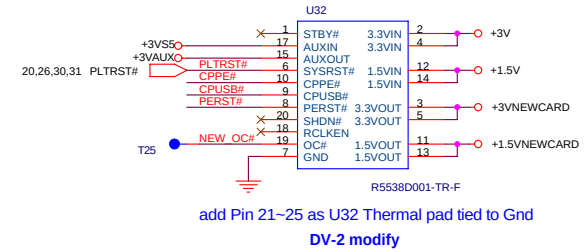
SATA HDD CONNECTOR



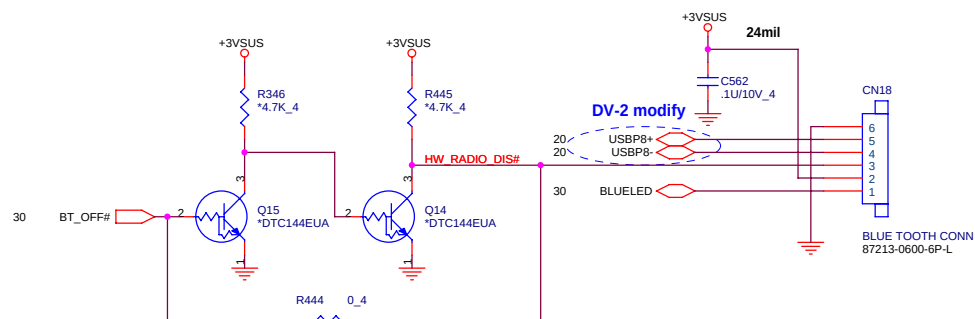
NEWCARD



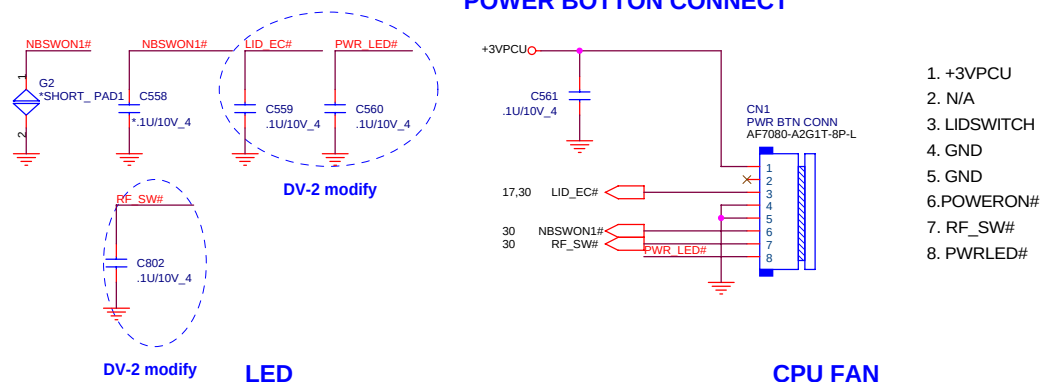
EXPCARD-48303-0042-26P-L-QT6 as ME modify Pad size(pin31,32) DV-2 modify



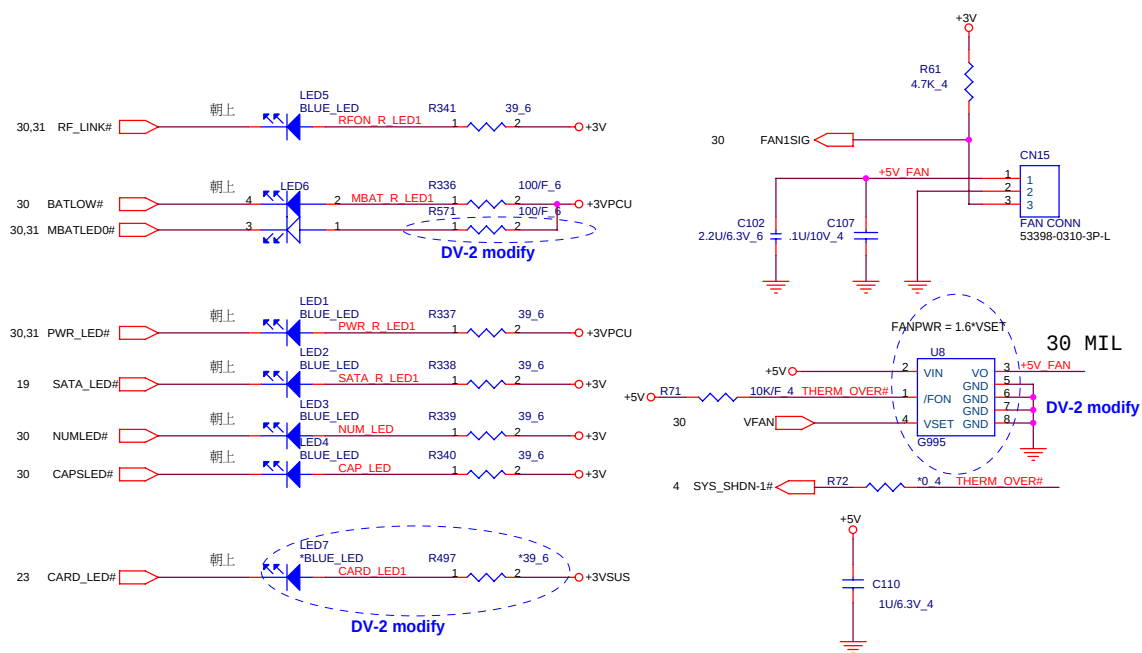
BLUETOOTH POWER



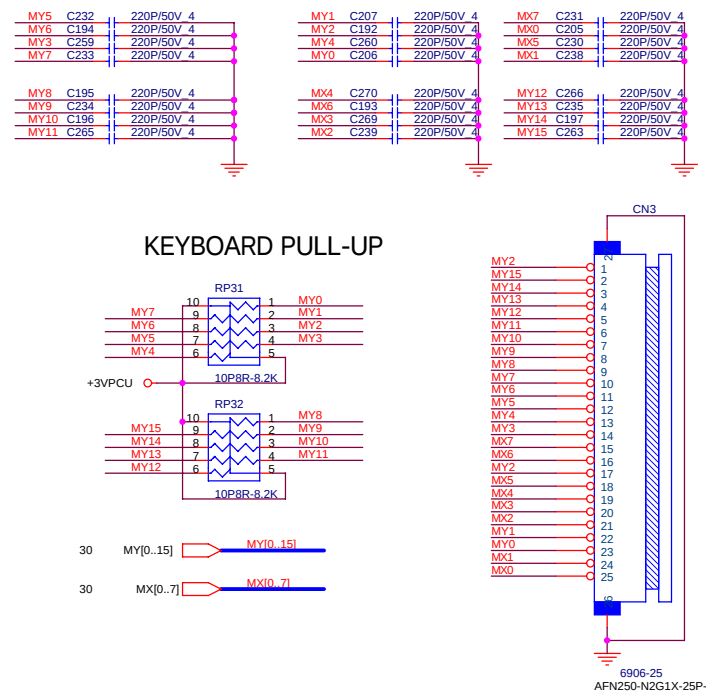
POWER BOTTON CONNECT



CPU FAN

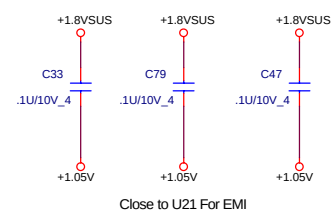


KEYBOARD PULL-UP



25	129 App	33 D	113 F2	59 Fn	46 Z	36 H	91 num 7	118 F7	119 F8		12 —	102 num 6	124 Prt			
24	17 Q	104 num Del	115 F4	112 F1	99 num 0	48 C	22 Y	122 F11	106 num +	117 F6	120 F9	108 num Ent	123 F12	125 Scr	126 Pause	
21	1 ~	31 A	110 Esc	93 num 1	6 %	7 ^	121 F10	116 F5	9 #	45 ~	127 L Win	11) 0	13 + =	76 Del	127 80	
20	19 E	4 # 3	3 @ 2	98 num 2	5 \$ 4	8 & 7	10 (9		9 ~	45 ~	58 L Ctrl	26 P	15 BS	80 Home	128 Del	
19	16 Tab	2 1	18 W	83 ↑	20 R	23 U	25 O	57 R Shift	24 J	92 num 4		27 { }	28 []	86 PgDn	129 80	
18	30 Caps	11 F3	32 S	103 num 3	34 F	37 J	39 L	44 L Shift	38 K	79 ~		40 :	85 PgUp	130 80	131 80	
16	96 num 8	62 R Alt	35 G	47 X	84 ↑	49 V	52 M	54 ~	53 ~	101 num 9		55 ? /	41 ~	81 End	132 80	
15	56 Y /	60 L Alt	97 num 5	21 T	10 num Lk	50 B	51 N	95 num /	100 num *	89 +		105 num -	43 Ent	61 Space	133 80	
23	22	17	14	13	12	11	10	9	8	7	6	5	4	3	2	1

1&17 pin short circuit

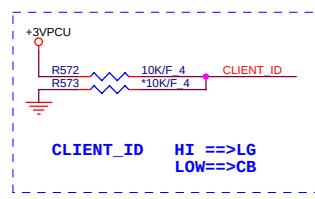
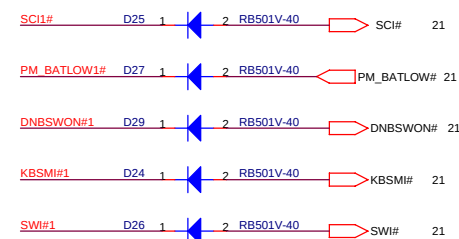
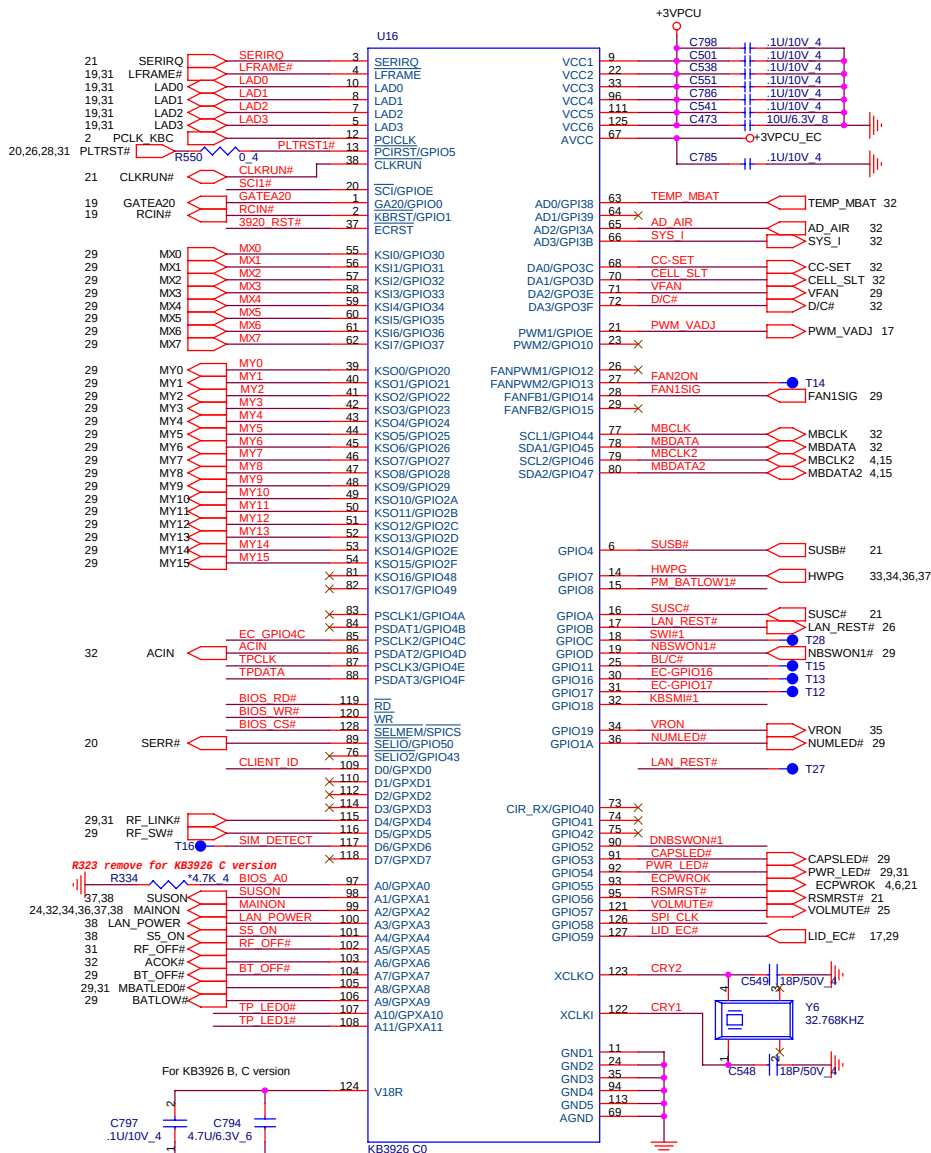
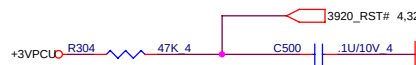
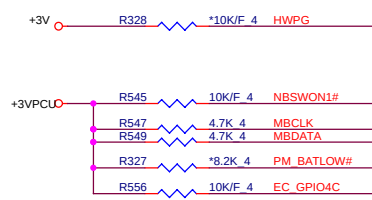
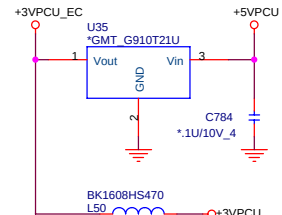
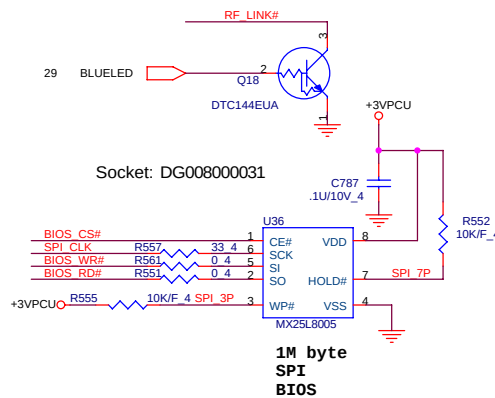
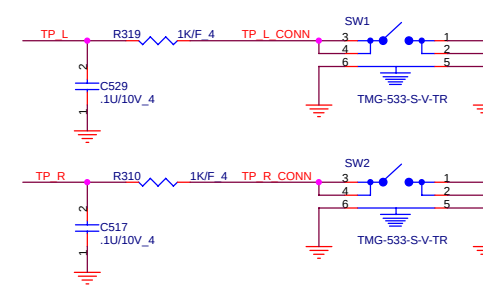
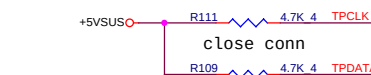
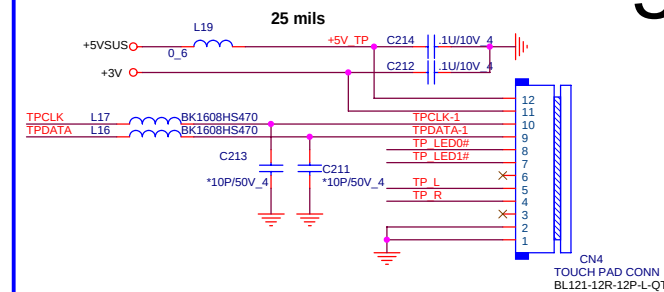


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TOUCH PAD CONNECTOR

TOUCH PAD L/R



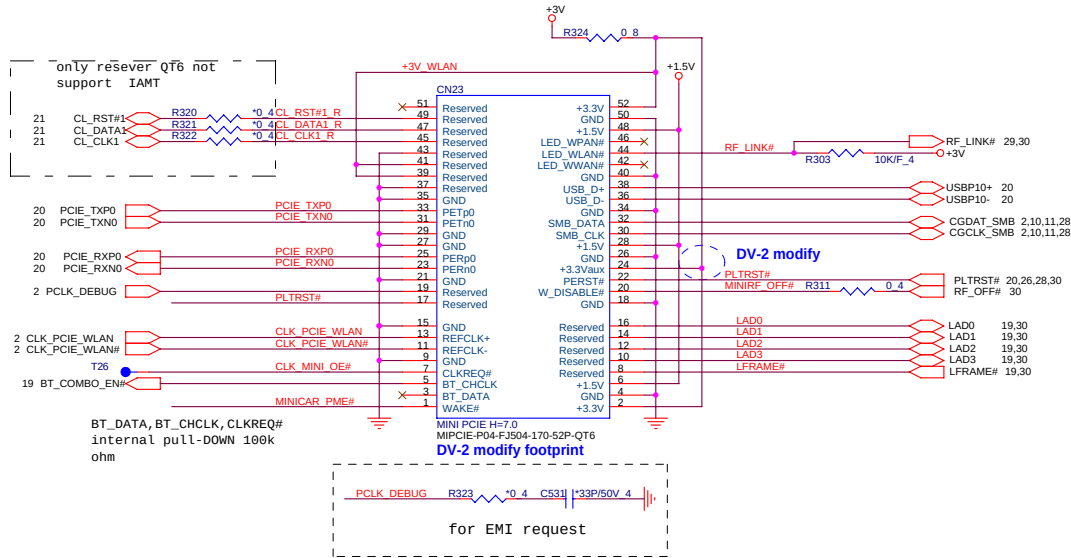
PROJECT : QL6
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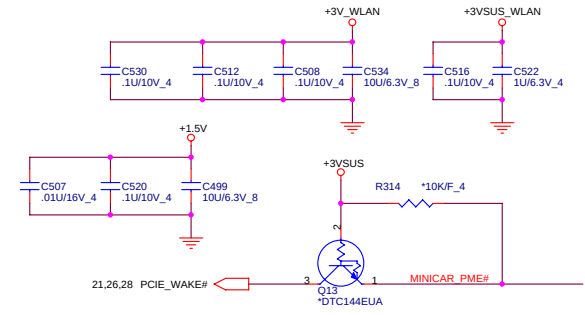
NB5

Size Custom	Document Number KB3926/ROM/TP	Rev 2/
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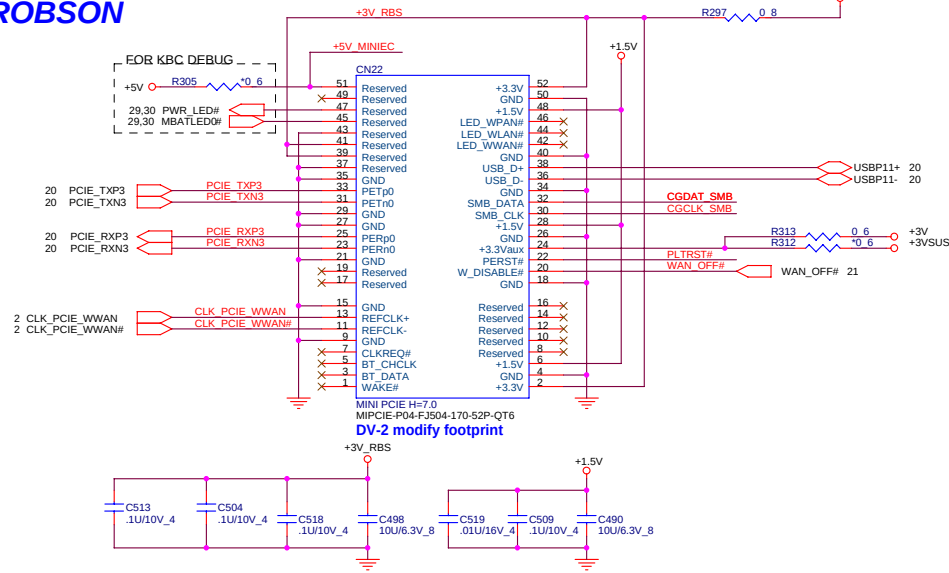
Mini PCI-E Card 1 WLAN



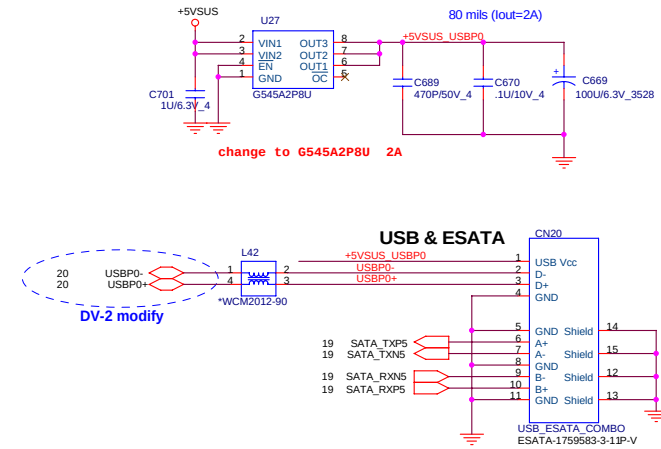
INTEL WLAN
CARD PIN 20
W_DISABLE#
have
internal
pull-up 110k
ohm



Mini PCI-E Card 2 ROBSON

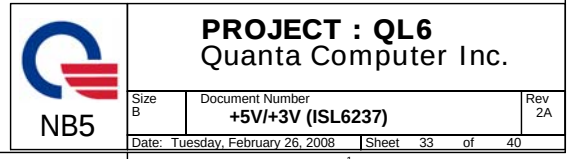


E-SATA/USB COMBO



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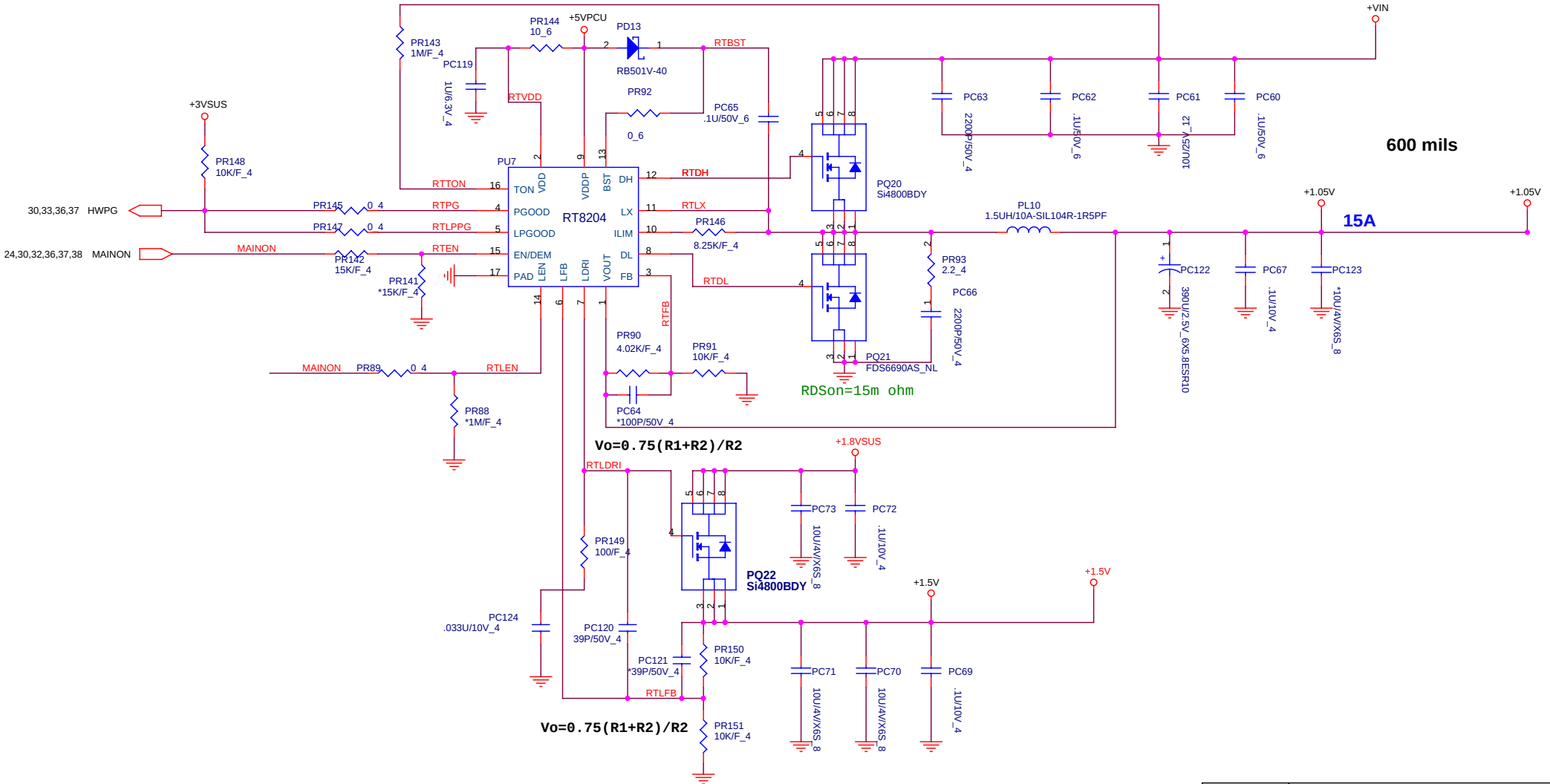
Size	Document Number	Rev
Custom	MINI PCIE CONN X2/E-SATA	2A
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VCCP1.05V & +1.5V

+1.05Volt +/- 5%
 Countinue current:7.5A
 Peak current:10A
 OCP minimum 15A

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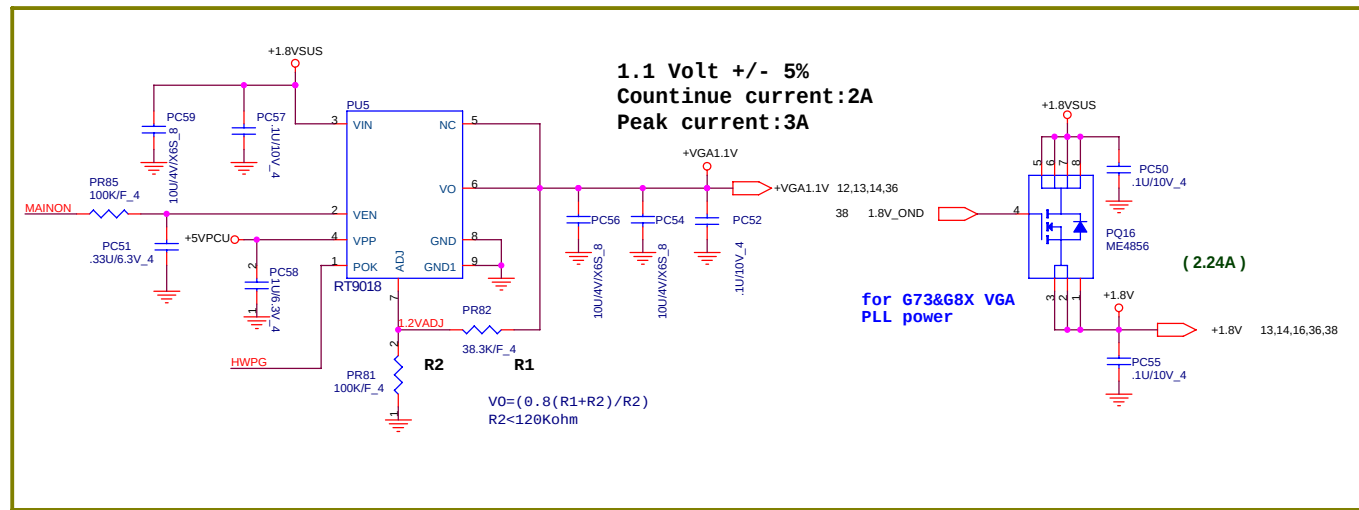
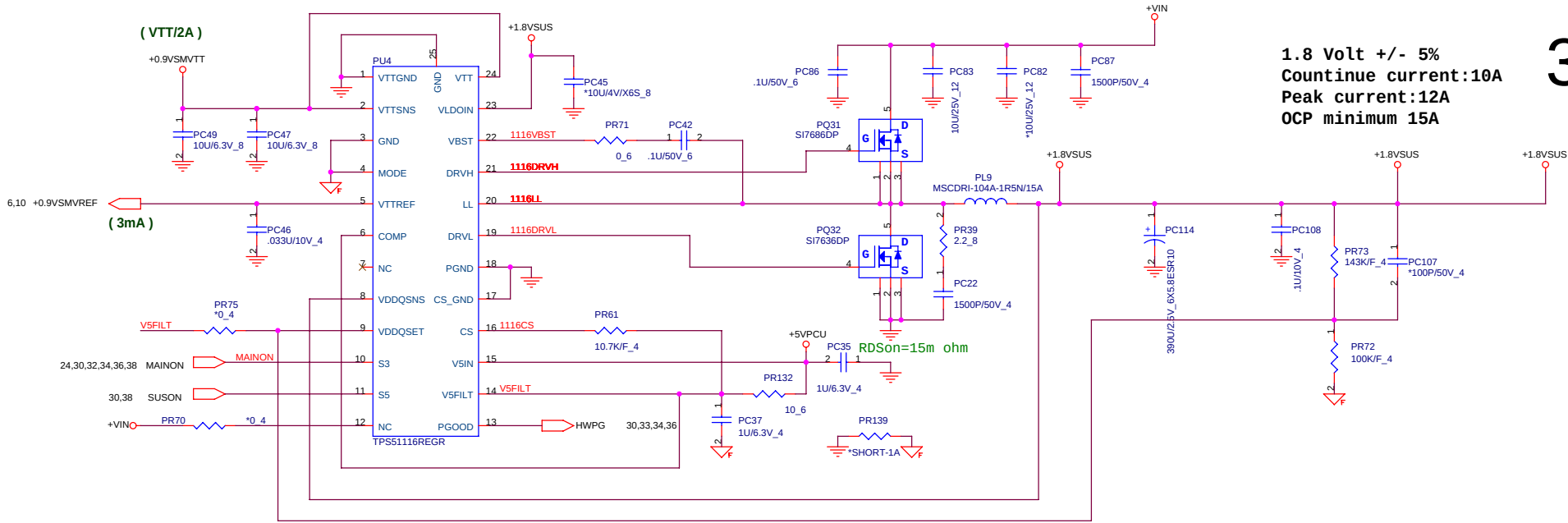


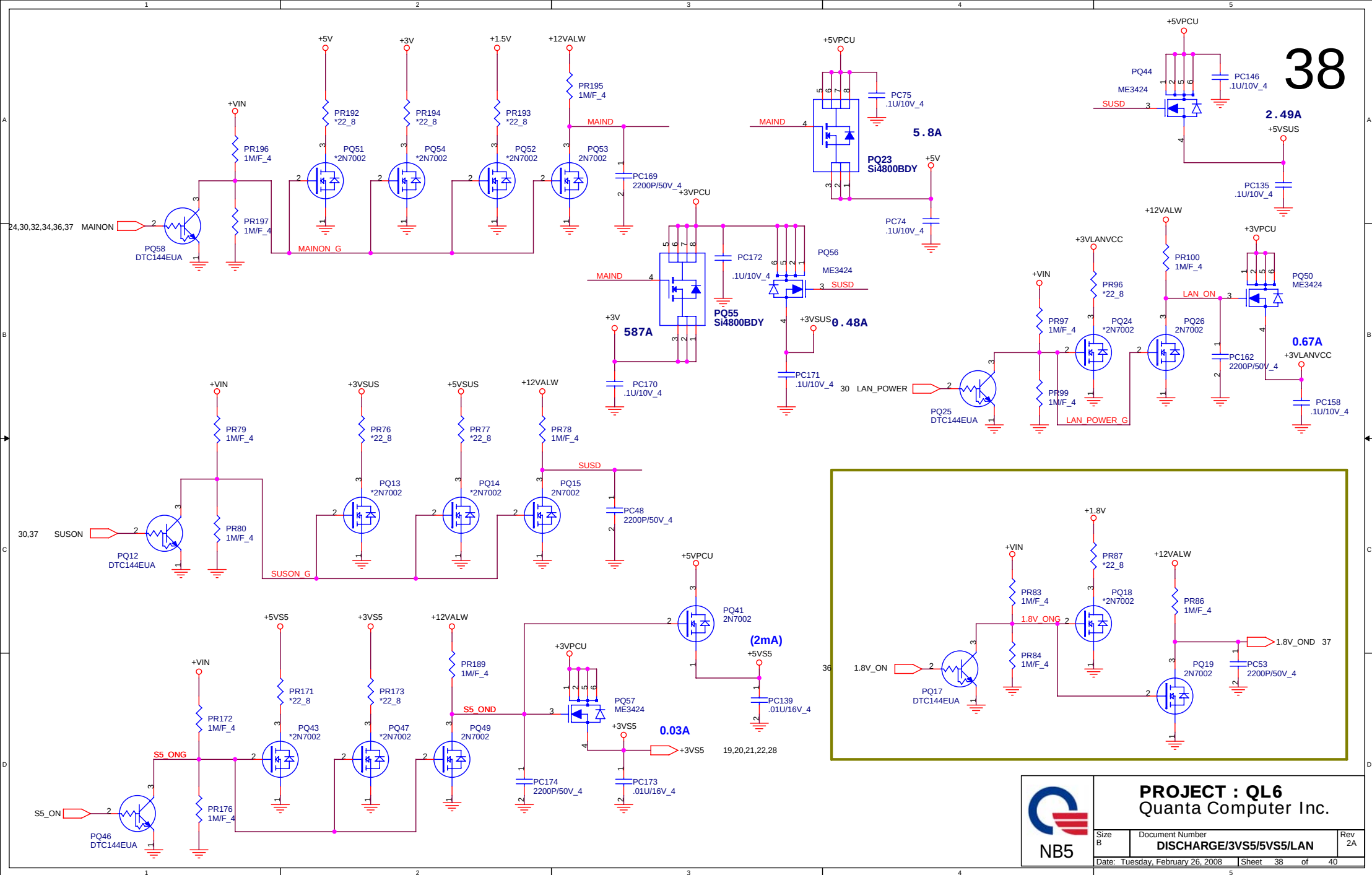
		PROJECT : QL6	
		Quanta Computer Inc.	
Size B	Document Number	+1.05V/+1.5V (RT8204)	
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Rev 2A			



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B	DISCHARGE/3VS5/5VS5/LAN	2A
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	Voltage level	AC MODE				DC MODE			
		S0	S3	S4	S5	S0	S3	S4	S5
+3VPCU	3.3V +/- 5%	V	V	V	V	V	V	V	V
+5VPCU	5V +/- 5%	V	V	V	V	V	V	V	V
+3VRTC	3.3V +/- 5%	V	V	V	V	V	V	V	V
+3VS5	3.3V +/- 5%	V	V	V	V	V	V		
+5VS5	5V +/- 5%	V	V	V	V	V	V		
+3VSUS	3.3V +/- 5%	V	V			V	V		
+5VSUS	5V +/- 5%	V	V			V	V		
+1.8VSUS	1.8V +/- 5%	V	V			V	V		
+0.9VSMVTT	0.9V +/- 5%	V	V			V	V		
+1.5V	1.5V +/- 5%	V				V			
+1.05V	1.05V +/- 5%	V				V			
+VCORE	0.9~1.15V	V				V			
+VGA_CORE	0.9~1.2V	V				V			
+VGA1.1V	1.1V +/- 5%	V				V			
+1.8V	1.8V +/- 5%	V				V			
+3VLAVCC	3.3V +/- 5%	V				V			



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