PROJECT : CHICAGO (For Intel Huron River Platform)

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P. Leader	Check by	Design by

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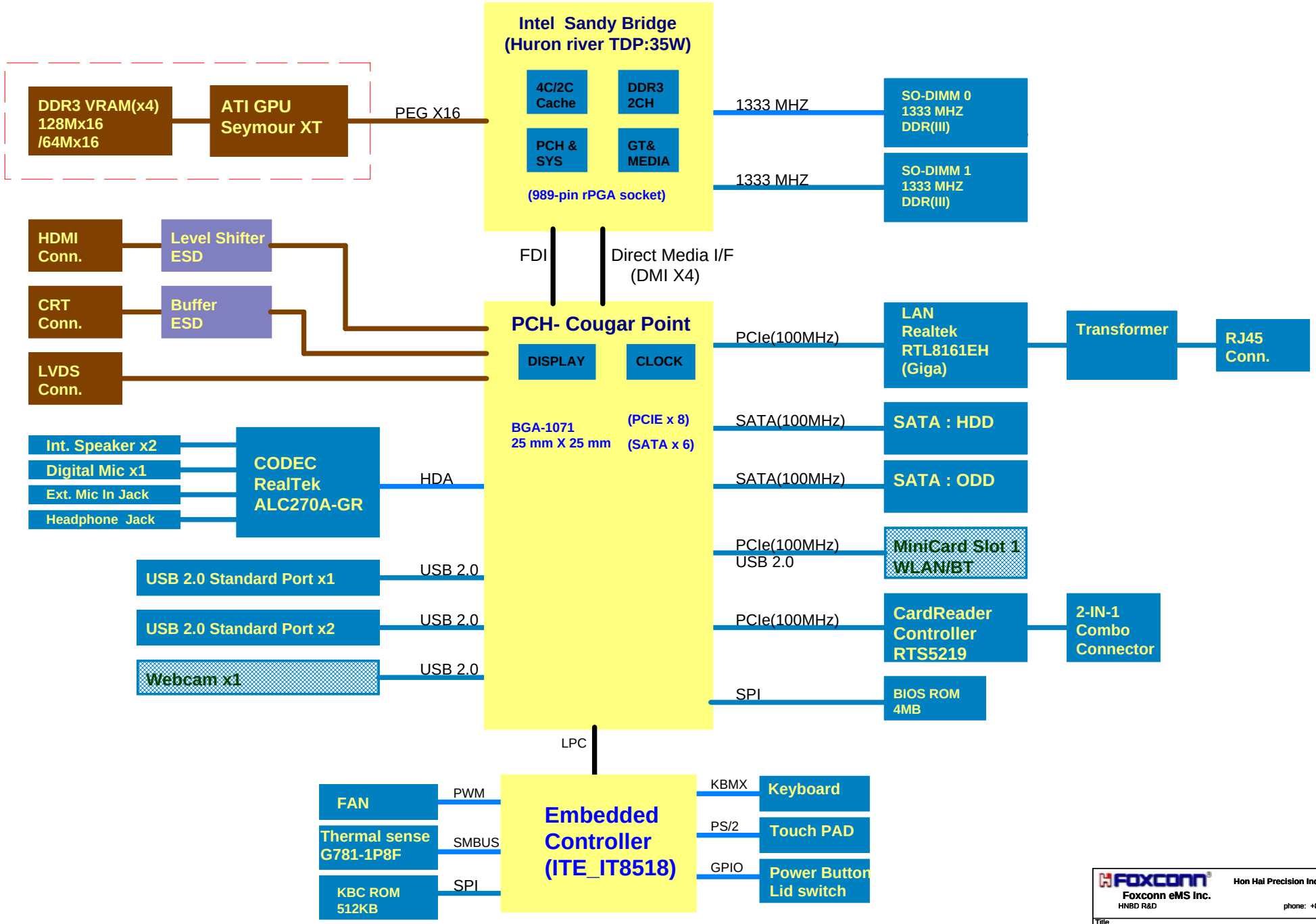

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Title: SYSTEM BLOCK DIAGRAM

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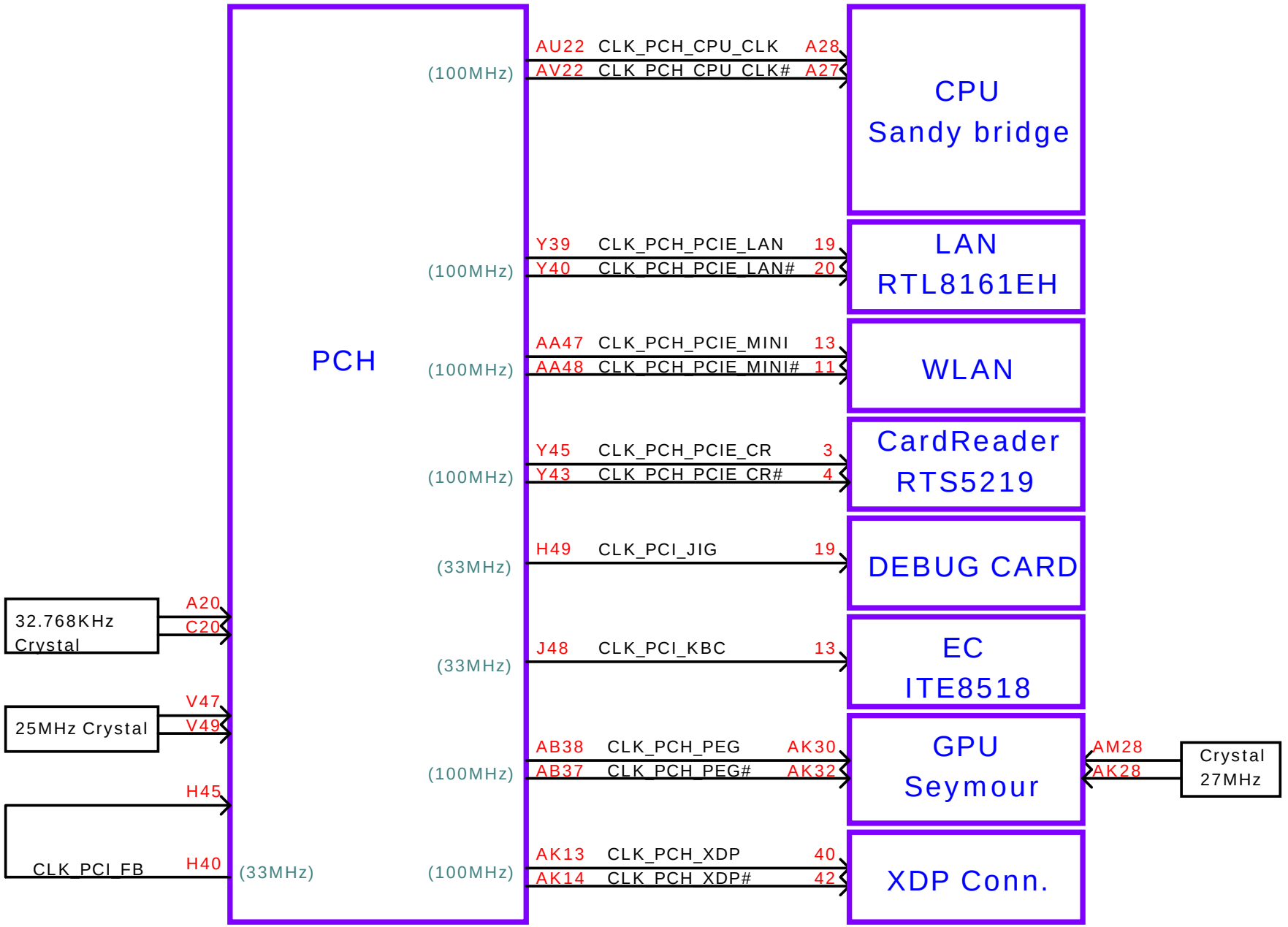

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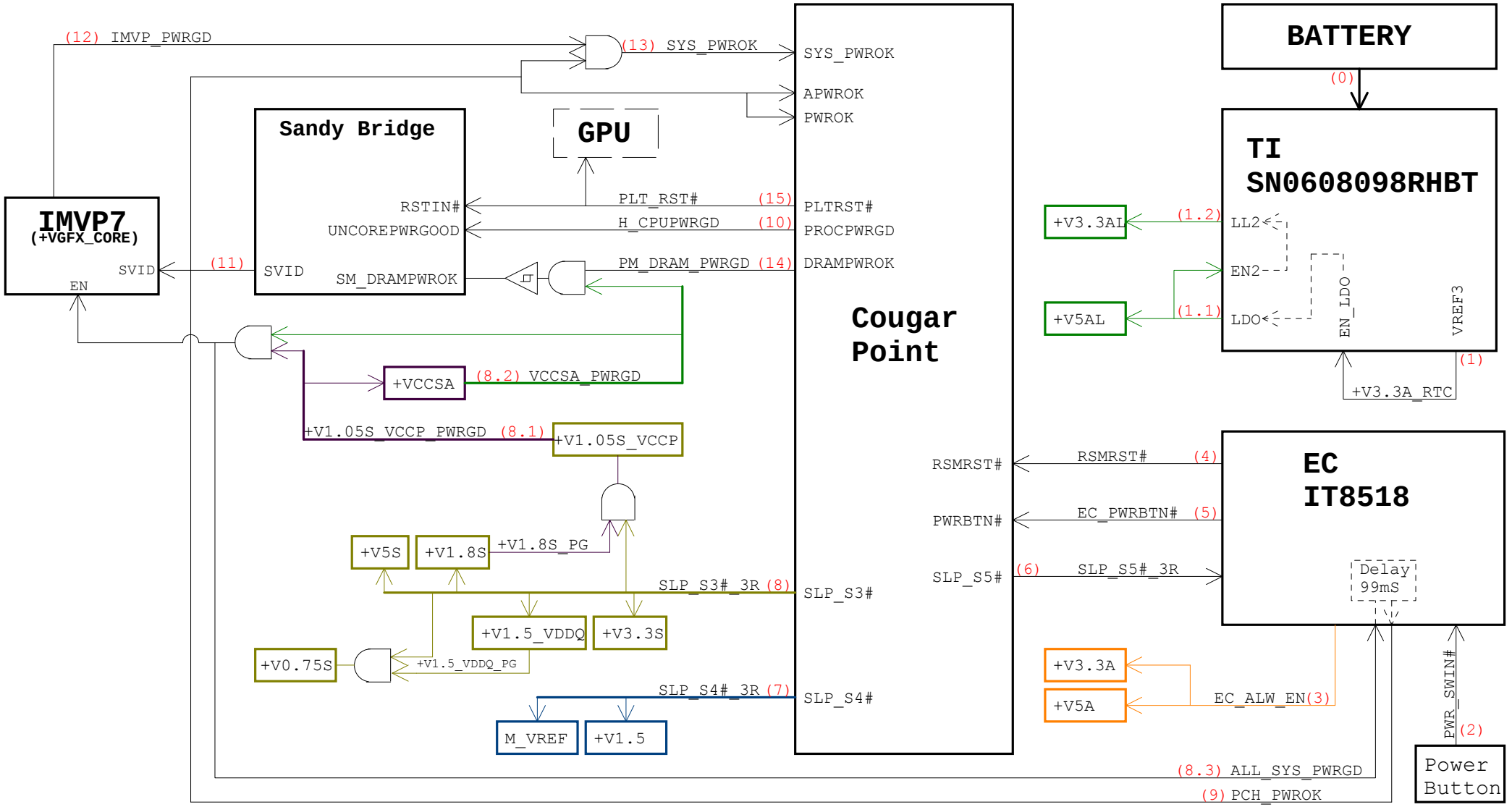

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Title: POWER SEQUENCY DIAGRAM

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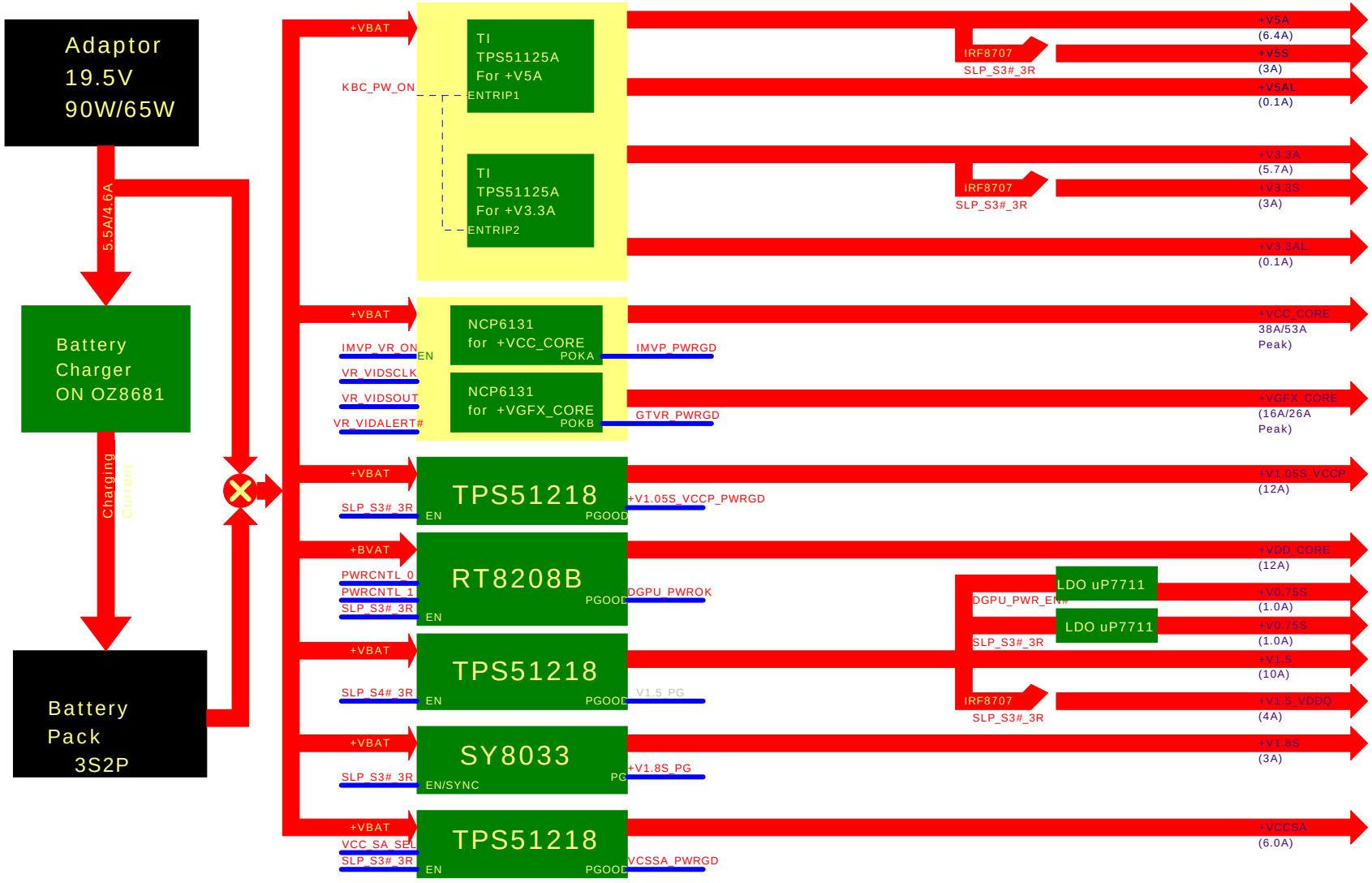
POWER MAP



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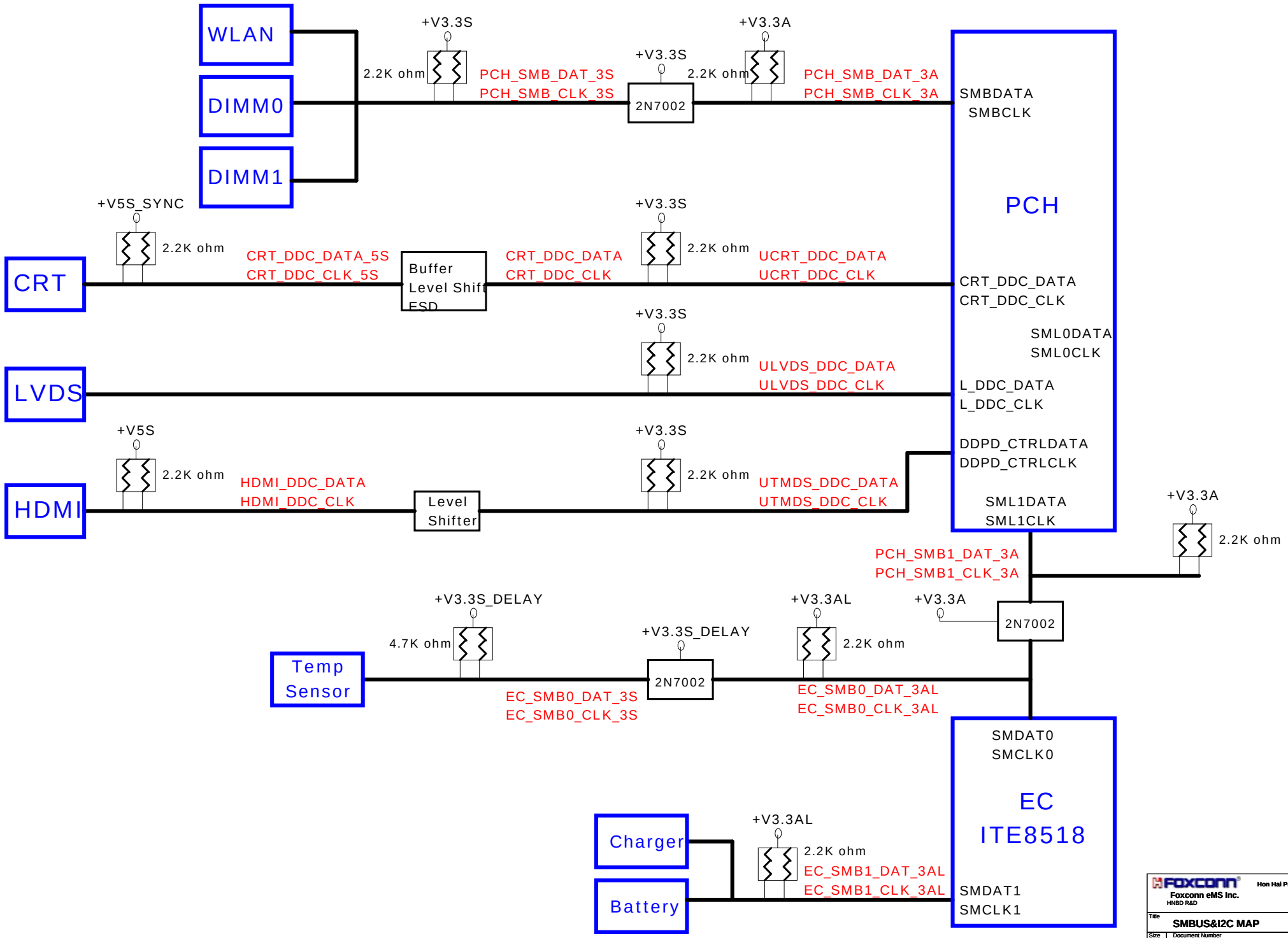

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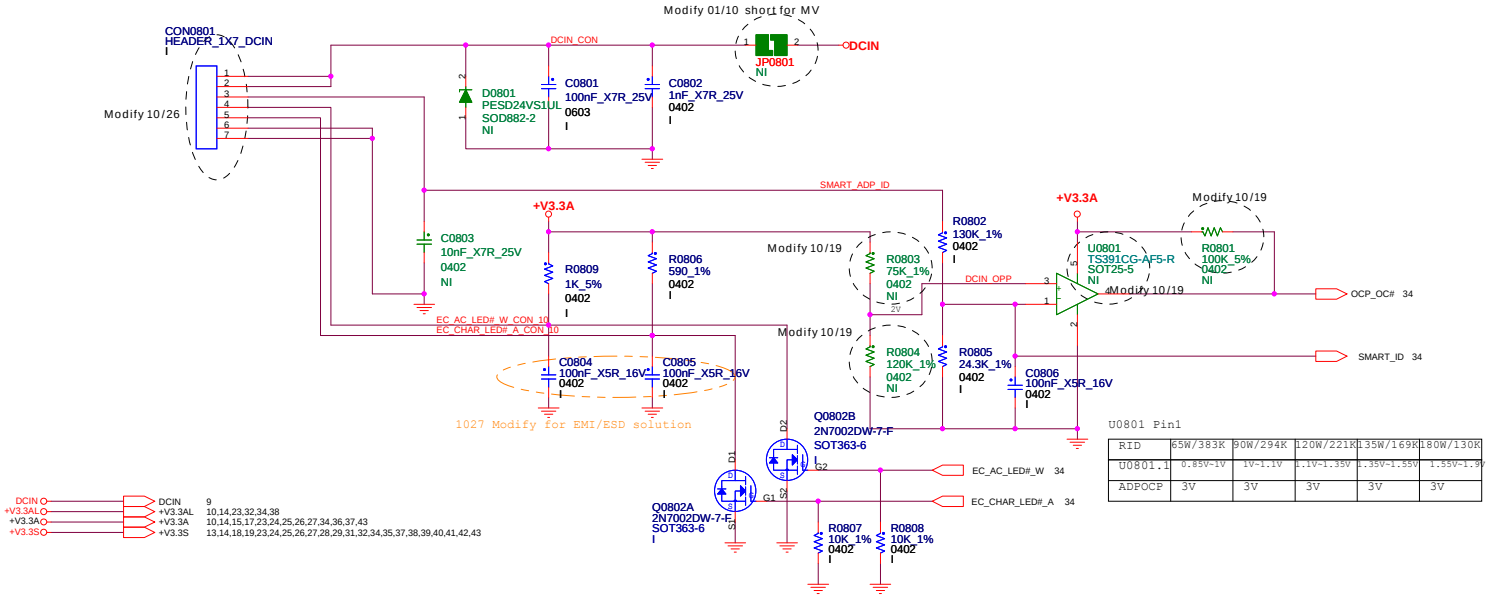
DC_JACK WIRE to BOARD CONNECTOR

2010.1203.0

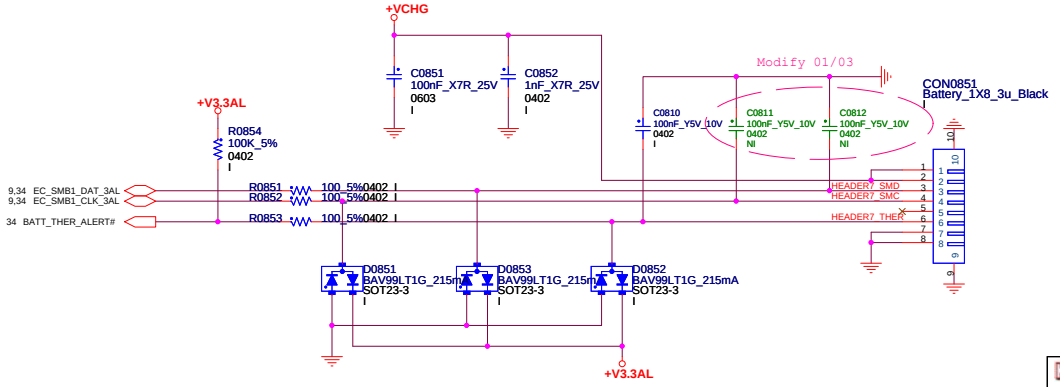


U0801 Pin1

RID	65W/383K	90W/294K	120W/221K	135W/169K	180W/130K
U0801.1	0.85V~1V	1V~1.1V	1.1V~1.35V	1.35V~1.55V	1.55V~1.9V
ADPOCP	3V	3V	3V	3V	3V

BATTERY CONNECTOR

2010.0914.0



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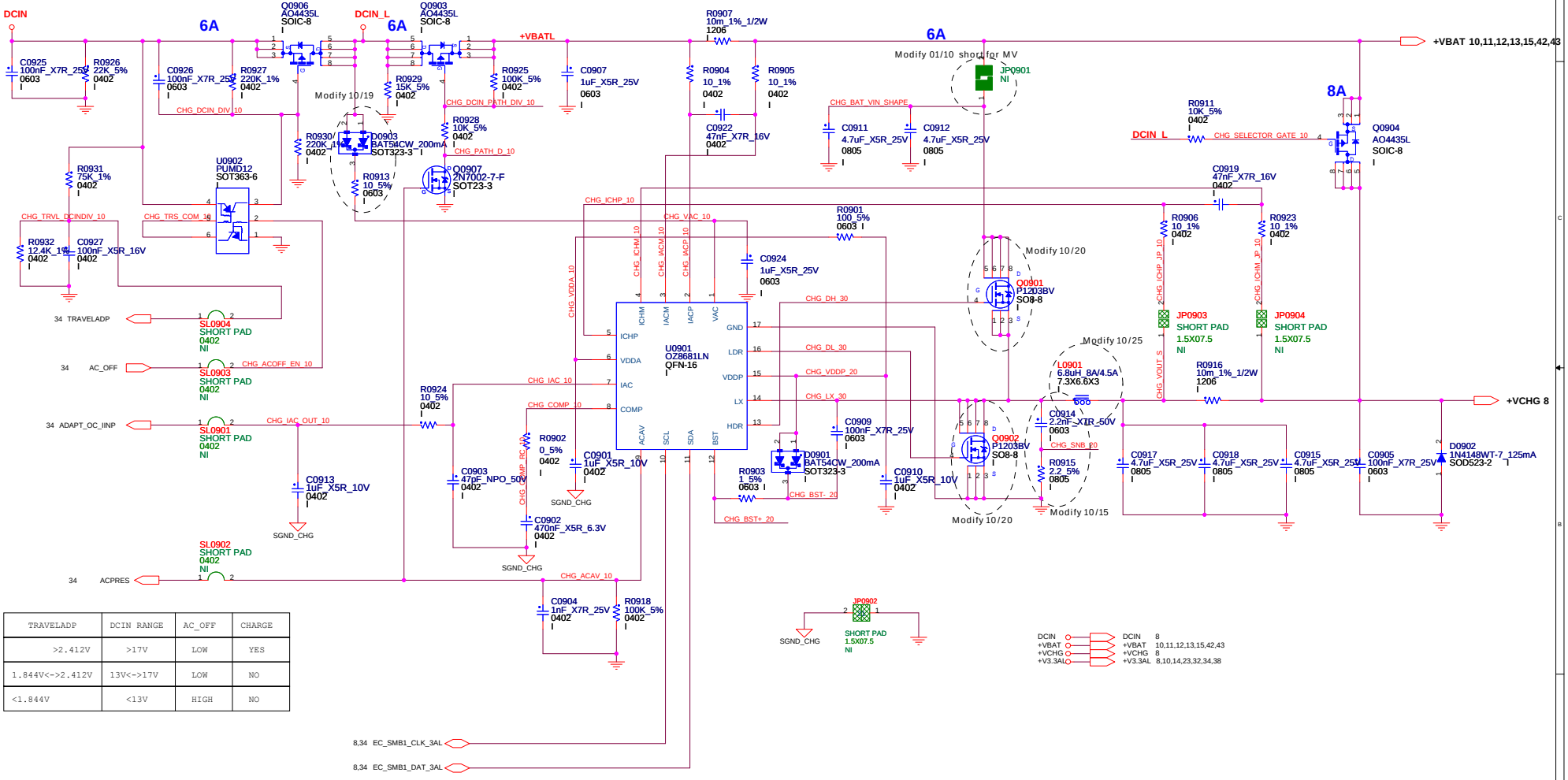
BATTERY CHARGER



TRAVELADP	DCIN RANGE	AC_OFF	CHARGE
>2.412V	>17V	LOW	YES
1.844V<->2.412V	13V<->17V	LOW	NO
<1.844V	<13V	HIGH	NO

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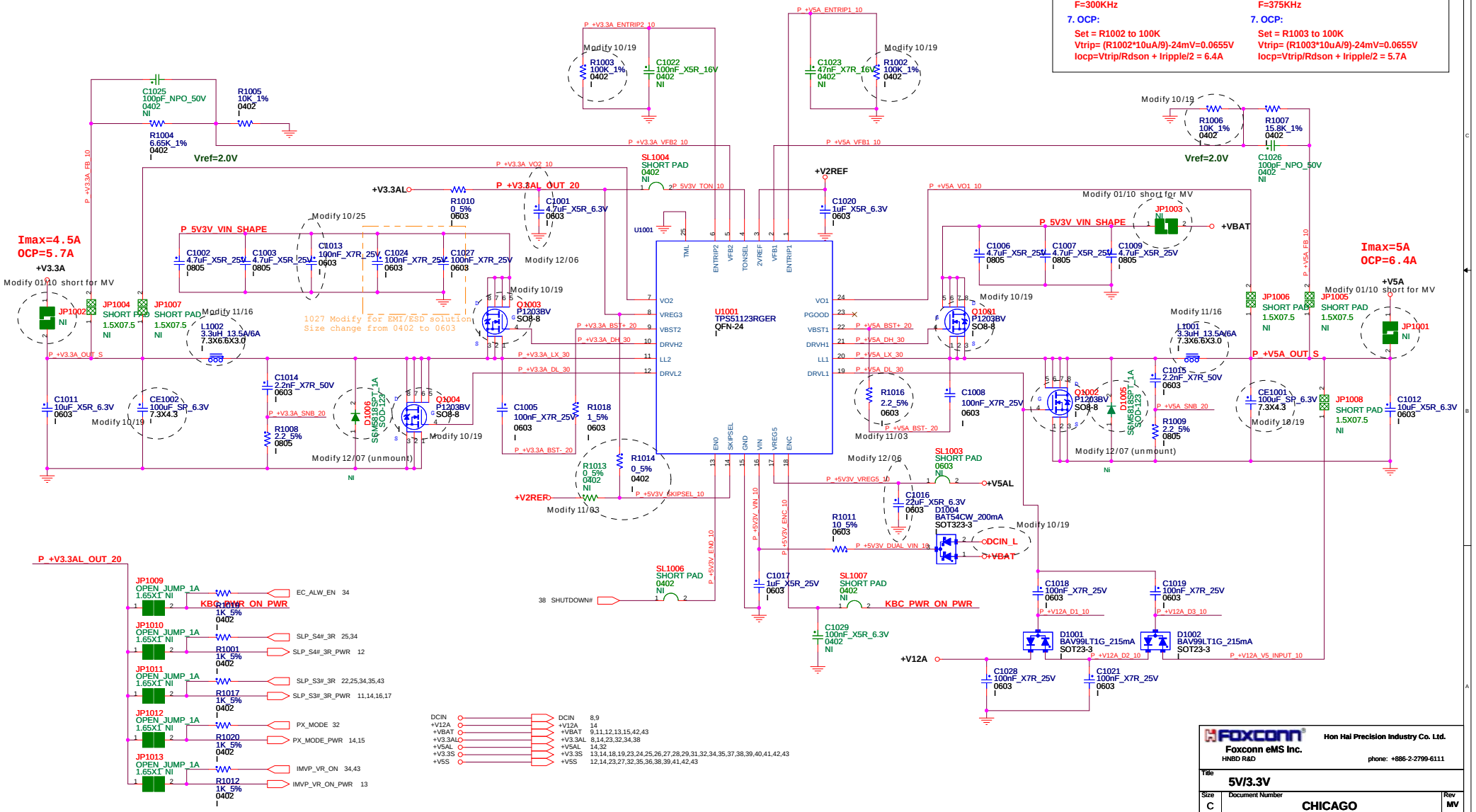
+V5A / +V3.3A POWER SUPPLY

2010.1103.0

+V5A:	+V3.3A:
1. I/P Current:	1.I/P Current:
Iin=Vo*Io/(0.75*Vin)=3.7A	Iin=Vo*Io/(0.75*Vin)=2.2A
2. Ripple Current:	2.Ripple Current:
Irip=3.72A	Irip=2.21A
3. Ripple Voltage:	3.Ripple Voltage:
ESR/1=15mohm	ESR/1=15mohm
Vrip=55.8mV	Vrip=33.15mV
4. Inductor Spec:	4.Inductor Spec:
Isat=13.5A	Isat=13.5A
Idc=6A	Idc=6A
DCR=30mohm	DCR=30mohm
5.MOSFET Spec:	
H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)	Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)	I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)	I peak = 88A (Pause =10 us)
6. Frequency:	6. Frequency:
F=300KHz	F=375KHz
7. OCP:	7. OCP:
Set = R1002 to 100K	Set = R1003 to 100K
Vtrip= (R1002*10uA/9)-24mV=0.0655V	Vtrip= (R1003*10uA/9)-24mV=0.0655V
Iocp=Vtrip/Rdson + Iripple/2 = 6.4A	Iocp=Vtrip/Rdson + Iripple/2 = 5.7A



JP1009	OPEN_JUMP_1A 1.65X1 NI	EC_ALW_EN 34
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JP1011	OPEN_JUMP_1A 1.65X1 NI	SLP_S3#_3R 22,25,34,35,43
JP1012	OPEN_JUMP_1A 1.65X1 NI	PX_MODE 32
JP1013	OPEN_JUMP_1A 1.65X1 NI	IMVP_VR_ON 34,43

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+V5AL	+V5AL	14,32
+V3.3S	+V3.3S	13,14,18,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V5S	+V5S	12,14,23,27,32,35,36,38,39,41,42,43

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+VTT POWER SUPPLY

2010.1103.0

+V1.05S_VCCP:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.24A

2. Ripple Current:

Irip=3.42A

3. Ripple Voltage:

ESR/1=9mohm
Vrip=30.78mV

4. Inductor Spec:

Isat=36A
Idc=18A
DCR=3.3mohm

5.MOSFET Spec:

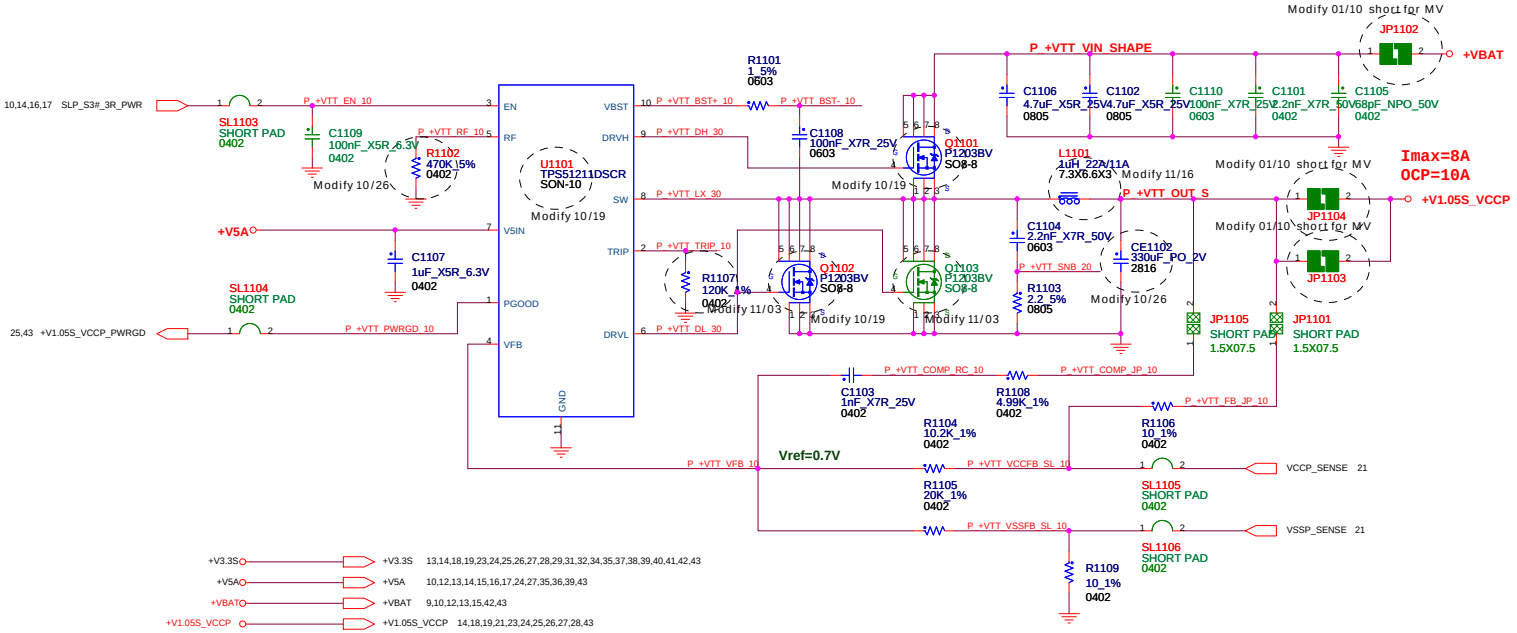
H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)	Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)	I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)	I peak = 88A (Pause =10 us)

6. Frequency:

F=290KHz (R1102=0ohm)

7. OCP:

Set = R1107 to 120K
Vtrip= R1107*10uA=1.2V
Iocp=(Vtrip/8*Rdson) + Iripple/2 = 10A



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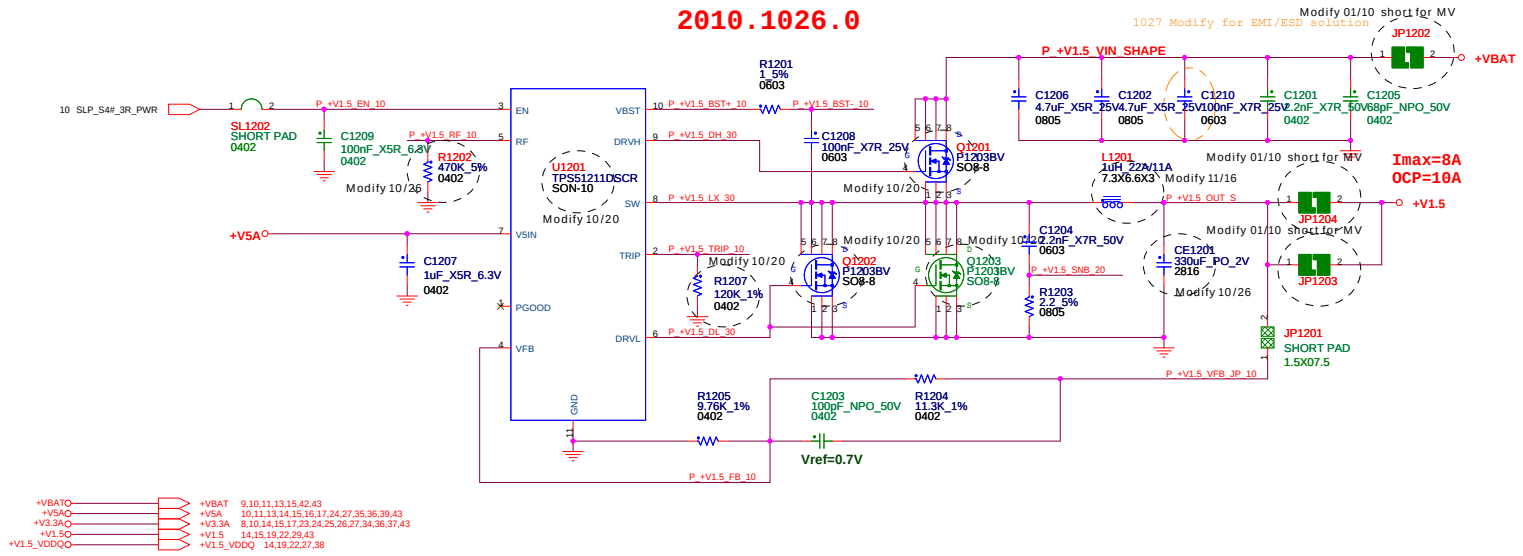
+V1.5 POWER SUPPLY

2010.1026.0



+V1.5:

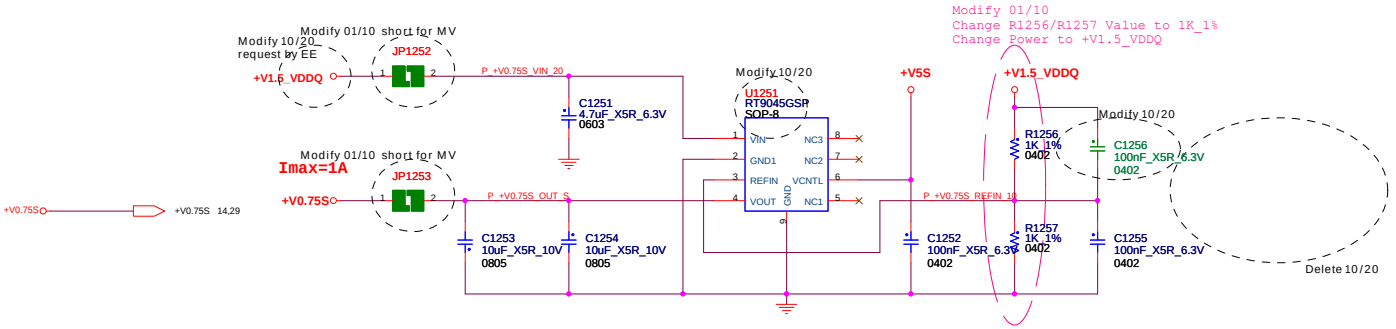
1. **I/P Current:**
   Iin=Vo*Io/(0.75*Vin)=1.78A
2. **Ripple Current:**
   Irip=3.34A
3. **Ripple Voltage:**
   ESR/1=9mohm
   Vrip=30.6mV
4. **Inductor Spec:**
   Isat=36A
   Idc=18A
   DCR=3.3mohm
5. **MOSFET Spec:**

H-side MOSFET: IRF8707PBF			L-side MOSFET: IRF8707PBF		
Rds(ON)=17.5mohm	(Vgs=4.5 V)		Rds(ON)=17.5mohm	(Vgs=4.5 V)	
I cont = 11A	(T =25 ℃)		I cont = 11A	(T =25 ℃)	
I peak = 88A	(Pause =10 us)		I peak = 88A	(Pause =10 us)	

6. **Frequency:**
   F=290KHz (R0902=0ohm)
7. **OCP:**
   Set = R1207 to 120K
   Vtrip= R1207*10uA=1.2V
   Iocp=(Vtrip/8*Rdson) + Iripple/2 = 10A

+V0.75S POWER SUPPLY

2010.1026.0



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Title: 1.5VDDR3/0.75V			
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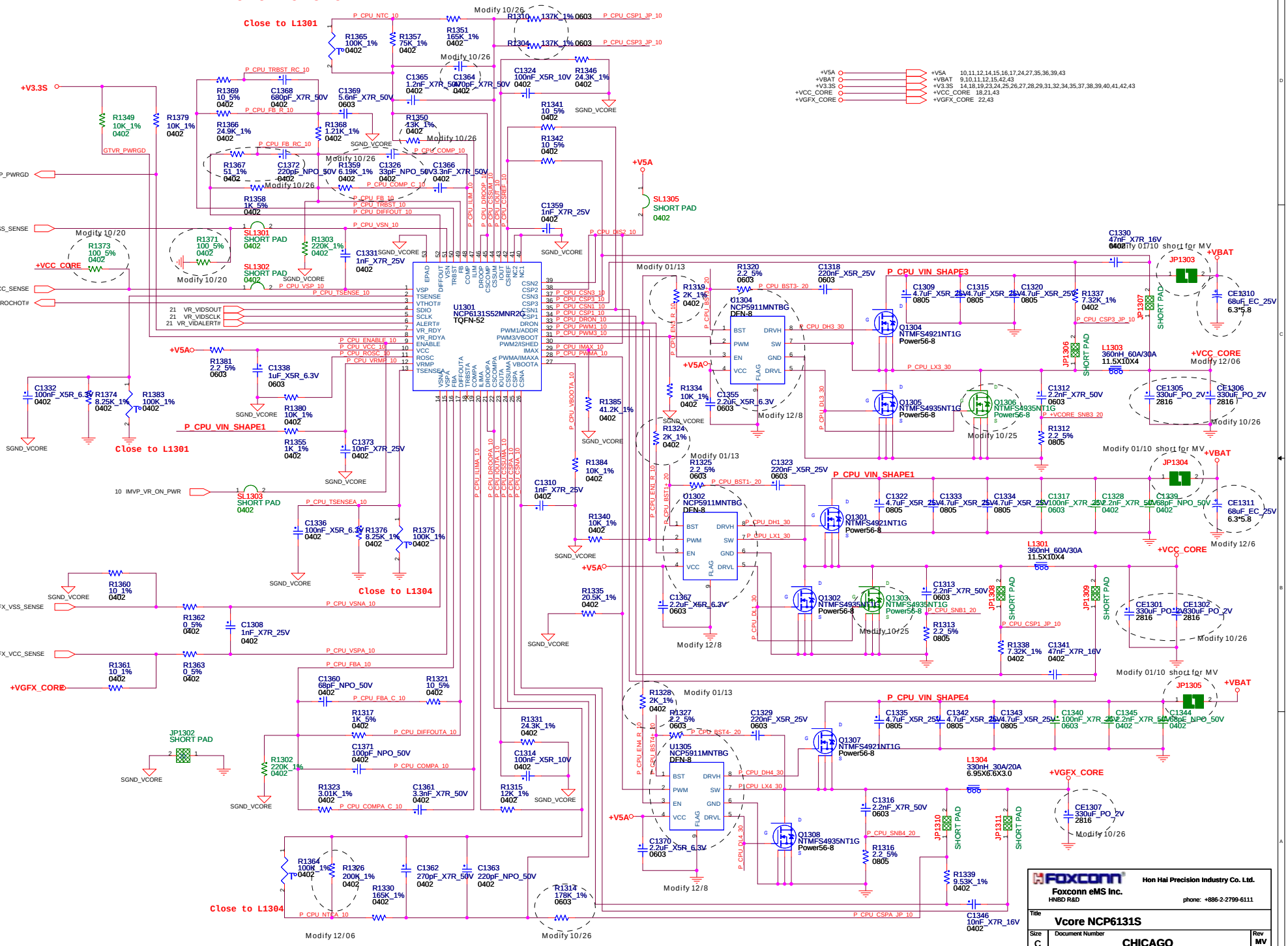
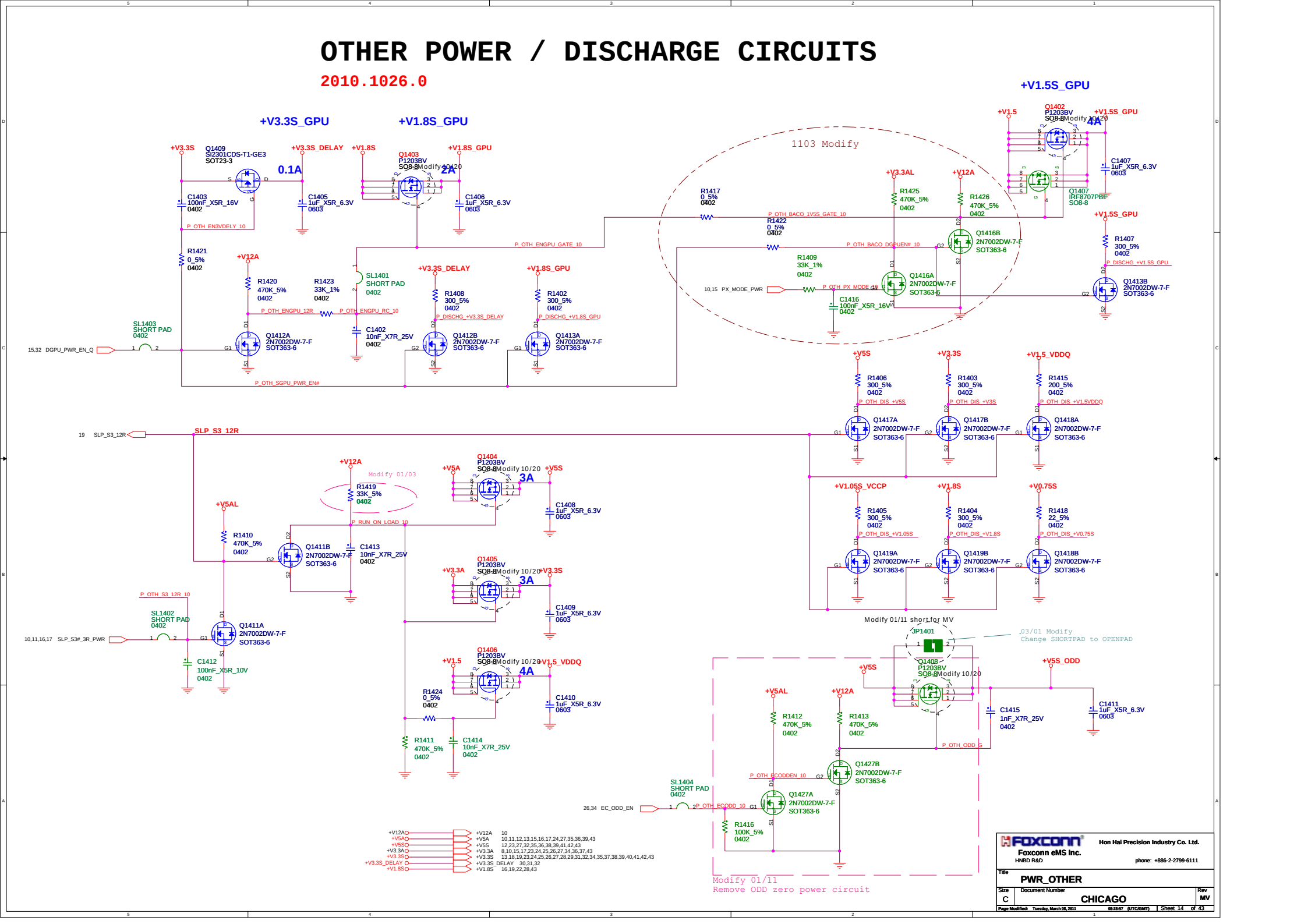
IMVP7 CPU VCORE POWER SUPPLY

2010.1026.0



OTHER POWER / DISCHARGE CIRCUITS

2010.1026.0



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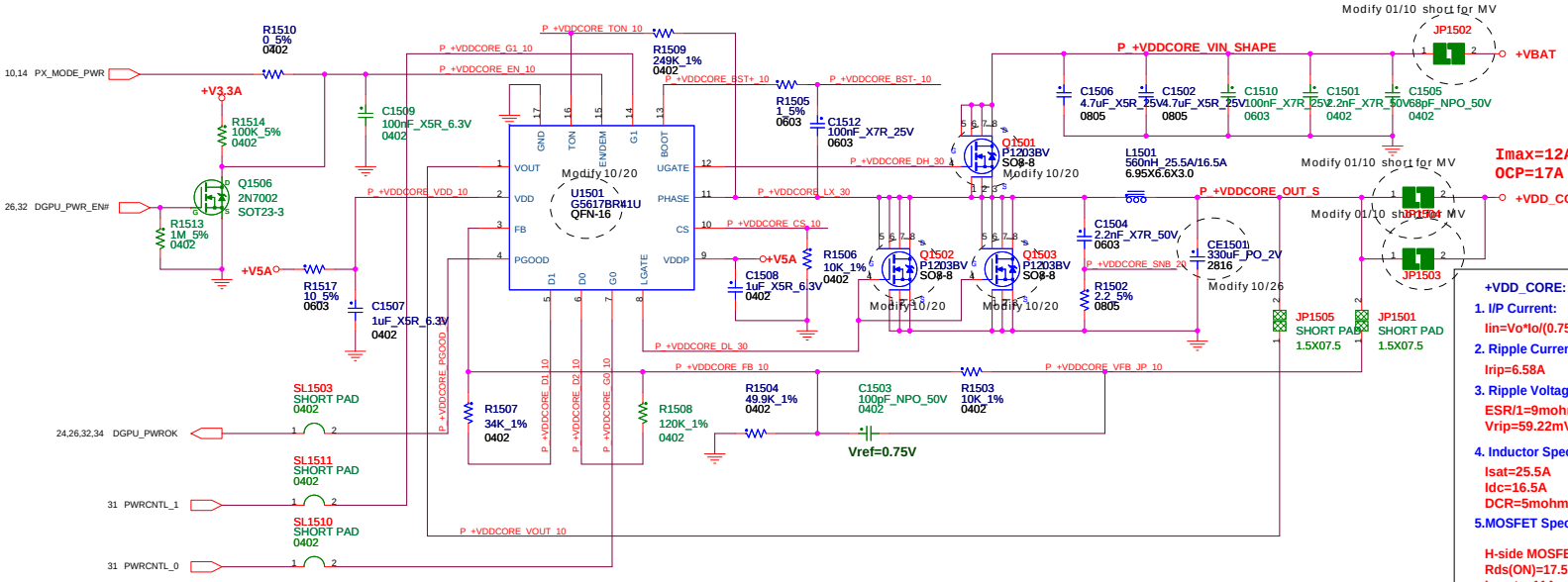
+VDD_CORE POWER SUPPLY

2010.1026.0



PWRCNTL_1	PWRCNTL_0	VDD_CORE
0	---	1.121V
---	---	---
1	---	0.9V
---	---	---

+VDD_CORE:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.48A

2. Ripple Current:

Irip=6.58A

3. Ripple Voltage:

ESR/1=9mohm

Vrip=59.22mV

4. Inductor Spec:

Isat=25.5A

Idc=16.5A

DCR=5mohm

5.MOSFET Spec:

H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
Rds(ON)=17.5mohm (Vgs=4.5 V)	Rds(ON)=17.5mohm (Vgs=4.5 V)
I cont = 11A (T =25 ℃)	I cont = 11A (T =25 ℃)
I peak = 88A (Pause =10 us)	I peak = 88A (Pause =10 us)

6. Frequency:

TON=9.6P*R1509*(VOUT+0.1) / (VIN-0.3)+50ns=206ns

F=VOUT/(VIN*TON)=286KHz

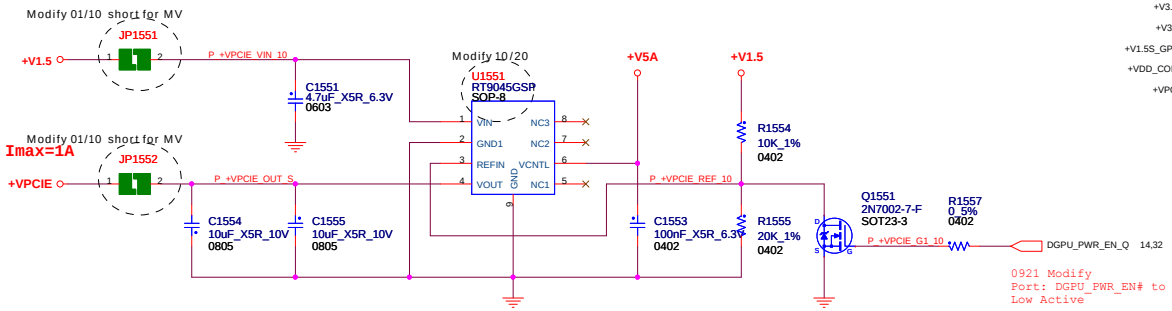
7. OCP:

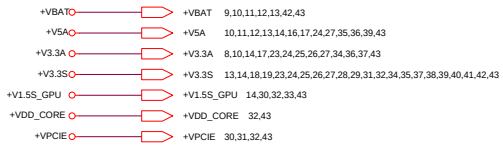
Set = R1506 to 10K

Vtrip= R1206*10uA=0.1V

Iocp=(Vtrip/Rdson) + Iripple/2 = 17A

2010.1020.0 +VPCIE POWER SUPPLY





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+V1.8S POWER SUPPLY

2010.1025.0

+V1.8S:

1. I/P Current:

Iin=Vo*Io/(0.75*Vin)=1.44A

2. Ripple Current:

Irip=0.53A

3. Ripple Voltage:

ESR/3=3.3mohm
Vrip=1.75mV

4. Inductor Spec:

Isat=14A
Idc=8A
DCR=20mohm

5.MOSFET Spec:

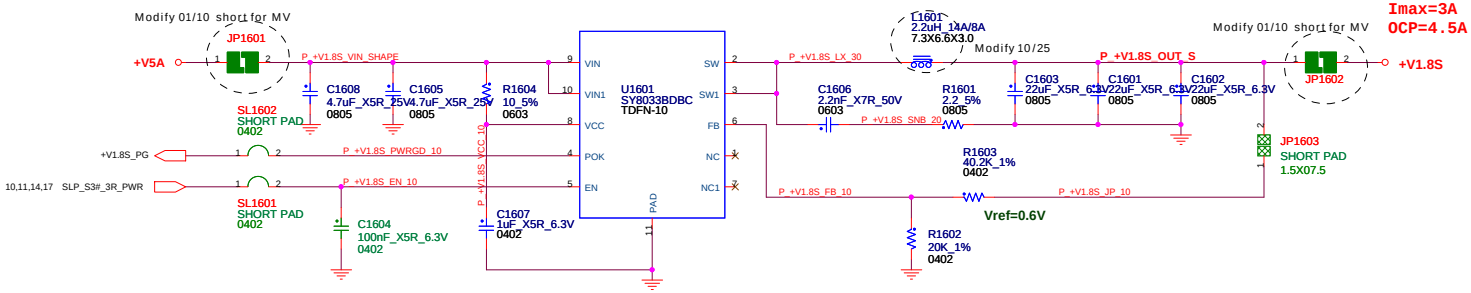
H-side P-MOSFET:	L-side N-MOSFET:
Rds(ON)=110mohm (Vgs=4.5 V)	Rds(ON)=75mohm (Vgs=4.5 V)

6. Frequency:

F=1MHz (min=800KHz, max=1.2MHz)

7. OCP:

Iocp=4A(min)/4.5A(typ)/5A(max)



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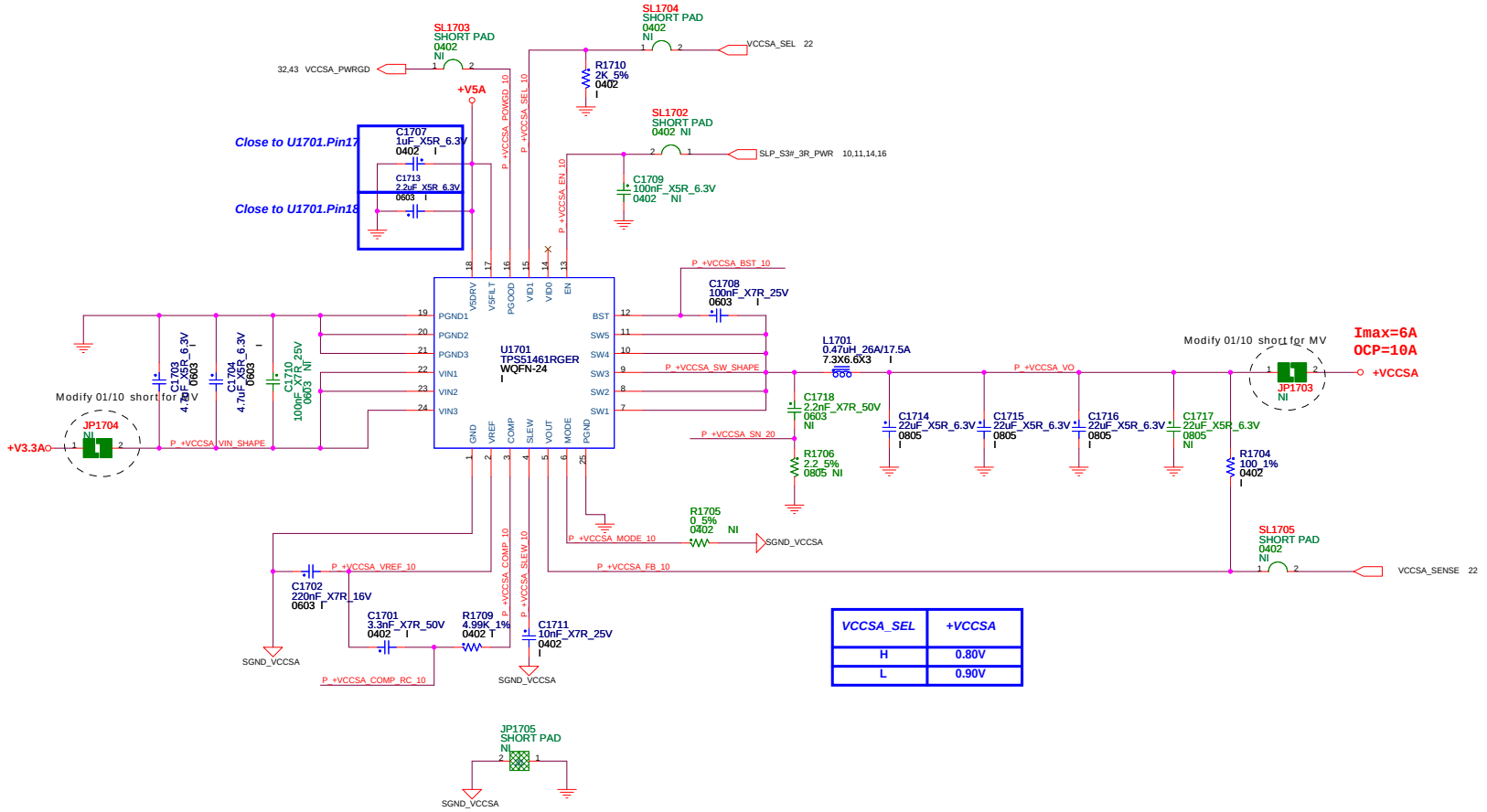
+VCCSA POWER SUPPLY

2010.1026.0

+VCCSA:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.18A
2. Ripple Current:
   Irip=1.39A
3. Ripple Voltage:
   ESR/4=1mohm
   Vrip=1.39mV
4. Inductor Spec:
   Isat=26A
   Idc=17.5A
   DCR=4.2mohm
5. MOSFET Spec:
6. Frequency:
   F=1MHz (R1705=Open)
7. OCP:
   Min : 6A / Typ : 7.5A



VCCSA_SEL	+VCCSA
H	0.80V
L	0.90V

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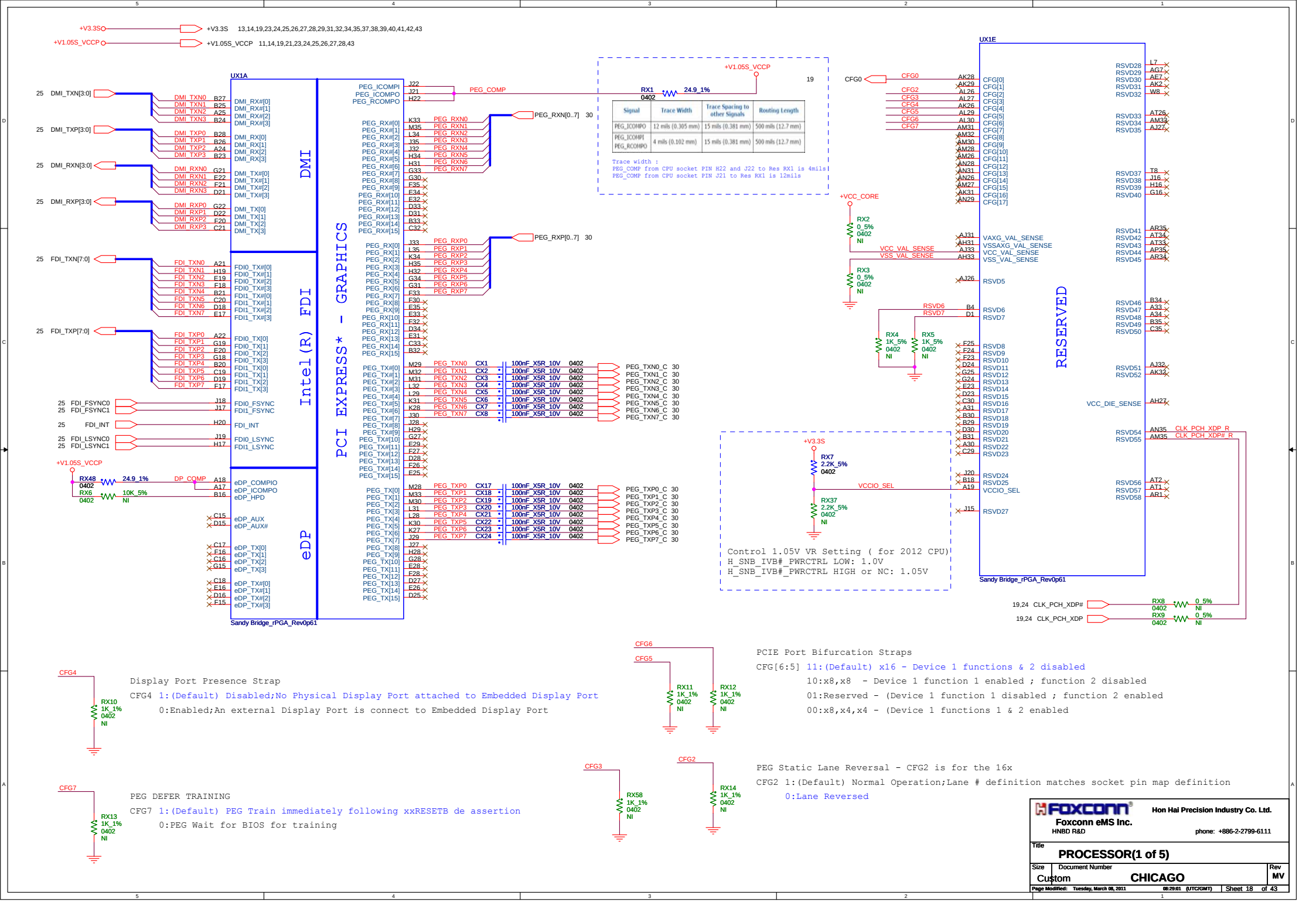
+V3.3S +V3.3S 13,14,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.05S_VCCP +V1.05S_VCCP 11,14,19,21,23,24,25,26,27,28,43
UX1A
DMI
Intel(R) FDI
PCI EXPRESS* - GRAPHICS
eDP
Sandy Bridge_rPGA_Rev0p61
Trace width :
PEG_COMP from CPU socket PIN H22 and J22 to Res RX1 is 4mils
PEG_COMP from CPU socket PIN J21 to Res RX1 is 12mils
Control 1.05V VR Setting (for 2012 CPU)
H_SNB_IVB#_PWRCTRL LOW: 1.0V
H_SNB_IVB#_PWRCTRL HIGH or NC: 1.05V
UX1E
RESERVED
Sandy Bridge_rPGA_Rev0p61
Display Port Presence Strap
CFG4 1:(Default) Disabled;No Physical Display Port attached to Embedded Display Port
0:Enabled;An external Display Port is connect to Embedded Display Port
PEG DEFER TRAINING
CFG7 1:(Default) PEG Train immediately following xxRESETB de assertion
0:PEG Wait for BIOS for training
PCIE Port Bifurcation Straps
CFG[6:5] 11:(Default) x16 - Device 1 functions & 2 disabled
10:x8,x8 - Device 1 function 1 enabled ; function 2 disabled
01:Reserved - (Device 1 function 1 disabled ; function 2 enabled
00:x8,x4,x4 - (Device 1 functions 1 & 2 enabled
PEG Static Lane Reversal - CFG2 is for the 16x
CFG2 1:(Default) Normal Operation;Lane # definition matches socket pin map definition
0:Lane Reversed
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+V3.3S +V3.3S 13,14,18,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.05S_VCCP +V1.05S_VCCP 11,14,18,21,23,24,25,26,27,28,43
+V1.5_VDDQ +V1.5_VDDQ 12,14,22,27,38
+V1.8S +V1.8S 14,16,22,28,43
+V1.5 +V1.5 12,14,15,22,29,43

UX1B
Sandy Bridge_rPGA_Rev0p61

MISC
26 H_SNB_IVB# — RX15 2.2K_5% 0402 — +V1.8S
C26 PROC_SELECT#
AN34 SKTOCC#

CLOCKS
BCLK A28 — CLK_PCH_CPU_CLK 24
BCLK# A27 — CLK_PCH_CPU_CLK# 24 (100MHz)
DPLL_REF_CLK A16 — 0402 RX71 1K_5% 1K_5% — +V1.05S_VCCP
DPLL_REF_CLK# A15 — 0402 RX72 1K_5% 1K_5%

THERMAL
+V1.05S_VCCP — RX18 62_5% 0402
TP_P30 TP1 — 1 H_CATERR# — AL33 CATERR#
26,34 H_PECI — AN33 PECI
13,38 H_PROCHOT# — H_PROCHOT# — RX20 0402 56_5% — H_PROCHOT# R — AL32 PROCHOT#
CX33 43pF_X7R_50V 0402 — Close to VR
26 H_THRMTRIP# — AN32 THERMTRIP#

DDR3 MISC
SM_DRAMRST# R8 — SM_DRAMRST#
SM_RCOMP[0] AK1 — SM_RCOMP0 RX22 140_1% 0402
SM_RCOMP[1] A5 — SM_RCOMP1 RX23 25.5_1% 0402
SM_RCOMP[2] A4 — SM_RCOMP2 RX24 200_1% 0402
RX16 0402 0_5% NI
+V1.5 — RX17 1K_5% 0402
SM_DRAMRST# Q — QX1 2N7002-7-F SOT23-3
RX21 4.99K_1% 0402
RX19 0402 1K_5% — DDR3_DRAMRST# 29
RX25 0402 0_5% — DRAMRST_CNTRL 22,24
CX34 47nF_X7R_16V 0402

PWR MANAGEMENT
25 H_PM_SYNC — AM34 PM_SYNC
26 H_CPUPWRGD — H_CPUPWRGD — AP33 UNCOREPWRGOOD
CX125 100nF_X5R_10V 0402
RX27 10K_5% 0402
SM_DRAMPWROK — V8 SM_DRAMPWROK
BUF_PLT_RST#_R — AR33 RESET#

JTAG & BPM
PRDY# AP29 — XDP_PRDY#
PREQ# AP27 — XDP_PREQ#
TCK AR26 — XDP_TCK
TMS AR27 — XDP_TMS
TRST# AP30 — XDP_TRST#
TDI AR28 — XDP_TDI
TDO AR26 — XDP_TDO
DBR# AL35 — XDP_DBR# — RX26 0402 1K_5% NI — +V3.3S
RX69 0402 0_5% NI — SB_RST# 25
BPM#[0] AT28 — XDP_OBS0
BPM#[1] AR29 — XDP_OBS1
BPM#[2] AR30 — XDP_OBS2
BPM#[3] AT30 — XDP_OBS3
BPM#[4] AP32 — XDP_OBS4
BPM#[5] AR31 — XDP_OBS5
BPM#[6] AT31 — XDP_OBS6
BPM#[7] AR32 — XDP_OBS7

PU/PD for JTAG signals
+V1.05S_VCCP
XDP_TDO RX28 0402 51_5%
XDP_TMS RX29 0402 51_5%
XDP_TDI RX30 0402 51_5%
XDP_PREQ# RX32 0402 51_5% NI
XDP_TCK RX33 0402 51_5%
XDP_TRST# RX35 0402 51_5%

+V3.3S — RX36 200_1% 0402
RX31 0402 0_5% NI — SM_DRAMPWROK_R
+V3.3S — CX126 100nF_Y5V_10V 0402
+V1.5_VDDQ — CX129 1uF_Y5V_6.3V 0402 — RX34 200_1% 0402
25 PM_DRAM_PWRGD
34,43 ALL_SYS_PWRGD
UX4 74LVC2G07GW.125 (1A 1Y 6, GND 3, VCC 2, 2A 5, 2Y 4)
RX38 0402 130_1% — SM_DRAMPWROK
RX75 39_5% 0603 NI
QX4 2N7002-7-F SOT23-3 NI — SLP_S3_12R 14

HEADER1 BSH-030-01-L-D-A-TR NI
XDP_PREQ# XDP_PRDY# XDP_OBS0 XDP_OBS1 XDP_OBS2 XDP_OBS3 XDP_OBS4 XDP_OBS5 XDP_OBS6 XDP_OBS7
GND0 OBSFN_A0 OBSFN_A1 GND2 OBSDATA_A0 OBSDATA_A1 GND4 OBSDATA_A2 OBSDATA_A3 GND6 OBSFN_B0 OBSFN_B1 GND8 OBSDATA_B0 OBSDATA_B1 GND10 OBSDATA_B2 OBSDATA_B3 GND12 PWRGOOD_HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 GND14 SDA SCL TCK1 TCK0 GND16
GND1 OBSFN_C0 OBSFN_C1 GND3 OBSDATA_C0 OBSDATA_C1 GND5 OBSDATA_C2 OBSDATA_C3 GND7 OBSFN_D0 OBSFN_D1 GND9 OBSDATA_D0 OBSDATA_D1 GND11 OBSDATA_D2 OBSDATA_D3 GND13 ITPCLK_HOOK4 ITPCLK#_HOOK5 VCC_OBS_CD RESET#_HOOK6 DBR#_HOOK7 GND15 TDO TRSTn TDI TMS GND17
Hole1 Hole2 62 61
CLK_PCH_XDP 18,24
CLK_PCH_XDP# 18,24
XDP_RST# — RX41 0402 1K_5% NI — +V1.05S_VCCP — BUF_PLT_RST# 26,34,37,38,40
XDP_DBR#
XDP_TDO XDP_TRST# XDP_TDI XDP_TMS

H_CPUPWRGD — RX39 0402 1K_5% NI — XDP_H_CPUPWRGD
25,34 EC_PWRBTN#
+V1.05S_VCCP — RX40 0402 1K_5% NI — XDP_HOOK2
18 CFG0
25,43 SYS_PWROK
CX37 100nF_X5R_6.3V 0402 NI — XDP_TCK

RX70 0402 1.5K_1%
+V3.3S — CX36 100nF_Y5V_10V 0402 NI
+V1.05S_VCCP — RX42 75_1% 0402 NI
26,34,37,38,40 BUF_PLT_RST#
UX3 74LVC1G07GW.125 SOT353-5 NI
BUFO_CPU_RST# — RX43 0402 43_1% NI — BUF_PLT_RST#_R
RX44 750_1% 0402

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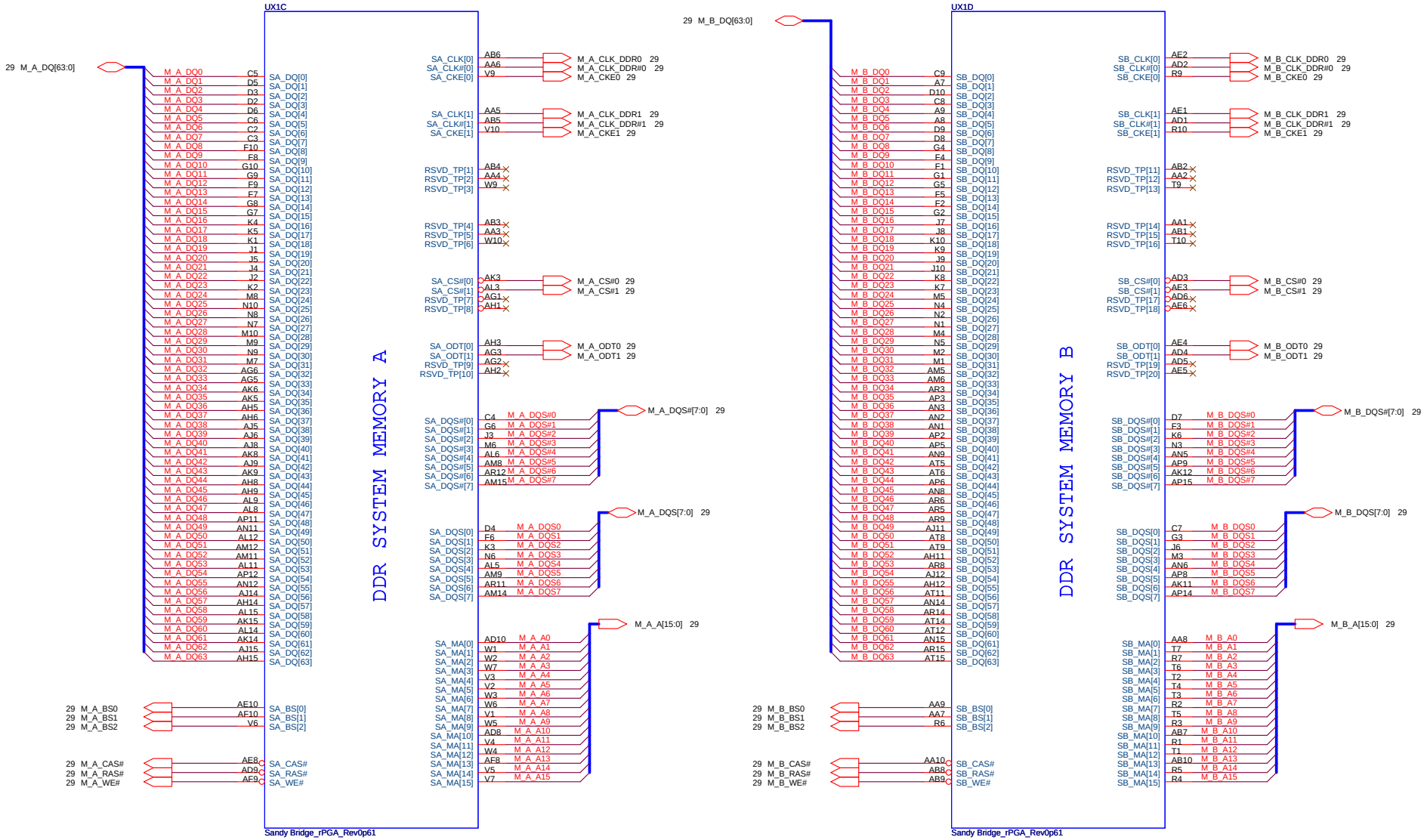

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+V1.05S_VCCP +V1.05S_VCCP 11,14,18,19,23,24,25,26,27,28,43

+VCC_CORE +VCC_CORE 13,18,43

POWER

UX1F

FOR VCC:
4x 330 µF Bottom Edge,
10x 0603 10 µF Bottom Cavity,
8x 0805 22 µF Top Cavity,
8x 0805 22 µF Top Edge,

+VCC_CORE

53A />2120mils

CX41 22uF_X5R_6.3V 0805
CX42 22uF_X5R_6.3V 0805
CX43 22uF_X5R_6.3V 0805
CX44 22uF_X5R_6.3V 0805
CX50 22uF_X5R_6.3V 0805

CX59 22uF_X5R_6.3V 0805
CX60 22uF_X5R_6.3V 0805
CX61 22uF_X5R_6.3V 0805
CX62 22uF_X5R_6.3V 0805
CX63 22uF_X5R_6.3V 0805

RX45 22uF_X5R_6.3V 0805
CX72 22uF_X5R_6.3V 0805
RX46 22uF_X5R_6.3V 0805
CX73 22uF_X5R_6.3V 0805
CX74 22uF_X5R_6.3V 0805

CX75 22uF_X5R_6.3V 0805

CX79 10uF_X5R_6.3V 0603
CX80 10uF_X5R_6.3V 0603
CX81 10uF_X5R_6.3V 0603
RX51 10uF_X5R_6.3V 0603
CX82 10uF_X5R_6.3V 0603

RX54 10uF_X5R_6.3V 0603
CX83 10uF_X5R_6.3V 0603
RX55 10uF_X5R_6.3V 0603
CX84 10uF_X5R_6.3V 0603
CX85 10uF_X5R_6.3V 0603

RX59 33pF_NPO_50V 0402
CX87 33pF_NPO_50V 0402

+VCC_CORE

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AF26 VCC20
AD35 VCC21
AD34 VCC22
AD33 VCC23
AD32 VCC24
AD31 VCC25
AD30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AA35 VCC41
AA34 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
AA26 VCC50
Y35 VCC51
Y34 VCC52
Y33 VCC53
Y32 VCC54
Y31 VCC55
Y30 VCC56
Y29 VCC57
Y28 VCC58
Y27 VCC59
Y26 VCC60
V35 VCC61
V34 VCC62
V33 VCC63
V32 VCC64
V31 VCC65
V30 VCC66
V29 VCC67
V28 VCC68
V27 VCC69
V26 VCC70
U35 VCC71
U34 VCC72
U33 VCC73
U32 VCC74
U31 VCC75
U30 VCC76
U29 VCC77
U28 VCC78
U27 VCC79
U26 VCC80
R35 VCC81
R34 VCC82
R33 VCC83
R32 VCC84
R31 VCC85
R30 VCC86
R29 VCC87
R28 VCC88
R27 VCC89
R26 VCC90
P35 VCC91
P34 VCC92
P33 VCC93
P32 VCC94
P31 VCC95
P30 VCC96
P29 VCC97
P28 VCC98
P27 VCC99
P26 VCC100

PEG AND DDR

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AG10
VCCIO4 AC10
VCCIO5 Y10
VCCIO6 U10
VCCIO7 P10
VCCIO8 L10
VCCIO9 J14
VCCIO10 J13
VCCIO11 J12
VCCIO12 J11
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
VCCIO34 B14
VCCIO35 B12
VCCIO36 A14
VCCIO37 A13
VCCIO38 A12
VCCIO39 A11
VCCIO40 J23

FOR VCCIO:
2x 330 µF,
5x 0805 22 µF Bottom Cavity,
7x 0805 22 µF Top Cavity,

RF solution

0402 68pF_NPO_50V CX113 NI
0402 1nF_X7R_16V CX112 NI

+V1.05S_VCCP

8.5A />340mils

CX65 22uF_X5R_6.3V 0805
CX66 22uF_X5R_6.3V 0805
CX47 22uF_X5R_6.3V 0805
CX38 22uF_X5R_6.3V 0805
CX48 22uF_X5R_6.3V 0805
CX39 22uF_X5R_6.3V 0805
CX40 22uF_X5R_6.3V 0805

CX70 330uF_PO_2V 2816
CX54 22uF_X5R_6.3V 0805
CX55 22uF_X5R_6.3V 0805
CX56 22uF_X5R_6.3V 0805
CX57 22uF_X5R_6.3V 0805
CX58 22uF_X5R_6.3V 0805

CORE SUPPLY

SVID

VIDALERT# AJ29 VR_SVID_ALERT#_R
VIDSCLK AJ30 VR_SVID_CLK_R
VIDSOUT AJ28 VR_SVID_DATA_R

Close to VR

+V1.05S_VCCP

RX47 75_5% 0402
CX123 100nF_X5R_10V 0402 NI

Close to CPU

RX49 43_5% 0402

VR_VIDALERT# 13

Close to VR

+V1.05S_VCCP

RX50 54.9_1% 0402

RX52 0_5% 0402

VR_VIDSCLK 13

Close to CPU

+V1.05S_VCCP

CX124 100nF_X5R_10V 0402 NI

RX53 130_5% 0402

Close to VR

+V1.05S_VCCP

RX56 130_5% 0402

RX57 0_5% 0402

VR_VIDSOUT 13

SENSE LINES

+VCC_CORE

RX76 100_5% 0402

VCC_SENSE AJ35
VSS_SENSE AJ34

VCC_SENSE 13
VSS_SENSE 13

RX77 100_5% 0402

VCCIO_SENSE B10
VSSIO_SENSE A10

VCCP_SENSE 11
VSSP_SENSE 11

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VSS

UX1H

AT35 VSS1
AT32 VSS2
AT29 VSS3
AT27 VSS4
AT25 VSS5
AT22 VSS6
AT19 VSS7
AT16 VSS8
AT13 VSS9
AT10 VSS10
AT7 VSS11
AT4 VSS12
AT3 VSS13
AR25 VSS14
AR22 VSS15
AR19 VSS16
AR16 VSS17
AR13 VSS18
AR10 VSS19
AR7 VSS20
AR4 VSS21
AR2 VSS22
AP34 VSS23
AP31 VSS24
AP28 VSS25
AP25 VSS26
AP22 VSS27
AP19 VSS28
AP16 VSS29
AP13 VSS30
AP10 VSS31
AP7 VSS32
AP4 VSS33
AP1 VSS34
AN30 VSS35
AN27 VSS36
AN25 VSS37
AN22 VSS38
AN19 VSS39
AN16 VSS40
AN13 VSS41
AN10 VSS42
AN7 VSS43
AN4 VSS44
AM29 VSS45
AM25 VSS46
AM22 VSS47
AM19 VSS48
AM16 VSS49
AM13 VSS50
AM10 VSS51
AM7 VSS52
AM4 VSS53
AM3 VSS54
AM2 VSS55
AM1 VSS56
AL34 VSS57
AL31 VSS58
AL28 VSS59
AL25 VSS60
AL22 VSS61
AL19 VSS62
AL16 VSS63
AL13 VSS64
AL10 VSS65
AL7 VSS66
AL4 VSS67
AL2 VSS68
AK33 VSS69
AK30 VSS70
AK27 VSS71
AK25 VSS72
AK22 VSS73
AK19 VSS74
AK16 VSS75
AK13 VSS76
AK10 VSS77
AK7 VSS78
AK4 VSS79
AJ25 VSS80

VSS81 AJ22
VSS82 AJ19
VSS83 AJ16
VSS84 AJ13
VSS85 AJ10
VSS86 AJ7
VSS87 AJ4
VSS88 AJ3
VSS89 AJ2
VSS90 AJ1
VSS91 AH35
VSS92 AH34
VSS93 AH32
VSS94 AH30
VSS95 AH29
VSS96 AH28
VSS97 AH26
VSS98 AH25
VSS99 AH22
VSS100 AH19
VSS101 AH16
VSS102 AH7
VSS103 AH4
VSS104 AG9
VSS105 AG8
VSS106 AG4
VSS107 AF6
VSS108 AF5
VSS109 AF3
VSS110 AF2
VSS111 AE35
VSS112 AE34
VSS113 AE33
VSS114 AE32
VSS115 AE31
VSS116 AE30
VSS117 AE29
VSS118 AE28
VSS119 AE27
VSS120 AE26
VSS121 AE9
VSS122 AD7
VSS123 AC9
VSS124 AC8
VSS125 AC6
VSS126 AC5
VSS127 AC3
VSS128 AC2
VSS129 AB35
VSS130 AB34
VSS131 AB33
VSS132 AB32
VSS133 AB31
VSS134 AB30
VSS135 AB29
VSS136 AB28
VSS137 AB27
VSS138 AB26
VSS139 Y9
VSS140 Y8
VSS141 Y6
VSS142 Y5
VSS143 Y3
VSS144 Y2
VSS145 W35
VSS146 W34
VSS147 W33
VSS148 W32
VSS149 W31
VSS150 W30
VSS151 W29
VSS152 W28
VSS153 W27
VSS154 W26
VSS155 U9
VSS156 U8
VSS157 U6
VSS158 U5
VSS159 U3
VSS160 U2

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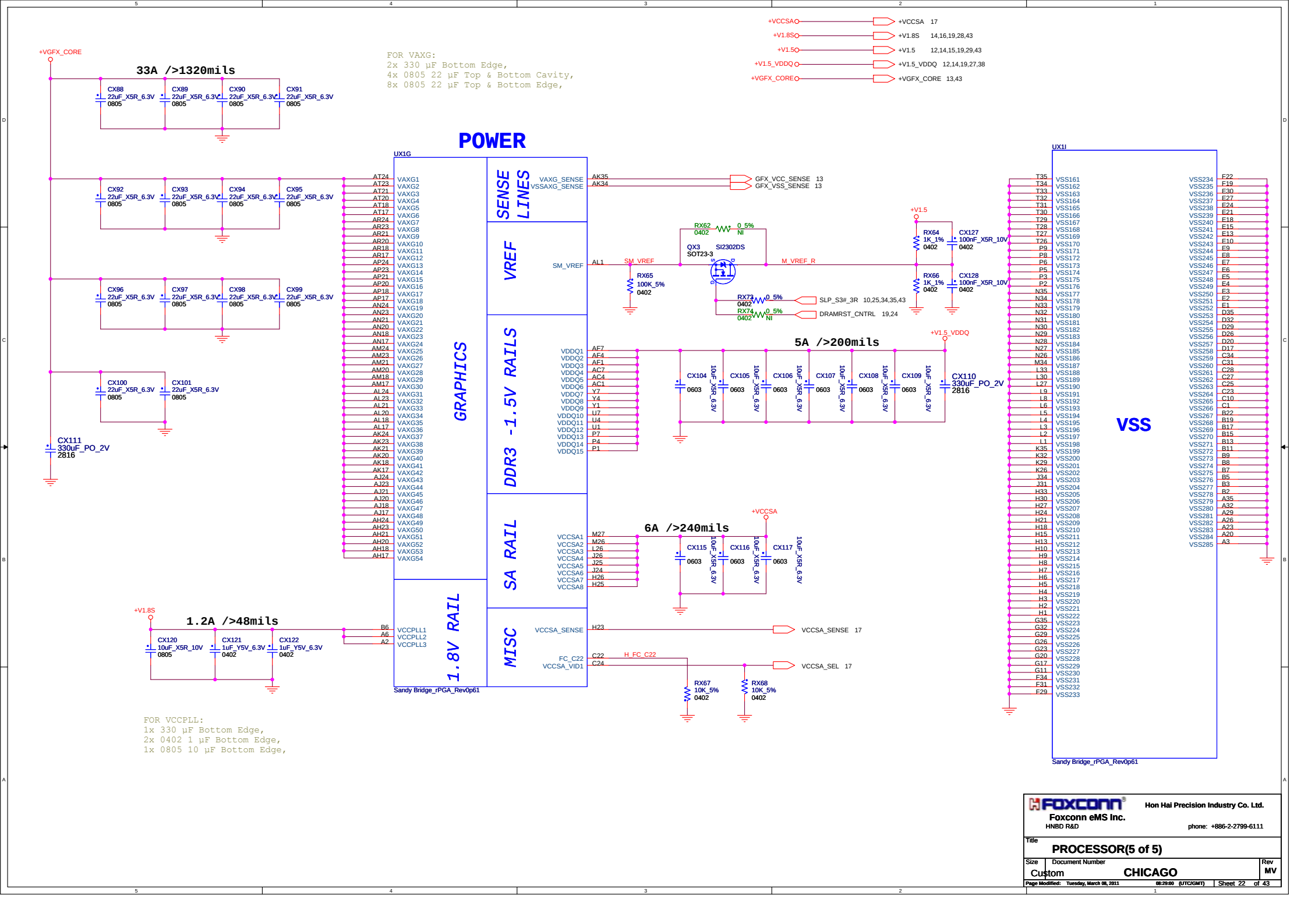
+VCCSA 17
+V1.8S 14,16,19,28,43
+V1.5 12,14,15,19,29,43
+V1.5_VDDQ 12,14,19,27,38
+VGFX_CORE 13,43
+VGFX_CORE
33A />1320mils
CX88 22uF_X5R_6.3V 0805
CX89 22uF_X5R_6.3V 0805
CX90 22uF_X5R_6.3V 0805
CX91 22uF_X5R_6.3V 0805
CX92 22uF_X5R_6.3V 0805
CX93 22uF_X5R_6.3V 0805
CX94 22uF_X5R_6.3V 0805
CX95 22uF_X5R_6.3V 0805
CX96 22uF_X5R_6.3V 0805
CX97 22uF_X5R_6.3V 0805
CX98 22uF_X5R_6.3V 0805
CX99 22uF_X5R_6.3V 0805
CX100 22uF_X5R_6.3V 0805
CX101 22uF_X5R_6.3V 0805
CX111 330uF_PO_2V 2816
FOR VAXG:
2x 330 µF Bottom Edge,
4x 0805 22 µF Top & Bottom Cavity,
8x 0805 22 µF Top & Bottom Edge,
POWER
UX1G
SENSE LINES
VAXG_SENSE
VSSAXG_SENSE
AK35
AK34
GFX_VCC_SENSE 13
GFX_VSS_SENSE 13
VREF
SM_VREF
AL1
RX62 0_5% 0402 NI
QX3 SI2302DS SOT23-3
RX65 100K_5% 0402
RX73 0_5% 0402
RX74 0_5% 0402 NI
SLP_S3#_3R 10,25,34,35,43
DRAMRST_CNTRL 19,24
+V1.5
RX64 1K_1% 0402
RX66 1K_1% 0402
CX127 100nF_X5R_10V 0402
CX128 100nF_X5R_10V 0402
GRAPHICS
DDR3 -1.5V RAILS
5A />200mils
+V1.5_VDDQ
VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15
AF7 AF4 AF1 AC7 AC4 AC1 V7 Y4 Y1 U7 U4 U1 P7 P4 P1
CX104 CX105 CX106 CX107 CX108 CX109 0603 10uF_X5R_6.3V
CX110 330uF_PO_2V 2816
SA RAIL
6A />240mils
+VCCSA
VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8
M27 M26 L26 J26 J25 J24 H26 H25
CX115 CX116 CX117 0603 10uF_X5R_6.3V
MISC
VCCSA_SENSE
H23
VCCSA_SENSE 17
FC_C22
VCCSA_VID1
C22 C24
H_FC_C22
VCCSA_SEL 17
RX67 10K_5% 0402
RX68 10K_5% 0402
1.8V RAIL
+V1.8S
1.2A />48mils
CX120 10uF_X5R_10V 0805
CX121 1uF_Y5V_6.3V 0402
CX122 1uF_Y5V_6.3V 0402
B6 A6 A2
VCCPLL1 VCCPLL2 VCCPLL3
Sandy Bridge_rPGA_Rev0p61
FOR VCCPLL:
1x 330 µF Bottom Edge,
2x 0402 1 µF Bottom Edge,
1x 0805 10 µF Bottom Edge,
UX1I
VSS
VSS161 VSS162 VSS163 VSS164 VSS165 VSS166 VSS167 VSS168 VSS169 VSS170 VSS171 VSS172 VSS173 VSS174 VSS175 VSS176 VSS177 VSS178 VSS179 VSS180 VSS181 VSS182 VSS183 VSS184 VSS185 VSS186 VSS187 VSS188 VSS189 VSS190 VSS191 VSS192 VSS193 VSS194 VSS195 VSS196 VSS197 VSS198 VSS199 VSS200 VSS201 VSS202 VSS203 VSS204 VSS205 VSS206 VSS207 VSS208 VSS209 VSS210 VSS211 VSS212 VSS213 VSS214 VSS215 VSS216 VSS217 VSS218 VSS219 VSS220 VSS221 VSS222 VSS223 VSS224 VSS225 VSS226 VSS227 VSS228 VSS229 VSS230 VSS231 VSS232 VSS233
T35 T34 T33 T32 T31 T30 T29 T28 T27 T26 P9 P8 P6 P5 P3 P2 N35 N34 N33 N32 N31 N30 N29 N28 N27 N26 M34 L33 L30 L27 L9 L8 L6 L5 L4 L3 L2 L1 K35 K32 K29 K26 J34 J31 H33 H30 H27 H24 H21 H18 H15 H13 H10 H9 H8 H7 H6 H5 H4 H3 H2 H1 G35 G32 G29 G26 G23 G20 G17 G11 F34 F31 F29
VSS234 VSS235 VSS236 VSS237 VSS238 VSS239 VSS240 VSS241 VSS242 VSS243 VSS244 VSS245 VSS246 VSS247 VSS248 VSS249 VSS250 VSS251 VSS252 VSS253 VSS254 VSS255 VSS256 VSS257 VSS258 VSS259 VSS260 VSS261 VSS262 VSS263 VSS264 VSS265 VSS266 VSS267 VSS268 VSS269 VSS270 VSS271 VSS272 VSS273 VSS274 VSS275 VSS276 VSS277 VSS278 VSS279 VSS280 VSS281 VSS282 VSS283 VSS284 VSS285
F22 F19 E30 E27 E24 E21 E18 E15 E13 E10 E9 E8 E7 E6 E5 E4 E3 E2 E1 D35 D32 D29 D26 D20 D17 C34 C31 C28 C27 C25 C23 C10 C1 B22 B19 B17 B15 B13 B11 B9 B8 B7 B5 B3 B2 A35 A32 A29 A26 A23 A20 A3
Sandy Bridge_rPGA_Rev0p61
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Title
PROCESSOR(5 of 5)
Size Custom
Document Number CHICAGO
Rev MV
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RTCRST# 18~25msS

+VCC_RTC

12/06 Modify

RF solution

<24MHz>

6 mils

02/14 Modify
Change SATA port from SATA1 to SATA2

On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low. (Default:1.5V for Mobile)

No REBOOT

RS24 NI=Disabled
RS24 I=Enabled

GPIO33 Internal PU PD for Manufacturing environment

PCH JTAG Disable

FOR ME FUNCTION

Flash Descriptor Security overridden

Modify 11/11
Remove parts from PV build

Place R12 resistor close to PCH

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Title	CougarPoint(1 of 6)
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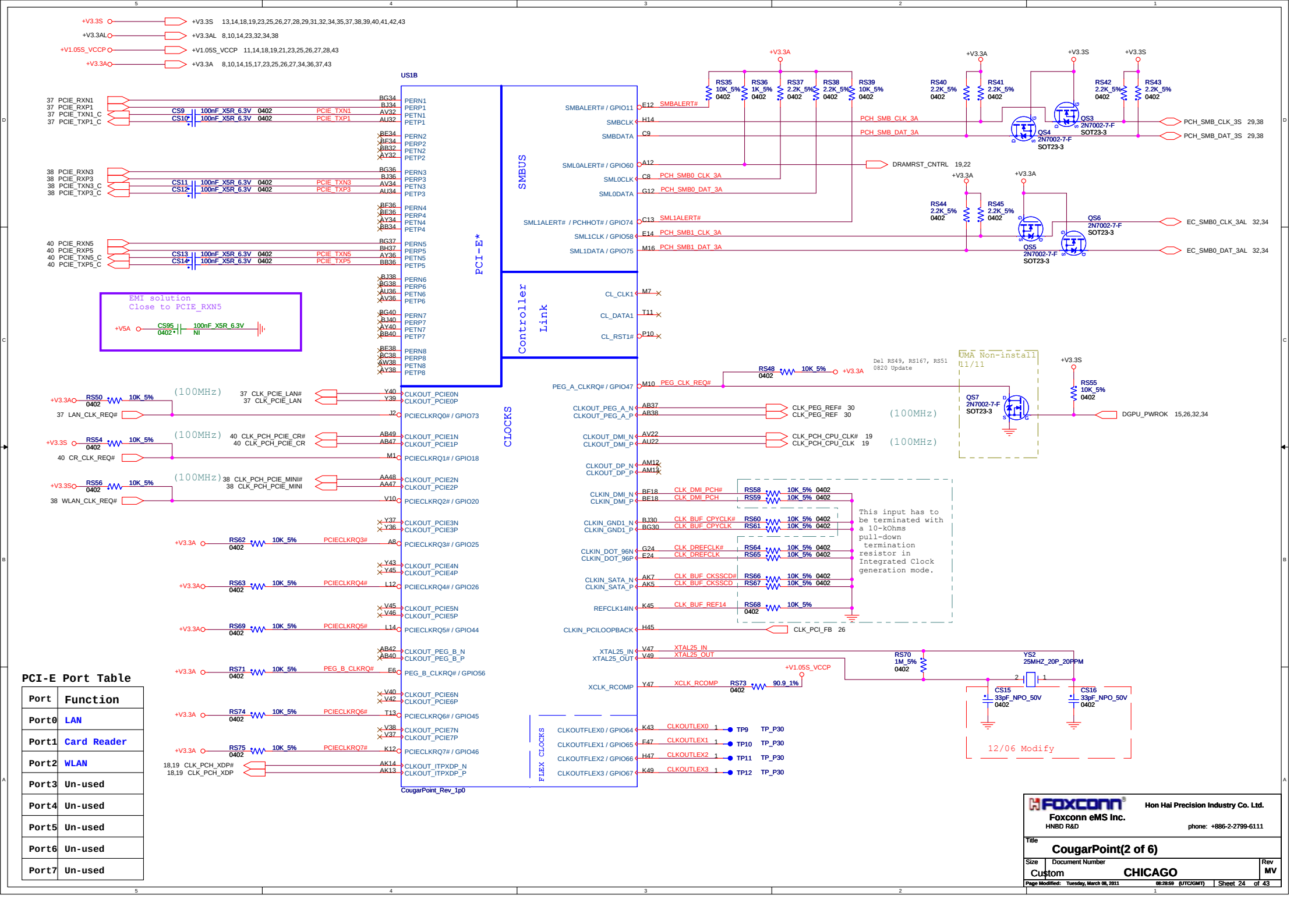

PCI-E Port Table

Port	Function
Port0	LAN
Port1	Card Reader
Port2	WLAN
Port3	Un-used
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used

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Title	CougarPoint(2 of 6)
Size: Custom	Document Number: CHICAGO
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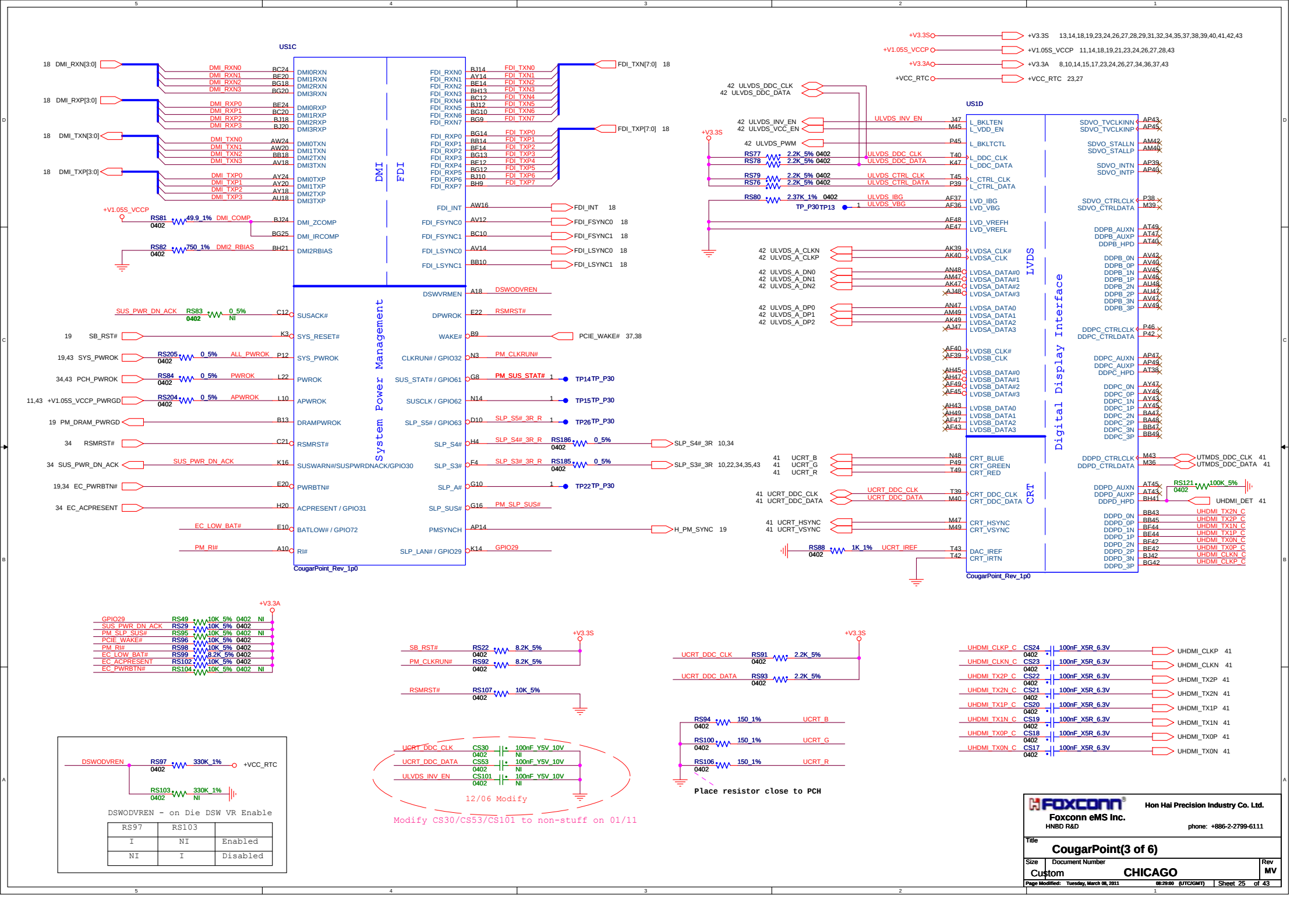
US1C
DMI
FDI
System Power Management
CougarPoint_Rev_1p0
US1D
LVDS
Digital Display Interface
CRT
CougarPoint_Rev_1p0
DSWODVREN - on Die DSW VR Enable
RS97 | RS103 |
I | NI | Enabled
NI | I | Disabled
12/06 Modify
Modify CS30/CS53/CS101 to non-stuff on 01/11
Place resistor close to PCH
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CougarPoint(3 of 6)
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Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

RS108 0402 1K_5% NI BBS_BIT1

+V3.3S

RS111 0402 8.2K_5% INT_PIRQA#
RS113 0402 8.2K_5% INT_PIRQB#
RS115 0402 8.2K_5% INT_PIRQC#
RS117 0402 8.2K_5% INT_PIRQD#
RS118 0402 8.2K_5% DGPU_HOLD_RST#
RS119 0402 8.2K_5% NI DGPU_DDC_SELECT#
RS120 0402 8.2K_5% DGPU_PWR_EN#
RS122 0402 8.2K_5% SB_ODD_MD#
RS123 0402 8.2K_5% SATA_ODD_DA#
RS124 0402 8.2K_5% INT_PIRQG#
RS125 0402 8.2K_5% INT_PIRQH#

RS126 0402 100K_5% NI PLT_RST#

Del RS121 8.2Kohm to +V3.3S
0820 Update

30 DGPU_HOLD_RST# DGPU_HOLD_RST# RS46 0402 0_5% DGPU_PWR_EN# 15,32 DGPU_PWR_EN#
12/06 Modify

TP_P30 TP17 1 DGPU_PWM_SELECT# DGPU_DDC_SELECT#

39 SB_ODD_MD# SB_ODD_MD# SATA_ODD_DA# INT_PIRQG# INT_PIRQH#

TP_P30 TP18 1 PCI_PME#

30 PLT_RST# PLT_RST#

38 CLK_PCI_JIG RS134 0402 22_5% TP_P30 TP19 1 CLK_PCI_JIG_R
34 CLK_PCI_KBC RS135 0402 22_5% TP_P30 TP20 1 CLK_PCI_KBC_R
24 CLK_PCI_FB RS136 0402 22_5% CLK_PCI_FB_R

US1E

RSVD: TP1–TP20, TP21–TP24, TP25–TP40

PCI: PIRQA# PIRQB# PIRQC# PIRQD# REQ1# / GPIO50 REQ2# / GPIO52 REQ3# / GPIO54 GNT1# / GPIO51 GNT2# / GPIO53 GNT3# / GPIO55 PIRQE# / GPIO2 PIRQF# / GPIO3 PIRQG# / GPIO4 PIRQH# / GPIO5 PME# PLTRST# CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4

USB: USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P USBRBIAS# USBRBIAS OC0# / GPIO59 OC1# / GPIO40 OC2# / GPIO41 OC3# / GPIO42 OC4# / GPIO43 OC5# / GPIO9 OC6# / GPIO10 OC7# / GPIO14

USB_PN0 39 USB_PP0 39 USB_PN1 39 USB_PP1 39 USB_PN2 39 USB_PP2 39
USB_PN10 42 USB_PP10 42 USB_PN11 38 USB_PP11 38
USBRBIAS RS131 0402 22.6_1%
USB_OC#0 39 USB_OC#1 39

CougarPoint_Rev_1p0

US1F

GPIO: GPIO0 BMBUSY# / GPIO0 … GPIO57

CPU/MISC: TACH4 / GPIO68 … TACH7 / GPIO71 A20GATE PECI RCIN# PROCPWRGD THRMTRIP# INIT3_3V# DF_TVS TS_VSS1–4 NC_1

NCTF: VSS_NCTF_1 … VSS_NCTF_32

CougarPoint_Rev_1p0

34 PCI_SERR# RS17 0402 0_5%
34 EC_SMI#
DGPU_HPD_INTR#
34 RUN_SCI#
TP_P30 TP25 1
GPIO12
23 MB_FLASH0_EN
GPIO16
15,24,32,34 DGPU_PWROK
GPIO22
TP_P30 TP16 1
GPIO24
GPIO27
GPIO28
GPIO34
GPIO35
SB_ODD_IN# Q
GPIO37
MFG_MODE
GFX_DET
GPIO48
GPIO49
GPIO57

RS127 10K_5% 0402

+V3.3S +V3.3S 13,14,18,19,23,24,25,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V3.3A +V3.3A 8,10,14,15,17,23,24,25,27,34,36,37,43

C40 RS201 0402 0_5% EC_ODD_EN 14,34
B41 GPIO69
C41 GPIO70
A40 GPIO71
RS109 10K_5% 0402

P4 A20GATE 34
AU16 H_PECI_R RS110 0402 0_5% NI H_PECI 19,34
P5 KBRST# 34
AY11 H_CPUPWRGD 19
AY10 H_THRMTRIP# R RS112 0402 390_1% H_THRMTRIP# 19
T14 RS114 0402 56_5% NI +V1.05S_VCCP
AY1 H_SNB_IVB# R RS116 0402 1K_5% H_SNB_IVB# 19

AH8 AK11 AH10 AK10

P37

BG2 BG49 BH3 BH47 BJ4 BJ44 BJ45 BJ46 BJ5 BJ6 C2 C48 D1 D49 E1 E49 F1 F49

PLL ON DIE VR ENABLE		
GP28	0	disable
	1	Enable(Default)

+V3.3A
RS132 0402 10K_5% GPIO28 RS130 0402 1K_5% NI

+V3.3A
RS195 0402 10K_5% GPIO24
RS137 0402 10K_5% GPIO12
RS138 0402 1K_5% MB_FLASH0_EN

+V3.3S
RS139 0402 10K_5% GPIO70
RS140 0402 10K_5% GPIO71
RS141 0402 10K_5% GPIO0
RS142 0402 10K_5% EC_SMI#
RS146 0402 10K_5% DGPU_HPD_INTR#
RS154 0402 10K_5% MFG_MODE
RS158 0402 10K_5% GFX_DET
RS159 0402 10K_5% GPIO16
RS160 0402 10K_5% GPIO49
RS161 0402 10K_5% GPIO22
RS162 0402 10K_5% GPIO34
RS163 0402 10K_5% GPIO48
RS133 0402 220K_5% GPIO37

GPIO27 RS143 0402 10K_5%
GPIO35 RS148 0402 1K_5% NI
DGPU_PWROK RS155 0402 100K_5% NI

+V3.3S
US4 74LVC1G17GW.125
19,34,37,38,40 BUF_PLT_RST# RS152 100K_5% 0402 PLT_RST#

USB_OC#0 0402 10K_5% RS144
USB_OC#1 0402 10K_5% RS145
USB_OC#2 0402 10K_5% RS147
+V3.3A

12/06 Modify
DGPU_HOLD_RST# CS102 0402 100nF_Y5V_10V NI
SB_ODD_MD# CS103 0402 100nF_Y5V_10V NI

Modify CS102/CS103 to non-stuff on 01/11

+V3.3S
QS10 2N7002-7-F SOT23-3 NI
RS164 220K_5% 0402
39 SB_ODD_IN# SB_ODD_IN# Q
PLT_RST#

02/24 Modify
same as the PV build

USB PORT	Function	OC#
PORT-0	USB Port	OC0#
PORT-1	USB Port	
PORT-2	USB Port	OC1#
PORT-3	NC	
PORT-4	NC	
PORT-5	NC	
PORT-6	NC	
PORT-7	NC	
PORT-8	NC	
PORT-9	NC	
PORT-10	Camera	
PORT-11	WLAN/BT	
PORT-12	NC	
PORT-13	NC	

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Title: CougarPoint(4 of 6)

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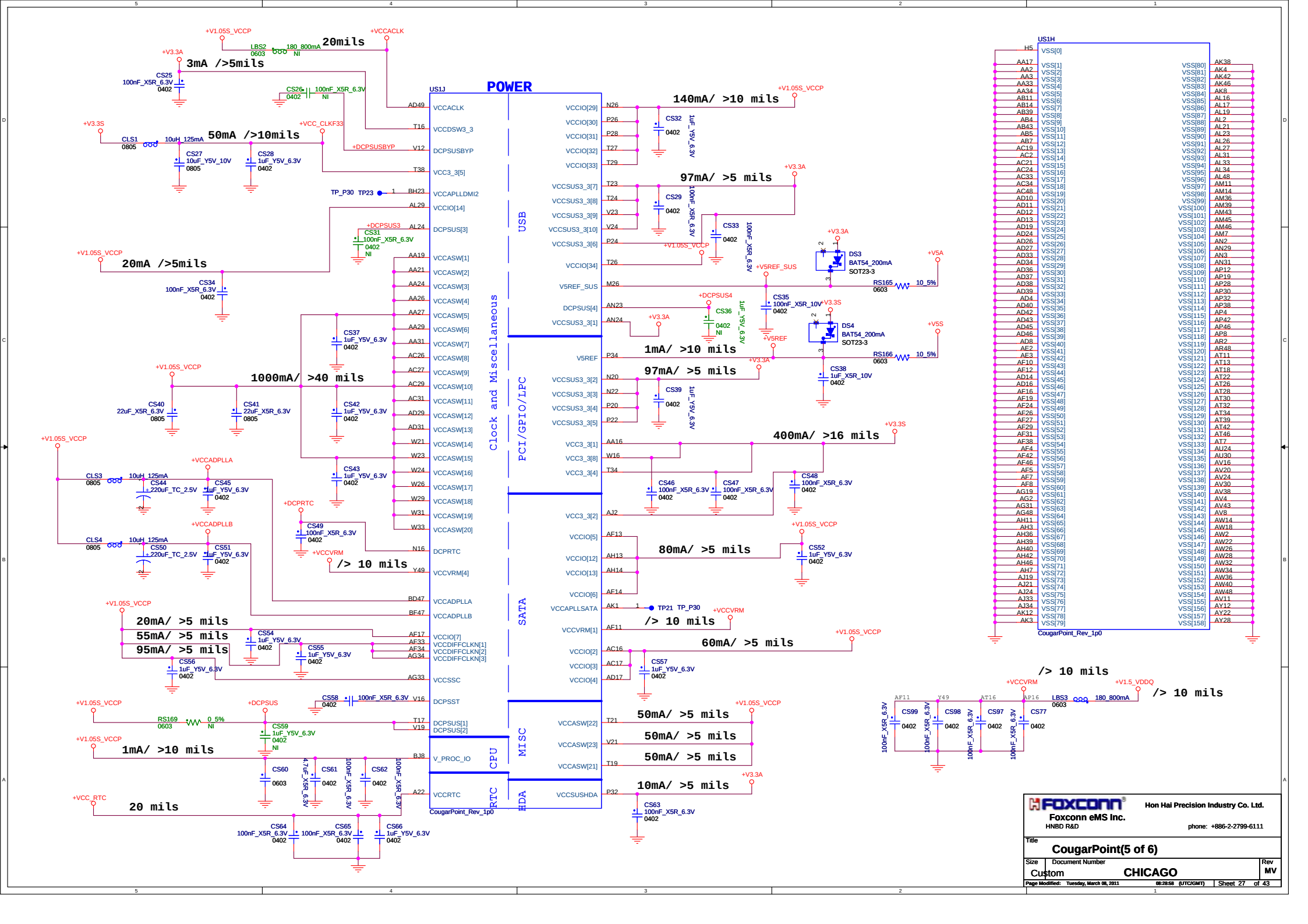
POWER
US1J
CougarPoint_Rev_1p0
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
20mils
3mA />5mils
50mA />10mils
20mA />5mils
1000mA/ >40 mils
/> 10 mils
20mA/ >5 mils
55mA/ >5 mils
95mA/ >5 mils
1mA/ >10 mils
20 mils
140mA/ >10 mils
97mA/ >5 mils
1mA/ >10 mils
97mA/ >5 mils
400mA/ >16 mils
80mA/ >5 mils
/> 10 mils
60mA/ >5 mils
50mA/ >5 mils
50mA/ >5 mils
50mA/ >5 mils
10mA/ >5 mils
/> 10 mils
/> 10 mils
US1H
CougarPoint_Rev_1p0
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CougarPoint(5 of 6)
Custom
CHICAGO
Rev MV
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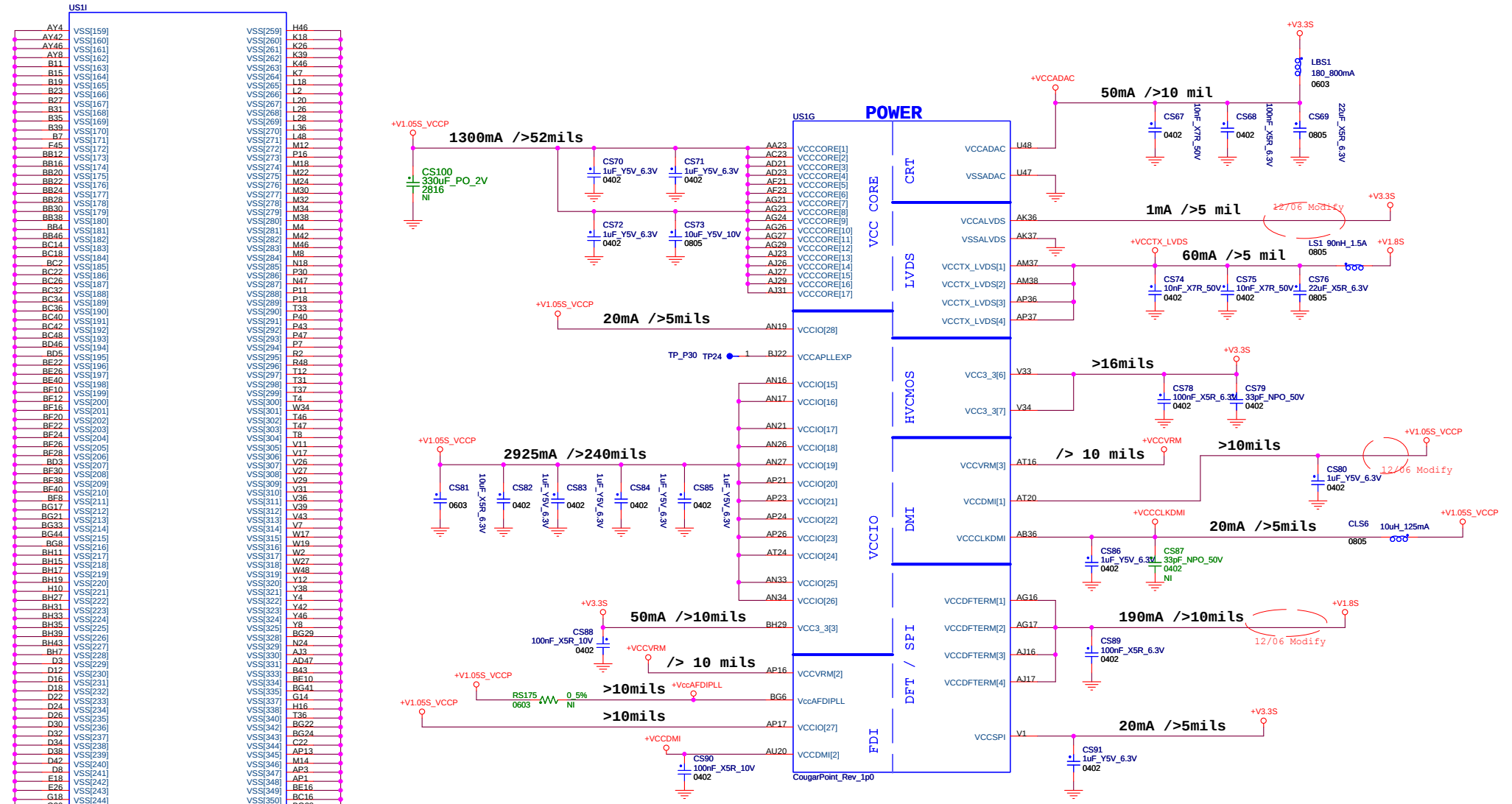
US1I
CougarPoint_Rev_1p0
US1G
POWER
VCC CORE
VCCIO
CRT
LVDS
HVCMOS
DMI
SPI
DFT / FDI
CougarPoint_Rev_1p0
1300mA />52mils
20mA />5mils
2925mA />240mils
50mA />10mils
/> 10 mils
>10mils
>10mils
50mA />10 mil
1mA />5 mil
12/06 Modify
60mA />5 mil
>16mils
/> 10 mils
>10mils
12/06 Modify
20mA />5mils
190mA />10mils
12/06 Modify
20mA />5mils
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CougarPoint(6 of 6)
Custom
CHICAGO
Rev MV
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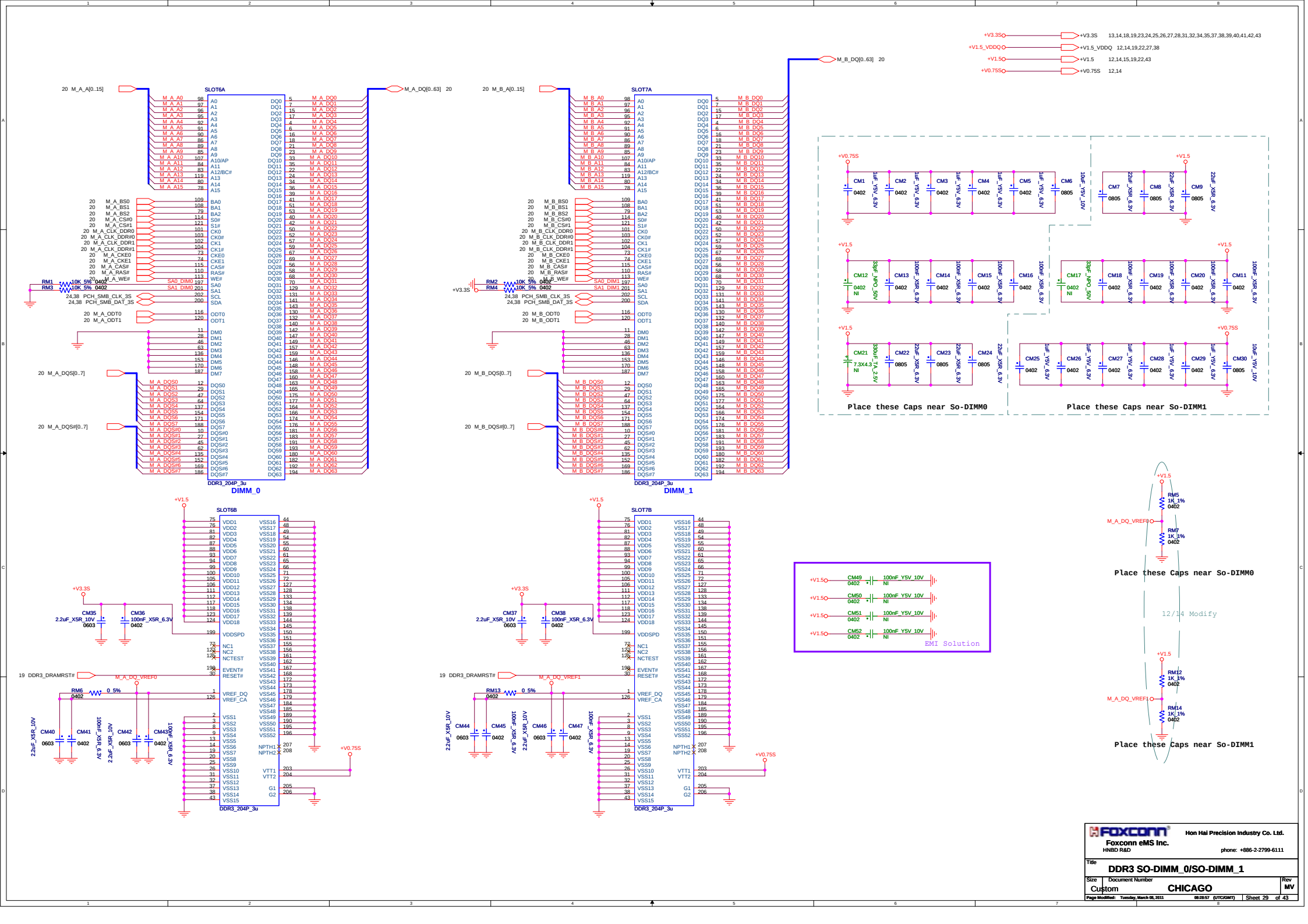

Foxconn eMS Inc. HNBD R&D	Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111
Title	DDR3 SO-DIMM_0/SO-DIMM_1
Size: Custom	Document Number: CHICAGO
Rev	MV
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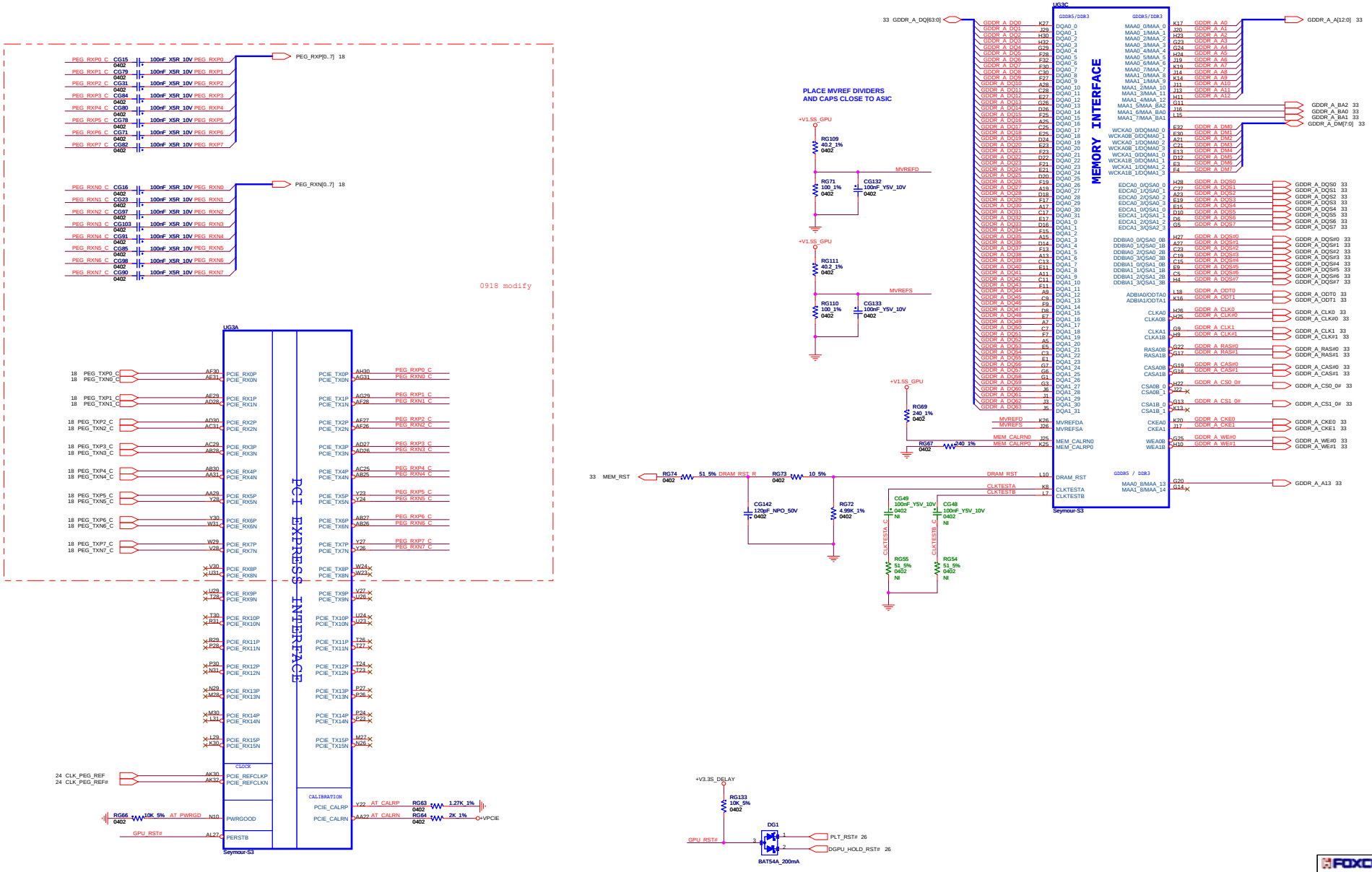
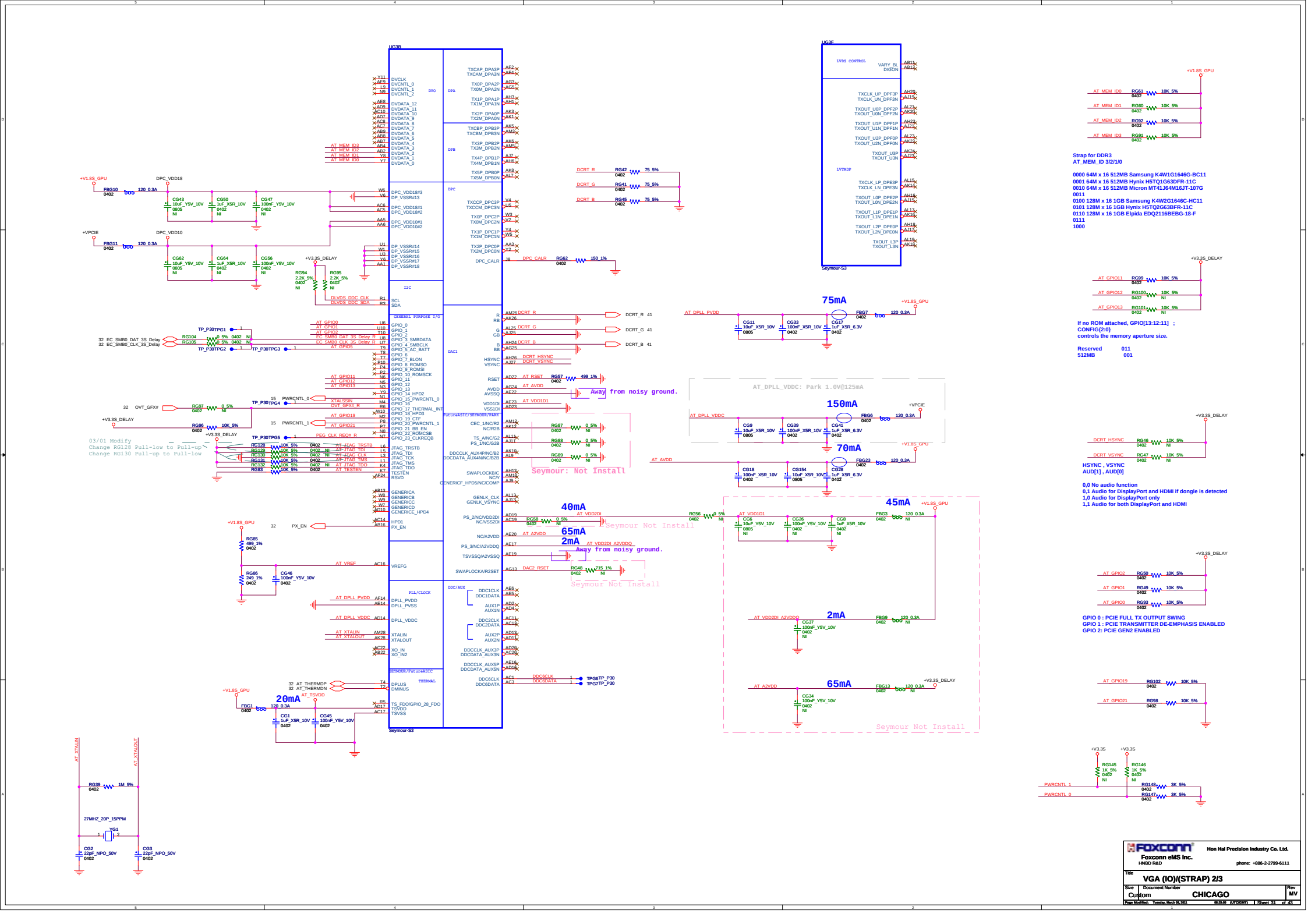


Foxconn eMS Inc. HNBD R&D	Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111		
Title: VGA_S3 (PCI-E) 1/3			
Size: Custom	Document Number: CHICAGO	Rev: MV	
Page Modified: Tuesday, March 08, 2011	08:29:05 (UTC/GMT)	Sheet 30 of 43	


UG3B
Seymour-S3
UG3F
Seymour-S3
Strap for DDR3
AT_MEM_ID 3/2/1/0
0000 64M x 16 512MB Samsung K4W1G1646G-BC11
0001 64M x 16 512MB Hynix H5TQ1G63DFR-11C
0010 64M x 16 512MB Micron MT41J64M16JT-107G
0011
0100 128M x 16 1GB Samsung K4W2G1646C-HC11
0101 128M x 16 1GB Hynix H5TQ2G63BFR-11C
0110 128M x 16 1GB Elpida EDQ2116BEBG-18-F
0111
1000
If no ROM attached, GPIO[13:12:11] ;
CONFIG{2:0}
controls the memory aperture size.
Reserved 011
512MB 001
HSYNC , VSYNC
AUD[1] , AUD[0]
0,0 No audio function
0,1 Audio for DisplayPort and HDMI if dongle is detected
1,0 Audio for DisplayPort only
1,1 Audio for both DisplayPort and HDMI
GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2: PCIE GEN2 ENABLED
75mA
150mA
70mA
45mA
40mA
65mA
2mA
20mA
Away from noisy ground.
Seymour: Not Install
Seymour Not Install
AT_DPLL_VDDC: Park 1.0V@125mA
03/01 Modify
Change RG128 Pull-low to Pull-up
Change RG130 Pull-up to Pull-low
Foxconn
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HNBD R&D
Hon Hai Precision Industry Co. Ltd.
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Title
VGA (IO)/(STRAP) 2/3
Size
Custom
Document Number
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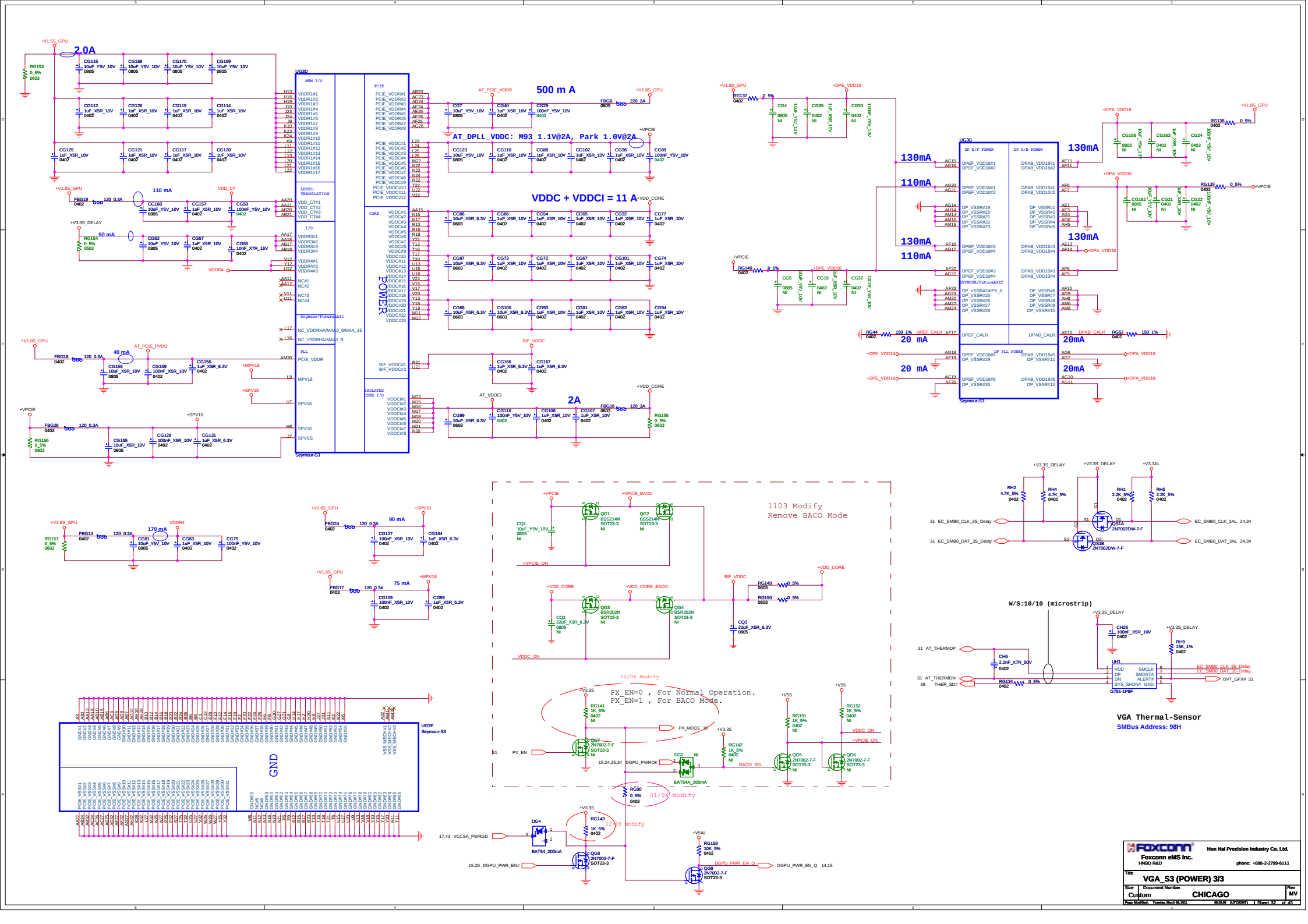

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Title: VGA_S3 (POWER) 3/3

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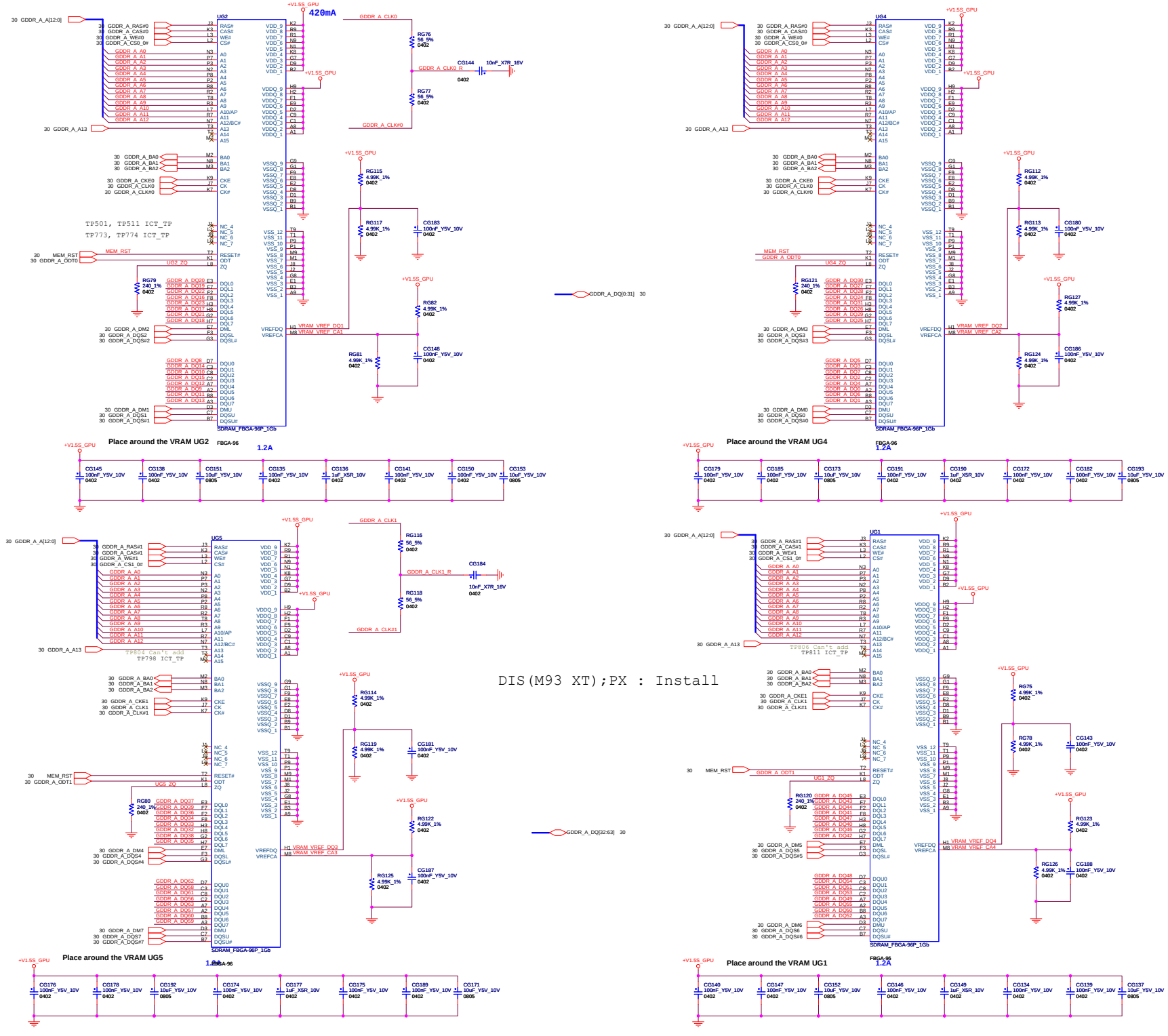
420mA
UG2
UG4
UG5
UG1
SDRAM_FBGA-96P-1Gb
FBGA-96
1.2A
Place around the VRAM UG2
Place around the VRAM UG4
Place around the VRAM UG5
Place around the VRAM UG1
TP501, TP511 ICT_TP
TP773, TP774 ICT_TP
DIS(M93 XT);PX : Install
GDDR_A_DQ[0:31]
GDDR_A_DQ[32:63]
Foxconn
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VRAM (DDR3)
CHICAGO
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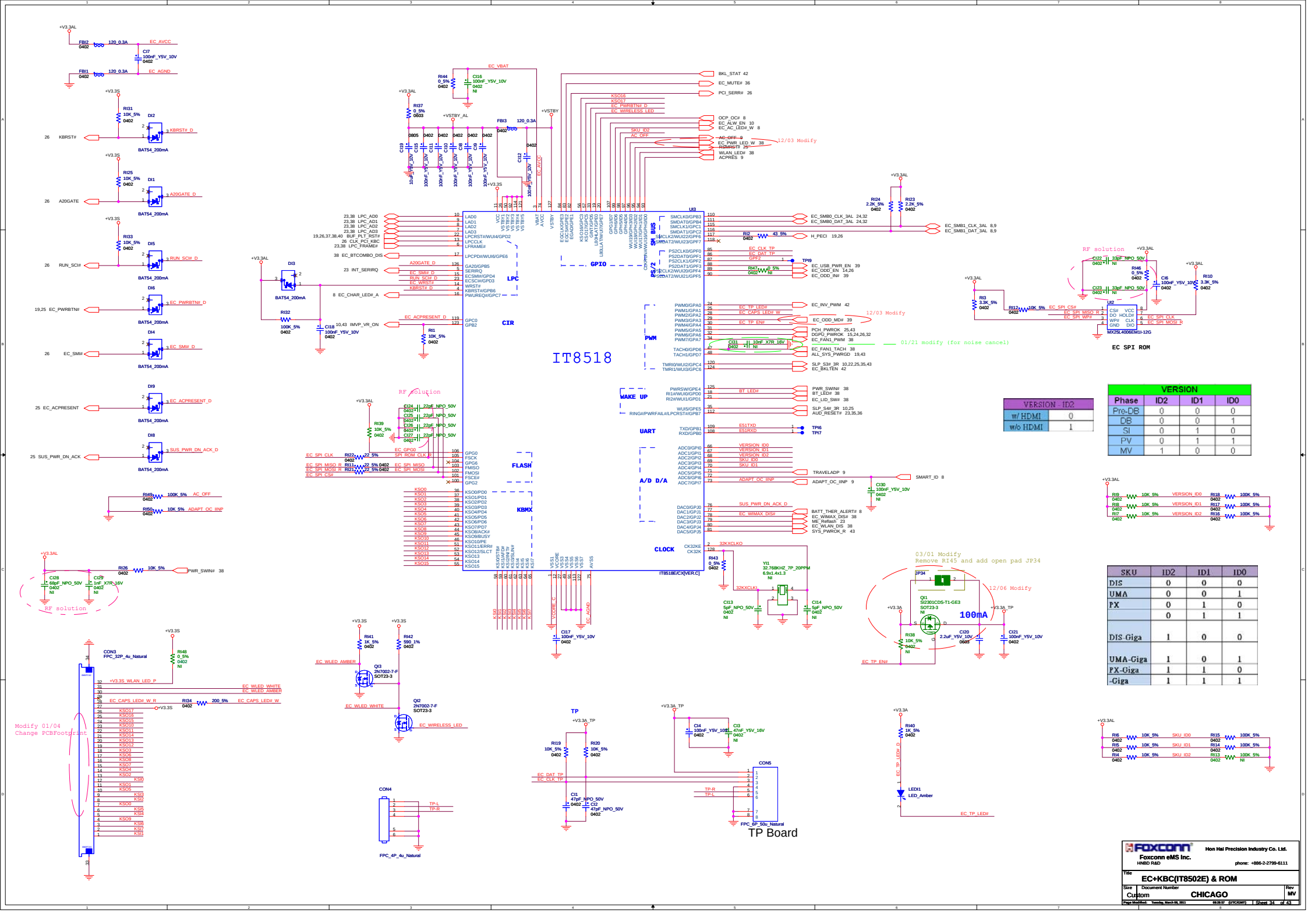

VERSION - ID2	
w/ HDMI	0
w/o HDMI	1

VERSION			
Phase	ID2	ID1	ID0
Pre-DB	0	0	0
DB	0	0	1
SI	0	1	0
PV	0	1	1
MV	1	0	0

SKU	ID2	ID1	ID0
DIS	0	0	0
UMA	0	0	1
PX	0	1	0
	0	1	1
DIS-Giga	1	0	0
UMA-Giga	1	0	1
PX-Giga	1	1	0
-Giga	1	1	1

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Title: EC+KBC(IT8502E) & ROM

Size: Custom | Document Number: CHICAGO | Rev: MV

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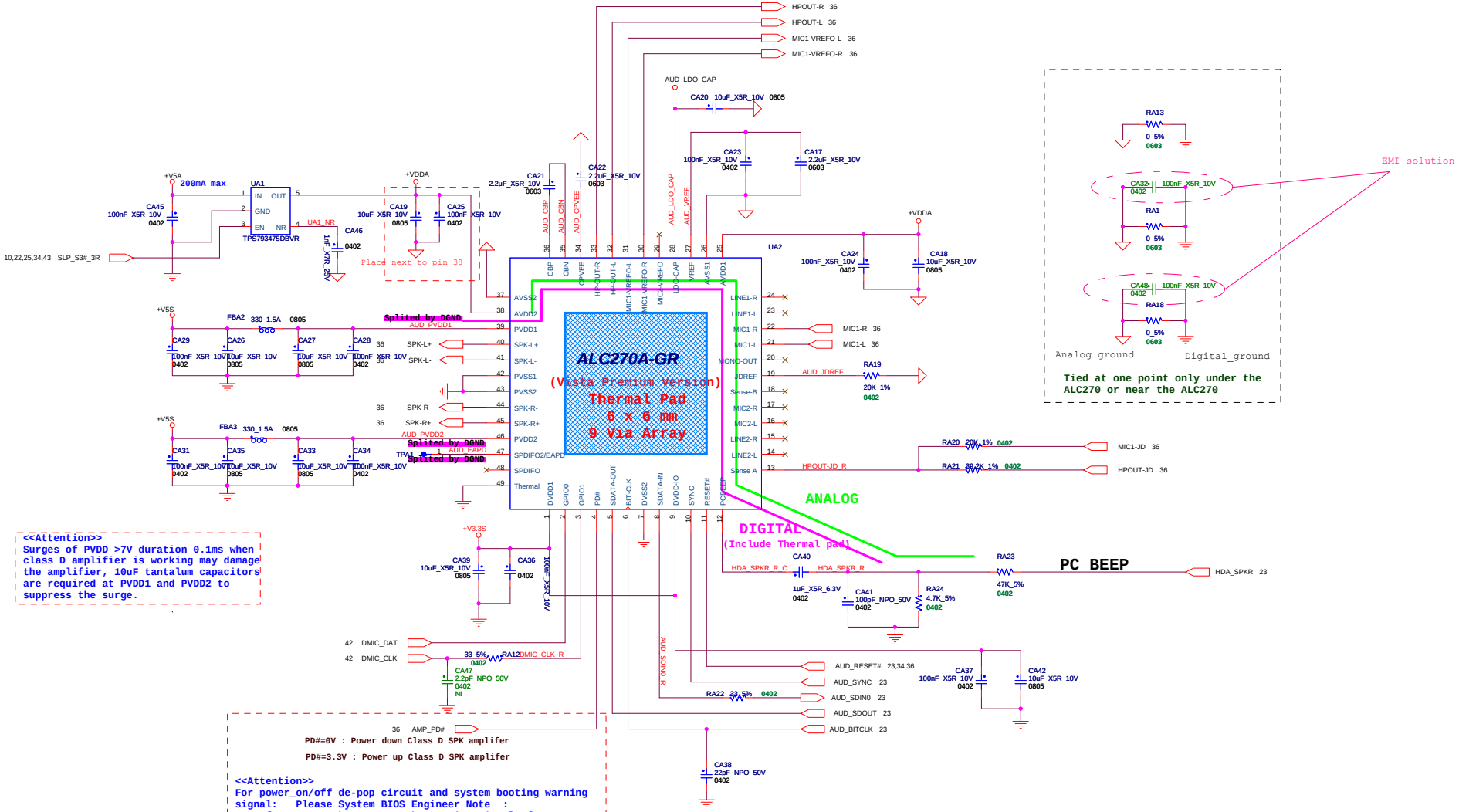
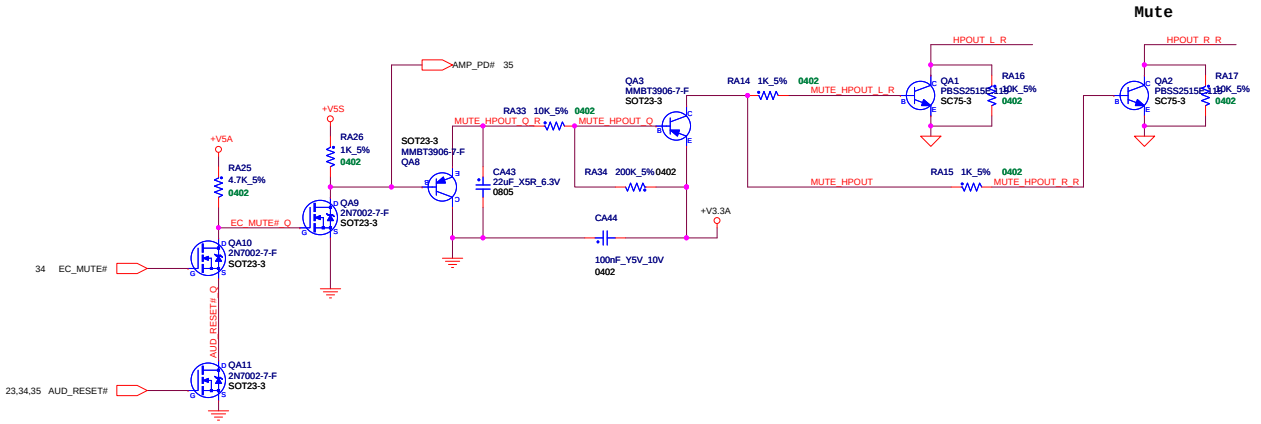
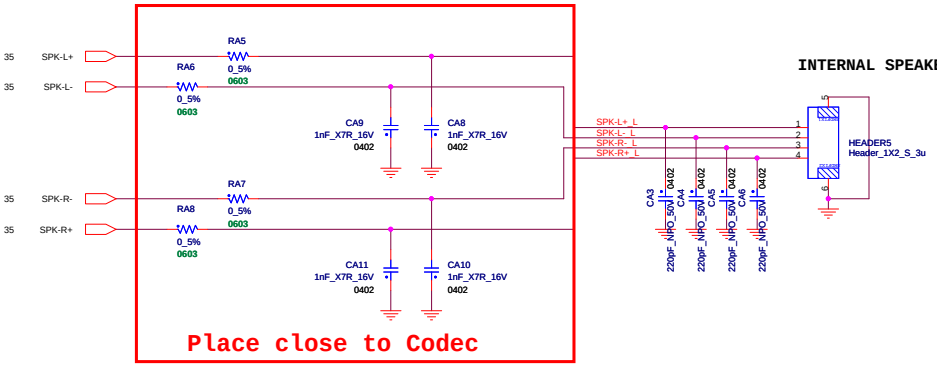
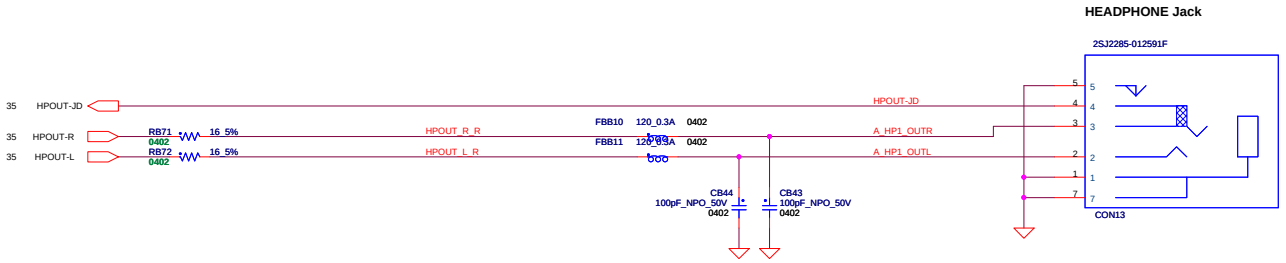
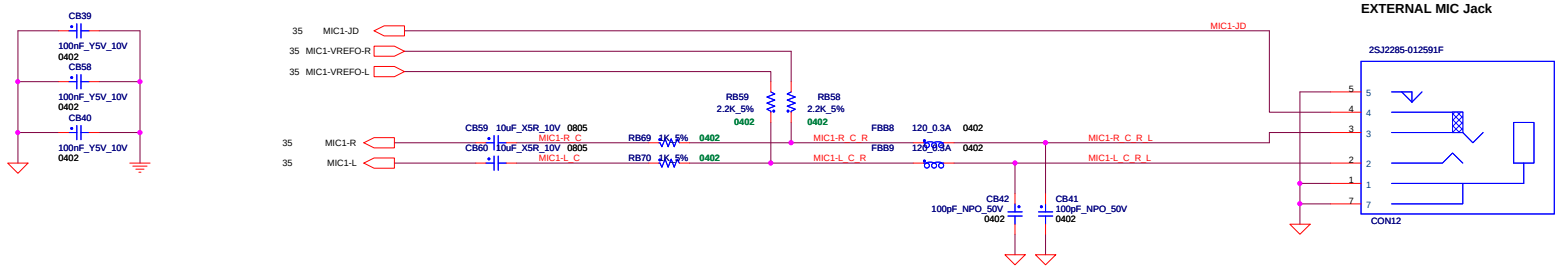


Foxconn eMS Inc. HNBD R&D	Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111	
Title: Audio (CODEC_ALC270A)		
Size: Custom	Document Number	Rev
Page Modified: Tuesday, March 08, 2011 08:28:58 (UTC/GMT)	Sheet 35 of 43	









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Hon Hai Precision Industry Co. Ltd.
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Title: Audio (JACK+AMP+SPK+Mute)

Size: Custom | Document Number: CHICAGO | Rev: MV

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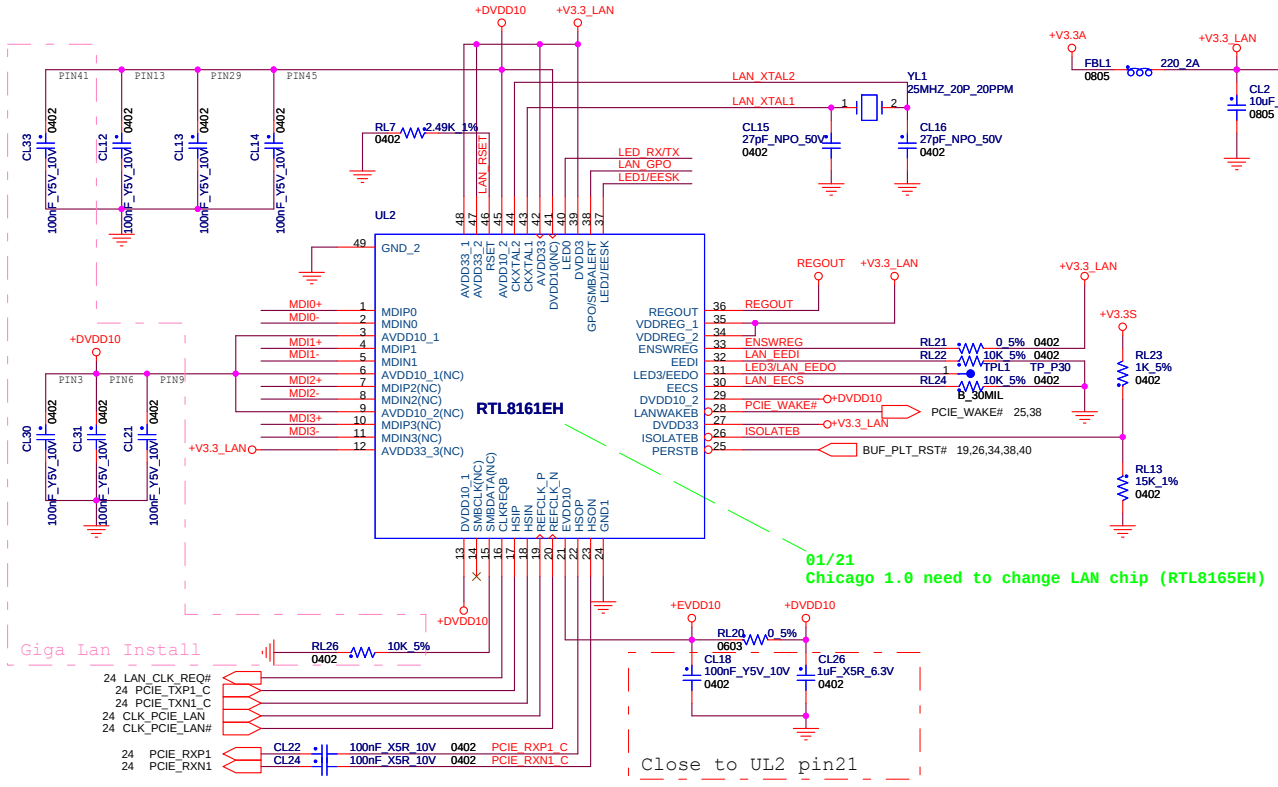
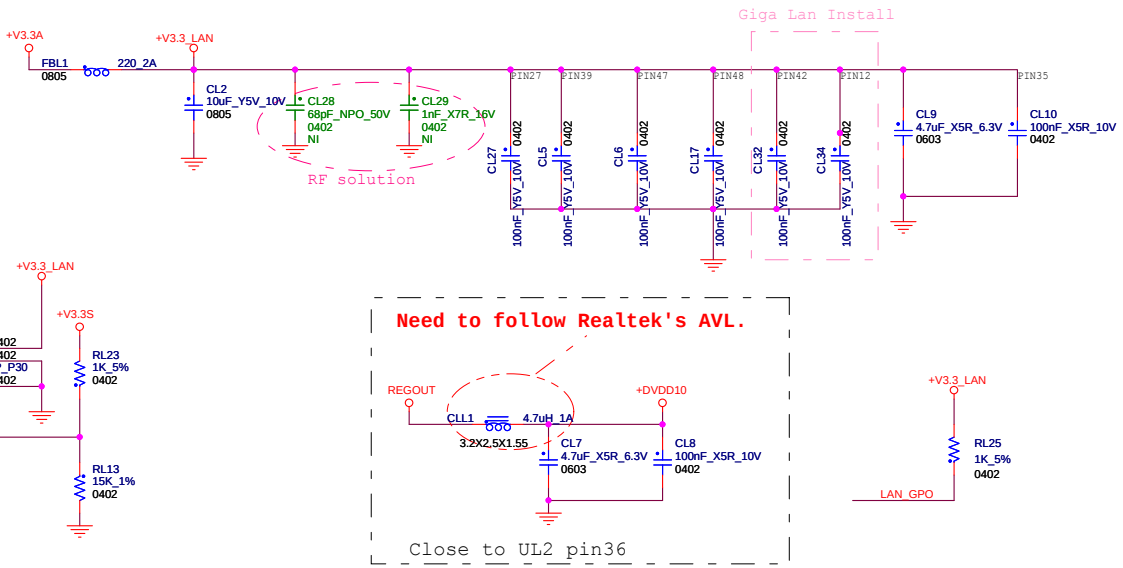
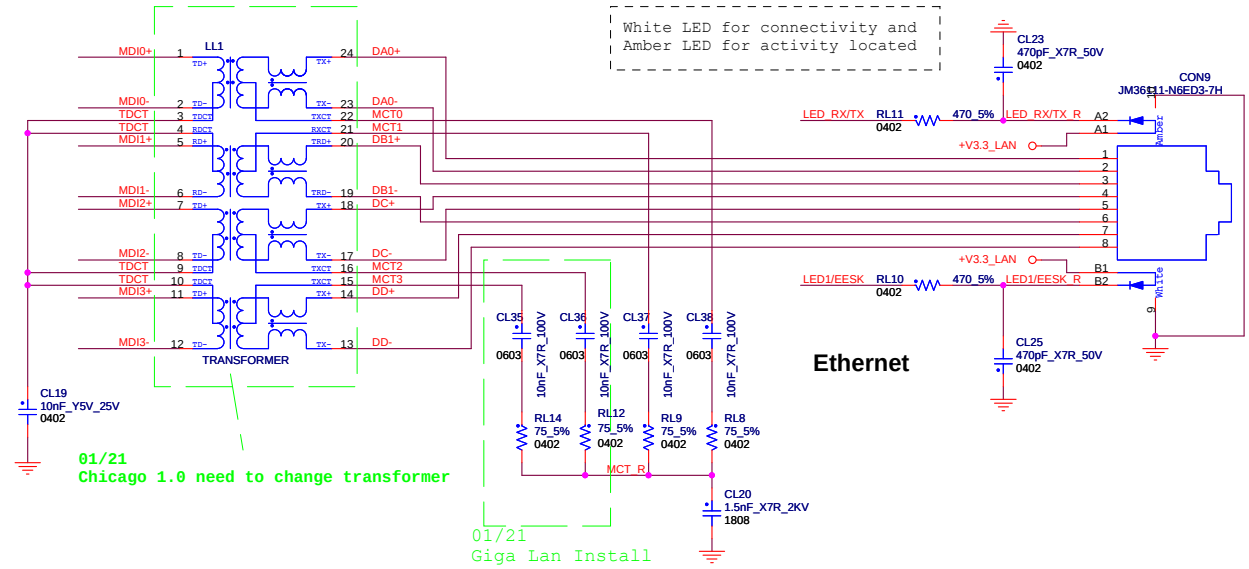


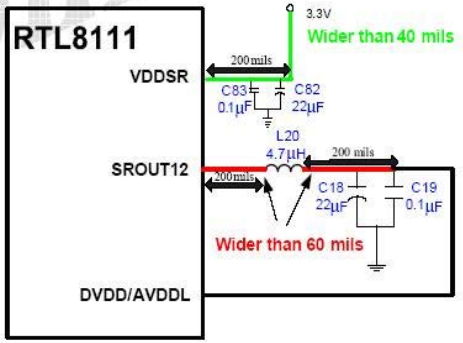




7.1. PCB Layout

- The input 3.3V power trace connected to the VDDSR pin should be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200mils (0.5cm) of the VDDSR pin to prevent input voltage overshoot.
- The output power trace out of the SROUT12 pin should be wider than 60mils.
- Keep L20 within 200mils (0.5cm) of the SROUT12 pin.
- Keep C18 and C19 within 200mils (0.5cm) of L20 to ensure stable output power and better power efficiency.
- Both C18 and C82 are strongly recommended to be ceramic capacitors.

Note: Violation of the above rules will damage the IC.



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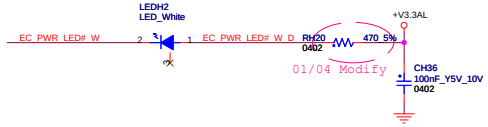
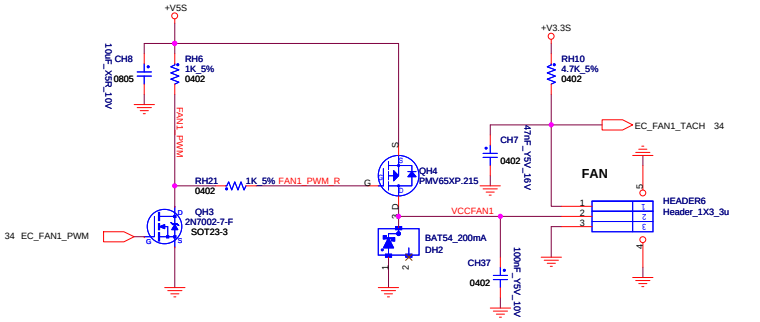
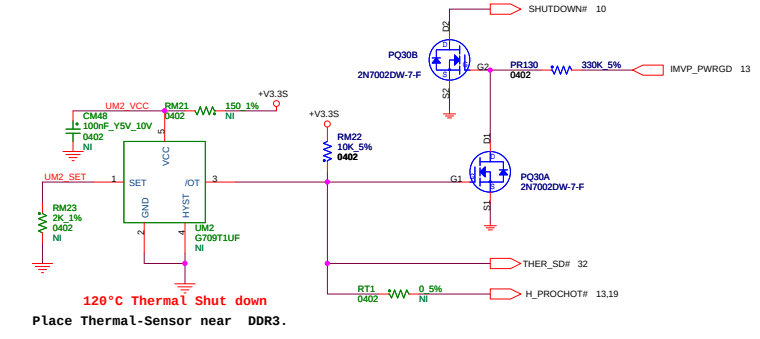
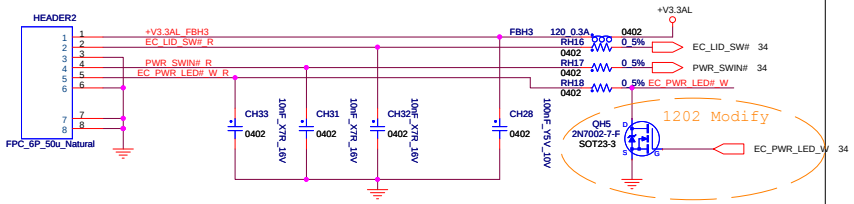
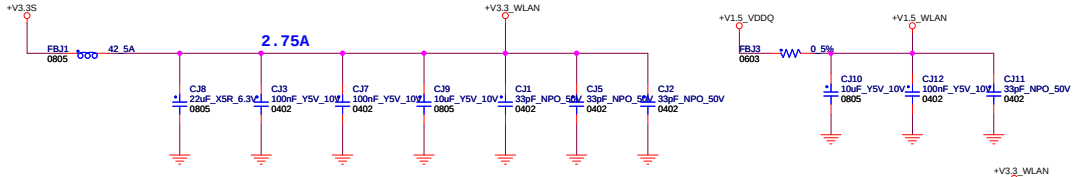


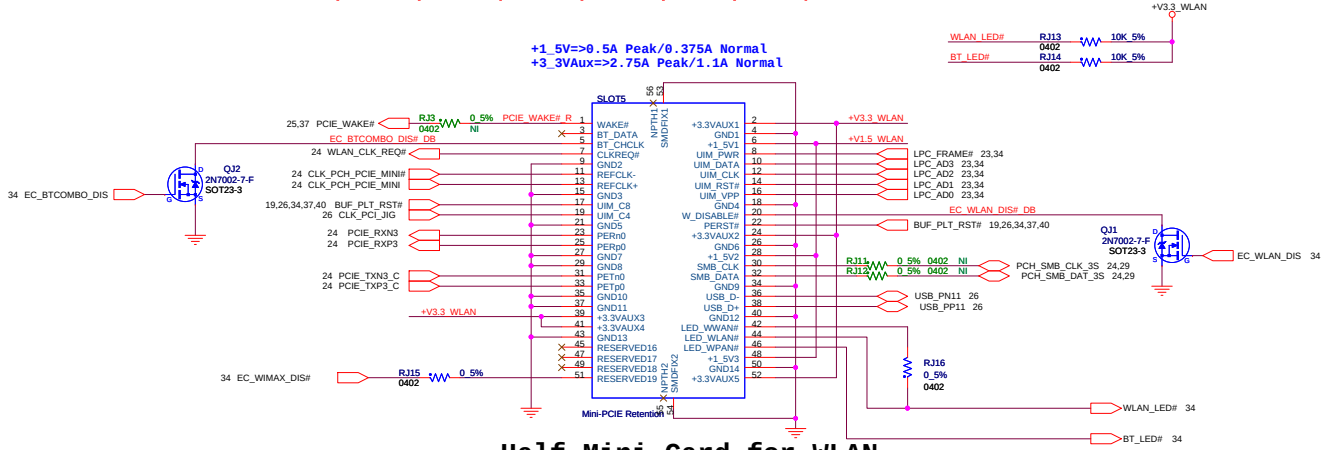




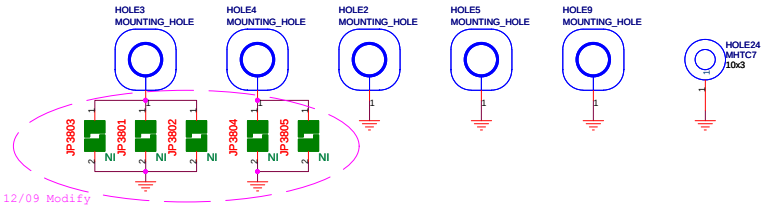
PWR Board CONN.

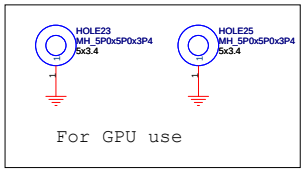


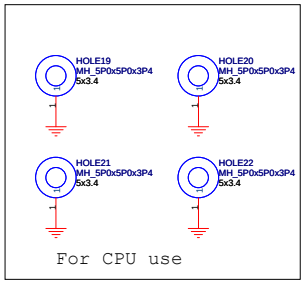




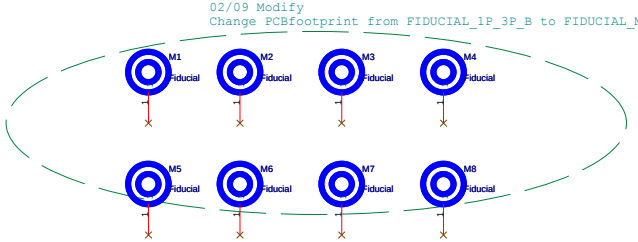
Half Mini Card for WLAN







Mounting HOLE



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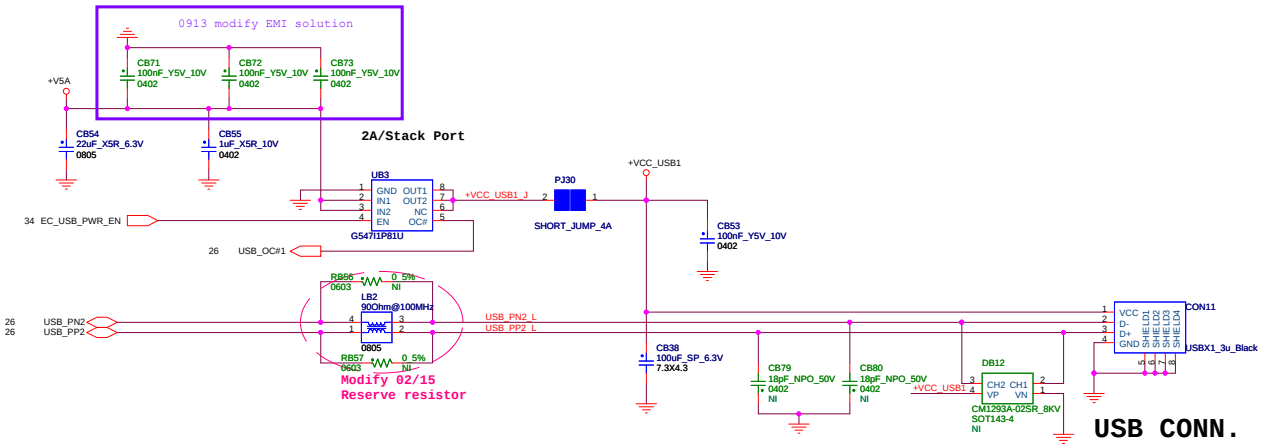
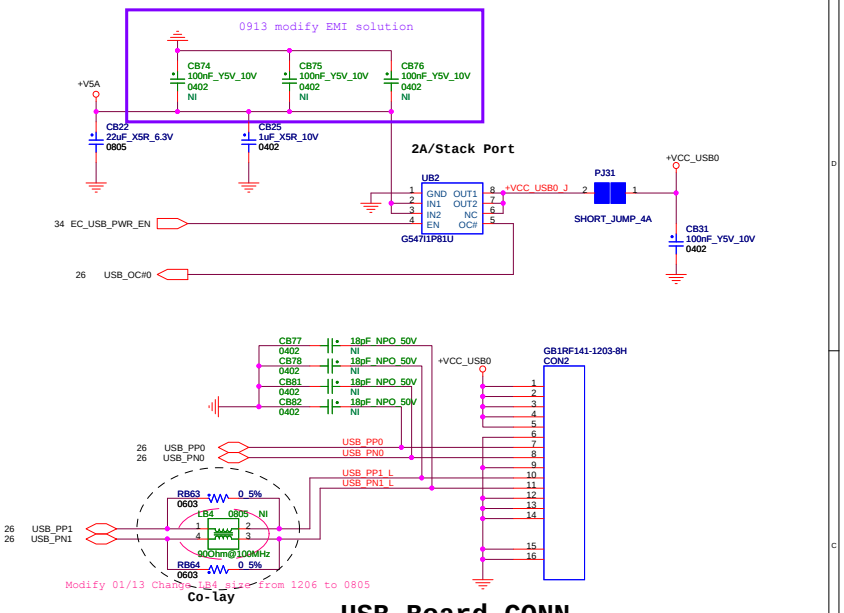
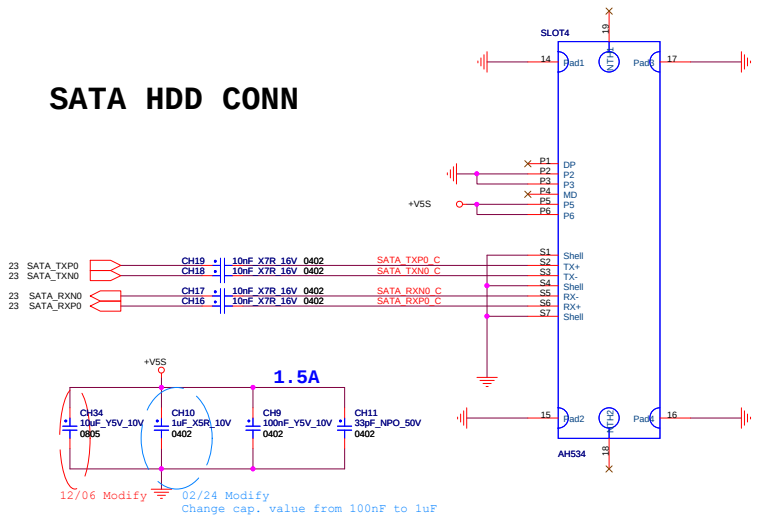


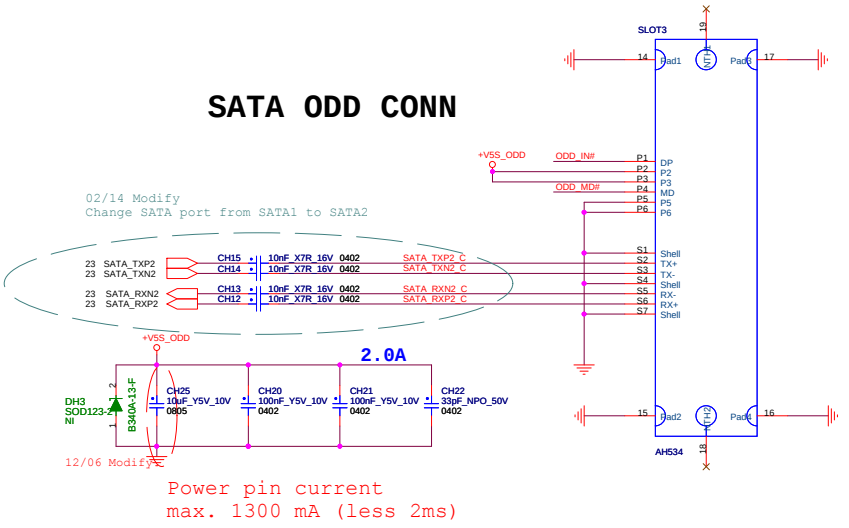


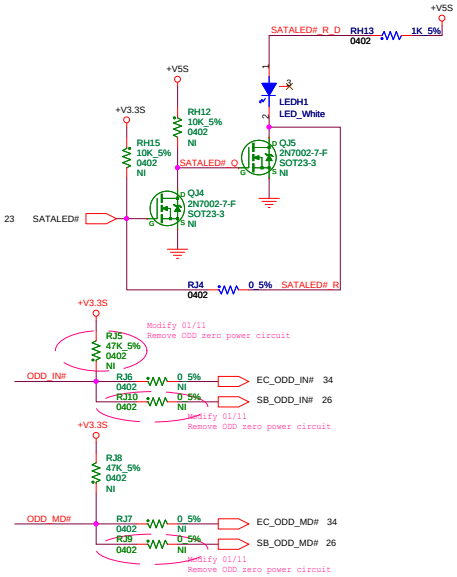
HDD/ODD Status LED

SATA HDD CONN



SATA ODD CONN





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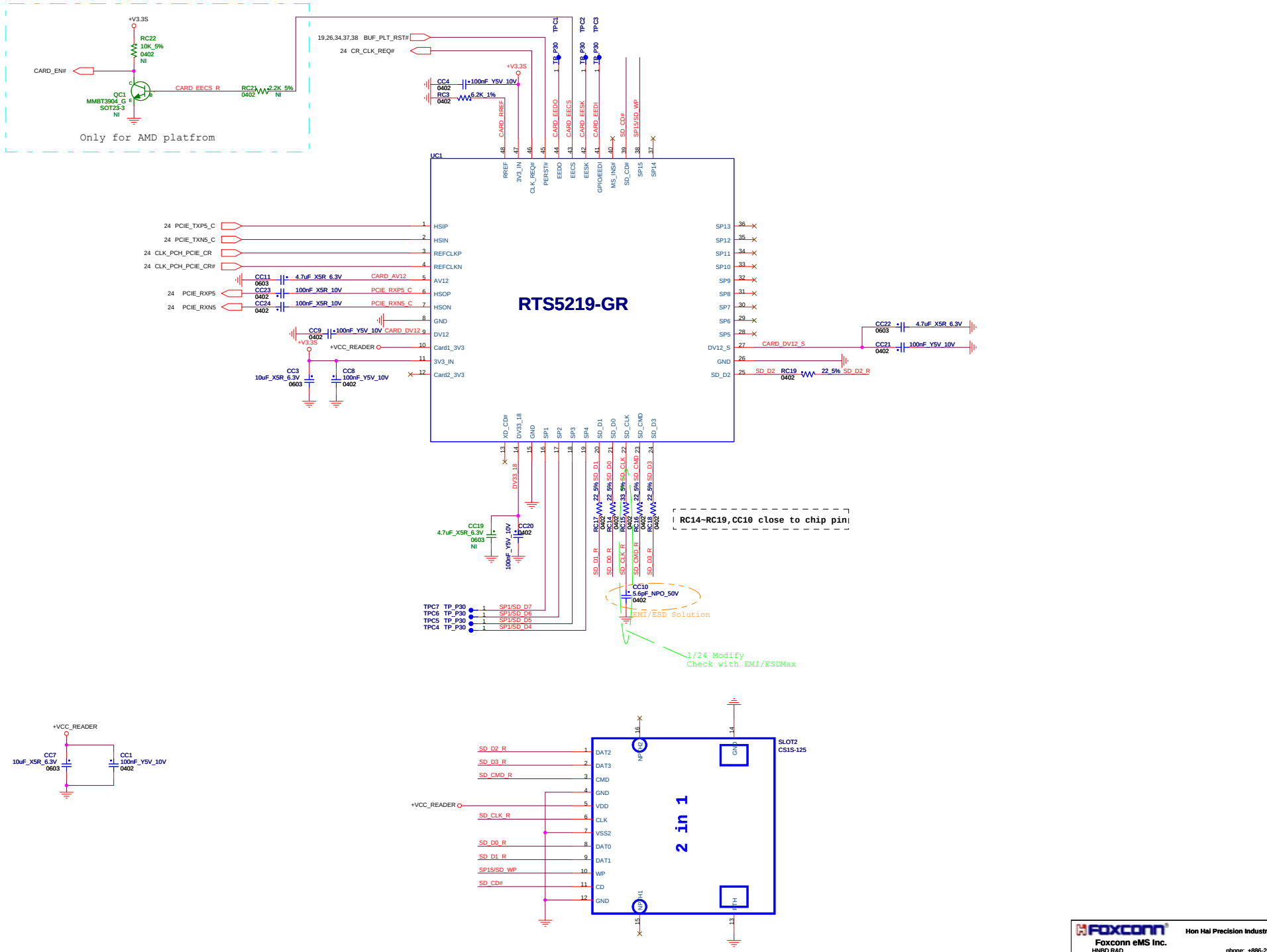
Only for AMD platfrom
RTS5219-GR
UC1
RC14~RC19,CC10 close to chip pin
EMI/ESD Solution
1/24 Modify
Check with EMI/ESDMax
2 in 1
SLOT2
CS1S-125
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Card Reader
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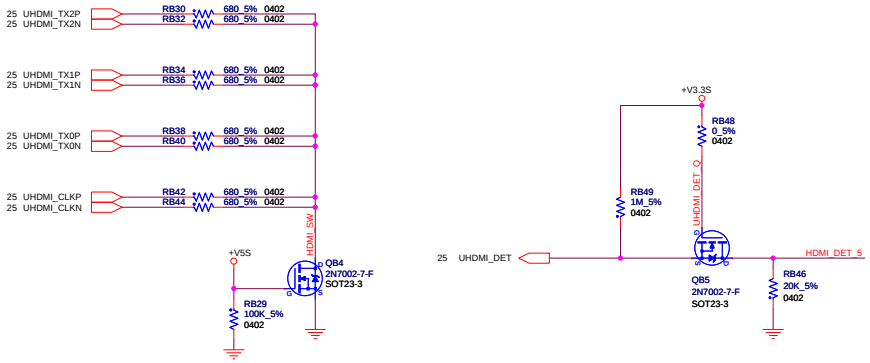
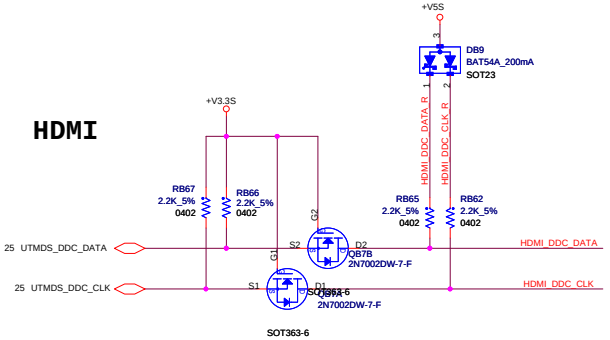
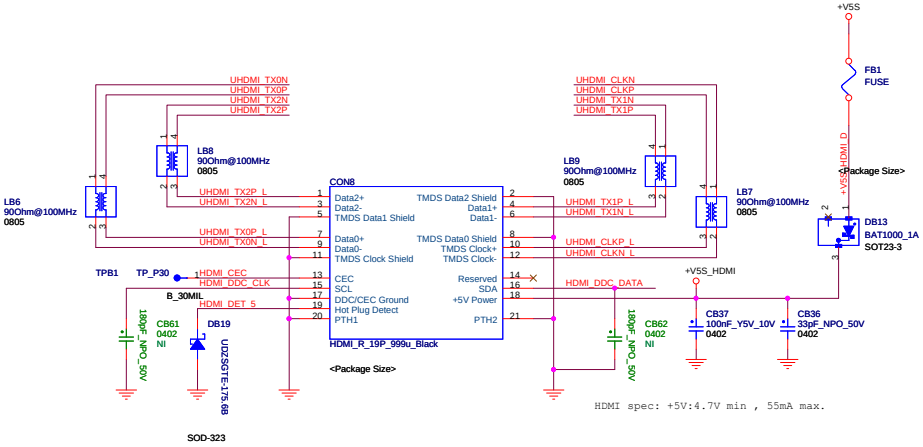


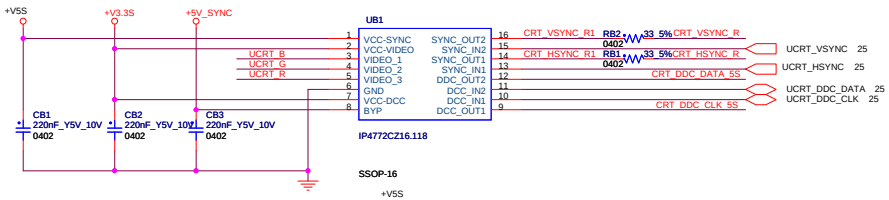
HDMI

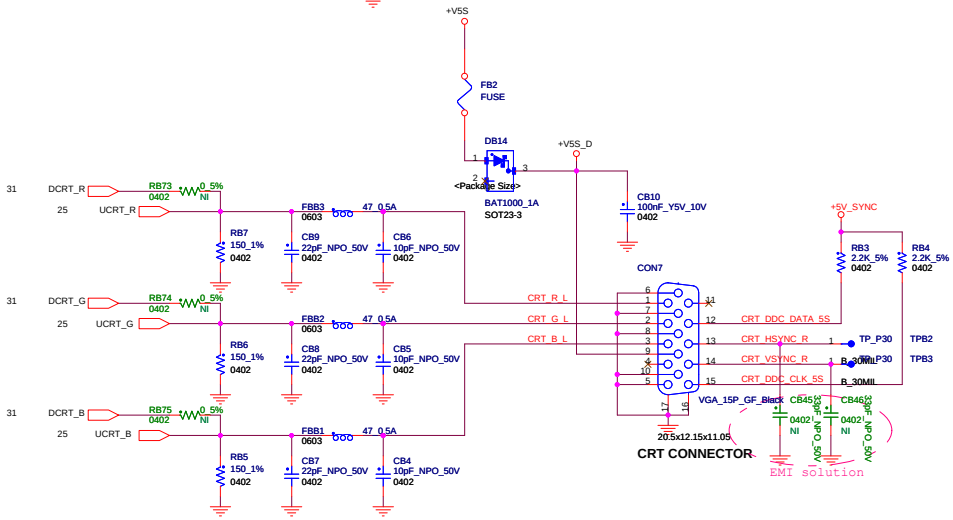




HDMI spec: +5V:4.7V min , 55mA max.

CRT





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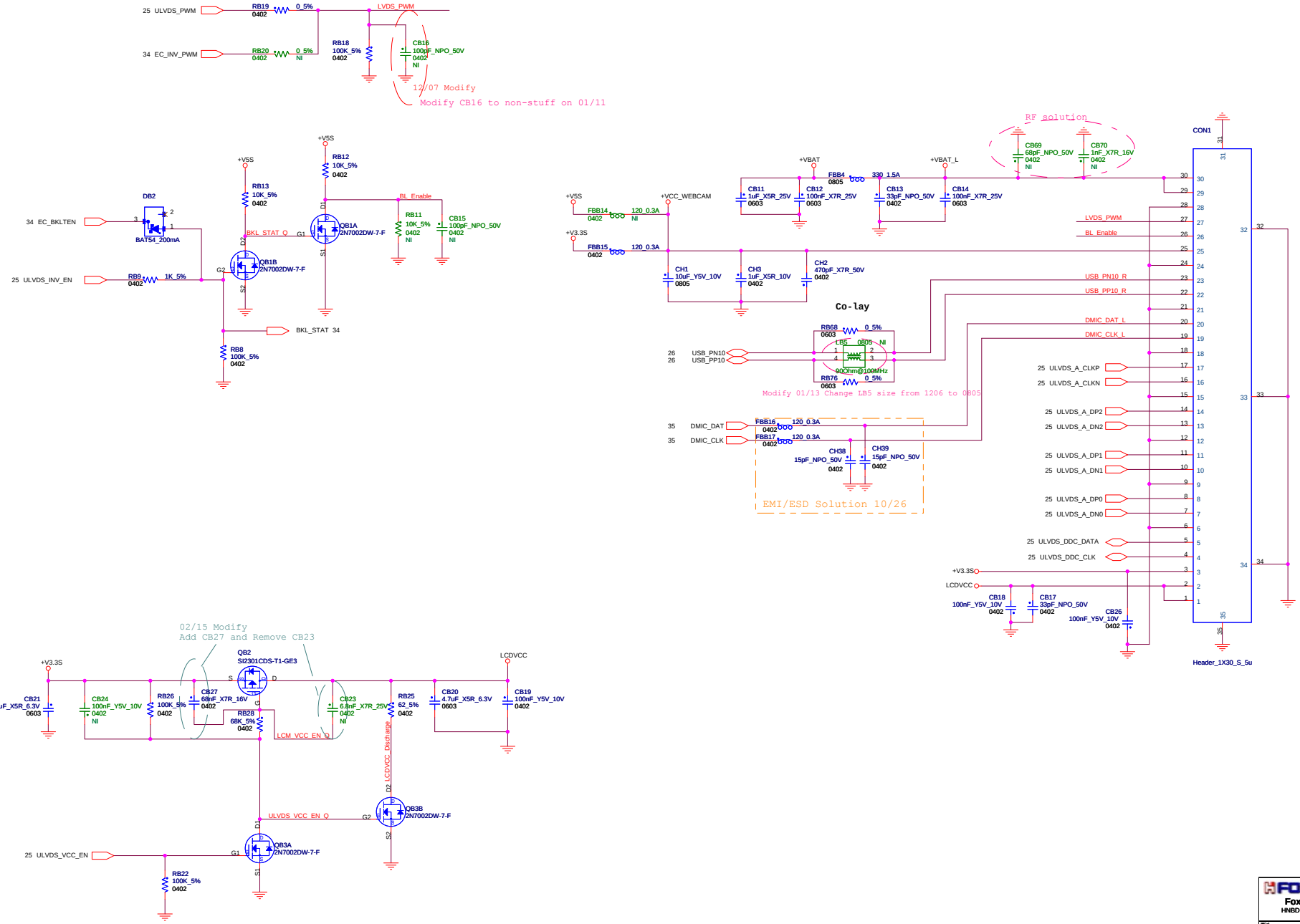

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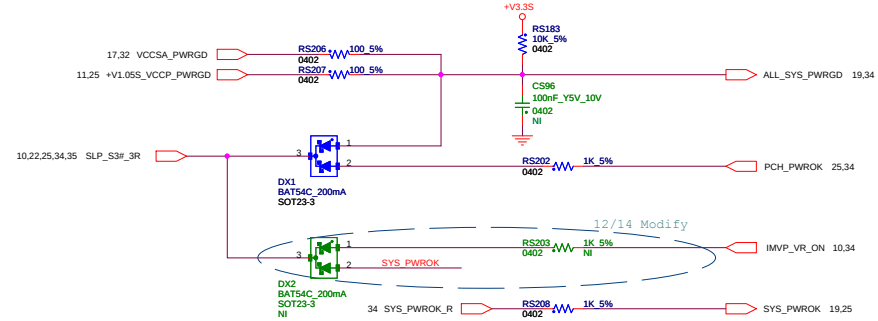

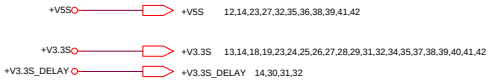

12/07 Modify

1117 Modify

Modify 11/11

C19 100nF_Y5V_10V 0402 NI
C20 100nF_Y5V_10V 0402 NI
CB56 22uF_X5R_6.3V 0805
C60 100nF_Y5V_10V 0402 I
C27 100nF_Y5V_10V 0402 NI
C28 100nF_Y5V_10V 0402 NI
CB57 22uF_X5R_6.3V 0805
C61 100nF_Y5V_10V 0402 I
C33 100nF_Y5V_10V 0402 NI
C34 100nF_Y5V_10V 0402 NI
C26 100nF_Y5V_10V 0402 NI
C62 100nF_Y5V_10V 0402 I
C35 100nF_Y5V_10V 0402 NI
C36 100nF_Y5V_10V 0402 NI
C37 100nF_Y5V_10V 0402 NI
C63 100nF_Y5V_10V 0402 I
C38 100nF_Y5V_10V 0402 NI
C39 100nF_Y5V_10V 0402 NI
C42 100nF_Y5V_10V 0402 NI
C43 100nF_Y5V_10V 0402 NI
C44 100nF_Y5V_10V 0402 NI
C45 100nF_Y5V_10V 0402 NI

C1 C4 C8 C13 C17 C21 C31
C2 C5 C9 C14 C18 C22 C32
C3 C10 C15 C46 C23
C40 C6 C11 C16 C47 C24 C29
C41 C7 C12 C58 C59 C25 C30

EMI/ESD Solution 10/26

C48 C49 C50 C51 C52 C53 C54 C55 C56 C57
100nF_X5R_25V 0402
100nF_Y5V_10V 0402

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